Electronics Research Laboratory
University of California
Berkeley, California
Internal Technical Memorandum M-100

CERTAIN SEMICONDUCTOR APPLICATIONS OF THE SCANNING ELECTRON MICROSCOPE

by

T. E. Everhart

This work was supported by the Electronics Technology Division, Air Force Avionics Laboratory, Research and Technology Division, United States Air Force, Wright-Patterson Air Force Base, Ohio, under Contract No. AF 33(615)-1045; by Joint Services Electronics Programs U. S. Army, U. S. Navy, and U. S. Air Force) under Grant No. AF-AFOSR-139-64; and by the University of California, Berkeley.

October 22, 1964

CERTAIN SEMICONDUCTOR APPLICATIONS OF THE SCANNING ELECTRON MICROSCOPE

T. E. Everhart
Department of Electrical Engineering
University of California
Berkeley, California

ABSTRACT

Semiconductor device evaluation in the scanning electron microscope is reviewed briefly. A scanning electron microscope recently designed for both the qualitative evaluation of semiconductor devices, and the quantitative measurement of certain material or device parameters, is described. Micrographs illustrating the present capabilities of this instrument are shown. New results include the observation of depletion-layer broadening with increasing reverse bias, and the observation of n-type inversion layers on passivated high-resistivity p-type silicon surfaces.

This work was supported by the Electronics Technology Division, Air Force Avionics Laboratory, Research and Technology Division, United States Air Force, Wright-Patterson Air Force Base, Ohio, under Contract No. AF 33(615)-1045; by Joint Services Electronics Programs (U.S. Army, U.S. Navy, and U.S. Air Force) under Grant No. AF-AFOSR-139-64; and by the University of California, Berkeley.

INTRODUCTION

The scanning electron microscope can image potential differences between adjacent areas of a specimen surface as brightness differences between the corresponding areas of the scanning electron micrograph. This very useful ability has recently been utilized for the evaluation of passivated integrated circuits.[1] Energetic electrons penetrating into semiconductors or insulators excite valence electrons to the conduction band, enhancing the electrical conductivity of the material. In silicon, a hole-electron pair is produced for approximately every 4 to 5 ev of primary electron energy;[2, 3] substantial current multiplication is thus possible with primary energies of 10 to 30 kev. When these carriers are generated in a region of high electric field, such as exists in the depletion layer of a semiconductor p-n junction, an electron-beam-induced (EBI) current results. This current can be used as the video signal for a scanning electron microscope display, to give information concerning the uniformity and magnitude of junction depth beneath the device surface.[3] The selective recombination of these carriers can produce useful information about crystal imperfections; this recombination can be observed as a reduction in the EBI current,[4] or in some cases at least, as a source of infra-red radiation.[5]

The scanning electron microscope is also useful for high-resolution resist exposure.[6, 7, 8] This application shows considerable promise. As the author's work is not at present in this important area, this paper will concentrate on the device evaluation and device measurement applications of the instrument.

Scanning electron microscope evaluation of semiconductor devices is nondestructive in that no Frenkel defects are formed by the low energy beam (typically, beam energies range from 5 to 40 kev). However, beta degradation on high-gain transistors has sometimes been observed; the beta can be restored to its original value by proper heat-treatment of the transistor.[9]

A scanning electron microscope has been constructed in the Electronics Research Laboratory, University of California, Berkeley, during the past year, to extend the integrated circuit evaluation work previously reported, to improve high-resolution semiconductor device measurements, and to improve our understanding of electron-beam interactions with solid materials. The instrument will first be described briefly, and then preliminary results obtained with it will be shown.

INSTRUMENT DESCRIPTION

The Berkeley Scanning Electron Microscope employs a conventional electron microscope gun followed by two magnetic electron lenses. The filament can be positioned in x, y, and z with respect to the grid, and the anode can be positioned in x and y while the instrument is in operation. Provision is made for an anode aperture to define the electron source. Aluminized ruled uranium glass screens are provided below the gun and below the first lens to aid in instrumental alignment. These screens may be used as mirror to inspect the column to align the filament optically in the grid, and as flourescent screens to observe the beam shape. They swing out of the beam when not in use. Two commercial available deflection coils are located between the first and second lens. Both coils are outside the vacuum and can be rotated about the beam axis. The first coil deflects the beam away from the axis, and the second deflects it back toward the axis such that it crosses the axis at the final lens aperture. The first lens is conventional; the second employs a pin-hole pole-piece. Both have apertures which can be adjusted while the instrument is in operation. The power supply voltage is variable from 3 to 30 kv; this voltage and the lens currents are stable to 50 ppm.

The specimen x-y motion of one inch by one inch is controlled by rotating two 40 tpi precision lead screws. The secondary electron collection system employs a plastic scintillator and photomultiplier tube in the configuration described by Everhart and Thornley.[10]

The scan waveforms are derived from completely transistorized digital and analog circuits. A 32 kc clock frequency is divided by binary stages, and all sweep waveforms are locked to the clock. Line sweep rates of 1 ms/line, 4, 16, 64, 256, and 512 ms/line are available, and frames consisting of 256, 512, or 1024 lines may be chosen. The frame sweep may also be stopped, so that a single line may be repetitively swept over any spot on the specimen. This mode of operation is particularly useful when recording signals generated within the specimen by the electron beam. While the line-sweep-waveform is a sawtooth, the frame-sweep-waveform is a stairstep. Partial scan of the raster is also available, giving a higher signal-to-noise ratio in the observed image, which is particularly convenient for focussing.

The sweep may be turned off, and the beam electrically steered to any point in the raster. The beam may be switched off at the specimen by deflecting it off an aperture before the first lens using electrostatic deflection plates. The rise and fall time of the pulse at the specimen is less than one microsecond. Thus any point on the specimen may be pulsed with the electron beam, and the time-response of the Electron-Beam-Induced current (EBI current) measured at that spot. Mr. S. R. Pedersen deserves credit for the design and construction of the custom-built electronic circuits used in this instrument.

The vacuum system employs 15 cubic feet/minute forepump, a 400 liter/second oil-diffusion pump, and a custom-built liquid nitrogen trap which holds an 18 hour supply. Separate high-vacuum valves for the column and specimen chamber enable the specimen to be changed while the main electron column is held at high vacuum. Dry gaseous nitrogen is used to backfill the column and specimen chamber. A pressure of a few times 10^{-5} Torr is achieved after two minutes pump-down from atmospheric pressure, and a pressure of a few times 10^{-6} Torr is achieved within 15 to 30 minutes. Viton O-rings are used throughout.

INITIAL RESULTS

Resolutions of from 0.1 to 0.2 μ have been obtained at beam currents of from 0.1 to 0.5 nanoamps, and beam voltages of 15 to 20 kv. Resolution is presently limited by the electron optics of the final lens, and vibration sometimes is also troublesome. The microscope is presently being used to examine semiconductor specimens as it stands. A small area of the surface of a commercial-field-effect transistor (FET) is shown in Fig. 1. The edge of a thermocompression bond is shown in the top right-hand corner of the micrograph, where it is connected to the evaporated aluminum lead. During the bonding process, gold seems to have migrated several microns down the aluminum lead (see vertical arrow), for this area of the lead has a much higher secondary emission coefficient than the adjacent aluminum, suggesting that it is either gold, or aluminum-gold alloy. The aluminum lead below this point seems rough and buckled; measurements of the EBI current verify that the aluminum is either thinner, or entirely missing at the circular spot toward the bottom of the micrograph (see horizontal arrow). This micrograph suggests that the heat-pressure cycle for this thermal-compression bond was not optimum.

One of the first working devices made in our integrated circuits laboratory was a uni-junction transistor (UJT) oscillator, designed and fabricated by G. Hachtel over one year ago. This device was one of the first examined in our scanning electron microscope for sentimental reasons, and Fig. 2 shows part of the metal-oxide-semiconductor capacitor of this integrated UJT oscillator, with and without applied bias. Note that the potential of the silicon shows clearly through the passivating oxide layer around the periphery of the capacitor, and also through the holes in the aluminum top electrode. These holes resulted from faulty resist protection of the aluminum during one of the processing steps; fortunately, these holes do not degrade the device performance. (I am pleased to report that our graduate students rapidly overcame this sort of processing fault.)

On this same device, irregular black dots, approximately 1 μ across, were observed on the evaporated aluminum interconnections. They are believed to be micro-holes in the aluminum, and sometimes follow scratch marks on the surface, as in the micrograph shown in Fig. 3. The white objects observed in this micrograph are believed to be small bits of photoresist which were not completely removed from the surface.

A schematic diagram of another semiconductor specimen is shown in Fig. 4. This metal-oxide-semiconductor field-effect transistor (MOS FET), which was made in our laboratory by N. MacDonald, was angle-lapped and polished at an angle of approximately thirty degrees to the device surface. The source electrode was grounded to the high-resistivity p-type substrate, and potentials were applied to the gate and drain electrodes. Typical micrographs of this device are shown in Fig. 5; the top region of each micrograph is the lapped region, and the regions on the lower half of the micrograph, from left to right are (a) passivated high-resistivity p-type surface, (b) drain region, (c) gate region, and (d) source region. In these micrographs, the darker the image, the greater the EBI current flowing at that point on the micrograph. There are several interesting features of these micrographs. First, note that the passivated, high-resistivity p-type material in region (a) is dark. This implies that a field exists in this region which separates the holes and electrons produced by the primary beam, and thus produces an EBI current in this region. This field is believed to exist across a depletion region between the n-type inversion layer which generally exists at the surface of a passivated, high-resistivity p-type region, and the substrate. Subsequent micrograph will support this interpretation. Micrographs 5(a) and (b) are produced by an EBI current video signal only, while micrograph 5 (c) has the secondary electron video signal mixed in as well, to give information about the surface topography such as the gate electrode position (slightly misaligned).

Note the large "streamer" at the top left of these micrographs. With a 10 v reverse-bias between drain and substrate, the "streamer's" width is substantial, implying that the depletion region is much larger around it, and that it is n-type material, at least at the surface. Decreasing the reverse bias, as shown in 5 (b), greatly decreases the "streamer's" width, and also reduces the distance the EBI current signal extends into the substrate region. Rough measurements on micrographs such as these indicate that the EBI current signal is significant for 13 to 14 μ along the lapped surface when the reverse bias is 9.9 v, and is significant for about 9 μ when the reverse bias is 1.4 v. To gain additional information about these junctions, higher magnification micrographs using only the secondary electron video signal were taken. Two typical micrographs are shown in Fig. 6. The darkened area extends approximately 10 μ along the lapped surface when the reverse bias is 10 v, and approximately 8 μ along the lapped surface when the reverse bias is 3 v. This latter value of 8 μ corresponds to the estimated junction position in the absence of surface states. Another interesting feature of Fig. 6 is the thin dark region observed at the edge of the lapped surface with 10 v reverse bias. This is believed to be an n-type inversion layer, which takes on the positive potential of the drain. Its width is approximately 2 μ.

Because of the geometry, and the unknown value of the surface states on the lapped surface, calculated values of depletion layer distance from the edge of the lapped region have not been completed. However, using either an EBI current display, or a secondary electron display, the boundary of the junction has been observed to move with applied bias, and the inversion layer has also become more prominent. We intend to study this motion in more detail, in order to learn more about these devices, and also to learn more about the relationship between the voltage-contrast display using secondary electrons from the specimen, and the EBI current display, where the video signal is generated within

the specimen itself. It should be mentioned that inversion layers have also been observed in scanning microscope investigation of high-field triodes carried out at Westinghouse Research Laboratories.

Figure 7 shows an enlarged view of the active region of the MOS FET. When V_{GS} = -3 v, the darkened region which corresponds to the n region exists along the edge of the lapped region beneath the gate. When V_{GS} = -6 v, the darkened region ends abruptly beneath the gate. This latter value of gate-source voltage is sufficient to reduce the device current to zero in the absence of the electron beam. Figure 8 shows a similar pair of micrographs, with V_{SD} = 10 v. While no source-drain current flows in the device with V_{GS} = -4.5 v, a small saturated current flows when V_{GS} = -3 v. With the larger field between gate and drain, the darkened region beneath the gate extends a much shorter distance into the lapped surface region. A more detailed explanation of these micrographs will be the subject of a future paper.

CONCLUSIONS

A scanning electron microscope designed primarily for semiconductor device measurements has been constructed, and is currently in operation. This instrument is being used by students and faculty to evaluate integrated circuits fabricated in our laboratory, and to investigate high-resolution device measurements. It is expected to provide new information about semiconductor devices themselves, as well as about the interaction of electrons with matter.

ACKNOWLEDGMENTS

The author gratefully acknowledges helpful discussions concerning scanning electron microscope design with Drs. O. C. Wells and R. F. M. Thornley; mechanical design and assembly assistance from G. Becker, drafting assistance from J. Meade, and accurate parts fabrication by J. Tombaugh and L. Baldwin are also greatly appreciated. The electronic circuits were designed and constructed by S. R. Pedersen. N. MacDonald provided the angle-lapped sample.

REFERENCES

1. T. E. Everhart, O. C. Wells, and R. K. Matta, J. Electrochem. Soc. 111, 929 (1964).
2. A. V. Brown, IEEE Trans., ED-10, 8 (1963).
3. T. E. Everhart, O. C. Wells, and R. K. Matta, Proc. IEEE (to be published).
4. W. Czaja and G. H. Wheatley, J. Appl. Phys. 35, 2782 (1964) and J. J. Lander, T. M. Buck, H. Schreiber, Jr. and J. R. Mathews, Appl. Phys. Letters 3, 203 (1963).
5. D. B. Wittry and D. F. Kyser, J. Appl. Phys. 35, 2439 (1964).
6. O. C. Wells, T. E. Everhart, and R. K. Matta, Abstract No. 120, Fall meeting, Electrochemical Society, New York (1963).
7. A. N. Broers, Conference on electron beam techniques, RRE, Malvern, July (1964).
8. See Westinghouse Research Laboratories Seventh Interim Engineering Report, prepared under Contract No. AF 33(657)-9897, p. 38.
9. Ibid, p. 31.
10. T. E. Everhart and R. F. M. Thornley, J. Sci. Instr. 37, 246 (1960).

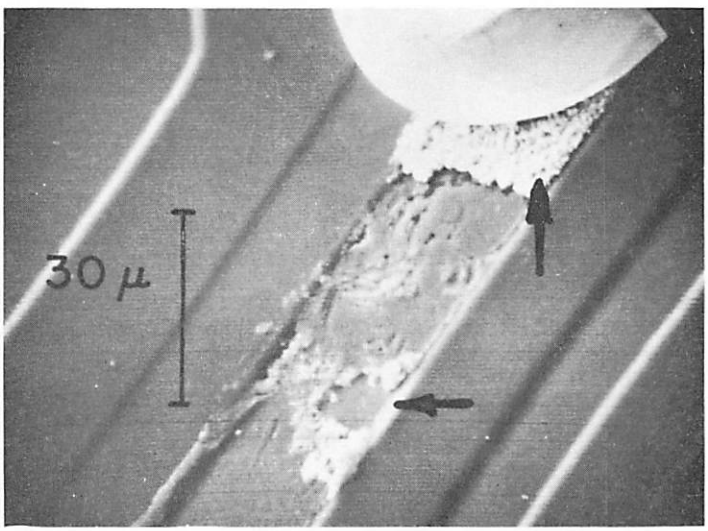
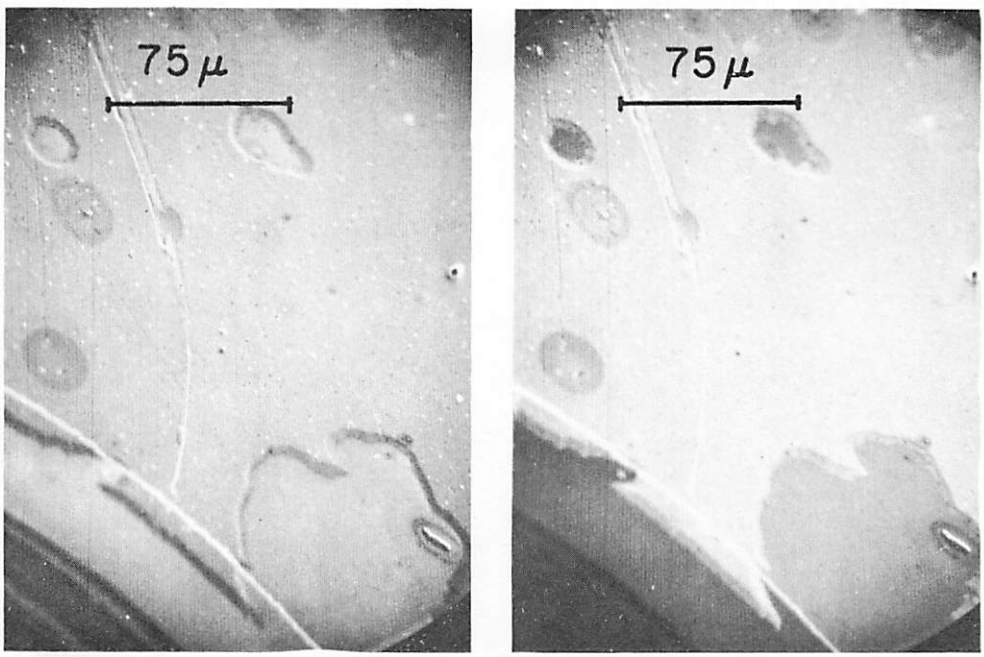


Fig. 1. Scanning electron micrograph of thermal-compression bond on a field-effect transistor.



zero bias 15v bias

Fig. 2. Scanning electron micrographs of a metal-oxide-semiconductor capacitor on a uni-junction transistor integrated circuit oscillator.

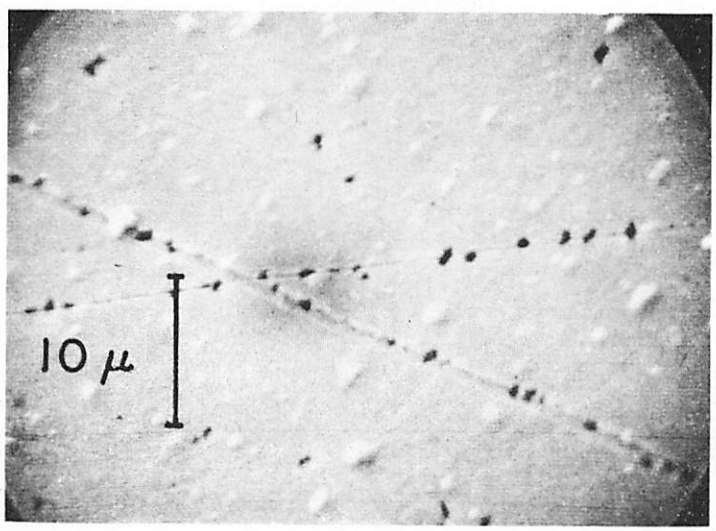


Fig. 3. Scanning electron micrograph of irregularities observed on the evaporated leads of the UJT oscillator of Fig. 2.

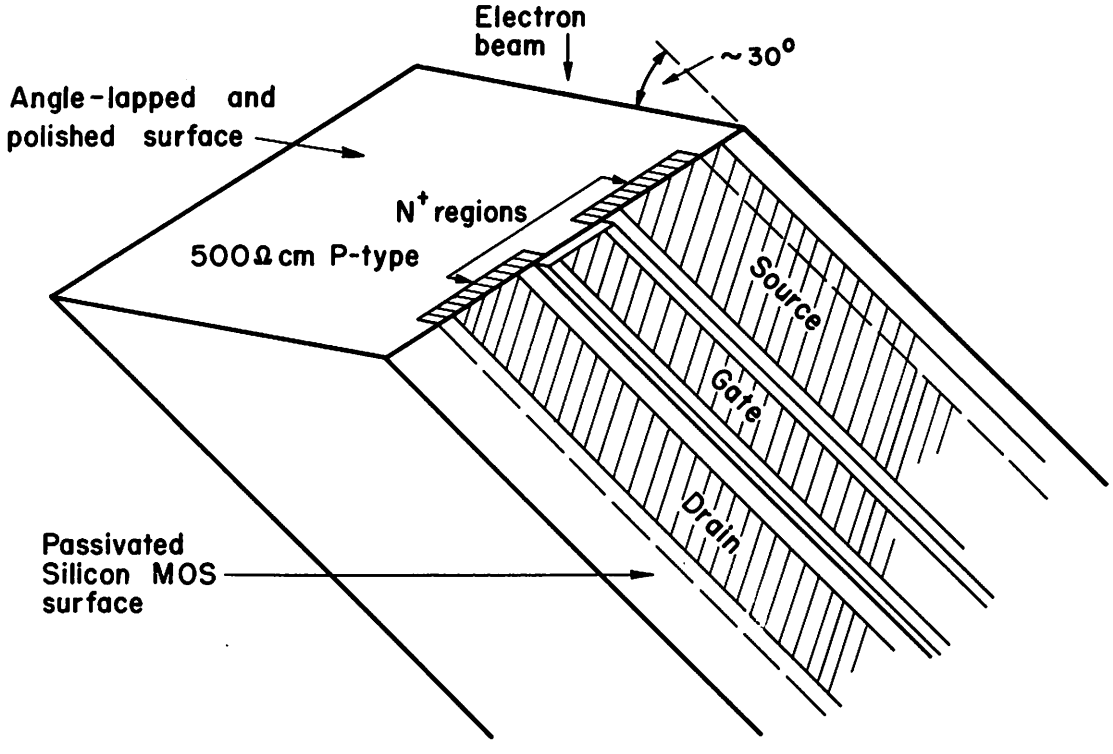


Fig. 4. Schematic diagram of lapped metal-oxide-semiconductor field-effect transistor (MOS FET).

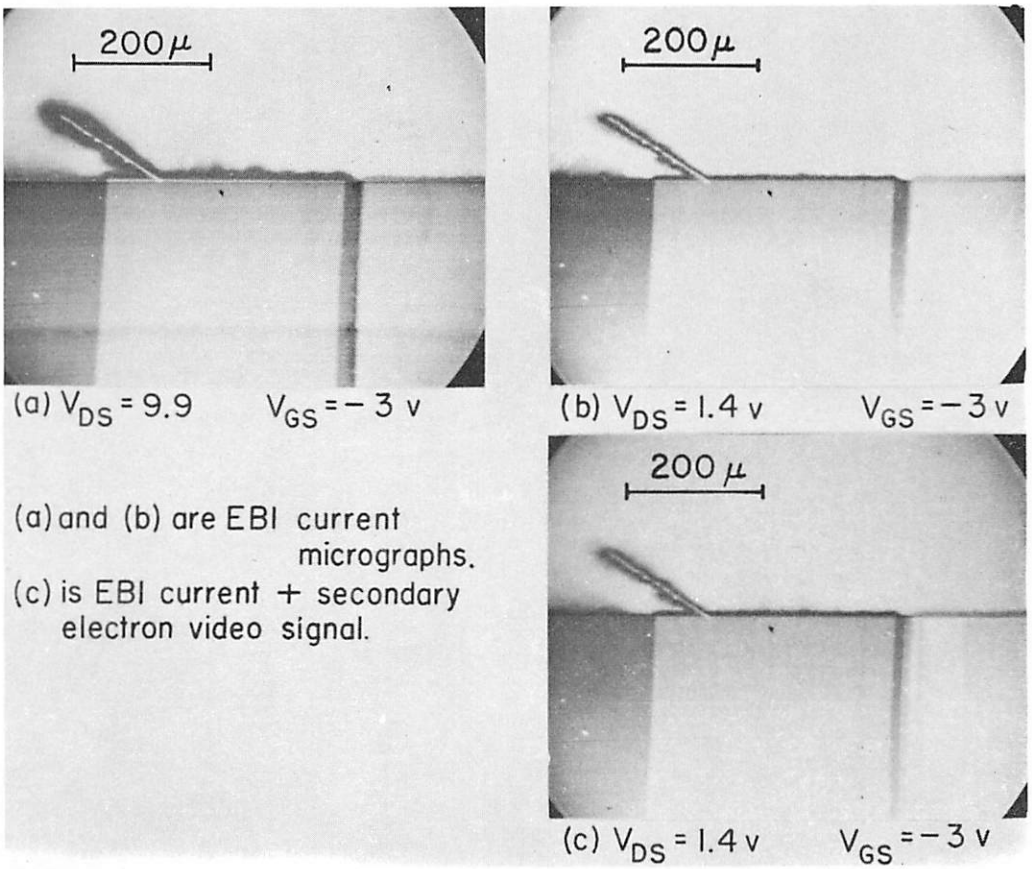
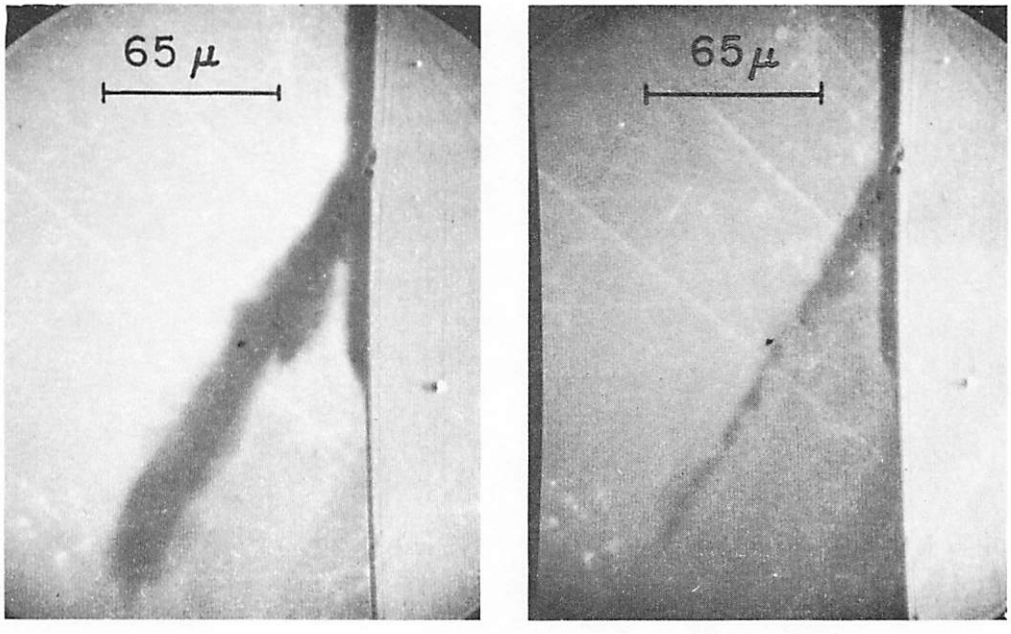


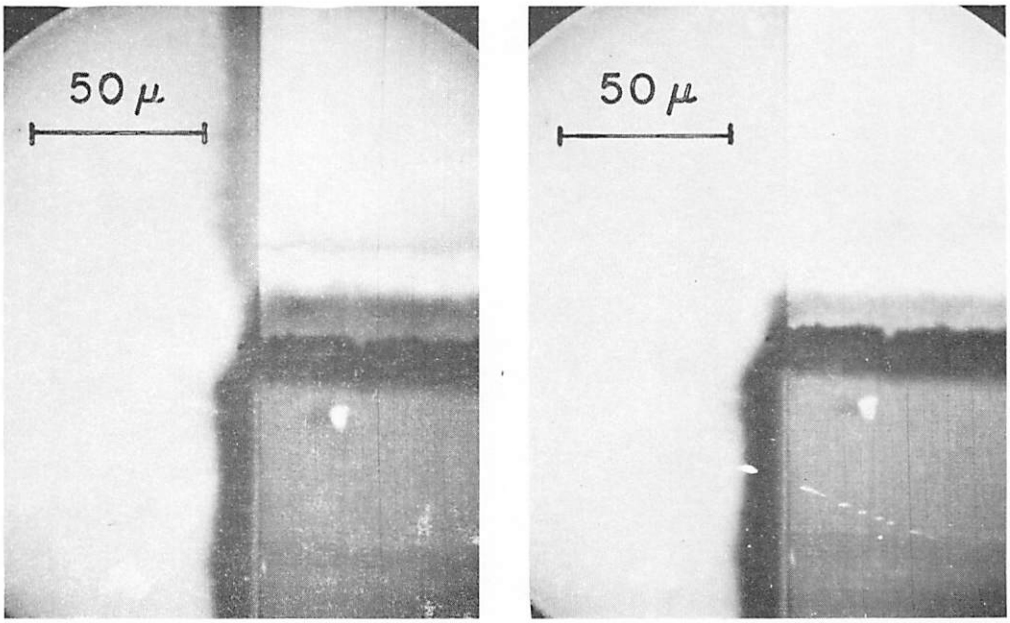
Fig. 5. Scanning electron micrographs of lapped MOS-FET.



V_{DS} = 10v V_{DS} = 3v

Secondary electron video signal.
MOS FET

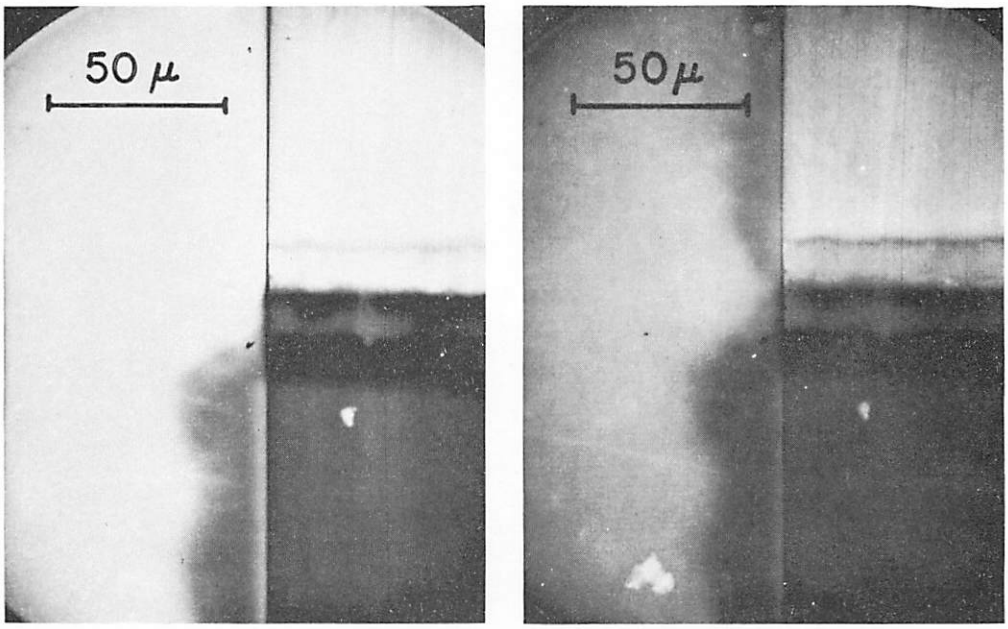
Fig. 6. Scanning electron micrographs of lapped MOS-FET.



V_{GS} = -3v V_{DS} = 1.5v V_{GS} = -6v

EBI current plus secondary electron video signal.
MOS FET

Fig. 7. Scanning electron micrographs of the source-gate-drain region of a MOS-FET.



V_{GS} = -4.5v V_{GS} = -3v

V_{DS} = 10v

EBI current plus secondary electron video signal.
MOS FET

Fig. 8. Scanning electron micrographs of the source-gate-drain region of a MOS-FET.