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HIGH-PERFORMANCE FIELD-EFFECT TRANSISTORS FORMED BY IMPURITY REDISTRIBUTION

by

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Unipolar field-effect transistors used as low-level, linear amplifiers should have a low pinch-off voltage. For a specified pinch-off current, transconductance is inversely proportional to pinch-off voltage[1] and equivalent noise resistance is approximately proportional to pinch-off voltage.[2]

Very precise process controls are necessary to fabricate reproducible low pinch-off field-effect transistors by ordinary methods of double-diffusion or epitaxy and diffusion. Alternative, less critical fabrication techniques are thus of interest. Impurity redistribution effects at a $Si-SiO_2$ interface, as described by Atalla and Tannenbaum,[3] may be employed to obtain a thin, lightly doped n-type layer at the surface of a p-type silicon wafer. It appears that such a layer may be designed to have the properties required for the channel of a field-effect transistor with low pinch-off voltage.

As the surface of a silicon sample is thermally oxidized, phosphorous in the silicon is almost entirely rejected by the oxide (the segregation coefficient $k \cong 0$ for phosphorous in this system). Hence, the

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phosphorous concentration in the silicon near the interface is increased. On the other hand, boron near an oxide interface is appreciably taken into the oxide, reducing the boron concentration in the silicon. The magnitude of this effect is not known exactly, but evidence developed in this laboratory and elsewhere indicates that the segregation coefficient for boron in the $Si-SiO_2$ system is in the range 10 to 1000.[4, 5]

If a silicon sample, homogeneously doped to 4×10^{17} atoms/cm^3 with boron and 10^{17} atoms/cm^3 with phosphorous, is oxidized in wet oxygen at 1000°C. until the oxide is 0.5 micron thick, the resulting impurity distribution in the silicon may be found using the solutions of Atalla and Tannenbaum. Assuming segregation coefficients k = 0 for phosphorous and k = 100 for boron, the results are shown in Fig. 1. A thin n-type region is formed in the silicon adjacent to the oxide; the main body of the silicon remains p-type. (With proper adjustment of the initial doping concentrations, a thin n-type region may be obtained for any assumed value of the boron segregation coefficient greater than about 10.) It appears that in processing it should be relatively easy to control the properties of the n-type region. For the case shown, the average net donor concentration in the n-region should be about 1.6×10^{17} atoms/cm^3.

The unipolar transistor structure shown in Fig. 2 may be formed using only two basic steps.

1) The n^+ source and drain contacts are formed using a conventional oxide-masked diffusion.

2) The oxide over the desired channel region is removed. A new 0.5 micron oxide is formed under the conditions described above.

The gate of the field-effect device is formed by the p-type region under the channel. There should be no inversion to n-type except in the desired channel region if the oxide over the surrounding regions has been grown slowly. However, possible problems due to such an undesired inversion could be eliminated with a diffused p-type guard ring surrounding the entire structure.

For a device of the dimensions shown, approximate calculations (taking the net impurity concentration gradient at the gate-channel junction as 5×10^{22} atoms/cm^4 and the contact potential as 0.85 volt) give the following electrical parameters: pinch-off voltage $V_p = 0.5$ volt, transconductance $g_{fs} = 2000$ micromhos, pinch-off current $I_{DSS} = 0.5$ milliampere. The current gain-bandwidth product for this device is approximately $f_T = \frac{g_{fs}}{2\pi C_{in}}$. The total input capacitance C_{in} should be about 9 pf. Therefore f_T for the device shown would be about 35 megacycles/sec. (The maximum frequency of oscillation[6] should be about 180 megacycles/sec.)

In comparison with the metal-oxide-silicon (MOS) field-effect transistor,[7] the device proposed here has a much higher ratio g_{fs}/I_{DSS}, a lower pinch-off voltage, and a comparable f_T. A potential advantage is

that close tolerances on the dimensions of the active region may be maintained without special care, because the geometry of the proposed device is fixed by the single mask of step (1) and by the controlled impurity redistribution process of step (2). An accurately indexed masking step to locate the gate (as must be used in the MOS device) is not needed, because the substrate serves as the gate.

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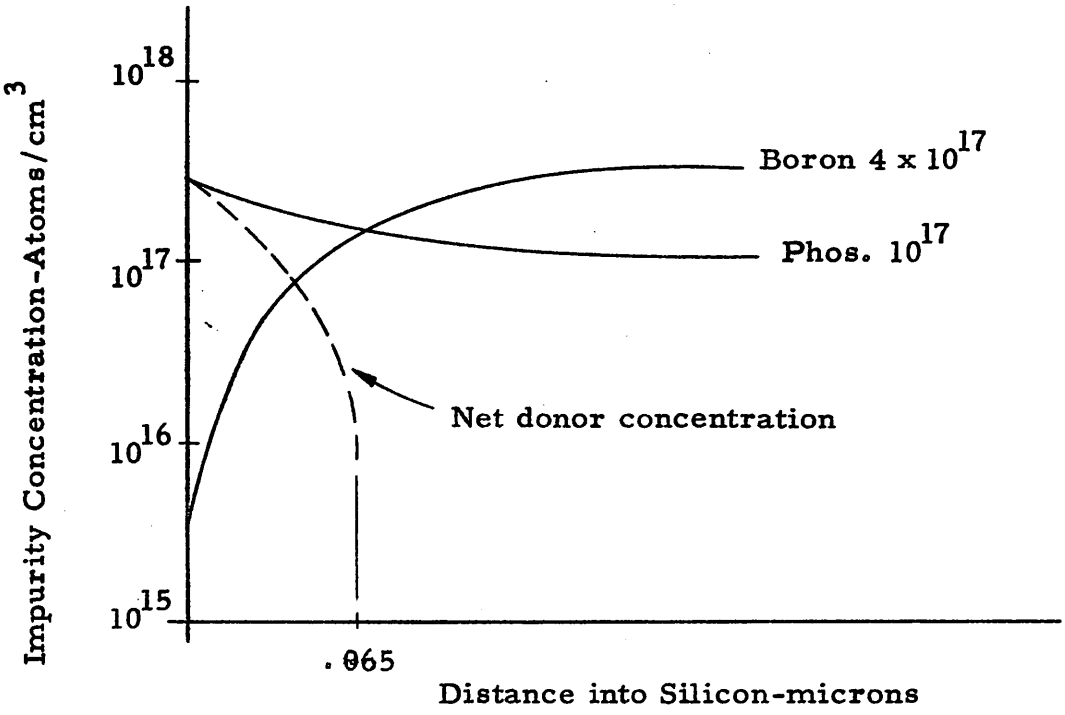

Fig. 1

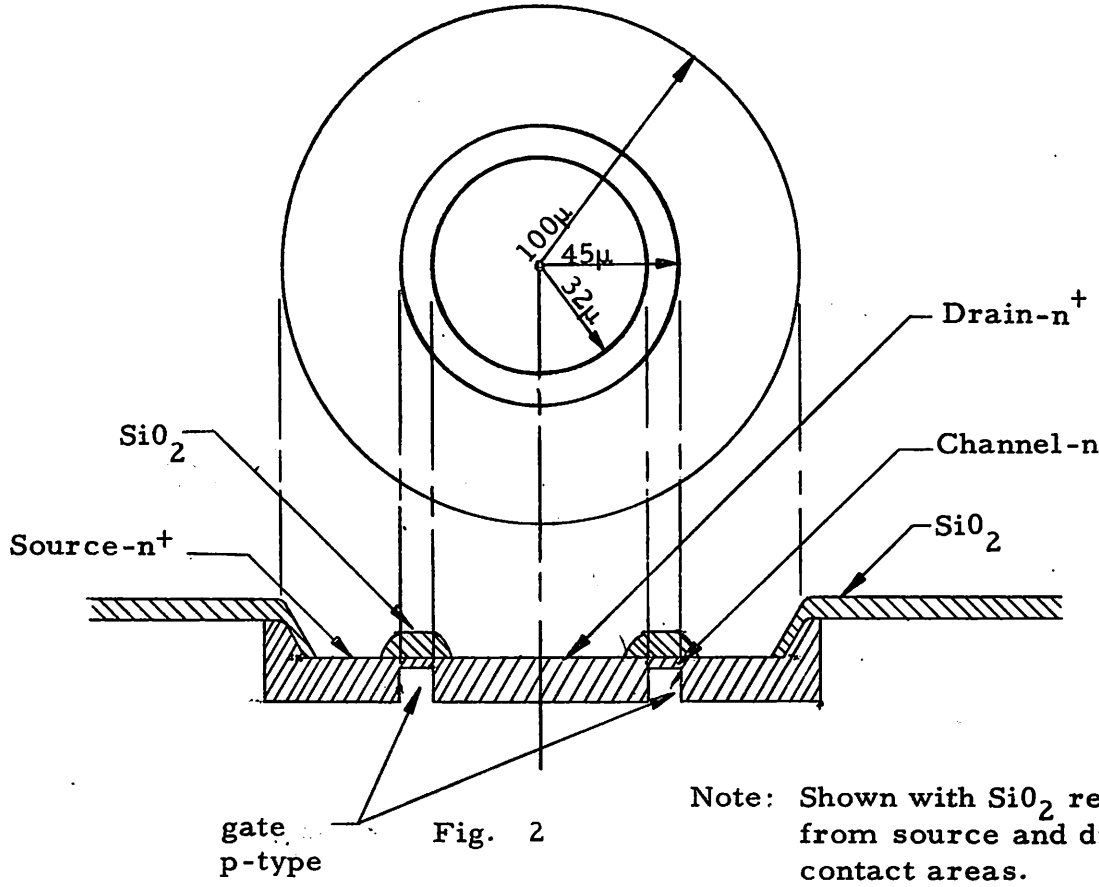

Fig. 2

Note: Shown with SiO_2 removed from source and drain contact areas.

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