Electronics Research Laboratory
University of California
Berkeley, California
Internal Technical Memorandum M-92

SYSTEMATIC GENERATION OF MONOSTABLE AND COUNTING BISTABLE CIRCUITS*

by

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*This research was supported by Aeronautical Systems Division, Wright-Patterson Air Force Base, under Contract No. AF33(615)-1045.

August 17, 1964

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Abstract--In this paper systematic procedures are developed for generating, from a given dc bistable configuration, monostable circuits and bistable circuits with the counting property. Essential to the synthesis is the controlled-resistance model, which represents those characteristics of three-terminal active devices necessary for the stable state realization of switching circuits. The synthesis methods make use of a new, simplified form of the total dc I-V characteristics of a complete bistable configuration viewed at any node pair. Criteria are developed for systematically determining all possible locations for the necessary energy storage elements of monostable and counting bistable circuits. Basic means of triggering these circuits are discussed. The procedures developed lead to existing and new circuits employing conventional (bipolar) and field-effect transistors. Some of these circuits are well suited to integrated realization. Experimental verification of the synthesis procedures is presented.

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I. INTRODUCTION

The principal procedure now being followed in the design of semiconductor integrated circuits is to achieve as closely as possible a one-to-one correspondence of regions in a semiconductor block with elements in a lumped prototype circuit. It is therefore desirable to have a means of obtaining prototype circuits which are in some sense optimum for integrated realization. This requires a knowledge of all possible circuits realizing the prescribed circuit function.

A recent paper shows that the dc configurations of all possible bistable circuits may be systematically generated.[1] The present paper describes a systematic technique by which monostable and bistable circuits with the counting property may be generated from given dc-bistable configurations.

Essential to the synthesis of bistable and monostable circuits is the controlled-resistance model for active devices.[1] The controlled-R model represents those characteristics of active devices essential to the stable-state realization of switching circuits, independent of the electronic processes of any particular device.

Bistable configurations may be synthesized by a systematic reduction of the group of all possible connections of two controlled-R models and one dc source. Most known bistable circuits and some new ones may be developed from the two dual configurations of Fig. 1(a) and (b) as shown in Ref. 1. A load resistance may be included, in series with the dc source V_s in Fig. 1(a) or in parallel with the dc source I_s in Fig. 1(b). However, these load resistances are not essential to bistable operation.

In order to obtain bistability, it is necessary to use two Class I active devices in the configuration of Fig. 1(a) and two Class II devices in the configuration of Fig. 1(b). (The Classes of active devices are defined in Ref. 1.) Systematic device and configuration conversion procedures make possible thirty different bistable circuits based on these two configurations, using only bipolar and unipolar transistors.[1] The simplest of the thirty circuits are shown in Fig. 1(c) and 1(d). These are derived from Fig. 1(a) and 1(b), respectively, and are called the basic bipolar and basic unipolar circuits. Load resistors are included in these practical circuits.

II. SIMPLIFIED I-V CHARACTERISTICS

The synthesis procedures developed in this paper require knowledge of the dc I-V characteristics of bistable circuits at all node pairs which may be created by "soldering iron" or "pliers" type entries[2] to a bistable configuration. In the discussion that follows, I-V characteristics are defined for the complete configuration, dc sources included. This convention is adopted in order that a uniform procedure for finding the I-V characteristics will be valid at all node pairs. The nature of the I-V characteristics at a node pair in a basic configuration is the same as that at the corresponding location in any circuit derived from the configuration.

A simplified form of the complete I-V characteristics, useful in switching circuit synthesis, may be developed directly from the essential stable-state and triggering properties of bistable circuits. If a soldering iron (pliers) entry is made at any node pair (branch) of a complete bistable configuration, the two stable states of the configuration will be observed as two stable values of the open-circuit node-pair voltage (short-circuit branch current). By inspection of the configuration in each stable state, it is determined whether a particular voltage (current) must be increased or decreased to cause a change of state. The results of this investigation are plotted on a set of I-V axes, with the direction of positive-current flow defined such that the slope of the plot is positive for small perturbations

about the stable points (as required by physical arguments for stability). The results of this inspection determine the location of the idealized dc trigger points with respect to the stable regions.

Fig. 2 shows the possible locations of trigger points relative to stable regions for any dc bistable configuration. Figs. 2(a) and 2(b) refer to soldering iron entries; Figs. 2(c) and 2(d) refer to pliers entries. I-V characteristics of the general form shown in Figs. 2(a) and 2(c) are called Type A; those of the form shown in Figs. 2(b) and 2(d) are called Type B. Because Type A and Type B characteristics are entirely defined by the relative locations of two stable regions and two trigger points, I-V characteristics in these forms are called simplified I-V characteristics. For many applications, the shape of the lines representing the stable regions is unimportant; straight lines are shown for convenience. It should be noted that the location of the I-V axes is not important in the definition of the simplified I-V characteristics; only the relative locations of the stable regions and trigger points are significant.

In the study of switching circuits, the simplified I-V characteristics have two principal advantages over continuous I-V plots of the usual sort. First, the simplified characteristics represent the complete circuit with all components and sources connected. Therefore, a single set of examination and circuit modification procedures is applicable at any node pair, even if there is no removable resistance between the nodes.[3] Second, the simplified I-V characteristics emphasize the information essential to the synthesis of monostable and counting bistable circuits. The relative locations of the trigger points and stable regions are all that are required; these are often easily determined by inspection. The details of a complete, continuous I-V characteristic which are hard to find by inspection are not needed.

It will now be shown that the simplified characteristic across any R_0 branch of any bistable configuration is Type A. In every case, when the controlled-resistance is in the state involving the lower value of the control current I_1, I_1 must be increased to cause a major change

in $R(I_1)$ and a change of state of the configuration. Similarly, when I_1 is at its higher stable value in a bistable configuration, I_1 must be decreased to cause a change of state. Referring to Fig. 2(a) we see that these statements completely define the Type A characteristic at a soldering iron entry. Therefore, the simplified I-V characteristic across any R_0 is always Type A.

Examination shows that in the basic configurations of Fig. 1, the controlled-resistance branches are not independent. Thus their simplified I-V characteristics are the same as those for the R_0 branches except for the possible addition of a dc voltage offset. Therefore every node-pair in a basic configuration has Type A simplified I-V characteristics for soldering iron entries.

Now consider the form of the simplified I-V characteristics at a pliers entry made in an R_0 branch as shown in Fig. 3(a). When the current in this branch is at the lower of its two stable values, this current must be increased to cause a change of state. When initially in the higher current state, the current must be decreased. These statements define the Type B characteristic at a pliers entry as shown in Fig. 2(d). Following a similar line of argument, it may be determined that the characteristic for a pliers entry in a branch leading to any of the three terminals of either active device is Type B.

Later it will be seen that in the synthesis of monostable and counting bistable circuits it is essential to have available a Type B characteristic at a soldering iron entry. Such may be obtained by inserting a resistance R_a in a pliers entry, as shown for example in Fig. 3(b). There are limits on the magnitude of R_a; these must be determined in the final design of a practical circuit.

III. MONOSTABLE CIRCUIT SYNTHESIS

A monostable circuit has one dc stable state. An electrical input exceeding a certain threshold and of proper polarity (henceforth called the trigger) causes a monostable circuit to switch regeneratively to a distinct quasi-stable state. The circuit remains in the quasi-stable state for a time substantially independent of the characteristics of the trigger, because the energy required to maintain the quasi-stable state originates within the circuit. A portion of the return from the quasi-stable state to the stable state must also be regenerative. Regenerative switching implies that every nondegenerate node-pair of the complete circuit displays a negative conductance in its I-V characteristics, bounded by two positive conductance regions.

A general method for creating a monostable circuit from a bistable circuit will nowbe described. The objective of this procedure is to develop the dc topology and the locations for the essential energy storage elements of a monostable circuit. All monostable circuits have nonzero switching and recovery times. These times, as well as the duration of the quasi-stable state, can be determined by the techniques of conventional circuit analysis. Comments on triggering are added in the next section.

Consider first any node pair which has a Type B characteristic for a soldering iron entry. This will occur at the terminals of inserted resistor(s) R_a. Note that in the Type B characteristic in Fig. 2(b) one stable state may be eliminated by connecting at this entry a current source of the proper value, denoted by I_s[4]. The I-V characteristic with I_s connected, viewed at the same node pair, becomes that shown in Fig. 4(a). Alternatively, one dc stable state often may be eliminated by adjusting the value of R_a. In either case, there are still two separate segments in the simplified I-V characteristics after eliminating one stable state.

A quasistable state may now be created by connecting a capacitor at the Type B node pair, provided that if the voltage at this node pair is

held constant, there is a possible operating point on each of the two stable segments of the simplified characteristic. This latter requirement is met by proper adjustment of I_s and/or R_a. The current through the added capacitor immediately following a change of state caused by an external trigger[5] assumes a value on the segment of the simplified I-V characteristic which has no stable intercept with the V axis. The value of current assumed must be consistent with the charge on the capacitor and with the magnitude of the trigger present at the instant of observation.

The monostable circuit is in the quasi-stable state as long as it is on the segment of the I-V characteristic which has no intercept with the V axis. While the circuit is in the quasi-stable state the capacitor discharges through the positive conductance represented by the upper segment of the I-V characteristic until the trigger point (T_{12} in Fig. 4(a)) is reached. At this point, the circuit returns regeneratively to the I-V segment which includes the dc stable point.

Using the above synthesis procedures a monostable circuit may be created from any bistable configuration through simple operations at a soldering iron entry which displays a Type B simplified I-V characteristic. The basic technique is to eliminate one stable state of the bistable configuration and add a capacitor to store the energy necessary to obtain a quasi-stable state.

Consider now the Type A simplified characteristic shown in Fig. 2(a) for a soldering iron entry. A current source may be added, eliminating one stable state. The resulting simplified characteristic is shown in Fig. 4(b). A quasi-stable state cannot be created by connecting a capacitor at a node pair displaying this type of characteristic, because a constant voltage line through the stable value of node pair voltage does not intercept the other segment of the characteristic. The voltage across the capacitor must be changed in order to obtain an operating point other than the stable point. If such an arrangement were to be

monostable, the trigger would be the source of the change in stored energy. Thus monostable circuits cannot be created using capacitors connected at Type A soldering iron entries.

A number of practical monostable circuits employing bipolar and unipolar transistors may be systematically developed using the techniques described above in conjunction with the device and configuration conversion procedures described in Ref. 1. For illustration, a practical monostable circuit is now generated starting with the bistable configuration of Fig. 5(a). A consistency argument shows that this configuration has stable states with both controlled-Rs in the low resistance state and with both in the high resistance state. Examination shows that node pair DC has the Type B simplified I-V characteristic for pliers entry shown in Fig. 5(b). Note that one stable state may be eliminated by simply open-circuiting this pliers-type entry, as discussed earlier. Thus monostable behavior is expected if a capacitor is connected at this node pair.

To obtain a practical circuit, the controlled-Rs are replaced with normal active devices. Unipolar transistors are chosen because of the requirement for Class II controlled-Rs in this configuration. Polarity restrictions require one transistor of each conductivity type. The basic circuit is shown in Fig. 5(c).

The final practical circuit is shown in Fig. 6(a). To stabilize the performance of the circuit against the effects of the temperature dependent leakage current of the gate-channel junction of the unipolar transistor, a resistor R_x is connected between nodes D and B. Monostable operation of this circuit has been observed experimentally; the output waveform is shown in Fig. 6(b). The circuit may be triggered at node A, as shown, or at other locations.

IV. BISTABLE CIRCUITS WITH THE COUNTING PROPERTY

A bistable circuit has the counting property if a monopolarity trigger pulse train applied at one port causes the circuit to alternate between its two stable states. Counting bistable circuits may be divided into three classes. The first class makes use of energy stored in properly located "memory" elements in order to obtain the counting property. A second class of counting circuit relies upon delays in gates or other elements to properly route trigger pulses. Generally more elements are required to obtain a counting circuit with this technique than with the first. These two classes of counting circuits are of interest for semiconductor integrated realization. The discussion in this section centers on the memory circuits. It can be shown that the delay-routed circuits may be regarded as a special case of the memory circuits.

A third class comprises all counting circuits which require a resonant combination of capacitors and inductors, as well as resistors and active elements. These circuits are analyzed in the literature;[6, 7] they are of little interest for integrated circuitry because of the difficulty of obtaining inductance in semiconductor integrated form.

The possible locations for energy storage in a monostable circuit are directly related to the energy storage locations in a bistable circuit if it is to have the counting property. In this section, memory and triggering criteria for basic configurations will be determined, and a systematic procedure is developed which will produce a counting bistable circuit from a basic bistable configuration. The conclusions drawn concerning memory in a basic configuration hold true for all circuits derived from it by device and configuration conversions,[1] because these conversions do not change the Type of the simplified I-V characteristics at any given node pair.

Memory and triggering criteria are first established for the basic configuration of Fig. 1(b) which is reproduced here as Fig. 7(a).

This configuration is chosen for discussion because of the many practical bistable circuits which are derived from it, e.g., the Eccles-Jordan, Schmitt, and some new circuits.[1]

The simplified I-V characteristics obtained by examination of a dc configuration are meaningful only for dc or very slowly changing conditions. However, it can be seen from the simplified characteristics of Fig. 2 that a capacitance, if it is to provide memory during switching of a previous state, should not be connected with a soldering iron entry at a Type A node pair. The voltage at a Type A node pair must change in order to obtain a change of state; since the charge of the previous state is lost in switching, the capacitance across a Type A node pair cannot supply memory.

Now consider the effect of capacitors connected at Type B node pairs as shown for instance in Fig. 7(b). (Two R_a-C_a pairs are used to preserve the symmetry of the configuration; only one such pair is essential to operation. The values of R_a must not be so large as to destroy the dc bistability.) A physical argument to determine the effect of the capacitors C_a may be developed as follows. The equilibrium voltage V_a across the capacitors C_a assumes one of two values, depending upon the state of the circuit. If these capacitors are large, V_a does not change during switching. Therefore, for switching analysis, the combination R_a-C_a may be replaced by a battery, as shown in Fig. 7(c).

Starting from each of the two stable states, we must compare the action of the circuit just after some disturbance which forces the circuit into the active region. The voltages V_a have either low values or high values depending on the previous state of the configuration. After the disturbance, a low value of V_a leads to a relatively large current in R_0 which corresponds to the opposite state. Similarly, if the V_a are large, relatively small currents flow in the R_0, corresponding again to the opposite state. Therefore, the V_a favor a change of state, starting from either stable state.

The physical reasoning suggested above concerning the effects of memory elements on the switching properties of a configuration has been verified using a conventional analysis of the circuit when both devices are active. For this analysis, simple charge-controlled models of the active devices suitable for active region analysis replace the non-linear, controlled-R models.

The triggering properties of a counting bistable circuit may rely on second-order effects in the active devices not represented by the first-order controlled-R and charge-controlled models. To obtain a complete picture of triggering performance it is often necessary to model active devices in greater detail than has been done here. However, it is possible to provide a general guide to several potentially workable means of triggering counting bistable circuits, as shown with reference to the following example. A simple bistable circuit with memory may be created by replacing the controlled-R models in Fig. 7(b) with unipolar transistors, adding resistors R_x to stabilize the circuit against the effects of variation in the gate leakage current. The resulting circuit is shown in Fig. 8(a); this is called the Basic Unipolar Circuit. A load resistor is included, as would be the case in all circuits of practical interest.

One possible means of triggering the circuit is to put a normally-on current switch in the common ground lead of the circuit and to use a trigger pulse to open this switch. A convenient current switch is a normally saturated bipolar transistor, connected as shown in Fig. 8(b). The action of the circuit is as follows. When both unipolar transistors are in the OFF state, V_1 and V_2 are large. Opening the transistor switch with a trigger pulse stops the current flow from V_{cc} and allows V_1 and V_2 to decay toward zero. Therefore, at the end of the trigger pulse both devices may be active. If the loop gain is greater than unity, the circuit will switch regeneratively to the low voltage state.

On the other hand, when the circuit is initially in the low voltage state, it remains in this passive state at the end of the trigger. Switching therefore does not occur. One way to overcome this difficulty is to

connect a small capacitance C_L across the load resistor. At the end of the trigger, the voltage $(V_{cc} - 2V_a)$ divides initially across C_L, C_{01}, and C_{02}. (Before adding C_L, all of this voltage appeared initially across R_L.) The voltage thus developed across the two C_0 may be sufficient to pull the devices into the active region; the circuit may then switch regeneratively to the high voltage state. Note that C_L is placed at a Type A node pair. This tends to slow the operation of the circuit once regeneration begins and to increase the required memory.

Another means of triggering which at first appears possible is through the application of either a positive or negative current trigger pulse at the midpoint between the two unipolar transistors. This is shown as the current source I_b in Fig. 8(b). This technique does not work with the circuit as shown because the circuit is unbalanced with respect to the midpoint. One state is favored, and if the circuit is adjusted to be well within its normal limits of operation as a dc bistable circuit, triggering to the nonfavored state is impossible. However, if R_L is split as shown in Fig. 8(c), midpoint triggering in the counting mode is possible with a pulse train of either polarity.

Triggering with a current pulse I_a at the load, as shown in Fig. 8(b), is generally undesirable because isolation between input and output is lost.

Three basic triggering techniques may now be listed, with the necessary form of entry to the circuit for each case.[8]

a. Interrupt main line current--one pliers entry.
b. Current trigger at midpoint--one soldering iron entry.
c. Alternate node routing of current trigger--two soldering iron entries.

The most familiar form of alternate node routing is diode routing, as when two diodes are used to route trigger pulses to collectors or bases of a conventional cross-coupled Eccles-Jordan flip-flop. A necessary condition for alternate node routing is that a change of state causes a polarity reversal between two floating nodes.

Conversion of devices and configurations leads to a number of other circuits, many of which are easier to trigger in the counting mode than the Basic Unipolar circuit discussed above. When triggering becomes easier, it is usually the result of a more favorable change of charge in the active devices during or after triggering. Further study of triggering properties of counting circuits is needed.

A systematic procedure for obtaining a memory-type counting bistable circuit from a dc bistable configuration is now described.

a. Choose a basic bistable configuration. Make device and/or configuration conversions in the light of particular needs.
b. Create one or more Type B node pairs.
c. Substitute practical devices for the controlled-R modes; establish element values and supply voltages; install memory capacitors.[9]
d. Select a practical triggering technique.

As an example of the synthesis, a new bistable counting circuit is now described. The basic configuration used is shown in Fig. 7(a). Converting controlled-R model number 2 at its input and replacing the models with appropriate physical devices, we obtain the bistable circuit of Fig. 9(a).[1] This circuit has stable states with both devices ON and both OFF. A Type B node pair is created through the addition of resistor R_a; establishing suitable element values and adding a memory capacitor C_a, we obtain the circuit of Fig. 9(b).[10] This circuit was used for experimental studies.

The trigger input is applied with a soldering-iron entry at the emitter of the bipolar transistor. This is equivalent to midpoint triggering of the basic configuration. With a negative current trigger, the favored switching direction is OFF to ON. When the circuit is initially ON, a negative trigger drives the bipolar transistor further ON and the unipolar transistor toward OFF; furthermore, the voltage V_a is increased by the trigger. At the end of the trigger pulse, the base-emitter voltage of the bipolar transistor can fall below its equilibrium

ON value, allowing the device to enter the active region. Because the unipolar transistor is already in the active region, regenerative switching can take place. The observed operating waveforms verify this explanation of ON to OFF switching.

A working silicon integrated realization of this circuit has been fabricated in our laboratory. (See Fig. 10.) This circuit offers certain advantages in simplicity and performance over conventional integrated counting circuits.[11]

ACKNOWLEDGEMENT

The authors are indebted to G. D. Hachtel for many ideas and helpful discussions.

FOOTNOTES

* Received _____. This research was supported by Aeronautical Systems Division, Wright-Patterson Air Force Base, under Contract No. AF 33(615)-1045.

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1. L. O. Hill, D. O. Pederson, and R. S. Pepper, "Synthesis of electronic bistable circuits," IEEE Trans. on Circuit Theory, vol. CT-10, no. 1, pp. 25-35; March 1963.

2. E. A. Guillemin, Introductory Circuit Theory, John Wiley and Sons, New York, N. Y., p. 92; 1953.

3. The usual form of I-V characteristics for bistable circuits represent the circuit with a resistance removed at the point of inspection. This approach is the result of a device-oriented, rather than circuit-oriented, view of negative resistance. Cf. L. Strauss, Wave Generation and Shaping, McGraw-Hill Book Co., New York, N. Y., pp. 315-325; 1960.

4. One stable state may alternatively be eliminated by some other adjustment of the circuit.

5. The trigger may be applied at any convenient location. It is obviously not practical to apply the trigger across the capacitor.

6. W. J. Cunningham, Introduction to Nonlinear Analysis, McGraw Hill Book Co., New York, N. Y., pp. 106-114; 1958.

7. A. L. Whetstone and S. Kounosu, "One-tunnel-diode binary," Proc. IRE (correspondence), vol. 49, no. 9, p. 1445; Sept. 1961.

8. The triggering conditions for monostable circuits are basically the same as those for bistable circuits.

FOOTNOTES (Cont'd.)

9. There is a minimum size for the memory elements, determined by the capacitances shunting the Type A node pairs and by the method of triggering. Cf. D. K. Lynn, and D. O. Pederson, "Switching and Memory Criteria in Transistor Flip-Flops," IRE International Convention Record, Part II, p. 3; 1960.

10. R_a also could have been placed in the emitter-source or gate-collector branch in the circuit of Fig. 9(b). The location chosen is advantageous for integrated realization.

11. D. A. Hodges, D. O. Pederson, and R. S. Pepper, "A simple integrated realization of a new bistable circuit," Digest of Technical Papers, 1964 International Solid-State Circuits Conference, pp. 72-73; 1964.

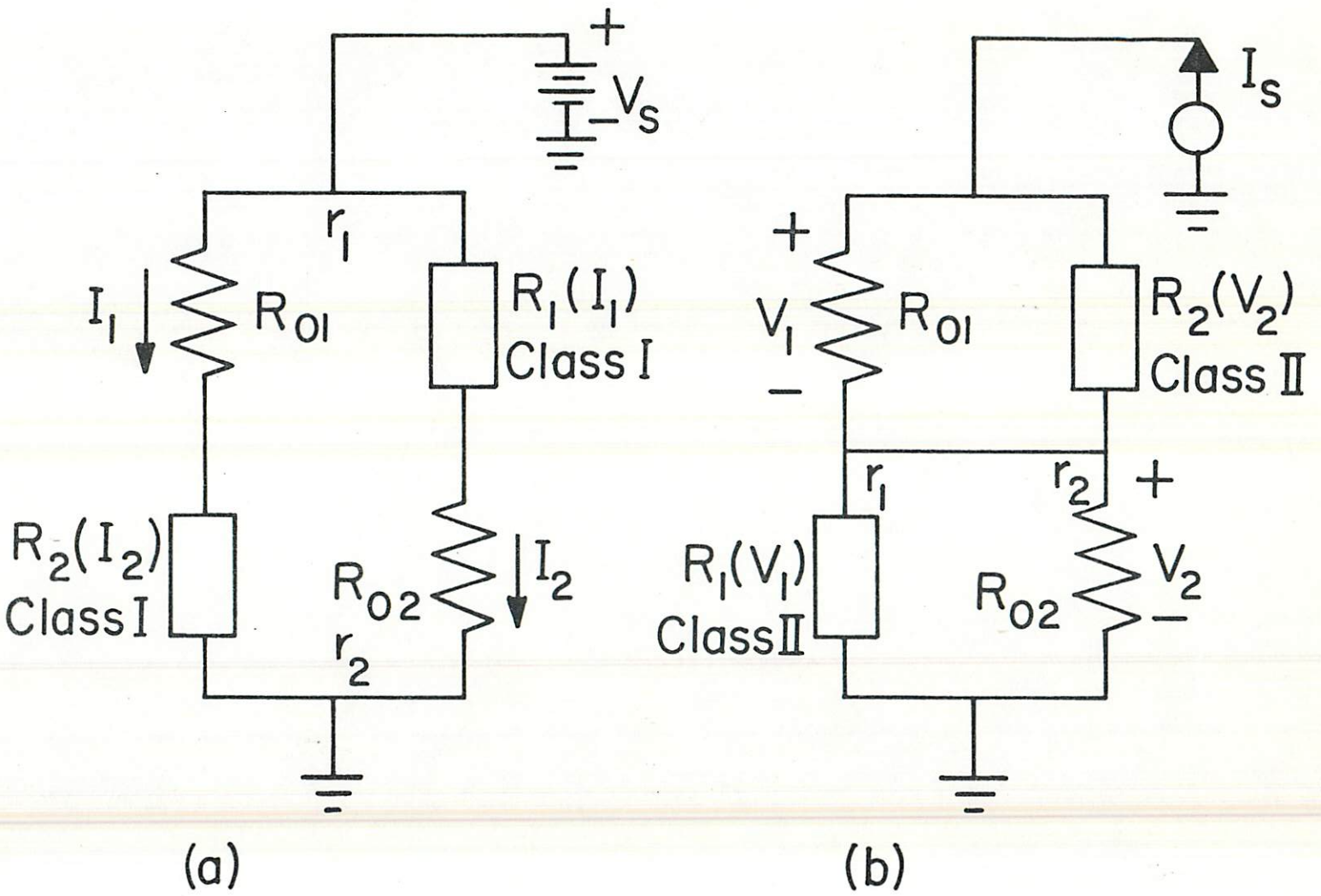

Fig. 1. Basic bistable configurations and simplest related circuits.

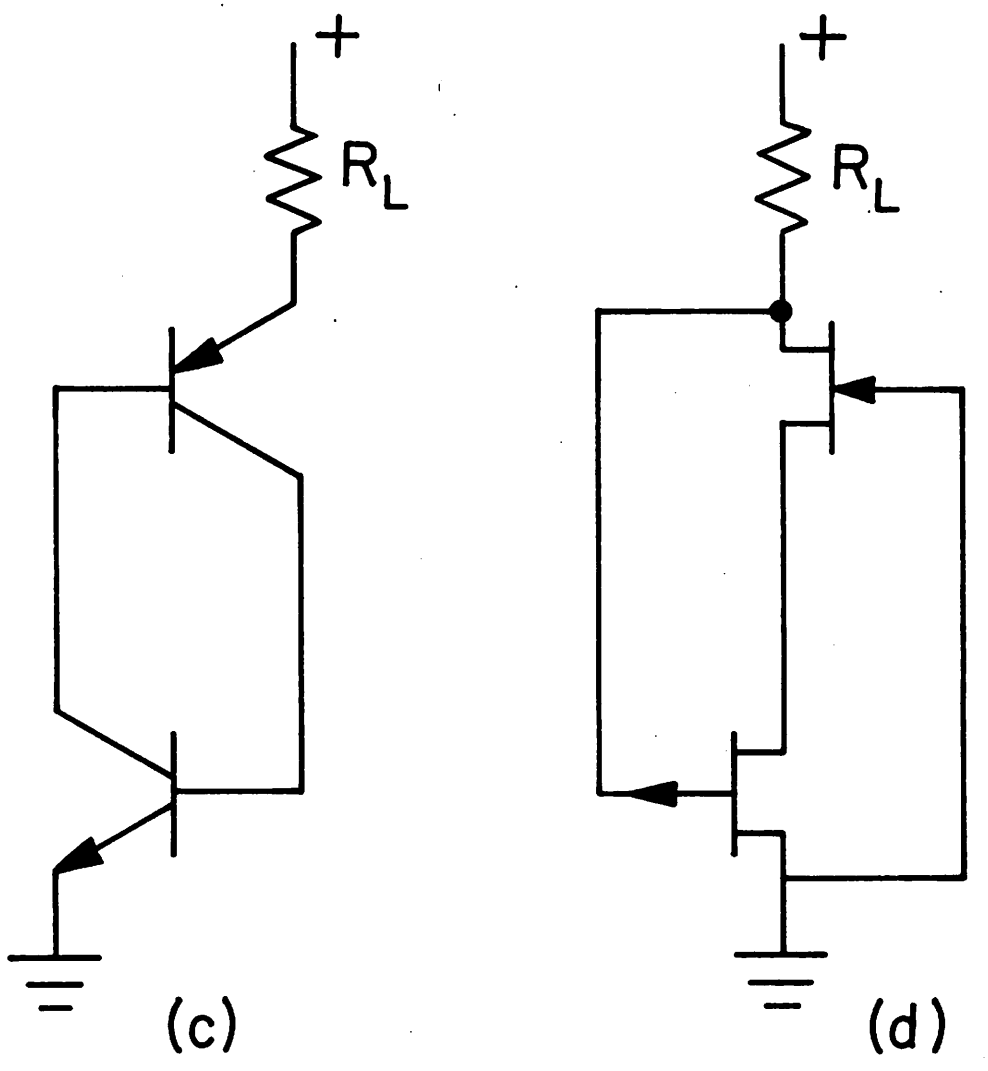

Fig. 1. (Cont'd.) Basic bistable configurations and simplest related circuits.

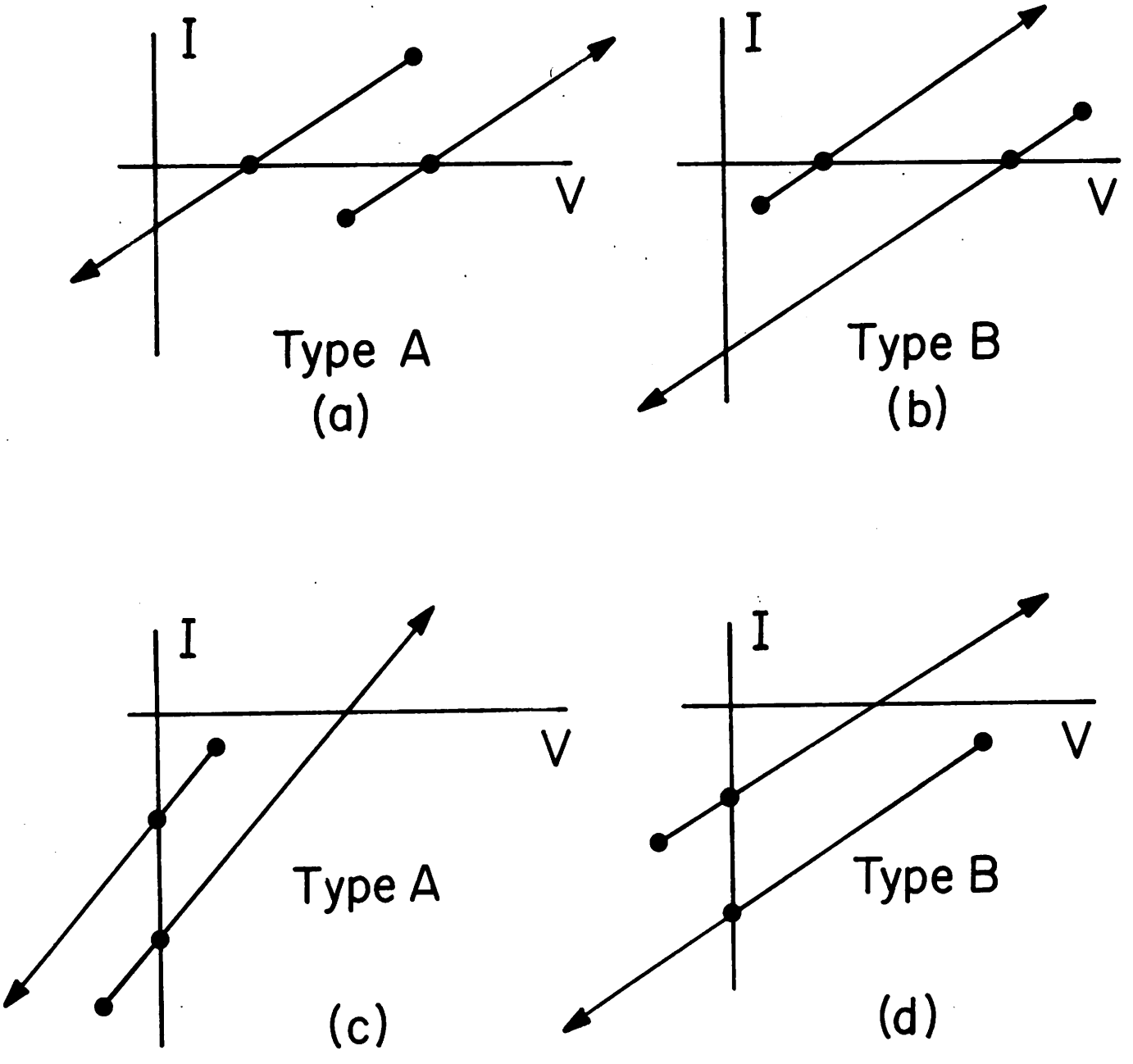

Fig. 2. Simplified I-V characteristics for bistable circuits.

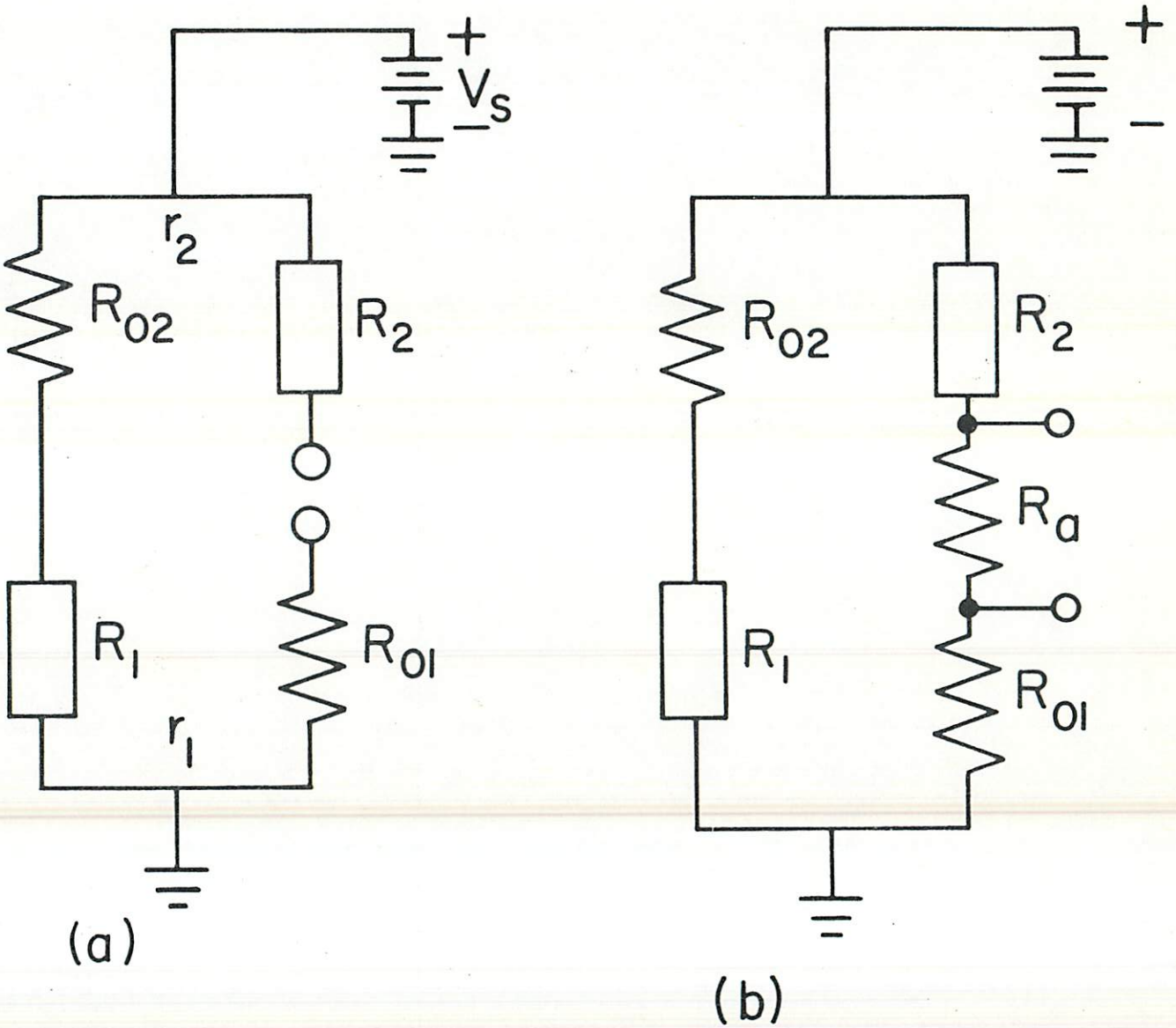

Fig. 3. Obtaining a Type B node pair.

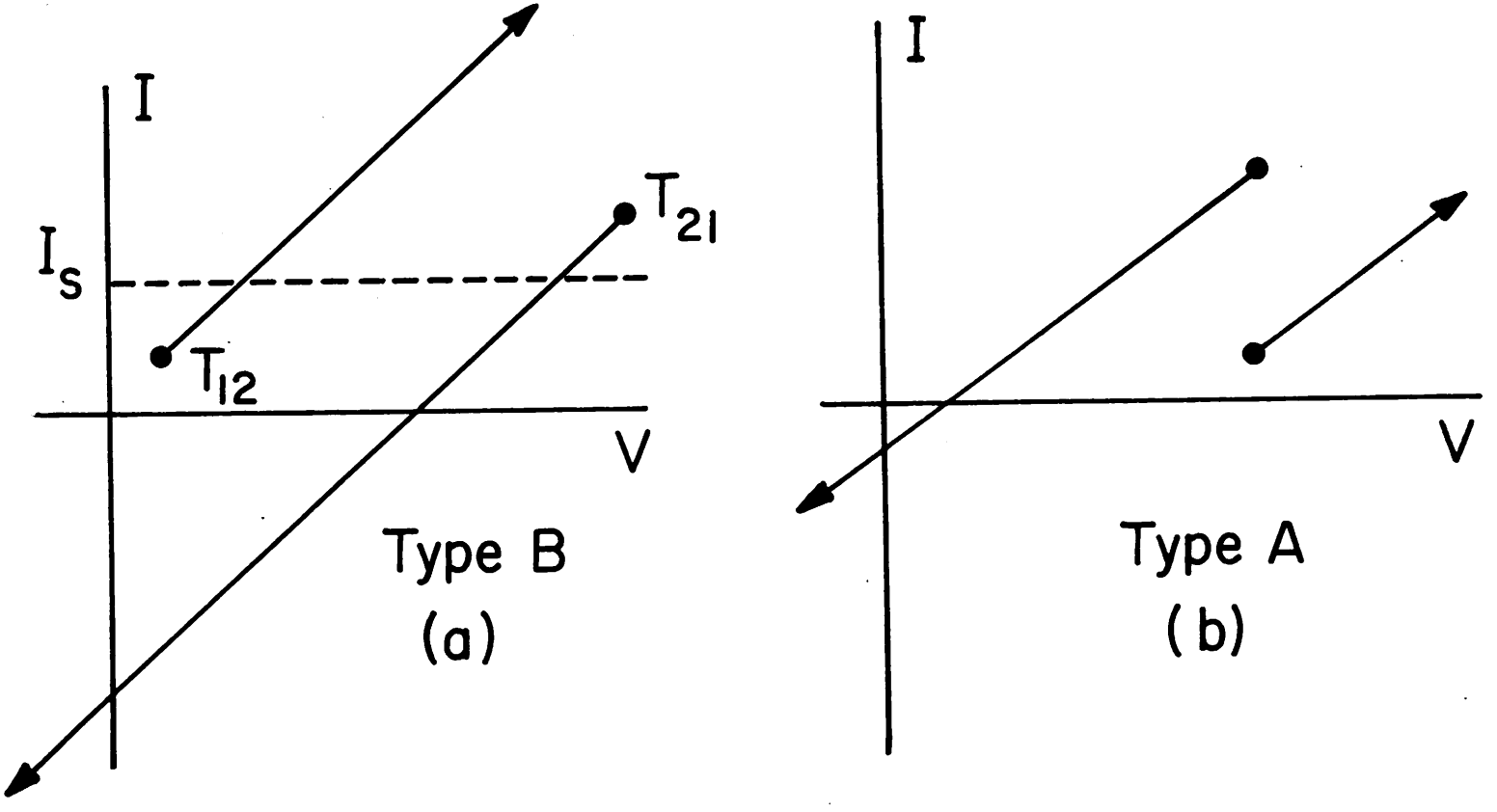

Fig. 4. Elimination of one stable state.

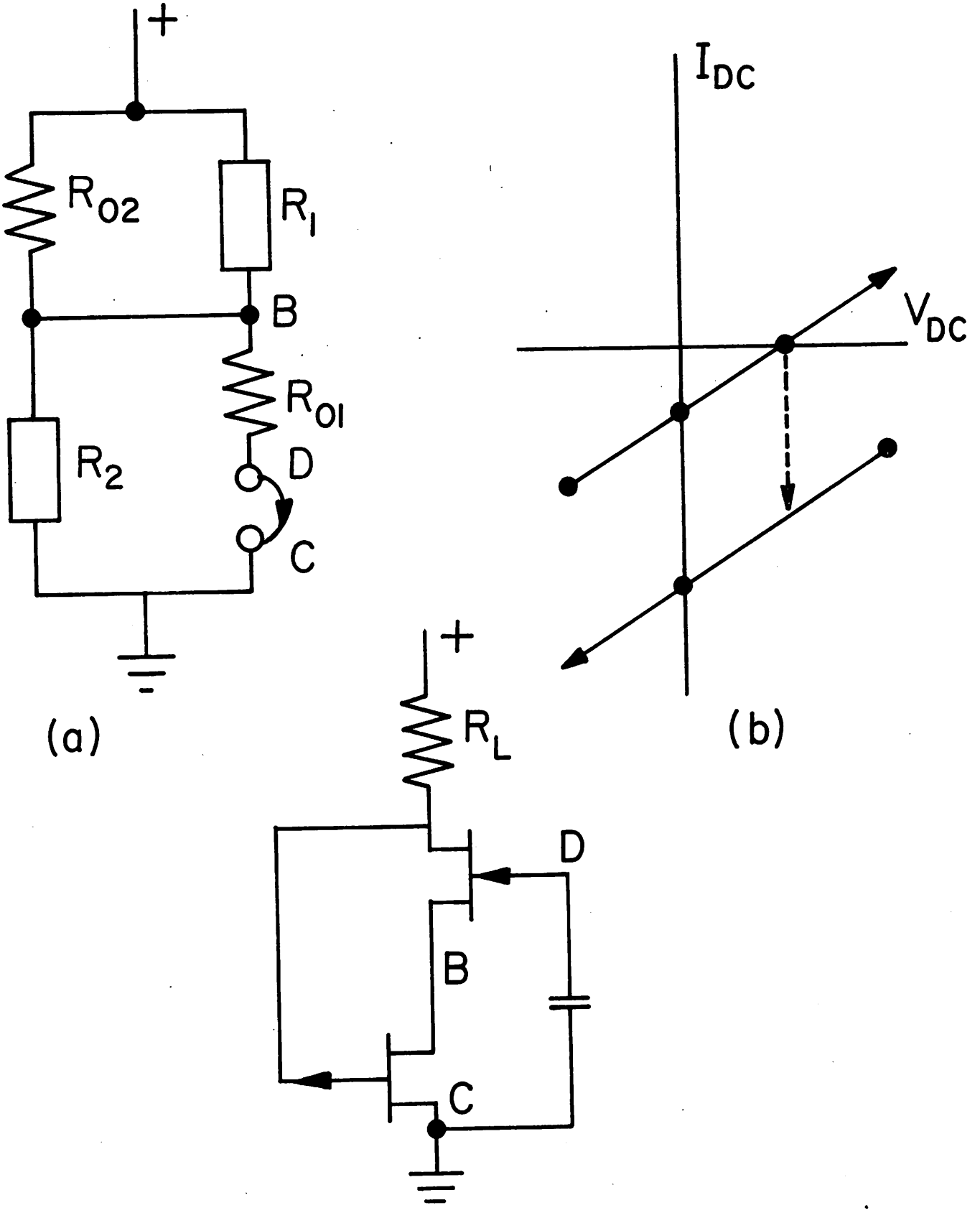

Fig. 5. Developing a monostable circuit.

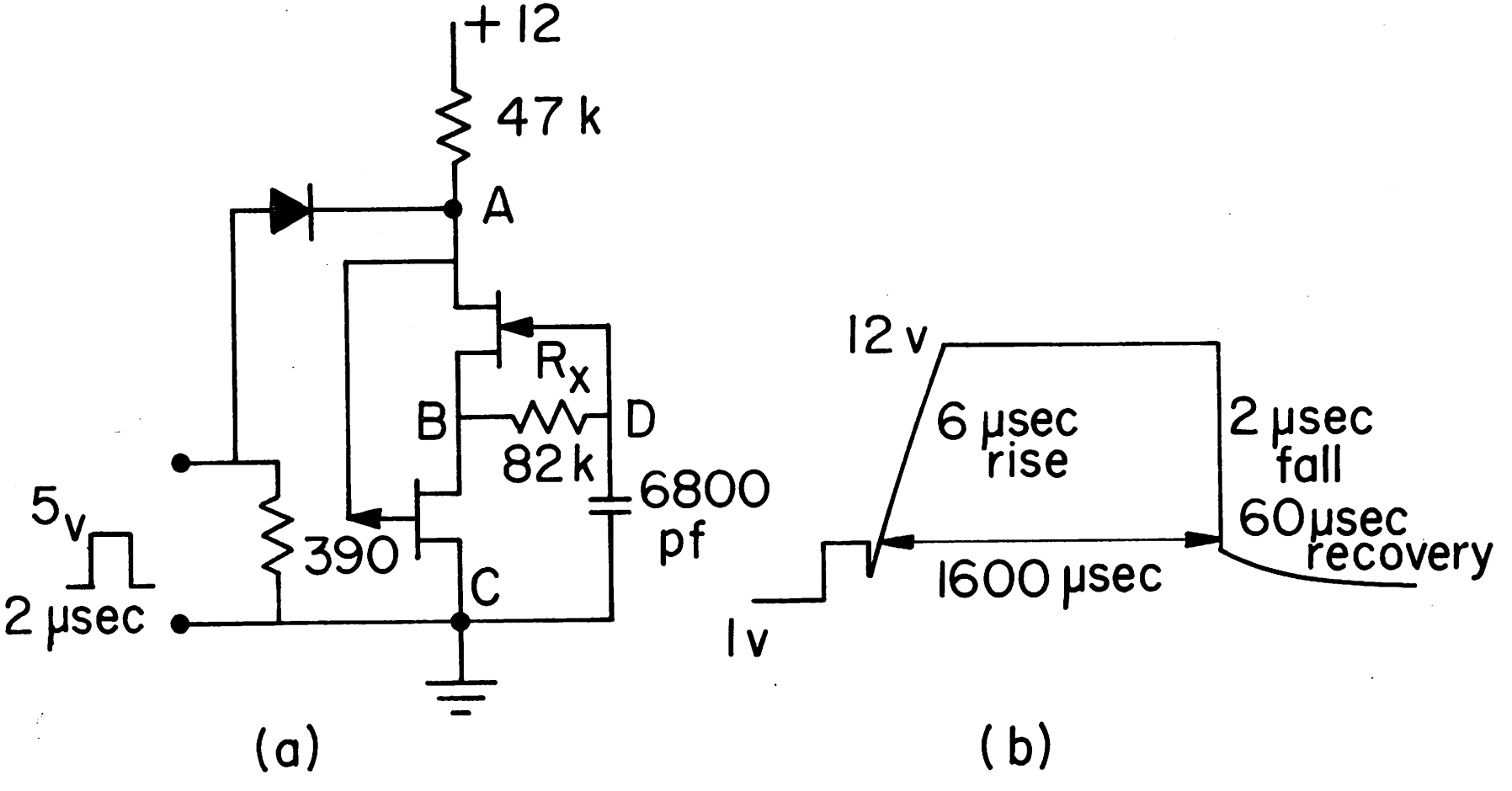

Fig. 6. Experimental monostable circuit.

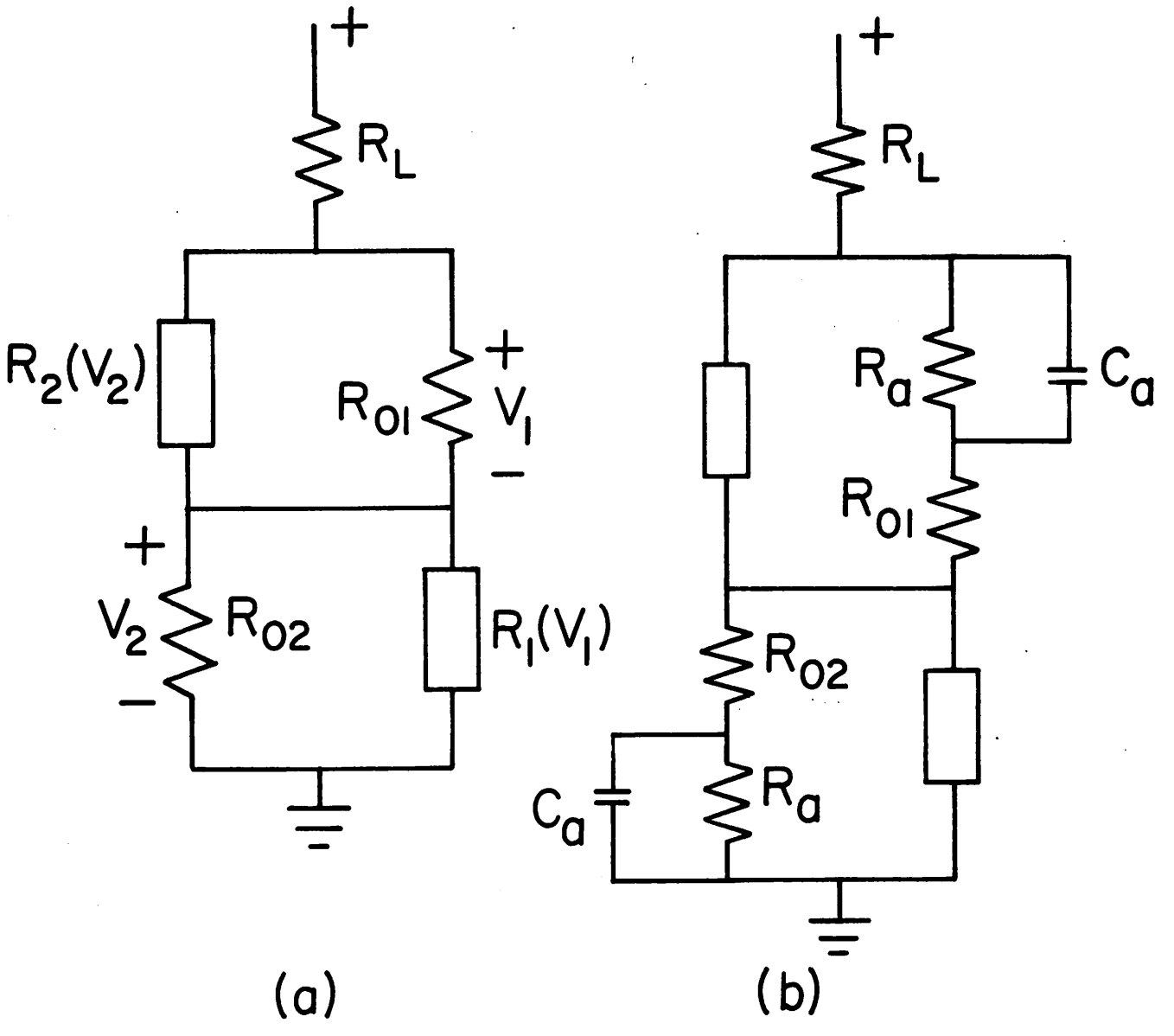

Fig. 7. Adding "memory" to a basic configuration.

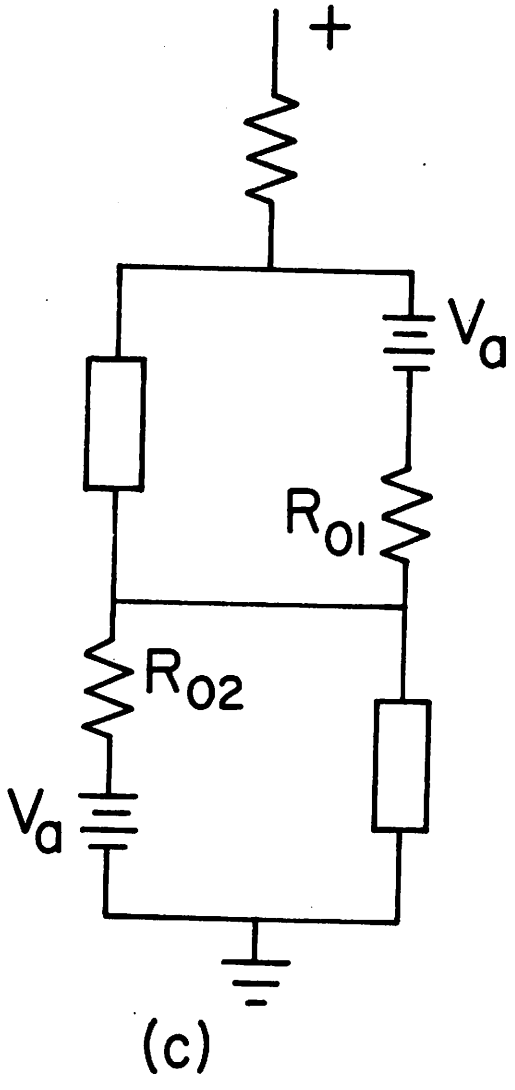

Fig. 7. (Cont'd.) Adding "memory" to a basic configuration.

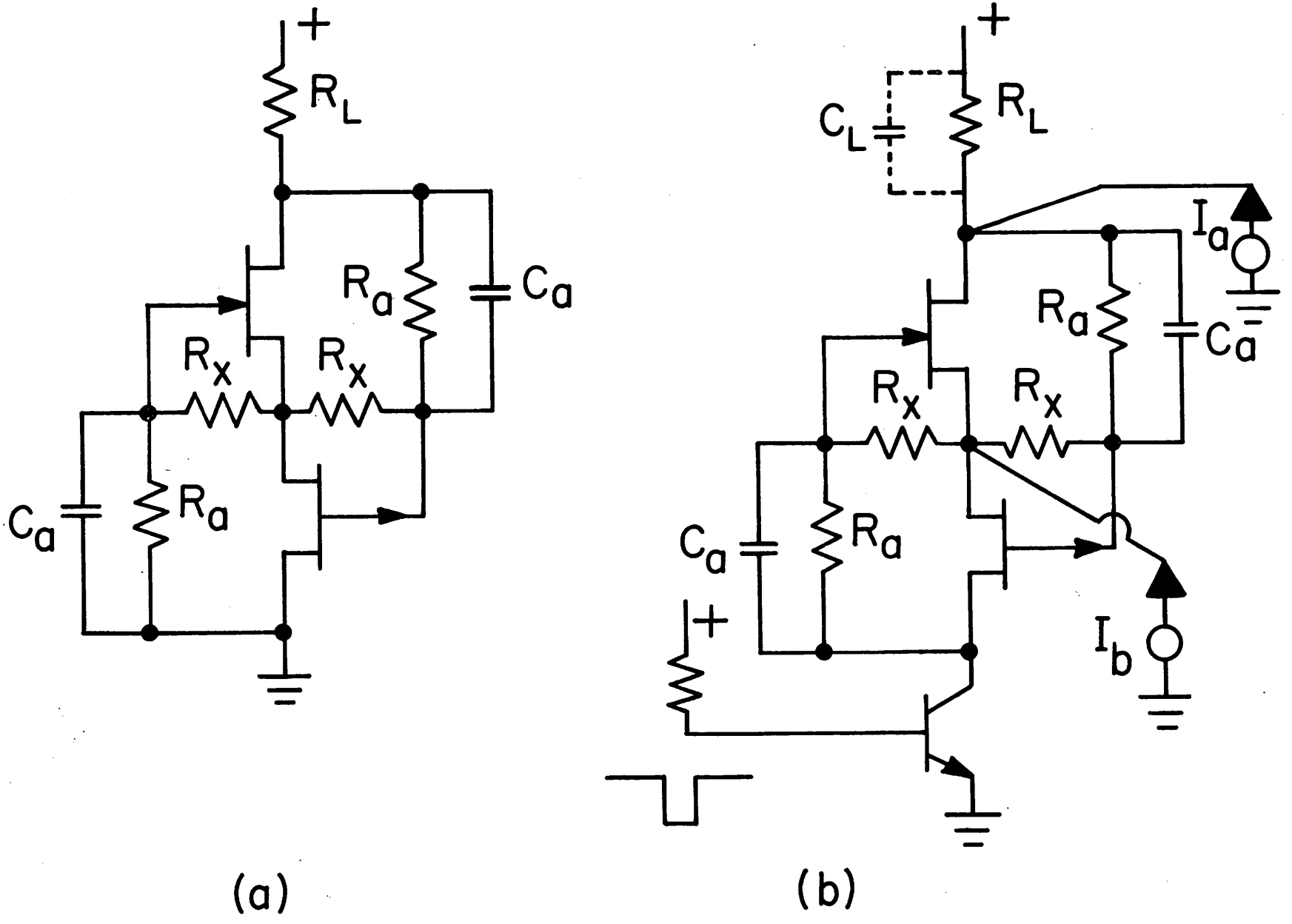

Fig. 8. Basic unipolar circuit--triggering techniques.

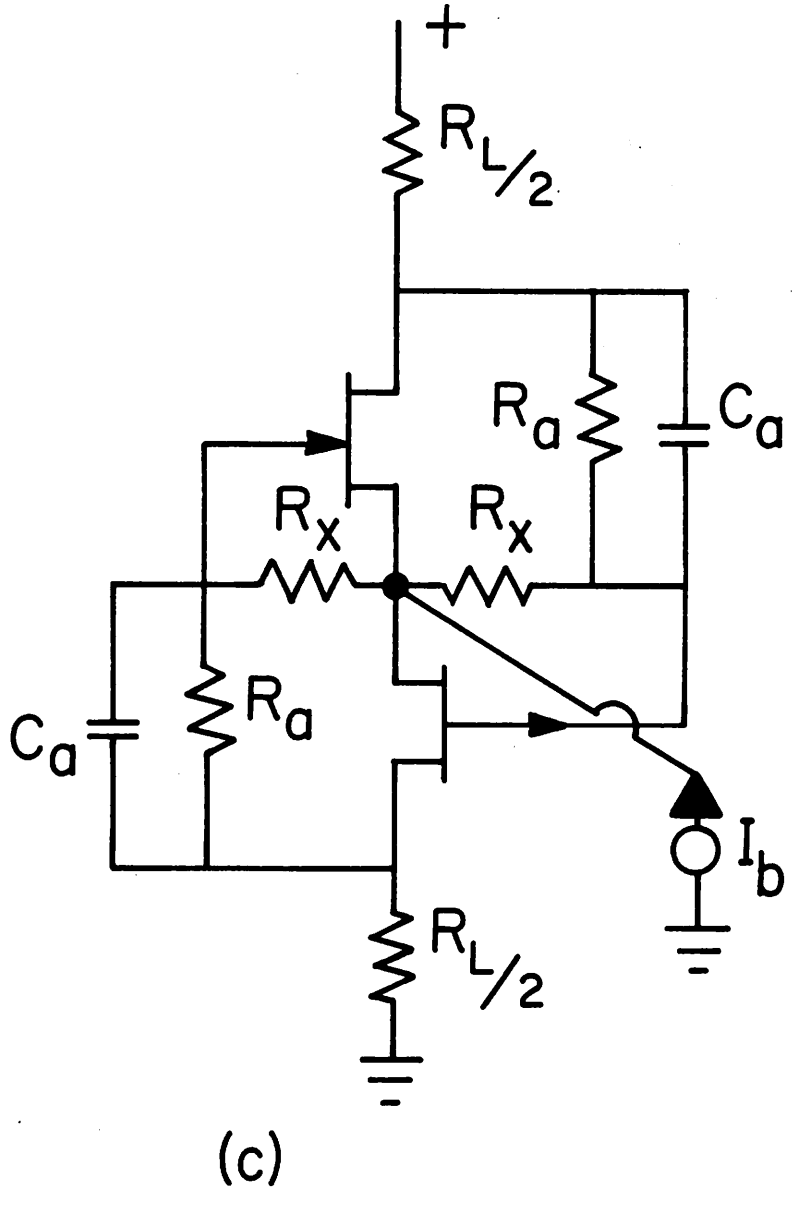

Fig. 8. (Cont'd.) Basic unipolar circuit--triggering techniques.

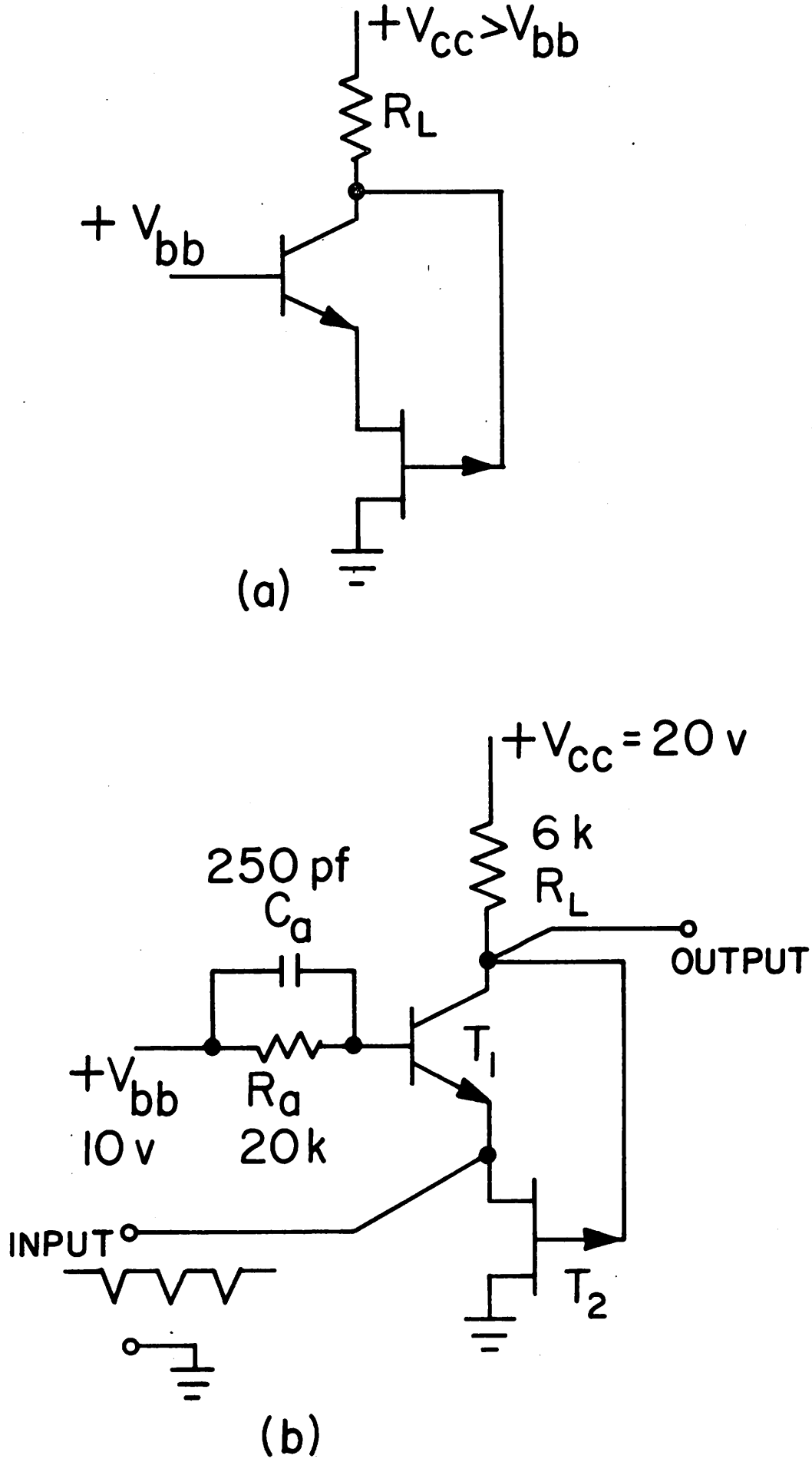

Fig. 9. Bipolar-unipolar counting circuit.

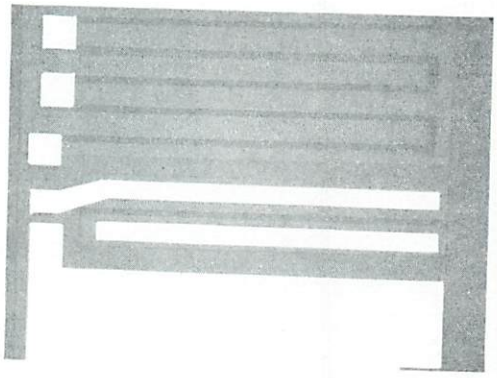

Fig. 10. Integrated realization of bipolar-unipolar circuit.