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THEORETICAL INVESTIGATION OF A NON-PLANAR FIELD EFFECT TRANSISTOR

by

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ABSTRACT

This report applies the generalized analysis of planar field-effect transistors developed by Richer* to the calculation of theoretical performance in a volume field-effect transistor. Richer's analysis is illustrated first, then the mathematical techniques are extended to cover the case of an arbitrarily-shaped volume FET. This extended general analysis is then applied to a FET with circular cylindrical-geometry. Graphs of computer solutions of FET drain-current, drain-voltage characteristics, and of equivalent-circuit element values are presented. The characteristics of the planar and cylindrical FET's are compared.

*Ira Richer, "Properties of an Arbitrarily Doped Field-Effect Transistor," Technical Report, Solid-State Electronics Laboratory, California Institute of Technology, May 1964.

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ACKNOWLEDGMENT

I thank Professor Richard Muller whose guidance, patience, and encouragement underlie this report. I also thank the Computer Center who provided the necessary time and much assistance.

I. INTRODUCTION

The motivation for this analysis of a volume field-effect transistor (FET) was the announcement by Zuleeg[1] of the successful construction of such a device. Shockley[2] had discussed the general properties of a volume FET in 1952, but a complete analysis of current dependence, channel profiles, and equivalent-circuit values for the device has not yet appeared. As in other FET analyses, calculations are made only in the region below pinch-off. The characteristics in the important drain-current saturation range are obtained by extension of the conditions at pinch-off.

In this paper we give a simple analysis for a volume FET of arbitrary cross-section. We begin by presenting Richer's[3] analysis of a planar FET. Richer has given a general analysis of a planar FET in which he demonstrates that the general characteristics of these devices are practically independent of doping profiles. The model taken is that of a depletion-mode device having an n-type channel and a p-type gate.

The FET's to be described consist of a block of n-type material to which is attached a block of p-type material called the gate. For useful device properties, the gate is much more highly doped than the channel.

When the p-n junction is reverse biased, the space-charge region penetrates the lower conductivity n-type region (Fig. 1). When a voltage V_D is placed on terminal 3, a current will flow in the undepleted portion of the n-type material. This region is called the channel. The carriers flow out of terminal 1, which is called the source, into terminal 3, which is called the drain. Because of the potential drop in the direction of current flow, the channel has the shape which is shown in Fig. 1. There are essentially no free carriers in the space-charge region, hence the drain current is determined by the shape of the charge-free channel.

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1. R. Zuleeg and V. O. Hinkle, "Multi-Channel Field-Effect Transistor," Sept. 1964, presented at the 1964 Electronic Devices Meeting, Oct. 28-31, Washington, D.C.
2. W. Shockley, "A Unipolar Field-Effect Transistor," Proc. IRE, 40, 1365 (1952).
3. Ira Richer, "Properties of an Arbitrarily Doped Field-Effect Transistor," Technical Report, Solid-State Electronics Laboratory, California Institute of Technology, May 1964.

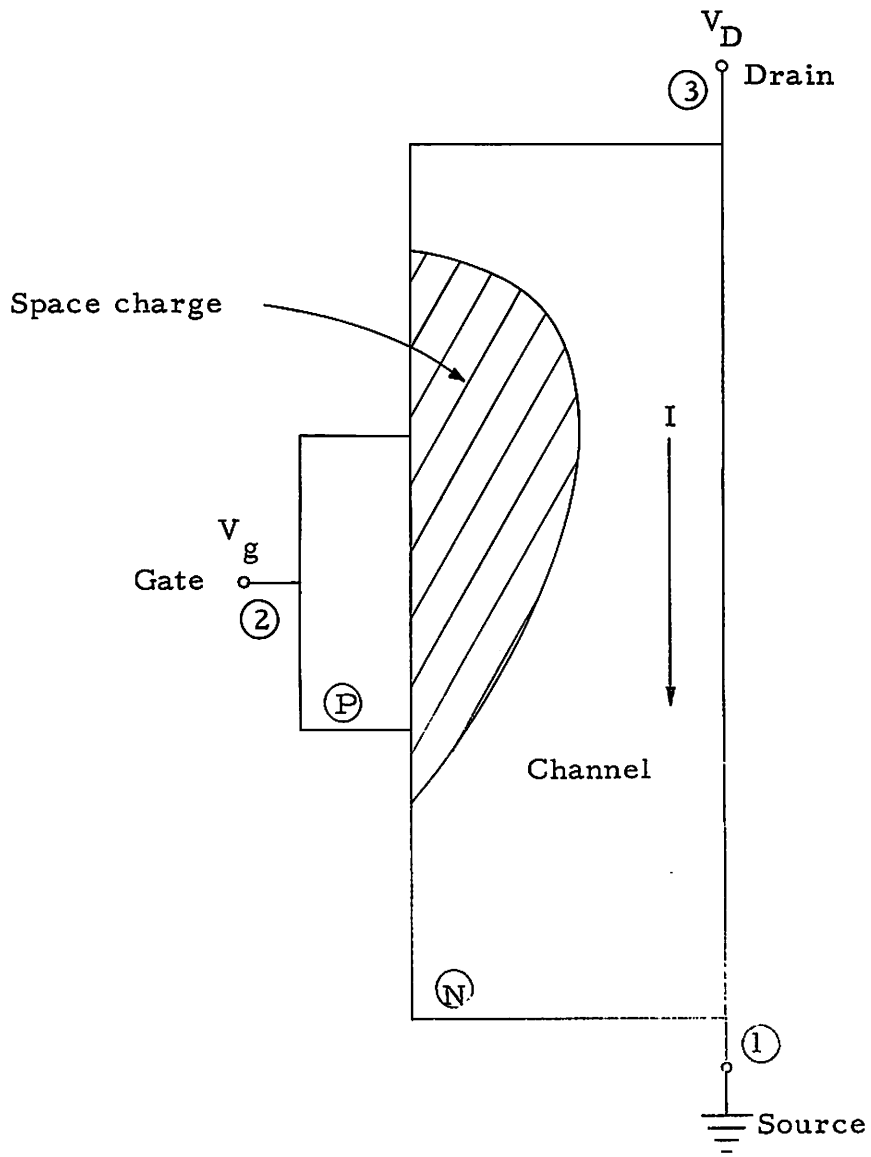


Fig. 1. Section of a planar field-effect transistor.

Mathematical analysis will be carried out on two types of field-effect transistors. The first type is the one-dimensional FET sketched in Fig. 1. The second type consists on an n-type region completely surrounded by a p-type gate, which we designate a volume FET. In considering volume FET's, the general analysis for an arbitrary cross-section will be discussed, and the detailed solutions for a right-circular cylindrical geometry will be given. The goal of the analysis is to obtain an equivalent circuit for these devices.

In Sec. II, we cover the analysis for a planar FET. Sections III and IV contain a discussion of the analysis for an arbitrary cross-section volume FET and the detailed analysis for a cylindrical volume geometry FET respectively. In Sec. V, we compare our results for the planar and the cylindrical volume FET's.

II. ANALYSIS OF A PLANAR FET

In this section the one-dimensional planar FET is analyzed. The analysis is due entirely to Richer[3] and is repeated here for illustrative purposes. The model to be used is sketched in Fig. 2. To simplify the analysis, Richer makes the following assumptions.

1. The doping profile is specified as:

$$e(N_d - N_a) = +\rho_0 \qquad \text{in n-type region}$$

$$e(N_d - N_a) = -K\rho_0 \qquad \text{in gate region}$$

where $K \gg 1$, N_d is the donor density and N_a is the acceptor density. Thus, the gate conductivity is much greater than the channel conductivity. Therefore, when the p-n junction is reverse biased, essentially all of the space-charge region appears in the channel.

2. The built-in potential at the junction will be neglected when compared to the applied bias.
3. Carrier mobility is constant.
4. Drain current is carried only by majority carriers (electrons for the profile given in assumption 1).
5. Gate current is negligible.
6. The boundary between the gate and the channel is sharp. No current flows in the depletion region since there is no mobile charge present.
7. In the channel region

$$|E_x| \ll |E_z|$$

$$|E_y| \ll |E_z|$$

By this it is meant that in the x-y plane there is no appreciable voltage drop and hence uniform current density across the channel.

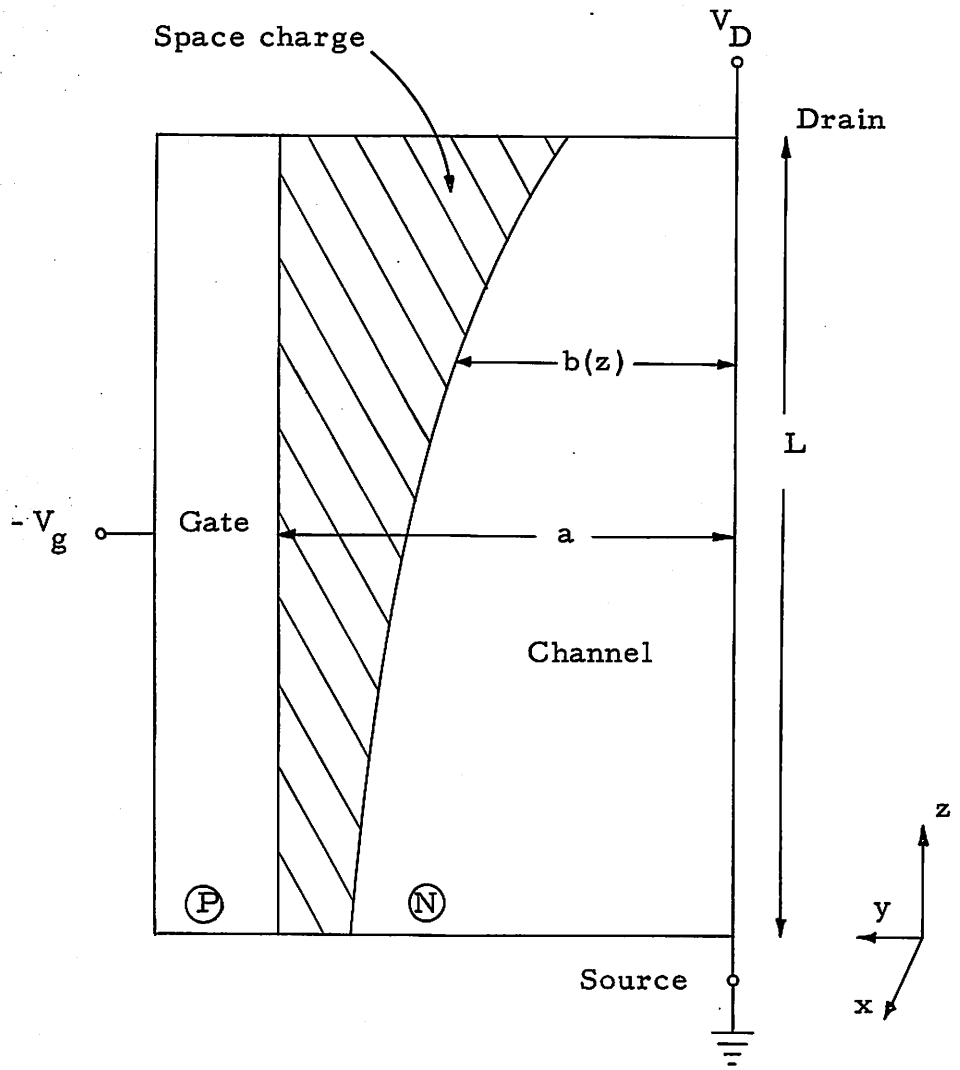


Fig. 2. Model for the analysis of a planar field-effect transistor.

8. In the space-charge region

$$\left|\frac{\partial E_z}{\partial z}\right| \ll \left|\frac{\rho}{\epsilon}\right|$$

where ϵ is permittivity of the material.

Assumption 8 says that the channel shape does not change rapidly with increasing z. Such an assumption is obviously true when $V_D \approx 0$ since then the width of the channel is approximately uniform. We assume here that the assumption holds even when V_D is not small. Assumption 8 is called the "gradual approximation" since it implies that the channel width does not change rapidly in the z direction.

Richer shows in some detail that these eight assumptions are valid for virtually all types of commercial FET's. We now proceed with the analysis.

Consider the potential $V(z,y)$ at some point z,y in the space-charge region. There the potential satisfies Poisson's equation,

$$\frac{\partial^2 V}{\partial y^2} = -\frac{\rho_0}{\epsilon} \tag{1}$$

At the channel edge of the space-charge region, the electric field is zero; thus,

$$E_y = -\frac{\partial V}{\partial y} = 0 \qquad \text{at} \quad y = b(z)$$

and at the gate edge the potential is V_g.

Integrating Eq. (1) under the above boundary conditions, we obtain the potential in the space-charge region,

$$V(z,y) = V_g + \frac{\rho_0}{2\epsilon}\left[(a - b(z))^2 - (y - b(z))^2\right] \qquad \text{where} \quad b(z) \leq y \leq a$$

Because of assumption 7 we see that there can be no potential drop across the channel. Therefore, the potential at any point within the channel is equal to the potential at the channel-space charge boundary; hence

$$V(z,b) = V_g + V_{pp}\left[1 - \frac{b(z)}{a}\right]^2 \qquad 0 \leqq y \leqq b(z) \qquad (2)$$

is the potential in the channel where

$$V_{pp} = \frac{\rho_0 a^2}{2\epsilon}$$

From Eq. (2), if $b = 0$, $V(z,b) - V_g = V_{pp}$. Another way of viewing this is that if the potential V_{pp} is placed across the gate-channel junction, the channel width becomes zero. Hence, the potential V_{pp} causes the channel to become pinched off.

We now define several normalized parameters as follows:

$$u(z) = \frac{b(z)}{a}$$

$$V_{gn} = \frac{|V_g|}{V_p}$$

$$V_{Dn} = \frac{V_D}{V_p}$$

$$d = \frac{|V_D - V_g|}{V_p}$$

Since we are concerned with operation only as a depletion mode device, V_g will always be negative.

In terms of the newly-defined variables, Eq. (2) becomes

$$\frac{V(z,b)}{V_{pp}} = -V_{gn} + (1 - u)^2 \tag{3}$$

Consider a differential element of channel having length dz. The resistance between z and z + dz planes is

$$dR = \frac{dz}{\mu\rho_0 bD} = \frac{1}{\mu\rho_0 aD}\frac{dz}{u}$$

where D is the width of the device in the X direction and μ is the mobility of the majority carriers in the channel.

The voltage drop across the element is -dV which is calculated from Eq. (3); accordingly

$$-dV = 2V_{pp}(1 - u)\, du$$

therefore

$$I = \frac{dV}{dR} = -2G_{op}LV_{pp}\, u(1 - u)\frac{du}{dz} \tag{4}$$

where

$$G_{op} = \frac{\mu\rho_0 aD}{L}$$

Since we have no current flow from channel to gate, I is not a function of z. Therefore, we can easily integrate Eq. (4).

From Eq. (3), we can obtain the proper boundary values; thus

$$u(0) = 1 - \sqrt{V_{gn} + \frac{V(0,b)}{V_{pp}}} = 1 - \sqrt{V_{gn}} \qquad V(0,b) = 0$$

and

$$u(L) = 1 - \sqrt{V_{gn} + \frac{V(L,b)}{V_{pp}}} = 1 - \sqrt{\frac{V_D - V_g}{V_{pp}}} = 1 - \sqrt{d}$$

The minus sign in the equation for $u(L)$ occurs because V_{gn} was defined as the absolute value of V_g/V_p but V_g is always negative.

Now we integrate Eq. (4):

$$\int_0^L I\, dz = -2G_{op}\, L\, V_{pp} \int_{1-\sqrt{V_{gn}}}^{1-\sqrt{d}} u(1 - u)\, du$$

therefore

$$I_{Dp} = \frac{I_{op}}{3}\left[(1 - \sqrt{V_{gn}})^2\,(1 + 2\sqrt{V_{gn}}) - (1 - \sqrt{d})^2\,(1 + 2\sqrt{d})\right] \qquad (5)$$

where $I_{op} = G_{op}V_{pp}$.

$I_{op}/3$ is the maximum current that can flow in this FET ($V_g = 0$). Given a block of semiconductor of conductance G_{op}, a current I_{op} will flow when a voltage V_{pp} is applied across it. In the FET however, the presence of the space-charge region limits the current to $I_{op}/3$. At this current, the FET is saturated and an increase in voltage will not change the current. Hence $I_{op}/3$ is the maximum current that can flow in the planar FET. A plot of normalized drain current $(3I_{Dp}/I_{op})$ versus normalized drain voltage is shown in Fig. 3.

Now we find the expression for the channel shape by integrating Eq. (4) to some point z along the channel.

$$I\,\frac{z}{L} = \frac{I_{op}}{3}\left[(1 - \sqrt{V_{gn}})^2\,(1 + 2\sqrt{V_{gn}}) - u^2(3 - 2u)\right]$$

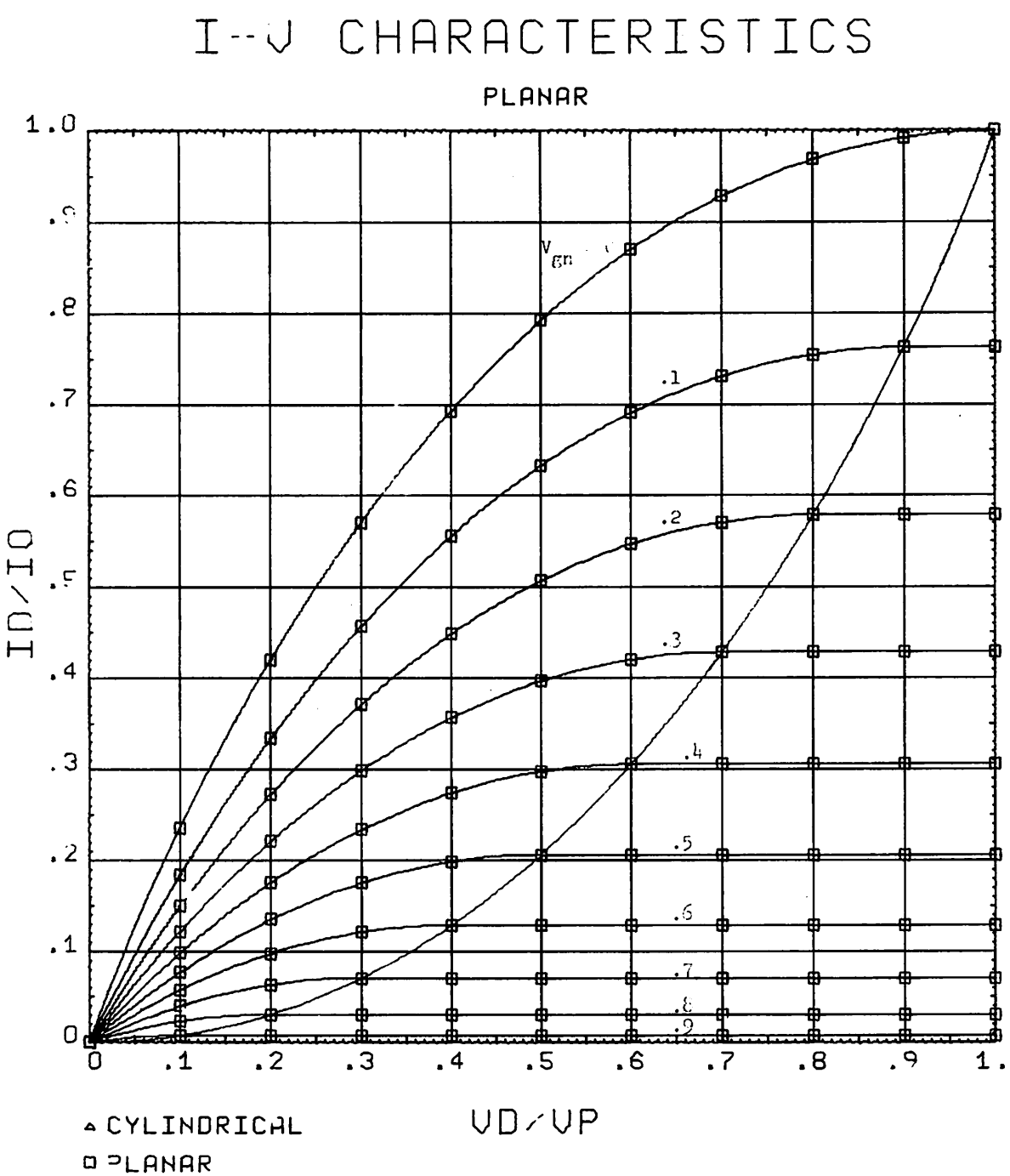


FIG. 3. NORMALIZED DRAIN CURRENT VS NORMALIZED DRAIN VOLTAGE FOR A PLANAR FET.

Combining this expression with Eq. (5) we find that

$$\frac{z}{L} = \frac{(1 - u)^2 (1 + 2u) - V_{gn}(3 - 2\sqrt{V_{gn}})}{d(3 - 2\sqrt{d}) - V_{gn}(3 - 2\sqrt{V_{gn}})} \tag{6}$$

Equation (6) gives the relationship between z and u as a function of the applied bias. Thus, we have an expression for the location of the channel edge for any combination of normalized gate and drain voltages.

Now we turn our attention to the small signal equivalent circuit. First, we derive the forward transconductance and output conductance. These are calculated easily from Eq. (5);

$$g_m = \left|\frac{\partial I_{Dp}}{\partial V_g}\right| = G_{op}(\sqrt{d} - \sqrt{V_{gn}}) \tag{7a}$$

$$G_{22} = \left|\frac{\partial I_{Dp}}{\partial V_D}\right| = G_{op}(1 - \sqrt{d}) \tag{7b}$$

Alternatively, we may calculate normalized g_m and G_{22} as follows,

$$g_m = \left|\frac{\partial I_{Dnp}}{\partial V_{gn}}\right| = 3(\sqrt{d} - \sqrt{V_{gn}}) \tag{8a}$$

$$G_{22} = \left|\frac{\partial I_{Dnp}}{\partial V_{Dn}}\right| = 3(1 - \sqrt{d}) \tag{8b}$$

where $I_{Dnp} = 3I_{Dp}/I_{op}$.

It will be useful in later discussions to have g_m and G_{22} defined in this way. Figure 4 shows normalized g_m versus V_{gn} and Fig. 5 shows normalized G_{22} versus V_{Dn}.

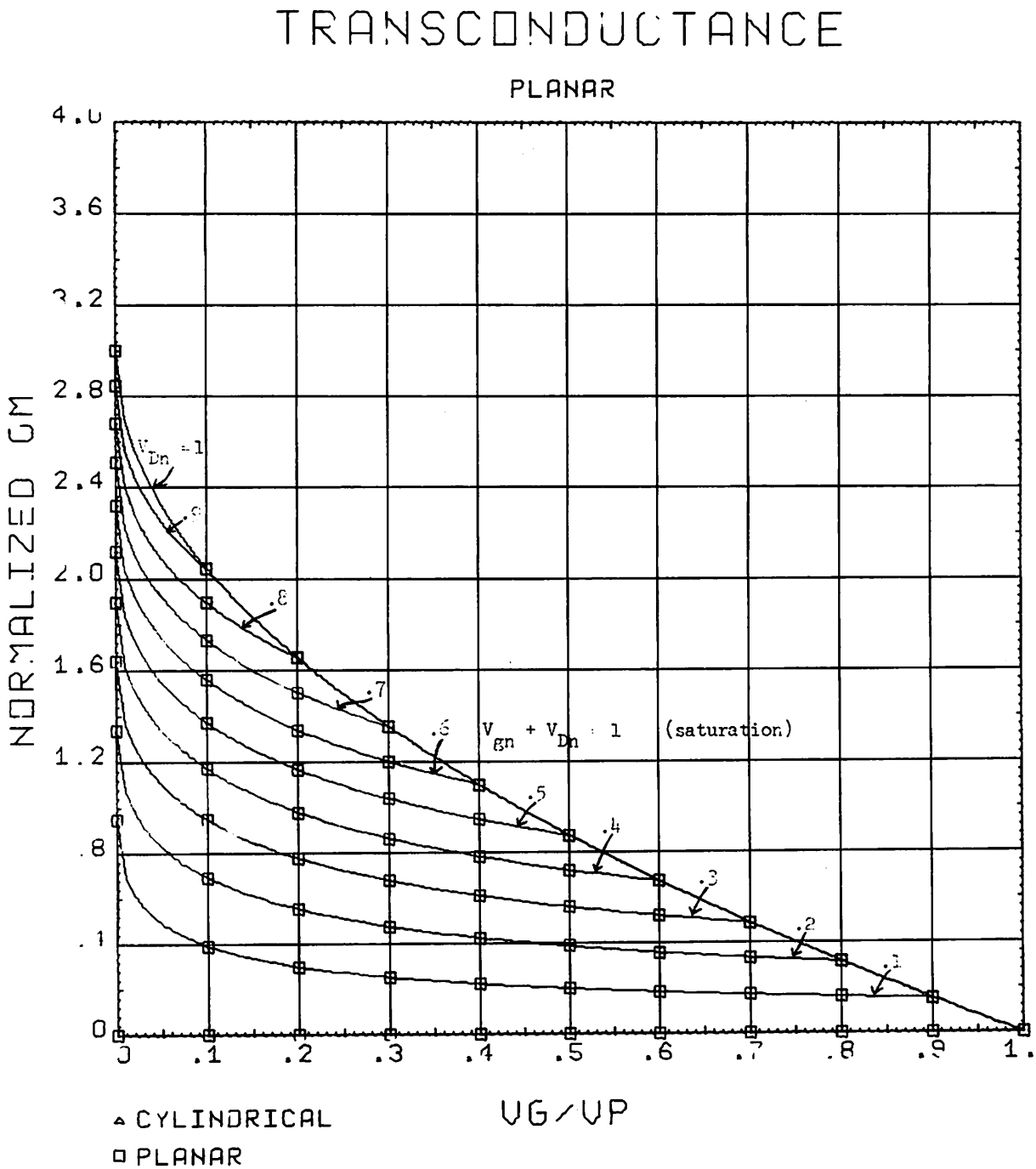


FIG. 4. NORMALIZED g_m VS NORMALIZED GATE VOLTAGE FOR A PLANAR FET (Maximum Drain Current Normalized to Unity).

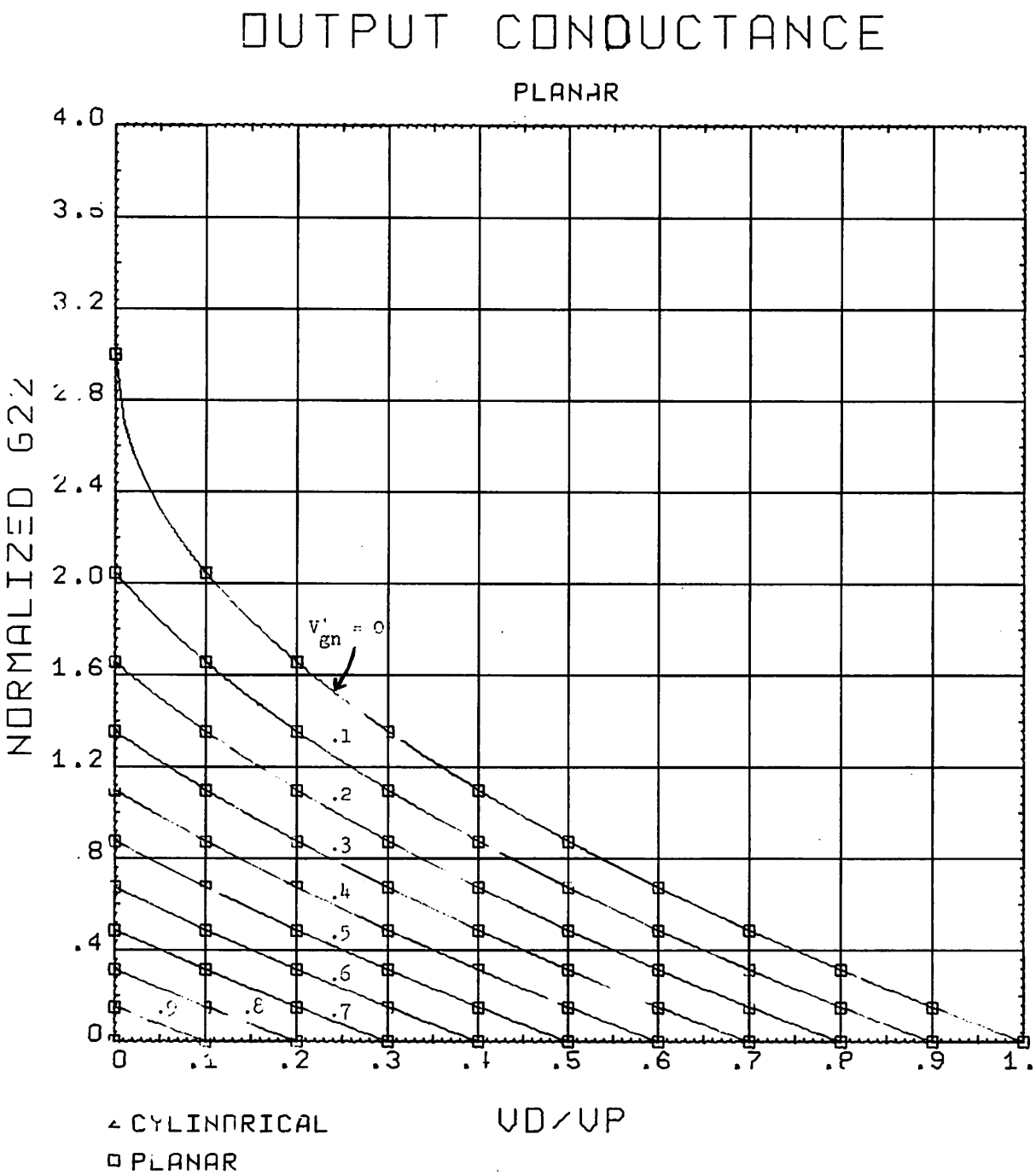


FIG. 5. NORMALIZED G_{22} VS NORMALIZED DRAIN VOLTAGE FOR A PLANAR FET (Maximum Drain Current Normalized to Unity).

The remaining elements to be derived are capacitive. Richer defines short circuit input "charge-capacitance" and output "charge-capacitance" as follows,

$$C_{11}^{*} = \left| \frac{dQ}{dV_g} \right| \tag{9a}$$

$$C_{22}^{*} = \left| \frac{dQ}{dV_d} \right| \tag{9b}$$

where dQ/dV is the voltage rate of change of charge in transit between source and drain. Actually, $C_{11}^{*} = -dq_{in}/dV_q$, where q_{in} is the charge placed on gate. However, for every element of charge that is placed on the gate, an equal amount of charge goes into the space-charge region from the channel; thus

$$\frac{dq_{in}}{dQ} = -1$$

or

$$C_{11}^{*} = \frac{dq_{in}}{dV_g} \cdot \frac{dQ}{dq_{in}} = \left| \frac{dQ}{dV_g} \right|$$

Richer shows in some detail that C_{11}^{*} is identical to the "real" short circuit input capacitance, Eq. (10a), and that C_{22}^{*} is that fraction of C_{22} that appears between source and drain.

$$C_{11} = \frac{1}{\omega} \cdot \frac{1}{V_g} \left[\text{quadrature component of } i_g \right]_{V_D=0} \tag{10a}$$

$$C_{22} = \frac{1}{\omega} \cdot \frac{1}{V_g} \left[\text{quadrature component of } i_D \right]_{V_g=0} \tag{10b}$$

Since we have a uniformly doped channel, the charge is simply proportional to the channel volume; thus

$$Q = \rho_0 aDL \left[u(L) + \int_{u(L)}^{u(0)} \frac{z}{L}\, du \right]$$

$$= \frac{\rho_0 aDL}{2} \left[1 + 3\, \frac{d(1 - \sqrt{d})^2 - V_{gn}(1 - \sqrt{V_{gn}})^2}{d(3 - 2\sqrt{d}) - V_{gn}(3 - 2\sqrt{V_{gn}})} \right] \tag{11}$$

Application of Eqs. (9a) and (9b) yields the desired capacitances as follows,

$$C_{11}^* = C_0^*(\sqrt{d} + \sqrt{V_{gn}})\, \frac{(1 - \sqrt{d})^2 + 4(1 - \sqrt{d})(1 - \sqrt{V_{gn}}) + (1 - \sqrt{V_{gn}})^2}{\left[3(\sqrt{d} + \sqrt{V_{gn}}) - 2(d + \sqrt{dV_{gn}} + V_{gn})\right]^2} \tag{12a}$$

$$C_{22}^* = C_0^*(\sqrt{d} + \sqrt{V_{gn}})\, \frac{(1 - \sqrt{d})^2 + 2(1 - \sqrt{d})(1 - \sqrt{V_{gn}})}{\left[3(\sqrt{d} + \sqrt{V_{gn}}) - 2(d + \sqrt{dV_{gn}} + V_{gn})\right]^2}$$

$$+ C_0^*(\sqrt{d} - \sqrt{V_{gn}})\, \frac{(1 - \sqrt{d})(1 - \sqrt{V_{gn}})}{\left[3(\sqrt{d} + \sqrt{V_{gn}}) - 2(d + \sqrt{dV_{gn}} + V_{gn})\right]^2} \tag{12b}$$

where

$$C_0^* = 3\epsilon D\, \frac{L}{a}$$

In our model, the source and drain are indistinguishable so that

$$C_{dg}^* = C_{sg}^*$$

also

$$C^*_{sg} = (C^*_{11} - C^*_{dg})$$

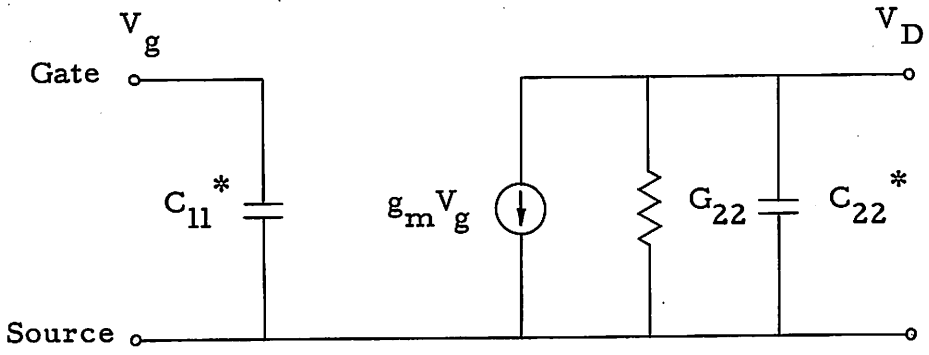
$$C^*_{dg} = (C^*_{11} - C^*_{sg})$$

therefore $C^*_{11} = 2C^*_{dg}$. Richer shows that when $V_d = 0$

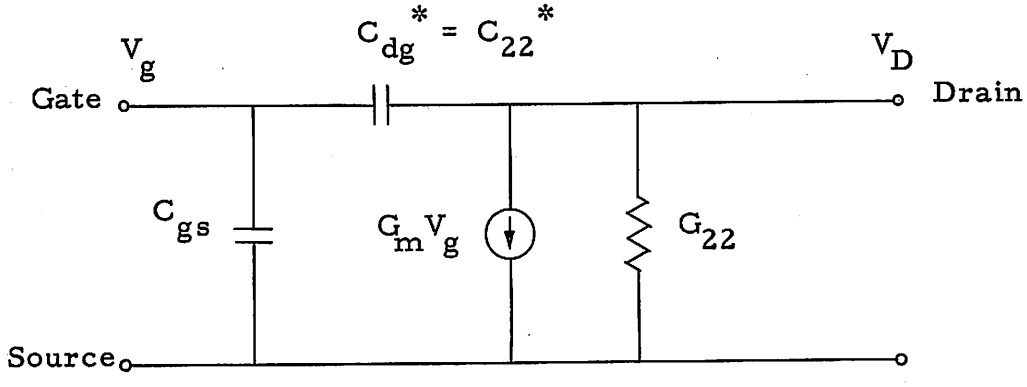
$$C^*_{22} = \frac{C^*_{11}}{2}$$

Based on the above discussion, Richer postulates the equivalent circuit shown in Fig. 6.

We will now extend the method illustrated above to cover the case of an arbitrary shape for the FET.



General Circuit



Modified Circuit

Fig. 6. Equivalent circuit for a FET.

III. GENERAL ANALYSIS

In this section an analysis, similar to the above, is presented for a volume field-effect transistor of arbitrary cross section. The model to be used is shown in Fig. 7. This analysis is still first order and retains all of the assumptions specified at the beginning of Sec. II.

Since the p-type gate is much more highly doped than the n-type bulk, we show the gate only as the boundary of the n-type region. Point O represents the point to which the channel converges as one approaches the pinch-off condition. Line C represents the boundary between the channel and space-charge region and hence must be an equipotential line. A Represents the area of the channel. We may define the $\mathcal{J}$ axis by an arbitrary straight line passing through point O. The boundary between the gate and the space-charge region intersects the $\mathcal{J}$ axis at W. We assume that W is not a function of z, i.e., that the FET is cylindrical but not necessarily circular. The equipotential line C intersects the $\mathcal{J}$ axis at $\mathcal{J}_1$. At this time we define $x_1 = \mathcal{J}_1/W$, where $0 \leq x_1 \leq 1$.

In terms of the new variable, the equipotential line C intersects the $\mathcal{J}$ axis at x_1. From the uniqueness theorem we know that only one equipotential line can pass through point x_1. Thus the channel area must be definable as a function of x_1 only.

We define the potential in the channel (along the equipotential line C) as $v(x_1)$, where $v(1) = 0$. Again, by the uniqueness theorem, the channel voltage is a function of x_1 only. We may now define a potential $V(x_1)$ as follows,

$$V(x_1) = V_g + v(x_1) \tag{13}$$

where V_g is the gate voltage usually referred to the source.

We define the pinch-off voltage V_p as the voltage drop across the space-charge region when $x_1 = 0$; thus

$$V_p = v(0) = V(0) - V_g$$

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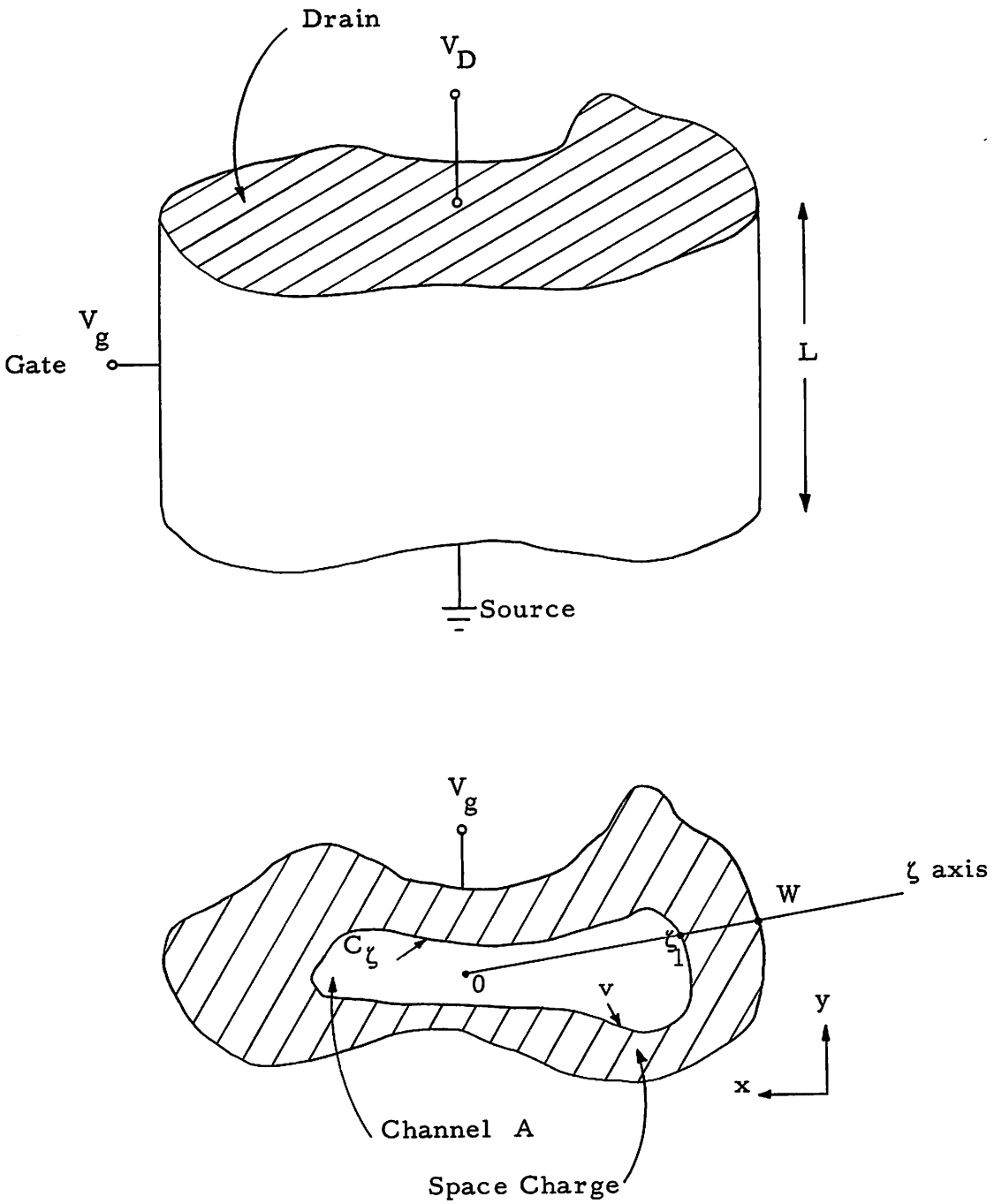

Arbitrary cross section FET

Fig. 7. Model of a volume FET.

Another way of viewing this is that when $V - V_g = V_p$ (the channel has zero area), it is pinched off.

It is not always easy to solve Poisson's equation for an arbitrarily shaped FET. The problems involved in the solution are discussed at the end of this section. For the present, let us assume that we have both $v(x_1)$ and $A(x_1)$ and proceed.

Consider an element of channel having length dz. Then we calculate that

$$dR = \frac{dz}{\mu\rho_0 A(x_1)} \tag{14}$$

From Eq. (13) we have

$$\frac{dV}{dx_1} = \frac{dv}{dx_1} = v'(x_1) \tag{15}$$

To obtain an expression for drain current, we calculate

$$\int_0^L I\, dz = v'(x_1)\, \mu\rho_0 A(x_1)\, dx_1 = \int_{X_1}^{X_2} \mu\rho_0 v'(x_1)\, A(x_1)\, dx$$

where we have defined the quantities

$$X_1 = x_1(z = 0)$$

$$X_2 = x_1(z = L)$$

therefore

$$I = \frac{\mu\rho_0}{L} \int_{X_1}^{X_2} v'(x_1)\, A(x_1)\, dx_1 \tag{16}$$

To find a relationship between the channel-edge (x_1) and z, we integrate the current to an arbitrary z.

$$\int_0^z I\, dz = \mu\rho_0 \int_{X_1}^{x_1(z)} v'(x_1)\, A(x_1)\, dx_1$$

Combining this form with Eq. (16), we find that

$$\frac{z}{L} = \frac{\displaystyle\int_{X_1}^{x_1(z)} v'(x_1)\, A(x_1)\, dx_1}{\displaystyle\int_{X_1}^{X_2} v'(x_1)\, A(x_1)\, dx_1} \tag{17}$$

To find the small signal circuit elements, we proceed as in the planar case. Although V_g and V_D do not appear explicitly in Eq. (16), X_1 and X_2 are functions of V_g and V_D.

$$g_m = \left|\frac{\partial I}{\partial V_g}\right| = \frac{\mu\rho_0}{L}\left|\frac{\partial}{\partial V_g}\left[\int_{X_1}^{X_2} v'(x_1)\, A(x_1)\, dx_1\right]\right| \tag{18a}$$

Similarly, we have that

$$G_{22} = \left|\frac{\partial I}{\partial V_D}\right| = \frac{\mu\rho_0}{L}\left|\frac{\partial}{\partial V_D}\left[\int_{X_1}^{X_2} v'(x_1)\, A(x_1)\, dx_1\right]\right| \tag{18b}$$

As in the planar case, we find that

$$C_{11}^* = \left|\frac{dQ}{dV_g}\right|, \qquad C_{22}^* = \left|\frac{dQ}{dV_D}\right|$$

where $Q = \rho_0$ (volume of the channel); thus

$$Q = \rho_0 \int_{A(X_1)}^{A(X_2)} A(x_1)\, dz$$

We have found an implicit relationship between z and x_1 in Eq. (17). Let us say that $x_1 = f_1(z)$; then

$$Q = \rho_0 \int_0^L A(f_1(z))\, dz \tag{19}$$

The capacitances can then be calculated in a straightforward manner by means of derivatives, as in the planar case.

This completes the general analysis. For all but the simplest geometries, the above functions will be tables of numbers and the specified integrations and differentiations must be carried out numerically.

As mentioned earlier, Poisson's equation for arbitrary shapes cannot be solved in a straightforward manner. Two distinct problems are encountered when trying to calculate $v(x_1)$ and $A(x_1)$. The first is the numerical solution of Poisson's equation given the two boundaries, their respective boundary values, and the charge distribution between them. Computer programs have been written to solve these mixed boundary value problems (one boundary specified in terms of potential and the other in terms of gradient) using relaxation methods. Setting up this problem for an arbitrary shape is not straightforward and the convergence of a solution procedure cannot always be guaranteed.

The second problem arises when we realize that the location of only the outer boundary is known at the start of the problem. The inner boundary is specified only as an equipotential and one must guess at its initial location. The problem is now one of trying to find the exact shape and location of the inner boundary by solving Poisson's equation until this inner boundary is an equipotential line. There is

no assurance of convergence in general because the charge distribution is a function of the shape of the inner boundary. So far as has been determined by this author, each geometry must be considered separately, and no guaranteed solution techniques are available.

IV. CYLINDRICAL GEOMETRY

One geometry that can be used to illustrate the general analysis given in the previous section is that of a circular-cylindrical FET. For this geometry, $v(\mathcal{Y})$ becomes $v(r)$ and can be found by application of Gauss' Law (Fig. 8).

$$2\pi\epsilon r E_r = \rho_0 \pi (r^2 - r_1^2) \tag{20}$$

The boundary condition is that $V = V_g$ at r_2. We want to calculate the potential at $r = r_1$ since this is the potential in the channel. Integrating Eq. (20) we find

$$V = \frac{\rho_0}{2\epsilon}\left[r_1^2 \ln r_1 - \frac{r_1^2}{2} - r_1^2 \ln r_2 + \frac{r_2^2}{2}\right] + V_g$$

Again, we let x_1 be the normalized variable

$$x_1 = \frac{r_1}{r_2}$$

We simplify the expression for V,

$$V(x_1) = V_g + \frac{\rho_0 r_2^2}{4\epsilon}\left(x_1^2 \ln\left(\frac{x_1^2}{e}\right) + 1\right) \tag{21}$$

When $x_1 = 0$

$$V - V_g = \frac{\rho_0 r_2^2}{4\epsilon} = V_{pc} \tag{22}$$

Equation (22) defines the pinch-off voltage for the cylindrical geometry.

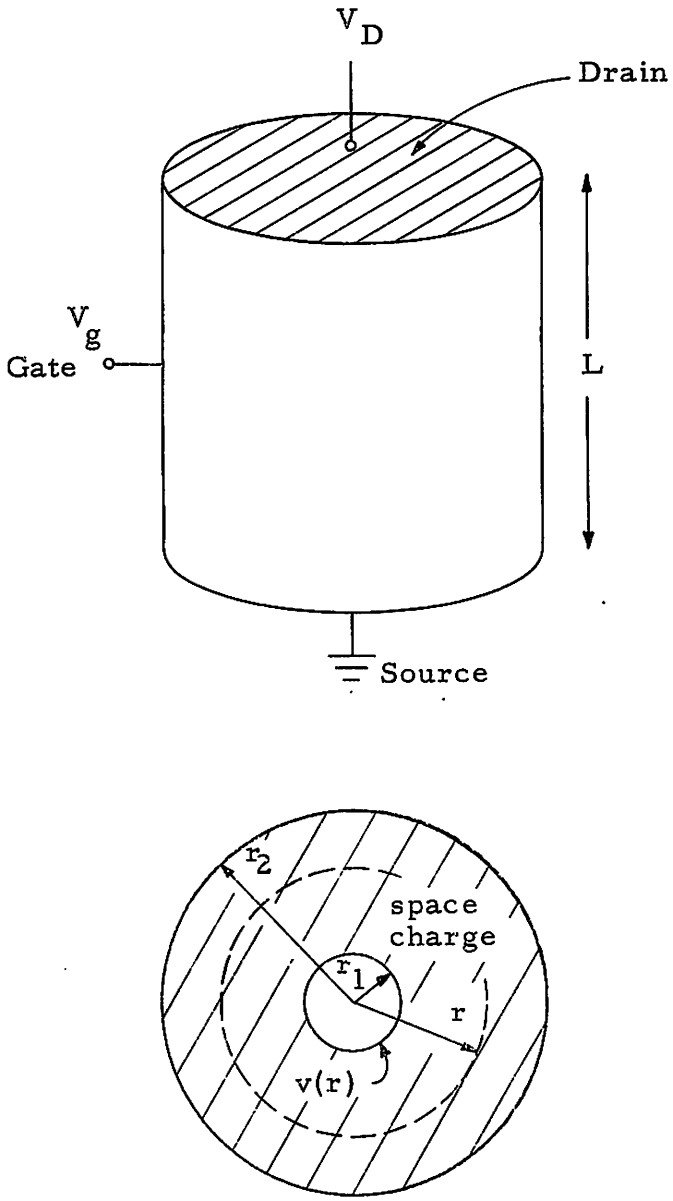

Fig. 8. Model for a cylindrical volume FET.

Looking at an element of channel dz, we calculate

$$dR = \frac{dz}{\mu \rho_0 \pi r_2^2 x_1^2}$$

From Eq. (21) we find

$$-dV = 4V_{pc}\, x_1 \ell n\, x_1$$

therefore

$$I = \frac{dV}{dR} = -4V_{pc}\, G_{oc}\, L\, x_1^3 \ell n\, x_1 \frac{dx_1}{dz}$$

where

$$G_{oc} = \frac{\mu \rho_0 \pi r_2^2}{L}$$

is the conductance in the absense of any biases. Therefore

$$\int_0^L I\, dz = -4V_{pc}\, G_{op}\, L \int_{X_1}^{X_2} x^3 \ell n\, x\, dx \qquad (23)$$

To find the boundary conditions for the right hand side of Eq. (23), we must solve for x_1 at the source and the drain. We have the relationship (Eq. (21)) between x_1 and the potential in the channel. We know that at the source, $V = 0$, and at the drain $V = V_D$. We call the value of x_1 at the source, X_1, and the value of x_1 at the drain, X_2. Rewriting Eq. (21) at the source and drain, we find

$$V_{gn} = X_1^2 \ell n \left(\frac{X_1^2}{e}\right) + 1 \qquad z = 0$$

$$V_{gn} + V_{Dn} = X_2^2 \ell n \left(\frac{X_2^2}{e}\right) + 1 \qquad z = L$$

It should now be clear that we cannot solve for X_1 and X_2 directly since this involves the solution of a transcendental equation. We will derive all of our expressions in terms of X_1 and X_2, leaving it to the computer to substitute the numerical values when we evaluate the final expressions.

Carrying out the integration in Eq. (23) we find

$$I_{Dc} = \frac{I_{oc}}{4}\left[(X_2^4 - X_1^4) + 4(X_1^4 \ell n\, X_1 - X_2^4 \ell n\, X_2)\right] \tag{24}$$

where

$$I_{oc} = V_{pc}\, G_{oc} \tag{25}$$

We notice that for the cylindrical geometry, the presence of the gate limits the current to one-fourth its maximum, were there no gate present. This result will be compared with the planar FET in the next section. A plot of normalized drain current $(4_{IDc}/I_{oc})$ versus normalized drain voltage (V_D/V_p) is shown in Fig. 9.

By integrating Eq. (23) to an arbitrary x_1 and combining this result with Eq. (24) we can calculate the relationship between x_1 and z.

$$\frac{z}{L} = \frac{x_1^2(\frac{1}{4} - \ell n\, x_1) - X_1^4(\frac{1}{4} - \ell n\, X_1)}{X_2^4(\frac{1}{4} - \ell n\, X_2) - X_1^4(\frac{1}{4} - \ell n\, X_1)} \tag{26}$$

Again this gives us the channel shape versus applied bias.

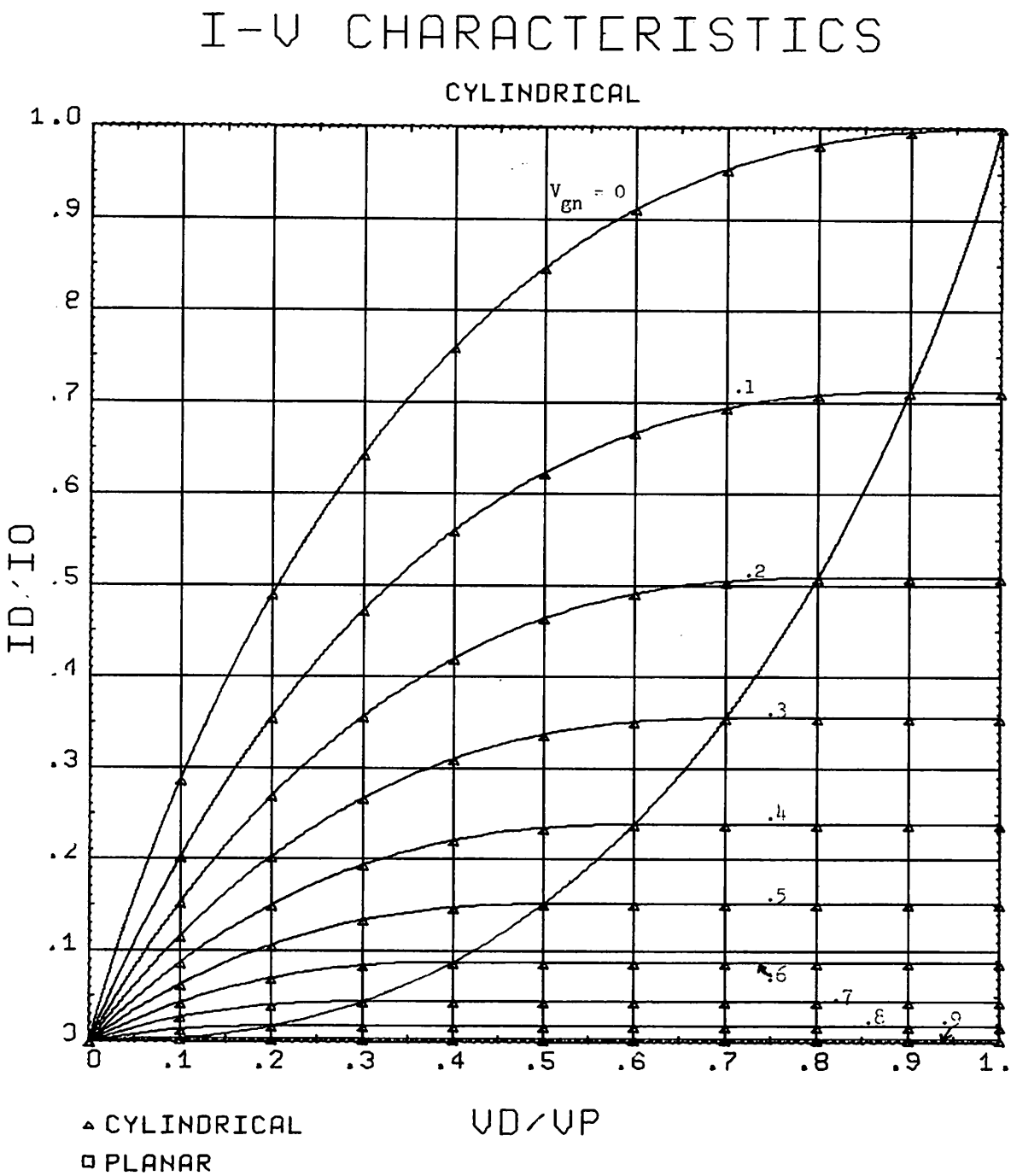

FIG. 9. NORMALIZED DRAIN CURRENT VS NORMALIZED DRAIN VOLTAGE FOR A CYLINDRICAL FET.

We now calculate the elements in the small-signal equivalent circuit. For the transconductance, we have

$$g_m = \left| \frac{\partial I_{Dc}}{\partial V_g} \right| = 4V_{pc}\, G_{oc} \left[X_2^3 \ell n\, X_2 \frac{dX_2}{dV_g} - X_1^3 \ell n\, X_1 \frac{dX_1}{dV_g} \right]$$

We now calculate dX_1/dV_g and dX_2/dV_g from Eq. (21) as follows

$$-\frac{V_g}{V_p} = X_1^2 \ell n \left(\frac{X_1^2}{e} \right) + 1 \qquad z = 0, \quad V = 0, \quad x_1 = X_1$$

$$-dV_g = 4V_p\, X_1 \ell n\, X_1\, dX_1$$

$$\frac{dX_1}{dV_g} = + \frac{1}{4V_{pc}\, X_1 \ell n\, X_1}$$

The plus sign is chosen since V_g is always negative. The same results follow for X_2.

$$\frac{dX_2}{dV_g} = + \frac{1}{4V_{pc}\, X_2 \ell n\, X_2}$$

Now we simplify g_m

$$g_m = G_{oc} \left[X_2^2 - X_1^2 \right] \tag{27a}$$

The calculation for G_{22} is similar

$$G_{22} = \left| \frac{\partial I_{Dc}}{\partial V_D} \right| = G_o\, X_2^2 \tag{27b}$$

As in the planar analysis we may define normalized g_m and G_{22} as follows

$$g_m = \left| \frac{I_{Dnc}}{V_{gn}} \right| = 4 \left[X_2^2 - X_1^2 \right] \tag{28a}$$

$$G_{22} = \left| \frac{I_{Dnc}}{V_{Dn}} \right| = 4G_o X_2^2 \tag{28b}$$

where $I_{Dnc} = 4 \cdot I_{Dc}/I_{oc}$. Normalized g_m versus V_{gn} is shown in Fig. 10 and normalized G_{22} versus V_{Dn} is shown in Fig. 11.

To calculate the capacitances, we first need to find the volume of the channel.

$$Q = \rho_0 \pi X_2^2 L + \rho_0 L \int_{X_2}^{X_1} \frac{z}{L} 2\pi x_1 \, dx_1$$

Substituting Eq. (26) for z/L we find

$$Q = \rho_0 r_2^2 \pi L \left[X_2^2 - \frac{B}{A - B} (X_1^2 - X_2^2) - \frac{\left[X_1^6 (\ell n X_1 - \frac{5}{3}) - X_2^6 (\ell n X_2 - \frac{5}{3}) \right]}{3(A - B)} \right]$$

where

$$A = X_2^4 (\tfrac{1}{4} - \ell n X_2)$$

$$B = X_1^4 (\tfrac{1}{4} - \ell n X_1)$$

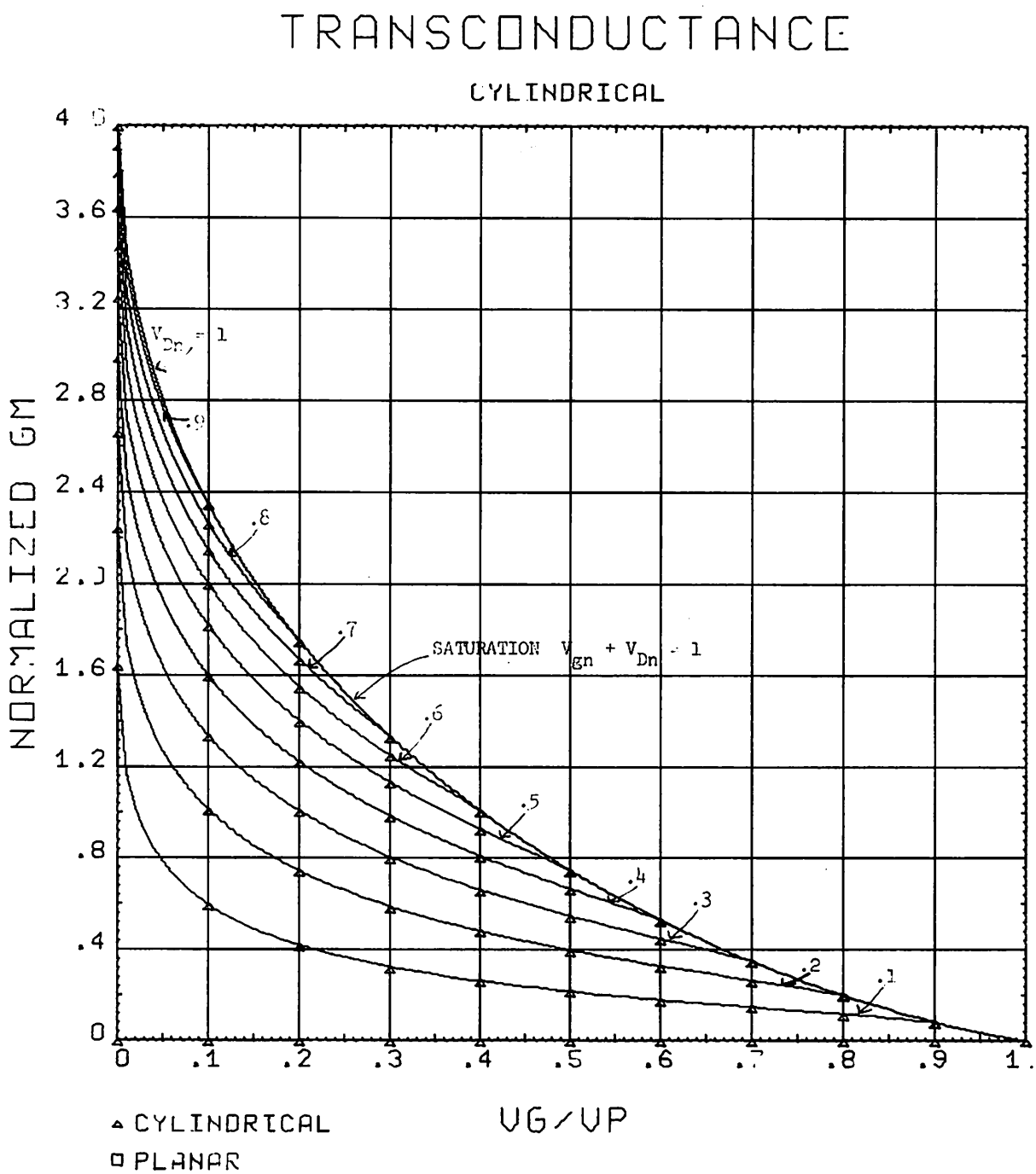

FIG. 1C. NORMALIZED g_m VS NORMALIZED GATE VOLTAGE FOR A CYLINDRICAL FET (Maximum Drain Current Normalized to Unity).

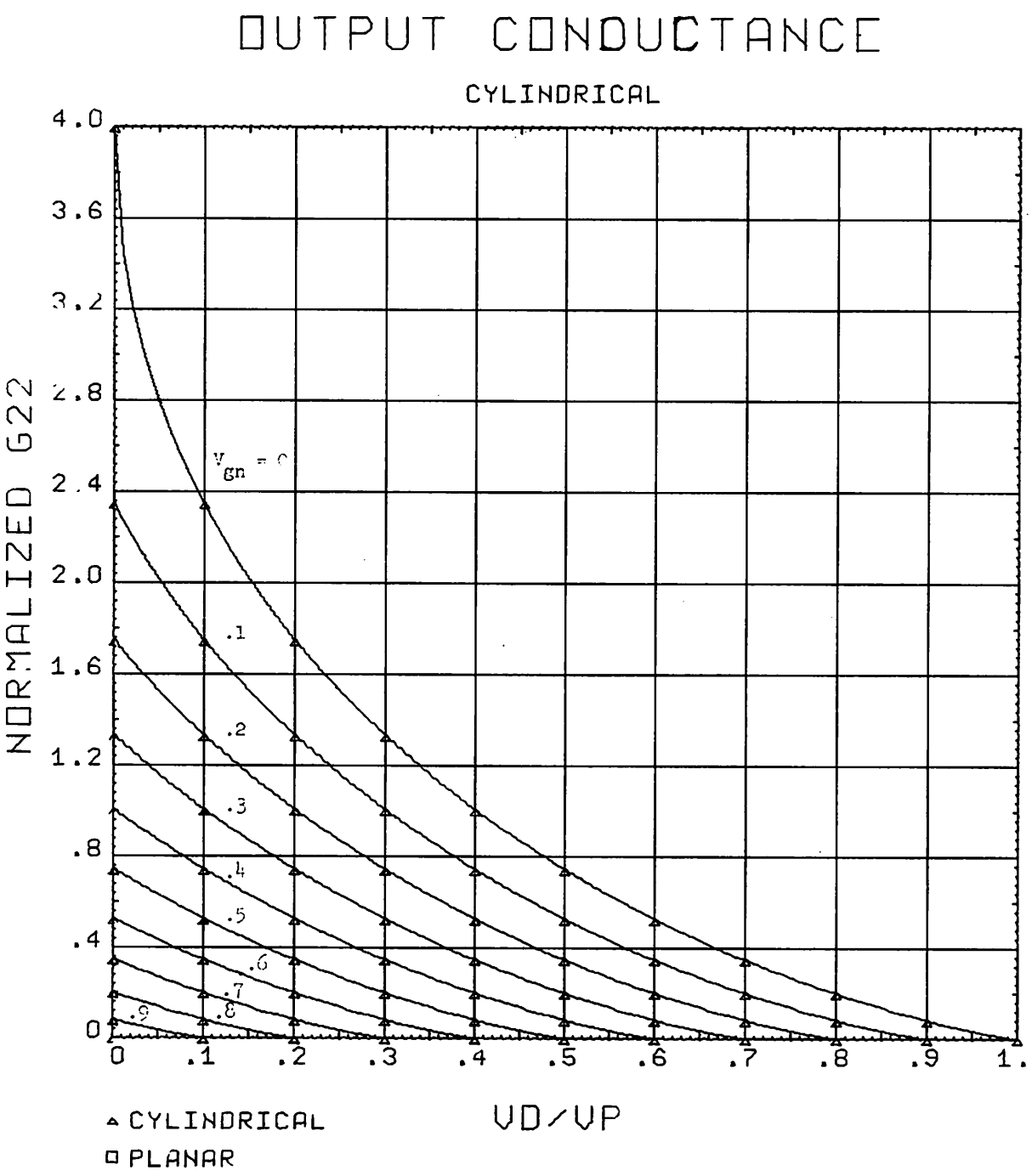

FIG. 11. NORMALIZED G_{22} VS NORMALIZED DRAIN VOLTAGE FOR A CYLINDRICAL FET (Maximum Drain Current Normalized to Unity).

The capacitances

$$C_{11}^{*} = \left| \frac{dQ}{dV_g} \right|$$

$$C_{22}^{*} = \left| \frac{dQ}{dV_D} \right|$$

cannot be easily represented. The numerical analysis to obtain these values on the computer is straightforward however.

This completes the analysis of the cylindrical geometry. Plots (both planar and cylindrical geometries) of channel chape, channel volume, input and output capacitance, as well as I-V characteristics, g_m and G_{22}, are given in the next section.

V. DISCUSSION

Let us review for a moment the mechanism of current flow in a FET. Let the gate voltage, V_g, equal zero volts. As the drain voltage is increased to V_p, the current approaches its maximum value, $I_{max} = V_p G_o / K$ where

V_p is the pinch-off voltage
G_o is the equivalent conductance of a block of semiconductor
$K = 3$ for the planar FET
$K = 4$ for the cylindrical FET

We have previously stated that when the channel is at potential V_p with respect to the gate, the channel is pinched off and $x_1 = 0$. Actually, this is not quite the case for, if the channel area were actually zero and all of the assumptions stated at the beginning of Sec. II remained valid, no current could flow. In real devices, current does flow at voltages above pinch-off. Assume that the drain is at potential $V_p + \Delta V$ and $V_g = 0$. For a real FET, instead of approaching zero area, the channel becomes very narrow $(x = 0^+)$. The resistance in this region becomes large so that there results a large field in the z direction. Thus, the gradual approximation (assumption 8) becomes invalid in the pinch-off region. Instead of the current going to zero at pinch-off, it saturates at $G_o V_p / K$.

For the planar transistor, the space-charge depletion limits the current at pinch-off to one-third of the value which would flow if there were no gate present. For the cylindrical FET, the maximum saturation current is limited to one-fourth its ungated value. Clamping of the current to a small fraction of its ungated value implies good coupling between gate and channel. This good coupling has the effect that if one wished to have planar and cylindrical devices with the same current at pinch off for zero gate bias, the cylindrical FET would have a larger volume than the planar FET. The dimensional ratios are calculated by requiring that the two devices have the same current at $V_g = 0$ and $V_D = V_p$.

$$\frac{I_{oc}}{4} = \frac{I_{op}}{3}$$

where

$$\frac{I_{oc}}{4} = \frac{G_{oc}\, V_{pc}}{4} = \frac{\rho_0 r_2^2}{4\epsilon} \cdot \frac{\mu\rho_0 \pi r_2^2}{L} \cdot \frac{1}{4}$$

$$\frac{I_{op}}{3} = \frac{G_{op}\, V_{pp}}{3} = \frac{\rho_0 a^2}{2\epsilon} \cdot \frac{\mu\rho_0 aD}{L} \cdot \frac{1}{3}$$

where a = width of planar FET; D = depth of planar FET; and r_2 = radius of cylindrical FET.

Since we are just comparing volumes let D = a. Then

$$r_2^2 = \sqrt{\frac{8}{3\pi}}\ a^2$$

and the volume of the cylinder is equal to $\pi r_2^2 L = 2.89La^2$; volume of planar device is equal to La^2.

Hence, the volume of the cylindrical device would have to be approximately three times the volume of the planar device to have the same current at $V_g = 0$, $V_D = V_p$.

In order to compare the performance of the planar FET with that of the cylindrical-volume FET, we normalize the I_{max} for each device to unity. Plots of drain current versus drain voltage as calculated from Eqs. (5) and (24) are shown in Fig. 12. This plot enables us to compare the characteristics of the two devices.

Figures 5 and 10 showed the g_m for each device. This data is replotted in Fig. 13 so that one can compare device performance. Because of the I_{max} normalization, the cylindrical device starts out with a g_m four-thirds that of the planar device. As is evident in Fig. 13, at $V_{gn} \approx .275$, the g_m for both devices are equal and for large V_{gn}, g_m

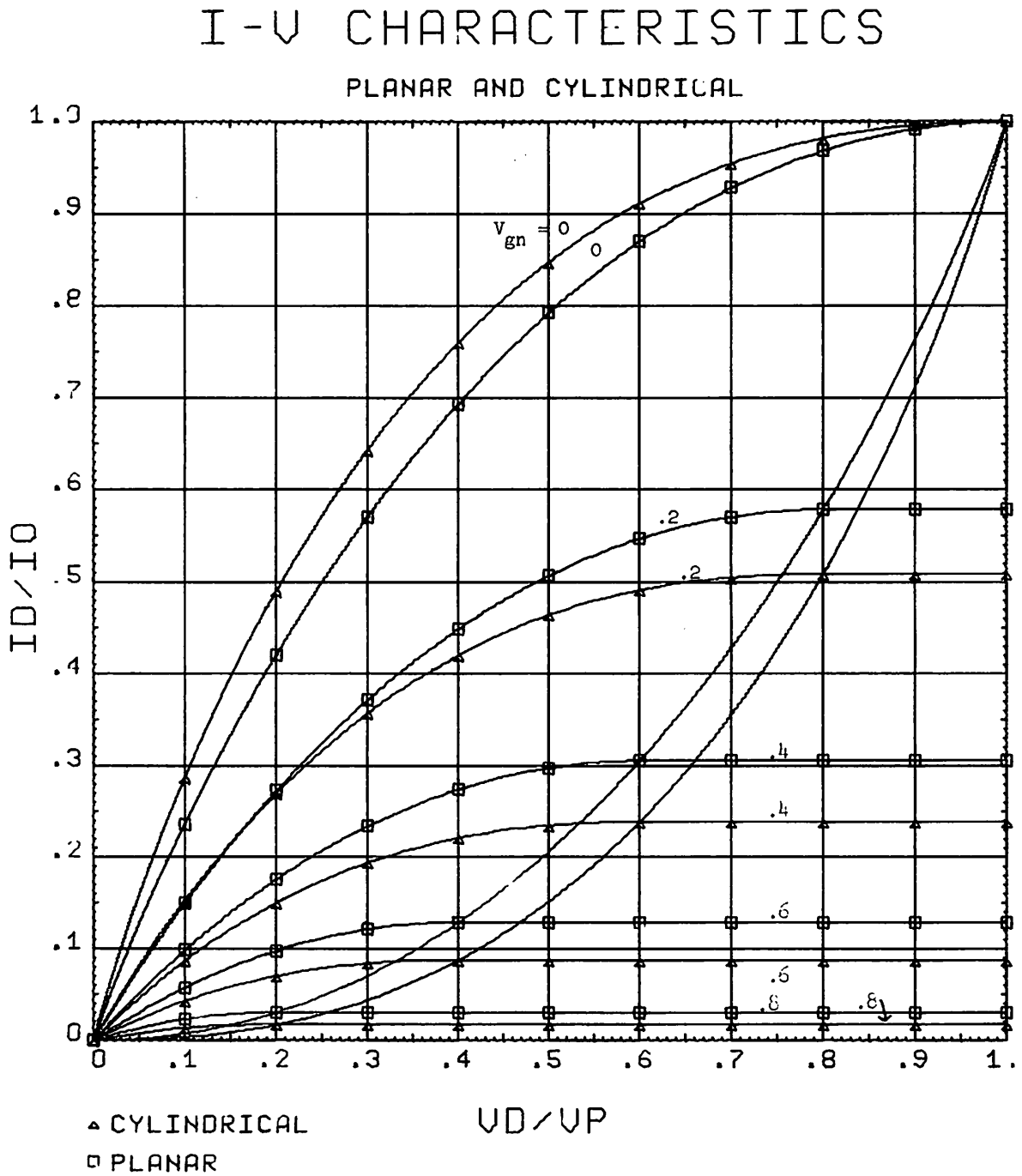

FIG. 12. NORMALIZED DRAIN CURRENT VS NORMALIZED DRAIN VOLTAGE FOR THE PLANAR AND CYLINDRICAL FET.

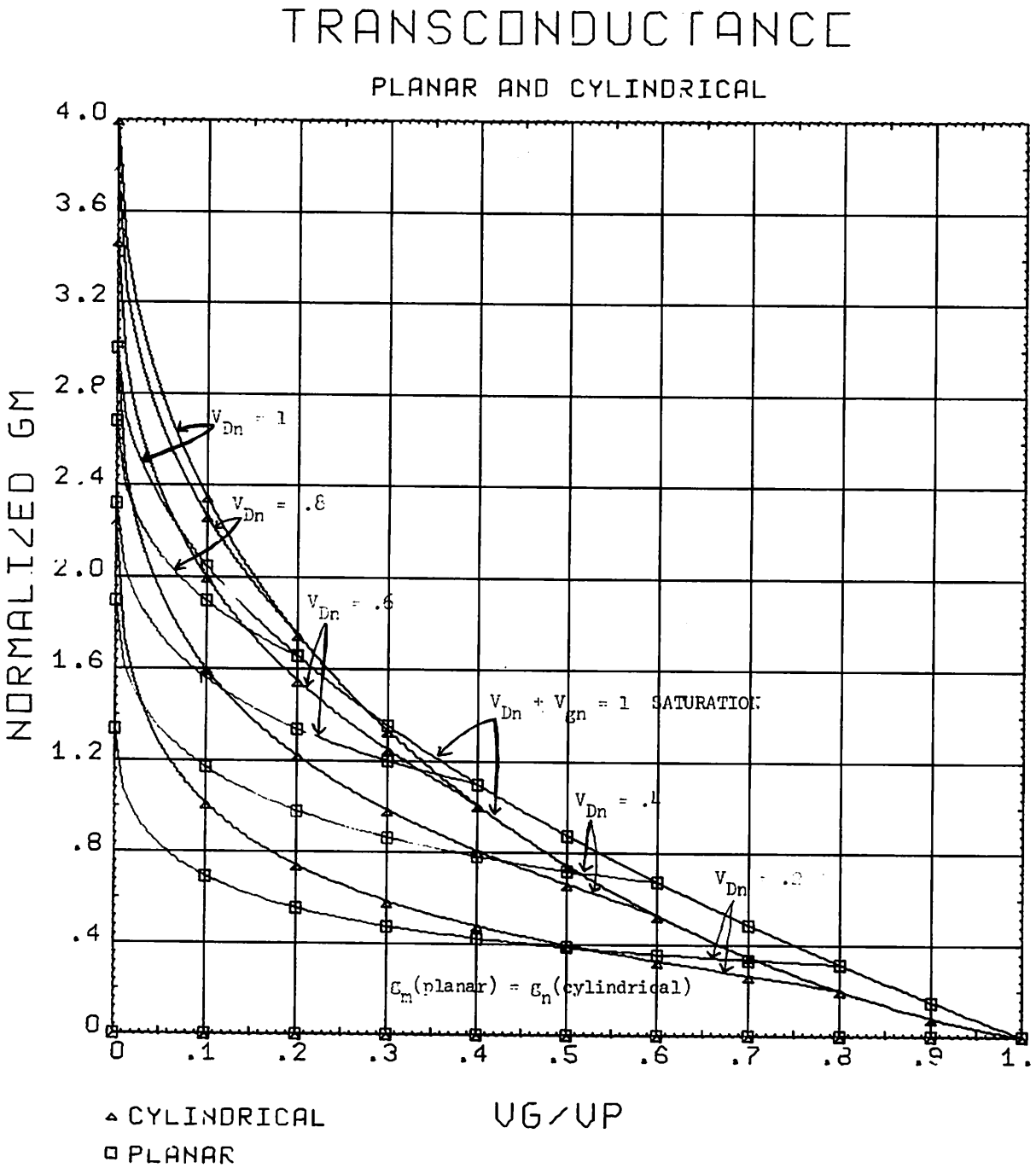

FIG. 13. NORMALIZED g_m VS NORMALIZED GATE VOLTAGE FOR THE PLANAR AND CYLINDRICAL FET (Maximum Drain Current Normalized to Unity).

for the planar device is greater than g_m for the cylinder. Computer code "Cross" was written to calculate the cross-over point to five places. The g_m are equal (in saturation) at $V_{gn} = .27727$.

For biases below saturation $(V_{Dn} + V_{gn} < 1)$, there exists a family of points at which both g_m's are equal. We see from Fig. 13 that the locus of these points is a straight line of slope -4. The equation for this line is

$$g_{mco} = -4V_{gn} + 2.5294 \qquad .27727 \leqq V_{gn} \leqq .6323$$

or

$$g_{mco} = -1.9517\ V_{Dn} \qquad 0 \leqq V_{Dn} \leqq .72773$$

where g_{mco} refers to the common values of g_m shared by the two forms of the FET. A similar plot giving G_{22} for both the planar and cylindrical FET's is shown in Fig. 14.

A possible explanation for the cross-over behavior in g_m is that in the planar device, the area of the boundary between the channel and the space-charge region is approximately planar and remains constant as V_{gn} is varied. In the cylindrical device however, this area is an annular shape and is progressively reduced as V_{gn} is increased. The plausibility for this argument can be established by study of the curves of channel volume and channel shape (x_1 vs z) versus applied bias. These curves are given in Figs. 15 through 26. Although it is not apparent in the curves given, the current is less than half its maximum saturation value when the g_m are equal in the pinch-off region.

It should be apparent that any attempted comparison in the performance of these FET's is dependent on the normalization chosen. For example, assume that we wish now to have both devices have the same V_p and G_o. If this were true, we recognize that the planar device would have a maximum I_D/V_pG_o of 1/3 and the cylindrical device a maximum value for this quantity of 1/4. First, we equate the pinch-off voltages

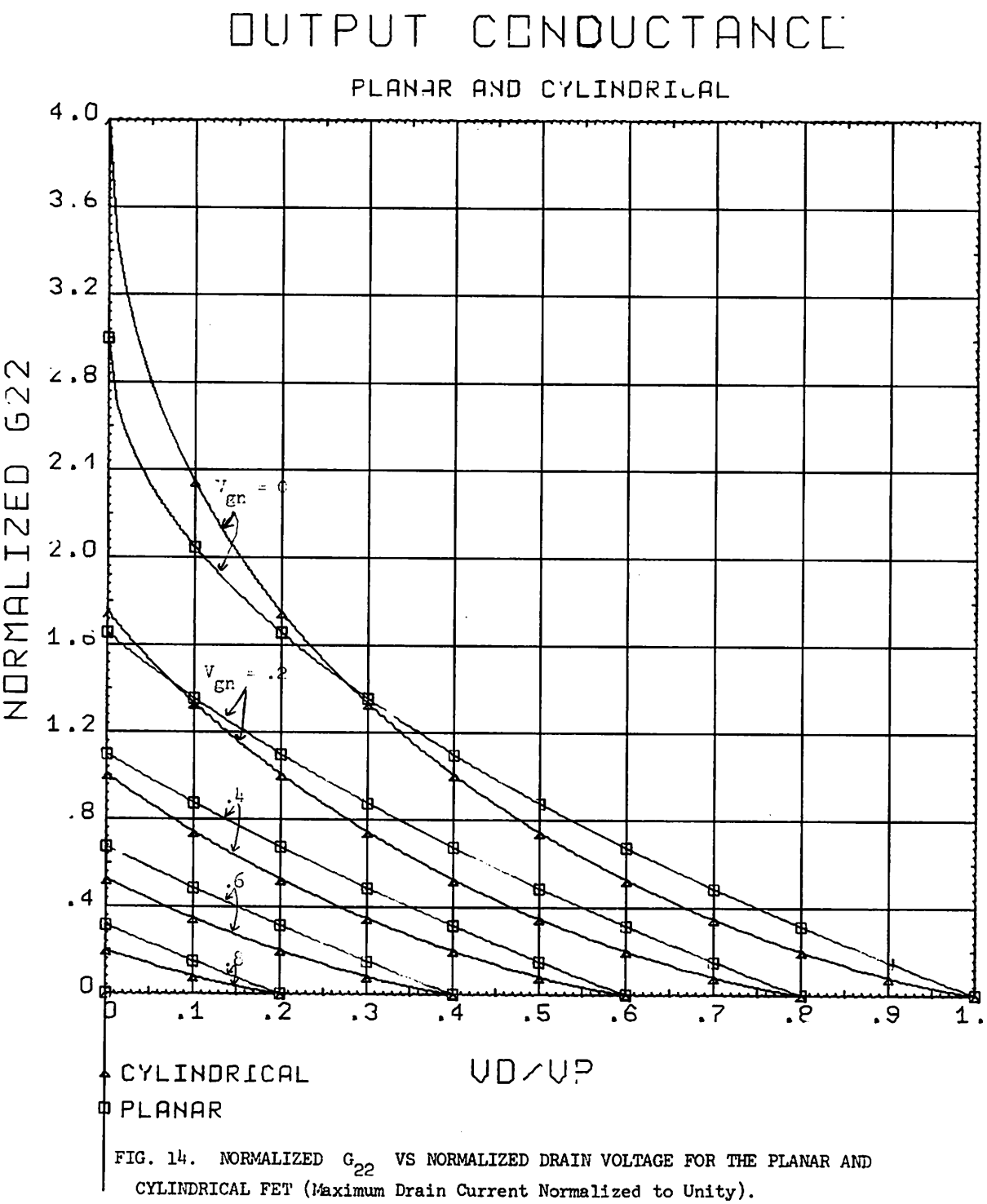

FIG. 14. NORMALIZED G_{22} VS NORMALIZED DRAIN VOLTAGE FOR THE PLANAR AND CYLINDRICAL FET (Maximum Drain Current Normalized to Unity).

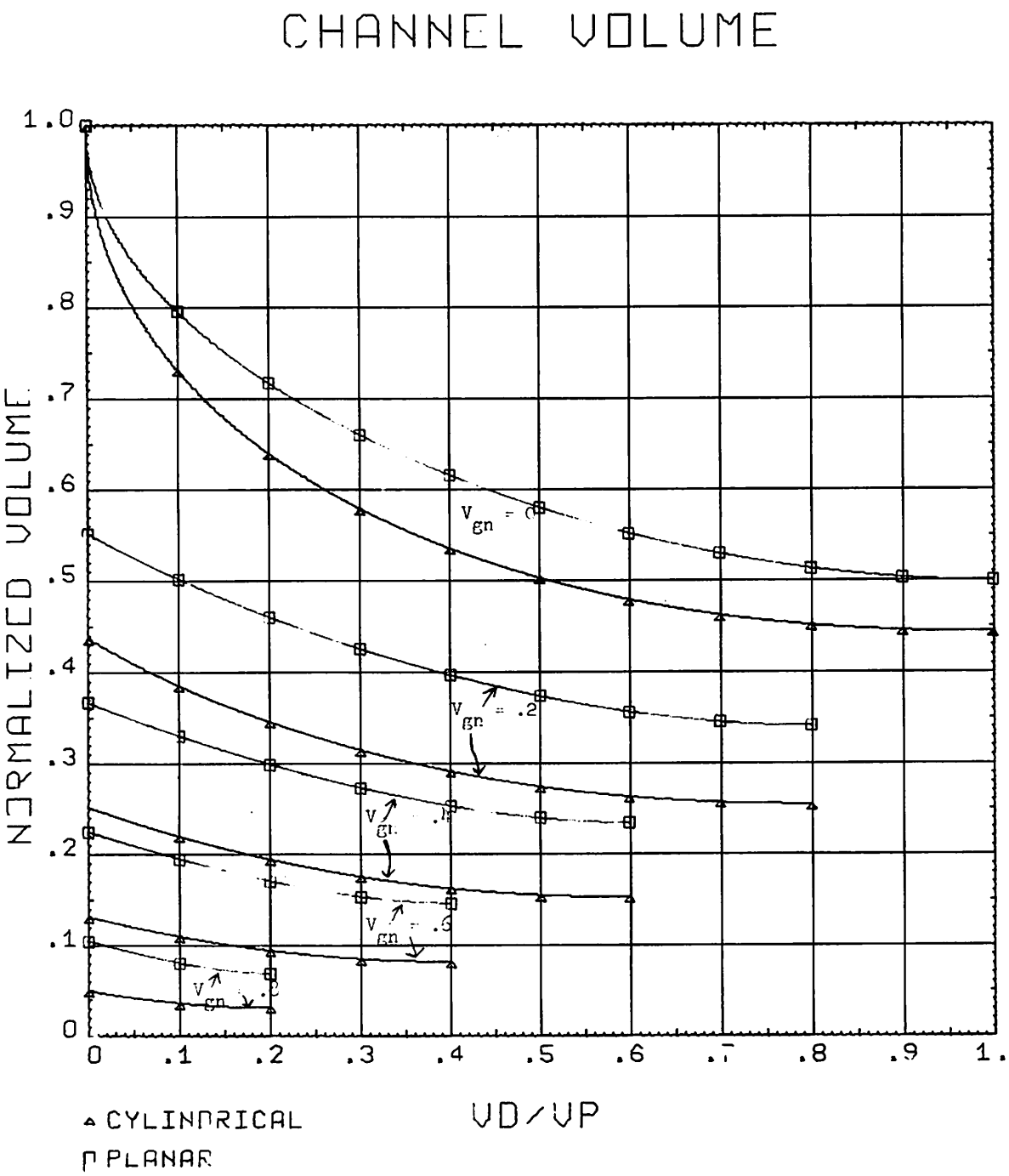

FIG. 15. NORMALIZED CHANNEL VOLUME VS NORMALIZED DRAIN CURRENT FOR THE PLANAR AND CYLINDRICAL FET.

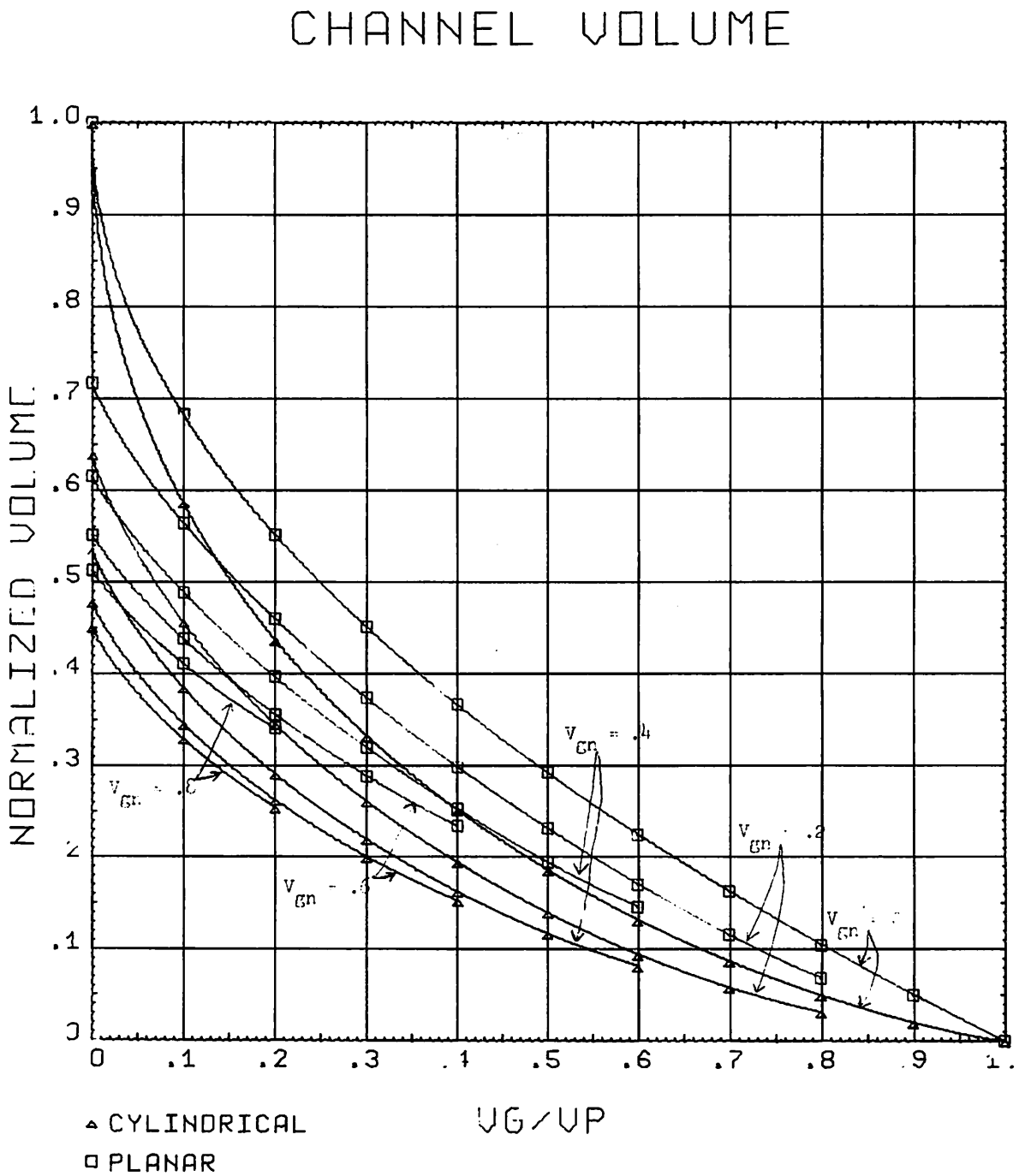

FIG. 16. NORMALIZED CHANNEL VOLUME VS NORMALIZED GATE CURRENT FOR THE PLANAR AND CYLINDRICAL FET.

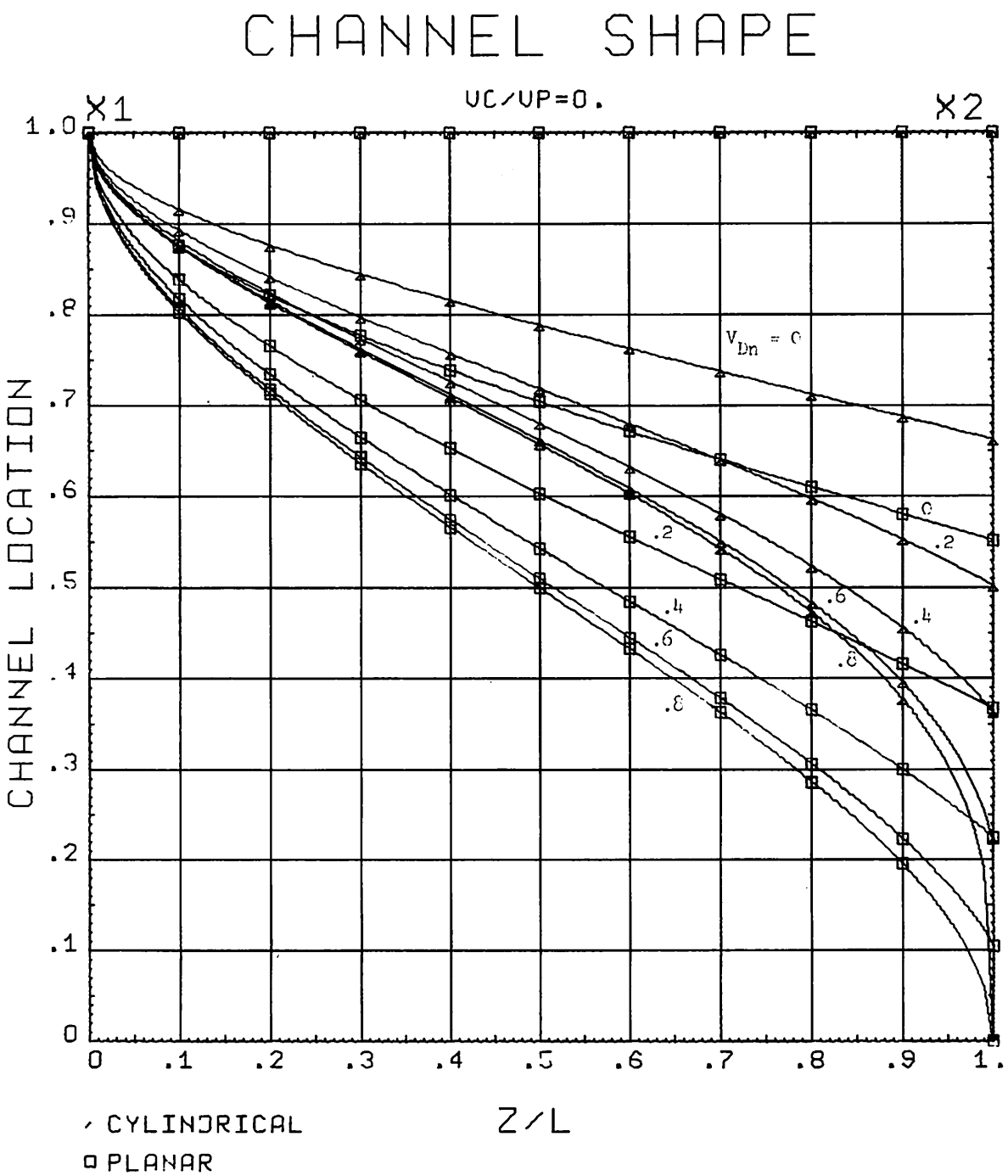

FIG. 17. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

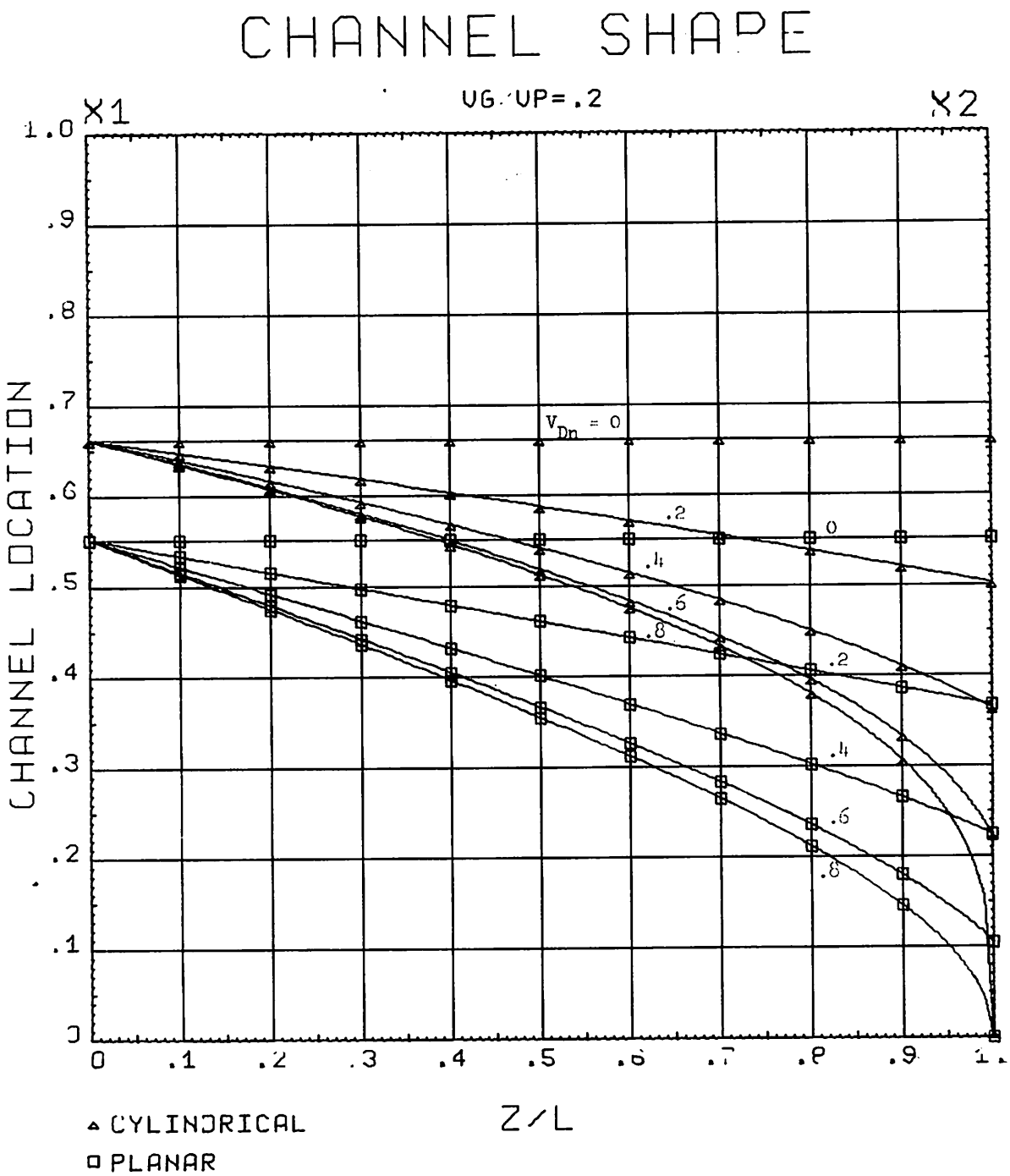

FIG. 18. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

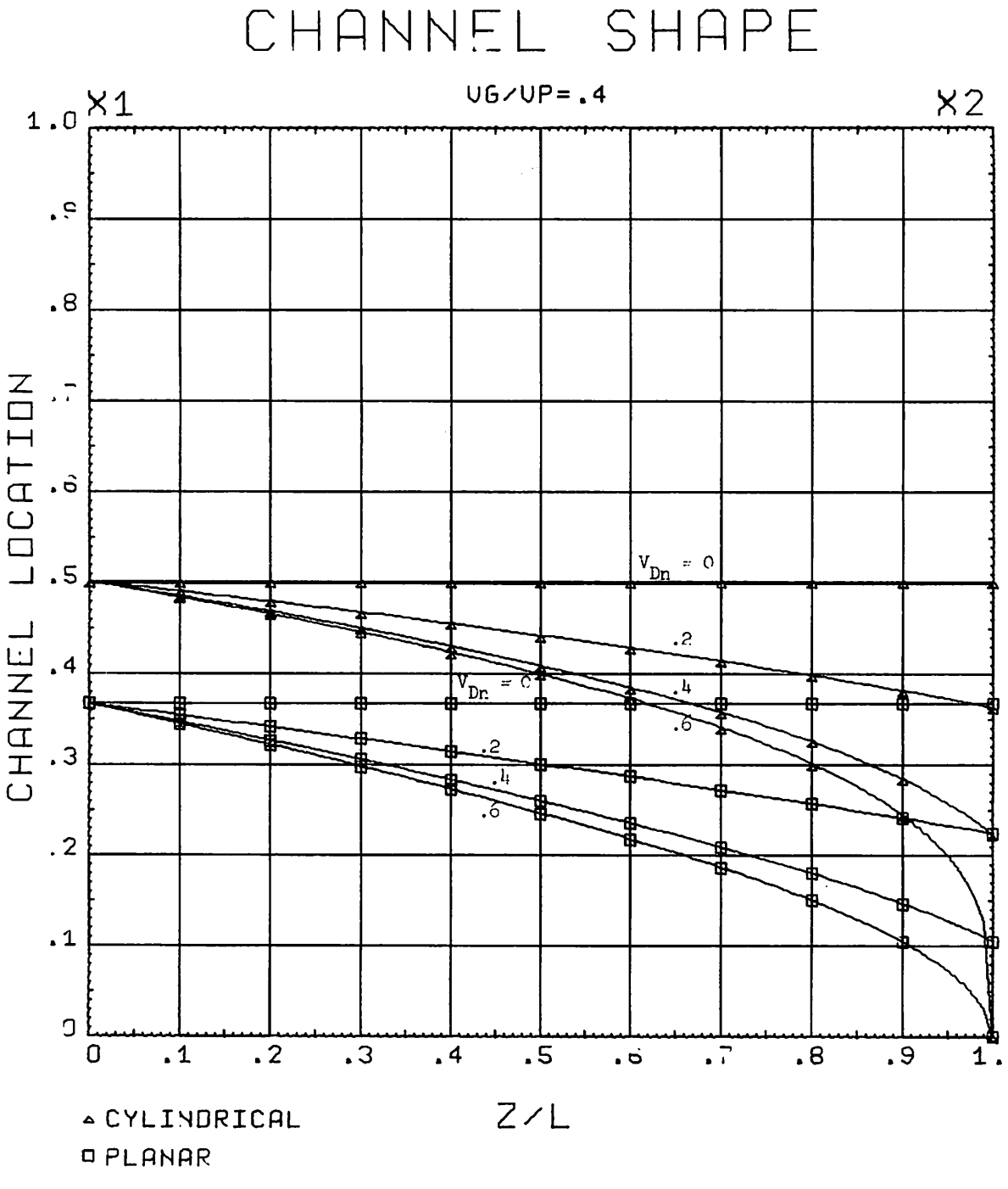

FIG. 19. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

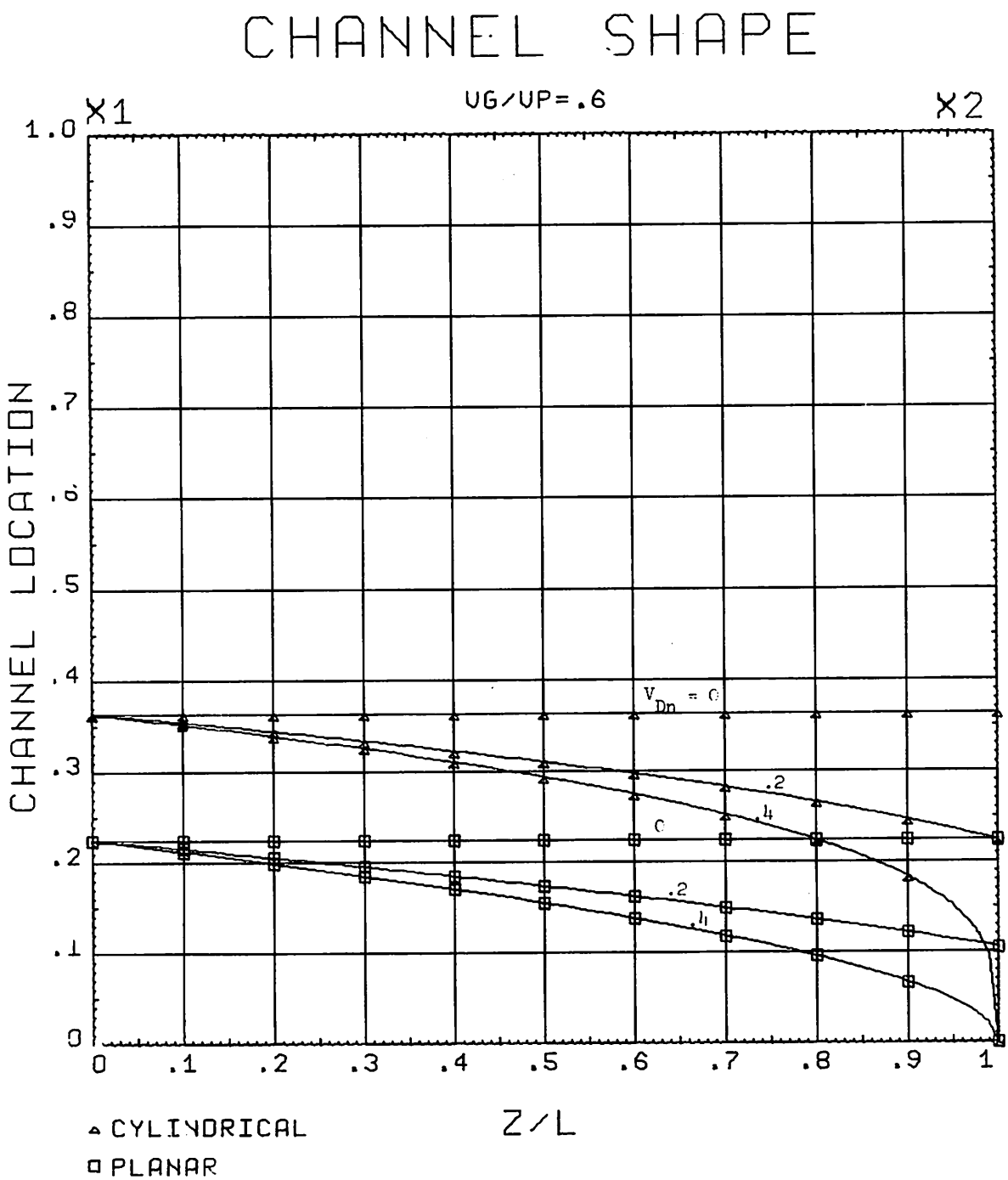

FIG. 20. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

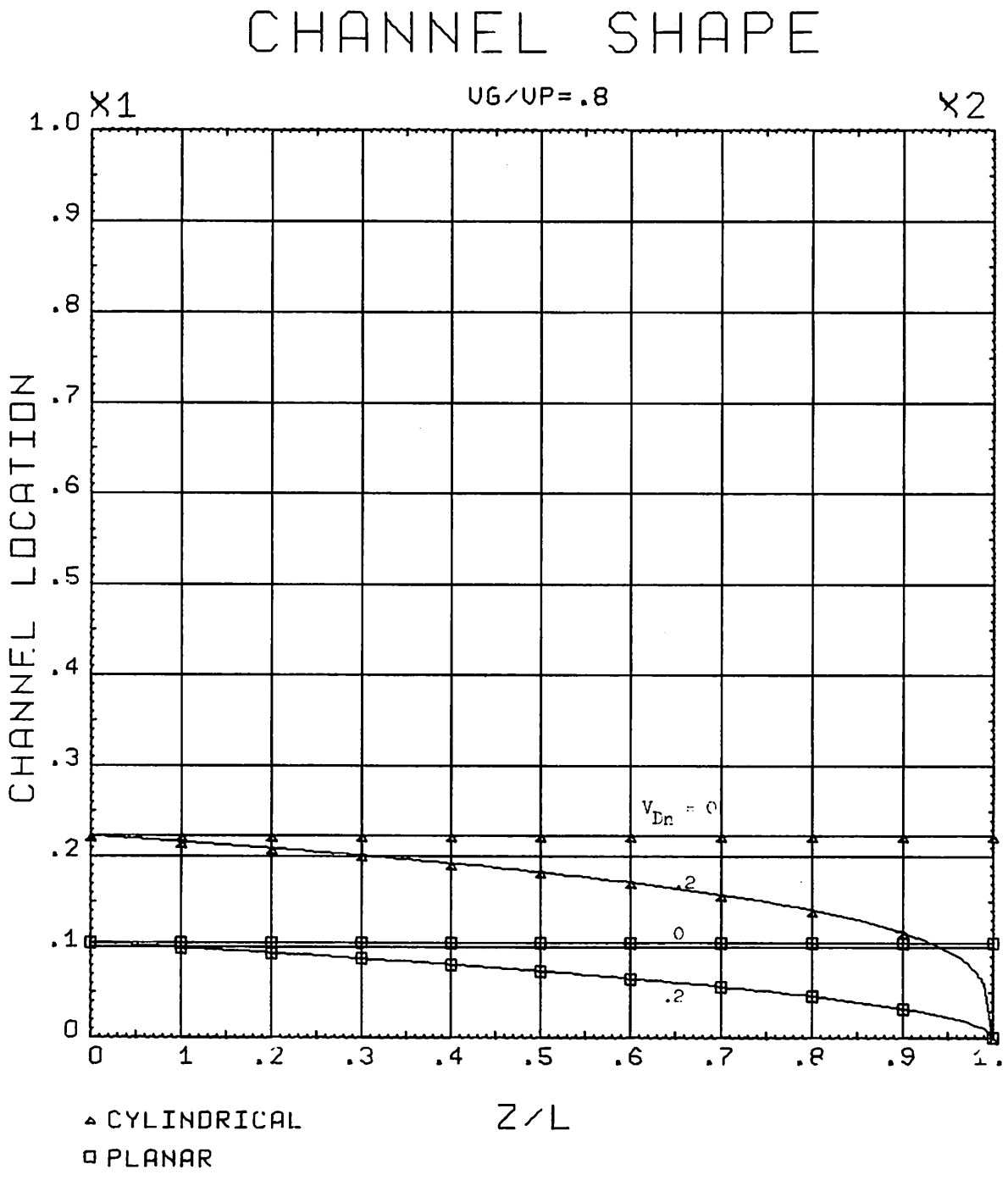

FIG. 21. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

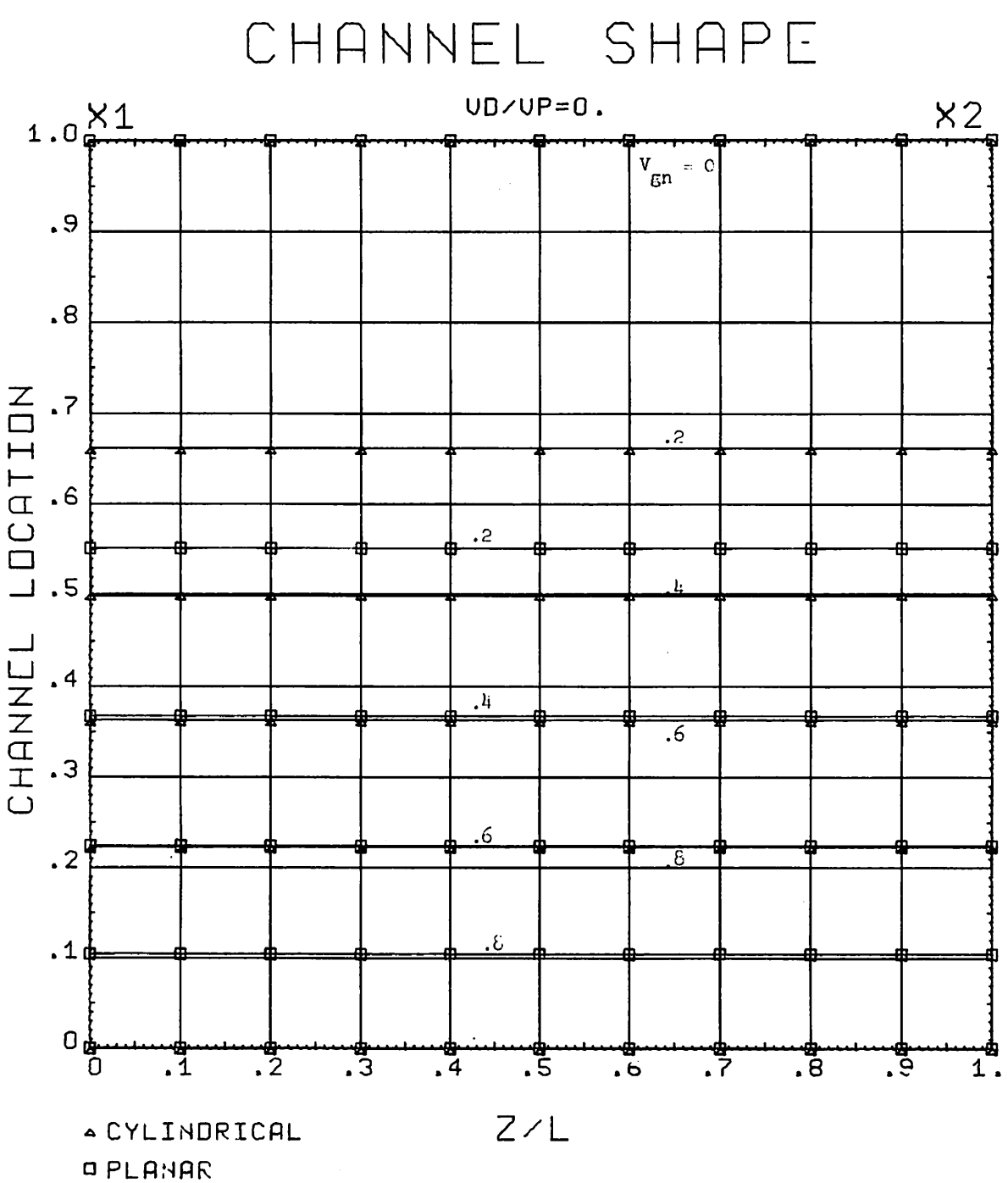

FIG. 22. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

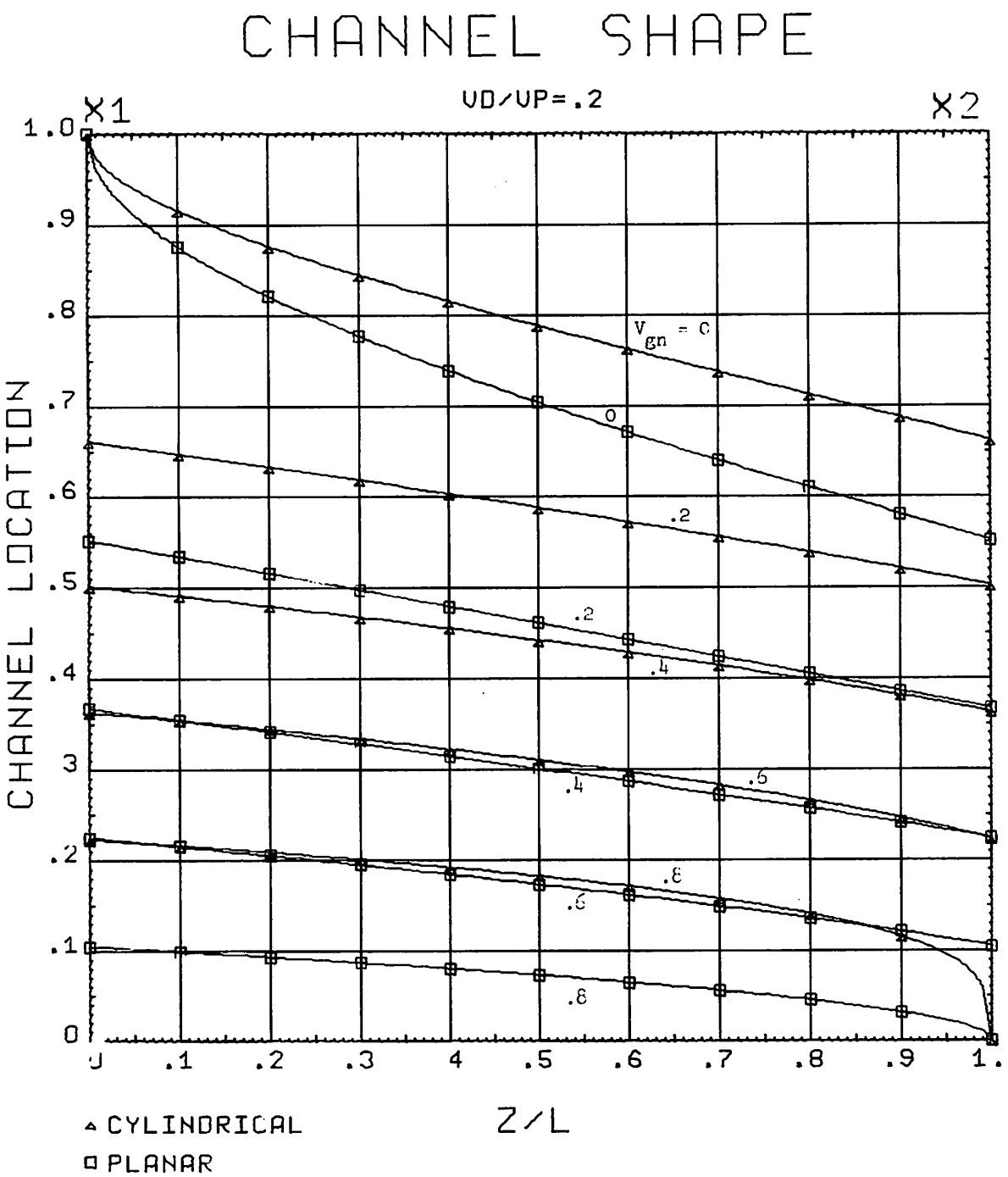

FIG. 23. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

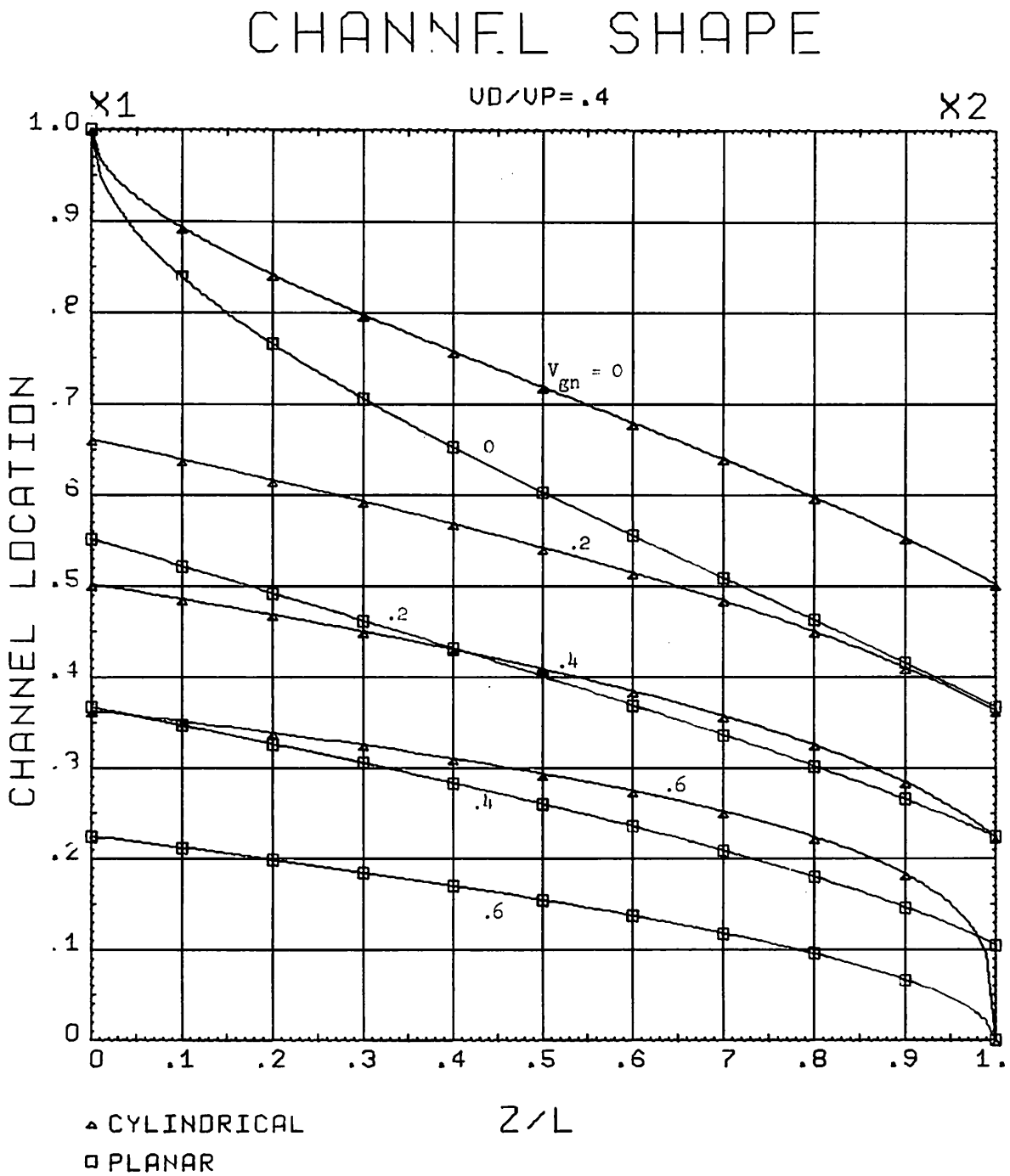

FIG. 24. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

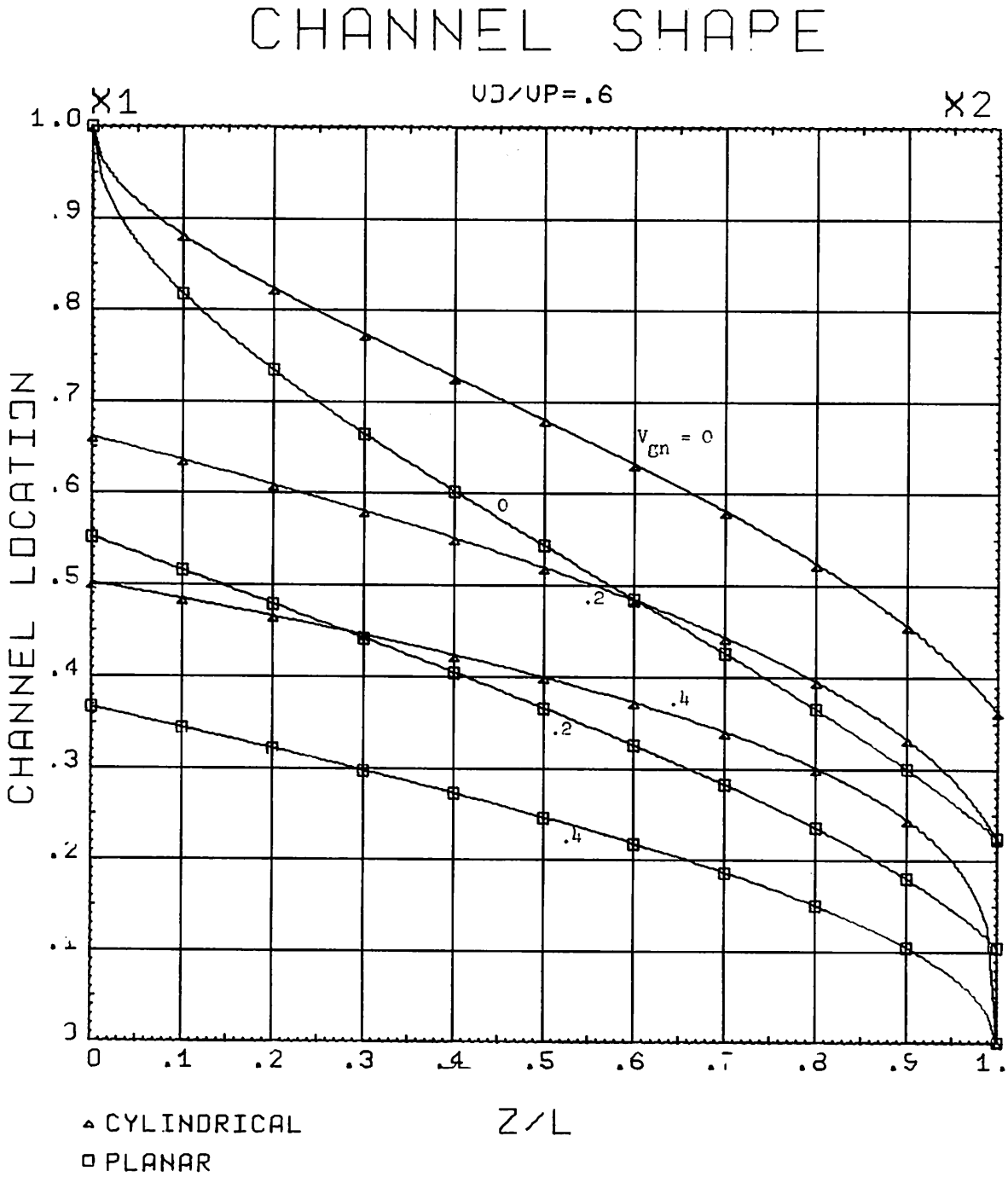

FIG. 25. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

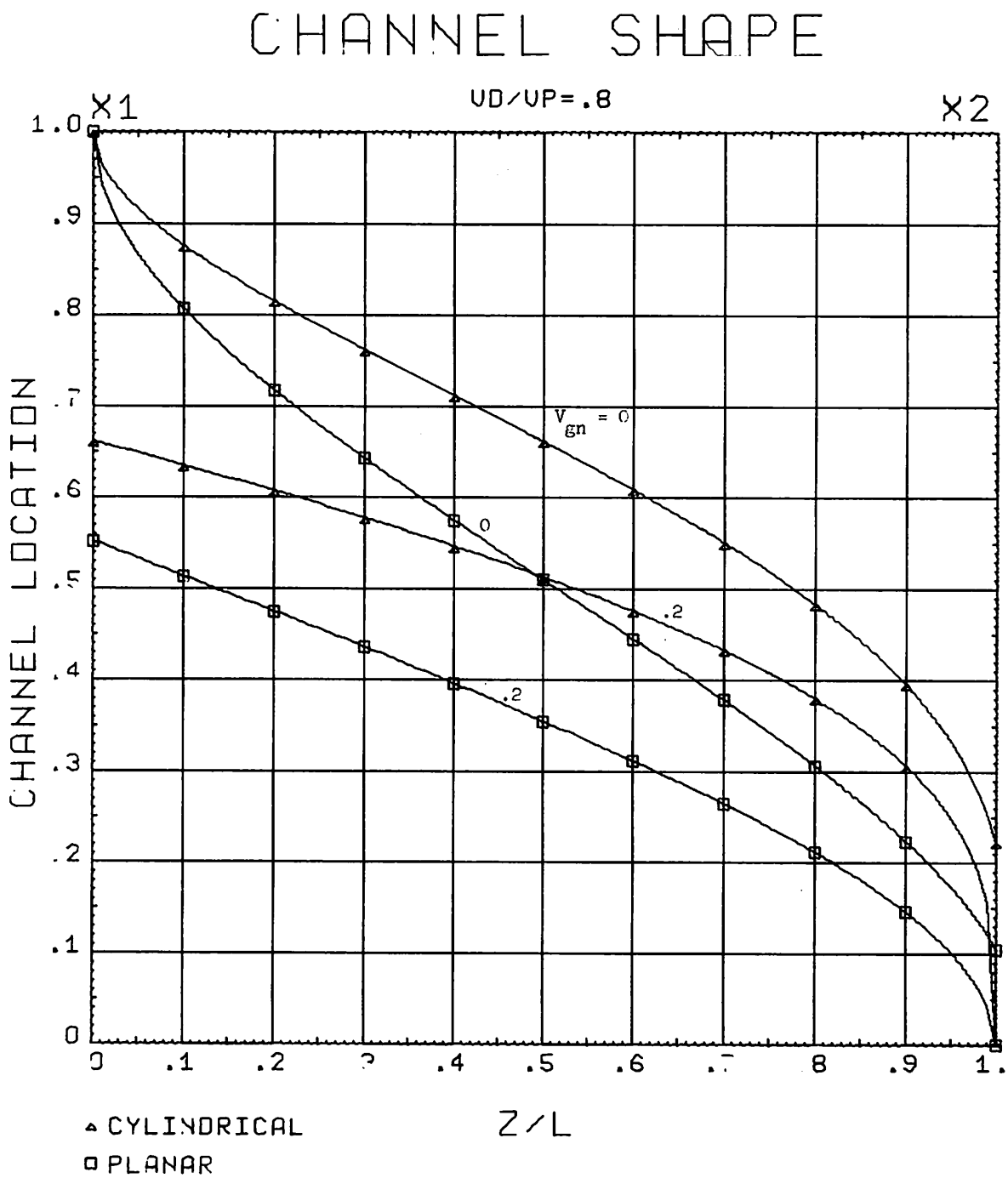

FIG. 26. THE CHANNEL SHAPE (x_1 for cylinder and b for planar) VS Z/L FOR SEVERAL VALUES OF V_{Dn} AND V_{gn}. The two devices are normalized to have the same volume.

$$\frac{\rho_0 r_2^2}{4\epsilon} = \frac{\rho_0 a^2}{2\epsilon} \Rightarrow r_2 = \sqrt{2}\, a$$

Now equate G_o

$$\frac{\mu\rho_0 \pi r_2^2}{L} = \frac{\mu\rho_0 aD}{L}$$

This gives us

$$D = 2\pi a$$

therefore

$$A_p = ad = \frac{r_2}{\sqrt{2}} \cdot 2\pi \frac{r_2}{\sqrt{2}} = \pi r_2^2 = A_c$$

Hence, we have the same volume of material. Now if we calculate g_m we find that both devices have the same values at pinch-off ($V_g = 0$), but g_m for the planar device is greater everywhere else. This is not surprising since the cylindrical device has only 3/4 of I_{max} of the planar device to start with.

Let us now look at the capacitances (Figs. 27, 28). The capacitance values were calculated using Eqs. (9a) and (9b). The total charge in the channel was calculated from Eqs. (11) and (29). These total charges were normalized to have a maximum value of unity which means that the two devices have the same volume. It seems appropriate that to compare the two devices with respect to capacitance, they should have the same maximum channel volume. The input capacitance was calculated by calculating (for V_{Dn} fixed) the channel volume for $V_{gn} = 0$ to $V_{gn} = 1 - V_{Dn}$ in increments of $V_{gn} = .001$. The capacitance at $V_{gn}(I)$ is

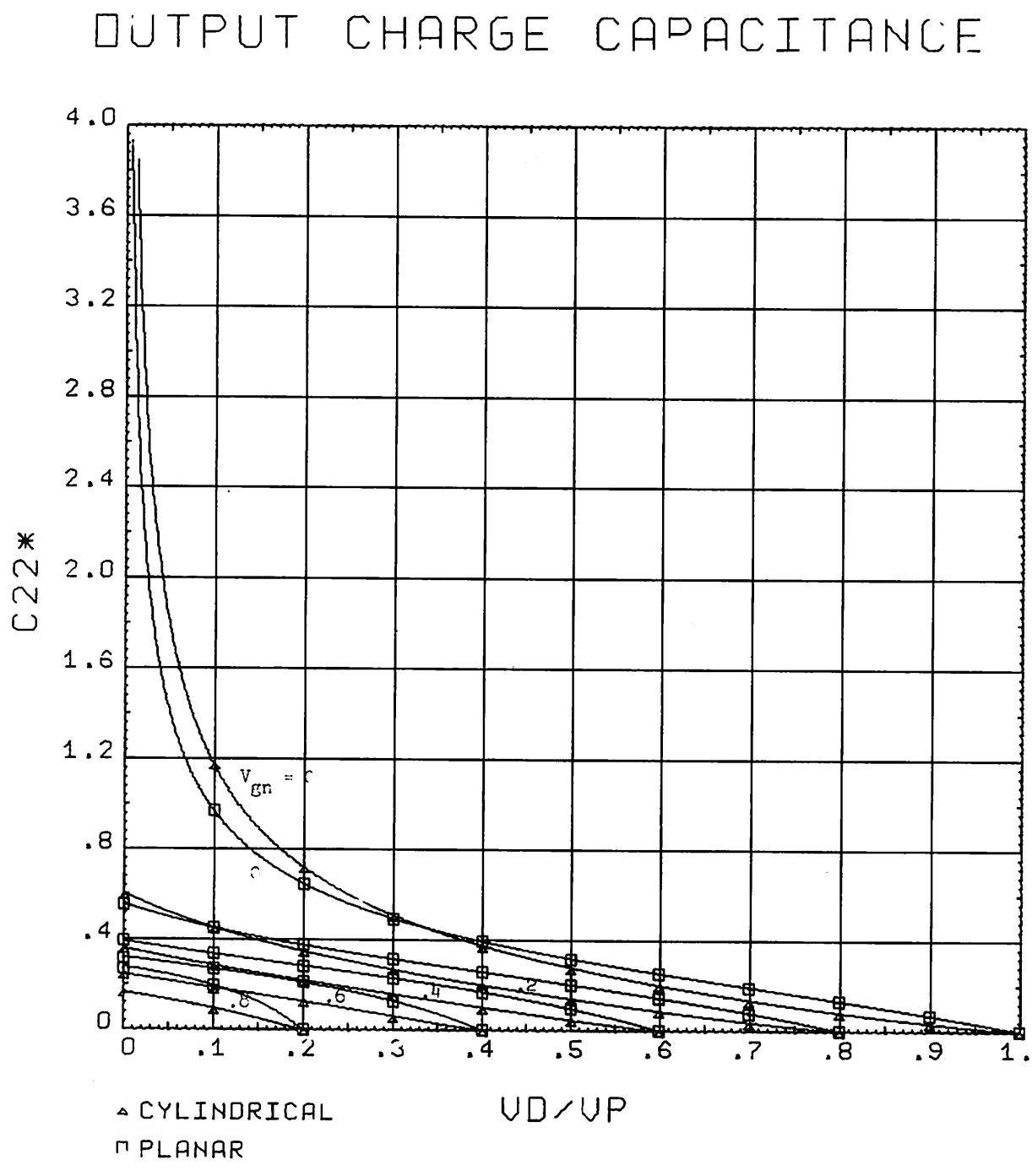

FIG. 27. OUTPUT CHARGE CAPACITANCE (rate of change of normalized channel volume with respect to normalized drain voltage) VS NORMALIZED DRAIN VOLTAGE (Maximum Channel Volume Normalized to Unity).

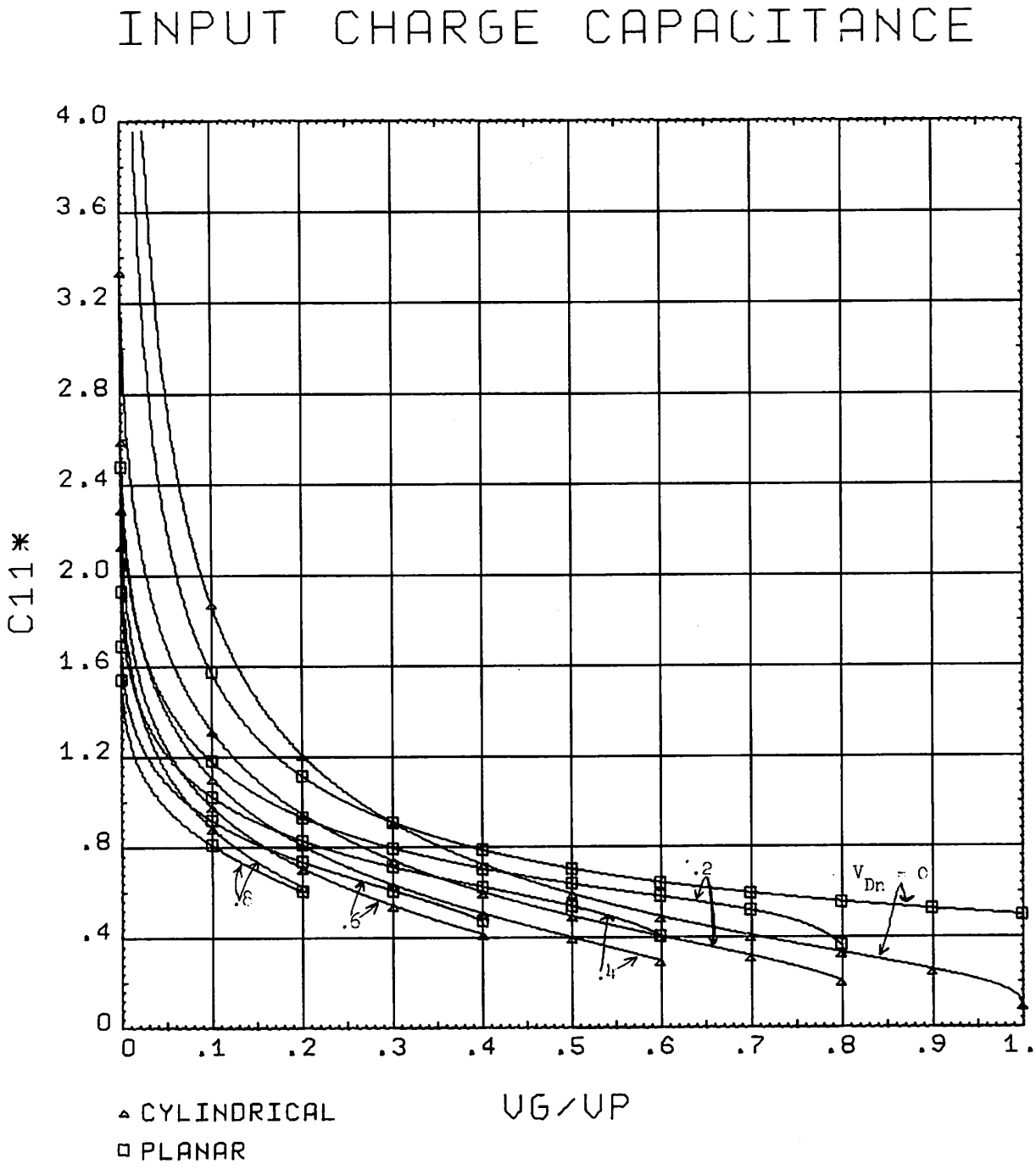

FIG. 28. INPUT CHARGE CAPACITANCE (rate of change of normalized channel volume with respect to normalized gate voltage) VS NORMALIZED GATE VOLTAGE (Maximum Channel Volume Normalized to Unity).

$$C_{11}^{*}(I) = \left.\frac{Q(I-1) - Q(I+1)}{.001}\right|_{V_{Dn} = \text{const.}}$$

$$C_{22}^{*}(I) = \left.\frac{Q(I-1) - Q(I+1)}{.001}\right|_{V_{gn} = \text{const.}}$$

A check on the accuracy was made by calculating C_{11}^{*} for the planar geometry by Eq. (12a) and comparing the results with the method as stated above. Except at $V_{gn} \approx 0$ where the error was approximately 1 part in 100, the two results compared within 1 part in 1000. Since this is greater accuracy than one can read from the graphs, it was deemed sufficient.

In this discussion we have shown that in an absolute theoretical sense, one cannot say which device is "better." On a practical basis, the cylindrical device does have an advantage which occurs from fabrication techniques. This is the fact that large numbers of these devices can be constructed in parallel (Zuleeg) with no stray inter-electrode capacitance. This makes for a device with high current, high gain and high frequency. Zuleeg has reported the following characteristics for a volume FET with 100 parallel channels.

$$g_m = 10 \text{ mA/V}$$

$$I_{max} = 25 \text{ mA}$$

$$V_p = 10 \text{ V}$$

$$C_{GD} = 5 \text{ pf} \quad (\text{at } 10 \text{ V})$$

$$\text{Power Gain} = 14 \text{ db at } 60 \text{ MC}$$
$$= 10 \text{ db at } 100 \text{ MC}$$

$$\text{Extrapolated } f_{max} = 300 \text{ MC}$$

3 db g_m cut-off frequency = 275 MC

Zuleeg reports that with optimizing geometry and impurity profiles, a maximum frequency of oscillation of 1000 MC should be possible.

APPENDIX A

In this section we present a brief note on the use of the computer in performing the calculations. All calculations were performed on an IBM 7040 - 7094 computer. The computer prepared a plot tape which was plotted by a Cal-Comp 11 inch plotter. The computer was used because the solution to a transcendental equation was needed at a large number of points. It was an easy step then to machine program the output plots for the various functions. Each code simply evaluates the expressions derived in the text in a direct manner. The major portion of each code was in preparation of the plots. All calculations for the cylindrical geometry used subroutine X4. This routine calculated X_1 and X_2 given V_{gn} and V_{Dn}. To make this calculation, we first rewrite Eq. (21) in the following manner, defining a new variable VN.

$$VN = V + V_{gn} = x_1^2 \ell n \left(\frac{x_1^2}{e}\right) + 1 \qquad (A.1)$$

The plus sign on V_{gn} in Eq. (A.1) is written because V_{gn} is always negative in reality. At $x_1 = X_1$, $V = 0$ and at $x_1 = X_2$, $V = V_{Dn}$. We first prepare a table of VN versus x_1 for $1 \geqq x_1 \geqq 0$ in increments of .001. Then when we call X4 the channel edge at $z = 0$ is found by setting $VN = V_{gn}$ and looking up the closest value of x_1 and interpolating. To find X_2 we let $VN = V_{gn} + V_{Dn}$ and proceed as before. This method is used also in evaluating the channel shape. If one desires greater accuracy, second order interpolation can be used. In all plots, except channel volume and capacitance, points were calculated and plotted 10 per inch. In these plots, points were calculated and plotted 100 per inch. The accuracy obtained in each case is greater than can be observed on the plots. A complete listing of all the codes is available from the author.