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AN ELECTRON BEAM ACTIVATED CHARGE STORAGE DEVICE
AND ASSOCIATED MEMORY

by

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ABSTRACT

A new type of electron-beam-activated switch is described which utilizes electron-beam-induced charge storage in the metal-oxide-semiconductor system. The state of the electron-beam-activated switch (EBAS) is determined by monitoring the surface conductance of the semiconductor. The basic charge-storage phenomena is discussed. Memory arrays that use the electron beam for storing and reading information are described. A matrix array of EBAS's in which information is stored using the electron beam and read by row-column access circuits is discussed in detail. The time to store a bit of information is a function of the current density of the electron beam; an approximate dosage of 10^{-5} C/cm² is required for storage.

A practical memory design using Schlesinger's microspot tube for the electron optics is discussed. It is shown that a storage of 3.4×10^7 bits per tube is possible with presently available electron optical design and semiconductor technology.

LIST OF SYMBOLS

A_s	Area scanned by the electron beam
C_0	Capacitance per unit area of the oxide layer ($C_0 = \epsilon_{ox}/x_0$)
D	Drain
E	Electric field
EBAS	Electron beam activated switch
g_{ds}	Small signal drain-source conductance
I_B	Primary electron beam current
\bar{J}_B	Average current density of the scanning electron beam
L	Channel length of a MOST, or the distance between the source and drain regions of a MOST; length of storage area
LS	Left side
MOS	Metal-oxide-semiconductor
MOST	Metal-oxide-semiconductor transistor
NB	Number of bits
PD	Packing density, bits/cm ²

q	Electronic charge $1.6 \times 10^{-19} \text{ C}$	
Q_n	Charge due to mobile electrons within the inversion layer	} per unit area
Q_0	Total net charge in the oxide	
Q_{SB}	Electron beam induced charge in the oxide	
Q_S	Net total charge within the semiconductor	
$Q'_S(\text{SAT})$	Saturation value of Q'_S for a given V_{GB}	
Q_{SS}	Charge in the surface States	
R	Read area	
RS	Right side	
S	Store area; source	
SEM	Scanning electron microscope	
t	Time	
V_B	Primary electron beam accelerating potential	
V_D	Drain potential of a MOST with respect to the source	
V_G	Gate potential of a MOST with respect to the source	
V_{GB}	V_G during electron bombardment of the gate electrode	

V_T	Initial threshold voltage of the MOST before electron bombardment
V_T'	Threshold voltage of the MOST during electron bombardment
V_{TS}'	Saturation value of V_T' for a given value of V_{GB}
W	Width of device
w	Width of a storage area; spacing between storage areas
x	Position
x_1	Position of the charge sheet Q_{SB} or characteristic length associated with the charge distribution
x_0	Thickness of the oxide
ϵ_{ox}	Dielectric permittivity of the oxide
τ_c	Characteristic time constant for the radiation induced charge accumulation in the oxide
τ_B	Time to store a bit
τ_d	Characteristic time constant for the radiation induced discharge in the oxide
ρ	Net charge density
ρ_B	Electron beam induced charge density in the oxide

TABLE OF CONTENTS

	<u>Page No.</u>
INTRODUCTION	1
THE BASIC CHARGE STORAGE PHENOMENA	3
THE MEMORY OPERATION	9
PRACTICAL MEMORY CONFIGURATIONS	16
DISCUSSION	20
REFERENCES	27
TABLES	
I and II	31-32
LIST OF FIGURES	33

INTRODUCTION

Many schemes for electron beam recording and information storage have been proposed [1]. The electrostatic storage tube of Williams [1], thermoplastic recording [2, 3], and electron beam exposure of photographic emulsions [4] are but a few of the systems that utilize electron beams for information storage. Electrostatic storage of charge patterns on insulators [1, 5, 6] suffers from the instability of the storage media and the charge patterns. In the Williams' tube the information must be rewritten periodically, the readout is destructive, and indexing the beam to a given bit for random access is difficult. Electrostatic storage on the surface of insulators is, for the most part, used today for information display. Electron beam exposure of photographic emulsion [4, 7, 8] is practical in very very large stores, 10^{12} bits, and instances where random access time is not of paramount importance.

In this paper a new electron beam activated switch EBAS is described. By the utilization of state-of-the-art solid-state technology, the metal-oxide-semiconductor system MOS [9], and state-of-the-art electron-optical design [10-13], a stable charge-storage memory is

described. The basic EBAS uses the storage of fixed positive charge in the insulator by electron bombardment of the MOS system [14-15], the state of a memory element is determined by monitoring the surface conductance of the semiconductor. A memory which uses electron beam storage and retrieval of the information and a memory which uses electron beam storage and matrix readout are described. The matrix readout memory, or the EBAS memory, should provide very short random access times and a very high information transfer rate for readout.

The basic storage phenomena are first described, then practical memory arrays and logic functions are considered. System parameters that determine response times are discussed. Finally, a practical memory design that uses Schlesinger's microspot tube is discussed in detail to illustrate the characteristics of the EBAS memory.

THE BASIC CHARGE STORAGE PHENOMENA

The basic charging effects associated with electron bombardment of the metal-oxide-semiconductor system are discussed in this section. It is shown that the electric field at the semiconductor-insulator interface, and consequently, the charge induced in the semiconductor Q_S^1 can be reversibly changed by electron bombardment of the MOS system at different gate-substrate potentials.

Figure 1 is a schematic diagram of a p channel¹ MOS transistor (MOST) [16]. For the discussion that follows the reader should consider the MOST as a charge-controlled resistor. The drain-to-source conductance g_{ds} is controlled by the gate-substrate potential V_G and by the charges in the insulator. In order to produce a large increase in g_{ds} , the semiconductor surface beneath the insulator must be inverted the entire length of the channel L . Figure 1 shows fixed positive charges in the insulator. The positive charges induce a corresponding negative charge in the semiconductor [9], and hence a negative gate

¹ Unless specifically indicated to the contrary, a p channel MOST will be used for explaining the various phenomena. Similar results hold for n channel MOST's.

potential must be applied to produce an inversion layer. The voltage one must apply to the gate just to cause inversion is defined as the threshold voltage of the device. By increasing the positive charge in the oxide, we find that the magnitude of the threshold voltage increases.

Positive charges are introduced in the oxide during device fabrication, and these charges produce an initial MOST threshold voltage V_T [9]. It is also possible to introduce fixed positive charge in the oxide by electron bombardment at a positive gate voltage. The additional positive charge in the oxide induces a corresponding negative charge in the semiconductor Q'_S , and the new threshold voltage of the device V'_T is given by Eq. (1) where C_0 is the capacitance.

$$V'_T = V_T + Q'_S/C_0 \quad (1)$$

per unit area of the oxide layer. Since $|V'_T| > |V_T|$, a larger negative gate voltage must be applied to induce a channel after electron bombardment of the MOST.

With reference to Fig. 1, the primary electron beam is scanned over the metal gate electrode. The 10 - 30 kV electrons penetrate through the metal gate and insulating layer and come to rest in the semiconductor. The main effect of the electron beam is the ionization of various valance band and trapping states in the oxide. With an applied positive gate voltage during electron bombardment V_{GB} electrons drift

toward the gate electrode leaving behind fixed positive charge near the Si - SiO₂ interface. Figure 2(a) shows a section of the MOS structure after electron bombardment at a positive gate voltage. The fixed positive charges in the oxide induce negative charges, mobile electrons and acceptor atoms, in the p-type semiconductor. A plot of the charge density in the oxide and the semiconductor is given in Fig. 2(b). A sheet charge equivalent* of the charge distribution of Fig. 2(b) is shown in Fig. 2(c). The positive charge introduced during the device fabrication that accounts for V_T is modelled as a sheet charge Q_{SS} located at the interface. The charge introduced by the electron beam is modelled as a sheet charge of magnitude Q_{SB} where

$$Q_{SB} = \int_0^{x_0} \rho_B dx .$$

The distance from the interface at which the average of the electron-beam-induced charge resides is x₁ where x₁ is defined by the following relation [17]

* The two distributions of Fig. 2(b) and 2(c) are equivalent, by definition, in the sense that the same amount of charge is induced in semiconductor Q_S' by either distribution.

$$x_1 = \frac{\int_0^{x_0} x \rho_B dx}{\int_0^{x_0} \rho_B dx} .$$

If it is assumed that x_1 is a constant [14], the charge accumulates about a mean position x_1 from the interface as electron bombardment at a positive gate voltage V_{GB} proceeds [14]. The pertinent boundary condition is that

$$V_{GB} = - \int_0^{x_0} E(x, t) dx$$

is constant during bombardment. An increase in Q_{SB} increases the magnitude of the electric field at the interface and reduces the magnitude of the electric field in the remainder of the oxide [14]. A graphical picture of the charging phenomena is shown in Fig. 3. Figure 3(a) shows the sheet charge located at $x = x_1$. The electric field in the oxide as a function of time is shown in Fig. 3(b). At $t = 0$, a uniform field of magnitude V_{GB}/x_0 exists throughout the oxide. At some later time $t = \tau_c$ the electric field increases in Region I of the oxide and decreases in Region II of the oxide. The steady state is reached when the entire potential V_{GB} is dropped across Region I, and the field in Region II is zero. The potential distribution as a function of time is

shown in Fig. 3(c). The steady-state field at the interface is equal to V_{GB}/x_1 , and since $x_1 \ll x_0$, the steady-state field at $x = 0$ is much larger than the field before electron bombardment of magnitude V_{GB}/x_0 . If x_1 is constant, independent of the gate voltage as assumed, the steady-state field at the interface should increase linearly with V_{GB} . In terms of the charge induced in the semiconductor, the steady-state value of Q'_S denoted by $Q'_S(\text{SAT})$ is then linearly related to V_{GB} . The steady-state threshold voltage corresponding to $Q'_S(\text{SAT})$ is denoted by V'_{TS} . Using Eq. (1) and the relation $Q'_S(\text{SAT}) = -\epsilon_{ox}(V_{GB}/x_1)$, we obtain the following expression for V'_{TS}

$$V'_{TS} = V_T - (x_0/x_1)V_{GB} \quad (2)$$

Since, by assumption, x_1 is constant and x_0 is known, a plot of V'_{TS} vs V_{GB} should be linear with a slope of magnitude x_0/x_1 . An experimental plot of V'_{TS} vs V_{GB} for a p channel MOST is shown in Fig. 4. For $0 < V_{GB} \lesssim 4V$ the slope of the curve is 27, and for $x_0 = 1200\text{\AA}$ the experimental data yields a value for x_1 of 45\AA . Second-order effects come into play for $V_{GB} > 4V$, and the curve becomes horizontal; it is believed that this abrupt decrease in slope is partially due to high field effects (10^7 V/cm) at the interface [14].

A derivation of the time dependent buildup of charge in the oxide using the boundary conditions and assumptions given above is easily

carried out [14]. A simple circuit analog of the charging phenomena is shown in Fig. 5. At $t = 0$, electron bombardment starts and mobile electrons are transported across Region II leaving a positive charge on C_1 . The steady-state for the simple RC circuit is such that all the voltage V_{GB} is dropped across C_1 (i.e. Region I).

An experimental plot of $Q'_S(t)$ against the time of electron bombardment for $V_{GB} = +0.8V$ is given by curve (A) of Fig. 6. The value of the ordinate corresponding to the horizontal portion of curve (A) is $Q'_S(\text{SAT})$. Also shown by curve (B) of Fig. 6 is a plot of $Q'_S(t)$ vs t for a negative voltage during electron bombardment of $V_{GB} = -0.8V$. The gate voltage $V_{GB} = -0.8V$ is applied at $t \approx 2.6$ sec., while bombarding the device, and the result is a reduction of Q'_S to its initial value at $t = 0$. Note that if electron bombardment is stopped at any time during the bombardment cycle shown in Fig. 6, the value of Q'_S , and hence V'_T (see Eq. 1), for that time remains until subsequent electron bombardment changes the state of the oxide.

The charge-discharge cycle shown in Fig. 6 is the basic phenomenon that is utilized to devise an electron-beam activated charge-storage device. In the next section, electron bombardment sequences on an MOST device are discussed that allow the storage of a bit of information in areas of a few square microns.

THE MEMORY OPERATION

Using the procedure discussed in the previous section, we can easily change the threshold voltage of the MOST, in a reversible manner, by electron bombardment. The basic charge-discharge cycle shown in Fig. 6 is easily pictured if one correlates the values of Q_S' , Q_{SS} , and Q_{SB} to actual charge distributions in the MOS system. Figure 7 illustrates three different states of the MOS system for $V_G = 0$ after various bombardment sequences. The charge distribution in the oxide before electron bombardment is shown in Fig. 7(a). The positive charge in the oxide is the Q_{SS} charge that accounts for the initial threshold voltage of the MOST V_T . To simplify the discussion that follows, it is assumed that the Q_{SS} charge produces a value for V_T of $-3V$. If the MOST is bombarded at a positive gate voltage for a given time, additional changes are introduced in the oxide. Figure 7(b) illustrates the state of the MOST after such a bombardment schedule. The oxide is in a state that corresponds to a point on curve (A) of Fig. 6. Again for discussion purposes, the new threshold voltage V_T' for the charge distribution shown in Fig. 7(b) is taken as $-40V$. If the device with $V_T' = -40V$ is subsequently bombarded at V_{GB} negative, the new value of V_T' is $V_T = -3V$; the charge distribution after bombardment which is identical to that of Fig. 7(a), is shown in Fig. 7(c). The later bombardment sequence corresponds to the discharge curve (B) of Fig. 6.

Since $V_G = 0$ and $V_T' < 0$ for the charge distributions in Fig. 7, the value of g_{ds} is very small.

A storage device with nondestructive readout is obtained by using half of the channel, the left side, to store the information and the remaining half of the channel to read the information. The device is first set to the state $V_T' = -40V$ over the entire area of the channel (see Fig. 7(b)). The various charge distributions after electron bombardment to store and read a "1" and a "0" are shown in Fig. 8. Consider the sequence Figs. 8(a), (b), (c), where a "1" is stored on the left side (LS) of the channel, and the stored "1" is read on the right side (RS) of the channel. By electron bombardment of the LS of the channel at $V_{GB} < 0$, V_T' is increased from $-40V$ to $-3V$ as shown in Fig. 8(a). Since $V_G = 0$, the channel is not inverted and $g_{ds} \approx 0$. Even if V_G is set equal to $-5V$, only half of the channel is inverted and g_{ds} is still small. The charge distribution for $V_G = -5V$ with a "1" stored is shown in Fig. 8(b). If one is to read the stored information, the LS of the channel must be bombarded at $V_{GB} < 0$ to increase V_T' from $-40V$ to $V_T' = -3V$. Figure 8(c) illustrates the charge distribution for $V_G = -5V$ after bombardment at $V_{GB} < 0$. In this state (Fig. 8(c)), an inversion layer exists between the source and the drain and $g_{ds} > 0$. A large increase in g_{ds} upon reading the RS of the channel indicates that the LS of the channel has $V_T' = -3$, or equivalently, a "1" is stored on the LS of the channel. Before the next bit

is read, the RS of the channel is bombarded at $V_{GB} > 0$ to set it in the state $V_T' = -40V$. This sequence of bombardment conditions leaves the "1" stored in the LS of the channel for subsequent reading cycles.

Charge distributions illustrating the various states of the device when a "0" is stored and read are shown in Figs. 8(d), (e), and (f). To store a "0", the LS of the channel is not bombarded, and consequently, $V_T' = -40V$ over the entire length of the channel as shown in Fig. 8(d). If a voltage $V_G = -5V$ is applied to the gate $g_{ds} \approx 0$. Electron bombardment of the RS of the channel at $V_{GB} < 0$ yields a V_T' of $-3V$. Figure 8(f) illustrates the charge distribution in the MOST after the read cycle with $V_G = -5V$. The RS of the channel is inverted, but $V_T' = -40V$ for the LS of the channel; hence, after reading $g_{ds} \approx 0$ if a "0" is stored on the LS of the channel.

Information is stored and read by electron bombardment of small areas of the gate electrode while the entire gate electrode is at a fixed potential. In particular a "1" is stored by electron bombardment of a small area of the gate electrode at $V_{GB} > 0$ and the "1" is read by electron bombardment of an adjacent area at $V_{GB} > 0$ and monitoring the increase in g_{ds} . A zero is stored by not bombarding a given area of the gate electrode, and the "0" is read in the same manner as the "1", but no increase in g_{ds} occurs. A plan view of the MOST structure is shown in Fig. 9. The cross-hatched areas of the gate are

assumed to be in the state $V_T' = -3V$, and the remaining area of the gate is in the state $V_T' = -40V$. The area 1 of Fig. 9 represents a high conductance path between S and D and this function corresponds to an electron-beam-activated switch. The areas 2S and 3S indicate storage of a "1" and a "0", respectively. When the RS of the channel is read by electron bombardment of areas 2R and 3R, adjacent to areas 2S and 3S, an increase in g_{ds} is observed when area 2R is bombarded at $V_{GB} < 0$, but no significant increase in g_{ds} is observed when area 3R is bombarded at $V_{GB} < 0$. To store many bits of information, the electron beam is scanned along the width W of the device on the LS of the channel. By a combination of pulsing the beam and pulsing the gate voltage V_{GB} , the information is stored in areas $L/2 \times w$. The information is nondestructively retrieved by scanning the electron beam over the RS of the device while pulsing V_{GB} and the beam and monitoring g_{ds} .

The number of bits that can be stored is determined by total area of the gate $L \times W$ and the minimum area in which a bit can be stored which includes the distance between successive bits. For a spacing between bits of w the area per bit is $2w \times L$. Additional area must be allowed for the source and drain electrodes. The storage density and related topics are discussed more completely in the following sections. The main asset of storing and reading of information as described above is that only three terminals are required to store and

read all the information. In addition, the readout process is non-destructive and the sequence for reading is the same whether a "0" or "1" is read. The storage is stable and does not require rewriting the information, and no power is required to maintain storage of the information. Momentary or long-term removal of potentials applied to the device do not alter the stored information. By different electron-bombardment sequences, more complex logic functions can be performed. A simple two-input "and gate" charge configuration is illustrated by areas 4S1 and 4S2 of Fig. 9. If both 4S1 and 4S2 are bombarded at $V_{GB} < 0$, subsequent reading of 4R produces a large increase in g_{ds} . If area 4S1 or 4S2, but not both, is bombarded, a subsequent reading by electron bombardment of 4R will produce only a small increase in g_{ds} ; hence, a two input "and gate" is obtained in this manner.

A scanning electron microscope (SEM) [18, 19] is used to experimentally store and read information in an area of dimensions $L = 10 \mu\text{m}$ and $w = 5 \mu\text{m}$. Figure 10 shows three micrographs of a commercial p channel MOST device. An electron beam approximately $0.1 \mu\text{m}$ in diameter was scanned over the surface of the device, and the resulting secondary electrons were collected to provide a video signal that modulated the intensity of a synchronously scanned cathode-ray tube. A full frame was scanned in a minimum time of 0.256 sec., but partial scans over a small area of the device were performed in a minimum time of 8 msec. A secondary electron emission micrograph

illustrating the geometry of the device is shown in Fig. 10(a); the letters S, G, and D indicate the source, gate, and drain electrodes, respectively. The three bright balls are the gold lead bonds. The gate electrode appears white, because it is biased negatively with respect to the surrounding electrodes [18]. A high magnification micrograph of an area of the gate electrode is shown in Fig. 10(b); the channel length L is marked on the micrograph. The electron beam is scanned over the area of the device in a raster, and by suitable adjustment of the scan amplitude, smaller areas of a micrograph are scanned. A record of the small bombarded areas is obtained by overexposing the film for these areas. Figure 10(c) illustrates typical storage and reading areas obtained using the SEM. The entire gate area G is bombarded at $V_{GB} > 0$ to obtain $V_T' \approx -40V$. Area 1 represents the electron-beam-activated switch function as described in relation to area 1 of Fig. 9. Using the top of the gate electrode for storing information, we bombarded area 2S at $V_{GB} > 0$ to store a "1" while areas 3S and 4S were not bombarded to store two successive "0"s. Each area is scanned in approximately 8 ms. To read the area 2R (not shown in white for clarity) is scanned at $V_{GB} > 0$ resulting in a high conductance path like 1. The area 2R is bombarded at $V_{GB} > 0$ to attain $V_T' \approx -40V$ before area 3R is read. When area 3R is bombarded, essentially no increase in g_{ds} is observed, thus indicating that area 3S is not in the "1" state. A similar result is obtained when area 4R is bombarded at

$V_{GB} < 0$. To summarize, the procedure for storing and reading information, as described in this section, in areas 5 microns \times 5 microns was experimentally achieved by using the SEM for selective bombardment of areas of a commercial p channel MOST.

PRACTICAL MEMORY CONFIGURATIONS

Once the basic electron beam activated switch is described, many memory configurations are possible. Here we consider a few memory schemes to illustrate pertinent design variables and the versatility of the device. Memory schemes that provide electron beam storage and electronic readout are also considered.

For the memory operation described in the previous section, the areas used for reading must be reset each time a bit is read. If there is any beam wobble during the read or reset cycle, a portion of the stored information is erased after many read cycles, the value of g_{ds} corresponding to a stored "1" will decrease. A structure that reduces the effects caused by beam wobble and beam misalignment is shown in Fig. 11. The structure is essentially the same as that shown in Fig. 1 except for the addition of diffused p^+ islands in the center of the gate, shown as cross-hatched squares in Fig. 11(a). Each bit has a p^+ island. Referring to Fig. 11(b), we used the LS of the channel for storing the information and the RS side of the channel for reading. Since the store and read areas are a distance L_2 apart, beam wobble during storing or reading will not significantly alter the stored information. Note that since the additional p^+ diffused areas are spaced by a distance L_2 along the width W of the device, the adverse effects of electron beam misalignment with a given bit along this dimension are reduced. The

additional area consumed by the p^+ islands reduces the bit packing density, but the added assurance of bit integrity after a number of read cycles may justify the use of this lower packing density structure.

Construction of "and gate" arrays is accomplished by diffusing a row of small p^+ islands separated by a distance w_1 . The MOS structure is placed over the space between the islands. A nine input "and gate" array is shown in Fig. 12(a). The tenth column of the device shown in Fig. 13(a) is used to read the various rows. A significant increase in the conductance between terminals A and B is observed only if all nine areas, of dimensions $L_1 \times w_1$, between the p^+ islands are inverted. Figure 12(b) illustrates a ten input "and gate" which utilizes electronic readout of the rows. For a configuration of k rows, $(k+2)$ terminals are needed. By reading the information electronically, the access time and read cycle time depends only on interelectrode capacities and the speed of the access circuits.

High packing density coupled with high speed readout is obtained by arranging electron-beam-activated switches in an array. A typical array is shown in Fig. 13(a), and the cross sectional view of one storage element of the array is shown in Fig. 13(b). For the memory shown in Fig. 13 the electron beam is used only to store the information. A typical storage area is shown in row 1 - column 1 of the array. If upon reading the information the conductance between row 1 and column 1 is large a "1" is stored in this position; if the conductance is small a "0"

is stored in this position. The information is read by row-column access circuits. The structure of Fig. 13 is very simple, and therefore, large packing densities should be attainable. Since the readout is performed by access circuits, the reading speed and minimum access time are determined by the interelectrode capacities and the speed of the access circuitry. An electron-beam-activated switch EBAS array is of particular advantage when a given set of stored information is read many times before the storage is erased or if only a portion of the information is altered during successive read cycles.

The packing density of the EBAS structure of Fig. 13 will now be discussed. With reference to Fig. 13, one bit requires a total area, including diffusions and spacing of the bits, of $(L_1 + L_2 + L_3 + L_4) \times (w_1 + w_2) \text{ cm}^2$. This yields a bit-packing density for the EBAS memory of

$$\text{PD} = 1 / (L_1 + L_2 + L_3 + L_4)(w_1 + w_2) \text{ bits/cm}^2 .$$

The dimensions L_1 and w_1 are determined by the spot diameter of the electron beam, and for very small spot diameters ($\sim 1 \mu\text{m}$) the minimum size of L_1 and w_1 will depend on the resolution of the process used to define the diffusion and electrode patterns. Pattern dimensions L_2 , L_3 , L_4 , and w_2 depend on the resolution of the pattern generating process, e.g., photolithographic techniques for mask making. If we assume that an $8 \mu\text{m}$ diameter electron beam is used to store the

information and that a practical pattern dimension obtainable by photolithographic techniques is 5 μm (silicon technology), a conservative estimate of the PD for the EBAS memory is

$$\text{PD} = [(8 + 5 + 5 + 5)(8 + 5) \times 10^{-8}]^{-1} = 3.4 \times 10^5 \text{ bits/cm}^2 .$$

An estimate of the PD for other structures discussed in this section is obtained by similar calculations.

Only row-column access is illustrated for the EBAS memory of Fig. 13, but the basic EBAS is amenable to many different word arrangements. For the system designer, various word arrays and associated access circuitry are possible that allow a reduction in both the access time and the time to read a given word.

In the next section factors that determine the rate at which information can be stored and read by the electron beam are discussed. Since the total number of bits NB in an array is determined by the total area of the array, the factors that determine the maximum usable storage area are considered.

DISCUSSION

It is now necessary to discuss the rate at which information is stored in the MOS media. Experimentally it is found, for an average electron beam current density² of the order of 10^{-3} A/cm², that an approximate dosage of 10^{-6} to 10^{-5} C/cm² is needed to attain a detectable change in the threshold voltage of the MOS system. For the purpose of the discussion that follows it is assumed that a value for the electron beam dosage Q_{EB} of 5×10^{-6} C/cm² is needed for storage to occur. If \bar{J}_B is the average current density of the electron beam, and if τ_B is the time the beam bombards a given storage element of area A_s , then $Q_{EB} = \bar{J}_B \tau_B$. Then for a given beam current density \bar{J}_B , the time to store a bit is given by the following expression³

$$\tau_B = \frac{5 \times 10^{-6}}{\bar{J}_B} \quad (3)$$

² If A_s is the area scanned by the electron beam and if I_B is the beam current, the average current density \bar{J}_B is defined as I_B/A_s .

³ Equation (3) assumes that the meaningful parameter is the electron beam dosage of 5×10^{-6} C/cm². The constancy of $\bar{J}_B \tau_B$ is experimentally verified for the range $10^{-5} < \bar{J}_B < 10^{-2}$ A/cm².

For microsecond bit storage, \bar{J}_B must be 5 A/cm^2 . Since the charging time constant τ_c is at least five times the discharge time constant τ_d (see Fig. 6 and related discussion), the oxide charging process determines the electron beam information storage rate. The time τ_d , unlike τ_c , decreases as the value of V_{GB} during discharge is made more negative [14].

To increase the PD, a small spot size is needed. To increase the storage rate, a high current density is needed. In addition, to obtain a large number of bits NB, the electron beam deflection system must be able to maintain a small spot diameter over a large area. Various deflection aberrations increase the spot diameter as much as an order of magnitude when the beam is deflected only a few inches from the center of the storage area [12]. A microspot tube designed by Schlesinger [10, 12] that is capable of maintaining an $8 \mu\text{m}$ spot diameter over a 4.25 in. diameter circle is used to illustrate the storage capacity and information storage rate of an EBAS memory (Fig. 13).

Table I is a summary of the pertinent characteristics of the microspot tube. The beam voltage V_B determines the maximum total thickness of the thin films over the channel region of the device [14]. With Eq. 3 and the value of J_B obtained from Table I, the storage time per bit is approximately $2 \mu\text{s}$; this corresponds to an information storage rate of 0.5×10^6 bits/sec. If it is assumed that the $8 \mu\text{m}$ spot diameter is maintained over a $10 \times 10 \text{ cm}^2$ area of the tube face, the

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value NB can be obtained by using the PD figure of 3.4×10^5 bits/cm² given in the previous section for an 8 μm diameter spot size. Then the value for NB for the EBAS memory incorporated in the microspot tube is 3.4×10^7 bits. For the square array of 3.4×10^7 bits, approximately 5,830 rows and 5,830 columns are needed to form the array. The random access time for storing information is determined by the electron beam deflection system and access circuitry; access times of a few microseconds or less should be attainable. It is possible that the random access time for this memory may be smaller than that of a ferrite core memory, since only low-level signals are needed for readout. A summary of the characteristics of the EBAS memory utilizing the electron optics of the microspot tube for storage and a two-dimensional array with address circuitry for reading is given in Table II.

A very important attribute that an erasable memory must possess is stability. In terms of the electron beam bombardment of the MOS device, the charge in the oxide once stored must remain stored until subsequent electron bombardment, and the storage media must be capable of many storage cycles without device degradation. Experimental results indicate stable storage over periods of a few months at ambient conditions; and no significant reduction in V_T when the device is subjected to temperatures of 150°C. An area 10 × 30 μm was subjected to 24 hours of continuous electron bombardment or approximately 5×10^5 switching cycles. The result was a reduction in the amplitude

of the readout pulse of approximately 30%. Part of the reduction in the amplitude of the g_{ds} pulse ($\sim 10\%$) is due to a decrease in the electron beam current over the twenty-four hour period of electron bombardment. Oscillographs of the gate pulse and the store-read pulse at the beginning and end of one hour of continuous electron bombardment are shown in Fig. 14(a), (b), respectively. The gate voltage V_{GB} is pulsed at ± 2.5 volts; V_{GB} and g_{ds} (Fig. 14) increase in the downward direction of the ordinate. No significant decrease in the pulse amplitude is observed after one hour of electron bombardment. It should be noted that the lifetime of the EBAS memory shown in Fig. 13 is increased since electron bombardment is not used for reading the information.

In discussing the characteristics of the EBAS system a specific device, the microspot tube, is used to obtain quantitative estimates of the various memory parameters. For a faster storing rate, J_B must be increased (see Eq. 3), hence field emitter guns [20] and the associated electron optics may increase the rate for storing information by at least an order of magnitude. Interconnection problems between the electron beam storage media and the access circuits can be accomplished by locating the access circuit array adjacent to the storage media. It may also prove to be advantageous to incorporate diodes on the storage media or use the diodes in the memory structure to provide electron-beam-induced signals to serve and position the electron beam.

Further simplification of the system accrues from the fact that a portion of the logic circuitry and the storage media can be mounted in a closed vacuum system, e.g., the microspot tube. The simple, linear geometry of the EBAS memory should allow use of thin film techniques and electron beam exposure of photoresist to increase the packing density.

An idea of the capability of the EBAS memory, as compared with other types of computer memories, is obtained by considering the various performance characteristics of the memory example given in Table II. For storage, the access time of the EBAS memory is comparable or better than the access time of a ferrite core memory, but the information transfer rate of EBAS memory only approaches that of a magnetic tape memory. The storage capacity of the EBAS memory is similar to the storage capacity of a magnetic drum memory [1]. For reading the information, the EBAS memory is similar to the access time and information transfer rate of a ferrite core memory while maintaining the storage capacity similar to that of a magnetic drum memory. From this rough comparison it is inferred that the EBAS competes with available memories if once the information is stored many random access read cycles (short access time coupled with a high information transfer rate and large storage capacity) are performed before a significant portion (say greater than 10^4 bits) of the memory storage is altered. It should be noted that since the storage access time for the EBAS memory is much shorter than the access time of a

magnetic disk memory [1] (typically 100 ms) of comparable bit capacity approximately 10^4 bits can be stored in the EBAS memory in the time it takes the disk memory to locate the first storage area. Once the magnetic disk memory has been indexed, the higher information storage rate allows approximately two to four times the storage per unit time than the rate obtainable with the EBAS memory.

If various areas of an MOS structure are bombarded for a given time but the gate voltage during bombardment V_{GB} is different for each area, the value of V_T for each area is different. The latter fact allows the storage of analog information.⁴ Figure 15 illustrates the store and read cycle. An electron beam is scanned at a constant rate over the upper half of the channel, but V_{GB} is varied along the width of the channel as shown in Fig. 15(a). The analog information is read by bombarding small areas of the gate on the lower half of the channel and measuring g_{ds} . Each area is erased before proceeding to the next area. Figure 15(b) shows the linear plot of g_{ds} along W indicating retrieval of the linear ramp stored in the upper half of the channel. An array of EBAS's can also be used to convert analog information to digital information; the magnitude of g_{ds} for a given row-column

⁴ The authors wish to thank D. A. Hodges of Bell Telephone laboratories for posing the question: Could your device be used to store analog information?

position in the array provides a digital signal of a magnitude proportional to the analog information that is stored at that location.

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LIST OF TABLES

Table
No.

- I Microspot Tube Characteristics
- II Characteristics of EBAS Memory Using the
Microspot Tube

TABLE I

Microspot Tube Characteristics (Ref. 12)

Beam current	1.5 μ A
Average current density, \bar{J}_B	2.7 A/cm ²
Spot diameter	8 - 9 μ m
Useful screen diameter	10.8 cms
Beam voltage V_B	16 - 20 kV
Length of tube (approx.)	43 cms
Maximum tube diameter (approx.)	13 cms

TABLE II

Characteristics of EBAS Memory
Using the Microspot Tube (Ref. 12)

Storage capacity	3.4×10^7 bits
Rows \times columns	5,830 \times 5830
Random access time for storage (estimate)	Time it takes to position beam $\sim 1 \mu\text{S}$
Information transfer rate for storage	$\sim 5 \times 10^5$ bits/S
Random access time for reading	Determined by array circuitry $\sim 0.1 - 10 \mu\text{S}$
Information transfer rate for reading (estimate)	Determined by array circuitry $10^6 - 10^8$ bits/S

LIST OF FIGURES

Figure No.

- 1 Schematic diagram of a cross-section of the metal-oxide-semiconductor transistor.
- 2 Schematic diagram illustrating: (a) the MOS structure, (b) the continuous charge distribution in the oxide and the semiconductor, and (c) the lumped approximations to the actual charge distributions.
- 3 Graphical display of the charge distribution (a), the electric field distribution (b), and the potential distribution (c) in the oxide during electron bombardment. The distributions are illustrated for $t = 0$, $t = \tau_c$, and $t \gg \tau_c$.
- 4 Experimental plot of $-V_{TS}^i$ against V_{GB} for a p channel MOST.
- 5 An electrical circuit analog that models the electron beam induced charging of the oxide.
- 6 A plot of Q_S^i/q vs the bombardment time. Curve (A) is a charging cycle with $V_{GB} = 0.8V$. Curve (B) is a discharge curve for $V_{GB} = -0.8V$. The discharge begins at $t \approx 2.6$ S.

Figure No.

- 7 Schematic diagrams of a MOST device illustrating various charge distributions in the oxide. (a) Charge distribution before electron bombardment for $V_T = -3V$. (b) Charge distribution in the oxide after electron bombardment with V_{GB} positive and $V_T^i = -40V$. (c) Charge distribution in the oxide after electron bombardment of the charge configuration shown in (b) with V_{GB} negative.
- 8 Charge distribution in the oxide using the left side of the channel for storing and the right side of the channel for reading. The sequence (a), (b), (c) illustrate storing and reading a "1", and the sequence (d), (e), (f) illustrates storing and reading a "0".
- 9 Plan view of the MOST. The cross-hatched areas of the gate illustrate charge patterns in the oxide such that $V_T = -3V$. The remainder of the gate has $V_T^i = -40V$.
- 10 Micrographs of a p channel MOST obtained with a scanning electron microscope. (a) Low magnification micrograph showing the source S, the gate G, and the drain D regions of the device. (b) High magnification micrograph of the gate region of the MOST with $L = 10 \mu m$. (c) Typical areas of the gate that were selectively bombarded to demonstrate the operation of the memory.

Figure No.

- 11 (a) A memory array which uses electron beam read and store cycles. (b) A cross section of the array through one of the p^+ islands.
- 12 (a) A memory array of a nine input "and gate" with electron beam readout. (b) A ten input "and gate" which uses electronic readout.
- 13 A plan view of an electron beam activated switch (EBAS) array (a), and the cross section of the array (b).
- 14 Oscilloscope traces of V_{GB} (a), the change in g_{ds} at the beginning of the experiment and after electron bombardment for eight hours (b).
- 15 Schematic diagram illustrating the storage of analog information in the upper half of channel (a), and the reading of the information in the lower half of the channel (b).

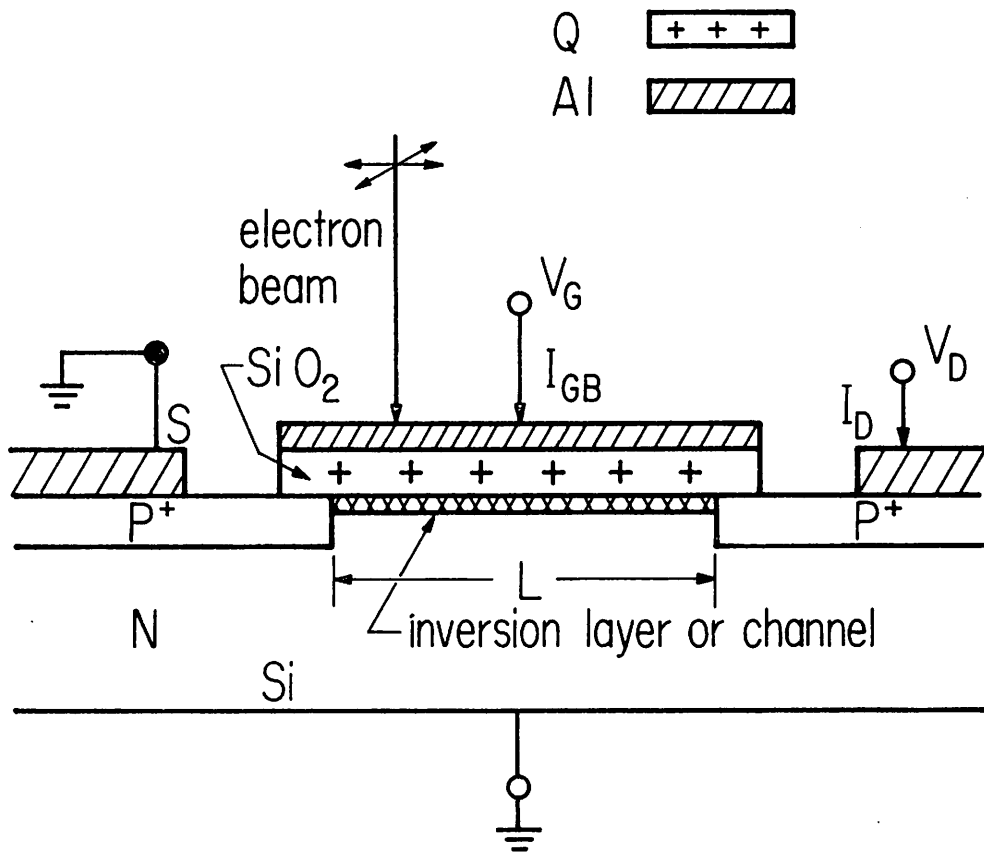


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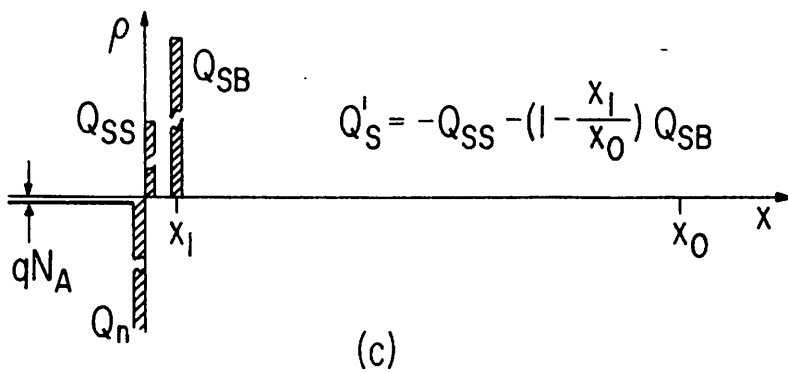
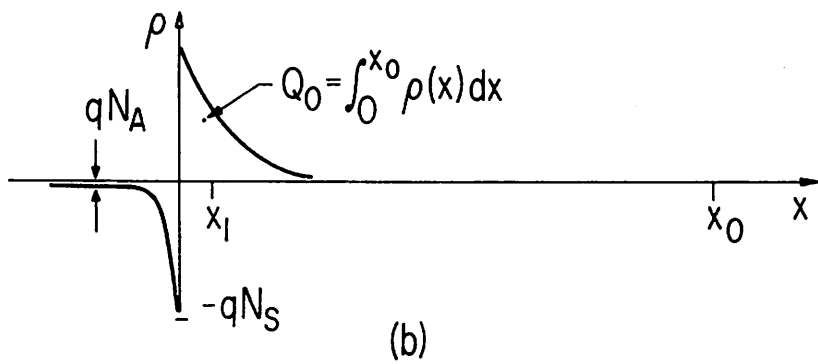
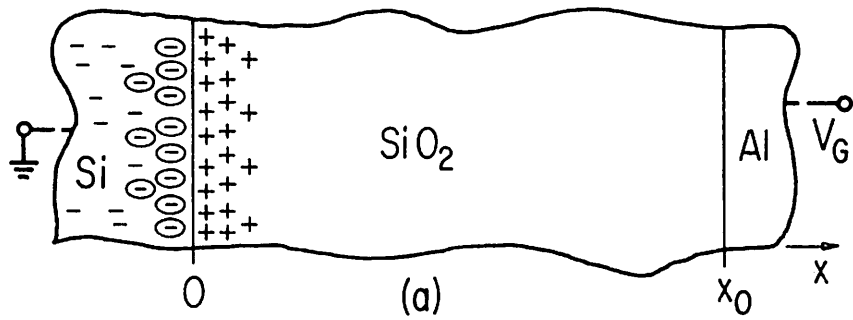


Fig. 2.

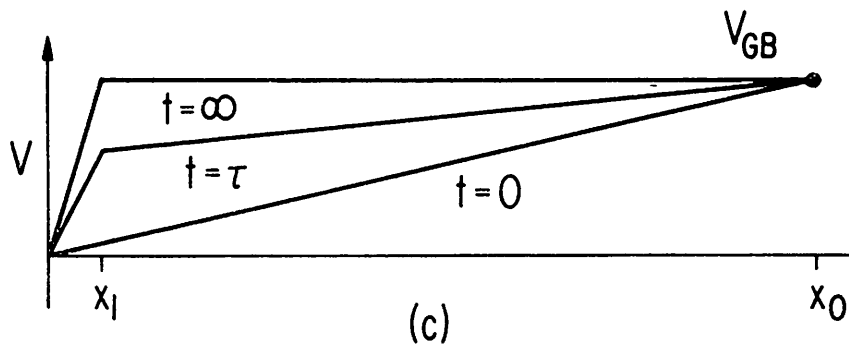
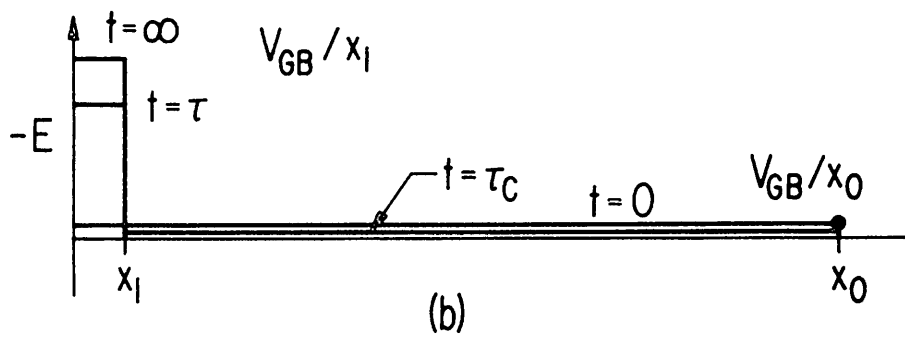
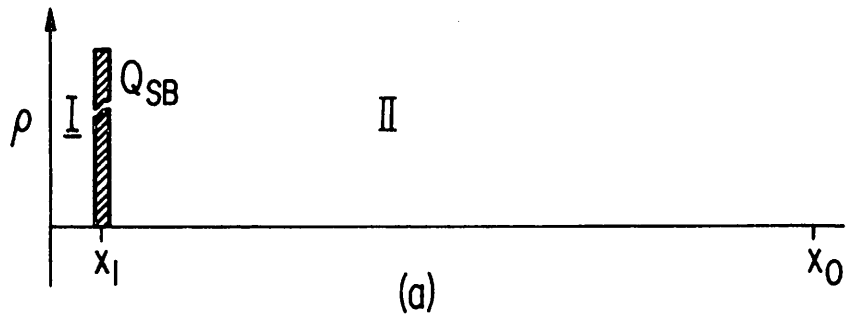


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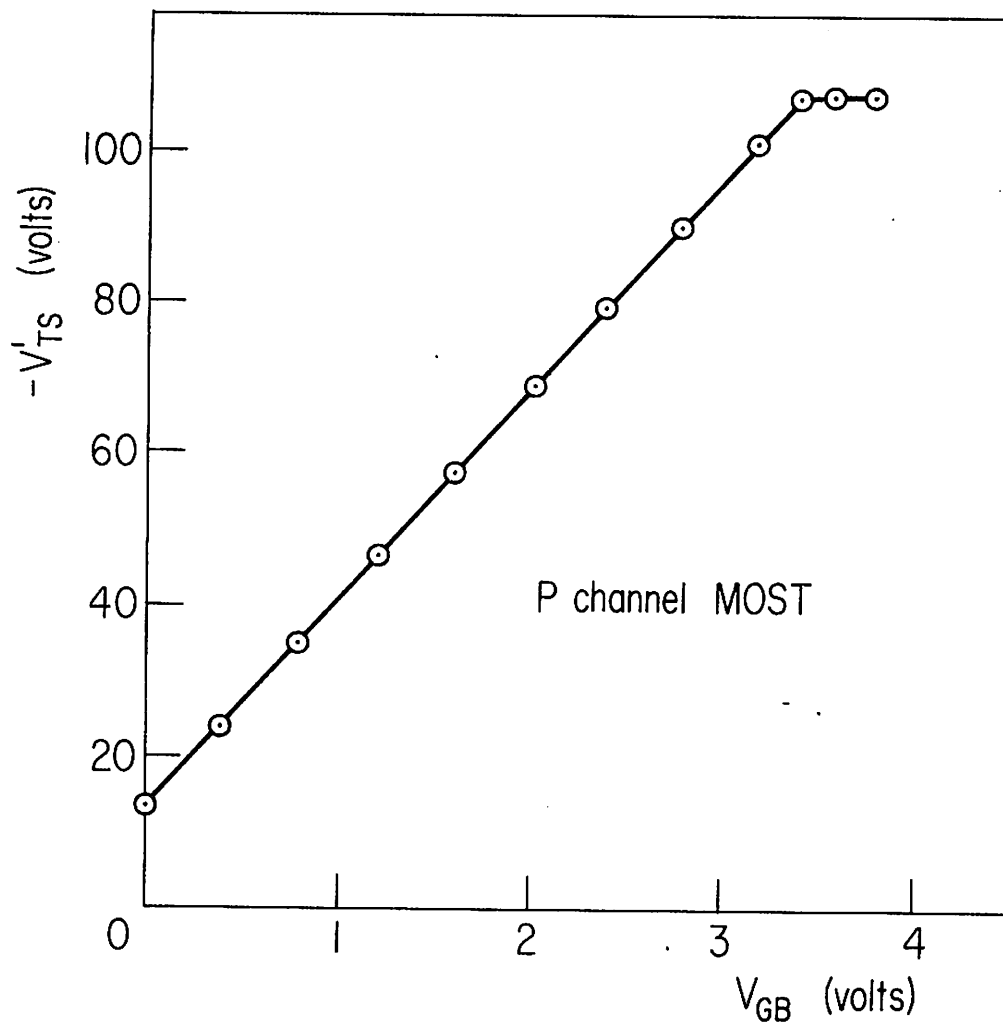


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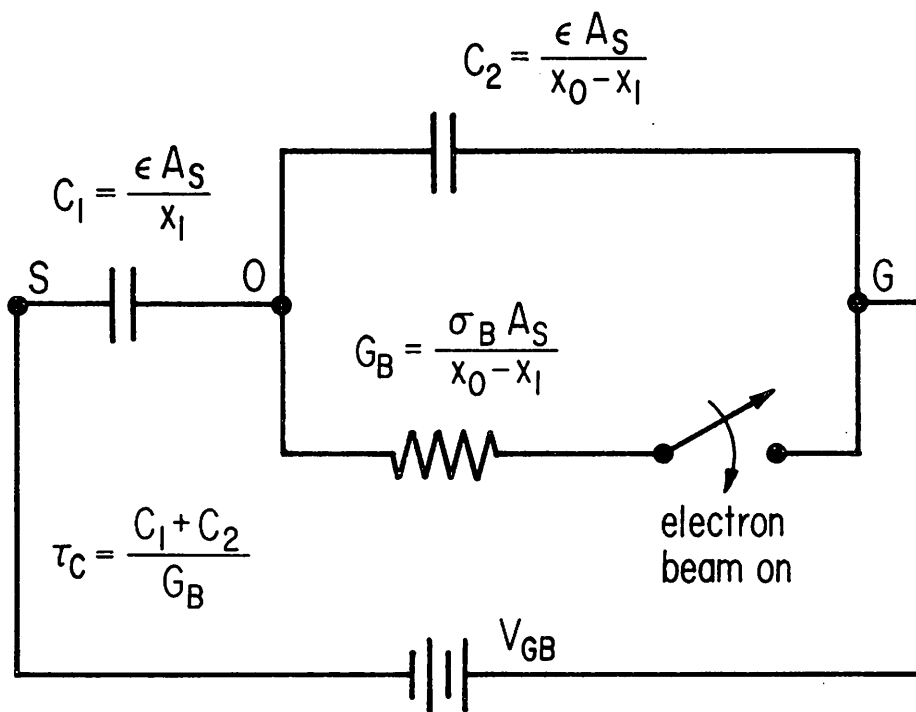


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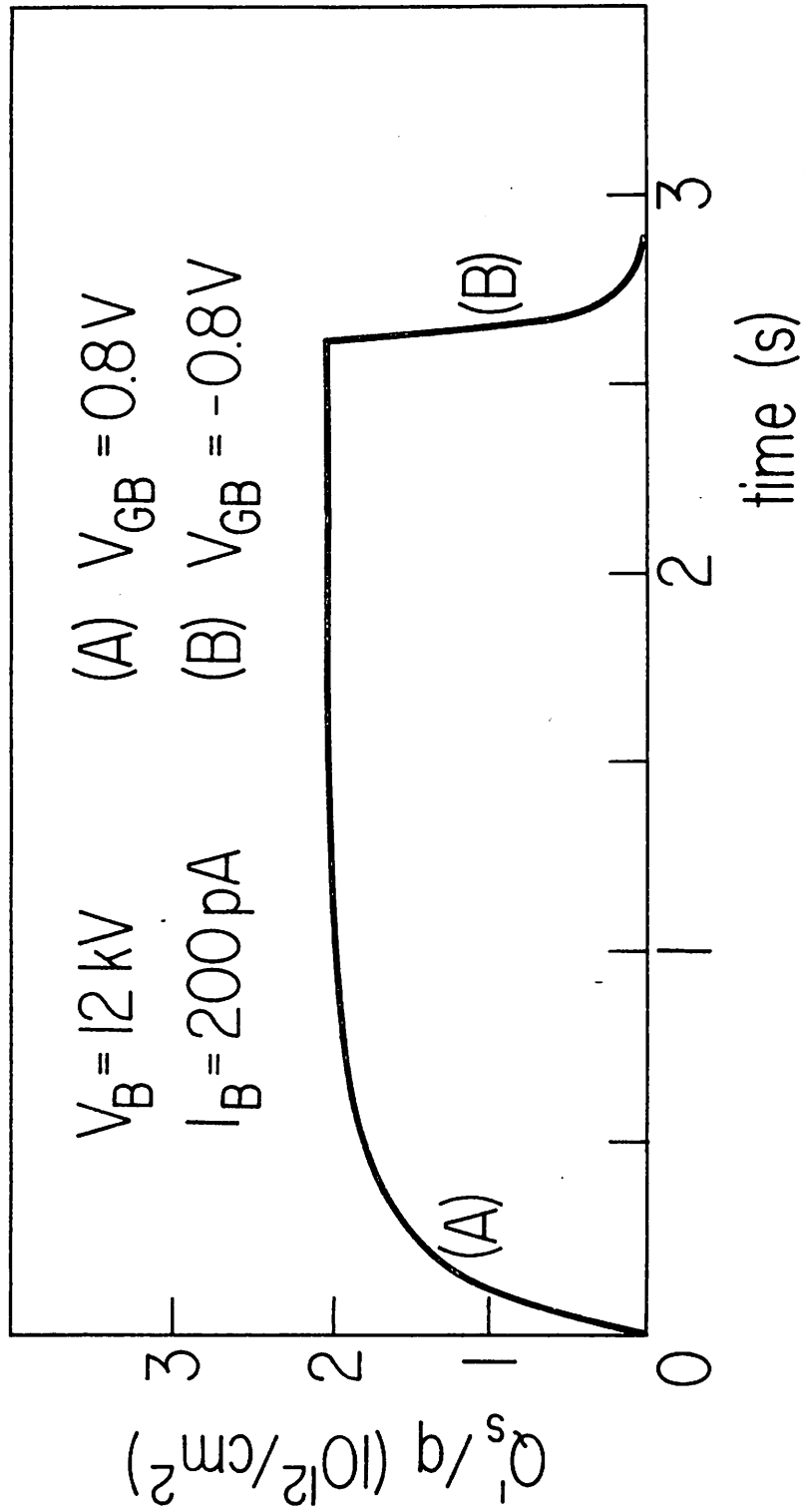


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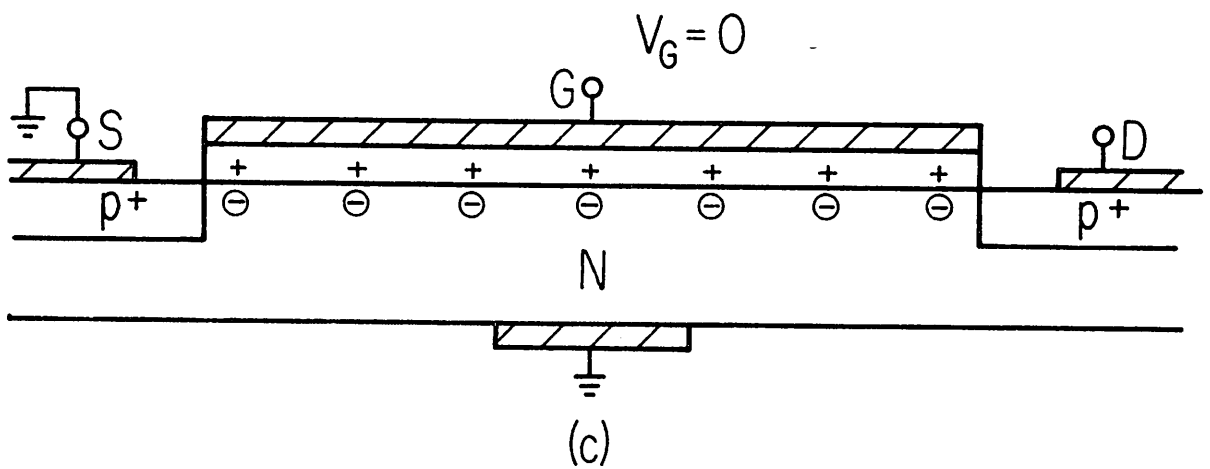
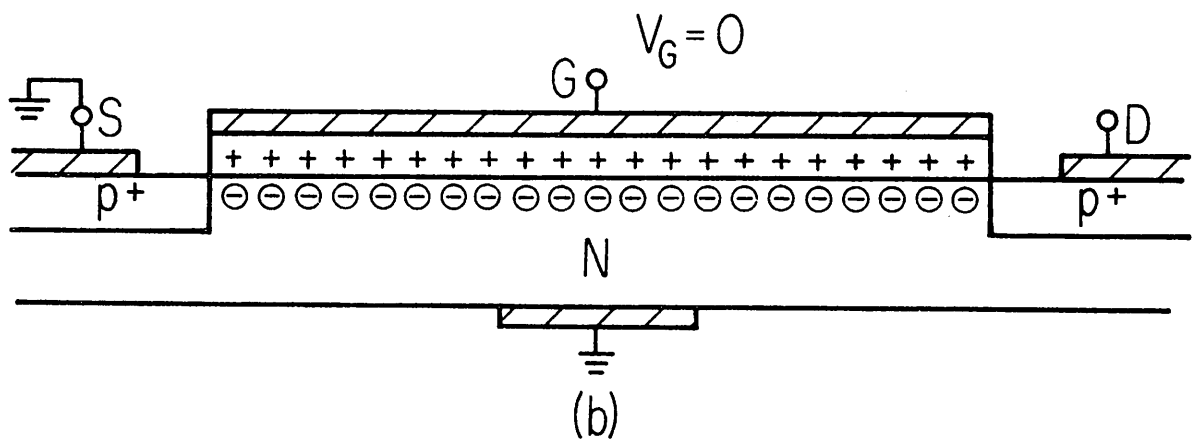
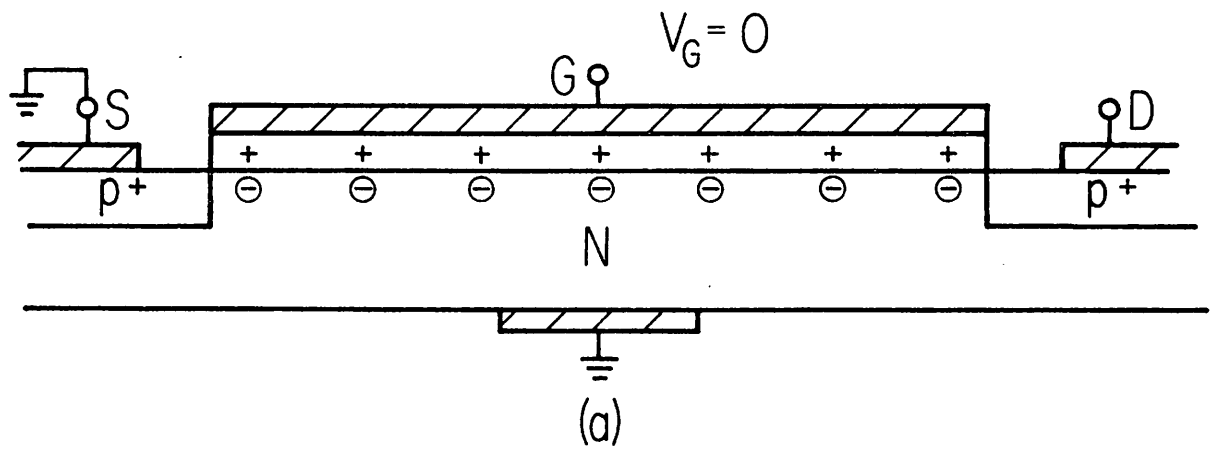


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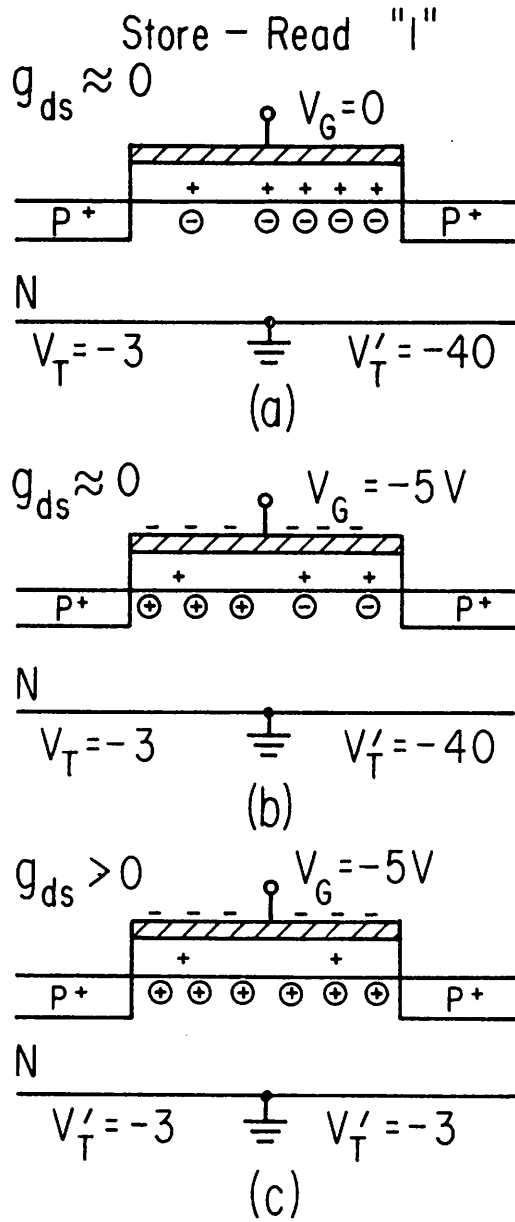


Fig. 8.

Store - Read "0"

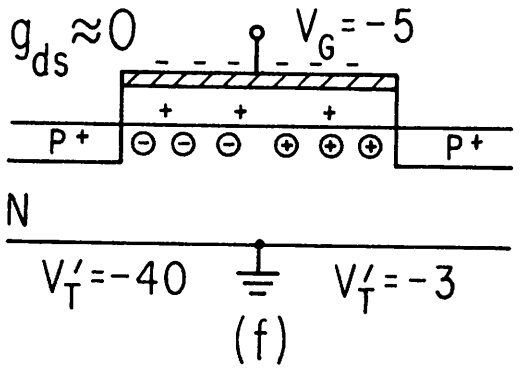
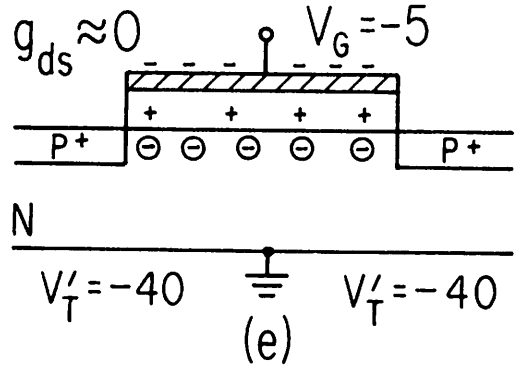
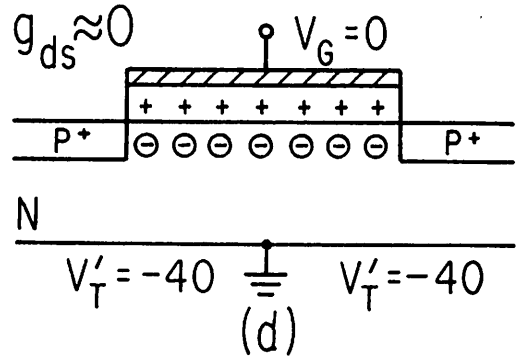


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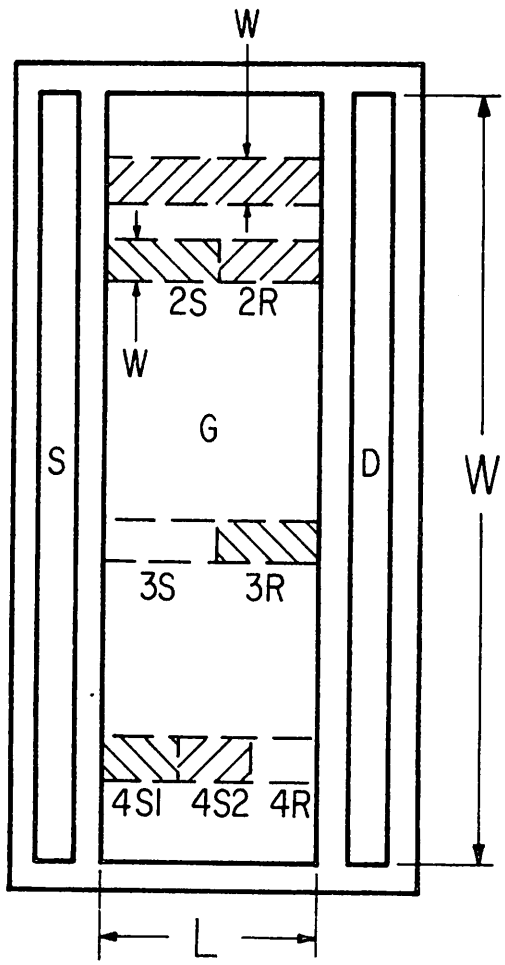
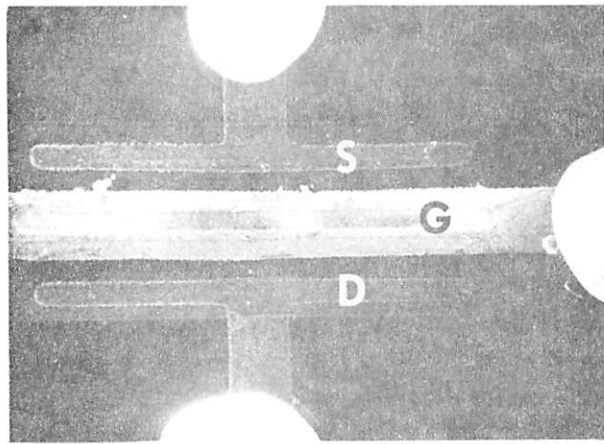
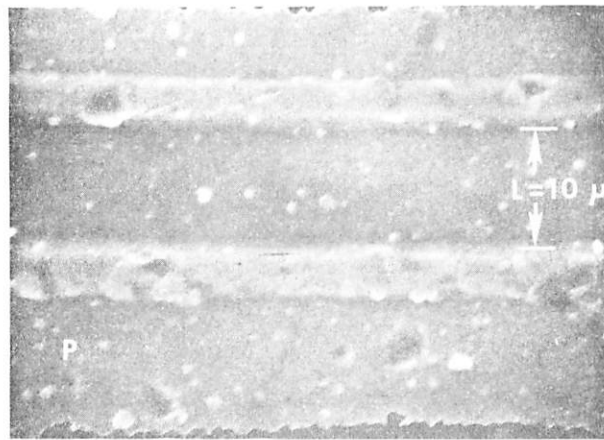


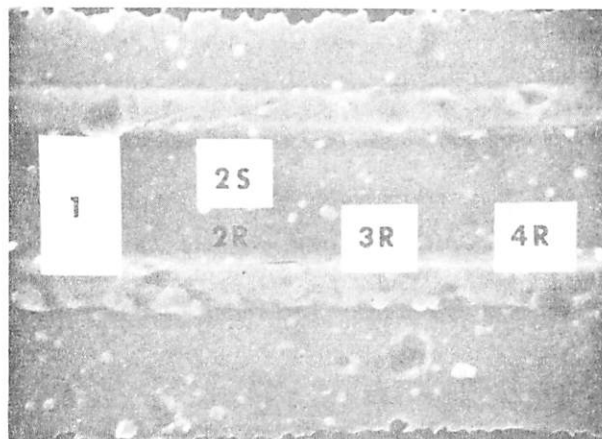
Fig. 9.



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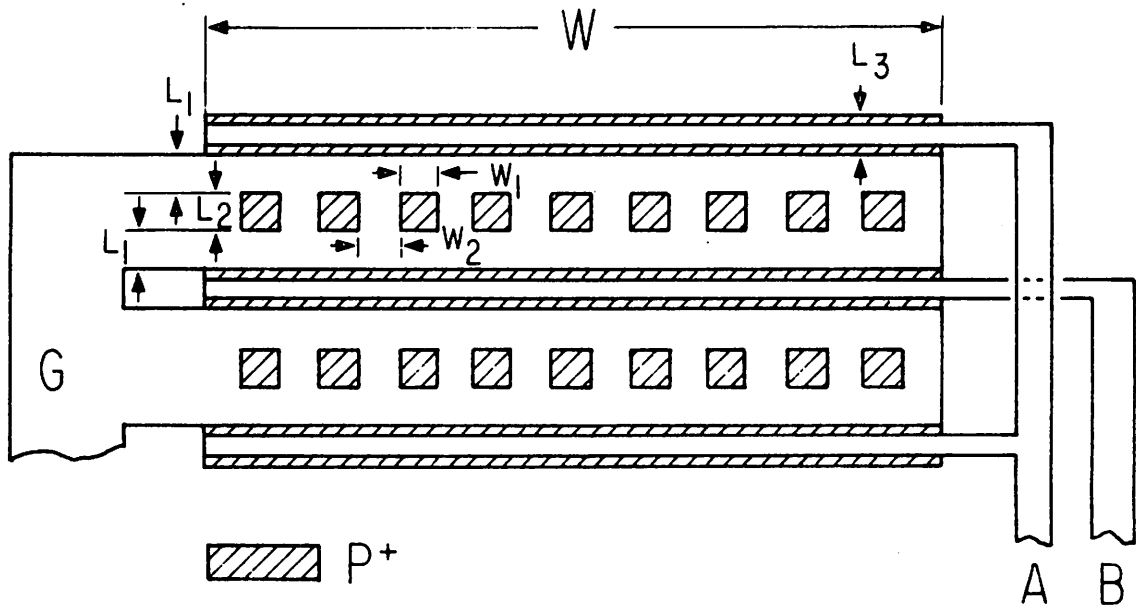


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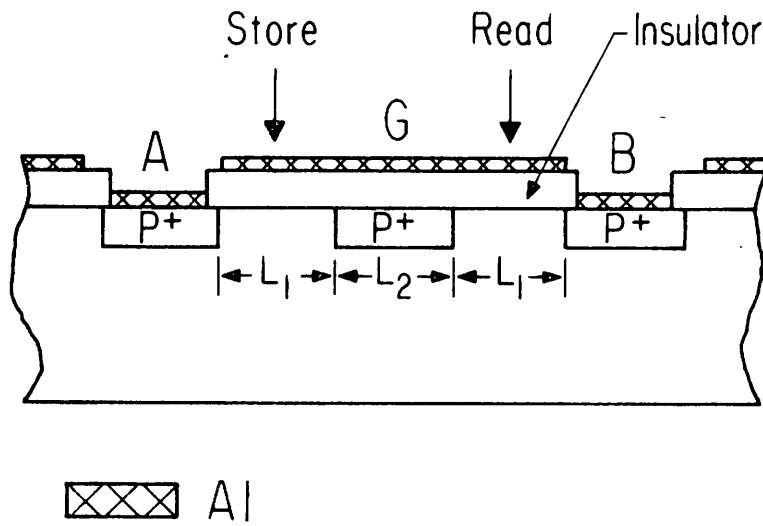


(c)

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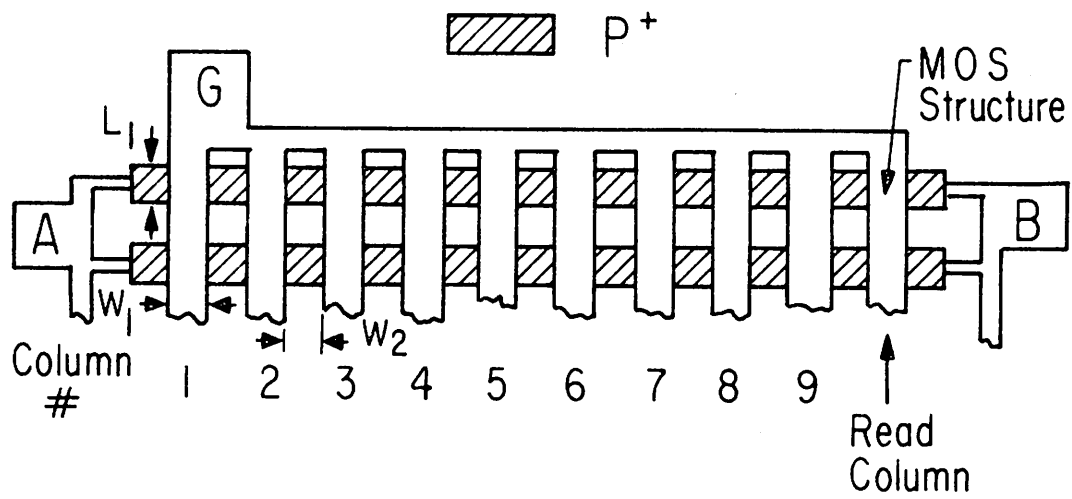


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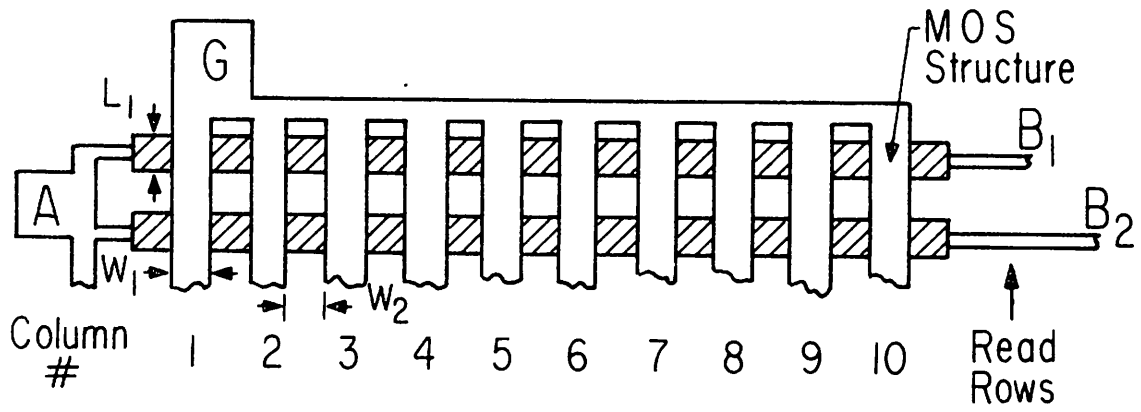


(b)

Fig. 11.



(a)



(b)

Fig. 12.

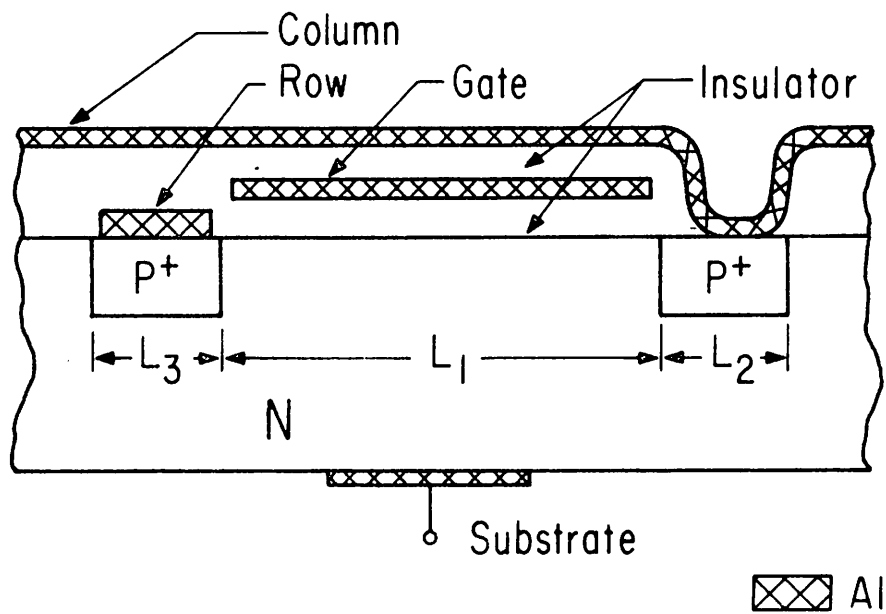
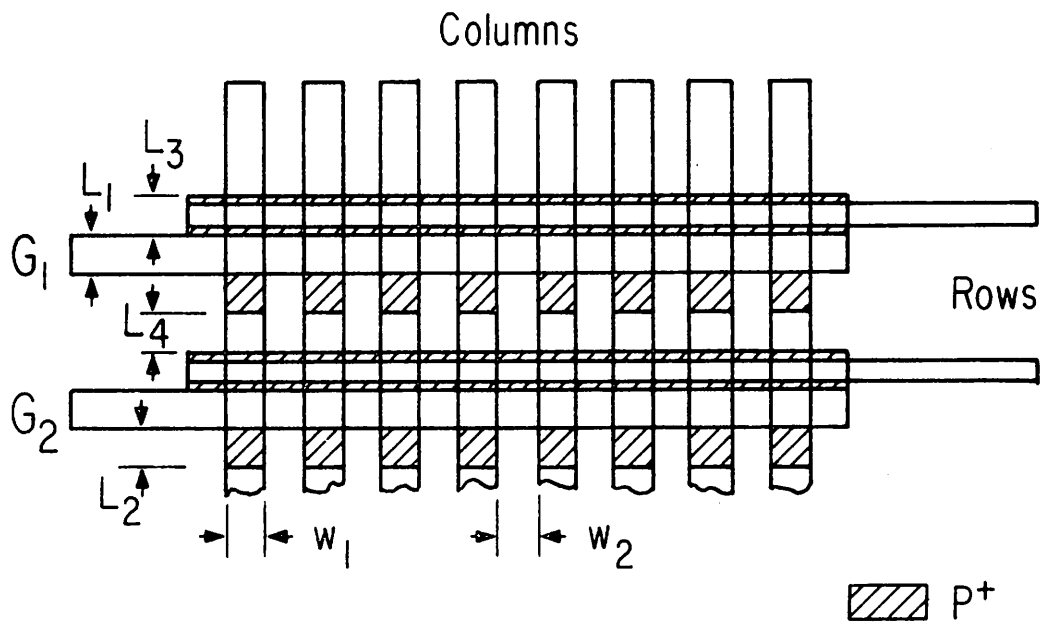


Fig. 13.

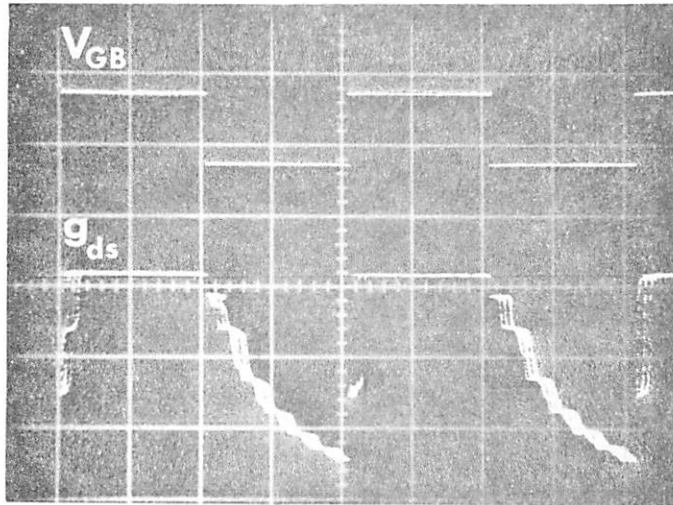
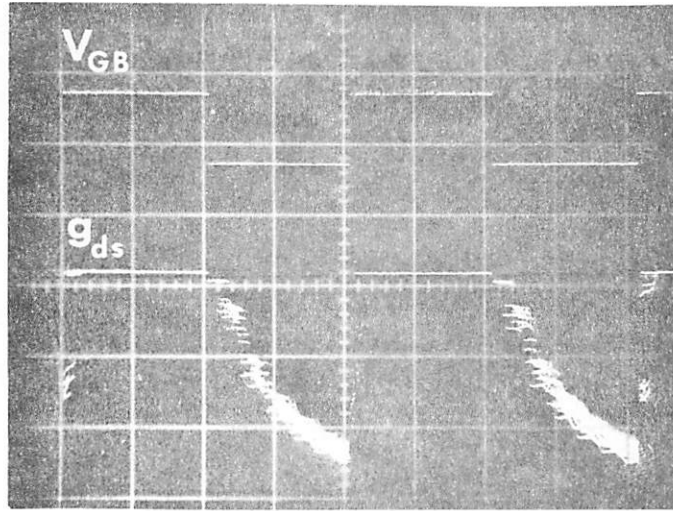


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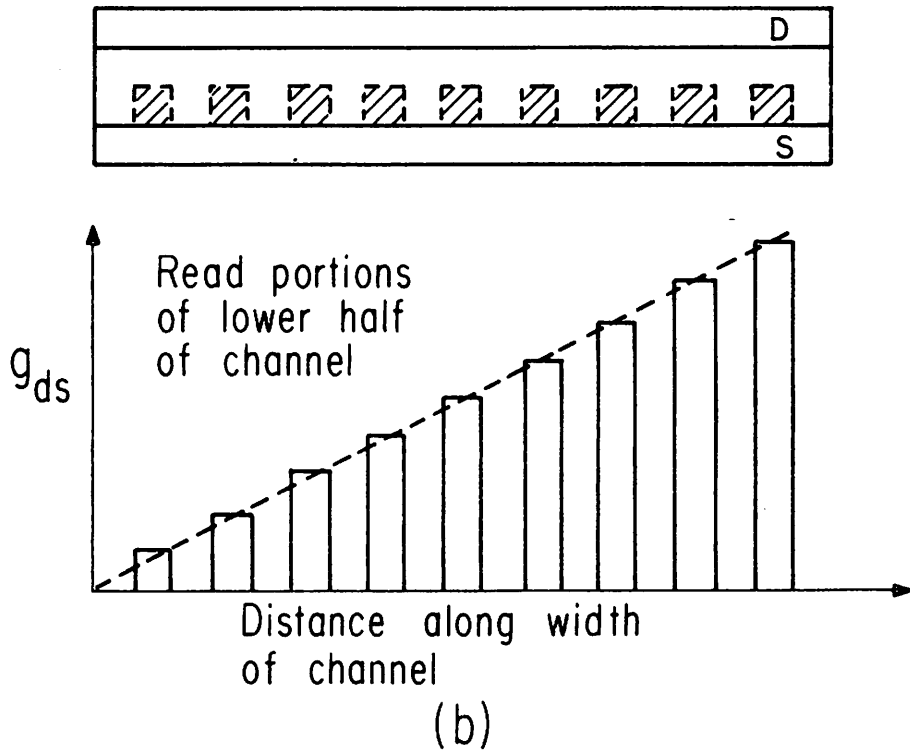
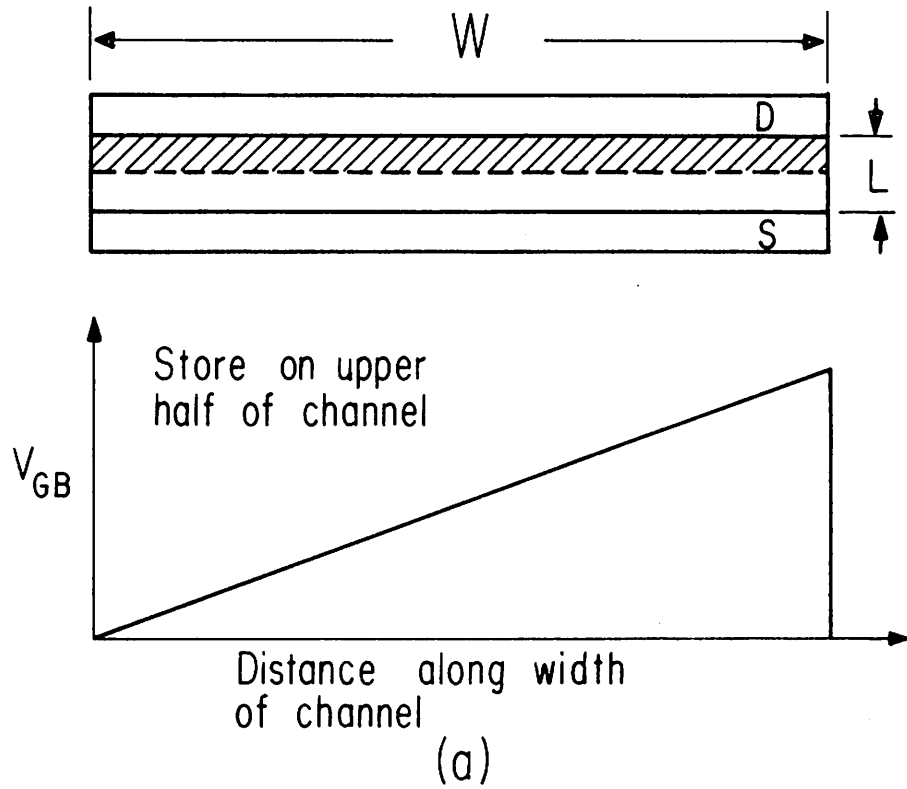


Fig. 15.