MONOLITHIC WIDEBAND AMPLIFIERS

by

Bruce A. Wooley

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INTRODUCTION

A general design approach for wideband lowpass amplifiers is difficult to establish because of the diverse applications for such amplifiers. Design usually proceeds on the basis of the specific situation for which the amplifier is intended. However, in integrated circuits a single design approach, flexible enough to meet a wide range of specifications, becomes increasingly desirable because of the high cost associated with realizing a design prototype. The primary objective of this report is the formulation of a flexible design for a fully integrated, temperature insensitive, wideband amplifier.

Because of its adaptability,a building block approach is adopted for meeting typical overall amplifier specifications. Most of the report is concerned with the realization of the individual building blocks. A completely monolithic structure, with direct coupling capability between blocks, is specified.

Typically, desensitization of lowpass amplifier configurations is accomplished through the use of negative feedback. A feedback approach is particularly suitable

for integrated circuits because the response can often be cast in terms of ratios of passive feedback elements. Such ratios can usually be realized with good precision in integrated circuits, even though actual element tolerances are quite large. Hence, considerable emphasis is given in this study to a number of fundamental feedback configurations.

The basic feedback configurations are studied on a small-signal basis through computer-aided analysis. For all but elementary configurations, precise analysis is generally limited to numerical evaluations whether or not a computer is used. The use of the computer, however, allows the investigation of a large number of designs in order to reach a general conclusion.

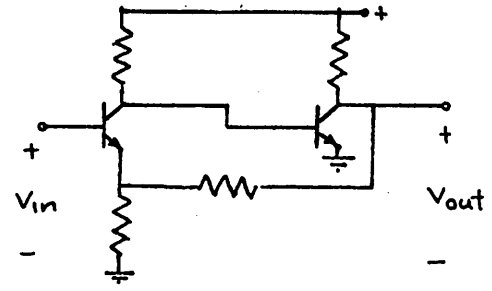
CHAPTER 1: BUILDING BLOCK AMPLIFIERS

I. Review

The background for this study is provided primarily by the work of Brodersen[1]; Solomon and Wilson[2]; and Breuer, Buie, Schmunk, Braun and Sandlar[3]. These authors have considered in detail the realization of wideband lowpass amplifiers in integrated circuits.

In order to establish a temperature insensitive amplifier response while maintaining a large bandwidth, some form of negative feedback is generally employed. Brodersen has given attention to all of the basic feedback configurations shown in Fig. 1. Particular emphasis was accorded the feedback pairs and the corresponding two device local feedback cascades. Complete integrated realizations were produced for the shunt-series pair and the shunt-series cascade.

The series-series triple of Solomon and Wilson is representative of typical integrated amplifiers. In the paper the authors first discuss the suitability of the triple, shown in Fig. 1(f) in basic form, for desensitized wideband amplification. Then the configuration is analyzed in detail and a full monolithic design is realized.



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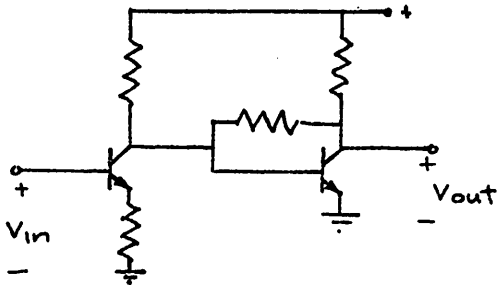
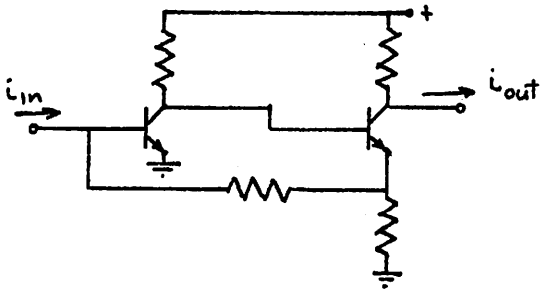
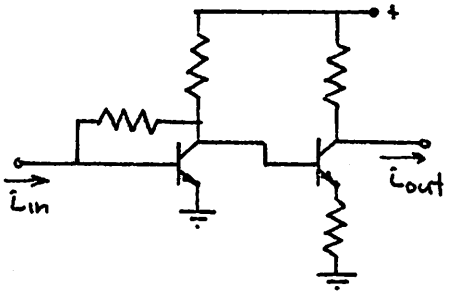


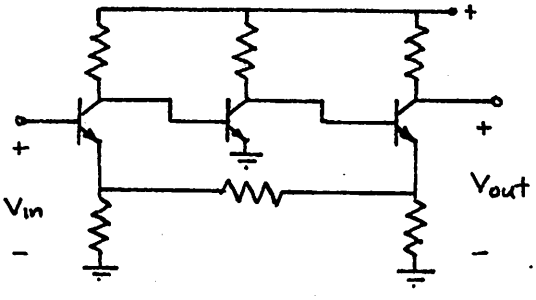
(b) SERIES-SHUNT CASCADE



(c) SHUNT-SERIES PAIR



(d) SHUNT-SERIES CASCADE



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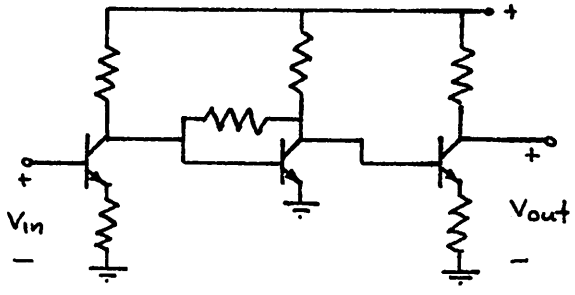
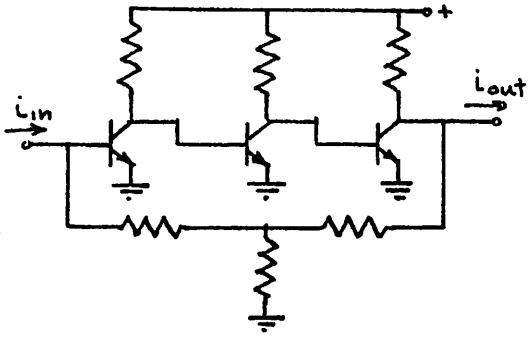
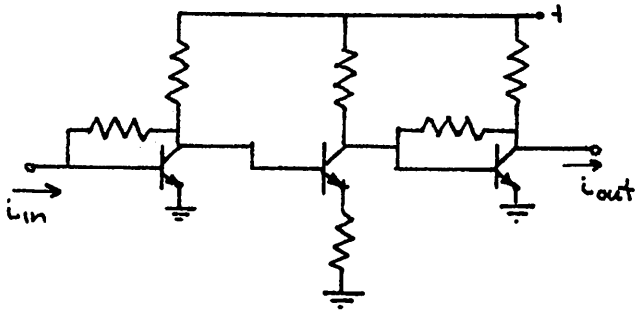


(f) SERIES-SHUNT-SERIES CASCADE



(g) SHUNT-SHUNT TRIPLE



(h) SHUNT-SERIES-SHUNT CASCADE

Fig. 1 Fundamental feedback configurations

Breuer, et al. undertook an extensive comparison of a number of broadband amplifier configurations. Their objective was the realization of an integrated memory sense amplifier using a building block approach. Blocks consisting of several common-emitter stages with local shunt and series feedback were designed and realized in integrated form.

Among other important work in the area of integrated broadband amplifiers is the integrated gain block developed by Haines[4]. This block provides a nearly one-pole response that is insensitive to temperature.

In monolithic circuits restrictions on element size and type have made dc problems particularly important. As a result this aspect of integrated amplifiers has received intensive study. Widlar[5] has presented a number of examples wherein the inherent properties of integrated circuits are used in overcoming the biasing problem. Solomon[6] has pointed out several approaches to the biasing of monolithic configurations and has demonstrated the effectiveness of a differential amplifier approach.

II. The Building Block Concept

In situations where lowpass broadband amplifier specifications cannot be satisfied with a relatively simple ciruit configuration the building block concept is often employed.[3,7,8] This concept involves the cascading of a number of ideally non-interacting blocks to produce an overall amplifier. The amplifier can then be discussed from a systems point of view in terms of the basic blocks.

Design of an individual block configuration is usually straightforward and hence the block approach offers a tractable design situation in cases where consideration of the complete amplifier might be impossibly complex. In addition, a wide range of overall specifications can be met with a single block configuration through minor modifications in the block design and variation of the number of blocks used. Because of this design ease and flexibility the block approach will be adopted in this study.

a. Examples

The actual structure of the individual building blocks may take many forms, perhaps the simplest being a single common-emitter stage with local series or shunt feedback. An amplifier consisting of an alternating cascade of such stages is shown in Fig. 2. The shunt feedback stage approximates a transimpedance, providing low input and output

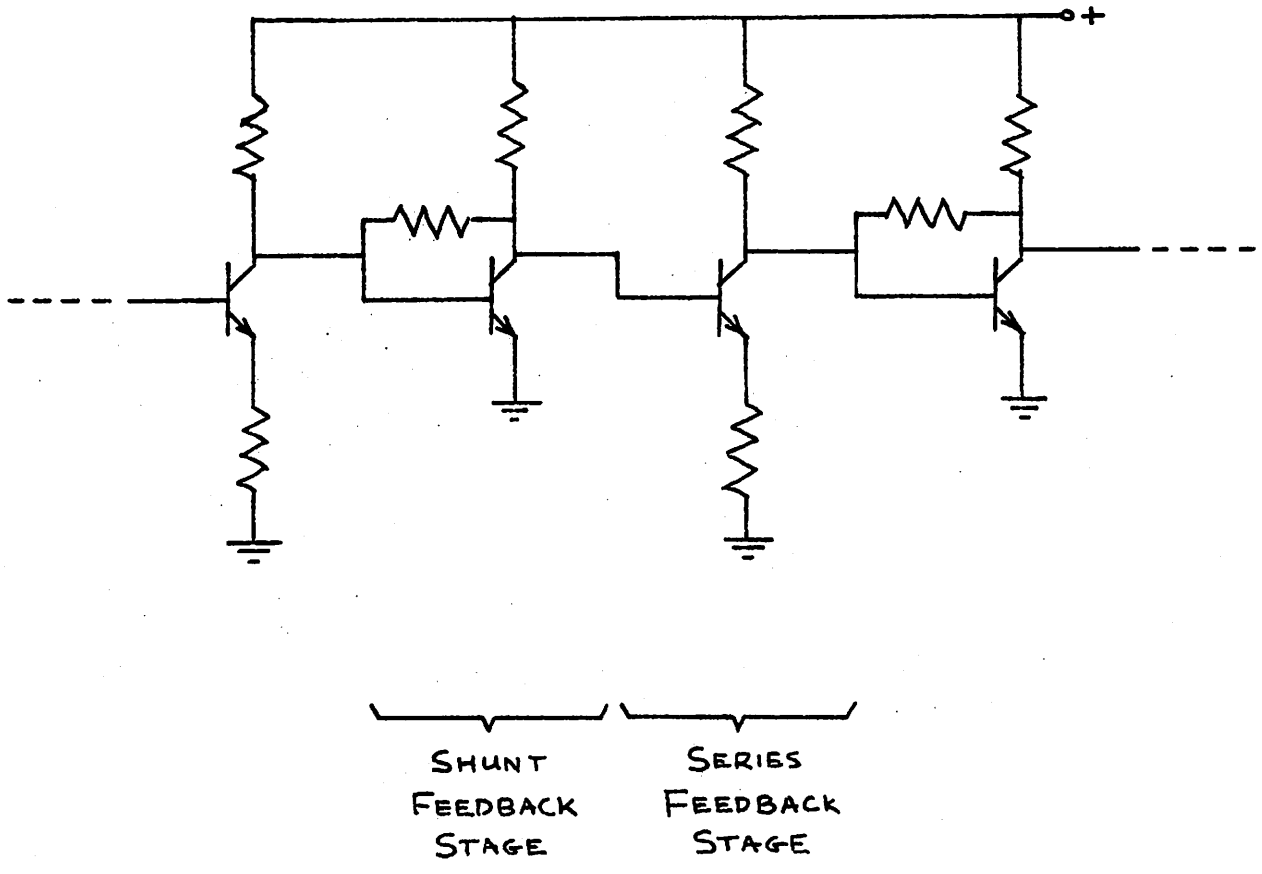


Fig. 2 An alternating cascade of local shunt and series feedback stages

impedance levels, while the series feedback stage produces an approximate transadmittance, characterized by high input and output impedances. Thus, in the alternating cascade of Fig. 2 a high output impedance is coupled into a low input impedance while a high input impedance is driven from a low output impedance. This impedance mismatch tends to minimize the interaction between stages. Of course, truly non-interacting stages are obtained only if the mismatch is very great. In a configuration such as Fig. 2 the interaction is significant and must be taken into account in any precise design procedure.

Detailed considerations of the local feedback cascade from a building block point of view have been undertaken by Cherry and Hooper[7] and by Breuer, et al.[3]; the latter dealing with integrated circuits. Design procedures are established and comparisons with other configurations are carried out. The gain-bandwidth performance of the local feedback cascade is concluded to be near optimum. However, it should be noted that in neither of the studies is temperature sensitivity taken to be of major concern.

An example of a more complicated realization for a basic block is the gain block realized by Haines.[4] In this configuration a number of stages are used along with overall feedback in an effort to realize an "ideal" gain element characterized by the transfer function

$$A(p) = \frac{K_o}{P + P_o} \qquad (1.1)$$

where p_o and K_o are insensitive to changes in temperature. The reduction in temperature sensitivity is considered to be of primary importance in the design. A complete monolithic realization of the block is produced and studied in detail. The work is rather narrow however in that the advantages and disadvantages of the circuit used, relative to other possible configurations, are not examined.

b. Restriction to monolithic realizations

In this study only completely self-contained monolithic realizations are to be considered for the individual blocks. The blocks should be capable of being directly coupled in cascade without the use of additional circuit elements. The usual approach to satisfying this requirement in integrated circuits is to establish a method of maintaining a zero volt dc level at both input and output ports. This necessitates some method of dc level shifting to compensate for the dc collector-emitter drops which build up through the amplifier.

Because some type of level shifting network must be included within the block, an integrated block should probably consist of more than a single common emitter stage for the amplifier. The gain-bandwidth product of such a

stage is generally not sufficient to warrant the incorporation of a relatively complicated level shifting mechanism with each stage.

III. Realizing the Basic Block

In realizing the basic building block, the emphasis of this report is to be on the small-signal ac performance. This is not to say that dc considerations are unimportant. On the contrary, the question of integrated realizability is primarily a dc problem; and this question is to be kept in mind at all times. However, the interest in this study centers on how a number of common approaches to the dc problem affect ac performance. The development of new dc techniques will not be considered.

a. Ac considerations

From a small-signal ac standpoint, most practical lowpass amplifiers can be related to one of the eight basic configurations of Fig. 1. These configurations result from various applications of negative feedback in a cascade of common-emitter stages. Consideration is

limited to at most three such stages. Because of stability considerations, three is usually the largest number of common-emitter stages that can be effectively employed within a feedback loop. Also, three such stages is often the most that can be conveniently cascaded without including a dc level shift in the cascade.

A suitable means must now be established for deciding which among the basic configurations is most effective in meeting a typical set of broadband specifications. The initial step is to consider just what constitutes such a set of specifications. An accurate, designable low-frequency gain may be regarded as a primary objective. It will also be required that the gain magnitude roll off monotonically with frequency. The low-frequency gain sensitivity should minimized and a large bandwidth guaranteed. Typical numerical specifications might be a voltage gain of 10, a 5 ns 10-90% rise time (bandwidth of 70 MHz), and a maximum gain deviation of ± 2 % over a 180°C temperature range.

Consideration is to be given only to cascades of identical blocks. This implies a restriction to either voltage gain or current gain as a transfer function since the use of transfer impedances or admittances requires an alternating cascade, as in Fig. 2. No specification as to whether voltage or current gain is prefered will be assumed. Rather a decision is to be made as to which of these transfer functions is more suitable for integrated

realization.

The transfer function, current or voltage gain, that is more appropriate for each of the basic configurations in Fig. 1 can be determined by assigning so-called natural input parameters. The input parameter designated as natural for a configuration is that for which a non-ideal source impedance level has the less degrading effect. For example, suppose a voltage source is used to drive a low input impedance amplifier. A practical voltage source has associated with it a low series source resistance. If the amplifier input impedance is low, a considerable portion of the source signal may be lost across the source resistance. On the other hand, a non-ideal current source exhibits a high shunt source resistance. This resistance, though finite, does not seriously degrade performance as long as the amplifier input impedance is low. Thus, the natural input parameter for a low input impedance configuration is a current. This situation corresponds to all of the configurations in Fig. 1 with shunt feedback at the input.

By a dual argument to the one above, the natural driving situation for a high input impedance is a voltage source. The configurations with series feedback at the input correspond to this situation.

The argument as to what constitutes the natural input parameter can also be stated in terms of the type of feedback involved. Where shunt feedback is employed at the input, much of the feedback signal would be lost through the source

if a voltage source, i.e. a low impedance source, were used. Hence, the natural input is a current. Similarly, for a configuration where series feedback is used at the input the natural driving situation is a voltage source.

The transfer functions to be considered for the basic feedback configurations are indicated in Fig. 1 through the labeling of input and output parameters. These transfer functions have been assigned on the basis of the natural input parameter and the restriction to either voltage or current gain.

b. Local and overall feedback

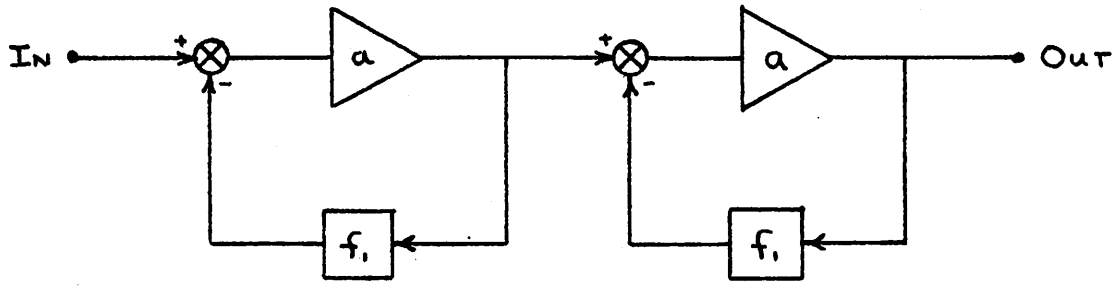
The configurations of Fig. 1 can be divided into two classes on the basis of whether local or overall feedback is used. As noted earlier, several authors have concluded that the gain-bandwidth performance of the local feedback cascades is generally as good as that obtained with the corresponding overall feedback configurations.[1,3,7] For example, Cherry and Hooper[7] compared the shunt-series cascade (Fig. 1(d)) with the shunt-series pair (Fig. 1(c)), which has been analyzed in detail by Ghausi.[9] The cascade was found to exhibit only a slightly smaller bandwidth than the pair for a given mid-band gain specification. Brodersen has also compared the shunt-series pair and cascade and has demonstrated the reason for their similar

gain-bandwidth performance.[1] In both configurations a current is fed back to the base of the input transistor. However, in the pair the feedback network samples the voltage at the emitter of the second transistor while in the local feedback cascade the base voltage of the second transistor is sampled. Since the small-signal voltage at the base is almost the same as the emitter for a transistor with local series emitter feedback, the performance of the two configurations is quite similar. The similarity in performance of the series-shunt feedback pair (Fig. 1(a)) and cascade (Fig. 1(b)) has also been pointed out by Brodersen.

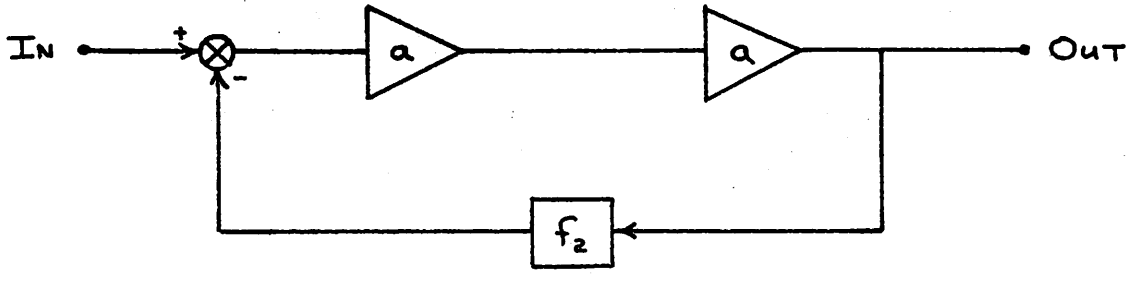
In making a comparison between the feedback pairs and local feedback cascades Broderson cites the latter as being more conveniently handled when certain dc coupling and biasing techniques are used; in particular, when voltage reference diodes are used for coupling.

The principle argument in favor of overall, as opposed to local, feedback is the improved desensitization of the amplifier response that is obtained, while comparable gain-bandwidth performance is maintained. This improvement is made apparent by the following analysis.[10]

Consider the two general feedback configurations of Fig. 3. These diagrams represent local and overall feedback systems which both utilize two identical forward gain blocks. The forward transmission of the blocks is denoted by a and the reverse transmission is assumed to be zero. For the



(a) Local feedback



(b) Overall feedback

Fig. 3 Ideal two stage feedback configurations

case where there is no interaction between blocks the overall gain of the configuration in Fig. 3(a) is given by

$$A_1 = \left[\frac{a}{1 - f_1 a}\right]^2 \qquad (1.2)$$

f_1 is the local feedback around each forward gain block. The sensitivity of A_1 with respect to the forward transmission a is

$$S_a^{A_1} = \frac{dA_1/A_1}{da/a} = 2\left[\frac{1}{1 - f_1 a}\right] \qquad (1.3)$$

In Fig. 3(b) overall feedback has been used around the two forward gain blocks. The feedback transmission is denoted by f_2 and the overall gain is given by

$$A_2 = \frac{a^2}{1 - f_2 a^2} \qquad (1.4)$$

The sensitivity of A_2 with respect to the block forward transmission is

$$S_a^{A_2} = \frac{dA_2/A_2}{da/a} = \frac{2}{1 - f_2 a^2} \qquad (1.5)$$

For an equal overall gain specification, $A_1 = A_2$, it follows from equations (1.2) and (1.4) that

$$1 - f_2 a^2 = [1 - f_1 a]^2 \qquad (1.6)$$

Upon subsitution of this result in equation (1.5), one finds

$$S_a^{A_2} = \frac{1}{1-f_1 a} S_a^{A_1} \qquad (1.7)$$

Thus, for negative feedback, i.e. $(1-f_1 a) > 1$, the sensitivity of the configuration in Fig. 3(b) is less than that for system in Fig. 3(a) by a factor of $1/(1-f_1 a)$. Essentially, the feedback has been more effectively utilized in the overall feedback configuration.

c. Composite devices

Aside from the comparison of the standard configurations, another ac consideration to be investigated is the composite device idea. The composite device is a two device configuration that is used as a direct replacement for a single device, say in one of the basic configurations of Fig. 1. The most common example of a composite device is probably the Darlington pair.

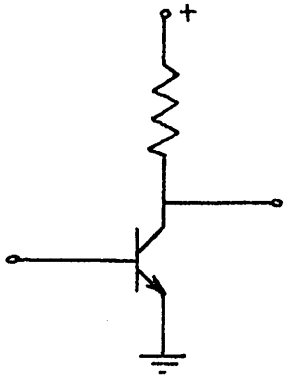
Several authors have considered the composite stage in some detail and this work is to be expanded on in this report.[1,11] There are nine possible dc connections of two transistors of like polarity (e.g. both npn). Three of these are simply cascades of the same device configuration and are not particularly useful in situations where broadband performance is desired. Brodersen has compared the

remaining six possibilities with a reference common emitter stage on the basis of gain-bandwidth product. Three of the six configurations were found to provide a gain-bandwidth product than the reference stage; these are shown in Fig. 4.

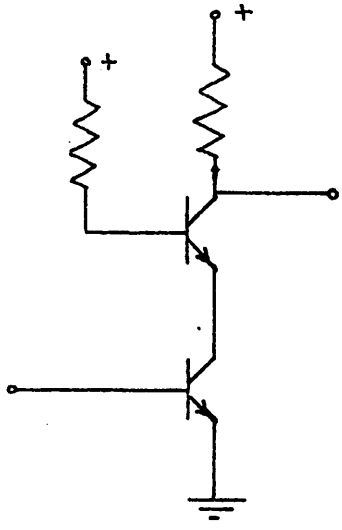
The ce-cb cascade is the familiar cascode circuit. As is obvious from Fig. 4b, this configuration easily replaces a single device. Additional elements are required to bias the base of the common-base transistor, but these elements do not significantly affect the small-signal performance of the configuration. The improved performance obtained with the cascode circuit results primarily from the reduction in the load impedance presented to the common-emitter transistor. The very low impedance presented by the input of the common-base greatly reduces the Miller effect in the common-emitter device. It will be found in Chapter 2, however, that feedback through the common-base transistor may negate the improved performance expected from the cascode.

The cc-ce configuration, a generalized Darlington pair, also shows a gain-bandwidth product increase over the common-emitter reference device. Inductive-capacitive interaction between the common-collector output and common-emitter input is the reason for this increase. The cc-ce composite device is also useful for providing a very high input impedance.

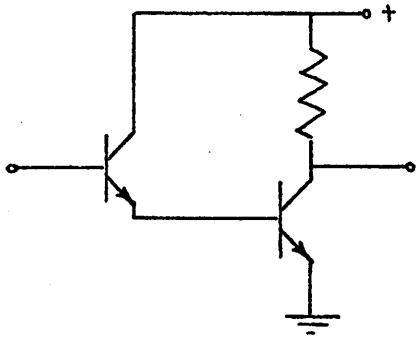
The cc-cb cascade is often refered to as the paraphase



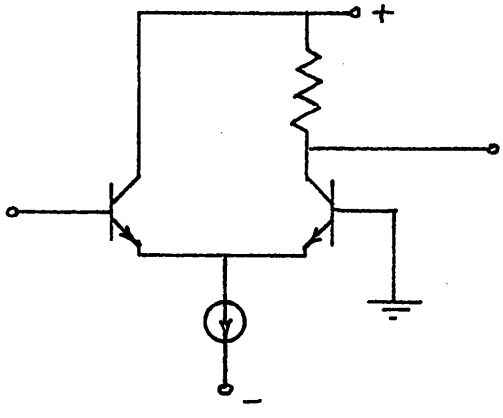
(a) ce



(b) ce-cb



(c) cc-ce



(d) cc-cb

Fig. 4 Common-emitter stage and composite devices

circuit or the emitter-coupled pair. The paraphase is a non-inverting configuration at low frequencies. That is, the output signal, taken at the collector of the common-base transistor, is in phase with the input. In contrast, a single common-emitter transistor, as well as the ce-cb and cc-ce configurations, is an inverting stage (the input and output are 180° out of phase) at low frequencies. Therefore, the paraphase circuit often cannot be subsituted directly for a common-emitter device in a feedback configuration. Hence, the circuit is not particularly suitable for use as a composite device. However, one common configuration that utilizes the emitter-coupled pair is shown in Fig. 5. Essentially, a paraphase circuit is used to replace both transistors in the series-shunt feedback pair. Note that to apply negative feedback to a paraphase circuit it is necessary to return the feedback signal to the base of the common-base transistor.

Because it is a non-inverting stage the emitter-coupled pair will not be considered further as a composite device. Instead, the configuration of Fig. 5 will be considered along with the configurations of Fig. 1 as a possibility for realizing the basic building block. The circuit of Fig. 5 is very well suited to integrated circuits from a dc standpoint.

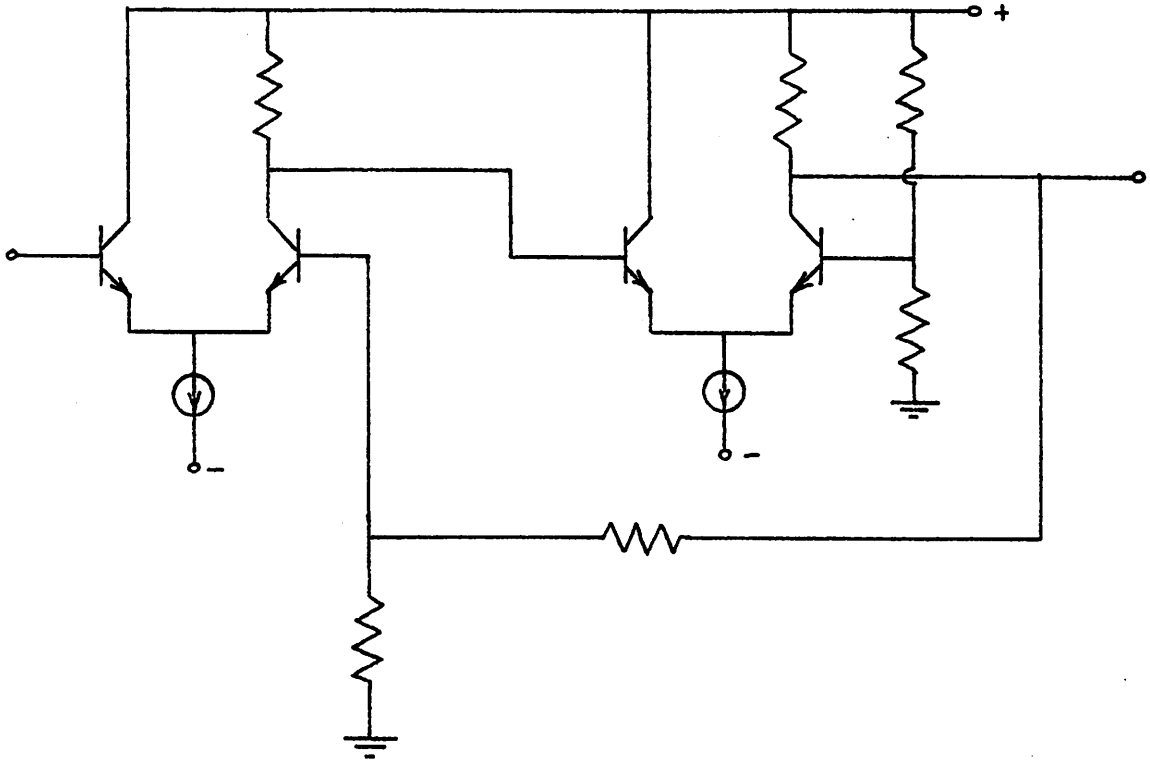


Fig. 5 Series-shunt pair with cc-cb composite devices

d. Dc considerations

The restriction to monolithic circuits generally implies a limitation to direct-coupled configurations. An exception to this has recently been introduced.[12] The configuration is ac coupled using integrated capacitors. However, the restriction on capacitor size leads to a lower bandedge on the order of 1 MHz. This value is considered here to be much too high for most lowpass applications. Hence, only direct-coupled configurations will be examined.

A monolithic structure possesses the advantage of close matching of thermal and electrical parameters between similar circuit elements. This matching is the basis of a number of techniques for achieving stable, direct-coupled configurations. As an example, consider the common-emitter bias scheme of Fig. 6. This circuit was developed by several authors independently.[5,6] It results in a relatively temperature insensitive collector voltage for the transistor Q_2. Because of the close matching of devices, the collector currents in Q_1 and Q_2 are nearly equal, both devices being driven by the same base-emitter voltage. The current in Q_1 is approximately given by

$$I_{c1} \approx \frac{V_{cc}}{R_1} \tag{1.8}$$

Then, since $I_{c2} \approx I_{c1}$, the collector voltage of Q_2 is

$$V_{c2} \approx \frac{R_2}{R_1} V_{cc} \tag{1.9}$$

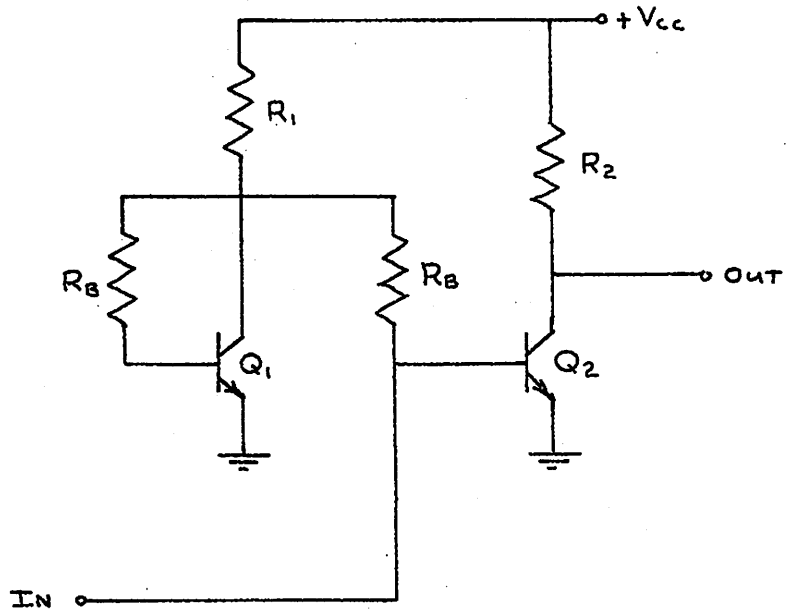


Fig. 6 Common-emitter bias scheme

If R_1 and R_2 are fabricated in the same diffusion step, the ratio R_2/R_1 is nearly temperature insensitive. Hence, V_{c2} is relatively insensitive to temperature changes.

The configuration of Fig. 6 has been considered by Solomon from a differential viewpoint.[6] That is, the configuration was developed from a general two transistor differential amplifier. In the development, the effectiveness of a differential (or balanced) approach to dealing with integrated circuits is emphasized.

Differential amplifiers are particularly well-suited to integrated circuits because of the excellent matching properties associated with monolithic structure. For this reason, and since low power dissipation is not of concern here, a differential configuration will be used for the basic gain block.

When dealing with a differential configuration two analysis approaches are available. One is to consider the configuration in terms of differential and common-mode equivalent half-circuits.[11,13] A basic configuration, such as those of Fig. 1, is taken as the differential-mode half-circuit and the overall amplifier is viewed as a double-ended connection of this half-circuit. An example of the double-ended approach is shown in Fig. 7. The series-shunt cascade is the basic configuration used. If a perfect match is obtained among the elements of this circuit, the differential small-signal response of

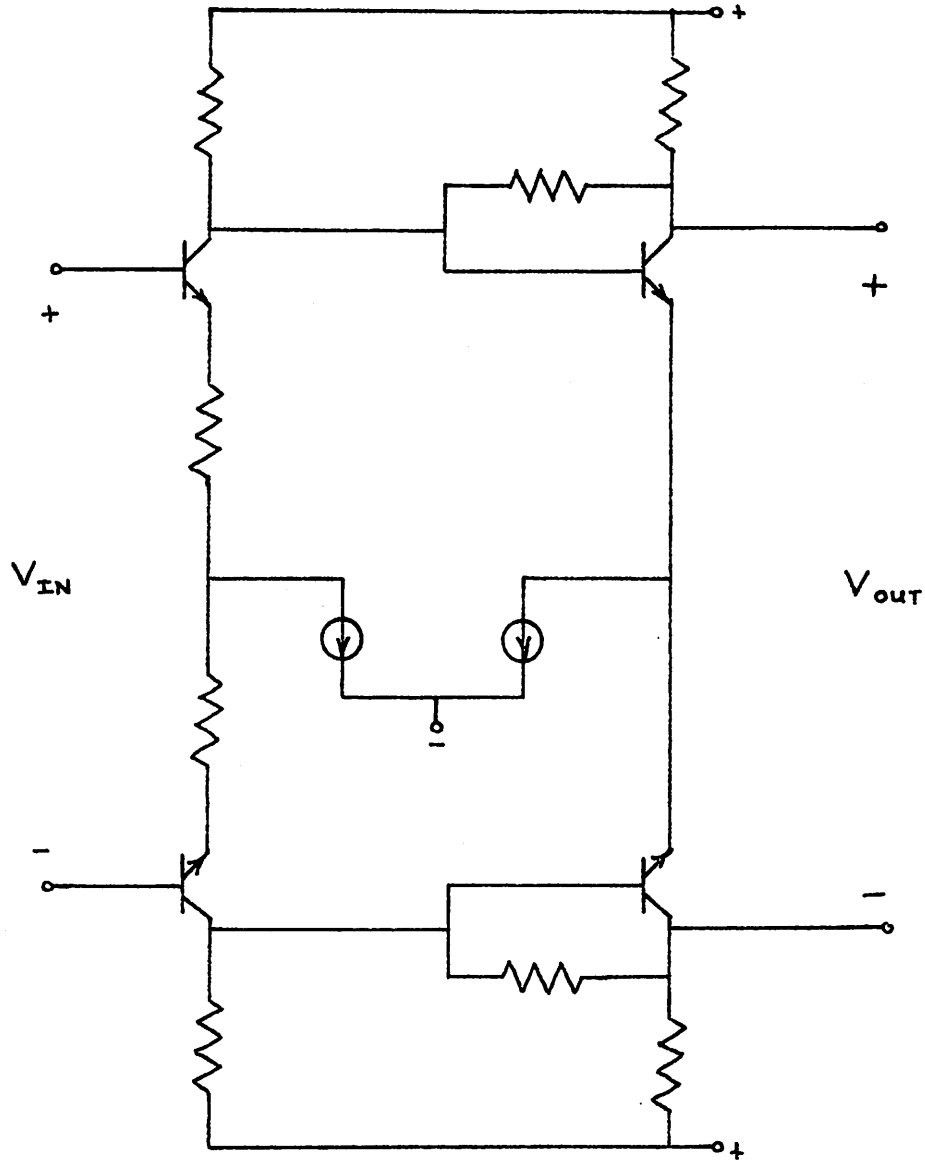


Fig. 7 Double-ended series shunt cascade

the full circuit is identical to that of the basic series-shunt cascade. Note that the biasing current sources in the configuration do not appear in the differential-mode equivalent half-circuit.

In the second approach to analyzing differential configurations the amplifier is considered in terms of a cascade of differential transistor pairs. For a configuration that is basically double-ended, such as that of Fig. 7, the pair approach offers no advantage over the half-circuit approach. However, when a differential balance is not maintained throughout the configuration, the pair approach must be used. An example is the paraphase cascade of Fig. 5. In this case the symmetry of the configuration has been destroyed; yet, from a dc standpoint, many of the advantages of a differential configuration have been retained.

It should be pointed out that two dc supplies, positive and negative, will generally be assumed available. If a zero volt dc level is to be maintained at input and output without ac coupling, two supplies are mandatory.

e. Level shifting

A differential approach to biasing has been introduced. It remains to consider methods of dc level shifting. Solomon has summarized three approaches to this problem: the use of alternate polarity transistors (i.e. npn and pnp), level shifting through resistive voltage drops, and the use of voltage reference diodes.[6]

In monolithic structures, pnp devices are generally limited to an f_t of less than 10 MHz. Hence, the alternate polarity approach does not appear suitable for wideband applications.

The use of voltage reference diodes entails two important disadvantages. First, the noise level in such devices is usually quite high. Second, the reverse breakdown voltage is not particularly well controlled. Nevertheless, the technique should be kept in mind where these disadvantages may not be critical. Brodersen has used reference diodes extensively for coupling and level shifting.

The resistive drop approach to level shifting appears at this point to be the most suitable in wideband applications. A common example of the techique is illustrated in Fig. 8. The level shift is accomplished via the drop across a resistance in an emitter-follower stage. By using a transistor current source to bias the emitter-follower, signal attenuation through the level shift is minimized.

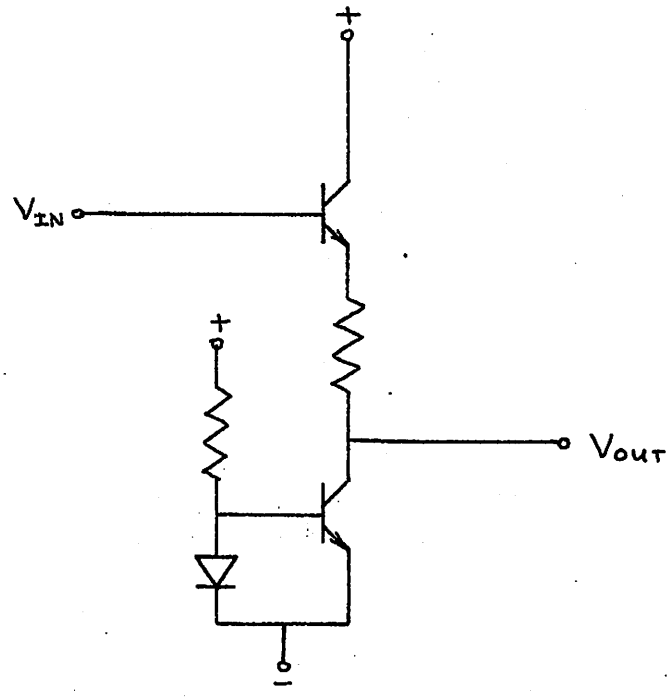


Fig. 8 Resistive level shift

CHAPTER 2: SMALL-SIGNAL PERFORMANCE

In this chapter the small-signal characteristics of the eight basic feedback configurations (Fig. 1) and the paraphase cascade (Fig. 5) are studied in detail. The Use of composite devices will also be examined on an ac basis. The principle tool of study is computer-aided simulation and analysis. The circuit analysis program by Calahan[14] is used for most of the analysis.

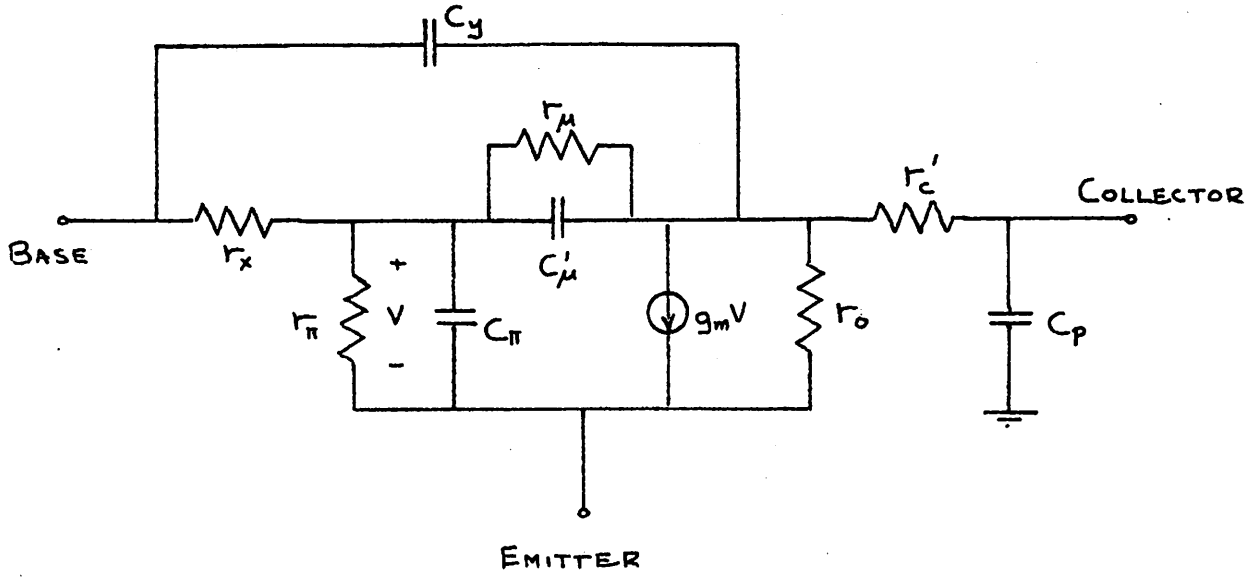
In relying on computer-aided analysis, one is of course restricted to numerical evaluation. However, except for elementary configurations, a precise frequency response analysis is usually obtainable only in numerical form, even if a computer is not used. Computer-aided analysis simply allows the investigation of a large enough number of circuits to justify a general conclusion.

I. The Small-Signal Models

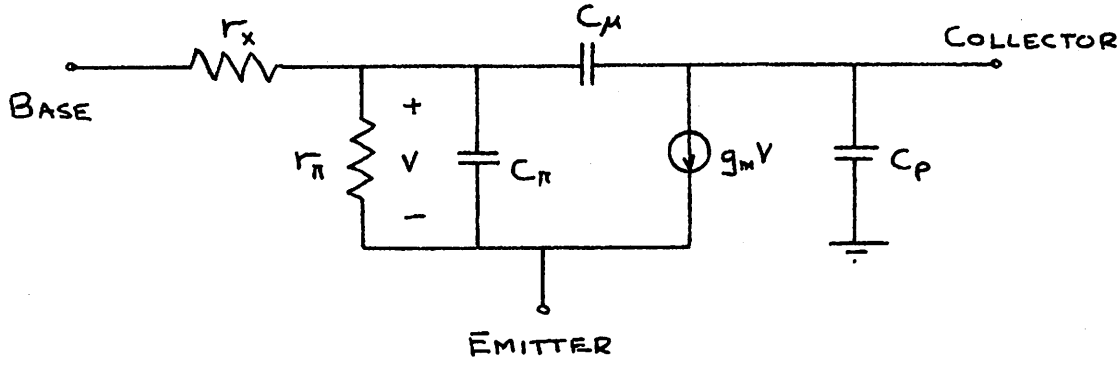
The first step in a small-signal analysis is to establish appropriate models for all circuit elements. The integrated circuit transistor is well represented by the complete hybrid-π model shown in Fig. 9(a).[15,16,17] Included in this model is the parasitic substrate capacitance between collector and ground.

While computer-aided analysis does permit the use of a more complicated model than might be chosen for hand calculations, there are definite limitations on the size of circuits that can be handled in a reasonable amount of time. Hence, it is advisable to keep the number of elements in any model to a minimum, commensurate with the overall precision desired. For the purposes of this study, the complete hybrid-π model can be reduced to the model shown in Fig. 9(b). All collector-base capacitance is lumped into the single capacitor C_μ. A buried layer technology is assumed so that r_c' is small enough to be neglected. As long as the collector load resistances encountered are not larger than a few kΩ, r_o and r_μ can usually be neglected.

All resistors are assumed to be fabricated with the base diffusion and can, in general, be modeled as a distributed RC line. However, if small geometries are maintained, the frequency effects associated with the resistors can usually be disregarded. For example,



(a) Complete hybrid-π model



(b) Reduced model

Fig. 9 Small-signal integrated circuit transistor model

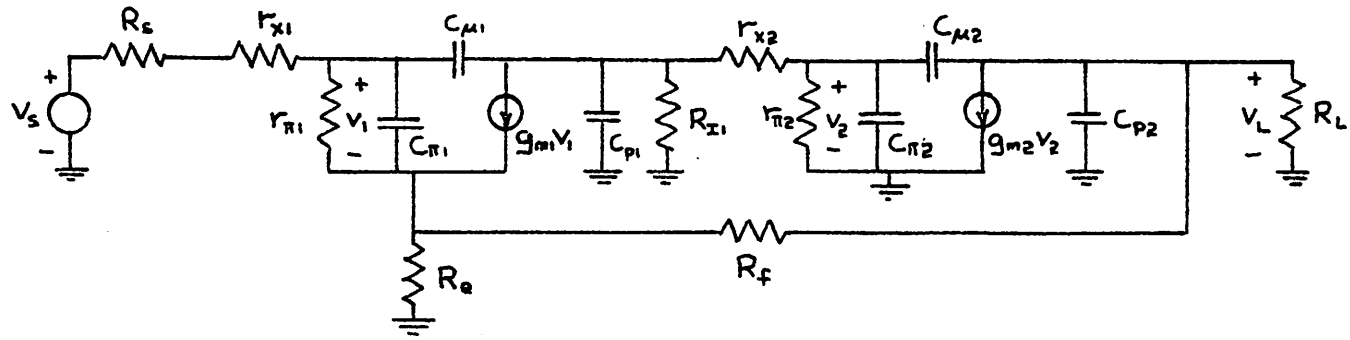
a 5 kΩ resistor with 0.5 mil line width typically has a net parasitic capacitance to ground on the order of 0.1 pF. This corresponds to a time constant of 0.5 ns. In most instances the capacitance can be neglected.

Capacitors are assumed to be MOS structures. For the applications to be encountered here, the primary parasitic element, a series resistance, can usually be neglected.

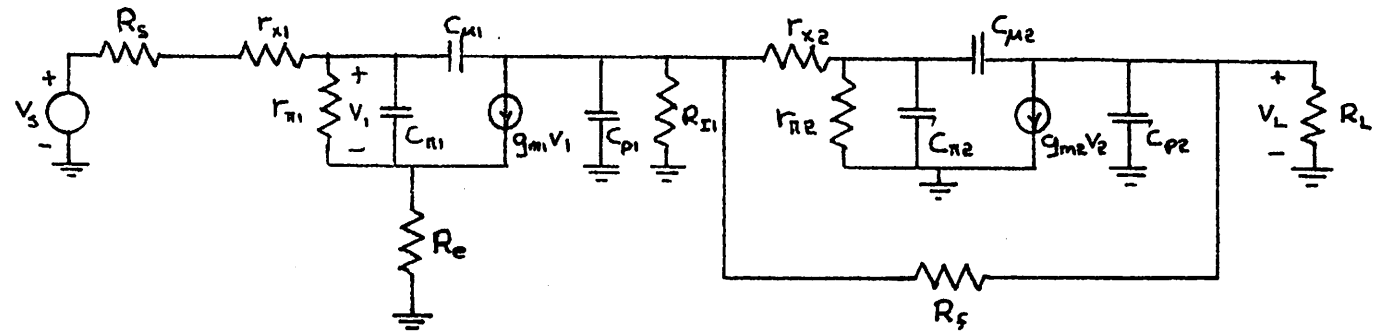
II. A Numerical Basis for Small-Signal Comparison

a. The complete small-signal circuits

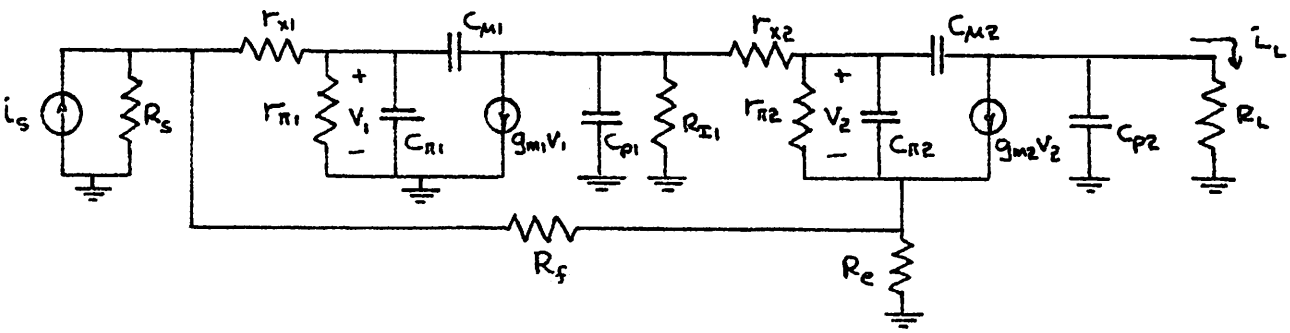
Incorporation of the transistor model of Fig. 9(b) in the basic feedback configurations of Fig. 1 leads to the small-signal circuits shown in Fig. 10. The particular numerical designs to be analyzed will be based on the specification of the low frequency gain. Therefore, the gain expressions for each of the circuits in Fig. 10 have been listed in Table I. A straightforward nodal analysis has been used to determine the gain expressions for the local feedback cascades. For the overall feedback



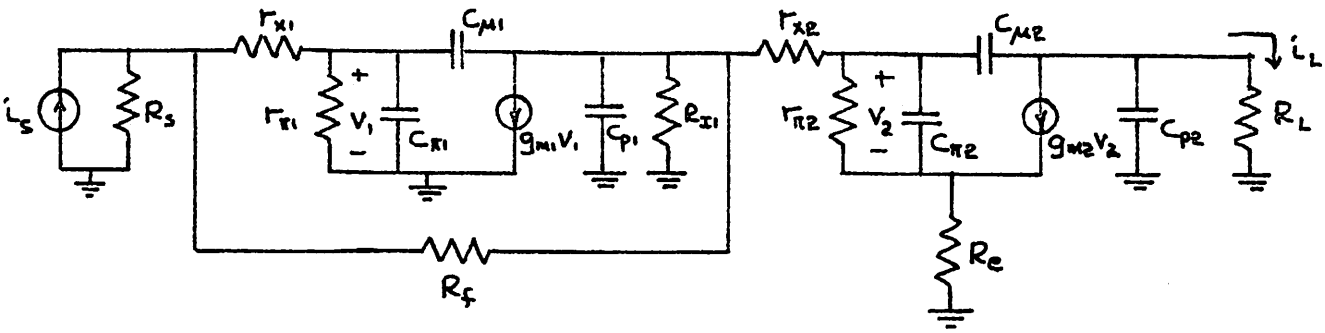
(a) SERIES-SHUNT PAIR



(b) SERIES-SHUNT CASCADE

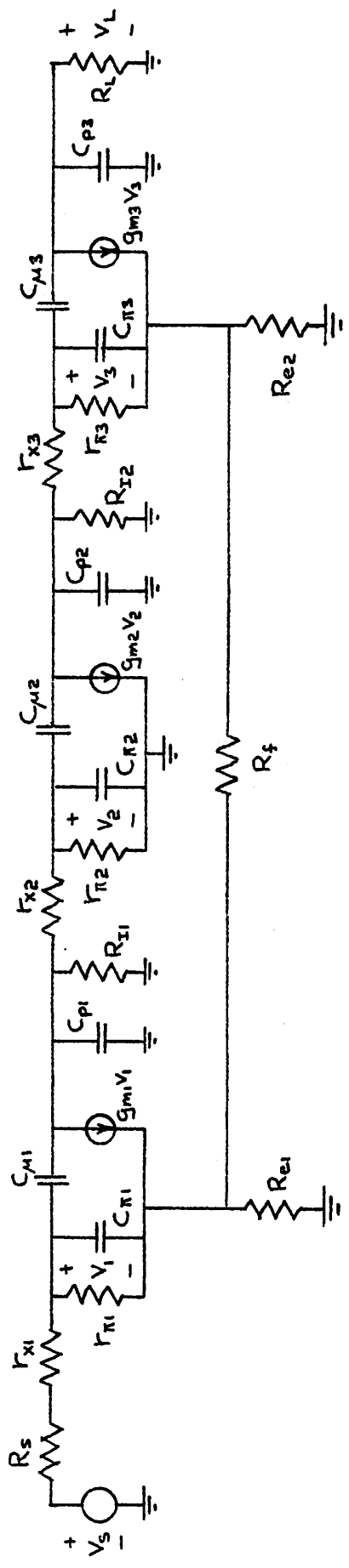


(c) SHUNT-SERIES PAIR

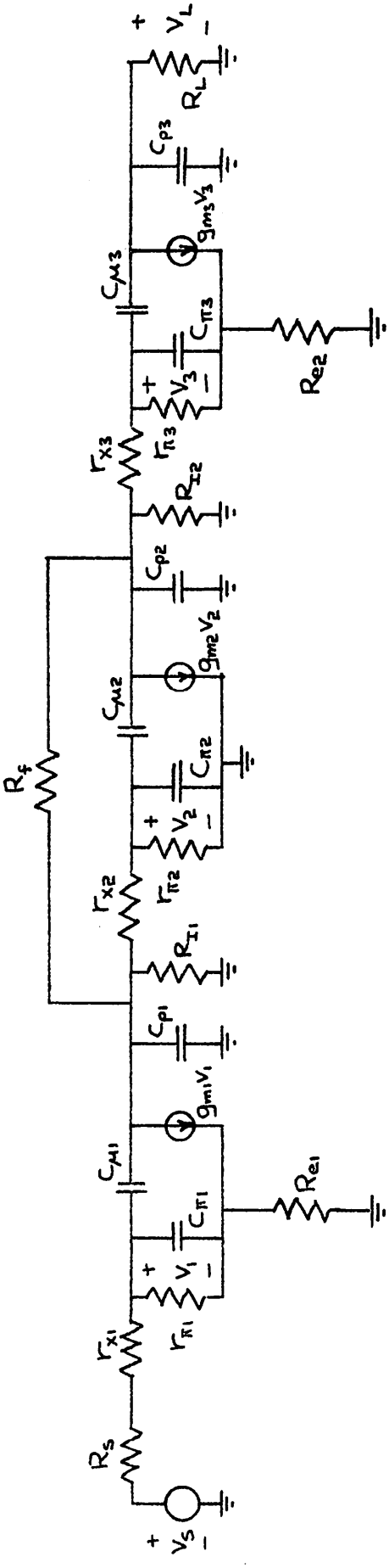


(d) SHUNT-SERIES CASCADE

Fig. 10 Small-signal equivalent circuits for the basic feedback configurations of Fig. 1

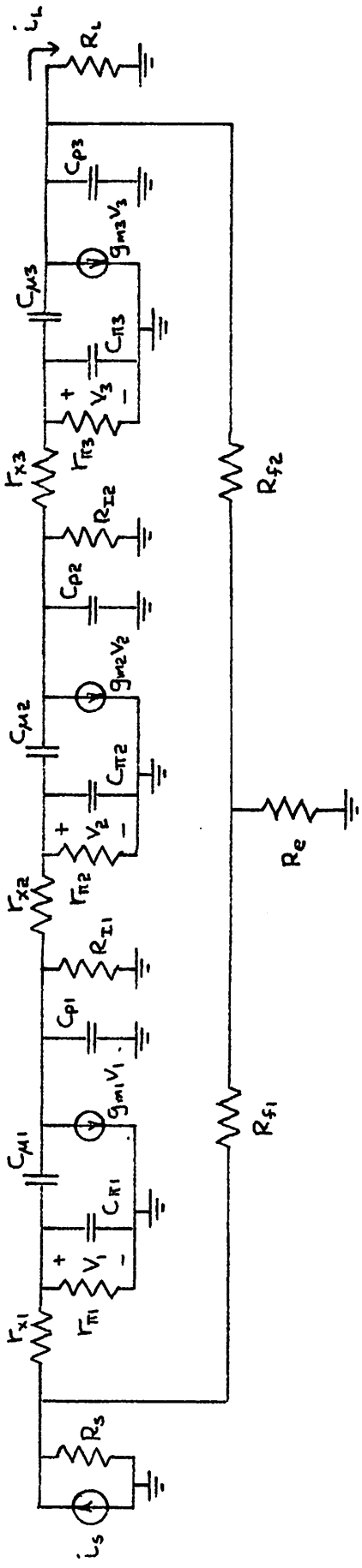


(e) Series-Series Triple

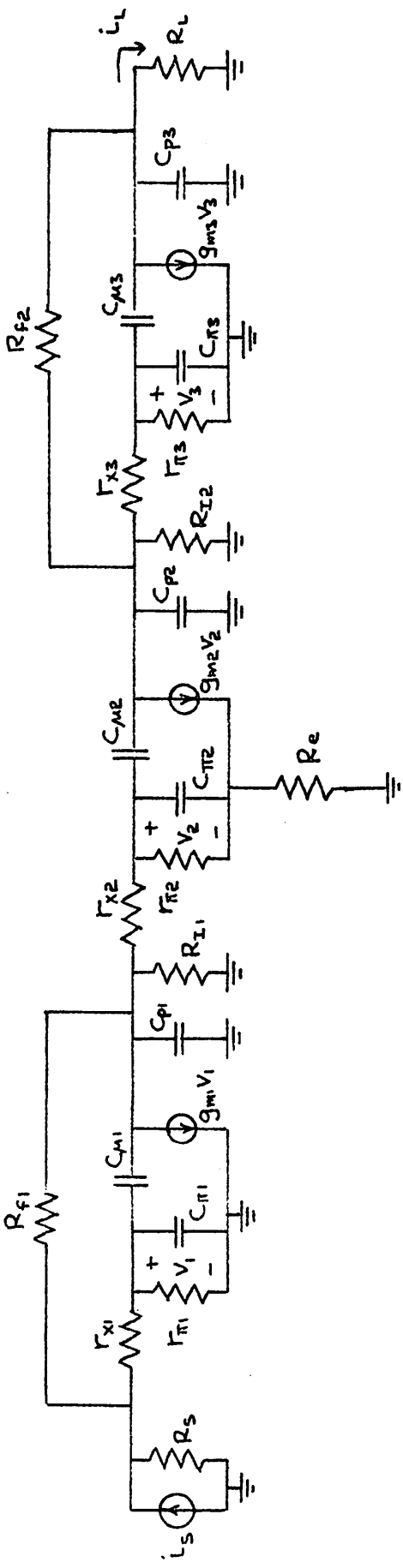


(f) Series-Shunt-Series Cascade

Fig. 10 Cont'd.



(g) Shunt-Shunt Triple



(h) Shunt-Series-Shunt Cascade

Fig. 10 Cont'd

Series-Shunt Pair

$$A_v(0) = \frac{a_v(0)}{1 - a_v(0)\, f_v(0)}$$

$$f_v(0) = -\frac{R_e}{R_e + R_f}$$

$$a_v(0) = \left(\frac{R_I R_L}{R_I + r_{x2} + r_{\pi 2}}\right)\left(\frac{\beta_{01}\beta_{02}}{\beta_{01}+1}\right)\left(\frac{R_e + R_f}{K_1 + R_e + R_f}\right)\left(\frac{R_e + R_f}{K_2(R_e+R_f) + R_e R_f}\right)$$

where

$$K_1 = R_L$$

$$K_2 = \frac{R_s + r_{x1} + r_{\pi 1}}{\beta_{01}+1}$$

Series-Shunt Cascade

$$A_v(0) = \left(\frac{R_I R_L}{R_I + r_{x2} + r_{\pi 2}}\right)\left(\frac{\beta_{01}\beta_{02}}{\beta_{01}+1}\right)\left(\frac{1}{R_e + K_1}\right)\left(\frac{R_f - K_2}{R_e + K_3}\right)$$

where

$$K_1 = \frac{R_s + r_{x1} + r_{\pi 1}}{\beta_{01}+1}$$

$$K_2 = \frac{r_{x2} + r_{\pi 2}}{\beta_{02}}$$

$$K_3 = \frac{(R_I + R_L)(r_{x2}+r_{\pi 2}) + (\beta_{02}+1) R_I R_L}{R_I + r_{x2} + r_{\pi 2}}$$

Table I Low-frequency gain expressions for the circuits of Fig. 10

Shunt-Series Pair

$$A_I(0) = \frac{a_I(0)}{1 - a_I(0)\, f_I(0)}$$

$$f_I(0) = -\frac{1}{\alpha_{02}} \frac{R_e}{R_e + R_f}$$

$$a_I(0) = \left(\frac{R_s R_I}{R_s + r_{x1} + r_{\pi 1}}\right)\left(\frac{\beta_{01}\beta_{02}}{\beta_{02}+1}\right)\left(\frac{R_e + R_f}{K_1 + R_e + R_f}\right)\left(\frac{R_e + R_f}{K_2(R_e+R_f) + R_e R_f}\right)$$

where

$$K_1 = \frac{R_s (r_{x1} + r_{\pi 1})}{R_s + r_{x1} + r_{\pi 1}}$$

$$K_2 = \frac{R_I + r_{x2} + r_{\pi 2}}{\beta_{02}+1}$$

Shunt-Series Cascade

$$A_I(0) = \left(\frac{\beta_{01}\beta_{02} R_s R_I}{(\beta_{02}+1)(R_s + r_{x1} + r_{\pi 1})}\right)\left[\frac{R_f - K_1}{K_2\left(R_e + \frac{r_{x2}+r_{\pi 2}}{\beta_{02}+1}\right) + K_3 + R_f\left(R_e + \frac{R_I + r_{x2} + r_{\pi 2}}{\beta_{02}}\right)}\right]$$

where

$$K_1 = \frac{r_{x1} + r_{\pi 1}}{\beta_{01}+1}$$

$$K_2 = \frac{(r_{x1} + r_{\pi 1})(R_I + R_s) + (\beta_{01}+1) R_I R_s}{R_s + r_{x1} + r_{\pi 1}}$$

$$K_3 = \frac{R_s R_I (r_{x1} + r_{\pi 1})}{(\beta_{02}+1)(R_s + r_{x1} + r_{\pi 1})}$$

Table I Cont'd

SERIES-SERIES TRIPLE

$$A(o) = \frac{a(o)}{1 - a(o)\,f(o)}$$

$$f(o) = \frac{1}{\alpha_{o3}} \left| \frac{R_{e1} R_{e2}}{R_{e1} + R_{e2} + R_f} \right| \frac{1}{R_L}$$

$$a(o) = - \frac{\beta_{o1} \beta_{o2} \beta_{o3}}{(\beta_{o1}+1)(\beta_{o3}+1)} \left(\frac{R_{I1} R_{I2} R_L}{R_{I1} + r_{x2} + r_{\pi 2}} \right) \left(\frac{1}{R'_{e1} + \frac{R_s + r_{x1} + r_{\pi 1}}{\beta_{o1} + 1}} \right) \left(\frac{1}{R'_{e2} + \frac{R_{I2} + r_{x3} + r_{\pi 3}}{\beta_{o3} + 1}} \right)$$

where

$$R'_{e1} = \frac{R_{e1} (R_f + R_{e2})}{R_{e1} + R_{e2} + R_f}$$

$$R'_{e2} = \frac{R_{e2} (R_f + R_{e1})}{R_{e1} + R_{e2} + R_f}$$

SERIES-SHUNT-SERIES CASCADE

$$A_v(o) = - \left(\frac{\beta_{o1} \beta_{o2} \beta_{o3}}{\beta_{o1} + 1} \right) \left(\frac{R_L}{r_{x2} + r_{\pi 2}} \right) \left(\frac{1}{R_{e1} + \frac{R_s + r_{x1} + r_{\pi 1}}{\beta_{o1} + 1}} \right)$$

$$\cdot \left\{ \frac{R_f - \frac{r_{x2} + r_{\pi 2}}{\beta_{o2}}}{1 + \left(\frac{R_{I1} + r_{x2} + r_{\pi 2}}{R_{I1} R_{I2}} \right) \left(\frac{R_{o2} + R_{I2}}{r_{x2} + r_{\pi 2}} \right) R_f + R_{o2} \left[\frac{(r_{x2} + r_{\pi 2})(R_{I1} + R_{I2}) + (\beta_{o2} + 1) R_{I1} R_{I2}}{(r_{x1} + r_{\pi 1}) R_{I1} R_{I2}} \right]} \right\}$$

where $R_{o2} = r_{x3} + r_{\pi 3} + (\beta_{o3} + 1) R_{e3}$

Table I Cont'd

Shunt-Shunt Triple

$$A_I(0) = \frac{a_I(0)}{1 - a_I(0) f_I(0)}$$

$$f_I(0) = \frac{R_e R_L}{R_{f1} R_{f2} + R_e (R_{f1} + R_{f2})}$$

$$a_I(0) = -\beta_{01}\beta_{02}\beta_{03}\left(\frac{R_S}{R_S + r_{x1} + r_{\pi 1}}\right)\left(\frac{R_{I1}}{R_{I1} + r_{x2} + r_{\pi 2}}\right)\left(\frac{R_{I2}}{R_{I2} + r_{x3} + r_{\pi 3}}\right) \cdot \left[\frac{R'_{f1}}{R'_{f1} + \frac{R_S (r_{x1} + r_{\pi 1})}{R_S + r_{\pi 1} + r_{\pi 1}}}\right]\left(\frac{R'_{f2}}{R'_{f2} + R_L}\right)$$

where

$$R'_{f1} = R_{f1} + \frac{R_e R_{f2}}{R_e + R_{f2}}$$

$$R'_{f2} = R_{f2} + \frac{R_e R_{f1}}{R_e + R_{f1}}$$

Shunt-Series-Shunt Cascade

$$A_I(0) = -\left(\frac{\beta_{01}\beta_{02}\beta_{03}}{\beta_{03} + 1}\right)\left(\frac{R_{I2}}{r_{x1} + r_{\pi 1}}\right) \cdot \left\{\frac{R_{f2} - \frac{r_{x3} + r_{\pi 3}}{\beta_{03}}}{\frac{(R_{I1} + r_{x3} + r_{\pi 3})}{(\beta_{03} + 1)} R_{f2} + \frac{(r_{x3} + r_{\pi 3})(R_{I2} + R_L)}{(\beta_{03} + 1)} + R_{I2} R_L}\right\} \cdot \left\{\frac{R_{f1} - \frac{r_{x1} + r_{\pi 1}}{\beta_{01}}}{1 + \frac{(R_S + r_{x1} + r_{\pi 1})(R_{I1} + R_{01})}{(r_{x1} + r_{\pi 1}) R_S R_{I1}} R_{f1} + R_{01}\left[\frac{(r_{x1} + r_{\pi 1})(R_S + R_{I1}) + (\beta_{01} + 1) R_S R_{I1}}{(r_{x1} + r_{\pi 1}) R_S R_{I1}}\right]}\right\}$$

where $R_{01} = r_{x2} + r_{\pi 2} + (\beta_{02} + 1) R_e$

configurations, an approximation to the ideal feedback equation

$$A = \frac{a}{1 - af} \qquad (2.1)$$

is established. This technique has been demonstrated by Ghausi and Pederson[18] and an example is given in Appendix A.

b. Appropriate bias, source and load resistances

To begin establishing numerical values for the elements of the small-signal circuits in Fig. 10, suitable source, load and bias resistances must be determined. This can be done by considering the practical limitations which are imposed on attaining the ideal operating conditions for either a voltage or current amplifier. A voltage gain configuration operates ideally from a zero impedance source into an open-circuit load, while a current amplifier is ideally driven by an infinite impedance source into a short-circuit load.

A typical low source or load impedance is 50 Ω. This choice may seem rather arbitrary but it does represent what is often encountered in a practical situation, such as terminated coaxial cables. In choosing a practical high resistance level, an important circuit limitation should be considered. The typical load to ac ground from

the collector of a transistor in a common-emitter configuration is generally limited to a few kΩ by the collector bias resistor. Thus, 2 kΩ will be used for high source and load impedances and for the interstage bias resistors, R_I. An argument for the 2 kΩ limitation can also be presented in terms of frequency response. A parasitic capacitance to ground of the order of 2 pF is generally associated with the collector of an integrated circuit transistor. A 2 kΩ collector load resistance leads to a time constant of 4 ns in conjunction with this capacitor. A significantly larger load resistance results in a proportionally larger time constant and might well represent a limitation on broadband performance.

c. Transistor characteristics

The transistors to be used correspond to devices that are quite readily realized in integrated circuits.[17,19] The device parameters assumed are as follows:

$\beta_o = 50$

$f_t = 600$ MHz

$r_x = 150\,\Omega$

$C_\mu = 2$ pF

$C_p = 2$ pF

These values have been assumed early in this study and may appear rather pessimistic, particularly the large value for C_μ, in view of the devices that can presently be realized.

For convenience, it will be assumed that all active devices in the circuits of Fig. 10 are biased at a collector current of 4 mA. This level is usually within the range of optimum transistor gain-frequency performance. For the choice of I_c = 4 mA, the following values are obtained for the remaining elements of the hybrid-π model (Fig. 9(b)):

$$g_m = 0.154 \text{ mho}$$

$$r_\pi = 325$$

$$C_\pi = 39 \text{ pF}$$

d. Values for the feedback elements

The remaining step in numerically establishing the circuits to be analyzed is the determination of values for the feedback elements. This determination is based on the specification of the low-frequency (midband) gain. For the initial analysis only resistive feedback will be employed. The use of capacitive compensation in the feedback network will be taken up in Chapter 3.

A decision must be made as to the relative gain requirements for the basic configurations. It seems reasonable to specify a given amount of midband gain per common-emitter device of a configuration. For example, suppose a low-frequency gain of 1000 is specified for the overall amplifier. This gain might be achieved with two blocks each utilizing a three transistor configuration, or with three blocks each consisting of a two device configuration. The appropriate gain requirements are then 31.6 for the three device configurations and 10 for the two device configuration. That is, a gain of 3.6 per common-emitter device is required. Since these specifications are typical of situations demanding a precise midband gain and a large bandwidth, they will be used in comparing the circuits of Fig. 10.

The design of the two stage local feedback cascades and the feedback pairs is now considered on the basis of the gain of 10 specification. Since two feedback elements, R_e and R_f, are involved, there is not a unique design for a given gain specification. Some additional criterion is needed to specify R_e and R_f uniquely. For the feedback pairs a simple requirement is to maximize the low-frequency forward transmission a(0), subject to a specified A(0), with respect to the loading effects

of R_e and R_f.* This is nearly equivalent to maximizing the low-frequency loop-gain

$$T(o) = - f(o)\, a(o) \qquad (2.2)$$

and hence minimizing the sensitivity factor

$$D_s = \frac{dA/A}{da/a} = \frac{1}{1 + T(o)} \qquad (2.3)$$

Unique "optimum" values of R_e and R_f can thus be established for the feedback pairs. The optimization procedure is carried out in Appendix B. Following the design of the feedback pairs, the local feedback cascades are designed of the basis of using the same value for R_e as used in the corresponding feedback pair.

The design values for R_e and R_f are given in Table II. Designs have been carried out for a spread of values about the optimum by assuming values for R_e of 0.75, 2 5, and 10 times the optimum value. For the feedback pairs the loop-gain has been calculated for each design and is included in the table.

---

* a(0) and A(0) are the low-frequency values of the open loop forward transmission and the overall gain, as defined in the ideal feedback equation (Eq. (2.1)).

DESIGN CASE	SERIES-SHUNT PAIR	SERIES-SHUNT CASCADE
1 (OPTIMUM)*	$R_e = 47\Omega$, $R_f = 437\Omega$	$R_e = 47\Omega$, $R_f = 617\Omega$
2	$R_e = 35\Omega$, $R_f = 326\Omega$	$R_e = 35\Omega$, $R_f = 489\Omega$
3	$R_e = 94\Omega$, $R_f = 884\Omega$	$R_e = 94\Omega$, $R_f = 1.12\,k\Omega$
4	$R_e = 235\Omega$, $R_f = 2.24\,k\Omega$	$R_e = 235\Omega$, $R_f = 2.67\,k\Omega$
5	$R_e = 470\Omega$, $R_f = 4.58\,k\Omega$	$R_e = 470\Omega$, $R_f = 5.38\,k\Omega$

DESIGN CASE	SHUNT-SERIES PAIR	SHUNT-SERIES CASCADE
1 (OPTIMUM)*	$R_e = 45\Omega$, $R_f = 425\Omega$	$R_e = 45\Omega$, $R_f = 590\Omega$
2	$R_e = 34\Omega$, $R_f = 320\Omega$	$R_e = 34\Omega$, $R_f = 471\Omega$
3	$R_e = 90\Omega$, $R_f = 846\Omega$	$R_e = 90\Omega$, $R_f = 1.08\,k\Omega$
4	$R_e = 225\Omega$, $R_f = 2.16\,k\Omega$	$R_e = 225\Omega$, $R_f = 2.56\,k\Omega$
5	$R_e = 450\Omega$, $R_f = 4.46\,k\Omega$	$R_e = 450\Omega$, $R_f = 5.17\,k\Omega$

DESIGN CASE	SERIES-SERIES TRIPLE	SERIES-SHUNT-SERIES CASCADE
1 (OPTIMUM)*	$R_{e1} = R_{e2} = 124\Omega$, $R_f = 0$	$R_{e1} = R_{e2} = 124\Omega$, $R_f = 315\Omega$
2	$R_{e1} = R_{e2} = 200\Omega$, $R_f = 245\Omega$	$R_{e1} = R_{e2} = 200\Omega$, $R_f = 764\Omega$
3	$R_{e1} = R_{e2} = 500\Omega$, $R_f = 3.25\,k\Omega$	$R_{e1} = R_{e2} = 500\Omega$, $R_f = 4.68\,k\Omega$

DESIGN CASE	SHUNT-SHUNT TRIPLE	SHUNT-SERIES-SHUNT CASCADE
1 (OPTIMUM)*	$R_e = \infty$, $R_{f1} = R_{f2} = 790\Omega$	$R_e = 500\Omega$, $R_{f1} = R_{f2} = 1.26\,k\Omega$
2	$R_e = 200\Omega$, $R_{f1} = R_{f2} = 397\Omega$	$R_e = 200\Omega$, $R_{f1} = R_{f2} = 755\Omega$
3		$R_e = 50\Omega$, $R_{f1} = R_{f2} = 387\Omega$

* DESIGN CASE WITH MAXIMUM LOOP GAIN FOR THE OVERALL FEEDBACK CONFIGURATION

Table II Design values for the feedback elements of the configurations in Fig. 10

For the three device configurations a third feedback element is involved and hence there is a third degree of freedom available in the design of the feedback network. As with the feedback pairs, the design of the triples is based on the maximization of the forward transmission a(0). In addition, the arbitrary constraints that $R_{e1} = R_{e2}$ and $R_{f1} = R_{f2}$ will be imposed. From the expressions for a(0) and f(0) in Table I the conditions for maximizing a(0), subject to a specified A(0), are obvious. For the series-series triple a(0) is maximum when $R_f = 0$. For the shunt-shunt triple the maximum a(0) is obtained when $R_e = \infty$. Design values corresponding to these conditions are given in Table II. In addition, designs have been carried out for the series-series configuration with $R_f > 0$, and for the shunt-shunt configuration with finite values of R_e.

Designs for the series-shunt-series cascade are based on using the values 124 Ω, 200 Ω, and 500 Ω for $R_{e1} = R_{e2}$. For the shunt-series-shunt cascade the values 500 Ω, 200 Ω, and 50 Ω were specified for R_e.

e. Temperature dependence

The designs for the configurations of Fig. 10 have been caried out on the basis of a temperature of 300°K. In order to determine the temperature sensitivity of the configurations, they are analyzed a number of times with the element values modified to correspond to various changes in temperature. The temperature range considered is from 225°K to 375°K.

The assumed effects of temperature changes on the elements in the transistor small-signal model are summarized in Table III. The temperature dependence of r_x is particularly difficult to establish. The value of +2000 ppm/°K at 300°K is chosen to correspond to a case where r_x is dominated by the ohmic resistance between the base contact and the edge of the emitter region. That is, the temperature dependence of r_x is taken to virtually the same as that of the diffused resistors. The decision to neglect the contribution to the sensitivity due to the active base region beneath the emitter is consistent with a condition of strong dc and ac crowding. Such a condition is appropriate to the relatively high collector current levels being considered, where the gain-frequency performance of the transistor is optimum, and to the high frequencies that are being considered.

At this point the direct effect of temperature on

Parameter	Assumed Temperature Dependence
β_o	Linear, +6000 ppm/°K @ 300°K
g_m	$\propto 1/T$
r_v	Linear, +2000 ppm/°K @ 300°K
ω_t	Insensitive
C_μ	Insensitive
C_p	Insensitive
r_π	$= \beta_o / g_m$
C_π	$= (g_m/\omega_t) - C_\mu$

Table III Assumed temperature dependence of the elements in the small-signal transistor model

ac performance is the subject of interest and hence the configurations are assumed to be temperature insensitive from a dc standpoint; that is, I_c is taken as constant with temperature. Note that in the final design of Chapter 4, I_c is not invariant with temperature and the effects of its variation must be incorporated in the small-signal element temperature dependence.

All resistors in the circuits to be analyzed, including the source and load resistances, are assumed to behave as if fabricated during the base (acceptor) diffusion. A linear temperature dependence of +2000 ppm/°K at 300°K is assumed. The assumption of linearity is not a precise one. However, the deviation from a linear relationship is not major and does not alter the conclusions reached in the analysis.

MOS capacitors will be taken as nearly temperature insensitive.

III. Analysis Results for the Basic Configurations

With suitable element values established, the circuits of Fig. 10 were analyzed using Calahan's ac analysis program. For the overall feedback configurations the open loop response was also determined. The results are summarized in Table IV. Gain variations with temperature were found to be monotonic and hence only the deviations over the full temperature range ($300°K \pm 75°K$) are given.

a. Gain designability

From Table IV it is seen that the designability of the low-frequency gain is satisfactory for all configurations, the analysis values being within ±1 % of the specified gain. In particular, this result confirms the validity of treating the overall feedback configurations through the ideal feedback equation, at least as far as the low-frequency performance is concerned.

Feedback Elements	$T_V(0)$	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)	$A_V(0)$	Deviation in $A_V(0)$ 225°K 375°K	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)
$R_e = 47\Omega$ $R_f = 437\Omega$	29.3	-.20 -3.7 -26 -41 -326	-96 +49 +770	9.95	-2.8% +1.1%	-1.6 ± j4.3 -28 -39 -326	-75 +33 ± j45
$R_e = 35\Omega$ $R_f = 326\Omega$	29.0	-.24 -3.2 -28 -41 -409	-107 +58 +770	9.96	-2.9% +.85%	-1.5 ± j4.4 -30 -40 -410	-78 +27 ± j48
$R_e = 94\Omega$ $R_f = 884\Omega$	27.3	-.14 -5.1 -24 -40 -203	-74 +31 +770	10.02	-2.9% +1.1%	-2.3 ± j3.6 -26 -39 -203	-67 +53 ± j24
$R_e = 235\Omega$ $R_f = 2.24k\Omega$	19.7	-.09 -7.3 -23 -40 -128	-58 +16 +770	10.00	-3.7% +1.4%	-3.4 ± j.96 -24 -40 -128	-56 +18 +188
$R_e = 470\Omega$ $R_f = 4.58k\Omega$	13.0	-.07 -8.8 -23 -40 -102	-50 +9.2 +770	9.93	-5.5% +2.2%	-1.1 -7.2 -24 -40 -102	-50 +9.7 +316

(a) Series-Shunt Pair

Table IV Small-signal analysis results for the configurations of Fig. 10

FEEDBACK ELEMENTS	$A_V(0)$	DEVIATION IN $A_V(0)$ 225°K	375°K	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
$R_e = 47\Omega$ $R_f = 617\Omega$	10.03	-7.8%	+2.7%	$-3.3 \pm j3.5$ -20 -47 -306	-92 $+46$ $+127$
$R_e = 35\Omega$ $R_f = 489\Omega$	10.03	-8.5%	+2.8%	$-3.4 \pm j3.6$ -19.5 -50 -382	-103 $+55$ $+104$
$R_e = 94\Omega$ $R_f = 1.12k\Omega$	10.01	-6.0%	+1.9%	$-3.4 \pm j2.7$ -21 -44 -193	-72 $+29$ $+204$
$R_e = 235\Omega$ $R_f = 2.67k\Omega$	10.01	-6.3%	+2.4%	-1.95 -6.1 -22 -41 -124	-56 $+15$ $+357$
$R_e = 470\Omega$ $R_f = 5.38k\Omega$	10.00	-7.7%	+3.1%	$-.89$ -8.3 -22 -41 -100	-49 $+8.5$ $+489$

(b) SERIES-SHUNT CASCADE

Table IV Cont'd

Feedback Elements	$T_I(0)$	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)	$A_I(0)$	Deviation in $A_I(0)$ 225°K	375°K	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)
$R_e = 45\Omega$ $R_f = 425\Omega$	48.9	-.11 -4.2 -39 -65 -390	-97 +50 +770	9.99	-3.6%	+1.2%	-2.2 ± j4.2 -39 -65 -384	-64 ± j40 +23 ± j31
$R_e = 34\Omega$ $R_f = 320\Omega$	48.0	-.13 -3.7 -39 -67 -470	-108 -59 +770	10.00	-3.6%	+1.2%	-2.0 ± j4.3 -39 -61 -265	-63 ± j41 +22 ± j33
$R_e = 90\Omega$ $R_f = 846\Omega$	43.3	-.08 -5.6 -36 -61 -266	-76 +32 +770	9.96	-3.7%	+1.2%	-2.8 ± j3.5 -39 -61 -265	-71 ± j33 +28 ± j36
$R_e = 225\Omega$ $R_f = 2.16k\Omega$	27.1	-.06 -7.7 -39 -55 -195	-58 +17 +770	10.01	-4.4%	+1.5%	-2.6 -5.1 -39 -55 -195	-67 -107 +21 +61
$R_e = 450\Omega$ $R_f = 4.46k\Omega$	16.7	-.06 -9.0 -39 -50 -172	-50 +9.5 +770	9.97	-6.2%	+2.3%	-1.0 -8.0 -39 -50 -172	-52 -166 +10 +103

(c) Shunt-Series Pair

Table IV Cont'd

Feedback Elements	$A_I(0)$	Deviation in $A_I(0)$ 225°K	375°K	Poles (10^8 rad/sec)	Zeros (10^8 rad/sec)
R_e=45Ω R_f=590Ω	10.03	-7.8%	+2.4%	-3.9±j2.8 -39 -65 -366	-93 +47 +122
R_e=34Ω R_f=471Ω	10.00	-8.4%	+2.5%	-4.0±j2.8 -39 -66 -439	-104 +56 +100
R_e=90Ω R_f=1.08kΩ	10.03	-6.7%	+2.2%	-3.9±j2.0 -39 -60 -255	-73 +30 +198
R_e=225Ω R_f=2.56kΩ	10.00	-6.5%	+2.2%	-1.8 -7.0 -39 -54 -191	-57 +15 +349
R_e=450Ω R_f=5.17kΩ	10.02	-8.3%	+3.2%	-.88 -8.8 -39 -50 -170	-50 +8.8 +482

(d) Shunt-Series Cascade

Table IV Cont'd

Feedback Elements	$T_v(0)$	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)	$A_v(0)$	Deviation in $A_v(0)$ 225°K 375°K	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)
$R_{e1} = R_{e2}$ = 124Ω $R_f = 0$	600	-.048 -.63 -4.6 -20 -37 -43 -249 -253	-83 -83 +38 +38 +770.	31.58	-.55% +.21%	-.27 ± j 8. -1.29 -26 -34 -42 -168	-4.8 ± j 29 -43 ± j 35 -52 +9.7
$R_{e1} = R_{e2}$ = 200Ω R_f = 245Ω	180	-.049 -.79 -6.4 -19 -38 -42 -155 -163	-64 -64 +22 +22 +770	31.44	-1.2% +.6%	-1.34 -1.8 ± j 5.3 -23 -36 -42 -136 -220	-50 ± j 33 -50 +1.5 ± j 30 +8.3
$R_{e1} = R_{e2}$ = 500Ω R_f = 3.25kΩ	21	-.050 -1.0 -8.8 -19 -39 -42 -101 -112	-50 -50 +9. +9. +770	31.83	-2.7% +1.5%	-1.0 ± j .56 -7.0 -19.8 -38 -41 -102 -113	-46 -60 -102 +5.4 +28 ± j 12

(e) Series-Series Triple

Table IV Cont'd

Feedback Elements	$A_v(0)$	Deviation in $A_v(0)$ 225°K	375°K	Poles (10^8 rad/sec)	Zeros (10^8 rad/sec)
$R_{e1} = R_{e2}$ = 124Ω R_f = 0	31.67	-3.1%	+1.2%	-.77 -5 ± j 4.9 -19 -36 -55 -169 -175	-66 -66 +24 +24 +69
$R_{e1} = R_{e2}$ = 200Ω R_f = 245Ω	31.64	-3.7%	+1.9%	-.89 -4.5 ± j 3.0 -19 -37 -47 -134 -140	-58 -58 +17 +17 +151
$R_{e1} = R_{e2}$ = 500Ω R_f = 3.25kΩ	31.63	-4.8%	+2.6%	-.96 ± j .15 -8.4 -19 -39 -42 -98 -110	-49 -49 +8.1 +8.1 +464

(f) Series-Shunt-Series Cascade

Table IV Cont'd

Feedback Elements	$T_I(0)$	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)	$A_I(0)$	Deviation in $A_I(0)$ 225°k	375°k	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)
$R_e = \infty$ $R_{f1} = R_{f2}$ $= 790\Omega$	1650	-.13 -.52 -1.8 -35 -43 -73	+770. +770±j.01	31.58	-.31%	+.19%	+2.4±j4.4 -8.0 -33 -44 -73	-56±j25 +.16±j38 +30
$R_e = 200\Omega$ $R_{f1} = R_{f2}$ $= 397\Omega$	1100	-.14 -.58 -1.8 -35 -43 -73	+770. +770±j.01	31.61	-.31%	+.19%	+2.1±j4.2 -7.5 -33.5 -44 -76	-56±j25 +.17±j38 +30

(g) Shunt-Shunt Triple

Table IV Cont'd

FEEDBACK ELEMENTS	$A_I(0)$	DEVIATION IN $A_I(0)$ 225°K 375°K	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
$R_e = 500\Omega$ $R_{f1} = R_{f2}$ $= 1.26k\Omega$	31.14	-13.7% +8.5%	-1.6 $-4.8 \pm j2.9$ -30 -41 -73 -128	-49 +8.1 +222 +222
$R_e = 200\Omega$ $R_{f1} = R_{f2}$ $= 755\Omega$	31.49	-12.0% +6.3%	-2.3 $-4.5 \pm j2.8$ -32 -41 -75 -159	-58 +17 +150 +150
$R_e = 50\Omega$ $R_{f1} = R_{f2}$ $= 387\Omega$	32.21	-8.8% +4.5%	$-3.7 \pm j2.9$ -4.0 -35 -43 -80 -315	-90 +44 +84 +84

(h) SHUNT-SERIES-SHUNT CASCADE

Table IV Cont'd

b. Frequency response - two device configurations

The frequency performance of the feedback pairs and the corresponding two device cascades is seen to be very similar. There are two dominant poles associated with each of these configurations. The local feedback configurations are seen to provide a greater stability margin than the pairs. That is, for the complex dominant poles, $|\sigma|/|\omega|$ is larger for the cascades. This is to be expected since, as noted in Chapter 1, the overall feedback configurations represent a more effective use of feedback.

The feedback pairs offer a distinct advantage over the cascades from the standpoint of frequency compensation. The pairs can be treated on a root loci basis and hence possible techniques for improving the bandwidth may be immediately apparent from the open loop response. For example, a common broadbanding technique is the introduction of phantom zeros (i.e., zeros of the feedback path) into the open loop response.[15,18] Such zeros can be used to distort the root loci, yet they do not appear explicitly in the closed loop response. Of course, there are compensation techniques suitable for dealing with the local feedback cascades but often they are not as precise as the root loci approach.

If the response of the shunt-series feedback pair is examined carefully, a characteristic common to overall feedback configurations with a series feedback connection at the output becomes apparent. The feedback network of this configuration does not sample the output variable, the current in the resistive load, directly. Rather, it is fed by the total emitter current of the output transistor. At low frequencies this distinction appears only through the factor $1/\alpha_{o2}$ in the expression for f(0). However, because of capacitive loading at the output collector a zero is introduced into the relationship between the output and feedback currents. The complete expression for the feedback transmission in the shunt-series pair is:

$$f(p) = \frac{1}{\alpha_{o2}} \left(\frac{R_e}{R_e + R_f}\right)\left(1 - \frac{p}{z_o}\right) \qquad (2.4)$$

Through an extensive computer-aided analysis the zero, z_o, was found to be given by

$$z_o = -\frac{1}{R_L C_o} \qquad (2.5)$$

where R_L is the resistive load presented to the output collector and C_o is an effective capacitance load given by

$$C_o = C_{\mu 2} + C_{\rho 2} + C_L \qquad (2.6)$$

C_L is the actual capacitive load. The form of C_o may not be immediately apparent since $C_{\mu 2}$ is not a capacitance to ground. That equation (2.6) is correct is brought out in Appendix C.

The effect of the output zero is essentially to introduce a phantom zero into the response. Whether or not this zero is important depends on the relative magnitudes of C_o and R_L. For the shunt-series pair $R_L = 50\,\Omega$ and $C_{\mu 2} + C_{p2} = 4$ pF. Therefore, for no capacitive load, $z_o = -50 \times 10^8$ sec^{-1}. This value is well outside the dominant poles for the shunt-series pair. Hence the zero does not significantly affect the bandedge frequency response. It should be remembered, however, that the output zero is present in any configuration with series feedback at the output. In particular, the zero may have a dominant effect on the response of the series-series triple.

c. Frequency response - three device configurations

From Table IV the three transistor configurations are seen to exhibit three dominant poles. The additional dominant pole associated with these configurations, as compared to the two device circuits, may represent a significant broadband limitation.

Comparison of the open loop responses for the series-

series triple and the shunt-shunt triple reveals that the largest dominant pole is of considerably smaller magnitude for the latter configuration. This would seem to impose a severe limitation on the frequency performance of the shunt-shunt triple. It is virtually impossible to obtain a closed loop bandwidth that is greater than the magnitude of the third (largest) dominant pole while maintaining a monotonically decreasing response. Therefore, based on the open loop results of Table IV, the bandwidth for the shunt-shunt triple appears limited to values on the order of 30 MHz. As will become apparent in Chapter 3, this is considerably less than bandwidths that can be obtained with configurations such as the series-shunt pair and the series-series triple.

The series-series triple does not appear to suffer as severely from dominant pole limitations as the shunt-shunt configuration, though it certainly appears to present a more difficult broadbanding problem than do the feedback pairs. However, as noted earlier, the so-called output phantom zero associated with series feedback at the output must be taken into consideration. Because of the large load resistance presented to the triple the zero is of the same order of magnitude as the dominant open loop poles. For example, with R_L = 2 kΩ and no capacitive load the zero is located at -1.25×10^8 sec^{-1}. Since the open loop zeros tend to "peg" the closed loop

poles, the zero represents a bandwidth limitation in this case. Obviously the output zero must be increased in magnitude if the configuration is to be useful as a wideband amplifier. This increase can be effectively achieved through a reduction in R_L. The topic is taken up in Chapter 3.

A comparison between the local and overall feedback three device configuration leads to conclusions similar to those from the comparison of the feedback pairs and two device cascades. Feedback is more effectively utilized in the overall feedback configurations and as a result the dominant complex closed loop poles are pushed further from the real axis. Hence the stability question becomes an increasingly important problem with the feedback triples, witness the right-half plane poles for the shunt-shunt triple. Effective methods of frequency compensation are obviously mandatory.

d. Temperature sensitivity

The gain temperature sensitivity results in Table IV confirm the superiority of overall feedback in providing a desensitized response. For every overall configuration there is a significant reduction in sensitivity compared to the corresponding local feedback cascade.

The series-shunt pair and the shunt-series pair are quite similar from the standpoint of temperature

sensitivity, despite the fact that the loop gain is significantly larger for the shunt-series configuration. This is accounted for by a less sensitive forward transmission with the series-shunt circuit. The closed loop gain sensitivity is given by

$$\frac{dA(o)}{dT} = \frac{1}{1+T(o)} \frac{da(o)}{dT} \qquad (2.7)$$

Thus, while T(O) is larger for the shunt-series pair, so is the forward transmission sensitivity $da(o)/dT$. As a result the overall gain sensitivity is comparable for the pairs.

The best sensitivity performance obtained is that for the feedback triples. The advantage is even more significant when it is recognized that a cascade of only two triples is used to realize the same overall gain as a cascade of three feedback pairs. The sensitivity of such an overall gain is twice that of a single triple when a triple cascade is used, but when a pair cascade is used it is three times the sensitivity of the pair alone.

While the sensitivity performance of the shunt-series-shunt cascade is very poor, that of the series-shunt-series cascade is surprisingly good. Though still inferior to the feedback triples, this cascade does appear comparable to the feedback pairs on a sensitivity basis.

e. Summary

Based on the above results a summary comparison of the small-signal performance of the basic feedback configurations can now be made. The performance of the two device feedback cascades is relatively poor compared to the feedback pairs. While the cascades are satisfactory in terms of gain-bandwidth product, the pairs offer significantly superior desensitization to changes in temperature. Also, the pairs are somewhat easier to design and broadband. Between the feedback pairs themselves, there is little distinction on a small-signal basis.

The feedback triples offer the lowest gain sensitivity among the basic configurations but introduce broadbanding and stability problems. These problems appear virtually insurmountable in the shunt-shunt triple, but the series-series triple definitely appears worthy of further consideration. The excellent sensitivity performance of this warrants a detailed consideration of the broadbanding aspects.

The shunt-series-shunt cascade appears to be an inferior configuration on almost any basis of comparison. The series-shunt-series cascade displays adequate sensitivity performance but the configuration is difficult to design and broadband.

From a small-signal standpoint it thus appears that three of the eight configurations in Fig. 1 should be examined in more detail. These three are the shunt-series pair, the series-shunt pair and the series-series triple. The series-shunt-series cascade might also be considered if overriding dc problems arise with the overall feedback configurations.

IV. The Emitter-Coupled Pair

In the first chapter it was noted that the cc-cb stage might best be considered in terms of the feedback configuration of Fig. 5. This configuration is basically a series-shunt feedback pair with the emitter-coupled pair used as a composite device. The output voltage is sampled and a voltage is fed back to the base of the common-base transistor in the first emitter-coupled pair. The emitter voltage of the common-base device approximately follows the base voltage, assuming the feedback network represents a large load impedance for the base. A positive increment in this emitter voltage corresponds to a negative increment in the emitter voltage of the common-collector transistor. Thus, the feedback appears as negative series

feedback at the input.

The small-signal equivalent circuit corresponding to Fig. 5 is given in Fig. 11. If an approximation to the ideal feedback equation is established for this circuit, using the technique demonstrated in Appendix A, the low-frequency forward transmission is given by

$$a(0) = \beta_{o1}\beta_{o3}\left(\frac{R_I}{R_I + r_{x3} + r_{\pi 3} + r_{x4} + r_{\pi 4}}\right)\left(\frac{R_L(R_b + R_f)}{R_L + R_b + R_f}\right)$$
$$\left(\frac{R_b + R_f}{(R_s + r_{\pi 1} + r_{x1} + r_{\pi 2} + r_{x2})(R_b + R_f) + R_b R_f}\right) \qquad (2.8)$$

The feedback transfer function at low frequencies is

$$f(0) = -\frac{R_b}{R_b + R_f} \qquad (2.9)$$

The configuration of Fig. 5 was designed for an overall voltage gain of 10. The expression for $a_v(0)$ is of the same form as for the series-shunt and shunt-series pairs and hence, the design of the feedback network can be optimized in the manner of Appendix B. The maximum loop gain of $T(0) = 166$ is obtained for $R_b = 467\,\Omega$ and $R_f = 4.25\ k\Omega$. Note that the loop gain is much higher than that obtained for the feedback pairs. In fact, the loop gain is seen to be higher than that of a number of the feedback triple designs. However, the triples have a higher specification for $A_v(0)$. Thus, while the loop gain may be higher for the circuit of Fig.

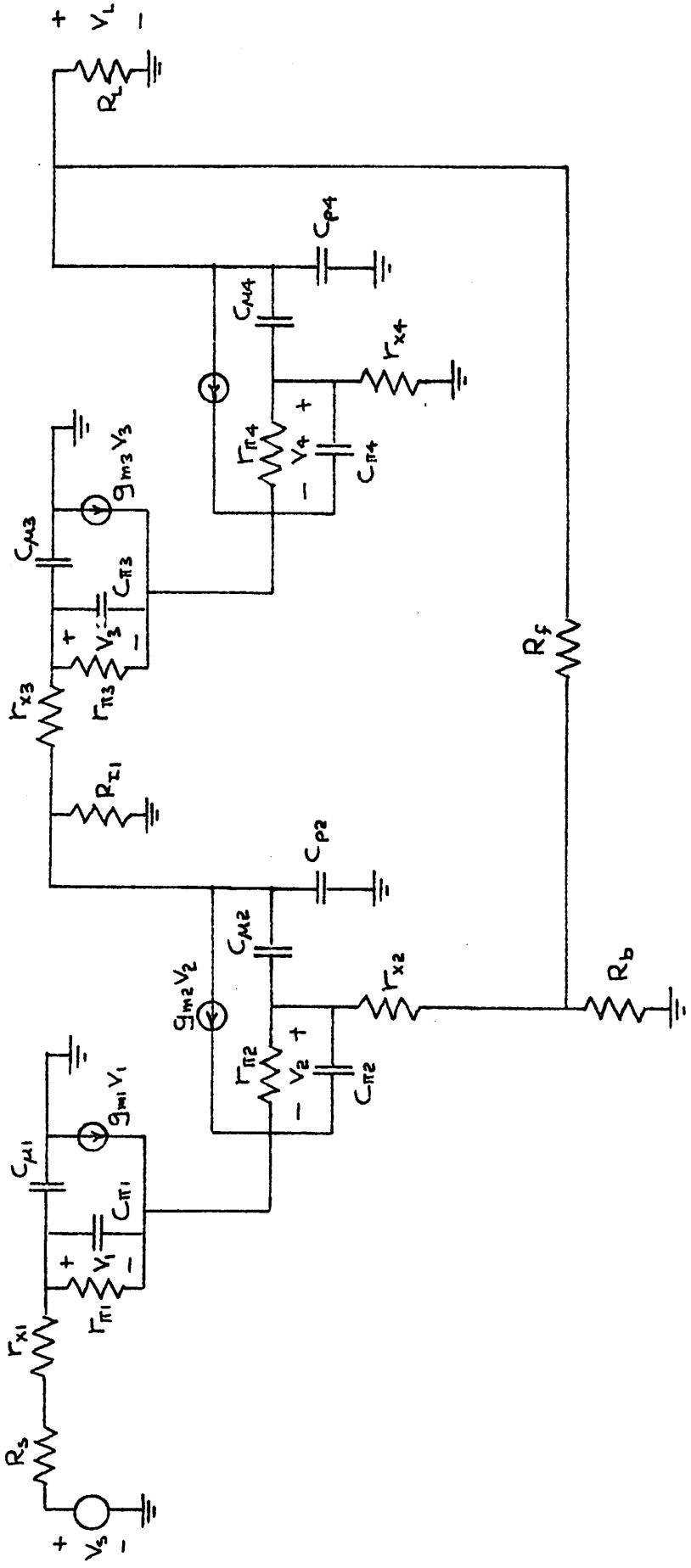


Fig. 11 Small-signal circuit for the configuration of Fig. 5

5 than for the triples, the triples still exhibit a larger forward transmission, a(0).

The small-signal open loop configuration corresponding to the maximum loop gain design for Fig. 11 was analyzed using the same transistor model as used for the circuits in Fig. 10. The results are given in Table V. Two serious disadvantages of the configuration are immediately apparent from the open loop response. First, a third dominant pole is present in comparison to the feedback pairs. More importantly, a dominant pair of the open loop poles is complex. Upon closing the feedback loop it is extremely difficult to maintain an unpeaked response, particularly with the large loop gain available.

The origin of the complex open loop poles is the interaction between the first and second emitter-coupled pairs. In the second pair, the common-base device exhibits an inductive input impedance that is magnified by the emitter-follower and presented to the first pair. Interaction between this inductance and output capacitance of the first common-base transistor leads to the complex pole pair.

Because of the disadvantages cited above, the configuration of Fig. 5 appears to be inferior to the feedback pairs and the series-series triple. Hence it will not be considered further.

Feedback Elements	$T_v(0)$	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)	$A_v(0)$	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)
$R_b = 467\Omega$ $R_f = 4.25k\Omega$	166	$-.26 \pm j.15$ -7.0 $-17.$ $-31.$ -40 -40 -66	-12 -28 $-20 \pm j30$ -40 -40	10.04	$+.65 \pm j\,3.4$ -9.1 -17.5 -31 -40 -40 -67	-12.7 -29 $-19 \pm j27$ -40 -40

Table V Analysis results for the configuration of Fig 11.

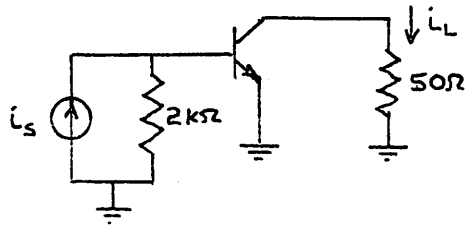
V. Analysis of the Composite Devices

In Chapter 1 three composite device configurations are noted to provide a higher gain-bandwidth product than a single common-emitter stage, when operating under comparable conditions. The cc-cb circuit is a non-inverting configuration and has already been considered in terms of the configuration in Fig. 5. The ce-cb and cc-ce configurations are suitable as direct replacements for a common-emitter stage and will now be investigated on a small-signal basis.

a. The ce-cb configuration

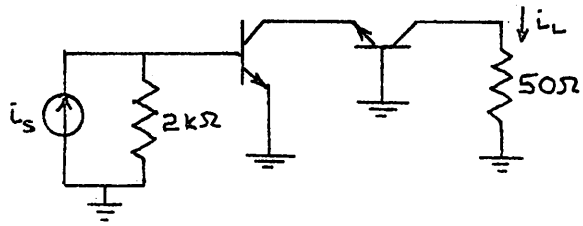
The cascode (ce-cb) circuit is a natural replacement for the common-emitter transistor in providing current amplification. Since the current gain of the common-base device is nearly unity, the current gain of the cascode is virtually the same as that of a common-emitter stage. However, the common-base transistor provides a low impedance load for the common-emitter transistor and hence reduces the Miller effect in that device. The result may be a significant broadbanding of the dominant pole.

In Fig. 12 the cascode is compared with a common-emitter stage on a current gain basis, driving a 50Ω load from a source with a 2 kΩ impedance. The same



$a_I(0)$	BAND-WIDTH	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
40.4	10MHz	-.623 -70.8	+770.

(a) Common-emitter stage



$a_I(0)$	BAND-WIDTH	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
39.7	13.5MHz	-.832 -18.2±j4.7 -79	-20±j30 +770.

(b) Ce-cb stage

Fig. 12 Comparison of the ce-cb stage with a common-emitter stage on a current gain basis

device model as used in previous work is assumed. The results indicate a marked shift in the dominant pole away from the origin. A pair of complex non-dominant poles that do not significantly affect the bandwidth are introduced. The net result is approximately a 35% increase in bandwidth.

On the basis of the results in Fig. 12, the cascode circuit appears attractive as a composite device. However, it should be noted that a single composite device is not often used to drive a load as low as 50Ω. Hence, the cascode has been analyzed for a number of larger load resistances. Results are summarized in Table VI. Also given in the table are the responses for a common-emitter stage operating into similar loads. Because of increased feedback through C_μ of the common-base transistor, an increase in the load resistance is seen to reduce drastically the magnitude of one of the non-dominant poles of the cascode. For example, when a load of 300Ω is used, the lowest non-dominant pole has moved in to $-4.44 \times 10^8 \text{ sec}^{-1}$. For an 800 Ω load this pole is moved in so far that a complex pair of dominant poles results. With a high load resistance the cascode still exhibits a higher gain-bandwidth product than a single common-emitter transistor driving a similar load; however, in a feedback loop the circuit has the effect of introducing an additional dominant pole.

R_L	CE-CB			COMMON-EMITTER		
	CURRENT GAIN	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)	CURRENT GAIN	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
50Ω	39.7	−.832 −18.2±j 4.7 −79	−20±j30 +770	40.4	−.623 −70.8	+770.
100Ω	39.7	−.841 −11.5 −24.7 −48	"	40.4	−.489 −45.3	"
200Ω	39.7	−.861 −6.47 −31.5±j 7.1	"	40.4	−.339 −32.6	"
300Ω	39.7	−.884 −4.44 −29.9±j 9.4	"	40.4	−.260 −28.4	"
800Ω	39.7	−1.23±j.26 −28.2±j11.0	"	40.4	−.119 −23.2	"
1 kΩ	39.7	−1.05±j.43 −28.0±j10.5	"	40.4	−.098 −22.6	"
2 kΩ	39.7	−.66±j.46 −27.6±j11.4		40.4	−.052 −21.4	"

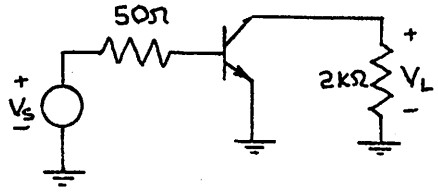
Table VI Effect of an increase in load resistance on the responses of the ce-cb and common-emitter stages. R_s = 2 kΩ

Thus, the cascode does not appear suitable for use as a composite device within a feedback configuration unless it is loaded by a resistance that is rather small, say less than 100 Ω.

b. The cc-ce configuration

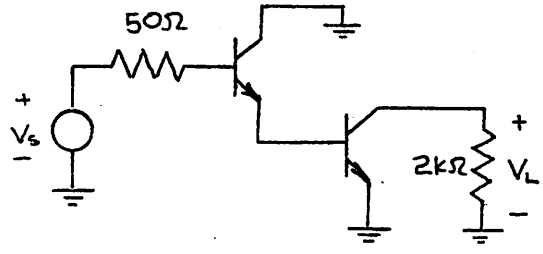
The low-frequency voltage gain of a common-emitter stage is not drastically altered by the addition of a common-collector transistor at the input. The voltage gain of the common-collector device is nearly unity. Thus, the generalized Darlington (cc-ce) circuit is compared to a single common-emitter device on the basis of voltage gain. A source resistance of 50Ω and a load of 2 kΩ are assumed in the initial analysis. The results are given in Fig. 13. The magnitude of the dominant pole is seen to be increased by about 15% in the cc-ce configuration as compared with the common-emitter stage. A second pole is introduced at approximately an order of magnitude above the dominant one. This pole may be undesirable in a feedback situation.

The responses of the cc-ce and common-emitter configurations are compared for increasing source impedances in Table VII. An increase in the source resistance for a cc-ce configuration has much the same effect as a load increase for the cascode. The lowest non-dominant pole



$a_v(0)$	Band-width	Poles (10^8 rad/sec)	Zeros (10^8 rad/sec)
191	1.8 MHz	-.112 -22.4	+770

(a) Common-emitter stage



$a_v(0)$	Band-width	Poles (10^8 rad/sec)	Zeros (10^8 rad/sec)
206	2.1 MHz	-.128 -13 -21 -89	-40.3 +770

(b) Cc-ce stage

Fig. 13 Comparison of the cc-ce stage with a common-emitter stage on a voltage gain basis

R_s	CC-CE			COMMON-EMITTER		
	VOLTAGE GAIN	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)	VOLTAGE GAIN	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
50Ω	206	-.128 -13.0 -21.1 -89.1	-40.3 +770.	191	-.112 -22.4	+770
100Ω	206	-.128 -10.7 -21.3 -86.2	"	174	-.100 -22.2	"
200Ω	205	-.127 -7.93 -21.5 -83.0	"	148	-.085 -21.9	"
300Ω	204	-.126 -6.34 -21.6 -81.3	"	129	-.076 -21.8	"
800Ω	200	-.123 -3.25 -21.7 -78.5	"	79	-.060 -21.5	"
1 kΩ	199	-.121 -2.75 -21.7 -78.0	"	68	-.058 -21.5	"
2 kΩ	191	-.114 -1.64 -21.8 -77.1	"	40	-.052 -21.4	"

Table VII Effect of an increase in source resistance on the responses of the cc-ce and common-emitter stages. R_L = 2 kΩ

is reduced in magnitude. The effect is not as severe as when the load for the cascode is increased, but none the less, the cc-ce cicuit does not appear suitable for use in a feedback configuration except when it is driven from a very low source or output resistance.

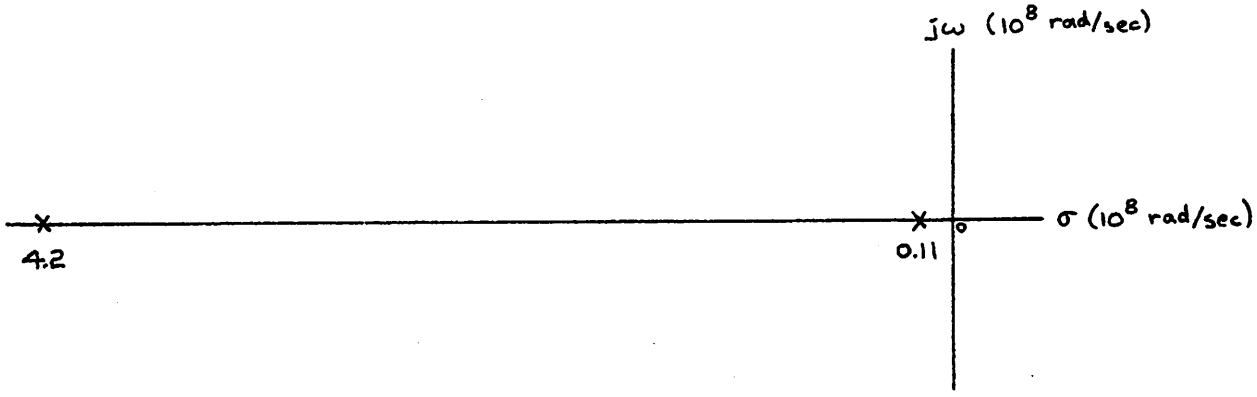
CHAPTER 3: BROADBANDING AND MONOLITHIC REALIZATION

In the previous chapter the basic configurations of Fig. 1 and the emitter-coupled configuration of Fig. 5 are analyzed strictly on a small-signal basis. The shunt-series pair, the series-shunt pair and the series-series triple are found to be the most suitable configurations for temperature insensitive broadband amplification. A further comparison among these configurations is now to be made through a detailed consideration of the problems faced in obtaining a complete integrated realization. In particular, the effects of dc level shifting and the various means of broadbanding are examined. From these considerations it will be shown that the shunt-series pair is not well suited to direct-coupled realizations. However, a decision as to the relative merits of the series-shunt pair and the series-series triple is not easily reached. A detailed consideration of possible broadbanding approaches does finally lead to a conclusion favoring the triple.

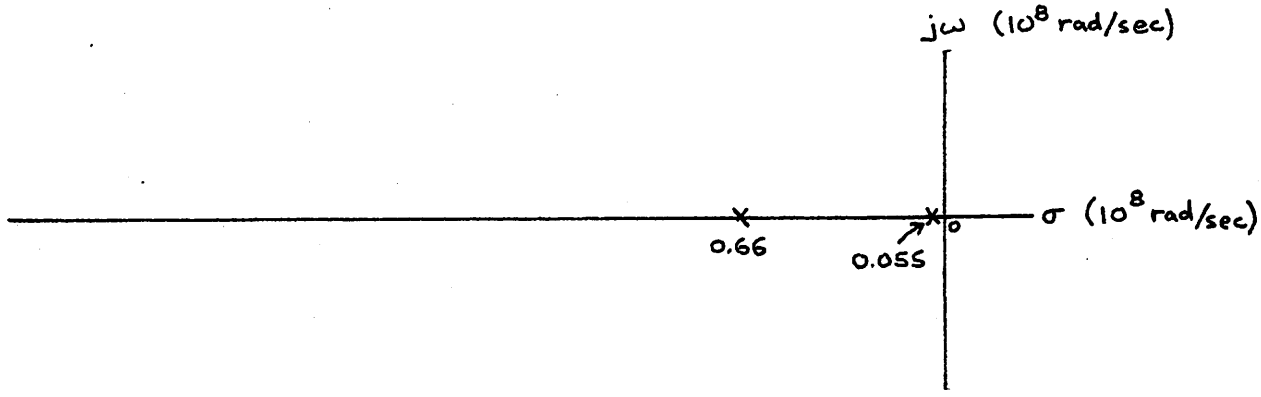
I. Consequences of Level Shifting

In Chapter 1 three approaches to dc level shifting in direct-coupled circuits are pointed out. The resistive level shifting technique (Fig. 8) is noted as the most suitable for wideband applications. With this technique the dc voltage drop is achieved simply by establishing a dc current through an appropriate resistor. A resistance of relatively large magnitude is required if typical low current levels are to be maintained. For example, a 2 kΩ reistor is needed if a 4 volt drop is to be achieved with a 2 mA current. Hence, it can be expected that a reistive level shift will present a high impedance load to the preceding network. This fact has immediate consequences with regard to the relative merits of the three configurations under consideration. The shunt-series pair is a natural current amplifier and has previously been examined with a low impedance load, while the series-shunt pair and series-series triple have been treated as voltage amplifiers driving high impedance loads. Thus, a resistive level-shift is consistent with the loading already considered for the series-shunt and series-series configurations, but the effect of such a high impedance load on the shunt-series pair is yet to be determined.

The shunt-series pair circuit of Fig. 10(c) is



(a) $R_L = 50\Omega$



(b) $R_L = 2k\Omega$

Fig. 14 Effect of an increase in load resistance on the dominant open loop poles of the shunt-series pair

analyzed using a 2 kΩ load in place of the natural 50Ω load. The resulting effect on the open loop natural frequencies is shown in Fig. 14. Both of the dominant poles are moved significantly toward the origin when the load is increased. The reduction in the magnitude of these poles is so severe that the broadband performance of the shunt-series configuration becomes markedly inferior to that of the series-shunt pair. Note that it is not feasible to improve the performance by shunting the input of the level shifting network with a small resistance (to reduce the load presented to the pair) because of the resulting loss in current gain.*

Because the series-shunt and shunt-series pairs offer similar sensitivity performance while resistive level shifting severely narrowbands the shunt-series configuration, the shunt-series pair is eliminated from further consideration.

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* It is assumed that the level shifting network will be located at the output of the block, as a load on the basic amplifier. If a resistive level shift is located within the amplifier, such as between the two transistors of the shunt-series pair, the associated gain attenuation reduces the amplifier loop gain. In addition, when located within the amplifier the level shifting network introduces another possibly significant pole into the feedback loop.

II. Broadbanding the Series-Shunt Pair and Series-Series Triple

At this point the series-shunt pair and the series-series triple remain for further investigation. Both configurations are considered as voltage amplifiers and appear well suited to monolithic realizations. The pair offers large bandwidth and fairly good sensitivity performance under low gain specifications. Also, it possesses a simple pole-zero distribution and as a result is easily designed and compensated. However, the pair does suffer from a limited loop gain. The triple provides a much larger loop gain, making it suitable for higher overall gain operation and leading to excellent response desensitization. The pole-zero distribution for the triple is somewhat more complicated than that for the pair and hence broadbanding may be more difficult.

In this section both the pair and the triple are to be broadbanded using simple capacitive compensation. The primary aim is to determine whether a bandwidth approaching that of the pair can be obtained for the triple.

Note that for any compensation scheme which is considered, element tolerances must be sufficiently large so as to make monolithic realization practical.

a. The series-shunt pair

The dominant and lowest non-dominant open loop pole locations for the series-shunt pair (corresponding to the $R_e = 47\Omega$ design of Chapter 2) are shown in Fig. 15. Compensation for broadbanding the pair is obtained via a shunt capacitor across the resistor R_f. This capacitor leads to a feedback transfer function

$$f_v(p) = \left(\frac{R_e}{R_e + R_f}\right) \frac{\left(1 - \frac{p}{z_f}\right)}{\left(1 - \frac{p}{p_f}\right)} \qquad (3.1)$$

where

$$z_f = -\frac{1}{R_f C_f}$$

$$p_f = -\frac{R_e + R_f}{R_e R_f} \frac{1}{C_f} \qquad (3.2)$$

The pole p_f is generally non-dominant since R_e is significantly less than R_f in most cases. The effect of the capacitor on the dominant pole loci arises from the phantom zero introduced at z_f.

Distortion of the dominant pole loci so as to broadband the pair can be obtained with the phantom zero in two ways. In Fig. 16 the zero is located outside both dominant poles. Upon closing the feedback loop the poles move together and split into the complex plane, assuming the loop gain is sufficient. The presence of the zero bends the loci away from the imaginary axis until the lowest non-dominant pole, which

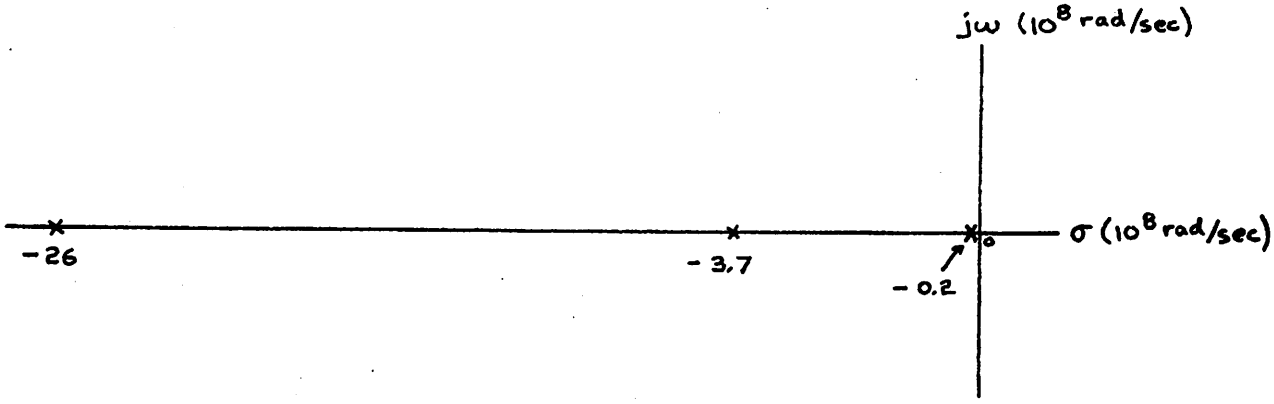


Fig. 15 Open loop poles of the series-shunt pair

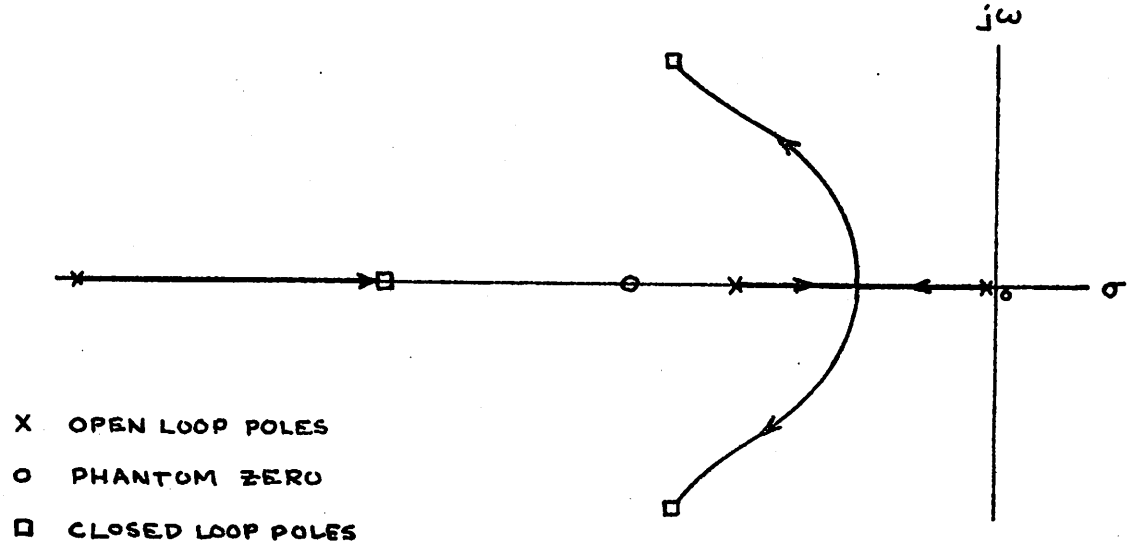


Fig. 16 One approach to positioning the phantom zero for broadbanding of the series-shunt pair

may be p_ϕ, approaches the zero. If there were no non-dominant poles the dominant pole loci would return to the negative real axis outside the phantom zero.

The extent of the broadbanding obtainable with the technique of Fig. 16 depends on how severely the loci can be bent toward the phantom zero and away from the imaginary axis. The closer the zero is located to the largest dominant pole, the more severe the distortion of the loci. However, the zero is also drawing in the lowest non-dominant pole and hence, the closer the zero is to the origin, the smaller the magnitude of this third pole in the closed loop response. If the third pole is brought in too far it may become the dominant factor governing the frequency performance.

For the $A_v(0) = 10$ specification with $R_e = 47\,\Omega$ the frequency response was determined for a number of phantom zero locations outside both dominant poles. Representative results are given in Table VIII. In case 1 the phantom zero is located too far out from the dominant poles and as a result the dominant pole loci are not sufficiently distorted; this leads to peaking in the frequency response corresponding to case 1. The zero location in case 2 appears to be near-optimum. For this case the complex poles lie at approximately 47° from the negative real axis with a magnitude of 5.15×10^8 sec^{-1}. The third pole is located

CASE	C_f	Z_f (10^8 rad/sec)	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
1	3.3pF	-6.9	-3.07±j3.87 -12.6 -42.3 -111.	-46.3±j12.3 +12.3±j24.4
2	3.9pF	-5.9	-3.48±j3.8 -10.6 -43. -106	-44.8±j12.3 +11.3±j23.8
3	5.1pF	-4.5	-4.83±j4.07 -6.01 -43 -97	-42.5±j6.98 +9.8±j23.
4	6pF	-3.8	-5.3±j5.1 -3.96 -43 -93	-38 -44 +8.8±j22.

Table VIII Series-shunt pairs responses for the phantom zero located as in Fig. 16

at -10.6×10^{8} sec^{-1}. The resulting bandwidth is 78 MHz. For the magnitude of z_f smaller than that in case 2, as in cases 3 and 4, the lowest non-dominant pole is brought in so far that it represents a limitation on the bandwidth.

An alternative possiblity for broadbanding the series-shunt pair is shown in Fig. 17. Here the phantom zero is located between the two dominant poles, preferably just inside the pole of larger magnitude. Upon closing the feedback loop the dominant pole closest to the origin moves out toward the zero; the dominant pole outside the zero moves to meet the lowest non-dominant pole. For this situation the frequency performance is governed primarily by lowest pole. The important conditions for using this technique are an accurate knowledge of the location of the largest dominant open loop pole, so the zero can be positioned just inside it, and sufficient loop gain to move the lowest pole close to the zero.

For the $R = 47\,\Omega$ design the second dominant pole is located at $-3.65\times10^{8}\,sec^{-1}$. Therefore the magnitude of the lowest closed loop pole, and hence the bandwidth is at best on the order of 50 MHz. This is well below the bandwidth obtainable with the approach of Fig. 16. In order to improve the performance it is necessary to move the second open loop pole away from the origin. This can be done through the use of a "pole-splitting"

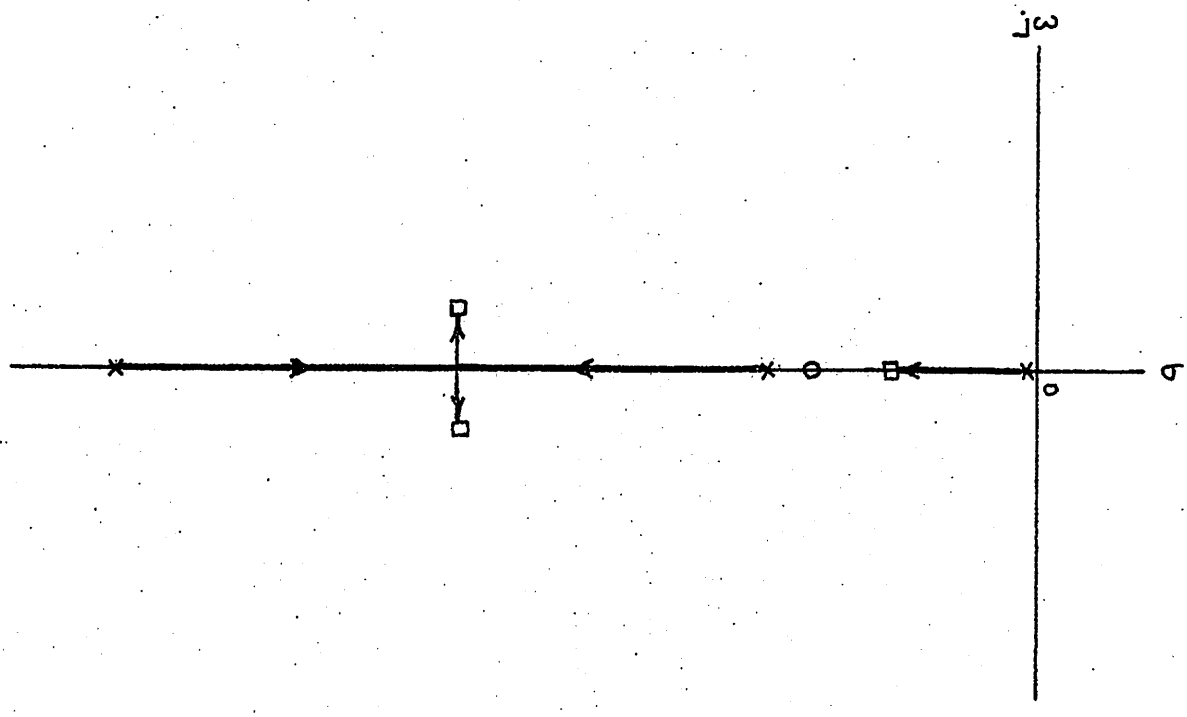


Fig. 17 Alternative positioning of the phantom zero in the series-shunt pair

capacitor in the forward transmission path.[2,11,15] A capacitor, C_s, between the collector and base of the shunt feedback transistor in the pair accomplishes the pole-splitting function (Fig. 18). In Table IX results are given for C_s = 5, 10 and 15 pF. For C_s = 10 pF the second open loop pole is moved out to $-6.25 \times 10^8 \text{ sec}^{-1}$. Hence, the phantom zero can be located much further from the origin than is the case without C_s. However, a new problem arises when C_s is used. Besides moving the second pole out, the lowest pole is moved in significantly. In the case of C_s = 10 pF it has been shifted to $-0.046 \times 10^8 \text{ sec}^{-1}$. The question arises as to whether the loop gain is still sufficient to bring the lowest pole out to the zero. Upon closing the loop with C_s = 10 pF, the dominant pole only moves out to $-1.48 \times 10^8 \text{ sec}^{-1}$. This indicates that the loop gain is not sufficient to achieve the desired broadbanding by the technique of Fig. 17. A number of additional designs were examined where less severe pole-splitting was employed, but it does not appear possible to obtain bandwidths as large as can be achieved with the approach of Fig. 16.

In summary, optimum broadband performance for the series-shunt pair appears to result from the compensation approach of Fig. 16. Pole-splitting does not appear to be a particularly desirable technique when dealing with

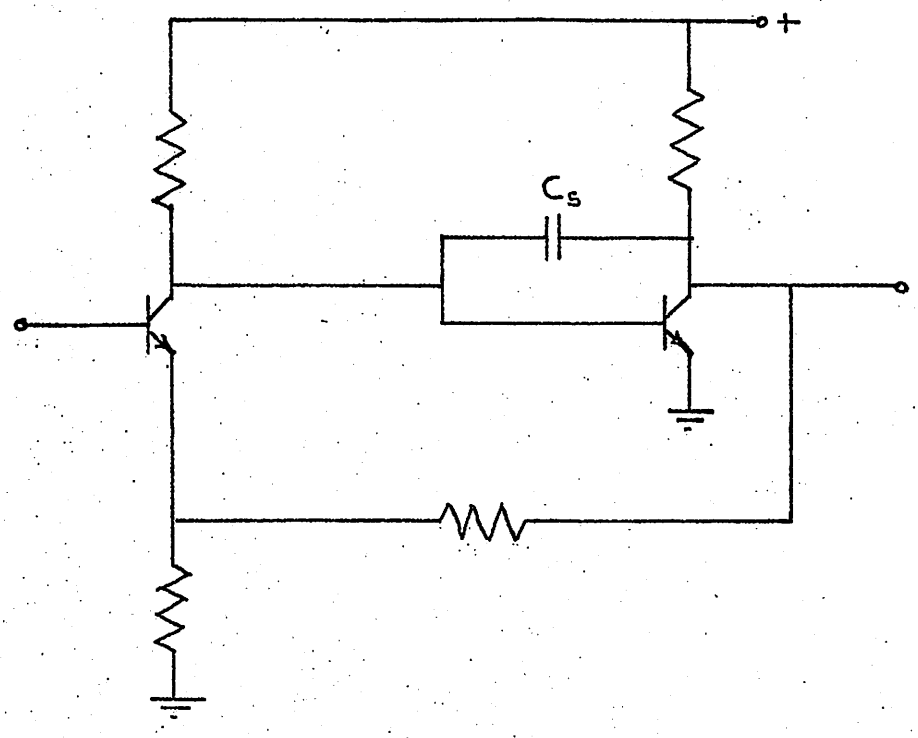


Fig. 18 Pole-splitting capacitor, C_s, in the series-shunt pair

C_s	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)
0	-.202 -3.65 -26.2 -40.5 -325	-96 +49 +770
5pF	-.075 -5.4 $-21.4 \pm j\,8.4$ -247	-23.9 -95 +21 +49
10 pF	-.046 -6.25 $-19.1 \pm j\,8.0$ -238	-17.2 -95 +15 +49
15 pF	-.026 -7.07 $-17.6 \pm j\,7.39$ -234	-14.3 -95 +12 +49

Table IX Effect of pole-splitting on the open loop response of the series-shunt pair

the pair because of the limited loop gain available. The largest closed loop bandwidth obtained for the series-shunt pair is 78 MHz, corresponding to case 3 of Table VIII.

b. The series-series triple

As noted in Chapter 2, the first consideration in broadbanding the series-series triple is the positioning of the feedback zero associated with the output collector. For the 2 kΩ load resistance used in Chapter 2, the output zero is located at $-1.25\times10^{8}\ sec^{-1}$ and represents a broadband limitation. In order to increase the magnitude of the zero, the net load resistance must be reduced. If the load resistance is changed from 2 kΩ to 200Ω, sufficient latitude is provided for the positioning of the zero through control of C_L. For no capacitive loading, a load resistance of 200Ω places the zero at $-12.5\times10^{8}\ sec^{-1}$. In any actual building block realization some load capacitance can be expected. For example, if the triple is to drive a resistive level shifting network such as that of Fig. 8, the input of the level shift appears approximately as a capacitive load. Because of the large series emitter resistance for the emitter-follower, the input capacitance is essentially C_μ of the common-collector transistor. For this situation

the output phantom zero (equation (2.5)) is located at $-8.33 \times 10^8 \text{ sec}^{-1}$.

It might first appear that the reduction of the load resistance to 200 Ω would seriously degrade the loop gain of the triple. This in fact is not the case if the values of R_f, R_{e1} and R_{e2} are modified to adjust for the change in loading on $a_v(\rho)$. For example, with a 2 kΩ load and a gain specification of 31.6 the maximum loop gain is obtained for $R_f = 0$, $R_{e1} = R_{e2} = 124\ \Omega$. Reduction in R_L to 200 Ω implies a corresponding reduction to $R_f = 0$, $R_{e1} = R_{e2} = 12.4\ \Omega$ if maximum loop gain is to be maintained. With this in mind a number of new designs were carried out for the series-series triple with $R_L = 200\ \Omega$. Values of $R_{e1} = R_{e2}$ were specified as 12.4 Ω, 50 Ω and 100 Ω. For a closed loop low-frequency gain of 31.6, appropriate values of R_f are given in Table X. Also given in this table are the values of $T_v(0)$ and the small-signal analysis results for the open loop pole and zero locations, and the closed loop low-frequency gain sensitivity.

The results in Table X indicate that, while the designs using low values for R_{e1} and R_{e2} exhibit a very high loop gain, the second and third dominant poles are of a considerably reduced magnitude for these designs. In order to obtain optimum broadband performance for the triple, the value of $R_{e1} = R_{e2}$ should be made as large

Feedback Elements	$T_V(0)$	$A_V(0)$	Deviation of $A_V(0)$ 225°K 375°K	Open Loop Poles (10^8 rad/sec)	Open Loop Zeros (10^8 rad/sec)
$R_{e1} = R_{e2}$ = 12.4Ω $R_f = 0$	546	31.7		-.115 -.834 -2.15 -30.5 -37.3 -43.8 -1740. -1752.	-12.5 -40.3 -224. +142. +770.
$R_{e1} = R_{e2}$ = 50Ω R_f = 303Ω	98.6	31.3	-1.3% +.64%	-.076 -2.11 -4.32 -29.3 -37.8 -43.2 -318. -332.	-12.5 -40.3 -94.1 +47.9 +770.
$R_{e1} = R_{e2}$ = 100Ω R_f = 1.45kΩ	35.5	31.4	-2.5% +1.2%	-.064 -3.17 -6.06 -28.2 -38.2 -42.7 -191. -270.	-12.5 -40.3 -72.1 +29.1 +770.

Table X Small-signal responses of the series-series triple designs for a load resistance of 200 Ω

as possible while still maintaining sufficient loop gain to position the closed loop poles properly. A low R_e design could be used along with a pole-splitting technique to increase the magnitude of the second and third dominant poles. However, because of the severe reduction in the magnitude of the lowest pole when a pole-splitting capacitor is used, a correspondingly larger loop gain is required for positioning the closed loop poles. The net effect remains about the same as merely increasing the specification for $R_{e1} = R_{e2}$. Extensive computer-aided analysis indicates that better performance can generally be obtained through increasing the emitter feedback resistors than by using a pole-splitting capacitor. The former approach also has the advantage of requiring fewer capacitors to be fabricated.

The $R_{e1} = R_{e2} = 50\,\Omega$ design of Table X represents a suitable compromise between the positioning of the open loop poles and the amount of loop gain available. In broadbanding this configuration two negative real axis phantom zeros are available: z_o associated with the series feedback at the output, and z_f resulting from the use of a capacitor in shunt with R_f. Possible locations for these zeros relative to the dominant open loop poles are shown in Fig. 19.

In cases (a) and (b) of Fig. 19, the bandwidth is limited by the location of the second lowest open loop pole. For the triple, the magnitude of this second pole

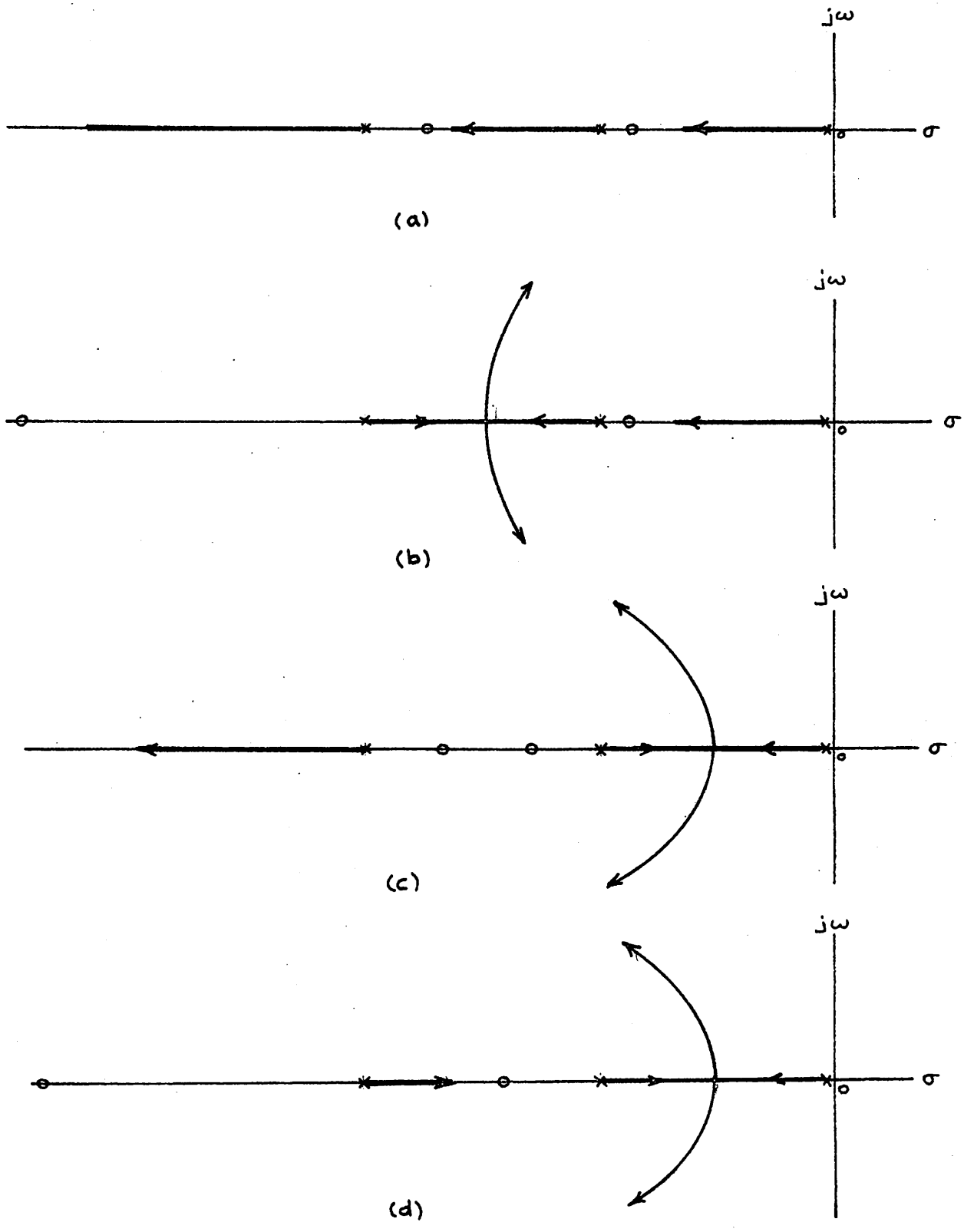


Fig. 19 Possible phantom zero locations for the series-series triple

is relatively small and hence the bandwidth obtainable in cases (a) and (b) is considerably less than that which can be achieved when the zeros are positioned as in case (d).

In Fig. 19(c) both feedback zeros are located between the second and third dominant poles, while in Fig. 19(d) the output zero is moved as far from the origin as possible. Which of these approaches will lead to the largest bandwidth can be perceived by considering the ideal feedback equation in the limit when $T(p)$ is large. For this limit $A(p) \simeq 1/f(p)$ so that the closed loop poles correspond to the feedback zeros. Hence, Fig. 19(c) corresponds to a two pole response with the poles in the neighborhood of the two phantom zeros, while Fig. 19(d) should lead to a response with a bandwidth which is nearly that of the single phantom zero, z_f. On this basis one might guess that the approach used in case (d) provides a larger bandwidth.

In Table XI typical results for broadbanding the $R_{e1} = R_{e2} = 50\,\Omega$ design with zero locations as in Fig. 19(c) are presented. These results, together with those of Table XII, clearly indicate the superiority of the technique of Fig. 19(d). For case (c) the lowest complex pole pair is not drawn sharply toward the phantom zeros but is pushed well away from the negative real axis. In addition, the third dominant pole and the lowest non-dominant

C_f	z_f (10^8 rad/sec)	Closed Loop Poles (10^8 rad/sec)	Closed Loop Zeros (10^8 rad/sec)	Bandwidth
11.8 pF	-2.8	$-2.74 \pm j6.05$ $-3.02 \pm j.753$ -18.7 -34.6 -42.7 -227	$-.54 \pm j31.4$ -12.0 $-43.1 \pm j39.0$ -58.3 +16.2	39 MHz
11 pF	-3.0	$-2.85 \pm j5.74$ $-3.18 \pm j.855$ -19.2 -34.6 -42.7 -227	$-.36 \pm j31.3$ -12.9 $-43.0 \pm j39.0$ -58.2 +16.3	42 MHz
10 pF	-3.3	$-2.90 \pm j5.6$ $-3.47 \pm j.945$ -20.1 -34.5 -42.7 -227	$-.083 \pm j31.2$ -4.2 $-42.8 \pm j39.1$ -58.2 +16.3	46 MHz

Table XI Results for broadbanding the series-series triple with the phantom zeros located as in Fig. 19(c)

pole split off the real axis and are brought quite close to the phantom zero locations. These poles have a dominant effect on the closed loop response and limit the bandwidth to less than 50 MHz. The shape of the root loci corresponding to Fig. 19(c) is shown in Fig. 20.

In Table XII representative results are given for broadbanding the $R_{e1} = R_{e2} = 50\ \Omega$ design via the approach of Fig. 19(d). Note that in this approach the output phantom zero is moved as far as possible from the origin and is not critical in determining the response. This is desirable since the output zero depends on active device and load capacitiances and hence is not as well controlled as $z_f = 1/R_f C_f$. Also, no C_L need be added to position the output zero.

In case 1 of Table XII, the complex poles have not been moved far enough from the real axis to provide the maximum bandwidth commensurate with a monotonic roll off. In case 2, a peaked response results since the complex poles are not moved far enough from the imaginary axis. Case 3 corresponds to the largest bandwidth that could be obtained for the series-series triple under the specification $A_v(0) = 31.6$. The dominant poles in this case are located at $-3.58\text{x}10^8\ \text{sec}^{-1}$ and $-1.85 \pm j4.43\text{x}10^8\ \text{sec}^{-1}$. The bandwidth is 80 MHz and the response is nearly maximally flat magnitude.

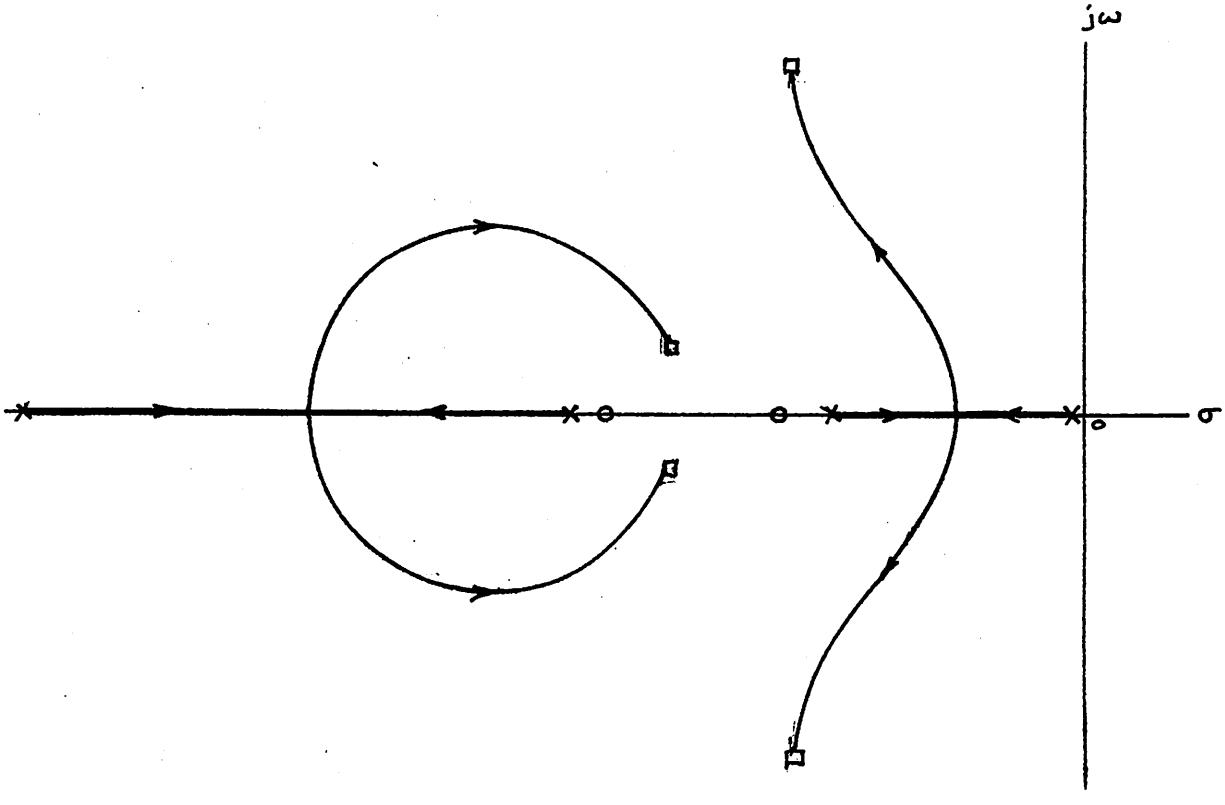


Fig. 20 Actual shape of the root loci when the phantom zeros are located as in Fig. 19(c) and a non-dominant pole is present

CASE	C_F	Z_f (10^8 rad/sec)	CLOSED LOOP POLES (10^8 rad/sec)	CLOSED LOOP ZEROS (10^8 rad/sec)	BAND-WIDTH
1	11.8pF	-2.8	-1.99±j4.92 -2.96 -9.79 -25.8 -34.3 -42.7 -257	-.54±j31.4 -12.0 -43.1±j39.0 -58.3 +16.2	74MHz
2	8.3pF	-4.0	-1.57±j4.05 -4.19 -13.5 -32.9 -32.9 -42.6 -257	-17.3 -42.4±j39.3 -57.9 +.522±j31.0 +16.6	PEAKED
3	10pF	-3.3	-1.85±j4.43 -3.58 -11.4 -26.8 -33.9 -42.7 -257	-.083±j31.2 -14.2 -42.8±j39.1 -58.2 +16.3	80MHz

Table XII Results for broadbanding the series-series triple with the phantom zeros located as in Fig. 19(d)

A number of attempts at broadbanding the $R_{e1} = R_{e2} = 50\Omega$ design were made using a pole-splitting capacitor between the collector and base of the second transistor in the triple. Values of 1, 2, 3, and 4 pF were used. In no case could a bandwidth larger than 80 MHz be obtained.

III. Conclusion

Based on the preceding results the series-series triple definitely appears to be the most suitable configuration for desensitized wideband amplification in integrated circuits. Though the pole-zero distribution is more complicated for this configuration than for the feedback pairs, a bandwidth comparable to that of the pairs can be achieved while providing a larger low-frequency gain and a much lower gain temperature sensitivity.

CHAPTER 4: FINAL AMPLIFIER DESIGN

In this chapter a complete design for a gain block, based on the series-series triple configuration, is developed. A low-frequency gain of 50 with a bandwidth greater than 50 MHz is specified. Gain sensitivity is to be less than a deviation of 0.3 dB over the full temperature range -55°C to 125°C. A zero volt dc level is to be maintained at the input and output. With a view toward possible realization of the design, devices are characterized as those that can be achieved in the forseeable future in the integrated circuits laboratory at Berkeley. Device parameters are summarized in Table XIII. The small-signal model of Fig. 9(b) is used in the analysis.

Element	Nominal Value	Assumed Temperature Dependence
Transistors		
β_o	80	Linear, +6000 ppm/°K @ 300°K
f_t	500 MHz	Insensitive
C_μ	1 pF	Insensitive
C_p	2 pF	Insensitive
r_x	200 Ω	Linear, +2000 ppm/°K @ 300°K
Base Diffused Resistors	200 Ω/□	Linear, +2000 ppm/°K @ 300°K
MOS Capacitors	.2 pF/mil²	Insensitive

Table XIII Device parameters assumed for design of the gain block

I. The Level Shifting Network

The series-series has been chosen for realizing the basic building block and the next step is to establish the level shifting network. A resistive level shift is to be used and has the general representation of Fig. 21. In this representation an ideal current source is used to bias the configuration. Such a source exhibits an infinite impedance and hence gain attenuation through the level shift is minimized. Two ways of approximating this current source are shown in Fig. 22.

In Fig. 22(a), as in Fig. 8, a transistor current source is used. This approach has the advantage of maintaining a very high impedance source, but it also entails a serious disadvantage in terms of frequency performance. In Fig. 22(b) the current source is approximated by a resistor. This leads to significant gain attenuation, but frequency limitations are avoided.

The small-signal equivalent circuits corresponding to the configurations of Fig. 22 have been analyzed using the transistor model employed in Chapters 2 and 3. A voltage source drive and 10 kΩ load are assumed. The voltage gain is the transfer function of interest. If a 1 kΩ level-shifting resistor, R_{LS}, is assumed, the configuration of Fig. 22(a) results in a voltage transfer ratio of 0.9 at low frequencies. Because of the capacitance seen at the collector of the current source transistor,

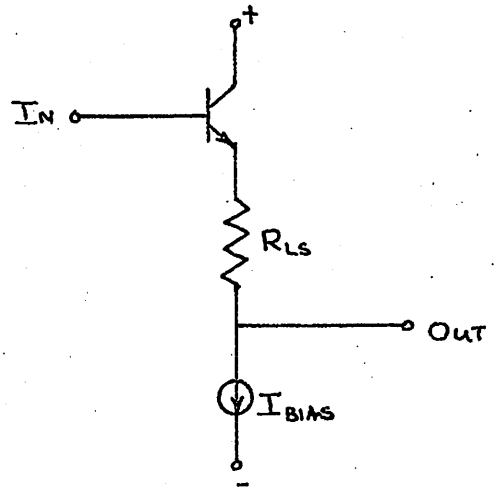


Fig. 21 General resistive level shift

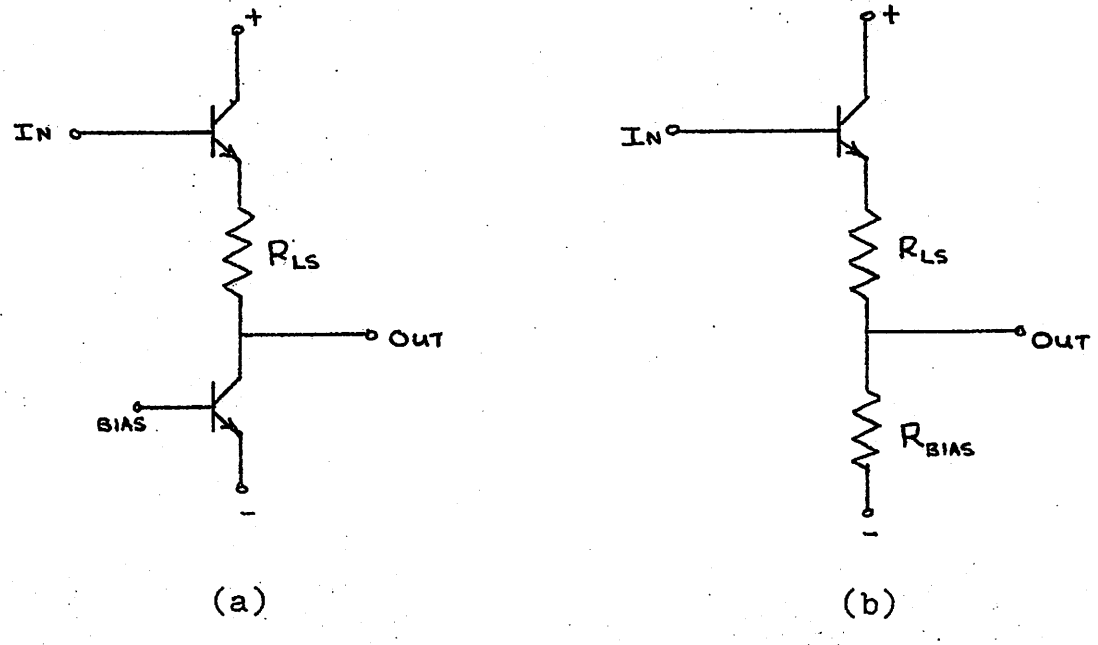


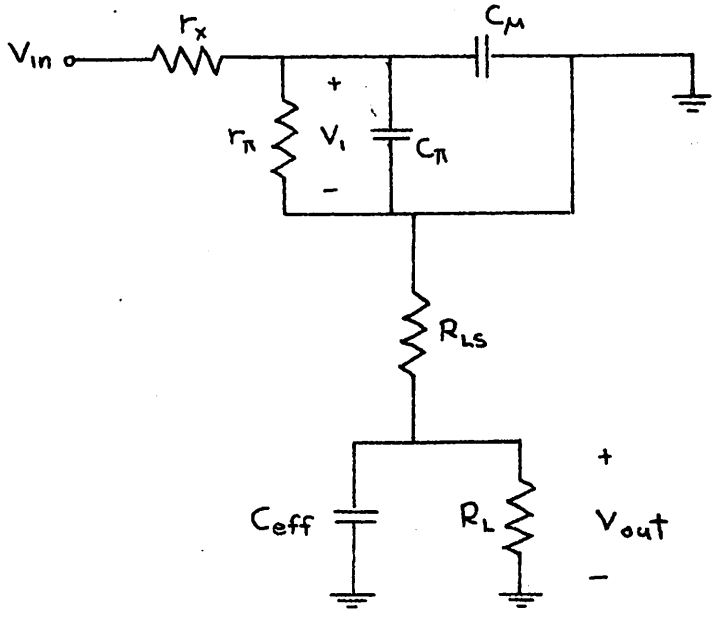
Fig. 22 Practical configurations for the resistive level shift

which is of the order of 4 pF and is in shunt with the 10 kΩ load resistance, the configuration exhibits a pole at $-2.7\times10^{8}\ sec^{-1}$. The presence of this low pole is found in general for the network of Fig. 22(a) and, hence, this circuit has severe limitations as far as wideband applications are concerned.

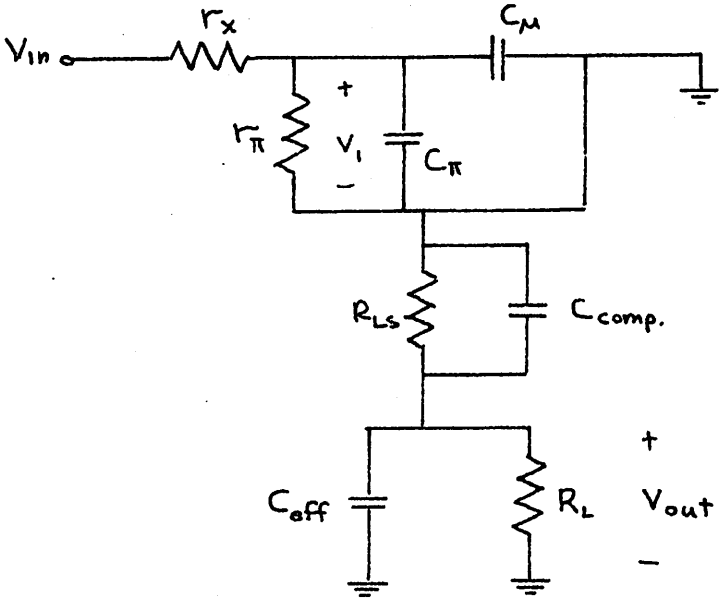
A possible solution to the frequency problem encountered with the circuit of Fig. 22(a) is the use of capacitive compensation across the level shift resistance, R_{LS}. The small-signal equivalent circuit for Fig. 22(a) can be approximated as shown in Fig. 23(a) For this circuit the dominant pole is located at $-1/R_L C_{eff}$. To compensate for this pole, a capacitor is introduced across R_{LS} (Fig. 23(b)) such that

$$R_L C_{eff} = R_{LS} C_{comp} \qquad (4.1)$$

Analysis of the actual small-signal configuration (based on Fig. 22(a)) when C_{comp} is introduced indicates that compensation is achieved. However, since C_{eff} is only an approximation to the loading presented by the bias transistor, it is virtually impossible to cancel precisely the dominant pole. In any case, a precise capacitance value could not be realized monolithically. As a result, a significant dip occurs in the gain magnitude-frequency response. This is illustrated in Fig. 24. Such a distorted response is generally not considered acceptable.



(a)



(b)

Fig. 23 (a) Approximate small-signal representation of the configuration of Fig. 22(a)

(b) Introduction of a compensation capacitor to achieve pole-zero cancellation

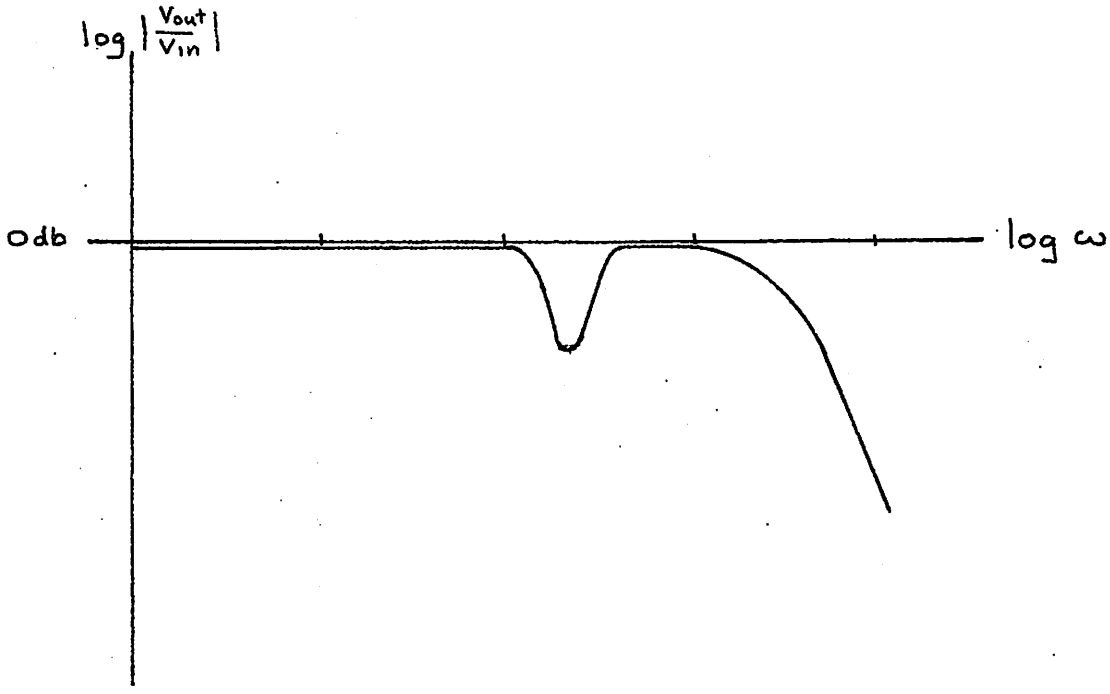


Fig. 24 Typical response shape when a compensation capacitor is used in Fig. 22(a)

Because of the frequency limitations of the transistor biased level shift, the configuration of Fig. 22(b) will be used in the block design. For typical resistor values of R_{LS} = 1 kΩ and R_{BIAS} = 3 kΩ, the voltage transfer ratio at low frequencies is 0.74 when a 10 kΩ load is assumed. The smallest pole of this configuration is located at $-29.9 \times 10^{8} sec^{-1}$ and is thus non-dominant with regard to the expected frequency response for the block.

II. Design of the Complete Block

The configuration chosen for the complete gain block is shown in Fig. 25. Most of the numerical design proceeds on a dc basis. Except for the elements R_{e1}, R_{e2}, C_f and R_D, element values are established from dc considerations. Of course, the choice of R_f must be such as to assure an adequate loop gain. That is, R_f cannot be chosen to be excessively large.

The dc design is carried out through consideration of the common mode equivalent half-circuit shown in Fig. 26. Transistor Q_{B1} provides the bias for devices

Q_1 and Q_3 and is driven by common mode feedback through the diode-connected transistor Q_{B2}. The feedback tends to dc stabilize the configuration in the following manner. Suppose, for some reason such as temperature, the base-emitter voltage of Q_2 begins to rise. This leads to an increase in the collector current of Q_2 and therefore the current in Q_{B2} increases. Since Q_{B1} and Q_{B2} are driven by the same base-emitter voltage, the current in Q_{B1} will increase. As a result, the collector current of Q_1 increases and there is a corresponding decrease in the collector voltage of Q_1. Thus, the tendency for the base-emitter voltage of Q_2 to increase is opposed. Because of this dc feedback, a suitable operating point can be maintained over large changes in temperature.

The bias transistors Q_{B1} and Q_{B2} are driven by the same base-emitter voltage. Hence, the ratio of collector currents in these devices is the same as the ratio of emitter areas. Thus, the amount of current in Q_{B1} relative to that in Q_{B2} is controlled by specifying the relative emitter areas for these devices.

Transistors Q_{B3} and Q_{B4} represent a common mode feedback loop that is used to maintain the dc output voltage at zero.[6] The average output voltage is sampled through the large resistors R_A and is fed into the differential pair formed by Q_{B3} and Q_{B4}. The other side of this pair is referenced to ground through a resistance comparable

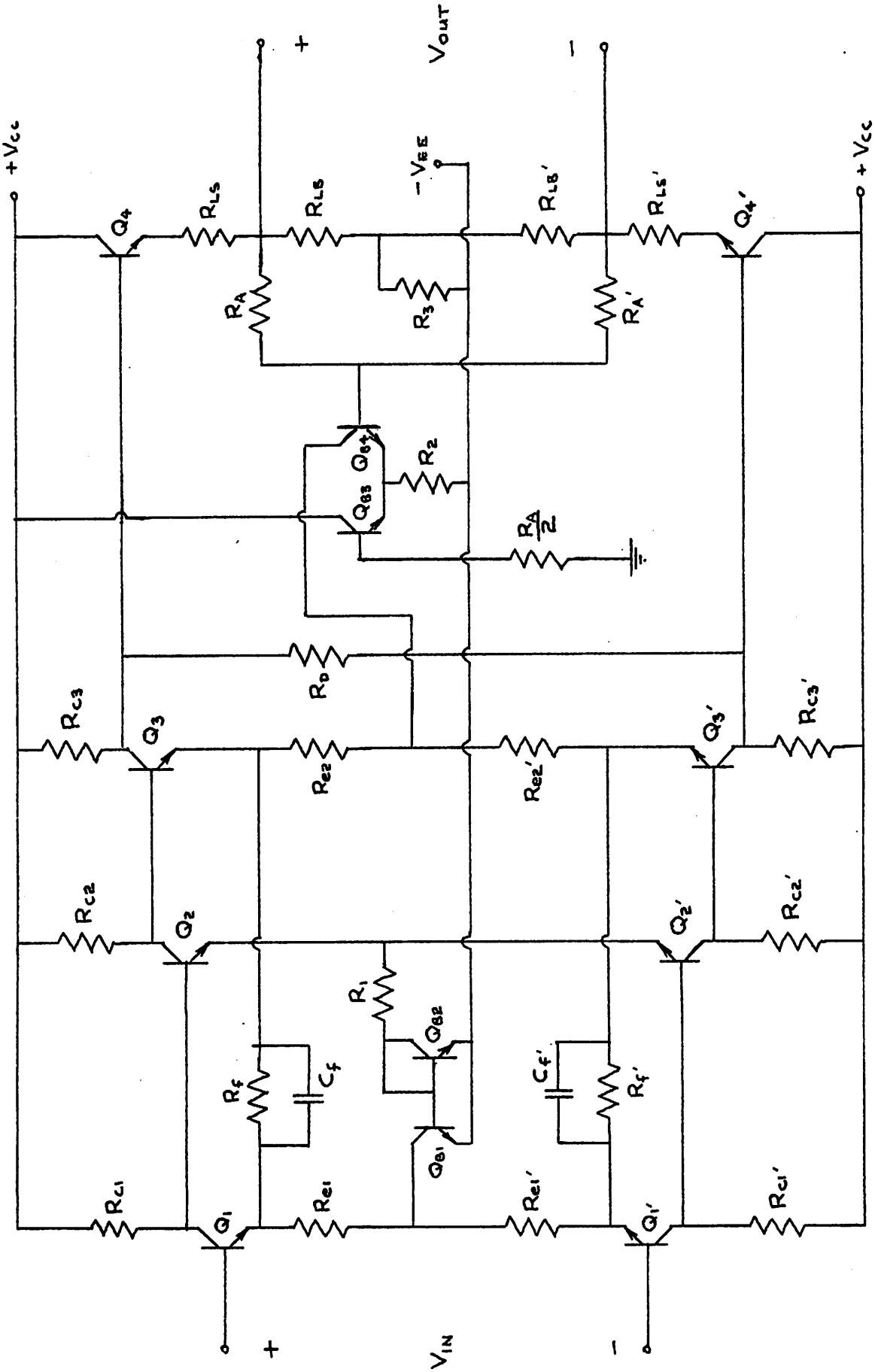


Fig. 25 Complete amplifier block configuration

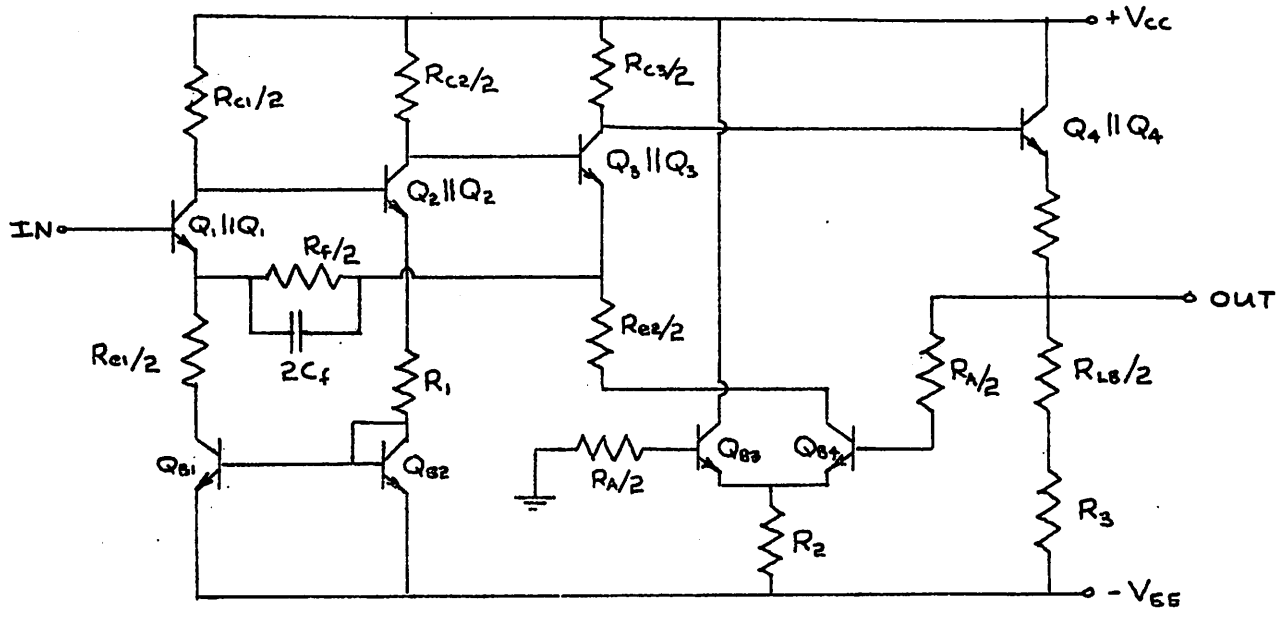


Fig. 26 Common-mode equivalent half-circuit for the block configuration of Fig. 25

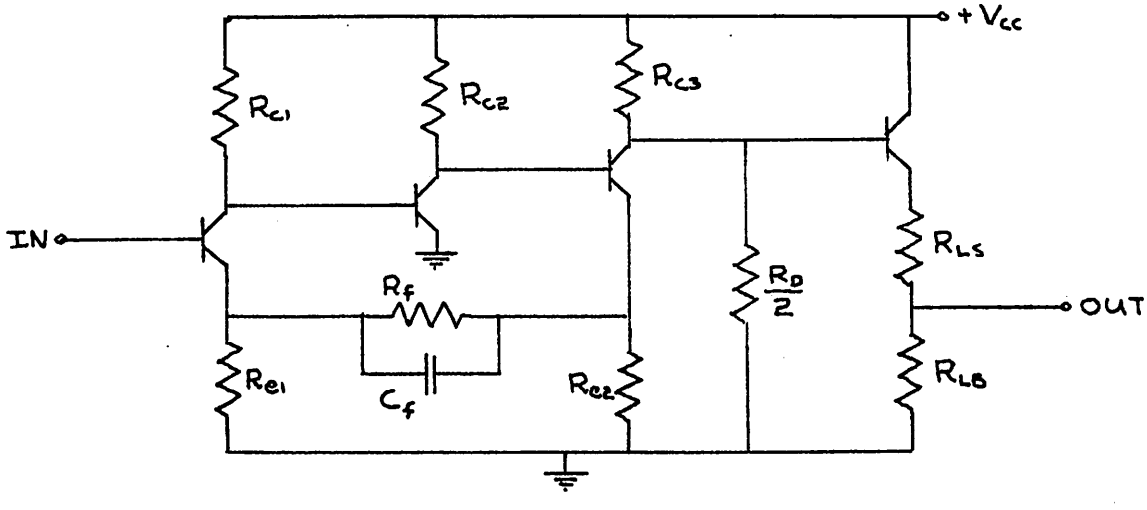


Fig. 27 Differential-mode equivalent half-circuit for the block configuration of Fig. 25

to that through which the output voltage level is sensed. Q_{B4} is used to supply part of the bias current for Q_3, thus completing the feedback loop. Consider the situation where the average output voltage rises above zero. This leads to an increase in the collector current of Q_{B4} and a corresponding increase in the collector current of Q_3. In turn, the base voltage of Q_4 is reduced. This voltage is tracked proportionally by the ouput dc voltage and hence, the increase in the output voltage is opposed.

To begin the numerical design, dc current and voltage levels are specified throughout the circuit. R_{C1}, R_{C2}, R_D, R_f, R_{C3}, R_3, R_{LS} and R_{LB} are then chosen to satisfy these levels. The emitter area of Q_{B1} relative to Q_{B2} is chosen to maintain the desired current levels in Q_1 and Q_3. R_2 is selected so that Q_{B4} draws the proper amount of current from Q_3. The sampling resistors R_A are kept as large as possible in order to minimize their attenuation effect on the ac output signal.

Values for R_{e1}, R_{e2}, C_f, and R_D are chosen using the differential mode half-circuit of Fig. 27. R_D is selected so that $R_D/2$ in parallel with R_{C3} provides the desired small-signal load for the triple. R_{e1} and R_{e2} are chosen to meet the low-frequency gain specification. Then, the open loop response of the triple is determined through a computer analysis and C_f is selected for proper shaping of the root loci.

Element values for the complete block design are listed in Table XIV. For any overall block gain specification, a somewhat higher gain is required for the triple alone to account for attenuation in the level shifting network. This attenuation is given by

$$A_{VL}(0) = \alpha_{04} \frac{R_{LB} R_A}{R_{LB} R_A + R_{LS}(R_{LB} + R_A)} \qquad (4.2)$$

Thus, the gain requirement for the triple is

$$A_V(0) = A_{VT}(0) / A_{VL}(0) \qquad (4.3)$$

where $A_{VT}(0)$ is the overall gain of the block. For the design at hand $A_{VL}(0) = 0.721$. Hence, for $A_{VT}(0) = 50$, it is required that $A_V(0) = 69.4$.

A value of 500 Ω is chosen for R_f so as to maintain a loop gain of at least 100 for the triple. The corresponding value for $R_{e1} = R_{e2}$ needed to obtain $A_V(0) = 69.4$ is 41 Ω. A differential load resistance, R_D, of 448 Ω is necessary to provide a net 200 Ω load for the triple.

The open loop response for the triple design is given in Table XV. In obtaining this response the loading effect of the level shifting network is represented by a load capacitance equal to C_μ (1 pF) of the emitter-follower. Based on the open loop response a number of values were considered for C_f. The maximum closed loop

$R_{e1} = 41\Omega$	$R_A = 20\ k\Omega$
$R_{e2} = 41\Omega$	$R_1 = 2.08\ k\Omega$
$R_f = 500\Omega$	$R_2 = 4.09\ k\Omega$
$R_{c1} = 8.3\ k\Omega$	$R_3 = 100\Omega$
$R_{c2} = 3.75\ k\Omega$	$R_D = 448\Omega$
$R_{c3} = 1.6\ k\Omega$	
$R_{LS} = 600\Omega$	$C_f = 8.0\ pF$
$R_{LB} = 1.8\ k\Omega$	

Table XIV Element values for the final design of the configuration in Fig. 25

$T_V(0)$	POLES (10^8 rad/sec)	ZEROS (10^8 rad/sec)
118	-.053 -1.5 -4.9 -19 -28 -34 -450 -503	-12.5 -33 -128 +70 +770

Table XV Open loop response for the series-series triple in the configuration of Fig. 25

bandwidth without peaking is obtained with C_f = 8 pF. For this case the bandwidth is 70 MHz.

III. Analysis of the Complete Block

The complete differential mode and common mode half-circuits for the block design corresponding to Table XIV have been analyzed. A computer-aided dc analysis of the common mode circuit, carried out using the program ECAP,[21] indicates that the desired dc voltage and current levels are obtained. The levels were found to be adequately insensitive to temperature over the full range of -55°C to +125°C.

The small-signal response of the common-mode circuit was examined to make sure that no instabilities arise as a result of the common-mode feedback loops. The response is found to be stable, exhibiting only left-half plane natural frequencies that are well away from the $j\omega$-axis.

The small-signal analysis results for the differential mode circuit are given in Table XVI. In establishing the temperature sensitivity of the response, the results of the common-mode dc analysis are used to take into account the variations in the collector currents of the transistors. The temperature dependence assumed for the

$A_{VT}(0)$	Deviation in $A_{VT}(0)$ −55°C	Deviation in $A_{VT}(0)$ +125°C	Poles (10^8 rad/sec)	Zeros (10^8 rad/sec)
49.4	-2.7%	+0.93%	$-1.54 \pm j\,3.90$	−18
			−2.89	−32
			−12.9	$-36 \pm j\,44$
Bandwidth	Deviation in Bandwidth −55°C	Deviation in Bandwidth +125°C	$-25 \pm j\,4.1$	+21
			−34	$+3.3 \pm j\,34$
70 MHz	+6%	−17%	−35	
			−80	
			−479	

Table XVI Small-signal response (differential-mode) of the final gain block design

device parameters is included in Table XIII.

From Table XVI it is seen that a low-frequency gain of 49.4 is obtained with the block, along with a bandwidth of 70 MHz. Over the full temperature range -55°C to +125°C, the gain exhibits a deviation of -0.24 dB to +0.09 dB (-2.7% to +0.93%).

SUMMARY

A building block approach has been presented as a flexible means of realizing a fully integrated wideband lowpass amplifier. On this basis a detailed study of a number of fundamental feedback configurations has been undertaken in order to select a configuration for use in realizing a basic building block. The study has shown the series-series feedback triple to be particularly suitable for desensitized wideband amplification in integrated circuits. A completely monolithic amplifying block, exhibiting zero volt dc levels at input and output, has been designed using the series-series triple.

From a general design standpoint it appears that superior broadband performance usually results when the signal amplification path is kept as "clean" as possible. The number of elements, particularly active devices, in this path, aside from the actual amplifying devices, should be kept to a minimum. This conclusion is based on the study of the composite device idea and on the consideration of various approaches to dc level shifting.

The use of composite devices in a feedback configuration is found to be unadvisable for wideband applications,

except under certain source and load conditions. For example, the ce-cb configuration, though providing a larger bandwidth than a single common-emitter stage, exhibits a second dominant pole relative to the common-emitter stage, except when the load resistance is kept small. The additional dominant pole is usually detrimental within a feedback loop.

The simple resistive level shift of Fig. 22(b) was found to be the most suitable for wideband applications, despite the gain attenuation associated with this network. Other approaches to level shifting were seen to introduce additional significant poles into the frequency response of the gain block.

The use of a differential, or balanced, amplifier configuration has been found to be well-suited to direct-coupled, integrated, wideband applications. By taking a differential approach the desired zero volt input and output dc levels can be achieved easily and the circuit elements needed to maintain dc stability can be kept out of the basic amplifying path. That is, the differential signal path can be kept as simple as possible.

A final comment on the analysis approach taken in this study is appropriate. Most of the conlusions reached herein have been arrived at through extensive computer-aided analysis. The size of this report is somewhat of an

indication of one of the disadvantages of such an approach. The effect is rather like that of a "shotgun" approach and in this sense is not fully satisfying. Yet, for the broad problem being considered no other precise method of attack is apparent. A number of the conclusions reached could not otherwise have been arrived at, except on an intuitive or approximate basis. The extensive use of computer-aided analysis, though somewhat tedious and lacking in elegance, is effective with regard to the general investigation of wideband lowpass amplification.

APPENDIX A: IDEAL FEEDBACK EQUATION REPRESENTATION

The technique of establishing an ideal feedback equation representation for a practical overall feedback amplifier configuration is given in several references.[15,18] As an example, the representation is established here for the shunt-shunt triple. The triple is shown in Fig. A.1. In Fig. A.2 a two port representation of a shunt-shunt feedback configuration is given. It is assumed that the two ports do not modify each other. For example, if the basic amplifier has a common ground, so does the feedback network.

For the configuration of Fig. A.2 the output voltage is related to the source current by

$$\frac{v_L}{i_s} = \frac{-y_{21}^T}{y_{11}^T y_{22}^T - y_{21}^T y_{12}^T} \qquad (A.1)$$

where $y_{ij}^T = y_{ij}^a + y_{ij}^f$. Note that R_s and R_L are included in the basic amplifier parameters y_{11}^a and y_{22}^a.

The overall current gain for the shunt-shunt configuration can be expressed as

$$A_I = \frac{i_L}{i_s} = \frac{v_L/R_L}{i_s} = \frac{\dfrac{-y_{21}^T/R_L}{y_{11}^T y_{22}^T}}{1 - \left(-\dfrac{y_{21}^T/R_L}{y_{11}^T y_{22}^T}\right)\left(-y_{21}^T R_L\right)} \qquad (A.2)$$

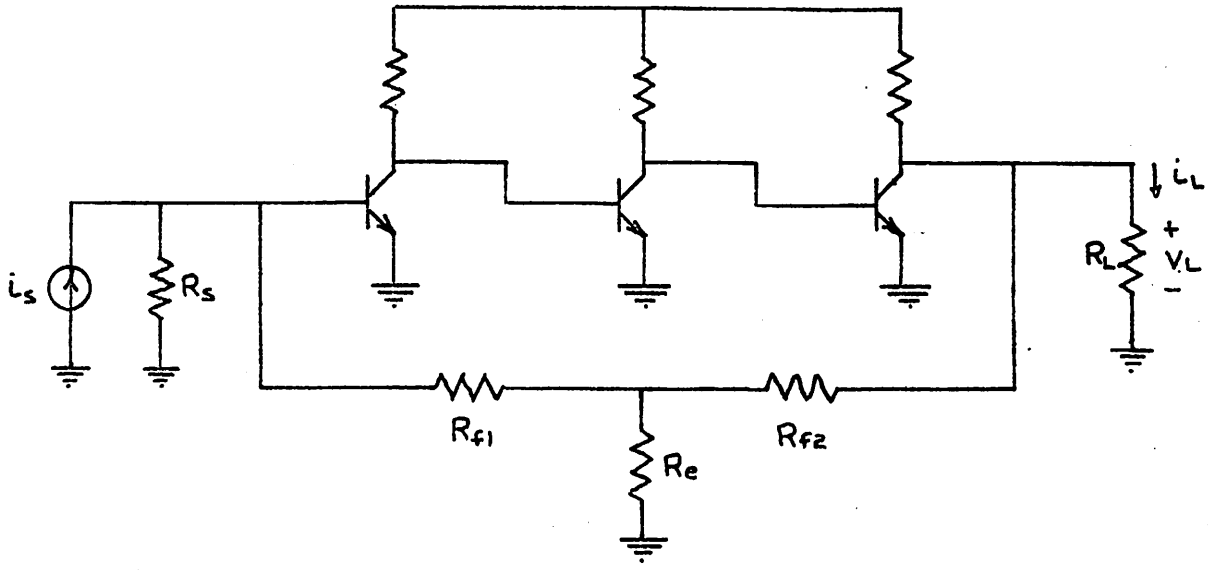


Fig. A.1 The shunt-shunt feedback triple

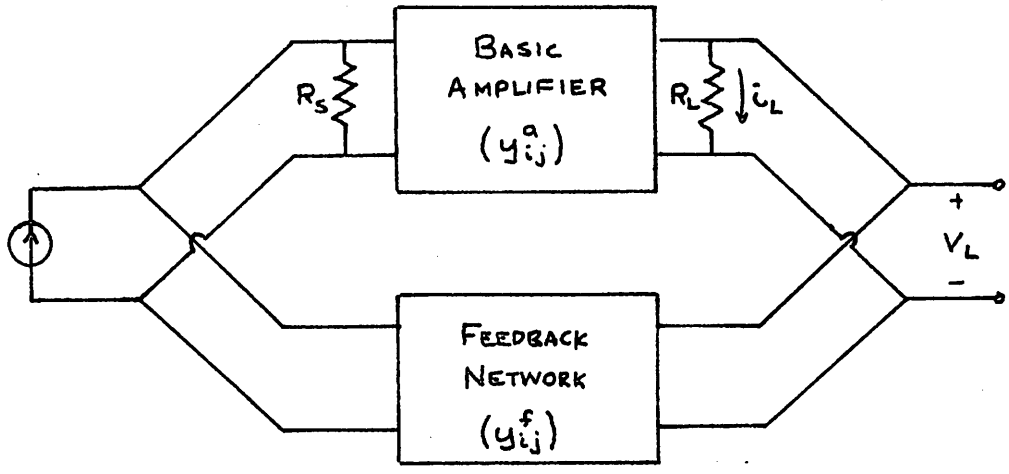


Fig. A.2 Two port representation of a shunt-shunt feedback configuration

To establish the form of the ideal feedback equation two approximations are necessary in equation (A.2). First, it must be assumed that $y_{12}^a \ll y_{12}^f$. That is, the reverse transmission through the basic amplifier is negligible compared to that through the feedback network. Under this assumption

$$y_{12}^T \simeq y_{12}^f \tag{A.3}$$

The second approximation required is that the forward transmission of the feedback network be much less than that of the basic amplifier ($y_{21}^a \gg y_{21}^f$). In such a case

$$y_{21}^T \simeq y_{21}^a \tag{A.4}$$

When the approximations represented by equations (A.3) and (A.4) hold, the overall current gain expression takes the form

$$A = \frac{a_I}{1 - a_I f_I} \tag{A.5}$$

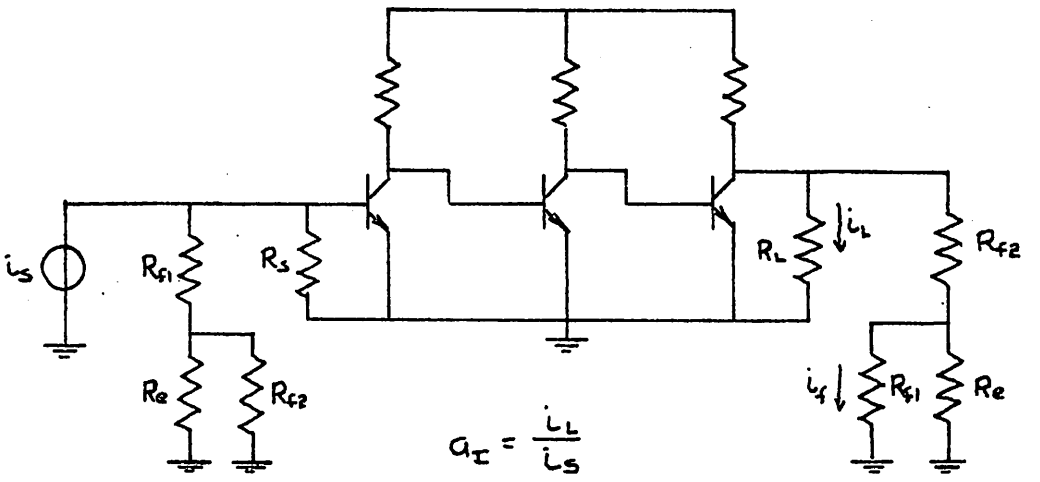
where

$$a_I = \frac{-y_{21}^a / R_L}{y_{11}^T \, y_{22}^T} \tag{A.6}$$

$$f_I = -y_{12}^f R_L \tag{A.7}$$

The expression for the forward transmission, a_I, is simply the current gain of the basic amplifier with the loading of y_{11}^f and y_{22}^f included. f_I is the reverse transmission of the feedback network.

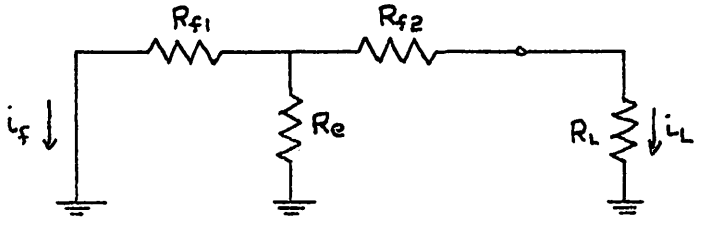
Appropriate circuits for determing a_I and f_I for the shunt-shunt triple are given in Fig. A.3. The circuit of Fig. A.3(a) is also suitable for determining the loop gain, $T_I = -a_I f_I$.



$$a_I = \frac{i_L}{i_s}$$

$$T_I = \frac{-i_f}{i_s}$$

(a)



$$f_I = \frac{i_f}{i_L}$$

(b)

Fig. A.3 Circuits for determining a_I, f_I, and T_I for the shunt-shunt triple

APPENDIX B: OPTIMIZATION OF FEEDBACK ELEMENT VALUES

The series-shunt pair (Fig. 1(a)), the shunt-series pair (Fig. 1(c)) and the emitter-coupled pair configuration of Fig. 5 all exhibit the same form of expressions for the forward and feedback transmission functions.

$$a(0) = K_1 \left(\frac{R_e + R_f}{R_e + R_f + K_2} \right) \left(\frac{R_e + R_f}{R_e R_f + K_3 (R_e + R_f)} \right)$$

and

$$f(0) = K_4 \frac{R_e}{R_e + R_f} \qquad (B.1)$$

where K_1, K_2, K_3, and K_4 are constants. From the feedback expression, the feedback elements are seen to be constrained in a linear manner for a given specification of f(0).

$$R_f = C R_e \quad , \quad C \text{ a constant} \qquad (B.2)$$

It is desired to maximize a(0) under the constraint (B.2). This is a straigntforward task consisting merely of subsituting (B.2) in the expression for a(0) and setting the derivative of tne resulting expression, with respect to R_e, equal to zero. Solving for R_e leads to

$$R_e = \left[K_2 K_3 / C \right]^{1/2} \qquad (B.3)$$

and hence

$$R_f = C R_e = \left[K_2 K_3 C \right]^{1/2} \qquad (B.4)$$

In a practical design situation an iterative procedure is used to establish the optimum values for R_e and R_f. First, an estimate of a(0) is made and used to determine the needed f(0) for a given A(0). Using the value obtained for f(0), R_e and R_f are determined from equations (B.3) and (B.4). These values can then be used to determine a(0) and the procedure is repeated. The processes usually converges in two or three cycles.

APPENDIX C: OUTPUT FEEDBACK ZERO

In Chapter 2 a feedback zero is found to be associated with the output collector in configurations with a series feedback connection at the output. The zero is located at

$$z_o = -\frac{1}{R_L C_o} \qquad (C.1)$$

where $C_o = C_\mu + C_p + C_L$.

That equation (C.1) does represent the exact location of the zero can be seen by considering the circuit of Fig. C.1. For the nodes as labeled in the figure, a nodal analysis leads to

$$\begin{pmatrix} \frac{1}{r_\pi} + p(C_\pi + C_\mu) & -pC_\mu & -(\frac{1}{r_\pi} + pC_\pi) \\ g_m - pC_\mu & \frac{1}{R_L} + p(C_\mu + C_p + C_L) & -g_m \\ -(g_m + \frac{1}{r_\pi} + pC_\pi) & 0 & g_m + \frac{1}{R_e} + \frac{1}{r_\pi} + pC_\pi \end{pmatrix} \begin{pmatrix} V_A \\ V_B \\ V_C \end{pmatrix} = \begin{pmatrix} i_s \\ 0 \\ 0 \end{pmatrix} \qquad (C.2)$$

The zeros of the relationship between i_e and i_L are simply the zeros of Δ_{cc}, the cofactor corresponding to the solution of (C.2) for V_C $(=i_e/R_e)$.

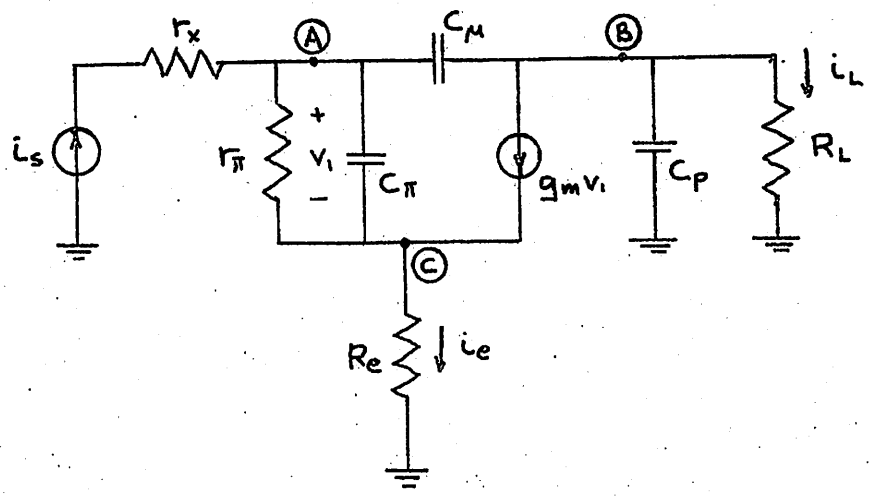


Fig. C.1 Small-signal equivalent circuit for a configuration with series feedback

$$\Delta_c(p) = -i_s\left(g_m + \frac{1}{r_\pi} + pC_\pi\right)\left(\frac{1}{R_L} + p(C_\mu + C_p + C_L)\right) \qquad (C.3)$$

Thus, the zeros of $i_e(p)/i_L(p)$ are located at

$$z_0 = -1/R_L(C_\mu + C_p + C_L)$$

$$z_1 = -\frac{1}{C_\pi}\left(g_m + \frac{1}{r_\pi}\right) \simeq -\frac{g_m}{C_\pi} \qquad (C.4)$$

$|z_1|$ is of the order of ω_t and may be neglected in most situations. z_0 is located as indicated in equation (C.1)

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