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COMPUTER EVALUATION OF MODERN OPERATIONAL AMPLIFIERS

by

Sing-Yui James Wong

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Electronics Research Laboratory

College of Engineering  
University of California, Berkeley  
94720

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Abstract

Small-signal performance of the input stage of the LM 101 and large-signal performance of the output stages of the LM 101 and the 741 have been examined extensively by Schwartz and Patel respectively in their M.S. reports. In this report performance of the ICL 8741 and the ULX 2139 are evaluated and compared. Emphasis is given on comparison between the two circuits along with detailed analysis. Extensive experimental work has been done on device characterization to provide sufficient and more realistic device data for both circuits for computer simulation analyses. Full circuits are used for small-signal computer aided analysis because program Rohrer X is available which allows larger and more flexible circuit configuration.

## Chapter I

### Introduction

A number of problems which prevailed in the early-version operational amplifier such as the 709, namely lack of proper short-circuit protection, difficulty in frequency stabilization, latch-up and lack of satisfactory offset voltage null method, have been obviated in the new amplifiers such as the ICL 8741 and the ULX 2139<sup>1</sup>(1). The complete schematics and the photomicrographs of both amplifiers are shown in Fig.1.1 and Fig.1.2 respectively. The complexity of the circuit is due to the facts that total circuit resistance has to be minimized, that the poor gain characteristic of some transistors has to be made up, and that power consumption has to be reduced. Active loads are employed by both amplifiers in the input stage to increase gain and reduce input bias current, resulting in increased input resistance, to increase output swing, to increase common-mode range and to permit the amplifier to operate over a wider range of supply voltage.

The purpose of this report is to establish acceptable models for the op-amps considered and undertake a detailed evaluation of the ICL 8741 and the ULX 2139 by means of extensive experimental characterization and recently available computer-aided analysis programs: Bias III, Pottle, Rohrer X

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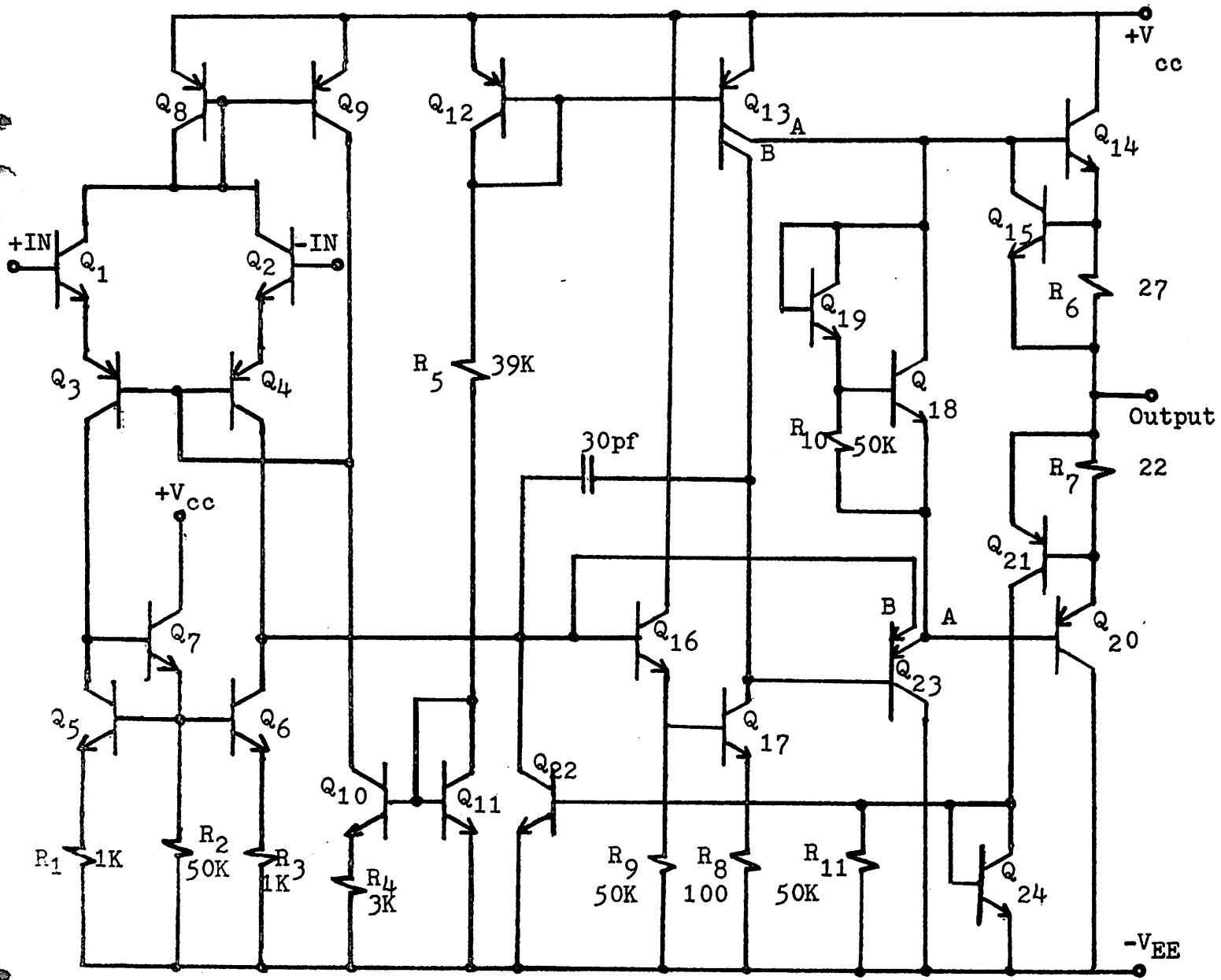
<sup>1</sup> ICL 8741 is produced by Intersil Inc., equivalent to Fairchild's  $\mu$ A 741. The ULX 2139 is produced by Sprague Electric Co., and is equivalent to Motorola's MC 1539.

and Time<sup>2</sup>.

Chapter II of this report is a circuit description of both amplifiers, Chapter III is concerned with device characterization in which various techniques in acquiring the data are reported, followed by dc, small-signal and large-signal analyses of the amplifiers in Chapter IV. The techniques used in frequency compensation are considered and evaluated and the frequency limitation of these devices when driven by a step function or a large, high-frequency sine wave is examined in Chapter IV.

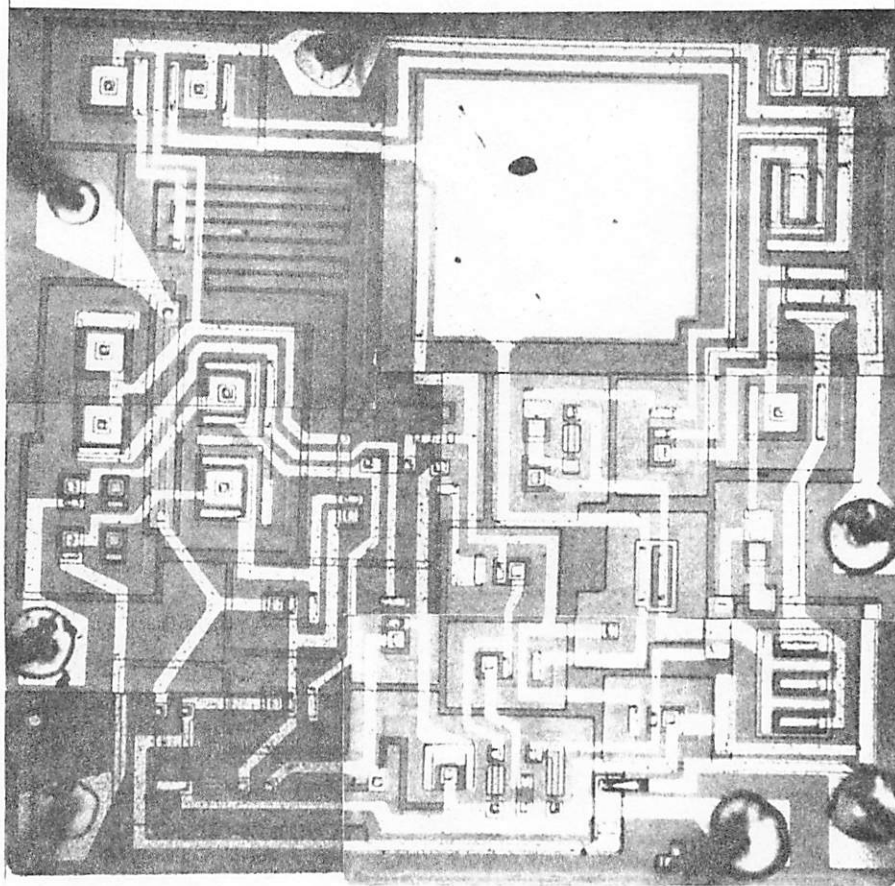
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<sup>2</sup>Rohrer X is an earlier version of Cancer. The author has private communication with Mr. Sui-Ping Fan and Mr. Nagel on Time and Rohrer X.

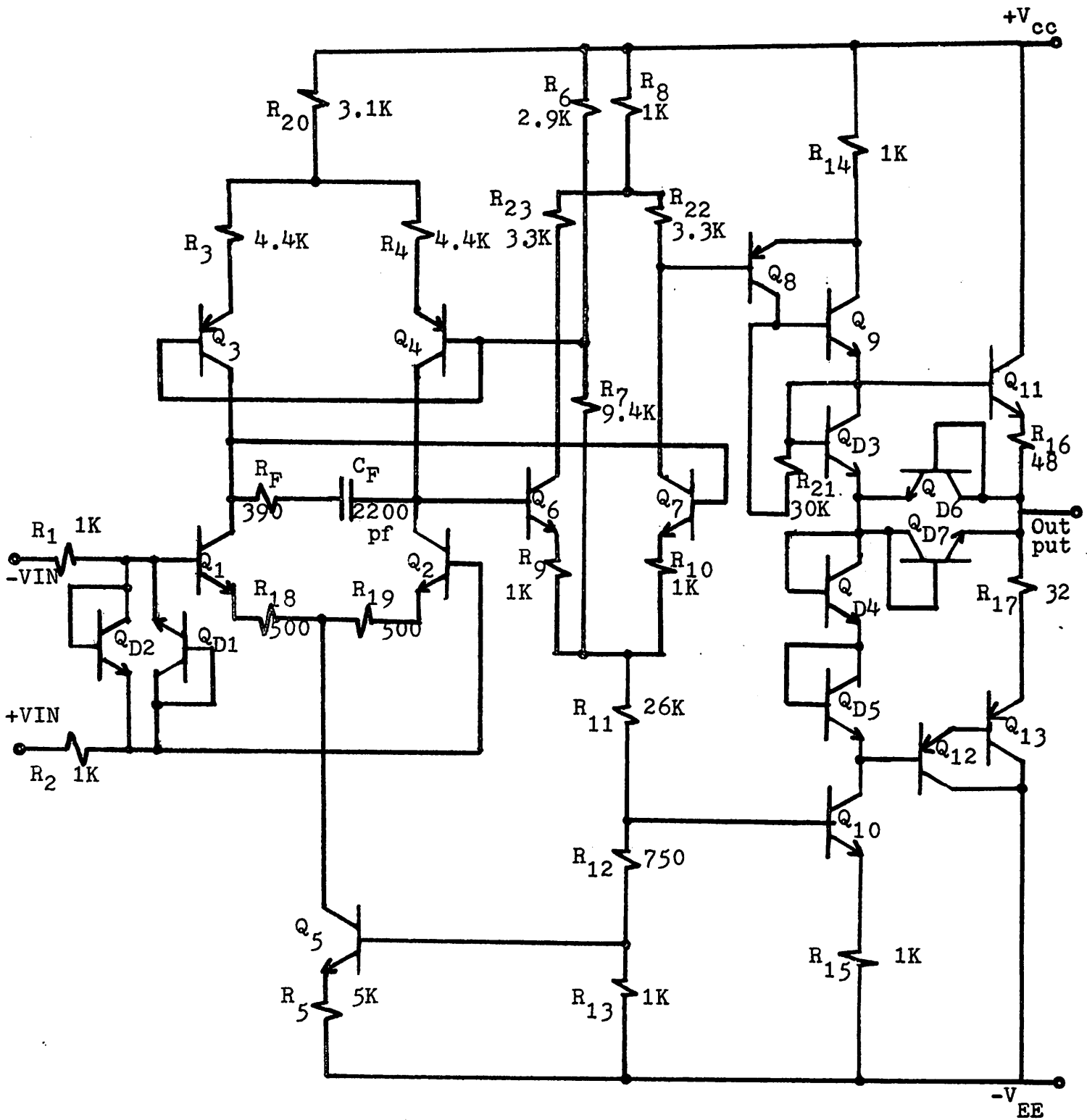


(a) Schematic of 741

Fig. 1.1 Schematic and photomicrograph of the 741

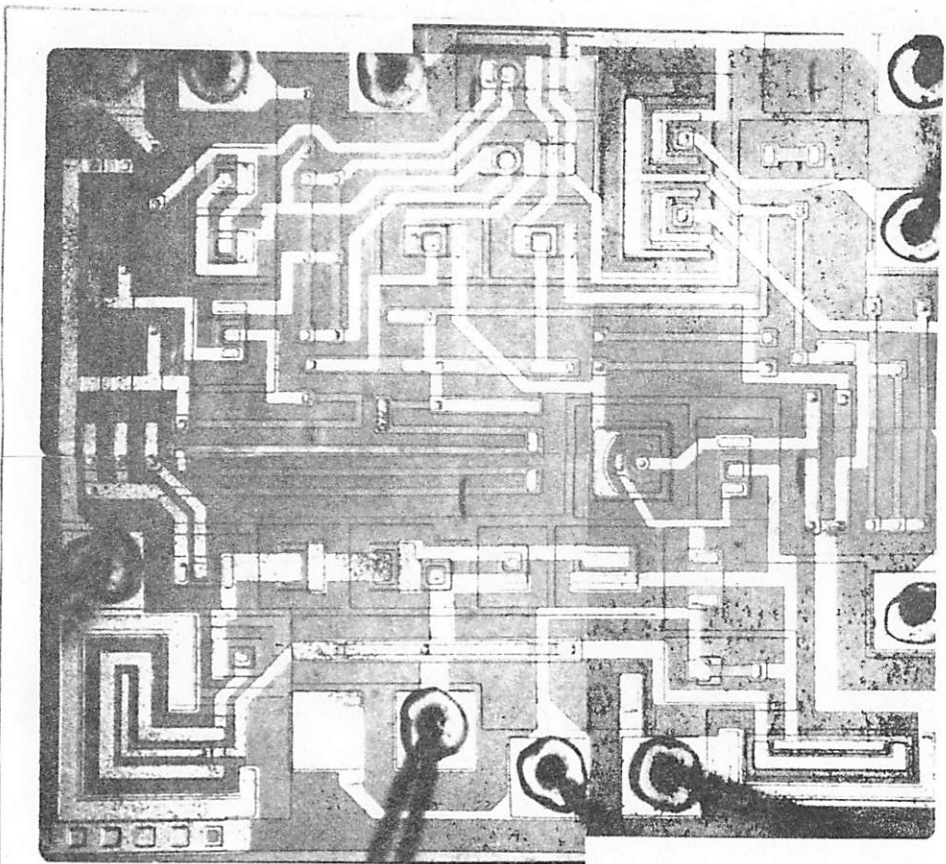


(b) Photomicrograph of the 741  
Fig. 1.1 Continued



(a) Schematic of ULX 2139

Fig. 1.2 Schematic and photomicrograph of the ULX 2139



(b) Photomicrograph of ULX 3129

Fig. 1.2 Continued

## Chapter II

### Circuit Description

#### 2.1 The 741

The complete schematic of the 741 is given in Fig.1.1a. It is a three-stage amplifier comprising a high gain, differential-input, single-ended-output input stage with double-to-single ended gain conversion, an intermediate stage with a Darlington pair and a complementary class AB output stage that is short-circuit protected.

#### Input Stage

The quiescent current of the input stage is established by diode biasing of  $Q_{10}$ . Transistors  $Q_5$ ,  $Q_6$  and  $Q_7$  provide the active load for the input composite (npn-pnp) device,  $Q_1$  and  $Q_3$ , and also act as balance-to-unbalance conversion circuit, providing full differential gain at the collector of  $Q_6$ . The potential at the emitter of  $Q_7$  is a constant for a given voltage supply and thus the quiescent operating current of  $Q_7$  is established by the bias resistor,  $R_2$ . Since the current in  $Q_7$  is not critical to the stage pinch resistor is used to save chip area. A brief picture of a pinch resistor and transistors, npn and lateral pnp, in the chip is shown in Fig.2.1.

#### Second Stage

A Darlington compound transistor which consists of  $Q_{16}$  and  $Q_{17}$  is used in the second stage. This avoids loading the first stage. Again because of large bias resistor  $R_9$ , the collector current of  $Q_{16}$  is comparable with that of the



input device. The Darlington configuration achieves high gain and high impedance level at the collector of  $Q_{17}$  and thus Miller-effect capacitor is able to be used for frequency compensation. Compensation through unity gain is made possible with a 30 pf MOS capacitor<sup>3</sup> across the base of  $Q_{16}$  and the collector of  $Q_{17}$ .

### Output Stage

The output stage is a complementary class AB stage with very high input impedance. Since the voltage drop between the base of  $Q_{14}$  and the base of  $Q_{20}$  is two diode drops contributed by  $Q_{18}$  and  $Q_{19}$ , the collector current of  $Q_{14}$  is kept low, typically 300  $\mu$ A. Transistors  $Q_{14}$  and  $Q_{20}$  are both kept active and thus the dead zone associated with the conventional class-B output stage is eliminated. Transistors  $Q_{15}$  and  $Q_{21}$  are part of the short-circuit protection. When large enough voltage develops across  $R_6$ ,  $Q_{15}$  conducts and rids  $Q_{14}$  of excessive base drive and thus short-circuit protection is achieved during the positive cycle. Transistor  $Q_{21}$  conducts in the same manner when negative overdrive occurs. This chain-action turns on transistor  $Q_{22}$ . The conducting  $Q_{22}$  then rids  $Q_{16}$  of base current and thus protects  $Q_{20}$  from overload. Transistor  $Q_{23}$  is a double-emitter transistor with emitter B inactive during normal operation and emitter A acting as an emitter follower. Transistor  $Q_{23B}$  prevents  $Q_{16}$  from saturating. When  $Q_{16}$  is saturated,  $Q_{17}$  is also saturated,

<sup>3</sup>David Fullagar, "A New High Performance Monolithic Op-Amp", Fairchild Semiconductor technical publication, 1968.

and the base of  $Q_{23B}$  will have the same potential as the base of  $Q_{17}$ . The emitter-base voltage of  $Q_{23B}$  will be the same as that of  $Q_{16}$  and thus  $Q_{23B}$  is in active mode. The effect of overload is thus avoided through the shunt feedback provided by the active emitter-base junction of  $Q_{23B}$ . Thus protection of Darlington pair is achieved.

## 2.2 ULX 2139

The complete schematic of the ULX 2139 is given in Fig.1.2a. It is basically a three-stage amplifier comprising a high gain, differential-input, differential-output input stage, a low gain, differential-input, single-ended-output second stage and a high gain, complementary class AB output stage. Both the input stage and the output stage are short-circuit protected. The elevated dc level due to the presence of the collector junction of transistor  $Q_7$  is shifted down by the composite pnp-npn device which consists of  $Q_8$  and  $Q_9$  to achieve zero quiescent output voltage. The composite device has the polarity of a pnp and the effective current gain of an npn transistor.

As is brought out later in Chapter III the small-signal current gain of the substrate devices used in the ULX 2139 is inferior to those fabricated by Intersil, used in the 741. The Darlington device has to be employed to aid the symmetry of current gain for the output stage and avoid unnecessary distortion. Short-circuit protection is provided by  $D_6$  and  $D_7$  which conduct current to or from the load when sufficient voltages are developed across  $R_{16}$  and  $R_{17}$ .

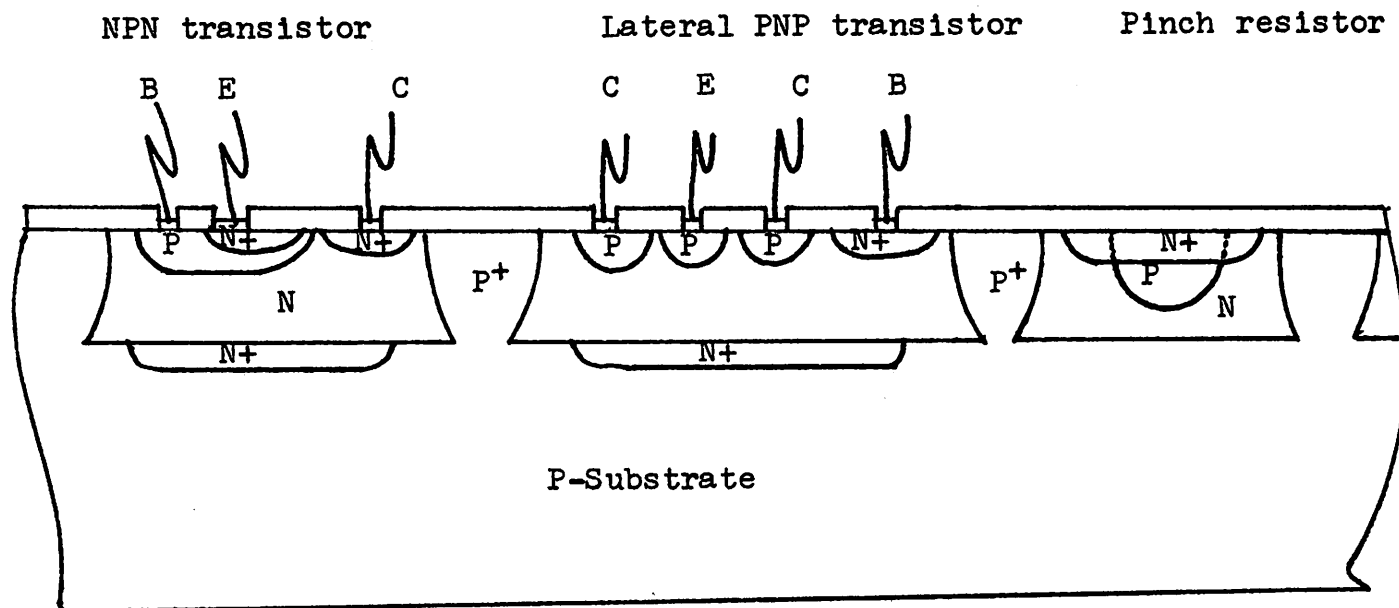


Fig. 2.1 Cross Sectional View of Integrated Components

## Chapter III

Device Characterization

For integrated bipolar transistor the modified hybrid  $\pi$  model is used for small signal analysis. The model parameters of each type of transistor used in the 741 and the ULX 2139 have to be measured. There are basically four types of devices used in the 741, namely the small npn, the small lateral pnp, the large npn and the large substrate pnp. In addition to the above four types of devices, the round npn and the round lateral pnp are also used in the ULX 2139.

The manufacturers<sup>4</sup> have supplied us with sufficient complete circuits and devices for both op-amps. The devices are isolated transistors which are identical to those used in the amplifiers. This is made possible by changing the aluminum metallization pattern such that special pads are connected to the devices for easy access to gold bonding.

Experiental Results and Discussion3.1 Characterization and measurement of base resistance  $r_x$ 

The presence of  $r_x$  in bipolar transistors is manifested by the effect of input impedance at high frequency. It is well established that base resistance decreases at high quiescent current due to dc crowding and high level injection (2). Measurement of  $r_x$  over a useful range of operating current

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<sup>4</sup> 741 circuits and devices have been supplied by Intersil Inc., Cupertino, Calif., ULX 2139 by Sprague Elec. Co., Worcester, Mass.

are made to show the decreasing trend of  $r_x$ .

Complex-impedance method<sup>5</sup> is employed to measure  $r_x$ . Measurement of input impedance of devices made on a Wayne-Kerr Bridge<sup>6</sup> is accomplished by a special test jig in which lead inductance has been minimized to avoid erroneous results at high frequency. The measured and calculated results fit nicely into the circle up to 20 M hz as shown in Fig.3.1, Fig.3.1 and Fig.3.3. The point the curve crosses the real axis at infinite frequency is a good measure of  $r_x$ .

The measured base resistance is plotted as a function of collector current in Fig.3.4. At current level below 1 mA, the small devices have much larger base resistance than the large devices. Both the large npn and the large substrate pnp have strip emitters as is shown in the photomicrographs in Appendix D. There are two strip base contacts very close to the longer sides of the emitter. This design reduces extrinsic base resistance a great deal<sup>7</sup>. The decrease in base resistance for small devices reflects that high level injection occurs at around 200  $\mu$ A. This is consistent with the fact, which will be brought out later in the chapter, that the unity gain frequency of small devices also falls off at around 200  $\mu$ A due to high level injection. Large devices,

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<sup>5</sup>Detailed explanation and illustration are given in Appendix B.

<sup>6</sup>Wayne-Kerr V.H.F. Admittance Bridge B801 for frequency higher than 5M hz.

<sup>7</sup>S.K. Gandhi, "The Theory and Practice of Micro-electronics", John Wiley & Sons, 1968.

with emitters at least three times as large as those of small devices, are more likely to reach high level injection at a higher current level. This is manifested by the range of current levels in which the base resistance of large devices remains unchanged.

The total base resistance of the large and small npn devices found in the ULX 2139 is much larger than those found in the 741 over the useful range of current levels. This might indicate that the resistivity of the base of the transistors made at Intersil is lower with different diffusion techniques.

### 3.2 Measurement of junction capacitance and substrate capacitance

The junction capacitance associated with the depletion layer is measured as a function of reverse bias voltage. A test jig has been built for measurement to reduce parasitics. The Direct Capacitance Bridge, Model 75C, Boonton Electronic Corporation, is employed to make the measurement. The procedure of the measurement of an npn transistor is outlined below to illustrate the method.

The junction capacitance associated with the transistor and the parasitic capacitance that cannot be neglected are shown in Fig. 3.6b. To measure the emitter junction capacitance the base-collector and collector-substrate junctions must be shorted in order to rid the parasitic capacitance,  $C_{pin}$ , which exists between the pin and the header as shown in Fig. 3.6a. However, the measured capacitance between the emitter and the base still includes one pin capacitance which has to be

accounted for in the  $C_{je}$  calculation. To measure  $C_{pin}$  one pin is shorted to the header. Measurement is then made between the shorted pin and another chosen pin. The average of several pin capacitances (0.7 pf) has been used for calculation. It follows from Fig.3.6b that

$$C_{je} = C_{BE} \text{ (measured)} - C_{pin}$$

Other junction capacitances have been found in an analogous manner. By shoring the appropriate terminals, the following relation is obtained for collector-base junction and collector-substrate junction capacitances.

$$C_{jc} = C_{BC} \text{ (measured)} - 2 C_{pin}$$

$$C_{cs} = C_{CS} \text{ (measured)} - 3 C_{pin}$$

The following have been obtained and plotted in Appendix B and Appendix C,  $C_{je}$  vs.  $V_{BE}$ ,  $C_{jc}$  vs.  $V_{cs}$  and  $C_{Bs}$  vs.  $V_{Bs}$  for lateral pnp transistors.

### 3.3 Collector Saturation Resistance

Photographs have been taken in saturation region for each device. From Grove (3),

$$V_{CE} = \pm \left[ \frac{kT}{q} \left| \ln \frac{\alpha_R (1 - I_c/I_B \beta_o)}{1 + I_c (1 - \alpha_R)/I_B} \right| + |I_E r_e| + |I_c r_c| \right] \quad (3.1)$$

Since  $r_c \gg r_e$

$$V_{CE} = \pm \left[ \frac{kT}{q} \left| \ln \frac{\alpha_R (1 - I_c/I_B \beta_o)}{1 + I_c (1 - \alpha_R)/I_B} \right| + |I_c r_c| \right] \quad (3.2)$$

Two points are taken,  $I_{c1}$  (at  $I_{B1}$ ) and  $I_{c2}$  (at  $I_{B2}$ ) such that  $I_{c1}/I_{B1} = I_{c2}/I_{B2} \ll \beta_o$  to guarantee saturation, then (3.3)

$$V_{CE1} = \frac{kT}{q} \left| \ln \frac{\alpha_R (1 - I_{c1}/I_{B1} \beta_o)}{1 + I_{c1} (1 - \alpha_R)/I_{B1}} \right| + I_{c1} r_c \quad (3.4)$$

$$V_{CE2} = \frac{kT}{q} \left| \ln \frac{\alpha_R (1 - I_{c2}/I_{B2} \beta_o)}{1 + I_{c2} (1 - \alpha_R)/I_{B2}} \right| + I_{c2} r_c \quad (3.5)$$

The following is obtained by combining equations (3.3), (3.4) and (3.5)

$$V_{CE2} - V_{CE1} = (I_{c1} - I_{c2}) r_c$$

$$r_c = \frac{V_{CE1} - V_{CE2}}{I_{c1} - I_{c2}}$$

Since  $V_{CE2}$ ,  $V_{CE1}$ ,  $I_{c2}$  and  $I_{c1}$  can be properly chosen to satisfy equation (3.3), with the aid of Fig.3.7,  $r_c$  can be readily calculated. For example, point 1 is chosen in the I-V curves in Fig.3.7 such that  $I_{c1} = 20I_{B1} = 100 \mu A$ , at where  $\beta_o$  is 200 as is brought out later in the chapter, In an analogous manner point 2 is chosen such that  $I_{c2}$  is  $200 \mu A$ .

$$r_c = \frac{200\text{mv} - 180\text{mv}}{200\mu A - 100\mu A} = 200 \text{ ohms}$$

The collector saturation resistance is then calculated for



each device and tabulated in Table 3.2. It is noted that the collector series resistance of the large npn is very low in comparison with that of other devices. This is consistent with the fact that large npn's have larger emitter area.

### 3.4 Measurement of other small signal parameters

Small-signal, low frequency current gain,  $\beta_o$ , can be readily obtained as a function of quiescent current by means of a single stage amplifier setup with which current gain of the transistors is measured at a frequency of 30 kHz. The results of measurements are presented later in Appendix B and C. The emitter junction reverse saturation current,  $I_{ES}$ , the output resistance,  $r_o$ , and the reverse current gain of the transistors,  $B_R$ , are measured and calculated with the aid of a curve tracer. The results of measurements are tabulated in Table 3.2.

The unity gain frequency,  $f_T$ , of the npn transistors is measured from  $f_t$  meter assuming frequency roll-off of 20 dB per decade (4). The  $f_T$  of the pnp transistors, however, has to be measured with the current-gain-vs-frequency method because of the existing uncertainty over whether the lateral pnp devices can be modelled with a single pole response transfer function<sup>8</sup>. A typical curve as shown in Fig.3.8 is obtained from experimental measurements. The measured current

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<sup>8</sup>J. Lindmayer and W. Schneider, "Theory of Lateral Transistors", Solid State Electronic, Pergamon Press 1967. Vol.10, pp225-234, Printed in Great Britain.

gain data points at some frequency beyond the break frequency of the transistors are projected down to the unity gain point and thus the unity gain frequency of the pnp transistors is obtained. The frequency roll-off of the lateral pnp devices used in this report is found experimentally to be 20 dB per decade. The distributed effect in the base of the lateral devices appears not to be large enough to affect the assumed modified hybrid  $\pi$  model. Using this method the unity gain frequency measurements are presented in Appendix B and C. For the sake of contrast, a plot of  $\beta_o$  and  $f_T$  versus frequency is shown in Fig.3.9 for the lateral transistors and other devices in both the 741 and the ULX 2139. The current dependence of  $f_T$  is somewhat greater for the lateral transistors than for the npn transistors. The peak of  $f_T$  is observed to occur at about 200  $\mu$ A for the lateral devices. The operating point for maximum  $f_T$  is nearly coincident with the maxima of the  $\beta_o$  versus  $I_c$ , as shown in Fig.3.9. The lateral devices found in the 741 are superior to those found in the ULX 2139 in current gain. However, The unity gain frequency of the lateral devices in both amplifiers has not been improved due to the minimum base width that can be controlled by modern diffusion techniques.

### 3.5 Transit Time

The transit time, one of the parameters needed for large-signal model of the devices, can be obtained as following: (4)

$$\frac{1}{2 \pi f_T} = \frac{kT}{qI_c} (C_{je} + C_{jc}) + \tau_N + \dots$$

$$\tau_N = \frac{1}{2 \pi f_T} - \frac{kT}{qI_c} (C_{je} + C_{jc})$$

Good estimate of  $\tau_N$  can be obtained at current level  $I_c$

such that  $\frac{1}{2 \pi f_T} \gg \frac{kT}{qI_c} (C_{je} + C_{jc})$

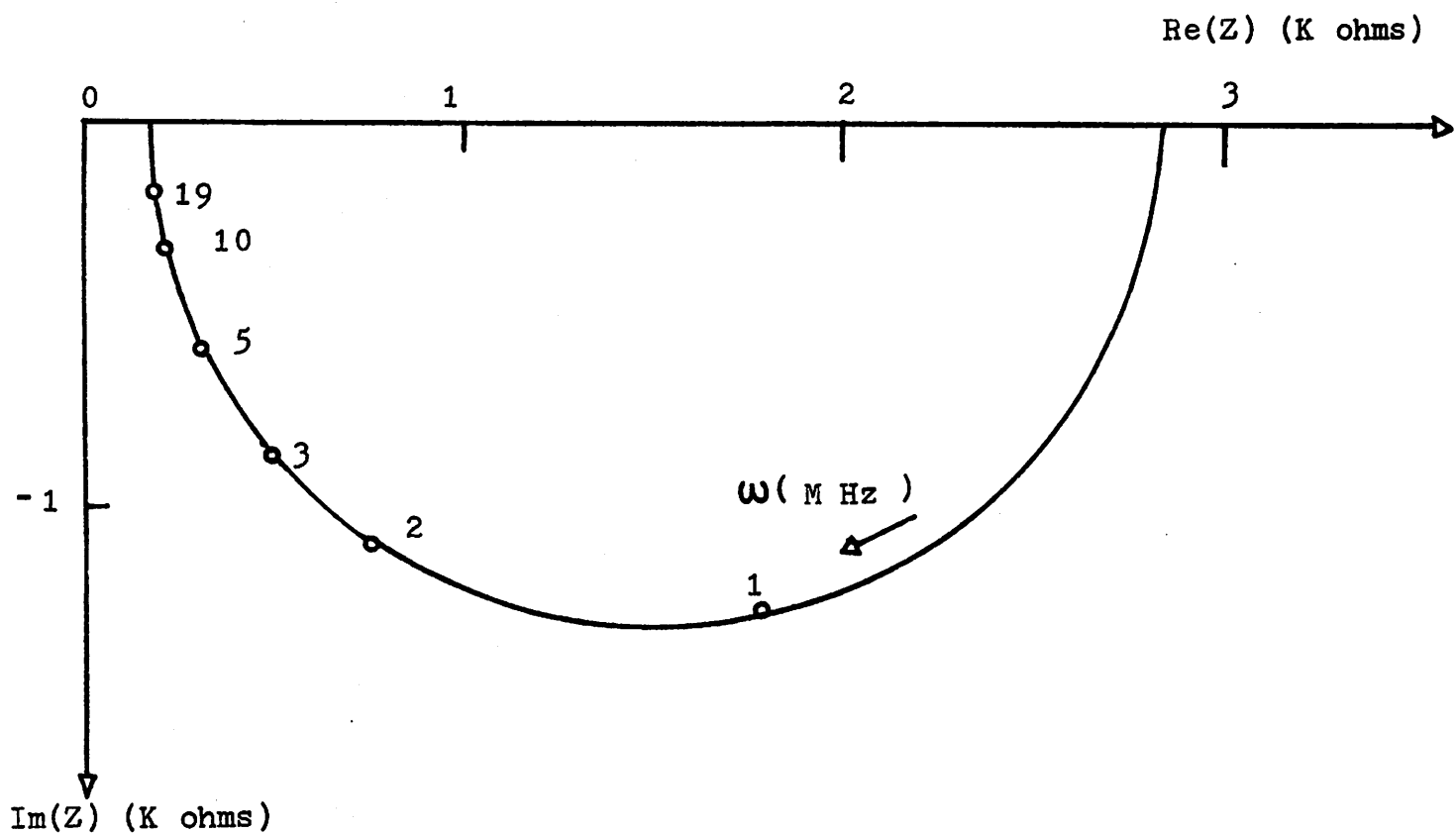


Fig. 3.1 Complex input impedance  
 Small Npn of 741  
 $I_c = 2.0 \text{ ma}$  , Base resistance  $r_x = 180 \Omega$

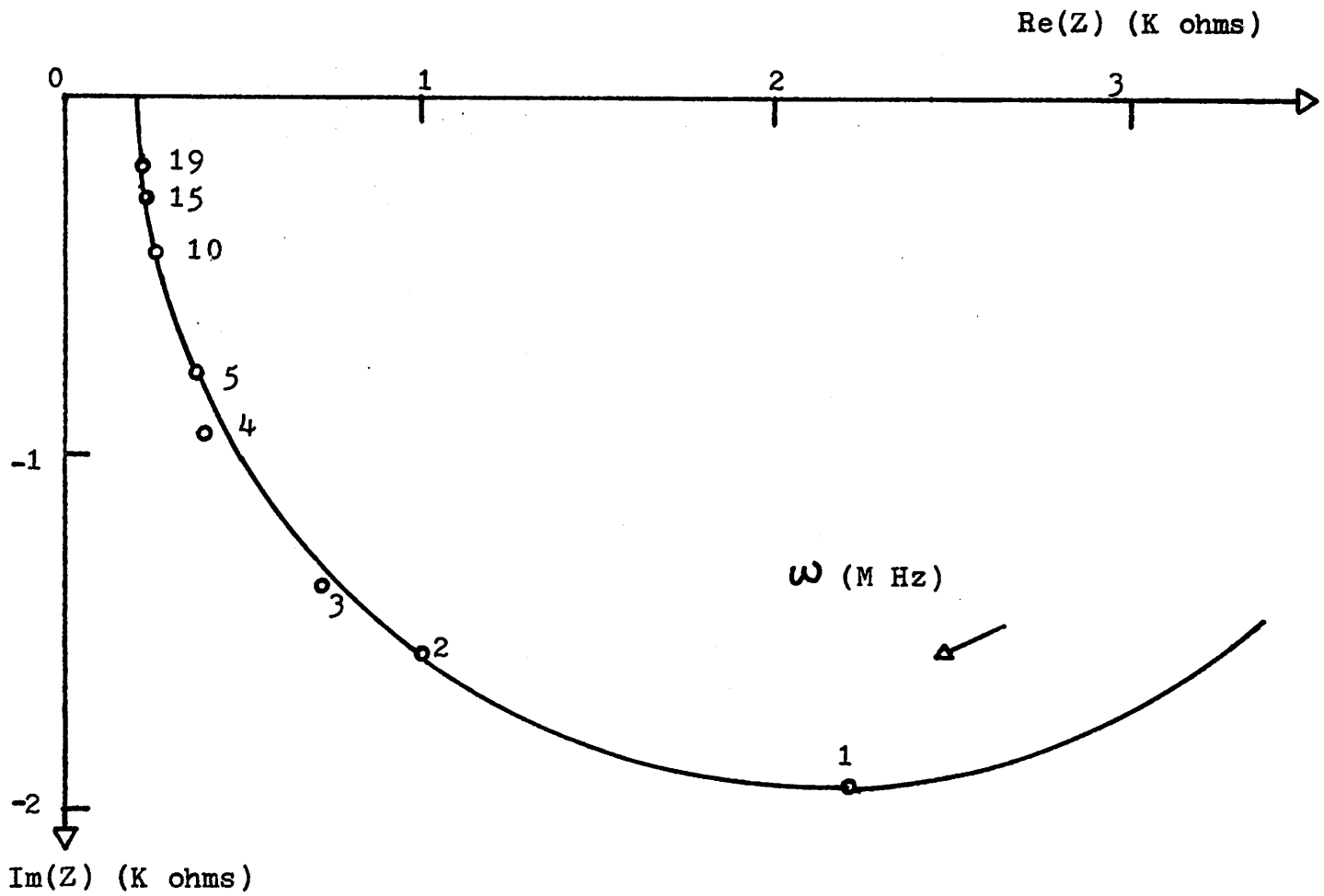


Fig. 3.2 Complex input impedance  
 Small NPN of 741  
 $I_c = 1.5 \text{ ma}$  , Base Resistance  $r_x = 200 \Omega$

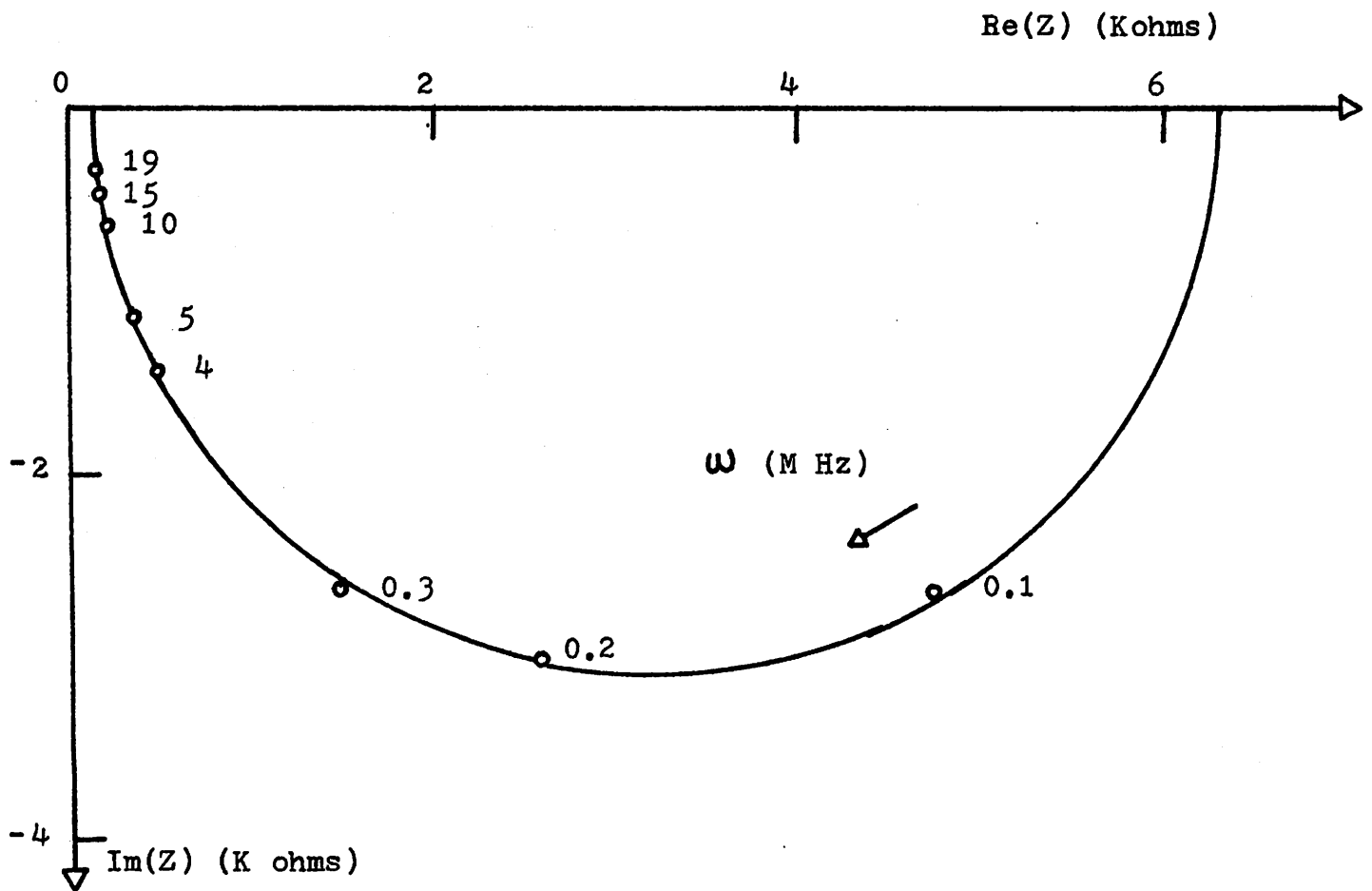


Fig. 3.3 Complex input impedance  
 Small NPN of 741  
 $I_c = 1.0 \text{ ma}$  , Base Resistance  $r_x = 200 \Omega$

$I_c$ (mA)	Small NPN	Small PNP	Large NPN	Substrate PNP	
10					
6					
4					
3			100	20	
2	180	150	110	20	
1.5	200	170			
1.0	200	180	110	35	
0.5	280	290			
0.3					
0.2					
0.1	500	400			
0.05		500			
0.02					

$I_c$ (mA)	Small NPN	Round Square PNP	Round PNP	Large NPN	Substrate PNP
10				340	
6	310	370		340	
4	400	470		340	
3					
2	560	780		340	22
1.5			46		
1.0			50	66	32
0.5	1050	1500	60	92	45
0.3				114	
0.2			84		
0.1			120		
0.05			210		
0.02			320		

 $r_x$   
(ohms)

ULX 2139
 $r_x$   
(ohms)

Table 3.1 Base resistance at different collector current levels

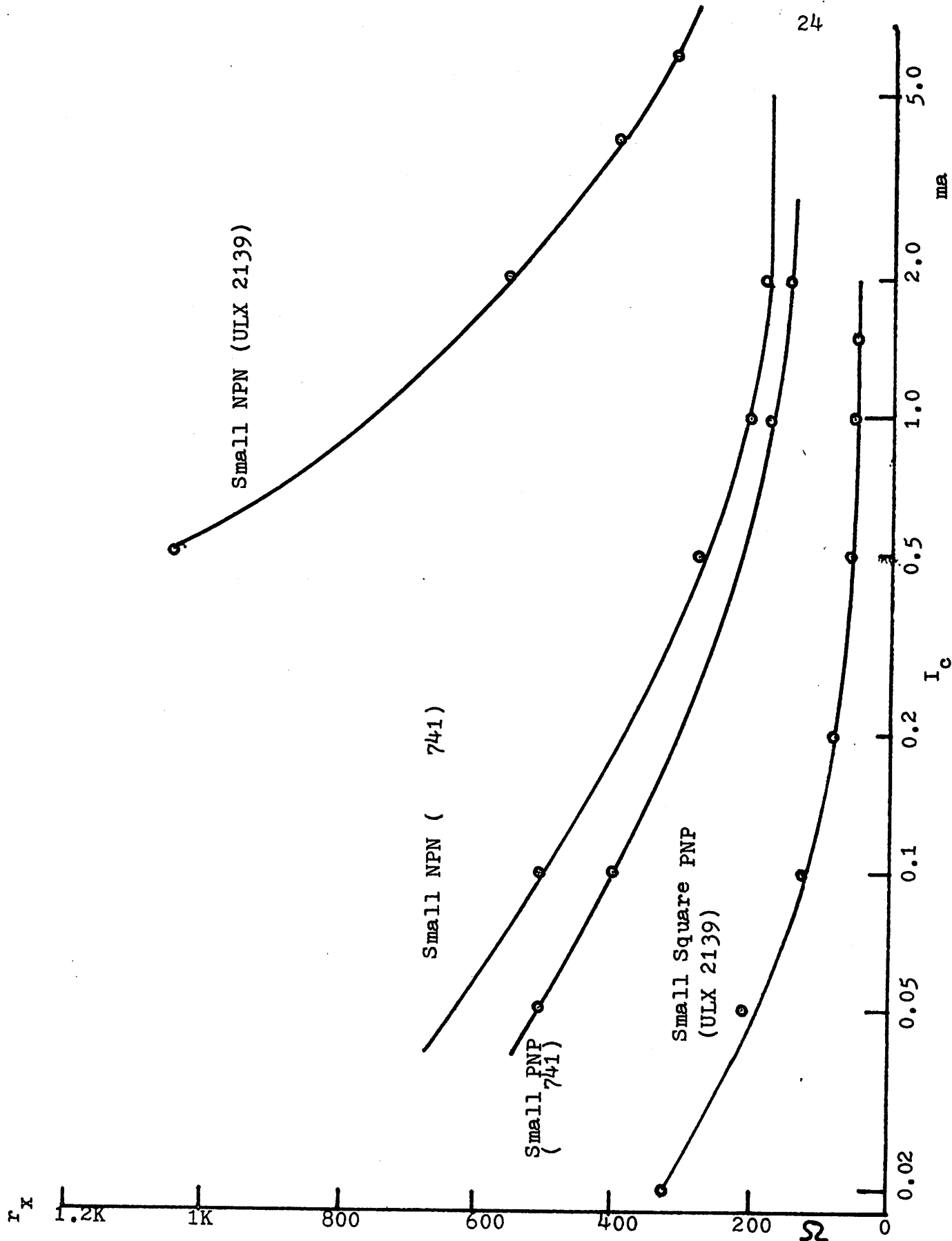
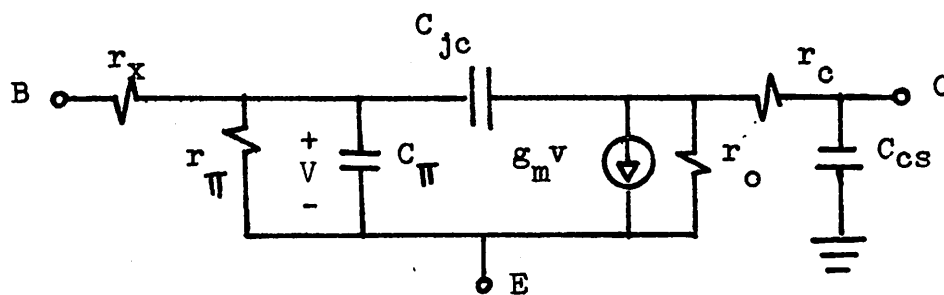
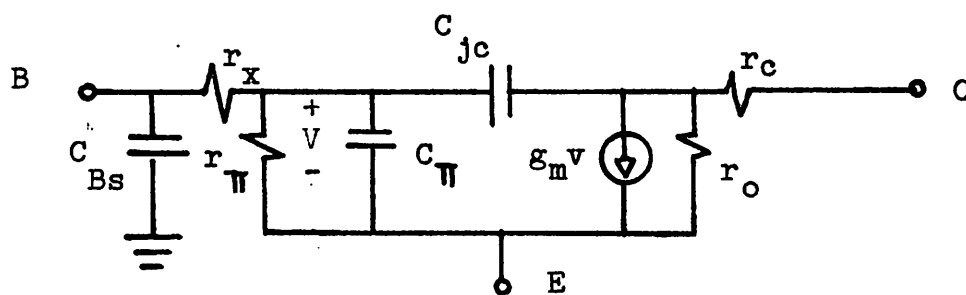


Fig. 3.4 Base resistance  $r_x$  as a function of collector current  $I_c$ .

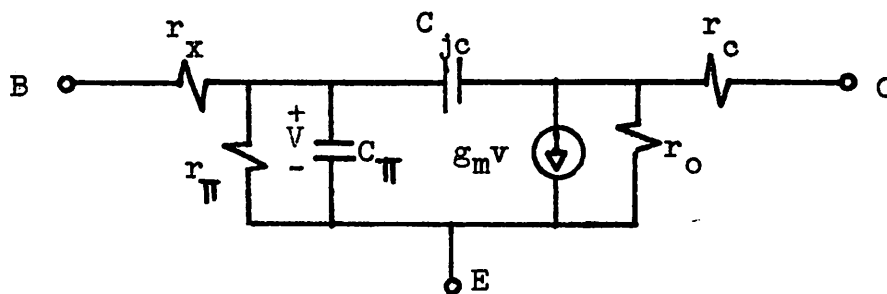




(a) NPN transistor

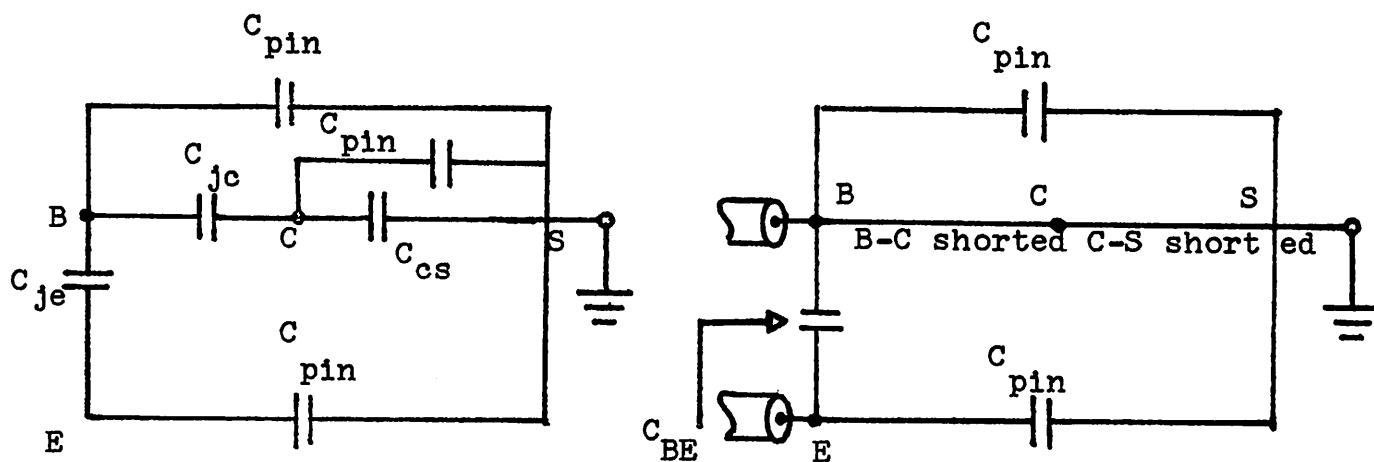


(b) Lateral PNP transistor



(c) Substrate PNP transistor

Fig. 3.5 Modified hybrid  $\pi$  models



(a) Junction and parasitic capacitance of npn transistor

(b) Measured capacitance between base and emitter

Fig. 3.6

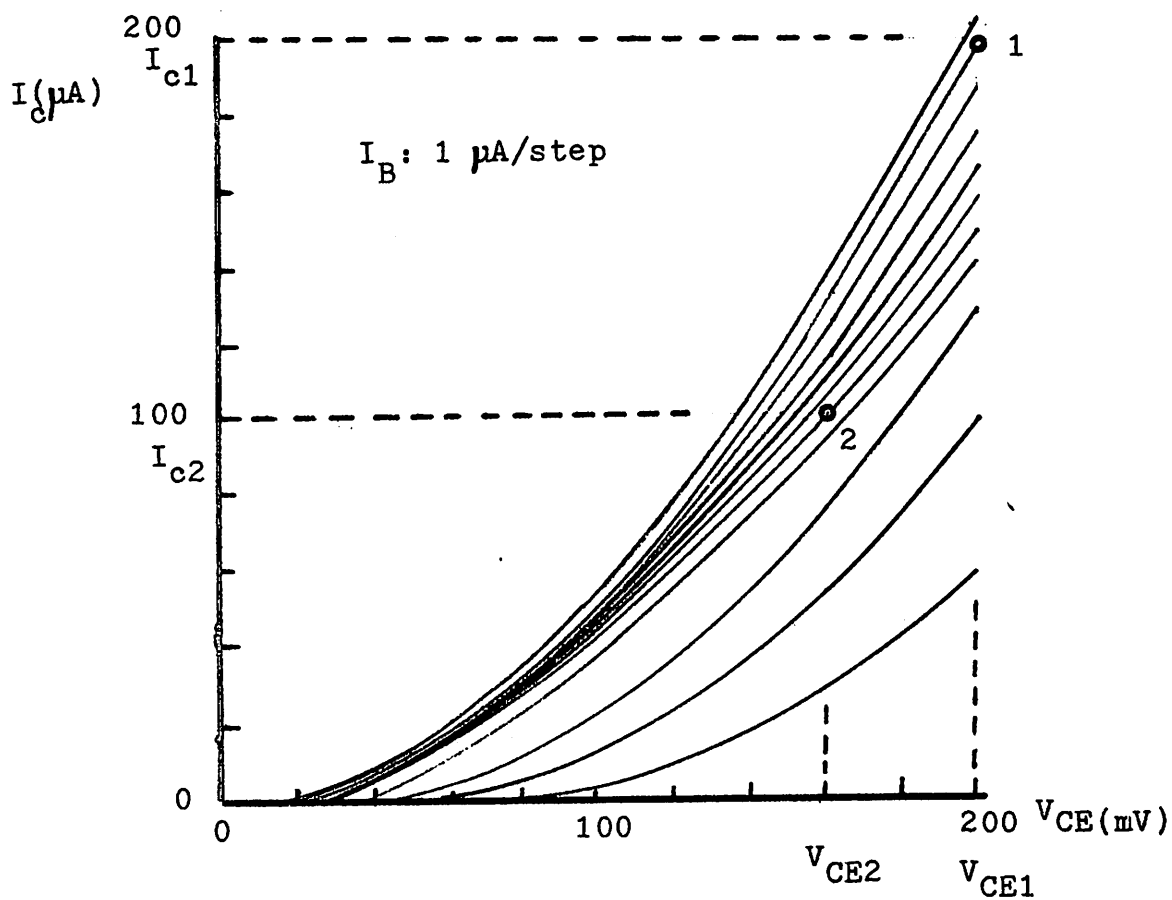


Fig. 3.7 I-V characteristic of an npn transistor in saturation region

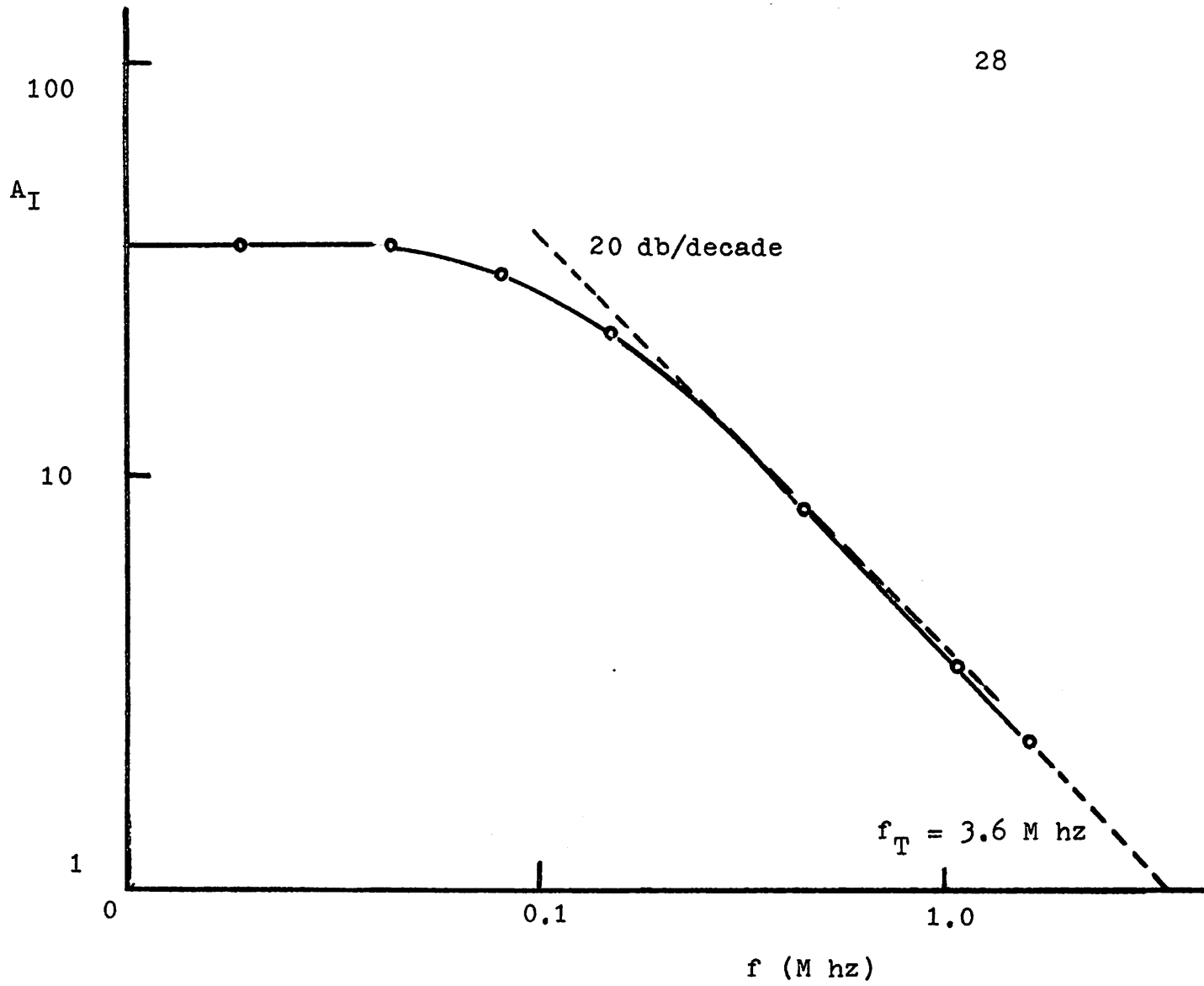


Fig. 3.8 Small signal current gain versus frequency

$f_T$  (MHz)  
 $P_o$

- 1 Small NPN
  - 2 Large NPN
  - 3 Small PNP
  - 4 Large Substrate PNP
- Broken line -----  $P_o$  vs  $I_c$  curves  
 Solid line \_\_\_\_\_  $f_T$  vs  $I_c$  curves

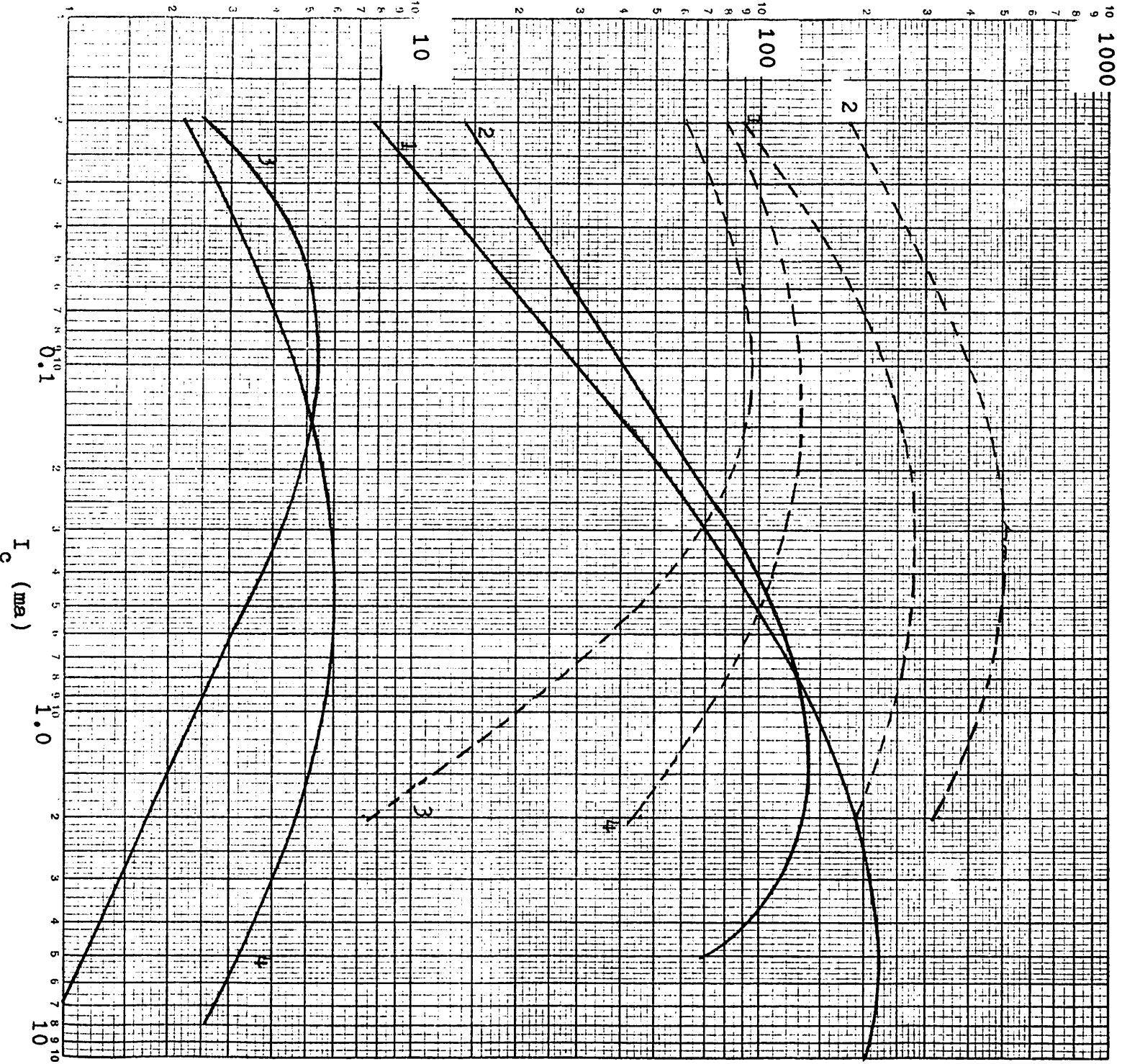
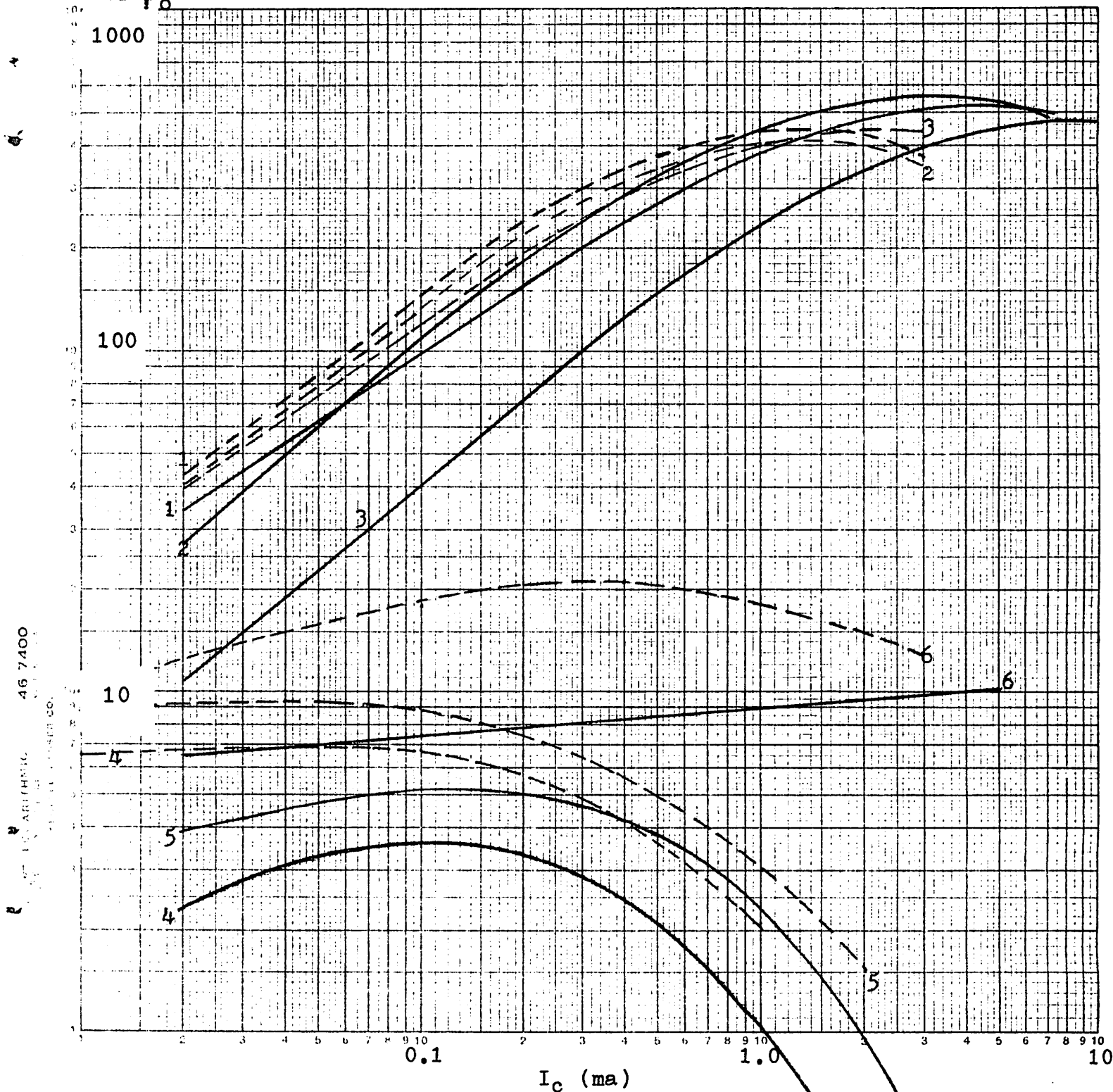


Fig. 3.9a 741 device characteristic

- 1 Small NPN
- 2 Round NPN
- 3 Large NPN
- 4 Small PNP
- 5 Round PNP
- 6 Large Substrate PNP

Broken line ----  $\beta_o$  vs  $I_c$  curves  
 solid line \_\_\_\_\_  $f_T$  vs  $I_c$  curves

$f_T$  (M Hz)  
 or  $\beta_o$



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Fig.3.9b ULX 2139 device characteristic

741						
	Small NPN	Large NPN	Small PNP	Substrate PNP		
$r_o^*$	180k	267k	55k	59.5k		
$B_R$	2.5	6.1	3.8	4.8		
$r_c$	300	15	150	156	ohms	
$I_{ES}$	1.26 $\times 10^{-15}$	3.95 $\times 10^{-16}$	3.15 $\times 10^{-15}$	1.76 $\times 10^{-14}$	Amps	
ULX 2139						
	Small NPN	Round NPN	Large NPN	Square PNP	Round PNP	Substrate PNP
$r_o^*$	34k	32.7k	28.1k	76k	61k	85.5k
$B_R$	3.0	3.0	6.0	1.8	1.8	1.2
$r_c$	130	80	10	240	320	200 ohms
$I_{ES}$	1.0 $\times 10^{-14}$	1.0 $\times 10^{-14}$	1.41 $\times 10^{-13}$	6.3 $\times 10^{-16}$	3.15 $\times 10^{-16}$	1.99 $\times 10^{-15}$ Amps

\*  
 $I_C = 1.0 \text{ mA}$

Table 3.2 Output resistance, reverse current gain, collector saturation resistance and reverse emitter saturation current

## Chapter IV

Circuit Analysis4.1 dc analysis

With +15 volt supplies and available data on  $\beta_0$  and  $I_{ES}$  as have been obtained in Chapter III, the operating points of the 741 and the ULX 2139 can be readily determined by Bias III, a nonlinear dc analysis program. Computer results of the transistor operating points are shown in Table 4.1 and 4.2.

The input current of the ULX 2139 is observed to be 40 nA, twice that of the 741. The collector current of the input device of the 741 is only 14  $\mu$ A, which accounts for the high input impedance as is brought out later in the ac analysis. However, it is very sensitive to voltage supplies. Lack of desensitization mechanism in the input stage for the operating collector current is probably the only drawback in the biasing scheme of the 741, which is simple and effective.

The insensitivity of current in current source of the input stage of the ULX 2139 is achieved by application of feedback from second stage back to first stage. As is illustrated in Fig.1.2a when there is an increase in the collector current of  $Q_5$  the collector voltage level of  $Q_2$  decreases, resulting in decrease in current through  $R_9$ ,  $R_{11}$ ,  $R_{12}$  and  $R_{13}$ . The decrease in voltage across  $R_{13}$  decreases collector current of  $Q_5$ . Negative feedback is therefore accomplished.



The collector current of  $Q_7$  and  $Q_{16}$ , in the 741, is kept to  $12 \mu\text{A}$  and  $18 \mu\text{A}$  respectively as has been predicted in Chapter II. The collector current of the output devices,  $Q_{14}$  and  $Q_{20}$ , is biased at  $400 \mu\text{A}$ , the level at which the  $I_C$  versus  $\beta_O$  curve of the substrate device,  $Q_{20}$ , reaches its maximum. The collector current of the output devices in the ULX 2139 is also biased at as low as  $700 \mu\text{A}$ .

The power dissipated in the devices in the ULX 2139 is expected to be higher than by those in the 741 since most devices in the former are observed to be operating at higher current levels.

#### Input Voltage Range

Differential-mode and common-mode input voltage range of the 741 and the ULX 2139 is examined through Bias runs. Again full circuits are used and unity feedback is applied to both amplifiers. With  $\pm 15 \text{ v}$  supplies different dc input voltages are applied to the inverting input terminals, with the non-inverting terminals grounded. The differential-mode input voltage range is the range of voltage which, if exceeded on the inverting terminal, causes the amplifier to cease functioning properly, one of the input devices being off, for example. Input of  $\pm 13 \text{ v}$  is observed from computer results to be the maximum input voltage that can be applied without turning off some of the devices in the ULX 2139. The 741 remains functioning until the input reaches  $\pm 12 \text{ volts}$ .

With the input applied at the non-inverting terminal, the common-mode input voltage range of both amplifiers are found in an analogous manner. The range of the ULX 2139 is  $\pm 6.5\text{v}$  and that of the 741 is  $+7.0\text{ v}$  to  $-6.5\text{v}$ .

#### Transfer characteristic of the output stage

Output stages of both the 741 and the ULX 2139 are shown in Fig. 3.15a and 3.15b. Transfer characteristics of both output stages are examined with the aid of Bias. Results of Bias runs are graphed in Fig. 4.1 and Fig. 4.2, which show that large output signals can swing up to  $\pm 14$  volts without loss of linearity in the 741 and  $\pm 12$  volts in the ULX 2139, both with  $\pm 15$  volt supplies. There is a problem in the ULX 2139 output stage which is shown in Fig. 3.15b. With the load open, the round lateral transistor  $Q_8$  starts turning off when the base of  $Q_8$  is driven positive with a large voltage. The impedance level at the collector of  $Q_8$  increases as the positive input increases until the high impedance path rids  $Q_9$  of its base charge. The off devices, transistors  $Q_8$  and  $Q_9$ , then cause the output to latch up the negative supply. This situation is also seen through computer result.

#### Experimental results

Output stages of both amplifiers were isolated and biased at  $\pm 15$  volts. DC voltages,  $+20$  volts to  $-20$  volts with 1 volt intervals, were applied at the base of  $Q_8$  for the ULX 2139, with the load open. Input voltages were also applied at the

base of  $Q_9$ , with  $Q_8$  scratched and separated from the output stage, and transfer characteristic was obtained. Linearity of both transfer characteristics is checked to insure that distortion, if occurs, is not caused by the high gain CC-CE device. Experimental results are shown in Fig.4.2. The transfer characteristic of the output stage of the 741 is also obtained with input voltage applied at the base of the substrate, double-emitter transistor,  $Q_{23A}$ . Both output stages can accommodate a large voltage swing without degrading linearity. It is also verified experimentally that as the base of  $Q_8$  in the ULX 2139 is driven positive and close enough to the supply, both  $Q_8$  and  $Q_9$  turn off and cause the output latching up with the negative supply. This will not happen, however, in normal use when the output is loaded with a much lower impedance. The large amount of current, gained by the composite device when it is driven negative, will saturate  $Q_{11}$  and sink through the load, instead of the Darlington substrate device. A 180 degree phase shift is therefore achieved as should have been.

For comparison Bias results and experimental results are plotted in the same graph as is shown in Fig. 4.1 and 4.2. They correspond to each other very closely.

OPERATIONAL AMPLIFIER WITH BIASING WITH BETA AND IES ADJUSTED 741

TEMPERATURE = 300.0

NUMBER OF ITERATIONS IN DC ANALYSIS = 40

NODE TO DATUM VOLTAGES

NODE	VALUE	NODE	VALUE	NODE	VALUE	NODE	VALUE
( 1 )	001872	( 2 )	002000	( 3 )	599914	( 4 )	599978
( 5 )	13.793686	( 6 )	13.622908	( 8 )	1.227796	( 9 )	-14.388461
( 10 )	14.354798	( 11 )	14.299904	( 12 )	14.270659	( 13 )	.673923
( 14 )	1.287311	( 15 )	14.228030	( 16 )	-14.928246	( 17 )	.070882
( 18 )	.627798	( 19 )	14.999182	( 20 )	011306	( 21 )	.009695
( 24 )	.000267	( 25 )	14.986006	( 26 )	14.915625	( 27 )	-14.986006
( 28 )	1.223693	( 29 )	.780193	( 30 )	-1.501603	( 31 )	.627663
( 32 )	13.791586	( 33 )	13.620814	( 34 )	-14.901245	( 35 )	-13.622944
( 36 )	14.994451	( 37 )	14.228677	( 22 )	15.000000	( 23 )	-15.000000
( 7 )	0.						

TRANSISTOR OPERATING POINTS

TRANSISTOR	IB	VBE	IC	VCE	BETA	GM	RPI
Q 1	0.0000020	.598042	.0001406	14.954712	70.000	.000544	1.2864E+05
Q 2	0.0000020	.597978	.0001403	14.954776	70.000	.000543	1.2896E+05
Q 3	0.0000028	.627882	.0001399	13.191672	50.000	.000541	9.2404E+04
Q 4	0.0000028	.627817	.0001395	13.020836	50.000	.000540	9.2634E+04
Q 5	0.0000020	.597545	.0001380	11.192320	70.000	.000534	1.3114E+05
Q 6	0.0000020	.597545	.0001380	11.363097	70.000	.000534	1.3114E+05
Q 7	0.0000023	.594775	.0001239	2.388461	54.000	.000479	1.1260E+05
Q 8	0.0000040	.645202	.00002733	.645202	68.000	.001057	6.4303E+04
Q 9	0.0000040	.645202	.00002733	16.223693	68.000	.001057	6.4303E+04
Q 10	0.0000025	.615721	.00002787	13.687829	110.000	.001078	1.0201E+05
Q 11	0.0000331	.700096	.00072902	.700096	220.000	.028203	7.8005E+03
Q 12	0.0000805	.729341	.00070845	.729341	88.000	.027407	3.2108E+03
Q 13A	0.0000805	.729341	.00070845	14.219807	88.000	.027407	3.2108E+03
Q 13B	0.0000805	.729341	.00070845	16.287311	88.000	.027407	3.2108E+03
Q 14	0.0000107	.662617	.00042756	14.988694	400.000	.016541	2.4182E+04
Q 15	0.0000000	.011573	.00000000	.674190	100.000	.000000	1.0000E+09
Q 16	0.0000021	.605086	.0001847	29.222480	190.000	.000715	1.2594E+05
Q 17	0.0000325	.699569	.00071430	13.426643	220.000	.027633	7.9614E+03
Q 18	0.0000329	.698680	.00069015	11.301721	210.000	.026699	7.8654E+03
Q 19	0.0000019	.603042	.00001707	.603042	88.000	.000660	1.3328E+05
Q 20	0.0000386	.617968	.00042467	14.990305	110.000	.016429	6.6956E+03
Q 21	0.0000000	.009428	.00000000	14.998915	20.000	.000000	1.0000E+09
Q 22	0.0000000	.000818	.00000000	1.377092	100.000	.000000	1.0000E+09
Q 23A	0.0000588	.659513	.00070538	14.273447	120.000	.027288	4.3975E+03
Q 23B	0.00000012	.335598	.00000000	1.377092	70.000	.000000	1.0000E+09
Q 24	0.0000000	.000818	.00000000	.000818	100.000	.000000	1.0000E+09

Table 4.1 dc biasing of the 741

OPERATIONAL AMPLIFIER DC BIASING OF THE ULX 2139

TEMPERATURE = 300.0

NUMBER OF ITERATIONS IN DC ANALYSIS = 9

NODE TO DATUM VOLTAGES

NODE	VALUE	NODE	VALUE	NODE	VALUE	NODE	VALUE
(1)	-00303	(3)	-00688	(4)	-00388	(5)	11.44255
(6)	11.339619	(7)	14.764039	(8)	13.958253	(9)	-583239
(10)	-566808	(11)	-566691	(12)	14.596582	(13)	14.596582
(14)	-14.688212	(15)	-14.083774	(16)	-13.396306	(17)	10.494338
(18)	10.723109	(19)	10.815936	(20)	13.701274	(21)	13.404250
(22)	14.453872	(23)	14.051858	(24)	1.272966	(25)	620357
(26)	-032799	(27)	-685955	(28)	-1.339112	(29)	-14.049648
(30)	007095	(31)	-016296	(32)	-0.703386	(33)	042198
(34)	15.000000	(35)	-15.000000	(36)	0		

TRANSISTOR OPERATING POINTS

TRANSISTOR	IB	VBE	IC	VCE	BETA	GM	RPI
Q 1	0000040	566120	0003247	12.008063	82.000	001256	6.5284E+04
Q 2	0000040	566303	0003270	11.906311	82.000	001265	6.4823E+04
Q 3	00000464	638329	0003342	-3.155327	7.200	001293	5.5695E+03
Q 4	00000464	638329	0003342	-3.256963	7.200	001293	5.5695E+03
Q 5	0000041	584437	0006594	14.084973	160.000	002551	6.2713E+04
Q 6	0000071	616511	00022806	2.978165	320.000	008823	3.6269E+04
Q 7	0000094	625319	0003205	2.588314	340.000	012405	2.7408E+04
Q 8	0000260	647608	0002392	-12.778891	9.200	000926	9.9440E+03
Q 9	0000219	652610	00092160	13.431501	420.000	035653	1.1780E+04
Q 10	0000226	653342	00094809	12.710536	420.000	036678	1.1451E+04
Q 11	0000203	578158	00072930	14.957802	360.000	028214	1.2760E+04
Q 12	0000458	635726	0003022	14.296614	6.600	001169	5.6463E+03
Q 13	00003481	687090	00069615	-14.983704	20.000	026931	7.4264E+02
Q 14	0000000	000300	0000000	000300	200.000	000000	1.0000E+09
Q 15	0000000	000300	0000000	000300	200.000	000000	1.0000E+09
Q 16	0000224	653156	00094130	653156	420.000	036415	1.1534E+04
Q 17	0000000	0000000	0000000	0000000	200.000	000000	1.0000E+08
Q 18	0000000	0000000	0000000	0000000	200.000	000000	1.0000E+08

ELAPSED TIME = 2.08 SECONDS

Table 4.2 dc biasing of the ULX 2139

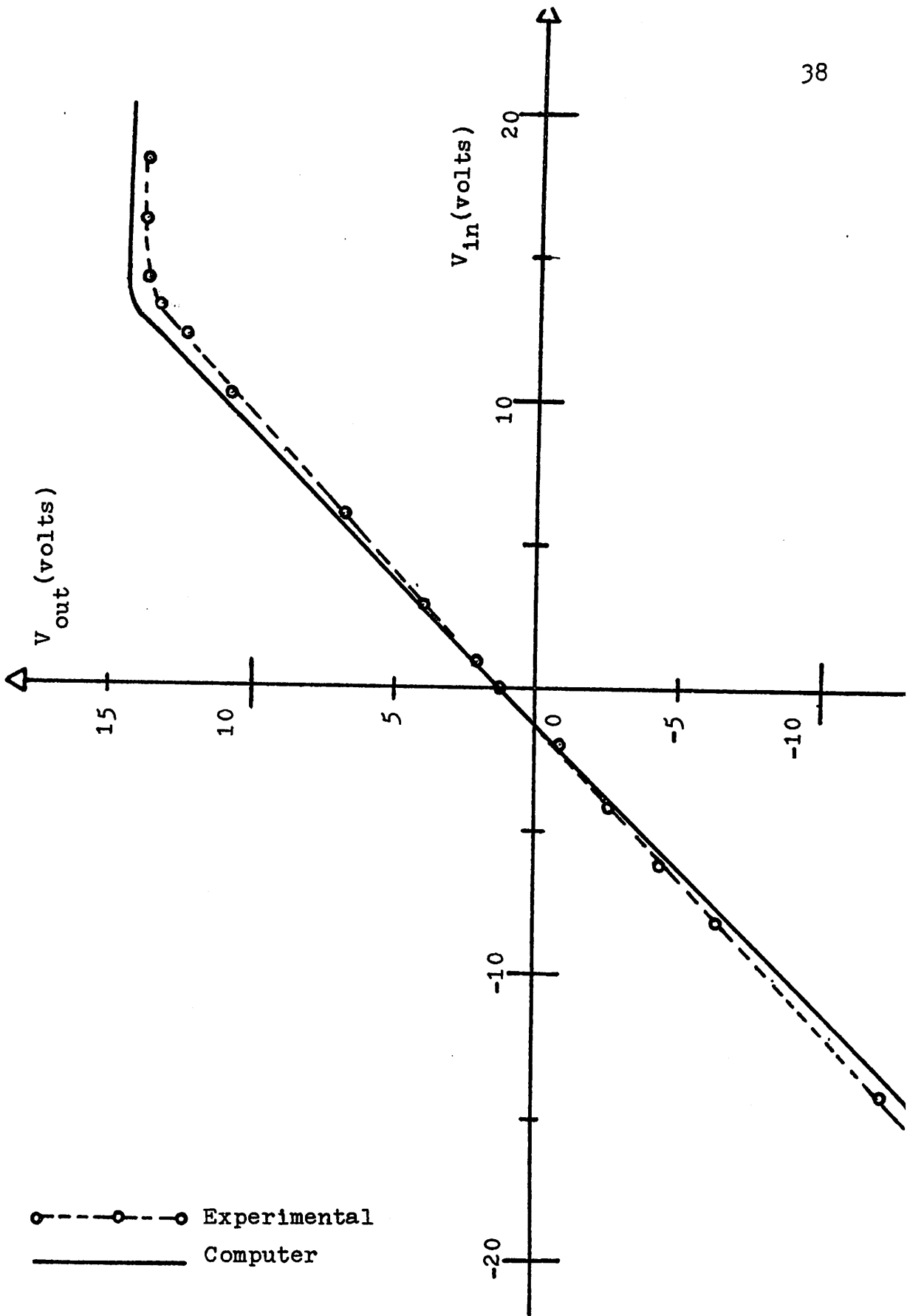


Fig. 4.1 Transfer characteristic of the output stage 741

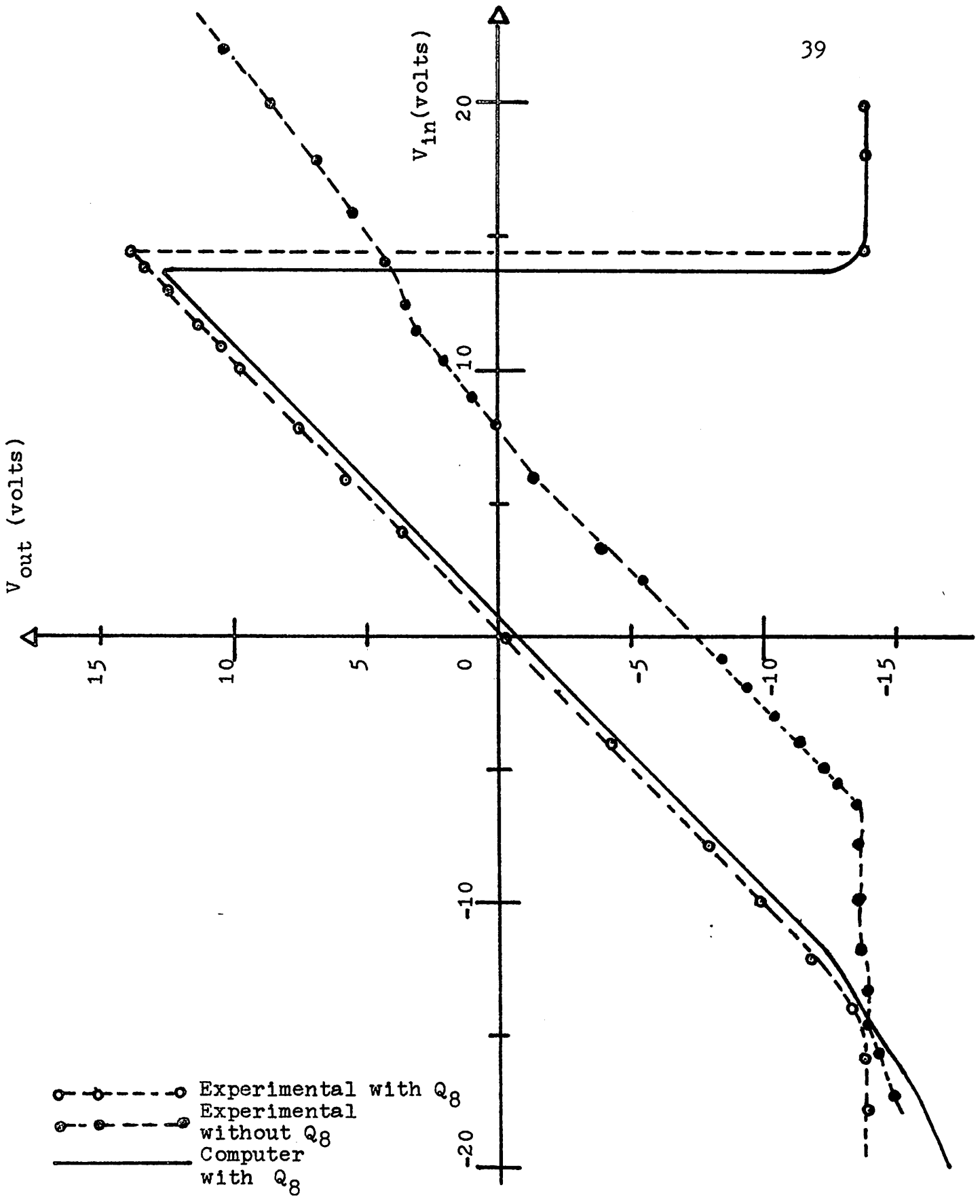


Fig. 4.2 Transfer characteristic of the ULX 2139 output stages

## 4.2 ac analysis

### The 741

The methods used in achieving high gain, high input impedance and high common-mode rejection are discussed here. Input impedance of the amplifier can be calculated by means of differential half circuit as follows:

With base resistance  $r_x$  neglected it follows from Fig. 4.3 that

$$R_{in(diff)} = r_{\pi_1} + \frac{\beta_1 + 1}{\beta_2 + 1} r_{\pi_2} = r_{\pi_1} + \frac{\beta_1 I_{c1}}{V_T} = 2r_{\pi_1}$$

Note that the input impedance of the amplifier is exclusively dependent on the quiescent current level of the input stage. Since an increase in voltage supplies would cause an increase in collector current of the input stage, the input resistance of the amplifier, in effect, is decreased with increase in bias voltages.

To achieve high input impedance the collector dc current must be as low as possible. On the other hand, the slew rate of the amplifier is directly proportional to the input stage quiescent current if compensation is achieved at the intermediate gain stage (5); lowering the collector current will adversely affect the slew rate.

Two unbalance-to-balance conversion stages are shown in Fig. 4.4. The diode-connected circuit is the simplest scheme for gain conversion. The incremental change of collector



current  $i_1$  due to the differential input causes same amount of current  $i_3$  to flow through  $Q_6$  provided the emitter area are the same for both  $D_5$  and  $Q_6$ . For differential-mode operation,

$$i_1 = -i_3 \quad (4.1)$$

$$i_L = i_2 - i_3 = i_2 + i_1 \quad (4.2)$$

Full differential gain can therefore be realized at the load.

If both  $i_1$  and  $i_2$  are flowing the same direction, as in common-mode operation,  $i_2$  will approximately cancel  $i_3$  as shown in equation (4.2); thus common-mode signal is rejected. There is a mismatch between  $i_2$  and  $i_3$  for diode-connected conversion circuit,  $i_2 = \frac{\beta_0}{\beta_0 + 1} i_3$  for open load. To reduce the mismatch between  $i_2$  and  $i_3$  an improved version is employed as shown in Fig.4.4b, in which  $Q_7$  is a substitute for diode,  $D_5$ . Now

$$i_3 = i_4 = i_1 - i_5 + (1/\beta_0) i_1 \approx i_1$$

Thus  $i_L = i_2 - i_3 = 0$ , and common-mode signal is perfectly rejected.

#### Compensation of the 741

The Darlington compound transistor provides high impedance level for compensation. With results obtained from computer-aided analysis with Pottle, an ac analysis program, the first two poles of first three dominant poles, which are given in Table 4.3, are believed to be contributed by

the Darlington pair. The first pole is observed in Table 4.3 to move much closer to the imaginary axis while the second dominant pole moves further outward by more than an order of magnitude, which is generally described as pole-splitting action, when the Miller compensation capacitor is applied. With the ac equivalent circuit shown in Fig. 4.8a it can be estimated that the new, most dominant pole is determined by the time constant of the Miller capacitance of the 30pf capacitor, which is about 30pf multiplied by the gain of the pair, and the impedance at the collector of  $Q_{17}$ . Results from Rohrer X runs are shown in Fig. 4.9 in which small-signal voltage gain and phase shift of the amplifier shown in Fig. 3.8a are plotted as functions of frequency. Phase crossover is observed to occur at 0.51 Mhz without compensation. With compensation the phase shift due to the compensated second and third poles is reduced because the new poles are located at higher frequency. Phase crossover is thus improved, occurring at 4.1 Mhz with compensation.

It is worth noticing that phase is reduced by about 10 degrees at 6 Mhz if the input lateral pnp were replaced with high performance pnp's, with frequency and current gain performance improved as good as the npn's, in the uncompensated phase response. A 20 dB per decade frequency roll-off and a  $61^\circ$  phase margin is achieved at unity-gain

cross-over frequency with compensation. Low frequency gain is also increased by about 10% when high performance pnp's are used. With improved phase response and gain the high performance pnp might provide partial solution to improve phase margin and crossover frequency in the compensated response.

The gain and phase response are also examined with diode-connected unbalance-to-balance conversion circuit used in the amplifier. No appreciable change in gain and phase shift are noticed. This agrees with the fact that the improved version of conversion circuit helps only the cancellation of common-mode signal, gives no significant improvement over differential-mode signal gain.

#### The ULX 2139

Emitter couple pair with emitter degeneration resistors configuration being inferior to the composite device configuration is evidenced by the inferior frequency performance and lower input impedance of the input stage of the ULX 2139. Input impedance and phase response of the amplifier are given in Fig. 4.10 and Fig.4.11 respectively. Note that excess phase shift contributed by transistor  $Q_8$ , a round lateral device, is appreciable. Reduction of  $15^\circ$  phase shift can be achieved if a high performance pnp is used. This is an equivalence of 5 dB gain margin which is needed very much because a phase margin of only  $24^\circ$  degrees

is achieved for the compensated amplifier as shown in Fig.3.10. It will be shown later that the phase margin is reduced further when high source resistance is presented. The only feasible solution to improve the unfavorable phase response of this design is the replacement of  $Q_8$  with better pnp.

For the sake of contrast, common-mode rejection ratio of the ULX 2139 and the 741 is plotted against frequency in Fig. 4.12. A rejection of 92 dB and 100 dB is achieved with the diode-connected conversion and the improved conversion respectively in the 741. The common-mode rejection capability of the ULX 2139 is 20 dB better than what the 741 can achieve with improved unbalance-to-balance conversion. A brief common-mode analysis is given below for the ULX 2139: Common-mode half circuit is given in Fig.3.5. When common-mode signal is high there is tendency to increase  $i_1$  in the direction indicated by the arrow. Due to the presence of current source  $I_1$ ,  $i_2$  is pulled out of  $Q_7$  with an increase of  $i_2$ , resulting in decrease in  $i_3$  and  $i_4$ . Cancellation occurs between  $i_1$  and  $i_4$  and thus common-mode signal is rejected. With the high impedance at first and second stages and the addition of feedback, the CMR of the ULX 2139 is 120 dB.

### Compensation of the ULX 2139

With compensation being able to be achieved at any of the three gain stages every possibility is evaluated here. The only high impedance point present in the second and third stages is at the collector of  $Q_7$ . Due to the high current gain characteristic of the CC-CE compound device, the input impedance presented by the emitter follower is very high. If compensating capacitor is shunted at the collector of  $Q_7$ , the slew rate of the amplifier is limited by the amount of collector current available in second stage and the response delay due to two differential stages. Therefore slew rate consideration limits the degree of freedom into one, compensation in the first stage as designed. Results from Pottle analysis, which are given in Table 4.3, reveals that the second dominant, open-loop, uncompensated pole is contributed by  $Q_8$  and the first pole by the second stage. By using the RC series network for compensation, which is shown in Fig. 3.8, a new pole and zero are introduced in the open-loop transfer function. The approximate input lag model given in Fig. 3.6 reveals tentatively the new location of the most dominant pole and the introduced zero. The most dominant pole becomes  $\frac{1}{R_{2nd} C_F}$ , and the added pole is  $\frac{1}{R_F C_1}$ . The zero is  $\frac{1}{R_F C_F}$ . The first, new pole as is given in Table 4.3 is at 770 rad/sec, which seems reasonable considering the magnitude

of  $R_{2nd}$  and the 2200 pf of  $C_F$ , the second pole due to the round lateral transistor  $Q_8$  remains unchanged. This partially explains why the phase margin of the ULX 2139 is so poor.

Another drawback of this compensation technique is the use of hybrid capacitor to avoid the size of a 2200 pf MOS capacitor.

741		
	Without compensation	With compensation
Pole positions (rad/s)	$-3.136 \times 10^4$	-9.116
	$-7.797 \times 10^5$	$-2.132 \times 10^7$
	$-1.738 \times 10^7 \pm j1.114 \times 10^7$	$-3.668 \times 10^7$
zero positions (rad/s)	$-6.669 \times 10^6 \pm j2.531 \times 10^8$	$-6.669 \times 10^6 \pm j2.531 \times 10^8$
	$-3.663 \times 10^7$	$-3.663 \times 10^7$
	$-3.792 \times 10^7$	$-3.792 \times 10^7$
ULX 2139		
Pole position (rad/s)	$-7.687 \times 10^3$ (cancellation)	$-7.714 \times 10^2$ (first pole)
	$-2.936 \times 10^5$ (first pole)	$-7.687 \times 10^3$ (cancellation)
	$-1.682 \times 10^6$ (second pole)	$-1.479 \times 10^6$ (second pole)
Zero position (rad/s)	$-7.687 \times 10^3$ (cancellation)	$-7.687 \times 10^3$ (cancellation)
	$-6.003 \times 10^7$ (first zero)	$-1.167 \times 10^6$ (first zero)
	$-1.079 \times 10^8$	$+3.015 \times 10^7 \pm j2.100 \times 10^8$

Table 4.3 Poles and zeros of the 741 and the ULX 2139<sup>9</sup>

<sup>9</sup>Some approximation is assumed in obtaining the poles and zeros. Half circuit of the ac equivalent circuit shown on Fig. 3.8a is used for the 741 for Pottle analysis. Refer to Schwartz's report for balance and unbalance consideration. Full circuit of that shown in Fig. 3.8b is used for the ULX 2139 with current source considered open, active load infinite impedance and effective load at the emitter of Q<sub>9</sub> 100 k ohms.

### Effect of Source Resistance on Frequency Response

The effect of source resistance on frequency response of the 741 and the LUX 2139 is examined by using Rohrer X. The phase responses of both amplifiers which are shown in Fig. 4.8a and 4.8b are observed to be degraded due to the presence of  $R_s$ , resulting in unbalance in the input stages. Compensated phase crossover is observed to decrease with increase in source resistance. As shown in Table 4.4 the compensated phase crossover frequency is decreased from 3.2 M hz to 2.65 M hz for the ULX 2139 in comparison to the decrease of the 741, from 4.1 M hz to 3.5 M hz. It is detrimental to the ULX 2139, as is shown in Table 4.4, to have a phase margin of only 16.5 degrees. Stability cannot be ensured at frequency close to the unity gain crossover frequency, with  $R_s$  being 5k. Although the 741 suffers the loss of almost 5 degrees of phase margin with  $R_s$  being 5k ohms, it is still far from having problem of instability.



741					
$R_s$ (k ohm)	Voltage gain $\times 10^5$	Phase crossover		Phase margin with comp (degrees)	Unity gain freq.w.comp. (Mhz)
		Without comp (Mhz)	With comp (Mhz)		
0	1.3	0.51	4.1	61	1.26
100	1.3	0.51	4.1	60.7	1.26
500	1.3	0.51	4.0	60.3	1.26
1k	1.3	0.51	3.9	59.7	1.26
2k	1.298	0.51	3.8	58.4	1.26
5k	1.290	0.51	3.5	54.7	1.26
ULX 2139					
0	.369	0.49	3.2	24	2.0
100	.369	0.49	3.18	23.86	2.0
500	.368	0.49	3.1	23.2	2.0
1k	.367	0.48	3.05	22.5	2.0
2k	.364	0.48	2.9	20.9	2.0
5k	.358	0.47	2.65	16.5	2.0

Table 4.4 Effect of source resistance,  $R_s$ ,  
on frequency response of  
the 741 and the ULX 2139

### Slew Rate

Detailed treatment of slew rate of simple op-amps and fast op-amps is found in Solomon's paper on slew rate. As is shown in Fig.4.7b, the slew rate of the simplified 741 and ULX 2139 is  $2I_C/C_F$  and  $A_V(I_C/C_F)$  respectively. The slew rate of the ULX 2139 is greatly boosted by the gain available in the succeeding stages with compensation achieved in the input stage as shown in Fig. 4.7a. A quick calculation shows that the slew rate is  $0.9v/\mu s$  and  $3.5v/\mu s$  respectively. This justifies why compensation for the ULX 2139 is done in the input stage.

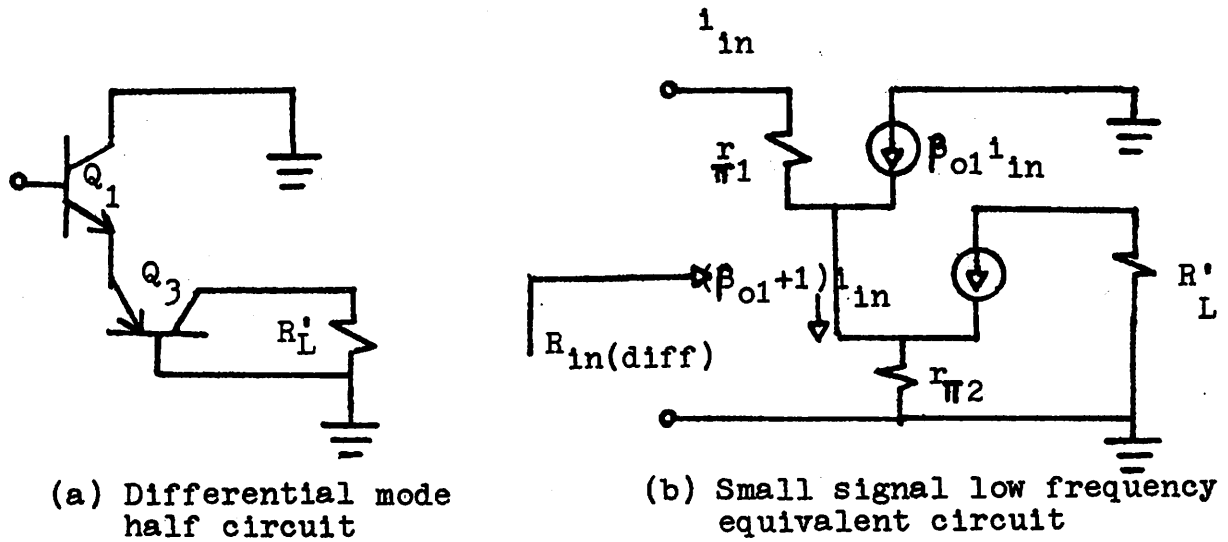


Fig. 4.3

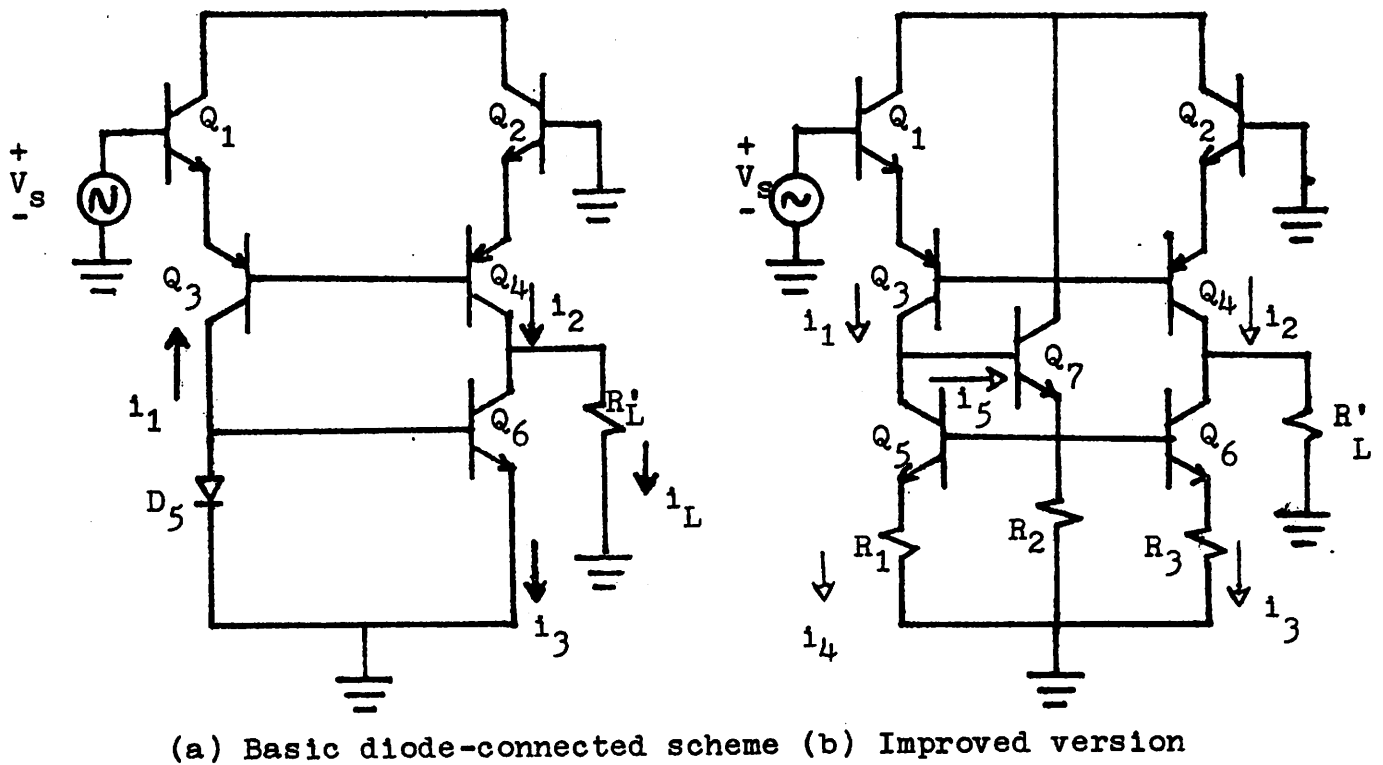


Fig. 4.4 Gain conversion stages

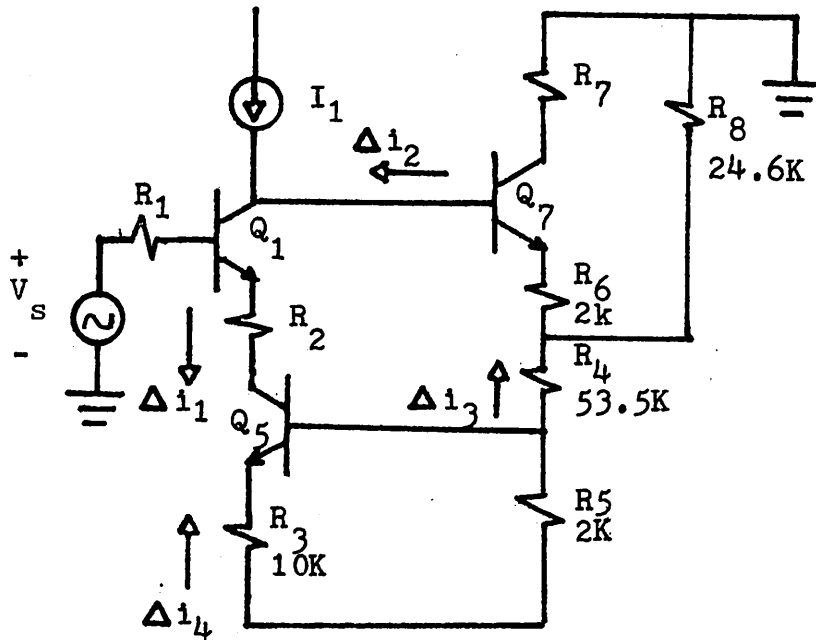
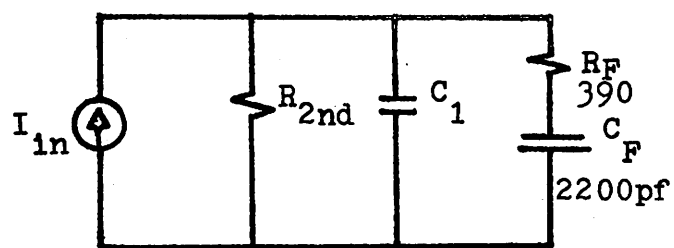


Fig. 4.5 Common mode half circuit



$R_{2nd}$  is the effective differential loading of the second stage and  $C_1$  is the parasitic capacitance between collectors of  $Q_1$  and  $Q_2$

Fig. 4.6 Approximate input lag model

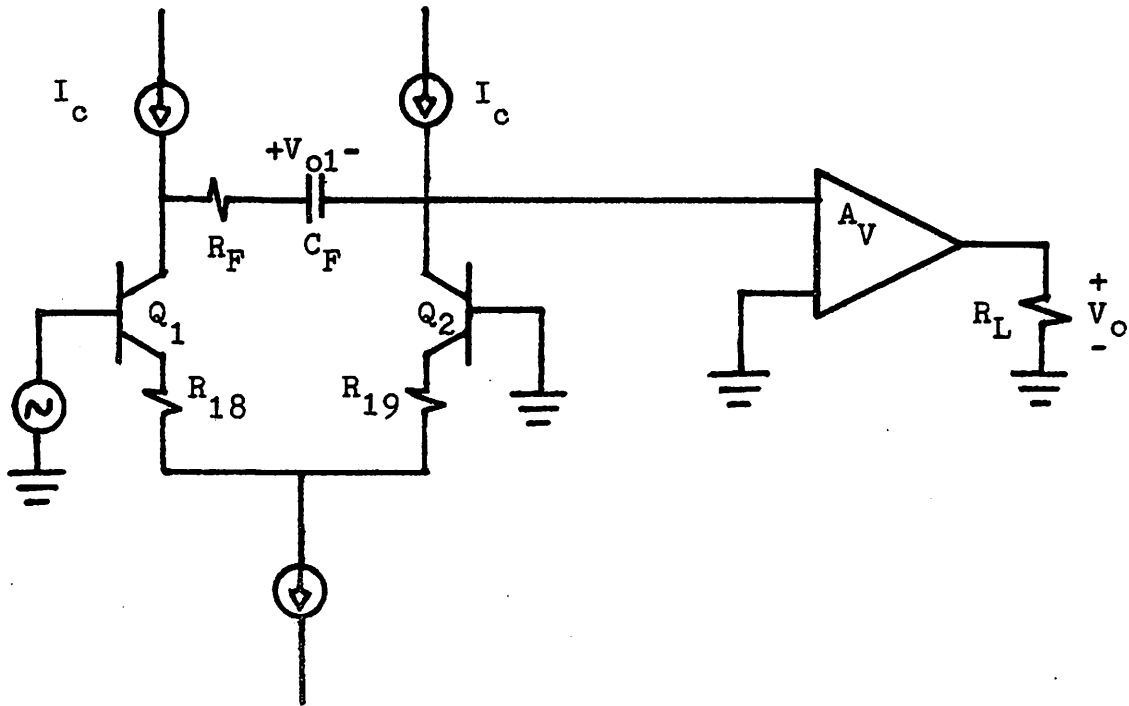


Fig. 4.7a Second and third stages as an ideal amplifier

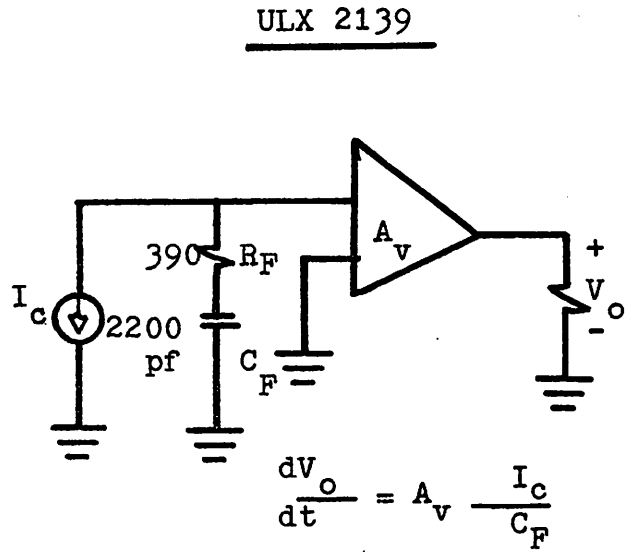
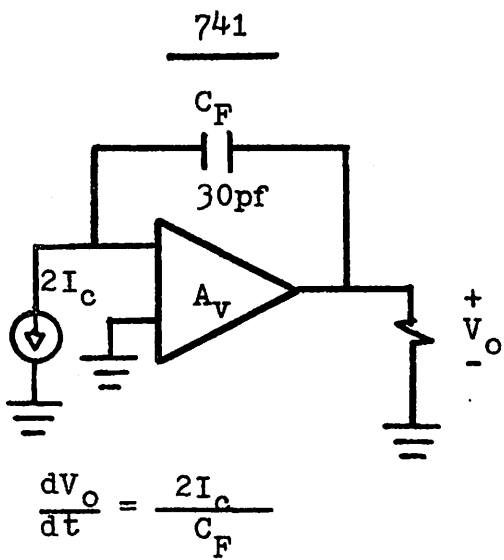
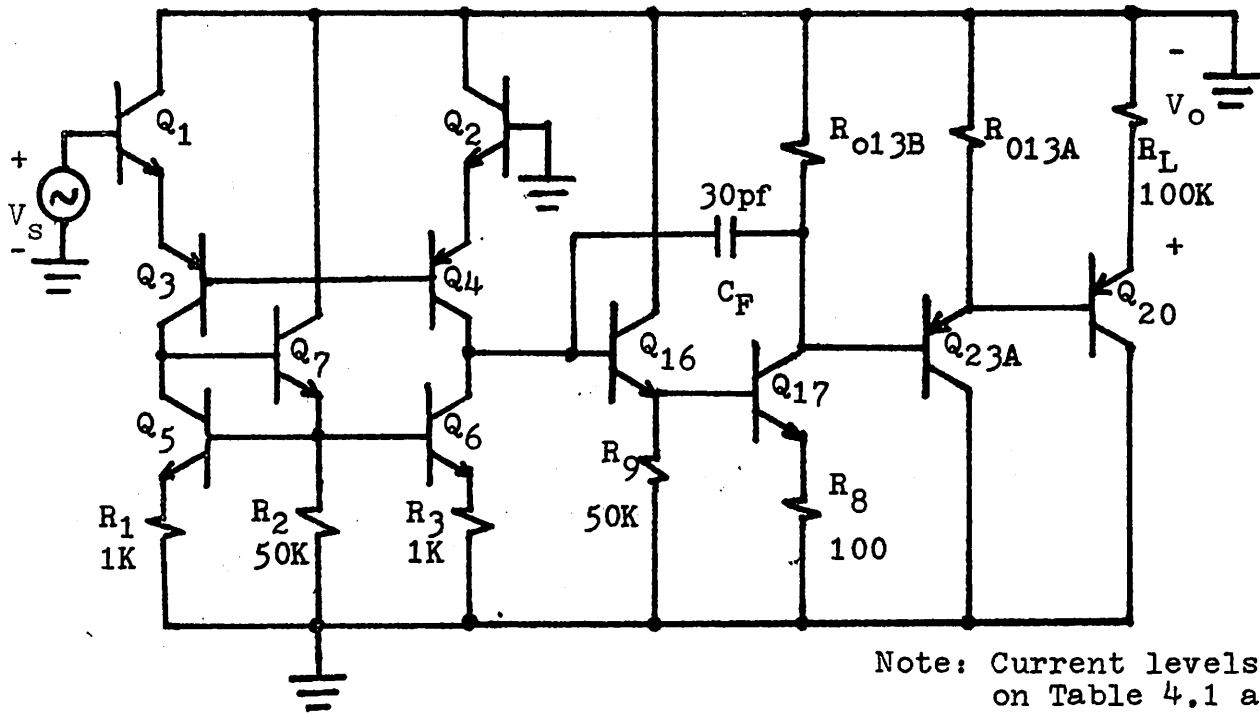
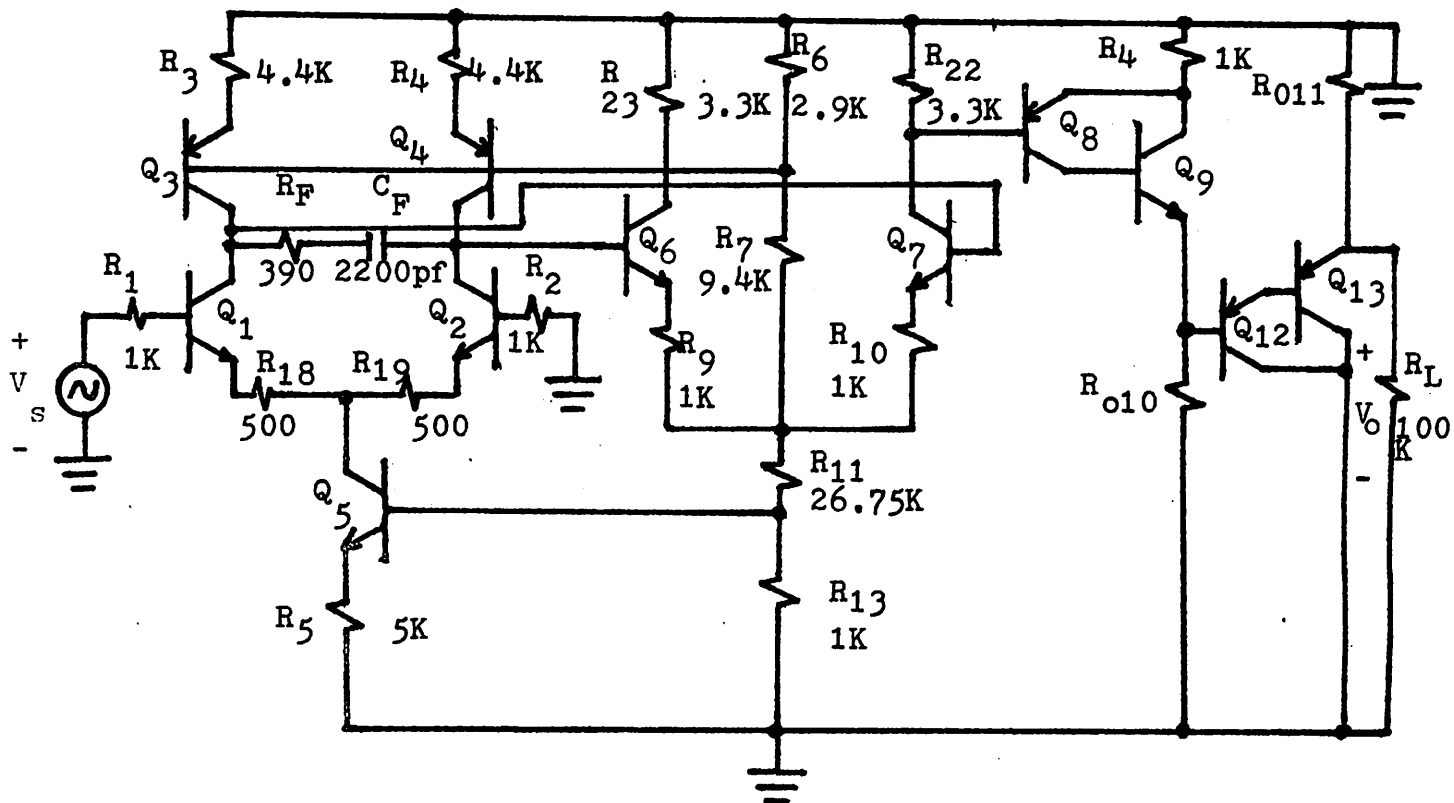


Fig. 4.7b Calculation of slew rate for the 741 and the ULX 2139



(a) 741

Note: Current levels are found on Table 4.1 and 4.2. Effect of different  $R_S$  is found on Table 4.4. Both circuits are analysed with  $R_L=100k$ .



(b) ULX 2139

Fig. 4.8 AC analysis-small signal equivalent circuits

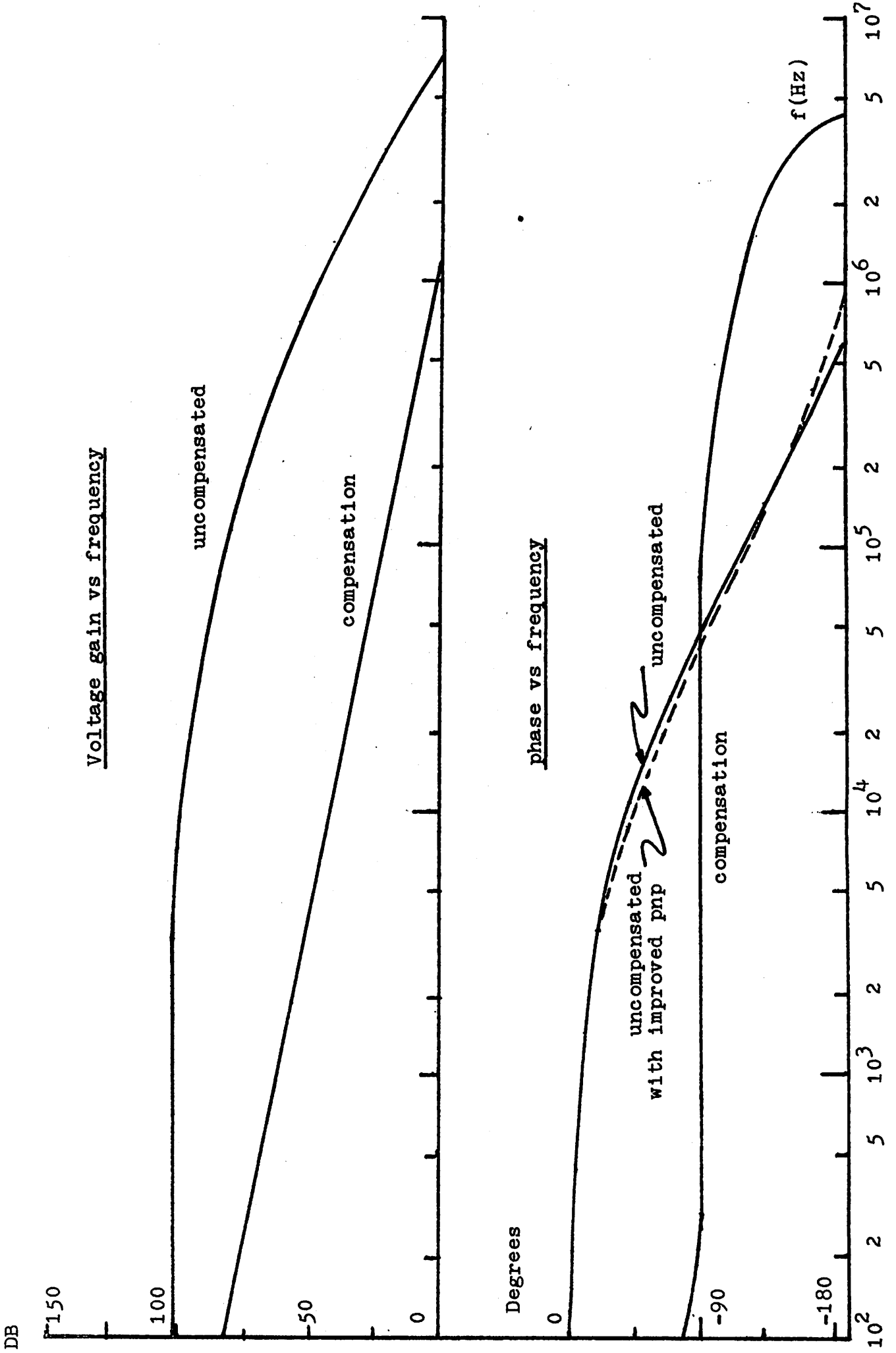


Fig. 4.9 Small signal voltage gain and phase shift as functions of frequency



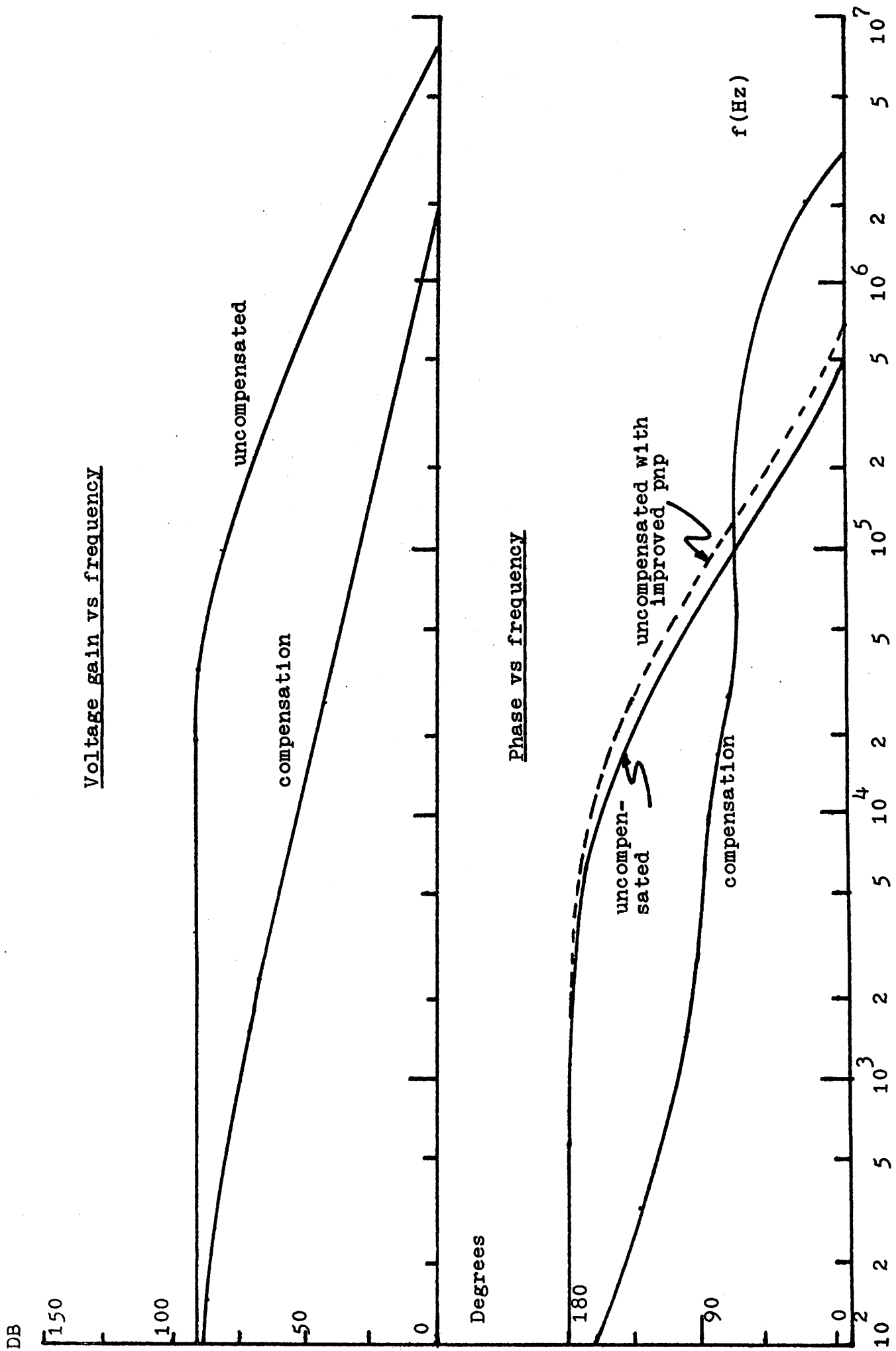


Fig. 4.10 Small signal voltage gain and phase shift as functions of frequency  
ULX 2139

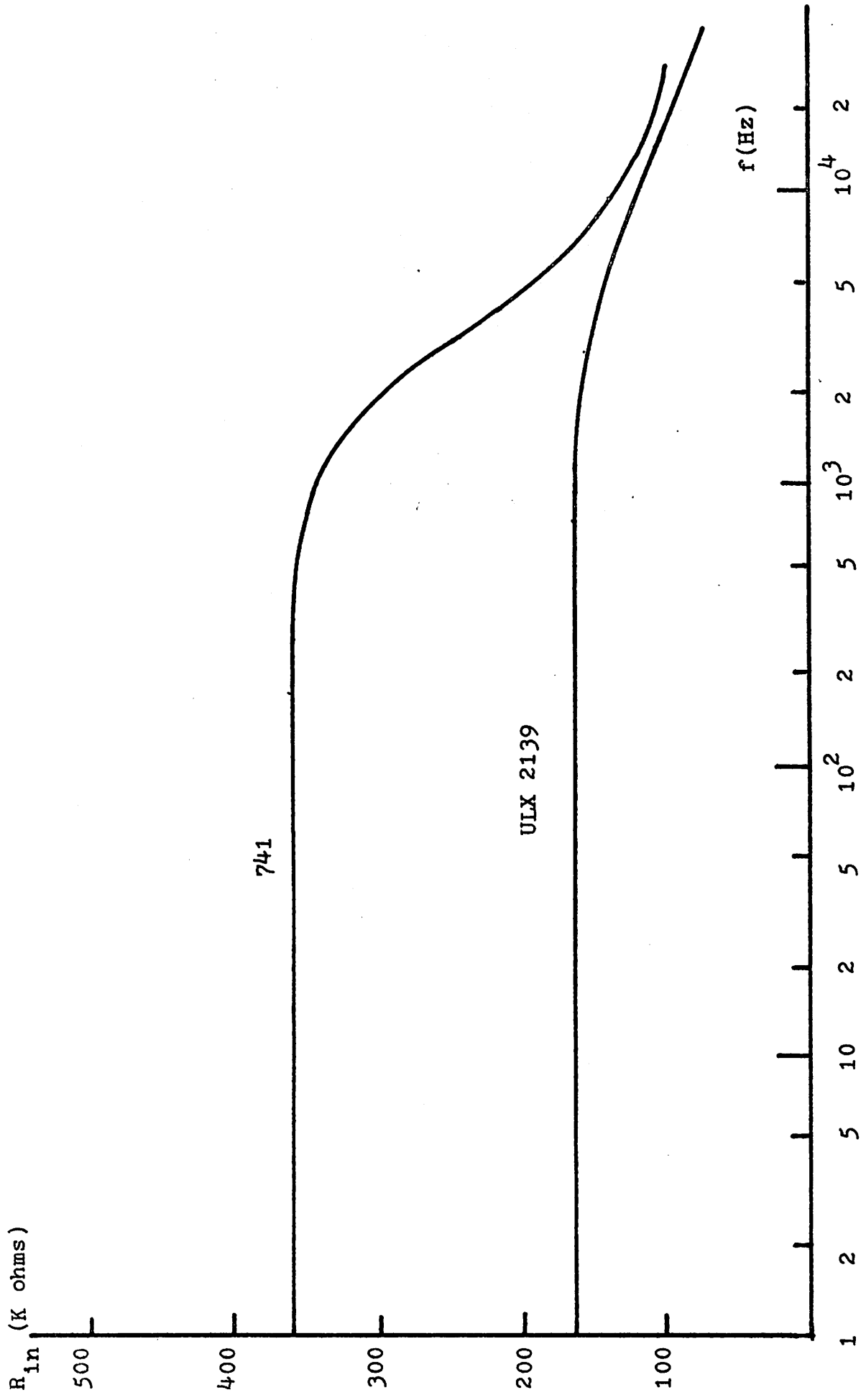


Fig. 4.11 Input resistance as function of frequency

CMR  
DE

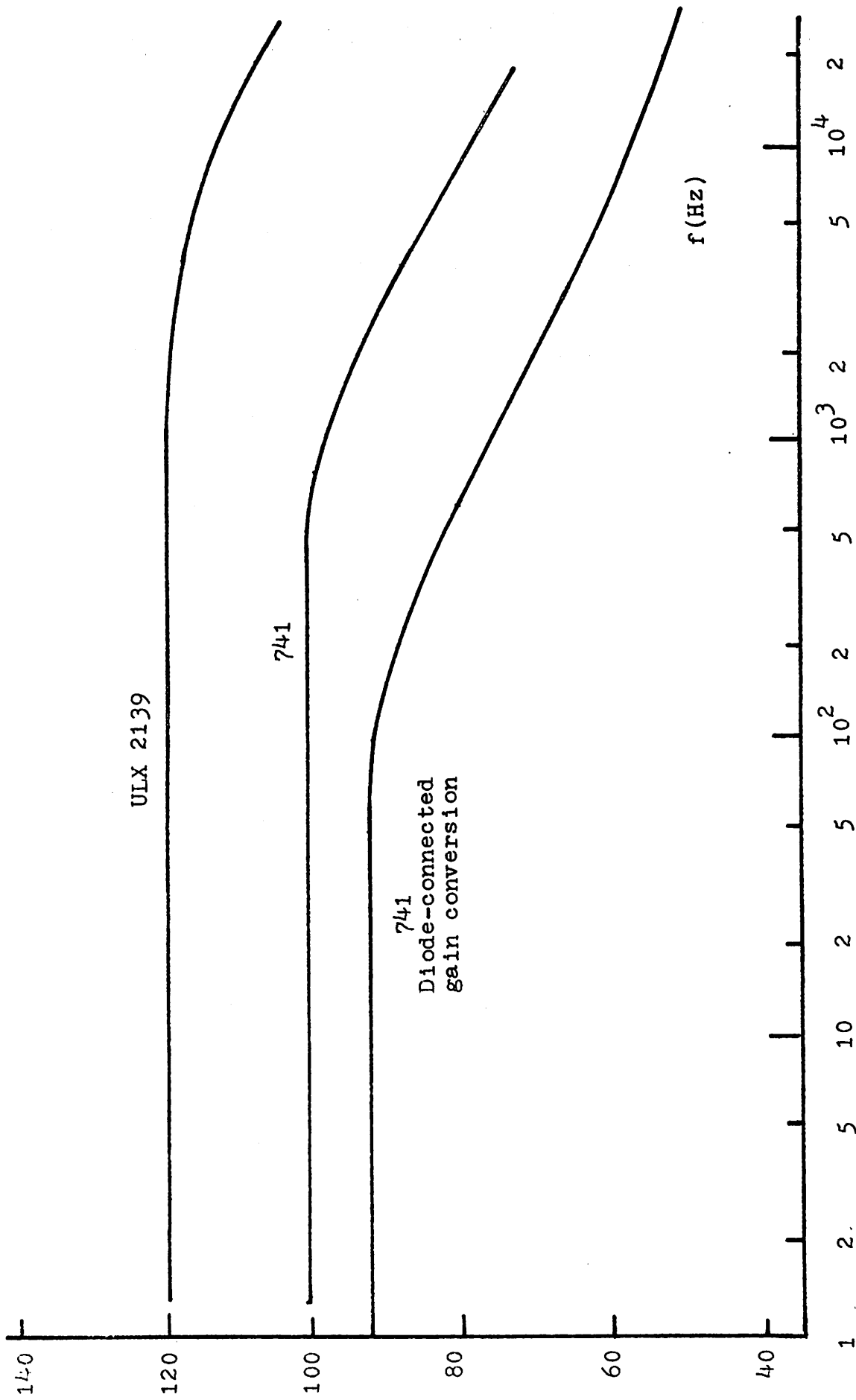


Fig. 4.12 Common mode rejection ratio as function of frequency

### 4.3 Large Signal Analysis

Large signal model parameters used in Time are obtained by the available data and both the output stages of the 741 and the ULX 2139 are analysed by Time, a transient analysis program. With large applied sinusoidal input voltage, distortion at high frequency is investigated and compared for both output stages. The amplitude of the input signal is 10 volts because higher applied voltage results in more severe distortion which is needed here for comparison. Phase shift is observed in Fig. 4.13 and 4.14 to occur at the output waveforms of both the 741 and the ULX 2139 at 1 M hz. The base substrate capacitance of the round lateral transistor  $Q_8$ , along with all other substrate capacitances associated with the npn transistors, in the ULX 2139 hold charge during the negative swing and thus the waveform is not symmetrical at 2 M hz as is shown in Fig. 4.13. The positive cycles of the 741 output waveform are distorted very seriously at 2 M hz. By removing all of the substrate capacitors shunting the collectors of the npn transistors to ground and the base of the lateral pnp transistor to ground, it is revealed by several Time runs that distortion, which occurs at frequency up to 5 M hz, is eliminated. Reduction of substrate capacitance might provide a partial solution to improving frequency performance of the output stage.

The symmetry of the large signal output waveform is worsened due to the presence of the Darlington pnp device in the ULX 2139 output stage. As a consequence output stages also pose problem in slew limiting when the amplifier is driven by high frequency, large signals.

#### Experimental Result

Output stages of both amplifiers, as illustrated in Fig. 4.15, are tested for large-signal frequency performance. Large voltage signals with amplitude of 1v, 2v, 5v and 7v<sup>10</sup> are applied at 1 M hz and 2 M hz to both output stages. In the case of the ULX 2139, output stage with Q<sub>8</sub> removed is also examined to ensure no distortion is caused by gain available at the output stage. With load open experimental results are obtained for both output stages and are shown in Fig. 4.16.

The output waveforms of the 741 - With an input of one volt no apparent distortion and phase shift are noticed at both 1 M hz and 2 M hz. With 2 volts applied, 8° of phase shift is noticed and the waveform is no longer symmetrical. With 5 volts applied, distortion and phase shift occur at both 1 M hz and 2 M hz. As is shown in Fig.4.16, severe distortion results as 7 volt input is applied to

---

<sup>10</sup> Ac signal generator with output of 10 volts p-p when loaded is not available. Since it is not critical to the evaluation of the output stages, measurement with V<sub>S</sub>=10v is not attempted.

to the output stage. Distortion appear at the positive cycles is mainly caused by the slow discharging action at the base of the substrate, double-emitter transistor,  $Q_{23A}$ , as the input swing positively. This situation has been predicted by the computer simulation.

The output waveforms of the ULX 2139 - With the same sequence of input voltages applied to the output stage of the ULX 2139, first significant distortion is spotted when 5-volt input is applied at a frequency of 2 M hz. The predicted distortion due to the base substrate capacitance of  $Q_8$  and all other substrate capacitance becomes more prominent at  $V_{s1} = 7$  volts and a frequency of 2 M hz.

The dead zone is eliminated in both output stages, as shown in Fig. 4.16, and there is no visible crossover distortion. The ULX 2139 manages to achieve good symmetry in the output stage by employing Darlington compound, substrate pnp device to compensate for its poor gain characteristic.

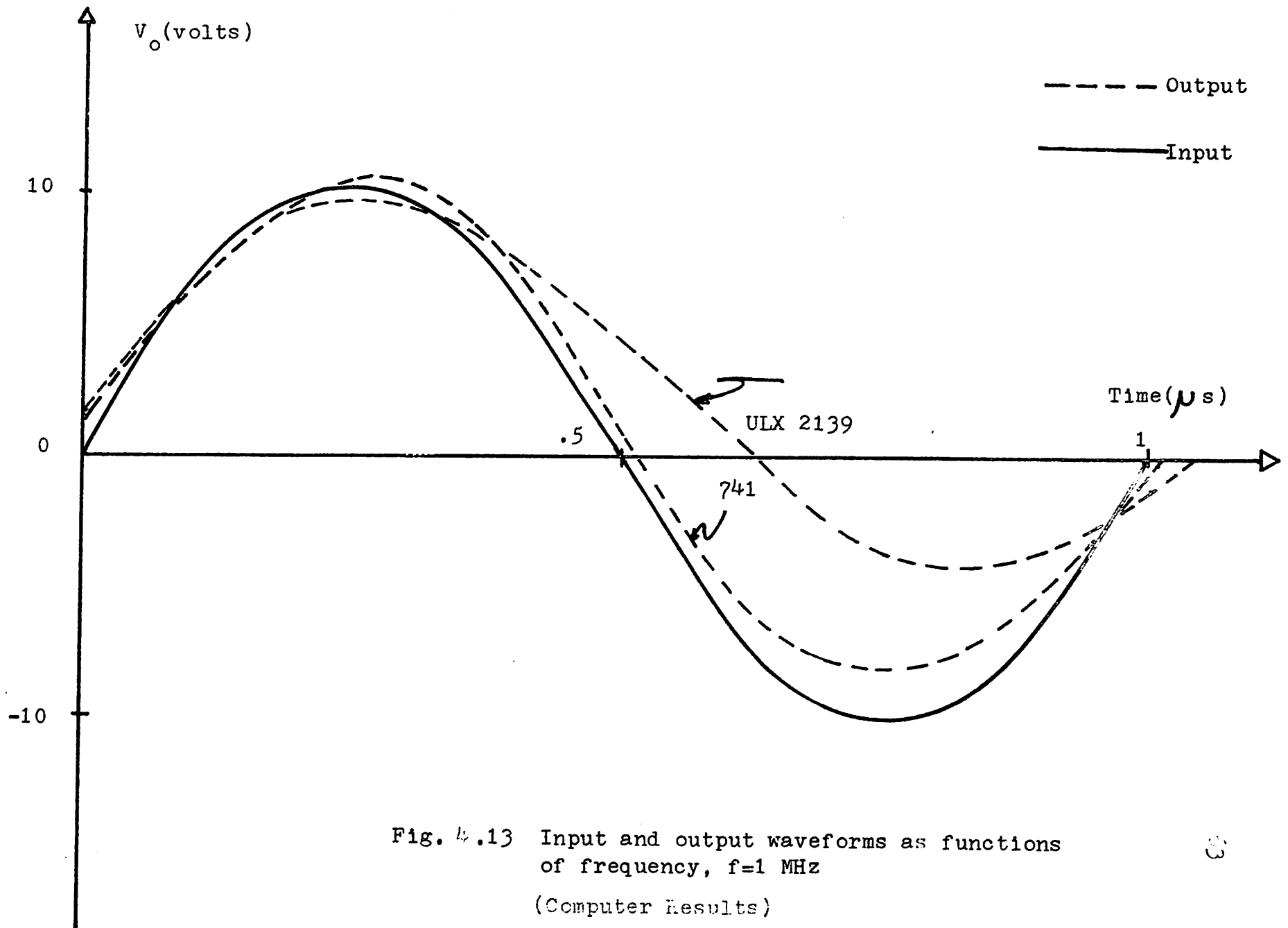


Fig. 4.13 Input and output waveforms as functions of frequency,  $f=1$  MHz  
(Computer Results)

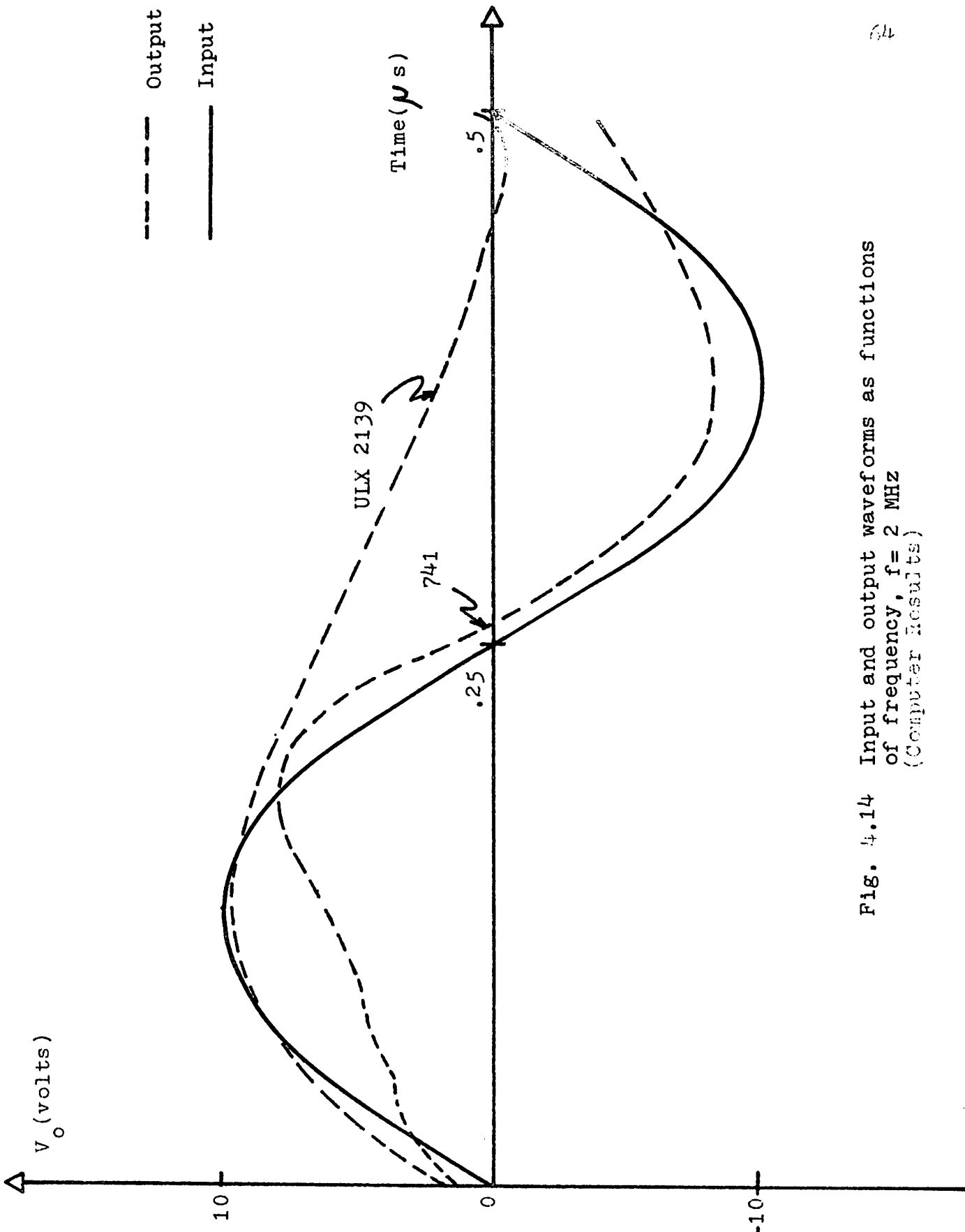
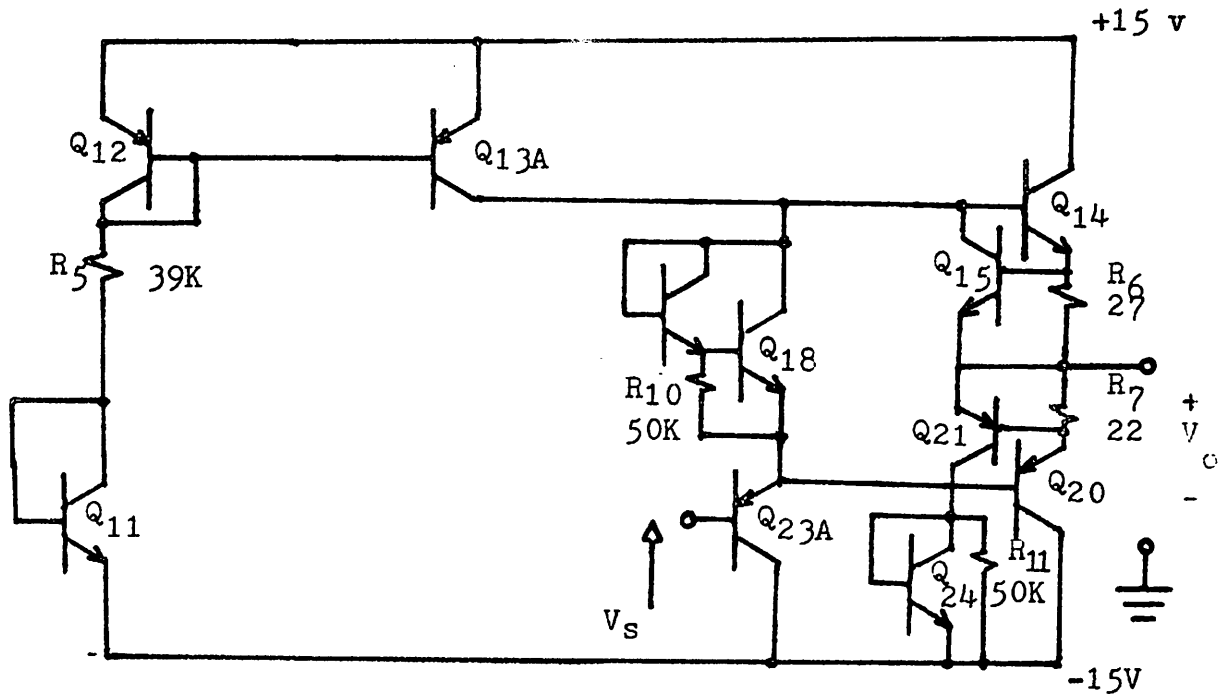
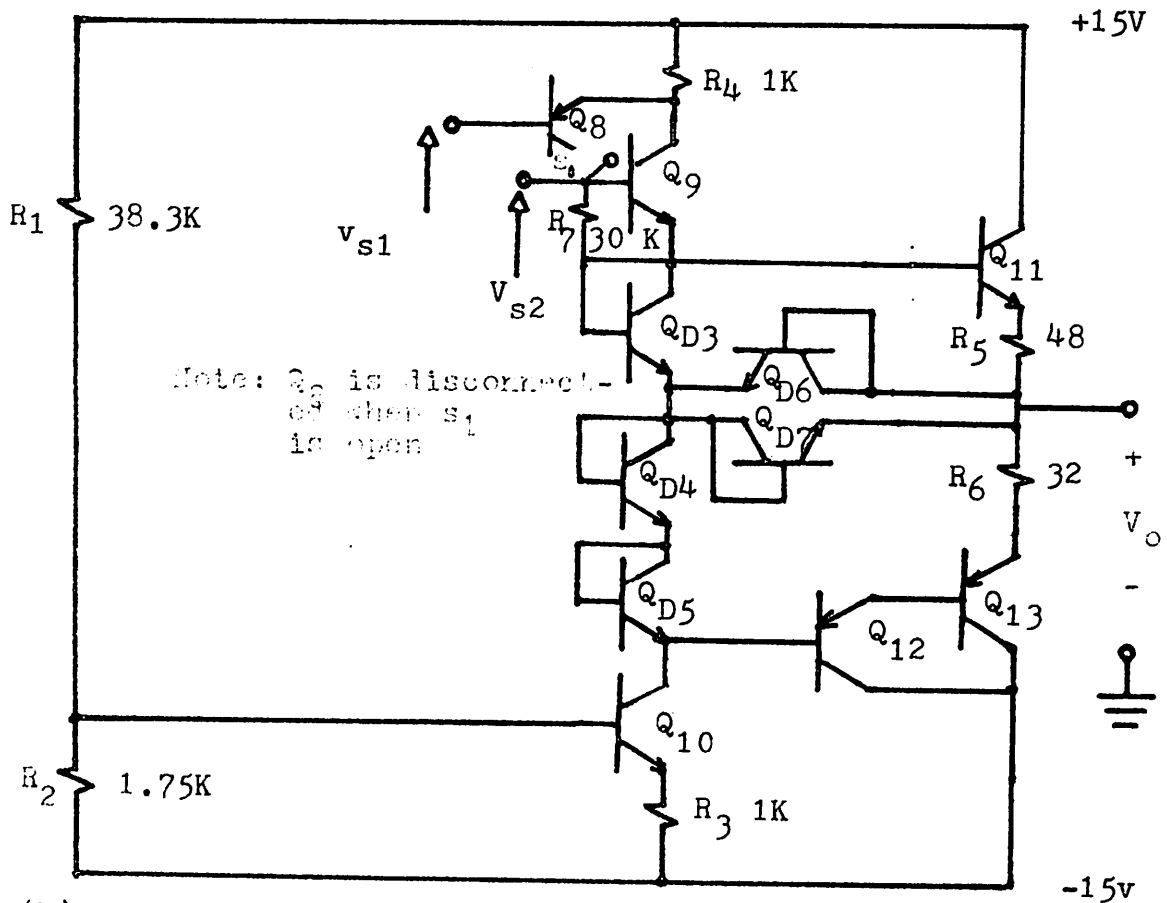


Fig. 4.14 Input and output waveforms as functions of frequency,  $f = 2$  MHz (Computer Results)





(a) 741 output stage

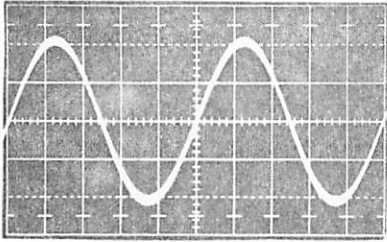


(b) ULX 2139 output stage ( $V_{s1}$ , signal applied when  $Q_8$  is included in the output stage;  $V_{s2}$ , when  $Q_8$  is disconnected as shown.)

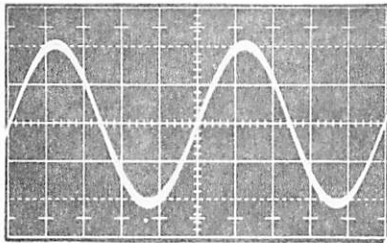
Fig. 15 Output stages

f=1M hz

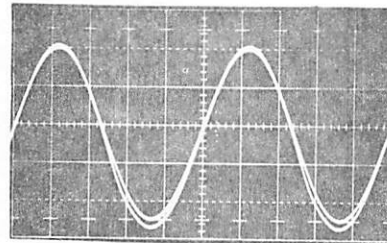
$V_S=1v$



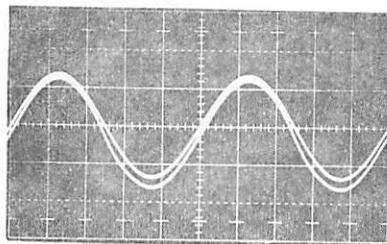
$V_S=2v$



$V_S=5v$

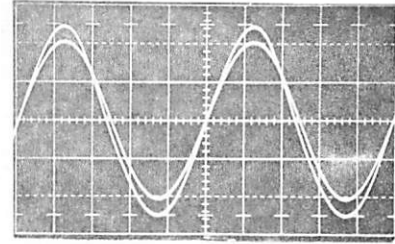


$V_S=7v$

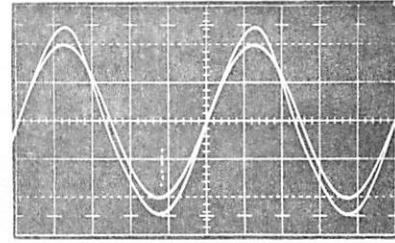


f=2M hz

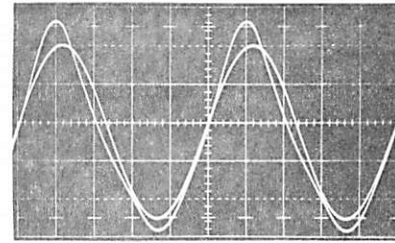
$V_S=1v$



$V_S=2v$



$V_S=5v$



$V_S=7v$

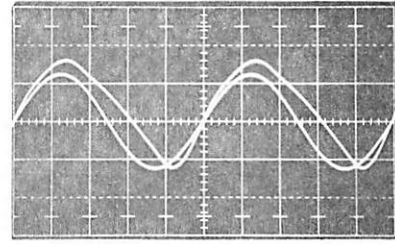
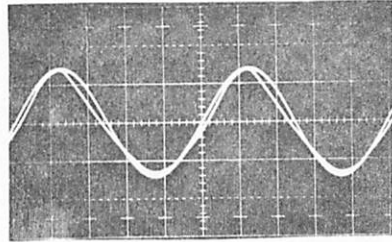


Fig. 4.16 Input and output waveforms of output stage of the ULX 2139

$f=1\text{M hz}$

$V_s=7\text{v}$



$f=2\text{M hz}$

$V_s=7\text{v}$

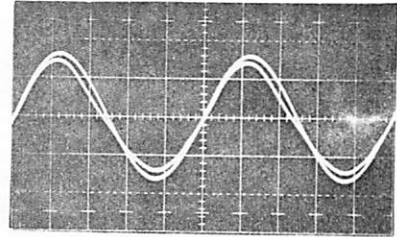


Fig. 4.16(continued) Input and output waveforms  
of output stage the the ULX 2139  
with  $Q_8$  removed

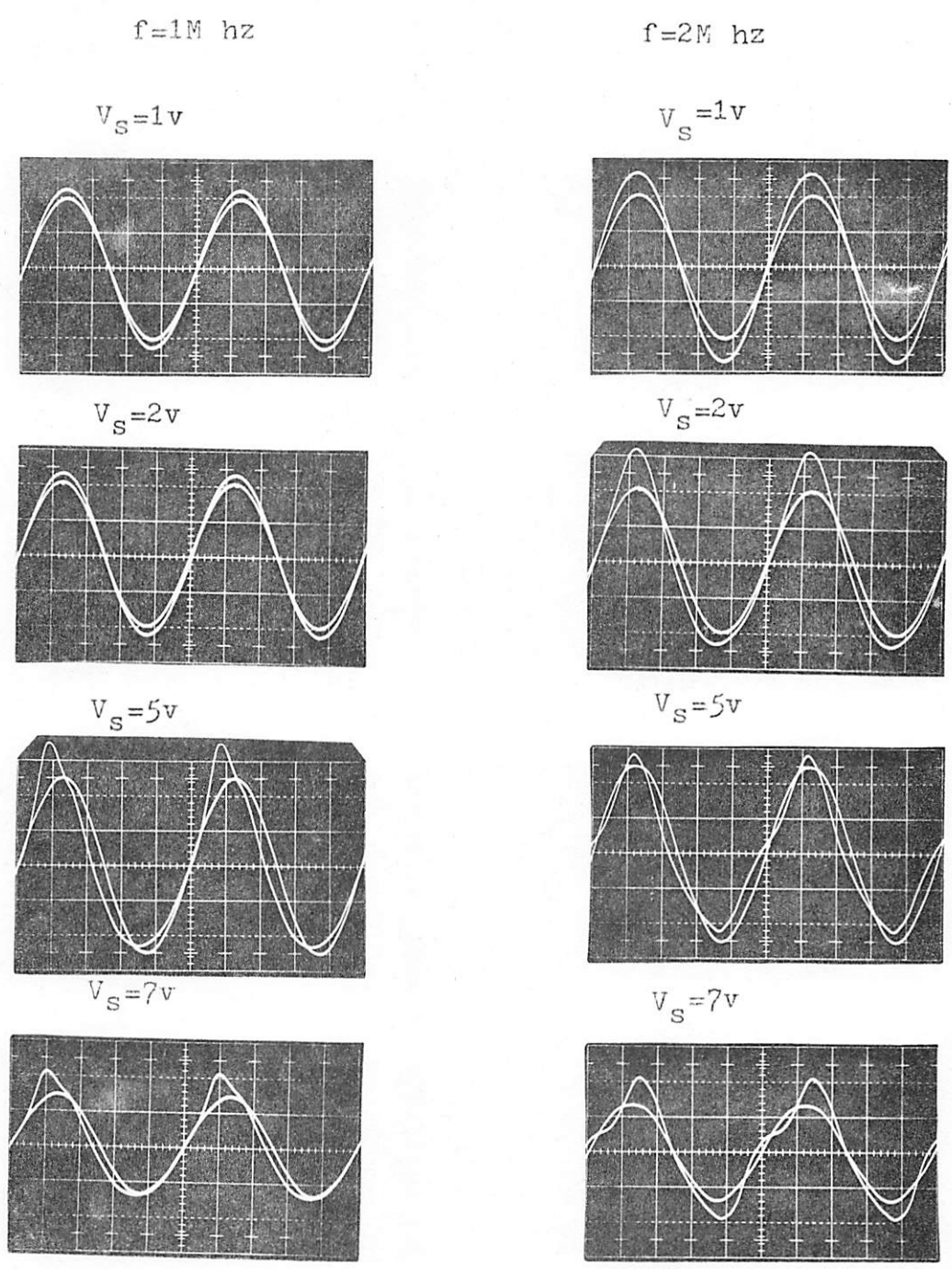


Fig. 4.16(continued) Input and output waveforms of output stage of the 741

### Summary

By using Miller-effect compensation, a phase margin of  $61^\circ$  is achieved in the 741. This cannot be achieved by the ULX 2139 regardless of the amount of capacitance that is being used externally for compensation. A phase margin of  $24^\circ$  in the phase response will result in considerable peaking in voltage gain versus frequency curve as has been brought out in the Manufacturer's application note. Improvement on phase margin is feasible if pnp technology is improved.

The biasing levels in the 741 can be made insensitive to voltage supply either by use of temperature insensitive regulator or current source with better desensitization design. The slew rate of the 741, which is considerably less than that of the ULX 2139, could have been improved should the current, which charges up the compensating capacitor when large input signal is applied, is not so badly restricted by the extremely low collector quiescent current of the input stage.

Frequency performance does not seem to be improved significantly in both cases by simply improving the pnp technology; it is observed to be ultimately limited by the output stage.

## Appendix A

Circle in Complex Impedance Plane Technique in Measuring Base Resistance

The input impedance of a bipolar transistor can be simply characterized as  $r_x$  in series with parallel  $C_{\pi}$  and  $r_{\pi}$  as shown in Fig. A.1.

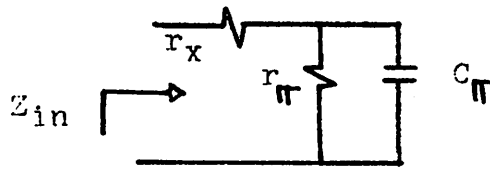


Fig. A.1

$$Z_{in} = \left( r_x + \frac{r_{\pi}}{1 + \omega^2 C_{\pi}^2 r_{\pi}^2} \right) - j \left( \frac{\omega C_{\pi} r_{\pi}^2}{1 + \omega^2 C_{\pi}^2 r_{\pi}^2} \right) \quad A.1$$

The measured impedance with a low frequency Wayne-Kerr Bridge is given as resistance in parallel with capacitance as is given in Fig. A.2.

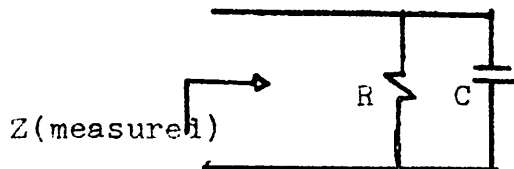


Fig. A.2

$$Z_{(measured)} = \left( \frac{R}{1 + \omega^2 C^2 R^2} \right) - j \left( \frac{\omega C R^2}{1 + \omega^2 C^2 R^2} \right) \quad A.2$$

$$= \text{Re}Z - j\text{Im}Z$$

By plotting  $\text{Re}Z$  versus  $\text{Im}Z$  with  $\omega$  as a running parameter a typical circle is obtained with radius  $\frac{1}{2}r_{\pi}$ , and horizontal intersections at  $\text{Re}Z = r_x$  and  $r_x + \frac{1}{2}r_{\pi}$ , as is shown in Fig. A.3.

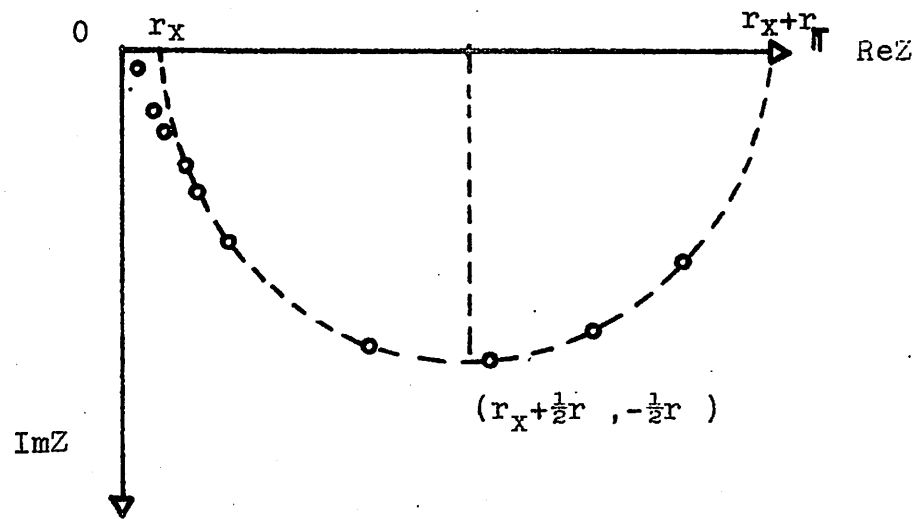


Fig. A.3

For the point  $w = C_{\pi} r_{\pi}$ , equation A.1 becomes

$$Z_{in} = (r_x + \frac{1}{2} r_{\pi}) - j(\frac{1}{2} r_{\pi}) \text{ which is in the locus of equation A.1.}$$

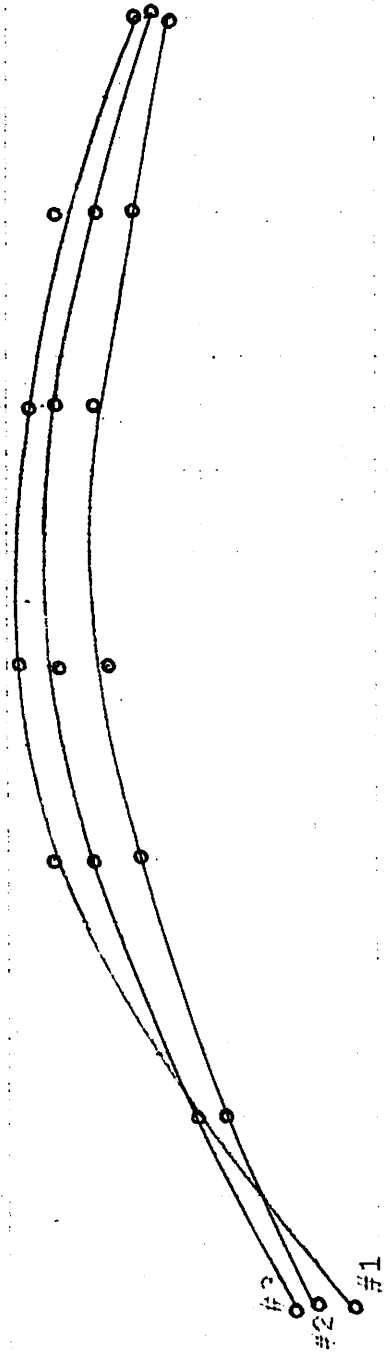
## Appendix B

Device Data for the 741Table of Contents

- (1) Dc current gain versus collector current..... Fig.B.1-Fig.B.4
- (2) Small signal current gain versus frequency... Fig.B.5-Fig.B.8
- (3) Unity gain frequency versus collector  
current ..... Fig.B.9-Fig.B.12
- (4) Capacitance versus reverse bias voltage ..... Fig.B.13-Fig.B.22



Small NPN #1

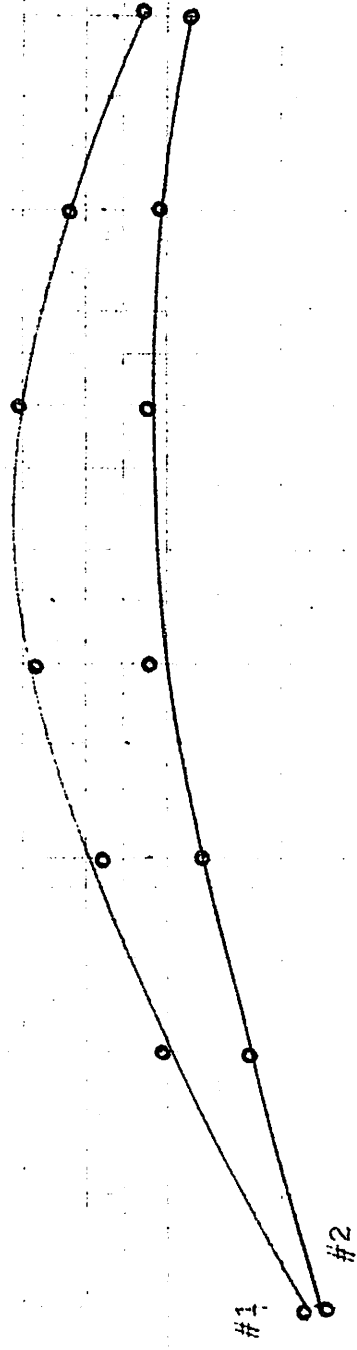


$\beta$  vs  $I_c$

$I_c$  (ma)

Fig. B.1

Large NPN



$\beta$  vs  $I_C$

$I_C$  (ma)

Fig. B.2

100 10 1 0.1

$\beta_o$   
100

#1

#2

#3

Small PNP

$\beta$  vs  $I_c$

$I_c$  (ma)

1.0

0.1

Fig. B.3

10

Large PNP

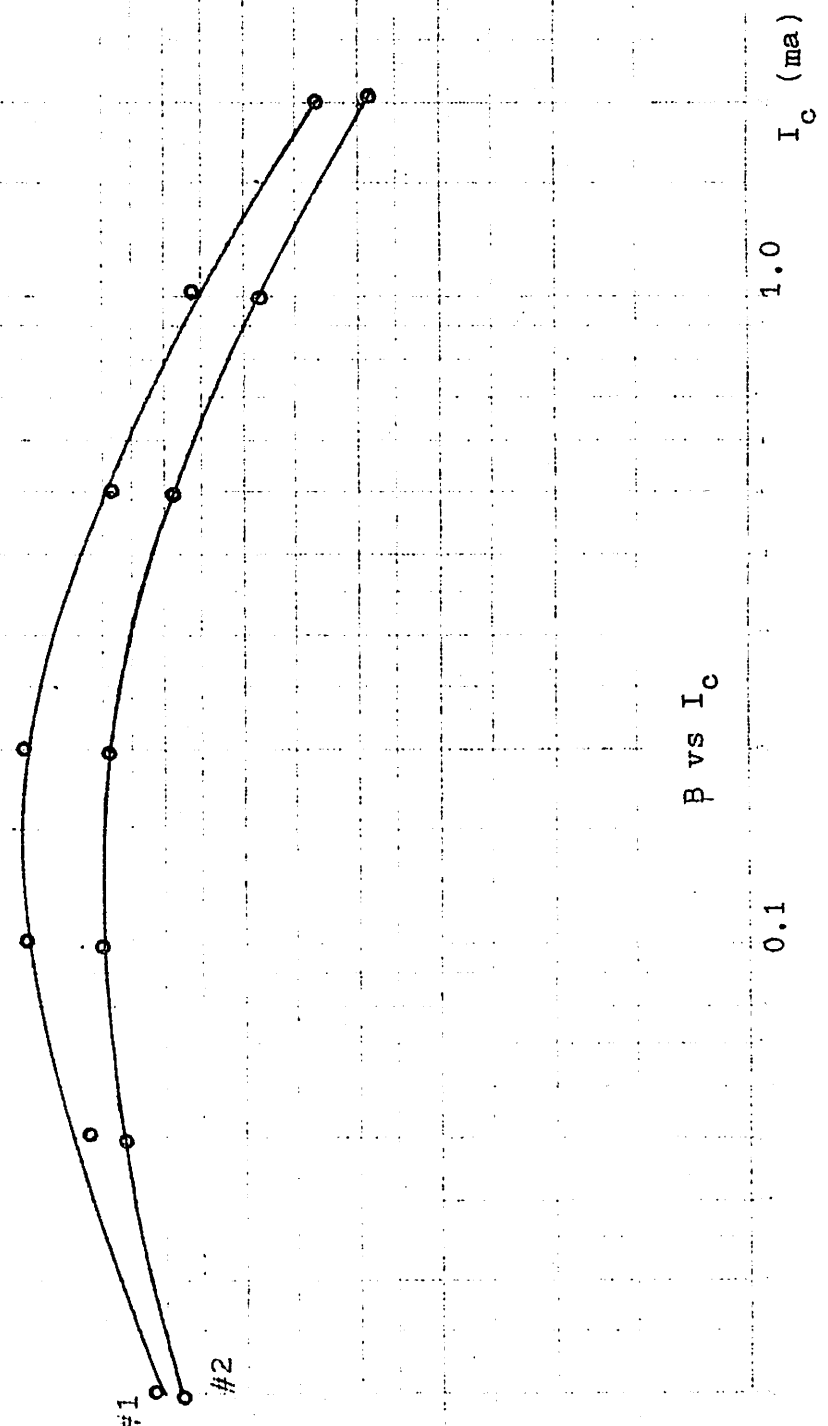
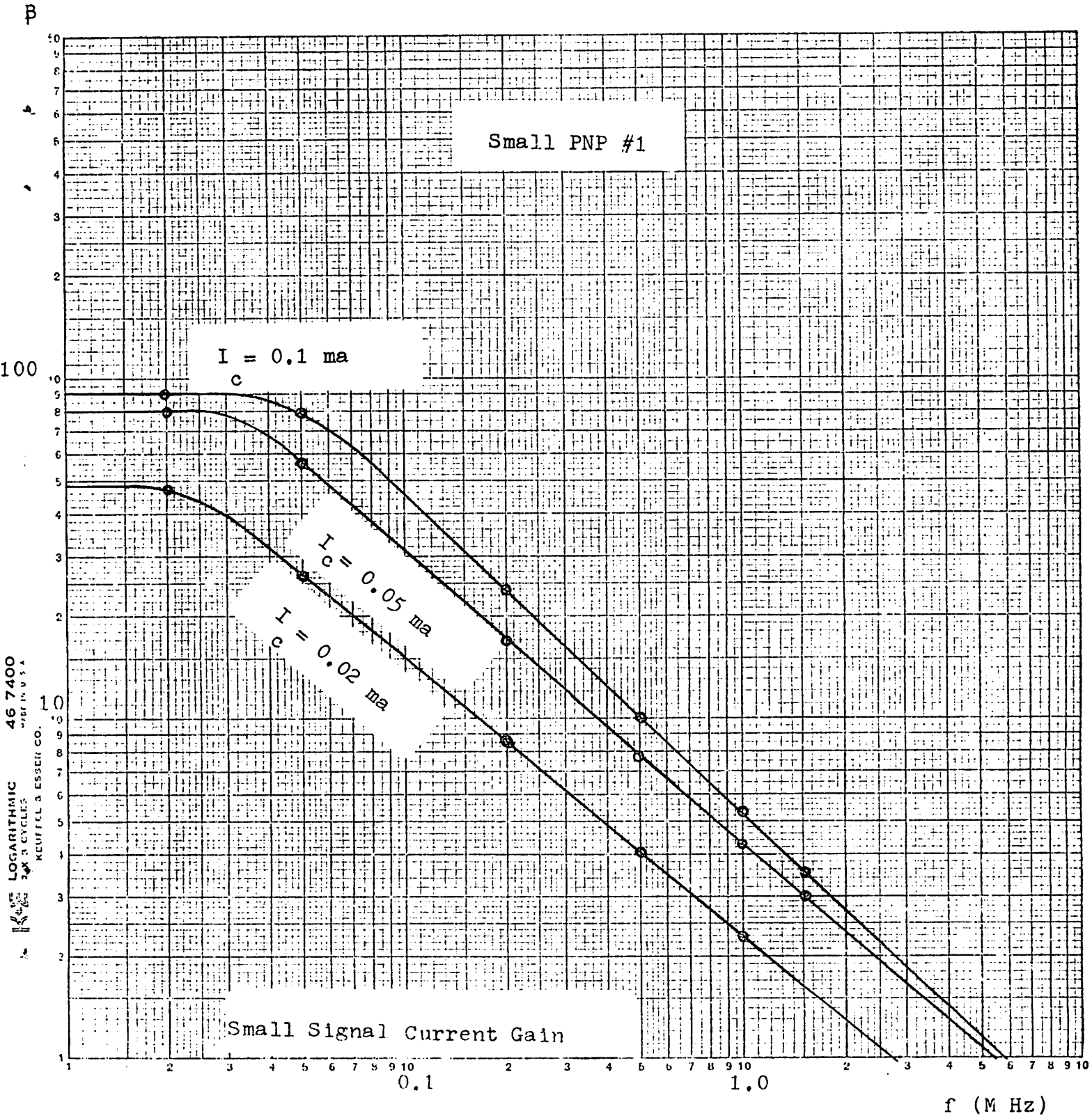


Fig. B.4



46 7400  
 LOGARITHMIC  
 KEUFFEL & ESSER CO.

Fig. B.5

P

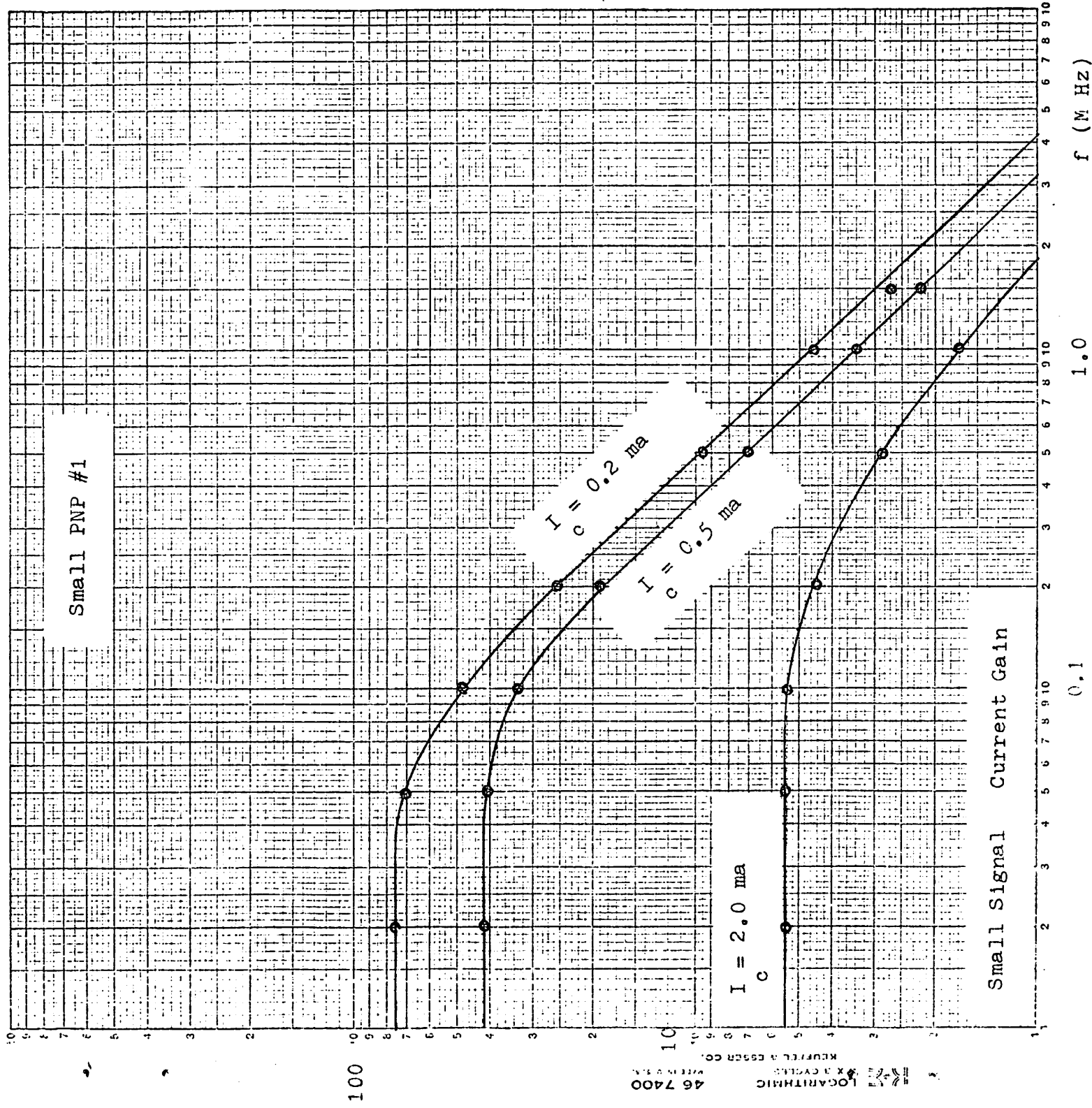


Fig. B.6

46 7400  
LOGARITHMIC  
3 X 5 CYCLES  
NEUFULL & ESSER CO.

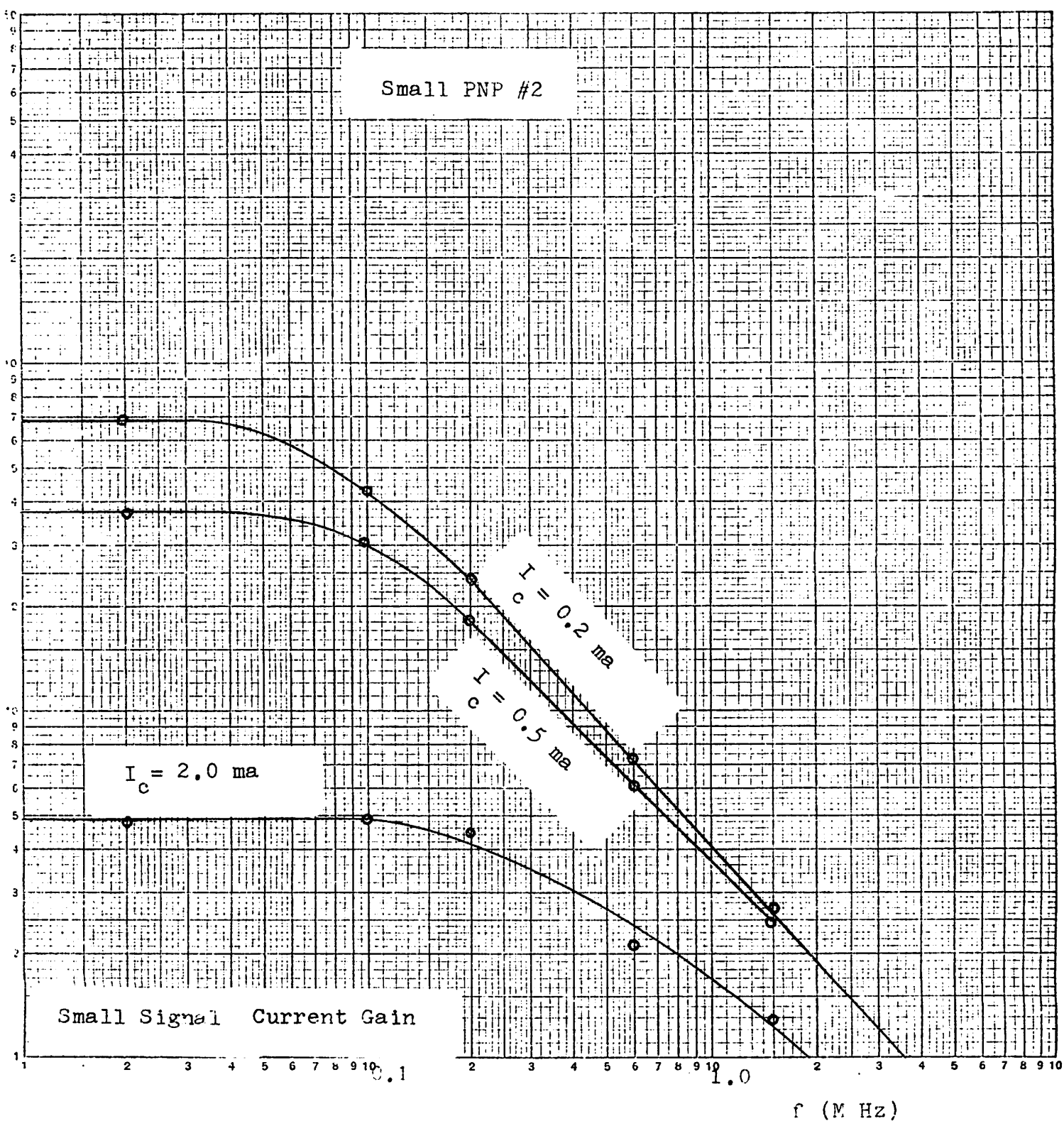


Fig. B.7

Small Signal Current Gain

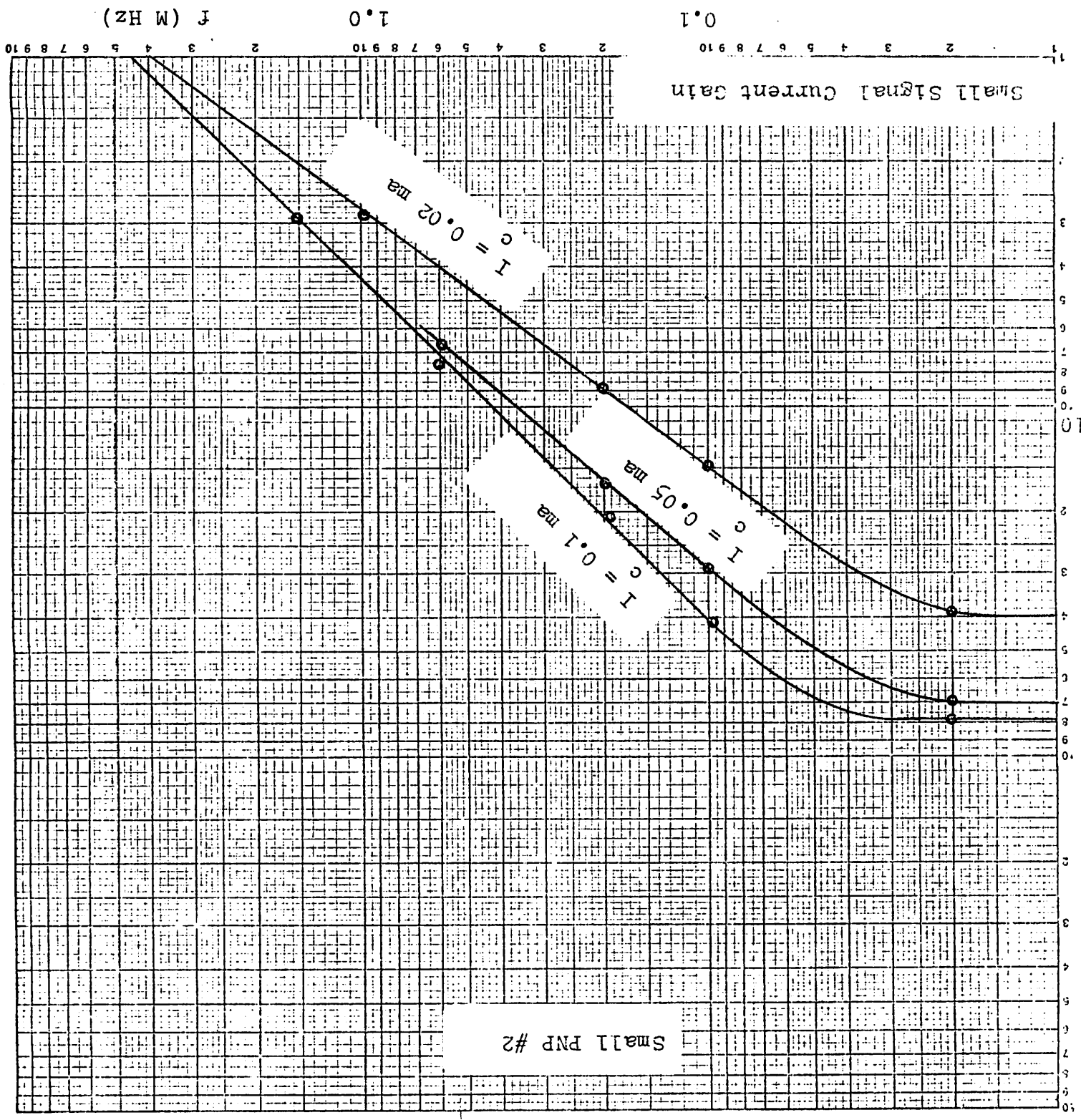


FIG. B.8



$f_T$  (M HZ)

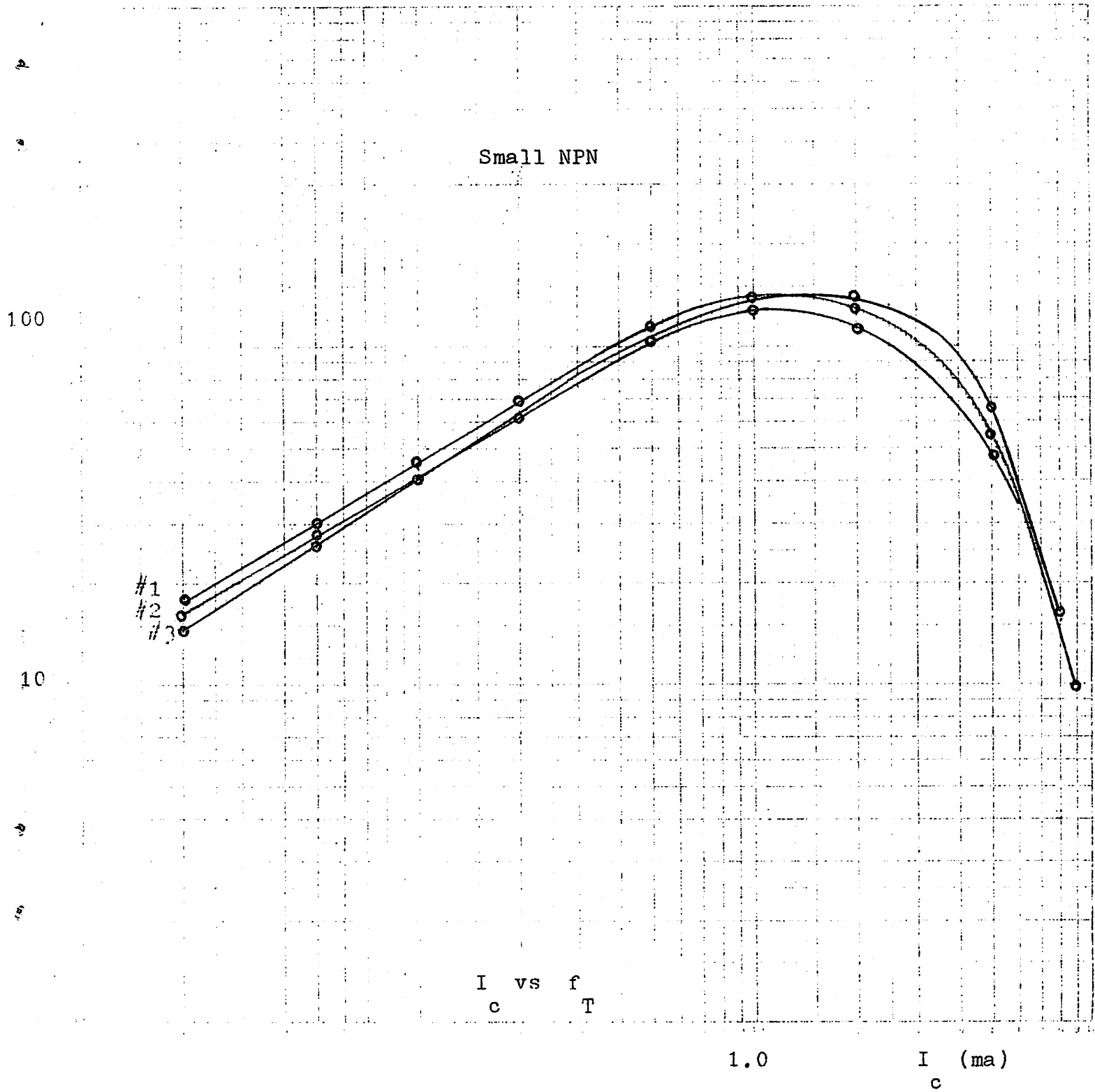


Fig. B.9

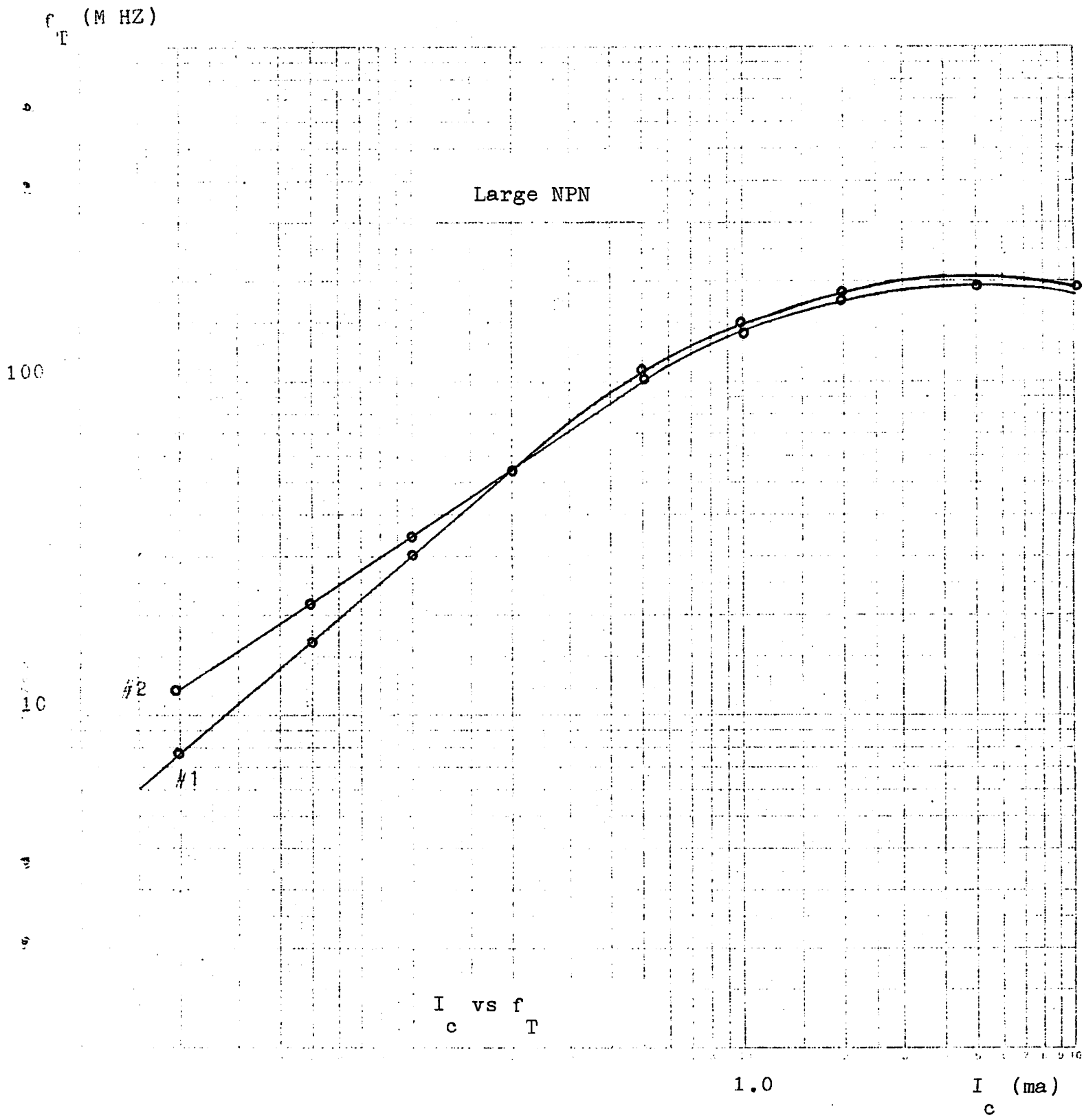


Fig. B.10

$f_T$  (M Hz)

Small PNP

#1

#2

$I_c$  vs  $f_T$

0.1

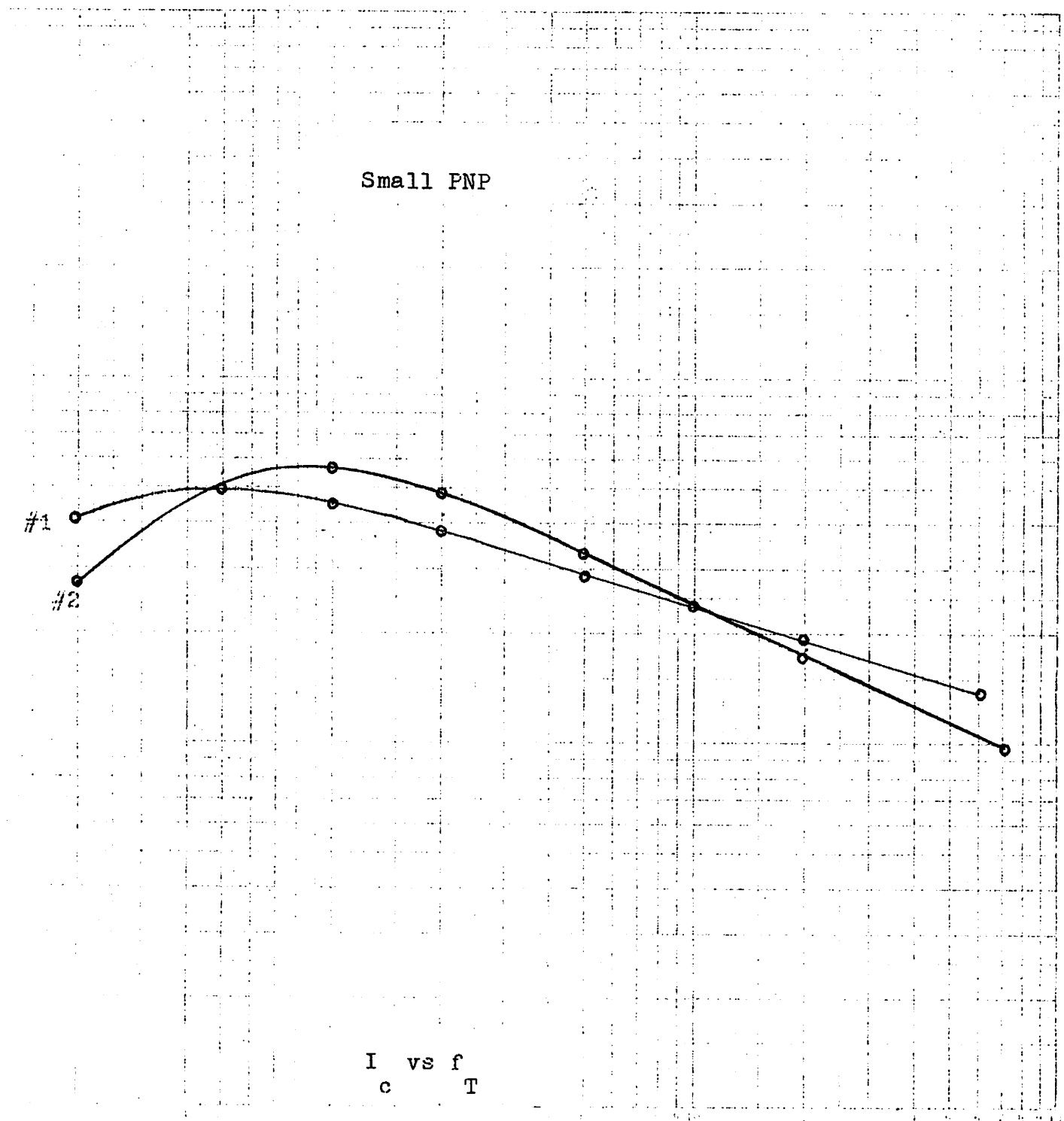
1.0

$I_c$  (ma)

10.0

1.0

Fig. B.11



$f_T$  (M HZ)

10

Large PNP

#2

#1

$I_c$  vs  $f_T$

1.0

$I_c$  (ma)

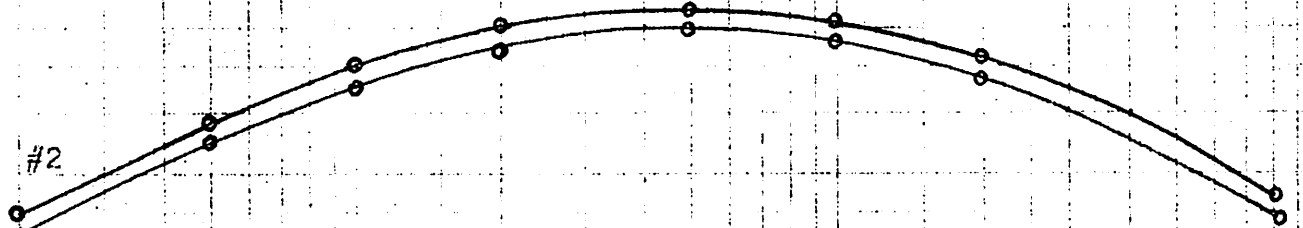


Fig. B.12

Capacitance (pf)

Small NPN #1

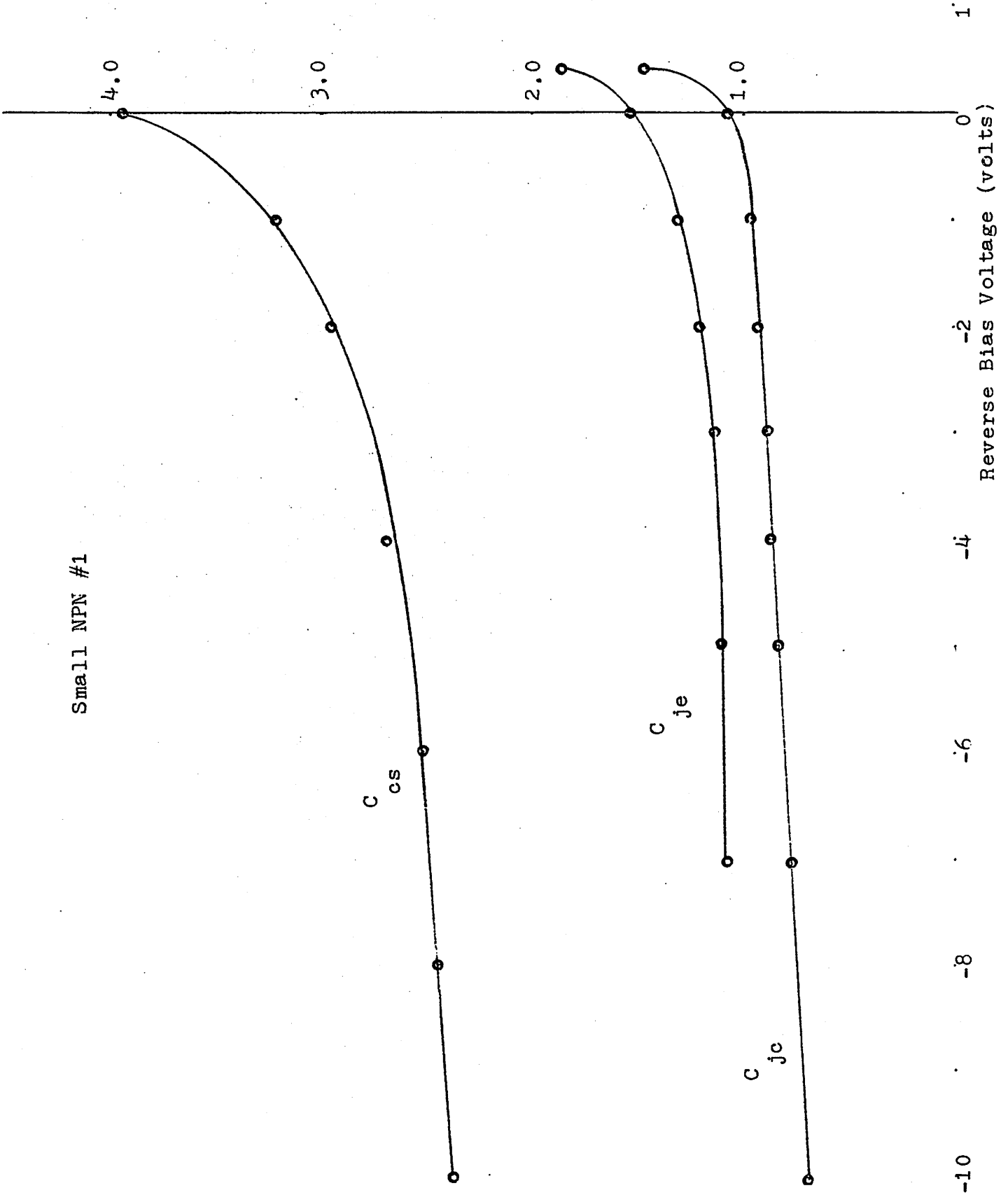


Fig. B 13

Capacitance (pf)

Small NPN #2

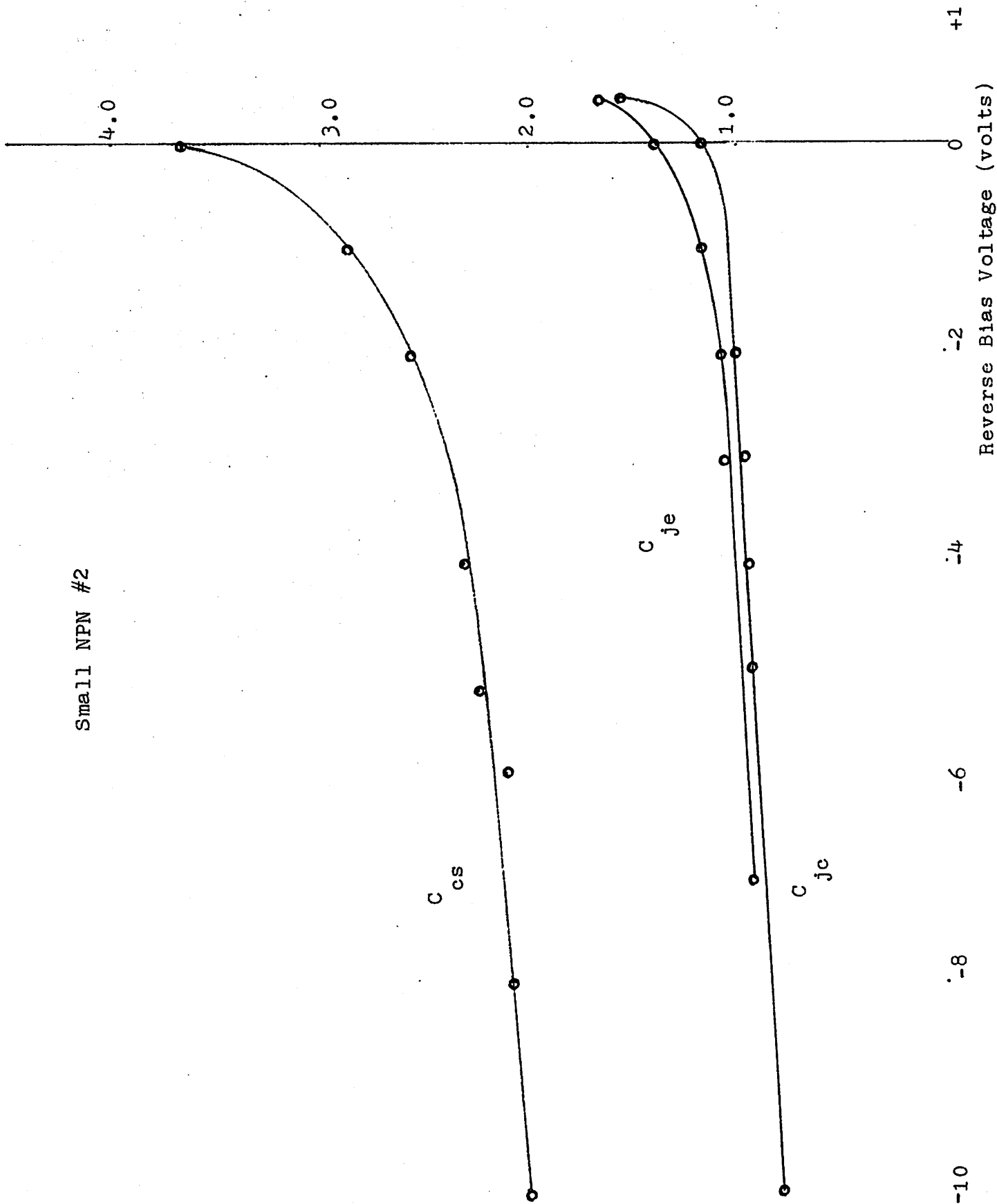


Fig. B.14

Capacitance (pf)

Small NPN #3

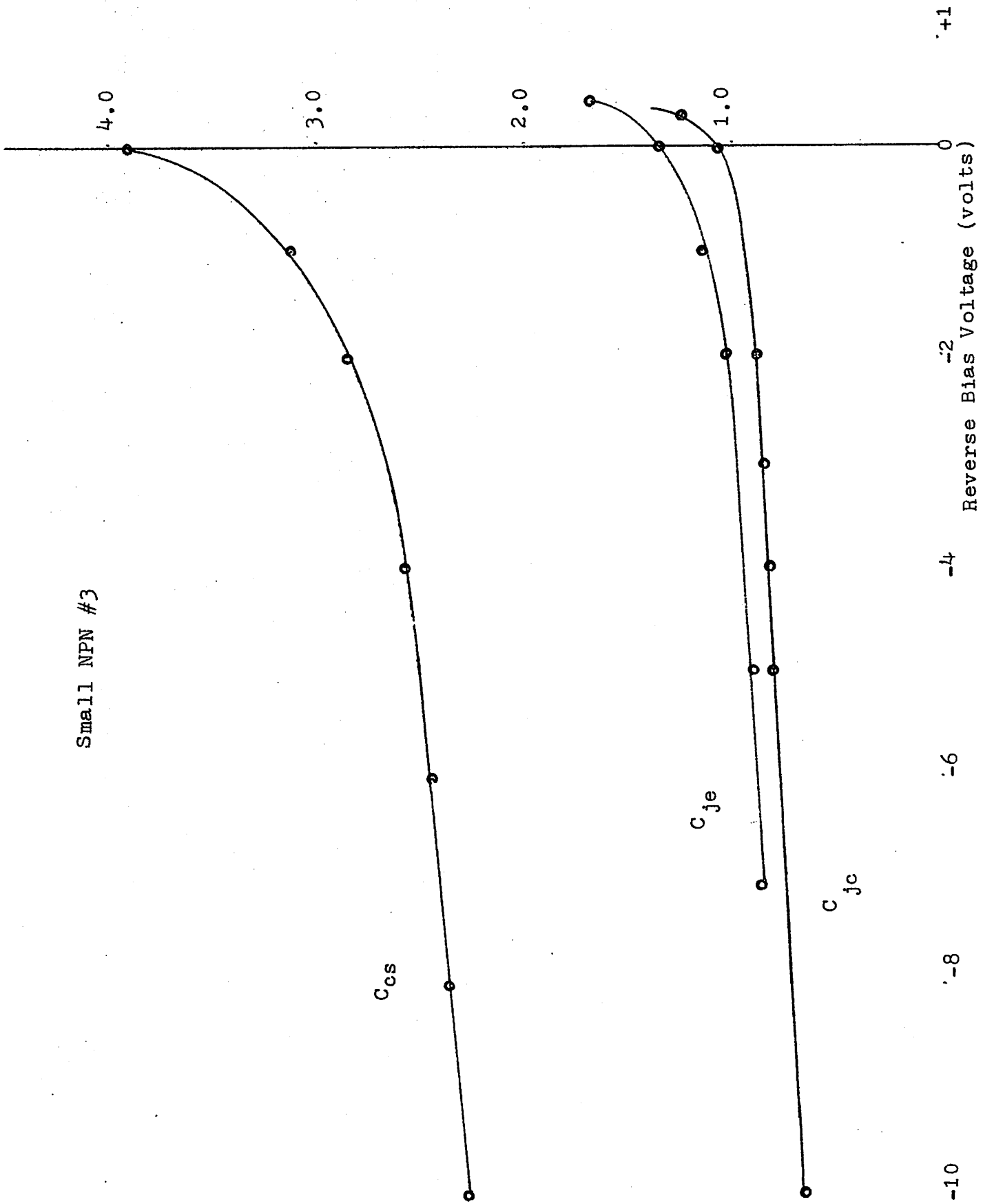


Fig. B.15

Capacitance (pf)

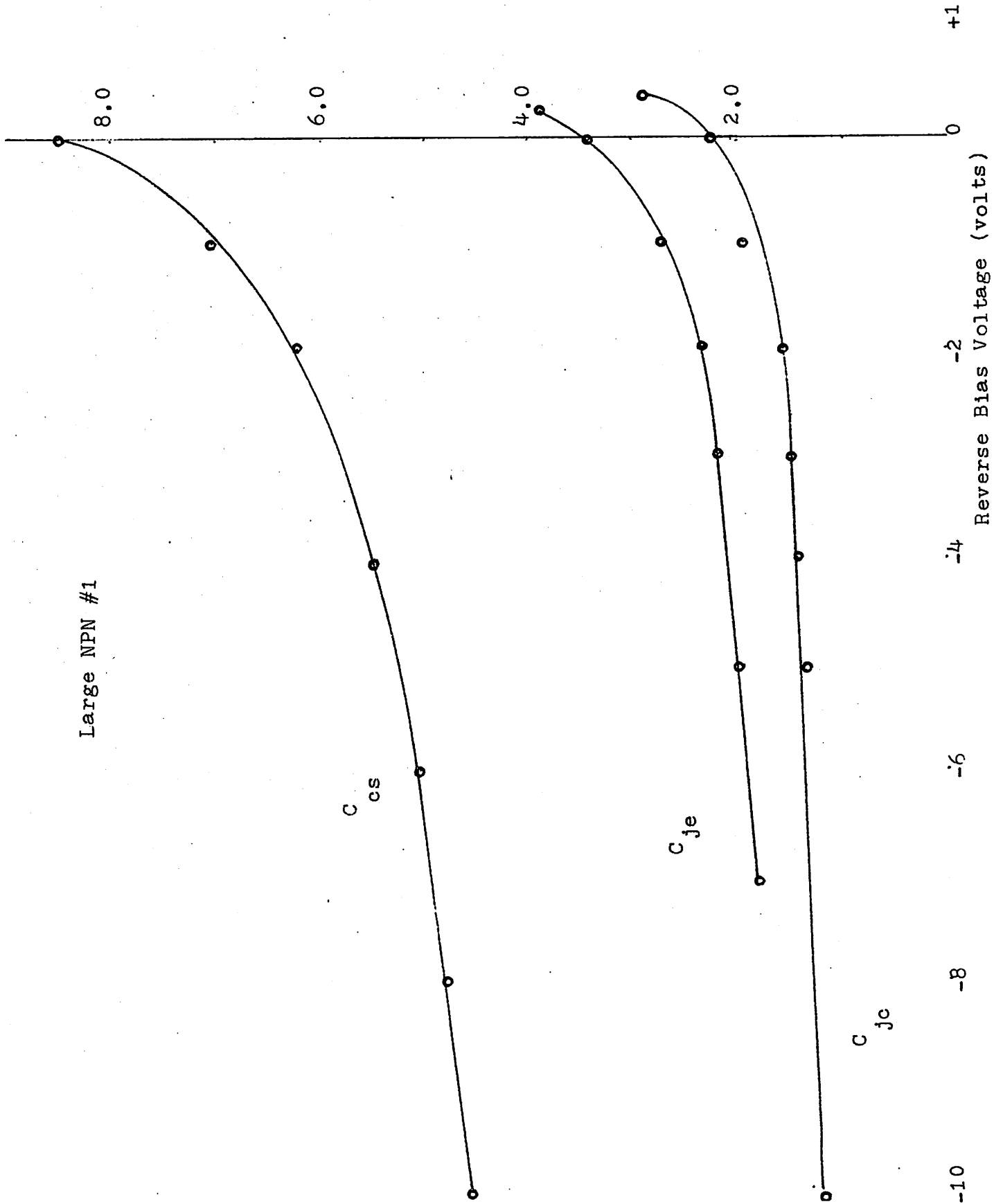


Fig. R 16



Capacitance (pf)

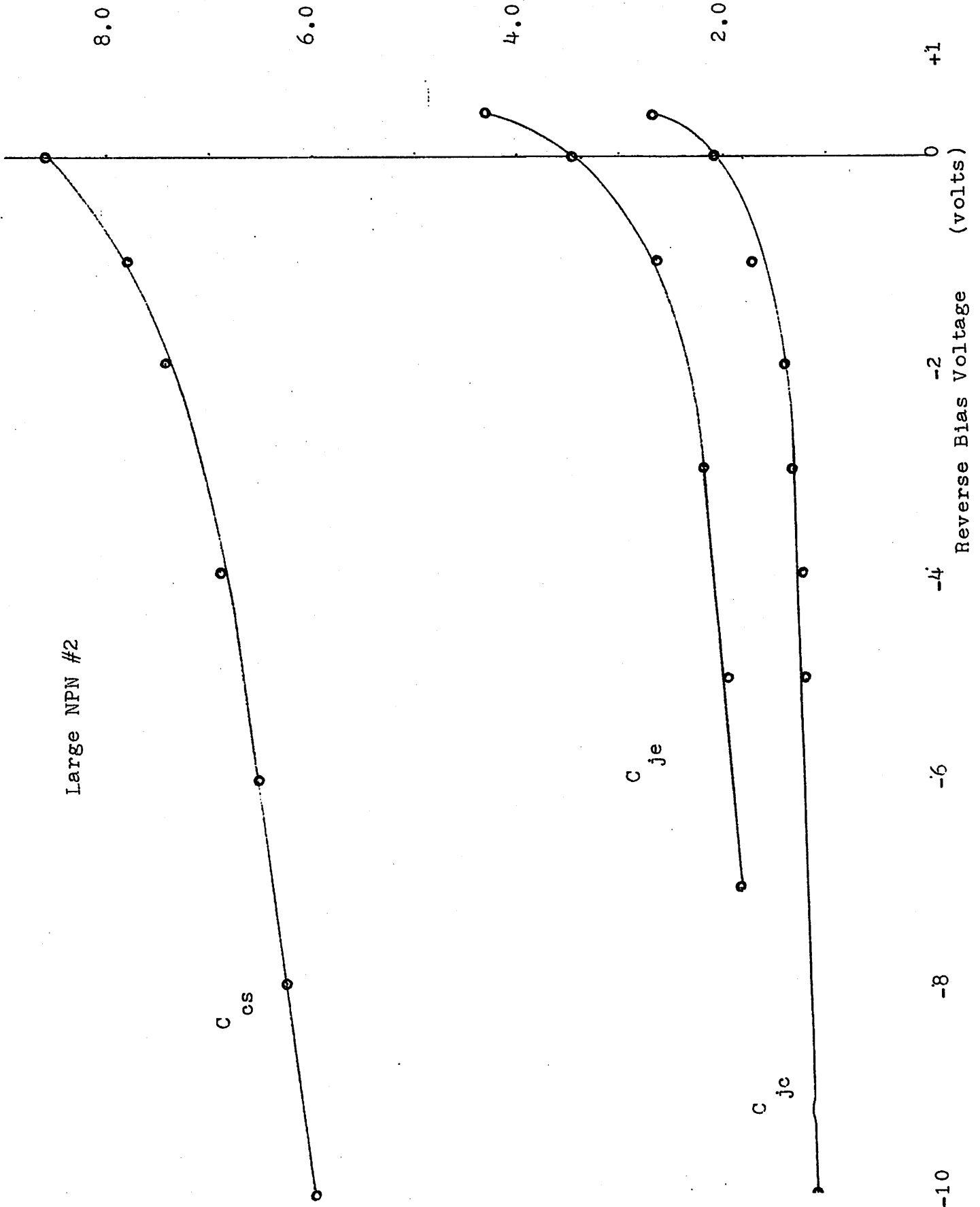


Fig. B.12

Capacitance (pf)

Small PNP #1

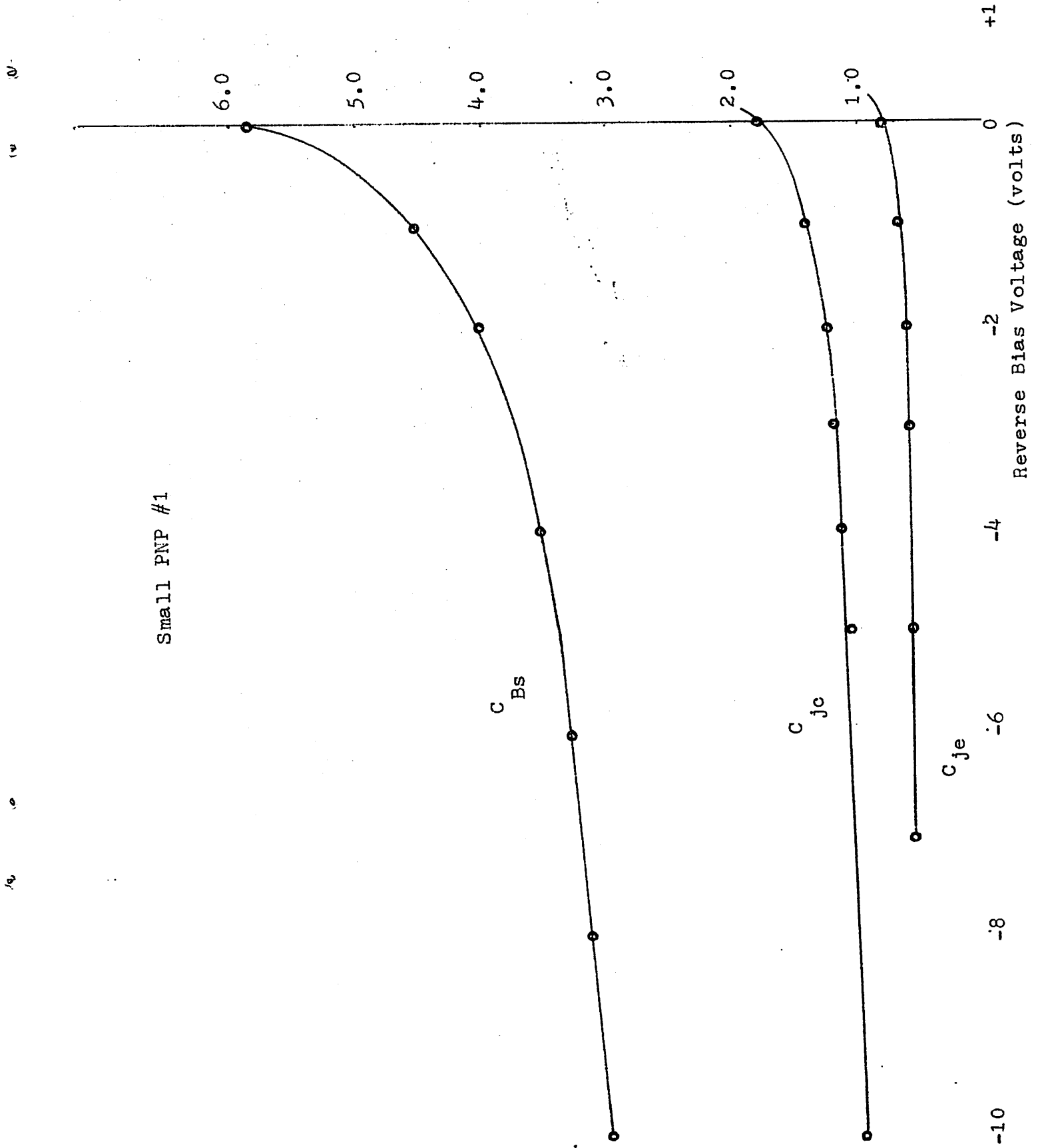


Fig. B.18

Capacitance (pf)

Small PNP #2

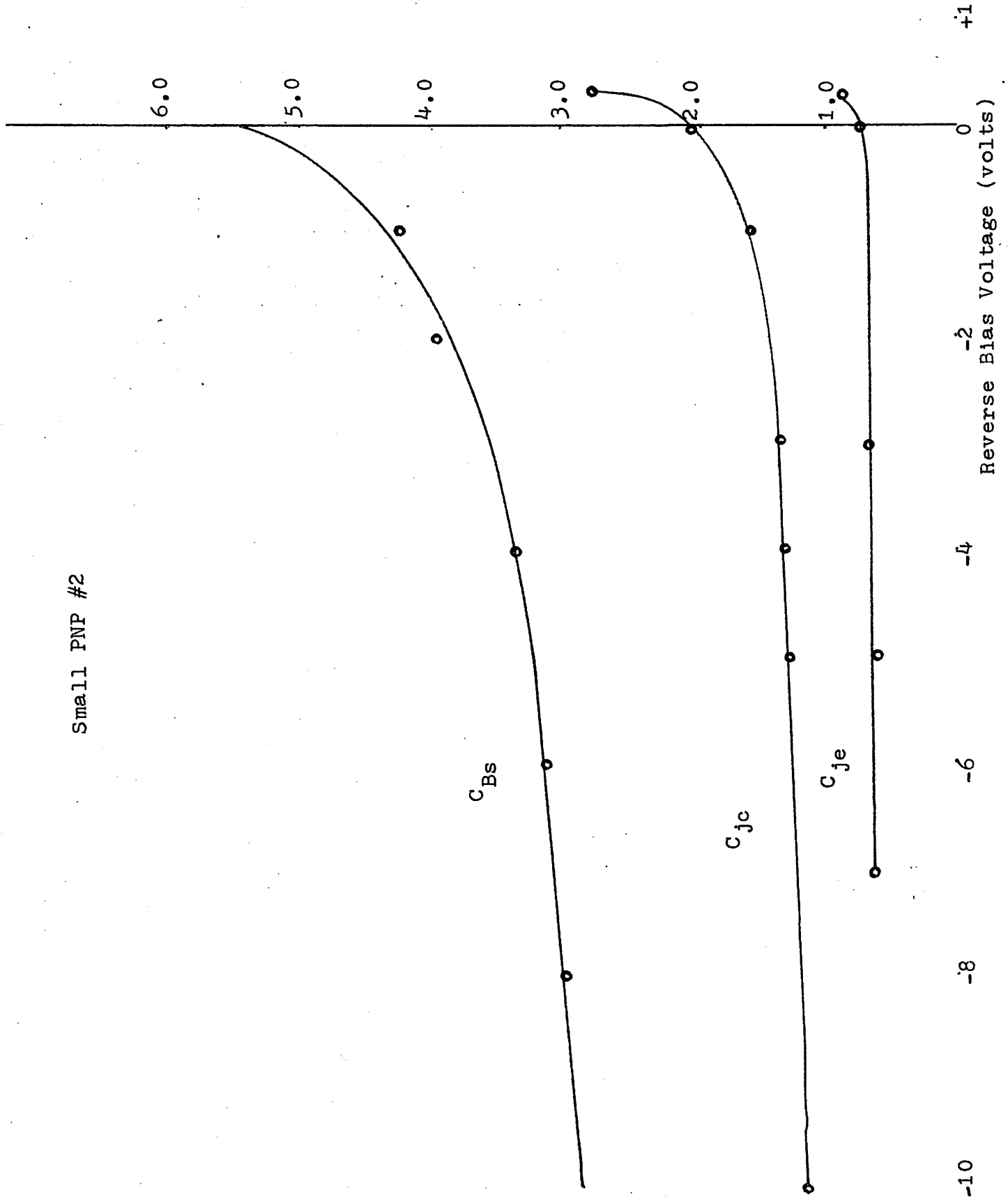


Fig. B.19

Capacitance (pf)

Small PNP #3

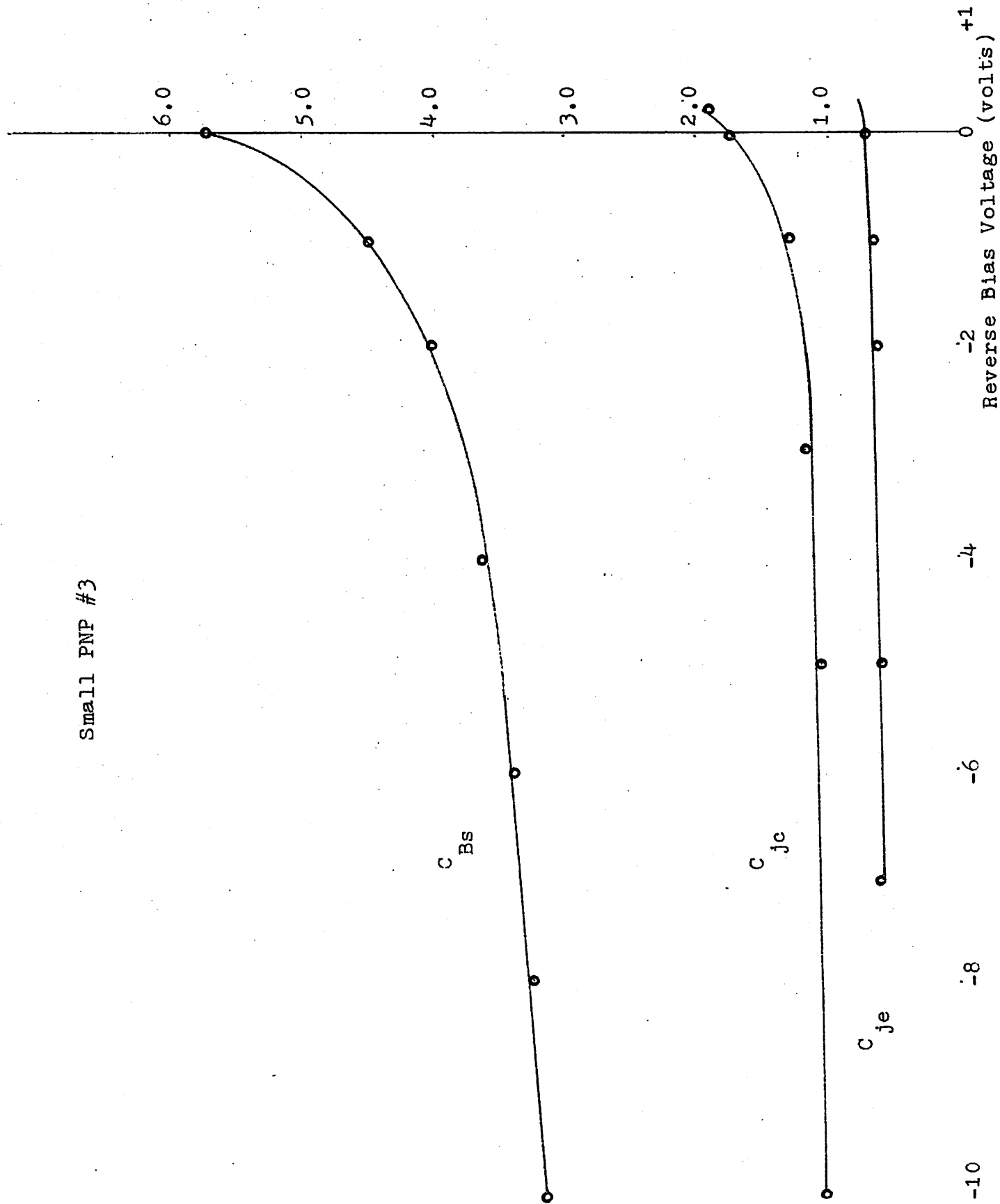


Fig. B.20

Capacitance (pf)

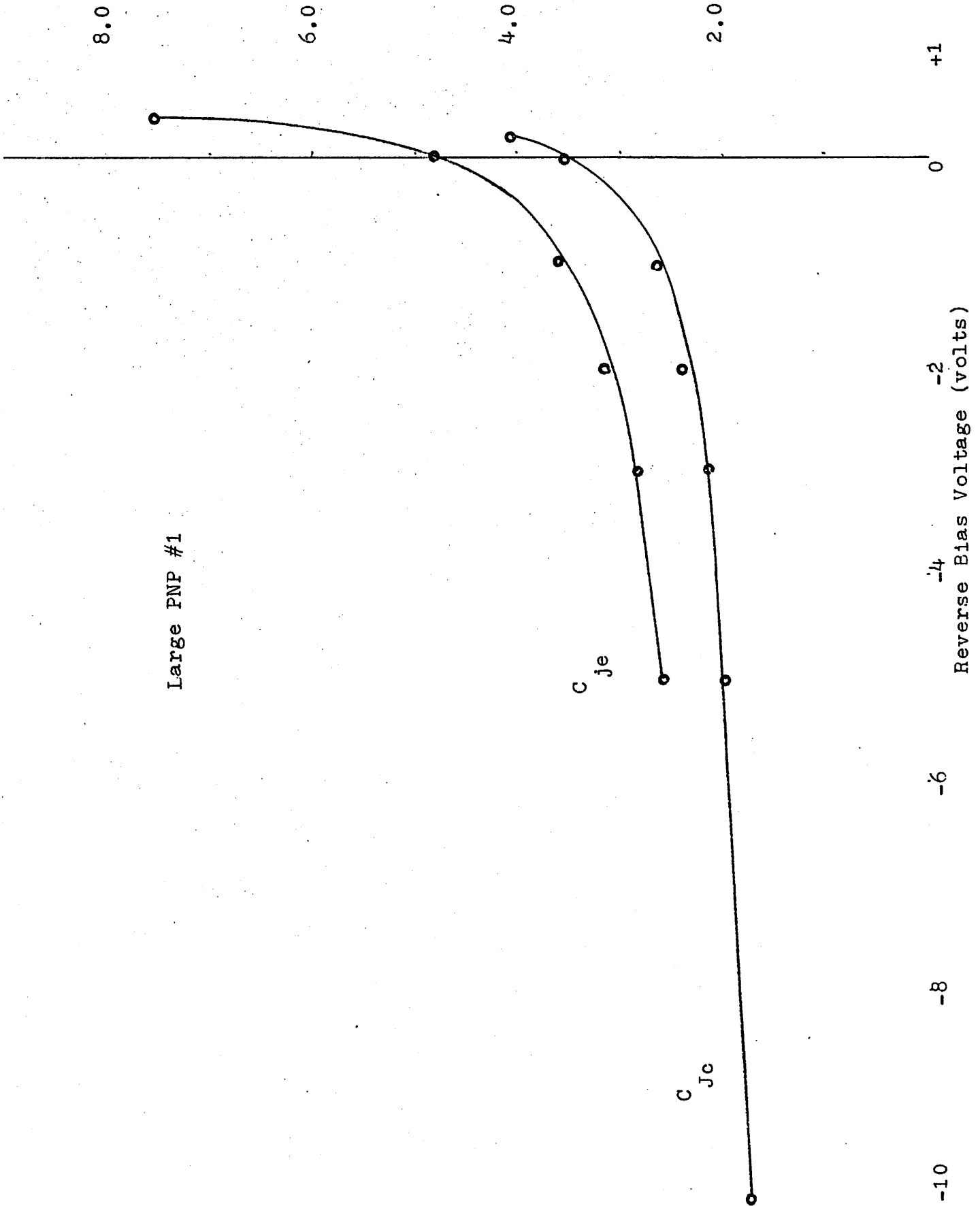


Fig. B.21

Capacitance (pf)

8.0

6.0

4.0

2.0

+1

Large PNP #2

$C_{je}$

-2

-4

-6

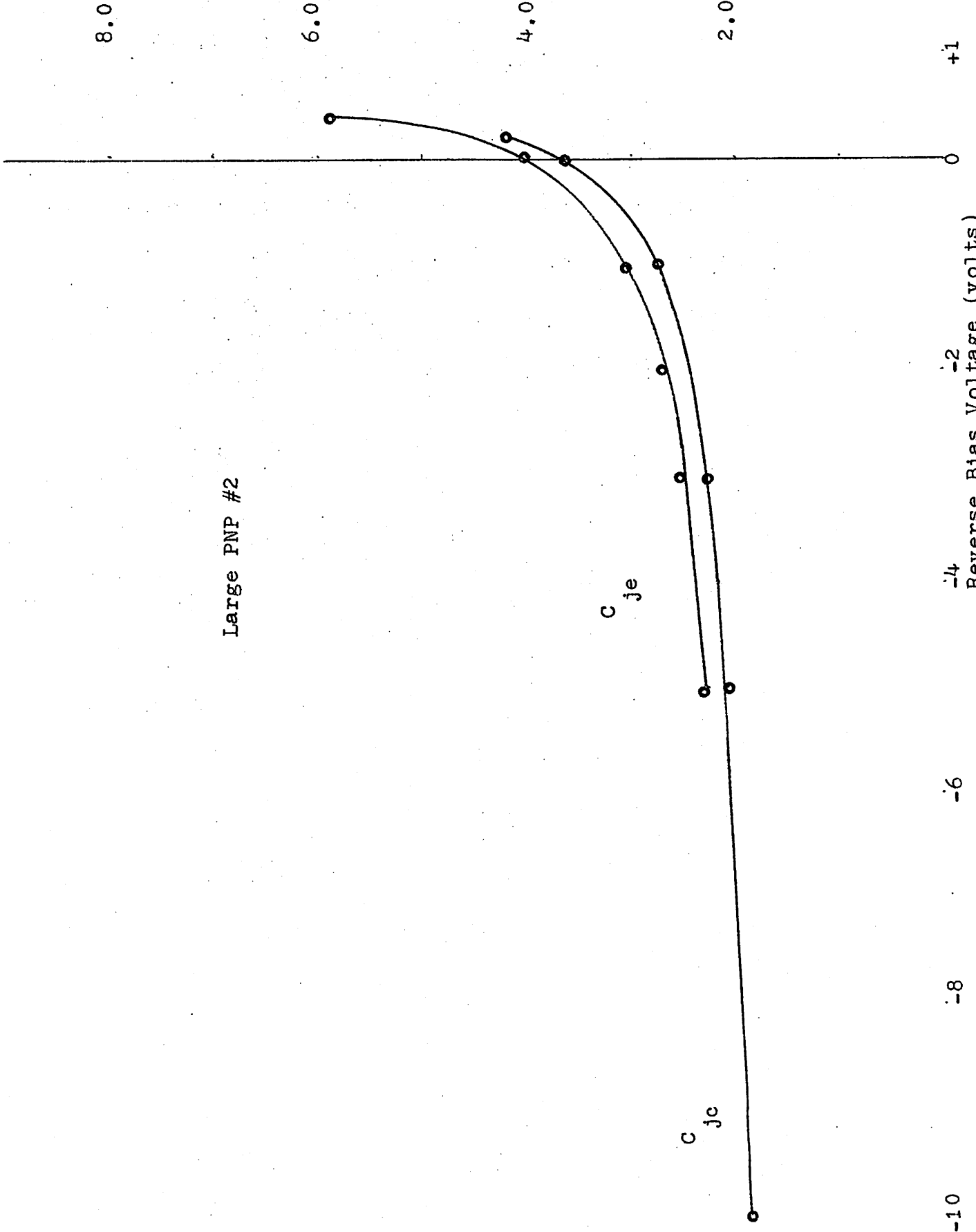
-8

-10

Reverse Bias Voltage (volts)

$C_{jc}$

Fig. B 22



Appendix C

Device Data for the ULX 2139

Table of Contents

- (1) Dc current gain versus collector current ...Fig.C.1-Fig.C.2
- (2) Unity gain frequency versus collector current .....Fig.C.3-Fig.C.8
- (3) Small signal current gain versus frequency..Fig.C.9-Fig.C.20
- (4) Capacitance versus reverse bias voltage.....Fig.C.21-Fig.C.32

1000  $\beta_0$

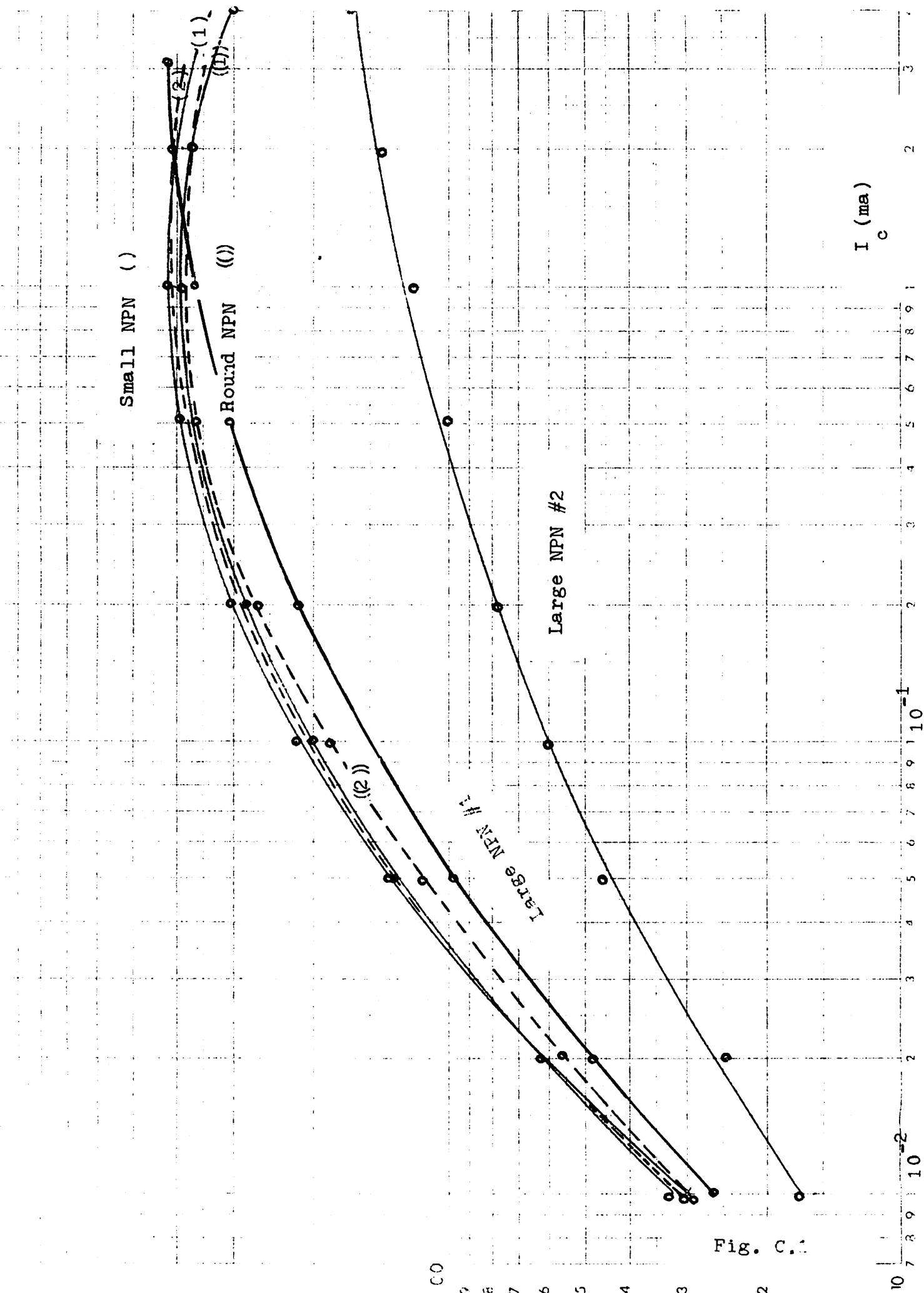


Fig. C.1



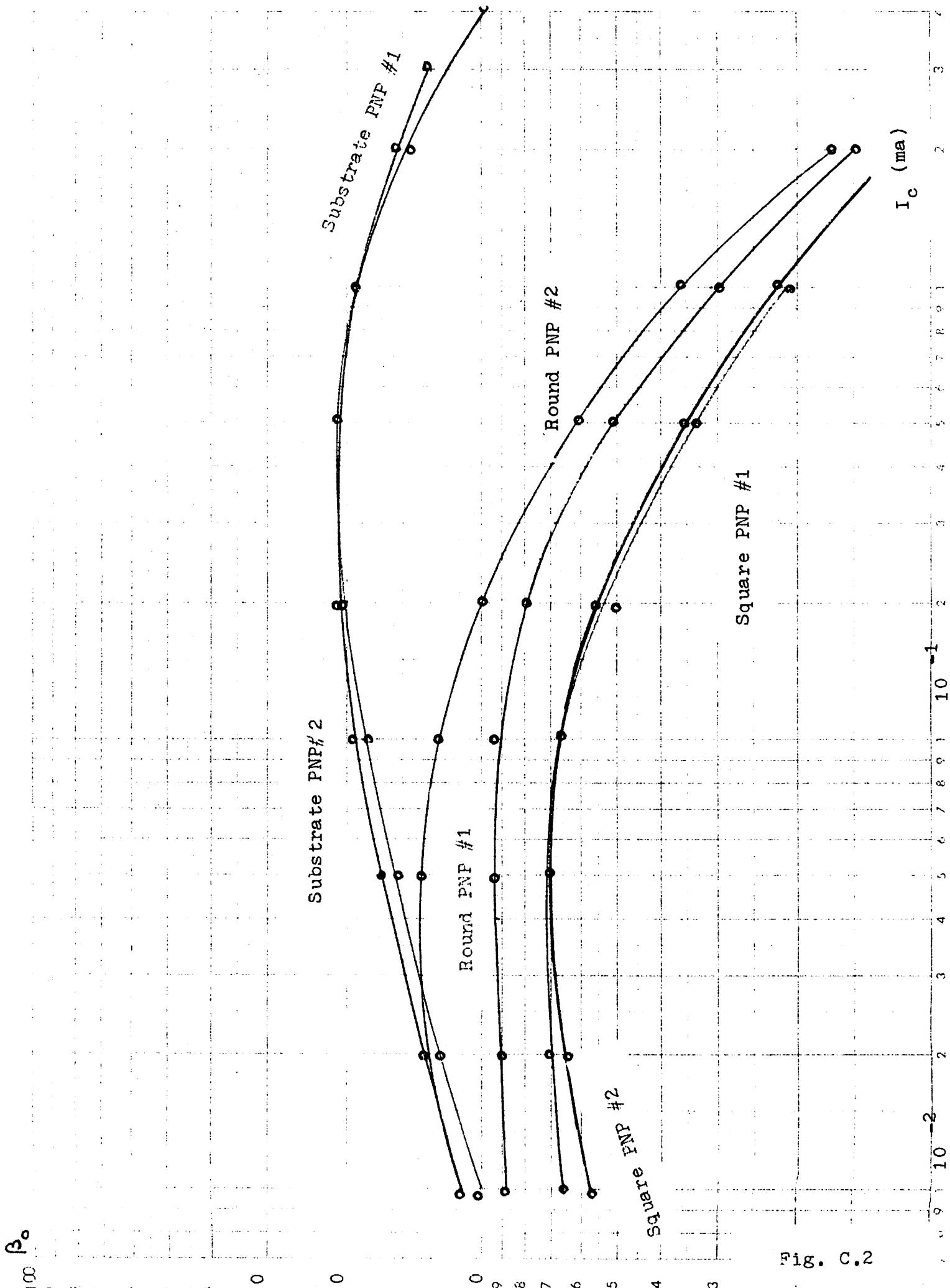


Fig. C.2

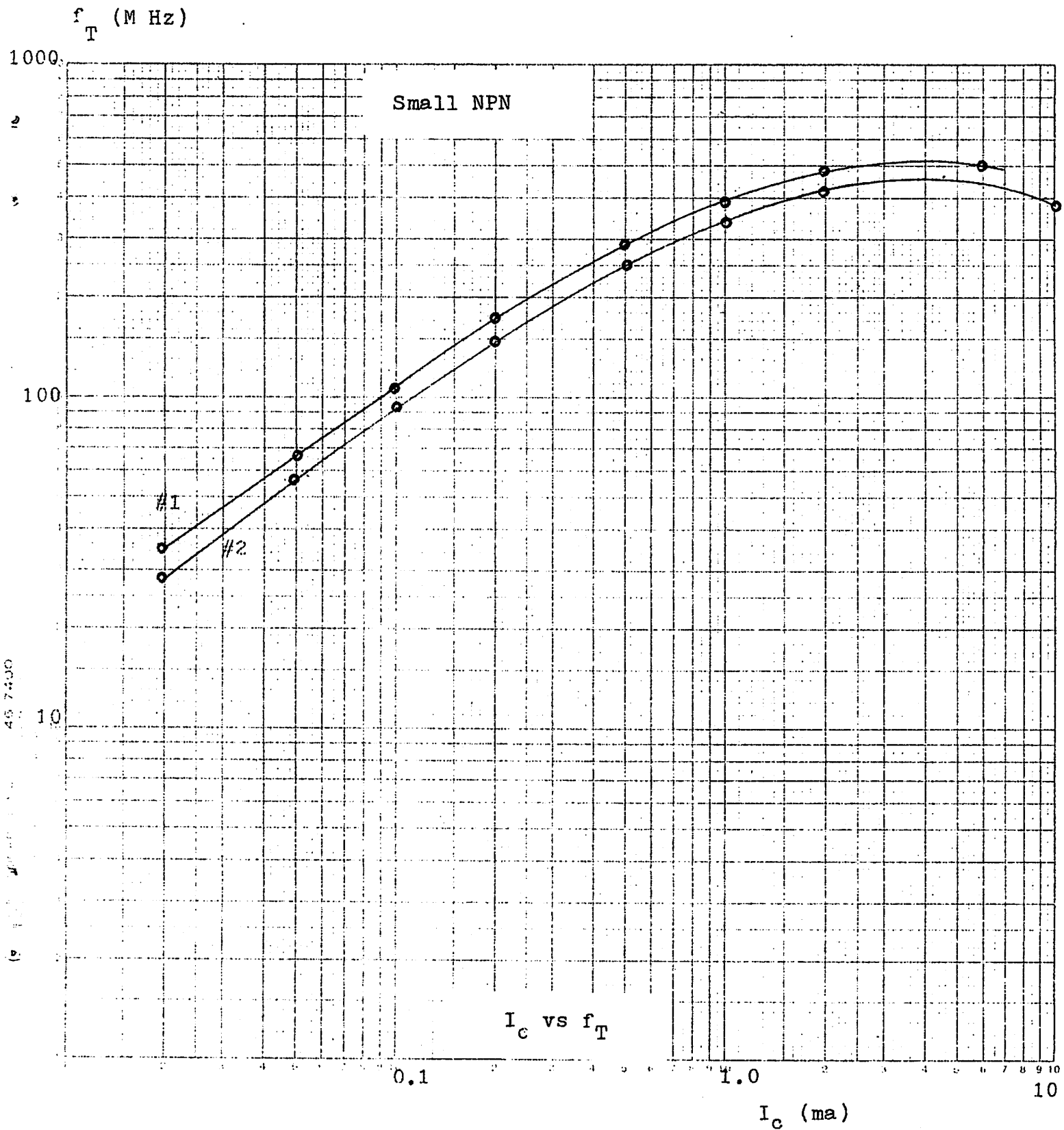


Fig. C.3

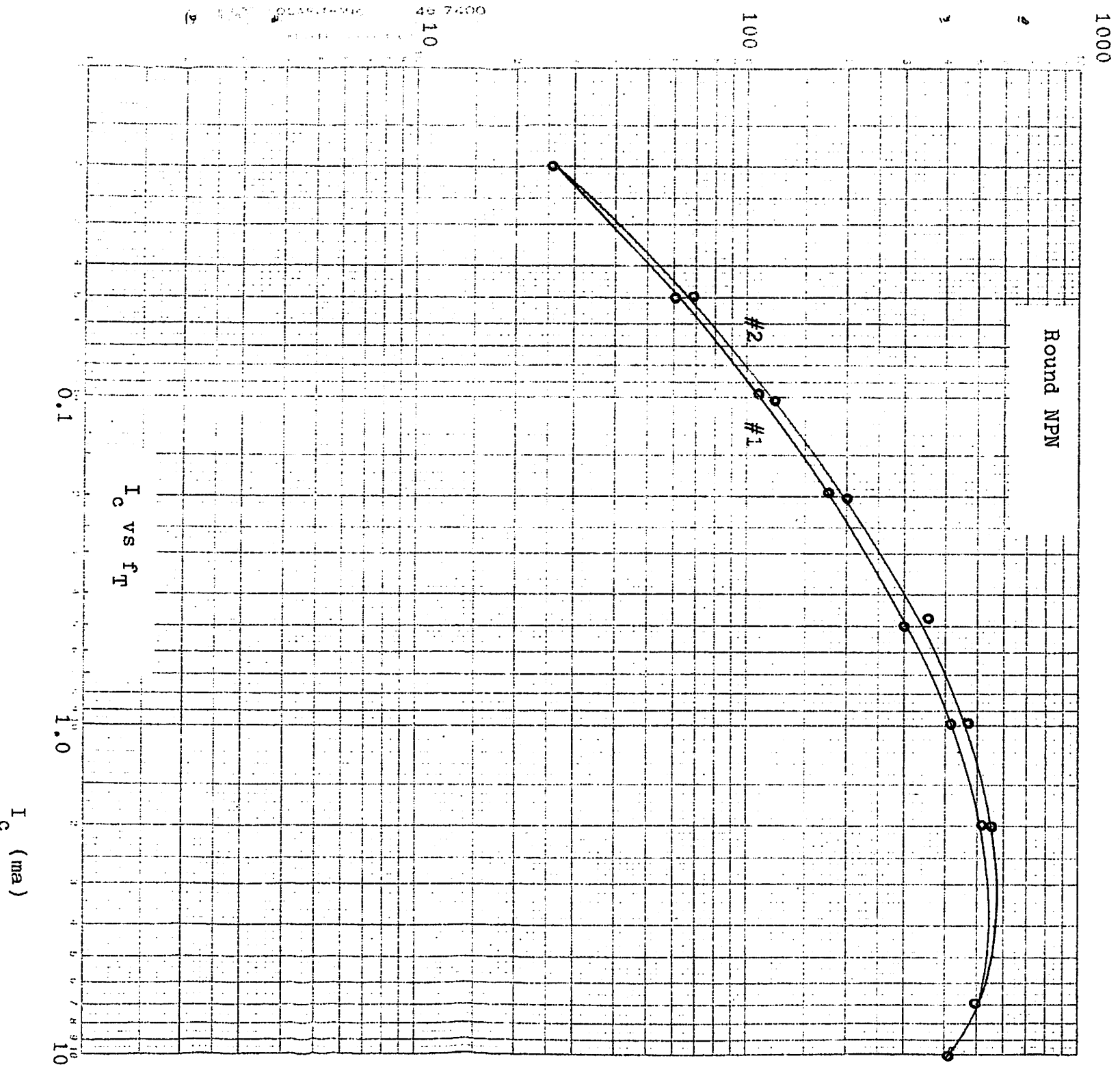


FIG. C.4

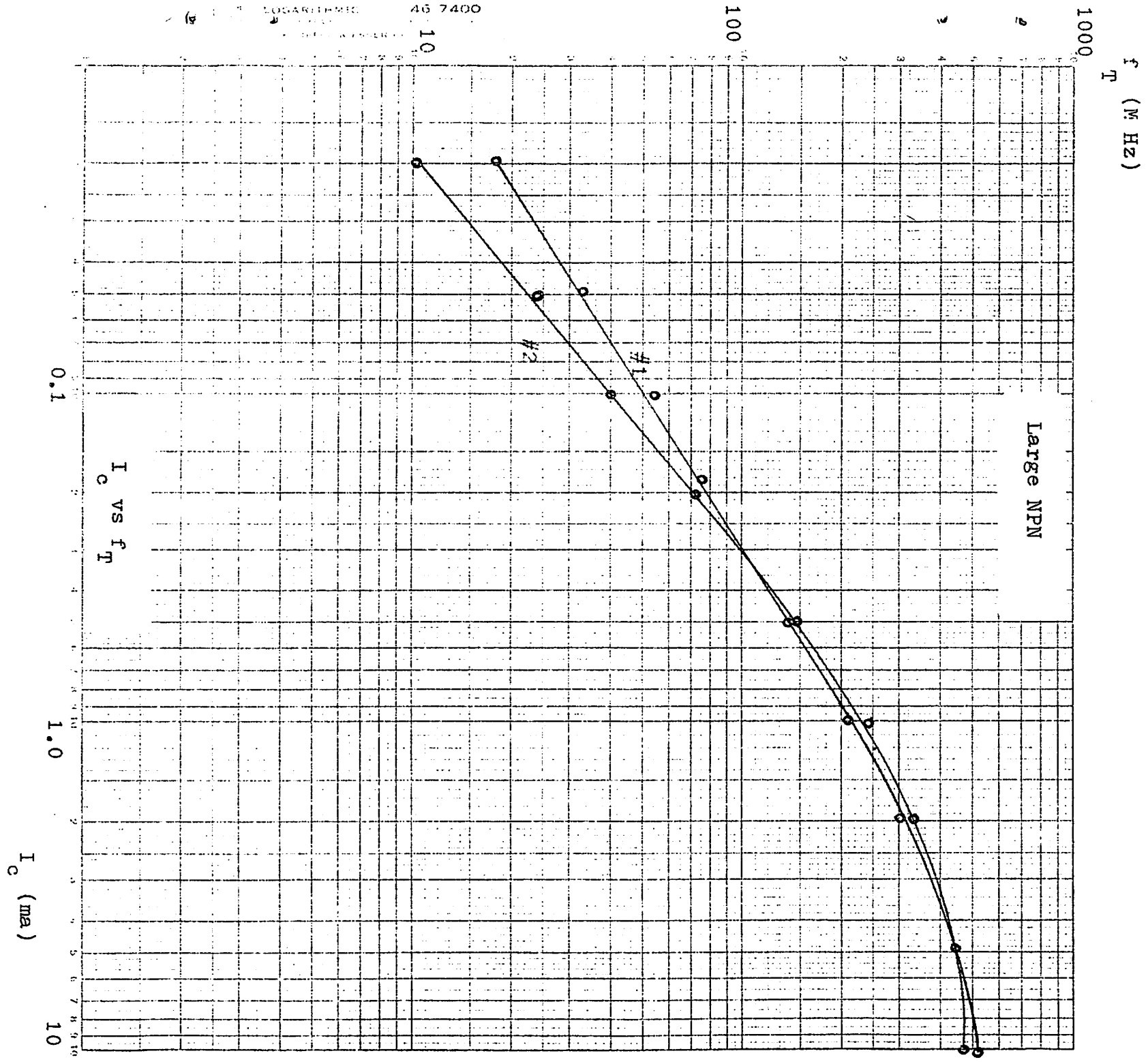
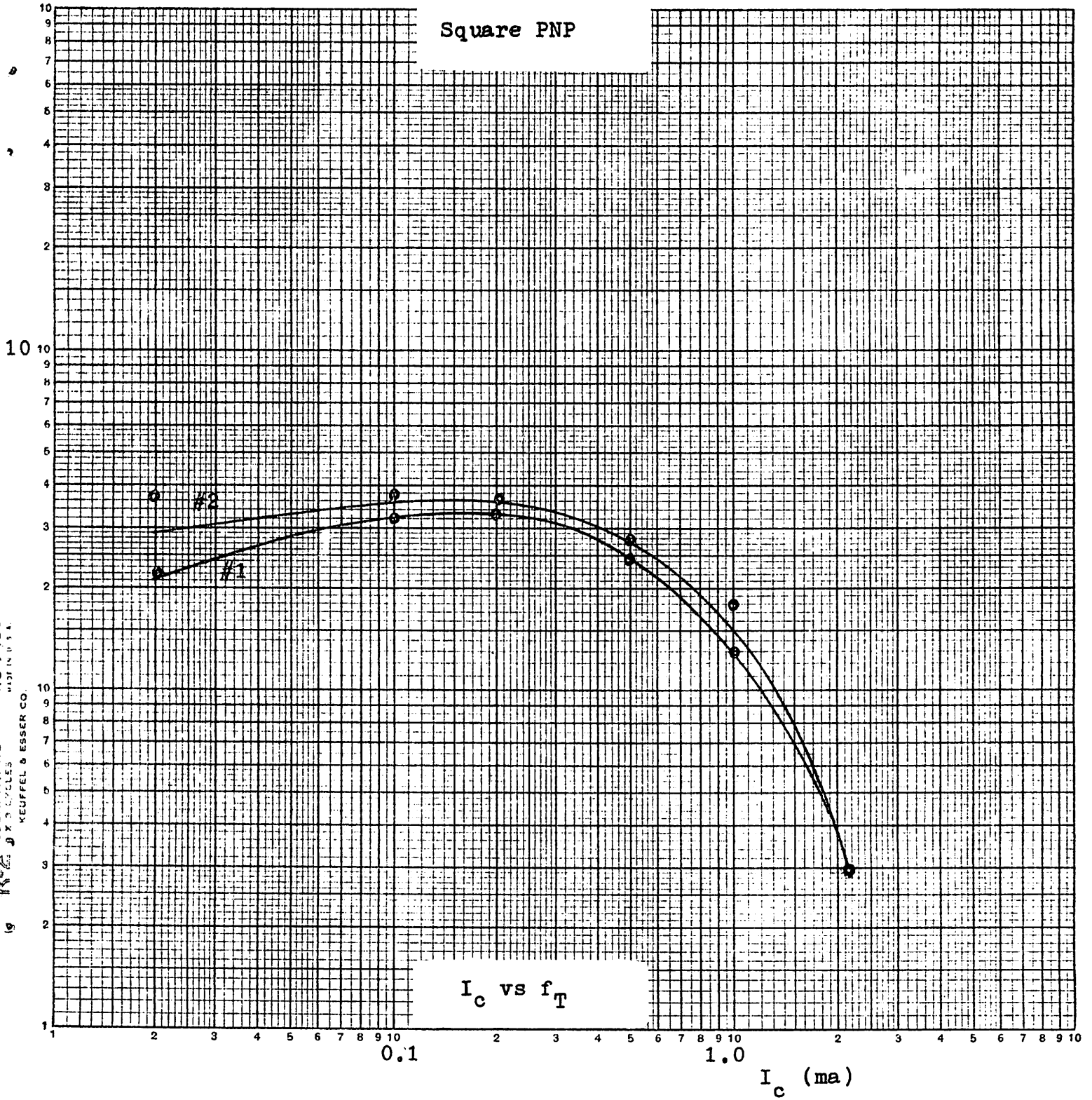


Fig. C.5

$f_T$  (M Hz)



LOGARITHMIC 46 7400  
CYCLES  
KEUFFEL & ESSER CO.

Fig. C.6

$f_T$  (MHz)

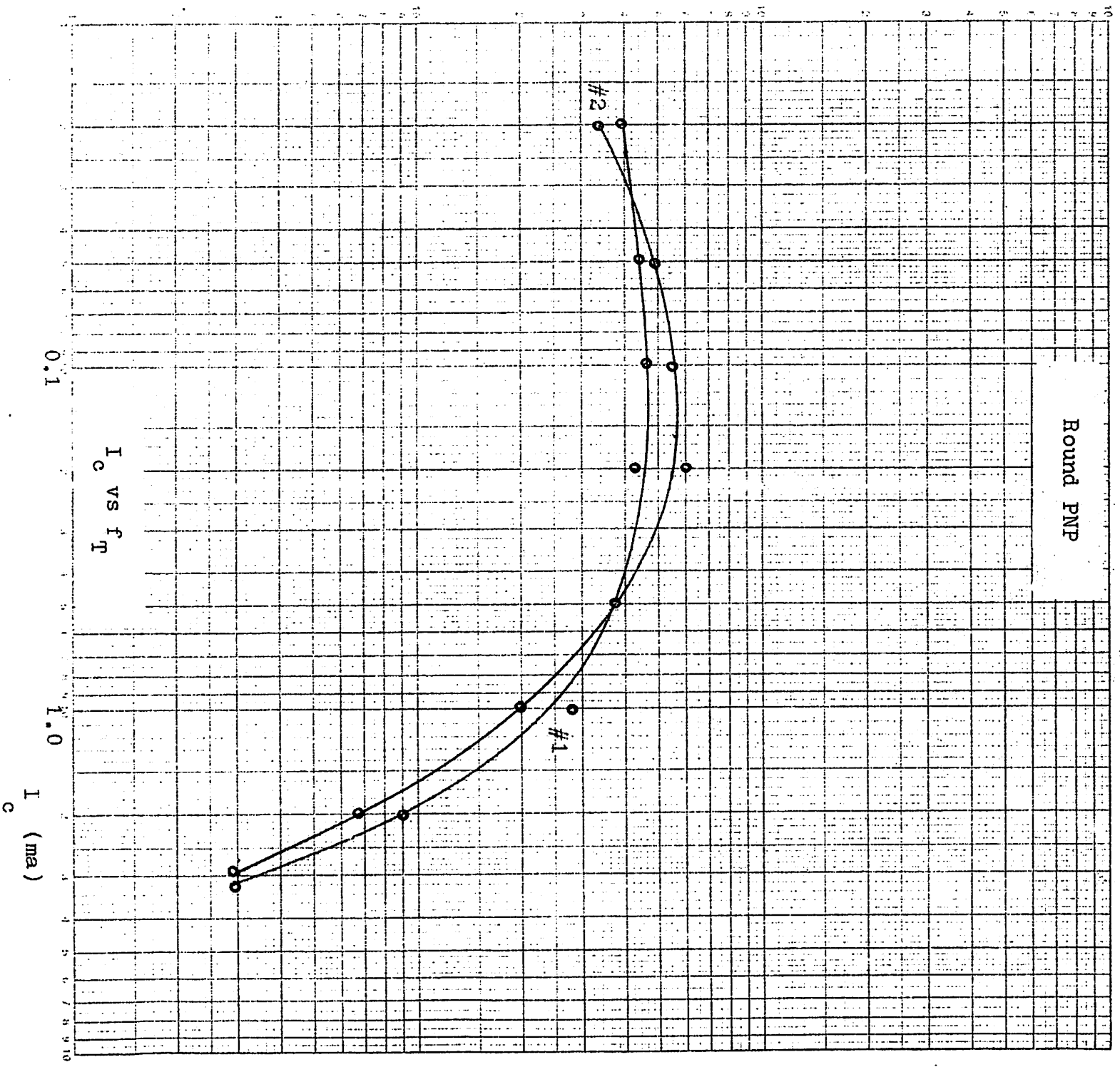


Fig. C.7

$f_T$  (M Hz)

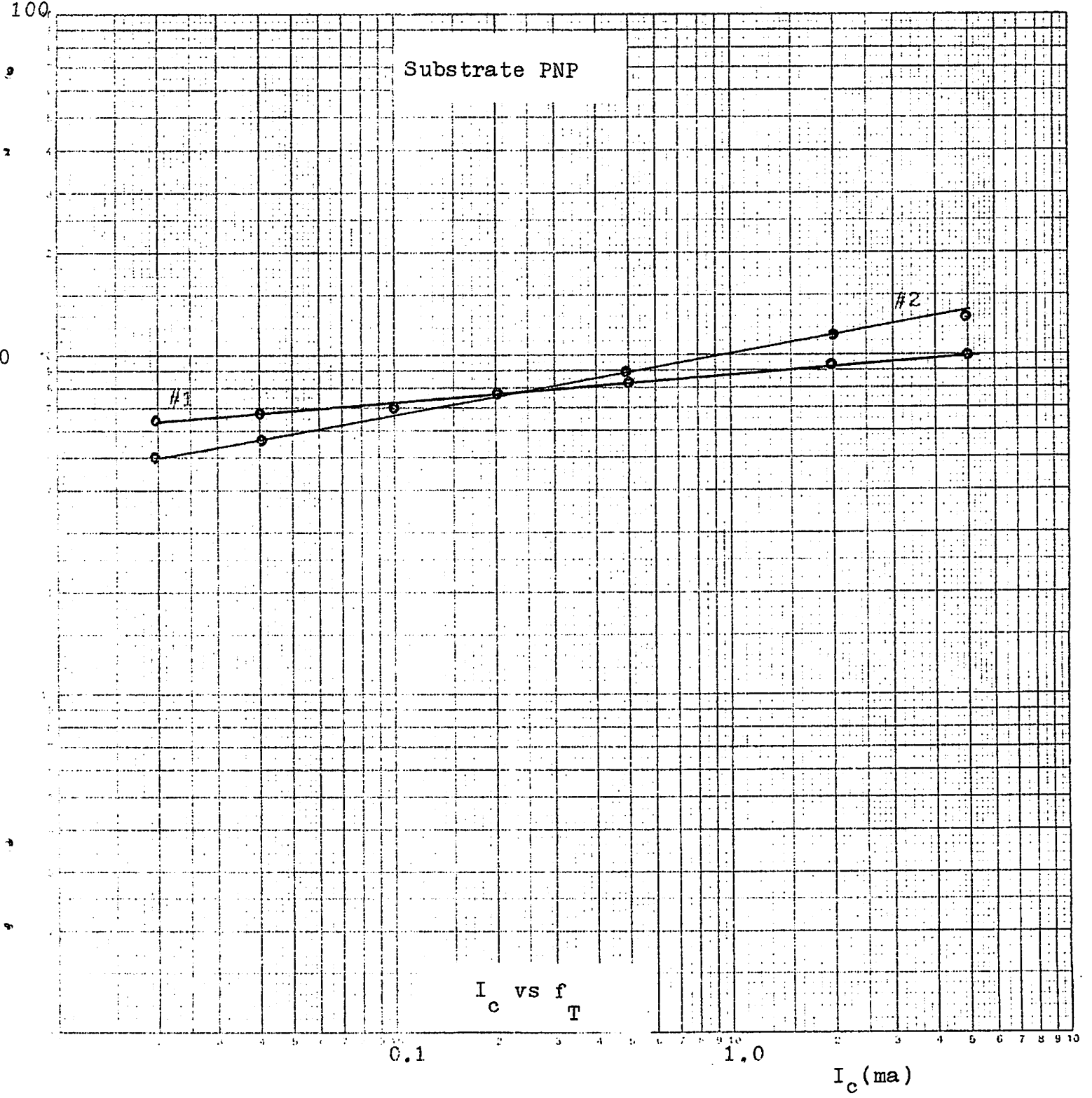


Fig. C.8

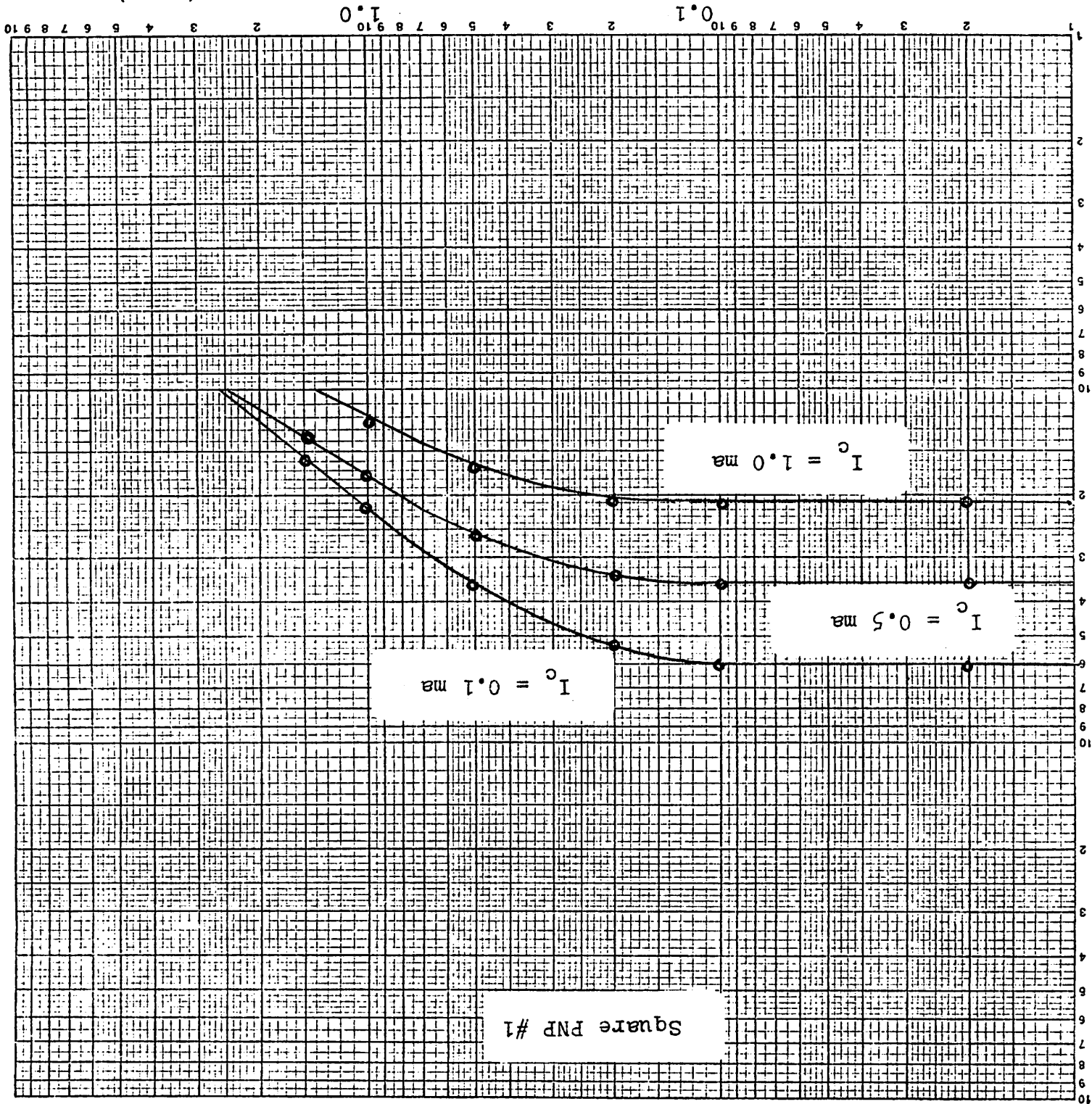


FIG. C.9

$f$  (MHz)

Square PNP #1

$I_c = 0.1 \text{ ma}$

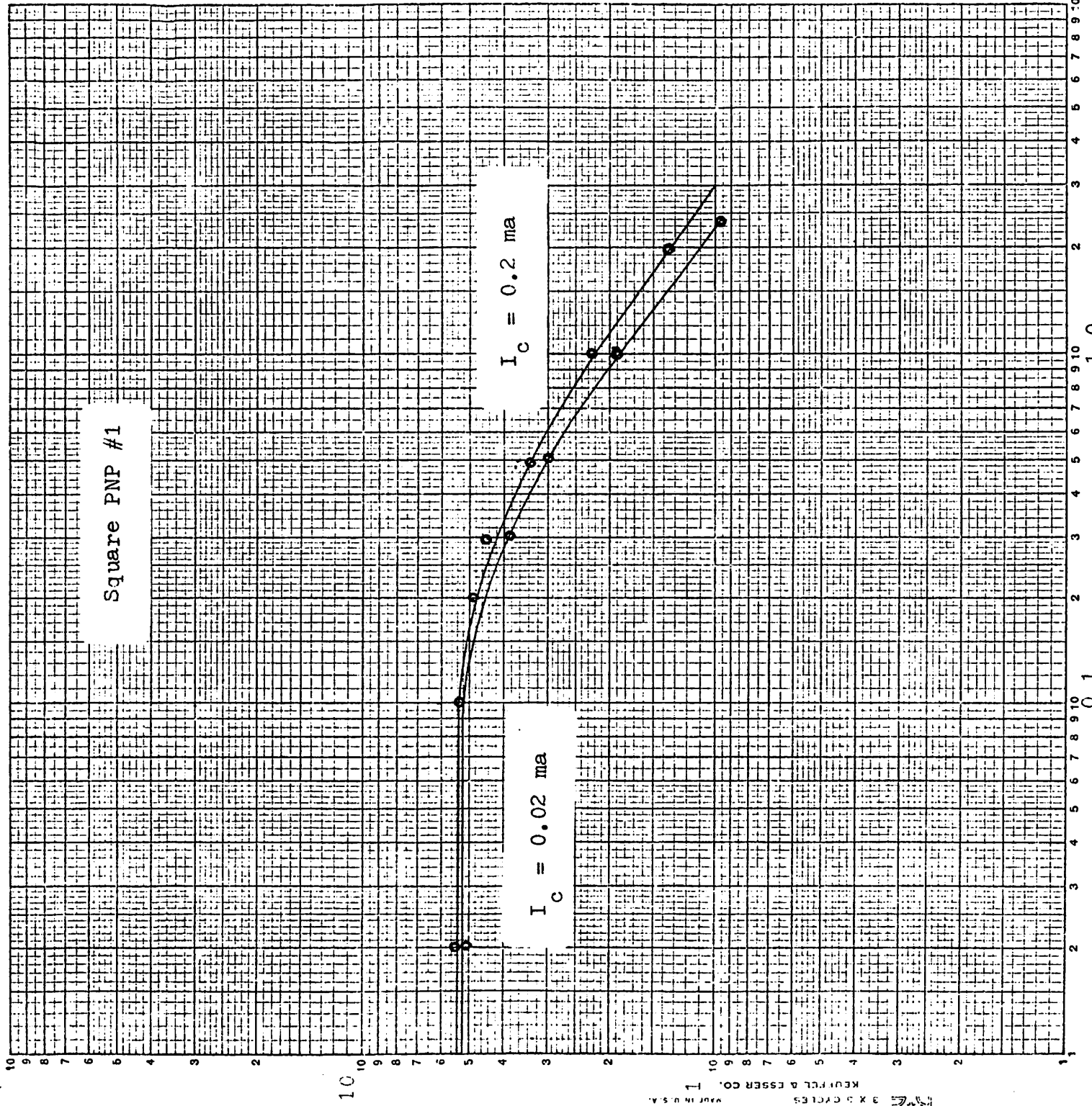
$I_c = 0.5 \text{ ma}$

$I_c = 1.0 \text{ ma}$

10  
10  
10



B



Square PNP #1

$I_C = 0.2$  ma

$I_C = 0.02$  ma

$f$  (M Hz)

FIG. C.10

46 7400  
ANALOGIC  
3 X 3 CYCLES  
KEUFEL & ESSER CO. 1  
MADE IN U.S.A.

β

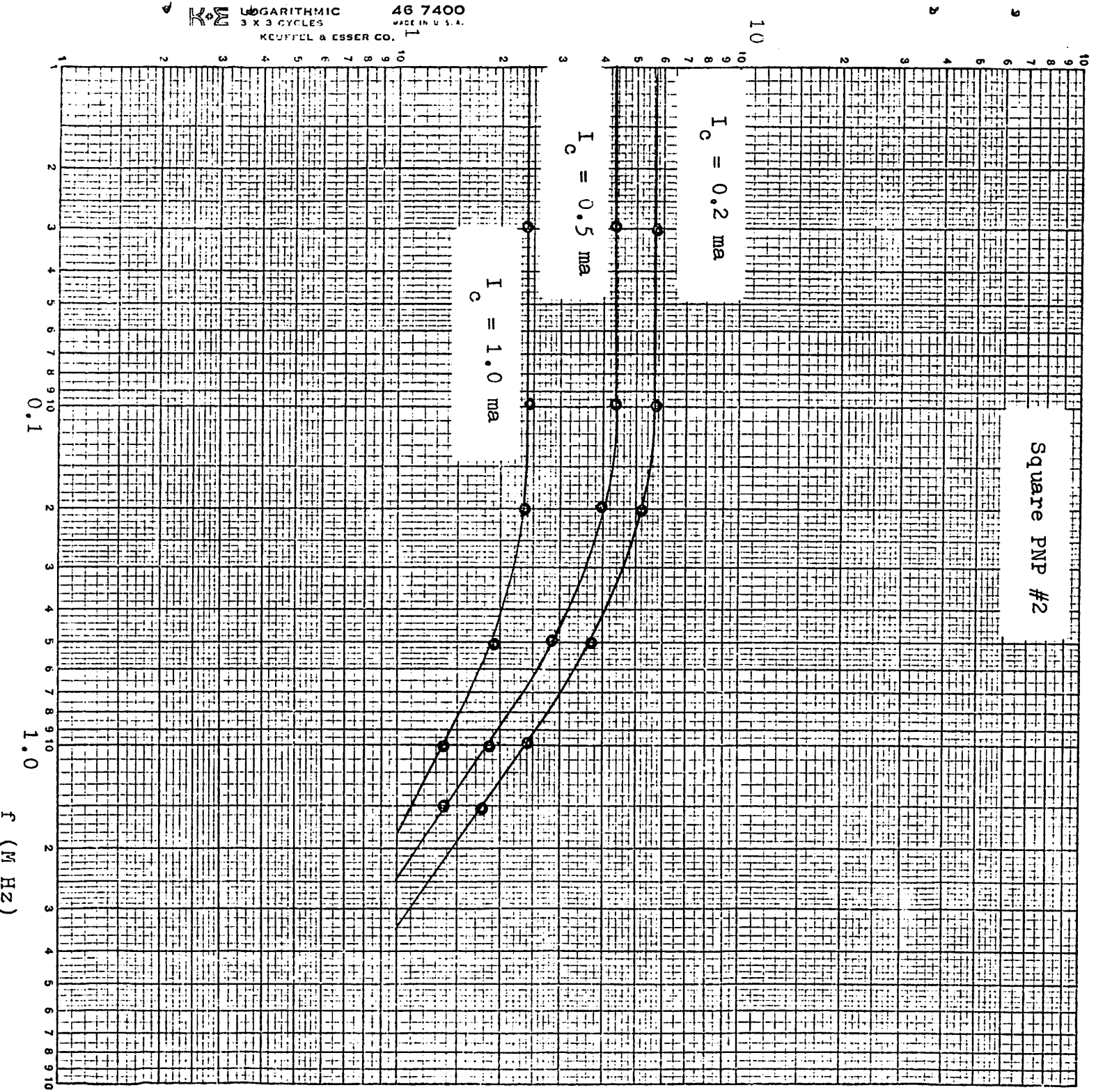
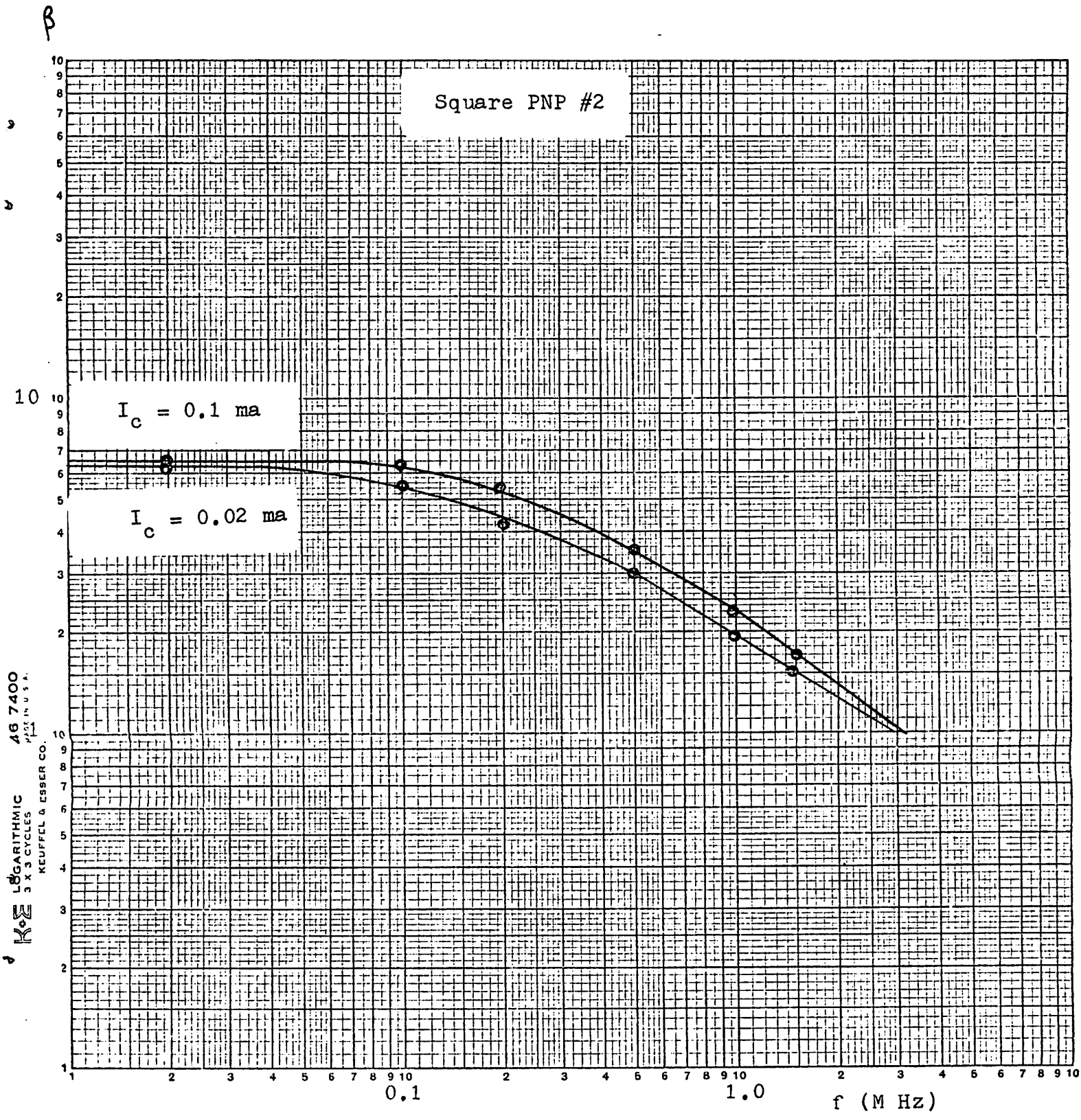


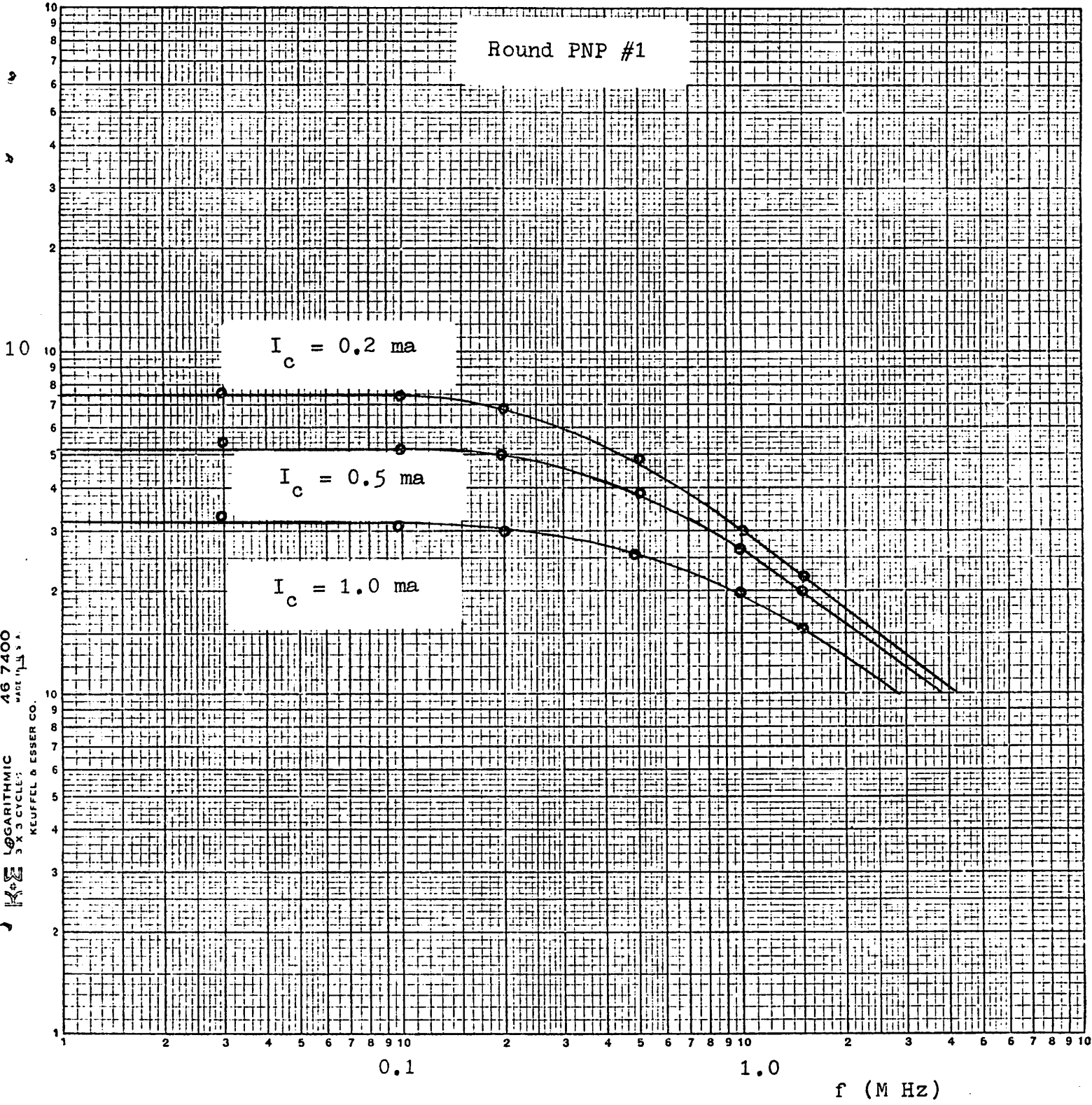
FIG. C.11



KEITHLEY LOGARITHMIC 46 7400 MADE IN U.S.A. KEUFFEL & ESSER CO.

Fig. C.12

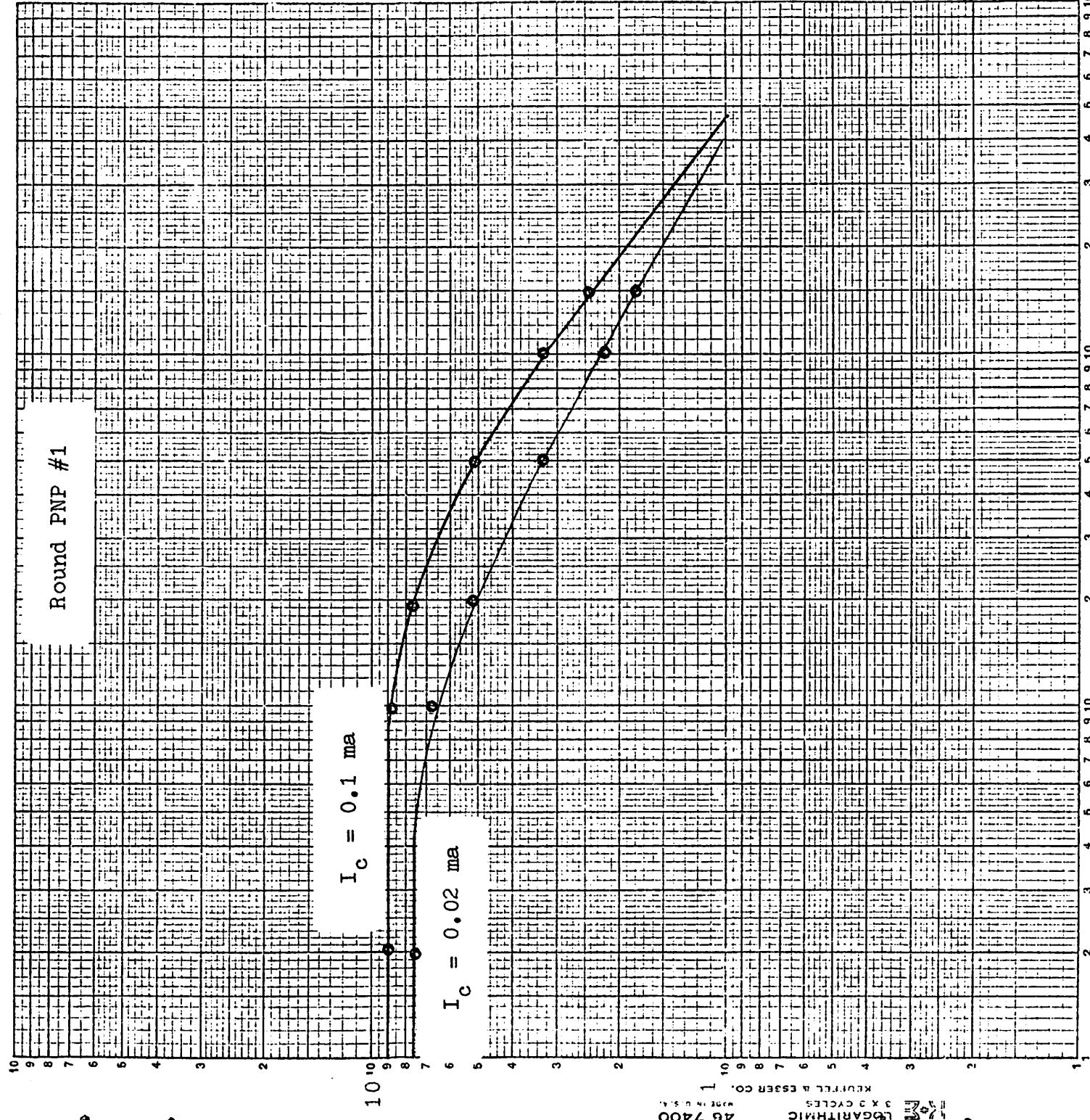
B



46 7400  
LOGARITHMIC  
3 X 3 CYCLE  
KEUFFEL & ESSER CO.

Fig. C.13

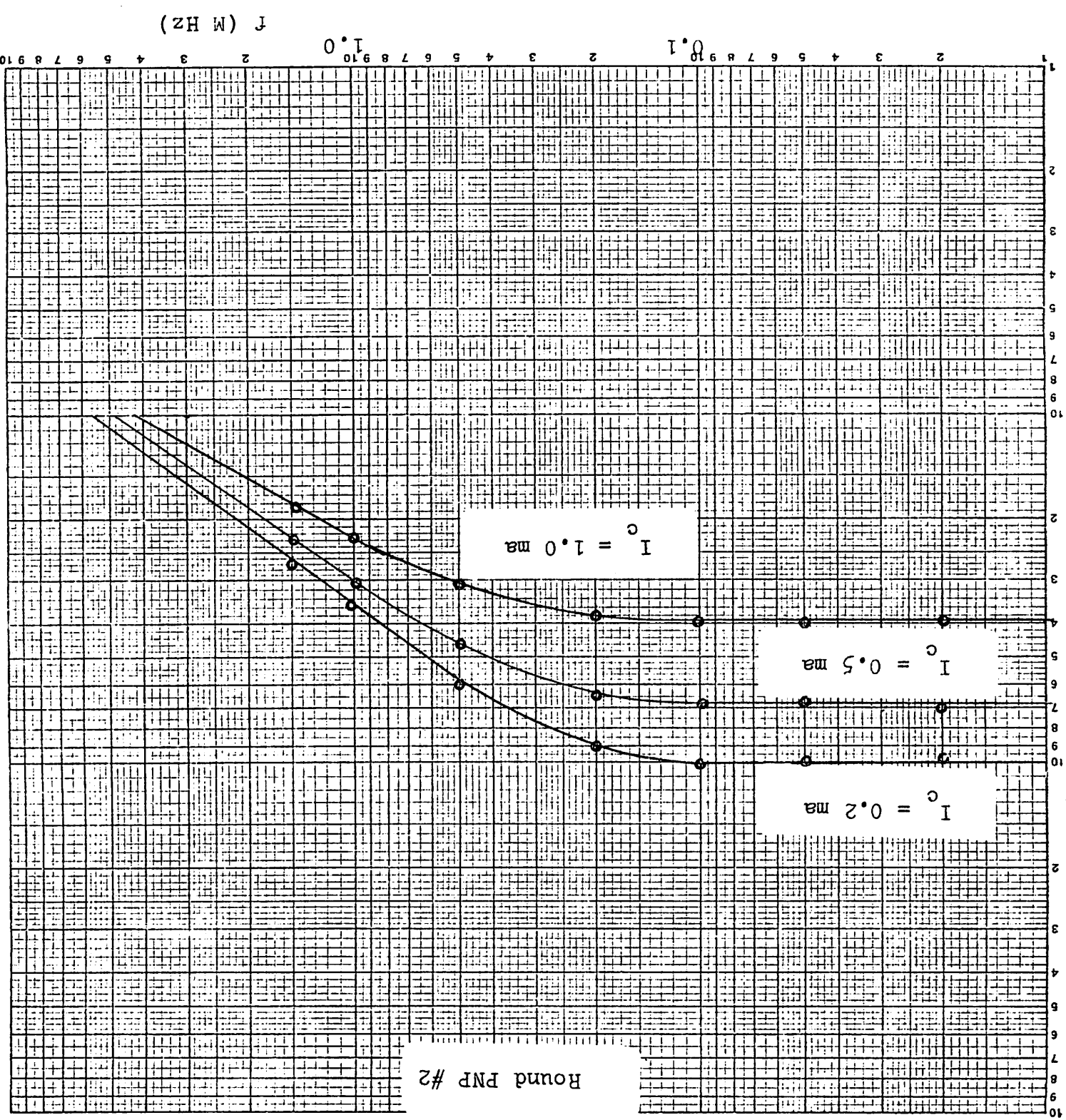
$\beta$



46 7400  
LOGARITHMIC  
3 X 3 CYCLES  
KEUFFEL & ESSER CO.  
MADE IN U.S.A.

Fig. C.14



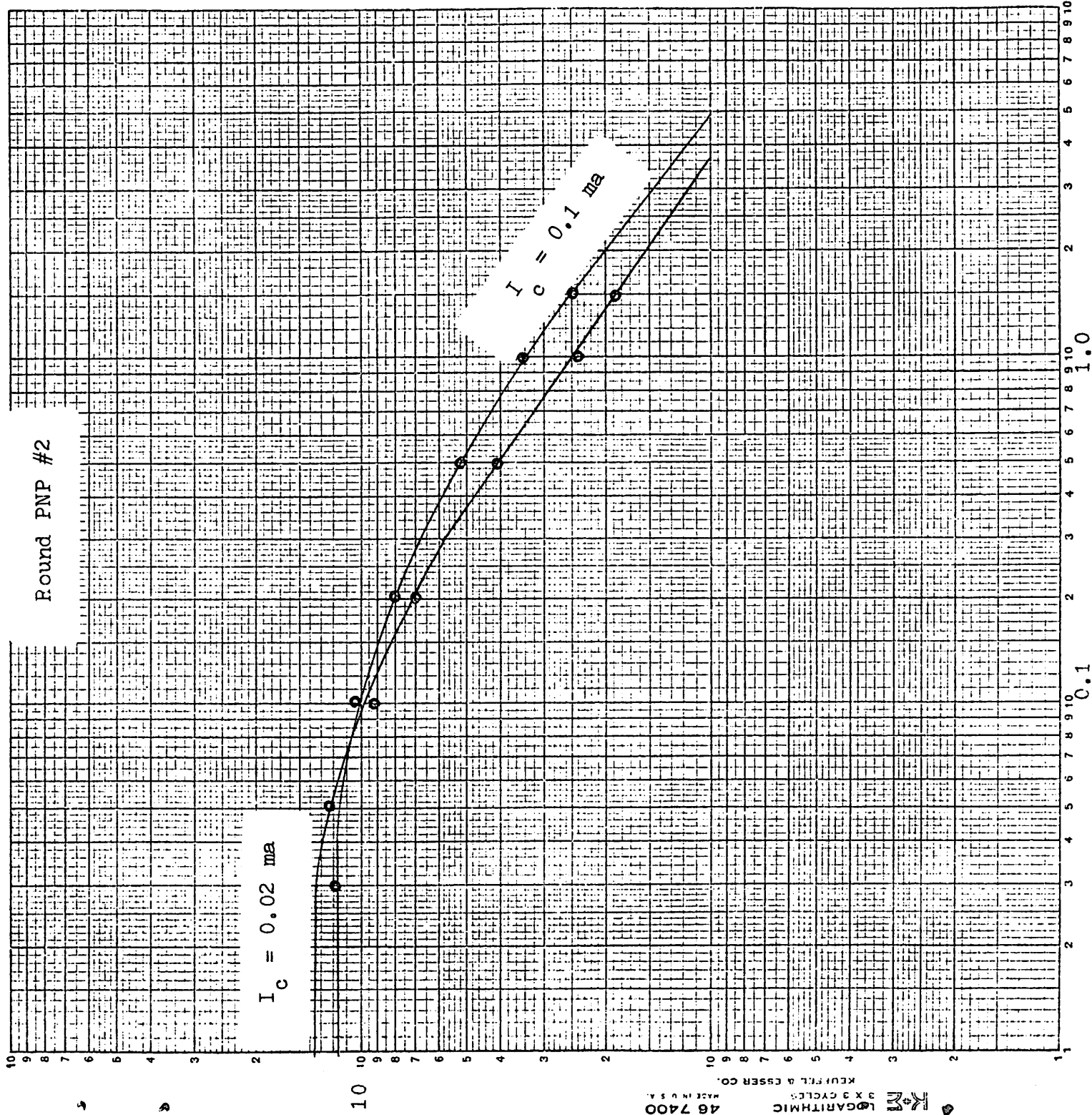


Round PNP #2

ETS. C.15

B

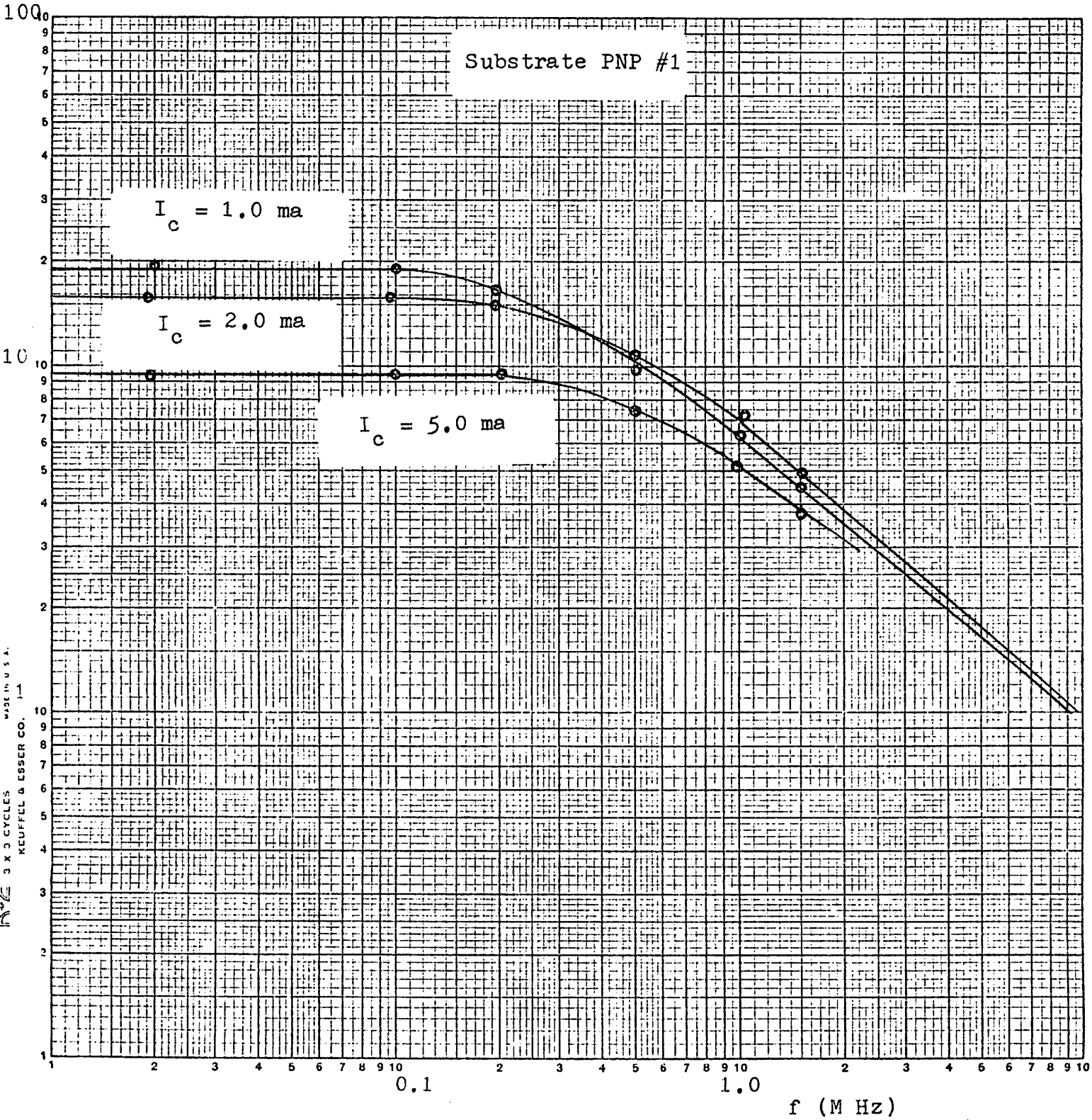
$\beta$



46 7400  
LOGARITHMIC  
3 X 3 CYCLE  
KEUFFEL & ESSER CO.  
MADE IN U.S.A.

FIG. C.16

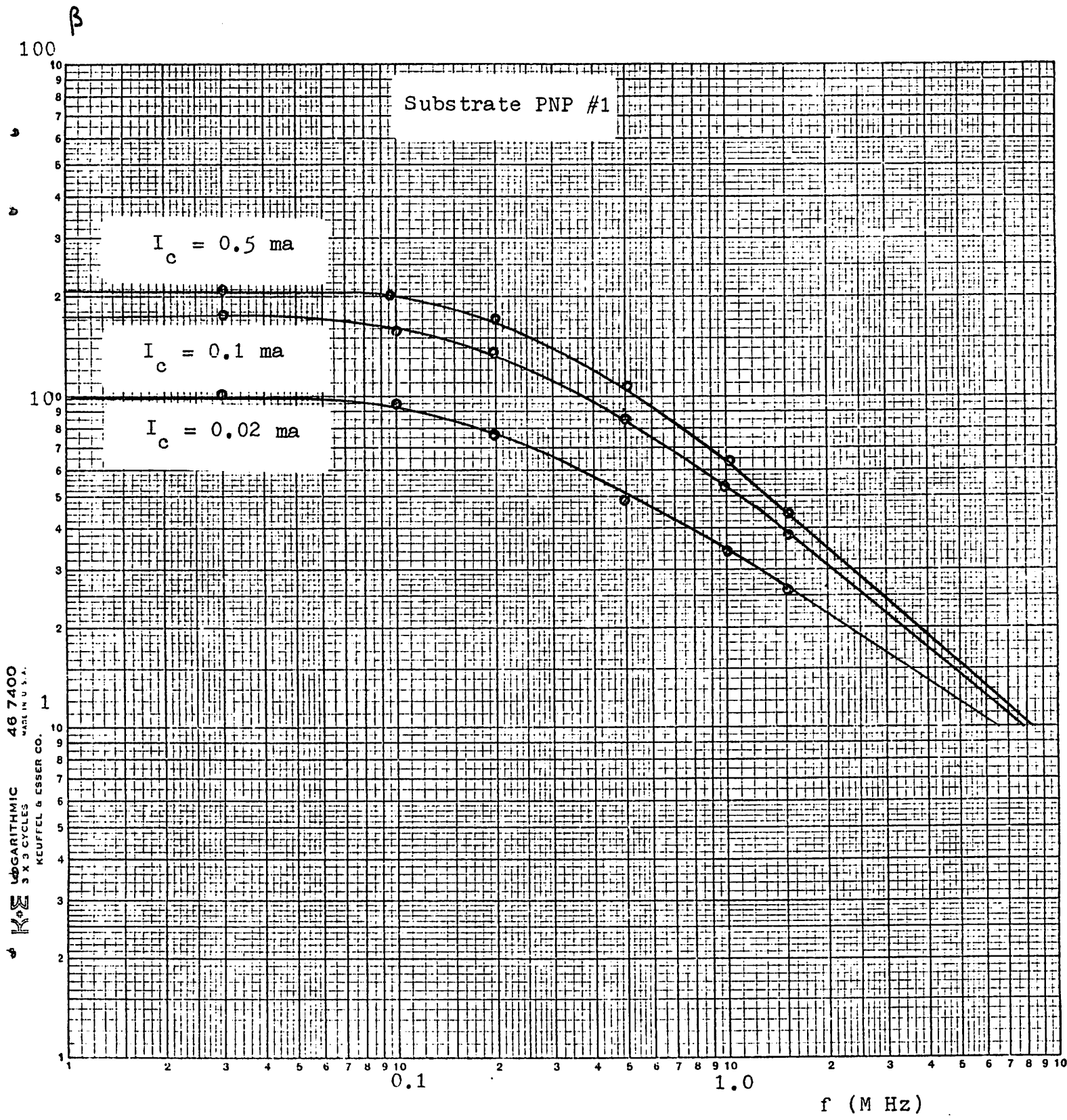
$\beta$



46 7400  
MADE IN U.S.A.  
LOGARITHMIC  
3 X 3 CYCLES  
HEUFFEL & ESSER CO. 1-1

Fig. C.17

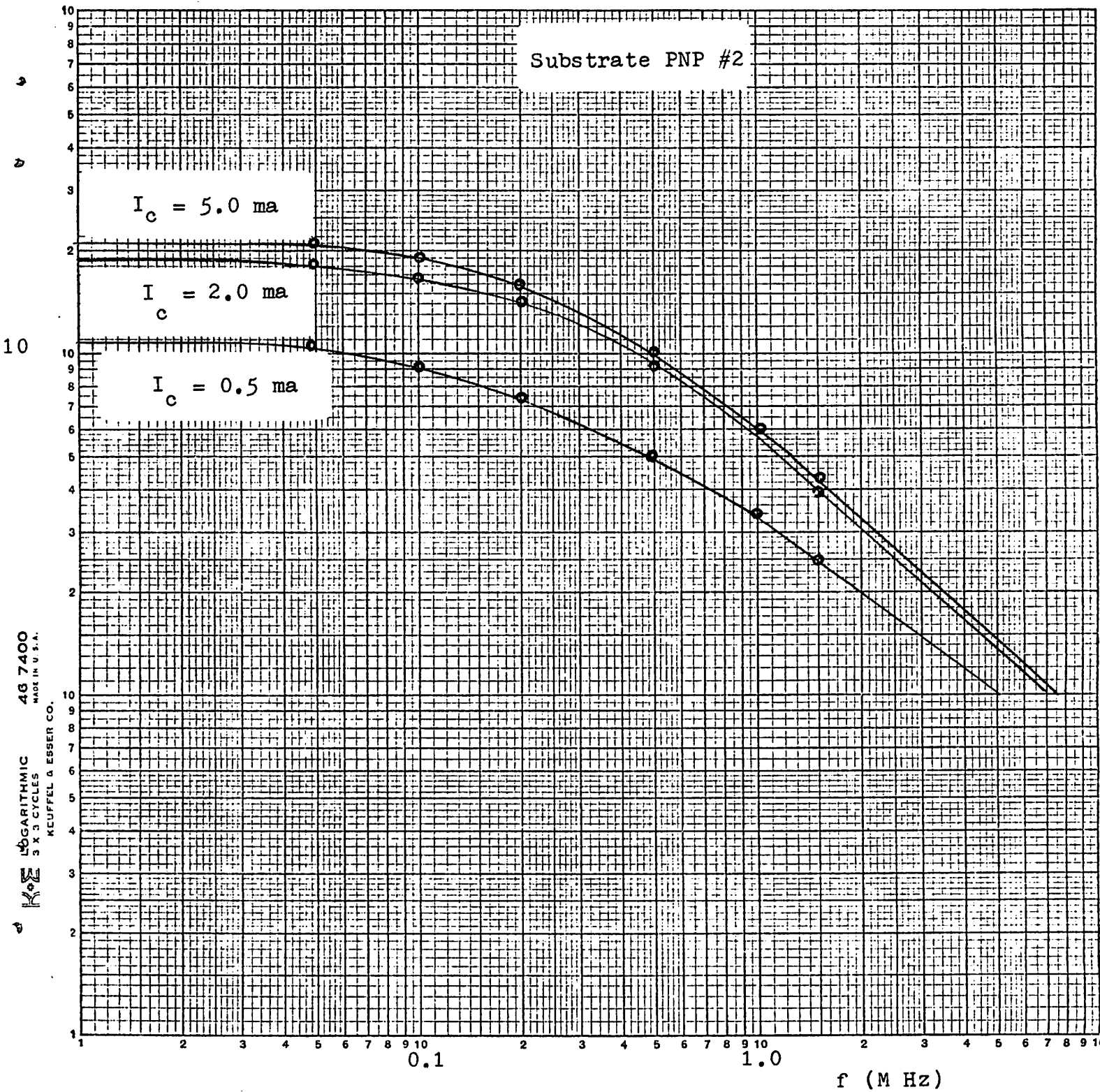




46 7400  
 KEUFFEL & ESSER CO.  
 LOGARITHMIC  
 3 X 3 CYCLES  
 MADE IN U.S.A.

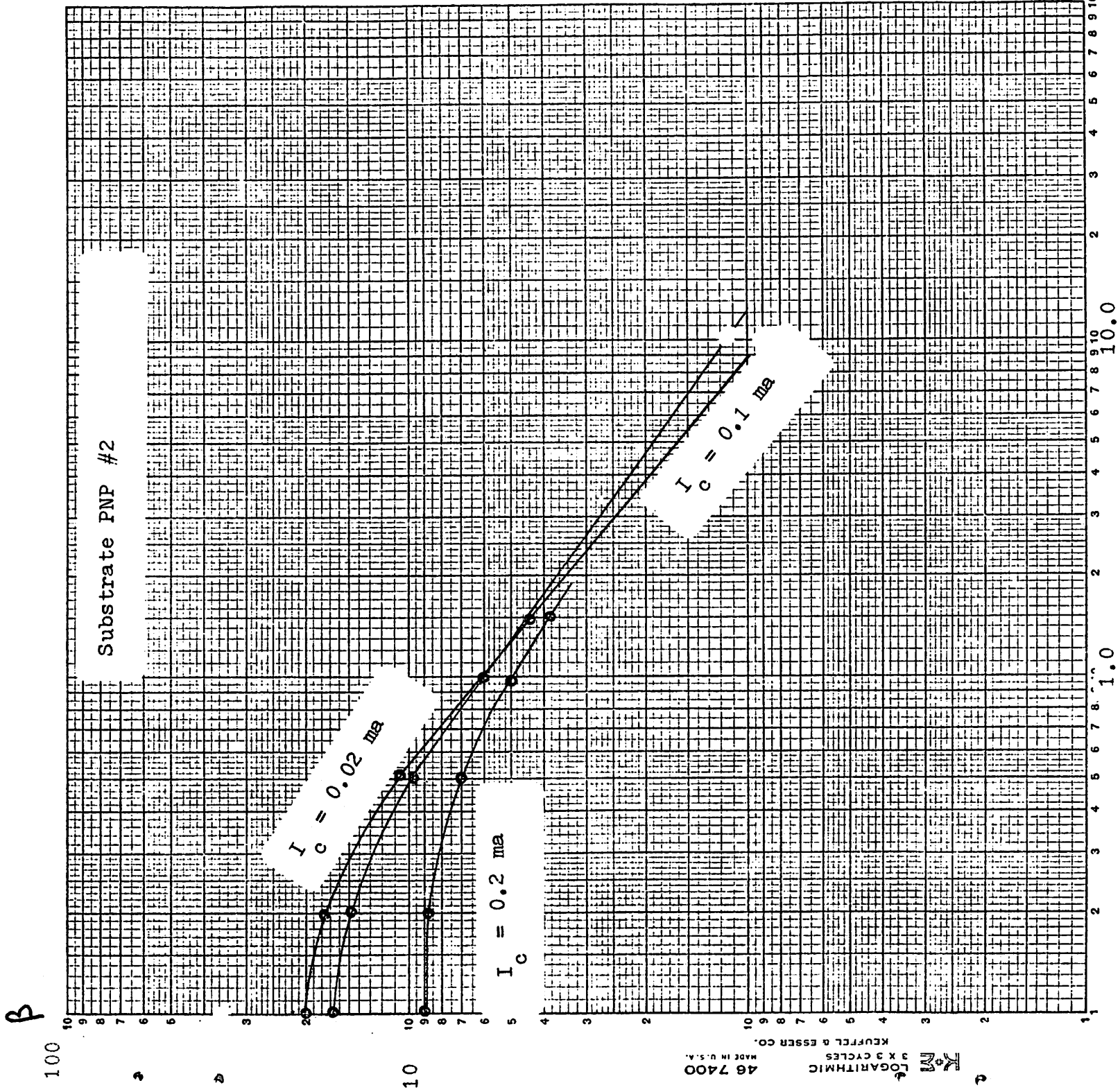
Fig. C.18

$\beta$



46 7400  
LOGARITHMIC  
3 X 3 CYCLES  
KEUFFEL & ESSER CO.  
MADE IN U.S.A.

Fig. C.19




 LOGARITHMIC  
 3 X 3 CYCLES  
 KEUFFEL & ESSER CO.  
 MADE IN U.S.A.  
 46 7400

FIG. C.20

Capacitance (pf)

Small NPN #2

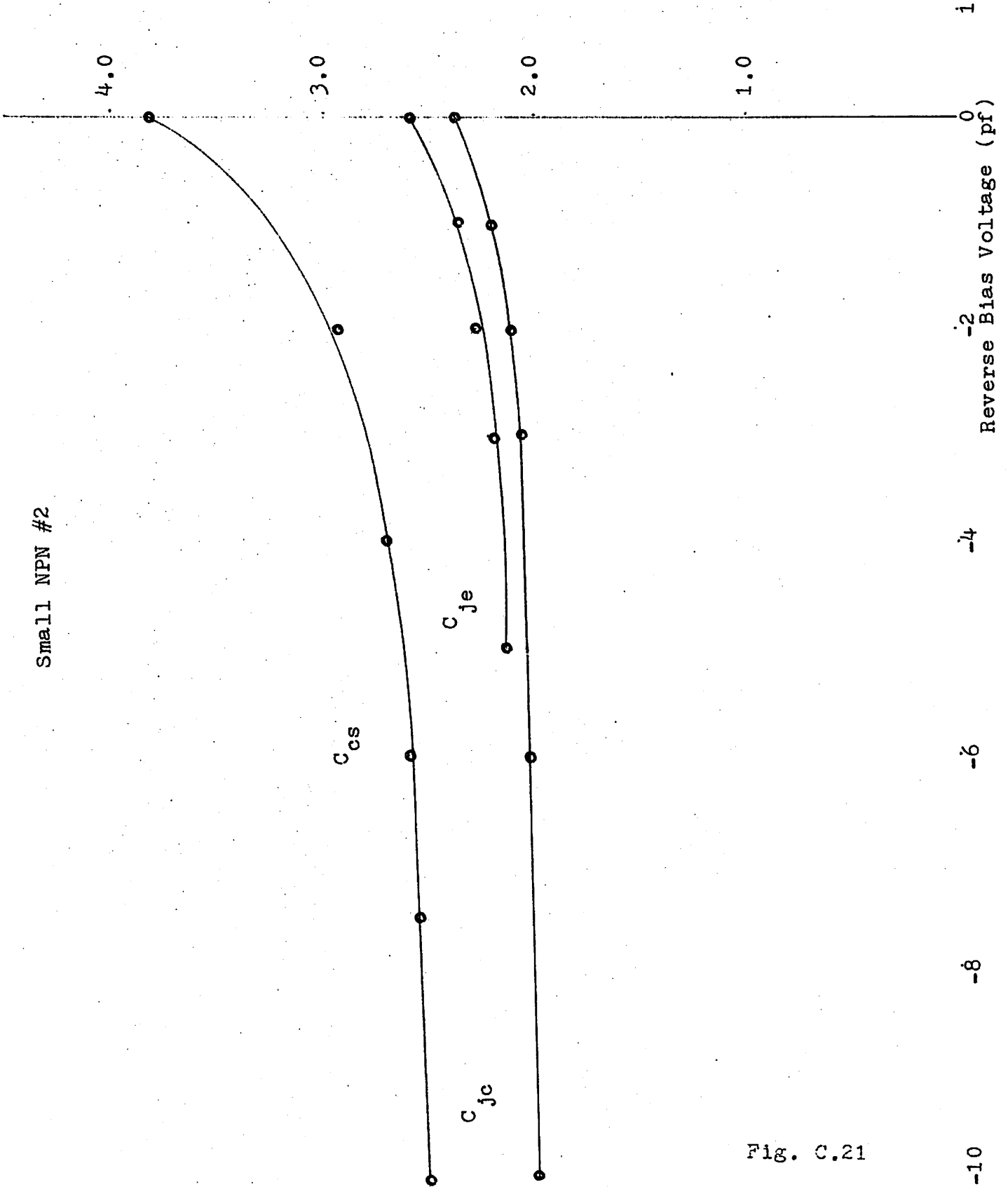


Fig. C.21

Capacitance (pf)

Round NPN #2

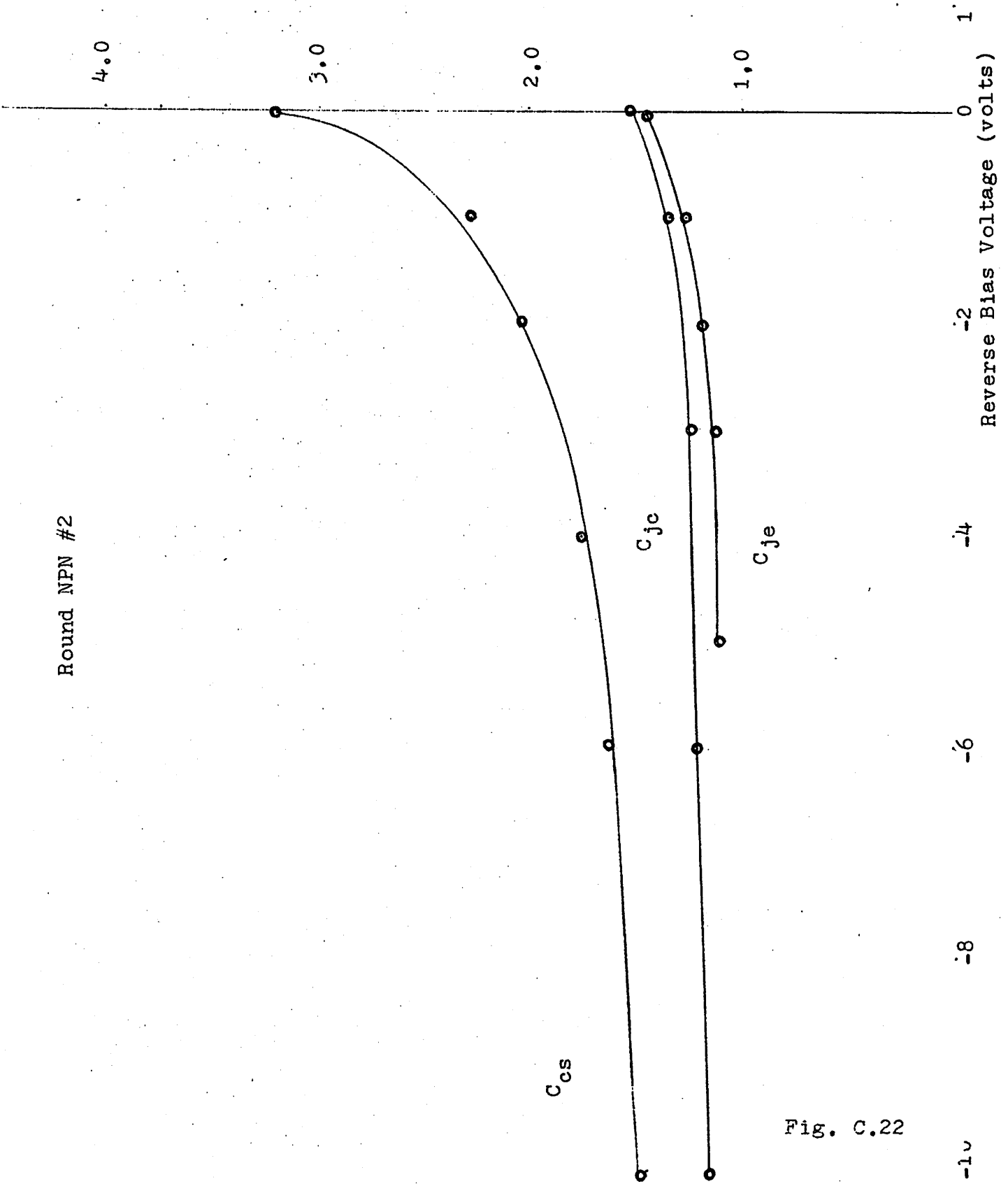


Fig. C.22

Capacitance (pf)

Large NPN #2

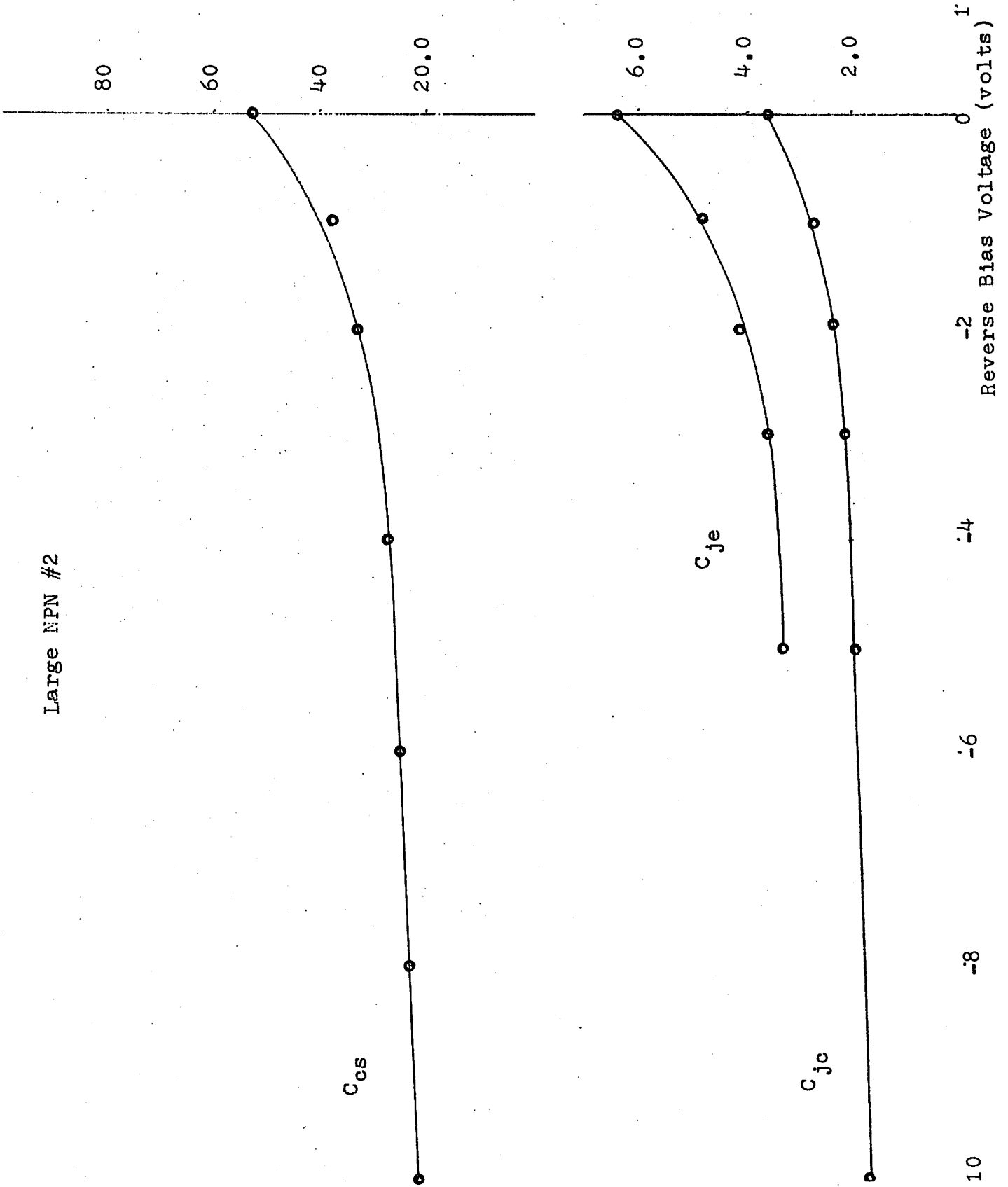


Fig. C.23

Capacitance (pf)

Square PNP #2

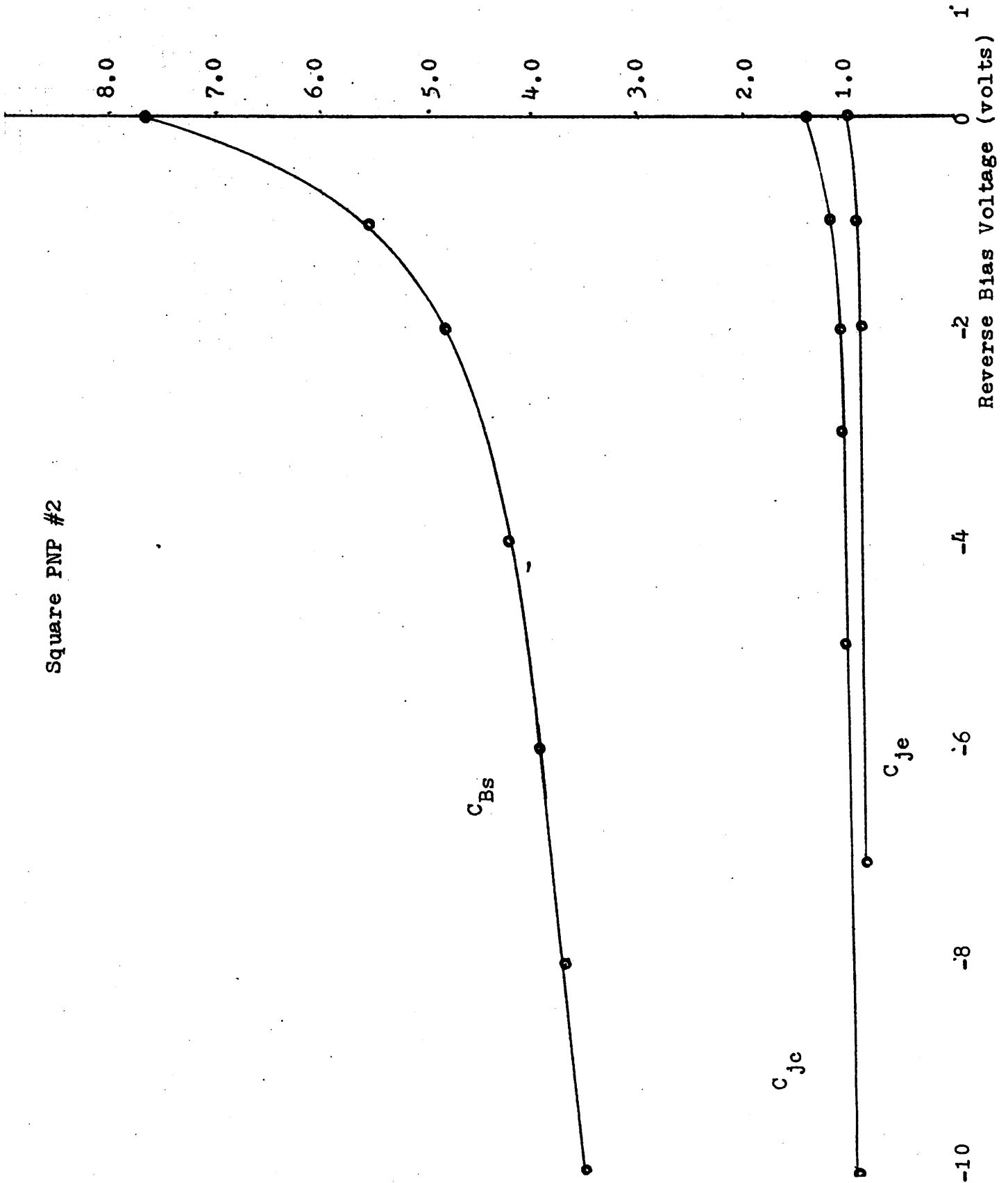


Fig. C.24

Capacitance (pf)

Round PNP #2

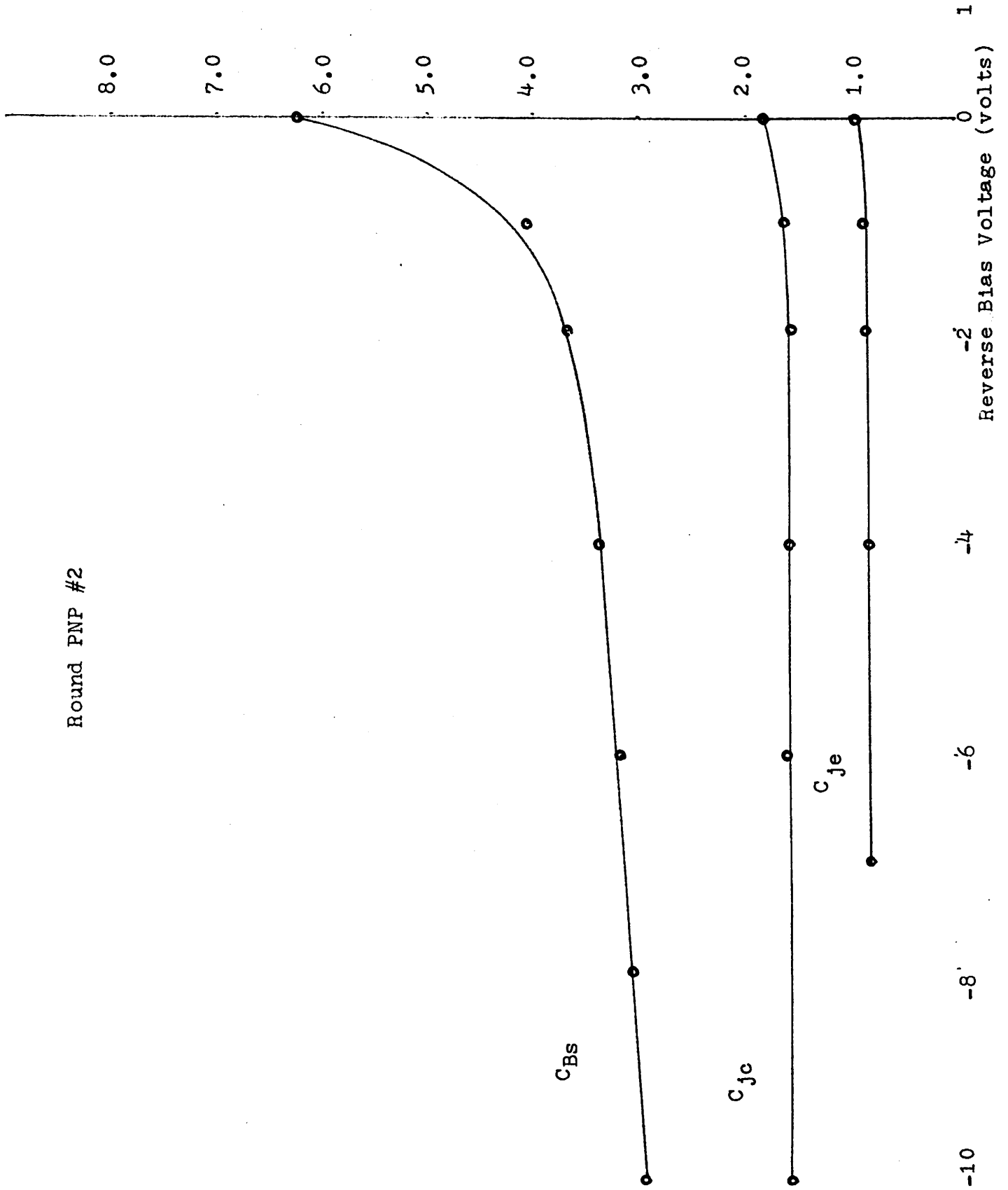


Fig. C.25



Capacitance (pf)

Substrate PNP #2

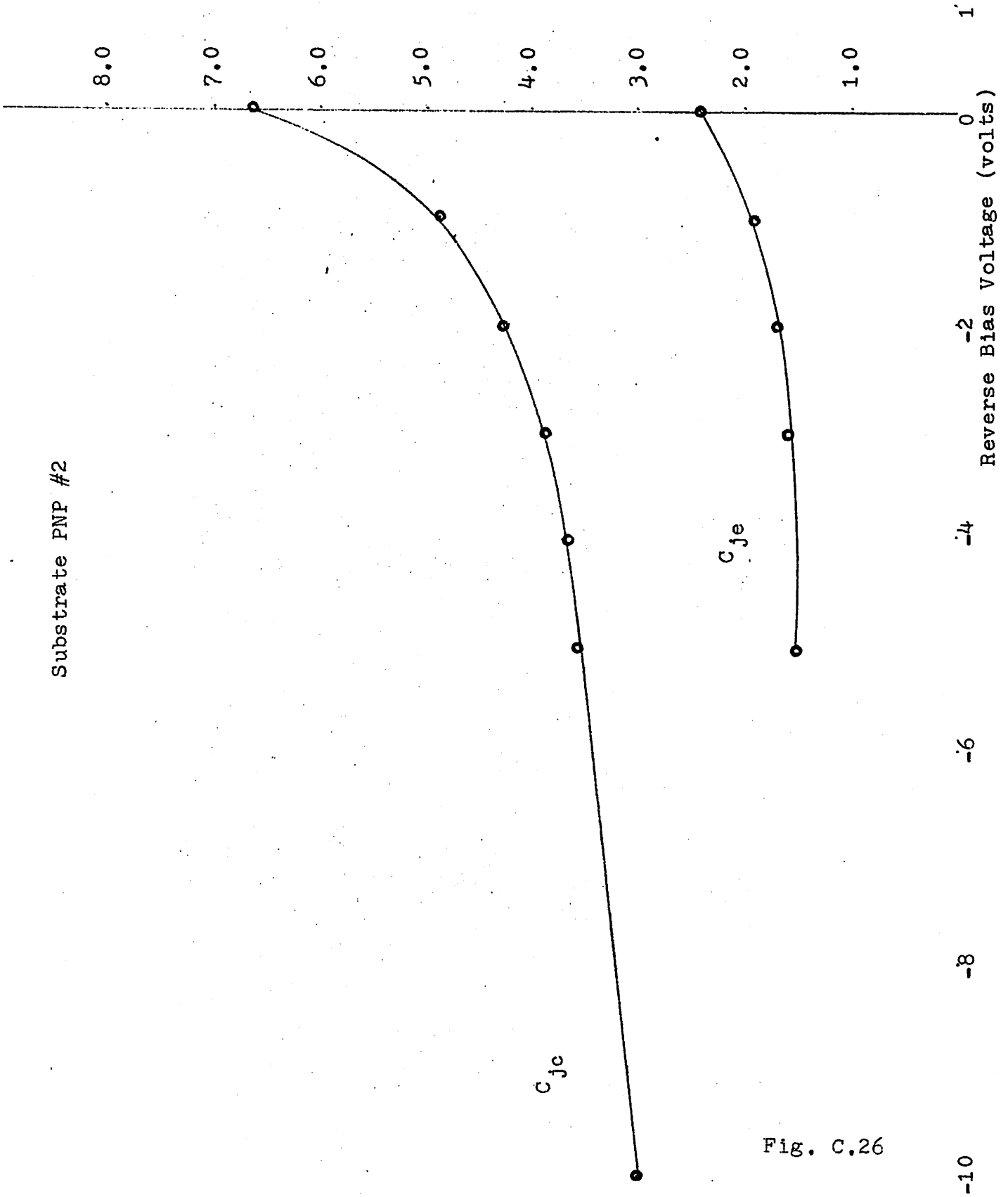


Fig. C.26

Capacitance (pf)

Small NPN #1

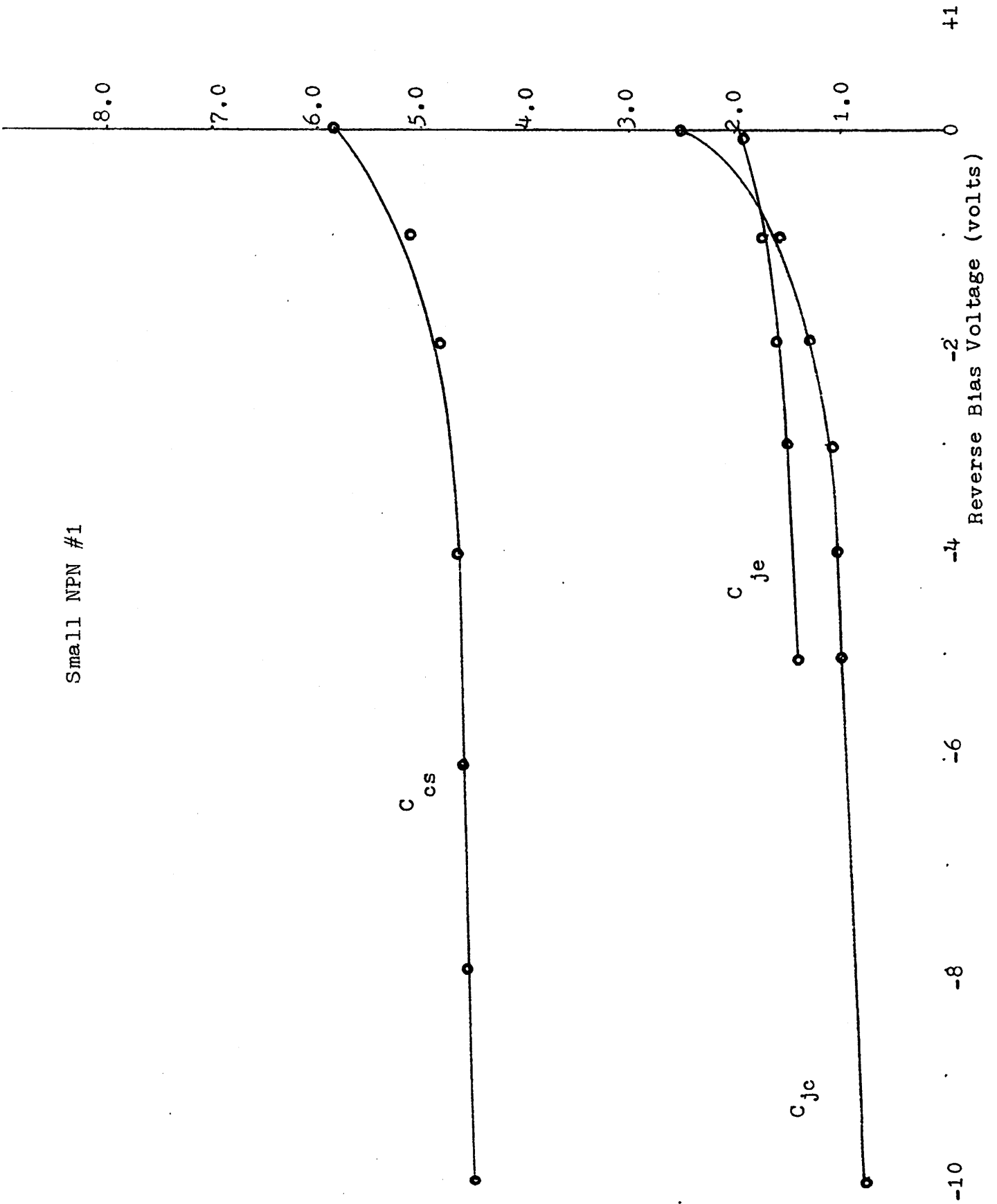


Fig. C.27

Capacitance (pf)

Round NPN #1

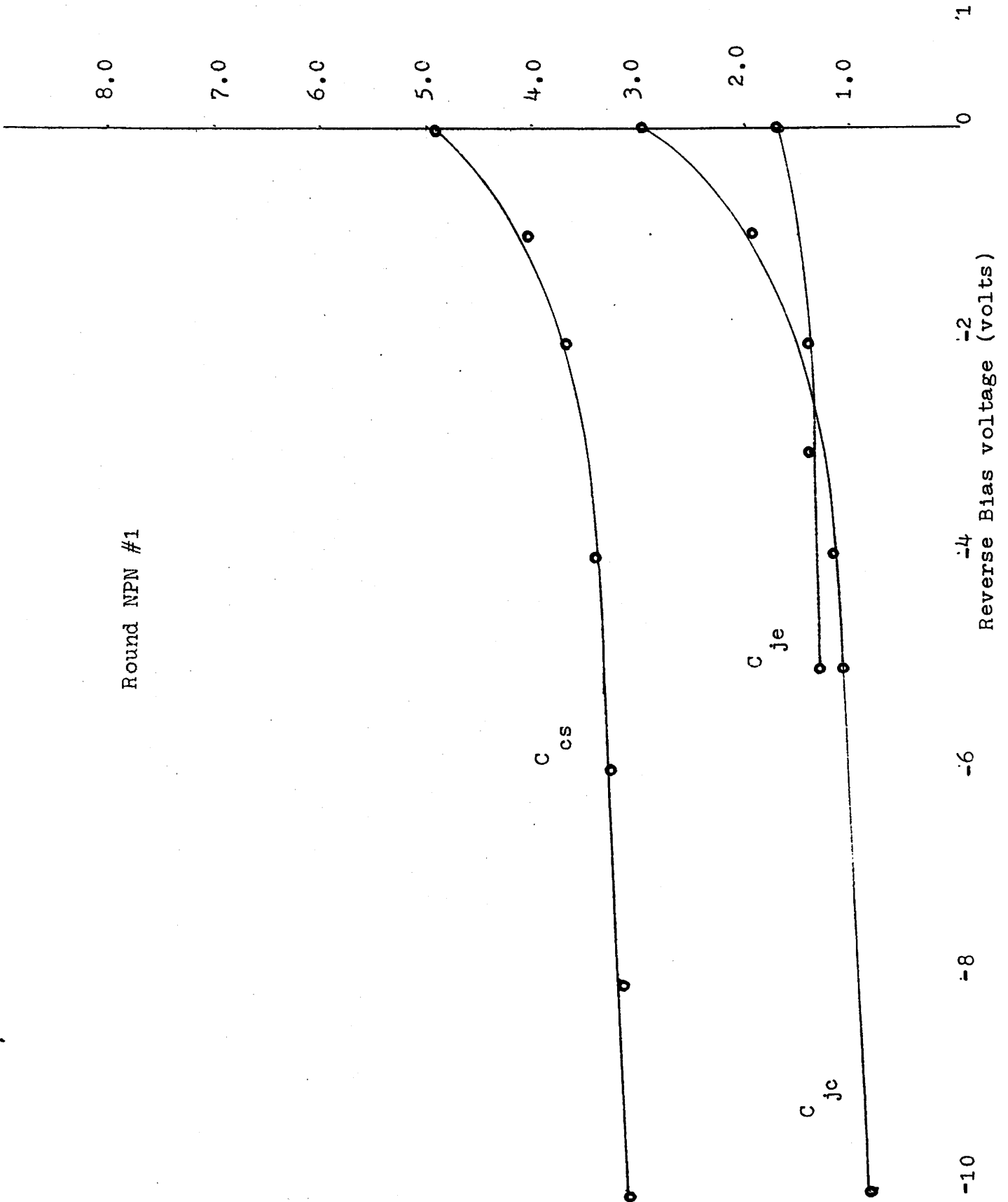


Fig. C.28

Capacitance (pf)

Large NPN #1

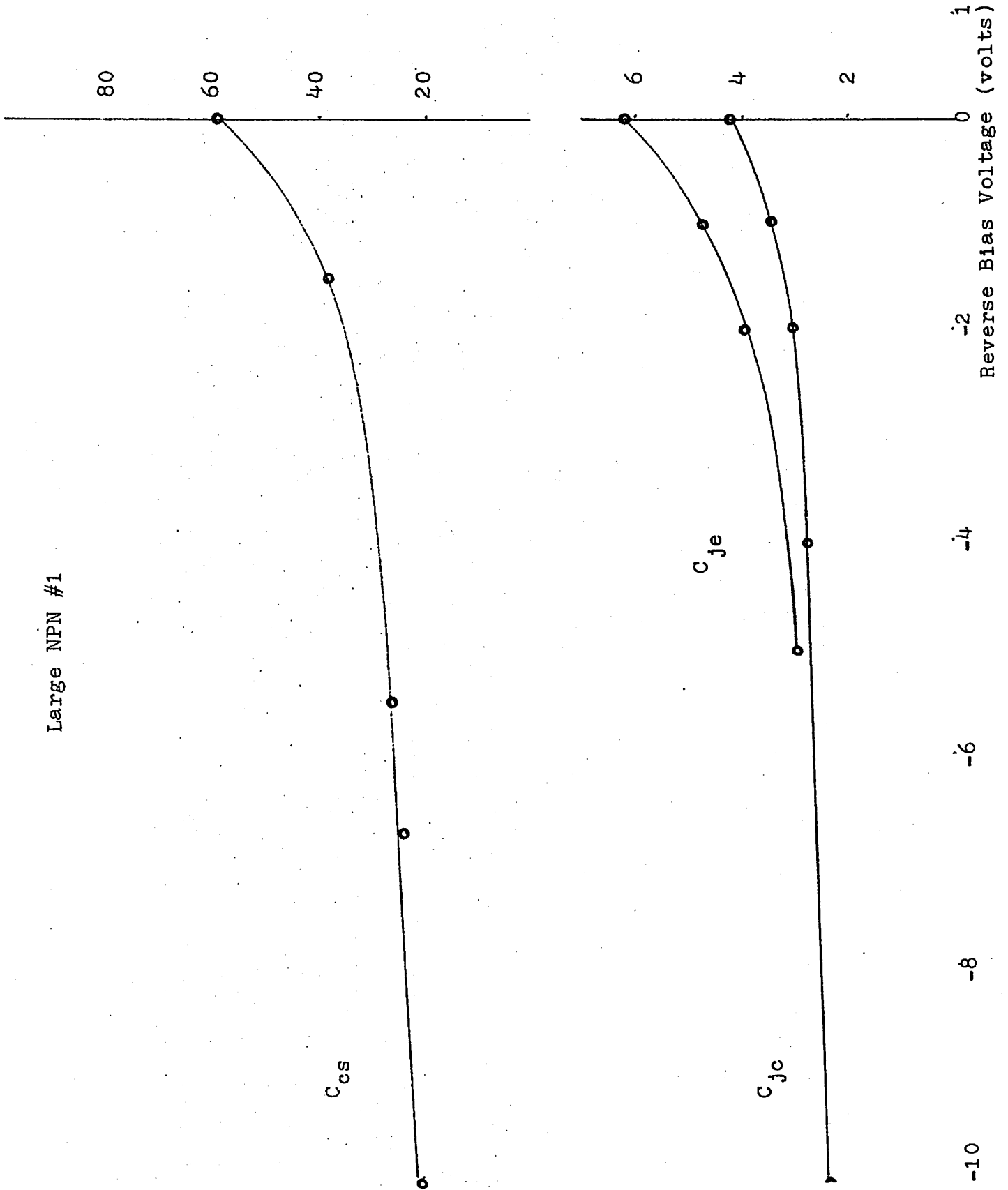


Fig. C.29

Square PNP #1

Capacitance (pf)

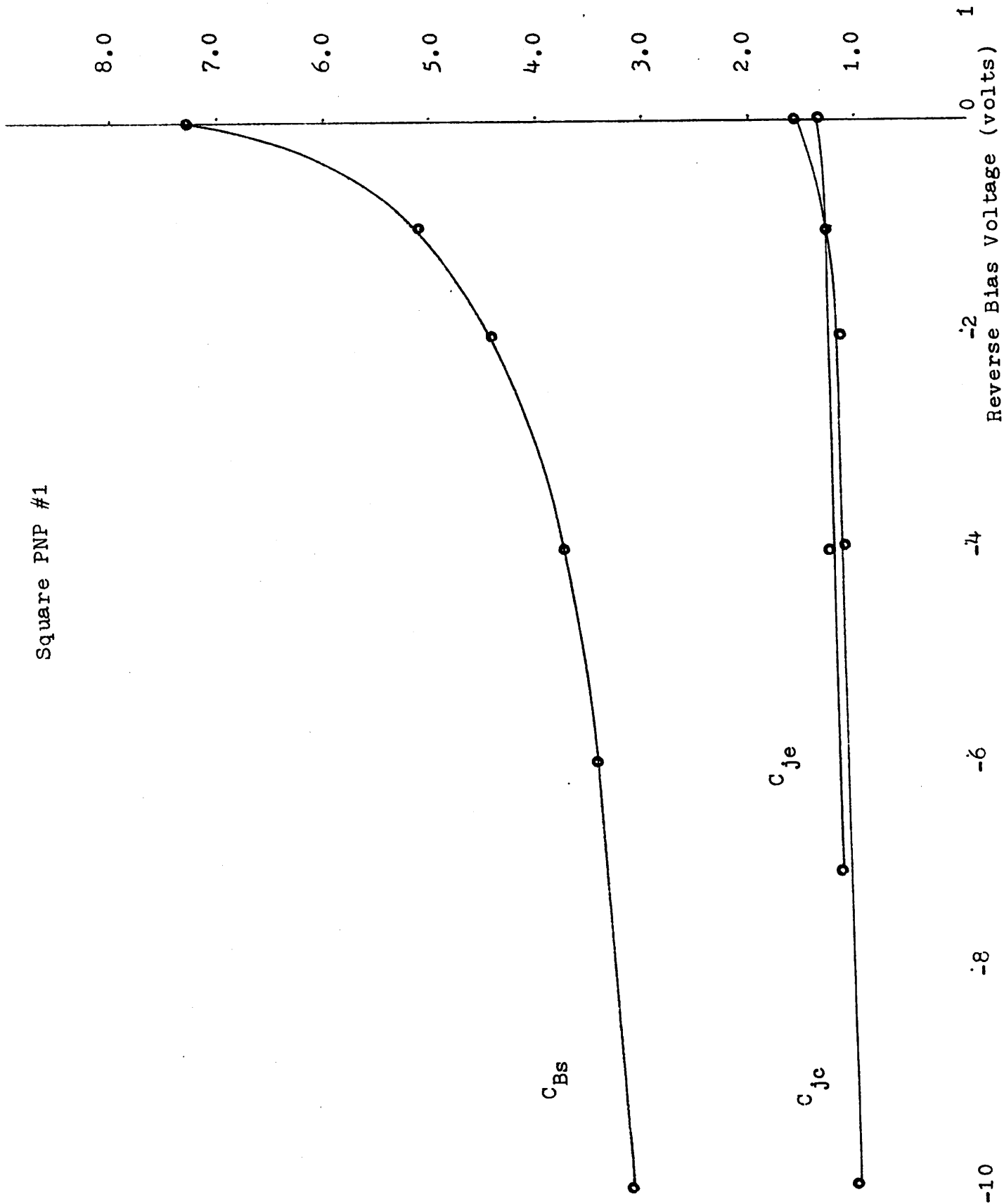


Fig. C.30  
Fig. C.31

Round PNP #1

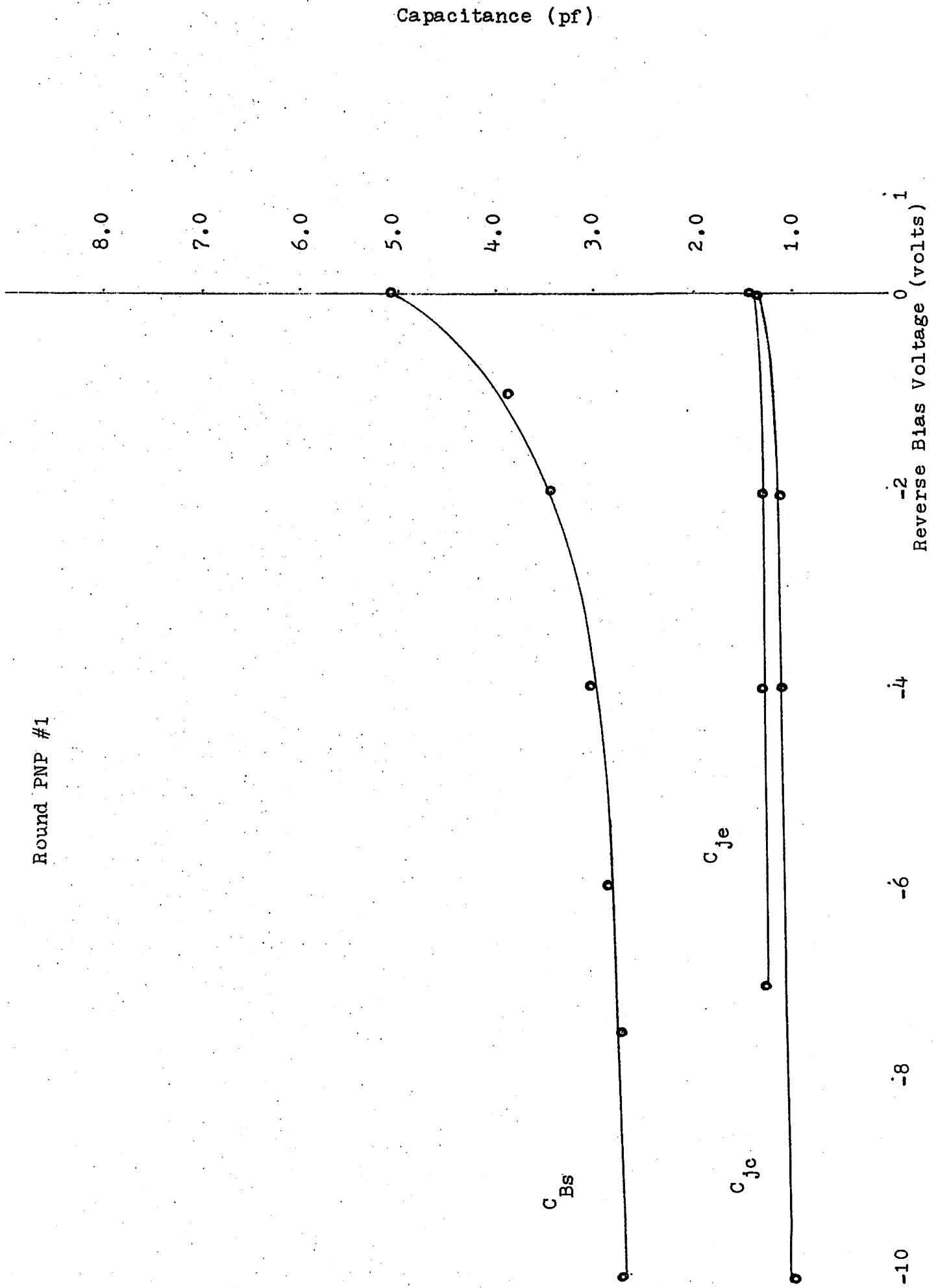


Fig. C.31

Capacitance (pf)

Substrate PNP #

Reverse Bias Voltage (volts)

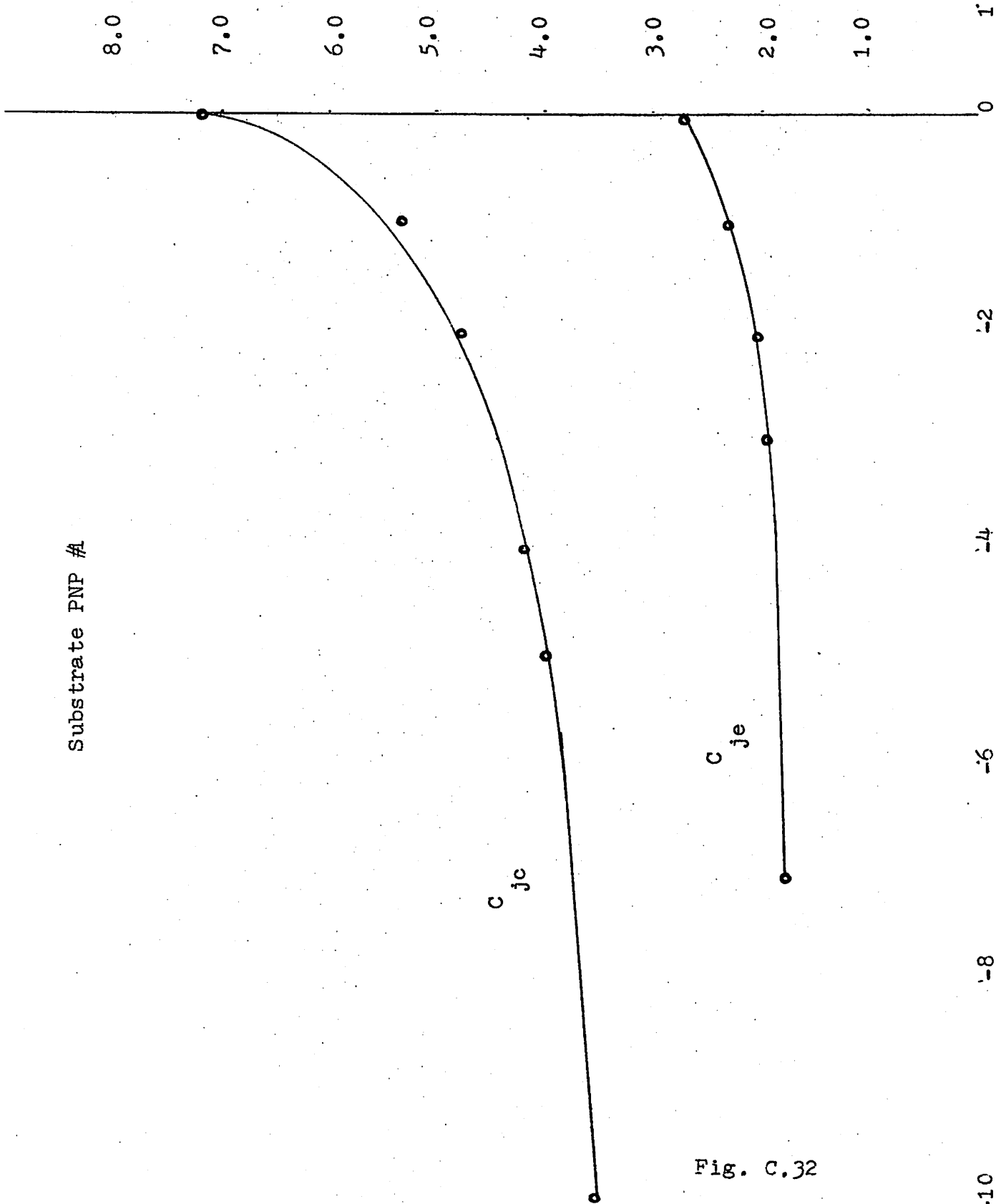


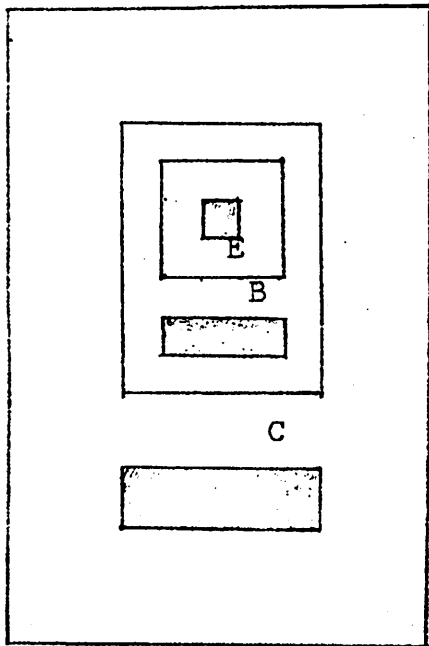
Fig. C.32

## Appendix D

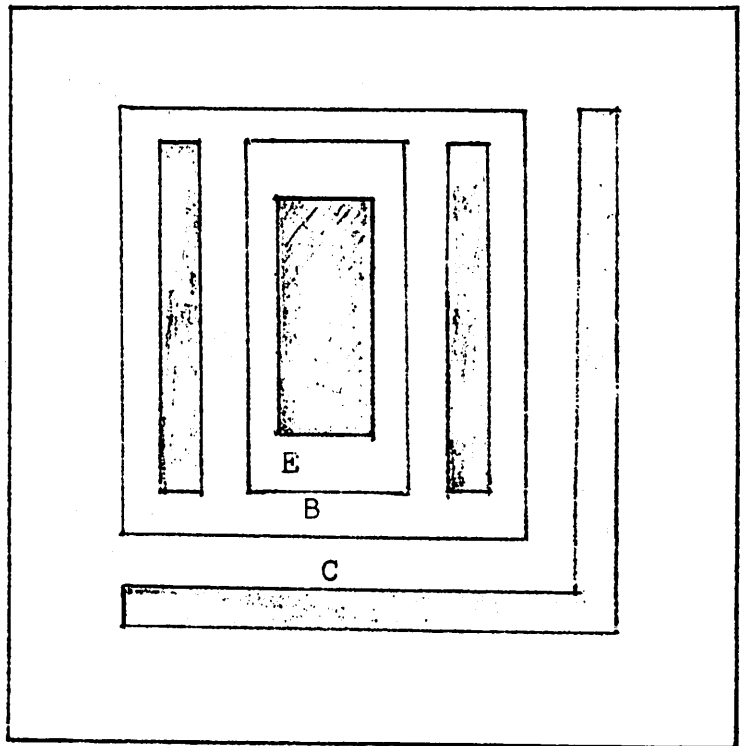
Device Geometry

There are basically six kinds of devices used in the 741 and the ULX 2139. Fig. D.1 shows the top view of each of these devices in magnified scale. To identify the type of device used for each transistor in the amplifier one should refer back to the photomicrographs that are shown in Fig. 1.1b and Fig.1.2b.

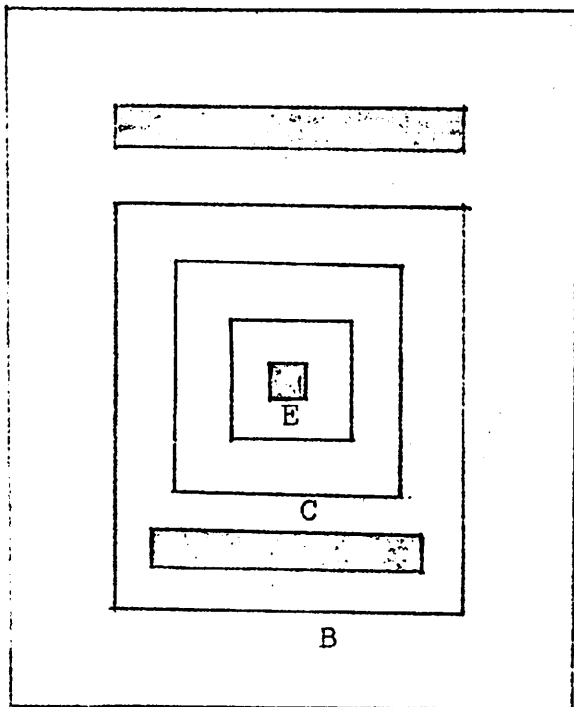




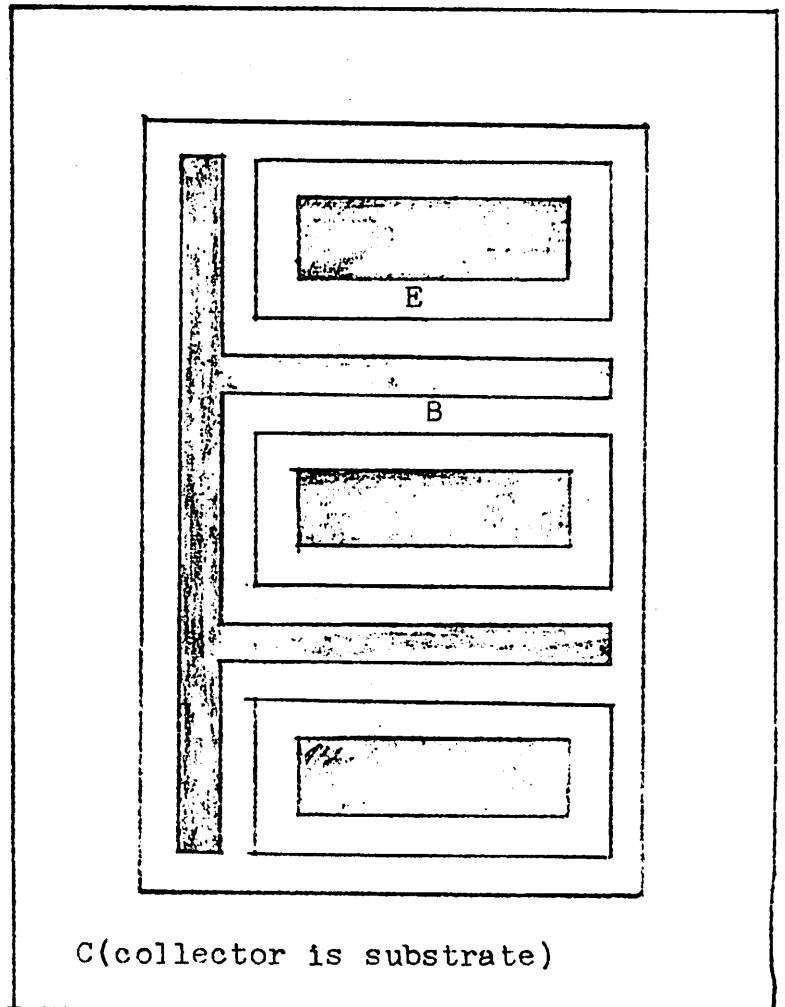
(1) Small NPN  
2 x 2 mils emitter  
(estimate)



(2) Large NPN



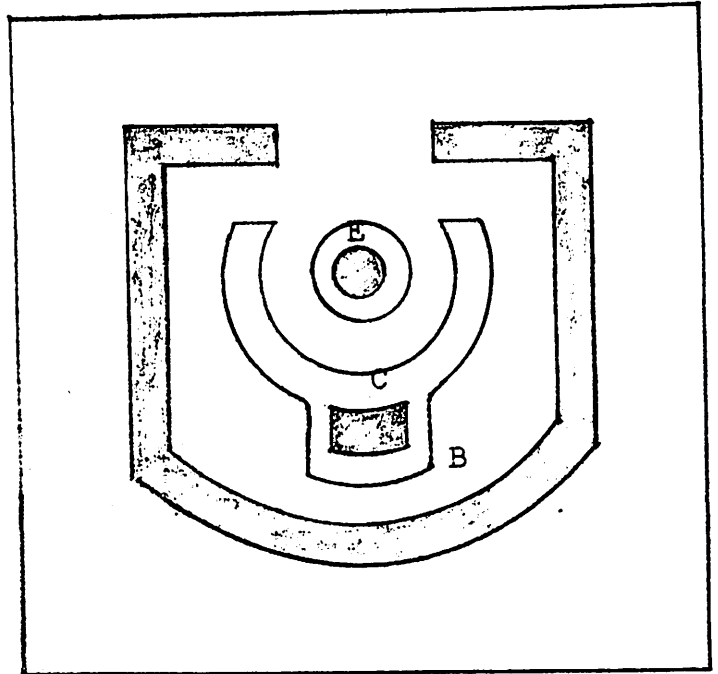
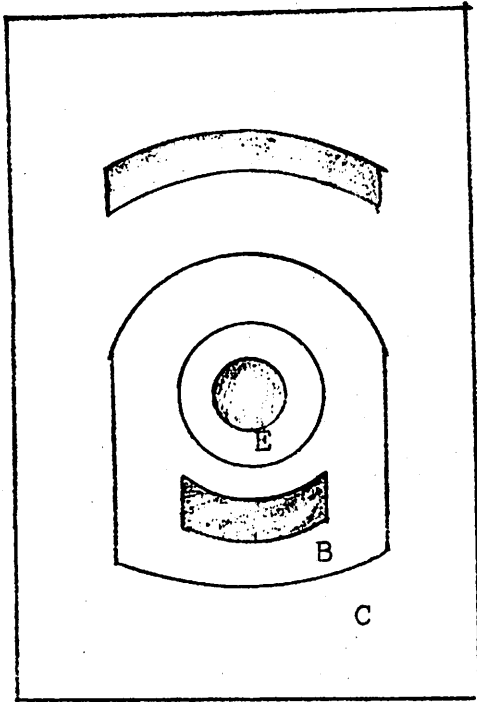
(3) Lateral PNP



C(collector is substrate)

(4) Large Substrate PNP

Fig. D.1  
Device geometry



(5) Round small npn

(used only in the ULX 2139)

(6) Round lateral PNP

(used only in the ULX 2139)

Fig. D.1 Device geometry (continued)

References

- (1) David Fullagar, "A New High Performance Monolithic Amplifier Design ", Fairchild Semiconductor Technical Paper, 1968.
- (2) Gray, Dewitt, Boothroyd and Gibbons, "Physical Electronics and Circuit Models of Transistors", SEEC Volume II, Wiley, 1964.
- (3) A.S. Grove, "Physics and Technology of Semiconductor Device", John Wiley and Sons, Inc., N.Y., 1967.
- (4) D.O. Pederson, " Electronic Circuits", Preliminary edition, McGraw-Hill Book Co.
- (5) J.E. Solomon, Davis and Lee, "A Self-Compensated Monolithic Op-Amp with Low Input Current and High Slew Rate", IEEE International Solid-State Circuits Conference, 1969.
- (6) Gantam R. Patel, "A Study of the Output Stages of High Performance Operational Amplifiers", MS Plan II report, 1969, U.C., Berkeley.
- (7) Michael Schwartz, "Input Stages of New Monolithic Operational Amplifiers", MS Plan II report, June, 1969, U.C., Berkeley.
- (8) B.A. Wooley and D.O. Pederson, "A computer-Aided Evaluation of New Integrated Circuit Operational Amplifiers", NEREM Record, 1969, pp88-89.