AN IMPROVED VERSION OF SLIC

by

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ABSTRACT

SLIC is a computer program which simulates and analyses linear integrated circuits. SLIC performs the following four types of analyses: nonlinear dc analysis, linear small-signal analysis, noise analysis, and sensitivity analysis. The dc analysis computes the dc node voltages and the transistor operating points. The small-signal analysis first generates linearized small-signal transistor models and then computes the poles and zeros and/or frequency response of a specified transfer function. The noise analysis computes the the equivalent thermal and shot noise sources and at five frequencies computes the noise at the output port. The sensitivity analysis computes the sensitivities (partial derivatives) of the transistor operating points and the specified transfer function (at five frequencies) with respect to specified passive circuit elements. In addition SLIC allows the temperature and a single dc source to be varied and also allows analyses of altered versions of the original circuit.

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I. INTRODUCTION

The SLIC (simulator for linear integrated circuits) program has undergone a number of modifications and additions since the original work of Idleman [1] [2] was completed. Larger circuits (up to 100 nodes) can be simulated and simulation times have been reduced with the implementation of sparse matrix techniques. Voltage-controlled current sources, mutual inductors, and junction and MOS field-effect transistor models have been added. The option to plot a specified dc voltage as a single source is varied (dc transfer curve) has been added. The provision to bypass the dc analysis and proceed directly into a small-signal analysis has also been included. The implementation of Muller's method which is used to compute poles and zeros has been modified to reduce pole-zero computation times. The optional noise analysis now computes the rms output port noise generated by each equivalent thermal and shot noise source at up to five user specified frequencies. Previously, only the total rms output noise was computed. An optional sensitivity analysis has been added which computes the sensitivities (partial derivatives) of the transistor junction voltages with respect to certain user specified passive circuit elements. At up to five user specified frequencies, the sensitivities of a defined transfer function with respect to the transistor small-signal parameters and the selected passive elements are also computed. The input data format has been modified to allow the use of keywords in the description of transistor

models. Of the above modifications and additions, William McCalla was responsible for implementing sparse matrix techniques, adding mutual inductors, modifying the implementation of Muller's method, and adding the sensitivity analysis.

The bipolar transistor model used in SLIC is described by McCalla [3]. The dc model is a nonlinear hybrid-pi equivalent of the Ebers and Moll transport model [4]. Incorporated in this model are basewidth modulation effects, a current-dependent short-circuit dc current gain β_F, high level injection effects, and temperature-dependent effects. A linear, small-signal hybrid-pi model is used for the small-signal analyses. The junction and MOS field-effect transistor models used are based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11].

SLIC consists of approximately 5100 Fortran statements and has a field length of 41000 decimal words. It is capable of simulating and analyzing circuits of up to 100 nodes with the following limitations: 40 resistors, 20 capacitors, 20 inductors, 20 voltage-controlled current sources, 10 mutual inductors, 30 bipolar and field-effect transistors, 10 bipolar transistor models, 10 field-effect transistor models, 10 current sources, and 10 grounded voltage sources.

II. USER'S GUIDE

This section contains the SLIC user's guide which describes the input data language and the various analysis options. An example is also included to illustrate circuit and analysis descriptions.

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USERS GUIDE FOR SLIC VERSION H

GENERAL PROGRAM DESCRIPTION

SLIC SOLVES FOR THE DC NODE-TO-DATUM VOLTAGES, TRANSISTOR OPERATING POINTS, SMALL-SIGNAL POLES, ZEROS, AND FREQUENCY RESPONSE, NOISE PERFORMANCE, AND SENSITIVITY OF CIRCUITS CONTAINING RESISTORS, CAPACITORS, INDUCTORS, VOLTAGE-CONTROLLED CURRENT SOURCES, MUTUAL INDUCTORS, BIPOLAR TRANSISTORS, JUNCTION AND MOS FIELD-EFFECT TRANSISTORS, CURRENT SOURCES, AND GROUNDED VOLTAGE SOURCES. SLIC ALLOWS THE USER TO CHOOSE A COMBINATION OF THE ABOVE TYPES OF ANALYSES. ANALYSES MAY BE REPEATED FOR SEVERAL DIFFERENT TEMPERATURES AND/OR FOR SEVERAL DIFFERENT VALUES OF ANY DC SOURCE.

THE NONLINEAR BIPOLAR TRANSISTOR MODEL IS EQUIVALENT TO THAT OF EBERS AND MOLL WITH BASEWIDTH MODULATION EFFECTS AND A CURRENT-DEPENDENT BETA INCORPORATED AND THE SMALL-SIGNAL MODEL IS THE EXTRINSIC HYBRID-PI. THE MODELS FOR BOTH JUNCTION AND MOS FIELD-EFFECT TRANSISTORS ARE BASED ON THE INSULATED-GATE FIELD-EFFECT TRANSISTOR MODEL OF SHICHMAN AND HODGES.

PROGRAM LIMITATIONS

100 NODES + DATUM NODE (NUMBERED 0)
40 RESISTORS
20 CAPACITORS
20 INDUCTORS
20 VOLTAGE-CONTROLLED CURRENT SOURCES
10 MUTUAL INDUCTORS
10 BIPOLAR TRANSISTOR MODELS
10 FIELD-EFFECT TRANSISTOR MODELS
30 TRANSISTORS OF THE FOLLOWING TYPES -
BIPOLAR TRANSISTORS (NPN OR PNP)
JUNCTION FIELD-EFFECT TRANSISTORS (N OR P CHANNEL)
MOS FIELD-EFFECT TRANSISTORS (N OR P CHANNEL)
10 CURRENT SOURCES
10 GROUNDED VOLTAGE SOURCES

REMARKS

THE FOLLOWING ARE GENERAL COMMENTS CONCERNING CHARACTERISTICS AND LIMITATIONS OF THE PROGRAM.

1) JOBS MAY BE BATCHED BY PLACING THEM SEQUENTIALLY -- A TITLE CARD FOR EACH NEW JOB FOLLOWING THE END CARD OF THE PRECEEDING JOB.

2) ALL ELEMENT NAMES MUST BE UNIQUE. REPETITION OF A NAME WILL CAUSE ITS PREVIOUS OCCURANCE TO BE DELETED OR REPLACED. NAMES MUST NOT CONTAIN ANY DELIMITERS (BLANKS, COMMAS, EQUAL SIGNS, AND PARENTHESES).

3) THE GROUND OR DATUM NODE MUST BE NUMBERED 0.

4) THE USE OF EACH OHMIC BASE, COLLECTOR, DRAIN, AND SOURCE RESISTANCE IN TRANSISTORS CREATES AN EXTRA NODE IN THE CIRCUIT.

CONVERGENCE

OHMIC BASE, COLLECTOR, DRAIN, AND SOURCE RESISTANCES CAN BE INCLUDED IN THE TRANSISTOR MODELS. IN SOME INSTANCES, WHERE STRINGS OR LOOPS OF TRANSISTORS AND DIODE-CONNECTED TRANSISTORS ARE PRESENT, CONVERGENCE CAN BE IMPROVED BY THE INCLUSION OF THESE OHMIC RESISTANCES.

BIPOLAR TRANSISTOR OPERATING POINT VARIATIONS

FOR A NONLINEAR DC ANALYSIS, THE DEPENDENCE OF THE OUTPUT CONDUCTANCE ON COLLECTOR CURRENT IS MODELED. THE DEPENDENCE OF THE FORWARD TRANSISTOR BETA ON COLLECTOR CURRENT ALSO CAN BE MODELED. BETA IS ASSUMED TO FALLOFF AT LOW CURRENTS AS THE ONE-HALF POWER AND TO FALLOFF LINEARLY AT HIGH CURRENTS. OUTPUT CONDUCTANCE IS ASSUMED TO VARY LINEARLY WITH COLLECTOR CURRENT. FOR A LINEAR, SMALL-SIGNAL ANALYSIS, THE DEPENDENCE OF COMPUTED SMALL-SIGNAL BETA CAN BE MODELED WITH RESPECT TO COLLECTOR CURRENT. TRANSIT TIME AND JUNCTION CAPACITANCES ARE MODELED WITH RESPECT TO JUNCTION VOLTAGES.

TEMPERATURE ANALYSIS

THE TEMPERATURE SENSITIVITY OF DC OPERATING POINTS AND SMALL-SIGNAL PERFORMANCE CAN BE ANALYZED THROUGH AUTOMATIC VARIATIONS OF RESISTOR, CAPACITOR, INDUCTOR, VOLTAGE-CONTROLLED CURRENT SOURCE, AND MUTUAL INDUCTOR VALUES AND TRANSISTOR PARAMETERS WITH TEMPERATURE. THE USER CAN SPECIFY VALUES FOR THESE PARAMETERS EFFECTIVE AT A NOMINAL TEMPERATURE (TNOM). ALSO USER SPECIFIED ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS FOR THE ABOVE STATED ELEMENTS AND BIPOLAR TRANSISTOR BETAS, OHMIC BASE RESISTANCES, AND OHMIC COLLECTOR RESISTANCES. THE NOMINAL TEMPERATURE VALUES ARE THEN MULTIPLIED BY THE FACTOR

$$1 + TC1 * (T - TNOM) + TC2 * (T - TNOM)**2$$

WHERE T IS THE TEMPERATURE OF INTEREST AND TC1 AND TC2 ARE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY. BIPOLAR TRANSISTOR JUNCTION SATURATION CURRENTS, OUTPUT CONDUCTANCE, TRANSIT TIME, AND JUNCTION CAPACITANCES ARE VARIED FOR BOTH LARGE AND SMALL-SIGNAL ANALYSES ACCORDING TO THE THEORETICALLY DERIVED RELATIONSHIPS FOR SILICON TRANSISTORS.

INPUT DATA FORMAT.

THE INPUT DATA FORMAT OF SLIC IS OF THE FREE FORMAT TYPE. FIELDS ON A CARD ARE SEPARATED BY ONE OR MORE DELIMITERS. BLANKS, COMMAS, EQUAL SIGNS, LEFT PARENTHESES, AND RIGHT PARENTHESES ARE ALL DELIMITERS.

ALL CARDS MUST BEGIN WITH A NAME FIELD STARTING IN COLUMN 1, WITH THE EXCEPTION OF TITLE CARDS, COMMENT CARDS, AND CONTINUATION CARDS.

A NAME FIELD MUST CONTAIN FROM ONE TO FOUR CHARACTERS. ANY TRAILING CHARACTERS ARE IGNORED. THE FIRST CHARACTER OF A NAME FIELD MUST BE A LETTER AND ONLY CERTAIN LETTERS WHICH ARE DESCRIBED BELOW IN THE GUIDE MAY BE USED. THE REMAINING (UP TO THREE) CHARACTERS MAY BE COMPOSED OF ANY COMBINATION OF ALPHANUMERIC CHARACTERS EXCEPT DELIMITERS.

A NUMERIC FIELD MAY BE AN INTEGER FIELD (12, -44), A FLOATING POINT FIELD (3.14159), EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY AN INTEGER EXPONENT (1E-14, 2.65E0), OR EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY ONE OF THE FOLLOWING SCALE FACTORS -

G	1.0E+9
MEG	1.0E+6
K	1.0E+3
M	1.0E-3
U	1.0E-6
N	1.0E-9
P	1.0E-12

ANY LETTERS IMMEDIATELY FOLLOWING A NUMBER THAT ARE NOT SCALE FACTORS ARE IGNORED, AND ANY LETTERS IMMEDIATELY FOLLOWING A SCALE FACTOR ARE IGNORED. HENCE 10, 10V, 10VOLTS, AND 10HZ ALL REPRESENT THE SAME NUMBER, AND M, MA, MSEC, AND MMHOS ALL REPRESENT THE SCALE FACTOR M. NOTE THAT 1000, 1000.0, 1000HZ, 1E3, 1.0E3, 1KHZ, AND 1K ALL REPRESENT THE SAME NUMBER. VALUES IN NUMERIC FIELDS MAY BE DEFAULTED BY A SLASH, /, AND DELIMITERS NEED NOT BE USED BETWEEN SUCCESSIVE SLASHES. FOR EXAMPLE, THE GROUP OF NUMBER FIELDS (10K//9.6U) IS EQUIVALENT TO (10K 0.0 0.0 9.6U).

CONTINUATION CARDS ARE BEGUN WITH A PLUS, +, IN COLUMN 1 AND MAY BE USED IN DESCRIBING TRANSISTOR MODELS, VARIABLE CURRENT SOURCES, AND VARIABLE GROUNDED VOLTAGE SOURCES.

THE FIRST CARD OF AN INPUT DECK MUST BE A TITLE CARD AND THE LAST CARD AN END CARD. THE ORDER OF ALL OTHER CARDS IS ARBITRARY.

CONTROL CARDS

1) TITLE CARD -- A CARD WHOSE CONTENTS ARE PRINTED OUT VERBATIM AT THE HEAD OF EACH SECTION OF OUTPUT.

EXAMPLE -

```
SOLOMON AND WILSON SERIES-SERIES TRIPLE BROADBAND AMPLIFIER
```

2) COMMENT CARDS -- CARDS (OPTIONAL) WHOSE CONTENTS ARE PRINTED OUT VERBATIM WHEN READ.

EXAMPLE -

```
*  OPEN LOOP -- NO FEEDBACK
```

COLUMN 1 MUST CONTAIN AN ASTERISK, *. THE REST OF THE CARD MAY CONTAIN ANY COMMENTS.

3) PRINT CARD -- A CARD WHICH SPECIFIES THE TYPE OF DC AND/OR SMALL-SIGNAL ANALYSIS DESIRED.

GENERAL FORM -

```
PRINT DCMODE ACMODE VAR(PTS,FMIN,FMAX) OUTPUT(NO+,NO-) INPUT(NI+,NI-)
```

EXAMPLES -

```
PRINT DC PZ FLOG(10,1HZ,100MEGHZ) VOUT(7,0) IIN(1,C)
PRINT    AC    FLIN 10 95KHZ 105KHZ    VOUT 15 0    VIN 2 C
PRINT  DC
```

DCMODE IS THE LETTERS DC IF A DC ANALYSIS IS DESIRED OR BLANK IF NONE IS DESIRED.

ACMODE IS THE LETTERS PZ IF POLES AND ZEROS (WITH OR WITHOUT A FREQUENCY RESPONSE) ARE DESIRED, THE LETTERS AC IF ONLY A FREQUENCY RESPONSE IS DESIRED, OR BLANK IF NEITHER IS DESIRED.

IF ACMODE IS PZ TWO OPTIONAL NUMERIC FIELDS MAY IMMEDIATELY FOLLOW THE LETTERS PZ. THE FIRST NUMERIC FIELD IS THE UPPER FREQUENCY LIMIT FOR POLES AND THE SECOND NUMERIC FIELD IS THE UPPER FREQUENCY LIMIT FOR ZEROS. THESE LIMITS ARE SPECIFIED IN HERTZ. IF EITHER NO POLES OR NO ZEROS ARE DESIRED, THE NUMBER 0 (ZERO) SHOULD BE SPECIFIED. THE SPECIFICATION OF A / (SLASH) WILL CAUSE ALL POLES OR ZEROS TO BE FOUND.

THE VAR SPECIFICATIONS MUST BE PRESENT IF ACMODE IS AC. IF ACMODE IS PZ AND A FREQUENCY RESPONSE IS ALSO DESIRED, THEN THE VAR SPECIFICATIONS SHOULD BE PRESENT. TWO TYPES OF FREQUENCY VARIATION ARE ALLOWED. VAR IS THE LETTERS FLOG FOR A LOGARITHMIC VARIATION AND PTS IS THE NUMBER OF FREQUENCY POINTS PER

DECADE. FMIN IS THE STARTING FREQUENCY AND FMAX IS THE FINAL FREQENCY. VAR IS THE LETTERS FLIN FOR A LINEAR VARIATION AND PTS IS THE NUMBER OF FREQUENCY POINTS STARTING WITH FMIN AND ENDING WITH FMAX.

THE OUTPUT AND INPUT SPECIFICATIONS SPECIFY THE TRANSFER OR DRIVING POINT FUNCTION FOR POLES AND ZEROS AND/OR FREQUENCY RESPONSE. OUTPUT IS THE LETTERS VOUT FOR VOLTAGE OUTPUT OR THE LETTERS ICUT FOR CURRENT OUTPUT AND NO+ AND NO- ARE THE POSITIVE AND NEGATIVE OUTPUT NODES, RESPECTIVELY. INPUT IS THE LETTERS VIN FOR VOLTAGE INPUT OR THE LETTERS IIN FOR CURRENT INPUT AND NI+ AND NI- ARE THE POSITIVE AND NEGATIVE INPUT NODES, RESPECTIVELY.

4) DC CARD -- A CARD (OPTIONAL) WHICH SPECIFIES THE PLOTTING OF A DC TRANSFER CURVE. A SPECIFIED DC OUTPUT VOLTAGE IS PLOTTED AS A SINGLE VOLTAGE OR CURRENT SOURCE IS VARIED. THE NUMBER OF POINTS PLOTTED CANNOT EXCEED 101.

GENERAL FORM -

```
DC SNAME START STOP STEP ONAME N1 N2
```

EXAMPLES -

```
DC VS -0.5 +0.5 40MV VOUT 7 0
DC II 0.0 1MA 10UA V34 3 4
```

SNAME IS THE NAME OF THE VOLTAGE OR CURRENT SOURCE THAT IS VARIED. THIS SOURCE MUST ALSO BE SPECIFIED ON A *VOLTAGE OR CURRENT SOURCE CARD*. START IS THE INITIAL SOURCE VALUE, STOP IS THE FINAL SOURCE VALUE, AND STEP IS THE INCREMENT. ONAME IS THE NAME OF THE OUTPUT VOLTAGE WHICH EXISTS BETWEEN NODES N1 AND N2.

5) TEMPERATURE CARD -- A CARD (OPTIONAL) WHICH SPECIFIES THE NOMINAL TEMPERATURE AND UP TO FIVE TEMPERATURES AT WHICH THE CIRCUIT IS TO BE ANALYZED. TEMPERATURES ARE SPECIFIED IN DEGREES KELVIN. IF THIS CARD IS OMITTED, AN ANALYSIS IS PERFORMED AT THE ASSUMED NOMINAL TEMPERATURE OF 300 DEGREES KELVIN. IF ONLY THE NOMINAL TEMPERATURE IS SPECIFIED, A SINGLE ANALYSIS IS PERFORMED AT THIS TEMPERATURE. THIS CARD HAS NO EFFECT ON A TRANSISTOR WHICH HAS A TEMPERATURE SPECIFIED ON ITS *TRANSISTOR CARD*.

GENERAL FORM -

```
TEMP TNOM T1 T2 T3 T4 T5
```

EXAMPLES -

```
TEMP 300 300 305 310
TEMP  298
```

TNOM IS THE NOMINAL TEMPERATURE. T1, T2, T3, T4, AND T5 ARE THE UP TO FIVE TEMPERATURES AT WHICH THE CIRCUIT IS TO BE ANALYZED. IN THE FIRST EXAMPLE ABOVE, TNOM IS 300 DEGREES AND THE CIRCUIT IS ANALYZED AT 300, 305 AND 310 DEGREES. IN THE SECOND EXAMPLE, ONLY ONE ANALYSIS IS PERFORMED AT THE NOMINAL TEMPERATURE OF 298 DEGREES.

6) NOISE CARD — A CARD (OPTIONAL) WHICH SPECIFIES UP TO FIVE FREQUENCIES AT WHICH NOISE ANALYSES ARE TO BE PERFORMED. THE EQUIVALENT SHOT AND THERMAL NOISE SOURCES FOR THE DC CIRCUIT ARE COMPUTED AND PRINTED. FOR EACH FREQUENCY SPECIFIED, THE RMS NOISE CONTRIBUTION AT THE OUTPUT PORT FROM EACH EQUIVALENT NOISE SOURCE IS COMPUTED AND PRINTED. THE TOTAL RMS NOISE AT THE OUTPUT PORT AND THE TOTAL RMS NOISE REFERRED TO THE INPUT PORT ARE ALSO PRINTED AT EACH FREQUENCY. A BANDWIDTH OF 1 HERTZ IS ASSUMED IN THE NOISE CALCULATIONS.

GENERAL FORM -

```
NOISE F1 F2 F3 F4 F5
```

EXAMPLE -

```
NOISE  1KHZ 10KHZ 100KHZ 1MEGHZ
```

F1, F2, F3, F4, AND F5 ARE THE UP TO FIVE FREQUENCIES AT WHICH THE NOISE ANALYSIS IS TO BE PERFORMED.

7) SENSITIVITY CARD — A CARD (OPTIONAL) WHICH SPECIFIES UP TO FIVE FREQUENCIES AT WHICH SENSITIVITY (PARTIAL DERIVATIVE) ANALYSES ARE TO BE PERFORMED. ONLY SENSITIVITIES WITH RESPECT TO THE PASSIVE ELEMENTS (R, C, L, AND G) CAN BE PERFORMED. ALSO, THE CARDS OF THE PASSIVE ELEMENTS OF INTEREST MUST CONTAIN THE LETTER V IN THE FIELD IMMEDIATELY FOLLOWING THE SECOND-ORDER TEMPERATURE COEFFICIENT. NOTE THAT FOR RESISTORS AND INDUCTORS, THE COMPUTED SENSITIVITIES ARE WITH RESPECT TO THEIR RECIPROCALS (I. E. 1/R AND 1/L).

GENERAL FORM -

```
SENS  F1 F2 F3 F4 F5
```

EXAMPLE -

```
SENS  1MEGHZ  10MEGHZ
```

F1, F2, F3, F4, AND F5 ARE THE UP TO FIVE FREQUENCIES AT WHICH THE SENSITIVITY ANALYSIS IS TO BE PERFORMED.

8) ALTER CARD — A CARD (OPTIONAL) WHICH INDICATES THAT UPON COMPLETION OF THE PRESENT ANALYSIS (INCLUDES ALL VARIABLE SOURCE VALUES AT EACH SPECIFIED TEMPERATURE) THE CIRCUIT AND/OR RESPONSE CONTROL CARDS ARE TO BE ALTERED.

1) ANY TYPE OF CARD MAY FOLLOW AN ALTER CARD. THE PROGRAM VIEWS SUCH CARDS AS A CONTINUATION OF THE CIRCUIT OR RESPONSE CONTROL CARD DESCRIPTION. THUS

I) FOR DC AND/OR SMALL-SIGNAL ANALYSES, ANALYSIS SPECIFICATIONS MAY BE INTRODUCED, DELETED, OR CHANGED BY INCLUDING A PRINT CARD WITH NEW ANALYSIS SPECIFICATIONS, DELIMITERS, OR ALTERED ANALYSIS SPECIFICATIONS, RESPECTIVELY.

II) TEMPERATURE VARIATIONS MAY BE INTRODUCED, DELETED, OR CHANGED BY INCLUDING A TEMPERATURE CARD WITH, WITHOUT, OR WITH NEW TEMPERATURE DATA, RESPECTIVELY. NOISE FREQUENCIES MAY BE INTRODUCED, DELETED, OR CHANGED BY INCLUDING A NOISE CARD WITH, WITHOUT, OR WITH NEW NOISE FREQUENCIES, RESPECTIVELY. SENSITIVITY FREQUENCIES MAY BE INTRODUCED, DELETED, OR CHANGED BY INCLUDING A SENSITIVITY CARD WITH, WITHOUT, OR WITH NEW SENSITIVITY FREQUENCIES, RESPECTIVELY.

III) ELEMENTS MAY BE ADDED, DELETED, OR CHANGED BY INCLUDING A NEW ELEMENT NAME AND DESCRIPTION, AN OLD ELEMENT NAME WITH NO DESCRIPTION, OR AN OLD ELEMENT NAME AND NEW DESCRIPTION, RESPECTIVELY.

IV) TRANSISTOR MODEL PARAMETERS MAY BE ADDED, DELETED, OR CHANGED BY INCLUDING A NEW KEYWORD AND NUMERIC FIELDS, AN OLD KEYWORD WITH NO NUMERIC FIELDS, OR AN OLD KEYWORD WITH NEW NUMERIC FIELDS, RESPECTIVELY, ON A CARD WITH AN OLD TRANSISTOR MODEL NAME.

2) ANY NUMBER OF SUCCESSIVE ALTER CARD CYCLES ARE ALLOWED.

EXAMPLE -

```
ALTER
```

COLUMNS 1 - 5 MUST CONTAIN THE WORD ALTER.

9) END CARD -- A CARD WHICH INDICATES THAT UPON COMPLETION OF THE PRESENT ANALYSIS, A NEW CIRCUIT IS TO BE ENTERED. THIS CARD MUST BE INCLUDED.

EXAMPLE -

```
END
```

COLUMNS 1 - 3 MUST CONTAIN THE WORD END.

ELEMENT CARDS

1) RESISTOR, CAPACITOR, AND INDUCTOR CARDS

GENERAL FORM -

```
RXXX N1 N2 VALUE TC1 TC2 VAR
CXXX N1 N2 VALUE TC1 TC2 VAR
LXXX N1 N2 VALUE TC1 TC2 VAR
```

EXAMPLES -

```
R1  01  21  300K  2.0E-3
C1  01  00  12.0P  //  V
LZRO  02  10  0.000001
```

THE FIRST FIELD MUST CONTAIN AN ELEMENT NAME THAT BEGINS WITH THE LETTER R FOR RESISTOR CARDS, C FOR CAPACITOR CARDS, AND L FOR INDUCTOR CARDS. N1 AND N2 ARE THE NODES OF THE ELEMENT. VALUE IS THE NOMINAL RESISTANCE IN OHMS FOR RESISTOR CARDS, NOMINAL CAPACITANCE IN FARADS FOR CAPACITOR CARDS, AND NOMINAL INDUCTANCE IN HENRIES FOR INDUCTOR CARDS. VALUE CANNOT BE ZERO OR NEGATIVE. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY. UNSPECIFIED TEMPERATURE COEFFICIENTS ARE ASSUMED TO BE 0.0. VAR IS AN OPTIONAL FIELD USED TO SPECIFY A SENSITIVITY ANALYSIS VARIABLE. IF VAR IS THE LETTER V AND A *SENS CARD* IS INCLUDED IN THE DATA DECK, SENSITIVITIES (PARTIAL DERIVATIVES) WITH RESPECT TO THE SPECIFIED ELEMENT WILL BE PERFORMED.

2) VOLTAGE-CONTROLLED CURRENT SOURCE CARDS

GENERAL FORM -

```
GXXX N+ N- NC+ NC- VALUE TC1 TC2 VAR
```

EXAMPLE -

```
GM2  7 0 3 0  3M  2E-3
```

GXXX IS THE VOLTAGE-CONTROLLED CURRENT SOURCE NAME WHICH MUST BEGIN WITH THE LETTER G. N+ AND N- ARE THE POSITIVE AND NEGATIVE NODES, RESPECTIVELY, OF THE CONTROLLED SOURCE. A POSITIVE CURRENT FLOWS FROM N+ THROUGH THE SOURCE TO N-. NC+ AND NC- ARE THE POSITIVE AND NEGATIVE CONTROLLING NODES, RESPECTIVELY. VALUE IS THE NOMINAL TRANSCONDUCTANCE IN MHOS. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY. UNSPECIFIED TEMPERATURE COEFFICIENTS ARE ASSUMED TO BE 0.0. VAR IS AN OPTIONAL FIELD USED TO SPECIFY A SENSITIVITY ANALYSIS VARIABLE. IF VAR IS THE LETTER V AND A *SENS CARD* IS INCLUDED IN THE DATA DECK, SENSITIVITIES (PARTIAL DERIVATIVES) WITH RESPECT TO THE SPECIFIED ELEMENT WILL BE PERFORMED.

3) MUTUAL INDUCTOR CARDS

GENERAL FORM -

MXXX N1 N2 N3 N4 VALUE1 VALUE2 VALUE3 TC1 TC2

EXAMPLE -

ML1 2 5 4 6 10U 10U 5U 0.1M

MXXX IS THE MUTUAL INDUCTOR NAME WHICH MUST BEGIN WITH THE LETTER M. N1 AND N2 ARE THE NODES OF THE PRIMARY WINDING AND N3 AND N4 ARE THE NODES OF THE SECONDARY WINDING. VALUE1 IS THE NOMINAL SELF-INDUCTANCE OF THE PRIMARY WINDING, VALUE2 IS THE NOMINAL MUTUAL INDUCTANCE BETWEEN THE PRIMARY AND SECONDARY WINDINGS, AND VALUE3 IS THE NOMINAL SELF-INDUCTANCE OF THE SECONDARY WINDING. ALL INDUCTANCES ARE SPECIFIED IN HENRIES. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY. UNSPECIFIED TEMPERATURE COEFFICIENTS ARE ASSUMED TO BE 0.0.

4) CURRENT SOURCE CARDS

GENERAL FORM -

IXXX N+ N- VALUE VALUES

EXAMPLE -

IS 02 03 0.002

IXXX IS THE CURRENT SOURCE NAME WHICH MUST BEGIN WITH THE LETTER I. N+ AND N- ARE THE POSITIVE AND NEGATIVE NODES, RESPECTIVELY. A POSITIVE CURRENT FLOWS FROM N+ THROUGH THE SOURCE TO N-. VALUE IS THE NOMINAL CURRENT IN AMPERES OF THE CURRENT SOURCE.

FOR A SINGLE CURRENT SOURCE (OR GROUNDED VOLTAGE SOURCE) UP TO TWENTY VALUES OF CURRENT (OR VOLTAGE) FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE ENTERED. THESE ADDITIONAL VALUES ARE ENTERED ON THE REMAINDER OF THE SOURCE CARD AND IF NECESSARY ON CARDS FOLLOWING IMMEDIATELY. THESE CARDS THAT FOLLOW MUST CONTAIN A PLUS, +, IN COLUMN 1. NOTE THAT ADDITIONAL SOURCE VALUES SHOULD NOT BE SPECIFIED FOR THE GENERATION OF A DC TRANSFER CURVE (SEE *DC CARD* ABOVE).

5) GROUNDED VOLTAGE SOURCE CARDS.

GENERAL FORM -

VXXX N+ 0 VALUE VALUES

EXAMPLE -

V+ 1 0 15.0 10.0

VXXX IS THE GROUNDED VOLTAGE SOURCE NAME WHICH MUST BEGIN WITH THE LETTER V. N+ IS THE POSITIVE NODE OF THE GROUNDED VOLTAGE SOURCE. VALUE IS THE NOMINAL VOLTAGE (POSITIVE OR NEGATIVE) IN VOLTS OF THE VOLTAGE SOURCE.

FOR A SINGLE GROUNDED VOLTAGE SOURCE (OR CURRENT SOURCE) UP TO TWENTY VALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE ENTERED AS DESCRIBED UNDER THE CURRENT SOURCE CARDS.

6) TRANSISTOR (BIPOLAR AND FIELD-EFFECT) CARDS

GENERAL FORM -

QXXX N1 N2 N3 N4 MODEL AREAF CUR VOLT TEMP

EXAMPLES -

```
Q5  7 6 3  BNS  2 1MA 3.0
Q10  7 3 4  FJUN
Q25  11 1 0 0 FMOS 2
```

QXXX IS THE TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q.

FOR BIPOLAR TRANSISTORS, N1 IS THE COLLECTOR NODE, N2 IS THE BASE NODE, N3 IS THE EMITTER NODE, AND N4 IS NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT TRANSISTORS, N1 IS THE DRAIN NODE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE, AND N4 IS NOT SPECIFIED. FOR MOS FIELD-EFFECT TRANSISTORS, N1 IS THE DRAIN NODE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE, AND N4 IS THE SUBSTRATE (BULK) NODE.

MODEL IS THE FOUR CHARACTER TRANSISTOR MODEL NAME WHICH MUST BEGIN WITH THE LETTER B FOR A BIPOLAR TRANSISTOR MODEL OR THE LETTER F FOR A FIELD-EFFECT TRANSISTOR MODEL.

AREAF IS THE AREA FACTOR THAT IS TO BE USED WITH THE TRANSISTOR MODEL. IF DEFAULTED, A VALUE OF 1.0 IS ASSUMED. AN AREA FACTOR OF 2.0 FOR EXAMPLE, IMPLIES THAT TWO TRANSISTORS OF THE MODEL INDICATED ARE TO BE PLACED IN PARALLEL. HENCE, FOR A BIPOLAR TRANSISTOR, RB AND RC ARE HALVED WHILE ISS, CJE, AND CJC ARE DOUBLED.

FOR BIPOLAR TRANSISTORS, CUR AND VOLT ARE VALUES OF THE COLLECTOR CURRENT AND COLLECTOR-EMITTER JUNCTION VOLTAGE, RESPECTIVELY. IF THE DC ANALYSIS IS 3 BYPASSED, THESE VALUES WILL BE USED AS THE OPERATING POINT TO GENERATE THE SMALL-SIGNAL PARAMETERS. IF DEFAULTED, VALUES OF 0.1 MA FOR CUR AND 1.0 VOLT FOR VOLT ARE ASSUMED. CUR AND VOLT ARE NOT SPECIFIED FOR FIELD-EFFECT TRANSISTORS.

TEMP IS THE TEMPERATURE IN DEGREES KELVIN AT WHICH THE TRANSISTOR IS TO BE 2 HELD. IF OMITTED, THE TRANSISTOR WILL BE ALLOWED TO FOLLOW THE TEMPERATURES AS SPECIFIED ON THE *TEMPERATURE CARD*.

1

BIPOLAR TRANSISTOR MODEL CARDS

THESE CARDS DESCRIBE THE BIPOLAR TRANSISTOR MODELS USED IN THE CIRCUIT. THE MODEL PARAMETERS ARE ENTERED AS GROUPS OF NUMERIC FIELDS PRECEDED BY SPECIFIC KEYWORDS WHICH ARE DESCRIBED BELOW. THE ORDER IN WHICH GROUPS OF PARAMETERS ARE ENTERED IS ARBITRARY AND ANY GROUP MAY BE OMITTED, IN WHICH CASE THE DEFAULT VALUES ARE ASSUMED. WITHIN A GROUP SLASHES MAY BE USED TO DEFAULT LEADING NUMERIC FIELDS AND ANY OMITTED TRAILING NUMERIC FIELDS TAKE ON DEFAULT VALUES. AS MANY CONTINUATION CARDS (SPECIFIED BY A PLUS, +, IN COLUMN 1) AS NECESSARY MAY BE USED.

GENERAL FORM -

```
BXXX  TYPE  BF=BFMAX,ICMAX,BFLOW,ICLOW,VCE,TC1,TC2  BR=VALUE
+  RB=VALUE,IC,VBE,VCE  RB=VALUE,TC1,TC2  RC=VALUE,TC1,TC2
+  FT=VALUE,IC,VCE,CJE/WB,ICO  TSAT=VALUE  CJE=VALUE,VBE,PHIE,NE
+  CJC=VALUE,VBC,PHIC,MC,RATIO  CSUB=VALUE  TEMP=VALUE  ISS=VALUE
+  TF=VALUE  VA=VALUE
```

EXAMPLES -

```
BNPN=NPN  BF=100,1.0MA(40,1.0UA,3.0V,6.667%,-36.0U)  BR=1  ISS=2.0E-14
+   RB=150.(2.0M,9.6U)  RC=100.0(1.5M,7.0U)  PC=50K,2MA
+   CJE=3.0PF,0.65V  CJC=1.0PF,-5.0V  CSUB=2.0PF
+   FT=600MEGHZ(1.0MA,5.0V)

BNS NPN BF 290 BR 1 ISS 1.26E-15 RB 670 RC 300 RO 180K 1M
+   FT 703MEG 1M CJE .65P CJC .36P CSUB 3.2P VA 50.0V

BPNP  RB=100  CSUB=3.2PF  BF=110  PNP
```

1) NAME

BXXX IS THE BIPOLAR TRANSISTOR MODEL NAME WHICH MUST BEGIN WITH THE LETTER B.

2) TYPE KEYWORD : NPN OR PNP

TYPE IS EITHER THE KEYWORD NPN OR PNP DEPENDING ON WHETHER THE BIPOLAR MODEL TYPE IS NPN OR PNP, RESPECTIVELY. IF OMITTED, NPN IS ASSUMED.

3) FORWARD BETA KEYWORD : BF

BFMAX IS THE NOMINAL FORWARD BETA. FOR A CURRENT-DEPENDENT FORWARD BETA, BFMAX IS THE MAXIMUM VALUE OF THE FORWARD BETA, ICMAX IS THE COLLECTOR CURRENT AT WHICH BFMAX OCCURS, BFLOW IS A VALUE OF THE FORWARD BETA AT A CURRENT BELOW ICMAX, AND ICLOW IS THE COLLECTOR CURRENT AT WHICH BFLOW OCCURS. VCE IS THE CONSTANT VALUE OF THE COLLECTOR-EMITTER VOLTAGE AT WHICH BOTH BFMAX AND BFLOW OCCUR. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY, FOR BOTH THE FORWARD AND REVERSE BETAS.

4) REVERSE BETA KEYWORD : BR

VALUE IS THE NOMINAL REVERSE BETA. NOTE THAT THE TEMPERATURE COEFFICIENTS FOR THE REVERSE BETA ARE THE SAME AS THOSE FOR THE FORWARD BETA AND ARE SPECIFIED IN THE BF GROUP. THE REVERSE BETA IS NOT COLLECTOR CURRENT DEPENDENT.

5) OUTPUT RESISTANCE KEYWORD : RO

VALUE IS THE OUTPUT RESISTANCE. IC, VBE, AND VCE ARE THE VALUES OF COLLECTOR CURRENT, BASE-EMITTER VOLTAGE, AND COLLECTOR-EMITTER VOLTAGE, RESPECTIVELY, AT WHICH THE OUTPUT RESISTANCE IS MEASURED. IF THE EARLY VOLTAGE IS NOT SPECIFIED, THE RO DATA IS USED TO COMPUTE THE EARLY VOLTAGE (SEE *EARLY VOLTAGE* DESCRIPTION BELOW). NOTE THAT VBE AND VCE ARE OPTIONAL. IF SPECIFIED, THE DATA IS USED TO COMPUTE THE REVERSE SATURATION CURRENT AS DESCRIBED BELOW UNDER *REVERSE SATURATION CURRENT*. IF OMITTED, A DEFAULT OR EXPLICITLY SPECIFIED VALUE FOR THE REVERSE SATURATION CURRENT IS ASSUMED.

6) BASE RESISTANCE KEYWORD : RB

VALUE IS THE NOMINAL OHMIC BASE RESISTANCE. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY.

7) COLLECTOR RESISTANCE KEYWORD : RC

VALUE IS THE NOMINAL OHMIC COLLECTOR RESISTANCE. TC1 AND TC2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY.

8) SMALL-SIGNAL UNITY GAIN FREQUENCY KEYWORD : FT

VALUE IS THE FREQUENCY AT WHICH THE SMALL-SIGNAL SHORT-CIRCUIT COMMON-EMITTER CURRENT GAIN IS UNITY. IC AND VCE ARE THE COLLECTOR CURRENT AND COLLECTOR-EMITTER VOLTAGE, RESPECTIVELY, AT WHICH FT IS MEASURED. FT, IC, AND VCE ARE USED TO COMPUTE THE FORWARD TRANSIT TIME, TF. LE/WB AND ICO ARE USED TO MODEL HIGH-CURRENT FT ROLL-OFF. LE/WB IS THE RATIO OF THE LATERAL EMITTER DIMENSION TO THE BASEWIDTH AND ICC IS THE CURRENT AT WHICH FT STARTS TO ROLL-OFF. TO ACCOUNT FOR HIGH CURRENT FT ROLL-OFF, THE COMPUTED VALUE OF TF IS MULTIPLIED BY THE FACTOR

(1 + 0.25 * (LE/WB)**2 * (IC/ICC - 1)**2)

9) SATURATION TIME CONSTANT KEYWORD : TSAT

VALUE IS THE SATURATION TIME CONSTANT WHICH IS PRESENTLY NOT USED IN SLIC.

10) EMITTER JUNCTION CAPACITANCE KEYWORD : CJE

VALUE IS THE EMITTER JUNCTION CAPACITANCE AND VBE IS THE BASE-EMITTER

VOLTAGE AT WHICH THE EMITTER JUNCTION CAPACITANCE IS MEASURED. PHIE IS THE CONTACT POTENTIAL AND NE IS THE GRADIENT FACTOR. THE EMITTER JUNCTION CAPACITANCE AT A GIVEN VBE IS DESCRIBED BY THE FOLLOWING EQUATION

CJE = CJE(VBE=0) / (1 - VBE/PHIE)**NE

FOR BOTH NPN AND PNP DEVICES, VBE SHOULD BE POSITIVE FOR A FORWARD BIASED JUNCTION AND NEGATIVE FOR A REVERSE BIASED JUNCTION.

11) COLLECTOR JUNCTION CAPACITANCE KEYWORD : CJC

VALUE IS THE COLLECTOR JUNCTION CAPACITANCE AND VBC IS THE BASE-COLLECTOR VOLTAGE AT WHICH THE COLLECTOR JUNCTION CAPACITANCE IS MEASURED. PHIC IS THE CONTACT POTENTIAL AND NC IS THE GRADIENT FACTOR. THE COLLECTOR JUNCTION CAPACITANCE AT A GIVEN VBC IS DESCRIBED BY THE FOLLOWING EQUATION

CJC = CJC(VBC=0) / (1 - VBC/PHIC)**NC

RATIO IS THE FRACTION OF THE ABOVE DESCRIBED CJC THAT OVERLAPS THE BASE OHMIC RESISTANCE. THUS, RATIO*CJC IS THE CAPACITANCE THAT EXISTS BETWEEN THE COLLECTOR AND THE BASE CONTACT AND (1.0-RATIO)*CJC IS THE CAPACITANCE THAT EXISTS BETWEEN THE COLLECTOR AND THE BASE ACTIVE REGIONS. FOR BOTH NPN AND PNP DEVICES, VBC SHOULD BE POSITIVE FOR A FORWARD BIASED JUNCTION AND NEGATIVE FOR A REVERSE BIASED JUNCTION.

12) SUBSTRATE CAPACITANCE KEYWORD : CSUB

VALUE IS THE SUBSTRATE CAPACITANCE. FOR AN NPN TRANSISTOR, CSUB IS ASSUMED TO EXIST BETWEEN THE EXTERNAL COLLECTOR AND GROUND, WHILE FOR A PNP TRANSISTOR CSUB IS ASSUMED TO EXIST BETWEEN THE INTERNAL BASE AND GROUND.

13) TEMPERATURE KEYWORD : TEMP

VALUE IS THE TEMPERATURE AT WHICH THE MODEL PARAMETERS ARE MEASURED.

14) REVERSE SATURATION CURRENT KEYWORD : ISS

VALUE IS THE NOMINAL REVERSE SATURATION CURRENT AND IS RELATED TO THE SHORT-CIRCUIT FORWARD AND REVERSE SATURATION CURRENTS BY THE FOLLOWING EQUATION -

ISS = ALPHAF * IES = ALPHAR * ICS

IF ISS IS NOT SPECIFIED AND IF VBE AND VCE OF THE RD SPECIFICATION ARE ALSO NOT SPECIFIED, THEN ISS IS DEFAULTED TO 1.0E-14 AMPERES. IF ISS IS NOT SPECIFIED BUT VBE AND VCE ARE SPECIFIED FOR RD, THEN ISS IS COMPUTED FROM THE RD DATA BY THE FOLLOWING EQUATION

ISS = IC / ((1 + VCB/VA) * EXP(VBE/VT))

WHERE VA IS THE EARLY VOLTAGE AND VT THE THERMAL VOLTAGE.

15) FORWARD TRANSIT TIME KEYWORD : TF

VALUE IS THE FORWARD TRANSIT TIME. IF UNSPECIFIED, TF IS COMPUTED FROM THE FT DATA. IF FT IS UNSPECIFIED, THEN TF IS SET TO 0.0. IF TF IS SPECIFIED, THIS VALUE REPLACES ANY FT DERIVED VALUE.

16) EARLY VOLTAGE KEYWORD : VA

VALUE IS THE EARLY VOLTAGE. IF UNSPECIFIED, VA IS COMPUTED FROM THE RO DATA BY THE FORMULA

$$VA = RO * IC$$

IF RO IS UNSPECIFIED, THEN VA IS SET TO INFINITY. IF VA IS SPECIFIED, THIS VALUE REPLACES ANY RO DERIVED VALUE.

PARAMETER	DEFAULT VALUE
TYPE	NPN
BF=BFMAX	100.0
ICMAX	IGNORED
BFLOW	IGNORED
ICLOW	IGNORED
VCE	0.0
TC1	0.0
TC2	0.0
BR=VALUE	1.0
RO=VALUE	INFINITE
IC	IGNORED
VBE	IGNORED
VCE	IGNORED
RB=VALUE	0.0
TC1	0.0
TC2	0.0
RC=VALUE	0.0
TC1	0.0
TC2	0.0
FT=VALUE	INFINITE
IC	IGNORED
VCE	IGNORED
LE/WB	IGNORED
ICO	IGNORED
TSAT=VALUE	0.0
CJE=VALUE	0.0
VBE	0.0
PHIE	0.7 VOLTS (NPN) 0.5 VOLTS (PNP)
ME	0.33333
CJC=VALUE	0.0
VBC	0.0
PHIC	0.5 VOLTS
MC	0.33333
RATIO	0.0
CSUB=VALUE	0.0
TEMP=VALUE	300 DEG K
ISS=VALUE	SEE DESCRIPTION ABOVE
TF=VALUE	SEE DESCRIPTION ABOVE
VA=VALUE	SEE DESCRIPTION ABOVE

FIELD-EFFECT TRANSISTOR MODEL CARDS

THESE CARDS DESCRIBE THE FIELD-EFFECT TRANSISTOR MODELS USED IN THE CIRCUIT. THE MODEL PARAMETERS ARE ENTERED BY SPECIFYING A PARAMETER KEYWORD FOLLOWED BY THE PARAMETER VALUE. THE ORDER IN WHICH PARAMETERS ARE ENTERED IS ARBITRARY AND ANY PARAMETER MAY BE OMITTED, IN WHICH CASE THE DEFAULT VALUE IS ASSUMED. AS MANY CONTINUATION CARDS (SPECIFIED BY A PLUS, +, IN COLUMN 1) AS NECESSARY MAY BE USED.

GENERAL FORM -

```
FXXX  TYPE  VTO=VAL1  PHI=VAL2  BETA=VAL3  GAMMA=VAL4  LAMBDA=VAL5  RD=VAL6
+  RS=VAL7  CGS=VAL8  CGD=VAL9  CGB=VAL10  CBD=VAL11  CBS=VAL12  PB=VAL13
+  IS=VAL14
```

EXAMPLES -

```
FJ1 NJUN VTO=-3 BETA=0.001 LAMBDA=0.05 RD=500 RS=500 CGS=10PF CGD=10PF

FM4  NMOS  VTO 1.0  BETA 1.25U  GAMMA 0.5  CGB 0.32PF  CBD 0.2PF  CBS 0.2PF
```

1) NAME

FXXX IS THE FIELD-EFFECT TRANSISTOR MODEL NAME WHICH MUST BEGIN WITH THE LETTER F.

2) TYPE KEYWORD : NJUN, PJUN, NMOS, OR PMOS

FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS, TYPE IS EITHER THE KEYWORD NJUN OR PJUN DEPENDING ON WHETHER THE MODEL IS N CHANNEL OR P CHANNEL, RESPECTIVELY. FOR MOS FIELD-EFFECT TRANSISTOR MODELS, TYPE IS EITHER THE KEYWORD NMOS OR PMOS DEPENDING ON WHETHER THE MODEL IS N CHANNEL OR P CHANNEL, RESPECTIVELY.

3) THRESHOLD VOLTAGE KEYWORD : VTO

VAL1 IS THE THRESHOLD VOLTAGE. FOR BOTH N CHANNEL AND P CHANNEL DEVICES, VTO SHOULD BE POSITIVE FOR ENHANCEMENT MODE AND NEGATIVE FOR DEPLETION MODE.

3

4) SURFACE POTENTIAL KEYWORD : PHI

THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSISTOR MODELS ONLY. VAL2 IS THE CHANNEL SURFACE POTENTIAL.

2

5) TRANSCONDUCTANCE PARAMETER KEYWORD : BETA

VAL3 IS THE TRANSCONDUCTANCE PARAMETER. BOTH THE THRESHOLD VOLTAGE AND THE TRANSCONDUCTANCE PARAMETER DETERMINE THE VARIATION OF DRAIN CURRENT WITH GATE VOLTAGE.

1

6) BULK THRESHOLD PARAMETER KEYWORD : GAMMA

THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSISTOR MODELS ONLY. VAL4 IS THE BULK (SUBSTRATE) THRESHOLD PARAMETER. BOTH THE SURFACE POTENTIAL AND THE BULK THRESHOLD PARAMETER DETERMINE THE VARIATION OF THE THRESHOLD VOLTAGE WITH SUBSTRATE VOLTAGE.

7) CHANNEL LENGTH MODULATION PARAMETER KEYWORD : LAMBDA

VAL5 IS THE CHANNEL LENGTH MODULATION PARAMETER WHICH DETERMINES THE OUTPUT CONDUCTANCE.

8) DRAIN RESISTANCE KEYWORD : RD

VAL6 IS THE OHMIC DRAIN RESISTANCE.

9) SOURCE RESISTANCE KEYWORD : RS

VAL7 IS THE OHMIC SOURCE RESISTANCE.

10) GATE-SOURCE CAPACITANCE KEYWORD : CGS

FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS, VAL8 IS THE ZERO BIAS GATE-SOURCE JUNCTION CAPACITANCE WHICH VARIES AS THE -1/2 POWER OF THE GATE-SOURCE VOLTAGE. FOR MOS FIELD-EFFECT TRANSISTOR MODELS, VAL8 IS THE LINEAR GATE-SOURCE CAPACITANCE.

11) GATE-DRAIN CAPACITANCE KEYWORD : CGD

FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS, VAL9 IS THE ZERO BIAS GATE-DRAIN JUNCTION CAPACITANCE WHICH VARIES AS THE -1/2 POWER OF THE GATE-DRAIN VOLTAGE. FOR MOS FIELD-EFFECT TRANSISTOR MODELS, VAL9 IS THE LINEAR GATE-DRAIN CAPACITANCE.

12) GATE-BULK CAPACITANCE KEYWORD : CGB

THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSISTOR MODELS ONLY. VAL10 IS THE LINEAR GATE-BULK CAPACITANCE.

13) BULK-DRAIN CAPACITANCE KEYWORD : CBD

THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSISTOR MODELS ONLY. VAL11 IS THE ZERO BIAS BULK-DRAIN JUNCTION CAPACITANCE WHICH VARIES AS THE -1/2 POWER OF THE BULK-DRAIN VOLTAGE.

14) BULK-SOURCE CAPACITANCE KEYWORD : CBS

THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSITOR MODELS ONLY. VAL12 IS THE ZERO BIAS BULK-SOURCE JUNCTION CAPACITANCE WHICH VARIES AS THE -1/2 POWER OF THE BULK-SOURCE VOLTAGE.

15) JUNCTION POTENTIAL KEYWORD : PB

VAL13 IS THE GATE JUNCTION POTENTIAL FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS OR THE BULK JUNCTION POTENTIAL FOR MOS FIELD-EFFECT TRANSISTOR MODELS. THIS PARAMETER IS USED TO COMPUTE THE JUNCTION CAPACITANCES.

16) SATURATION CURRENT KEYWORD : IS

VAL14 IS THE GATE JUNCTION SATURATION CURRENT FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS OR THE BULK JUNCTION SATURATION CURRENT FOR MOS FIELD-EFFECT TRANSISTOR MODELS.

NOTE : EACH OF THE ABOVE JUNCTION CAPACITANCES AT A GIVEN JUNCTION VOLTAGE (VJUN) IS DESCRIBED BY THE FOLLOWING EQUATION

$$CJUN = CJUN(VJUN=0) / (1 - VJUN/PB)^{**0.5}$$

PARAMETER	DEFAULT VALUE
VTO	-2.0 VOLTS (JFET, N AND P CHANNEL) +2.0 VOLTS (MOSFET, N AND P CHANNEL)
PHI (MOSFET ONLY)	0.5 VOLT
BETA	1.0E-4
GAMMA (MOSFET ONLY)	0.0
LAMBDA	0.0
RD	0.0
RS	0.0
CGS	0.0
CGD	0.0
CGB (MOSFET ONLY)	0.0
CBD (MOSFET ONLY)	0.0
CBS (MOSFET ONLY)	0.0
PB	1.0 VOLT
IS	1.0E-14 AMPS

EXAMPLE

THE SET OF DATA CARDS BELOW DESCRIBE A BROADBAND AMPLIFIER AND ILLUSTRATE THE CODING FORMAT FOR SLIC. ANALYSES ARE PERFORMED FOR TWO TEMPERATURES AND A NOISE ANALYSIS IS PERFORMED FOR THREE FREQUENCIES.

```
SOLOMON AND WILSON SERIES-SERIES TRIPLE BROADBAND AMPLIFIER
PRINT DC AC ELOG(10,1MEGHZ,100MEGHZ) VOUT 14 0  VIN 1 0
TEMP  300  300  305
NOISE 1MEGHZ 10MEGHZ 100MEGHZ
*
BNPN=NPN   BF=100,1.0MA(40,1.0UA,3.0V,6.667M,-36.0U)   BR=1   ISS=2.0E-14
+      RB=150.(2.0M,9.6U)   RC=100.0(1.5M,7.0U)   RQ=50K,2MA
+      CJE 3.0PF 0.65V   CJC 1.0PF -5.0V   CSUB 2.0PF
+      FT=600MEGHZ(1.0MA,5.0V)
*
VS(1,0)=0.0
RS  1 2  50.0
CCS(2,3)=1.0UF
Q1 5 3 4 BNPN
RE1(4,0)=100.0
RA  13 5  9K
Q2 6 5 0 BNPN
CP  6 5  3PF
RB(13,6)=5.0K
Q3 8 6 7 BNPN
RE2(7,0)=100.0
RF(7,4)=1.0K
RC  13 8  600
Q4 13 8 9 BNPN
RG(9,10)=3.0K
RK(12,11)=6.0K
Q5(13 13 12)=BNPN
Q6 10 11 0 BNPN
CBYP  10 0  10UF
RD(10,3)=12.0K
Q7  (11,11,0)  BNPN   1.0
Q8 9 11 0 BNPN
Q9(9,11,0) BNPN
Q10 9 11 0 BNPN
CCL  9 14  1UF
RL(14,0)=50.0
VCC(13,0)=6.0VOLTS
END
```

III. PROGRAM DESCRIPTION

The following sections describe the operation of the SLIC program. The total program consists of a main program and thirty-five subroutines. A written description and a flowchart of the execution sequence are provided for the main program and each subroutine. A description of the function of each common block variable is also included.

Main program:	SLIC
Data read-in subroutines:	READ
	ELEMNT
	BMODEL
	VJCT
	FIT
	FMODEL
	INLIST
	CHECK
	CLKST
Matrix set-up subroutines:	SETUP
	NCODE
	OPTORD
	NUMSET

DC subroutines:	DCMOD
	DCTRAN
	PLOT
	DCANAL
	BJTDC
	JFET
	MOSFET
	UPDATE
	DCSOLV
	DCADJ
AC subroutines:	ACMOD
	ACANAL
	ACSOLV
	ACADJ
Pole-zero subroutines:	PZANAL
	MULLER
	CDET
	LOG2
	SORT
Other subroutines:	SENSE
	NOISE
	CLOCK

MAIN PROGRAM SLIC

SLIC controls the overall program execution sequence. The first step is the reading of input data describing the circuit and the the types of analyses. Subroutine READ reads and checks the input data and subroutine CHECK prints transistor model parameters and processes transistors. If fatal errors are discovered in the input data, the job is aborted and a new job is begun. If no fatal errors are found, the specified analyses are performed.

For the dc analysis, subroutine SETUP sets up the dc sparse matrices and subroutine DCMOD computes the dc circuit models. If a dc transfer curve is requested, subroutine DCTRAN computes and plots the transfer curve. Next, subroutine DCANAL computes and prints the dc node voltages and transistor operating points. If a frequency response or pole-zero analysis is not also requested, subroutine ACMOD computes and prints the small-signal transistor parameters. If one of these analyses is also requested, ACMOD will be called later.

SLIC performs two types of small-signal analyses: a frequency response or a pole-zero analysis with an optional frequency response. Only one of these two analyses can be requested for a job.

For the frequency response, subroutine SETUP sets up the ac sparse matrices and subroutine ACMOD computes and prints the small-signal transistor parameters. Subroutine ACANAL then computes the magnitude, phase, real part, and imaginary part of the transfer

function directly from the complex nodal admittance equations and prints these values.

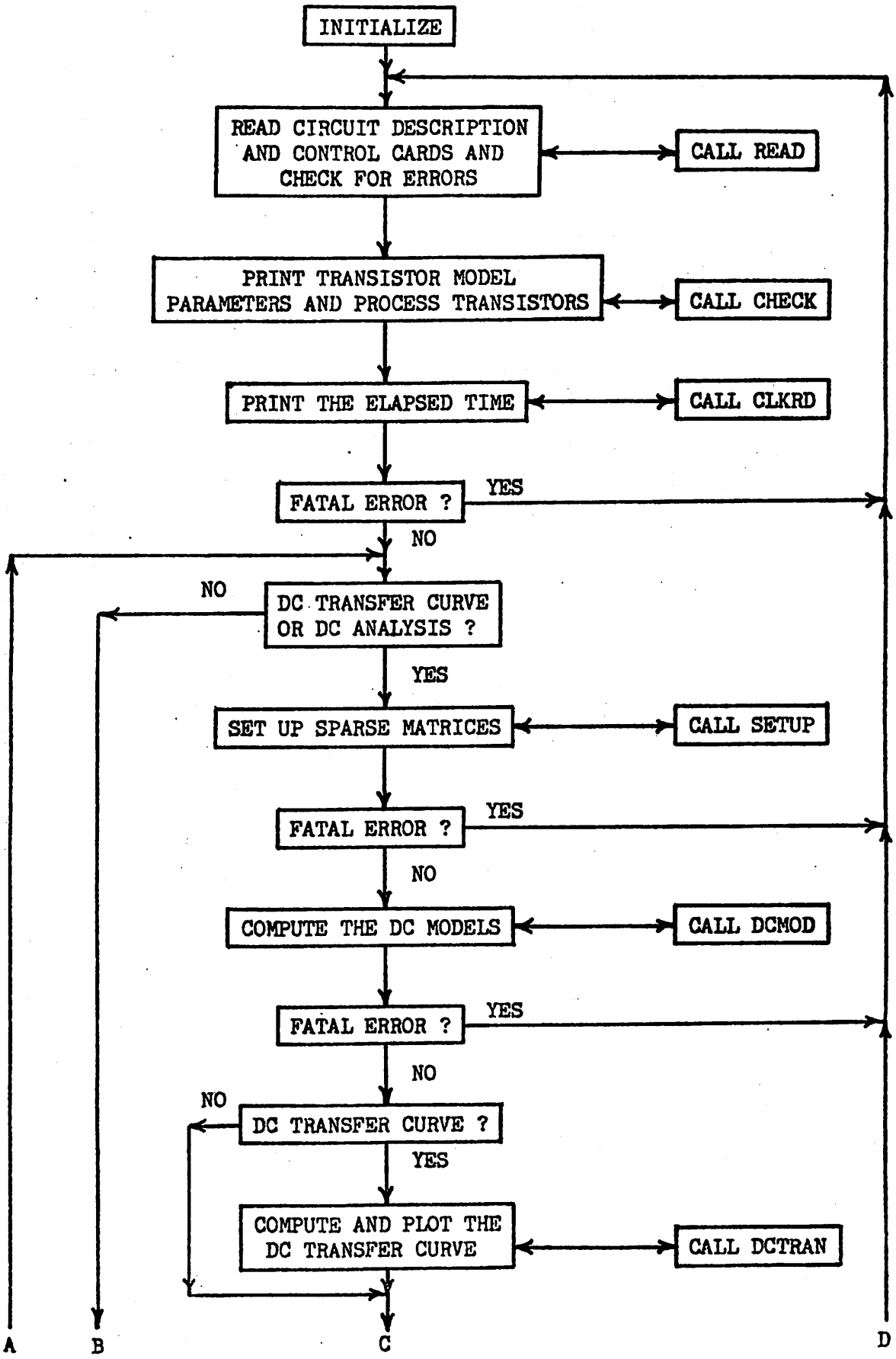
For the pole-zero analysis, subroutine ACMOD first computes and prints the small-signal transistor parameters. Next, subroutine PZANAL computes and prints the poles and zeros of the transfer function. If a frequency response is also requested, PZANAL computes and prints the magnitude, phase, real part, and imaginary part of a pole-zero derived transfer function.

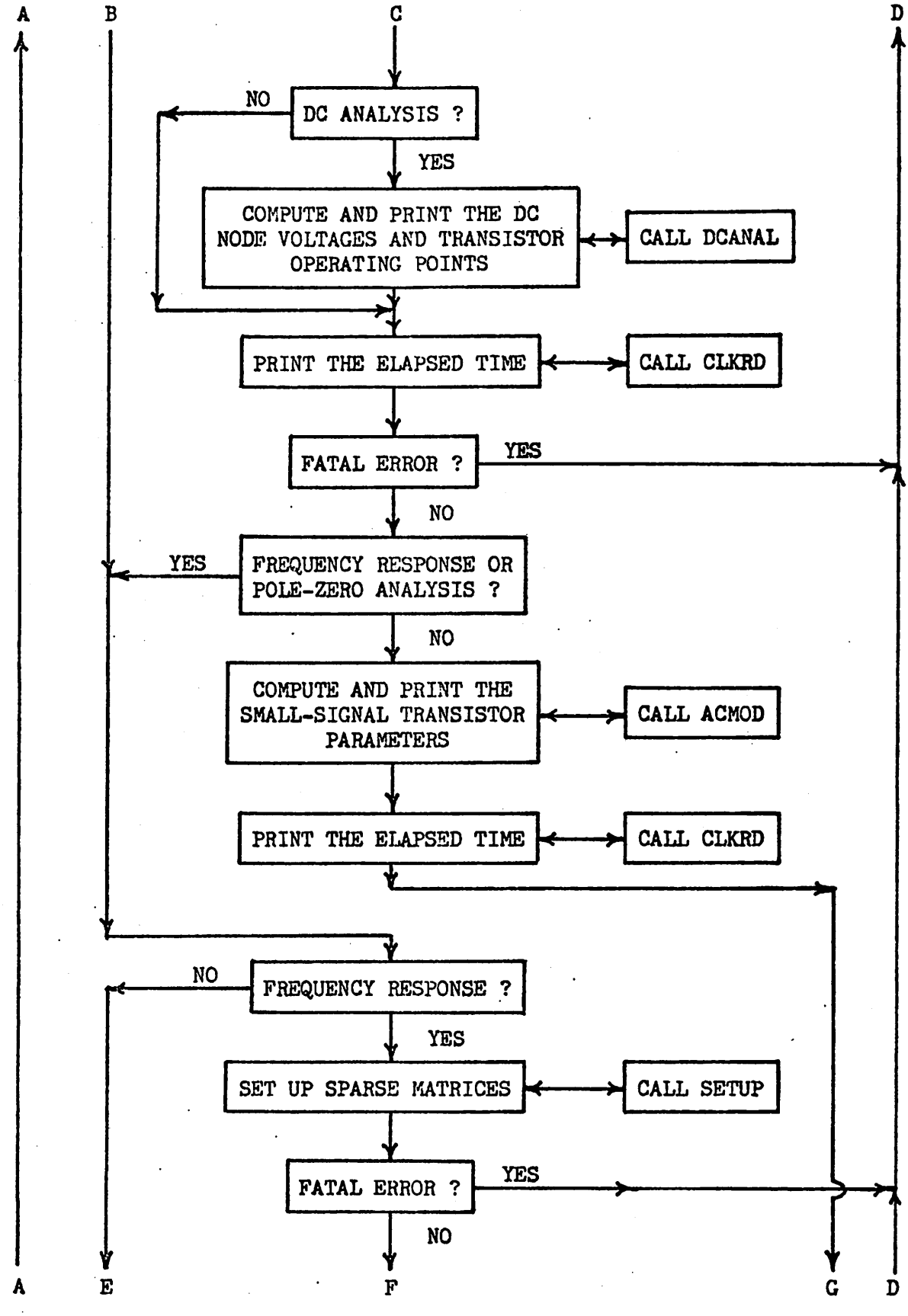
For the noise analysis, subroutine NOISE computes and prints the equivalent noise sources and at each requested frequency the rms noise at the output port. For the sensitivity analysis, subroutine SENSE computes and prints the sensitivities (partial derivatives).

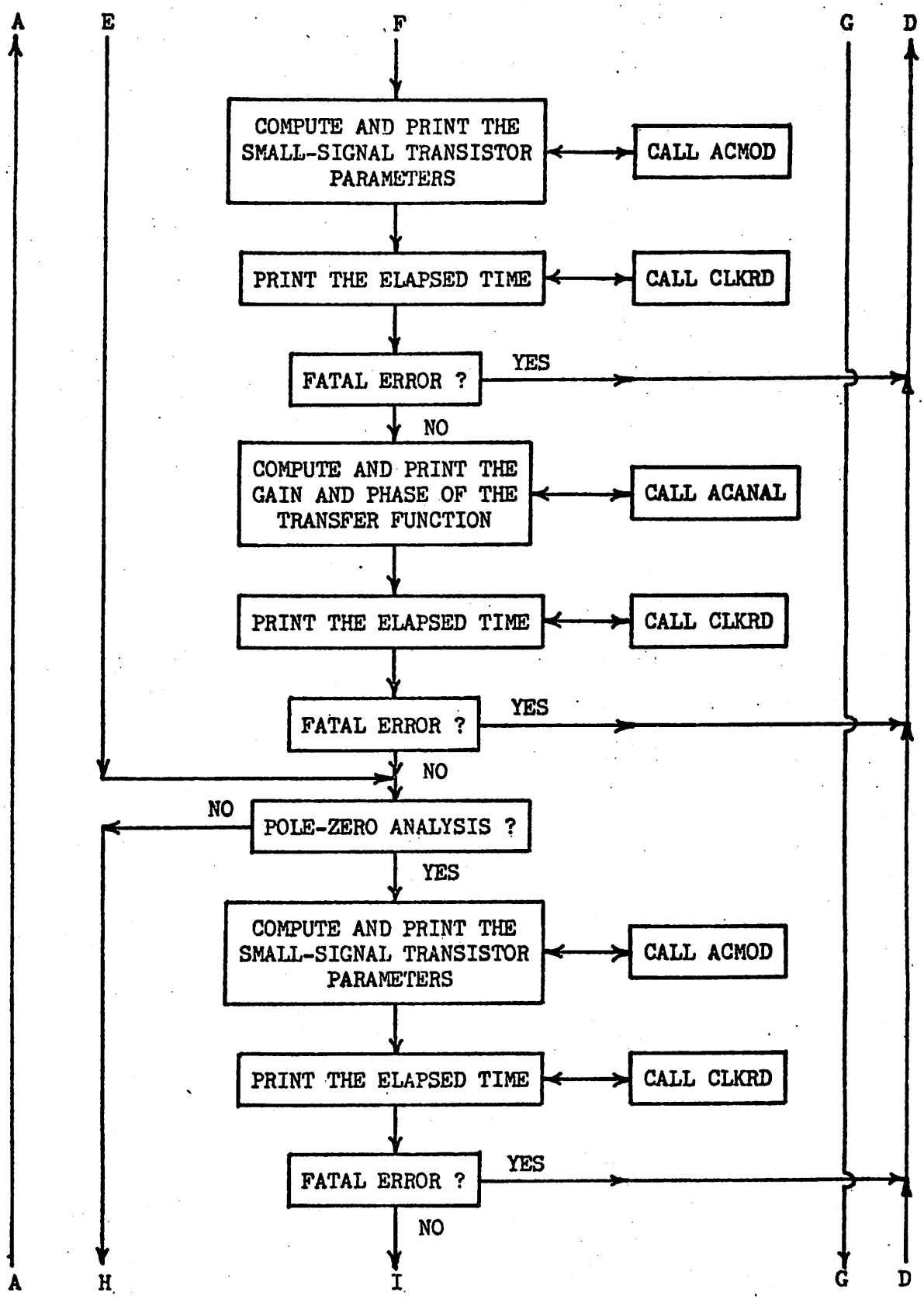
If a variable source and/or temperature variations are specified, the requested analyses are repeated for each source and/or temperature value.

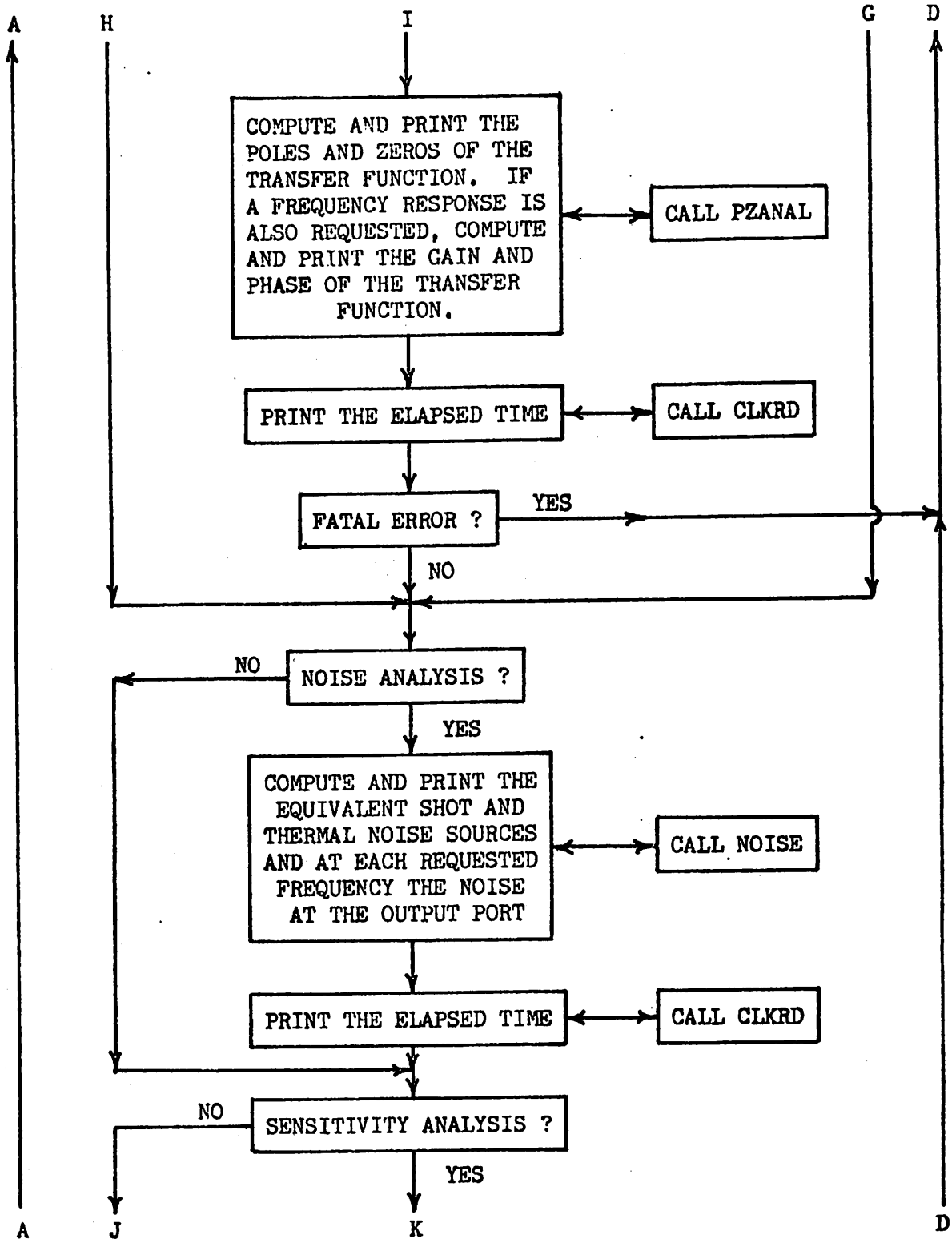
Throughout the execution of a job, subroutine CLKRD computes and prints the elapsed job time. The elapsed time is printed at the end of each type of analysis. Also, if a fatal error is encountered during the execution, the job is aborted.

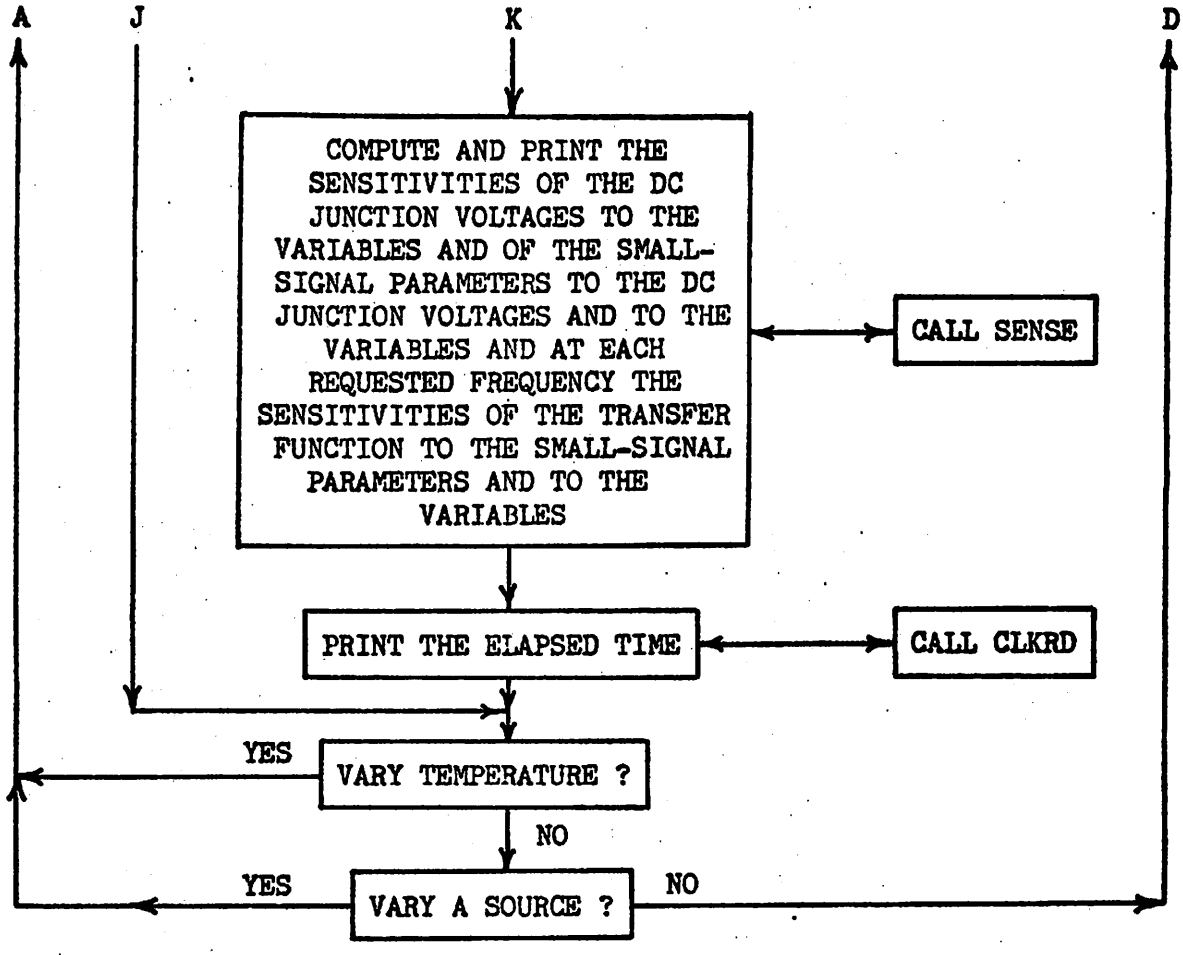
MAIN PROGRAM SLIC




A
B
C
D
NO
DC ANALYSIS ?
YES
COMPUTE AND PRINT THE DC NODE VOLTAGES AND TRANSISTOR OPERATING POINTS
CALL DCANAL
PRINT THE ELAPSED TIME
CALL CLKRD
FATAL ERROR ?
YES
NO
YES
FREQUENCY RESPONSE OR POLE-ZERO ANALYSIS ?
NO
COMPUTE AND PRINT THE SMALL-SIGNAL TRANSISTOR PARAMETERS
CALL ACMOD
PRINT THE ELAPSED TIME
CALL CLKRD
NO
FREQUENCY RESPONSE ?
YES
SET UP SPARSE MATRICES
CALL SETUP
FATAL ERROR ?
YES
NO
A
E
F
G
D


A
E
F
G
D
COMPUTE AND PRINT THE SMALL-SIGNAL TRANSISTOR PARAMETERS
CALL ACMOD
PRINT THE ELAPSED TIME
CALL CLKRD
FATAL ERROR ?
YES
NO
COMPUTE AND PRINT THE GAIN AND PHASE OF THE TRANSFER FUNCTION
CALL ACANAL
PRINT THE ELAPSED TIME
CALL CLKRD
FATAL ERROR ?
YES
NO
NO
POLE-ZERO ANALYSIS ?
YES
COMPUTE AND PRINT THE SMALL-SIGNAL TRANSISTOR PARAMETERS
CALL ACMOD
PRINT THE ELAPSED TIME
CALL CLKRD
FATAL ERROR ?
YES
NO
A
H
I
G
D

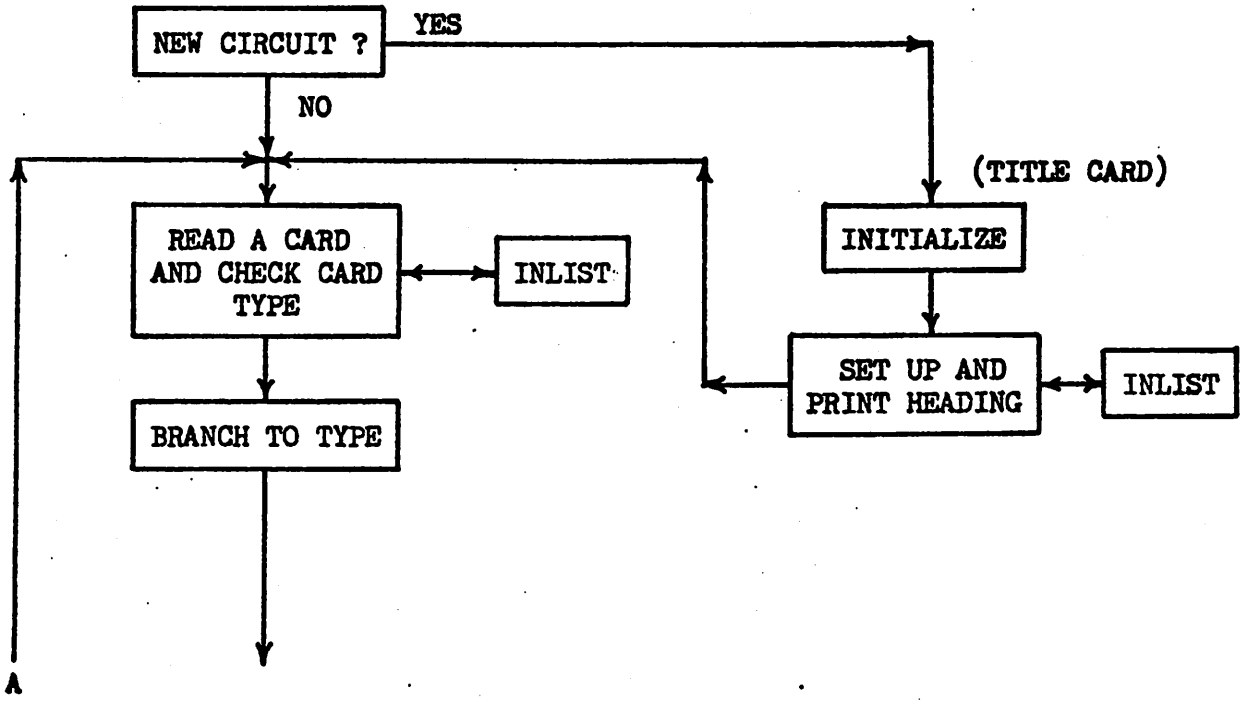

A
H
I
G
D
COMPUTE AND PRINT THE POLES AND ZEROS OF THE TRANSFER FUNCTION. IF A FREQUENCY RESPONSE IS ALSO REQUESTED, COMPUTE AND PRINT THE GAIN AND PHASE OF THE TRANSFER FUNCTION.
CALL PZANAL
PRINT THE ELAPSED TIME
CALL CLKRD
FATAL ERROR ?
YES
NO
NOISE ANALYSIS ?
NO
YES
COMPUTE AND PRINT THE EQUIVALENT SHOT AND THERMAL NOISE SOURCES AND AT EACH REQUESTED FREQUENCY THE NOISE AT THE OUTPUT PORT
CALL NOISE
PRINT THE ELAPSED TIME
CALL CLKRD
SENSITIVITY ANALYSIS ?
NO
YES
A
J
K
D


A
J
K
D
COMPUTE AND PRINT THE SENSITIVITIES OF THE DC JUNCTION VOLTAGES TO THE VARIABLES AND OF THE SMALL-SIGNAL PARAMETERS TO THE DC JUNCTION VOLTAGES AND TO THE VARIABLES AND AT EACH REQUESTED FREQUENCY THE SENSITIVITIES OF THE TRANSFER FUNCTION TO THE SMALL-SIGNAL PARAMETERS AND TO THE VARIABLES
CALL SENSE
PRINT THE ELAPSED TIME
CALL CLKRD
YES
VARY TEMPERATURE ?
NO
YES
VARY A SOURCE ?
NO

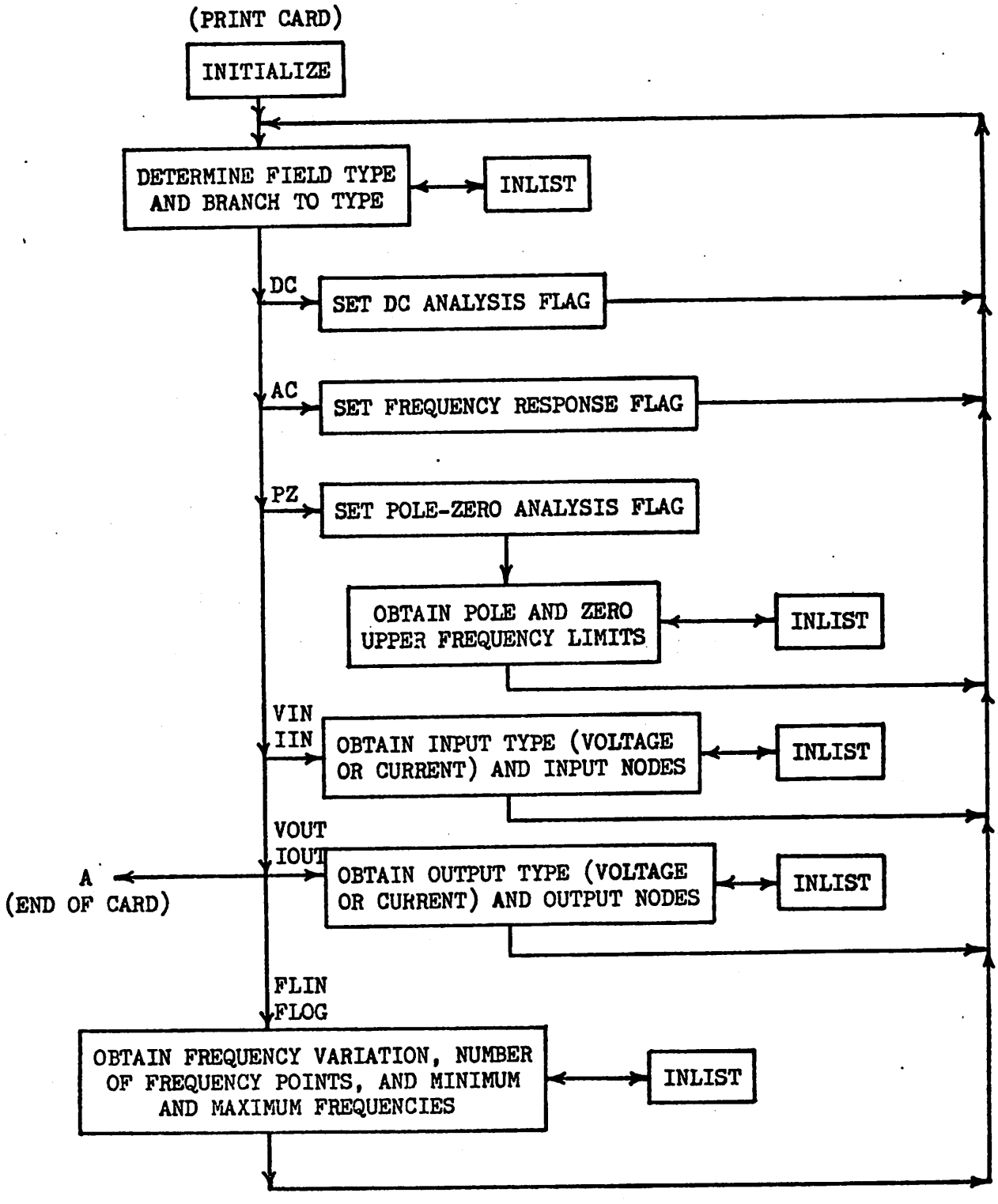
SUBROUTINE READ

This subroutine controls the reading and processing of input data. Subroutine INLIST reads an input data card and if recognizable, control is transferred to a section of READ that handles the particular type of card. If unrecognizable, an error message is printed. The PRINT, TEMP, NOISE, SENS, and DC cards are read and processed within READ. Subroutine ELEMNT reads and processes resistor, voltage-controlled current source, capacitor, inductor, mutual inductor, transistor, voltage source, and current source cards. Subroutine BMODEL reads and processes bipolar transistor model cards while subroutine FMODEL reads and processes field-effect transistor model cards. The reading and processing of input data continues until an ALTER or END card is read.

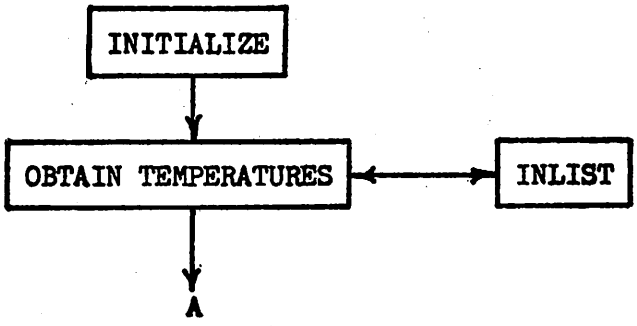
SUBROUTINE READ



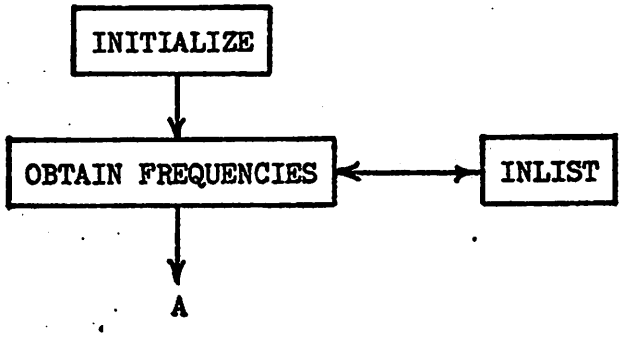
CARD TYPES:


(PRINT CARD)
INITIALIZE
DETERMINE FIELD TYPE AND BRANCH TO TYPE
INLIST
DC
SET DC ANALYSIS FLAG
AC
SET FREQUENCY RESPONSE FLAG
PZ
SET POLE-ZERO ANALYSIS FLAG
OBTAIN POLE AND ZERO UPPER FREQUENCY LIMITS
INLIST
VIN
IIN
OBTAIN INPUT TYPE (VOLTAGE OR CURRENT) AND INPUT NODES
INLIST
VOUT
IOUT
OBTAIN OUTPUT TYPE (VOLTAGE OR CURRENT) AND OUTPUT NODES
INLIST
A
(END OF CARD)
FLIN
FLOG
OBTAIN FREQUENCY VARIATION, NUMBER OF FREQUENCY POINTS, AND MINIMUM AND MAXIMUM FREQUENCIES
INLIST

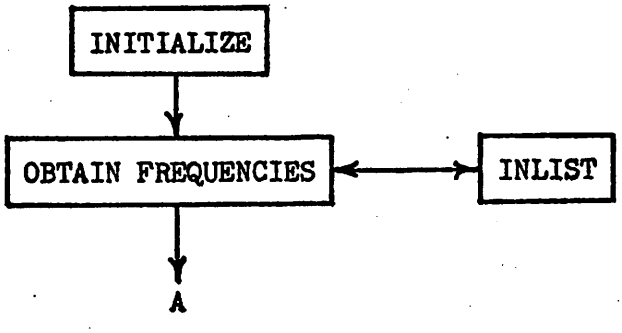
(TEMPERATURE CARD)



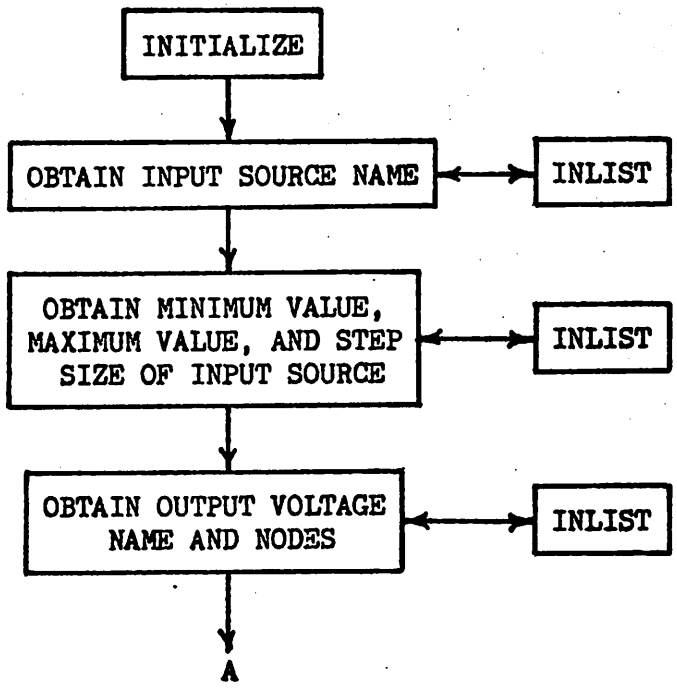
(NOISE CARD)



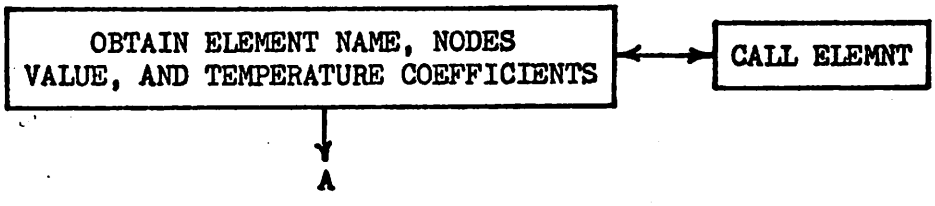
(SENSITIVITY CARD)



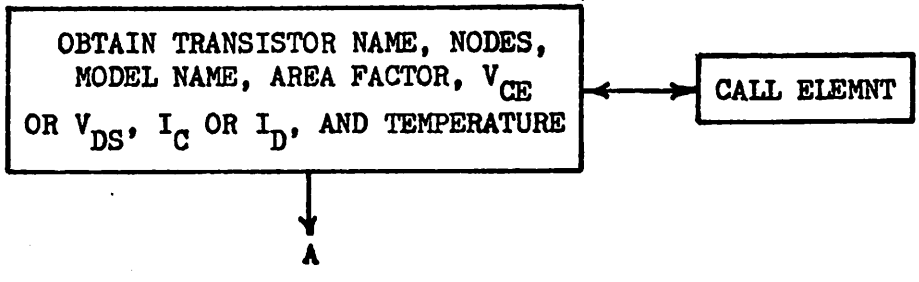
(DC CARD)



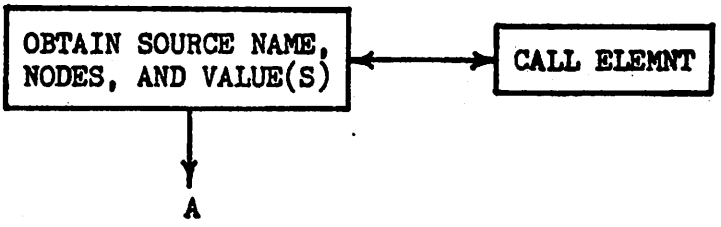
(RESISTOR, VOLTAGE-CONTROLLED CURRENT SOURCE, CAPACITOR, INDUCTOR, AND MUTUAL INDUCTOR CARDS)



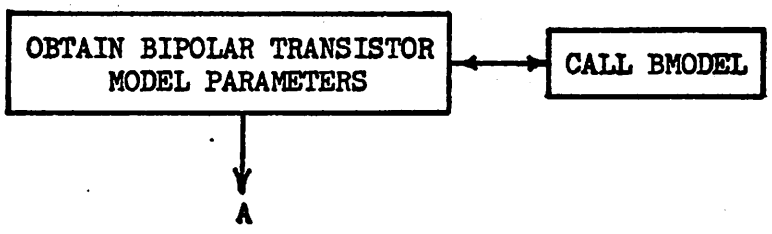
(TRANSISTOR CARDS)



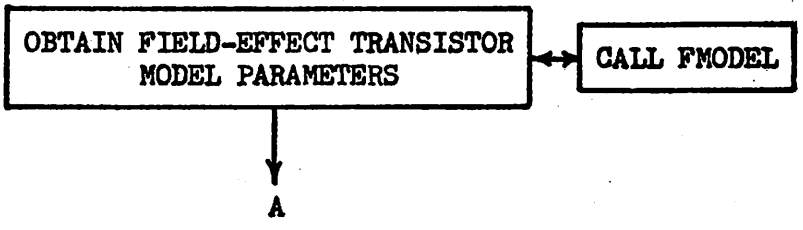
(VOLTAGE SOURCE AND CURRENT SOURCE CARDS)

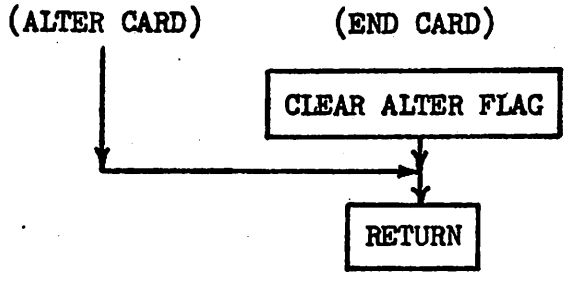


(BIPOLAR TRANSISTOR MODEL CARDS)



(FIELD-EFFECT TRANSISTOR MODEL CARDS)



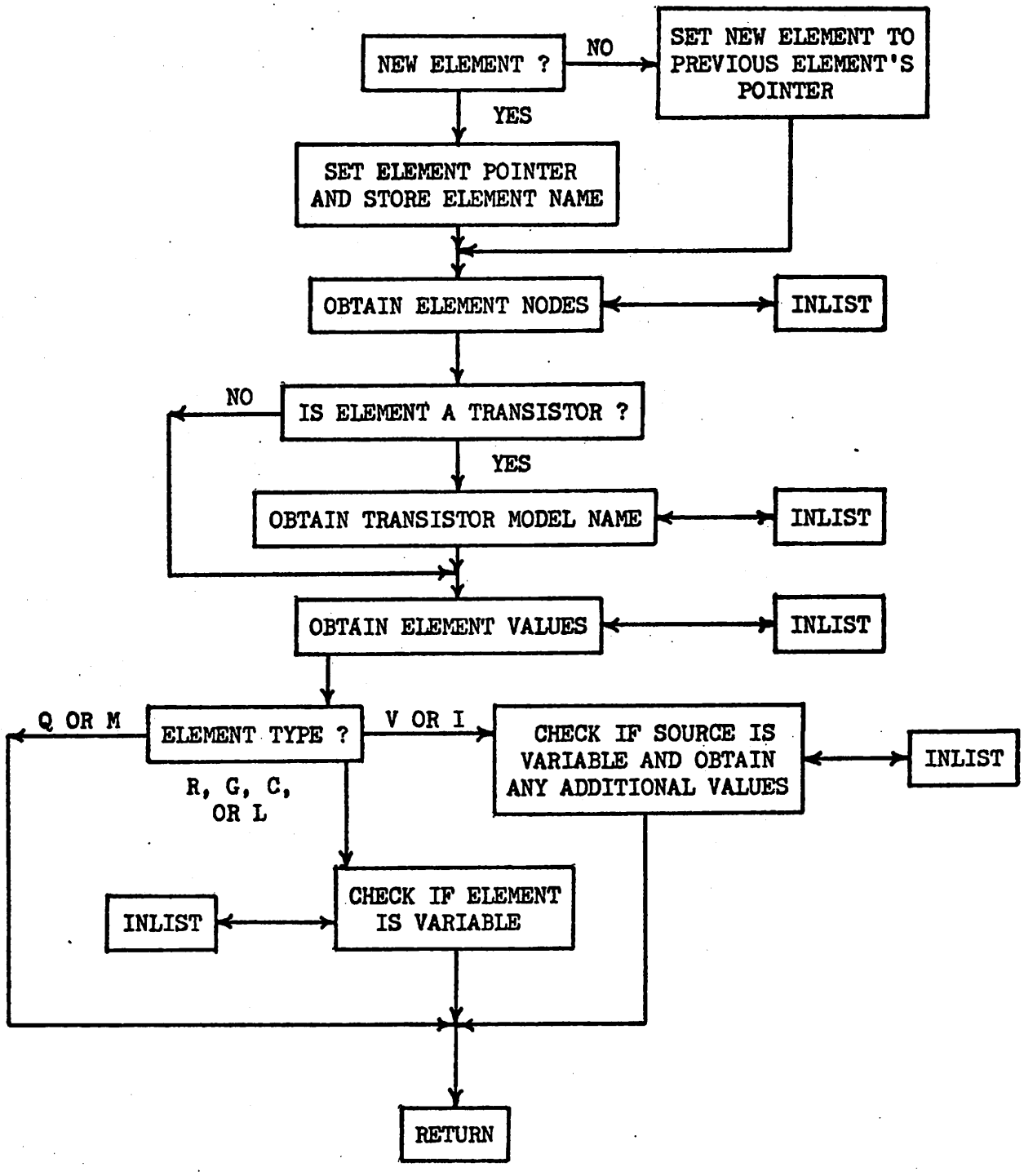


SUBROUTINE ELEMNT

This subroutine reads and processes data on resistor, voltage-controlled current source, capacitor, inductor, mutual inductor, transistor, voltage source, and current source cards. A different set of arguments is passed from subroutine READ for each type of card. Subroutine INLIST is called each time a new data record is needed.

Execution is started by checking if the element has previously been read. If so, the new data replaces old stored data. Next, the element nodes are obtained and if a transistor card is being processed, the transistor model name is also obtained. Then the element values are obtained. Finally any additional values are obtained for voltage and current sources; and resistor,voltage-controlled current source, capacitor, and inductor cards are checked for sensitivity analysis variable designation.

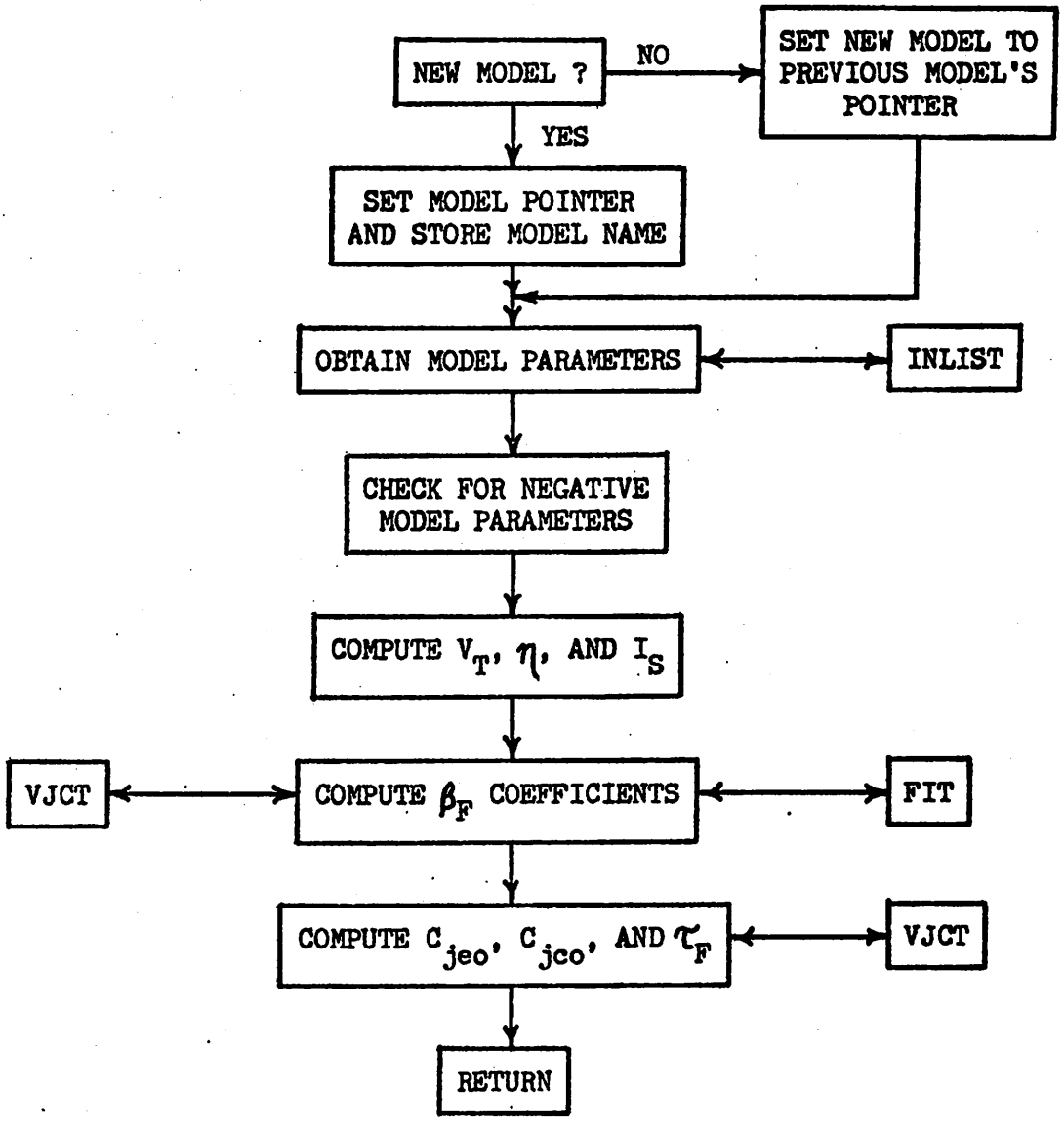
SUBROUTINE ELEMNT



SUBROUTINE BMODEL

This subroutine reads and processes data on bipolar transistor model cards. Subroutine INLIST is called each time a new data record is needed. If the model has previously been read, the new data replaces old stored data. The model parameters are first read, stored, and checked for negative values. Next a number of additional model parameters are computed from the user specified parameters. The thermal voltage ($V_T = \frac{kT}{q}$), basewidth modulation factor (η), reverse saturation current (I_s), current-dependent β_F coefficients, zero bias junction capacitances (C_{jeo} and C_{jco}), and forward base transit time (τ_F) are computed for each model. Subroutines VJCT and FIT are called during these calculations.

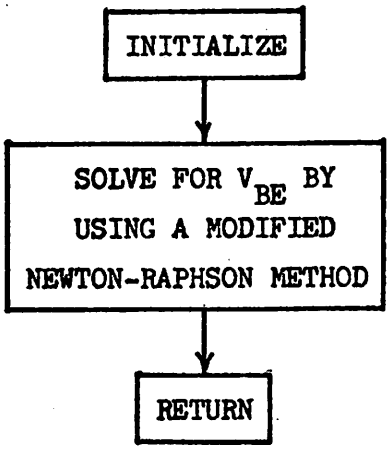
SUBROUTINE BMODEL



SUBROUTINE VJCT

This function subroutine computes the base-emitter junction voltage of a bipolar transistor from supplied values of collector current and collector-emitter voltage. A modified Newton-Raphson method similar to that of the BIAS-3 program [4] is used. VJCT is called from the subroutines BMODEL and CHECK.

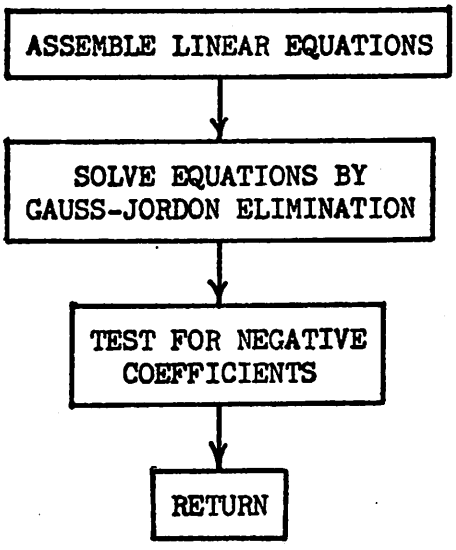
SUBROUTINE VJCT



SUBROUTINE FIT

This function subroutine computes the three current-dependent β_F coefficients from two sets of β_F and I_c specifications. The linear equations are first assembled [3] by a method of least squares. Next the equations are solved by the Gauss-Jordan elimination method. Finally a check is made for any negative coefficients. If any are found, FIT is set to -1.0.

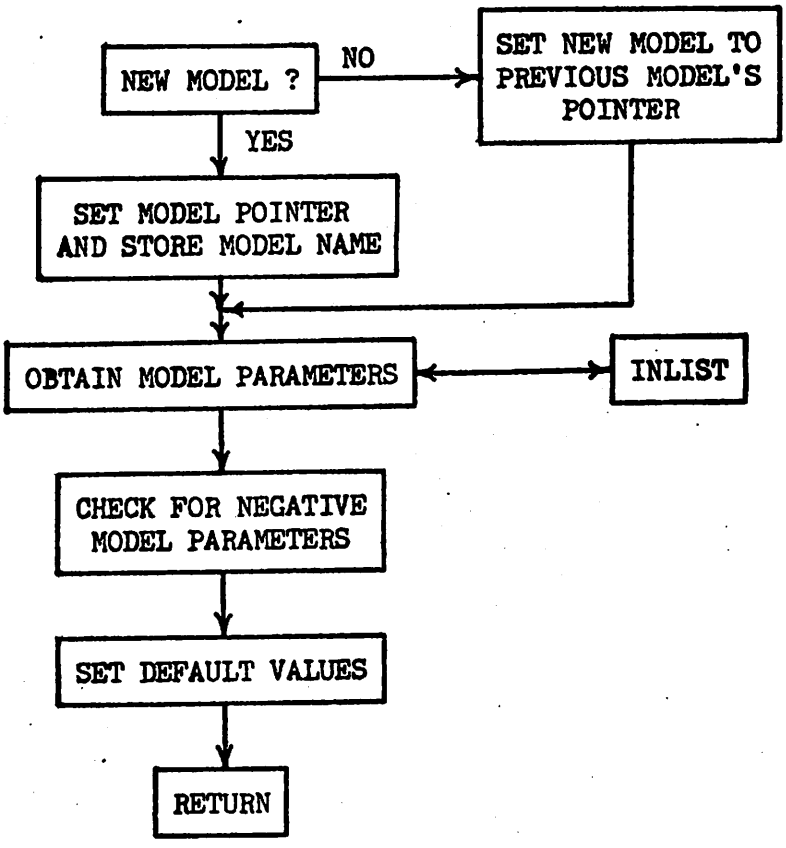
SUBROUTINE FIT



SUBROUTINE FMODEL

This subroutine reads and processes data on field-effect transistor model cards. Subroutine INLIST is called each time a new data record is needed. If the model has previously been read, the new data replaces old stored data. The model parameters are first read, stored, and checked for negative values. Finally any unspecified parameters are set to default values.

SUBROUTINE FMODEL



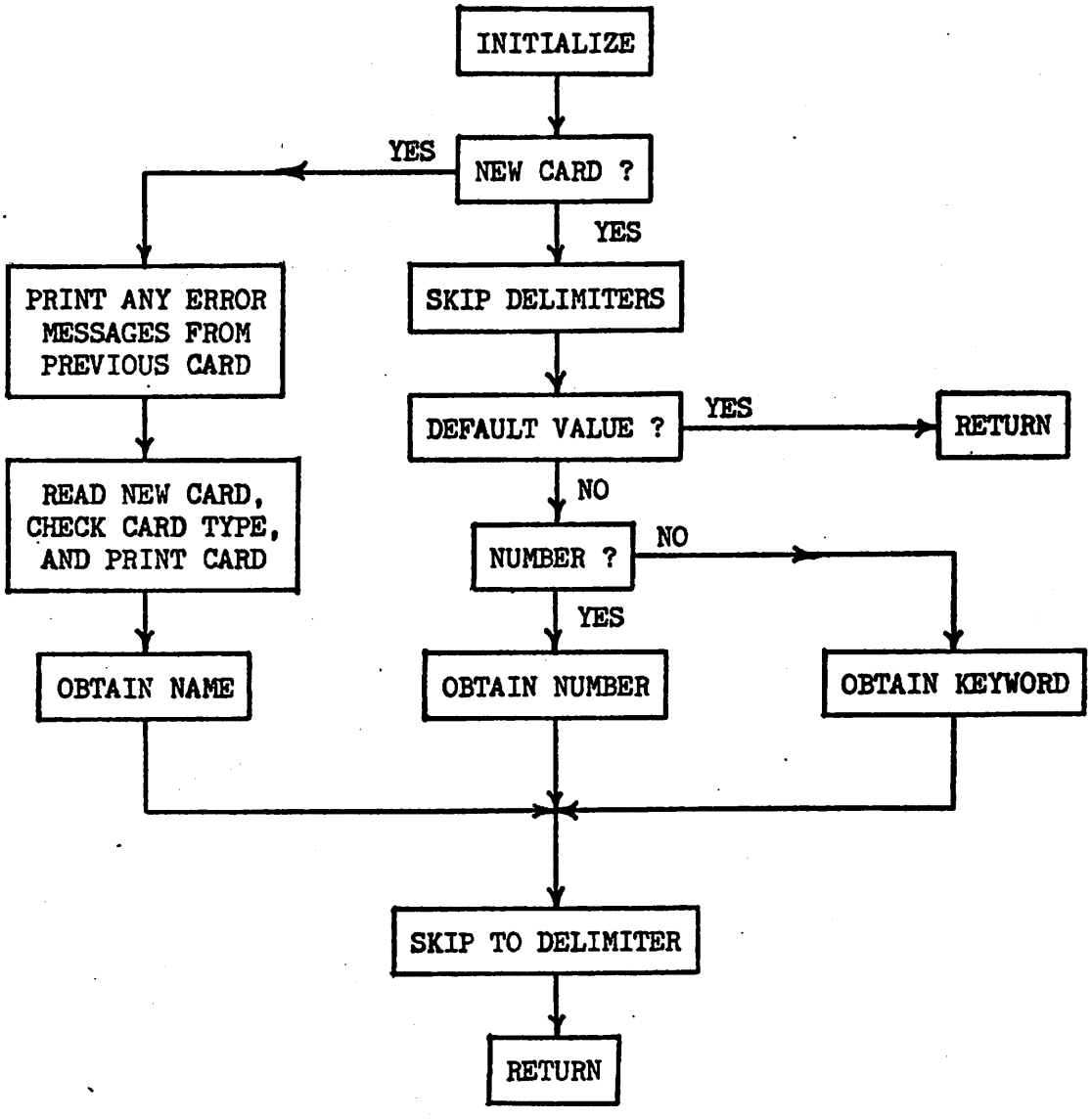
SUBROUTINE INLIST

This function subroutine reads and interprets the free-format input data. INLIST is called each time a new data record is needed.

Before reading a new data card, any error messages from the previous card are printed. The first record of the card is then read, the type of card identified, and the card printed. For element cards, the element name is also obtained. Control is then returned to the calling subroutine.

INLIST interprets a single data record as follows: first, a slash (/) indicating a default value is checked for. If found, control is returned to the calling subroutine. For a numeric data record, the value is obtained. Four forms of numeric data can be interpreted. A number may be an integer, a floating point number, either an integer or floating point number followed by an integer exponent (e.g., 1E-14 or 2.65E3), or either an integer or a floating point number followed by an engineering scale factor (G,MEG,K,M,U,N, or P). For a name data record, the type of keyword is determined. After interpretation of the data record, INLIST is set to -1 if no data was found, to 0 is a number was found, or to +1 if a name was found. Control is then returned to the calling subroutine.

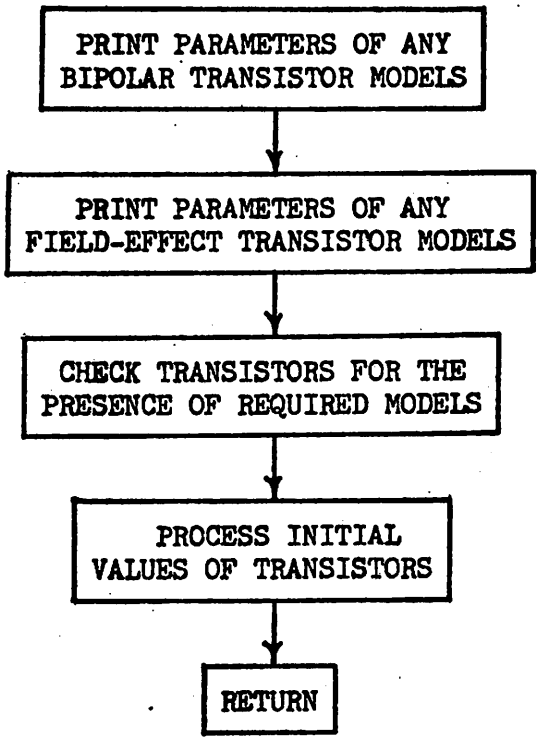
SUBROUTINE INLIST



SUBROUTINE CHECK

This subroutine begins by printing a summary of the transistor models. Bipolar transistor model parameters and then field-effect transistor model parameters are printed. Next transistors are checked for the presence of required models. Finally, initial values of bipolar and field-effect transistor junction voltages are determined.

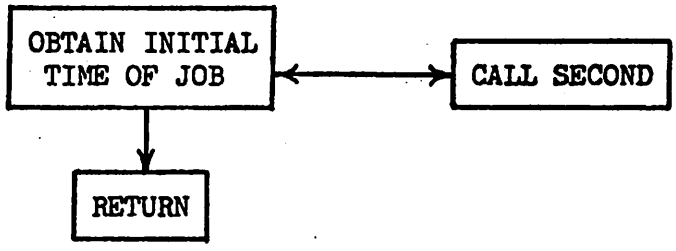
SUBROUTINE CHECK

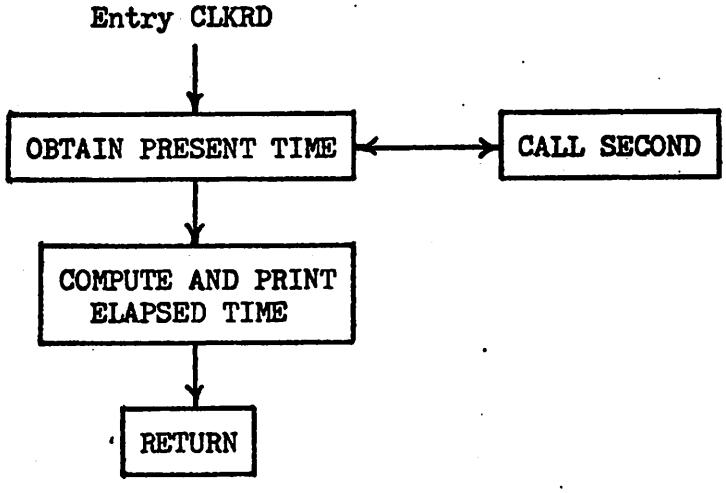


SUBROUTINE CLKST/CLKRD

This subroutine computes and prints the elapsed job time. A system library subroutine SECOND is called to obtain the time. At the beginning of each new job CLKST calls SECOND to obtain the initial job time. Entry CLKRD calls SECOND to obtain the present job time and then computes and prints the elapsed job time (the difference between the present job time and the initial job time).

SUBROUTINE CLKST/CLKRD



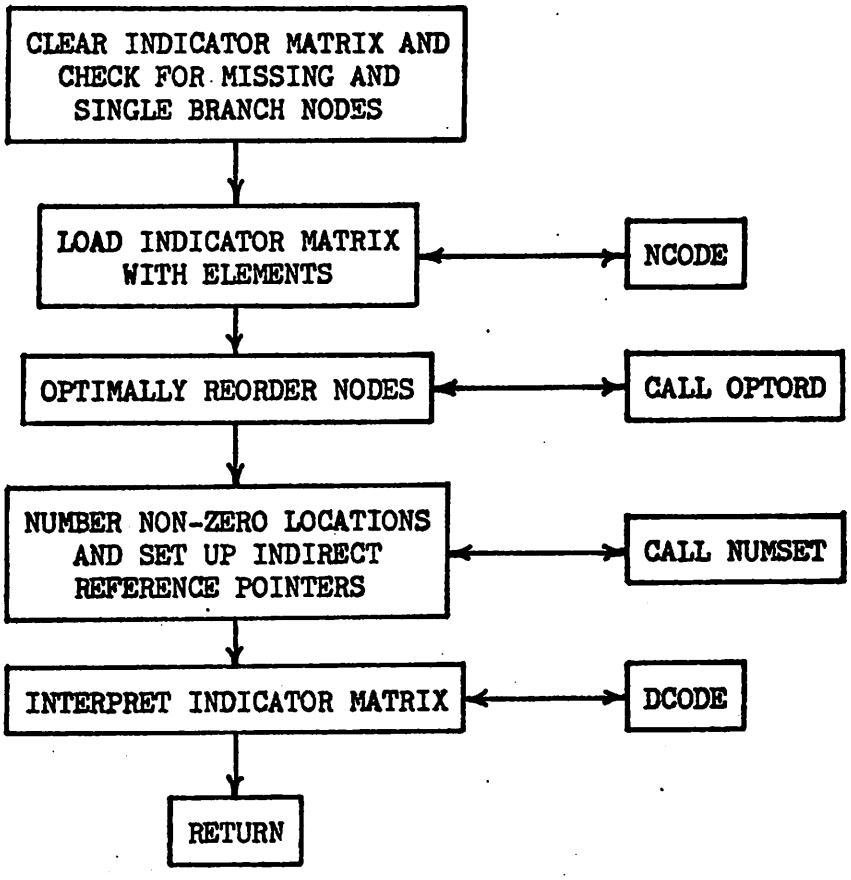


SUBROUTINE SETUP

This subroutine controls the generation of pointers used in a sparse matrix solution of a system of linear equations or in a sparse-matrix determinant evaluation. A square integer matrix called an indicator matrix is used here. This indicator matrix records the non-zero structure of the indefinite nodal admittance matrix.

First, the indicator matrix is zeroed and the circuit topology checked for missing and single branch nodes. Next, subroutine NCODE loads element positions into the indicator matrix. Subroutine OPTORD then optimally reorders the nodes and subroutine NUMSET numbers the non-zero entries of the indicator matrix and establishes arrays which store the singly dimensioned admittance matrix locations where the element values are later loaded.

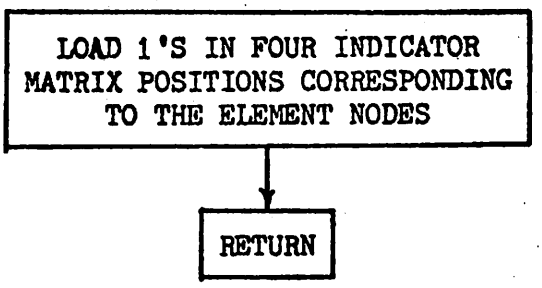
SUBROUTINE SETUP

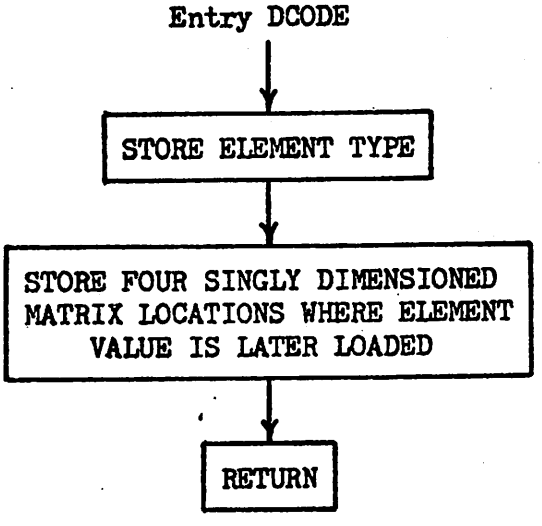


SUBROUTINE NCODE/DCODE

This subroutine loads and interprets the indicator matrix. Element nodes are received as arguments from the calling subroutine SETUP. For each element, NCODE loads non-zero values into four indicator matrix locations corresponding to locations in a square indefinite admittance matrix. Entry DCODE interprets the reordered indicator matrix by storing four locations of the singly dimensioned matrix where the element value is later loaded.

SUBROUTINE NCODE/DCODE

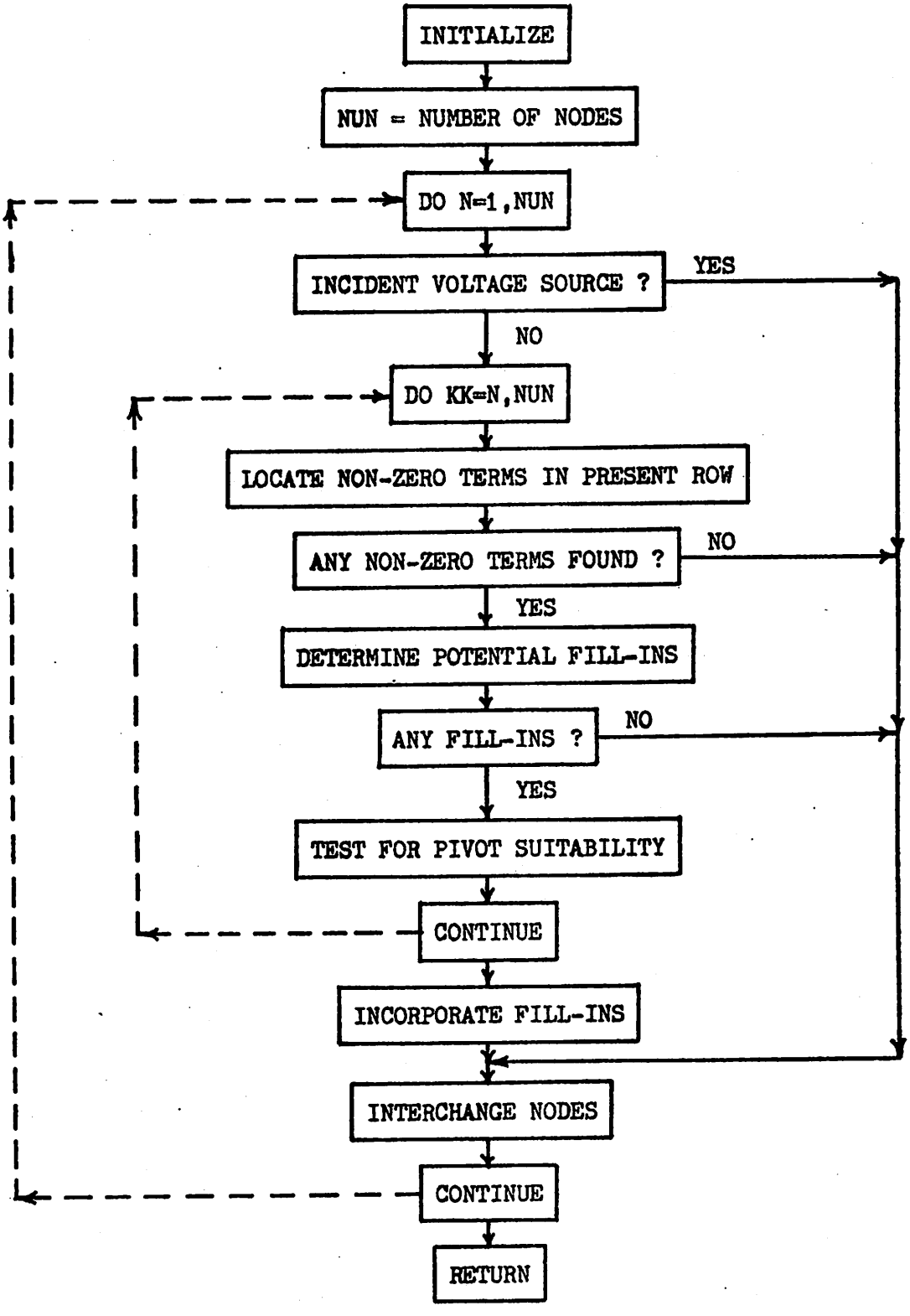




SUBROUTINE OPTORD

This subroutine optimally reorders the nodes to minimize the number of operations required in a sparse matrix solution of a system of linear equations or in a sparse matrix determinant evaluation. The method used is equivalent to that described by Berry [6]. A pseudo Gaussian elimination is performed on the indicator matrix to establish the optimal order. The node reordering process is conducted as follows: nodes incident with voltage sources are chosen first. Next selected are all nodes which as the pivot node in a Gaussian elimination create no new non-zero entries called fill-ins. Finally, the remaining nodes are reordered choosing at each step the node which creates the least number of fill-ins. In case of ties, nodes having the greatest number of off-diagonal entries are chosen first.

SUBROUTINE OPTORD

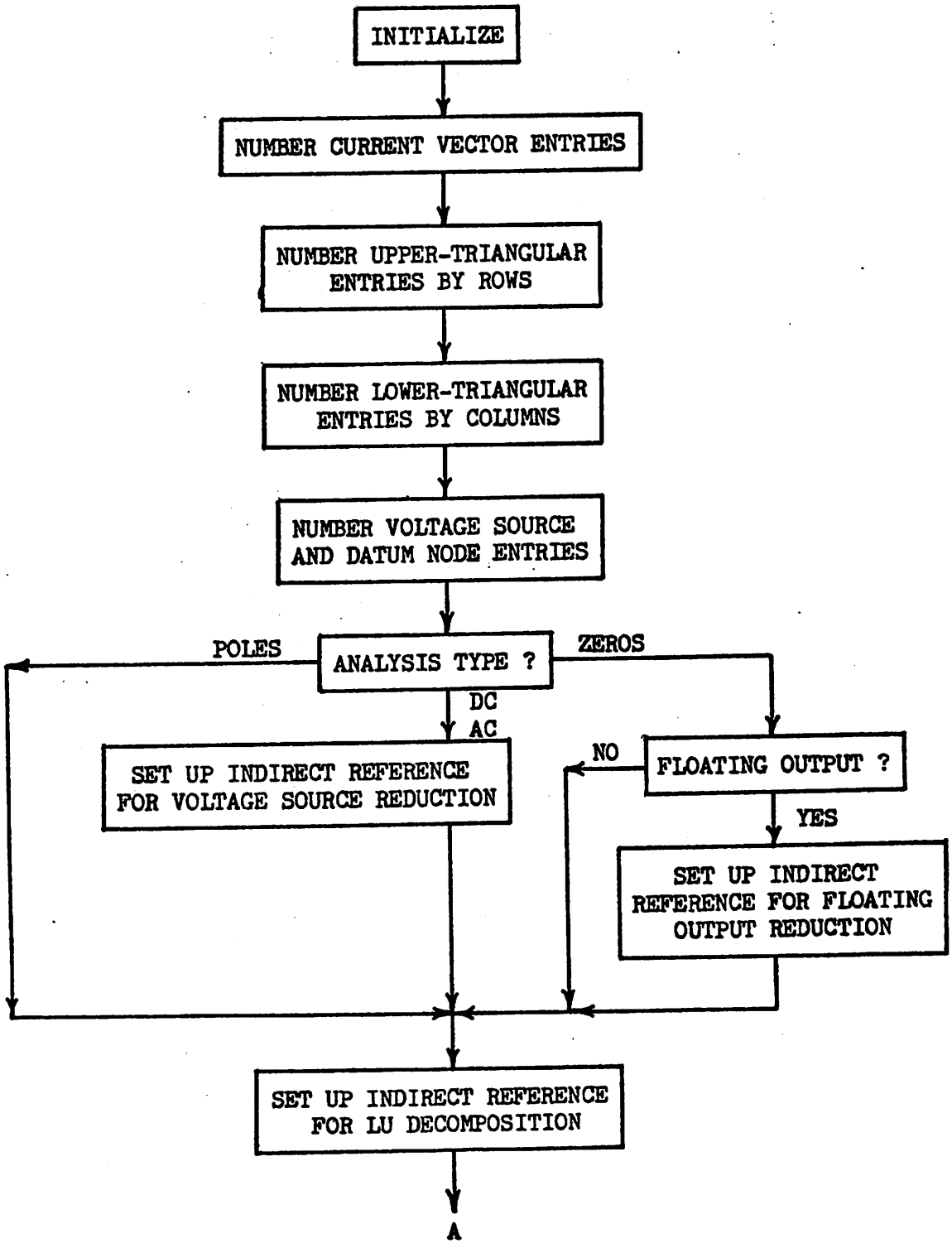


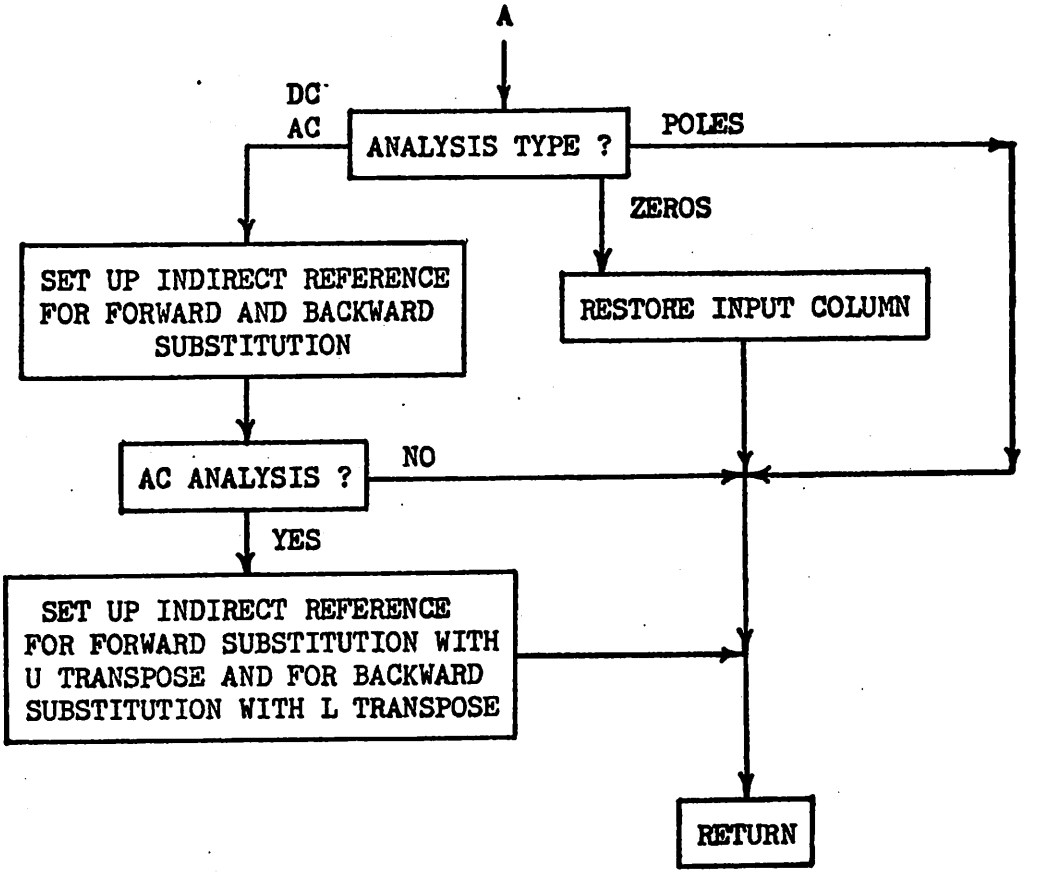
SUBROUTINE NUMSET

This subroutine first numbers the non-zero entries of the indicator matrix and then establishes the indirect reference pointers used in a sparse matrix solution of a system of linear equations or in a sparse matrix determinant evaluation. First, current vector entries are numbered. Next, entries on or above the matrix diagonal are numbered by rows from top to bottom and entries below the diagonal are numbered by columns from left to right. Finally, voltage source and datum node entries are numbered.

The indirect reference pointers are established in the following order: first, pointers for voltage source reduction, then pointers for the LU decomposition, followed by pointers for the forward substitution, and finally pointers for the backward substitution. For a small-signal analysis additional pointers are established for the forward substitution with the U transpose and the backward substitution with the L transpose. These additional pointers are used in computing the complex adjoint node voltages.

SUBROUTINE NUMSET

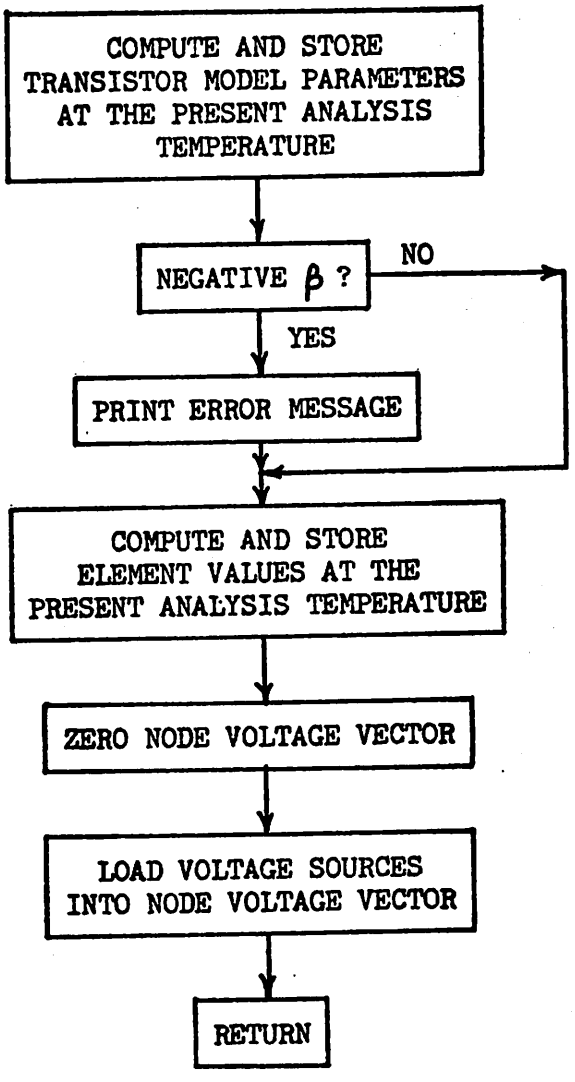



A
DC
AC
ANALYSIS TYPE ?
POLES
ZEROS
SET UP INDIRECT REFERENCE FOR FORWARD AND BACKWARD SUBSTITUTION
RESTORE INPUT COLUMN
AC ANALYSIS ?
NO
YES
SET UP INDIRECT REFERENCE FOR FORWARD SUBSTITUTION WITH U TRANSPOSE AND FOR BACKWARD SUBSTITUTION WITH L TRANSPOSE
RETURN

SUBROUTINE DCMOD

This subroutine computes the dc circuit models at the present analysis temperature. First, the saturation current, dc current gain β, basewidth modulation factor η, and the base and collector ohmic resistances are computed for each bipolar transistor. The thermal voltage and the drain and source ohmic resistances are computed for each field-effect transistor. Next, the resistor and voltage-controlled current source values are computed from the nominal values, first- and second-order temperature coefficients, and the present analysis temperature. Inductors and mutual inductance windings are modeled as 1 ohm resistances for the dc analysis. These element values are then stored for later loading into the singly dimensioned admittance matrix. Finally, the node voltage vector is zeroed and voltage source values are loaded into this vector.

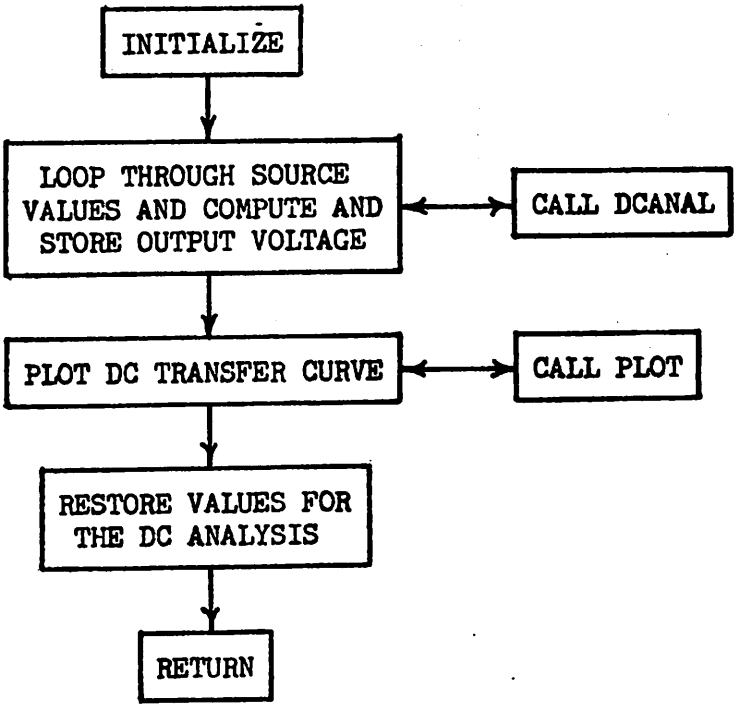
SUBROUTINE DCMOD



SUBROUTINE DCTRAN

This subroutine controls the calculation and plotting of a dc transfer curve. A single voltage or current source is stepped over a specified range. A maximum of 101 values is allowed. For each of these source values, a dc analysis is performed by calling subroutine DCANAL and a specified voltage between two nodes is stored. Next, subroutine PLOT plots this voltage as a function of the varied source. Finally, the dc circuit values are restored for the operating point dc analysis.

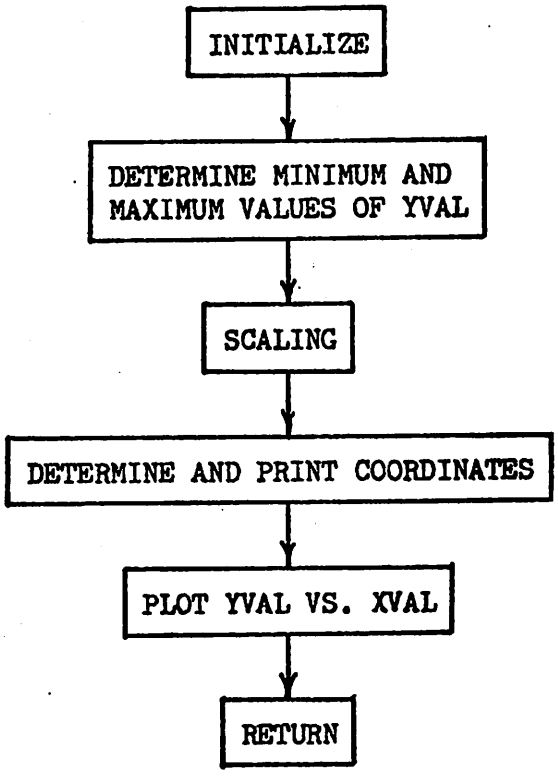
SUBROUTINE DCTRAN



SUBROUTINE PLOT

This subroutine plots the dc transfer curve. Two arrays containing the source and output voltage values are passed from the calling subroutine DCTRAN. The minimum and maximum values of output voltage are first determined. Next, a scaling operation is performed to determine the output voltage coordinates. These coordinates are then printed. Finally, each point of the dc transfer curve is printed along with the source and output voltage values.

SUBROUTINE PLOT



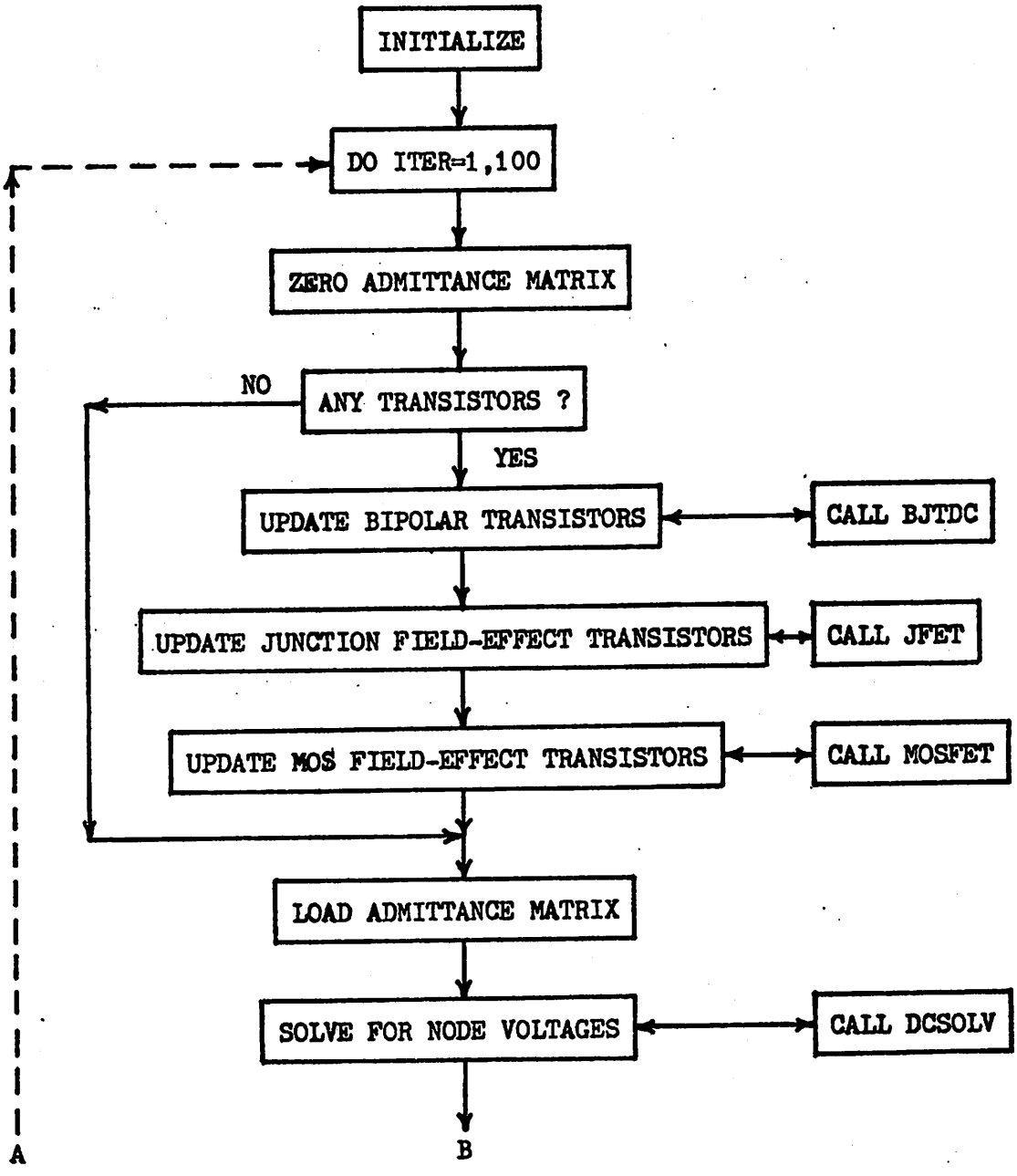
SUBROUTINE DCANAL

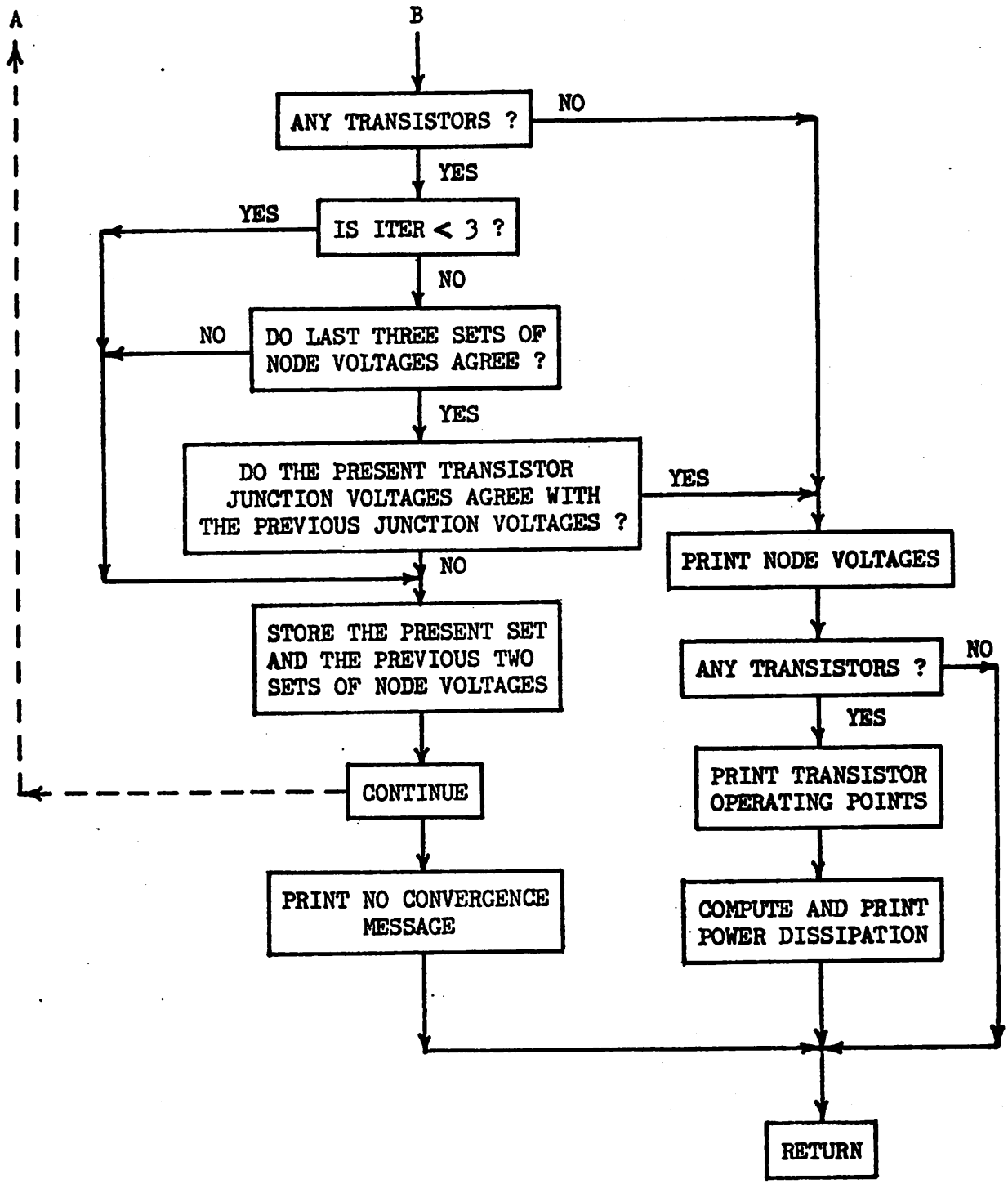
This subroutine controls the nonlinear dc analysis which computes the node voltages, transistor operating points, and power dissipation. The approach used is a modified Newton-Raphson procedure of BIAS-3 [4] in which changes in forward biased junction voltages are limited to values of less than $2V_T$ between iterations [7]. This method involves repeating a number of steps until node and transistor junction voltages agree with their previous values. First, trial transistor operating points are computed from the present set of node voltages, the nonlinear transistor models are linearized about these operating points, and a set of linear algebraic equations is assembled in terms of unknown node voltages. Next, a new set of node voltages is obtained by solving these equations and the new and old node voltage sets are compared. If there is no agreement to within 10 μV, the new node voltage set is used to generate new trial operating points and the process is repeated. This iterative process concludes when each node voltage agrees with two previous values and each junction voltage agrees with one previous value to within 10 μV.

The operation of DCANAL is now described. The singly dimensioned admittance matrix is first zeroed. Next, the transistor models are updated and linearized by calling subroutine BJTDC for bipolar transistors, subroutine JFET for junction field-effect transistors, and subroutine MOSFET for field-effect transistors.

The resistors, inductors (modeled as 1 ohm resistors), and linearized transistor model elements are then loaded into the admittance matrix and subroutine DCSOLV computes a new set of node voltages. For circuits with no transistors, only one iteration is needed to obtain the dc solution. For circuits containing transistors, three iterations are performed before circuit convergence is checked. At each iteration the present node voltage set and the previous two sets are stored. During the fourth and all following iterations circuit convergence is checked. If the present node voltage fails to agree with the previous two sets to within 10 μV, a new iteration is started. If agreement is reached, the present set of transistor junction voltages is compared with the previous set. If no agreement to within 10 μV, a new iteration is started. If agreement is reached, the iterative process is complete and the node voltages are printed. The transistor operating points and the circuit power dissipation are also printed for circuits containing transistors.

SUBROUTINE DCANAL




A
B
ANY TRANSISTORS ?
NO
YES
IS ITER < 3 ?
YES
NO
DO LAST THREE SETS OF NODE VOLTAGES AGREE ?
NO
YES
DO THE PRESENT TRANSISTOR JUNCTION VOLTAGES AGREE WITH THE PREVIOUS JUNCTION VOLTAGES ?
YES
NO
STORE THE PRESENT SET AND THE PREVIOUS TWO SETS OF NODE VOLTAGES
CONTINUE
PRINT NO CONVERGENCE MESSAGE
PRINT NODE VOLTAGES
ANY TRANSISTORS ?
NO
YES
PRINT TRANSISTOR OPERATING POINTS
COMPUTE AND PRINT POWER DISSIPATION
RETURN

SUBROUTINE BJTDC

This subroutine computes the incremental bipolar transistor models used in the nonlinear dc analysis. Based on the present set of node voltages, new base-emitter and base-collector junction voltages are first determined by subroutine UPDATE. UPDATE limits a new forward biased junction voltage to changes of less than $2V_T$ from the previous value [7]. Next, eight incremental model elements (g_{mf},$g_{\pi f}$,g_{mr},$g_{\pi r}$,I_{CCN},I_{CBN},I_{ECN}, and I_{EBN}) [3] are computed. The incremental model is shown on the next page. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements (refer to McCalla [3] for details):

$$\eta = \frac{V_T}{V_A}$$

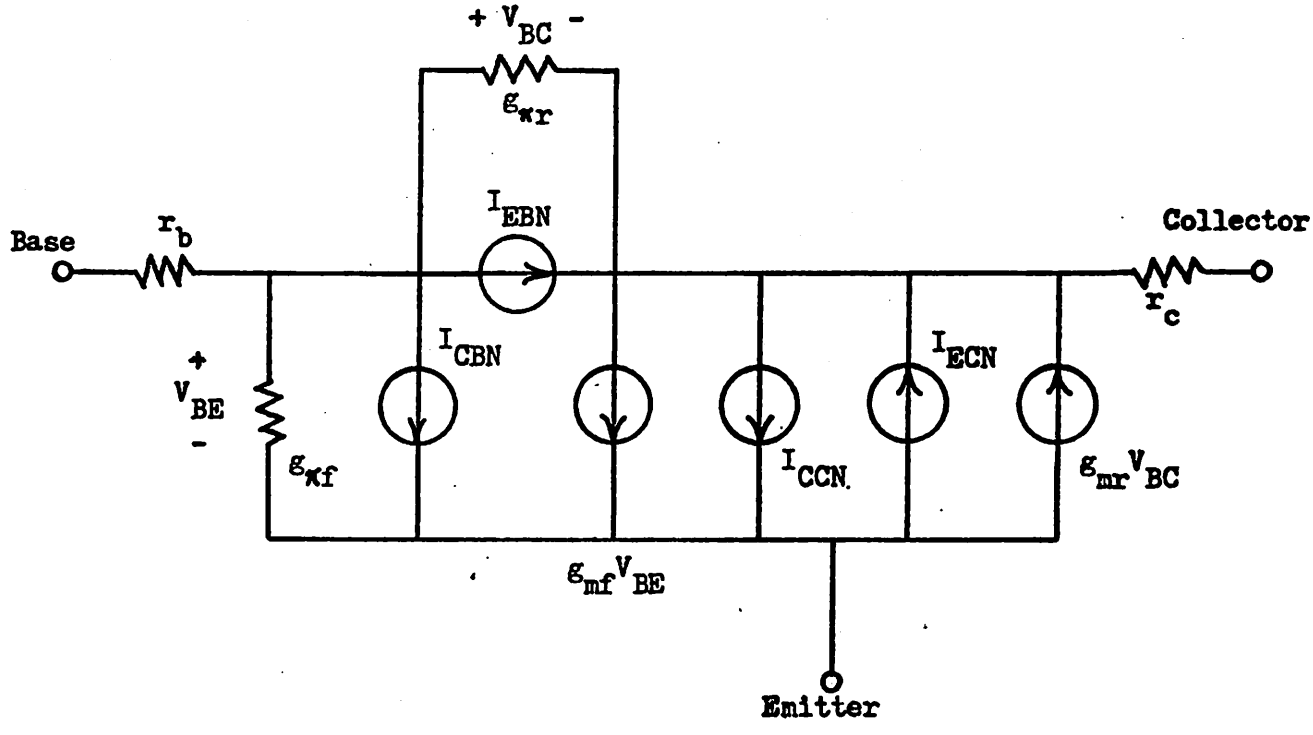
$$X = 1 - \eta \frac{V_{BC}}{V_T}$$

$$\theta = \left[\frac{C_3 I_{SS}}{C_1}\right]^{1/2}$$

$$I_{CC} = \frac{XI_{SS}}{1 + \theta e^{V_{BE}/2V_T}} e^{V_{BE}/V_T}$$

$$I_{EC} = XI_{SS} e^{V_{BC}/V_T}$$

$$I_{CT} = I_{CC} + XI_{SS}$$



Incremental Bipolar Transistor Model

$$\beta_F = \frac{X}{C_1 + C_2 I_{CT}^{-1/2} + C_3 I_{CT}}$$

$$\beta_R = X\beta_{RO}$$

$$\beta_0 = \frac{X}{C_1 + \frac{1}{2} C_2 I_{CT}^{-1/2} + 2C_3 I_{CT}}$$

$$g_{mf} = \frac{I_{CC}}{V_T} \frac{1 + \frac{\theta}{2} e^{V_{BE}/2V_T}}{1 + \theta e^{V_{BE}/2V_T}}$$

$$g_{\pi f} = \frac{1}{\beta_0} g_{mf}$$

$$g_{mr} = \frac{I_{EC}}{V_T} + \frac{1}{XV_T} \eta(I_{CC} - I_{EC})$$

$$g_{\pi r} = \frac{1}{\beta_R} \frac{I_{EC}}{V_T}$$

$$I_{CC1} = \frac{XI_{SS}}{1 + \theta e^{V_{BE}/2V_T}} (e^{V_{BE}/V_T} - 1)$$

$$I_{EC1} = XI_{SS}(e^{V_{BC}/V_T} - 1)$$

$$I_{CCN} = \frac{I_{CC1}}{X} - g_{mf} V_{BE}$$

$$I_{CBN} = \frac{I_{CC1}}{\beta_F} - g_{\pi f} V_{BE}$$

$$I_{ECN} = \frac{I_{EC1}}{X} - \frac{I_{EC}}{V_T} V_{BC}$$

$$I_{EBN} = \frac{I_{EC1}}{\beta_R} - g_{\pi r} V_{BC}$$

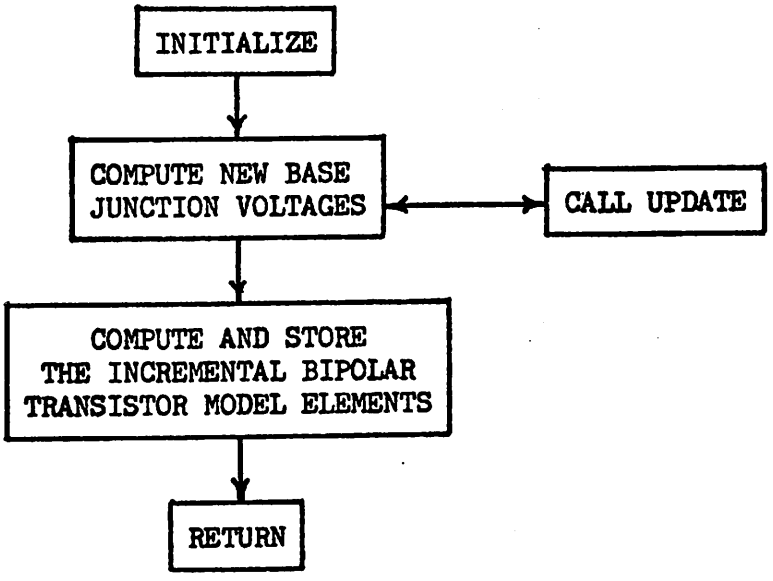
where: V_A = Early voltage

C_1, C_2, C_3 = coefficients of the current dependent forward β

I_{SS} = reverse saturation current

β_{RO} = reverse β

SUBROUTINE BJTDC



SUBROUTINE JFET

This subroutine computes the incremental models of junction field-effect transistors for the nonlinear dc analysis. The model used is based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11]. Based on the present set of node voltages, new gate-drain and gate-source junction voltages are first determined by calling subroutine UPDATE. Next, the gate junction model elements (g_{GD}, g_{GS}, I_{EQGD}, and I_{EQGS}) are computed. The drain current and derivatives (g_M and G_{DS}) are then computed for either the normal mode or inverse mode depending on the polarity of the drain-source voltage. Next, an equivalent drain current source (I_{DREQ}) is computed. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements:

I. Gate Junction Models

$$I_{GS} = I_S(e^{V_{GS}/V_T} - 1)$$

$$g_{GS} = \frac{I_S + I_{GS}}{V_T}$$

$$I_{EQGS} = I_{GS} - g_{GS}V_{GS}$$

$$I_{GD} = (e^{V_{GD}/V_T} - 1)$$

$$g_{GD} = \frac{I_S + I_{GD}}{V_T}$$

$$I_{EQGD} = I_{GD} - g_{GD}V_{GD}$$

II. Drain Current and Derivatives

A. Normal Mode $[V_{DS} \geq 0]$

1. Cutoff region $(V_{GS}-V_{TO}) \leq 0$

$$I_D = g_M = g_{DS} = 0$$

2. Saturation region $0 \leq (V_{GS}-V_{TO}) \leq V_{DS}$

$$I_D = \beta(V_{GS}-V_{TO})[(V_{GS}-V_{TO}) + \lambda V_{DS}]$$

$$g_M = \beta[2(V_{GS}-V_{TO}) + \lambda V_{DS}]$$

$$g_{DS} = \beta\lambda(V_{GS}-V_{TO})$$

3. Linear region $(V_{GS}-V_{TO}) \geq V_{DS}$

$$I_D = \beta V_{DS}[(2+\lambda)(V_{GS}-V_{TO}) - V_{DS}]$$

$$g_M = \beta(2+\lambda)V_{DS}$$

$$g_{DS} = \beta[(2+\lambda)(V_{GS}-V_{TO}) - 2V_{DS}]$$

B. Inverse Mode $[V_{DS} < 0]$

1. Cutoff region $(V_{GS}-V_{DS}-V_{TO}) \leq 0$

$$I_D = g_M = g_{DS} = 0$$

2. Saturation region $\quad 0 \leq (V_{GS}-V_{DS}-V_{TO}) \leq -V_{DS}$

$$I_D = -\beta(V_{GS}-V_{DS}-V_{TO})[(V_{GS}-V_{DS}-V_{TO}) - \lambda V_{DS}]$$

$$g_M = -\beta[2(V_{GS}-V_{DS}-V_{TO}) - \lambda V_{DS}]$$

$$g_{DS} = \beta\lambda(V_{GS}-V_{DS}-V_{TO}) - g_M$$

3. Linear region $\quad (V_{GS}-V_{DS}-V_{TO}) \geq -V_{DS}$

$$I_D = \beta V_{DS}[(2+\lambda)(V_{GS}-V_{DS}-V_{TO}) + V_{DS}]$$

$$g_M = \beta V_{DS}(2+\lambda)$$

$$g_{DS} = \beta[(2+\lambda)(V_{GS}-V_{DS}-V_{TO}) + 2V_{DS}] - g_M$$

III. Equivalent Drain Current Source

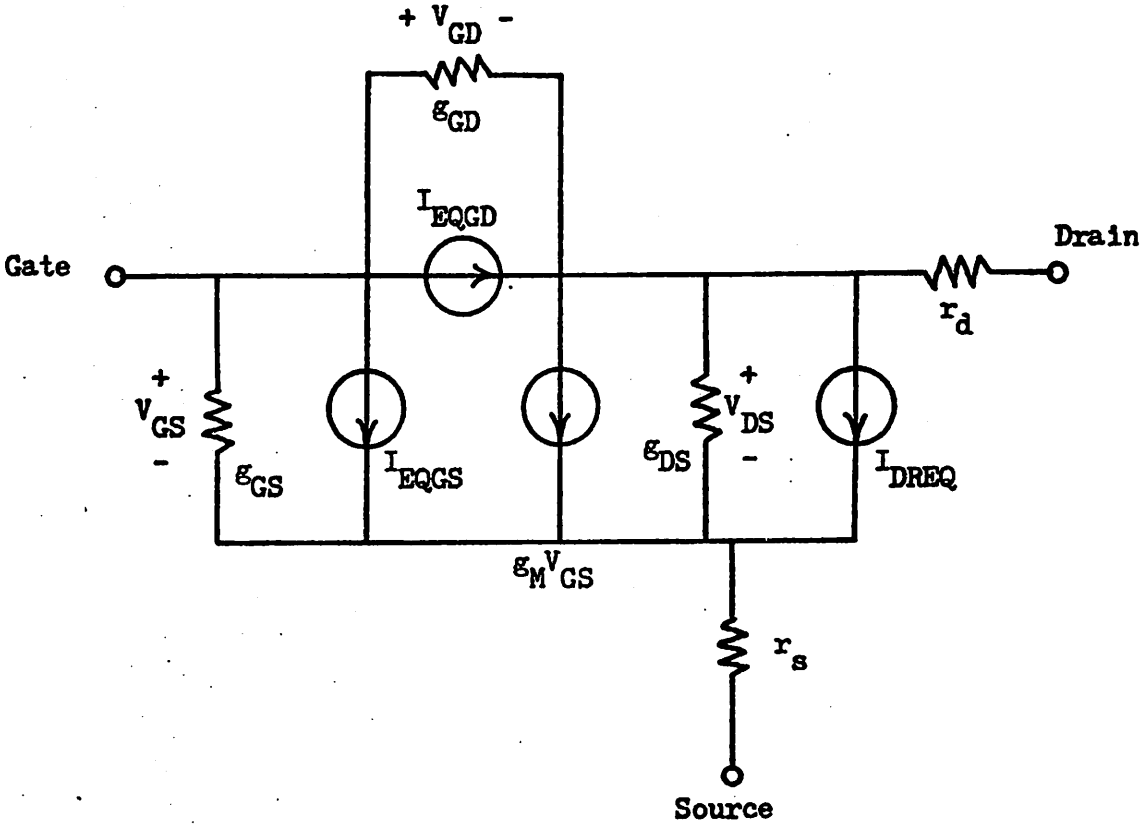
$$I_{DREQ} = I_D - g_M V_{GS} - g_{DS} V_{DS}$$

where: V_{TO} = threshold voltage

β = transconductance parameter

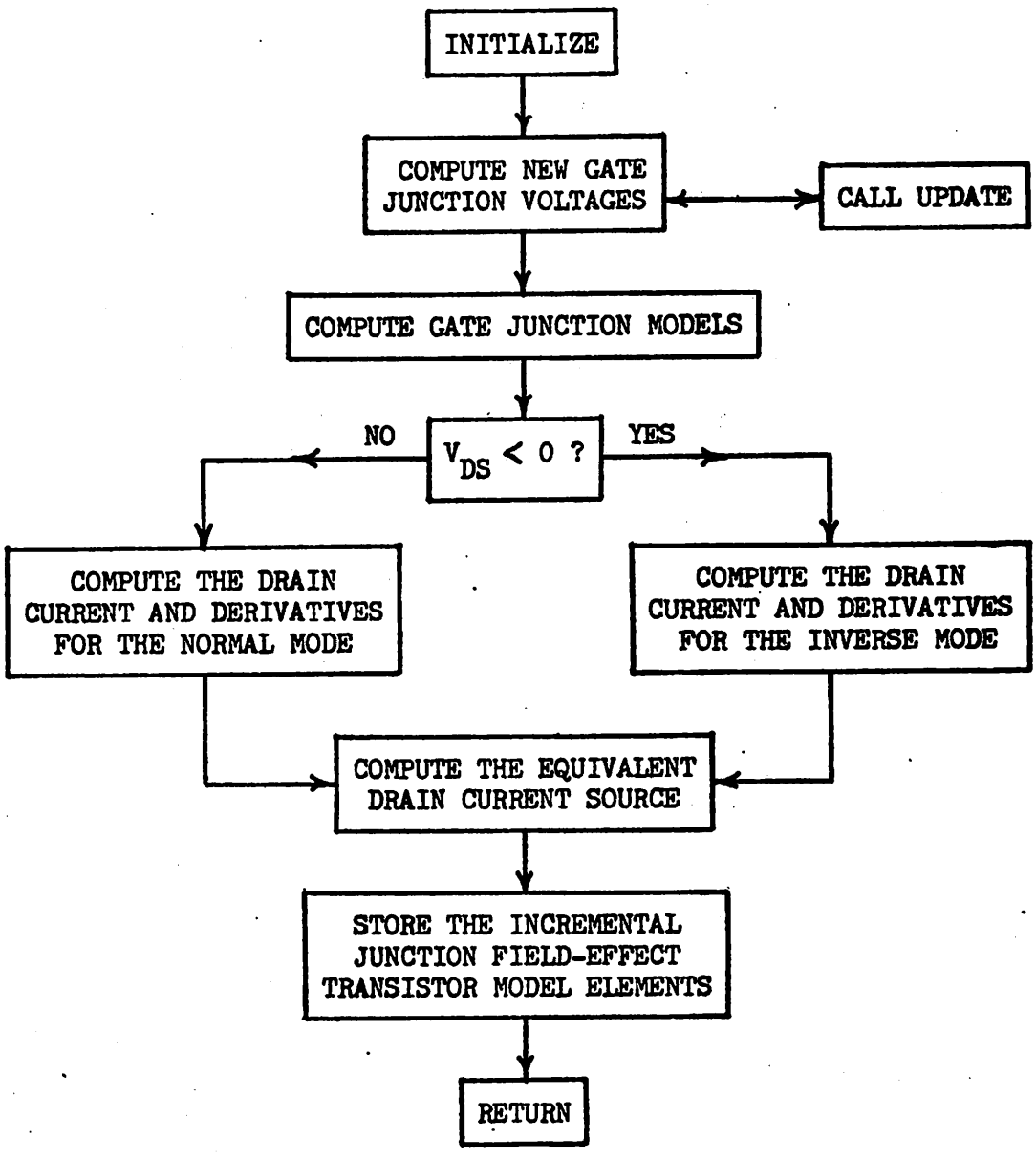
λ = channel length modulation factor

I_S = gate junction saturation current



Incremental Junction Field-effect Transistor Model

SUBROUTINE JFET



SUBROUTINE MOSFET

This subroutine computes the incremental models of MOS field-effect transistors for the nonlinear dc analysis. The model used is based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11]. Based on the present set of node voltages, new substrate-drain and substrate-source junction voltages are first determined by calling subroutine UPDATE. Next, the substrate (bulk) junction model elements (g_{BD},g_{BS},I_{EQBD}, and I_{EQBS}) are computed. The drain current and derivatives (g_M,g_{DS}, and g_{MBS}) are then computed for either the normal mode or inverse mode depending on the polarity of the drain-source voltage. Next, an equivalent drain current source (I_{DREQ}) is computed. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements:

I. Substrate Junction Models

$$I_{BD} = I_S(e^{V_{BD}/V_T} - 1)$$

$$g_{BD} = \frac{I_S + I_{BD}}{V_T}$$

$$I_{EQBD} = I_{BD} - g_{BD}V_{BD}$$

$$I_{BS} = I_S(e^{V_{BS}/V_T} - 1)$$

$$g_{BS} = \frac{I_S + I_{BS}}{V_T}$$

$$I_{EQBS} = I_{BS} - g_{BS}V_{BS}$$

II. Drain Current and Derivatives

A. Normal Mode $[V_{DS} \geq 0]$

$$V_T = V_{TO} + \gamma[(\phi - V_{BS})^{1/2} - \phi^{1/2}]$$

1. Cutoff region $(V_{GS}-V_T) \leq 0$

$$I_D = g_M = g_{DS} = g_{MBS} = 0$$

2. Saturation region $0 \leq (V_{GS}-V_T) \leq V_{DS}$

$$I_D = \beta(V_{GS}-V_T)[(V_{GS}-V_T) + \lambda V_{DS})$$

$$g_M = \beta[2(V_{GS}-V_T) + \lambda V_{DS}]$$

$$g_{DS} = \beta\lambda(V_{GS}-V_T)$$

$$g_{MBS} = \frac{g_M\gamma}{2}[\phi - V_{BS}]^{-1/2}$$

3. Linear region $(V_{GS}-V_T) \geq V_{DS}$

$$I_D = \beta V_{DS}[(2+\lambda)(V_{GS}-V_T) - V_{DS}]$$

$$g_M = \beta(2+\lambda)V_{DS}$$

$$g_{DS} = \beta[(2+\lambda)(V_{GS}-V_T) - 2V_{DS}]$$

$$g_{MBS} = \frac{g_M \gamma}{2} [\phi - V_{BS}]^{-1/2}$$

B. Inverse Mode $[V_{DS} < 0]$

$$V_T = V_{TO} + \gamma[(\phi + V_{DS} - V_{BS})^{1/2} - \phi^{1/2}]$$

1. Cutoff region $(V_{GS} - V_{DS} - V_T) \leq 0$

$$I_D = g_M = g_{DS} = g_{MBS} = 0$$

2. Saturation region $0 \leq (V_{GS} - V_{DS} - V_T) \leq -V_{DS}$

$$I_D = -\beta(V_{GS} - V_{DS} - V_T)[(V_{GS} - V_{DS} - V_T) - \lambda V_{DS}]$$

$$g_M = -\beta[2(V_{GS} - V_{DS} - V_T) - \lambda V_{DS}]$$

$$g_{DS} = \beta\lambda(V_{GS} - V_{DS} - V_T)$$

$$- g_M[1 + \frac{\gamma}{2}(\phi + V_{DS} - V_{BS})^{1/2}]$$

$$g_{MBS} = \frac{g_M \gamma}{2} [\phi + V_{DS} - V_{BS}]^{-1/2}$$

3. Linear region $(V_{GS} - V_{DS} - V_T) \geq -V_{DS}$

$$I_D = \beta V_{DS}[(2+\lambda)(V_{GS} - V_{DS} - V_T) + V_{DS}]$$

$$g_M = \beta V_{DS}(2+\lambda)$$

$$g_{DS} = \beta[(2+\lambda)(V_{GS} - V_{DS} - V_T) + 2V_{DS}]$$

$$- g_M[1 - \frac{\gamma}{2}(\phi + V_{DS} - V_{BS})^{-1/2}]$$

$$g_{MBS} = \frac{g_M \gamma}{2} [\phi + V_{DS} - V_{BS}]^{-1/2}$$

III. Equivalent Drain Current Source

$$I_{DREQ} = I_D - g_M V_{GS} - g_{DS} V_{DS} - g_{MBS} V_{BS}$$

where:

V_{TO} = threshold voltage

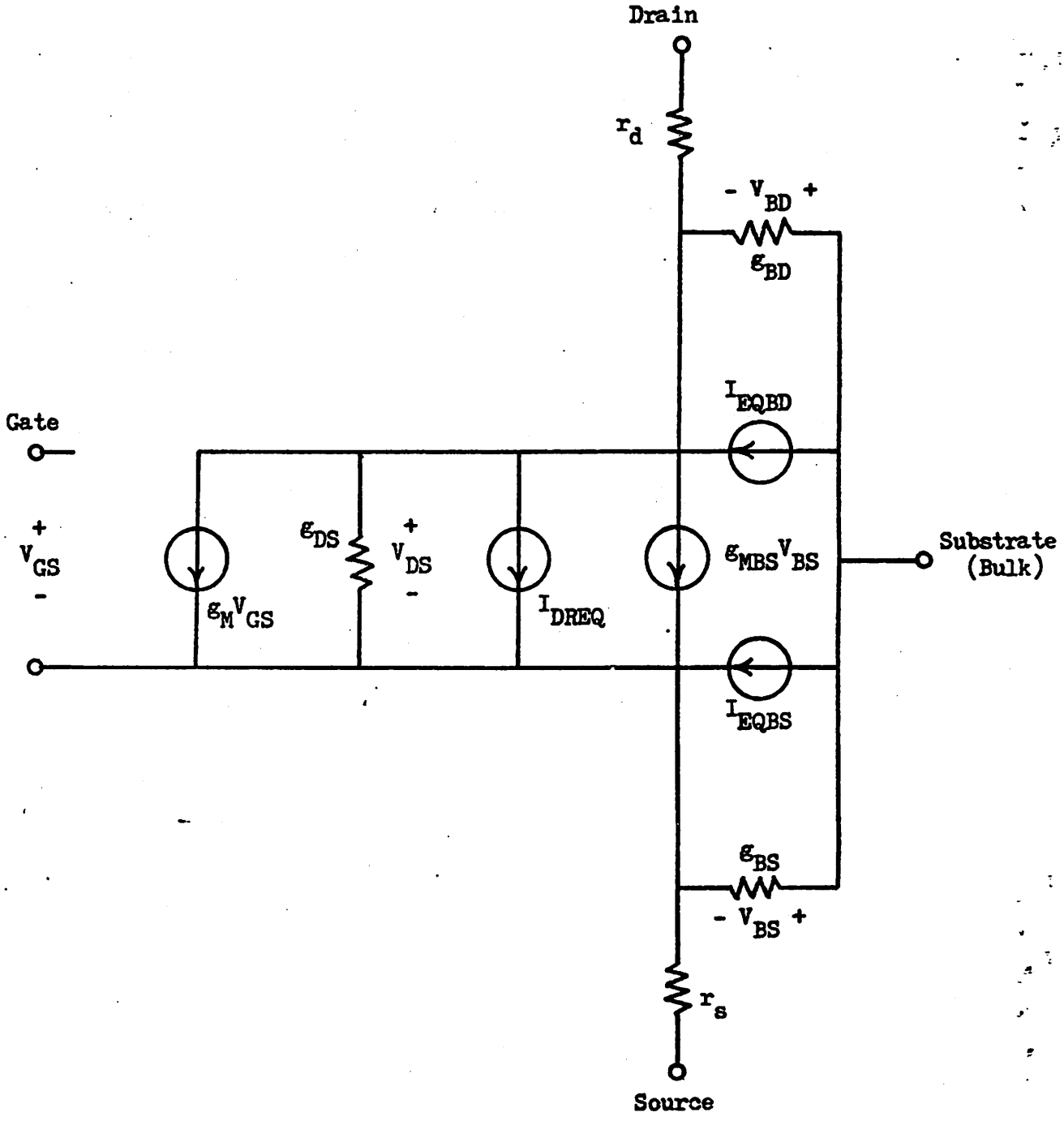
ϕ = surface potential

β = transconductance parameter

γ = substrate threshold parameter

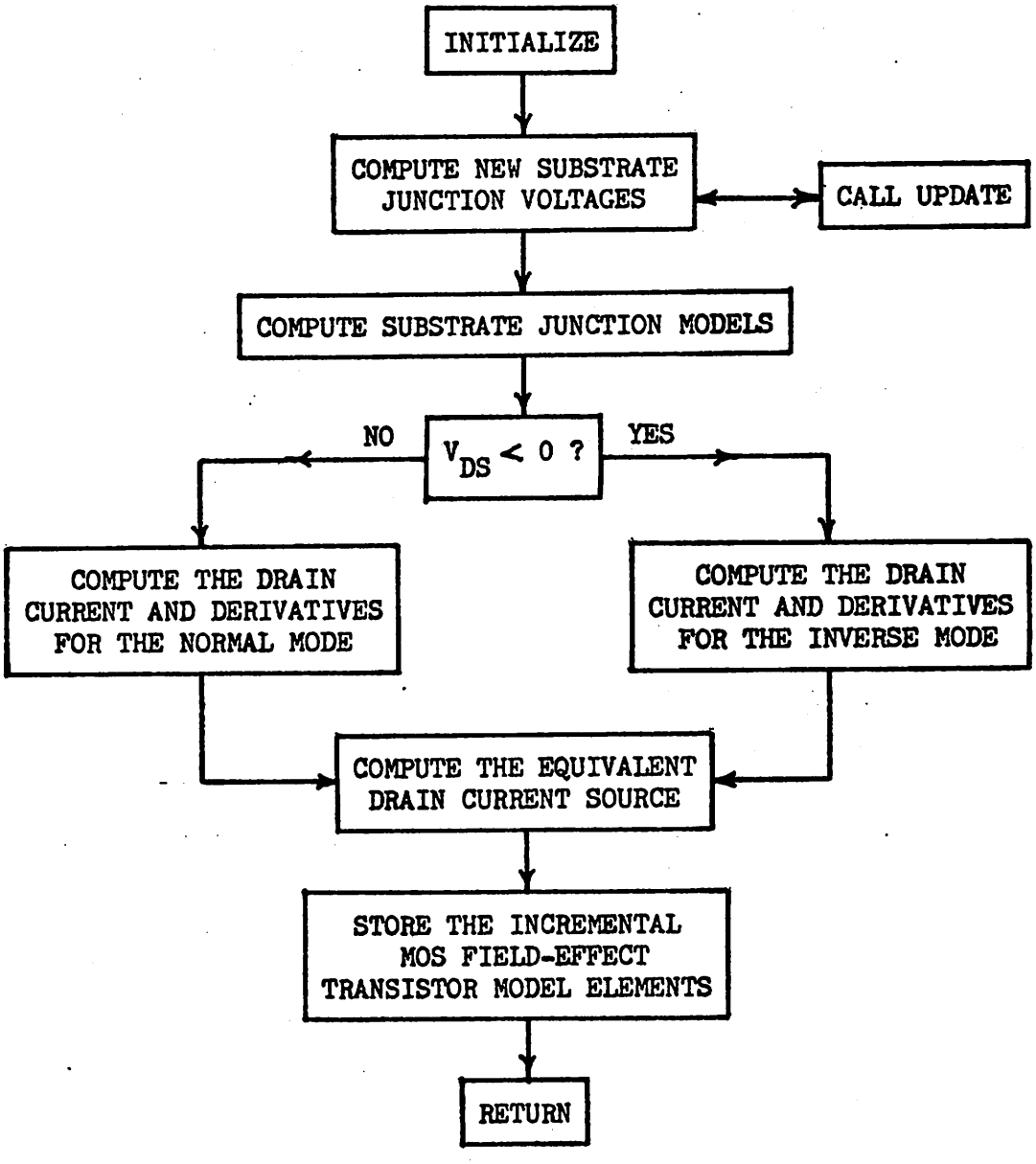
λ = channel length modulation factor

I_S = substrate junction saturation current



Incremental MOS Field-effect Transistor Model

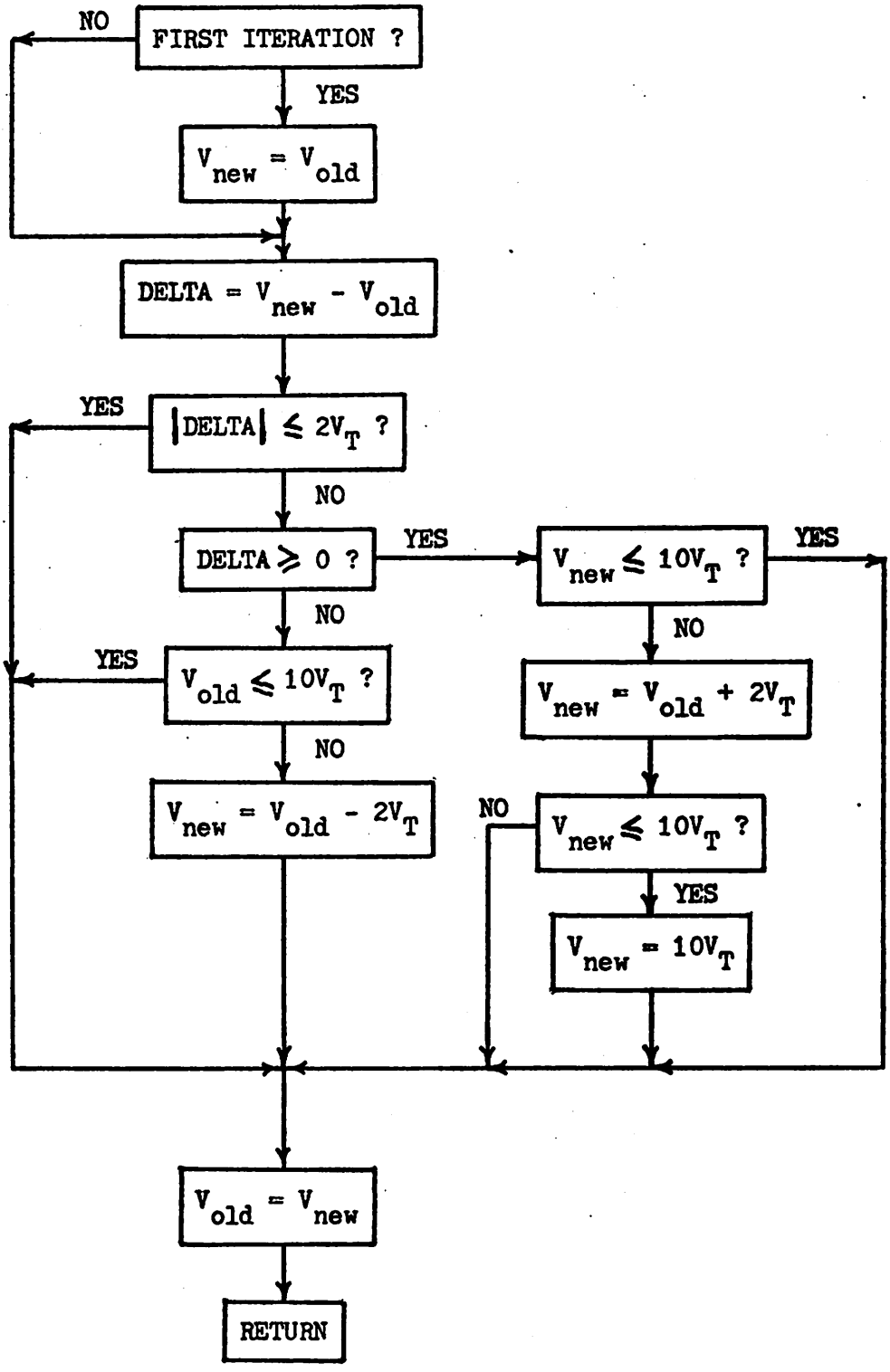
SUBROUTINE MOSFET



SUBROUTINE UPDATE

This subroutine determines a new transistor junction voltage from the previous value and the new node voltages. A forward biased junction voltage is limited to changes of less than $2V_T$ from the previous value. The difference between the previous junction voltage and the junction voltage obtained from the new node voltages is first computed. If the magnitude of this difference is less than or equal to $2V_T$, the new junction voltage is the value obtained from the node voltages. If the magnitude is greater than $2V_T$, the polarity of this difference is checked. For a negative difference and a previous junction voltage less than or equal to $10V_T$, the new junction voltage is the value obtained from the node voltages. For a negative difference and a previous junction voltage greater than $10V_T$, the new junction voltage is the previous value decreased by $2V_T$. For a positive difference and a value from the node voltages of less than or equal to $10V_T$, the new junction voltage is this value. For a positive difference and a value from the node voltages of greater than $10V_T$, the new junction voltage is the previous value increased by $2V_T$ or $10V_T$, whichever is greater. The above method is equivalent to that described by Nagel [7][11].

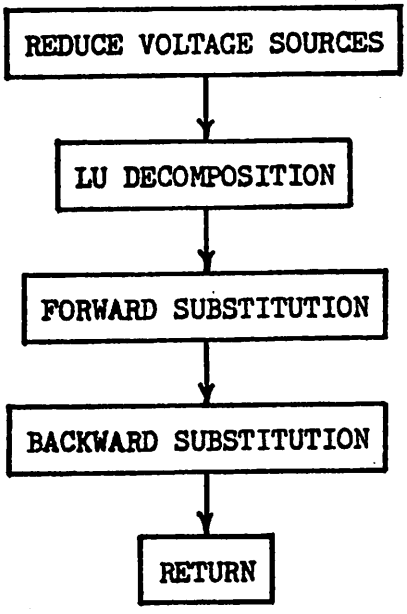
SUBROUTINE UPDATE



SUBROUTINE DCSOLV

This subroutine solves the sparse system of linear nodal admittance equations for the dc node voltages. First, the admittance matrix elements of the column corresponding to a voltage source node are multiplied by the value of the source and subtracted from the current vector. This is called voltage source reduction and is done for each voltage source. Next, an LU decomposition is performed on the singly dimensioned admittance matrix. This is equivalent to partitioning a square admittance matrix into upper and lower triangular matrices. Forward substitution is then performed which effectively transfers the lower triangular matrix into the current vector. Finally, backward substitution is performed resulting in the dc node voltages and voltage source currents.

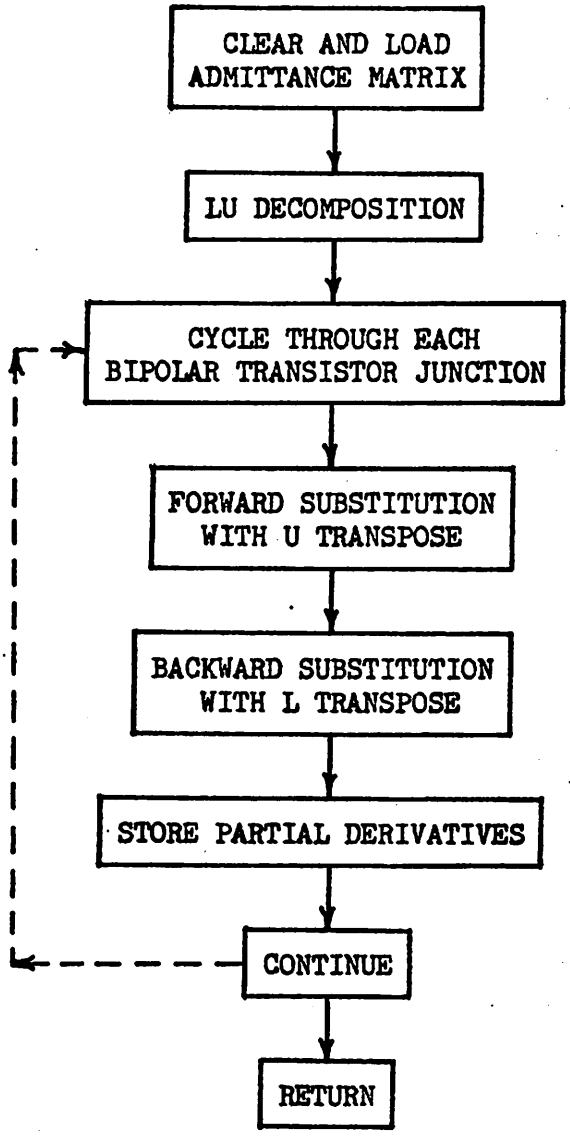
SUBROUTINE DCSOLV



SUBROUTINE DCADJ

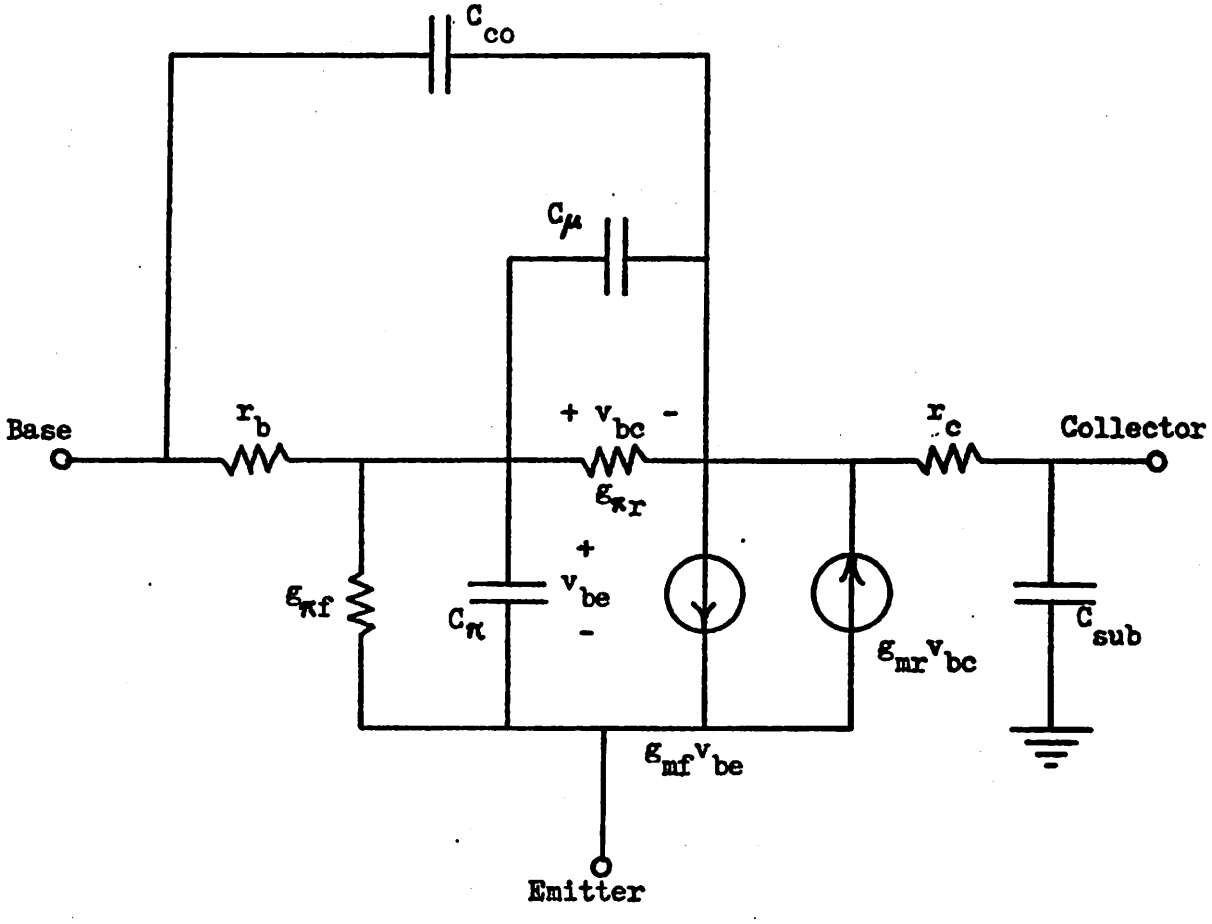
This subroutine computes the sensitivity (partial derivative) of each bipolar transistor junction voltage with respect to each sensitivity designated resistor. The adjoint method of Director and Rohrer [8] is used. The admittance matrix is first zeroed and loaded and then an LU decomposition is performed. Finally, for each bipolar transistor junction the following steps are performed: adjoint excitation vector computation, forward substitution with U transpose, backward substitution with L transpose, and storage of the partial derivatives.

SUBROUTINE DCADJ

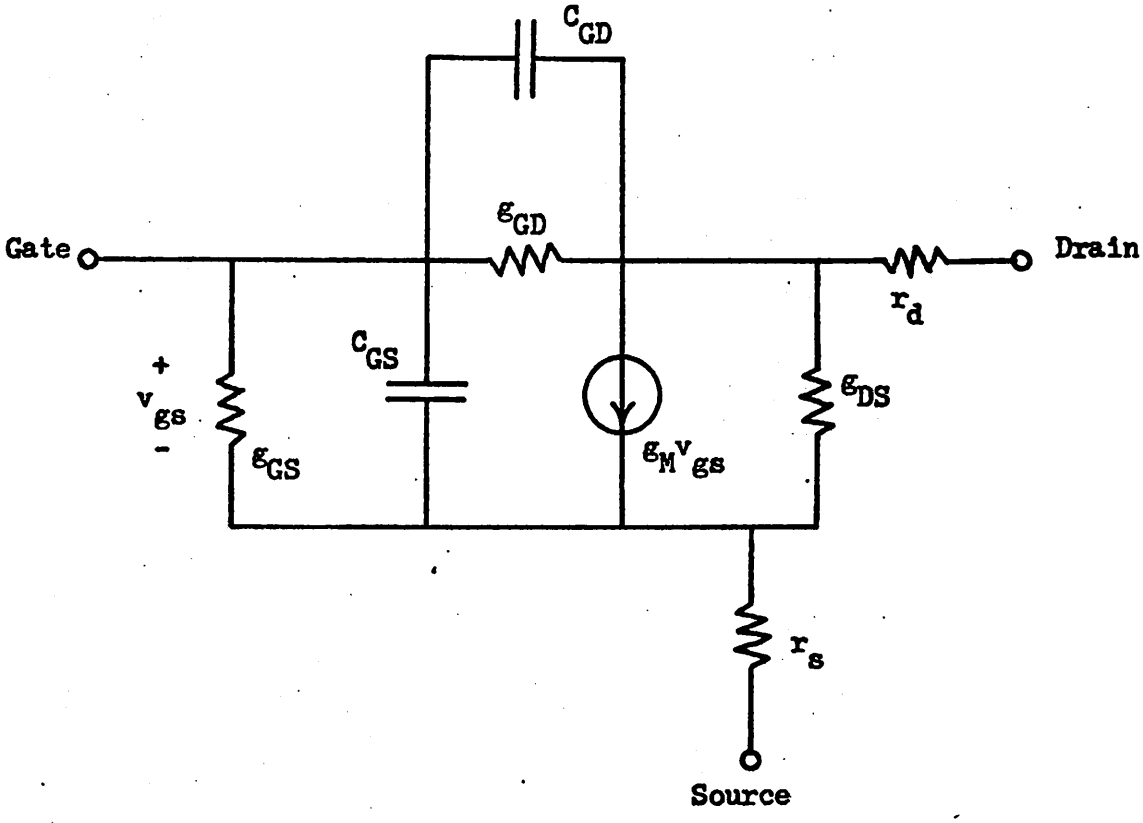


SUBROUTINE ACMOD

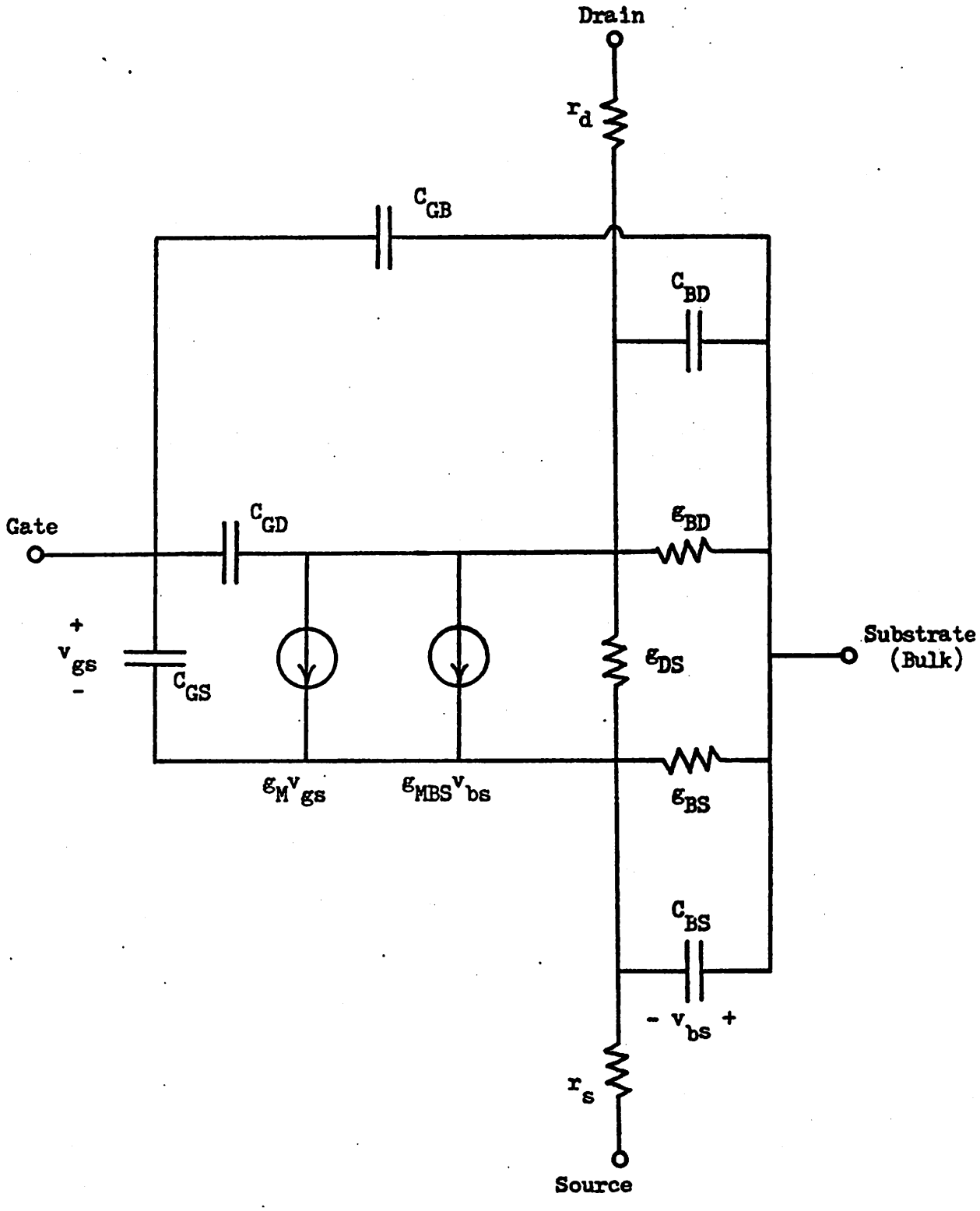
This subroutine computes the small-signal circuit models at the present analysis temperature. First, the small-signal bipolar transistor model parameters and their sensitivities (partial derivatives) with respect to the dc junction voltage are computed [3]. Next, the small-signal model parameters for the junction and MOS field-effect transistors are computed. These small-signal model parameters are computed based on the operating point of each transistor and are stored for later admittance matrix loading. The small-signal models for the three types of transistors are shown on the following pages. These small-signal transistor model parameters are then printed. Next, the values at the present analysis temperature of the resistors, voltage-controlled current sources, capacitors, inductors, and mutual inductors are computed and stored for later admittance matrix loading. Finally, the complex node voltage vector is zeroed.



Small-signal Bipolar Transistor Model

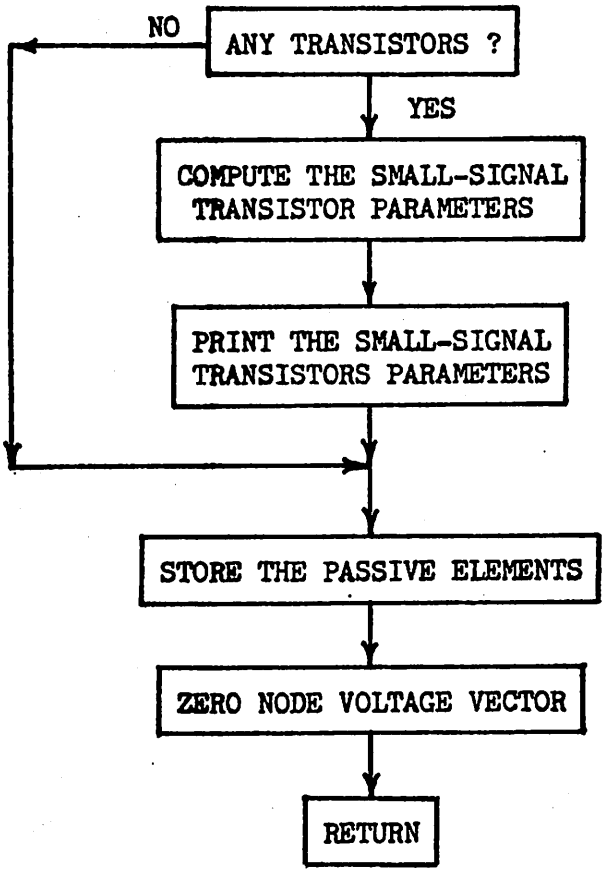


Small-signal Junction Field-effect Transistor Model



Small-signal MOS Field-effect Transistor Model

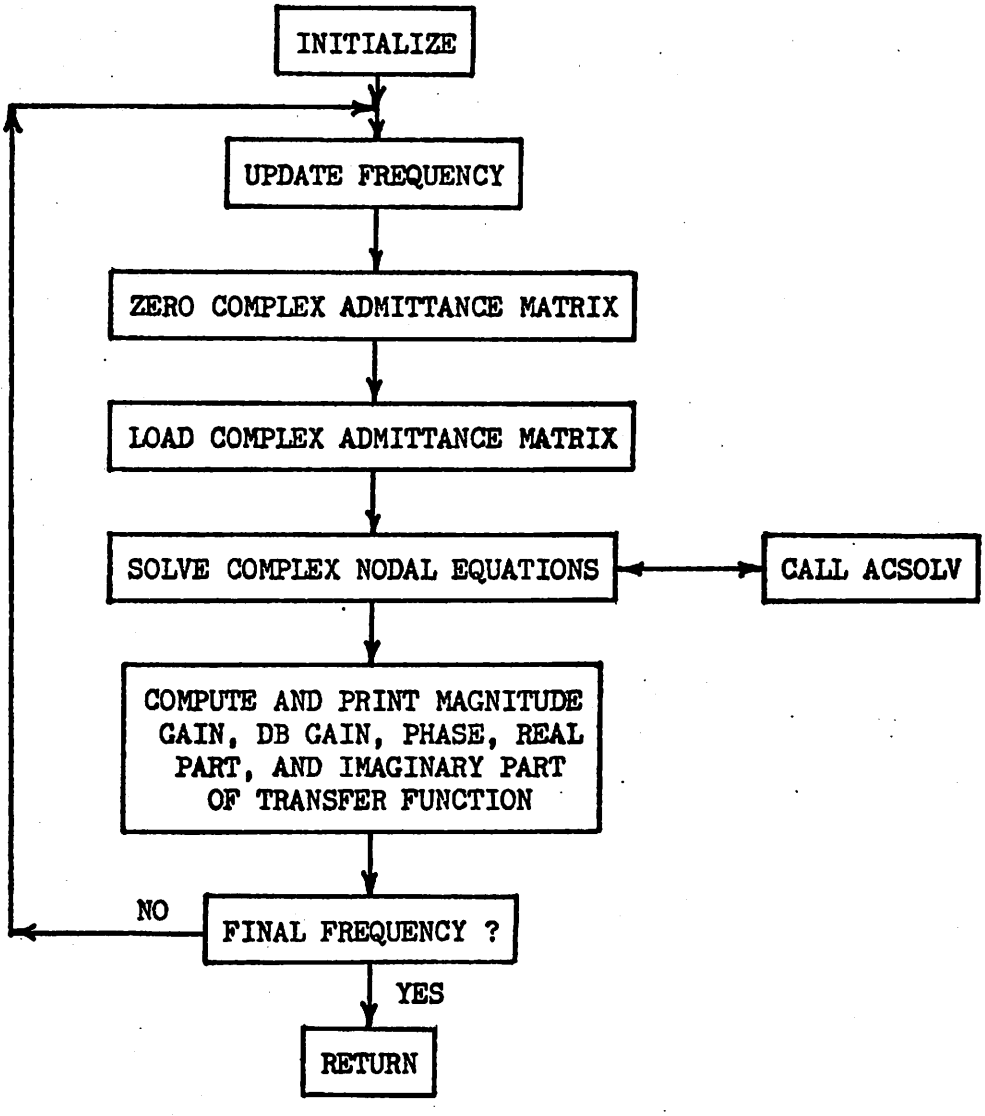
SUBROUTINE ACMOD



SUBROUTINE ACANAL

This subroutine controls the frequency response analysis in which the magnitude, phase, and real and imaginary parts of a specified transfer function is computed. The frequency response is obtained from a direct solution of the complex nodal admittance equations. For each frequency in the analysis, the following steps are performed: the complex admittance matrix is first zeroed and loaded with inductors, capacitors, and resistors; subroutine ACSOLV then solves the complex nodal equations; and finally the magnitude gain, db gain, phase, real part, and imaginary part of the transfer function are computed and printed.

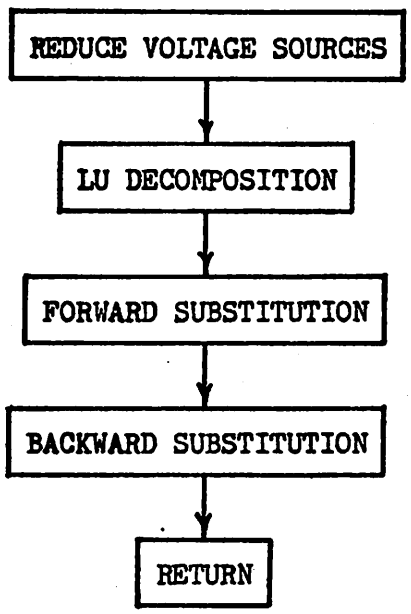
SUBROUTINE ACANAL



SUBROUTINE ACSOLV

This subroutine solve the sparse system of complex nodal admittance equations. The method used is identical to that of subroutine DCSOLV except that the admittance matrix and node voltage vector are complex. The complex nodal equations are solved in four steps: voltage source reduction, LU decomposition, forward substitution, and backward substitution.

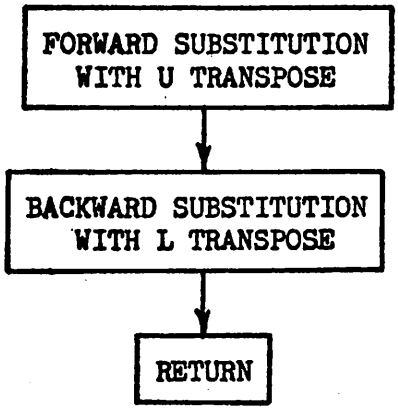
SUBROUTINE ACSOLV



SUBROUTINE ACADJ

This subroutine solves for the set of complex adjoint node voltages in two steps. First, a forward substitution with the U transponse is performed, and second, a backward substitution with the L transpose is performed.

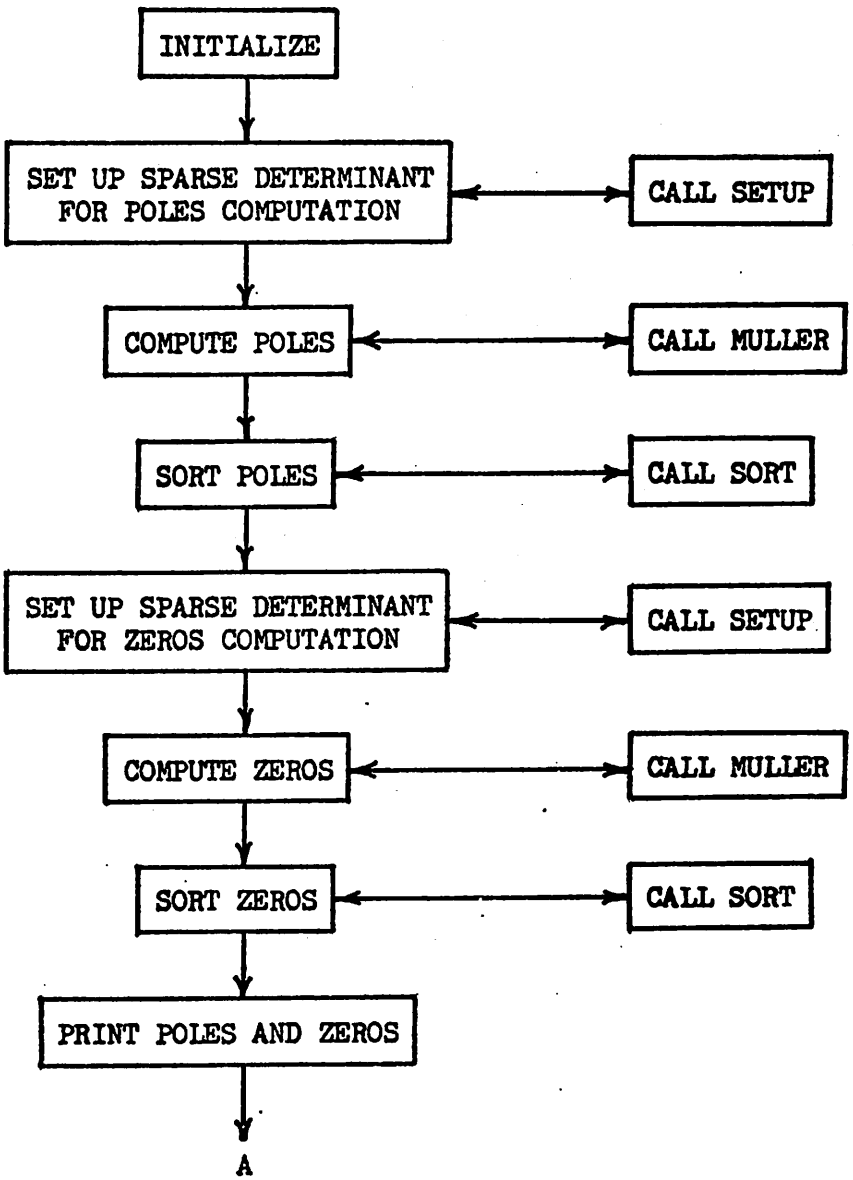
SUBROUTINE ACADJ

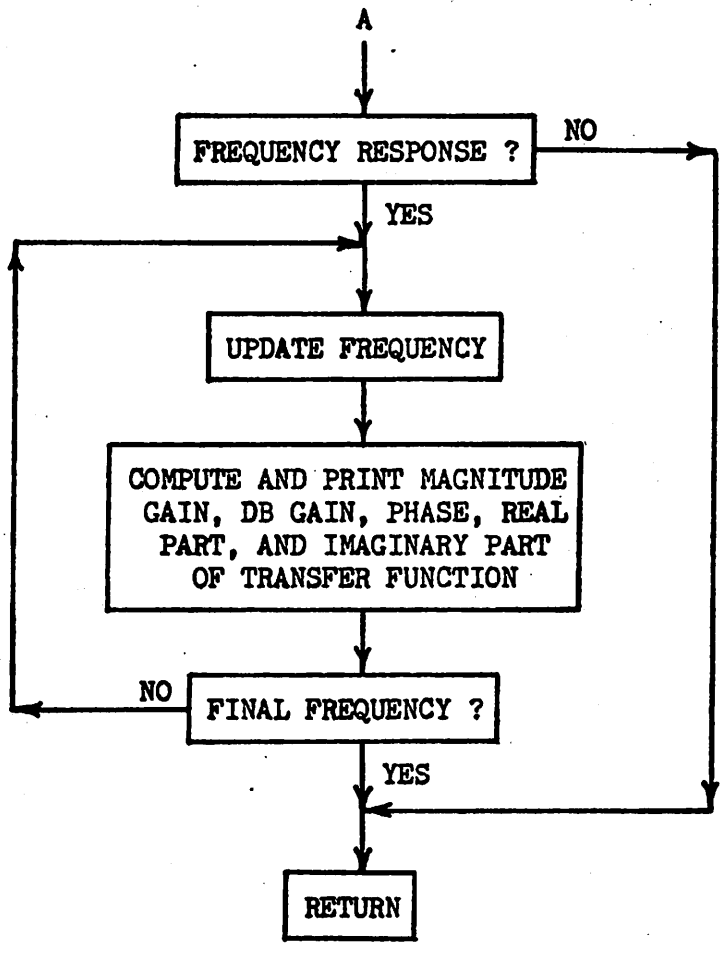


SUBROUTINE PZANAL

This subroutine controls the calculation of the poles and zeros of a specified transfer function and if requested, computes a frequency response from a pole-zero derived transfer function. The poles are first computed. Subroutine SETUP sets up the sparse determinant, subroutine MULLER computes the poles, and subroutine SORT rearranges the stored poles in an ascending order in terms of the magnitudes of the real parts. The zeros are then computed in a similar manner by calling subroutines SETUP, MULLER, and SORT. Next the poles and zeros are printed. If a frequency response is also requested, the following two steps are performed for each frequency: the specified transfer function is computed from the poles and zeros; and then the magnitude gain, db gain, phase, real part, and imaginary part of the transfer function are computed and printed.

SUBROUTINE PZANAL



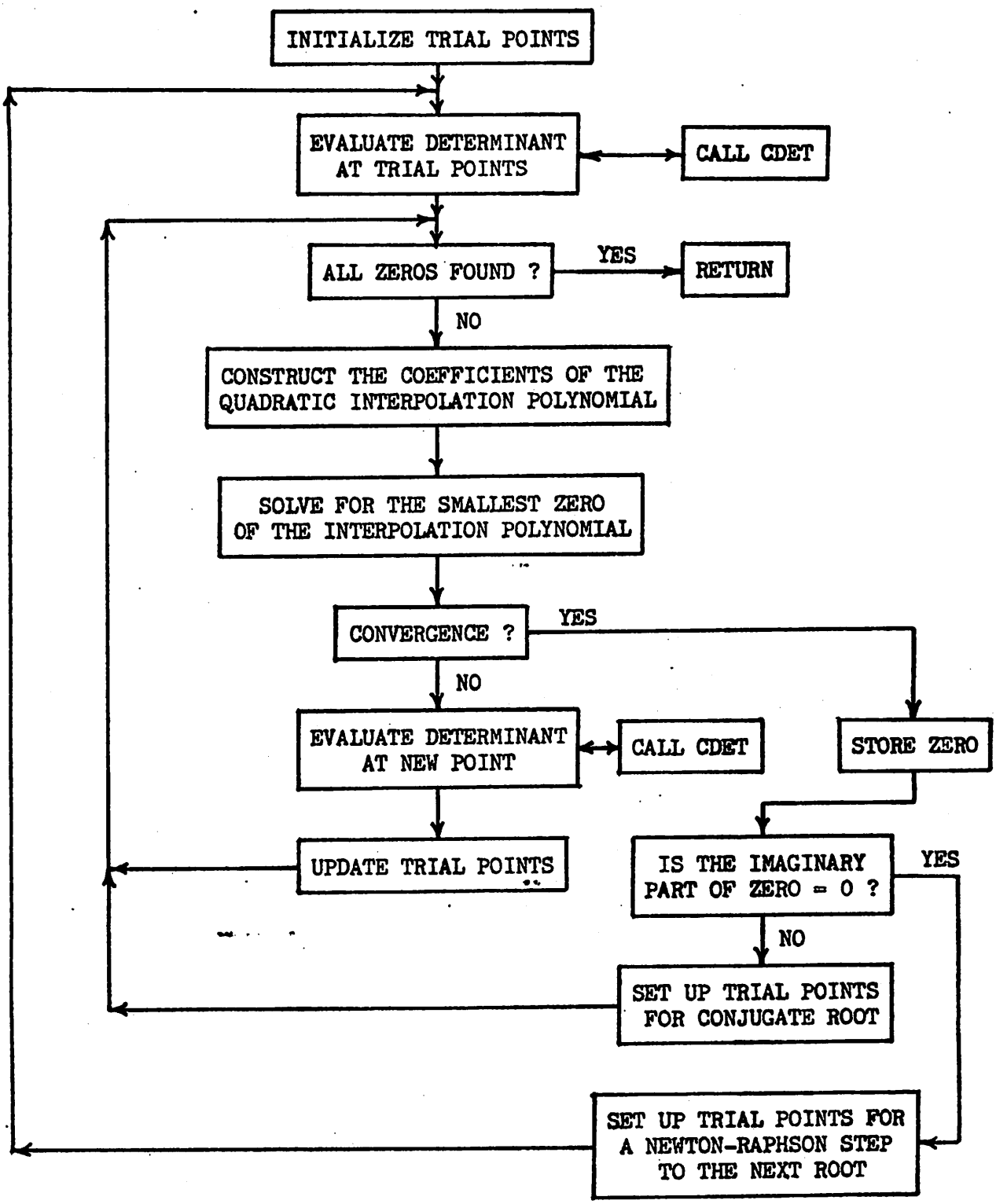

A
FREQUENCY RESPONSE ?
NO
YES
UPDATE FREQUENCY
COMPUTE AND PRINT MAGNITUDE GAIN, DB GAIN, PHASE, REAL PART, AND IMAGINARY PART OF TRANSFER FUNCTION
NO
FINAL FREQUENCY ?
YES
RETURN

SUBROUTINE MULLER

This subroutine solves for the zeros of a complex determinant using Muller's method [9]. First, three initial trial points are set up. The three initial points are presently chosen to be 1.0×10^{6}, -1.0×10^{9}, and -1.0×10^{4}. Next, subroutine CDET evaluates the complex determinant at each of these three trial points. Throughout MULLER, determinant values are scaled in terms of their integer logarithm to the base two. A quadratic interpolation polynomial is constructed through the determinant values of the three trial points. This polynomial is then solved for two zeros. The smaller zero replaces the oldest of the three previous trial points and the above process is repeated until the magnitudes of two successive trial points agree to within 5.0×10^{-7}. This smaller zero is then checked for a negligible real or imaginary part. The real part is considered negligible if its magnitude is six orders of magnitude smaller than the magnitude of the imaginary part, and likewise the imaginary part is negligible if it is six orders of magnitude smaller than the real part. If a negligible part is found, it is set to zero. The zero is then stored and its imaginary part is checked. If non-zero, a conjugate zero exists and the entire process is repeated using the conjugates of the three trial points. If zero, the two oldest trial points generate a third trial point by Newton-Raphson approximation and the entire process is repeated. All zeros of the complex determinant are

assumed found when the magnitudes of three successive determinant values agree to within 5.0×10^{-7}.

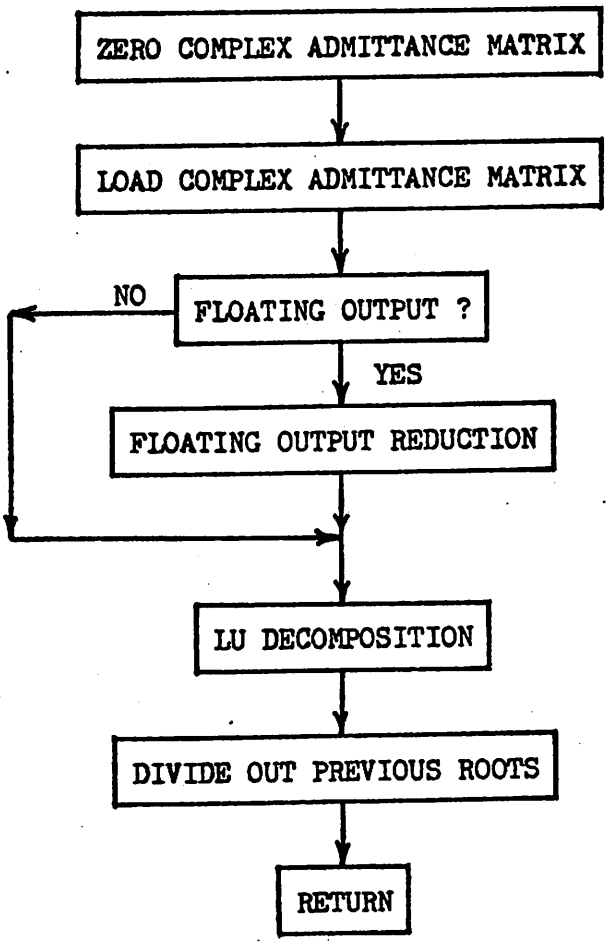
SUBROUTINE MULLER



SUBROUTINE CDET

This subroutine evaluates a complex determinant using sparse matrix techniques. The complex admittance matrix is first zeroed and then loaded with inductors, capacitors, and resistors. If the output port is not referenced to the datum (ground) node, a floating output reduction is performed. Next, an LU decomposition is performed and a determinant value is obtained. If any previously calculated zeros of the determinant exist, the determinant value is divided by the difference between each previous zero and the trial point.

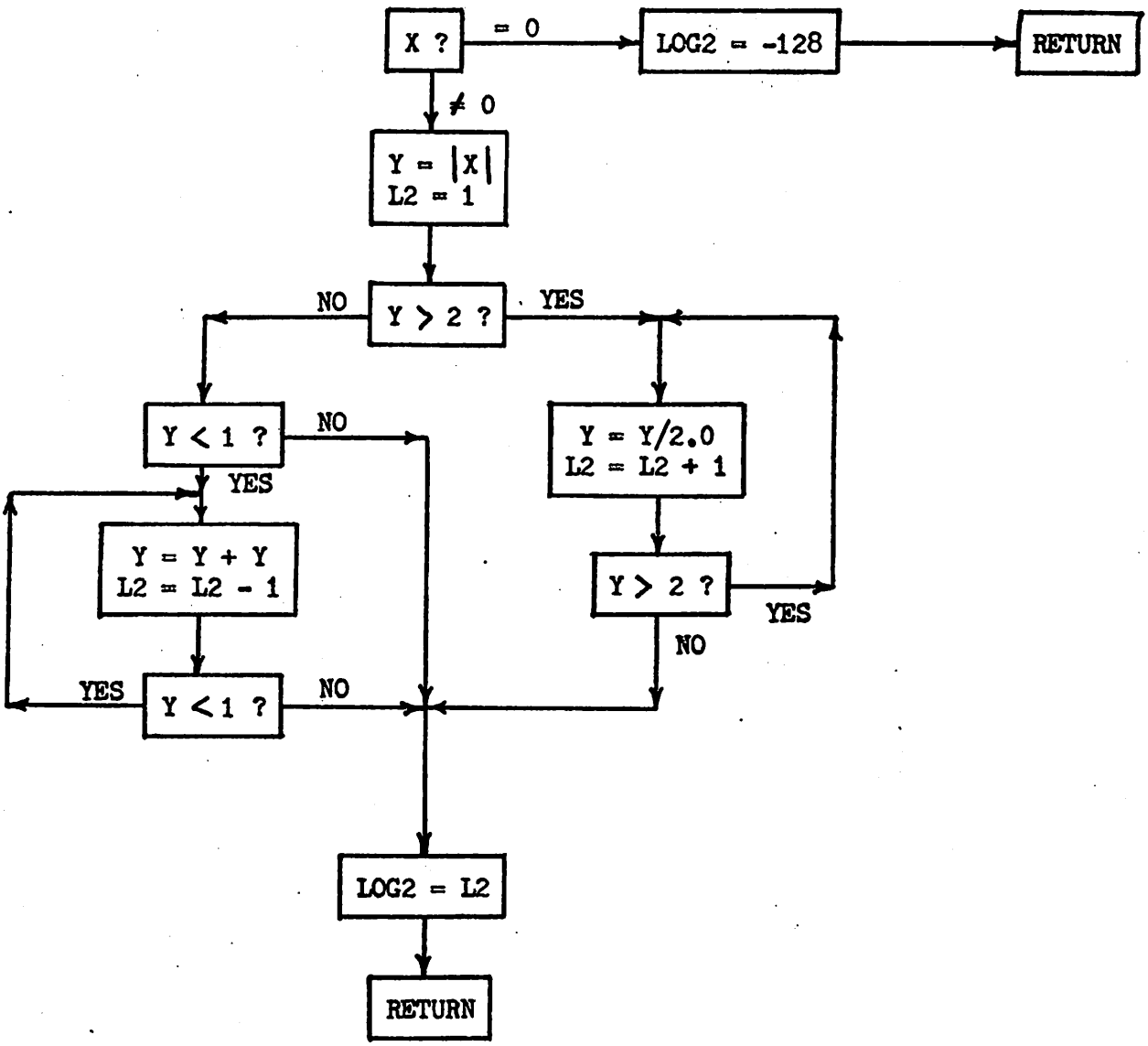
SUBROUTINE CDET



SUBROUTINE LOG2

This function subroutine computes the integer logarithm to the base two of the passed argument. If the argument is zero a value of -128 is returned. The process is initialized by setting the argument to its absolute value and setting the integer logarithm to 1. If the argument is less than 1, it is doubled and the integer logarithm is decreased by 1. This is repeated until the argument is greater than or equal to 1. The present value of the integer logarithm is returned. If the argument is between 1 and two, the initial integer logarithm value of 1 is returned. If the argument is greater than 2, it is halved and the integer logarithm is increased by 1. This is repeated until the argument is less than or equal to 2. The present value of the integer logarithm is then returned.

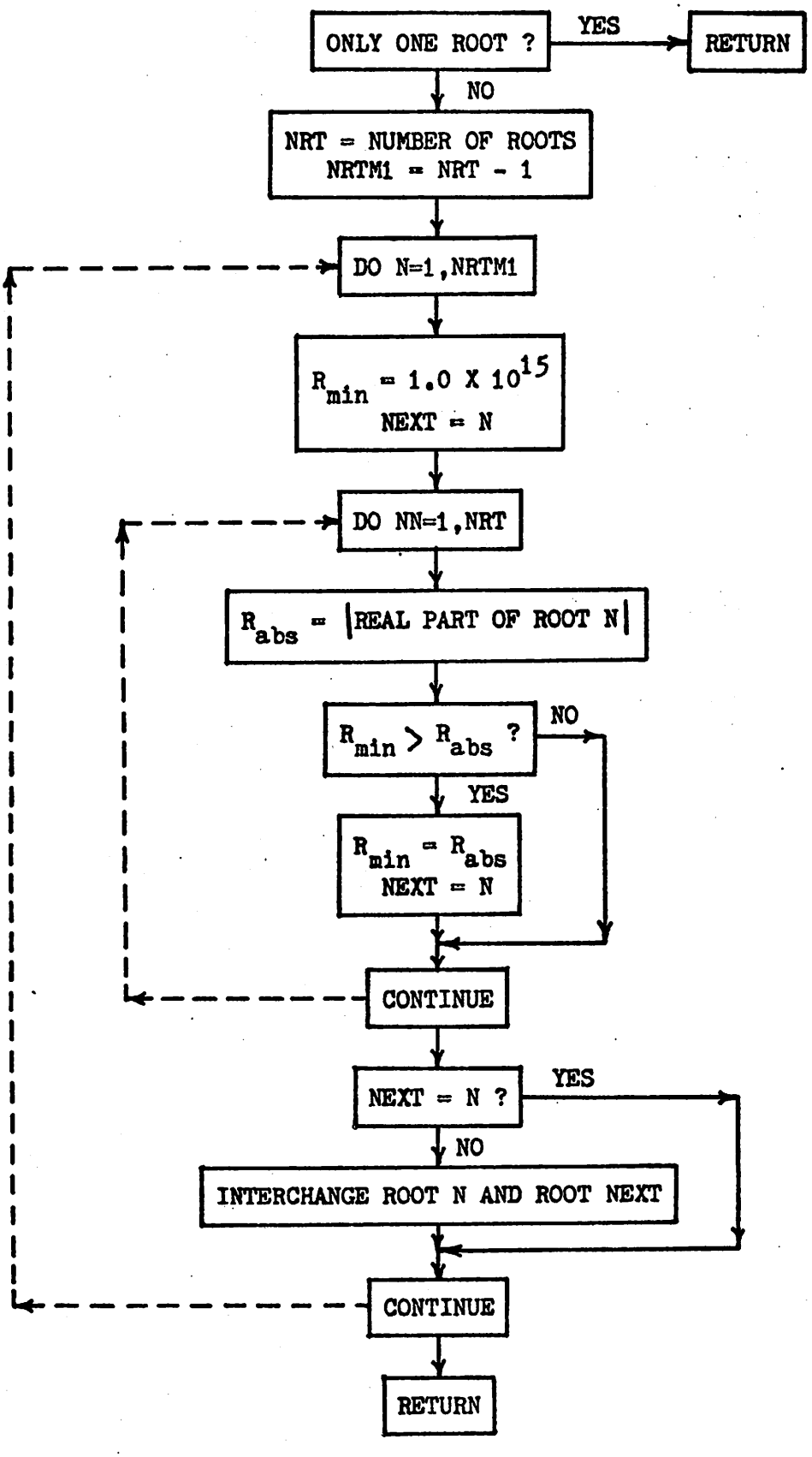
SUBROUTINE LOG2



SUBROUTINE SORT

This subroutine rearranges a set of stored complex roots so that the magnitudes of the real parts are in an ascending order. The root with the smallest real part magnitude is first found. This root becomes first in order. Of the remaining roots, the root with the smallest real part magnitude is again found. This root becomes second in order. The process continues until all the roots have been rearranged.

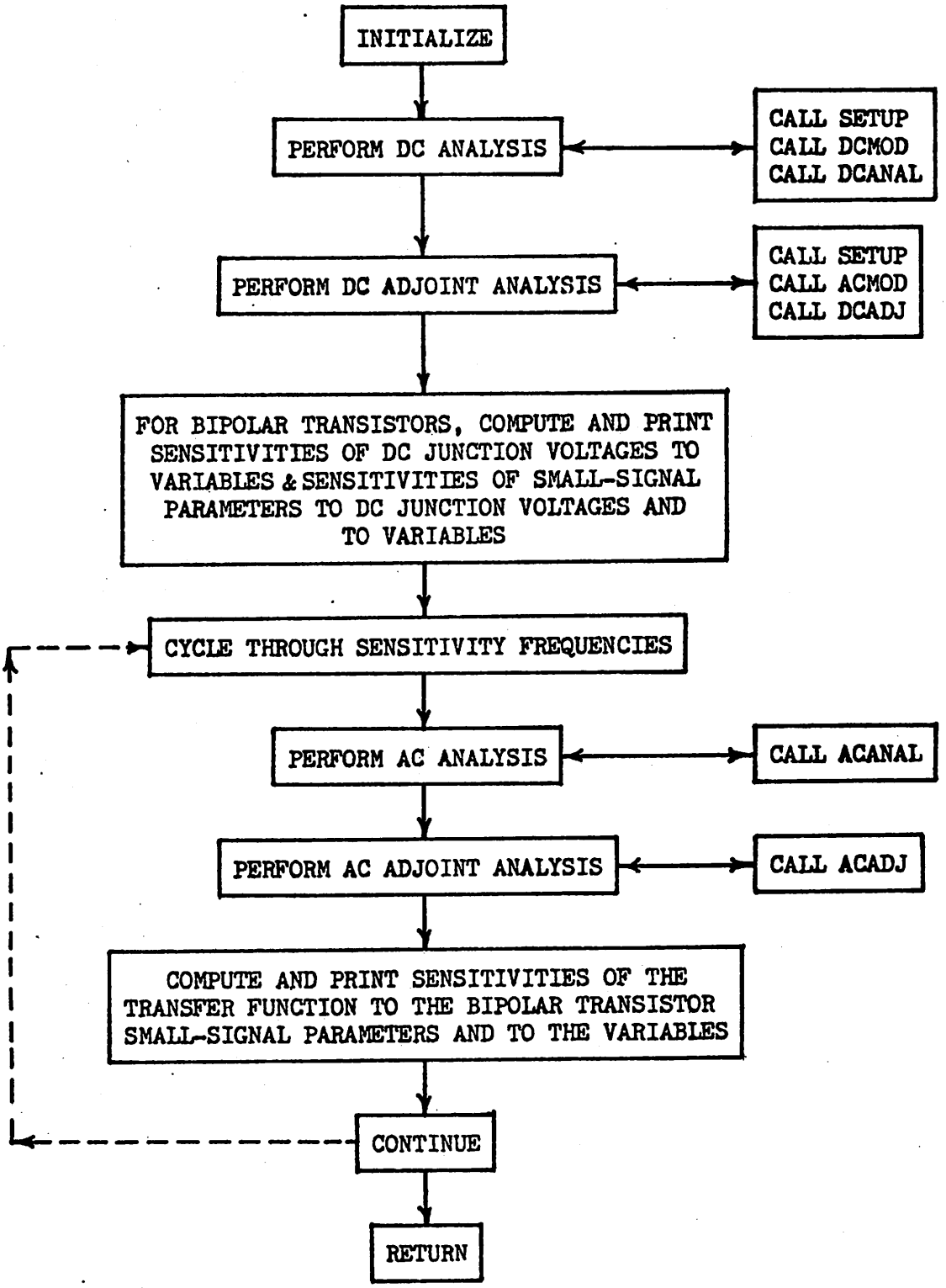
SUBROUTINE SORT



SUBROUTINE SENSE

This subroutine controls the sensitivity analysis in which sensitivities (partial derivatives) with respect to selected passive elements called variables are computed by the adjoint method [8]. A nonlinear dc analysis is first performed with calls to subroutines SETUP, DCMOD, and DCANAL. Then a dc adjoint analysis is performed by calling subroutines SETUP, ACMOD, and DCADJ. Next the following three types of sensitivities are computed and printed for the bipolar transistors: sensitivities of dc junction voltages to the variables, sensitivities of small-signal parameters to the dc junction voltages, and sensitivities of small-signal parameters to the variables. Finally for each of the up to five specified sensitivity frequencies, the following steps are conducted: subroutine ACANAL performs an ac analysis, subroutine ACADJ computes the complex adjoint node voltages, and the sensitivities of the transfer function to the bipolar transistor small-signal parameters and to the variables are computed and printed.

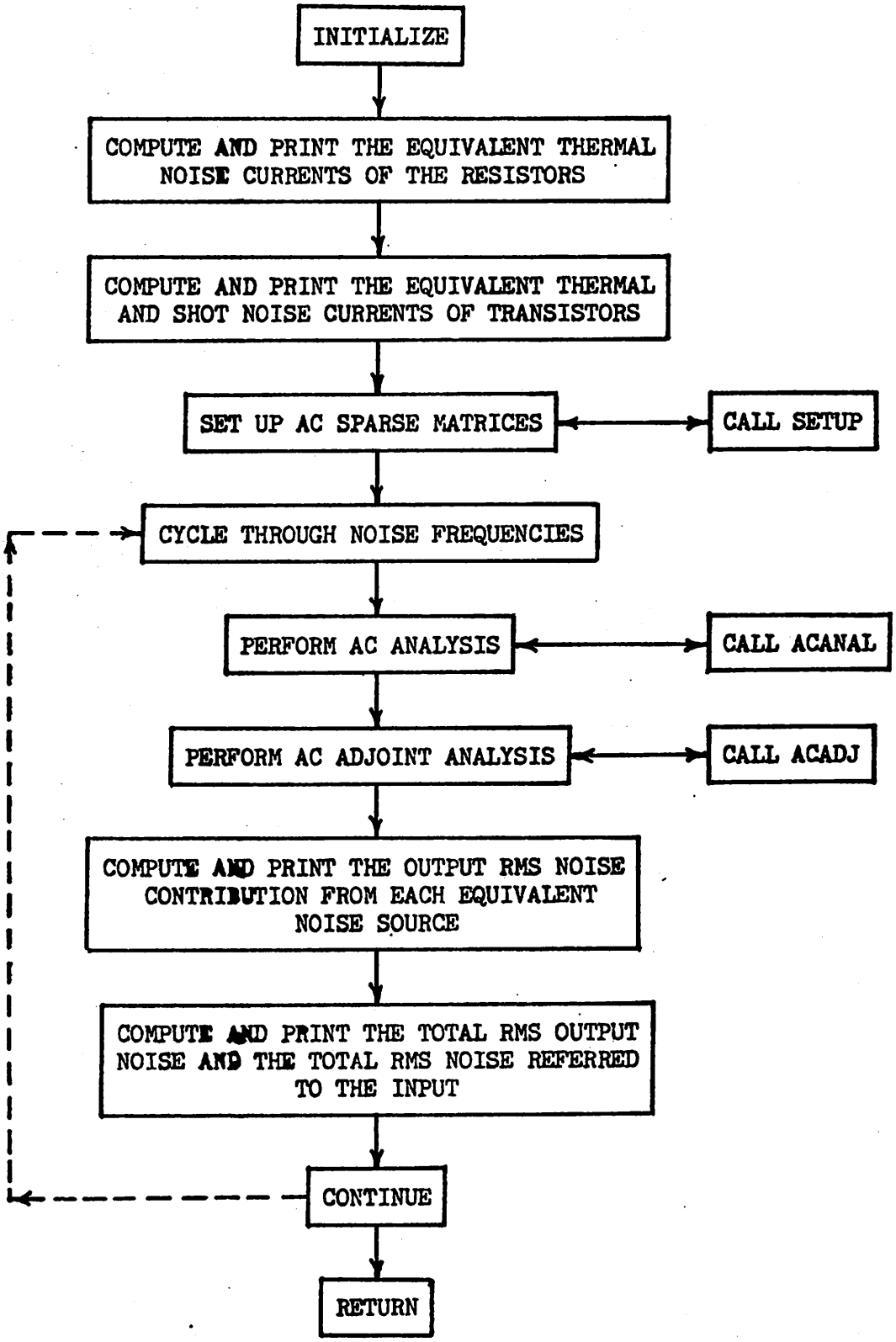
SUBROUTINE SENSE



SUBROUTINE NOISE

This subroutine uses the adjoint method and computes the noise at the output port from each thermal and shot noise source in the circuit [10]. First, the equivalent noise current sources are computed and printed. These noise sources are of two types: thermal noise sources due to the circuit resistors, bipolar transistor ohmic base and collector resistances, and field-effect transistor ohmic drain and source resistances; and shot noise sources due to the dc base and collector currents of bipolar transistors and the dc drain currents of field-effect transistors. Then for each of the up to five specified noise frequencies, the following steps are conducted: subroutine ACANAL performs an ac analysis; subroutine ACADJ computes the complex adjoint node voltages; and the rms output noise contribution from each noise source, the total rms output noise, and the total rms noise referred to the input are computed and printed.

SUBROUTINE NOISE



SUBROUTINE CLOCK

This subroutine is written in Control Data COMPASS assembly language and obtains the time and date of job execution. Due to its special nature, no description or flowchart is included for this subroutine.

COMMON BLOCK VARIABLES

This section lists and describes the common block variables.

UNLABELLED COMMON BLOCK

NPOS(2000)	-	storage for the pointers to the terms of the sparse Y-matrix and current vector that are modified during a sparse matrix solution

COMMON/NAM/

TITLE(20)	-	"Title card" image

COMMON/RES/

KR	-	the total number of resistors
RNAM(40)	-	names of the resistors
NR(40,2)	-	nodes of the resistors
R(40,3)	-	nominal resistances and first-order and second-order temperature coefficients, respectively, of the resistors

COMMON/GM/

KG	-	the total number of voltage-controlled current sources
GNAM(20)	-	names of the voltage-controlled current sources

NG(20,4) - positive and negative current source nodes and positive and negative controlling nodes, respectively, of the voltage-controlled current sources

G(20,3) - nominal transconductances and first-order and second-order temperature coefficients, respectively, of the voltage-controlled current sources

COMMON/CAP/

KC - the total number of capacitors

CNAM(20) - names of the capacitors

NC(20,2) - nodes of the capacitors

C(20,2) - nominal capacitances and first-order and second-order temperature coefficients, respectively, of the capacitors

COMMON/IND/

KL - the total number of the inductors

ALNAM(20) - names of the inductors

NL(20,2) - nodes of the inductors

AL(20,3) - nominal inductances and first-order and second-order temperature coefficients, respectively, of the inductors

COMMON/MUL/

KML - the total number of mutual inductors

AMLNAM(10) - names of the mutual inductors

NML(10,4) - primary winding and secondary winding nodes, respectively, of the mutual inductors

AML(10,5) - nominal primary self-inductances, nominal mutual inductances between the primary and secondary windings, nominal secondary self-inductances, and first-order and second-order temperature coefficients, respectively, of the mutual inductors

COMMON/CUR/

KCS - the total number of current sources

CSNAM(10) - names of the current sources

NCS(10,2) - positive and negative nodes, respectively, of the current sources

CS(10) - values of the current sources

COMMON/VOL/

KVS - the total number of voltage sources

VSNAM(10) - names of the voltage sources

NVS(10,2) - positive and negative nodes, respectively, of the voltage sources

VS(10) - values of the voltage sources

COMMON/TRN/

KQ	-	the total number of bipolar and field-effect transistors
QNAM(30)	-	names of the transistors
NQ(30,6)	-	external collector, external base, emitter, internal collector, and internal base nodes, respectively, for the bipolar transistors or external drain, gate, external source, internal drain, internal source, and substrate (MOSFET's only) nodes, respectively, for the field-effect transistors
QMOD(30)	-	names of the referenced transistor models
QARF(30)	-	area factors in relation to the referenced transistor models
QCUR(30)	-	initial collector currents for the bipolar transistors
QVOL(30)	-	initial collector-emitter voltages for the bipolar transistors
QTEMP(30)	-	temperatures at which the transistors are to be maintained
NQTYP(30)	-	indicators denoting the types of the transistors (1 for bipolar transistors, 2 for junction field-effect transistors, or 3 for MOS field-effect transistors)
IBJT	-	the total number of bipolar transistors

IJFET - the total number of junction field-effect transistors

IMFET - the total number of MOS field-effect transistors

COMMON/VAR/

KV - the total number of variable elements

VNAM(20) - names of the variable elements

VSCAL(20) - values of the variable elements

NPE(20) - pointers to the variable elements

NTV(20) - indicators denoting the type of variable element (1 for resistors, 2 for voltage-controlled current sources, 3 for capacitors, or 4 for inductors)

COMMON/BJT/

NBMOD(30) - names of the referenced bipolar transistor models

VBE(30) - base-emitter voltages of the bipolar transistors

VBC(30) - base-collector voltages of the bipolar transistors

CC(30) - collector currents of the bipolar transistors

CB(30) - base currents of the bipolar transistors

COMMON/FET/

NFMOD(30) - names of the referenced field-effect transistor models

ITC - indicator denoting the type of input source (0 for a voltage source or 1 for a current source)

TCVAL1 - initial value of the input source

TCVAL2 - final value of the input source

TCDEL - increment of the input source

TCNAMO - name of the output voltage

NTC1 - positive node of the output voltage

NTC2 - negative node of the output voltage

KNTC - pointer to the input source

IVS - pointer to the input voltage source in the sparse matrix

COMMON/CNTRL/

KDC - dc analysis indicator (0 for no dc analysis or 1 for a dc analysis)

KAC - frequency response only indicator (0 for no frequency response or 1 for a frequency response)

KPZ - pole-zero analysis indicator (0 for no pole-zero analysis or 1 for a pole-zero analysis)

KALTR - altered analysis indicator (0 for no altered analysis or 1 for an altered analysis)

COMMON/LIST/

KTEMP1 - indicator to denote which temperature value is presently being used

KTEMP2 - the total number of temperature values

TNOM - the nominal temperature

TEMP(5) - the temperature values at which the circuit is to be analyzed

KVARS1 - indicator to denote which variable source value is presently being used

KVARS2 - the total number of variable source values

VARNAM - the name of the variable source

VARVAL(20) - the variable source values

KNOIS1 - indicator to denote which noise analysis frequency is presently being used

KNOIS2 - the total number of noise analysis frequencies

FNOIS(5) - the noise analysis frequencies

KSENS1 - indicator to denote which sensitivity analysis frequency is presently being used

KSENS2 - the total number of sensitivity analysis frequencies

FSENS(5) - the sensitivity analysis frequencies

COMMON/TRFN/

NOUT - indicator to denote the type of small-signal output (1 for voltage output or 2 for current output)

NOP - the positive output node

NOM	-	the negative output node
NINP	-	indicator to denote the type of small-signal input (1 for voltage input or 2 for current input)
NIP	-	the positive input node
NIM	-	the negative input node
PLIM	-	the upper frequency limit for poles
ZLIM	-	the upper frequency limit for zeros
KFREQ	-	indicator to denote the type of frequency variation (1 for no frequency response, 2 for logarithmic variation, or 3 for linear variation)
GOUT	-	the conductance across the output nodes
DIV	-	the number of points per decade for a logarithmic frequency variation, or the number of frequency points for a linear frequency variation
FMIN	-	the initial frequency
FMAX	-	the final frequency
GSCAL	-	the small-signal analysis scale factor for conductances
CSCAL	-	the small-signal analysis scale factor for capacitances
ALSCAL	-	the small-signal analysis scale factor for inductances
FSCAL	-	the small-signal analysis scale factor for frequencies

COMMON/CRKT

VALU(500)	-	temporary storage for the values of all elements (including transistor model elements)
KODE(500)	-	indicators denoting each element type
LOC1(500), LOC2(500), LOC3(500), LOC4(500)	-	temporary storage for the nodes of all elements
NELT	-	the total number of elements

COMMON/NODE/

VDC(101)	-	dc node voltages
VAC(101)	-	complex ac node voltages
PSIDC(101)	-	dc adjoint node voltages
PSIAC(101)	-	complex ac adjoint node voltages
NINC(101)	-	number of incident branches to each circuit node
NORD(101)	-	the user specified nodes
NLOC(101)	-	the optimally ordered nodes
NMAX	-	the maximum user specified node number
NDMR	-	maximum number of rows in the indicator matrix
NDMC	-	maximum number of columns in the indicator matrix

COMMON/SPARSE/

NMOD	-	maximum number of user specified nodes

NUT - number of elements in the upper-triangular matrix

NLT - number of elements in the lower-triangular matrix

NTOT - total number of elements in the singly dimensioned admittance matrix and current vector

NADJ - starting pointer for ac adjoint analysis

NFO - number of extra elements due to floating output

NVC(10) - number of non-zero entries in the rows with voltage sources

NUR(101) - number of non-zero entries in each row of the upper-triangular matrix

NLC(101) - number of non-zero entries in each column of the lower-triangular matrix

NFS(101) - number of entries per column used in forward substitution

NBS(101) - number entries per row used in backward substitution

COMMON/FILE/

CARD(80) - temporary storage for eighty column data card

COL(80) - error pointers for an eighty column data card

FNUM - floating point free-format value

INUM - integer free-format value or keyword code

IPT - data card column that is being processed

ISTRT - starting column of free-format field that is being processed

ISET - indicator to denote continuation card (0 for non-continuation cards and 1 for continuation cards)

NERR - number of errors on a card

KERR(80) - indicators denoting the types of card errors

IPARAM - indicator to denote the type of card for keyword interpretation (1 for bipolar transistor model cards, 2 for PRINT cards, and 3 for field-effect transistor model cards)

COMMON/BJTMOD/

KBMOD - the total number of bipolar trnasistor models

BNAM(10) - names of the bipolar transistor models

BMOD(40,10) - bipolar transistor model parameters (both user-defined and computed):

1. type (+1.0 for NPN or -1.0 for PNP)
2. β_F : β_{FMAX}
3. I_{CMAX}
4. β_{FLOW}

5. I_{CLOW}
6. V_{CE}
7. T_{C1}
8. T_{C2}
9. β_R
10. r_O : r_O
11. I_C
12. V_{BE}
13. V_{CE}
14. r_B : r_B
15. T_{C1}
16. T_{C2}
17. r_C : r_C
18. T_{C1}
19. T_{C2}
20. f_T : f_T
21. I_C
22. V_{CE}
23. L_E/W_B
24. I_{CO}
25. t_{SAT}
26. C_{je} : C_{je}
27. V_{BE}
28. ϕ_e
29. n_e
30. C_{jc} : C_{jc}

32. V_{BC}
33. ϕ_C
34. ratio
35. C_{SUB}
36. temperature
37. I_S
38. τ_F
39. V_A

BCC(10,3) - three coefficients that model $_F$ vs. I_C

CSO(19) - reverse saturation currents at their defined temperatures

ETA(10) - basewidth modulation factors at their defined temperatures

CJO(10,2) - zero bias values of C_{je} and C_{jc}, respectively

TAUO(10) - forward transit times at their defined temperatures

IV. CLOSING NOTES

SLIC has undergone a number of changes which provide for more versatile use. However, there are two areas where improvement could be made. First, a considerable amount of core storage could be reduced by eliminating the use of a square indicator matrix in the sparse matrix set up. With the 100 node capability, a 101 by 101 square matrix or approximately 10,000 words of core storage is needed. Assuming that circuits will contain no more than 10 incident branches to each node, then only 1,000 (100 nodes times 10 off-diagonal terms) words of core storage will be needed. The time required to set up the sparse matrix would also be reduced since the sparse square indicator matrix would not have to be searched for non-zero terms. Changes to subroutines SETUP, NCODE, OPTORD, and NUMSET would be required. The second area concerns the way transistor data is stored. Presently, all types (bipolar, junction field-effect, and MOS field-effect) of transistor data are stored together in one storage area. Since each transistor type has a different model, a search is required to find the transistors of each type. This searching could easily be eliminated by creating a separate storage area for each transistor type.

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