ANALOG-TO-DIGITAL CONVERSION IN MOS INTEGRATED CIRCUITS

by

R. E. Suarez-Gärtner

Memorandum No. ERL-M494

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ELECTRONICS RESEARCH LABORATORY

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Dept. of Electrical Engineering and Computer Sciences

Chairman of Committee

ABSTRACT

Integrated circuit technology has not had as dramatic an impact on the cost of the analog-to-digital conversion function as in other types of analog and digital system building blocks. The objective of this work has been to determine the fundamental factors limiting the performance of monolithic A/D converters, and to devise new techniques which overcome these obstacles.

A novel charge-redistribution technique for analog-to-digital conversion has been developed. The conversion approach requires a minimum of two matched grounded capacitors and MOS transistor switches to perform a serial digital-to-analog conversion. Increased conversion speeds are attainable, however, through the use of additional capacitors of equal weight or with binary-weighted capacitors. The serial digital-to-analog converter (DAC) can be integrated with a voltage comparator, data storage registers and sequencing logic to form a single-chip successive approximation analog-to-digital converter (ADC).

The principal sources of error in a monolithic ADC have been systematically investigated. The primary accuracy limitations for a charge-redistribution DAC were determined to be component mismatches and feedthrough error voltages. Capacitor mismatches determine the

size of the charge-sharing capacitors. The capacitance value can be established by means of a simple statistical model for photolithographically-induced uncertainties in edge definition of component geometries. Feedthrough error voltages arise from the nonlinear capacitance of the MOS transistor switches. This source of error constraints the size of the switch devices in relation to the charge-sharing capacitors and thus determines conversion speed. The speed-accuracy tradeoff can be improved with reduced channel length of the MOS devices, but short-channel effects eventually limit this design degree of freedom. For the successive approximation ADC the input offset voltage of the voltage comparator is an additional accuracy limitation. Offset voltages can be corrected, however, with cancellation techniques which are compatible with MOS fabrication processes.

A monolithic DAC was built to verify experimentally the conversion approach. The two-capacitor aluminum gate circuit exhibits an accuracy of 8-bits and digital-to-analog conversion time of 13.5 μs. The die size is 48×52 mil^2. On the basis of these results it is expected that an 8-bit ADC can be constructed on a 70×70 mil^2 chip with an analog-to-digital conversion time of 100 μs. Extrapolated specifications for a 10-bit ADC include a 100×80 mil^2 chip area and 300 μs conversion time.

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A novel charge-redistribution technique for analog-to-digital conversion has been developed. The conversion approach requires a minimum of two matched grounded capacitors and MOS transistor switches to perform a serial digital-to-analog conversion. Increased conversion speeds are attainable, however, through the use of additional capacitors of equal weight or with binary-weighted capacitors. The serial digital-to-analog converter (DAC) can be integrated with a voltage comparator, data storage registers and sequencing logic to form a single-chip successive approximation analog-to-digital converter (ADC).

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CHAPTER I

INTRODUCTION

Widespread application of techniques for digital processing of analog signals has been hindered by the unavailability of inexpensive functional blocks for analog/digital conversion. Traditional approaches to analog-to-digital conversion have required the simultaneous implementation of high performance analog circuits, such as operational amplifiers, and of digital circuitry for counting, control and data storage. Analog circuit functions have thus far been compatible almost exclusively with bipolar junction transistor integrated circuit technologies. Digital circuits, on the other hand, are readily implemented in high density as metal-oxide-semiconductor (MOS) integrated circuits. Consequently, current analog-to-digital converter realizations have tended to be multiple-chip approaches [1] wherein the advantages offered by bipolar and MOS fabrication technologies are separately exploited.

The approach taken in the work reported in this dissertation has been to minimize the number of components with analog specifications required to perform the analog-to-digital conversion function. A novel successive approximation charge redistribution conversion technique has been devised which is realizable on a single low-cost MOS chip. Only two matched grounded capacitors plus MOS transistor switches are needed to implement a serial digital-to-analog converter which is basic to the technique.

In order to formulate fundamental definitions pertaining to analog-to-digital converters, a mathematical model -- the quantizer -- is described in Chapter II. An engineering characterization of

practical converters is then made, and a difference error function is introduced to specify common deviations from the ideal quantizer case.

Through a comparison of existing conversion approaches on the basis of component count and conversion speed, a class of integrable analog-to-digital converters is defined in Chapter III. A study is made in Chapter IV of important considerations for the generation of accurate fractions of a reference signal for successive approximation converters. Resistive and capacitive dividers are compared with respect to sensitivity to component mismatches and voltage and temperature coefficients.

In Chapter V a novel conversion technique based on charge redistribution is presented. A generalization of the technique is made to cover a wide range of potential applications. Chapter VI is an analysis of the most significant sources of error in a practical implementation of the charge redistribution conversion technique.

Finally, the design of an MOS digital-to-analog converter circuit to test the feasibility of the conversion technique is developed in Chapter VII. The chapter concludes with a description of measured data on the performance of the monolithic converter.

CHAPTER II

CHARACTERIZATION OF ANALOG TO DIGITAL CONVERTERS

Analog-to-digital converters (ADC's) transform signals which are continuous variables such as voltage or current into discrete-time, discrete-amplitude signals that can be processed, transmitted and stored more rapidly and accurately. In this chapter ADC's are first described in terms of a mathematical model known as the quantizer. Because the quantizing process introduces distortion to the signal, a mean square distortion measure is defined, and the locations of the quantizing intervals which minimize this distortion measure are established.

In the second half of the chapter an engineering characterization of an analog to digital converter is given. The effect of the most common deviations from the ideal case are described, and the design criterion regarding the maximum allowable error is given for the case of an N-bit ADC.

2.1. Mathematical Considerations

A. Definition of a Quantizer

In order to describe the quantization process mathematically, the analog signal is treated as a random variable X defined on a domain $\mathcal{D}$ and exhibiting a continuous probability density p(x). The domain is divided into a set of disjoint intervals by the specification of breakpoints $x_0,\ldots,x_M$ as indicated in Fig. 2.1. A quantizing interval is defined as the set of values of X which fall between two breakpoints, $I_i = \{x : x_{i-1} \leq x < x_i\}$, and the union of the M intervals expands the domain of X : $I_1 \cup I_2 \cup \ldots \cup I_M = \mathcal{D}$. In this work X

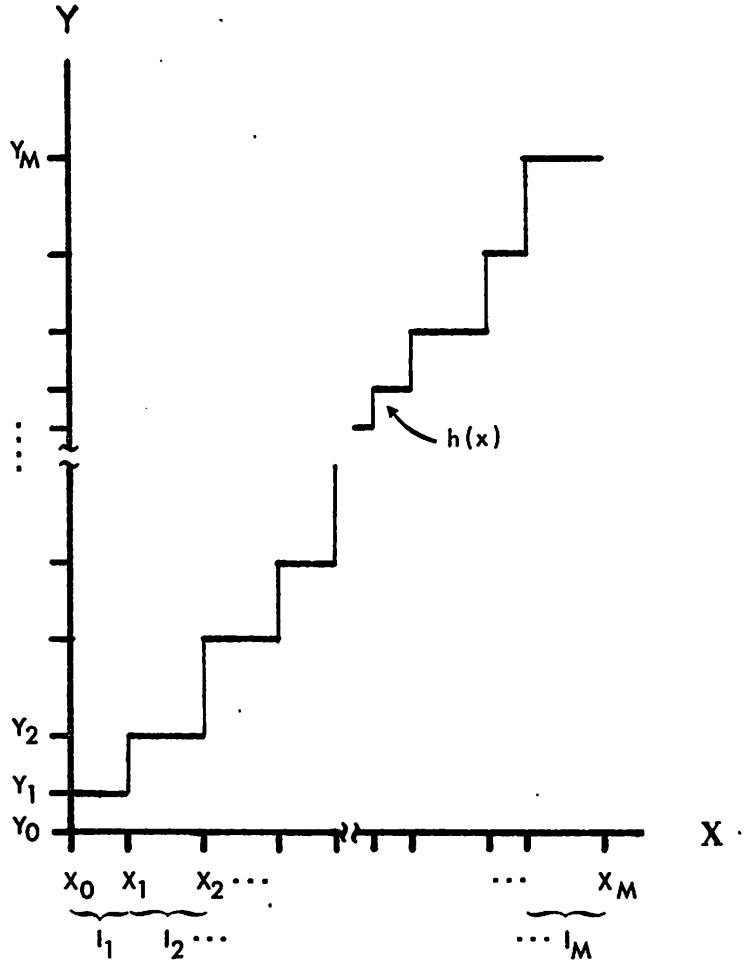


Fig. 2.1. General Quantization Process

is constrained to the interval [0,1].

A quantizer encodes the signal X into a set of disjoint intervals $I_1, \ldots, I_M$ by the assignment of a quantizing level y_i for each x in the interval I_i. This assignment defines a quantizing function $h(x) = y_i$, which is also shown in Fig. 2.1.

B. Quantization Distortion

Because a set of values of X are encoded into a single level y_i, distortion is an inherent characteristic of the quantization process. The resulting quantization error can be described by a mean-square distortion measure,

$$D_2 \equiv E[h(x)-x]^2, \tag{2.1}$$

where $E[\cdot]$ denotes the expectation or average value.

The relationship between the quantizing levels y_i and the breakpoints x_i which minimizes D_2 is found by rewriting (2.1):

$$D_2 = E[(y_i-x)\,|\,x \in I_i]^2. \tag{2.2}$$

Setting $\frac{dD_2}{dy_i} = 0$, the optimum value for y_i is obtained [2]:

$$y_i = E[x|x \in I_i] = \frac{\int_{x_{i-1}}^{x_i} x\,p(x)dx}{\int_{x_{i-1}}^{x_i} p(x)dx} \quad . \tag{2.3}$$

If the probability density is sufficiently smooth to be considered piecewise constant, i.e., $p(x|x \in I_i) = c_i$, then,

$$y_i = \frac{1}{2}(x_{i-1}+x_i). \tag{2.4}$$

Practical quantizers typically have uniformly spaced intervals for ease in implementation.* For a uniform quantizer $\Delta \equiv x_i - x_{i-1}$, and

$$y_i = x_i - \Delta/2. \tag{2.5}$$

The quantity $\pm \Delta/2$ is called the resolution of the quantizer and is related to D_2 by

$$\sqrt{D_2} = \pm \frac{1}{\sqrt{3}}\left(\frac{\Delta}{2}\right). \tag{2.6}$$

It is seen from (2.5) that a least-squares fit of the quantizing function h(x) about the reference line g(x) = x minimizes the mean square distortion measure. Figure 2.2 shows the relationship between h(x) and g(x).

2.2. Characterization of Practical ADC's

Figure 2.3 shows a block diagram of a practical analog to digital converter. The input S represents the signal to be digitized. A reference signal R defines the full-scale value of S, and the output O_D is the closest approximation to the ratio X = S/R within the specified resolution of the converter.

The transfer characteristic for an ideal N-bit, binary output A/D converter is shown in Fig. 2.4. The binary output word has the

*An important exception are pulse code modulation (PCM) coders in which a nonlinear conversion characteristic is used to accommodate a large dynamic range of the input signal with a specified signal to noise ratio.

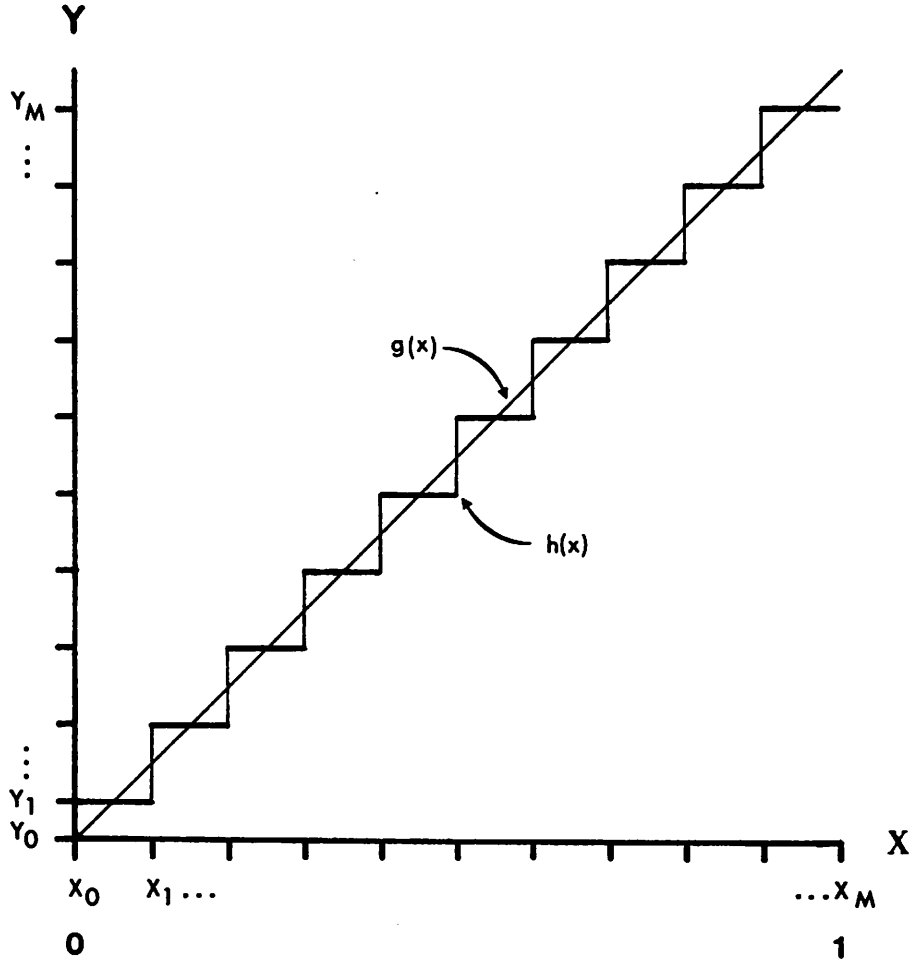


Fig. 2.2. Quantization Function Assignment for Minimum Distortion.

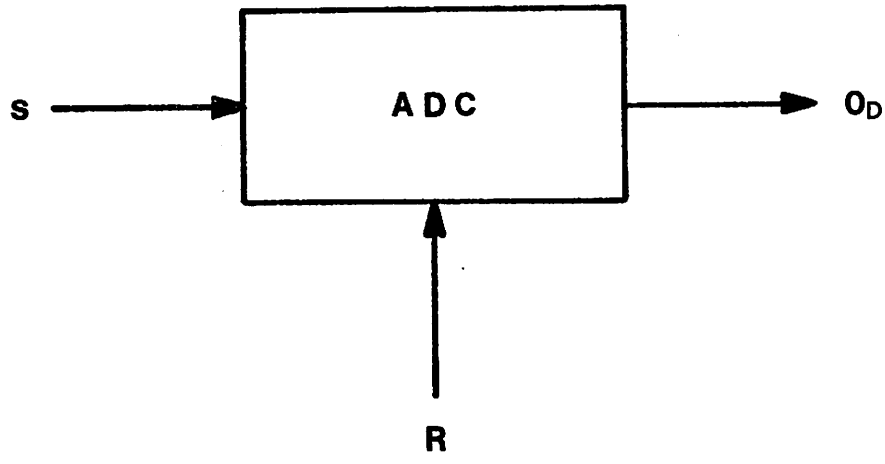


Fig. 2.3. Analog-to-Digital Converter.

form:

$$O_D = \sum_{i=1}^{N} a_i 2^{-i} \quad . \tag{2.5}$$

In this notation a_1 is the most significant bit (MSB) and a_N is the least significant bit (LSB). The resolution of the converter is $\pm (R/2^{N+1})$ or $\pm$ 1/2 LSB.

It was shown in the preceding section that the quantizing distortion measure D_2 is minimized by a least-squares fit of the quantizing function h(x) about the reference line g(x) = x. In practical converters this ideal assignment can only be approximated with physical components. Hence the measured quantizing characteristic h'(x) will differ from the ideal function h(x). Figure 2.5(a) illustrates an arbitrary form of h'(x) for a 3-bit converter. For circuit design purposes only deviations from the ideal quantizer are of concern. It is convenient, therefore, to define a difference error function,

$$\varepsilon_X(x) \equiv h'(x) - h(x) \ ,$$

which eliminates the inherent quantizing distortion from consideration. An inverse error function $\varepsilon_Y(y)$ may also be defined as a one-to-one relation of the error function $\varepsilon_X(x)$ to the digital output variable Y. This inverse error function is shown in Fig. 2.5(b) for the 3-bit case of Fig. 2.5(a). The use of $\varepsilon_Y(y)$ as an error measure permits ready identification of commonly specified nonideal characteristics exhibited by practical analog to digital converter.

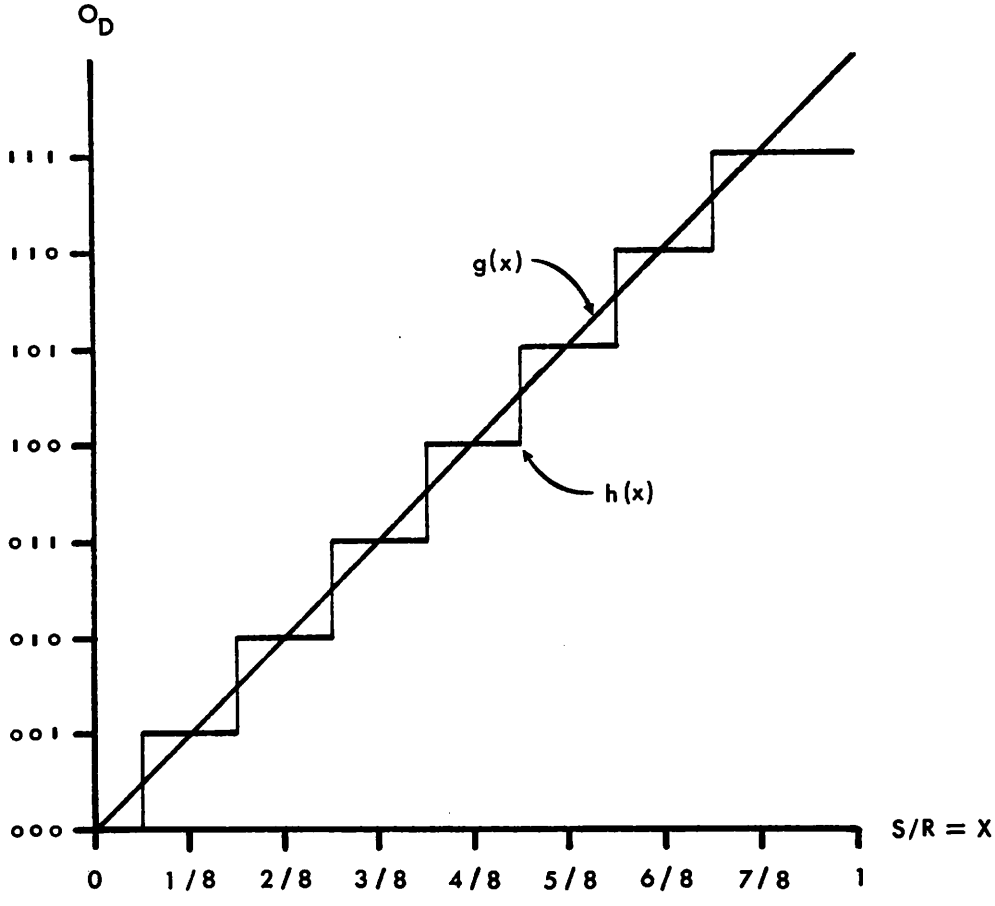
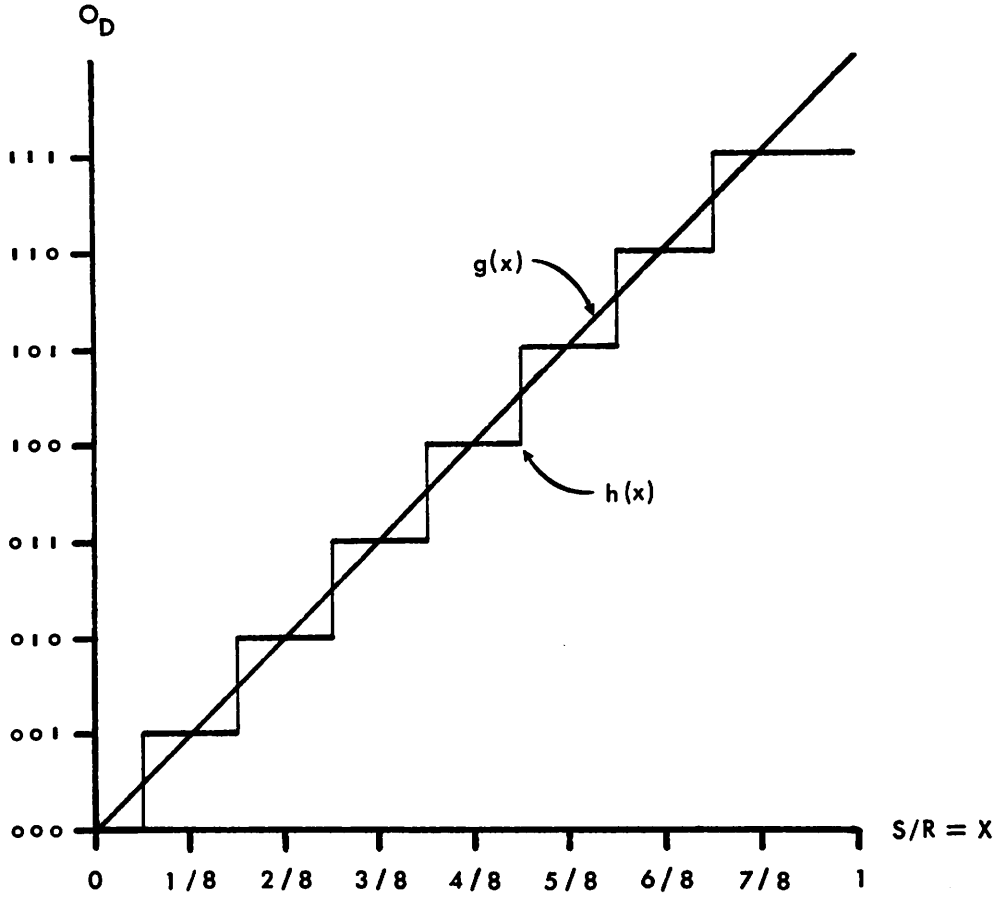


Fig. 2.4. Ideal Transfer Characteristic for a Binary Output ADC.



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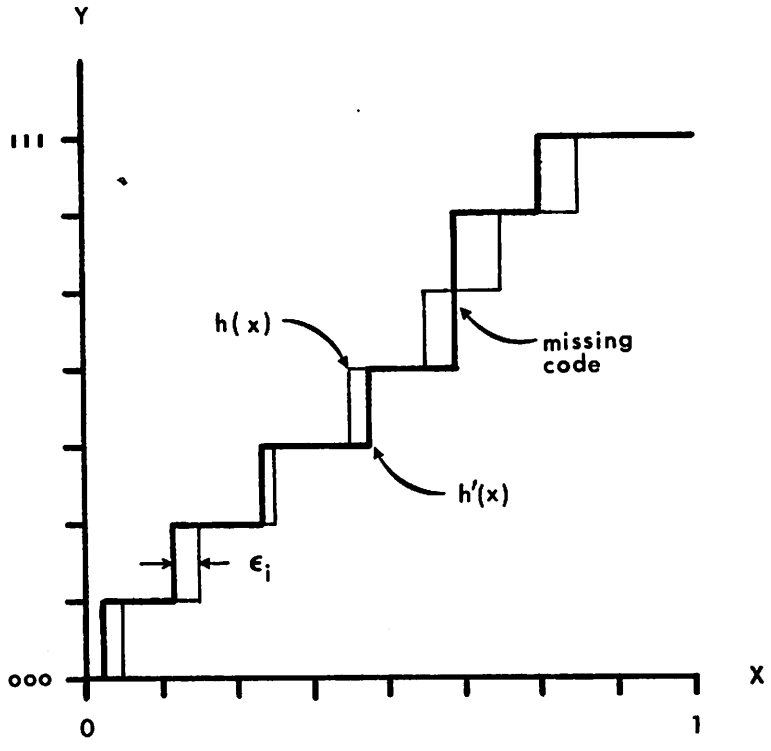
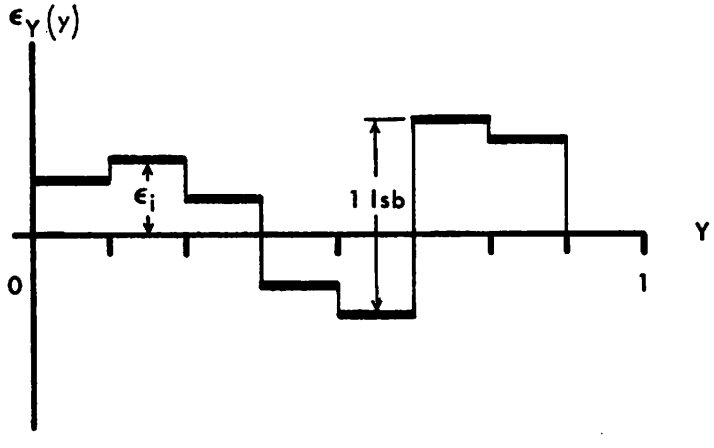


(a)



(b)

Fig. 2.5(a). Arbitrary Transfer Characteristic for a Nonideal ADC.

(b). Inverse Error Function for the Characteristic in Figure 5(a).

Offset is an error specification which indicates a constant shift of the measured characteristic h'(x) with respect to h(x). The offset error may be conveniently defined as:

$$\varepsilon_O = \varepsilon_Y(0) \ .$$

Similarly, a constant slope deviation in the line g'(x) which is induced by the midpoints of h'(x) with respect to the ideal reference line g(x) = x is denoted a gain or scale-factor error, ε_G. The error component ε_G is defined as

$$\varepsilon_G = \frac{2}{2^n-1} \sum_{i=1}^{2^n-1} [\varepsilon(y)-\varepsilon_O] \ .$$

Worst-case nonlinearity is specified from $\varepsilon_Y(y)$ as

$$\varepsilon_N = \text{Max}|\varepsilon_Y(y)| - \varepsilon_O - \varepsilon_G^* \ ,$$

where ε_G^* is the gain error component at the point y_M where $\varepsilon_Y(y)$ is a maximum,

$$\varepsilon_G^* = \varepsilon_G \frac{y_M}{2^n-1} \ .$$

Non-monotonicity is a qualitative term which refers to sign changes in the slope of the induced line g'(x) and is indicated directly by sign changes in the error function $\varepsilon_Y(y)$. Whenever differential nonlinearity becomes excessive missing output codes result; this is indicated whenever $|\varepsilon_Y(y_{i+1}) - \varepsilon_Y(y_i)| > \frac{1}{2^n}$ for an n-bit converter. Figure 2.6 shows these error components for a 3-bit converter.

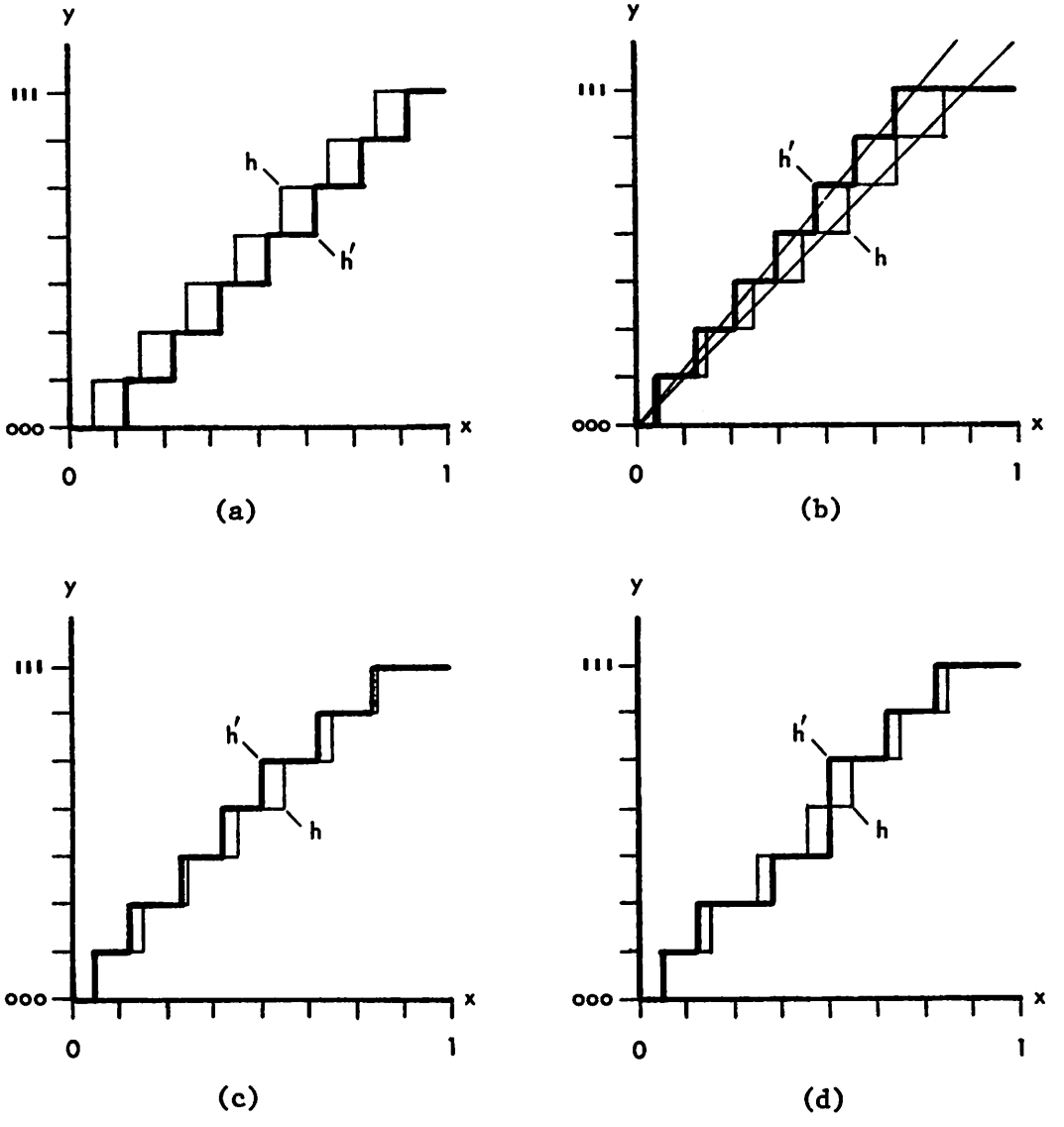


Fig. 2.6. Typical ADC Error Components

(a). Offset Error

(b). Gain Error

(c). Nonlinearity

(d). Missing Output Code.

It is common practice to specify the maximum cummulative conversion error at any point to be below the resolution of the converter ($\pm$ 1/2 LSB).* Hence, the restriction

$$\text{Max}|\varepsilon_Y(y)| \leq \frac{1}{2^{n+1}}$$

has to be maintained over the full range of operating conditions.

An additional specification is converter accuracy. The term absolute accuracy refers to how closely the converter output represents a known test signal such as a voltage standard, and is normally an indication of the quality of the reference signal R. The term relative accuracy, on the other hand, is a measure of how close the converter output is to the true value of any input signal with respect to the full-scale value. In this work the reference signal is assumed to be externally provided; therefore, only relative accuracy is a design consideration.

*In some converter applications resolution is higher than accuracy. The improved resolution at low signal levels increases the dynamic range of conversion. At larger signal levels, however, the resolution is decreased.

CHAPTER III

INTEGRABLE ANALOG TO DIGITAL CONVERTERS

Of the numerous approaches to analog to digital conversion that have been reported to date [3], only a few are amenable to monolithic integrated circuit (IC) realization. The most important restrictions for fabrication in monolithic form are power dissipation and chip size. The available power is limited by package dissipation ratings and the maximum temperature at which the circuit will operate within specifications. The number and size of the components required to implement a particular conversion approach determines the chip size, which in turn is limited by yield/cost considerations.

The attainable accuracy in a practical ADC is reflected by the matching characteristics of such critical components as resistors in precision voltage (or current) dividers and transistors in the input stage of voltage comparators. Integrated circuit fabrication using planar technology defines device surface geometries through photolithography. The resulting random edge location uncertainties demand increased component sizes for improved accuracy. An increase in component size, however, results in increased die size and cost. Lower operating speeds also result because parasitic capacitance increases. Higher current levels will increase operating speed at the expense of additional power dissipation and may eventually degrade accuracy because of thermal gradients on the chip.

In order to perform an n-bit analog to digital conversion it is necessary to generate the quantizing intervals ($I_1,\ldots,I_{2^n}$) defined in Section 2.1. The 2^n quantizing intervals represent information

which may be distributed both in space and in time. Thus, improved conversion speed may be obtained at the expense of an increased number of components and vice versa. The conversion approaches to be described reflect the tradeoff between conversion time and component count. At one extreme is the fastest conversion approach, in which all the quantizing intervals are generated simultaneously. In this parallel scheme it is necessary to match about 2^n components, and therefore a large silicon area is required. At the other extreme is a serial conversion approach in which one quantizing interval is generated at a time. Conversion speed is low, but only a minimal number of precision components is needed to implement a serial ADC. In successive approximation converters, on the other hand, a group of several quantizing intervals is considered at a time. The value of the unknown signal is approached through a sequence of decisions in which the number of intervals in the group is made progressively smaller. As a result, conversion speed is higher than for the serial converter and component count is less than for the parallel case. Successive approximation converters, therefore, represent an attractive compromise suitable for integrated circuit realization.

3.1. Topological Classification of Analog to Digital Converters

A. Parallel

Figure 3.1 shows the block diagram of a parallel ADC. The reference voltage V_R is divided into 2^N increments corresponding to the quantizing intervals. Each fraction of the reference voltage is connected to one input of a comparator, and the analog voltage V_X is connected to the other input. A "0" appears at the comparator output if V_X is less than the corresponding fractional reference; otherwise the output is "1". The exclusive-OR gates connected to the comparator outputs indicate the location of the closest approximation to V_X. This information is then encoded into an N-bit binary word. Conversion time is very short with this type of converter because the quantization process is realized in a single step. A large number of components is required, however, and to increase the resolution by one bit the component count is approximately doubled. For this reason monolithic parallel converters with resolutions higher than about 4 bits are not practical at present.

B. Serial

As indicated in Fig. 3.2, a serial ADC consists of a ramp generator, a voltage comparator, an AND gate and a digital counter. The counter is initially set to zero, and the ramp generator -- which transforms the reference voltage into a linear function of time -- is started. Clock pulses are counted until the ramp voltage exceeds V_X. The input to the counter is then blocked, and the number of pulses stored is the digital output. In order to resolve N bits to full

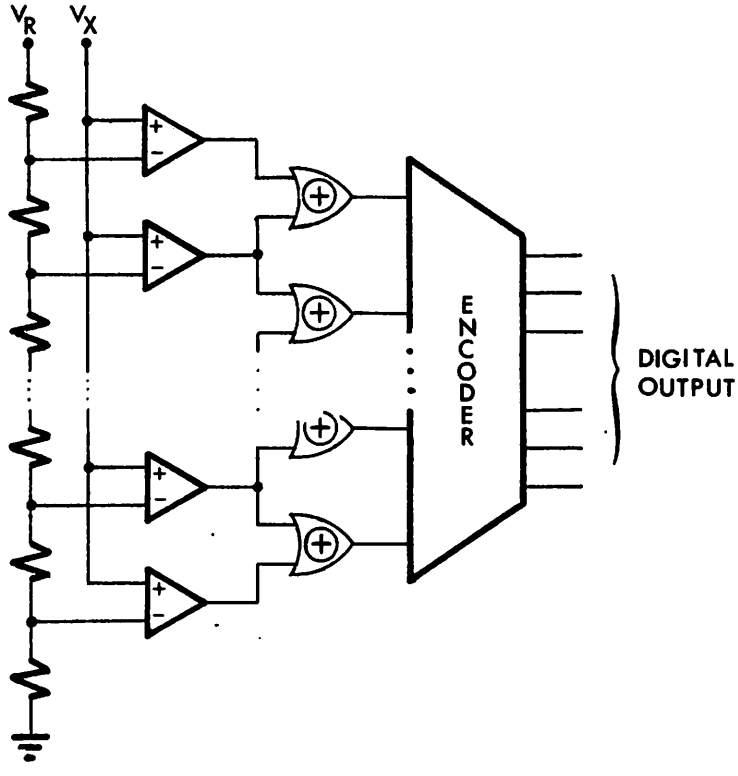


Fig. 3.1. Parallel Analog-to-Digital Converter.

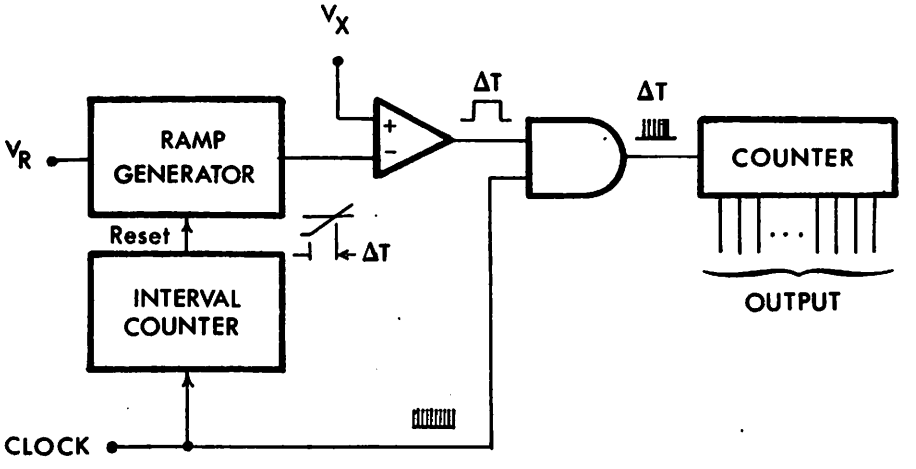


Fig. 3.2. Serial Analog-to-Digital Converter.

scale the counter has to count 2^{N-1} clock pulses. Therefore, conversion speed is low.

The ramp generator can be implemented in several ways. In the circuit of Fig. 3.3(a) a capacitor is charged with a current source proportional to V_R producing a linear ramp. The interval counter is programmed to close the switch and discharge the capacitor at the end of 2^N-1 clock pulses. The ramp can also be generated with an operational amplifier integrator circuit as shown in Fig. 3.3(b). Alternatively, as indicated in Fig. 3.3(c), the binary word stored in the output counter can be transformed into a voltage by means of a digital-to-analog converter. The output voltage of the DAC increases in a staircase fashion, one quantizing interval at a time, and is compared with the analog voltage V_X.

Slow conversion speed is the most important drawback of this method. However, for applications such as digital panel meters, where speed is unimportant, this method is attractive. A modified serial approach which employs three ramp periods and on-chip digital processing for offset cancellation has been reported [4]. The method is compatible with standard MOS fabrication processes and appears capable of resolving 11 bits in 30 ms.

C. Successive Approximation

i) Type I (Standard Successive Approximation)

In the converter shown in Fig. 3.4 each bit is compared in sequence, from MSB to LSB, with V_X. The programmer initially produces a DAC output voltage corresponding to $\frac{1}{2} V_R$, and comparison with V_X determines the value of the MSB. Thereafter the programmer uses the previously encoded bits to generate successively closer

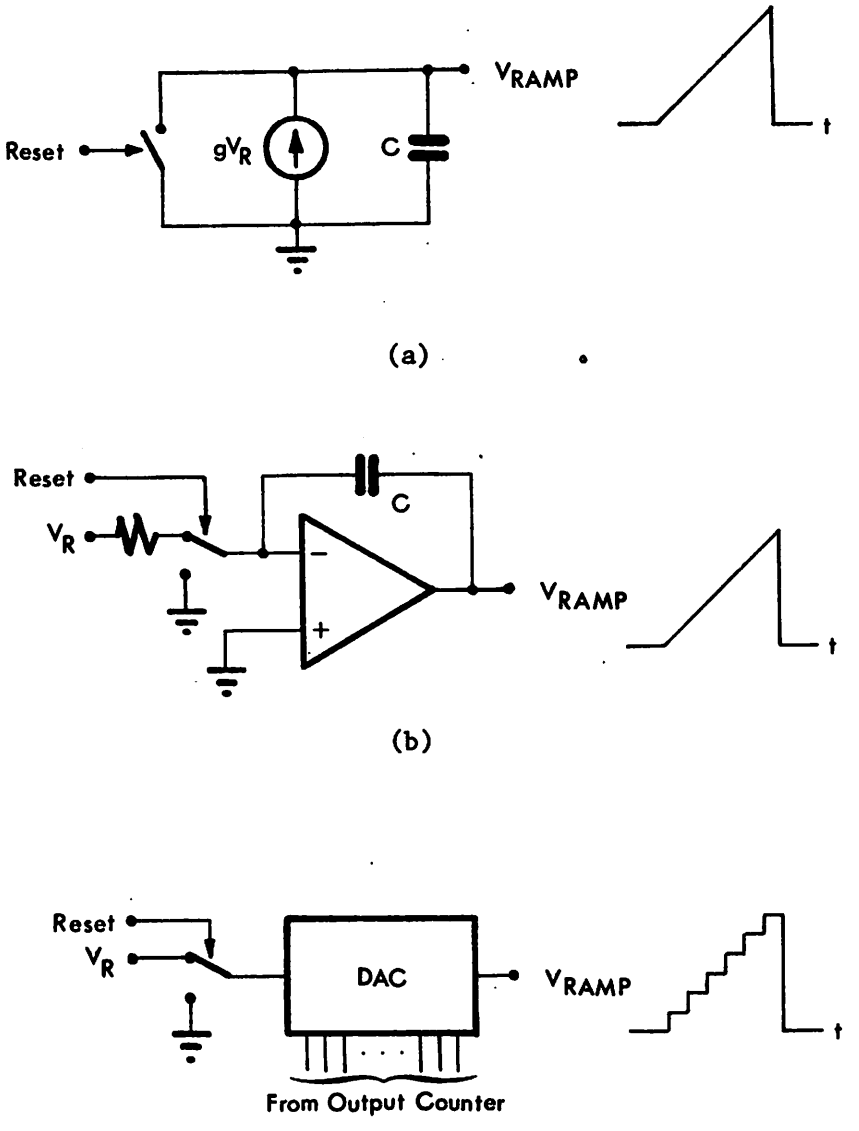


Fig. 3.3. Ramp Generator Implementations

(a). Current Source and Capacitor Circuit

(b). Operational Amplifier Integrator

(c). DAC Staircase Generator

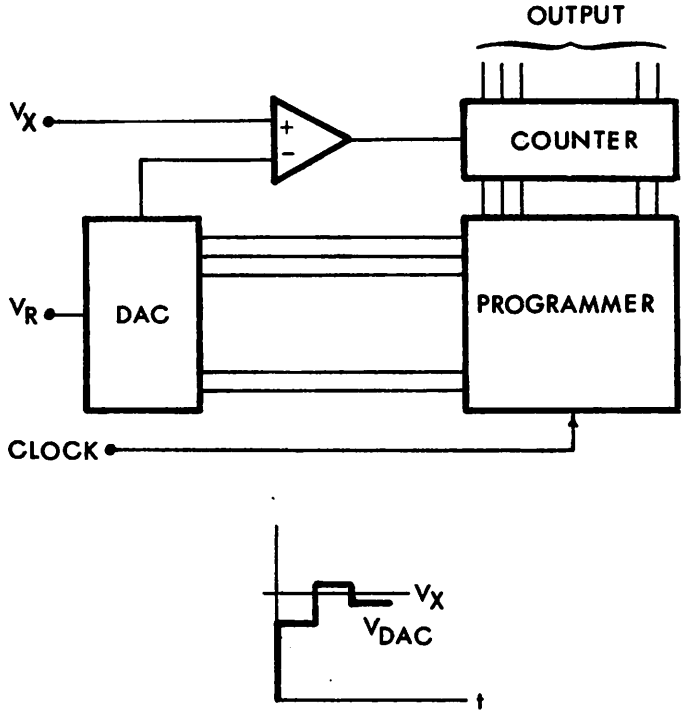


Fig. 3.4. Successive Approximation Analog-to-Digital Converter.

estimates of V_X in the DAC until the LSB is determined. Thus an N-bit conversion sequence is completed in N steps.*

ii) Type II (Serial/Parallel)

By converting n bits simultaneously the converter of Fig. 3.5 achieves an N-bit conversion in N/n steps. The system consists of an n-bit parallel ADC, two (n-1)-bit DAC's with input decoders, an output register, and a sequencing control circuit. Initially the DAC's set the low reference level to zero and the high reference level to V_R. Thus the ADC indicates in which of 2^n intervals V_X is located. This interval is then subdivided into 2^n levels by division and level shifting of V_R in the DACs. The new intervals are compared with V_X, and the process continues until the intervals correspond to the LSB. In this type of converter both the internal ADC and the DACs must have an N-bit relative accuracy.

It is evident that successive approximation methods being a compromise of conversion speed and component count represent a broad class of conversion approaches which are potentially realizable as a single-chip integrated circuit.

*This presumes that the digital to analog conversion takes place in a single step. The converter discussed in Chapter V requires more than one step per D/A conversion.

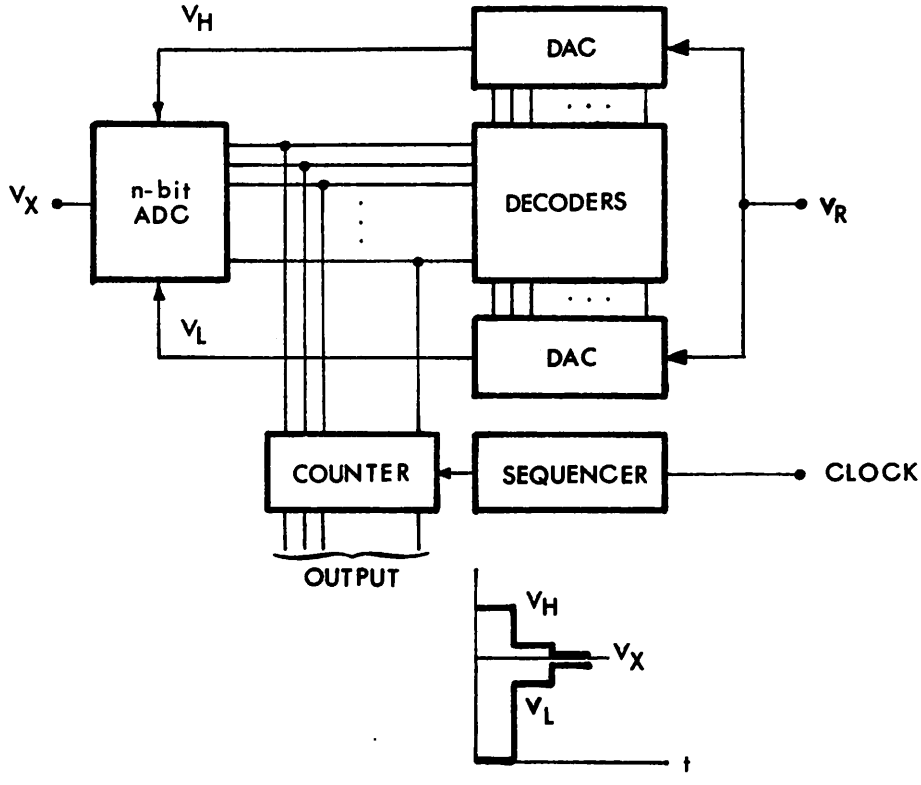


Fig. 3.5. Serial/Parallel Analog-to-Digital Converter.

CHAPTER IV

ACCURACY CONSIDERATIONS IN MONOLITHIC PASSIVE COMPONENTS

The comparison of conversion approaches carried out in the preceding chapter indicates that successive approximation converters are particularly suited for integrated realization. This class of converters generally require the generation of accurate fractions of the reference voltage to establish the value of the bits $a_1,\ldots,a_N$. In an integrated circuit these fractions can be obtained with resistor or capacitor dividers or through scaling of active device geometries. The relatively poor matching of active device characteristics, however, makes it difficult to achieve accurate voltage or current ratios over a large range of values and operating conditions. For this reason feedback techniques are normally used to define current or voltage ratios through fractions of passive components only. Therefore, conversion approaches based primarily on scaled dimensions of active devices are not given further consideration.

In this chapter resistor and capacitor dividers are compared with respect to matching characteristics and voltage and temperature coefficients of the components. The results of this comparison suggest that conversion approaches based on capacitor ratios, such as charge-redistribution converters, are potentially more accurate than approaches based on resistor ratios.

4.1. Component Mismatches

The basis of the planar technology used to fabricate integrated

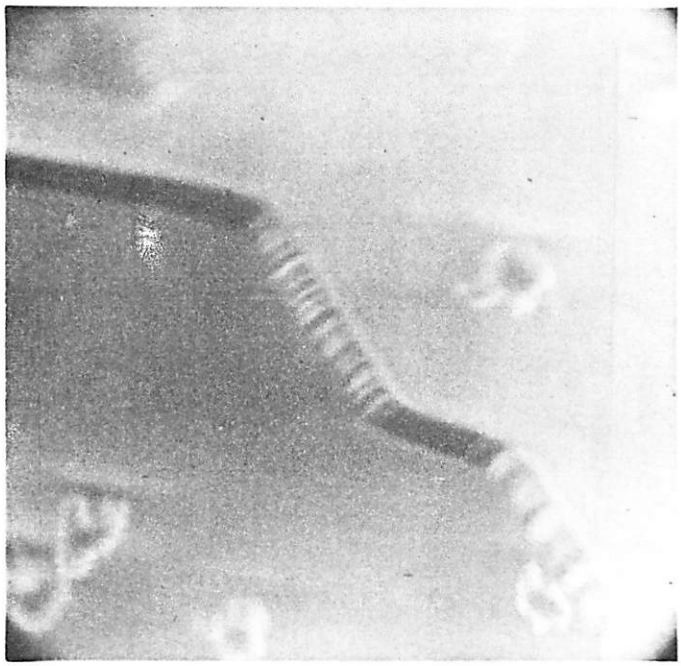


Fig. 4.1. SEM Photograph of SiO_2 Edge (6,880X, 70°).

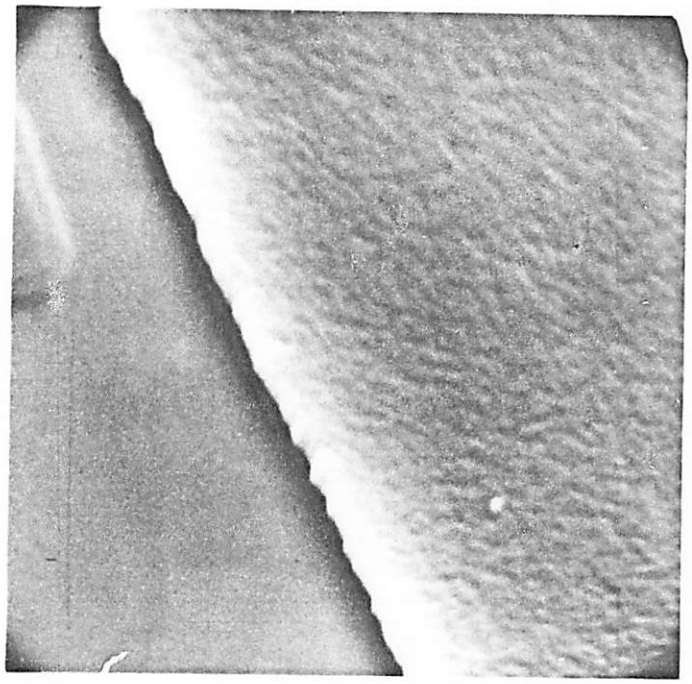


Fig. 4.2. SEM Photograph of Polycrystalline Silicon Edge. (6,880X, 70°).

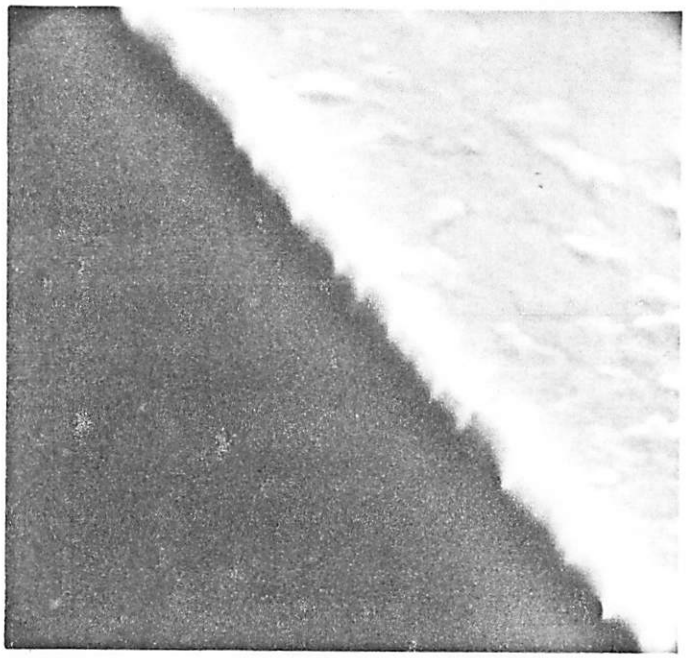


Fig. 4.3. SEM Photograph of Aluminum Edge (6,880X, 70°).

circuits in large volume is to define device surface geometries through photolithography. This process involves the removal from selected chip areas of layers of materials such as photoresist, silicon dioxide, polycrystalline silicon, and vacuum-evaporated aluminum. The chemical reactions involved in etching these amorphous or polycrystalline layers proceed nonuniformly. The random uncertainties in edge definition that arise are an important limitation in the attainable matching of components. Figures 4.1 through 4.3 are scanning electron microscope photographs which show the domain nature of the etching process in the abovementioned materials.

To determine the impact of component mismatches on the accuracy of the fractions required in successive approximation ADCs, consider the effect of small variations of the components in the fraction $F = A/(A+B)$:

$$S \equiv \frac{\Delta F}{F} = \frac{B}{A+B}\left[\frac{\Delta A}{A} - \frac{\Delta B}{B}\right] . \tag{4.1}$$

Taking these variations as uncorrelated random fluctuations with standard deviation σ, the mismatch sensitivity may be expressed as

$$\sigma_s = \frac{B}{A+B}\left[\sqrt{\left(\frac{1}{A}\right)^2+\left(\frac{1}{B}\right)^2}\right]\sigma. \tag{4.2}$$

In particular, for $A = B$,

$$\sigma_s = \frac{1}{\sqrt{2}}\frac{\sigma}{A} = \frac{1}{\sqrt{2}}\frac{\sigma}{B} . \tag{4.3}$$

Typical geometries for a pair of nominally identical resistors are shown in Fig. 4.4. The resistance value is approximately given by:

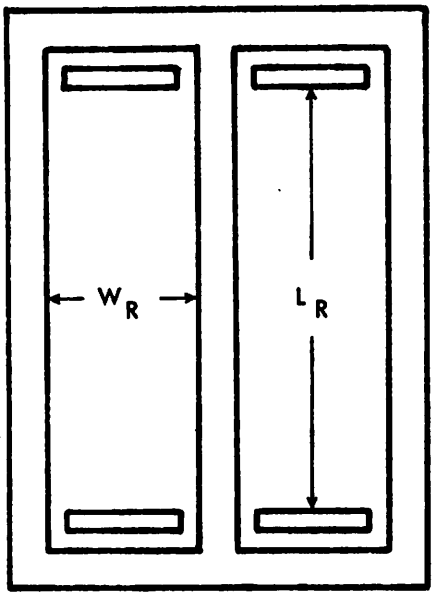


Fig. 4.4. Surface Geometries for a Pair of Integrated Resistors.

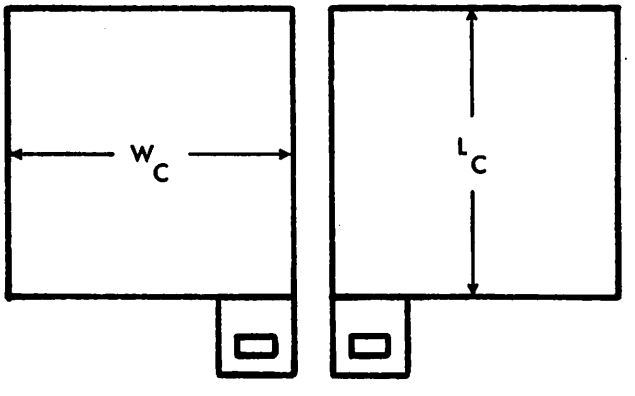


Fig. 4.5. Surface Geometries for a Pair of MOS Capacitors.

$$R = R_S \frac{L_R}{W_R} , \tag{4.4}$$

where R_S is the sheet resistance, $R_S = \bar{\rho}/t_R$, for an average resistivity $\bar{\rho}$ and resistor thickness t_R. The uncertainty in edge definition is modelled as a simple random displacement of the entire edge with standard deviation σ_X. This results in a relative mismatch,

$$\frac{\sigma_R}{R} = \left[\sqrt{\left(\frac{1}{L_R}\right)^2 + \left(\frac{1}{W_R}\right)^2} \right] \sigma_X . \tag{4.5}$$

Because the values of sheet resistance available in integrated resistors are limited, fairly large length-to-width ratios are normally used. Therefore,

$$\frac{\sigma_R}{R} \cong \frac{\sigma_X}{W_R} . \tag{4.6}$$

Thus, the mismatch sensitivity for a resistor ratio $F_R = R_1/(R_1+R_2)$ is:

$$\sigma_{S_R} \cong \frac{1}{\sqrt{2}} \frac{\sigma_X}{W_R} , \tag{4.7}$$

for $R_1 = R_2$.

For MOS capacitors, on the other hand, the capacitance is given by

$$C = C_{OX} L_C W_C , \tag{4.8}$$

where C_{OX} is the capacitance per unit area, $C_{OX} = \varepsilon_{OX}/t_{OX}$, for a dielectric permitivity ε_{OX} and oxide thickness t_{OX}. The dimensions L_C and W_C are shown in Fig. 4.5 for a pair of nominally identical

capacitors. The mismatch due to an edge uncertainty σ_X is

$$\frac{\sigma_C}{C} = \left[\sqrt{\left(\frac{1}{L_C}\right)^2+\left(\frac{1}{W_C}\right)^2}\right] \sigma_X . \tag{4.9}$$

For rectangular geometries this quantity is minimized* for $L_C = W_C$. Then,

$$\frac{\sigma_C}{C} = \sqrt{2}\,\frac{\sigma_X}{L_C} . \tag{4.10}$$

The mismatch sensitivity of a capacitor fraction $F_C = C_1/(C_1+C_2)$ with $C_1 = C_2$ is then

$$\sigma_{S_C} = \frac{\sigma_X}{L_C} . \tag{4.11}$$

From (3.7) and (3.11) the mismatch sensitivities of resistor and capacitor dividers can be compared:

$$\frac{\sigma_{S_R}}{\sigma_{S_C}} = \frac{1}{\sqrt{2}}\,\frac{L_C}{W_R} = \frac{\sigma_R/R}{\sigma_C/C} \tag{4.12}$$

Considering now resistors and capacitors which occupy approximately the same area,+ this ratio becomes

---

*The optimum capacitor shape for minimum mismatch sensitivity is a circle.

+Contact areas are neglected. In addition, the required isolation diffusion increases the resistor area significantly. In (4.13) the actual resistor area is taken as twice $W_R L_R$; i.e., $2W_R L_R = L_C^2$.

$$\frac{\sigma_{S_R}}{\sigma_{S_C}} \cong \sqrt{\frac{L_R}{W_R}} > 1 \ . \qquad (4.13)$$

Thus, MOS capacitors can be expected to exhibit better matching characteristics than integrated resistors of approximately the same size. This characteristic is a result of the fact that with capacitors the freedom exists to optimize the device geometry for minimum sensitivity to edge uncertainties. Table 4.1 lists published experimental data on component matching. The improved uniformity in sheet resistance obtained with ion implantation results in resistors with better matching characteristics than diffused resistors. However, photomasking uncertainties are still present for both fabrication technologies. The data in Table 4.1 suggests a standard deviation edge uncertainty of approximately 0.1 μm.

4.2. Voltage Coefficient

The variation of resistance with applied voltage in junction isolated resistors arises from changes in the width of the depletion region within the resistor. Figure 4.6 shows the cross-section of a typical p-base diffused resistor. Since the n isolation region is kept at a positive potential to maintain the junction reverse biased, this isolation region acts as the gate of a junction field-effect transistor (JFET) with the resistor terminals acting as drain and source.

The voltage coefficient of resistance can then be estimated in terms of conventional JFET theory. The analysis is simplified by considering only the effect that variations in the depletion width x_d have on the effective resistor thickness $t_R = x_j - x_d$. From

Table 4.1. COMPONENT MATCHING DATA

Component	Fabrication technique	Standard Deviation Matching	σ_x	Temperature coefficient	Voltage coefficient
Resistors	Diffused (W=50μ)	±0.23%[5]	0.1 μ	+2000 ppm/°C	~200 ppm/V[6]
	Ion-implanted (W=40μ)	±0.12%[5]	0.05 μ	+400 ppm/°C	~800 ppm/V[6]
Capacitors [6]	MOS (t_{OX}=0.1 μ L≈10mils)	±0.06%	0.1 μ	26 ppm/°C	~ 10 ppm/V

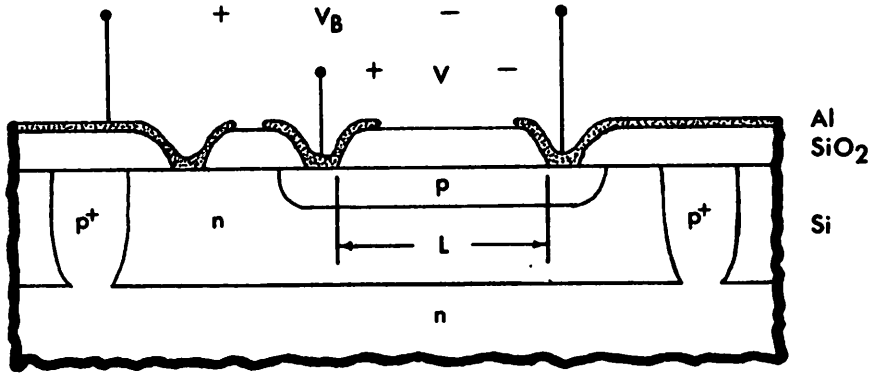


Fig. 4.6. Cross-section of a Diffused Resistor.

Appendix A the voltage coefficient of resistance can be expressed as

$$\gamma_V^R = \frac{1}{R}\frac{\partial R}{\partial V} = \frac{x_d\bar{\sigma}_d/x_j\bar{\sigma}}{2[V+\phi_B+V_B][1-x_d\bar{\sigma}_d/x_j\bar{\sigma}]} \qquad (4.14)$$

where,

$\bar{\sigma}_d$ = average conductivity substracted by the depletion layer

and $\bar{\sigma}$ = average conductivity of the p region.

For a standard base diffusion with $R_S = 200\ \Omega/\square$ and $x_j = 3\ \mu m$, Eq. (4.14) predicts $\gamma_V^R = 500$ ppm/V for typical operating voltages. The value of γ_V^R for a diffused resistor in Table 4.1 is for $R_S = 135\ \Omega/\square$.

The voltage coefficient for MOS capacitors is derived in Appendix B and can be expressed as

$$\gamma_V^C = \frac{1}{C}\frac{\partial C}{\partial V} = \frac{\frac{\partial^2}{\partial\phi_S^2}\left(\frac{Q_S}{C_O}\right)}{\left[1+\frac{\partial}{\partial\phi_S}\left(\frac{Q_S}{C_O}\right)\right]^3}\ , \qquad (4.15)$$

where Q_S is the net charge in the space charge region at the semiconductor surface and ϕ_S is the potential at the semiconductor surface. Equation (4.15) can be solved for lightly doped substrates where Boltzmann statistics apply [7], but it is known experimentally that the variation of capacitance with voltage is minimized when the semiconductor layer is degenerately doped. Under these conditions Fermi-Dirac statistics must be applied, and the effect of the impurity band "tailing" taken into account. Recent studies of the transport mechanisms of heavily doped semiconductors [8], [9] provide the

necessary theoretical framework to realize such calculation via computer. An estimate can be made, however, using the approach of Van Overstraeten, De Man and Mertens [8] which permits the use of the classical equations through the introduction of a concentration-dependend "effective" intrinsic concentration, n_{ie}, in place of the classical intrinsic concentration, n_i. A calculation for a surface concentration of 10^{20} indicates $\gamma_V^C \cong 10$ ppm/V in close agreement with the data on Table 4.1.

Comparison of resistors and MOS capacitors on the basis of voltage coefficients, therefore, shows that MOS capacitors exhibit at least an order of magnitude improvement in performance over integrated resistors.

4.3. Temperature Coefficient

The thermal variation of resistance has been described in some detail in the literature [10], [11]. It is found that for diffused resistors the thermal variations are dependent on the surface concentration (or average conductivity), and follows closely the thermal variations in mobility. For a sheet resistance of 200 Ω/□ with $x_j = 3\ \mu$, a numerical calculation for a Gaussian profile [12] indicates a $\gamma_T^C = 2000$ ppm/°C in agreement with the observed value shown on Table 4.1.

For MOS capacitors a calculation of the temperature coefficient entails computation of the effective intrinsic concentration for several temperatures. However, the experimentally observed value of 26 ppm/°C for a surface concentration of $\sim 10^{20} cm^{-3}$ suffices to indicate that in this regard also MOS capacitors exhibit superior

performance over integrated resistors.

On the basis of matching characteristics, voltage and temperature coefficients, therefore, A/D conversion schemes based on ratios of capacitors can be expected to be potentially more accurate than approaches which utilize resistive dividers.

CHAPTER V

CHARGE-REDISTRIBUTION CONVERSION APPROACHES

5.1. Overview

The excellent potential accuracy of MOS capacitor dividers can be exploited in the realization of monolithic converters through application of the principle of charge redistribution between capacitors. The principle is illustrated in the circuit in Fig. 5.1.

Initially capacitors C_1 and C_2 are charged to voltage levels $V_1(0)$ and $V_2(0)$ respectively. The initial charge in the circuit is:

$$Q(0) = C_1V_1(0) + C_2V_2(0) \ . \tag{5.1}$$

Subsequently the switch is closed and the charge is redistributed to make $V_1(f) = V_2(f) = V(f)$. Since the total charge is conserved,

$$Q(f) = Q(0). \tag{5.2a}$$

Then,

$$(C_1+C_2)V(f) = C_1V_1(0) + C_2V_2(0); \tag{5.2b}$$

or,

$$V(f) = \frac{C_1}{C_1+C_2} V_1(0) + \frac{C_2}{C_1+C_2} V_2(0) \ . \tag{5.3}$$

In this manner fractions of a reference voltage can be generated to perform a successive approximation A/D conversion.

Conventional charge-redistribution conversion realizations [13] have required operational amplifies and floating capacitors in addition to digital circuitry for counting, sequencing and data

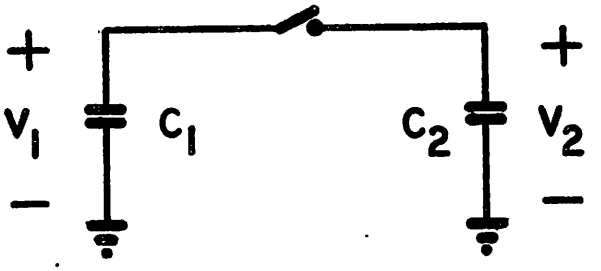
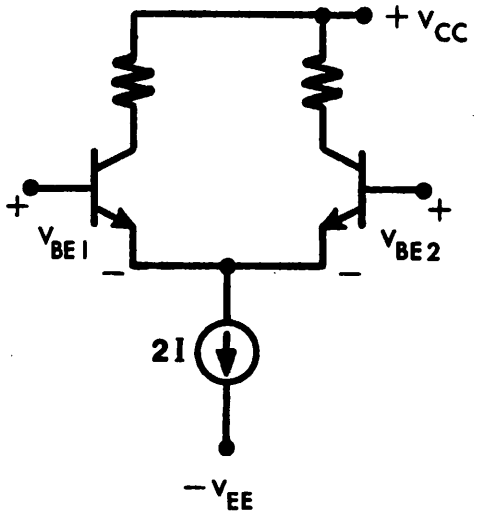


Fig. 5.1. Two-capacitor Circuit for Charge Redistribution.

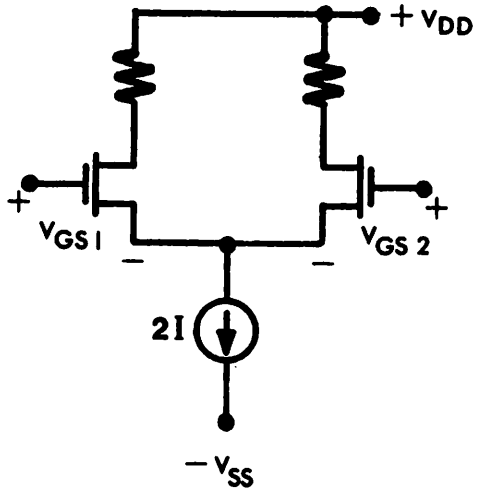
storage. The requirement for high performance analog circuit blocks can ordinarily be met with bipolar transistor circuit realizations. MOS transistor designs, on the other hand, offer the advantage of high density, low cost digital functions, but only analog circuits of significantly reduced performance are obtained with single-polarity MOS technologies. This dual requirement for high performance analog circuitry and high density digital circuits has been prevalent in current monolithic conversion approaches, and has tended to result in hybrid designs with one or more bipolar chips for the analog blocks and an MOS chip for the digital functions [14]. Recent developments in linear designs using complementary MOS (CMOS) [15] and newly-developed compatible bipolar-MOS technologies [16] [17], however, are promising solutions which may permit the realization of single chip analog-to-digital converters.

In this work the approach taken is to develop a conversion technique which is compatible with existing low-cost single polarity (n or p-channel) MOS technologies. The difficulty in obtaining high performance analog circuits with these technologies stems primarily from the parabolic current-voltage characteristic of MOS devices, in contrast with the exponential I-V characteristic of bipolar transistors. This results in low values of transconductance (g_m) for MOS transistors, which in turn is reflected in low gain and high input offset voltages. This fact can be illustrated by comparing a bipolar and an MOS differential pair.

With respect to the bipolar differential amplifier of Fig. 5.2(a), the dc collector current of the transistors is given by [18]:



(a)



(b)

Fig. 5.2(a). Bipolar Transisotr Differential Amplifier.

(b). MOS Transistor Differential Amplifier.

$$I = \alpha I_{EO} e^{qV_{BE}/kT} , \tag{5.4}$$

and

$$(g_m)_{bipolar} \equiv \frac{\partial I}{\partial V_{BE}} = \frac{q}{kT} I. \tag{5.5}$$

For a saturated MOS transistor in the differential pair of Fig. 5.2(b) the drain current is given by [19]:

$$I = k[V_{GS}-V_T]^2 , \tag{5.6}$$

where

$$k = \frac{\mu k_{OX} \epsilon_O}{t_{OX}} \frac{W}{L} ,$$

and

$$(g_m)_{MOS} \equiv \frac{\partial I}{\partial V_{GS}} = \frac{2I}{V_{GS}-V_T}$$

$$= 2\sqrt{kI} . \tag{5.7}$$

From (5.5) and (5.7) [20],

$$\frac{(g_m)_{bipolar}}{(g_m)_{MOS}} = \frac{1}{2} \frac{q}{kT} \sqrt{\frac{I}{K}} . \tag{5.8}$$

In the case of an n-channel MOSFET with parameters μ_n = 400 $cm^2/V \cdot sec$, t_{OX} = 1000 Å, channel width-to-length ratio W/L = 10, and I = 25 μA, the ratio (5.8) is approximately 8. This ratio becomes larger with increasing current levels. Moreover, although the transconductance of the MOS transistor can be increased with larger W/L ratios, the improvement is obtained at the expense of larger area and increased capacitance.

$$I = \alpha I_{EO} e^{qV_{BE}/kT} , \tag{5.4}$$

and

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For a saturated MOS transistor in the differential pair of Fig. 5.2(b) the drain current is given by [19]:

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where

$$k = \frac{\mu k_{OX} \epsilon_O}{t_{OX}} \frac{W}{L} ,$$

and

$$(g_m)_{MOS} \equiv \frac{\partial I}{\partial V_{GS}} = \frac{2I}{V_{GS}-V_T}$$

$$= 2\sqrt{kI} . \tag{5.7}$$

From (5.5) and (5.7) [20],

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The small values of transconductance also affect input offset voltage, a source of error in operational amplifiers and voltage comparators. For a mismatch ΔI in the drain or collector currents in a differential pair, an equivalent differential input voltage must be applied to equalize the currents. This "offset" voltage, V_{OS}, is given by

$$V_{OS} = \frac{\Delta I}{g_m} . \tag{5.9}$$

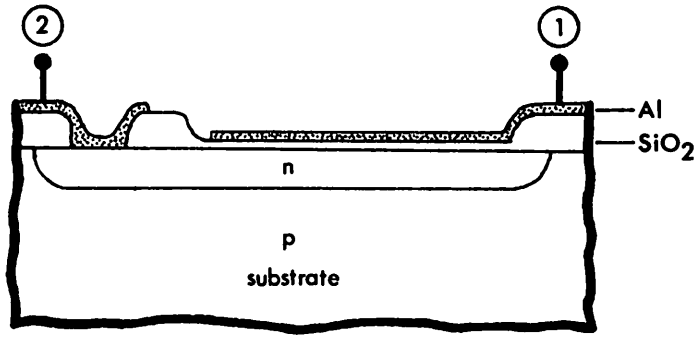
Comparing a bipolar and an MOS differential pair operating at the same current levels and with an identical current mismatch ΔI, the corresponding input offset voltages are [21]:

$$\frac{(V_{OS})_{bipolar}}{(V_{OS})_{MOS}} = \frac{(g_m)_{MOS}}{(g_m)_{bipolar}} . \tag{5.10}$$

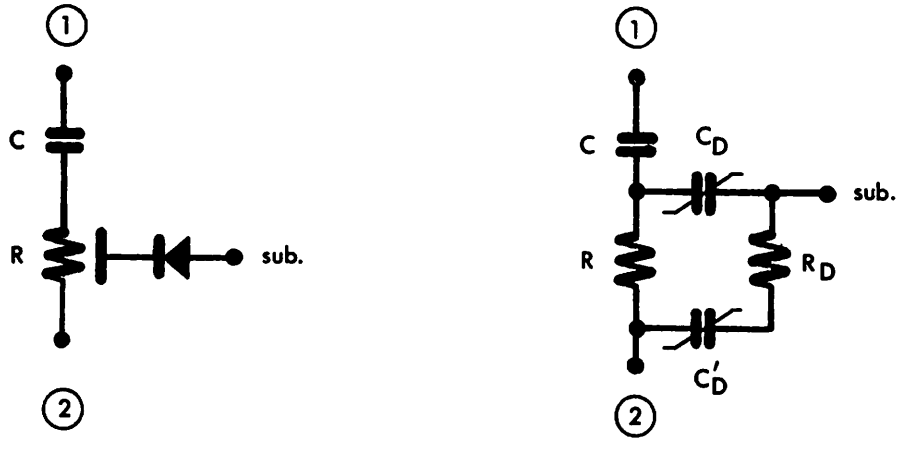
Thus, because the ratio g_m/I is lower for MOS transistors than for bipolar transistors, MOS differential pairs typically exhibit worse offset characteristics than bipolar pairs.

An additional consideration for charge-redistribution converters is the effect of the nonlinear parasitic capacitance which is present in the lower plate of the MOS capacitor structure. Figure 5.3 shows a cross-section of a typical MOS capacitor and an equivalent circuit model.

The parasitic n^+p diode which connects the bottom plate of the capacitor to the substrate will contribute a nonlinear capacitive component whenever the potential at node 2 is allowed to vary. Thus in the case of a voltage divider consisting of two capacitors in series precautions have to be taken to prevent errors arising from



(a)



(b)

Fig. 5.3(a). Cross-section of an MOS Capacitor.

(b). Equivalent Circuit Model.

this parasitic component.

The charge-redistribution conversion technique to be described in the following section overcomes most of the difficulties mentioned by minimizing the number of analog components required [22]. The basic DAC uses only two grounded matched capacitors and several MOS transistor switches. Moreover, the analog-to-digital conversion function is accomplished without an operational amplifier.+ The remaining two sections of the chapter are comparative studies in which the tradeoff between conversion time and the number and relative size of the capacitors for this circuit are analyzed.

5.2. The Two-Capacitor Converter

A. Serial DAC

The serial digital-to-analog converter with nominally identical capacitors C_1 and C_2 is shown in Fig. 5.4. To perform a K-kit D/A conversion, the least significant bit d_1 is considered first.* Capacitor C_1 is precharged either to the reference voltage V_R by a momentary closure of S_2 if $d_1 = 1$ or to ground through S_3 if $d_1 = 0$. Simultaneously C_2 is discharged to ground through S_4. The next step is to redistribute the charge by momentarily closing S_1. The resulting capacitor voltages are:

$$V_1(1) = V_2(1) = \frac{d_1}{2} V_R \ . \qquad (5.11)$$

The next most significant bit d_2 is considered next. Again C_1

+Patent pending.

*The jth bit is denoted d_j in a D/A conversion and a_j in an A/D conversion.

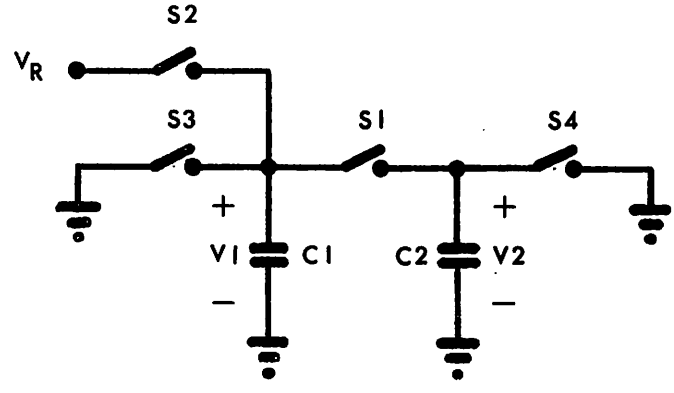


Fig. 5.4. Serial Digital-to-Analog Converter.

is precharged to either V_R or ground depending on the value of d_2 while C_2 holds the voltage level from the previous step. After redistribution the capacitor voltages are:

$$V_1(2) = V_2(2) = (\frac{d_1}{4} + \frac{d_2}{2})V_2 \ . \tag{5.12}$$

The process ends after K redistributions when the voltage on the capacitors is:

$$V_1(K) = V_2(K) = \sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}} V_R, \tag{5.13}$$

which corresponds to a K-bit D/A conversion. In all, a total of 2K charging steps are required to complete the conversion. The sequence is shown schematically in Table 5.1, and Fig. 5.5 illustrates the case for an input word ($d_1 = 1$, $d_2 = 0$, $d_3 = 1$, $d_4 = 1$), corresponding to $\frac{13}{16} V_R$.

B. Successive Approximation ADC

With the addition of a voltage comparator and logic circuitry to the serial DAC, as shown in Fig. 5.6, a successive approximation ADC can be constructed. The logic circuitry includes a data storage register (DSR), a control register for the DAC (DCR), and sequencing and control circuits.

In contrast with the D/A conversion previously described, the A/D conversion begins with the most significant bit a_N. To determine the value of the bit, it is assumed beforehand that its value is "1". A one-bit D/A conversion is performed, and comparison with the

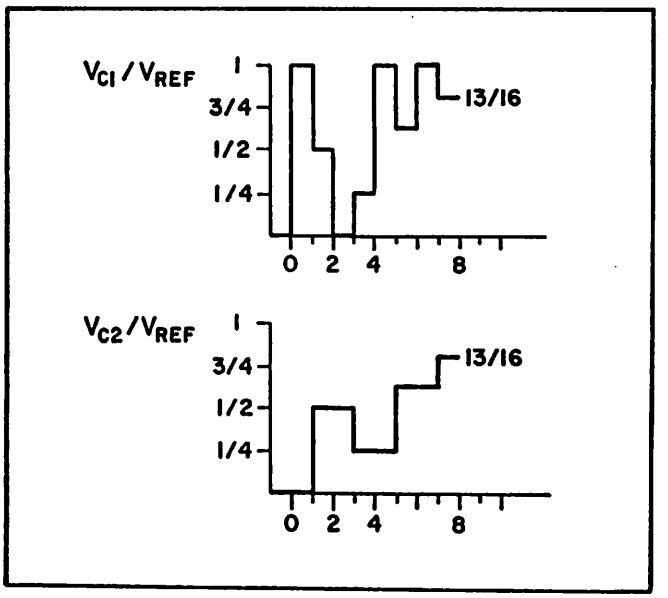


Fig. 5.5. Illustration of D/A Conversion Sequence for the Two-capacitor Converter.

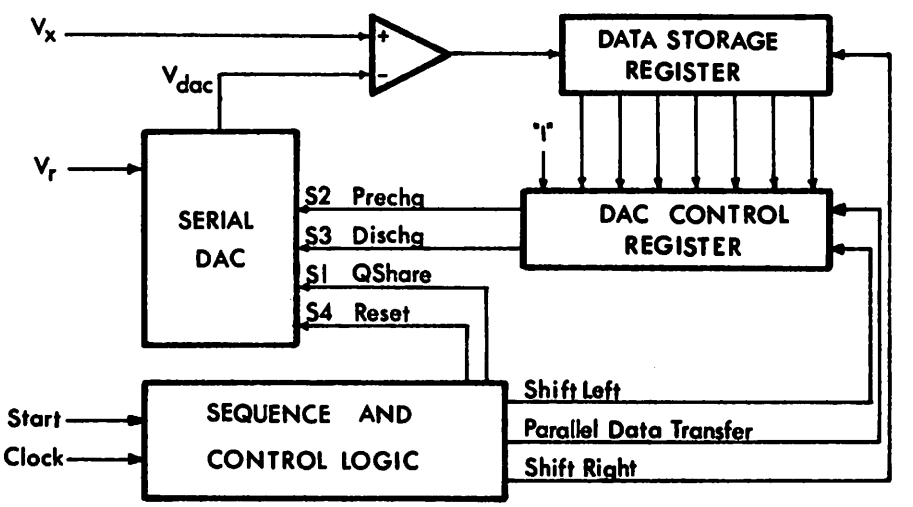


Fig. 5.6. Successive Approximation ADC Block Diagram.

Table 5.1. TWO-CAPACITOR DAC CONVERSION SEQUENCE

STEP	V_1/V_R	V_2/V_R	Switch Closures
0	0	0	S_3, S_4
1	d_1	0	$S_2(S_3)^*$
2	$d_1/2$	$d_1/2$	S_1
3	d_2	$d_1/2$	$S_2(S_3)$
4	$d_1/4 + d_2/2$	$d_1/4 + d_2/2$	S_1
.			
.			
K	$\sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}}$	$\sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}}$	S_1

*Figures in parenthesis represent alternative switch closures depending upon the value of the bit under consideration.

Table 5.2. TWO-CAPACITOR ADC CONVERSION SEQUENCE

Iteration No	DAC INPUT WORD						COMPARATOR OUTPUT
	d_1	d_2	d_3		d_{N-1}	d_N	
1	1	-	-	-	-	-	a_N
2	1	a_N	-	-	-	-	a_{N-1}
3	1	a_{N-1}	a_N	-	-	-	a_{N-2}
.	.	.	.	.	.	.	. .
N	1	a_2	a_3	.	a_{N-1}	a_N	a_1

unknown voltage V_X determines the true value of the bit, which is stored in the DSR. The next most significant bit a_{N-1} is determined by forming the word $(d_{N-1},d_N) = (1,a_N)$ in the DCR and performing a two-bit D/A conversion, which determines a_{N-1}. The value is stored in the DSR, and the process continues in this fashion. Thus, to determine the bit a_{j+1}, a (j+1)-bit word is formed in the DCR by adding a "1" as the LSB (d_{j+1}) to the previously encoded j-bit word from the DSR. A (j+1)-bit D/A conversion establishes the value of a_{j+1}. The conversion process is described schematically in Table 5.2. Figure 5.7 illustrates a four-bit A/D conversion for $V_X/V_R = 13/16$. The total conversion time for an N-bit A/D conversion is:*

$$T_{ADC} = \sum_{k=1}^{N} (2KT_Q+T_C) \qquad (5.14)$$

where T_Q = capacitor charging time,

and T_C = comparator settling time.

Summation of the series in (5.14) yields

$$T_{ADC} = N(N+1)T_Q + NT_C \; . \qquad (5.15)$$

*The actual number of steps can be reduced by two by condensing the first (1 bit) and second (2 bit) D/A conversions into a single 2 bit conversion. The required modification in hardware to remove this redundancy is minimal.

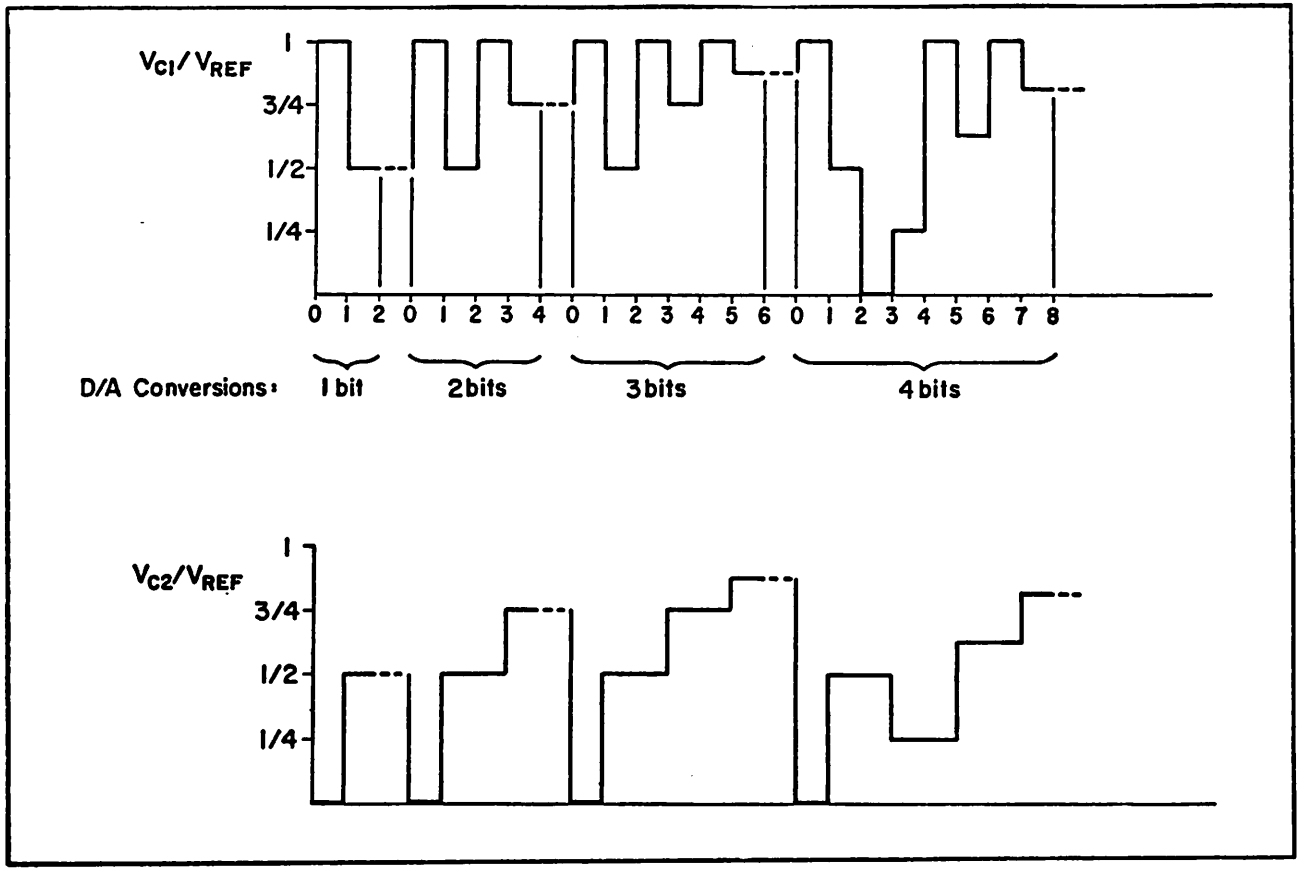


Fig. 5.7. Illustration of A/D Conversion Sequence for the Two-capacitor Converter.

5.3. Multiple Capacitor Converters

A study was made to determine the possible tradeoff between conversion time and the number of capacitors used in the converter. Two possibilities are apparent: multiple equal-weight capacitors and binary-weighted capacitor converters. In this section the first possibility is examined. The binary-weighted case is studied in the following section.

A. Three-Capacitor Converter

Examination of the two-capacitor DAC described in the previous section indicates that a substantial reduction in conversion time can be obtained by precharging a third capacitor in accordance with the next bit in the sequence while the charge-sharing step between the first two capacitors is taking place. In this manner a K bit D/A conversion is realized in (K+1) steps instead of 2K steps for the two-capacitor case. Figure 5.8 shows the capacitor arrangement for the new DAC, and Table 5.3 illustrates the conversion sequence. The specific case for the input word 1101, which corresponds to the fraction $(13/16)V_R$, is shown in Table 5.4. The conversion takes 5 steps compared with 8 in the process of Fig. 5.5.

An ADC can be built around the three capacitor DAC in the same manner as shown in Fig. 5.6. The only modification is the addition of a routing circuit at the output of the DAC control register (DCR) to precharge the odd-numbered bits onto C_1 and the even-numbered bits onto C_3. The conversion sequence is described in detail in Table 5.5 for the general case, and on Table 5.6 for the case $V_X/V_R = 13/16$. The total number of steps for an N-bit A/D conversion is:*

*Cf. footnote on p. .

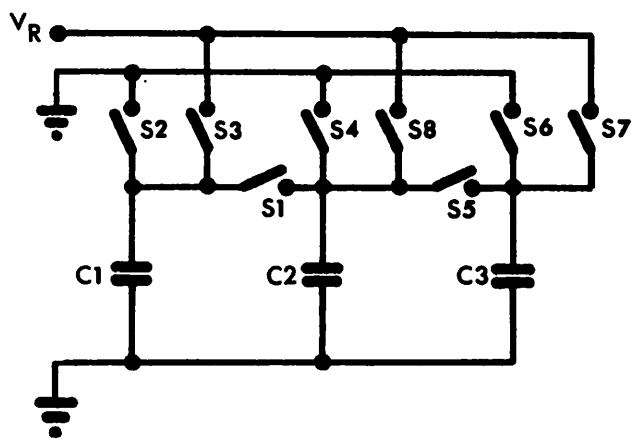


Fig. 5.8. Three-capacitor Serial DAC.

Table 5.3. THREE-CAPACITOR DAC CONVERSION SEQUENCE

STEP	V_1/V_R	V_2/V_R	V_3/V_R	Switch Closures
0	0	0	0	S_2, S_4, S_6
1	d_1	0	0	$S_3(S_2)^*$
2	$d_1/2$	$d_1/2$	d_2	S_1, $S_7(S_6)$
3	d_3	$d_1/4 + d_2/2$	$d_1/4 + d_2/2$	S_5, $S_3(S_2)$
4	$d_1/8 + d_2/4 + d_3/2$	$d_1/8 + d_2/4 + d_3/2$		S_1, $S_7(S_6)$
.				
.				
.				
K+1	. . .	$\sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}}$	. . .	$S_1(S_5)$

*Figures in parenthesis represent alternative switch closures.

Table 5.4. FOUR-BIT D/A CONVERSION EXAMPLE INPUT WORD: 1101

STEP	V_1/V_R	V_2/V_R	V_3/V_R
0	0	0	0
1	1 (LSB)	0	0
2	1/2	1/2	0 (NLSB)
3	1 (NMSB)	1/4	1/4
4	5/8	5/8	1 (MSB)
5	-	13/16	13/16

Table 5.5. THREE-CAPACITOR ADC CONVERSION SEQUENCE

STEP	DAC INPUT WORD	V_1/V_R	V_2/V_R	V_3/V_R	COMPARATOR OUTPUT
0	1	0	0	0	
1		①*	0	0	
2		1/2	1/2	0	a_N
3	$1a_N$	①	0	0	
4		1/2	1/2	(a_N)	
5		1/2	$\frac{a_N}{2} + \frac{1}{4}$	$\frac{a_N}{2} + \frac{1}{4}$	a_{N-1}
6	$1a_{N-1}a_N$	①	0	0	
7		1/2	1/2	(a_{N-1})	
8		(a_N)	$\frac{a_{N-1}}{2} + \frac{1}{4}$	$\frac{a_{N-1}}{2} + \frac{1}{4}$	
9		$(\frac{a_N}{2} + \frac{a_{N-1}}{4} + \frac{1}{8})$	$(\frac{a_N}{2} + \frac{a_{N-1}}{4} + \frac{1}{8})$	$(\frac{a_{N-1}}{2} + \frac{1}{4})$	a_{N-2}
.					
.					
.					
$\frac{N}{2}(N+3)$		. . .	$(\sum_{i=2}^{N} \frac{a_i 2^i}{2^{N+1}}) + \frac{1}{2^N}$		a_N

*Encircled entries indicate precharges.

Table 5.6. THREE CAPACITOR ADC CONVERSION EXAMPLE: $V_X/V_R = 13/16 = 1101$

STEP	DAC INPUT	V_1/V_R	V_2/V_R	V_3/V_R	COMPARATOR OUTPUT
0		0	0	0	
1	1	①	0	0	
2		1/2	1/2	0	$a_4 = 1$
3	11	①	0	0	
4		1/2	1/2	①	
5		1/2	3/4	3/4	$a_3 = 1$
6	111	①	0	0	
7		1/2	1/2	①	
8		①	3/4	3/4	
9		7/8	7/8	3/4	$a_2 = 0$
10	1011	①	0	0	
11		1/2	1/2	⓪	
12		①	1/4	1/4	
13		5/8	5/8	①	
14		5/8	13/16	13/16	$a_1 = 1$

$$T_{ADC} = \sum_{K=1}^{N} [(K+1)T_Q + T_C] \quad . \tag{5.16}$$

Carrying out the summation of the series:

$$T_{ADC} = \frac{N}{2}(N+3)T_Q + NT_C \quad . \tag{5.17}$$

For large N the number of charging steps is reduced by approximately a factor of 2 with respect to the two-capacitor converter.

B. Converter with an Unlimited Number of Equal-Weight Capacitors

To establish the number of equal-weight capacitors that would be required to perform an A/D conversion in a minimum number of steps, the charge-redistribution conversion process is re-examined in Table 5.7. The D/A conversion which is required to establish each of the bits is shown as a column, and each row represents a precharge and charge-sharing step. The upper entry at each step of a conversion represents a DAC input bit, and the lower entry at the bottom square of each column identifies the bit which is established at the end of that particular D/A conversion. Table 5.8 represents the same process with those DAC input bits which are unknown at any step in the process represented by an entry "X". These entries require that both a 1 and a 0 be used to generate all possible bit combinations up to the point where the necessary input bits are known. For 10 bits it is seen that 16 different bit combinations are required for the 9th and 10th D/A conversion. Taking into account the fact that at the end of each charge-sharing step two capacitors have the same voltage levels (i.e., the requirements of

Table 5.7. A/D CONVERSION PROCESS FOR AN UNLIMITED NUMBER OF EQUAL-WEIGHT CAPACITORS

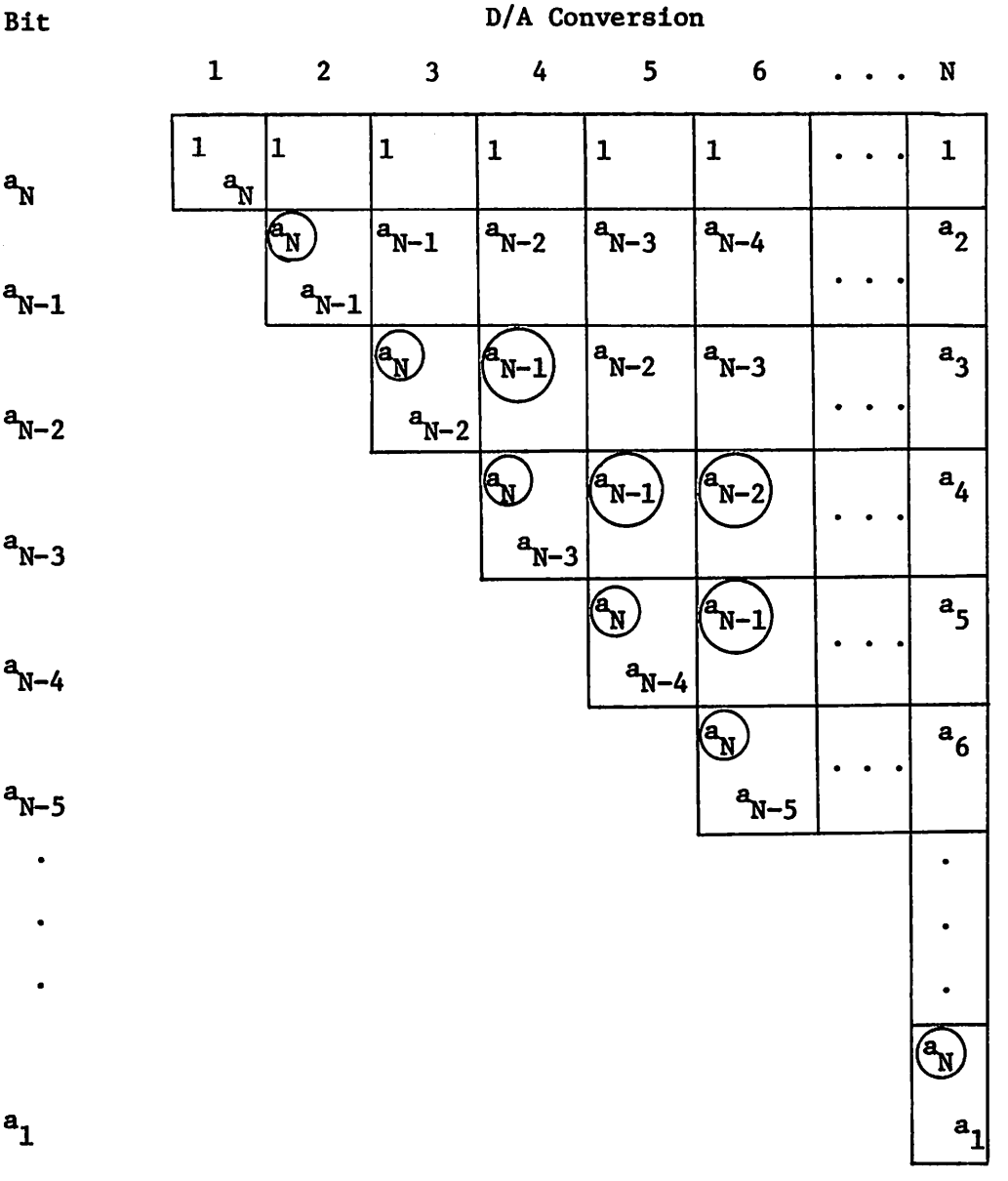


Table 5.8. TABULATION OF THE REQUIRED NUMBER OF CAPACITORS FOR A 10 BIT A/D CONVERSION

Bit	D/A Conversion									
	1		1	1	1	1	1	1	1	1
a_{10}	a_{10}									
		a_{10}	X	X	X	X	X	X	X	X
a_9		a_9								
			a_{10}	a_9	X	X	X	X	X	X
a_8			a_8							
				a_{10}	a_9	a_8	X	X	X	X
a_7				a_7						
					a_{10}	a_9	a_8	a_7	X	X
a_6					a_6					
						a_{10}	a_9	a_8	a_7	a_6
a_5						a_5				
							a_{10}	a_9	a_8	a_7
a_4							a_4			
								a_{10}	a_9	a_8
a_3								a_3		
									a_{10}	a_9
a_2									a_2	
										a_{10}
a_1										a_1

two columns with the same number of unknown bits are satisfied by one set of capacitors), the total number of capacitors is 71. Subtracting from this total the number of capacitors which become available after the D/A conversions corresponding to the MSB's have been concluded, the total number of capacitors is still 60. No straight-forward way is apparent at this point to implement further reductions in the capacitor count of any significance.

A study of a converter consisting of four capacitors was carried out. The reduction in conversion time for an A/D conversion is only about 10% compared with the three capacitor case for 10 bits. Therefore, no particular advantage is found for equal-weight capacitor approaches with more than three capacitors.

5.4. Binary-Weighted Capacitor Converter

Examination of the three-capacitor converter case indicates that significant reductions in conversion time are obtained by simultaneously precharging several bits before a charge redistribution. In order to achieve the proper weighing of the bits the capacitor values must be chosen so that $\sum_{i=0}^{N} C_i = 2^N C$, where C is the unity-weight capacitor, and $C_i = 2^{i-1} C$ for $i \geq 1$. This constrains the terminating capacitor C_o to the value $C_o = C$. The capacitor arrangement is shown in Fig. 5.9. To perform a D/A conversion the largest capacitor, C_N, is precharged according to the MSB, d_N. Each consecutively smaller capacitor is precharged with the corresponding bit, down to C_1 which is precharged with the LSB, d_1. In all cases the terminating capacitor C_o is loaded with a dummy bit $d_o = 0$. After precharging, the charge in the circuit is

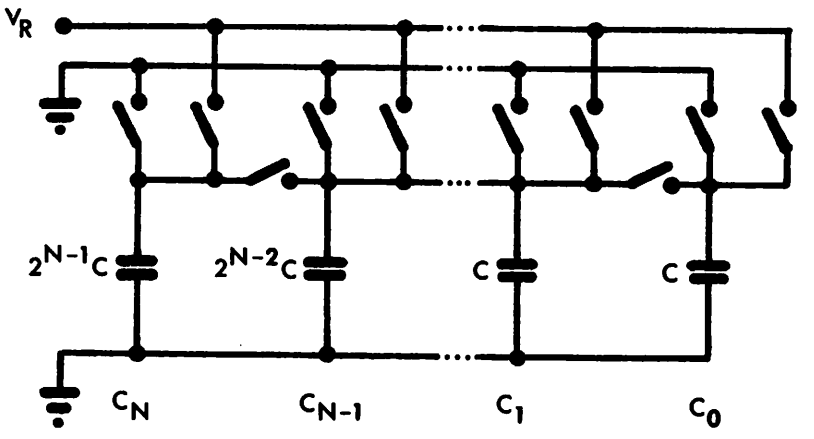


Fig. 5.9. Binary-weighted Capacitor DAC.

$$Q(0) = \sum_{i=0}^{N} d_i C_i V_R \quad . \tag{5.18}$$

The charge in all capacitors is redistributed to obtain a final voltage V(f) so that

$$Q(f) = V(f) \sum_{i=0}^{N} C_i \quad . \tag{5.19}$$

Replacing the value of each capacitor in terms of the unity-weight capacitance, C, (5.19) becomes

$$Q(f) = 2^N CV(f). \tag{5.20}$$

From (5.18) and Q(f) = Q(0), the final voltage is:

$$V(f) = \sum_{i=1}^{N} \frac{d_i 2^{i-1}}{2^N} V_R \quad , \tag{5.21}$$

or

$$V(f) = \sum_{i=1}^{N} \frac{d_i 2^i}{2^{N+1}} V_R,$$

corresponding to an N-bit D/A conversion performed in 2 steps.

The block diagram of a successive approximation ADC is shown in Fig. 5.10. The A/D conversion sequence starts with the MSB, a_N, and is performed in 2N steps: N pre-charges and N charge-shares. As usual, at each step it is assumed that the bit under consideration is a "1", and the comparator output establishes the true value of the bit. Table 5.9 lists the conversion sequence for N bits.

To examine the tradeoff between the number of capacitors and

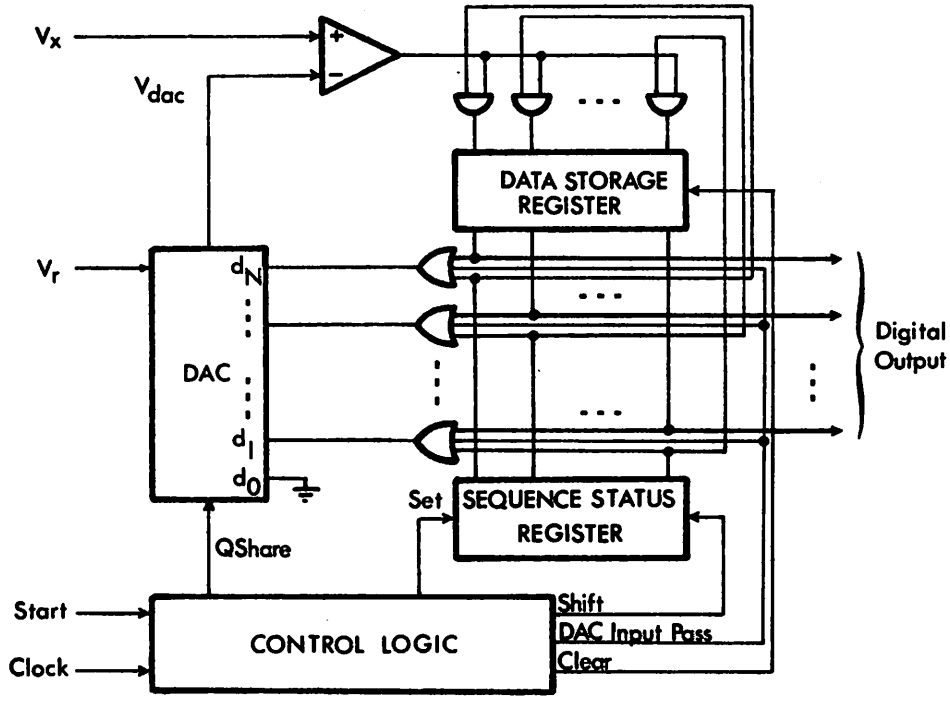


Fig. 5.10. Block Diagram for Successive Approximation ADC with Binary-weighted Capacitors.

Table 5.9. A/D CONVERSION SEQUENCE FOR BINARY-WEIGHTED CAPACITOR CONFIGURATION

Iteration	DAC Input Bits						Comparator Output
	d_N	d_{N-1}	d_{n-2}	. . .	d_2	d_1	
1	1	0	0	. . .	0	0	a_N
2	a_N	1	0	. . .	0	0	a_{N-1}
3	a_N	a_{N-1}	1	. . .	0	0	a_{N-2}
.							.
.							.
.							.
.							.
N	a_N	a_{N-1}	a_{N-2}	. . .	a_2	1	a_1

Second pre-charge:

$$Q_2(0) = [\sum_{i=1}^{J} 2^{i-1}C + C]V(1)$$

$$+ \sum_{i=J+1}^{K} d_{K-J+i} 2^{i-1}C\, V_R \qquad (5.25)$$

$$= 2^J C\, V(1) + \sum_{i=J+1}^{K} d_{K-J+i} 2^{i-1}C\, V_R . \qquad (5.26)$$

After charge-sharing:

$$V(2) = \frac{1}{2^K} [2^J \sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}}\, V_R] +$$

$$\frac{1}{2^K} [\sum_{i=J+1}^{K} d_{K-J+i} 2^{i-1}C\, V_R] \qquad (5.27)$$

$$= \sum_{i=1}^{K} \frac{d_i 2^i}{2^{2K-J+1}} V_R + \sum_{\ell=K+1}^{N} d_\ell \frac{2^{\ell-K}}{2^{2K-J+1}}\, V_R , \qquad (5.28)$$

where $\ell \equiv K-J+i$.

Using the fact that $2K-J = N$, the final voltage can be expressed as:

$$V(2) = \sum_{i=1}^{N} d_i \frac{2^i}{2^{N+1}} V_R , \qquad (5.29)$$

as in Eq. (5.21). Since K bits are converted simultaneously an N-bit D/A conversion is completed in 2N/K steps.*

*When the fraction 2N/K does not correspond to an even number, the actual number of charging steps is the nearest larger even number.

The tradeoff in the analog to digital conversion process can be established in a similar way. For an N-bit conversion performed with a (K+1) binary-weighted capacitor converter, N > K, it can be shown that if two integers r and q are defined as follows:

$$N = qK + r \quad (r < K) \tag{5.30}$$

The total number of steps in the A/D conversion is:

$$T_{ADC} = (N+r)(q+1)T_Q + NT_C. \tag{5.31}$$

In summary, two basic types of charge-redistribution convertion approaches have been developed which appear to be compatible with existing MOS integrated circuit technologies. The first type of converter consists of grounded capacitors of equal value. Within this group only the two and three-capacitor cases merit further consideration. The second class of converters is based on a binary-weighted grounded capacitor arrangement which exhibits a promising tradeoff between conversion speed and the number of capacitors used. A binary-weighted capacitor approach which promises yet improved performance characteristics is under study [23]. For this reason, the development of this class of converters is not pursued any further. The chapters which follow are directed toward the design and fabrication of a monolithic prototype of the equal-weight capacitor charge-redistribution conversion technique.

CHAPTER VI

ERROR ANALYSIS AND SPEED CONSIDERATIONS

In the ideal converters discussed thus far the output voltage resulting from a K-bit digital-to-analog conversion corresponds to Eq. (5.13):

$$V_K = \sum_{i=1}^{K} \frac{d_i 2^i}{2^{K+1}} \; V_R. \tag{6.1}$$

In practical converters, however, a non-zero error voltage V_ε exists, and the actual converter output is of the form:

$$V(K) = V_K + V_\varepsilon \; . \tag{6.2}$$

The primary sources of the error voltage are: feedthrough voltages ($V_{f\varepsilon}$), capacitor mismatches ($V_{m\varepsilon}$), voltage and temperature variations of capacitance ($V_{V\varepsilon}$ and $V_{T\varepsilon}$).

In the case of an A/D converter the input offset of the voltage comparator (V_{OS}) will contribute an additional error component. The total error voltage for an analog-to-digital conversion can be expressed as a sum:

$$V_\varepsilon = V_{f\varepsilon} + V_{m\varepsilon} + V_{V\varepsilon} + V_{T\varepsilon} + V_{OS} \; . \tag{6.3}$$

The maximum value of V_ε is the worst case conversion error which, as specified in Eq. (1.12), must be kept below the converter resolution. Thus, $\max|V_\varepsilon| < V_R/2^{N+1}$ for N bits.

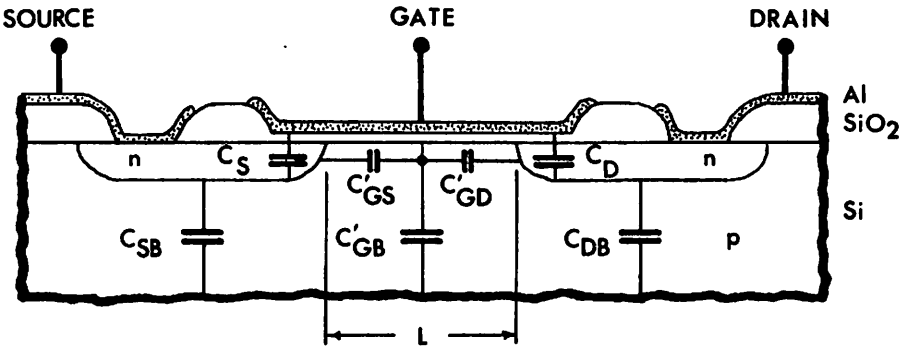
The error voltage components are studied in this chapter, and appropriate design measures are described to reduce the total error voltage in the conversion process. It is found that the ratio of

channel capacitance of the MOS transistor switches to the size of the charge-redistribution capacitors is a determining factor with respect to feedthrough error voltage. Moreover, the relative size of the transistor switches to the charge-redistribution capacitors determines the conversion speed. A speed-accuracy tradeoff therefore exists, and analysis indicates that the product of feedthrough error voltage ($V_{f\varepsilon}$) and capacitor charging time (T_{charge}) is proportional to the square of the channel length of the MOS transistor switches. Smaller channel lengths, therefore, will result in increased conversion speed and reduced feedthrough error voltages.

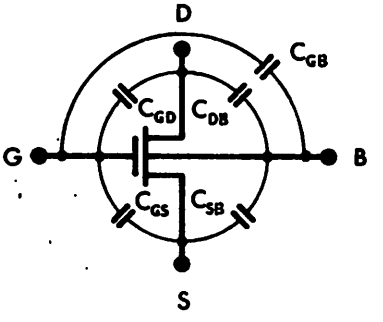
6.1. Feedthrough Error Voltages

Figure 6.1 shows a cross-section of an n-channel MOS transistor switch and the different capacitive components of the device [24]. With respect to the circuit in Fig. 6.2, the nonlinear capacitances associated with the charge-sharing transistor introduce an asymmetry into the circuit which results in a net feedthrough error voltage on capacitors C_1 and C_2 after charge redistribution. The feedthrough error voltage can be reduced by reading the capacitor voltages only after the gate voltage V_G has been returned to zero. In this manner the negative falltime feedthrough partially cancels the positive risetime feedthrough, but an exact cancellation is not achieved due to the nonlinearity of the transistor capacitances.

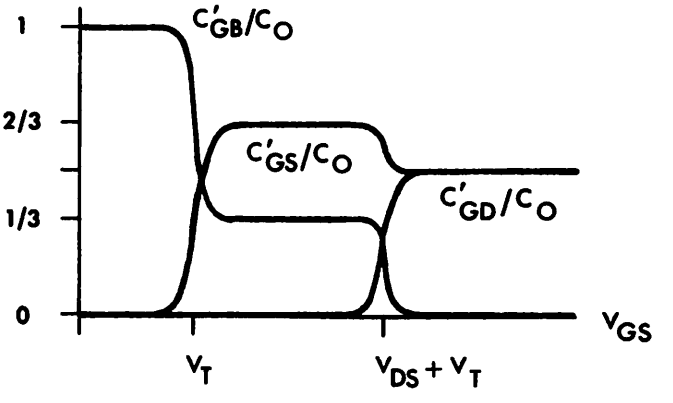
The worst-case feedthrough error voltage for a charge redistribution step, $V_{f\varepsilon 1}$, can be estimated by considering the condition in which the asymmetry in the circuit voltage levels is a maximum. This occurs when $V_1(0) = V_R$ and $V_2(0) = 0$. A piecewise



(a)



(b)



(c)

Fig. 6.1(a). Cross-section of MOS Transistor.

(b). Capacitive Components of an MOS Transistor.

(c). Nonlinear MOS Transistor Capacitive Components.

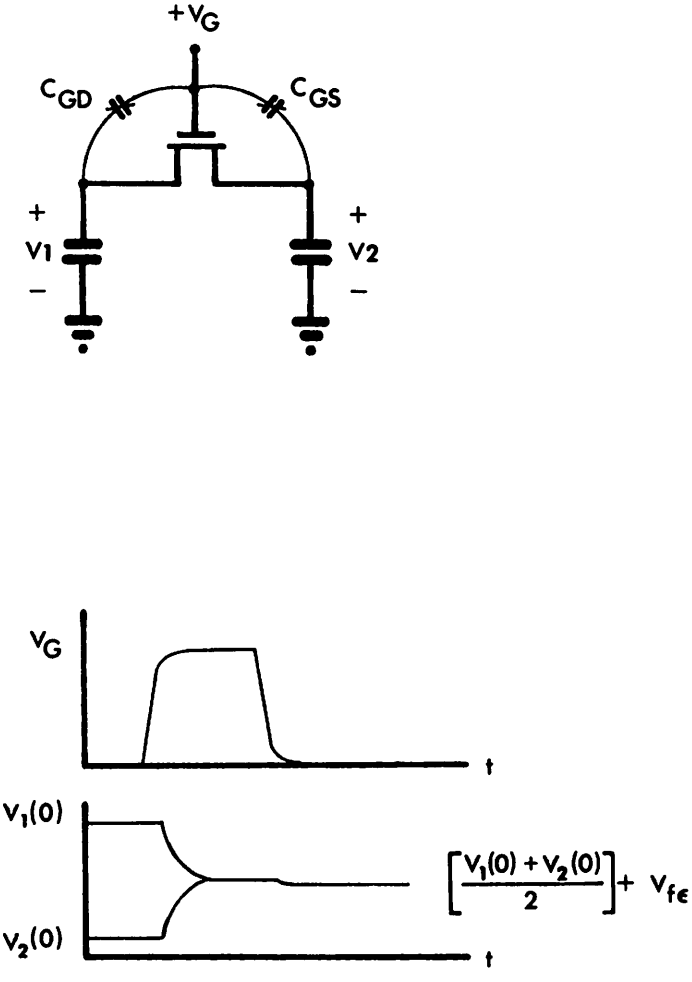


Fig. 6.2. Feedthrough Error Voltage During Charge Redistribution.

linear analysis can be made by use of the capacitance model shown in Fig. 6.3. This approximate analysis predicts a worst-case feedthrough voltage of the form:

$$V_{f\varepsilon 1} \cong - \frac{C_0}{2C} f(V), \tag{6.4}$$

where C_0 is the MOSFET channel capacitance, $C_0 = \frac{\varepsilon_{OX}}{t_{OX}} LW$ for a channel length L, channel width W, and oxide thickness t_{OX}. In this equation $C = C_1 = C_2$, and f(V) is a voltage function of approximately unity magnitude. For $V_R = 5V$, $|V_G| = 10V$, $V_{SS} = -5V$, $t_{OX} = 0.1\ \mu m$, $L = 7.5\ \mu m$, $W/L = 10$ and $C = 25$ pF, the resulting error voltage is approximately -5mV, in close agreement with computer simulations using the program ISPICE [25]. Equation (6.4) predicts that the ratio of the channel capacitance of the charge-sharing transistor to the sum of capacitors C_1 and C_2 determines the magnitude of the feedthrough error voltage $V_{f\varepsilon 1}$.

In addition to the feedthrough error introduced during the charge redistribution step, the precharge transistors also cause a feedthrough error component. As shown in Fig. 6.4, after the capacitor has been charged to the voltage V_B, a negative feedthrough voltage is introduced during the fall time of V_G. The worst-case condition now corresponds to the discharge of capacitor C to ground (V_B=0), since this represents the largest swing of the gate-to-source voltage V_{GS}. The error voltage is approximately given by:

$$V_{f\varepsilon 2} \cong - \frac{C_0/2}{C} |V_G| . \tag{6.5}$$

For the parameters given above the resulting error is $V_{f\varepsilon 2} \cong -40$mV. The magnitude of this error is clearly unacceptable for high accuracy

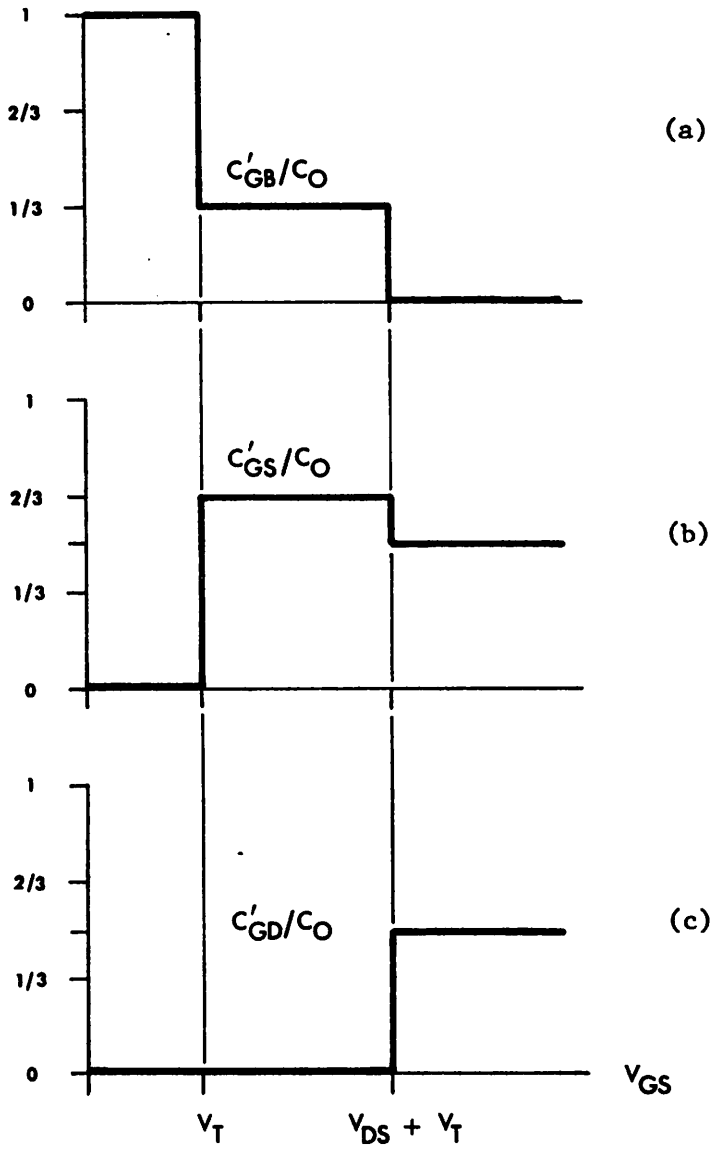


Fig. 6.3. Piecewise Linear Capacitance Model

(a). Gate-bulk capacitance

(b). Gate-source capacitance

(c). Gate-drain capacitance

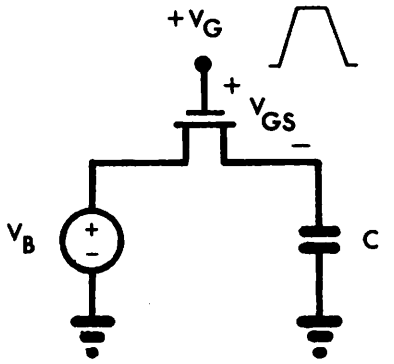


Fig. 6.4. Feedthrough Error Voltage During Precharge.

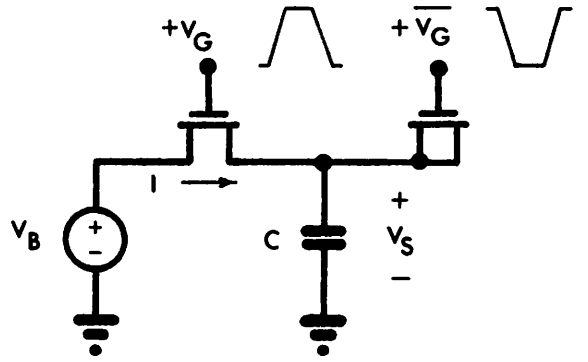


Fig. 6.5. Charge-cancelling Device.

converter realizations. However, the addition of a "charge-cancelling" device [26], as shown in Fig. 5.5, reduces the net precharge feedthrough voltage to approximately the same level as the feedthrough error voltage obtained during charge redistributions.

The charge-cancelling transistor is a dummy device with the source and drain short-circuited to prevent dc current flow and with one-half the channel area of the precharge device. The voltage applied at the gate of the charge-cancelling device is the complement of the precharge transistor gate voltage, V_G.

The total feedthrough error voltage for one precharge and one redistribution steps is

$$V_{f\varepsilon(1)} \cong \frac{V_{f\varepsilon 2}}{2} + V_{f\varepsilon 1}. \tag{6.6a}$$

At the end of a K-bit D/A conversion, the cummulative feedthrough error voltage is:

$$V_{f\varepsilon} = \frac{V_{f\varepsilon}(1)}{2^{K-1}} + \ldots + \frac{V_{f\varepsilon}(K-1)}{2} + V_{f\varepsilon}(K). \tag{6.6b}$$

Thus, the maximum total feedthrough error voltage is less than twice the worst case error voltage estimated in (6.4).

6.2. Capacitor Mismatch Error Consideration

For two nominally identical capacitors C_1 and C_2 initially charged to voltages $V_1(0)$ and $V_2(0)$ respectively, the resulting voltage after charge redistribution is:

$$V(f) = \frac{C_1}{C_1+C_2} V_1(0) + \frac{C_2}{C_1+C_2} V_2(0). \tag{6.7}$$

Let $m_1 = C_1/(C_1+C_2)$ and $m_2 = C_2/(C_1+C_2)$, where nominally $m_1 = m_2 = m = 1/2$. Following the sequence described by Eqs. (5.11) through (5.13), the capacitor voltages at the end of K precharge-redistribution steps is:

$$V_K = m_1 V_R [\sum_{i=1}^{K} m_2^{K-i} b_i] \quad . \tag{6.8}$$

Assume a capacitance mismatch $\Delta C \equiv C_2 - C_1$, and let $C = (C_1+C_2)/2$. Then,

$$C_1 = C - \frac{\Delta C}{2} \quad , \tag{6.9}$$

and

$$C_2 = C + \frac{\Delta C}{2} \quad .$$

The mismatch is reflected on the capacitor ratios as:

$$\Delta m_1 = - \frac{\Delta C}{4C} \quad ,$$

and (6.10)

$$\Delta m_2 = + \frac{\Delta C}{4C} \quad .$$

The voltage difference caused by the capacitor mismatch on V_K can be obtained from (6.8):

$$\frac{\Delta V_K}{V_R} = \Delta m_1 \sum_{i=1}^{K} m_2^{K-i} b_i + \Delta m_2 \sum_{i=1}^{K} (K-1) m_2^{K-i-1} b_i \quad . \tag{6.11}$$

Since $\Delta m_1 = -\Delta m_2 = -\Delta m$, and $m_1 = m_2 = 1/2$,

$$\frac{\Delta V_K}{V_R} = \Delta m \sum_{i=1} \frac{(K-i-1)}{2^K} \, 2^i b_i \quad . \tag{6.12}$$

Expanding the summation in (6.12) the error voltage becomes:

$$\frac{\Delta V_K}{V_R} = \Delta m\left[\frac{K-2}{2^{K-1}} b_1 + \frac{K-3}{2^{K-2}} b_2 + \ldots \frac{1}{2^2} b_{K-2} + 0 - b_K \right] . \quad (6.13)$$

The worst cases occur when $b_K = 1$ with $b_j = 0$ for $j \neq K$, and when $b_K = 0$ with $b_j = 1$ for $j \neq K$. The worst-case mismatch error voltage is then,

$$\frac{\Delta V_K}{V_R} = \pm \Delta m. \quad (6.14)$$

Taking ΔC as the standard deviation of the distribution of the capacitance mismatch, $\Delta C \equiv \sigma_C$, (6.14) becomes in view of Eqs. (6.10) and (4.10):

$$\frac{\Delta V_K}{V_R} = \pm \frac{\sqrt{2}}{4} \frac{\sigma_X}{L_C} \quad , \quad (6.15)$$

where σ_X is the standard deviation edge uncertainty as modelled in Chapter IV, and L_C is the length of one side of a square capacitor.

Another precharge sequence that could be used in performing a K-bit D/A conversion consists of alternatively precharging the bits on C_1 and C_2. The capacitor voltages for such a sequence progress as follows:

$$\left.\begin{aligned} \frac{V(1)}{V_R} &= m_1 b_1 \\ \frac{V(2)}{V_R} &= m_2 b_2 + m_1^2 b_1 \\ \frac{V(3)}{V_R} &= m_1 b_3 + m_2^2 b_2 + m_1^2 m_2 b_1 \\ \text{and} \quad \frac{V(K)}{V_R} &= \sum_{i=1}^{K} m_1^{x_i} m_2^{y_i} b_i \end{aligned}\right\} \quad (6.16)$$

For K even it can be shown that the exponents x_i and y_i are related as follows:

$$\text{for i even:} \quad \begin{aligned} y_i - x_i &= 1 \\ y_i + x_i &= K-i+1 \end{aligned} \tag{6.17}$$

$$\text{for i odd:} \quad \begin{aligned} y_i - x_i &= -2 \\ y_i + x_i &= K-i+1 \end{aligned} \tag{6.18}$$

The error voltage due to a mismatch Δm is:

$$\frac{\Delta V_K}{V_R} = \{\sum_{i=1}^{K} [y_i - x_i] \frac{2^i}{2^k} b_i \} \Delta m. \tag{6.19}$$

Expanding the summation by use of (6.17) and (6.18), ΔV_K becomes:

$$\frac{\Delta V_K}{V_R} = [- \frac{4}{2^K} b_k + \frac{4}{2^K} b_2 - \frac{16}{2^K} b_3 + \frac{16}{2^K} b_4 - + \ldots - b_{K-1} + b_K]\Delta m. \tag{6.20}$$

The worst-case conditions result when either all odd bits are "1" and all even bits are "0" or vice versa. Then,

$$\frac{\Delta V_K}{V_R} \cong \pm \frac{4}{3} \Delta m. \tag{6.21}$$

Comparison with (6.14) indicates that the first precharge scheme is somewhat less sensitive to capacitor mismatch induced errors than the alternating capacitor precharge sequence.

The capacitor mismatch error can be compensated by performing two A/D conversions so that on the first conversion all bits are precharged onto capacitor C_1, and on the second conversion the bits are precharged onto C_2. The resulting mismatch errors are equal in magnitude and opposite in sign. The encoded digital words which

result from the two conversions can then be added and divided by two to realize the mismatch error cancellation. This error cancellation method requires approximately twice the conversion time of a single conversion.

One further consideration with regard to mismatch errors is the effect of oxide thickness gradients for large capacitor areas. A symmetrical layout of the capacitors about a common centroid minimizes the effect of long range (across-the-chip) oxide gradients. Such a layout requires that the two capacitors be constructed as several small capacitors connected in parallel. It would be expected that the mismatch uncertainty for the resulting multiple capacitor structure should be higher than that for two single capacitors of the same size. However, the analysis of Appendix C indicates that on a first-order basis the edge mismatch uncertainties for both structures are comparable.

To summarize the results of this section, the worst-case mismatch error voltage for an edge uncertainty σ_x is given by Eq. (6.15). Thus,

$$V_{m\varepsilon} \cong \pm \frac{\sqrt{2}}{4} \frac{\sigma_x}{L_C} \tag{6.22}$$

6.3. Effects of Voltage and Temperature Coefficients of Capacitance

To characterize the error voltage due to capacitor nonlinearities let $\alpha = \gamma_V^C \equiv \frac{1}{C} \frac{\partial C}{\partial V}$, where γ_V^C is the effective voltage coefficient of capacitance. The charge-sharing capacitors then have the form:

$$C_1 = C(1+\alpha V_1),$$

and (6.23)

$$C_2 = C(1+\alpha V_2).$$

When the capacitors C_1 and C_2 are precharged to voltages $V_1(0)$ and $V_2(0)$ respectively the initial circuit charge is:

$$Q(0) = C(1+\alpha V_1(0))V_1(0) + C(1+\alpha V_2(0))V_2(0) \ . \tag{6.24}$$

After charge-redistribution to a final voltage V(f) the circuit charge becomes:

$$Q(f) = 2C(1+\alpha V(f))V(f). \tag{6.25}$$

Equating (6.24) and (6.25) and rearranging terms we have:

$$[1 + \alpha V(f)]V(f) = \frac{1}{2} (V_1(0)+V_2(0)) + \frac{1}{2} \alpha(V_1^2(0)+V_2^2(0)). \tag{6.26}$$

Solving for V(f):

$$V(f) = \frac{1}{2\alpha} [-1 \pm \sqrt{1 + 2\alpha[(V_1(0)+V_2(0)) + \alpha(V_1^2(0)+V_2^2(0))]} \ ] \ . \tag{6.27}$$

Expanding the terms under the radical sign to second order, the final voltage is:

$$V(f) \cong \frac{V_1(0)+V_2(0)}{2} + \frac{\alpha}{4} (V_1(0)-V_2(0))^2. \tag{6.28}$$

The worst-case deviation occurs when $V_1(0) = V_R$ and $V_2(0) = 0$ or vice versa. Then,

$$V(f) \cong \frac{V_1(0)+V_2(0)}{2} + \frac{\alpha}{4} V_R, \tag{6.29}$$

or $\quad V_{V\varepsilon} \cong \frac{1}{4} \gamma_V^C V_R.$

The results of Appendix B indicate that in order to minimize this voltage error component a heavy doping of the lower capacitor plate

must be insured. For a doping concentration of $5 \times 10^{20} cm^{-3}$ $\gamma_V^C < 10$ ppm/V. Hence, for $V_R = 5V$ the resulting error voltage due to capacitor nonlinearities is clearly negligible.

Temperature differences between the capacitors also introduce an error voltage. Because γ_T^C is very small ($\cong$ 20 ppm/°C), temperature gradients of a few degrees have a minimal effect on the capacitor voltages after redistribution.

6.4. Comparator Offset Voltage

Comparator input offset voltate contributes an additive error component to the DAC output voltage. As shown in Fig. 6.6, the differential input voltage to the comparator is

$$\Delta V_{in} = V_X + V_{OS} - V_K \quad . \tag{6.30}$$

V_X is the unknown analog voltage, V_{OS} is the comparator offset voltage, and V_K is the DAC output voltage after K precharge-redistribution steps. The effect of V_{OS} is to reduce the effective value of V_K, so that the DAC output voltage appears to be

$$V(K) = V_K - V_{OS},$$

and

$$\Delta V_{in} = V_X - V(K) \quad . \tag{6.31}$$

MOS differential amplifiers exhibit offset voltages in the order of 100 mV [27]. With respect to a 5 volt reference level this represents an error of 2%.

Several offset compensation schemes have been proposed [28]. The approach of Poujors, et. al. [29] is shown in Fig. 6.7. in a

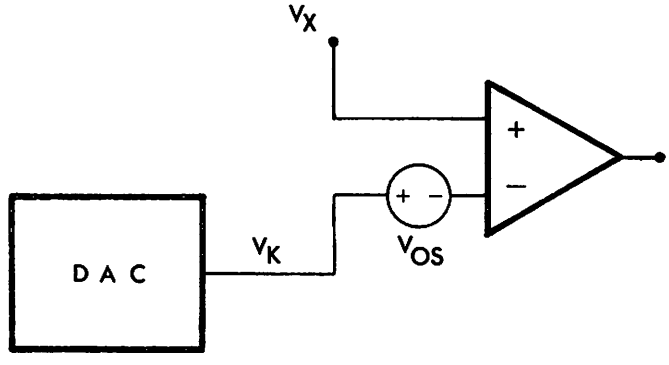


Fig. 6.6. Effect of Comparator Offset on Conversion Error.

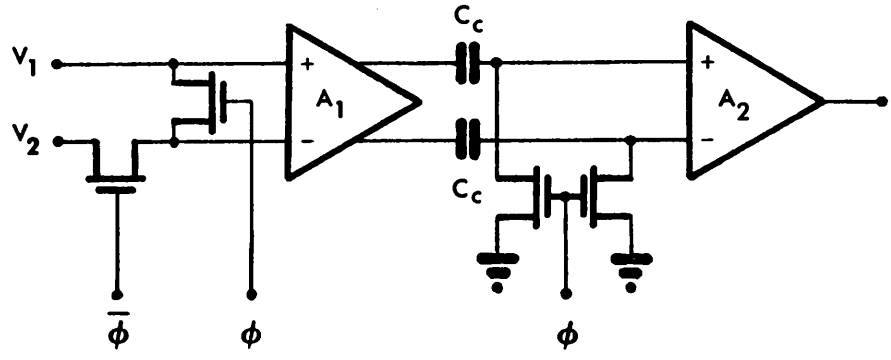


Fig. 6.7. Circuit for Offset Concellation by Storage of the Offset Voltage.

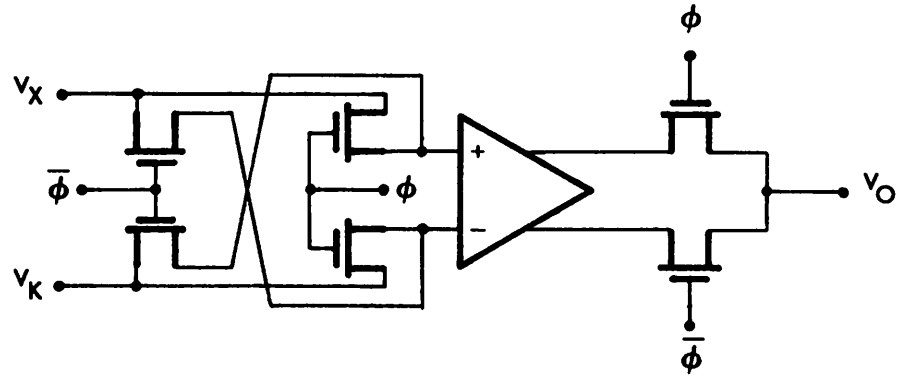


Fig. 6.8. Circuit for Offset Cancellation by Subtraction.

modified form. The amplifier consists of a cascade of two moderate gain stages, $A_1 \simeq A_2 \simeq 20$. When the pulse ϕ goes high the two input terminals of A_1 are connected to a common mode voltage voltage V_1, and the input terminals of A_2 are grounded. Capacitors C_C are charged to the differential output voltage of the first stage, $A_1 \cdot V_{OS1}$. When ϕ is returned to zero the capacitors remain charged and level shift the output voltage of A_1 thereby cancelling the offset voltage V_{OS1}. The amplifier input offset then becomes the offset of the second stage, V_{OS2}, divided by the gain of the first stage, A_1.

An alternative offset cancellation approach is shown in Fig. 6.8. Two conversion sequences are required to compensate the offset voltage. For the first A/D conversion pulse ϕ is high, and an offset voltage V_{OS} is encoded with each voltage difference $V_X - V_K$. On the second A/D conversion ϕ is low, the input terminals are inverted, and the comparator output is taken from the complementary output terminal. Each encoded bit includes a contribution of $-V_{OS}$ to the difference $V_X - V_K$. The two encoded words are added and divided by two to null out the offset voltage. Although this approach requires approximately twice the conversion time, it can be combined with the two-conversion mismatch cancellation scheme discussed in the previous section to eliminate both offset and capacitor mismatch errors simultaneously.

6.5. Speed-Accuracy Tradeoff

In order to determine the time required to precharge a capacitor in a D/A conversion step consider again the circuit of

Fig. 6.5. For $V_B = V_R$, $V_S(0) = 0$ and $V_G - V_T > V_R$, the transistor is nonsaturated and the drain current I is given by [30]:

$$I = \frac{\mu C_{OX}}{2} \frac{W}{L} [2(V_G - V_T) - (V_R - V_S)](V_R - V_S), \tag{6.32}$$

where μ is the average surface mobility, C_{OX} is the channel capacitance per unit area, and V_T is the threshold voltage. Figure 6.9 shows the variation of the current I with source voltage V_S. An effective "on" resistance can be defined at the point where the drain current equals one-half of the peak current I_o. Thus,

$$R_{ON} = \frac{V_R - V_S}{I} \Bigg|_{I=\frac{I_o}{2}} , \tag{6.33}$$

and,

$$R_{ON} = \frac{2}{\mu C_{OX} W/L} g(V). \tag{6.34}$$

$g(V)$ is a function of V_G, V_R, V_T and V_S'. The charging time constant τ is therefore given by:

$$\tau = R_{ON} C . \tag{6.35}$$

From (6.34),

$$\tau = \frac{2L^2}{\mu C_O} g(v) C \tag{6.36}$$

since the channel capacitance $C_O = C_{OX} WL$. The total charging time is given by:

$$T = R_{ON} C \ln(V_R / V_{error}) . \tag{6.37}$$

Combining (6.36) and (6.4), the product of charging time and feedthrough error voltage is:

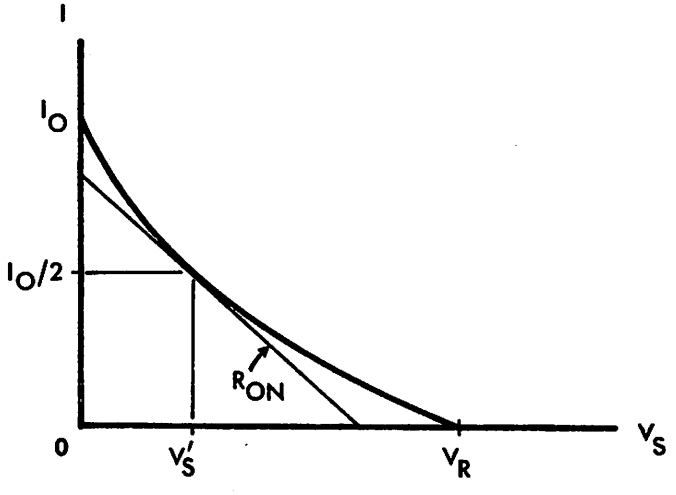


Fig. 6.9. Variation of Charging Current with Source Voltage.

$$\tau \cdot V_{f\varepsilon} = \frac{4L^2}{\mu} f(V)g(V) \ . \qquad (6.38)$$

Equation (6.38) indicates that the worst-case charging time and feedthrough error voltage are determined by the ratio of the switch transistor channel capacitance to the charge-sharing capacitance C, in such a way that a tradeoff exists. The product $\tau \cdot V_{f\varepsilon}$ is proportional to the square of the MOSFET channel length. Thus significantly improved performance can be attained with reduced channel lengths. Figure 6.10 is a plot of the feedthrough error voltage and charging time based on computer simulations for several channel lengths and W/L ratios.

In summary, in this chapter a characterization has been made of the most important sources of error in the two-equal-capacitor converter described in Chapter V. Some circuit design alternatives have been described to reduce the error voltage components. The design decisions which are made to reduce feedthrough error voltages determine the capacitor charging time and therefore affect conversion speed. Reduction of MOSFET channel lengths promises improved performance through reduced charging times and feedthrough error voltages. Breakdown voltages in short channel devices determines the smallest practical channel length of the devices.

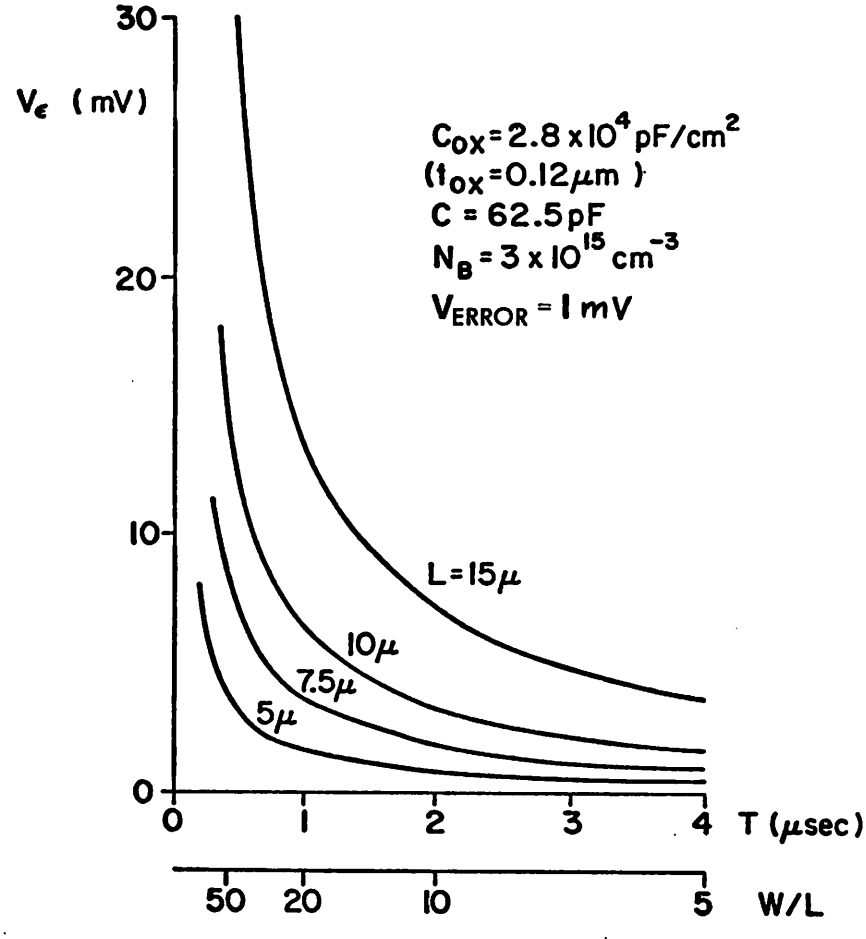


Fig. 6.10. Speed-Accuracy Tradeoff.

CHAPTER VII

MONOLITHIC INTEGRATED CIRCUIT REALIZATION

To verify experimentally the feasibility of the conversion technique developed in Chapter V, the two-capacitor DAC was fabricated by a five-mask n-channel aluminum gate MOS process* in the ERL integrated circuits laboratory at U.C.B. Figure 7.1 is a schematic diagram of the digital-to-analog converter circuit, and Fig. 7.2 is a photomicrograph of the 8-bit monolithic realization. The performance of the circuit was measured in a successive approximation analog-to-digital converter test configuration. The converter exhibits an 8-bit accurracy and an analog-to-digital conversion time of 100 μs.

7.1. Chip Design

The circuit shown in Fig. 7.1 was fabricated on a 1.8-2.4 Ω cm p-type [100] substrate according to the process schedule described in Appendix E. A p^+ channel-stop diffusion was included in the process to minimize device-to-device leakage currents arising from surface inversion. The charge-sharing switch transistor Q7 in Fig. 7.1 requires careful layout to maintain circuit sysmmetry. The geometry shown in Fig. 7.3 tends to compensate masking misalignments, thus keeping the source and drain overlap capacitances equal.

For an 8-bit design the mismatch data on Table 4.1 indicates that 25 pf of capacitance for the charge-sharing capacitors C1 and C2 is appropriate. With respect to a 5 volt reference voltage the worst case feedthrough voltage for a single step must be kept below

*An initial attempt was made to fabricate the circuit using silicon gate technology. The fabrication schedule is detailed in Appendix D. Further process development is required, however, to produce silicon gate circuits reliably.

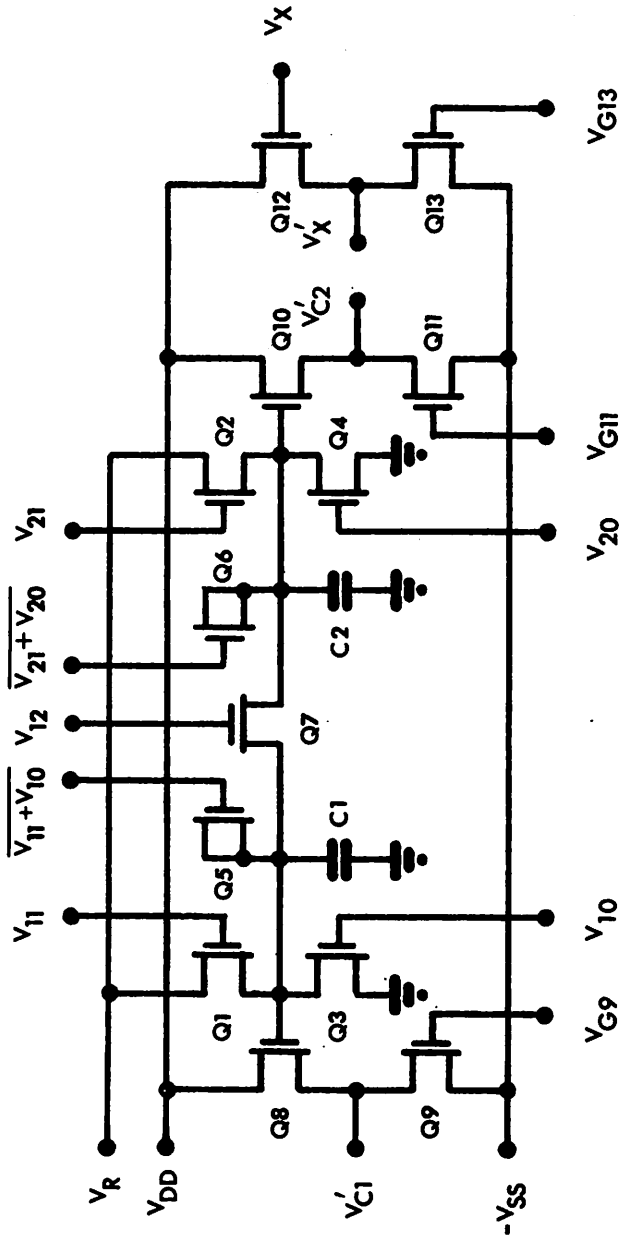


Fig. 7.1. Circuit Schematic of Monolithic DAC.

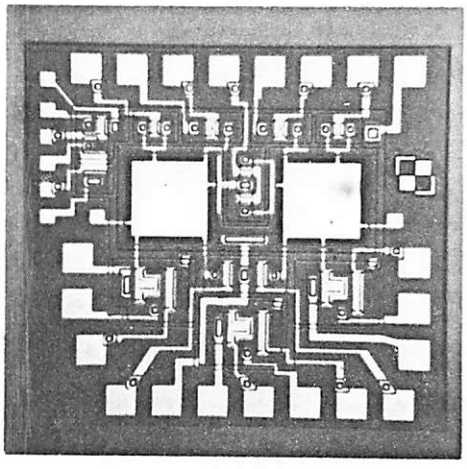


Fig. 7.2. Photomicrograph of Aluminum Gate DAC.

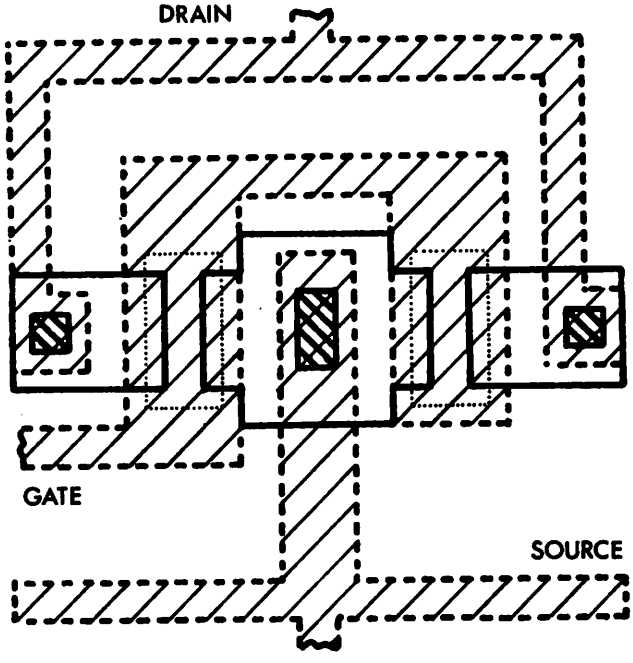


Fig. 7.3. Layout Geometry for Charge-Sharing Transistor Switch.

Legend:
- Diffusion Boundary
- Gate Oxide Edge
- Contact Window
- Aluminum Line

5 mV. According to Eq. (6.4), therefore, the channel capacitance of the switch transistors is limited to:

$$C_o < (5\times10^{-3}) \times 2 \times 25 \text{ pF} = 0.25 \text{ pF}. \qquad (7.1)$$

All transistors were designed with a nominal channel length L = 7 μm and an oxide thickness t_{OX} = 1000 Å. The choice of width-to-length ratio for transistors Q1-Q4 and Q7 is restricted in view of (7.1) to W/L < 16. The switch devices were assigned a W/L = 10 in the design. For the charge-cancelling transistors Q5 and Q6 a W/L = 5 is needed to make their channel capacitance one-half of the channel capacitance of the switch transistors.

The source followers Q8-Q11 are output buffers for the capacitor voltages. Source follower Q12-Q13 is included to level shift the unknown voltage V_X to the same level as the DAC output voltage. The pull-down devices Q9, Q11 and Q13 have W/L = 10 and are biased in saturation. A nominal bias current of 200 μA flows through these devices so that a 10 pF load capacitance can be discharged 5 volts in 100 ns. The pull-up transistors Q8, Q10 and Q12 have W/L = 15 to reduce the magnitude of the level shift voltage drop since

$$V'_{C1} = V_{C1} - V_{T8} - \sqrt{\frac{(W/L)_9}{(W/L)_8}}\ [V_{G9} + V_{SS} - V_{TO}] \qquad (7.2)$$

where [30] $V_{T8} = V_{TO} - \gamma[\sqrt{V_{SS}+\phi+V'_{C1}} - \sqrt{\phi}]$.

Since no offset-cancellation circuitry was included on the chip the gate terminals of the pull-down transistors are taken off-chip to permit offset nulling.

For the device geometries described the worst-case charging time to within 1 mV of V_R is estimated through Eq. (6.37) to be about 800 ns. Computer simulations using the device parameters listed on Table 7.1 predict a charging time of 800 ns and a maximum cummulative error voltage of 10 mV at the end of a 4-bit D/A conversion.

7.2. Experimental Results

Figure 7.2 is a photomicrograph of the experimental die. The chip size is 48×52 mil^2 of which the converter active area is 35×35 mil^2. The integrated DAC was tested in a successive approximation ADC circuit as shown in Fig. 7.4. Approximatley 40 bits of shift register plus some decoding gates were implemented with TTL logic. A bipolar integrated circuit was used for the voltage comparator.

A time diagram for the control signals is shown in Fig. 7.5. The oscilloscope photographs shown in Figs 7.6 and 7.7 correspond to an 8-bit D/A and A/D conversion. The control waveforms include a 5 μs time interval after each D/A conversion to take into account the estimated settling time of an MOS differential voltage comparator. The total conversion time for an A/D conversion is 100 μs, corresponding to:

$$T_{ADC} = 8 \times 9 \times (.74\ \mu s + .1\ \mu s) + 8 \times 5\ \mu s, \qquad (7.3)$$

as indicated by Eq. (5.15). The D/A conversion time for 8-bits is:

$$T_{DAC} = 2 \times 8\ (.74\ \mu s + .1\ \mu s) = 13.5\ \mu s. \qquad (7.4)$$

The capacitor matching data shown in Fig. 7.8 was obtained by measuring the mismatch in the DAC capacitor pairs on 16 circuits. The

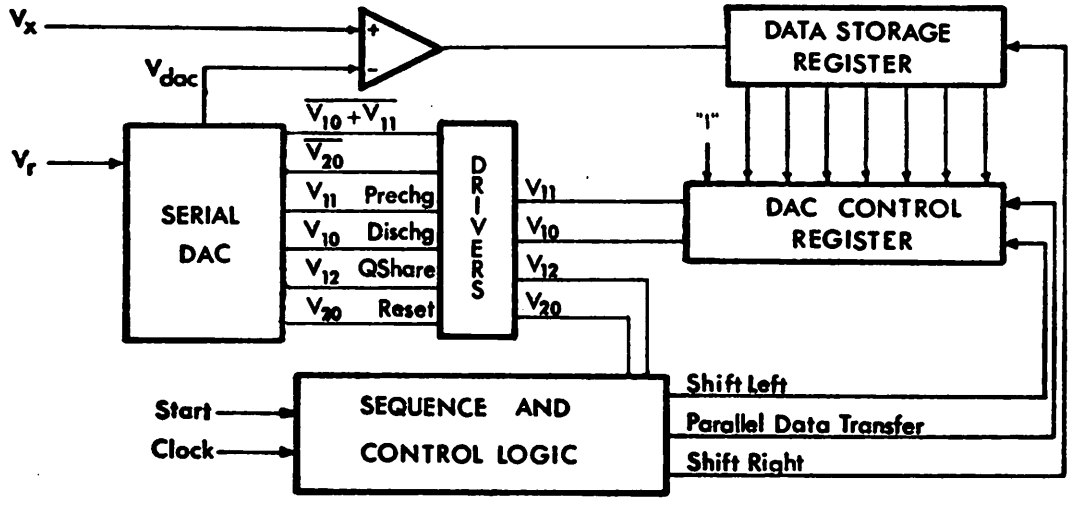


Fig. 7.4. Successive Approximation ADC Test Configuration.

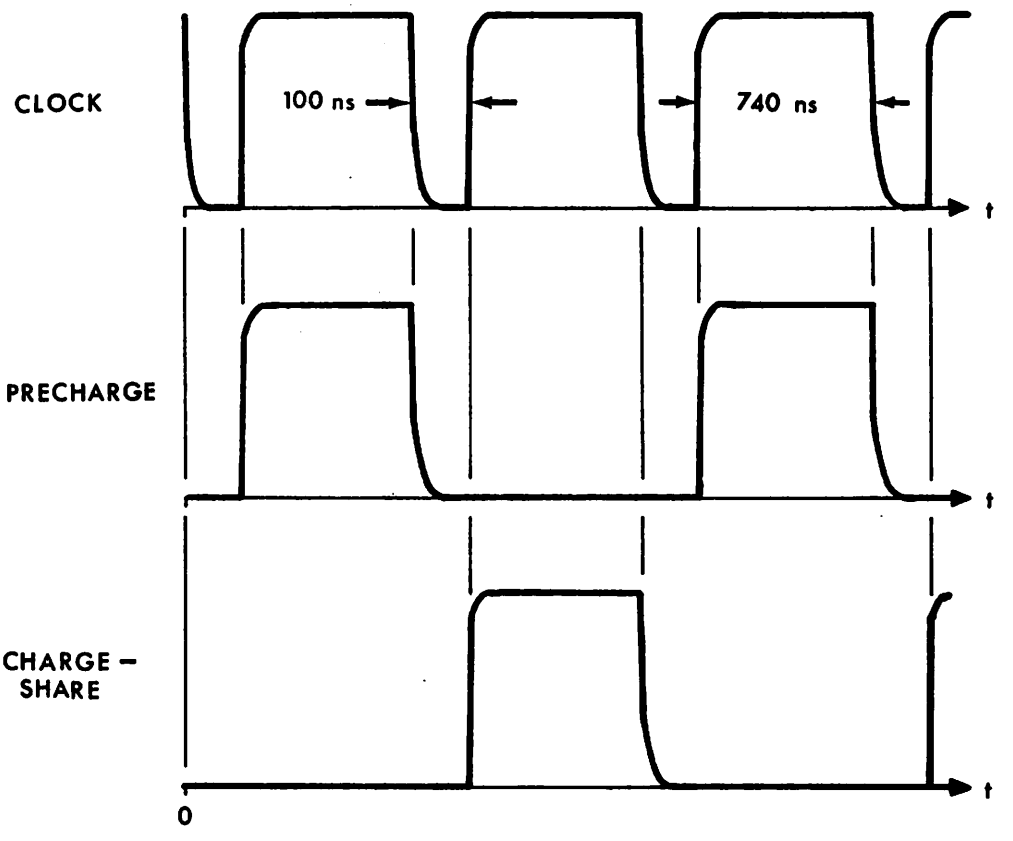


Fig. 7.5. Timing Diagram of Some ADC Control Signals.

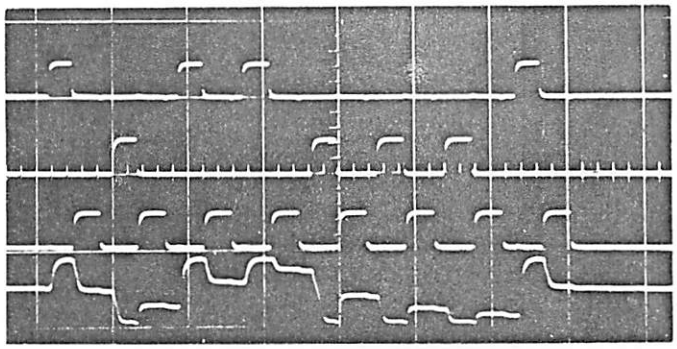


Fig. 7.6. Oscilloscope Photograph of D/A Conversion Sequence.

Input word:	10001101	Vertical	Horizontal
Top Trace:	V11		
Second Trace:	V10	20 v/div	2 μs/div
Third Trace:	V12		
Bottom Trace:	V'C1	5 v/div	

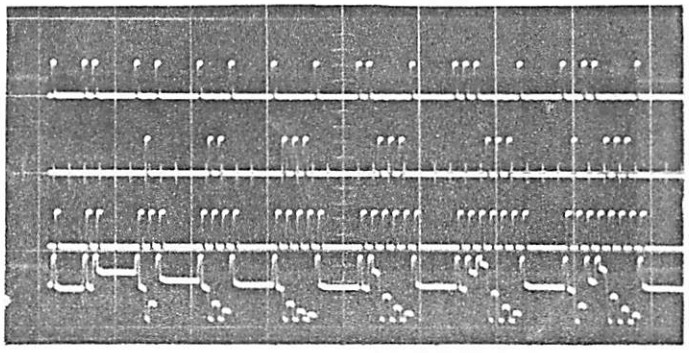


Fig. 7.7. Oscilloscope Photograph of A/D Conversion Sequence.

Output word:	10001101	Vertical	Horizontal
Top Trace:	V11		
Second Trace:	V10	20 v/div	uncalibrated
Third Trace:	V12		(8 div ≅ 100 μs)
Bottom Trace:	V'C1	5 v/div	

Table 7.1. DEVICE PARAMETERS FOR COMPUTER SIMULATIONS USING THE PROGRAM ISPICE

Parameter	Description
$V_{TO} = -0.3$ V	Zero-bias threshold voltage.
$N_B = 3 \times 10^{15} cm^{-3}$	Substrate Doping Concentration.
$C_O = 3.1 \times 10^{-8} F/cm^2$	Channel Capacitance/Area
$C_1 = C_2 = 40$ pF/cm	Overlap Capacitance/Width
$C_{BS} = C_{BD} = 30$ pF/cm	Zero-bias Junction Capacitance/Width
$\mu_0 = 300$ $cm^2/v \cdot sec$	Zero-bias Surface Mobility.

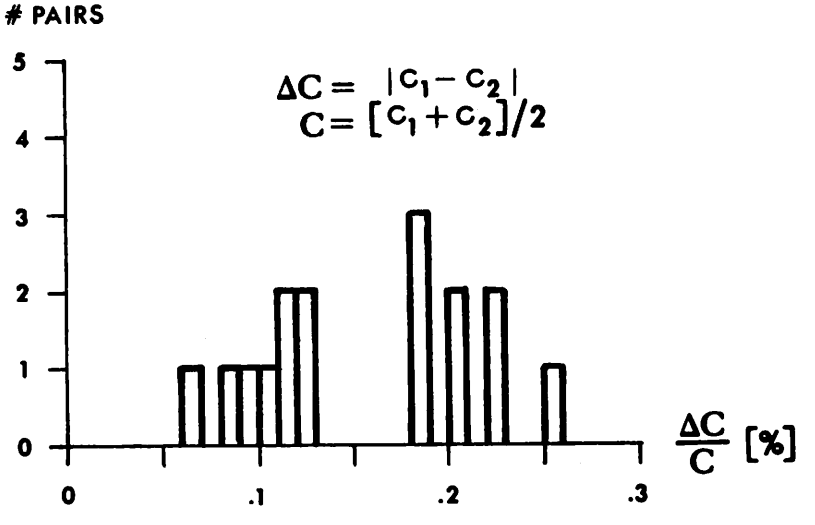


Fig. 7.8. Capacitor Matching Data.

standard deviation mismatch is 0.21%. Figure 7.9 is a plot of the error voltage for an 8-bit ADC versus input voltage. The maximum error is 9 mV which is less than 1/2 LSB for a reference voltage of 5.120 V.*

The general features of this error curve can be explained in terms of the error components shown in Fig. 7.10. A masking misalignment on the chip was observed which reduced the gate-source overlap capacitance of transistors Q1 and Q2 by approximately 15%. Since the capacitance components of the charge-cancelling devices Q5 and Q5 are unchanged, this misalignment results in a net positive error voltage on C1 and C2 when the most significant bits are "1", as shown in the computer simulation results in Fig. 7.10(a). The masking misalignment also causes a reduction of 15% on the gate-drain overlap capacitance of Q3 and a 15% increase in the gate-drain overlap capacitance of Q4. The change in the capacitances of Q3 and Q4 causes a net positive error voltage on C1 and C2 when the most significant bits are "0", as indicated by the computer simulation results in Fig. 7.10(b). A third error component arises from the mismatch between capacitors C1 and C2. Equation (6.13) predicts a discontinuity of approximately twice the value of the capacitor mismatch Δm at the (011..1) to (100..0) transition. The computer simulation points shown in Fig. 7.10(c) show this discontinuity for a capacitor mismatch of 0.1%. The composite diagram of the three error components shown in Fig. 7.10(d) is in general agreement with the measured error curve in Fig. 7.9.

Of the three error components isolated above the first two can

*This voltage level was chosen for convenience to make 1 LSB = 20 mV.

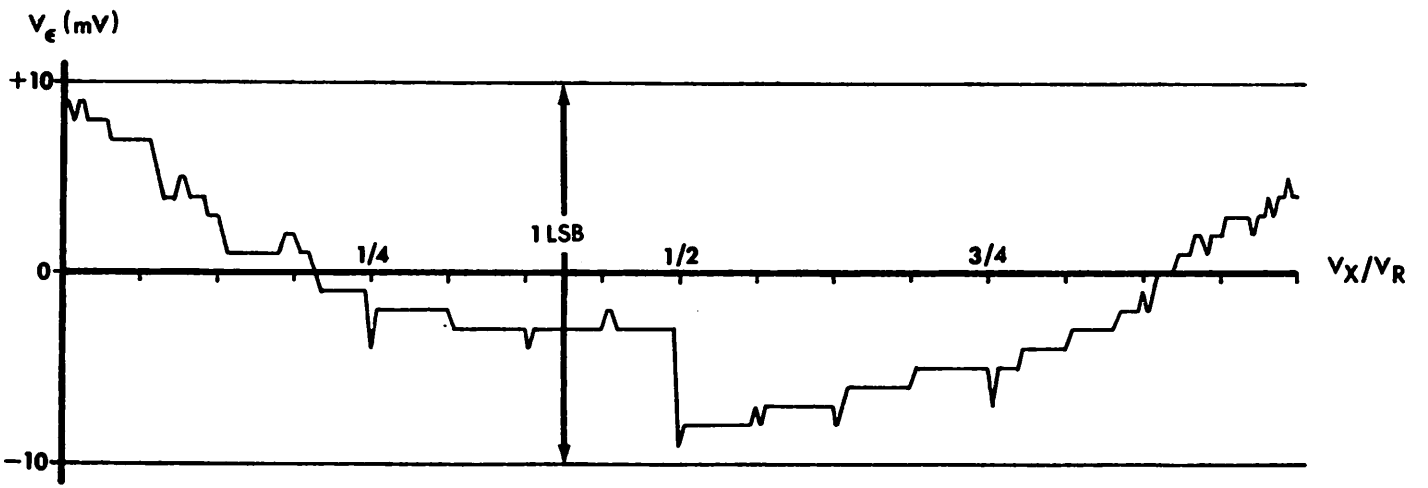


Fig. 7.9. Plot of Error Voltage vs Input Voltage for the Monolithic Converter.

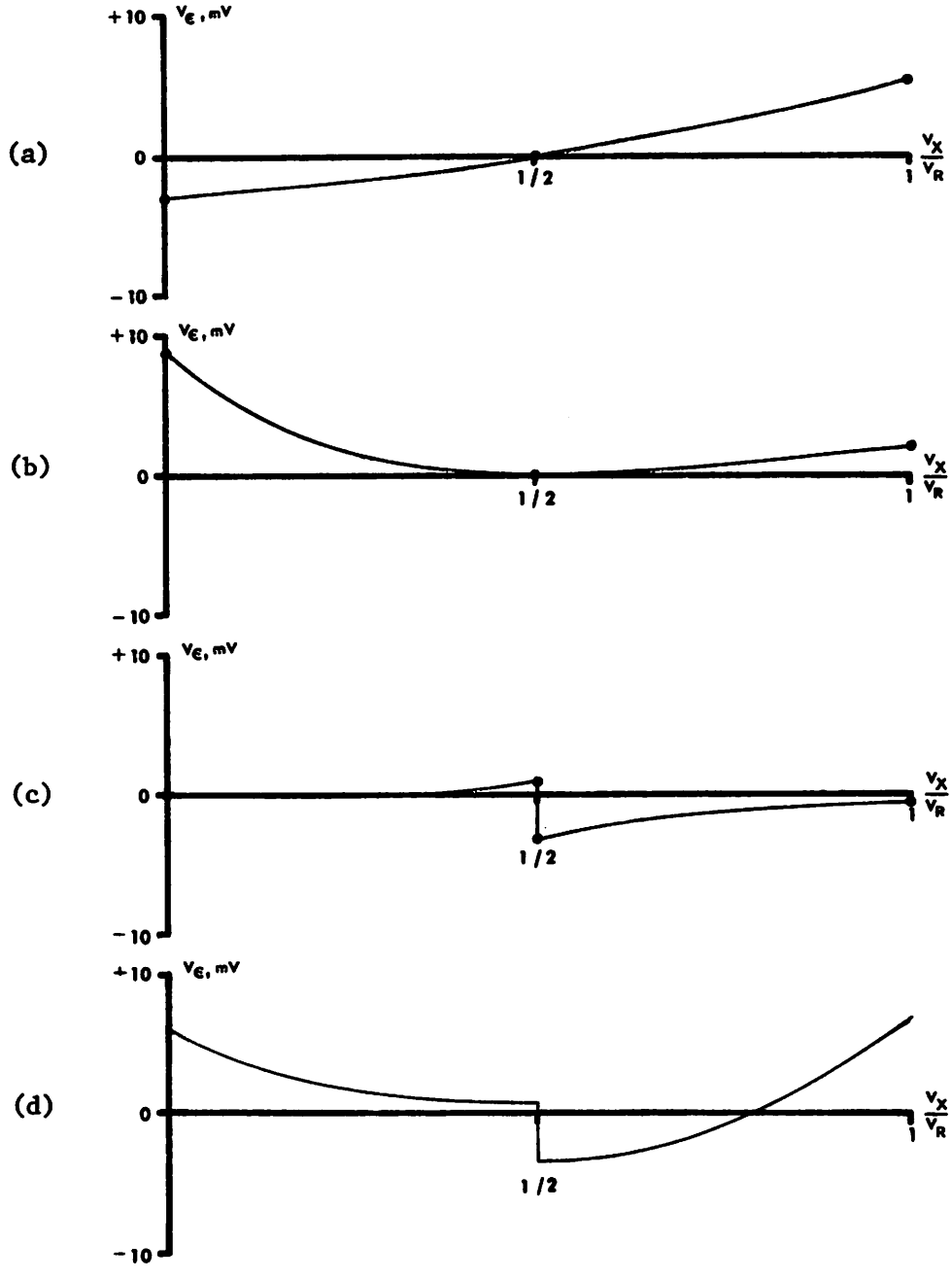


Fig. 7.10. Components of Error Voltage Curve.

(a) Q_1 and Q_2 Misalignment Error

(b) Q_3 and Q_4 Misalignment Error

(c) Capacitor Mismatch Error

(d) Composite Error Curve

be minimized by careful processing and/or a mask layout which is more tolerant to masking misalignments. Therefore, it appears that indeed the principal error sources in the DAC circuit are capacitor mismatches and feedthrough error voltages.

CHAPTER VIII

CONCLUSIONS

An MOS-compatible charge redistribution technique for analog-to-digital conversion has been developed. The conversion approach requires a minimum of two grounded matched capacitors in addition to MOS transistor switches to perform a serial digital-to-analog conversion. Increased conversion speed is possible through the use of additional capacitors. However, of the theoretically possible multiple-capacitor configurations only three are attractive for integrated circuit realization. The simplest circuit with two capacitors requires 2N charging steps for an N-bit D/A conversion. Addition of a third capacitor reduces the conversion time by a factor of two. Further improvements in conversion time with equal-weight capacitors appear possible only at an impractical increase in the number of required capacitors. A third practical alternative results from the use of binary-weighted capacitors, which can reduce the number of charging steps to just two per N-bit D/A conversion.

The primary accuracy limitations have been found to be feedthrough error voltages and capacitor mismatches. Capacitor mismatches place a lower limit on the value of the charge-sharing capacitors which is well within the restrictions for IC realization. Feedthrough error voltages establish a constraint on the size of the switch transistors relative to the size of the charge-sharing capacitors. Therefore, accuracy considerations limit the attainable conversion speed. Although the speed-accuracy tradeoff can be improved by reducing the channel length of the MOS devices, breakdown voltages place a limitation on this design degree of freedom.

It seems, therefore, that further work is warranted in the design of MOS transistor switches optimized for minimum feedthrough voltages.

An experimental chip has been fabricated using aluminum gate MOS technology to verify the feasibility of the conversion technique. The 8-bit monolithic DAC has been tested in a successive approximation ADC circuit and has performed within accuracy specifications with a conversion time of 100 μs. The conversion time includes allowance for eight voltage comparison steps. The settling time of an MOS comparator has been estimated to be 5 μs through computer simulation of a circuit consisting of a cascade of three differential amplifier stages. Since the comparator settling time accounts for 40% of the total conversion time for an 8-bit ADC, it is apparent that an improved design for a high speed, low offset MOS differential comparator is desirable.

Since component mismatches are an important limitation in A/D converter design, further work in the characterization and reduction of this source of error is needed. To this end the development of an improved statistical model for photolithographically-induced mismatches is desirable. In addition, an optimization of geometries and layout to improve component matching is recommended. Furthermore, the possibility of increasing masking resolution through alternative photomasking techniques should be investigated.

In order to achieve a self-contained monolithic analog-to-digital converter an MOS reference voltage needs to be developed. In addition, work on peripheral circuits such as input buffers and sample-and-hold circuits is needed.

On the basis of the experimental evidence obtained it is concluded

that a monolithic 8-bit analog-to-digital converter can be realized with the charge redistribution technique described in Chapter V. It is reasonable to expect, furthermore, that a 10-bit converter can be realized with the same design rules used in the 8-bit converter described in Chapter VII. Table 8.1 lists the characteristics of a monolithic 8-bit A/D converter and the extrapolated specifications for a 10-bit design.

Table 8.1. SPECIFICATIONS FOR A MONOLITHIC ADC.

8-Bit Design

COMPONENTS	AREA	POWER	CONV. TIME	SUPPLIES	INPUT RANGE
Serial DAC	35×35 mil^2	10 mW			
Shift Registers	35×35 mil^2	5 mW			
Comparator	35×35 mil^2	10 mW			
Logic & Interconn.	35×35 mil^2	10 mW			
Total:	70×70 mil^2	35 mW	100 μs.	+ 10 V - 5 V	0 - 5 V

10-Bit Design

COMPONENTS	AREA	POWER	CONV. TIME	SUPPLIES	INPUT RANGE
Serial DAC	50×50 mil^2	10 mW			
Shift Registers	50×40 mil^2	5 mW			
Comparator	50×30 mil^2	25 mW			
Logic & Interconn.	50×40 mil^2	10 mW			
Total:	100×80 mil^2	50 mW	300 μs	± 15 V	0 - 10 V

APPENDIX A

VOLTAGE COEFFICIENT OF DIFFUSED RESISTORS

A change in the applied voltage across the terminals of a junction isolated diffused resistor causes a variation in the width of the depletion region within the resistor and, therefore, a change in resistance value. Figure 4.6 is a cross-section of a p-base diffused resistor with an applied voltage V across the terminals, and an isolation well bias voltage V_B. The resistor acts as a p-channel JFET with $V_{DS} = -V$ and $V_{GS} = V_B$. Since $L > W >> x_j$ only the effect of V and V_B on the effective resistor thickness is important.

The conductance of the channel can be expressed as:

$$g_D = \frac{\partial I_D}{\partial V_{DS}} = \frac{W}{L} [x_j\bar{\sigma} - x_d\bar{\sigma}_d], \qquad (A.1)$$

where $\bar{\sigma}$ = average conductivity of the p region of thickness x_j.

and $\bar{\sigma}_d$ = average conductivity substracted by the depletion region of width x_d at the drain end.

The product $x_j\bar{\sigma}$ has been calculated by Irvin [31] from

$$x_j\bar{\sigma} = q \int_0^{x_j} \mu(p)[N(x)-N_{BC}]dx \qquad (A.2)$$

for a Gaussian profile N(x) into a bulk concentration N_{BC}. The product $x_d\bar{\sigma}_d$ has been calculated by Lawrence and Warner [32] from

$$x_d\bar{\sigma}_d = q \int_{x_j-x_d}^{x_j} \mu(p)[N(x)-N_{BC}]dx \; . \qquad (A.3)$$

The variation in channel conductance with applied voltage is:

$$\frac{\partial g_D}{\partial V_{DS}} = - \frac{W}{L} \frac{\partial}{\partial V_{DS}} [x_d \bar{\sigma}_a] \quad . \tag{A.4}$$

Applying the step junction approximation for a total applied potential $\phi_T = [V_B + V_{DS} + \phi_B]$ we have,*

$$x_d = \xi \phi_T^{1/2} \tag{A.5}$$

where

$$\xi = \sqrt{\frac{2K_S \epsilon_o}{qN_{eff}}} \quad .$$

Then,

$$\frac{\partial}{\partial V_{DS}} [x_d \bar{\sigma}_d] = \frac{1}{2} \frac{x_d}{\phi_T} \bar{\sigma}_d \quad . \tag{A.6}$$

The voltage coefficient of conductance is therefore,

$$\gamma_V^G = \frac{1}{g_D} \frac{\partial g_D}{\partial V_{DS}} = \frac{-x_d \bar{\sigma}_d}{2\phi_T [x_j \bar{\sigma} - x_d \bar{\sigma}_d]} \quad , \tag{A.7}$$

and

$$\gamma_V^R = - \gamma_V^G = \frac{x_d \bar{\sigma}_d / x_j \bar{\sigma}}{2\phi_T [1 - x_d \bar{\sigma}_d / x_j \bar{\sigma}]} \tag{A.8}$$

Table A.1 is a numerical calculation for a typical base diffusion resistor.

*The use of the step junction formulas is a valid approximation for the typical base diffused resistor parameters listed on Table A.1. The applicability of the approximation can be checked following Grove [33] Chpt. 6.

TABLE A.1

VOLTAGE COEFFICIENT OF A DIFFUSED RESISTOR

Parameters: Epitaxial layer concentration: $N_{BC} = 10^{16} cm^{-3}$.

Base diffusion sheet resistance: $R_s = 200\ \Omega/\square$

junction depth: $x_j = 3\ \mu m$.

average conductivity: $\bar{\sigma} = 16.7\ \mho/cm$.

bulk potential: $\phi_B \cong 0.8$ V.

ϕ_T	x_d μm	$\bar{\sigma}_d$ $\mho$/cm	$x_d\bar{\sigma}_d/x_j\bar{\sigma}$	γ_V^R ppm/V
5.8	.48	.9	$8.6\ 10^{-3}$	750
10.8	.50	1.0	1.0×10^{-2}	470
15.8	.52	1.0	1.04×10^{-2}	330

APPENDIX B

VOLTAGE COEFFICIENT OF MOS CAPACITANCE

An applied potential V_G at the metal plate of an MOS capacitor determines the surface potential ϕ_S at the oxide-semiconductor interface. The surface potential in turn determines the net charge Q_S in the space charge region at the semiconductor surface. A cross-section of an MOS capacitor is shown in Fig. 5.3. The charge density Q_G on the metal electrode can be expressed as

$$Q_G = C_O[V-\phi_S], \tag{B.1}$$

where C_O is the oxide capacitance per unit area. The voltage V is defined in (B.4) and ϕ_S has the polarity definition shown in Fig. B.1.

The capacitance of the MOS structure is given by:

$$C = \frac{\partial Q_G}{\partial V} = C_O[1 - \frac{\partial \phi_S}{\partial V}]. \tag{B.2}$$

The voltage coefficient of capacitance may be defined as [34]:

$$\gamma_V^C = \frac{1}{C_O}\frac{\partial C}{\partial V} = -\frac{\partial^2 \phi_S}{\partial V^2} \quad , \tag{B.3}$$

and the voltage V is given by:

$$V = V_G - \phi_{MS} + \frac{Q_S}{C_O} = \phi_S + \frac{\phi_S}{C_O} \quad . \tag{B.4}$$

ϕ_{MS} is the metal-semiconductor work function difference and Q_{SS} is the surface state charge density. Q_S is total semiconductor charge per unit area. Taking derivatives with respect to V in (B.4) yields:

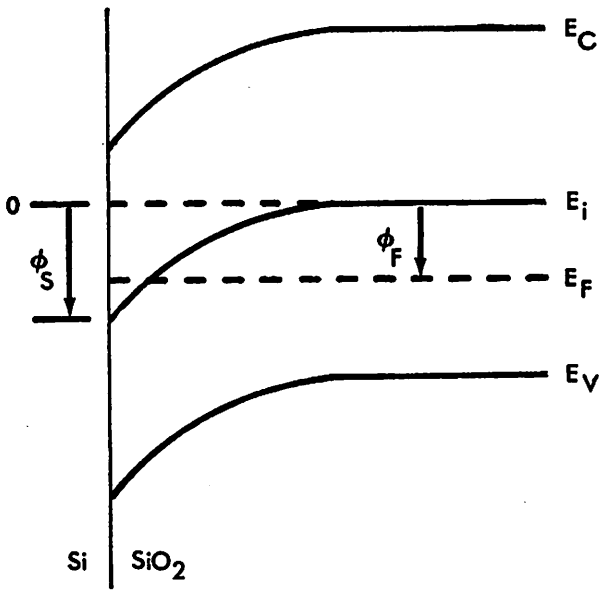


Fig. B.1. Band Diagram of p-type Silicon with the Surface Inverted.

$$\frac{\partial \phi_S}{\partial V} = \frac{1}{1 + \frac{\partial}{\partial \phi_S}\left(\frac{Q_S}{C_O}\right)} \tag{B.5a}$$

$$\frac{\partial^2 \phi_S}{\partial V^2} = \frac{-\frac{\partial^2}{\partial \phi_S^2}\left(\frac{Q_S}{C_O}\right)}{\left[1 + \frac{O}{\partial \phi_S}\left(\frac{Q_S}{C_O}\right)\right]^3} \tag{B.5b}$$

From an electrostatic study of the semiconductor surface using Boltzmann statistics [35] the term Q_S/C_O can be expressed as:

$$\frac{Q_S}{C_O} = \frac{KT}{q} \frac{\phi_S}{|\phi_S|} \frac{\epsilon_S}{\mathcal{L}_D} \frac{F}{C_O} \quad . \tag{B.6}$$

In this equation $\phi_S/|\phi_S|$ = sign $[\phi_S] > 0$ for enhancement of an n-type surface. $\mathcal{L}_D$ is the intrinsic Debye length,

$$\mathcal{L}_D = \sqrt{\frac{\epsilon_S}{q} \frac{kT}{q} \frac{1}{2n_i}} \quad , \tag{B.7}$$

and F is the electrostatic field function,

$$F = \sqrt{2B} \quad . \tag{B.8}$$

with $B = \text{Cosh}(U_S - U_F) + U_S \text{Sinh}\, U_F - \text{Cosh}\, U_F$,

and $U_S = \frac{q}{kT}\phi_S$, $U_F = \frac{q}{kT}\phi_F = \frac{E_F}{kT}$.

Let $F' = \frac{\partial F}{\partial U_S} = \frac{kT}{q}\frac{\partial F}{\partial \phi_S}$. (B.9)

Then, $\frac{F}{\partial \phi_S} = \frac{q}{T} F'$ (B.10)

and, $\frac{\partial^2 F}{\partial \phi 2_S} = \frac{q}{kT} F''$.

Using (B.6), then

$$\frac{\partial}{\partial \phi_S} \left(\frac{Q_S}{C_O}\right) = \text{Sign}[U_S] \frac{C_D}{C_O} F' \tag{B.11}$$

where the intrinsic Debye capacitance is defined as

$$C_D = \epsilon_S / \mathcal{L}_D \quad . \tag{B.12}$$

Similarly, $\frac{\partial^2}{\partial \phi_S^2} \left(\frac{Q_S}{C_O}\right) = \text{Sign}[U_S] \frac{C_D}{C_O} \frac{q}{KT} F''$. (B.13)

The derivatives of F are found from (B.8):

$$F' = B'/F \tag{B.14a}$$

and

$$F'' = \left[\frac{B''}{B'} - \frac{B'}{2B}\right] F' \quad . \tag{B.14b}$$

Letting $Z = \text{Sign}[U_S] \frac{C_D}{C_O}$, (B.15)

and using the above equations into (C.3) the voltage coefficient of capacitance is

$$\gamma_V^C = \frac{\frac{q}{kT} ZF''}{[1+ZF']^3} \quad . \tag{B.16}$$

An accurate study of the space charge at the semiconductor surface for heavily doped material requires the use of Fermi-Dirac statistics. In addition, account must be taken of the effect of impurity band tailing. Following the work of Van Overstraeten et al. [36], however, a concentration-dependent "effective" intrinsic concentration of carriers n_{ie} is used to fit the equations into the

forms obtained above where a parabolic density of states was assumed, and Boltzmann statistics applied. Thus,

$$n_b = n_{ie} e^{-U_F} \quad , \tag{B.17}$$

where n_b is the carrier concentration in the bulk.

For strongly extrinsic n-type material $U_F << 0$, and the function B can be simplified to:

$$B \cong \frac{1}{2} e^{-U_F} (e^{U_S} - U_S - 1) \quad . \tag{B.18a}$$

Similarly,

$$B' \cong \frac{1}{2} e^{-U_F} (e^{U_S} - 1) \quad , \tag{B.18b}$$

and,

$$B'' = \frac{1}{2} e^{-U_F} (e^{U_S}) \quad . \tag{B.18c}$$

Under these conditions the term

$$\Gamma = \left[\frac{B''}{B'} - \frac{B'}{2B}\right] \tag{B.19}$$

in (B.14b) is independent of U_F. Therefore in γ_V^C only the term ZF' contains information regarding doping level [37],

$$ZF' = \text{Sign}[U_S] \frac{\varepsilon_S}{\mathcal{L}_D} \frac{1}{2} e^{-U_F/2} \frac{e^{U_S} - 1}{(e^{U_S} - U_S - 1)^{1/2}} \quad . \tag{B.20}$$

Let

$$G(U_S) = \frac{e^{U_S} - 1}{(e^{U_S} - U_S - 1)^{1/2}} \quad , \tag{B.21}$$

and define the extrinsic Debye length as

$$\mathcal{L}_{DE} = \sqrt{2 \frac{kT}{q} \frac{\varepsilon_S}{q} \frac{1}{n_b}} \quad . \tag{B.22}$$

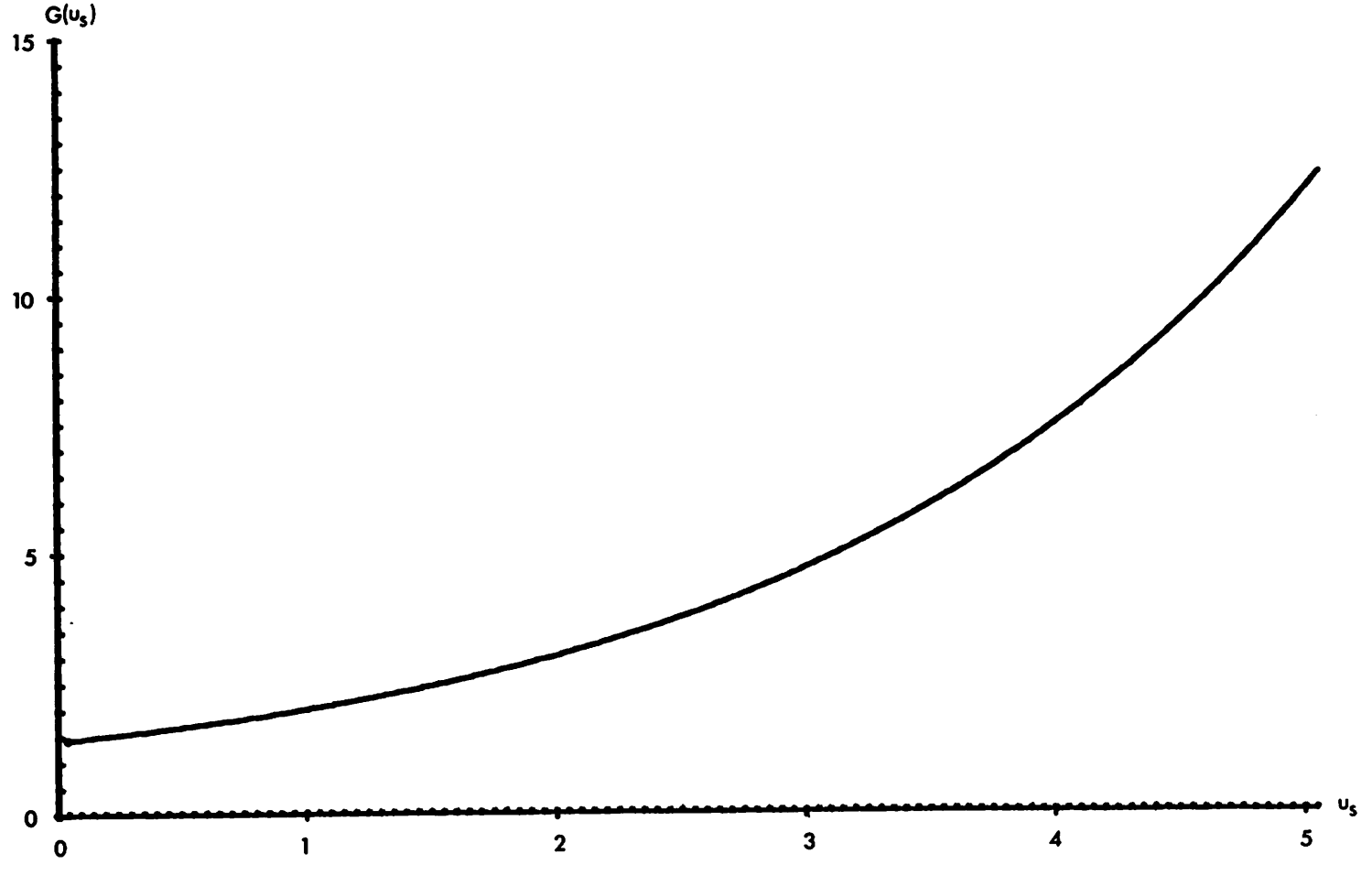


Fig. B.2. The Function $G(u_s)$ vs u_s.

The function $G(U_S)$ is plotted in Fig. C.2. It is convenient, in addition, to define the function

$$Z_O = \text{Sign}[U_S] \frac{\varepsilon_S}{DE} \frac{1}{C_O} = \text{Sign}[U_S] \frac{C_{DE}}{C_O} \quad , \tag{B.23}$$

where C_{DE} is the extrinsic Debye capacitance. Equation (B.20) then becomes,

$$ZF' = Z_O G(U_S) \quad . \tag{B.24}$$

It is interesting to note that ZF' depends on n_b but not on n_{ie}. The function $G(U_S) > 1$ in the accumulation region. For an enhanced n-type surface with $n_b \geq 10^{17} cm^{-3}$ (B.16) reduces to

$$\gamma_V^C = \frac{q}{kT} \frac{\Gamma}{(ZF')^2} \quad . \tag{B.25}$$

Substituting (B.18) and (B.19) into (B.25) yields,

$$\gamma_V^C = \frac{q}{kT} \frac{H(U_S)}{Z_O^2} \quad , \tag{B.26}$$

where

$$H(U_S) = \frac{e^{U_S}(e^{U_S}-2U_S)-1}{2(e^{U_S}-1)^3} . \tag{B.27}$$

The function $H(U_S)$ is plotted in Fig. C.3, and Eq. (B.26) is tabulated in Table B.1 for several doping levels of n-type material. For p-type material in the accumulation region a similar analysis gives:

$$G(U_S) = \frac{1-e^{-U_S}}{(e^{-U_S}+U_S-1)^{1/2}} \quad , U_S < 0, \tag{B.29a}$$

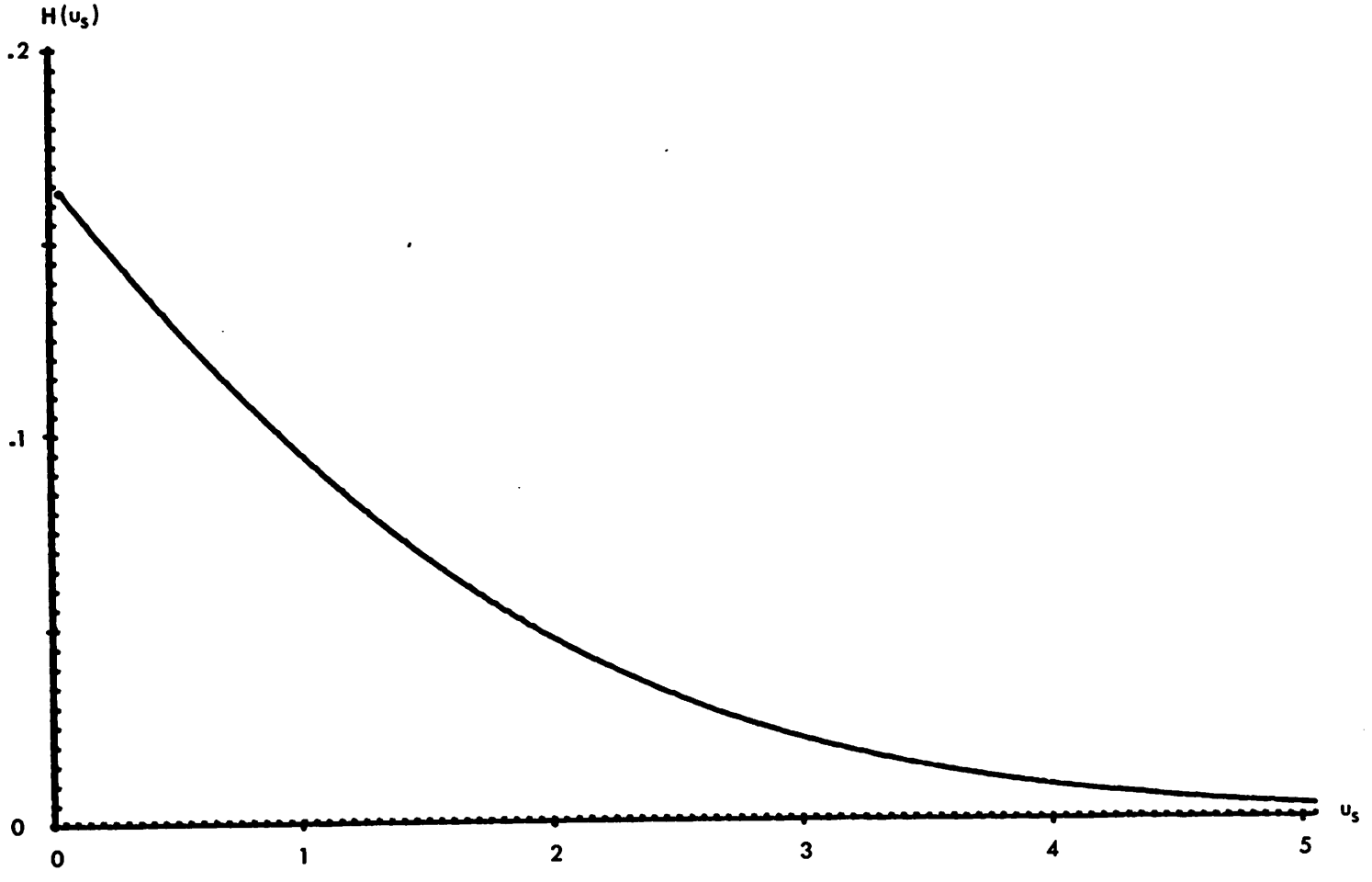


Fig. B.3. The Function $H(u_s)$ vs u_s.

Table B.1. DIFFERENTIAL VOLTAGE COEFFICIENT OF MOS CAPACITANCE

Parameters:

t_{OX} = 1000 Å

T = 300°K

n_b (cm^{-3})	U_S	γ_V^C (ppm/v)	Q_S/C_O (Volts)
10^{18}	3.0	288	10.7
	2.0	664	5.6
	1.0	1350	2.3
10^{19}	1.0	135	7.2
	0.5	183	3.3
	0.2	216	1.2
10^{20}	0.5	18.3	10.3
	0.2	21.6	3.9
	0.1	22.8	1.9
$5x10^{20}$	0.2	4.3	8.8
	0.1	4.6	4.3
	0.05	4.8	2.1

and

$$H(u_S) = \frac{e^{-U_S}(e^{-U_S}+2U_S)-1}{2(1-e^{-U_S})^3} \quad , U_S < 0. \tag{B.29b}$$

Therefore, the expressions for γ_V^C are identical for p-type and n-type material, except for a change in sign. $\gamma_V^C > 0$ for n-type and $\gamma_V^C < 0$ for p-type material.

The voltage dependance of an MOS capacitor is usually determined by measuring the capacitance value at two values of applied voltage, V_1 and V_2. Then

$$\hat{\gamma}_V^C = \frac{1}{V_1-V_2}\left[\frac{C(V_1)}{C_0} - \frac{C(V_2)}{C_0}\right]. \tag{B.30}$$

From (B.2), (B.5) and (B.11) we have,

$$\hat{\gamma}_V^C = \frac{1}{V_1-V_2}\left[\frac{1}{Z_0}\frac{1}{G(V_1)} - \frac{1}{Z_0}\frac{1}{G(V_2)}\right] \quad . \tag{B.31}$$

If the two voltage levels are such that the surface potential does not change sign the values of Z_0 are identical, and

$$\hat{\gamma}_V^C = \frac{1}{V_1-V_2}\,\frac{1}{Z_0}\left[\frac{1}{G(V_1)} - \frac{1}{G(V_2)}\right] \quad . \tag{B.32}$$

Using (B.4) and (B.6) with (B.18) for n-type material we have

$$V_G - \phi_{MS} + \frac{Q_{SS}}{C_0} = \phi_S + 2\frac{kT}{q} Z_0 (e^{U_S}-U_S-1)^{1/2} \tag{B.33a}$$

$$\simeq 2\frac{kT}{q} Z_0 (e^{U_S}-U_S-1)^{1/2} \quad , \tag{B.33b}$$

$$(e^{U_S}-U_S-1)^{1/2} = \frac{1}{2Z_0}\frac{q}{kT}\left(V_G-\phi_{MS}+\frac{Q_{SS}}{C_0}\right) \tag{B.34}$$

For a given value of applied voltage, $V_G = V_1$ or $V_G = V_2$, and information regarding doping level and Q_{SS} density, a value of normalized surface potential can be obtained from (B.34). The value of U_S can then be used in (B.32) to calculate $G(U_S)$ and $\hat{\gamma}_V^C$. Table B.2 lists measured and calculated values of $\hat{\gamma}_V^C$ for different doping levels.

Table B.2. LINEARIZED VOLTAGE COEFFICIENT OF MOS CAPACITANCE

Parameters:

$t_{OX} \cong 1000$ Å

$T = 300°K$

$-\phi_{MS} + Q_{SS}/C_O = 0.6$ V

n-type silicon

n_b (cm^{-3})	V_1 (V)	V_2 (V)	$\hat{\gamma}_V^C$ (ppm/V) calculated	measured [38]
10^{19}	0	+ 6	230	560
$5x10^{20}$	0	+ 6	6	8

APPENDIX C

MISMATCH CONSIDERATIONS FOR MULTIPLE CAPACITORS IN PARALLEL

Consider a capacitor of total area A consisting of r equal capacitors each of area A',

$$A = \sum_{i=1}^{r} A_i' \quad . \tag{C.1}$$

Nominally $A_1' = \ldots = A_r' = A'$, and $A = rA'$. The sides of each component capacitor are denoted L_i' and W_i'. The uncertainty in edge definition is modelled as a simple random displacement of the entire edge with average values L' and W' respectively and standard deviations $\sigma_L = \sigma_W = \sigma$. Figure C.1 shows a single capacitor of area $A = L^2$ and an equivalent capacitor with four equal components of area $A' = (L/2)^2$. The equations shown in the figure correspond to the result obtained in Eq. (C.10) below

Since the random mismatches are considered to be uncorrelated the variance of the total capacitor area is [39]:

$$Var(A) = \sum_{i=1}^{r} VAR(A_i') \tag{C.2}$$

The variance of a component capacitor is given by:

$$Var(A_i') = E(A_i'^2) - E(A_i')^2 \quad , \tag{C.3}$$

where $E(\cdot)$ denotes the average value, and

$$E(A_i') = E(L_i')E(W_i') = L'W' \tag{C.4a}$$

$$E(A_i'^2) = E(L_i'^2)E(W_i'^2)$$

$$= [\sigma^2+L'^2][\sigma^2+W'^2]. \tag{C.4b}$$

Thus,

$$\mathrm{Var}(A_i') = \sigma^2(\sigma^2+L'^2+W'^2). \tag{C.5}$$

Equation (C.5) is minimized for $L' = W'$. Then,

$$\mathrm{Var}(A_i') \cong \sigma^2(2L'^2+\sigma^2) \tag{C.6}$$

From (C.2), the variance of the total capacitor area is therefore,

$$\mathrm{Var}(A) = r\sigma^2(2L'^2+\sigma^2) \ . \tag{C.7}$$

The nominal value of $A = rA' = rL'^2$. For a single capacitor of area $\hat{A} = L^2$ the variance is found from (C.6),

$$\mathrm{Var}(\hat{A}) = \sigma^2(2L^2+\sigma^2) \ . \tag{C.8}$$

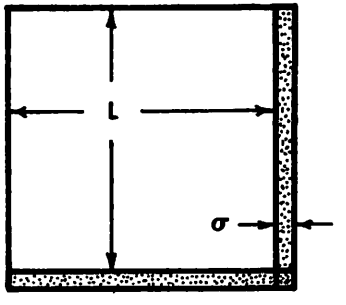
For $\hat{A} = A$, $L = \sqrt{r}\,L'$. Therefore, comparing (C.7) and (C.8),

$$\frac{\mathrm{Var}(A)}{\mathrm{Var}(\hat{A})} \cong 1 + \frac{r-1}{2}\frac{\sigma^2}{L^2} \tag{C.9}$$

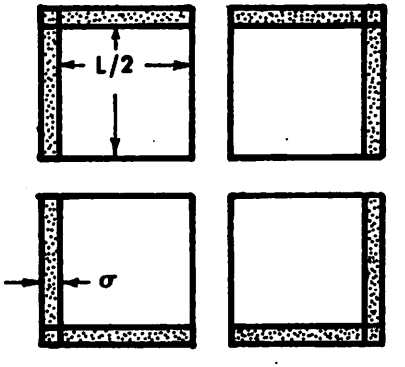
Normally $\sigma^2 << L^2$ then,

$$\frac{\mathrm{Var}(A)}{\mathrm{Var}(\hat{A})} \cong 1. \tag{C.10}$$

Hence, the edge definition uncertainty for a multiple parallel capacitor array is no worse than that for a single capacitor of the same value.



$$\mathrm{Var}(\hat{A}) = (2L^2 + \sigma^2)\,\sigma^2 \cong 2L^2\sigma^2$$



$$\mathrm{Var}(A) = 4\sigma^2\,[2(L/2)^2 + \sigma^2] \cong 2L^2\sigma^2$$

Fig. C.1. Edge Location Mismatches for Parallel Capacitors.

APPENDIX D

N-CHANNEL SILICON GATE PROCESS

D.1. Introduction

The processing schedule listed below is an adaptation of a previously developed procedure at the E.R.L. Integrated Circuits Laboratory [40]. The process was modified to include a p^+ channel-stop diffusion and additional steps to permit fabrication of MOS capacitors over heavily-doped silicon. Although single devices have been successfully made with this procedure, considerable difficulty was encountered in the fabrication of integrated circuits. The principal problems were unreliable interconnections between devices and high voltage coefficient in the MOS capacitors. These difficulties are discussed at the end of the appendix.

Figure D.1 illustrates the most important steps in the fabrication sequence. The starting substrates were 3-4 Ω-cm [100] boron-doped silicon wafers. Throughout the process the wafers were cleaned with the RCA Cleaning Procedure [41] before each thermal oxidation step and each predeposition. An alkaline solution (RCA #1) consisting of a 5:1:1 volume proportion of H_2O:NH_4OH:H_2O_2(30%) was used to clean the wafers after any photoresist step (except after metallization) to remove organic contaminants. A cleaning step in a 6:1:1 solution of H_2O:HCl:H_2O_2(30%) (RCA #2) followed to remove ionic contaminants.

After an initial degrease and chemical cleaning, a thermal oxide of 0.8 μm thickness was grown with wet O_2. A masking step then defined the p^+ channel-stop diffusion wells. After a boron predeposition the wafers were dipped in a 10% HF solution to remove

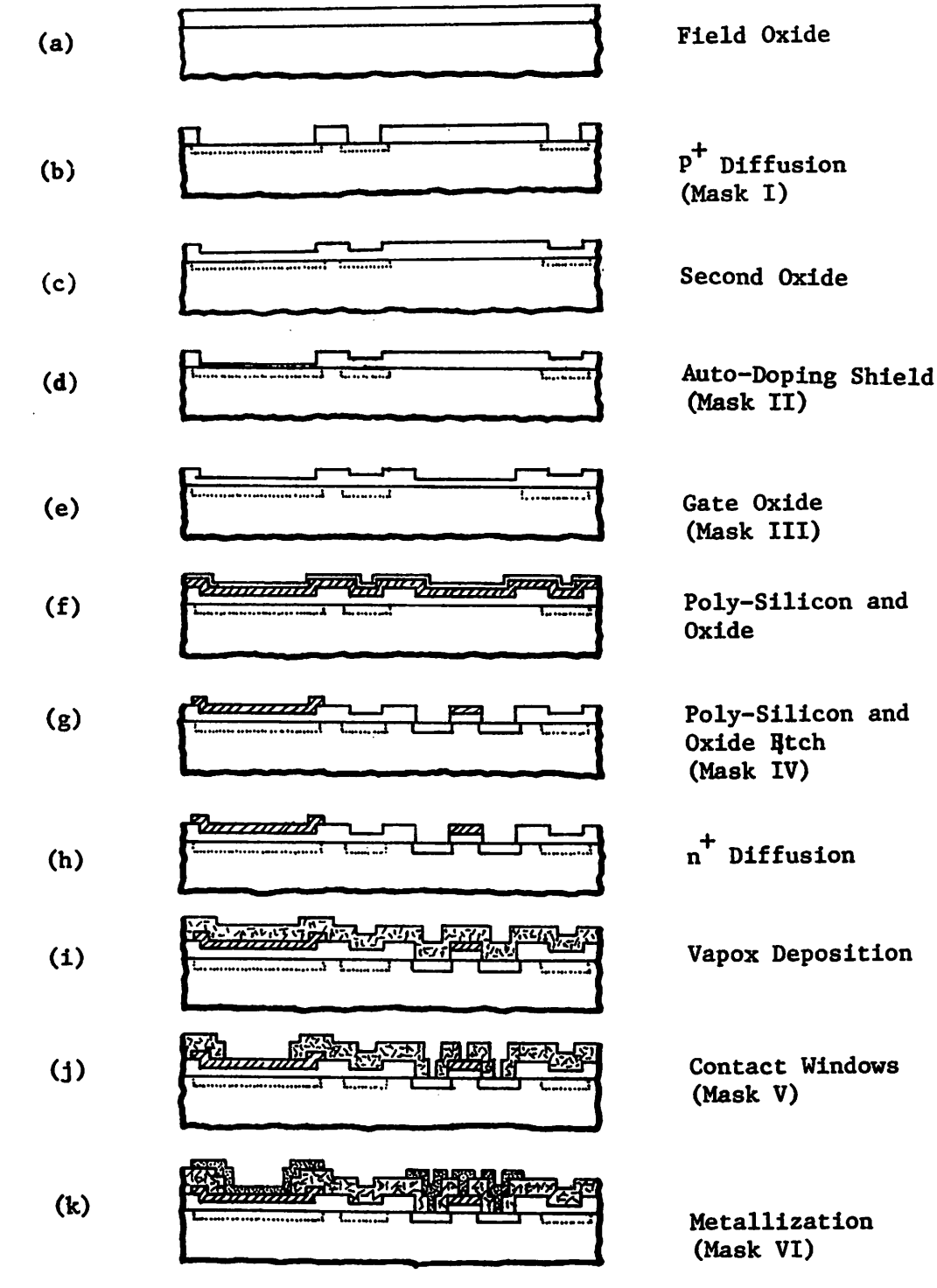


Fig. D.1. N-Channel Silicon Gate Fabrication Sequence.

the boron glass. Approximately 0.6 μm of SiO_2 was then grown over the p^+ regions by wet oxidation. The capacitor sites were subsequently opened through a second masking step. A dry oxide layer of ~ 200 Å was then grown over the capacitor bottom plates to reduce the possibility of auto-doping of the channel regions with boron from the p^+ areas. A third masking step was used to define the MOS device windows through the field oxide. The gate oxide (0.12 μm) was grown with trichloroethylene vapor in the oxidizing gas mixture to reduce the concentration of surface states in the oxide [42]. Immediately after the gate oxide growth a 0.4 μm layer of polycrystalline silicon (poly-silicon) was deposited, and a thin layer of oxide (~ 750 Å) was grown over the poly-silicon. The poly-silicon pattern was then defined by first masking and etching the surface thin oxide. The resulting pattern on the oxide served as a mask for the poly-silicon etch. An oxide etch removed the gate oxide over the source and drain regions and the oxide over the remaining poly-silicon. A phosphorus predeposition of the source, drain and poly-silicon areas followed. Experiments indicated that removal of the resulting phosphorus glass was unnecessary. Phosphorus-doped vapor-evaporated SiO_2 (Vapox) was then deposited as an insulating layer before metallization. Contact windows were opened through the vapox layer, and a 1 μm layer of Aluminum was evaporated. After the metallization pattern had been defined a final annealing step in forming gas was performed.

Figure D.2 shows the I-V characteristic for a device with W/L = 25. This device is a typical switch transistor in the circuit shown in the photomicrograph of Fig. D.3 consisting of an experimental DAC and a voltage comparator.

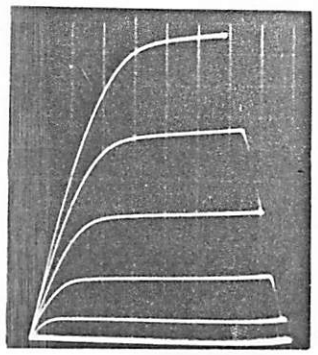


Fig. D.2. I_D vs V_{DS} for a Silicon Gate Transistor.

I_D: 50 μA/div

W/L = 25

V_{DS}: 0.5v/div

V_{GS}: 0.5v/step (Top Trace = 3.5v)

V_{SUB}: = 0v

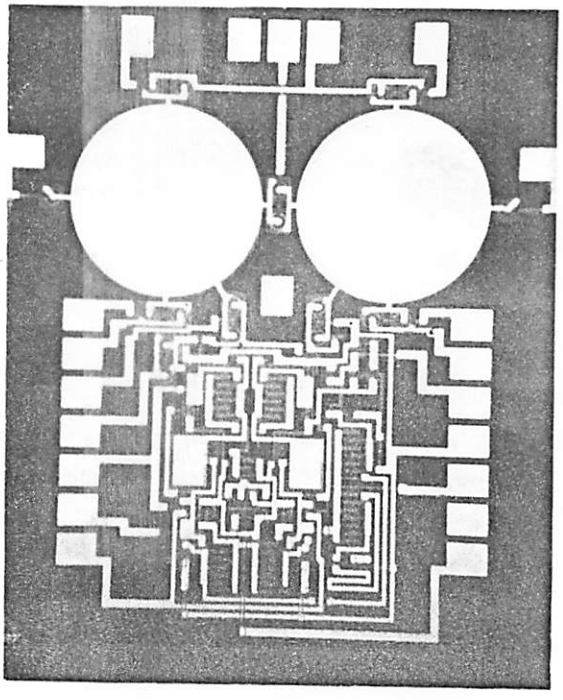


Fig. D.3. Photomicrograph of Experimental Silicon Gate DAC and Voltage Comparator.

D.2. Fabrication Schedule

1. Degrease

- Trichlroethylene (TCE) 60°C 10 min.
- Acetone room T 2 min.
- Deionized water (DiH_2O) Rinse.

2. Chemical Cleaning

- 10% HF Dip
- DiH_2O Rinse 2 min.
- RCA #1 5:1:1 $H_2O:NH_4OH:H_2O_2$(30%) 75°C 15 min.
- DiH_2O Rinse 2 min.
- RCA #2 6:1:1 $H_2O:HCl:H_2O_2$(30%) 75°C 15 min.
- DiH_2O Rinse 5 min.
- Blow dry with N_2

3. - Initial Oxide (Initial Oxidation Furnace) 0.8 μm.
- wet O_2 (97°C DiH_2O) 0.5 ℓ/min. 1050°C 120 min.
- N_2 1.0 ℓ/min. 1050°C 10 min.

4. Photolithography (P^+ Mask)

- 2 coats Kodak 747 (Microneg) resist 4000 rpm 30 secs
- Air dry 5 min.
- Prebake 90°C 30 min.
- Expose 5 secs.
- Spray develop 30 secs.
- Spray rinse 30 secs.
- Postbake 125°C 30 min.
- Cool 1 min.
- Oxide etch 5:1 $NH_4F:HF$(48%) 0.12 μm/min.
- DiH_2O Rinse 2 min.

- Strip photoresist 4:1 H_2SO_4:H_2O_2(30%) 90°C

- DiH_2O Rinse 5 min.

5. Chemical Cleaning

RCA #1 and RCA #2 as in Step 2.

6. P^+ Predeposit (Boron Predeposit Furnace)

B_2H_6	0.26 ℓ/min	1050°C 60 min.
O_2	11.0 ℓ/min.	
N_2	1.3 ℓ/min.	

7. Chemical Cleaning

- 10% HF Dip to remove boron glass

- DiH_2O Rinse 2 min.

- RCA #2 75°C 15 min.

- DiH_2O Rinse 5 min.

- Blow dry with N_2

8. Oxide over P^+ (P Drive-in Furnace) 0.6 μm.

- wet O_2 (97°C DiH_2O) 0.5 ℓ/min. 1050°C 60 min.

- N_2 1.0 ℓ/min. 1050°C 10 min.

9. Photolithography [Capacitor Mask]

Same as Step 4.

10. Chemical Cleaning

RCA #1 and RCA #2 as in Step 2.

11. Autodoping Shield [P Drive-in Furnace] ~ 200 Å

- O_2	1.5 ℓ/min.	1000°C* 13 min.
N_2/TCE	50 cc/min.	
- O_2	1.5 ℓ/min.	1000°C 2 min.
- N_2	1.0 ℓ/min.	1000°C 10 min.

*O_2 flow must be on for several minutes before turning on the flow through the TCE bubbler. Allow the furnace tube to flush for 30 minutes before inserting the wafer.

12. Photolithography [Gate Oxide Mask]

Same as Step 4.

13. Chemical Cleaning

RCA #1 and RCA #2 as in Step 2.

14. Gate Oxide Growth (P Drive-in Furnace) 1200 Å

- O_2	1.5 ℓ/min.	1150°C	18 min.
N_2/TCE	50 cc/min.		
- O_2	1.5 ℓ/min.	1150°C	2 min.
- N_2	1.0 ℓ/min.	1150°C	10 min.

15. Polycrystalline Silicon Deposition (AMH 704 Reactor) 0.4 μm.

- SiH_4 (100%)	80 cc/min.	800°C	7.5 min.
H_2	50 ℓ/min.		

16. Poly-silicon Oxidation (N Drive-in Furnace) 750 Å

- O_2	1.5 ℓ/min.	900°C	10 min.
- Wet O_2 (97°C DiH_2O)	0.5 ℓ/min.	900°C	10 min.
- O_2	1.5 ℓ/min.	900°C	10 min.

17. Photolithography [Poly-silicon Mask]

Same as Step 4.

18. Poly-silicon Etch

- Etching solution 1:50:20 HF(48%):HNO_3:H_2O.

  (Hold wafer with teflon tweezers and agitate back and forth inside plastic beaker at about two strokes per second until gate oxide color appears)

  Etching rate: 100-200 Å/sec poly-silicon

  ~1 Å/sec SiO_2

- DiH_2O Rinse

19. Gate Oxide Etch

- Oxide Etch 5:1 NH_4F:HF(48%) 0.12 μ/min.
- DiH_2O Rinse

20. Chemical Cleaning

RCA #1 and RCA #2 as in Step 2.

21. N Predeposit (Phosphorus Predeposit Furnace) 0.9 μm.

- O_2	0.1 ℓ/min.	1050°C	5 min.
N_2	1.25 ℓ/min.		
- O_2	0.1 ℓ/min.	1050°C	8 min.
N_2	1.25 ℓ/min.		
$N_2/POCl_3$	96 cc/min.		
- O_2	0.1 ℓ/min.	1050°C	2 min.
N_2	1.25 ℓ/min.		

22. Vapox Deposition

1 μm thickness, 400°C, 5% Phosphorus doped

[This step was graciously done by Signetics Corp.]

23. Photolithography [Contact Windows Mask]

Same as Step 4.

24. Chemical Cleaning

- RCA #1 and RCA # as in Step 2.
- 50:1 H_2O:HF(48%) Dip
- DiH_2O Rinse 5 min.
- Blow dry with N_2

25. Aluminum Evaporation

- Dry wafer in IR lamp for 15 minutes
- 4 Aluminum evaporations with 3 staples each.

Rotate 90° each time to cover steps.

26. Photolithography [Metallization Mask]

- 1 coat Shipley 1350J resist 3000 rpm 30 secs.
- Prebake IR Lamp 10 min.
- Expose 10 secs.
- Develop 1:1 MF312:H_2O 1-2 min.
- Rinse DiH_2O 2 min.
- Postbake IR lamp 10 min.
- Etch Al with H_3PO_4 50°C
- Strip resist ultrasonically with Acetone or 1112 remover 1-2 min.
- DiH_2O Rinse 5 min.
- Blow dry with N_2

27. Anneal

- Forming Gas (10% H_2 in N_2) 410°C 10 min.

D.3. Discussion

Some of the problems encountered in the process of developing a fabrication schedule for silicon gate integrated circuits are discussed below. Photoresist lifting problems were eliminated by the use of double coats of Kodak 747 photoresist and extending the prebake and postbake times to 30 minutes. Thermal cracking of undoped vapox layers over poly-silicon steps caused photoresist breaks. The vapox was etched through at these points producing short circuits between aluminum lines and poly-silicon undercrossings. This problem is conventionally solved by the addition of phosphorus to the gas mixture in the vapox deposition [43]. A reliable leak-tightness could not be guaranteed in the present vapox reactor, however, to permit the use of highly toxic phosphine gas. Therefore, the doped vapox layers

were deposited at Signetics Corp. A four-step aluminum deposition was necessary to insure adequate step coverage by the metal lines. The wafer was rotated 90° after each deposition to overcome the shadow effects of the steep vertical geometries.

The MOS capacitors which were built over the P^+ channel-stop diffusion were found to have unacceptably high voltage coefficients (in the order of 400 ppm/v). This indicates a substantial boron depletion during the oxidizing drive-in steps. Increased boron predeposition temperatures were tried in order to increase the boron surface concentration, but what appeared to be a boron skin was formed even when the O_2 flow was doubled. It seems advisable, therefore, to define the capacitors over the n^+ regions since there are fewer high temperature steps after the phosphorus predeposition, and phosphorus accumulates at the $Si-SiO_2$ interface during oxide growth.

APPENDIX E

N-CHANNEL ALUMINUM GATE PROCESS

The fabrication sequence is illustrated in Fig. E.1 and is detailed below. Boron-doped silicon substrates with 1.8-2.4 Ω/cm resistivity and [100] orientation were used. Following an initial degrease and chemical cleaning a first oxide is grown over the wafers. A p^+ channel stop diffusion is then made, followed by an oxidizing drive-in. The source, drain and capacitor regions are formed by a phosphorus predeposition step which is followed by a wet oxidation step. The gate areas are opened and a dry oxide with trichloroethylene is grown to form the gate insulator. The next step is to open the contact windows and evaporate aluminum. Finally, the metallization pattern is defined. In this process no final annealing was performed because the aluminum evaporation step was found to introduce a high concentration of impurities which were driven into the gate oxide during annealing.

Figure E.2 shows a typical I-V characteristic for a transistor fabricated with this schedule (W/L ≅ 25 for this device).

FABRICATION SCHEDULE

1. Degrease
   - Trichloroethylene (TCE) 60°C 10 min.
   - Acetone room T 2 min.
   - DiH_2O rinse
2. Chemical Cleaning
   - 10% HF Dip
   - DiH_2O Rinse 2 min.

- RCA #1 5:1:1 $H_2O:NH_4OH:H_2O_2$ 75°C 15 min.
- DiH_2O Rinse 2 min.
- RCA #2 6:1:1 $H_2O:HCl:H_2O_2$ 75°C 15 min.
- DiH_2O Rinse 5 min.
- Blow dry with N_2

3. Initial Oxide (Initial Oxidation Furnace) 0.8 μ
   - wet O_2 (DiH_2O 97°C) 0.5 ℓ/min. 1050°C 120 min.
   - N_2 1.0 ℓ/min. 1050°C 10 min.
4. Photolithography (p^+ Mask)
   - 2 coats Kodak 747 (Microneg) resist 4000 rpm 30 secs
   - Air Dry 5 min.
   - Prebake 90°C 30 min.
   - Expose 5 secs.
   - Spray develop 30 secs.
   - Spray rinse 30 secs.
   - Postbake 125°C 30 min.
   - Cool 1 min.
   - Oxide etch 5:1 $NH_4F:HF$(48%) 0.12 μ/min.
   - DiH_2O Rinse 2 min.
   - Strip Photoresist 4:1 $H_2SO_4:H_2O_2$(30%) 90°C
   - DiH_2O Rinse 5 min.
5. Chemical Cleaning

   RCA #1 and RCA #2 as in Step 2.
6. P^+ Predeposit (Boron Predeposit Furnace)

   - B_2H_6 0.26 ℓ/min.
     O_2 11.0 cc/min.
     N_2 1.3 ℓ/min
     } 1000°C 15 min.

7. Chemical Cleaning

- 10% HF Dip to remove boron glass
- DiH_2O Rinse 2 min.
- RCA #2 75°C 15 min.
- DiH_2O Rinse 5 min.
- Blow dry with N_2

8. Oxide over P^+ (P Drive-in Furnace) 0.6 μ

- wet O_2 (DiH_2O 97°C) 0.5 ℓ/min. 1050°C 60 min.
- N_2 1.0 ℓ/min. 1050°C 10 min.

9. Photolithograph [N^+ Mask]

Same as Step 4.

10. Chemical Cleaning

RCA #1 and RCA #2 as in Step 2.

11. N^+ Predeposit [Phosphorus Predeposit Furnace]

- O_2	0.1 ℓ/min.	1075°C	2 min.
N_2	1.25 ℓ/min.		
- O_2	0.1 ℓ/min.	1075°C	19 min.
N_2	1.25 ℓ/min.		
$N_2/POCl_3$	96 cc/min.		
- O_2	0.1 ℓ/min.	1075°C	2 min.
N_2	1.25 ℓ/min.		

12. Chemical Cleaning

- 10% HF Dip to remove phosphorus glass
- DiH_2O Rinse 2 min.
- RCA #2 75°C 15 min.
- DiH_2O Rinse 5 min.
- Blow Dry with N_2

13. Oxide over N^+ (N Drive-in Furnace) 0.6 μ

- wet O_2 (DiH_2O 97°C) 0.5 ℓ/min. 1050°C 60 min.
- N_2 1.0 ℓ/min. 1050°C 10 min.

14. Photolithography [Gate Oxide Mask]

Same as Step 4.

15. Gate Oxide Growth [N Drive-in Furnace] 1000 Å

- O_2 1.5 ℓ/min.
  N_2/TCE 50 cc/min. } 1100°C 21 min.
- O_2 1.5 ℓ/min. 1100°C 2 min.
- N_2 1.0 ℓ/min. (at mouth of tube) 5 min.

16. Photolithography [Contact windows Mask]

Same as Step 4.

17. Aluminum Evaporation

- IR Lamp drying 15 min.
- Evaporate 4 staples.

18. Photolithography [Metallization Mask]

- 1 coat Shipley 1350J resist 300 rpm 30 secs.
- Prebake IR lamp 10 min.
- Expose 10 secs.
- Develop 1:1 MF312:H_2O 1-2 min.
- Rinse DiH_2O 2 min.
- Postbake IR Lamp 10 min.
- Etch Al H_3PO_4 50°C
- Strip resist ultrasonically with Acetone or 1112 remover 1-2 min.
- DiH_2O Rinse
- Blow dry with N_2

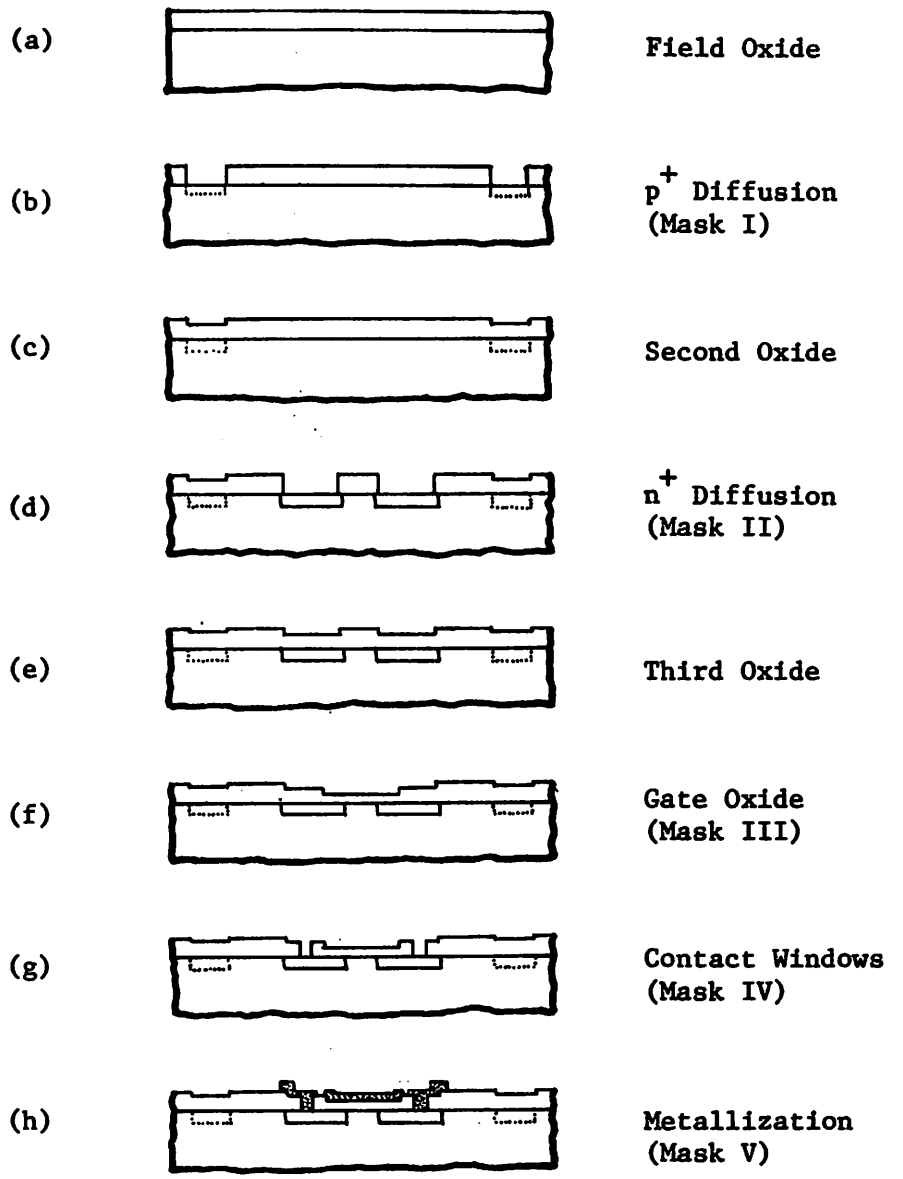


Fig. E.1. N-Channel Aluminum Gate Fabrication Sequence.

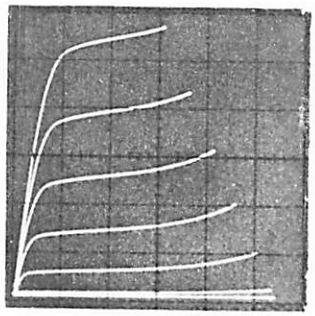


Fig. E.2. I_D vs V_{DS} for an Aluminum Gate Transistor

I_D: 1 mA/div W/L ≅ 25

V_{DS}: 5 v/div

V_{GS}: 1 v/step (Top Trace = 7v).

V_{SUB}: -3.5v

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