NONUNIFORM PULSE CODE MODULATION ENCODING USING INTEGRATED CIRCUIT TECHNIQUES

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Nonuniform Pulse Code Modulation Encoding Using Integrated Circuit Techniques

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Chairman of Committee

A B S T R A C T

This research deals with the investigation of techniques for integrated circuit implementation of nonuniform Pulse Code Modulation voice encoders. An encoder scheme is proposed, which can be realized as a single NMOS integrated circuit, and a partially integrated prototype is shown to exceed the specifications set by the Bell System for the D3 Channel Bank. An internally compensated NMOS operational amplifier has been designed and fabricated as part of this work.

A computer program has been developed for the simulation of PCM encoders and decoders, which has been used to determine the effect of component nonidealities on the performance of the proposed encoder scheme. The simulation, along with additional evidence from the experimental prototype, has shown that it is possible to realize a complete PCM encoder which follows the 15 segment approximation to the 255 μ law on a single NMOS integrated circuit of estimated active size of 120 mil × 120 mil, and whose estimated power consumption is 315 mW. The encoding time needed is 56 μsec.

The internally compensated NMOS operational amplifier occupies an active area of 1200 mil^2, has a power consumption of 150 mW, and, when connected as a unity gain buffer, settles within 1% in 2 μsec for an input step of 5 v and a capacitive load of 70 pF connected to the output through a series device. The amplifier can find additional uses in CCD and bucket brigade circuits.

A C K N O W L E D G E M E N T S

I am grateful to Professors Paul R. Gray and David A. Hodges, whose ideas led to this research effort, for their guidance, encouragement and suggestions. I have appreciated the collaboration of Jacob Chacko, Jr. who has been an integral part of this work. The help of Dr. James L. McCreary, who fabricated and made available to me a special version of his chips is really appreciated, and so are the discussions with Dr. D. L. Duttweiler and his useful suggestions. Many thanks are due to Jose Albarran, Kevin Burns, Fred Hosticka and Robert McCharles for very useful discussions, suggestions and technical advise. Working closely with these people has been both pleasant and rewarding.

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CHAPTER 1

INTRODUCTION

The basic problem of communication is the conveyance of information from a source to a destination. Direct transmission of the quantities representing the information is usually impractical, hence some form of modulation is employed. The particular modulation method to be used in a case in hand is dictated by many factors, including the type of information, the distance between source and destination, the type of the available transmission medium (or "channel"), the degree of interference in the channel, the accuracy desired and complexity and cost considerations.

The concept of Pulse Code Modulation (PCM), which is basically the conveyance of analog information in digital form, is more than half a century old. It is due to P. M. Rainey [1], and was subsequently conceived independently by A. H. Reeves in a form more closely related to today's PCM systems [2]. In the last three decades PCM has been a technique of growing importance, due to the definite advantages of digital transmission over analog transmission in certain cases.

A communication system using analog transmission is shown in Figure 1.1(a), and one using digital transmission in Figure 1.1(b). In both systems, the objective is to transmit information from a source S to a destination D with adequate precision. In some cases the attenuation of the signal in the transmission medium is intolerable, and this dictates the placement of repeaters in the path as shown, whose function is mainly to amplify and retransmit the signal. In addition to attenuation the

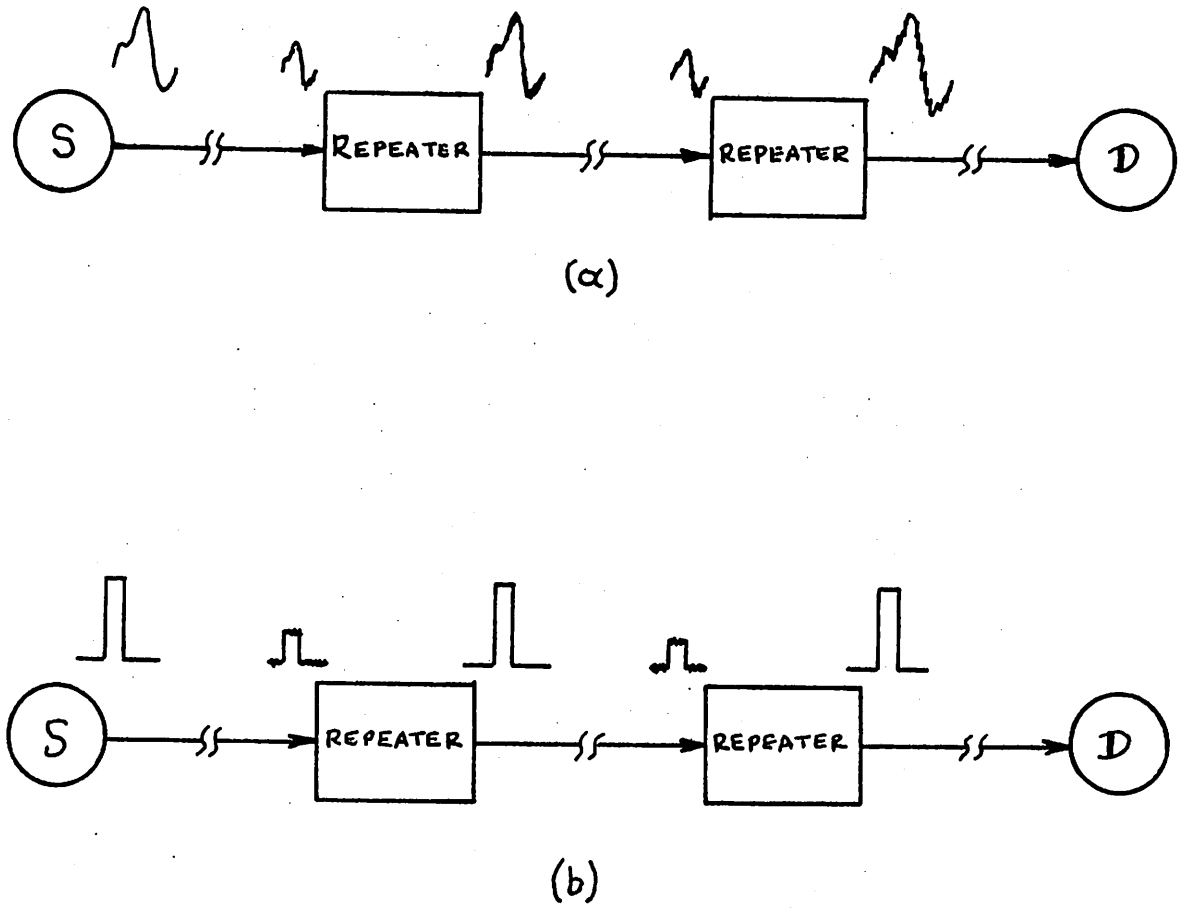


Figure 1.1: (a) Analog transmission system.
(b) Digital transmission system.

signal suffers noise impairment, whose characteristics are inherent to the transmission medium used. The presence of additive noise is very common. In the analog transmission case, signal and noise are indistinguishable to a simple repeater and will appear equally amplified at its output. The resulting noise-contaminated signal, along with additional noise collected on the way to the next repeater, will again be amplified and so on. For a given minimum acceptable signal-to-noise ratio at the receiving end, severe limitations on maximum source-destination distance and minimum transmitting power often must be imposed. The use of sophisticated repeaters which would be able to distinguish between signal and noise is not practical, and even such repeaters would be far from ideal. The performance of the analog transmission system is therefore inherently dependent on the distance between source and destination.

Contrary to this, in the digital transmission system sequences of logic 1's and logic 0's are sent, represented by the presence or absence of pulses. As long as the probability that the noise amplitude will exceed half the amplitude of these pulses is negligible, the reproduction of the original pulses at the output of the repeaters is trivial; it can be done by clipping and subsequent amplification. Since this applies to all repeaters in the path, the quality of the signal reaching the destination can be practically perfect, independently of the distance between source and destination.

Although in the above discussion repeaters are used for emphasis, the advantage of digital transmission over analog transmission remains in the absence of them, since large amounts of noise can still easily be removed at the receiver for the case of digital transmission.

In PCM, an analog signal at the source is adequately sampled, and the sample values are converted into digital words. These words are repre-

sented by pulses which are sent over the communication channel (digital transmission). At the receiving end, the digital words are converted into analog values which are used to construct an approximation of the original signal. In addition to the advantage of this scheme over analog transmission which was mentioned above, i.e. uniform transmission quality over noisy channels independent of distance, PCM offers several other advantages: switching can be easily accomplished using simple digital switches; time division multiplexing is thus readily feasible; and signal processing can be done by digital means, including filtering and storage. New communication techniques, such as pulsed lasers, are inherently adaptable to PCM more than other forms of modulation.

Prior to the last decade, complexity and cost were drawbacks of PCM. Both of these problems can be solved today. A PCM system requires both a considerable amount of digital logic and precision analog circuits. This has resulted in multi-chip approaches where the digital functions are handled by an LSI (Large Scale Integration) chip and the analog functions by one or more separate analog chips. Implementing a complete PCM encoder or decoder on a single chip would certainly be desirable both in terms of cost and flexibility in system design. The objectives of this research effort were: a) The investigation of the implementation of PCM systems for telephone applications using integrated circuit techniques, and the possibilities of realizing a complete encoder on a single chip, and b) The construction and evaluation of a prototype which would demonstrate the feasibility of such a realization.

To this end, the effect of errors in the static characteristic of PCM encoders and decoders on their overall performance was first studied by means of computer simulation. The accuracy required for satisfactory performance was found to be attainable by present IC techniques. In particu-

lar, the possibilities of using charge redistribution schemes were investigated and simulation showed that it should be possible to implement a complete PCM encoder on a single MOS chip. For experimental evidence of this conclusion a partially integrated prototype has been built and evaluated. All precision analog circuits required were fabricated in the integrated circuits laboratory at the University of California at Berkeley. Integration of the supporting logic gates and switches is straightforward and was therefore not attempted.

The performance of the prototype met or exceeded the specifications set by Bell Telephone Laboratories for their D3 channel bank system, and showed that the implementation of a PCM encoder is indeed possible using existing n-channel metal gate MOS technology, on a single chip of estimated size of 15,000 mil^2. As part of the system, an MOS operational amplifier was designed, fabricated and evaluated, which can find several uses in addition to that in the PCM encoder, especially in CCD and bucket-brigade circuits.

In Chapter 2, an outline of the principles of Pulse Code Modulation is given. The reasons for a form of nonuniform encoding, termed "companded encoding", are discussed, and the standard encoding/decoding laws are given.

Chapter 3 deals with the computer simulation of nonuniform encoder-decoder combinations.

In Chapter 4, the reasons for per-channel PCM encoding and the possibilities for a single-chip realization are discussed. A scheme which uses charge redistribution on MOS capacitor arrays is proposed, and the effect of the component nonidealities on the encoder's performance is investigated using computer simulation.

The implementation of analog circuits using single-channel MOS technology is discussed in Chapter 5.

In Chapter 6 an internally compensated NMOS operational amplifier is described, which has been designed and fabricated for use in the encoder proposed in Chapter 4. Computer simulation and experimental results are given.

A partially integrated prototype PCM encoder using the principle proposed in Chapter 4, is described in Chapter 7. The experimental measurements performed on this prototype are described, and the results are given and interpreted.

Chapter 8 contains the conclusions of this work.

CHAPTER 2

PRINCIPLES OF PULSE CODE MODULATION

2.1 INTRODUCTION

A general view of a PCM system in block diagram form and the properties of its components is undertaken in this chapter. In order that the principles of a PCM system be described, it is useful to examine first a form of modulation closely related to PCM, namely Pulse Amplitude Modulation (PAM). This represents no delay in this discussion, since actually every basic component of PAM systems is also a component of PCM systems.

A PAM system is shown in Figure 2.1(a). An analog signal x(t) at the source is low-pass filtered and sampled, and its sampled values, which themselves constitute an analog signal, are transmitted via the communication channel. At the receiving end the sampled signal is low-pass filtered and results in a reconstruction $\hat{x}(t)$ of the original signal x(t). The sequence of these operations is based on the celebrated sampling theorem, which will be discussed in section 2.2.

If the sampled values are encoded into digital words before being transmitted, and decoded into analog values again at the receiving end, then the resulting modified system is actually a PCM system and is shown in Fig. 2.1(b). The encoding is undertaken by an Analog-to-Digital (A/D) converter, and the decoding by a Digital-to-Analog (D/A) converter. The only difference between the PAM and the PCM systems is the form of the transmitted signal. If it is assumed that the communication channels in the two systems are noiseless, and that the A/D and D/A converters are ideal and of infinite resolution, then the signals at the input of the A/D and the output of the D/A converter are identical, and therefore the performance of the PAM and PCM systems is also identical. These assumptions

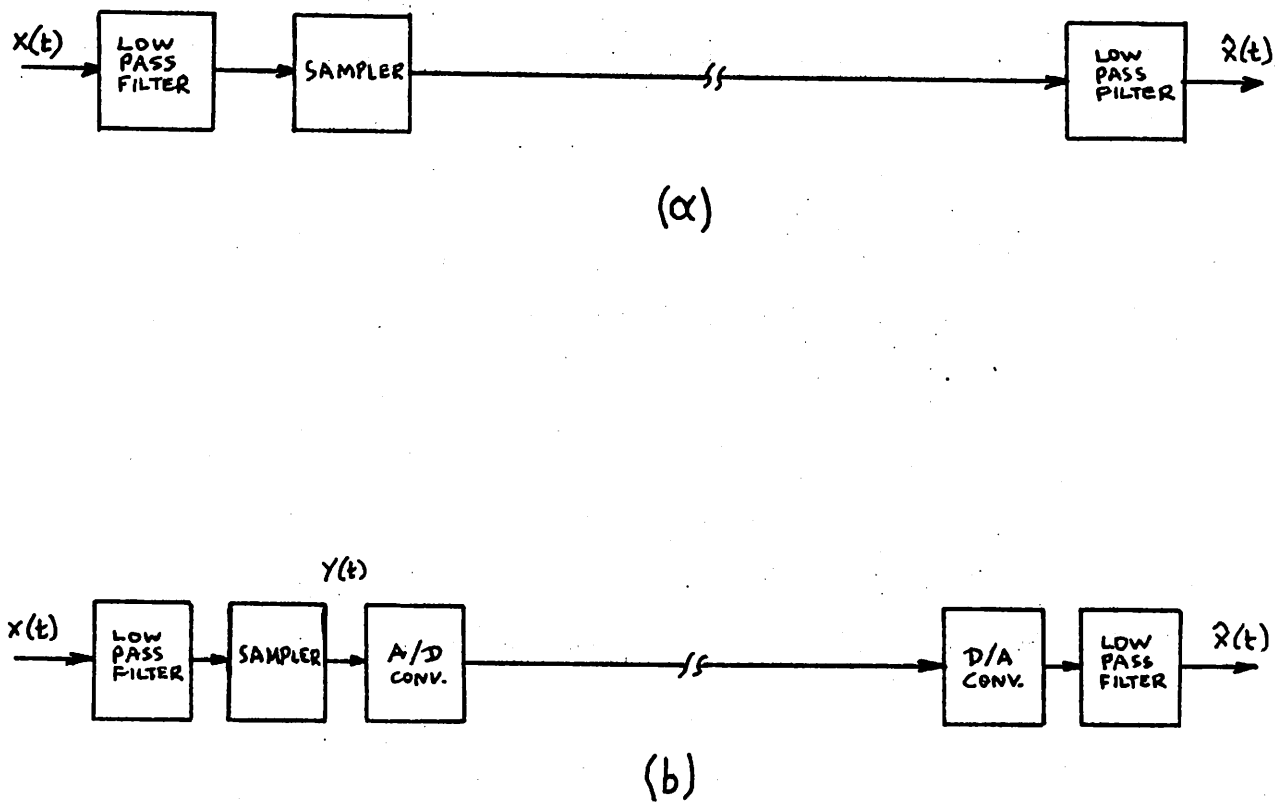


Figure 2.1: (a) Pulse Amplitude Modulation system.
(b) Pulse Code Modulation system.

are of course unrealistic. The channel is noisy, which makes PCM definitely advantageous relative to PAM. On the other hand, the A/D and D/A converters used in PCM can only have finite resolution which as will be seen results in a form of distortion.

It should be noted at this point that the A/D converter is sometimes referred to as the "encoder", whereas at other times this term is reserved for the combination of the A/D converter and the sampler, or even the input filter. Similarly, the term "decoder" might imply the D/A converter by itself, or along with any cooperating circuits that might be present. What is meant by the terms "encoder" and "decoder" when encountered, will usually be clear from the context.

For the purposes of this discussion, and unless stated otherwise, the PAM and PCM systems will be compared under the following conditions:

a) The communication channel is noiseless.

b) The components common to the two systems, namely the two low-pass filters and the sampler, are identical.

These assumptions are certainly justified for the purposes of comparison, and they are not unrealistic.

The principles of PAM will be discussed in section 2.2. Then, in section 2.3, an A/D and a D/A converter will be inserted in the transmission path to implement a PCM system, and the change of the system performance due to this modification will be discussed.

2.2 PULSE AMPLITUDE MODULATION (PAM)

2.2.1 Sampling

Of the many forms of the sampling theorem [3,4], on which PAM is based, the one most useful for the purposes of this discussion is given below:

"A signal bandlimited in $-w < f < w$ can be completely described by its

values at discrete time instants, taken at a uniform rate of f_s, where $f_s \geq 2w$".

The term "sampling rate" is commonly used for f_s, and the minimum adequate sampling rate of 2w is termed the "Nyquist rate".

The input low-pass filter in Figure 2.1(a) is used to ensure that the input to the sampler is indeed bandlimited in $-w < f < w$, and prevents the form of distortion known as "aliasing", which will be discussed below. We will assume that the input signal x(t) is properly bandlimited to begin with, so that it remains unaltered at the output of the filter. For instantaneous sampling the sampled values are represented by impulses whose area is proportional to the signal at the instant of sampling. This can be done by multiplying the signal x(t) by a train of impulses of equal area. The output of the sampler, y(t), will then be given by:

$$y(t) = x(t) \sum_{n=-\infty}^{\infty} \delta(t-nT_s) \tag{2.1}$$

where $T_s = \frac{1}{f_s}$.

The Fourier transform of this then gives the frequency spectrum at the output of the sampler as follows:

$$Y(f) = f_s \sum_{n=-\infty}^{\infty} X(f-nf_s) \tag{2.2}$$

which is simply the superposition of translations of the spectrum of x(t) by multiples of the sampling frequency. Since x(t) was properly bandlimited these spectra do not overlap, and passing y(t) through the output low-pass filter, which has a cutoff frequency of $f_s/2$, will eliminate all high frequency terms in the above sum except that for n=0, which is X(f) (except for a constant multiplier). After the output filter then, a perfect reconstruction of x(t) will appear.

Since impulses are not realizable in practice, actual sampling systems are periodic trains of pulses with finite amplitude and width s(t), by which x(t) is multiplied. This is shown in Figure 2.2. Since these pulse trains are periodic, they can be represented by a Fourier series as follows:

$$s(t) = a_o + \sum_{n=1}^{\infty} a_n \cos(n\omega_s t + \phi_n) \tag{2.3}$$

where $\omega_s = \frac{2\pi}{T_s}$.

The output y(t) of the sampler will therefore be:

$$y(t) = a_o x(t) + \sum_{n=1}^{\infty} a_n x(t) \cos(n\omega_s t + \phi_n) \tag{2.4}$$

The Fourier transform of this is:

$$Y(f) = a_o X(f) + \frac{1}{2}\sum_{n=1}^{\infty} a_n \left[\epsilon^{j\phi_n} X(f-nf_s) + \epsilon^{-j\phi_n} X(f+nf_s)\right] \tag{2.5}$$

It can be seen that all terms under the summation sign are outside the low-pass band $-w < f < w$. They can therefore be removed as before by low-pass filtering, after which only $a_o X(f)$ remains. The output of the low-pass filter is therefore again a perfect reconstruction of x(t) (within a multiplicative constant). The operations involved are shown in Figure 2.2. It is interesting to note that not only is the width of the sampling pulse not restricted for accurate reproduction, but even the shape of it does not need to be rectangular, since no particular sampling pulse shape was assumed in the above derivation. This can relax the practical requirements imposed on the sampler of a PAM system. The width of the pulses is therefore only restricted by the number of the channels that are to be multiplexed in a Time-Division-Multiplex (TDM) scheme.

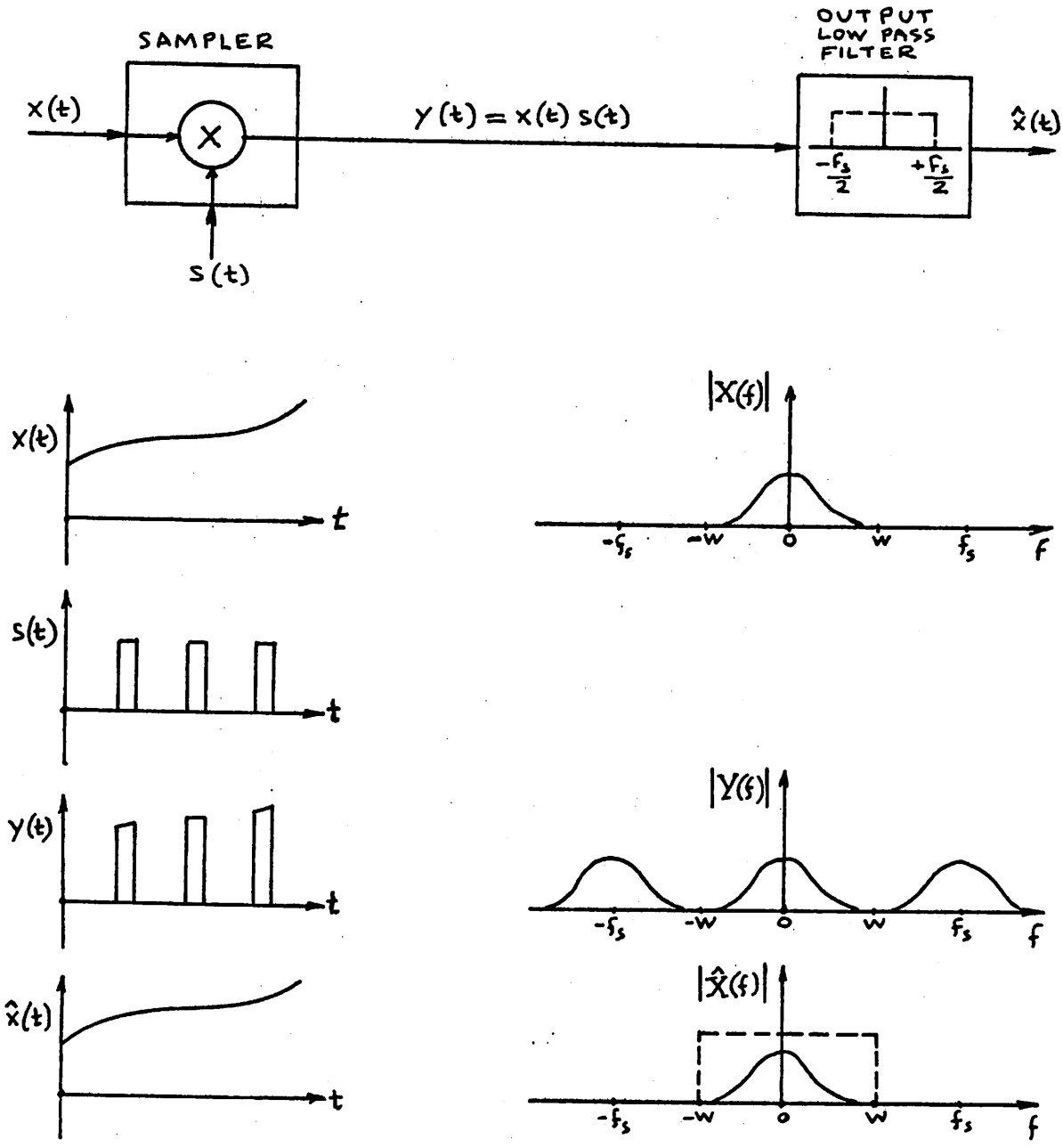


Figure 2.2: Waveforms and spectra in a PAM system.

2.2.2 Aliasing

The Sampling Theorem only holds for sampling rates equal to at least twice the bandwidth of the signal. If for some reason $f_s < 2w$, then examination of the equations given for Y(f) in the previous section shows that the spectra of y(t) will overlap as shown in Figure 2.3(a). Low-pass filtering the sampled signal will therefore not only cut-off the components corresponding to the tail of X(f) which might represent useful information, but also introduce undesired components in the pass-band resulting in additional distortion. This form of distortion is termed aliasing, and can be avoided by using a cut-off frequency for the input filter, which although is high enough to pass all components of x(t) which represent useful information, is still less than half the sampling rate f_s. It is usually made sufficiently less than that to introduce spacings between the translated spectra of y(f), called "guard bands", as shown in Figure 2.3(b). The input low-pass filter is called "anti-aliasing filter" for this reason, and it will be seen that although this name has been carried over to filters being used in PCM systems, aliasing cannot be avoided in PCM despite the fact that such filters are present.

2.2.3 Sampling of Periodic Signals.

Although the results to be stated in this section could have been derived from frequency domain considerations and the sampling theorem, the different approach taken will be found useful for later applications in section 2.3.10, when sampling in PCM systems will be considered.

Consider a periodic signal x(t), whose period we will call T_x, sampled by a periodic pulse train s(t), whose period is $T_s = 125$ μsec. Consider the interesting case where T_x is not an integer multiple of T_s. For example, let $T_x = 312.5$ μsec. This corresponds to a sampling rate of 8 KHz. The fundamental frequency component of x(t) will be at 1/(312.5 μsec),

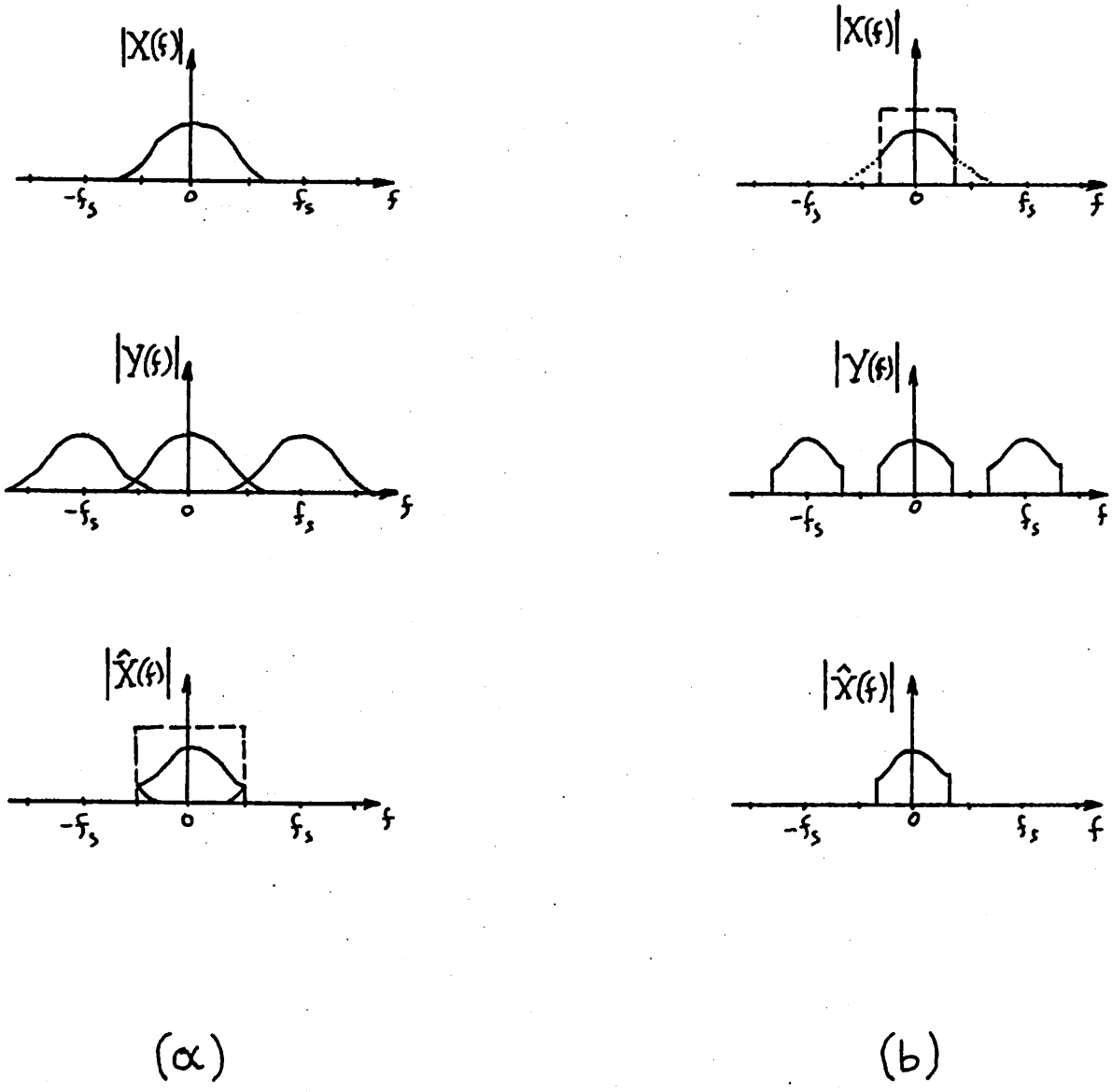


Figure 2.3: (a) Aliasing.
(b) Effect of input antialiasing filter.

or 3.2 KHz. The situation is shown in Figure 2.4. Since 312.5 μsec is not an integer multiple of 125 μsec, it can be seen that the shape of the sampled waveform y(t), shown in (c), will be different over any two consecutive periods of the input. In fact, it can be seen that y(t) repeats itself every 625 μsec, and therefore can be represented by a Fourier series whose fundamental component is at 1/(625 μsec)= 1.6 KHz. This frequency is smaller than the fundamental of the input, which means that at the output of the sampler a subharmonic at 1.6 KHz is present, along with other components at multiples of 1.6 KHz.

The frequency of the lowest order subharmonic present at the output of the sampler represents the fundamental of y(t), and can easily be determined as follows:

The period T_y of the sampled signal y(t) must contain an integer number of periods T_x of the input x(t), and an integer number of periods T_s of the sampling pulse train, in order that y(t) repeats itself every T_y sec. If these integers are k and ℓ respectively, then $T_y = kT_x$ and $T_y = \ell T_s$. From this it follows that k and ℓ must be the smallest integers that satisfy the relation $kT_x = \ell T_s$, which can be written as:

$$\frac{T_x}{T_s} = \frac{\ell}{k} \tag{2.5a}$$

or:

$$\frac{f_s}{f_x} = \frac{\ell}{k} \tag{2.5b}$$

where f_s and f_x are the fundamental frequencies of s(t) and x(t) respectively. For the numerical example given in Figure 2.4, f_s = 8 KHz, f_x = 3.2 KHz and it is found that ℓ = 5 and k = 2. Therefore, the period of the output y(t) is $T_y = \ell T_s = 5 \times 125$ μsec = 625 μsec as already mentioned.

Let us now consider the situation where the 8 KHz sampling pulse train

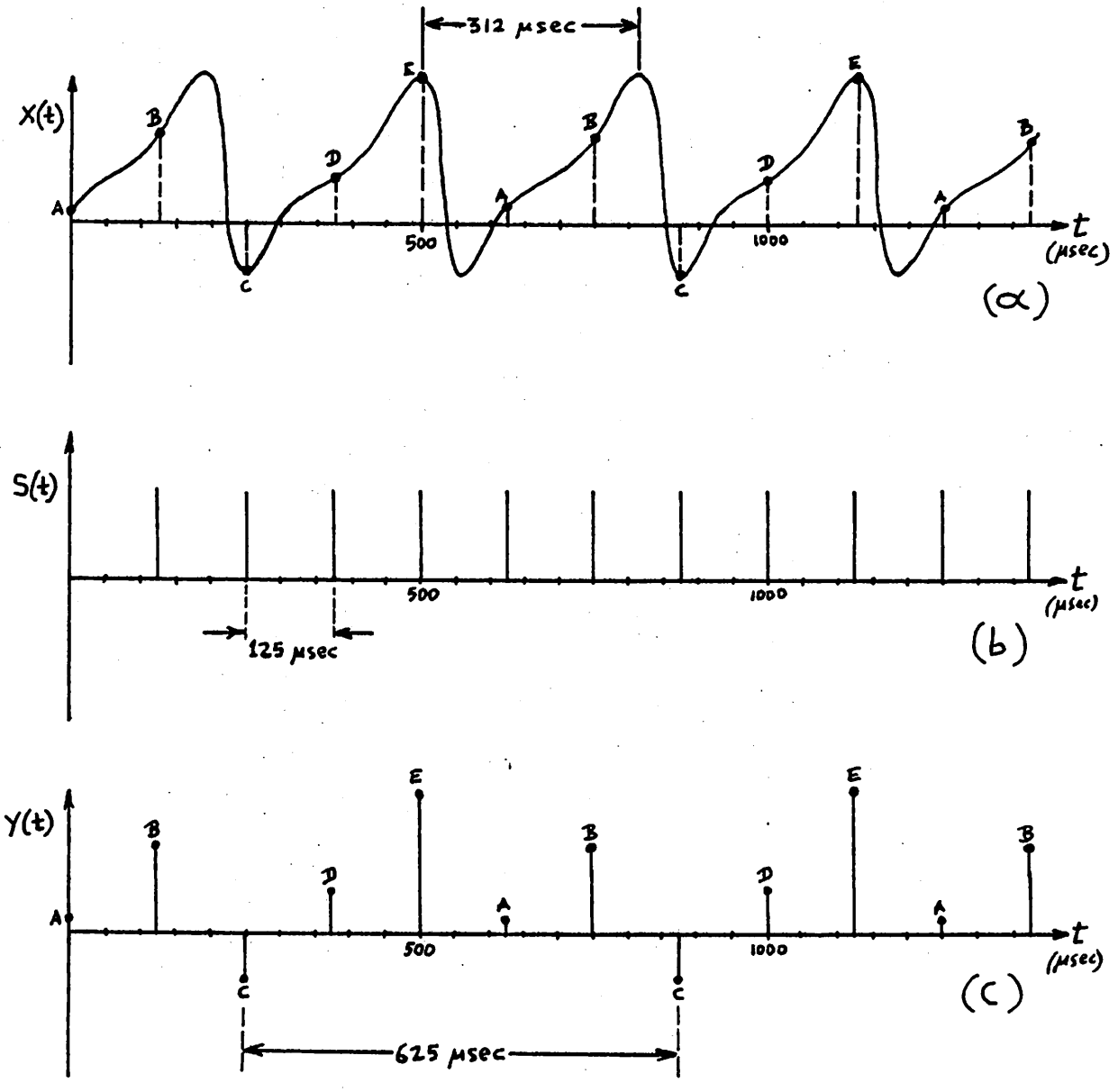


Figure 2.4: Sampling a periodic waveform.
(a) Waveform to be sampled.
(b) Sampling pulse train.
(c) Sampled signal.

samples a pure 3.2 KHz sinusoid, whose spectrum is shown in Figure 2.5(a). The period of the output waveform will still be 625 μsec as above, which means that the fundamental of the output y(t) is again 1.6 KHz. The output then should consist of components at 1.6 KHz, 3.2 KHz, 4.8 KHz, 6.4 KHz, 8 KHz, 9.6 KHz and so on. This appears to contradict the sampling theorem, since the 3.2 KHz sinusoidal input is properly bandlimited to less than half the sampling rate of 8 KHz, so nothing else except 3.2 KHz should be present in the baseband. The apparent contradiction is resolved when one actually evaluates the components of the Fourier series representing y(t): the coefficients for the components at 1.6 KHz, 6.4 KHz, 8 KHz, 9.6 KHz, etc. turn out to be zero, and nonzero components are only present at 3.2 KHz, 4.8 KHz, 11.2 KHz, etc. This is precisely what one gets if the translated spectra of Figure 2.2 are considered for this case. The result is shown in Figure 2.5(b).

The conclusion is as follows: Although the period of the output waveform y(t) of a sampler might suggest that subharmonics might be present, a calculation of the Fourier coefficients for these components will show that their amplitude is zero, if the input is properly bandlimited to less than half the sampling rate. If the calculation of the amplitudes of these subharmonics turns out non-zero values, then these subharmonics are due to aliasing (see section 2.2.2). This will be the case if the input does not satisfy the constraints stated in the sampling theorem.

As it will be seen, such subharmonics and, in general, extraneous components are not only present in PCM systems, but in fact it is impossible to avoid them, even in principle. This will be discussed in section 2.3.10.

2.3 PULSE CODE MODULATION (PCM)

2.3.1 Introduction

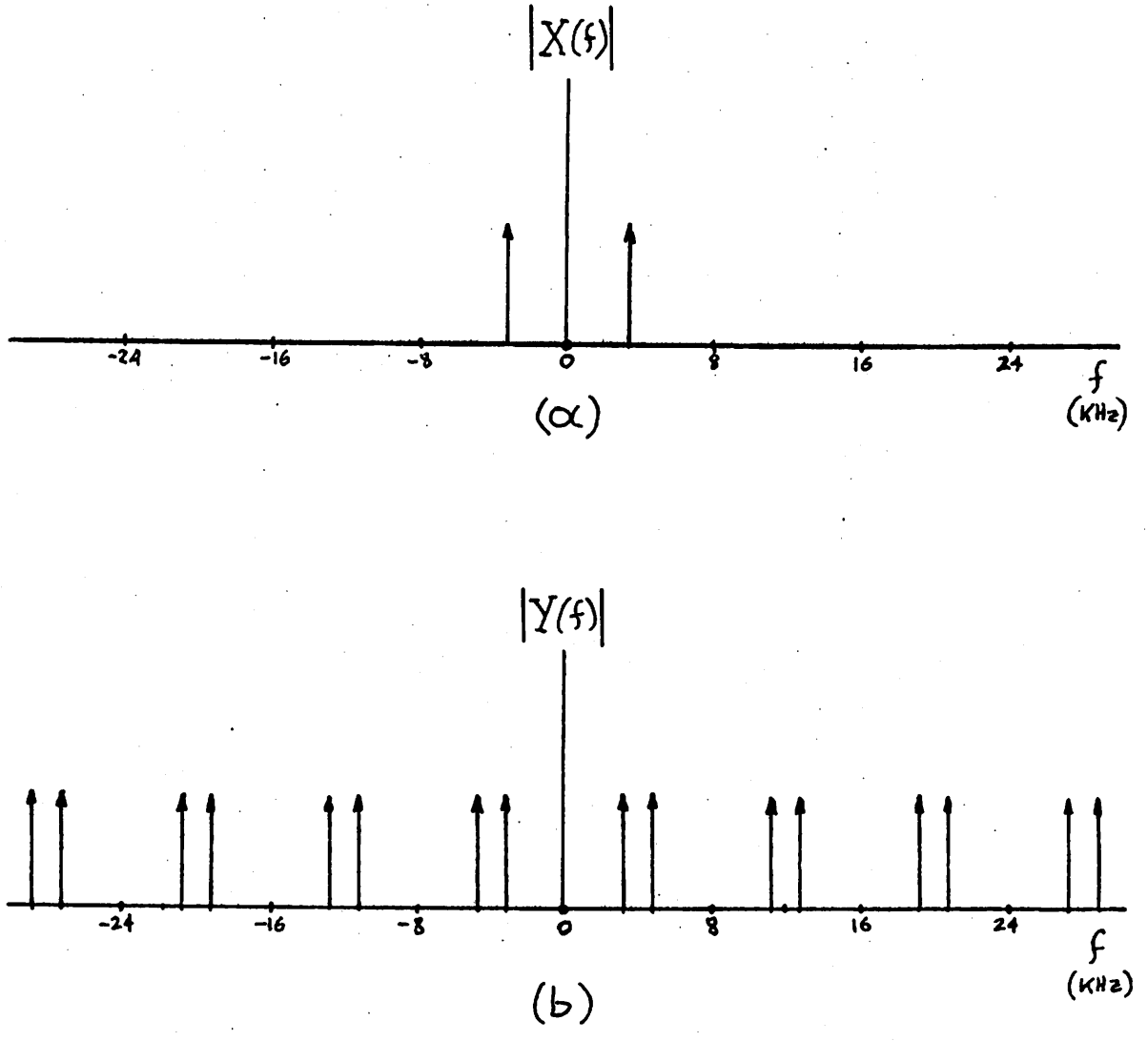


Figure 2.5 Sampling a 3.2 KHz sinusoid at a rate of 8 KHz.
(a) Input spectrum.
(b) Spectrum of sampled signal.

As has already been mentioned, the basic difference between PAM and PCM is the form of the transmitted signal: in the latter case it is digital. In the PCM system shown in Figure 2.1(b) the digital signal transmitted consists of words, each of which represents one sampled value of the original signal. The digits of each word can be sent either in parallel or sequentially. In either case, if a word consists of n digits and each digit can have b different values, there exist a total of b^n different words that can be transmitted. In the systems we will consider binary digits are used (b=2). Since the total number of different words that can be sent is finite, each word will have to represent not a single analog value of the signal, but a whole range of values. The range of the analog input will therefore have to be divided into 2^n intervals (or "quanta") and any value falling in a specific interval will be represented by a single digital word: the one representing that interval. This division of the input range into intervals is called quantization and can be uniform or nonuniform according to whether these intervals are of equal length or not.

2.3.2 The A/D Converter (ADC)

The static characteristic of an A/D Converter (ADC) is an adequate description of its operation in the case where no dynamic effects or hysteresis are present. An example is shown in Figure 2.6(a), for the case of 3 binary digit word representation and for uniform quantization of the input range. The horizontal axis is continuous and represents the analog input. The end points of each interval on this axis are called the decision levels. The vertical axis is discrete, and represents the digital words at the output of the ADC.

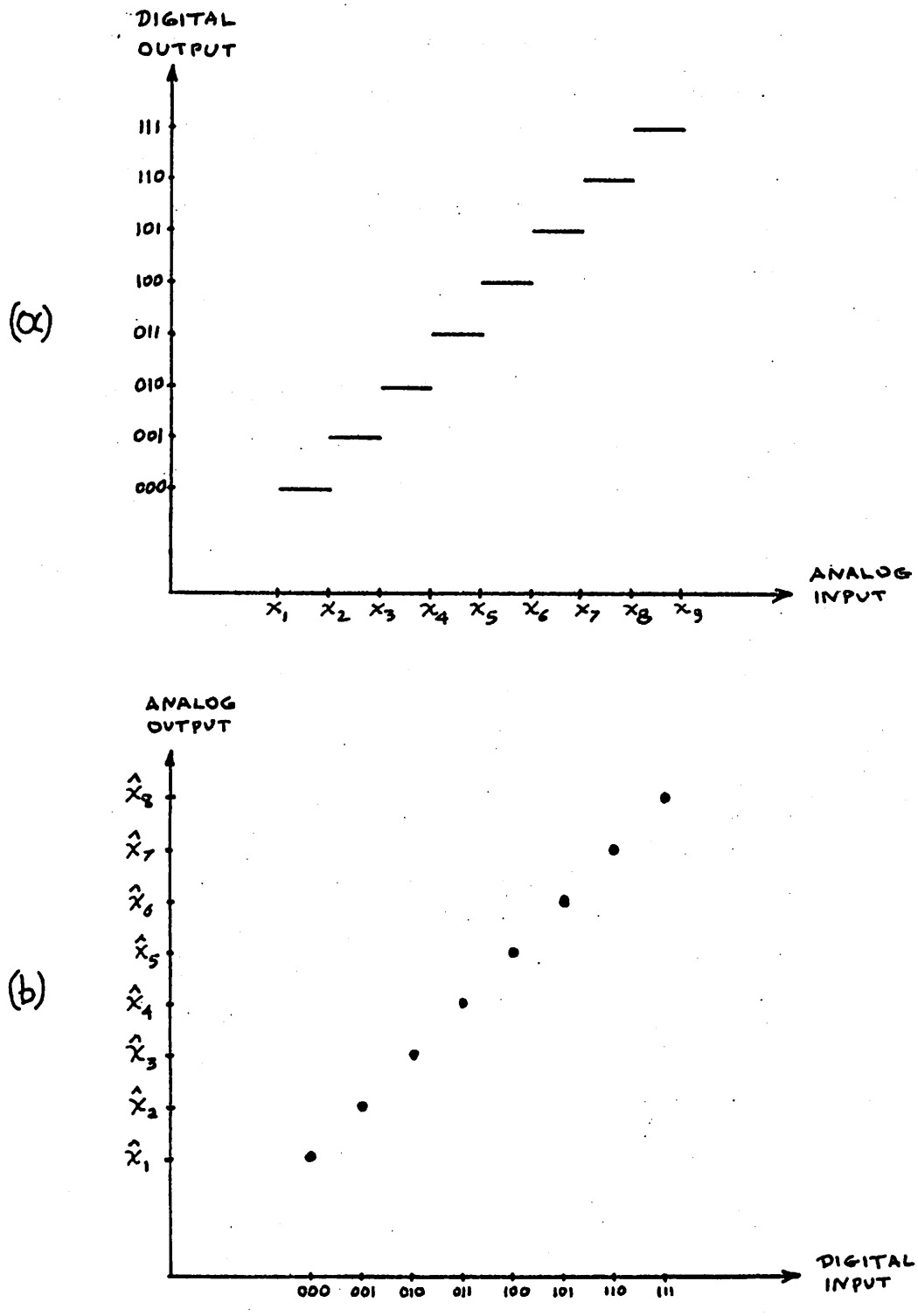


Figure 2.6: (a) Static characteristic of an ADC
(b) Static characteristic of a DAC

2.3.3 The D/A Converter (DAC)

The static characteristic of a D/A Converter (DAC) describes its performance adequately in the absence of hysteresis and dynamic effects, as in the ADC case. The example shown in Figure 2.6(b) is again for 3 binary digit words and uniform quantization. The horizontal axis is discrete and represents the input digital values. The vertical axis is also discrete, and represents the corresponding analog values at the output of the DAC. It is intuitively clear that in this case the output levels should be equal to the midpoints of the corresponding input intervals of the ADC, if the overall error for the ADC-DAC combination is to be minimized. These considerations will be made in more precise terms in section 2.3.4.

2.3.4 The ADC-DAC Combination

Consider an ADC whose useful input range extends from x_L to x_H. This range is quantized into 2^n intervals, where n is the number of bits in the output digital word. Let x_k be the decision level coinciding with the beginning of the kth interval, where k=1, 2,..., 2^n. Let I_k be the interval (x_k, x_{k+1}). Let the output digital word be D_k, and consider also a DAC, which upon the presence of D_k at its input, develops a corresponding analog output level $\hat{x}_k$. Assume that the mappings $\{I_k\} \rightarrow \{D_k\}$ and $\{D_k\} \rightarrow \{\hat{x}_k\}$, defined by the ADC and the DAC, are one-to-one. Then each input interval I_k can be considered as being directly mapped into a corresponding value $\hat{x}_k$ if one supresses the intermediate digital word D_k, and this mapping will also be unique. In this light, as long as one is not interested in what happens in the digital transmission channel (which in any case has been assumed noiseless), one can consider the cascode combination of the ADC and the DAC shown in Figure 2.5(a) as a single two-port, as shown in Figure 2.7(b). The static characteristic of this two-port is shown in

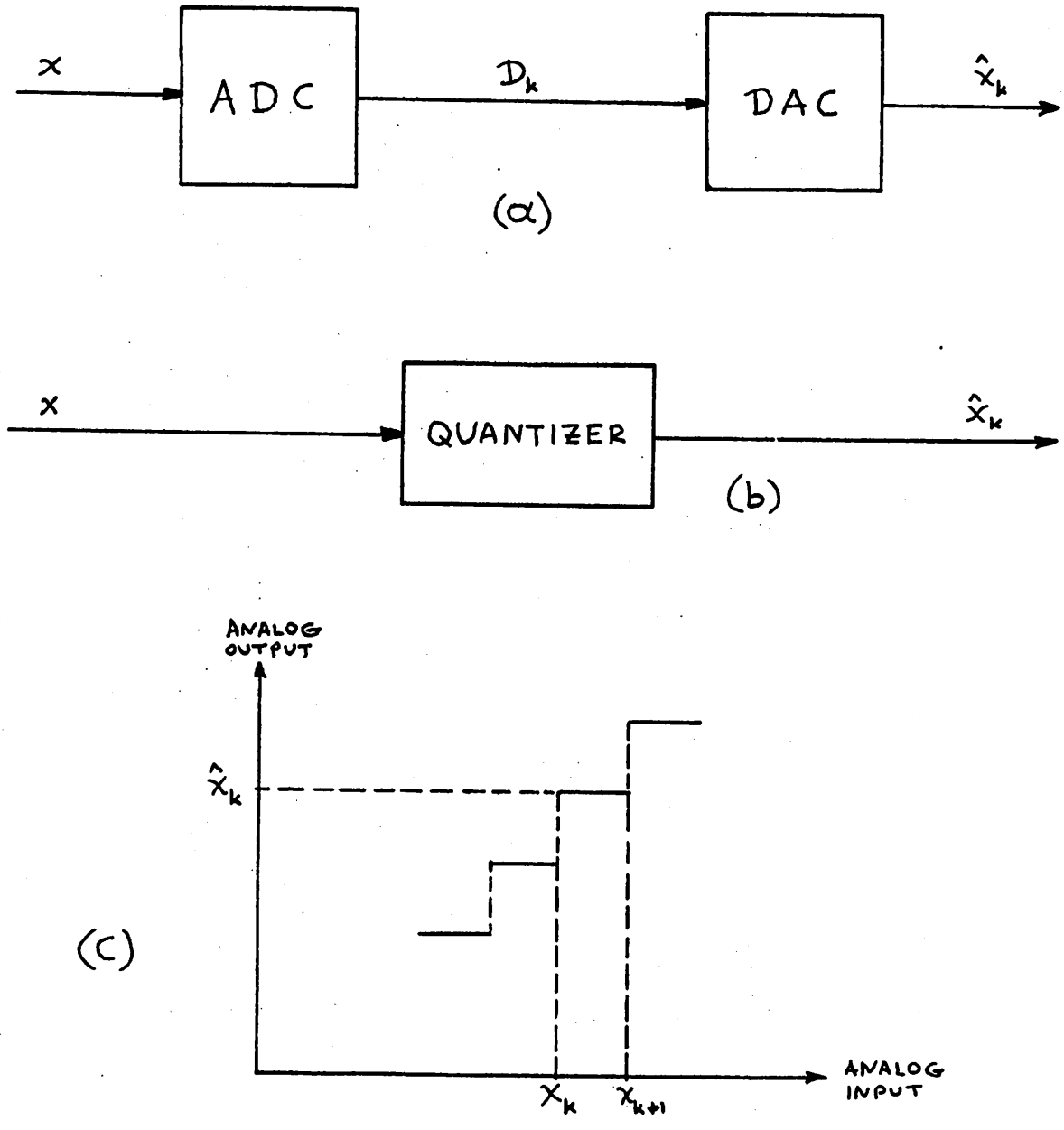


Figure 2.7: (a) An ADC-DAC combination
(b) An equivalent quantizer
(c) The quantizer characteristic

Figure 2.7(c), and has been derived from the two individual characteristics for the ADC and the DCA. In this characteristic both axes represent analog quantities with the horizontal axis being continuous and the vertical axis discrete. All of the quantizing information is present in this plot, and a two-port with this kind of characteristic is called a quantizer. In fact, in the literature a quantizer is defined as an analog input-analog output two port having a staircase characteristic, without reference to ADC's and DAC's. Quantization can be performed perfectly well by a nonlinear resistive network having the characteristic of Figure 2.7(c), and without any ADC or DAC.

In a practical PCM system, the analog values to be converted into digital words are applied to the ADC at a rate f_s, and the corresponding values are subsequently generated at the output of the DAC at the same rate. For the same input then, the outputs generated by the systems shown in Fig. 2.7(a) and 2.7(b) are identical, except for a pure delay. All the results we will present in this chapter are not altered whether the delay is present or not, and we will therefore use the simple quantizer instead of the ADC-DCA combination in our discussion.

2.3.5 Quantization

In our discussion of errors due to quantization, we will consider that the input to the quantizer is a random process. Moreover, for the systems we are concerned with, we are justified to make the additional assumption that these processes are ergodic, which simply means that for these signals time averages and statistical averages are identical. The random process approach will be used even in the case of pure sinusoidal inputs, for, as will be shown, the harmonic distortion at the output can be calculated statistically, assuming the input is a random-phase sinusoid. This repre-

sents considerable calculation ease relative to the lengthy Fourier analysis that might otherwise be used. The savings in calculation time will be appreciated in Chapter 3, where the computer simulation of PCM systems will be discussed.

No sampling will be considered in this section, this to be undertaken in section 2.3.11. We will only consider the error introduced by the quantizer of Figure 2.7(b), which, for our purposes, corresponds to the ADC-DAC combination. Referring to Figure 2.7(c), assume that the input x falls in the interval (x_k, x_{k+1}). Then its output representation will be $\hat{x}_k$, and the error will be $\hat{x}_k - x$. If the probability density of x is p(x), one can calculate the mean-square error contribution σ_k corresponding to this interval as follows:

$$\sigma_k = \int_{x_k}^{x_{k+1}} (\hat{x}_k - x)^2 p(x)\,dx \tag{2.6}$$

The total mean-square error due to the contribution of all intervals, often called "quantizing distortion" will then be:

$$\sigma = \sum_k \sigma_k = \sum_k \int_{x_k}^{x_{k+1}} (\hat{x}_k - x)^2 p(x)\,dx \tag{2.7}$$

If the intervals are sufficiently small and p(x) does not vary significantly within any particular interval, let p_k be the approximately constant value of p(x) in the interval (x_k, x_{k+1}). Then equation (2.7) becomes:

$$\sigma = \sum_k p_k \int_{x_k}^{x_{k+1}} (\hat{x}_k - x_k)^2\,dx \tag{2.8}$$

$$= \frac{1}{3}\sum_k p_k \left[(\hat{x}_{k+1} - x_k)^3 - (\hat{x}_k - x_k)^3\right] \tag{2.9}$$

We want to choose the output levels $\hat{x}_k$ so that the error σ is minimized. It is easily seen that $\hat{x}_k$ should be chosen as $(x_k + x_{k+1})/2$, and therefore the output levels should be in the middle between the corresponding decision levels. In this case, eq. (2.9) further reduces to:

$$\sigma = \frac{1}{12}\sum_k p_k (x_{k+1} - x_k)^3$$

$$= \frac{1}{12}\sum_k p_k \Delta_k^3 \tag{2.10}$$

where Δ_k is the length of the kth interval.

For any interval (x_k, x_{k+1}), $p_k\Delta_k = P_k$ is approximately equal to the probability that the input x falls in that interval, and, from equation (2.10):

$$\sigma = \frac{1}{12}\sum_k p_k \Delta_k \Delta_k^2 = \frac{1}{12}\sum_k P_k \Delta_k^2 \tag{2.11}$$

Notice that in the case of uniform quantization, where all Δ_k's are equal, this reduces to:

$$\sigma = \frac{1}{12}\sum_k P_k \Delta^2 = \frac{\Delta^2}{12}\sum_k P_k. \tag{2.12}$$

If p(x) is negligible outside the quantized input range, then $\sum_k P_k$, being the probability that the signal falls somewhere in the input range, is close to 1. The mean square error for uniform quantization then is:

$$\sigma = \frac{\Delta^2}{12} \tag{2.13}$$

independently of the form of p(x) inside the input range.

In the above discussion, and throughout this chapter, we have assumed that the probability of x falling outside the quantized range is negligible.

Thus, we are not considering peak clipping which can produce heavy distortion. For a discussion of this situation, see [5]. Peak clipping will be included in the computer simulation, discussed in Chapter 3.

2.3.6 Optimum Quantizing

If the probability density p(x) of the input is known, the relative interval sizes Δ_k can be selected so as to minimize the total mean square error. This is a problem of optimum quantizing, and extensive work on this subject has been done and can be found in the literature [6,7,8,9].

Assume that all values of the input in the input range (x_L, x_H) are equally likely. Then p(x) is constant within that range, say p(x) = c. Equation (2.10) then becomes:

$$\sigma = \frac{c}{12} \sum_k \Delta_k^3 \tag{2.14}$$

and it is easy to show that for a given input range and number of intervals, the above sum is minimized when all interval lengths are chosen equal, i.e. when the quantization is uniform.

In an actual telephony system, however, p(x) is far from being uniform. From equation (2.10) then it is intuitively clear that the interval sizes Δ_k should be chosen small where p(x) is high, and vice versa, in order to minimize the error σ. This makes sense, since one is trying to improve the resolution of the quantizer around the values of the input that are highly probable to occur. The quantitive aspects of the problem can be found in the references cited.

2.3.7 Quantizing Laws for Telephony

Optimum quantizing alone is not sufficient to produce a satisfactory quantizing law for telephony applications, since the complex requirements of a telephone system and the numerous compromises that have to be made in

its design are hardly described by a single probability density function p(x). Additional work has been done on this subject, including subjective evaluations, and several quantizing laws have been proposed. All these laws have in common the fact that the quantization is finer for small input amplitudes. There are two reasons for choosing such quantization:

a) Long term average studies of speech waveforms present in telephone systems have indicated that p(x) has a shape which favors small amplitudes. Both Gaussian and Laplacian functions have been proposed. In either case, the considerations given in the previous section for the minimization of the error suggest that quantization should be finer for smaller input amplitudes.

b) A telephone system is required to perform satisfactorily in a variety of individual situations. In particular, both loud talkers and weak talkers using the system should get adequate performance. This again suggests fine resolution for small amplitudes. Although human voice does not consist of pure sinusoids, sinusoidal response, as shown in Figure 2.8, is sufficient to indicate the point. In this figure, uniform quantization is compared to non-uniform quantization. Loud and weak talkers are represented by high and low amplitudes respectively. It is obvious that nearly equal signal-to-distortion ratios can be achieved for differing amplitudes in the case of Figure 2.8(b), whereas this is not true in Figure 2.8(a). The resulting signal-to-distortion ratios for these two cases are plotted versus the amplitude of the input sinusoid in Figure 2.8(c).

Consider now the average signal power at the input of the quantizer:

$$\text{Average signal power} = \int_{x_L}^{x_H} x^2 p(x)\,dx \tag{2.15}$$

where x_L and x_H are the endpoints of the useful input range, and p(x) is

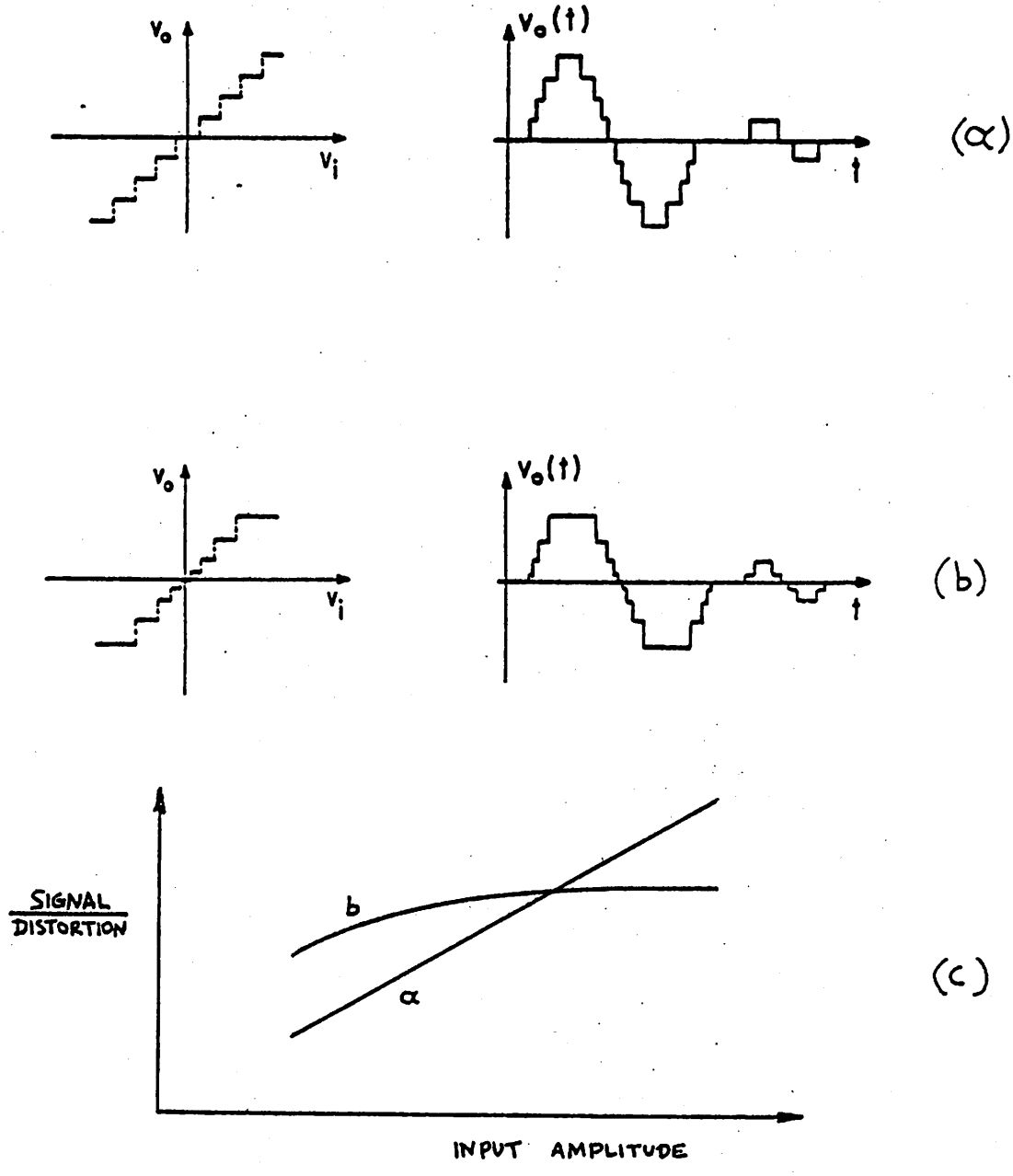


Figure 2.8: (a) Uniform quantization
(b) Nonuniform quantization
(c) Signal-to-distortion ratio vs. amplitude for the cases in (a) and (b)

assumed negligible outside this range. Assuming adequately fine quantizations, the above equation can be approximated by:

$$\text{Average signal power} \approx \sum_k x_{o,k}^2 P_k \Delta_k$$

$$= \sum_k x_{o,k}^2 P_k \tag{2.16}$$

where $x_{o,k}$ is the midpoint of the kth interval. The ratio of average signal power to quantizing distortion can then be found by using equations (2.16) and (2.11):

$$\frac{\text{Average signal Power}}{\text{Quantizing Distortion}} \triangleq \frac{S}{D} = \frac{\sum_k x_{o,k}^2 P_k}{\frac{1}{12}\sum_k (\Delta_k)^2 P_k} \tag{2.17}$$

Maintaining this ratio constant independently of the input probability density p(x) would certainly be a very desirable situation. By examination of the above equation, it is obvious that if one choses the interval lengths Δ_k to be <u>proportional</u> to their midpoint, i.e.:

$$\Delta_k = a x_{o,k} \tag{2.18}$$

where a is a proportionality constant, then:

$$\frac{S}{D} = \frac{\sum_k x_{o,k}^2 P_k}{\frac{1}{12}\sum_k a^2 x_{o,k}^2 P_k} = \frac{12}{a^2} \tag{2.19}$$

For this choice of interval lengths, then, S/D is independent of p(x). This is a very interesting and useful property.

Strictly speaking, the requirement that the interval size be proportional to the value at its middle point cannot be satisfied, as this would

require an infinite number of intervals. In addition, as far as practical circuit implementation is concerned, there is a limit to how small the intervals near the origin can be made. This results in practical quantizing characteristics in which the intervals near the origin are larger than what is dictated in the law discussed. The result of course is that the signal-to-distortion ratio will deteriorate at low amplitudes. One such quantizing law is shown in Figure 2.9.

Making the interval size vary gradually, as shown in Figure 2.9, is not easily accomplished in terms of the electronic circuitry required. Other characteristics, which approximate those described, but are at the same time simpler to implement have been proposed. In the United States, the most popular quantizing law has been selected so that it is easily realizable with the help of digital circuits. It is currently a standard used by Bell System in their PCM systems, and is shown in Figure 2.10. Rather than having the interval sizes vary gradually, they are combined into groups of sixteen intervals each. There are eight such groups (called "segments") for positive signals, and eight more for negative, each one having sixteen equal steps. As one moves from the origin towards high amplitudes, the interval size stays constant within any one segment, but increases (in fact doubles) from one segment to the next. Everything is symmetrical with respect to the origin. The two smallest intervals which are adjacent to the origin are merged into a single interval, and therefore the two segments adjacent to the origin can be considered as a single segment with a total of 31 intervals. Methods for implementing this characteristic will be discussed in this chapter as well as in Chapter 4.

2.3.8 Companding

All quantizing laws described in the previous section are implemented

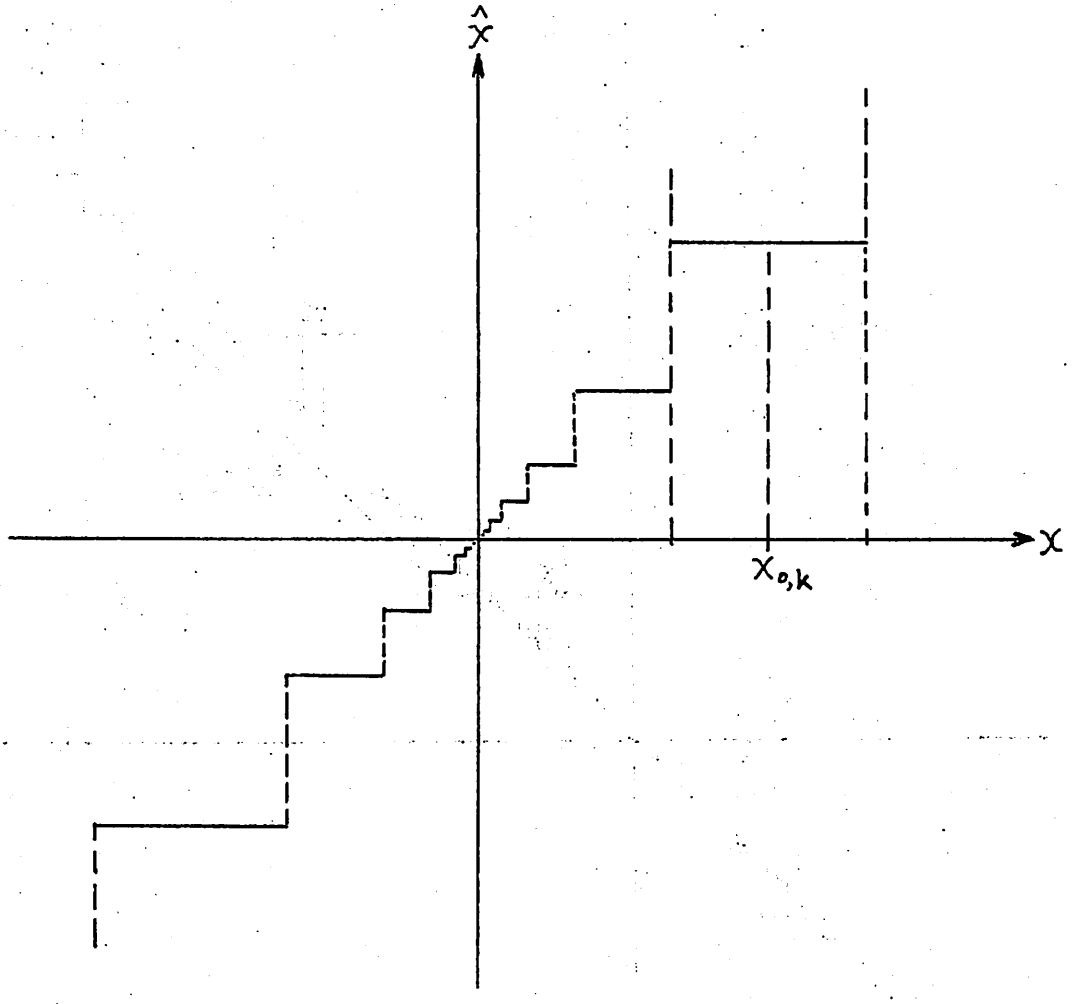


Figure 2.9: Quantizing law with interval size approximately proportional to x.

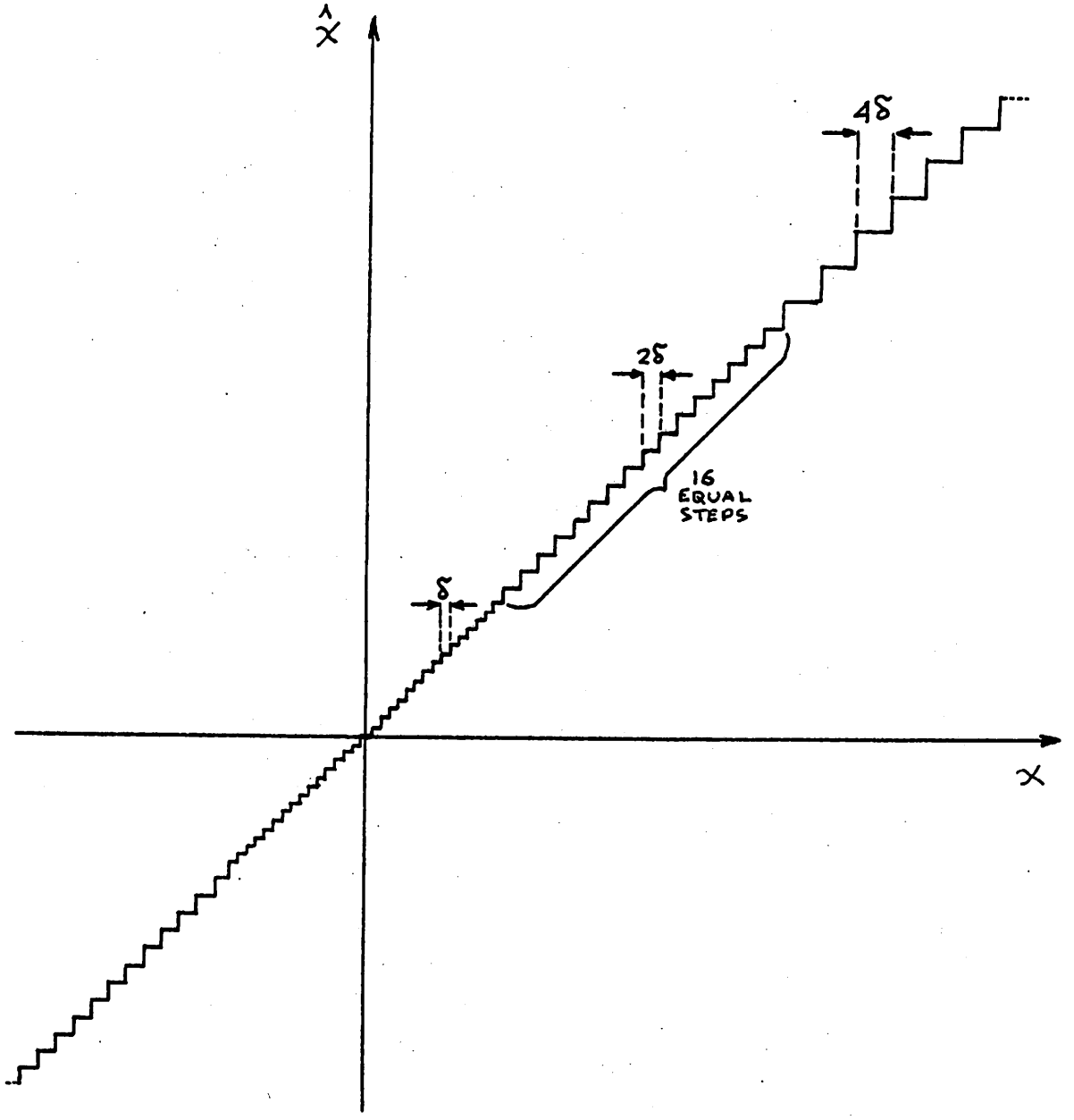


Figure 2.10: Standardized "digitally realizable" quantizing law.

by the cascade connection of an ADC and a DAC in PCM systems, the ADC being at the transmitter and the DAC at the receiver. The implementation of a uniform quantizer, shown in Figure 2.7, through a linear ADC and a linear DAC, shown in Figure 2.6, has already been discussed.

We will now undertake the realization of the nonuniform quantizing law of Figure 2.9. It is straightforward that the individual ADC and DAC characteristics required to implement this law will have the form indicated in Figure 2.11. These correspond to a form of nonuniform A/D and D/A conversion with small amplitudes favored in terms of resolution.

Another way to achieve the same quantizing law is shown in Figure 2.12. Here a uniform ADC and a uniform DAC are used. However, the input is passed through a nonlinear two-port before been A/D converted, which is called a compressor because it has the effect of reducing the useful dynamic range at the input of the ADC. The opposite is undertaken at the output of the DAC: The signal is passed through an expandor, whose nonlinear characteristic is the inverse of that of the compressor. It can be seen that the cascode of the compressor and the uniform ADC in Figure 2.12(a) is equivalent to the nonuniform ADC shown in Figure 2.11(a). Similarly, the cascode of the uniform DAC and the expandor in Figure 2.12(b) is equivalent to the nonuniform DAC of Figure 2.11(b).

For the system of Figure 2.12, the combined process of compressing and expanding is called "companding". This term is carried over to systems which do not explicitly contain compressors and expandors, as long as the overall effect is the same, as for example, the system of Figure 2.11. The effect of companding is basically the implementation of a nonuniform quantizing characteristic like the one shown in Figure 2.9.

Both varieties shown in Figures 2.11 and 2.12 have been used in practical PCM systems. The implementation shown in Figure 2.12 is more con-

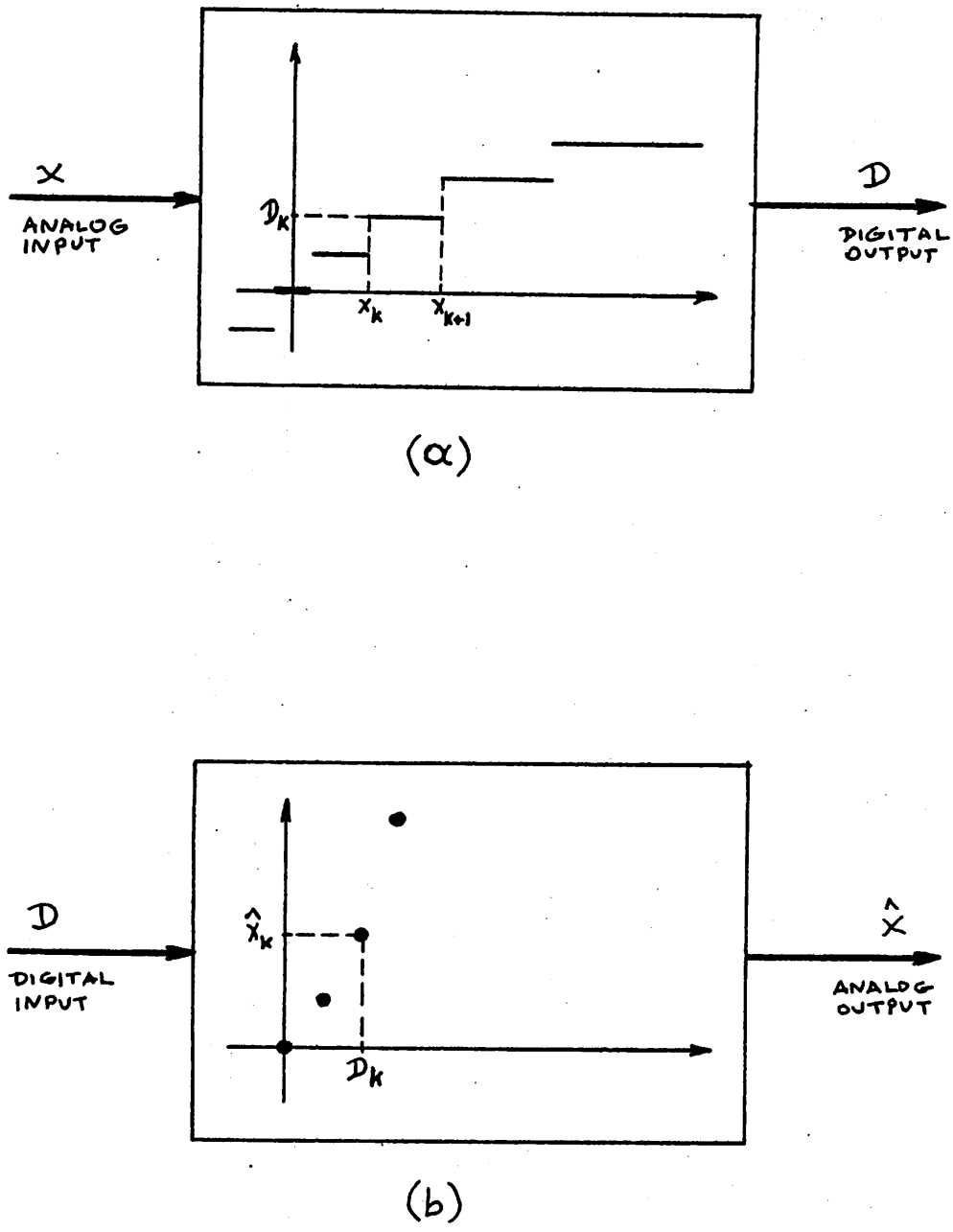


Figure 2.11: Nonuniform ADC and DCA required to implement the law of Figure 2.9.
(a) The ADC
(b) The DAC

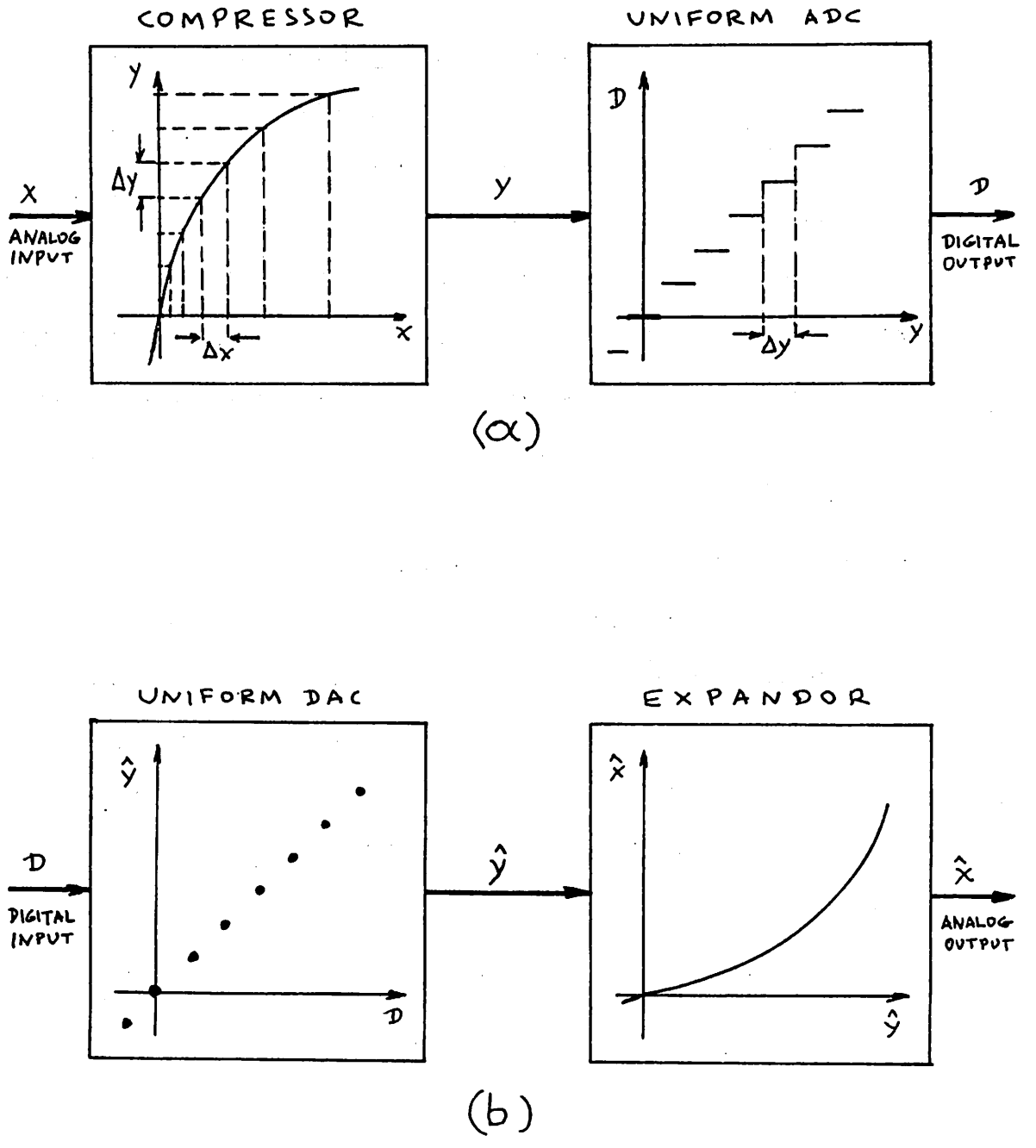


Figure 2.12: (a) A compressor and a uniform ADC.
(b) A uniform DAC and an expandor.

venient to describe in the case of quantizing laws where the interval size varies gradually, like in Figure 2.9. In such cases, the mathematical description can be in terms of the continuous compression and expansion characteristics of Figure 2.12. On the other hand, digitally realizable characteristics, like that shown in Figure 2.10, are easily described and implemented in terms of nonuniform ADC's and DAC's.

Consider first the quantizing law of Figure 2.9, implemented by the system shown in Figure 2.12. As explained in section 2.3.6, this law has the property that the interval size Δx around a point x is proportional to x itself, and this results in a signal-to-noise ratio which is independent of the probability density of the input. In the following we will limit our attention to positive x only, since everything will by symmetrical for negative x. Since the ADC is uniform, the horizontal axis y in its characteristic is divided into equal intervals Δy, as shown. The vertical axis for the compressor characteristic represents the same quantity y, and if the intervals Δy are carried over to that axis the corresponding intervals Δx along the horizontal axis will have the desired property, i.e.:

$$\Delta x = \alpha x \tag{2.20}$$

However:

$$\Delta y = \frac{dy}{dx} \Delta x \tag{2.21}$$

and, since Δy is a constant, say β, equations (2.20) and (2.21) give:

$$\frac{dy}{dx} = \frac{\beta}{\alpha x} \tag{2.22}$$

The solution of this differential equation is:

$$y = \frac{\log(bx)}{a} \tag{2.23}$$

which can also be written as:

$$y = \frac{c + \log(dx)}{a} \tag{2.24}$$

and where a, b, c, d are appropriate constants. This characteristic holds for positive x, and the symmetric of that with respect to the origin holds for negative x.

We have therefore derived the very important result that, for the signal-to-noise ratio to be independent of the probability density of the input, the compression characteristic must be logarithmic. This gives rise to all the approximately logarithmic characteristics in use in PCM systems.

Equations (2.23) ane (2.24) cannot be implemented as they are, since $\ell nx \to -\infty$ as $x \to 0$. Therefore, the compression characteristic must be modified for small values of x. The two most widely used approximations to the logarithmic laws will be discussed below. For simplicity, we will assume that x is restricted to the range $|x| \leq 1$.

The "μ law". In this law, in order to avoid the divergence of log(bx) in equation (2.23), unity is added to its argument. Also, it is customary to use the symbol μ for the constant b. Finally, in order to normalize y so that y=1 when x=1, the constant α is chosen as log(1+μ). This results in the well-known "μ-law":

$$y = \frac{\log(1+\mu x)}{\log(1+\mu)} \qquad , x \geq 0. \tag{2.25}$$

and a symmetric characteristic is used for $x < 0$. This characteristic has been considered by W.R. Bennett [10] and a number of other researchers [11, 12], but one of the most detailed investigation of it in terms of the resulting signal-to-noise ratio of the corresponding quantizer has been made in a classic paper by B. Smith [13]. The degree of compression can be varied

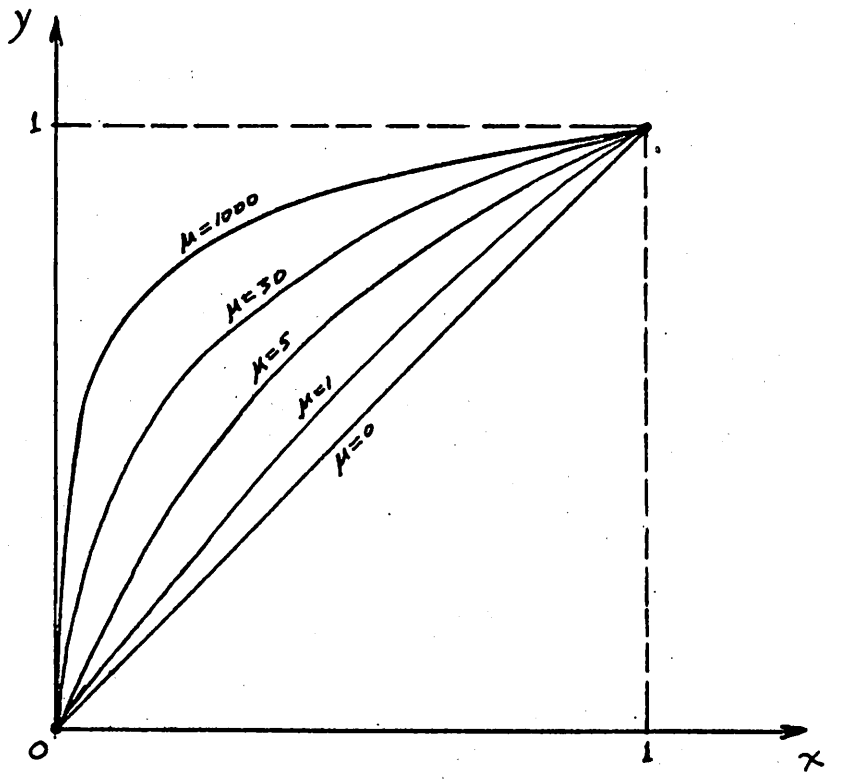


Figure 2.13: The "μ-law" compression characteristic plotted with μ as a parameter.

by varying μ, as shown in Figure 2.13. The value μ = 255 has been chosen as a standard, and the above law is in that case called the "255μ law"or the "μ255 law". A digitally realizable approximation to it is the most widely used in the United States today, and will be discussed in the next section.

The "A-law". Another widely used approximation to the logarithmic compression law can be derived from its form given by equation (2.24) by choosing c=1. The symbol A is usually used for the parameter d, and a is then chosen as 1 + log A so that y=1 when x=1. Since the resulting y still diverges for $x \to 0$, a straight line is used instead for small values of x. The resulting law is:

$$y = \frac{1 + \log Ax}{1 + \log A} \qquad \frac{1}{A} \leq x \leq 1$$

$$= \frac{Ax}{1 + \log A} \qquad 0 \leq x \leq \frac{1}{A} \tag{2.26}$$

and y is symmetrically defined for x < 0. This law is shown in Figure 2.14. A = 87.6 is a value commonly used, and digitally realizable approximations to the A-law is currently the standard in Europe [14].

In either law, if y = f(x) is the chosen compression characteristic, the corresponding expansion law will be of the form $\hat{x} = f^{-1}(\hat{y})$.

2.3.9 Digitally Realizable Encoding and Decoding Laws.

In section 2.3.6 a digitally realizable quantizing law was discussed, which was shown in Figure 2.10. The characteristics of the nonlinear ADC and DAC neccessary to realize that law are easily derived from Figure 2.10, and are shown in Figures 2.15 and 2.16.

In the encoding law of Figure 2.15 there is a total of 8 segments for each input polarity. Each segment consists of 16 equal steps, as for example is shown for segment AB. The step size within one segment is con-

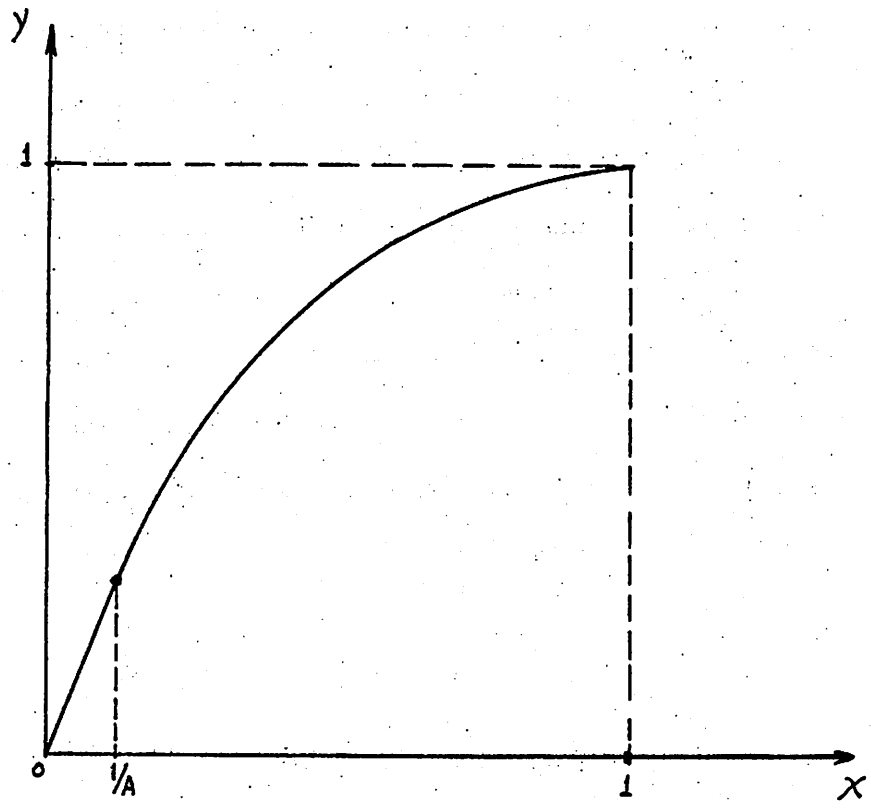


Figure 2.14: The "A-law" compression characteristic.

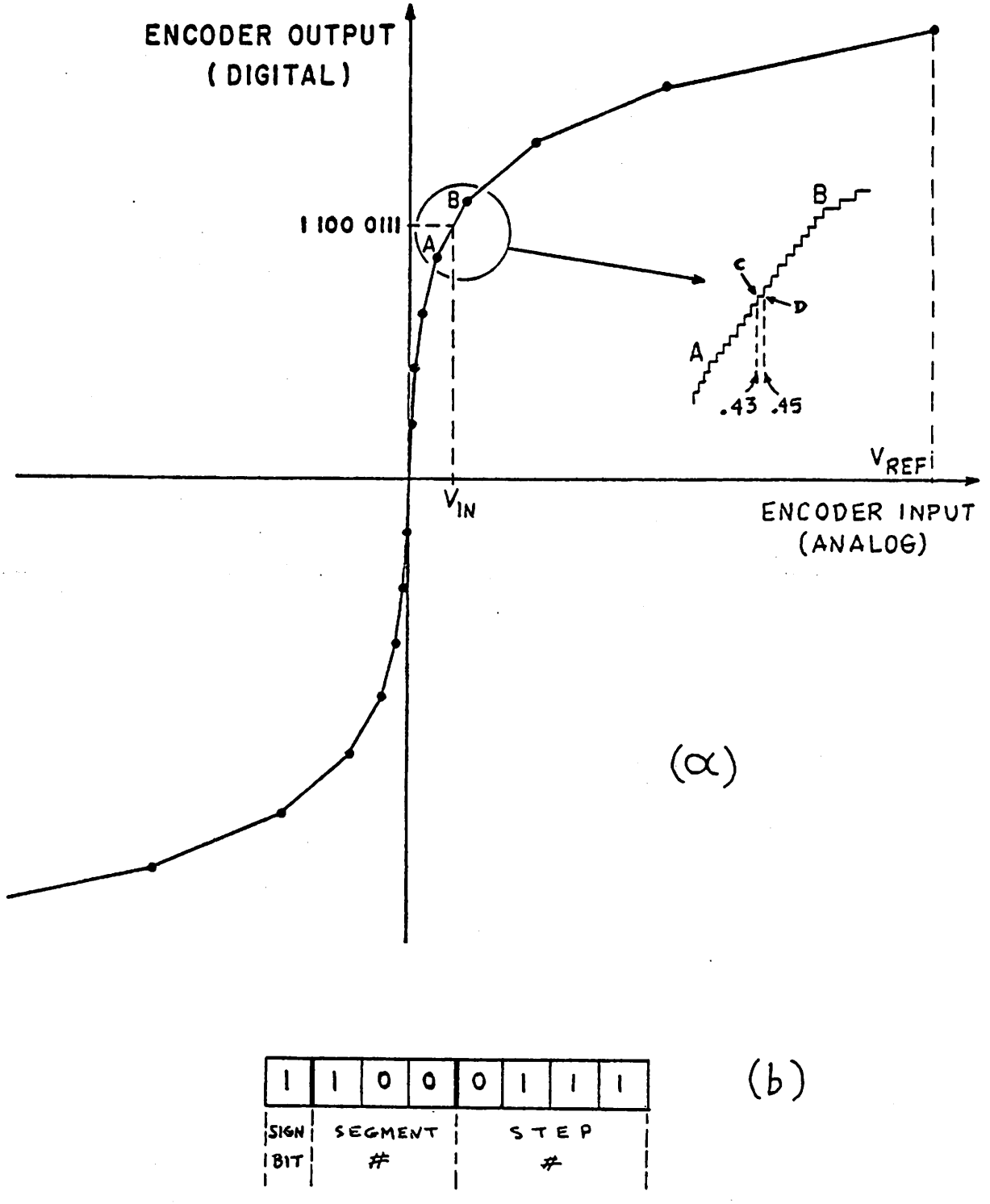


Figure 2.15: (a) The digitally realizable approximation to the 255μ encoding law.
(b) The encoding format.

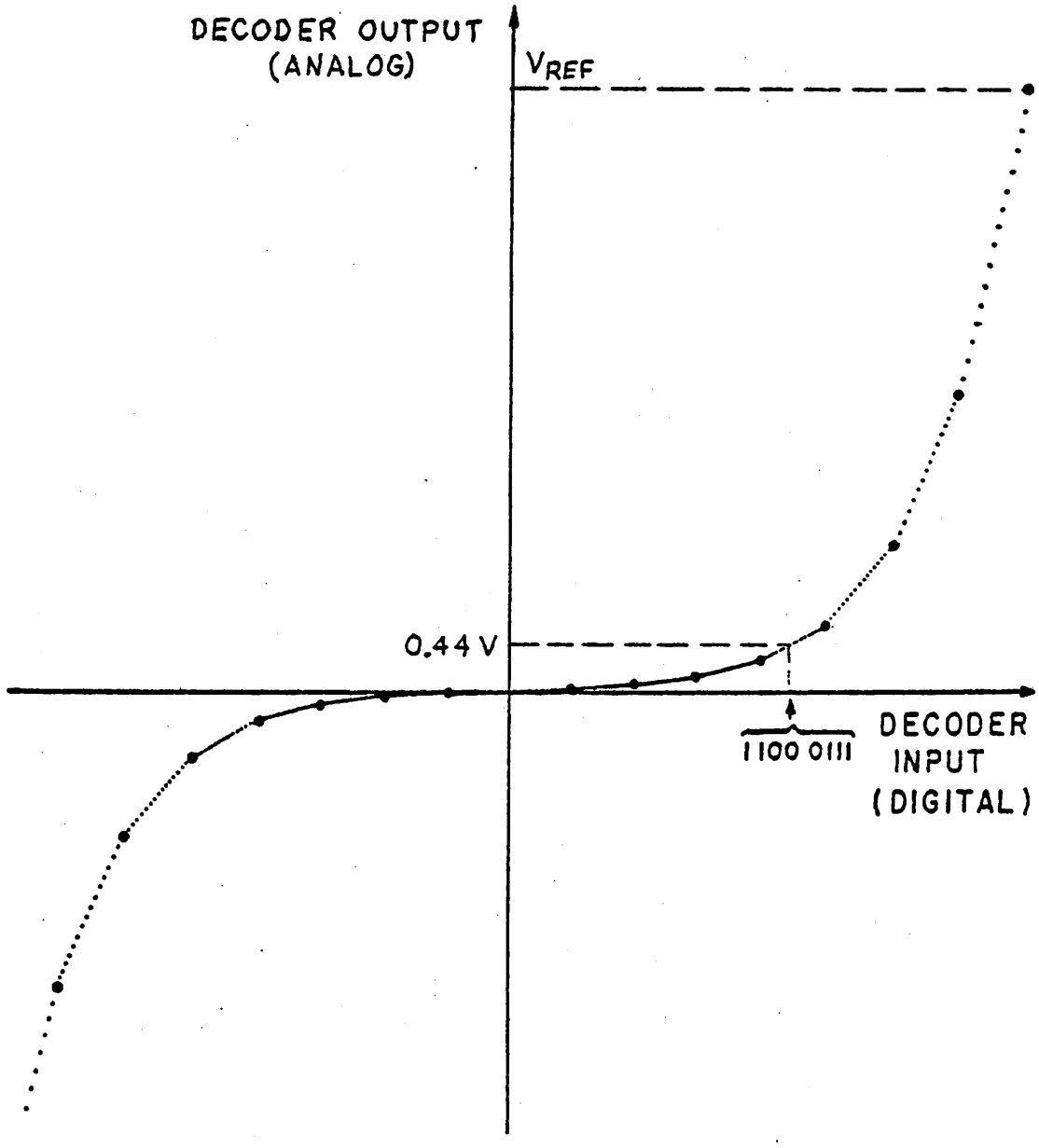


Figure 2.16: The digitally realizable approximation to the 255μ decoding law.

stant, but doubles as one goes from one segment to the next, starting from the segment adjacent to the origin and going towards higher amplitudes. Finally, the two steps adjacent and symmetrical to the origin are merged into a single step, with the origin as its middle point. The two segments adjacent to the origin can then be considered as a single segment with a total of 31 steps. There is therefore a total of 255 steps in the characteristic, and the ratio of the size of the largest step to that of the smallest is $2^7 = 128$. The decoding characteristic of Figure 2.16 is complementary to that of the encoding law just described.

If one plots the continuous 255μ law on the same plot with the digitally realizable encoding law of Figure 2.15 it will be found that it passes from the end-points of the segments. This should come as no surprise: the encoding law discussed in this section was derived from Figure 2.10, which was an approximation to the gradually varying interval size law of Figure 2.9. It will be recalled that it was precisely the law of Figure 2.9 which gave rise to the 255 μ characteristic. The encoding law of Figure 2.15 is then a segment approximation to the continuous 255 μ law, and it is called the "15-segment approximation to the 255 μ law", or the "digitally realizable approximation to the 255 μ law". This law has been standardized in the United States.

We will now consider the format of the digital word at the output of the ADC. Since there is a total of 255 intervals, an 8-bit word is needed since $2^8 = 256$. The format used for this word is shown in Figure 2.15(b). The first bit indicates the sign of the input, being 1 for positive and 0 for negative inputs. The next three bits indicate the number of the segment to which the input corresponds, with 000 representing the segment closest to the origin and 111 the longest segment. The last four bits represent the number of the step within the segment, to which the input

corresponds, with 0000 being the first step and 1111 the last. For example, if the input corresponds to the eight step of segment AB in Figure 2.15, the word at the output of the ADC will be 1 100 0111. This coding format is sometimes modified for actual transmission. We will however use it throughout our discussion, since it is completely straight-forward. Other coding formats can always be implemented with additional logic at the output of the ADC.

In Europe, a segment approximation to the A-law of equation (2.26) is used. This is shown in Figure 2.17. Again a total of 8 segments for each input polarity are used. The step size however remains the same for the four segments closest to the origin, which can be considered a single segment. With this exception, the step sizes of two adjacent segments are again related by a factor of 2. This law is called a "13-segment approximation to the A-law" or a "digitally realizable approximation to the A-law".

The two laws described above attain basically similar performance. Comparisons between the two can be found in [5] and [15].

2.3.10 Spectrum of the Quantizer Output.

Consider a sinusoidal signal $x(t) = \sin \omega t$ applied to the input of the quantizer, and the corresponding output $\hat{x}(t)$, as shown in Figure 2.18(a). The error $\hat{x}(t) - x(t)$ can be plotted by graphically subtracting the two waveforms, and is shown in Figure 2.18(b). Here, like in all sections of this chapter, it is assumed that $x(t)$ does not extend outside the quantized range. The waveform of the error has the period of the input, but, as is obvious from its shape it has a harmonic content which extents very high in frequency if the quantization is fine enough. For example, assume that the amplitude of the input covers the whole quantized range, and that the quantizer is of the "digitally realizable 255 μ law" kind,

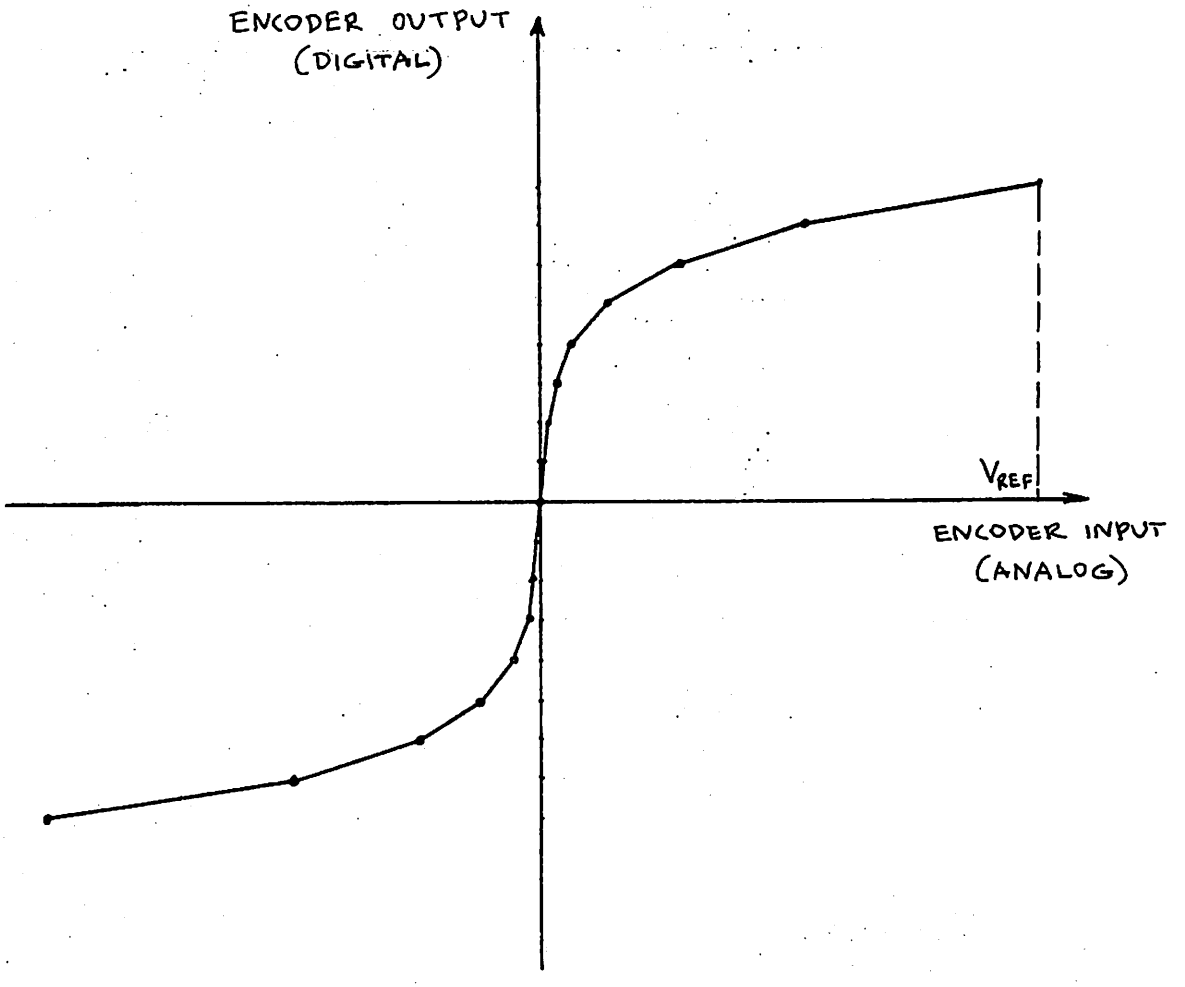
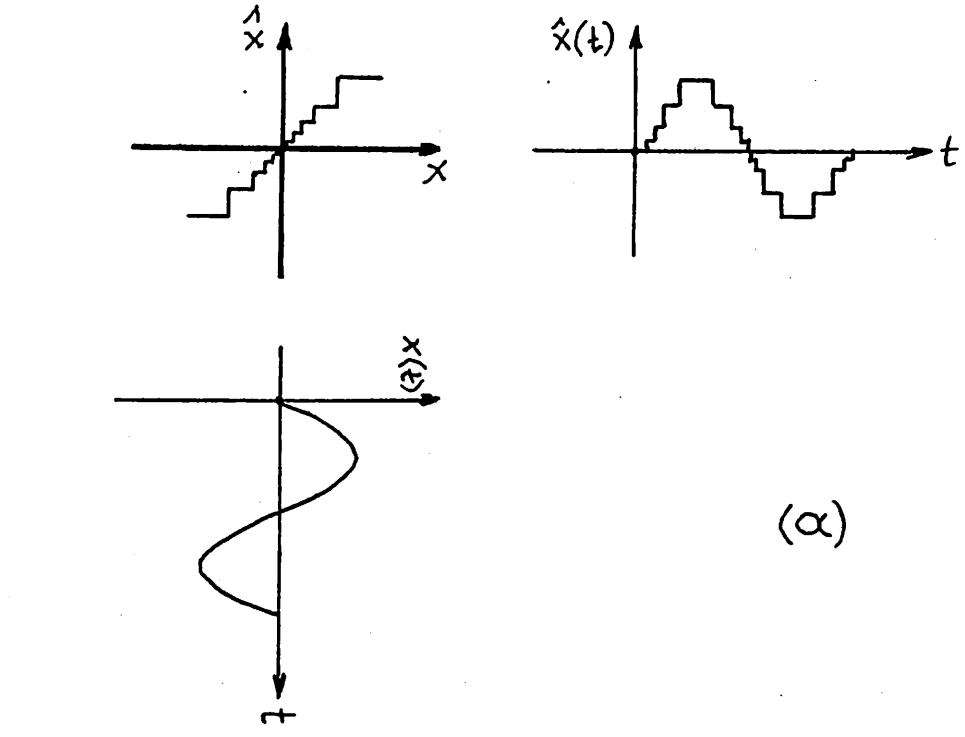


Figure 2.17: The digitally realizable approximation to the A encoding law.



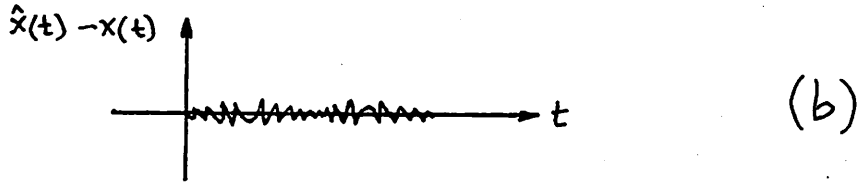


Figure 2.18: (a) Quantizer under sinusoidal excitation.
(b) Error waveform

which was discussed in the previous section. During each period of the input, x(t) goes through the total range twice, and since there are 255 steps in the quantizer characteristic, the waveform of the error $\hat{x}(t) - x(t)$ changes direction $2\times255 = 510$ times. This indicates that significant harmonics beyond the 510th harmonic can be expected. Also, for adequately fine quantization the power in the harmonics will be much smaller than that in the fundamental, this power being distributed among the large number of harmonics present.

The intuitive ideas presented above are supported by the results of rigorous treatments found in the literature. Especially in the case of bandlimited, nonperiodic signals, Bennett[16] and Velichkin [17,18] have investigated the output spectra of quantizers and have showed that for practical purposes they are flat. For example, when a 3 KHz bandlimited noise is applied to a quantizer, the output power density spectrum has only droped by a factor of 2 at a frequency of 450 KHz. The "flatness" observed in this cases has resulted in using the term "quantizing noise" for the quantizing error, although strictly speaking this is not a correct term to use. When sampling is combined with quantizing, a subject to be discussed in the following section, the justification for treating the quantization error as noise will become more apparent.

2.3.11 The Combined Effect of Sampling and Quantizing.

The performance of a complete PCM system, shown in Figure 2.19(a), will now be discussed. The ADC and DCA can be considered as a quantizer shown in Figure 2.19(b). An investigation of this system can proceed as follows: The sampled values, altered by the nonlinear quantizer characteristic, can be represented by a time function whose spectrum can subsequently be examined. A less tedious procedure is obvious when one compares Figures 2.19

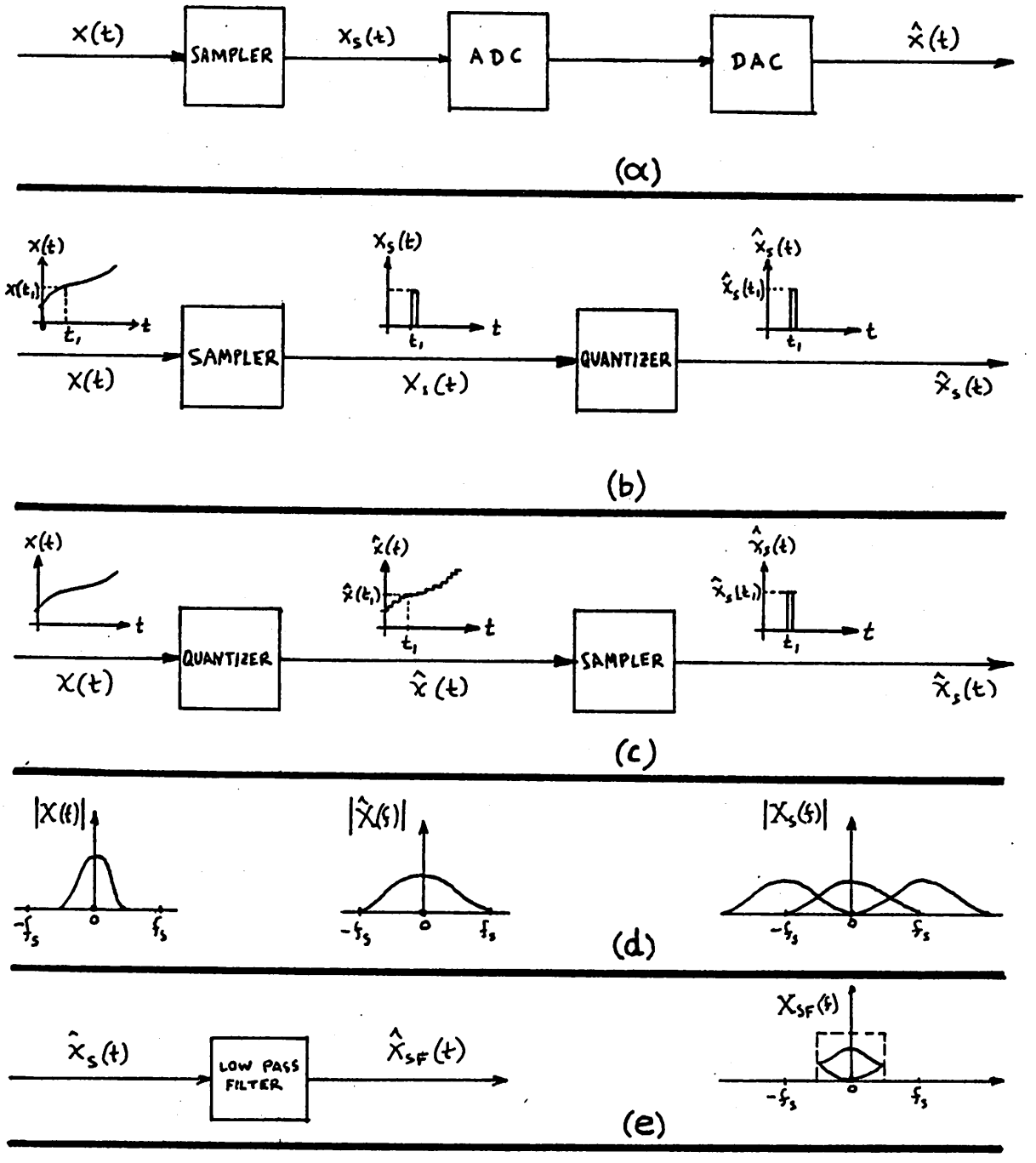


Figure 2.19: (a) A PCM system.
(b) The same system with a quantizer representing the ADC-DAC combination.
(c) The system after the quantizer and the sampler have been interchanged.
(d) Spectra for the system in (c).
(e) Low pass filtering the output in (c).

(b) and (c). From the details given in these Figures it is apparent that the two outputs are identical. It turns out that the investigation of the system in (c) is simpler, so we will undertake it below, and the results obtained for the output of this system will apply equally well for the output of the systems in (b) and (a).

Consider an input x(t) which is properly bandlimited to less than half the sampling rate, as shown in (d). If the quantizer was absent, x(t) could be recovered from the output of the sampler by low-pass filtering. However, the presence of the quantizer will cause the signal spectrum to spread to frequencies larger than $f_s/2$, as shown. For simplicity, we will assume that this spread extends to $\pm f_s$. When $\hat{x}(t)$ is sampled, the resulting waveform $\hat{x}_s(t)$ will have a spectrum as shown in (d), with the spectrum of $\hat{x}(t)$ translated by multiples of the sampling frequency, and therefore aliasing will be present. Actually, the quantized signal $\hat{x}(t)$ contains components which extend to frequencies far beyond f_s making its spectrum essentially "flat" for practical purposes. Therefore in the spectrum of $\hat{x}_s(t)$, even translations at very high multiples of f_s will have tails which extend down to the baseband, and the aliasing will be the combined effect of all of these. After low-pass filtering $\hat{x}_s(t)$, as shown in Figure 2.19(e), it can be seen that the tails of $|\hat{X}(f)|$ that fell outside the passpand and were therefore cutoff, have efectively been replaced by the corresponding tails coming from the translations of $|\hat{X}(f)|$ at multiples of f_s. It will be seen that under certain conditions, the error power of $\hat{X}_{SF}(f)$ is approximately equal to the error power of $\hat{X}(f)$ [5]. This is very fortunate, since under these conditions the error at the output of the low-pass filter can be estimated by simply looking at the error at the output of the quantizer in Figure 2.19(c).

The conclusion is that in a PCM system, even if one starts with a

"properly bandlimited" signal, the nonlinearities of the quantizer will create additional frequency components to make aliasing unavoidable. If one filters $\hat{x}_s(t)$ now, as shown in (e), some of the extraneous components remaining in the baseband will be due to quantization, and some due to aliasing.

Now consider a situation where a pure sinusoidal input x(t) of frequency f_x = 3.2 KHz is quantized and then sampled at a rate f_s = 8 KHz. The output of the quantizer will contain components at $\pm nf_x$, n = 0, 1, 2, ... After sampling, the translated spectra at multiples of f_s will contain components at $(\pm nf_x)$, $(\pm f_s \pm nf_x)$, $(\pm 2f_s \pm nf_x)$, etc. A graphical superposition of these spectra will show that the component closest to, and distinct from, f = 0, is at 1.6 KHz. The output of the sampler can therefore be represented by a Fourier series with a fundamental frequency of 1.6 KHz, all other components representing harmonics of this plus a DC component and its translations. These results are precisely what was obtained in section 2.2.3 with reference to Figure 2.4 from time domain considerations. The waveform x(t) sampled there, and the quantized signal $\hat{x}(t)$ sampled in the example described above have one thing in common: both have spectra which contain components at $\pm$ n 3.2 KHz, n = 0, 1, 2, ...

Although the kind of considerations given so far in this section are very useful in understanding a PCM system, they are almost useless for practical design purposes. To show this, assume that the input frequency of 3.2 KHz is changed by 0.1 Hz. The fundamental of the corresponding output $\hat{x}_s(t)$ can easily be determined as explained in section 2.2.3, and is found to be 0.1 Hz. This means that a 0.01% change of the input frequency made the fundamental of the output change by more than 10^4 times! These numbers become even more impressive if smaller changes

are considered. So, although all useful properties of the output remain practically unaltered by minute changes of the input frequency, its Fourier series representation changes completely. Therefore, the exact calculation of the individual harmonics is not only elaborate, but for all practical purposes meaningless as well.

Much simpler and meaningful calculations can be made if one regards the quantizing error as noise, as explained in section 2.3.9. For non-periodic signals, this assumption is very well justified. This is explained in Figure 2.20. Consider the quantizer output as consisting of the input $x(t)$ plus the error $\hat{x}(t) - x(t)$. Sampling $\hat{x}(t)$ then can be considered as the sampling of a signal $x(t)$ plus some "noise", $\hat{x}(t) - x(t)$. In other words, if $g_s(\cdot)$ denotes the sampled version of a function $g(\cdot)$, we have:

$$\hat{x}_s(t) = x_s(t) + [\hat{x}(t) - x(t)]_s \tag{2.27}$$

Consider the last term of this equation. It represents the sampling of the quantizing error shown in Figure 2.20(c). Benett [16] and Velichkin [17,18] have investigated such sampling and have shown that the samples of this quantizing error are practically uncorrelated, resulting in a spectral power density which is essentially flat.

If now the input is periodic, one can show that as long as the input fundamental and the sampling rate are not simply related, the resulting spectrum at the output of the sampler can be considered "flat" for measurement purposes. Cattermole [5], based on a work done by Bennett [17], has calculated that for 128-step uniform quantizing, as long as the correlation of the input signal is less than 0.9999, the correlation of the quantizing noise samples will be less than 0.0001. Even for a sinusoidal input, the combined effect of thermal noise, time jitter etc. would usu-

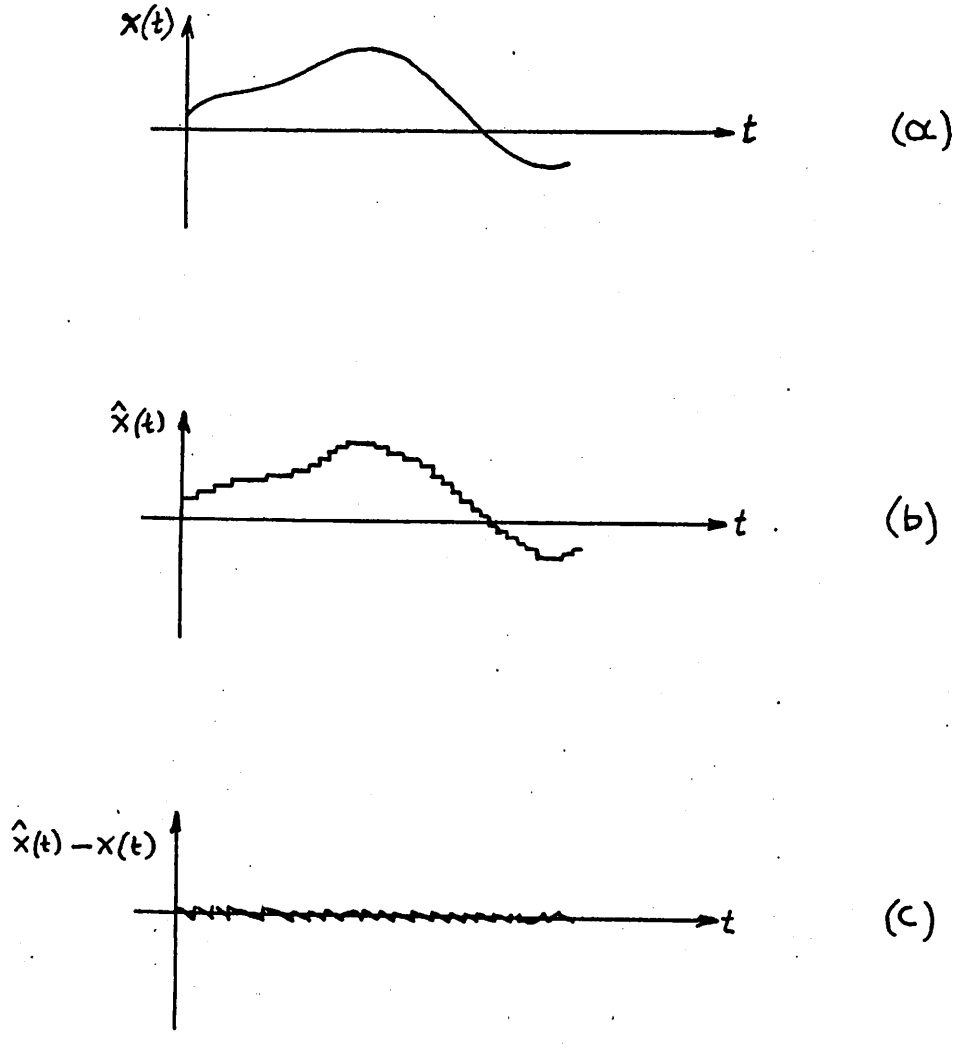


Figure 2.20: (a) Input signal.
(b) Effect of quantization.
(c) Quantizing error.

ally reduce the correlation of the input so that the above results are valid, and then the error can again be treated as noise in several cases. Experiments performed both as part of this research effort and elsewhere [19] have shown that, under sinusoidal excitations, the distortion measured after quantizing, sampling, and low-pass filtering, is very close to the value expected at the output of the quantizer by simulation.

2.3.12 Using a Zero-Order Hold Circuit in the Receiver.

We have so far assumed that the signal applied to the low-pass filter at the receiver in order to construct an approximation of the original, has the form of an impulse train, with the strength of each impulse representing one quantized sample value of the original input. In practice this can at most be approximated by a train of narrow pulses having a flat top, whose height represents the quantized sample value. We now undertake the investigation of the error introduced by the finite width of these pulses.

Consider the familiar impulse train representing the sample values, as shown in Figure 2.21(a). We can produce the finite width pulses described above by passing the impulses through a zero-order hold circuit as shown. This circuit has the property that, upon receiving an impulse of strength A at its input, it produces a rectangular pulse of height A and duration T, with $T \leq T_s$, where T_s is the sampling period. Therefore, if we define by $p_T(t)$ a rectangular pulse of unit height and width T centered around t = 0, the impulse response of the zero-order hold circuit will be:

$$h(t) = p_T(t - \frac{T}{2}) \tag{2.28}$$

The Fourier transform of h(t) now gives the network function of the

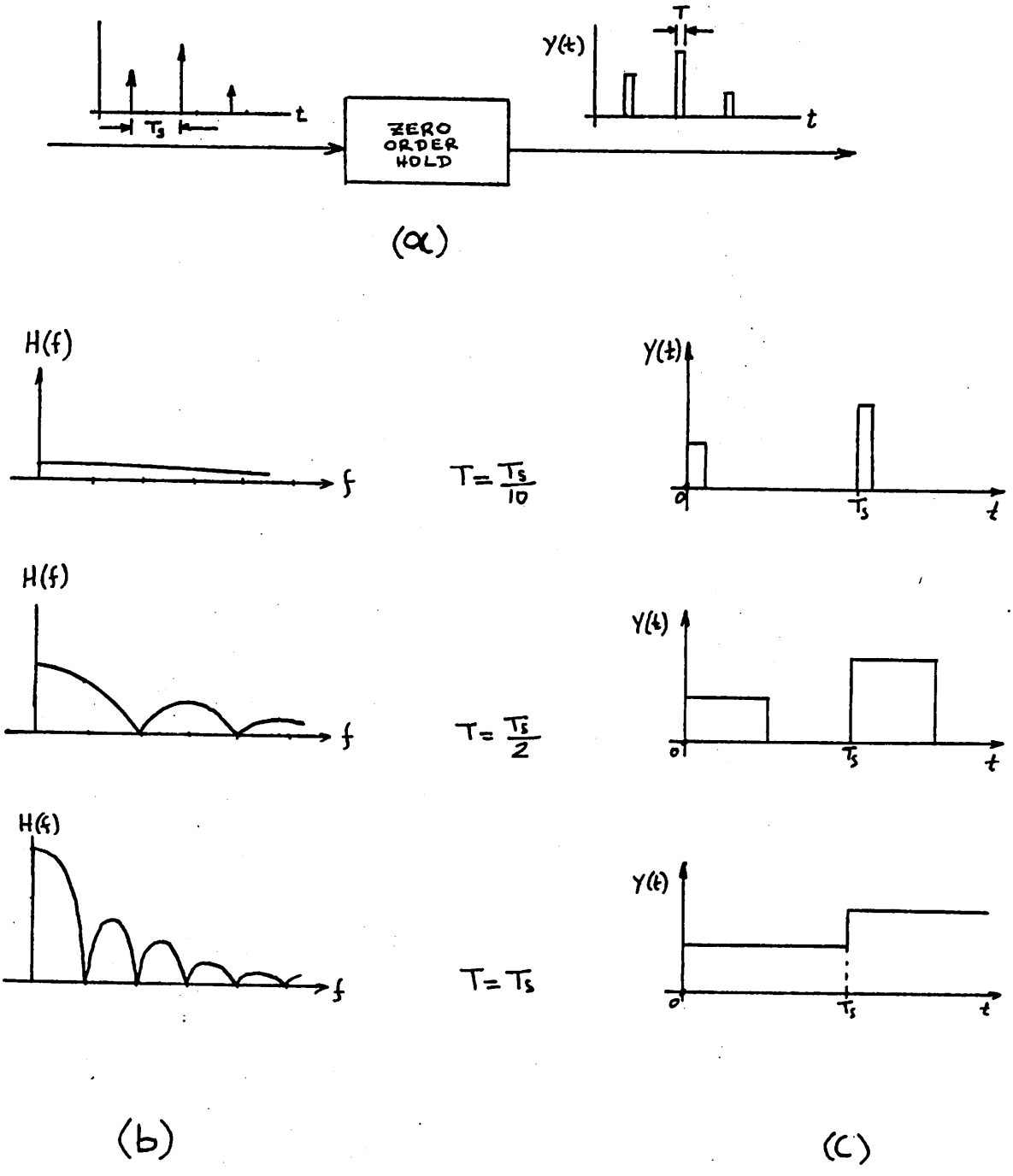


Figure 2.21: (a) A zero-order hold (ZOH) circuit.
(b) Network functions of the ZOH circuit for $T = T_s/10$, $T = T_s/2$ and $T = T_s$.
(c) Representative waveforms at the output of the ZOH circuit for the cases in (b).

zero-order hold circuit as follows:

$$H(f) = T \, \text{sinc} fT \, \epsilon^{-jnfT} \tag{2.29}$$

The magnitude of this function is plotted in Figure 2.21(b), for pulse widths of $T_s/10$, $T_s/2$, and T_s. Representative shapes of the output of the corresponding ZOH circuits are plotted in (c). It can be seen that the ZOH circuit can be viewed as a low-pass filter, and the smallest the pulse width, the flatter its frequency response will be over the base-band. However, any variation of $|H(f)|$ over that band can be compensated for by appropriate choice of the low-pass filter following the ZOH circuit. For the worse case of $T = T_s$ shown, equation (2.29) gives an attenuation of 3.9 db at $f = f_s/2$, which is the upper limit of the pass-band.

Consider now a ZOH circuit with $T = T_s$, whose input consists of a sinusoid at frequency f_1, plus noise with flat spectral density. By calculating the signal-to-noise ratio at the input and output of the filter over a bandwidth [0,w], it is seen that the improvement of the signal-to-noise ratio due to the presence of the ZOH circuit will be:

$$\frac{(S/N)_{out}}{(S/N)_{in}} = \frac{[\text{sinc}(f_1 T_s)]^2 w}{\int_0^w [\text{sinc}(fT_s)]^2 df} \tag{2.30}$$

2.3.13 Gain Tracking and Tracking Error

Assume that a PCM system is fed by a pure sinusoid. At the output, the signal consists of a sinusoid at the input frequency, plus extraneous components. The "gain" of the PCM system is usually defined as the ratio of the amplitude of the output component at the input frequency, over the amplitude of the input. It is of course desirable for this gain to stay

relatively constant, independently of the input amplitude. The term "gain tracking" is used for the deviation of this gain at any amplitude from the gain at some reference amplitude, usually chosen close to full amplitude. Full amplitude corresponds to the end of the last interval in the quantizer characteristic. Values of gain tracking different from zero are observed in PCM systems mainly due to the nonlinearities of the quantizer.

A term related to gain tracking is the "tracking error". This does not refer to the whole PCM system, but only to the quantizer characteristic, and is a measure of the deviation of the midpoints of the steps from their ideal value, which is equal to the corresponding output level. If x_m is the midpoint of such a step, and $\hat{x}$ the output level corresponding to that step, the "tracking error" is defined as $1 - x_m/\hat{x}$. The tracking error is of limited value as a performance measure and is not used as much as gain tracking.

2.3.14 Idle Channel Noise

If in a PCM system zero input corresponds to the midpoint of a step in the quantizer characteristic, as is the case for Figure 2.8, it is conceivable that no output is generated when no input is applied (except of course for noise sources in the receiver itself). Usually however, random fluctuations such as thermal noise can cause the equivalent input to cross at least one decision level, in which case the equivalent output is a random square wave of amplitude corresponding to a step of the smallest segment. This is worst when a small offset input voltage biases the quantizer so that zero input corresponds to a decision level, in which case the slightest noise will make the output switch between at least two successive values.

Assuming the noise is small enough so that only two values are excited, the r.m.s. value of the resulting output is at most $\Delta/2$, as can easily be shown, where Δ is the length of one step in the smallest segment. Most commonly, however, larger extraneous signals such as hum will exist, which will traverse more than two consecutive steps. Then the output will consist of the hum plus the quantizing error. Since usually the output filters used cut off the low frequencies, most of the hum components can be removed. Then the remaining quantizing error will have an r.m.s. value close to $\Delta/\sqrt{12}$, which is the value expected for the uniform quantization in the first segment (see equation 2.13).

2.3.15 C-Message Weighting

The effect of distortion on the performance of a communication system depends not only on the total power of the distortion components, but also on their relative magnitude. To make distortion measurements more meaningfull, various "weighted measurement" methods have been established. The distortion to be evaluated is passed through a filter whose transfer characteristic is selected so that its magnitude is larger at frequencies where the existence of distortion components is more undesirable, and smaller where distortion components are more tolerable. The total average power at the output of this filter is then measured and represents the distortion value. This method applies to noise measurements as well.

The standardized weighting filter characteristics are known as A, B, C etc., each being used in various situations. In PCM work, the C filtering characteristic is used [20]. Distortion and/or noise measurements made through a C filter are called "C-message weighted measurements". Let H(f) be the transfer junctions of a C filter, and assume that it is to be used in measuring noise whose spectrum is flat over the passband. Then the

ratio of the powers at the output, and input of the filter will be:

$$r = \frac{\int_0^w |H(f)|^2 df}{w} \qquad (2.31)$$

where w is the upper limit of the baseband. It is easily calculated that the value of r corresponds to -2.9 db. This means that the signal-to-noise ratio can be calculated from its unweighted value by merely adding 2.9 db. This result is also true to a good approximation in the case of distortion, as long as the spectrum of the latter consists of numerous components of comparable magnitudes, which is usually the case.

2.4 TECHNIQUES FOR PCM ENCODING

Numerous techniques have been developed for PCM encoding. A detailed description of many of these techniques, as well as comparisons between them, can be found in Cattermole [5]. A possible classification of PCM encoding techniques is as follows:

a) Sequential encoding. In this technique, the bits of the PCM word are determined one at a time by comparing the input to a fraction of the reference voltage. Sequential encoders are characterized by relatively low circuit complexity and low speed. Chapter 4 is devoted to the realization of an encoder using this technique.

b) Parallel encoding. All bits of the PCM word are determined at once in parallel encoding, by comparing the input to several fractions of the reference voltage simultaneously. Although this achieves very high conversion speeds, the amount of circuitry required is large. The "folded" encoding technique can be considered as a special case of parallel encoding [5].

c) Counting encoding. In this technique a counter determines the time

intervals it takes a ramp to reach values corresponding to the input and to the reference voltage. The PCM word is developed from the number of clock pulses in these intervals. The main advantage of this technique is that it does not rely on high component accuracy, except for the timer. The complexity is low, but so is the conversion speed.

d) Differential encoding. This technique is different in principle from those described above, in that the encoding relies on input changes rather than instantaneous values. A special case is the Delta modulation technique [21,5]. In the latter, high speed circuits must usually be employed. A comparison between PCM, Delta modulation and other forms of modulation can be found in [22].

e) Equilibrium encoding. This type of encoding is relatively new. Its principle of operation relies on a feedback system, which is designed so as to have a number of stable points, each corresponding to one PCM word. The input then causes the system to achieve equilibrium at one of these points. The detailed principle is involved [23,24]. This type of encoding has not been used to any extent.

In addition to the above, techniques have been devised which use principles from more than one of these categories. Thus, sequential-parallel encoding is possible, where the PCM word is divided into groups of bits, the groups being generated one at a time. Thus, a compromise between low complexity and high conversion speed can be achieved.

CHAPTER 3

COMPUTER SIMULATION OF PCM SYSTEMS

3.1 INTRODUCTION

For a PCM system like the one shown in Figure 2.1(b), it is desirable that the final signal $\hat{x}(t)$ at the destination is an adequately faithful reproduction of the signal $x(t)$ originating at the source. Since the objective of this work is the investigation of PCM encoders and decoders, we will assume that the communication channel is noiseless. Also, no digital transmission errors will be discussed, this being relegated to the references [25]. We will then limit our attention to the errors due to sampling, encoding/decoding, and filtering processes.

There are several different measures for the performance of a PCM system. However, extensive calculations are required for evaluating any such measure, since the overall performance depends on numerous factors, like, for example, the size of each step in the quantizing characteristic. Computer simulation is therefore appealing both as an analysis and a design tool.

3.2 ERRORS INTRODUCED BY THE QUANTIZER

3.2.1 Introduction

The combination of the A/D and D/A converters can be treated as a quantizer, as has been discussed in section 2.3.4. The error introduced by such a quantizer is considered in this section, assuming no sampling and filtering are present. The error calculated this way is useful not only because it characterizes the quantizer, but also because under certain conditions it is practically equal to the error introduced when a sampler and low-pass filter are included in addition to the quantizer. This is discussed in section 2.3.11.

3.2.2 Average Error Power and Mean Square Error.

Consider a quantizer defined by a relationship $\hat{x} = \hat{x}(x)$, as for example in Figure 2.9. If an input $x(t)$ is applied to the quantizer, as shown in Figure 3.1(a), the error between output and input will be:

$$\in_1(t) = \hat{x}(t) - x(t) \tag{3.1}$$

The average power of this error will be given by:

$$p_1 = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} [\hat{\in}_1(t)]^2 dt = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} [\hat{x}(t)-x(t)]^2 dt \tag{3.2}$$

This direct comparison between output and input is unfair for most applications. Consider for example a case where $\hat{x}(t) = Gx(t) + K$ for all t, where G and K are constants. In practice, G and K would correspond to a gain and a DC bias term, which can be easily taken care of and should not be thought as per se contributions to the distortion of the output. However, their presence can make the error measure given in equation (3.2) quite large, which makes the usefulness of this equation questionable.

A much more meaningful measure of the error is obtained by comparing the output $\hat{x}(t)$ to a function of the form $Ax(t) + B$, where A and B are allowed to vary so that they can eliminate the effect of any gain and DC bias terms in the output $\hat{x}(t)$. The error then becomes:

$$\in(t) = \hat{x}(t) - [Ax(t) + B] \tag{3.3}$$

and its average power is:

$$p = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \{\hat{x}(t) - [Ax(t) + B]\}^2 dt \tag{3.4}$$

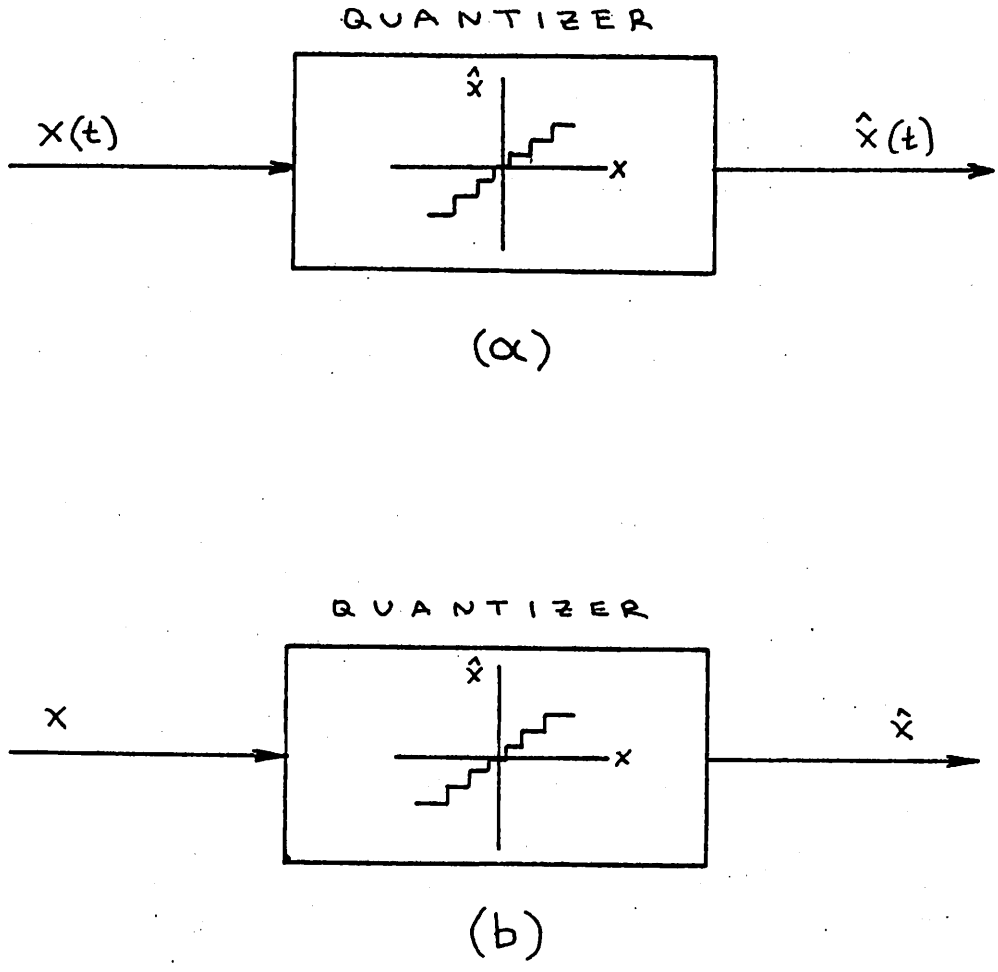


Figure 3.1: (a) Quantizer with deterministic input.
(b) Quantizer with random process input.

A and B can now be varied until the above average power becomes minimum. If A_{opt} and B_{opt} are the values of A and B for which this is achieved, the expression:

$$P = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \{\hat{x}(t) - [A_{opt}x(t) + B_{opt}]\}^2 dt \qquad (3.5)$$

should be taken as a measure of the error. In this way the system will not be penalized for a gain different from unity or a DC bias term different from zero.

Consider now the same quantizer as shown in Figure 3.1(b), where the input is a random process x. Following the same reasoning as above, we compare the output $\hat{x}$ to Ax + B. The mean square error will then be given by:

$$\overline{\epsilon^2} = E[\hat{x} - (Ax + B)]^2 \qquad (3.6)$$

where $E(\cdot)$ denotes the expected value.

If the input process is ergodic, the statistical average shown above will equal the time average, which will be of the form shown in equation (3.4). The mean square error in equation (3.6) will therefore be minimized for the same values $A = A_{opt}$ and $B = B_{opt}$ that minimize (3.4), and the resulting minimum square error will be:

$$D = E[\hat{x} - (A_{opt}x + B_{opt})]^2 \qquad (3.7)$$

The average power P given by equation (3.5) is therefore equal to the mean square error D given by equation (3.7):

$$P = D \qquad (3.7a)$$

This property will be used in calculating the harmonic distortion at

the output of a quantizer under sinusoidal excitation, which is discussed in the following subsection.

3.2.3 Relation Between Mean Square Error and Harmonic Distortion for Sinusoidal Inputs.

Although in telephony applications the signals encountered are not sinusoids, the performance of PCM systems and simple quantizers under sinusoidal excitation of various amplitudes constitutes a very simple and useful test. For purposes of simulating this performance, we consider the system of Figure 3.1(a) for the case where $x(t) = \cos \omega t$. We then compare the output $\hat{x}(t)$ to $Ax(t) + B$, as explained in the previous section. This can be done as shown in Figure 3.2 in terms of circuits, where A is an adjustable gain and B an adjustable DC bias. The average power of the error is read by an average power meter as shown. According to the discussion in the previous section, A and B are adjusted until the reading of the power meter is minimum. It will now be shown that this minimum reading actually gives the power in the harmonics at the output of the quantizer.

Since the output $\hat{x}(t)$ will be periodic, it can be represented by a Fourier series of the form:

$$\hat{x}(t) = a_o + a_1 \cos(\omega t + \phi_1) + \sum_{k=2}^{\infty} a_k \cos(k\omega t + \phi_k) \qquad (3.8)$$

or, as a complex exponential series:

$$\hat{x}(t) = \sum_{n=-\infty}^{\infty} C_n \in^{jn\omega t} \qquad (3.9)$$

In equation (3.8), a_o is the DC component of the output, and a_1 can be defined as the "gain" of the fundamental component with respect to the input. Our first observation is that ϕ_1, the phase of the fundamental in

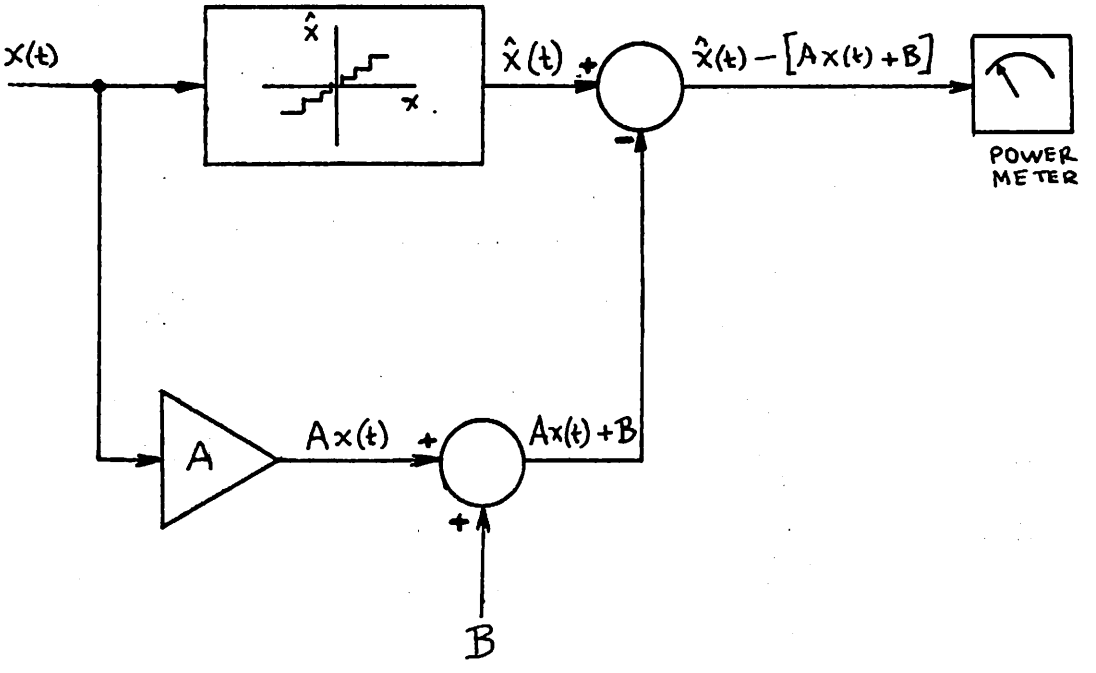


Figure 3.2: Determination of the error power.

equation (3.8), is zero. This can be shown as follows:

Consider the symmetry properties of the waveform of $\hat{x}(t)$ with respect to the vertical axis. It is evident that the part of the waveform in the interval $(-\frac{T}{4}, 0)$ is symmetric with that in $(0, \frac{T}{4})$. Similarly, the parts in $(-\frac{T}{2},-\frac{T}{4})$ and $(\frac{T}{4}, \frac{T}{2})$ are symmetric. We will now calculate the coefficient c_1 in equation (3.9):

$$c_1 = \frac{1}{T}\int_{-T/2}^{T/2} \hat{x}(t)\in^{-j\omega t}dt$$

$$= \frac{1}{T}\int_{-T/2}^{T/2} \hat{x}(t)\cos\,\omega t\,dt - j\,\frac{1}{T}\int_{-T/2}^{T/2} \hat{x}(t)\sin\,\omega t\,dt \qquad (3.10)$$

From the symmetry considerations mentioned above it can be seen that the last integral in (3.10) is zero, and that the first is non-negative. Therefore the angle of c_1 is zero, and since $\phi_1 = \measuredangle c_1$, ϕ_1 is zero as claimed. Equation (3.8) can then be written as follows:

$$\hat{x}(t) = a_o + a_1 \cos\,\omega t + \sum_{k=2}^{\infty} a_k \cos(k\omega t + \phi_k) \qquad (3.11)$$

The signal at the input to the power meter in Figure 3.2 will be:

$$\hat{x}(t) - [Ax(t) + B] = (a_o - B) + (a_1 - A)\cos\,\omega t + \sum_{k=2}^{\infty} a_k\cos(k\omega t + \phi_k) \qquad (3.12)$$

Therefore the average power read by the meter is:

$$(a_o - B)^2 + \frac{(a_1 - A)^2}{2} + \sum_{k=2}^{\infty} \frac{a_k^2}{2} \qquad (3.13)$$

This power is obviously minimized for $B = a_o$ and $A = a_1$. It follows that, if in Figure 3.2 the gain A and the DC bias B are adjusted so that the average power meter reading is minimum, $A = A_{opt}$ will be equal to the

amplitude of the output fundamental and $B = B_{opt}$ will be equal to the DC component of the output:

$$A_{opt} = a_1 \tag{3.14}$$

$$B_{opt} = a_o \tag{3.15}$$

For $A = A_{opt}$ and $B = B_{opt}$, the average power read by the meter will be solely due to the harmonics, and its value will be:

$$P = \sum_{k=2}^{\infty} \frac{a_k^2}{2} \tag{3.16}$$

Assume now that the input is a random process x, as in Figure 3.1, and that it is of the form:

$$x(t) = \cos(\omega t + \Theta) \tag{3.17}$$

where ω is a constant and Θ is a random variable, uniformly distributed in $(-\pi, \pi]$. Then x(t) is called a "random-phase sinusoid" and is ergodic. From equations (3.7), (3.7a) and (3.16) then we have:

$$P = \sum_{k=2}^{\infty} \frac{a_k^2}{2} = E[\hat{x} - (A_{opt}x + B_{opt}]^2 = D \tag{3.18}$$

The total harmonic distortion (THD) as a fraction of the power of the fundamental will be, from equations (3.14) and (3.18):

$$THD = \frac{\sum_{k=2}^{\infty} \frac{a_k^2}{2}}{a_1^2/2} = \frac{E[\hat{x} - (A_{opt}x + B_{opt})]^2}{A_{opt}^2/2} \tag{3.19}$$

To calculate the above expected values, the probability density of the random-phase sinusoid is needed. This can be readily calculated [26].

For a process of the form $x(t) = \cos(\omega t + \Theta)$ with Θ uniformly distributed in $(-\pi, \pi]$, it is found to be:

$$p(x) = \frac{1}{\pi\sqrt{a^2 - x^2}}, \quad |x| \leq a$$
$$= 0 \qquad , \quad |x| > a \tag{3.20}$$

Details for these calculations are given in the next subsection.

3.2.4 Calculation of the Mean Square Error D.

The problem to be discussed in this subsection is the following: Given the characteristic $\hat{x} = \hat{x}(x)$ of a quantizer, and the probability density $p(x)$ of the input random process, calculate the mean square error D defined in equation (3.7) [19]. Consider the mean square error $\overline{\epsilon^2}$:

$$\overline{\epsilon^2}(A,B) = E[\hat{x} - (Ax + B)]^2 \tag{3.21}$$

According to section 3.2.2 we have:

$$D \triangleq \min_{A,B}[\overline{\epsilon^2}(A,B)] = E[\hat{x} - (A_{opt}x + B_{opt})]^2 \tag{3.22}$$

To determine A_{opt} and B_{opt} we have to minimize $\overline{\epsilon^2}$ with respect to A and B. For brevity, we introduce the notation $\overline{g(x)} \triangleq E[g(x)]$. We must then have:

$$\frac{\partial}{\partial A}[\overline{\epsilon^2}(A,B)] = \frac{\partial}{\partial A}\overline{[\hat{x} - (Ax + B)]^2} = \overline{\frac{\partial}{\partial A}[\hat{x} - (Ax + B)]^2}$$
$$= \overline{2(-\hat{x}x + Ax^2 + Bx)}$$
$$= 2(-\overline{\hat{x}x} + Ax^2 + B\bar{x}) = 0 \tag{3.23}$$

And, similarly:

$$\frac{\partial}{\partial B}\left[\overline{\in^2}(A,B)\right] = 2(-\bar{\hat{x}} + Ax + B) = 0 \tag{3.24}$$

We will now assume that the mean value of the input is zero:

$$\bar{x} = 0 \tag{3.25}$$

This does not restrict the applicability of the results, since signals with $\bar{x} \neq 0$ can be handled by considering them as the sum of a constant plus a zero-mean signal:

$$x = \bar{x} + (x - \bar{x}) \tag{3.26}$$

The constant $\bar{x}$ can be easily taken care of separately, as will be seen.

The solution of (3.23) and (3.24) is unique, and taking the second partial derivatives of $\overline{\in^2}(A,B)$ at the corresponding point, it is easily checked that it corresponds to a minimum. This solution is:

$$A_{opt} = \frac{\overline{\hat{x}x}}{\overline{x^2}} \tag{3.27}$$

$$B_{opt} = \bar{\hat{x}} \tag{3.28}$$

It is worth noting that in the case of a sinusoidal input, if the statistical averages are substituted by the corresponding time averages, the above expressions reduce to:

$$A_{opt} = \frac{2}{T}\int_{-T/2}^{T/2} \hat{x}(t)\cos \omega t \, dt \tag{3.27a}$$

$$B_{opt} = \frac{1}{T}\int_{-T/2}^{T/2} \hat{x}(t)\, dt \tag{3.28a}$$

which are no more than the expressions for the amplitude of the fundamental component and the DC term of the Fourier series for the output $\hat{x}(t)$.

The standard deviations σ_x and $\sigma_{\hat{x}}$ and the correlation coefficient ρ are defined as follows:

$$\sigma_x^2 = \overline{(x - \bar{x})^2} = \overline{x^2} \tag{3.29}$$

$$\sigma_{\hat{x}}^2 = \overline{(\hat{x} - \bar{\hat{x}})^2} \tag{3.30}$$

$$\rho = \frac{\overline{(x - \bar{x})(\hat{x} - \bar{\hat{x}})}}{\sigma_x \sigma_{\hat{x}}} \tag{3.31}$$

In terms of these, A_{opt} can be written as:

$$A_{opt} = \rho \frac{\sigma_{\hat{x}}}{\sigma_x} \tag{3.32}$$

Upon substituting (3.27) and (3.28) into (3.22), we get for the mean square error D:

$$D = \overline{(\hat{x})^2} - (\bar{\hat{x}})^2 - \frac{(\overline{\hat{x}x})^2}{\overline{x^2}} \tag{3.33}$$

or, using (3.29), (3.30) and (3.31):

$$D = (1 - \rho^2)\sigma_{\hat{x}}^2 \tag{3.34}$$

Following the discussion of subsection 3.2.2 and 3.2.3, it is reasonable to define $A_{opt}x$ as the useful signal at the output (as has been shown, for a sinusoidal input this is simply the fundamental component of the output). The mean square signal at the output is:

$$S = A_{opt}^2 \overline{x^2} \tag{3.35}$$

and, from (3.34) and (3.35) the signal-to-distortion ratio at the output is:

$$\frac{S}{D} = \frac{A_{opt}^2 \overline{x^2}}{(1-\rho^2)\sigma_{\hat{x}}^2} \tag{3.36}$$

Using (3.32) this becomes:

$$\frac{S}{D} = \frac{\rho^2}{1 - \rho^2} \tag{3.37}$$

For the evaluation of S/D then, the calculation of the expected values of some functions of x, namely x^2, $\hat{x}$, $(\hat{x}^2)$, $\hat{x}x$ is necessary. Leg g(x) represent any one of these functions, and consider the quantizer characteristic as shown in Figure 3.3. Let the input range extend from $-\infty$ to $+\infty$ and assume the characteristic has k+1 steps. The kth step is defined by its endpoints (x_k, x_{k+1}), and the corresponding output level is denoted by $\hat{x}_k$. To include the effect of peak clipping, let $x_o = -\infty$ and $x_{K+1} = +\infty$. Then the expected value of g(x) can be calculated as follows:

$$E[g(x)] = \int_{-\infty}^{\infty} g(x)p(x)dx$$

$$= \sum_{k=0}^{K} \int_{x_k}^{x_{k+1}} g(x)p(x)dx \tag{3.38}$$

For the particular forms of g(x) we are interested in, this gives:

$$\overline{x^2} = \sum_{k=0}^{K} \int_{x_k}^{x_{k+1}} x^2 p(x)dx \tag{3.39}$$

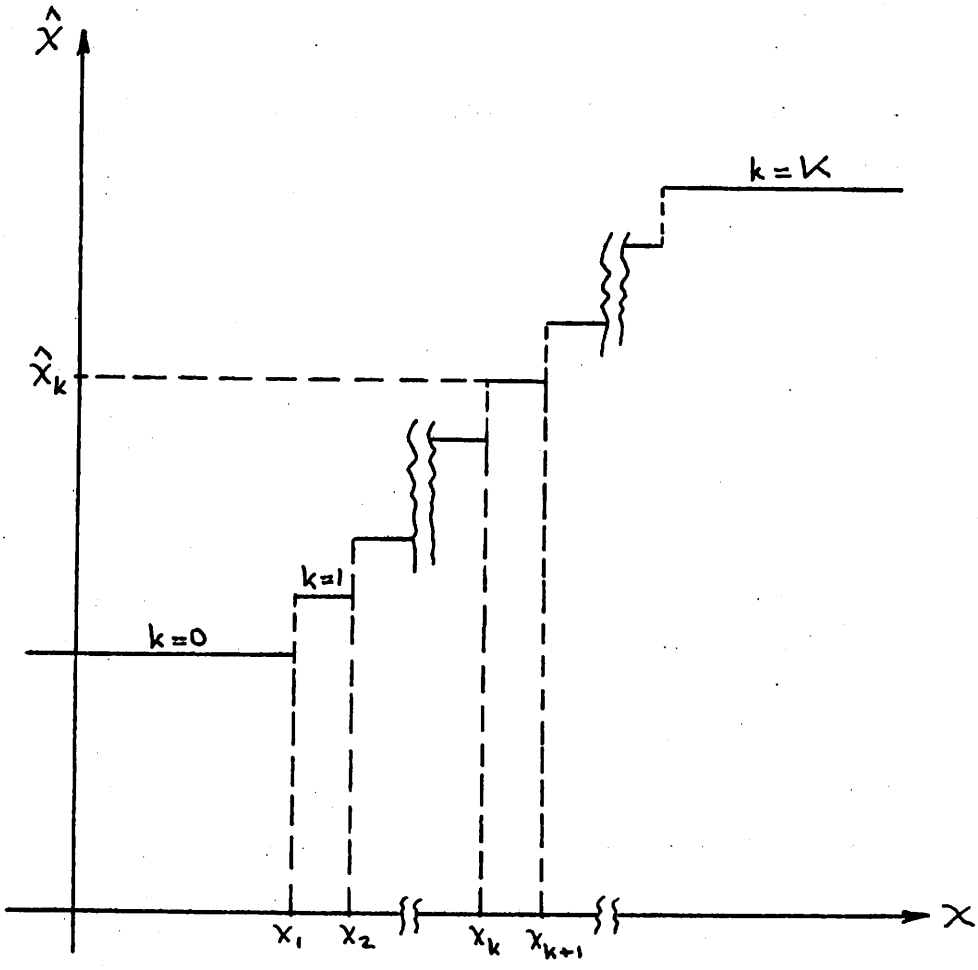


Figure 3.3: Quantizer characteristic and notation.

$$\overline{\hat{x}} = \sum_{k=0}^{K} \hat{x}_k \int_{x_k}^{x_{k+1}} p(x)\,dx \tag{3.40}$$

$$\overline{(\hat{x})^2} = \sum_{k=0}^{K} (\hat{x}_k)^2 \int_{x_k}^{x_{k+1}} p(x)\,dx \tag{3.41}$$

$$\overline{\hat{x}x} = \sum_{k=0}^{K} \hat{x}_k \int_{x_k}^{x_{k+1}} xp(x)\,dx \tag{3.42}$$

The particular p(x) used in the above expression depends on the application. A Gaussian or Laplacian p(x) can be used to represent the characteristics of speech waveforms on telephone lines. If the behavior of a quantizer under sinusoidal excitation is to be studied, p(x) as given by equation (3.20) is used.

3.3 EQUATIONS FOR SEGMENTED COMPANDING LAWS

3.3.1 Introduction

In order to construct the characteristics of ideal A/D and D/A converters, numerical values for the corresponding decision and output levels are needed. The general formulation of segment companding laws has been done by Kaneko [27]. Here, we will solve his equations for the particular case of the 15 segment approximation to the 255 μ law, described in section 2.3.8.

3.3.2 Calculation of Decision and Output Levels.

Consider the 15-segment approximation to the 255 μ law, shown in Figure 2.15 for the encoder (ADC) and in Figure 2.16 for the corresponding decoder. Referring to the coding format shown in Figure 2.15(b), let k be the sign bit, ℓ the segment number, and m the step number. Since these

characteristics are symmetric with respect to the origin, we will consider only the part corresponding to positive signals (k=1). Although in the digital word shown in Figure 2.15(b) ℓ varies from 000 to 111 in binary notation, we will assume that it takes values from 1 to 8 rather than 0 to 7, to be consistent with the notation used in the computer simulation to be described in section 3.4. Thus, ℓ=1 corresponds to the first segment and ℓ=8 to the last. Similarly, m will take values from 1 to 16.

Some features of the quantizing characteristic resulting from the combination of the encoder and decoder represented in Figures 2.15 and 2.16, are shown in Figure 3.4. With respect to these three figures, the constraints imposed on the decision levels of the encoder and the output levels of the decoder are as follows:

First, all sixteen input steps within any one segment of the encoding characteristic are required to have equal length. To normalize their sizes, we will take the input step size in the first segment equal to unity. Also, for reasons outlined in section 2.3.5, each output level is required to be at the middle between the two corresponding decision levels, as shown in Figure 3.4(a). This constraint, along with the equal input step size within one segment, implies that the output step sizes at the segment boundaries cannot be equal to the output step sizes in the inside of the segments. This is evident in Figure 3.4(a). The output step sizes are therefore functions of both the segment number and the step number, and can be described by:

$$\begin{aligned} \Delta\hat{x}(\ell) &= \hat{x}(\ell,m) - \hat{x}(\ell,m-1), \quad m \neq 16 \\ &= \hat{x}(\ell+1,1) - \hat{x}(\ell,16), \quad m = 16 \end{aligned} \tag{3.43}$$

Finally, the output level corresponding to the input interval centered around the origin must be zero, as shown in Figure 3.4(b):

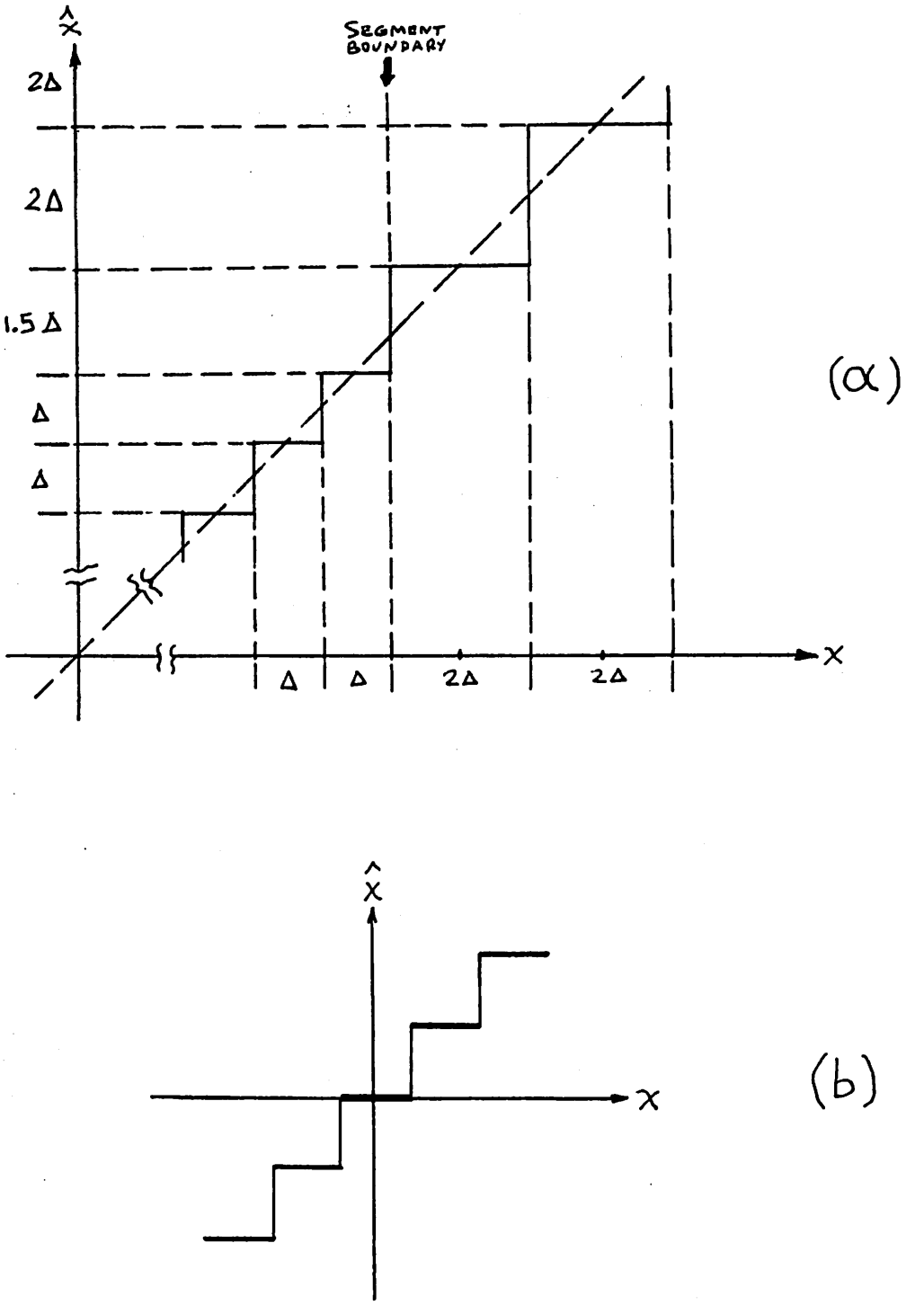


Figure 3.4: Standardized 15-segment approximation to the 255μ quantizing law.
(a) Detail around a segment boundary.
(b) Detail around the origin.

$$\hat{x}(1,1) = 0 \tag{3.44}$$

Given all of the above constraints, all that is needed is a difference equation, whose solution, subject to these constraints will give the required values for the output levels. The required difference equation is given by expressing the fact that, except at the segment boundaries, the ratio of the output step sizes of two consecutive segments must be equal to 2, as shown in Figure 3.4(a):

$$\frac{\Delta\hat{x}(\ell+1)}{\Delta\hat{x}(\ell)} = 2, \quad \ell = 1, 2, \ldots, 15 \tag{3.45}$$

The solution of this equation that satisfies the above constraints gives the following expression for the output levels $\hat{x}(\ell,m)$:

$$\hat{x}(\ell,m) = 2^{\ell-1}\,(m + 15.5) - 16.5 \tag{3.46}$$

These output levels correspond to input intervals whose upper limit $x_u(\ell,m)$ is easily found to be:

$$x_u(\ell,m) = 2^{\ell-1}\,(m + 16) - 16.5 \tag{3.47}$$

Similar considerations will give another set of equations for the A-law. The reader is referred to [27].

3.4 THE SIMULATION PROGRAM XCODEC

3.4.1 Introduction

The concepts described in sections 3.2 and 3.3 have been applied in the development of a computer program for the simulation of coder-decoder combinations (codecs). The analysis performed is static, and a particular codec is assumed to be completely described by its static characteristic. The program has been written in FORTRAN and a listing along with a sample

output and a detailed description from a user's point of view is given in Appendix A.

3.4.2 Program structure.

For convenience, two subroutines generate ideal encoder and decoder characteristics for the 15-segment approximation to the 255 μ law. Two more subroutines, which generate the characteristics of practical encoders and decoders under investigation, must be specified by the user.

The main program couples a practical or ideal encoder subroutine to a practical or ideal decoder subroutine according to the user's request, and generates a listing describing the corresponding quantizer characteristic. A subroutine then calculates signal-to-distortion ratio, gain tracking, output fundamental amplitude and DC component for any number of input amplitudes specified by the user.

Since codecs realizing the 15-segment approximation to the 255 μ law were of primary interest, the notation used in the program corresponds to the encoding format shown in Figure 2.15. Specifically, a digital word is described by a triple (k,ℓ,m), where k is 1 or 2 according to whether the corresponding analog value is positive or negative, ℓ is the segment number (1 through 8) and m is the step number (1 through 16) to which the digital word corresponds.

To each digital word (k,ℓ,m) corresponds one encoder input interval, bounded by a lower limit $x_\ell(k,\ell,m)$ and an upper limit $x_u(k,\ell,m)$. To the same word there also corresponds a decoder output level $\hat{x}(k,\ell,m)$. Thus, the decision levels and output levels are stored and handled as three-dimensional matrices whose indices are the sign bit, the segment number and the step number, as shown in Figure 3.5. Although normally an input interval upper level will coincide with the lower level of an adjacent

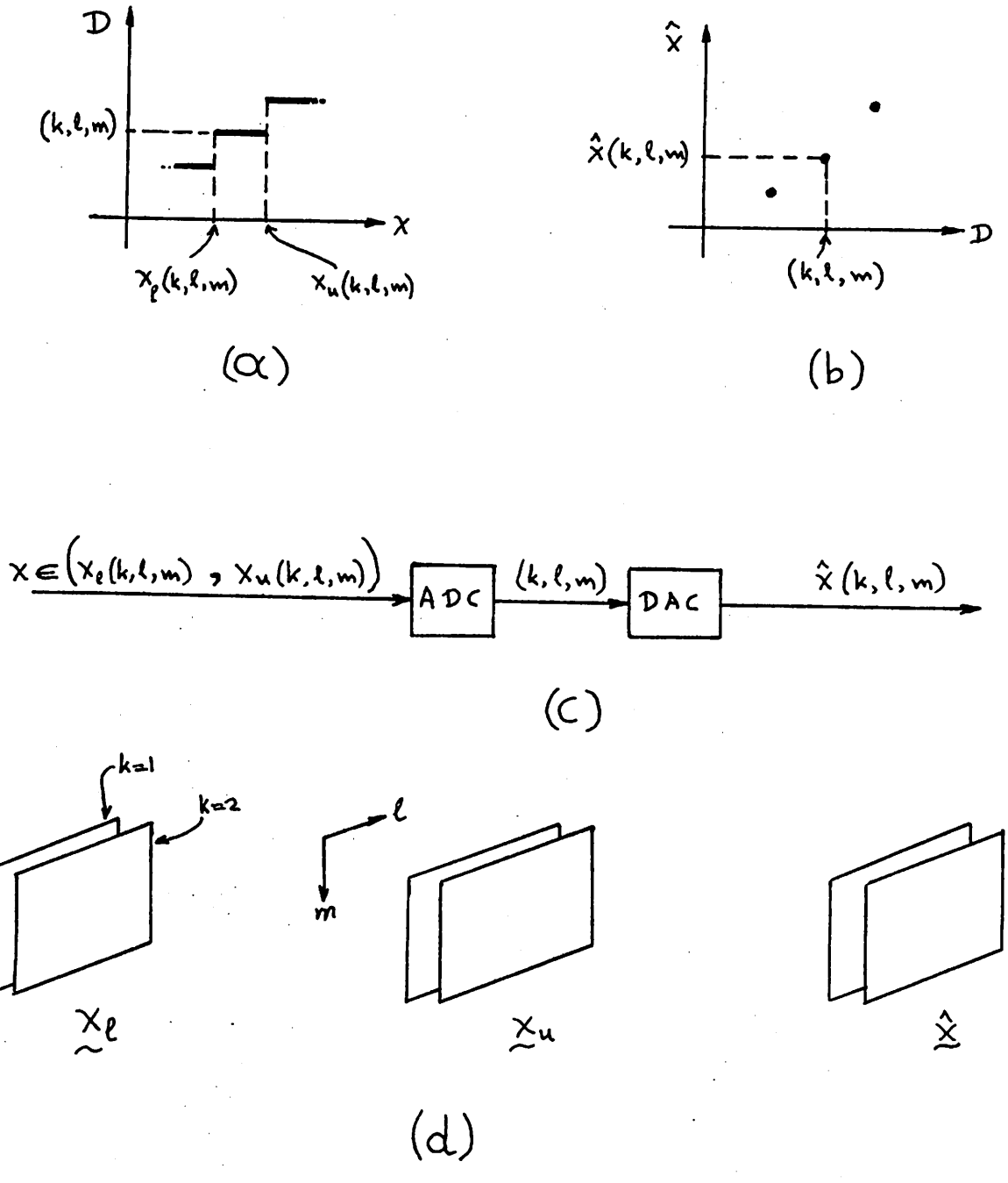


Figure 3.5: Notation used in computer simulation.
(a) ADC characteristic.
(b) DAC characteristic.
(c) ADC-DAC combination.
(d) Matrices for input step lower limits, input step upper limits and output levels.

interval, separate matrices for lower and upper levels have been used to allow for the simulation of more complex situations.

3.4.3 Calculations in XCODEC

The characteristics of ideal encoders and decoders are generated by the program using equations (3.46) and (3.47). Practical encoder and decoder characteristics are generated by user-specified subroutines. Once these characteristics are known, the program initially performs some trivial calculations like input step size, input middle point and quantizer tracking error (see section 2.3.13).

The program is intended for calculating the S/D of complete PCM systems. To calculate S/D for such systems excluding C-message weighting, equation (3.37) is used. Although this equation gives S/D for a quantizer only, it is explained in section 2.3.11 that in most cases the S/D for a complete PCM system, including sampling and filtering, will be approximately equal to that of the quantizer only, if the cutoff frequency of the output filter is equal to half the sampling rate. In practical systems this cutoff frequency is somewhat less than that, but not sufficiently less to introduce any significant error in the simulation. For example, in the D3 Channel Bank system the sampling rate is 8 KHz and the filter cutoff frequency close to 3.4 KHz. The specified input test frequency is 1.02 KHz. As explained in Chapter 2, the output of the decoder will consist of components of comparable amplitude in the baseband, which are spaced 20 Hz apart. A cutoff frequency of 3.4 KHz will then give a S/D which will be approximately 0.7 db higher than if a 4 KHz cutoff frequency was used, as can easily be calculated for this "flat" spectrum. This error is small enough to be neglected.

Also, for this spectrum the S/D if C-message weighting is included

can be easily obtained by adding 2.9 db to the unweighted value, as explained in section 2.3.15. This is done in the program. The values obtained this way represent a good estimation of the C-message weighted S/D, unless there are reasons to believe that the "flatness" assumption mentioned above is not valid, in which case detailed Fourier analysis would be required for accurate calculating of the C-message weighted S/D.

The S/D is calculated as explained for a set of user specified amplitudes of sinusoidal input. The corresponding output fundamental amplitude and DC component are calculated using equations (3.27) and (3.28), and the gain tracking is calculated according to its definition in section 2.3.13.

In the statistical calculations involved, which are of the form of equations (3.39) through (3.42), the probability density of a random-phase sinusoid as specified in equation (3.20) is used. The program searches for the appropriate encoder input steps spanned by the input, and includes only these steps in the summation indicated in equations (3.39) through (3.42). If only a fraction of a particular step is spanned by the input, that is properly taken into account.

A sample output of XCODEC, along with a program listing and a user's mannual, is given in Appendix A. The effective time for running this program on the CDC 6400 computer at U.C. Berkeley, was about 18 sec, including the calculation of S/D and gain tracking for 71 input amplitudes.

CHAPTER 4

AN ALL-MOS NONUNIFORM PCM VOICE ENCODER USING THE PRINCIPLE OF CHARGE REDISTRIBUTION

4.1 INTRODUCTION

The realization of a single-channel PCM voice encoder is investigated in this chapter. A single-chip Al-gate NMOS implementation of such an encoder is proposed, in which the principle of charge redistribution on weighted capacitor arrays [28], [29] is used to realize the 15 segment approximation to the 255-μ encoding law. The requirements imposed on the individual components for satisfactory system performance are investigated, and it is concluded that the realization of such an encoder which meets the Bell System specifications for the D3 Channel Bank [30] is indeed possible. The experimental evidence of this is given in Chapter 7.

4.2 PER-CHANNEL PCM VOICE ENCODING

In the approach usually taken up to now in PCM, systems called "channel banks" are used in which 24- 48 channels are time-division multiplexed in analog form, and subsequently encoded by a single high speed encoder. However, in several cases it might be preferable to use per-channel encoding, i.e. to encode each channel separately and then multiplex the resulting digital signals. In channel banks, this amounts to substituting a single costly high speed encoder by several low-cost, low speed ones. In addition, the analog multiplexer is replaced by a digital one, which is simpler and less vulnerable to crosstalk. The low encoder cost required for this approach to be preferable, can best be achieved by using some form of Large Scale Integration (LSI), and a single chip encoder implementation would certainly be desirable.

In addition to channel banks, single-chip encoders can find applications in subscriber loop carrier equipment, which is used in rural areas where subscribers are few and spaced a few miles apart. A single chip encoder would permit the substitution of the presently used frequency division multiplexing systems by simpler time-division multiplexing.

Further use of single-chip encoders can be found in PABX (Private Automatic Branch Exchange) equipment. Such equipment is becoming increasingly complex, with features like automatic dialing, temporary dialing information storage etc. These functions can best be handled in digital form, which is possible if the individual analog channels are first PCM encoded by low-cost encoders.

Assuming that the one-chip approach proves feasible, handling more than one channel on the same chip would be of questionable value. Not only would the large area required for such an application reduce the yield and increase the cost, but the very small amount of crosstalk required between the channels would be difficult to achieve. For these reasons, this research effort was directed towards a single-channel, one-chip approach.

4.3 PCM CIRCUITS AND TECHNOLOGY

4.3.1 Circuit Techniques for PCM Encoder Realization

In section 2.4, several encoding techniques have been described. Of these, equilibrium encoding has not adequately been investigated at the present. Also, it appears that the circuitry involved is too complicated to lend itself to integrated circuit realization on a reasonable chip area. The choice therefore is mainly among parallel, counting, differential and sequential encoding.

Parallel encoding is the fastest of these techniques. However, this is accomplished at the cost of complexity. The key components required are a sample-and-hold circuit, several comparators and precision voltage or current dividers. Also, the "folded" encoding scheme [31], which is a special case of parallel encoding, requires precision absolute value amplifiers. The amount of chip area required to accomodate such a system would be very large. Furthermore, since 125 μsec are allowed for encoding (for an 8 KHz sampling rate), there is no advantage in having a very fast single-channel encoder.

In the counting encoding scheme only moderate precision is required of the circuit elements, the accuracy of the encoding process relying on precise timing. A sample-and-hold function is required, along with a comparator and a counter. Although the sequential encoding scheme was the one finally realized, there is no particular reason to believe that a counting encoder is not just as feasible.

In differential encoding no sample-and-hold circuit is required, since an internally generated staircase-like voltage or current is caused to track the input continuously. In addition, it can be designed so that no high precision elements are required. Problems encountered in differential encoders include sloap overload [21], [5] and difficulty in maintaining an output corresponding to zero when no input is applied. Although the latter can be aleviated by using "leaky" integrators, in some cases this can result in worse idle channel noise behavior compared to standard PCM. Another drawback of differential encoding is that due to the continuous tracking mechanism, the system cannot be used as a decoder on a time-share basis unless very high bit rates are used. However, the possibility of time-sharing does exist with standard PCM system, as long as the encoding is accomplished in a time small enough to allow for the

system's being used as a decoder before the next sampled value to be encoded appears.

A technique [32] which is basically a variation of differential encoding uses a resistive ladder with a 5% accuracy. In integrated circuit form, the latter would be realized in bipolar technology. Additional logic to what is shown in the above paper would be required in order to convert the digital signal at the output of the system to standard PCM format. For a single-chip approach, excessive area should be expected.

The sequential encoding technique appears to be promising for a single-channel encoder. The conversion time will be shown to be less than half the sampling period, which allows for possible use of the circuit as a decoder on a time-share basis. The component precision required by this technique is moderate and can be achieved in a monolithic realization with a high yield. A sample-and-hold function is required, in addition to a single comparator. Most schemes for nonuniform PCM using sequential encoding require some additional analog function, such as a unity gain buffer. A single-channel nonuniform PCM encoder can be realized economically on a single chip using the principle of charge redistribution on weighted MOS capacitor arrays.

4.3.2 Technology for Single-Channel Encoder Realization

In any of the techniques discussed above, both analog functions and digital logic is required. In realizations using two or more chips, more than one integrated circuit technology can be used. For example, the high performance analog functions can be realized using a bipolar chip, and the digital functions using an MOS chip. For the single-chip realization discussed above, an all-bipolar approach is possible using I^2L technology. We have however chosen the all-MOS approach for several reasons.

First, the process is simple and requires only five masking steps. Second, it has been demonstated [28], [29] that voltage dividers of accuracy sufficient for this application can be constructed in MOS technology by using MOS capacitors. Third, a Sample-and-Hold function is easily realizable in MOS. The fourth, and perhaps the most important reason is that the process is compatible with Charge Coupled Device (CCD) and Bucket Brigade sampled-data filters, and thus the possibility of incorporating the encoder anti-aliasing filter and the decoder output filter on the same chip with the encoder/decoder exists, using transversal or recursive realizations [33]. The process is also compatible with MOS microprocessor technology. Furthermore, the MOS transistor inherently makes a good, zero-offset analog switch.

The efforts of this research have therefore been directed towards a single-channel, low cost chip which performs PCM encoding according to the 15 segment approximation to the 255-μ law utilizing NMOS technology.

4.4 CHARGE REDISTRIBUTION PCM ENCODER

4.4.1 Sequential Encoding

The principle of sequential encoding is described in the block diagram of Figure 4.1. Here, voltage input and voltage reference source have been chosen as an example, and encoding according to the 15 segment approximation to the 255-μ law is assumed. The Sample-and-Hold circuit samples the bandlimited analog input signal v_{IN} at a rate at least as high as the Nyquist rate, and the sampled values are held and applied to one input of a comparator. A "decision level generator" develops fractions of the reference voltage V_{REF}, which correspond to the decision levels of the 15 segment approximation to the 255μlow, shown in Figure 2.15(a). The simplest way to encode the input would be for the decision level generator to

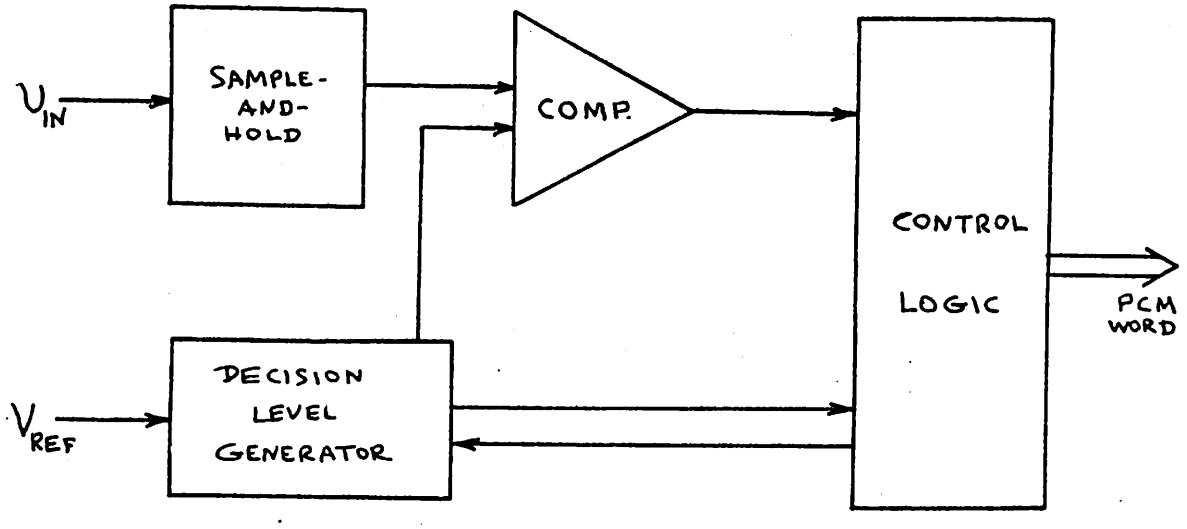


Figure 4.1: Sequential encoder principle.

start producing all decision levels of the encoding law in sequence until the comparator changes state, which would indicate that the input lies within the interval bounded by the decision levels generated just before and after the comparator switches. The change of state of the comparator is sensed by the logic, which then produces the appropriate PCM word.

However, the encoding time can be greatly reduced if a more efficient conversion sequence is used. For example, the decision level generator's output can be set to zero, and the sign of the input determined by the comparator's state. Then, decision levels corresponding to the endpoints of the segments can be generated, to determine in which segment the input lies. Finally, the interval in which the input lies can be determined by generating the decision levels for that segment only. This sequence will be considered in detail when the particular realization implemented will be described.

4.4.2 Decision Level Generator

For the reasons explained in section 4.2, an NMOS process has been chosen for the realization of the encoder. To generate fractions of the reference voltage, some form of voltage divider must be employed. This cannot be a resistive divider since resistors of appropriate sheet resistance are not available in NMOS. However, it has been shown that accurate capacitive voltage dividers can be constructed using the principle of charge redistribution [28], [29]. This principle is illustrated in Figure 4.2. In the circuit shown in (a), equilibrium has been achieved. For the principle to be described, the particular values of V_A, V_B, V_{CA}, V_{CB} are irrelevant as long as they satisfy Kirchoff's voltage law. Next, v_A is assumed to undergo a change of magnitude Δv_A. At the end of the transition, the situation shown in (b) occurs. From Kirchoff's voltage

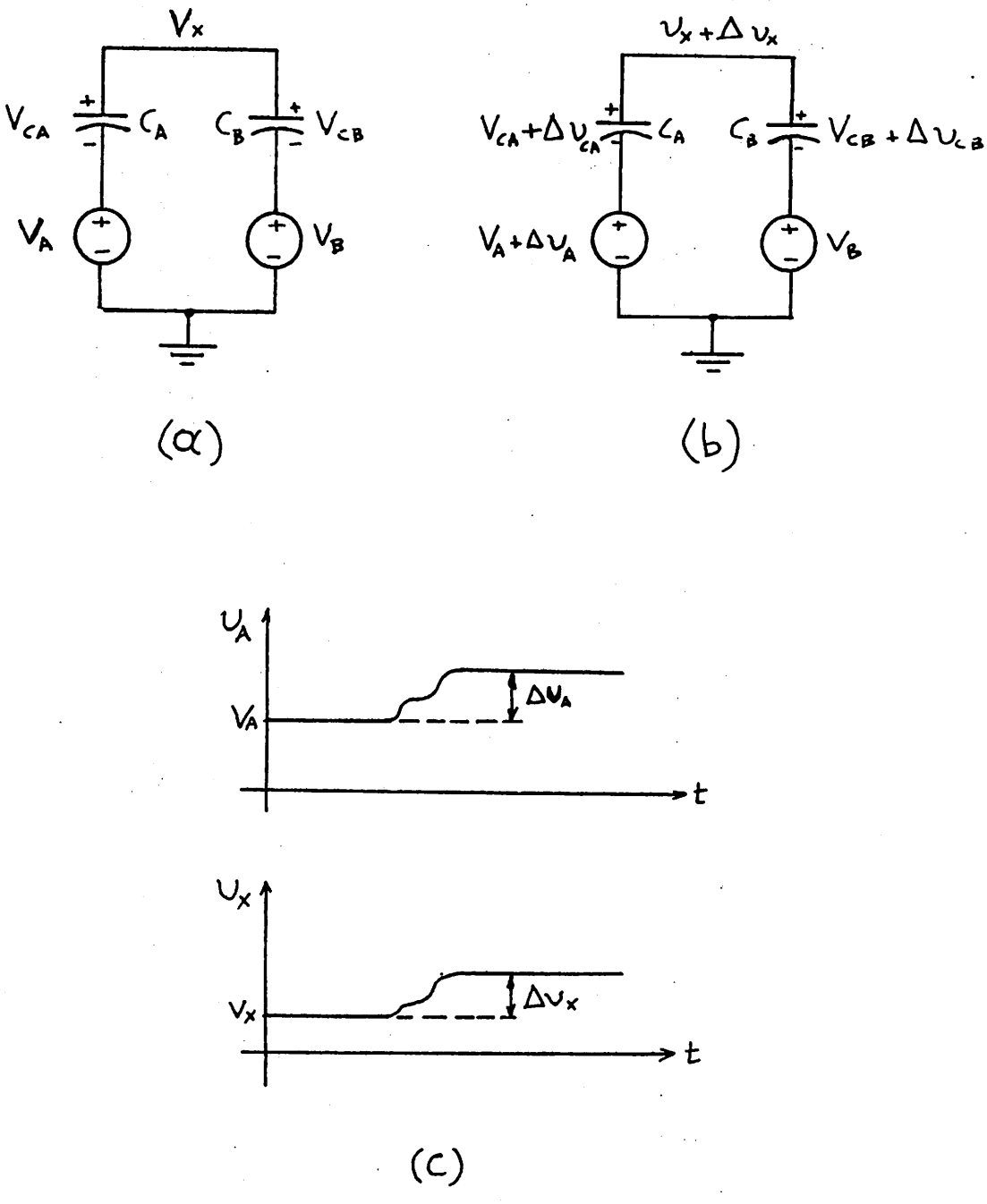


Figure 4.2: Principle of charge redistribution.
(a) Circuit before v_A transition.
(b) Circuit after v_A transition.
(c) Waveforms

law we must have:

$$\Delta v_A + \Delta v_{CA} = \Delta v_{CB} \tag{4.1}$$

The capacitor voltages have changed because an amount of charge ΔQ flowed out of the top plate of C_A and into the top plate of C_B. Therefore:

$$\Delta v_{CA} = - \frac{\Delta Q}{C_A} \tag{4.2}$$

$$\Delta v_{CB} = + \frac{\Delta Q}{C_B} \tag{4.3}$$

From Figure 4.2(b) we have:

$$\Delta v_X = \Delta v_{CB} \tag{4.4}$$

Combining the above four equations, we get:

$$\Delta v_X = \left(\frac{C_A}{C_A + C_B} \right) \Delta v_A \tag{4.5}$$

Several facts are important concerning this relation:

a) The capacitive divider actions displayed by equation (4.5) relates only <u>changes</u> of voltages. The total values of the voltages of the sources and the initial capacitor voltages do not enter in this equation.

b) The chape of $v_A(t)$ during the transition is completely irrelevant. It is only the change $v_{A,FINAL} - v_{A,INITIAL}$ that determines Δv_X.

c) If resistors are included in series with the capacitors to represent practical limitations, like switch resistances and source output resistances, equations (4.5) is still valid after the transients have died out. For example, if the transition of v_A is a step of magnitude Δv_A occuring at t=0, a straight-forward analysis of the circuit gives:

$$\Delta v_X(t) = \left[\left(\frac{C_A}{C_A + C_B}\right)\Delta v_A\right]\left(1 - \in^{-\frac{t}{RC}}\right) \tag{4.6}$$

where R is the total series resistance and C the equivalent capacitance of C_A and C_B in series. It is seen that for large t, equation (4.6) reduces to equation (4.5).

This principle of charge redistribution can be employed in the generation of the decision levels corresponding to the end points of the segments of the encoding law shown in Figure 2.15(a). For the moment, we will consider only the 8 segments corresponding to positive voltages. All segments have 16 steps each except for the first, which has 15 1/2 steps as explained in chapter 2. This last fact is of minor importance, and for the moment we will assume that that segment also has 16 steps. The modification needed to get 15 1/2 steps will be considered separately later.

Let ΔV be the input voltage interval corresponding to the first segment. Each segment corresponds to an input interval which is twice that for the previous segment. Therefore, the input interval corresponding to the kth segment will be given by:

$$I_k = 2^{k-1}\Delta V \tag{4.7}$$

Let the endpoint of the last segment correspond to the full reference voltage, V_{REF}. Then:

$$V_{REF} = \sum_{k=1}^{8} 2^{k-1}\Delta V \tag{4.8}$$

or:

$$\Delta V = \frac{V_{REF}}{255} \tag{4.9}$$

The upper endpoint of the nth segment will be at:

$$V_n = \sum_{k=1}^{n} 2^{k-1}\Delta V \tag{4.10}$$

and, using equation (4.9), this becomes:

$$V_n = \left(\frac{2^n-1}{255}\right)V_{REF} \tag{4.11}$$

The voltages V_n can be developed using the capacitor array of Figure 4.3 using the principle of charge redistribution. The switches shown in this figure are electronic switches thrown by control logic, and are for the moment assumed ideal. The system works as follows: Initially, all switches are thrown to ground, including that connected to the capacitors' top plates, so that all capacitors are discharged. Next, the top switch is opened, without affecting the capacitor voltages. Assume now that the first n switches, starting from the left, are thrown to the reference voltage. Applying equation (4.5) gives:

$$v_x = \left(\frac{\sum_{k=1}^{n} kC_x}{\sum_{k=1}^{8} kC_x}\right) V_{REF} \tag{4.12}$$

Simplifying this expression we get:

$$v_x = \left(\frac{2^n-1}{255}\right) V_{REF} \tag{4.13}$$

Comparing equations (4.13) and (4.11) it is clear that v_x corresponds to the upper endpoint of the nth segment. Thus, e.g., to develop a voltage corresponding to the upper endpoint of the third segment, the bottom plates of the first three capacitors must be connected to V_{REF}.

The problem of developing voltages corresponding to the endpoints of

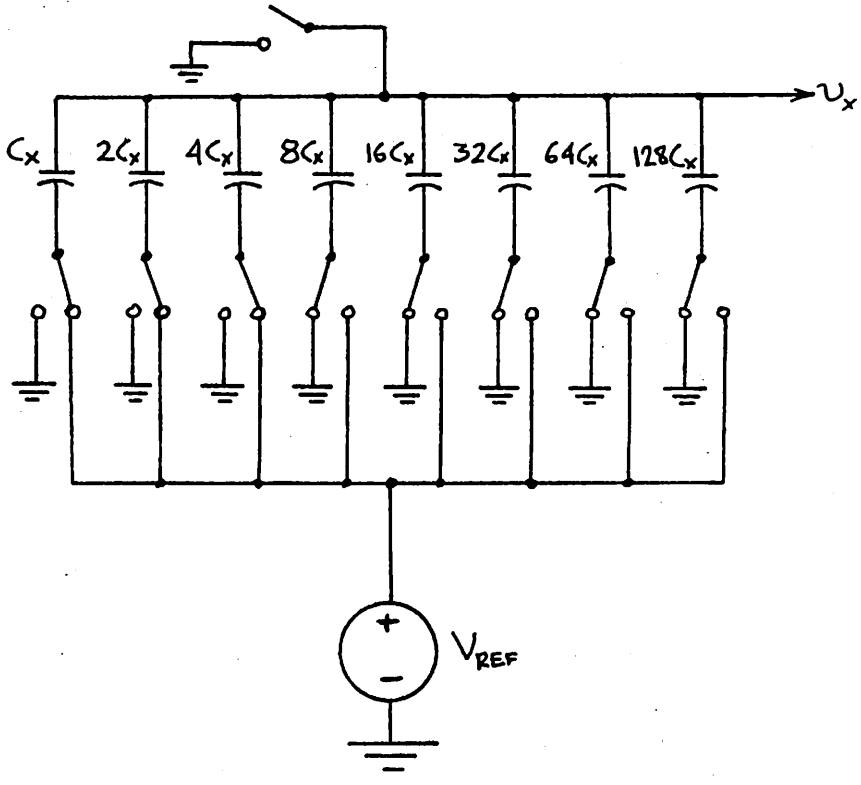


Figure 4.3: Capacitor array used to generate the decision levels corresponding to the end-points of the segments.

each one of the sixteen equal steps of any segment will now be considered. This could easily be done if the bottom plate of each capacitor could be thrown to not only V_{REF}, but to any integer multiple of $V_{REF}/16$ from $1 \times (V_{REF}/16)$ to $15 \times (V_{REF}/16)$. For example, to make v_x correspond to the end of the 3d step of the 5th segment, the first 4 switches should be thrown to V_{REF}, and the fifth one to $3 \times (V_{REF}/16)$.

These multiples of $V_{REF}/16$ must be developed separately. Another capacitor array can be used for this purpose, as shown in Figure 4.4. Notice that two equal capacitors of the smallest size are used, to bring the total capacitance to 16 Cy. Any integer multiplier of $V_{REF}/16$ can now be developed at the top plate, if after discharging all capacitors an appropriate combination of them is thrown to V_{REF}. More specifically, assume that $m \times (V_{REF}/16)$ is desired, where m is an integer between 1 and 15. The number m can be expressed as a sum of powers of 2:

$$m = \sum_{k=1}^{4} b_k 2^{k-1} \tag{4.14}$$

where b_k is 1 or 0. The bottom plates of the capacitors corresponding to $b_k = 1$ are then thrown to V_{REF}. The voltage v_y then, can be found from equation (4.5):

$$V_y = \frac{\sum_{k=1}^{4} b_k 2^{k-1} C_y}{16C_y} = \left(\sum_{k=1}^{4} b_k 2^{k-1} \right) \times \frac{V_{REF}}{16} \tag{4.15}$$

For example, if $V_y = 11 \times (V_{REF}/16)$ is desired, then since $11 = 1 + 2 + 8$, the bottom plates of the capacitors of values C_y, $2C_y$ and $8C_y$ must be thrown to V_{REF}.

The fractions of V_{REF} developed by this array must now be fed to the bottom plates of the x array of Figure 4.3, as mentioned above. Notice

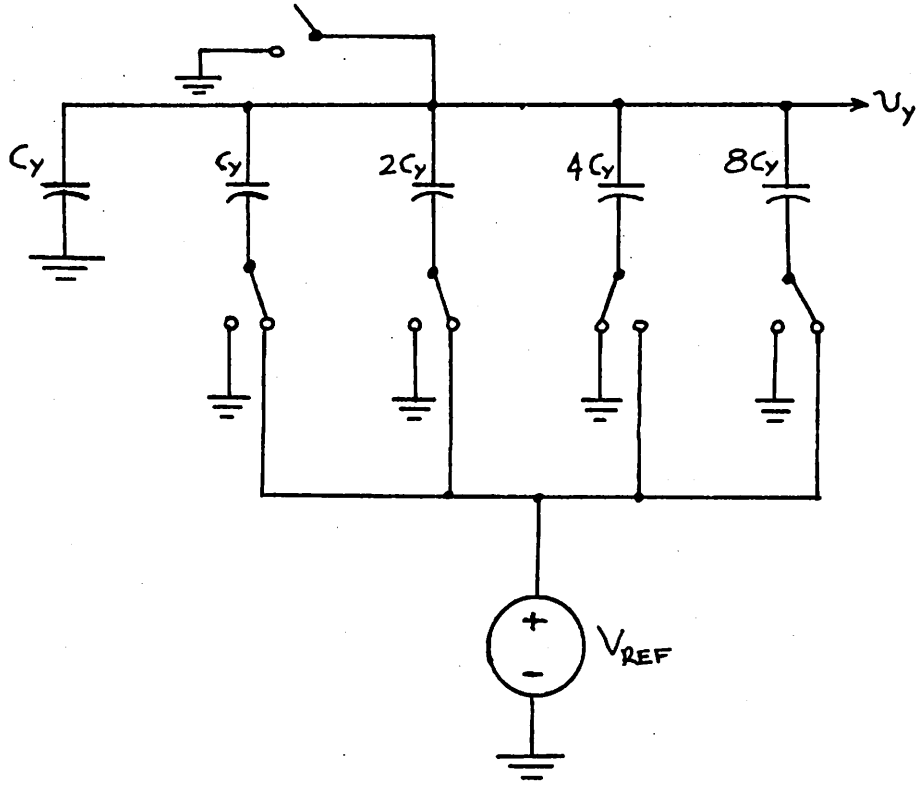


Figure 4.4: Capacitor array used to develop multiples of $\frac{V_{REF}}{16}$.

that the proper operation of these arrays is based on the fact that they are unloaded, and therefore v_y cannot be directly fed to the bottom plate of the x array. Therefore, unity gain buffer of very high input resistance must be placed in the path. The complete decision level generator is then as shown in Figure 4.5. Using this system, voltages corresponding to any decision level of the encoding law of Figure 2.15(a) can be generated. Negative decision levels can be generated using the principle explained above, but a negative reference voltage. To generate a decision level, all capacitors of both arrays are first discharged, by throwing all switches to ground. Next, the switches connected to the top plates of both arrays are opened. If the desired decision level corresponds to the end of the nth step of the nth segment, the first n-1 capacitors of the x array are thrown to V_{REF}^{+} (or V_{REF}^{-}), the nth capacitor of the x array is thrown to the output of the buffer, and in the y array these capacitors which result to $V_y = m(V_{REF}/16)$ are thrown to V_{REF}^{+} (or V_{REF}^{-}). The switches in Figure 4.5 are shown thrown to the positions necessary for generating a value of v_x corresponding to the end of the 3d step of the 5th segment.

4.4.3 Sample-and-Hold Function and Comparator

The Sample-and-Hold function required in the scheme of Figure 4.1 is easily realized by storing on a capacitor the value of the analog input voltage v_{IN} at the sampling instant. Once this is done, what remains is to determine the step in which v_{IN} lies, and then develop the PCM word corresponding to this step.

Let $\{V_{Dj}\}$ represent the ordered decision levels in the encoding law of Figure 2.15(a), starting with the most negative. Assume we form the difference $V_{Dj} - v_{IN}$ for all these decision levels. Determining the step which contains v_{IN} amounts to determining the only two consecutive de-

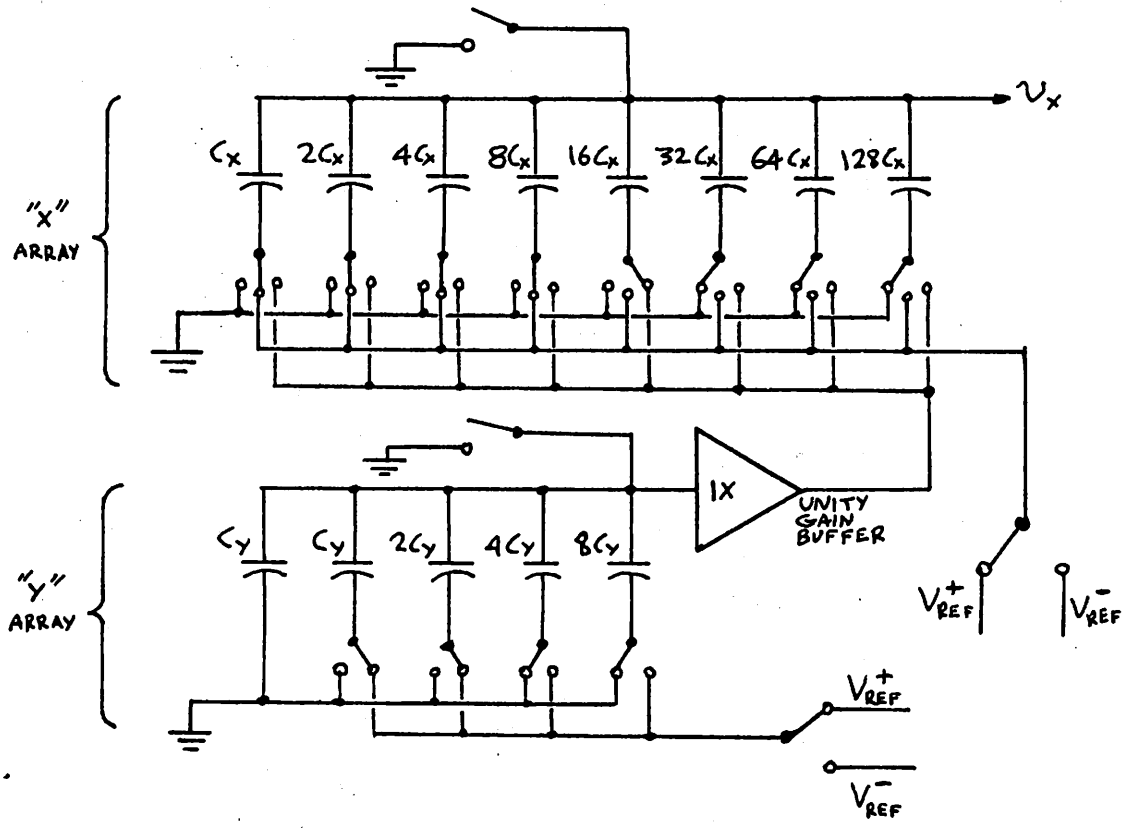


Figure 4.5: Complete decision level generator.

cision levels, $V_{D,k}$ and $V_{D,k+1}$ for which the differences $(V_{D,k} - v_{IN})$ and $(V_{D,k+1} - v_{IN})$ have opposite sign. This can easily be done by applying these differences to a comparator, which compares them to zero.

The two functions mentioned above, i.e. the Sample-and-Hold function and the function of taking the difference between two voltages can be performed using capacitors and switches. Assume that it is desired to sample v_{IN} and then take the difference between v_{IN} and a fraction of the reference voltage, representing a decision level. The circuit and the four steps required are shown in Figure 4.6. In (a), both capacitors are changed to v_{IN} as shown, and $v_x = 0$. In (b), the top switch is opened, with v_x remaining at 0. In (c), switches S_A and S_B are thrown to ground. This lowers the potential at the bottom plates of C_A and C_B by v_{IN}, and since there is no discharge path, the potential at the top plate will also be lowered by v_{IN}. Therefore, $v_x = - v_{IN}$. Finally in (d) S_A is thrown to V_{REF}, and the change in v_x is given by equation (4.5). At the end of this sequence, $V_{REF} \times [C_A/(C_A + C_B)]$, and the input v_{IN}, appears on the top plates. The sign of this difference can be sensed by a high input resistance comparator connected to that point.

The functions described above can be performed by the same capacitor array that generates the decision levels, which was described in the previous subsection. Rather than generating all decision levels in sequence, for a given voltage v_{IN} the segment determination is done first, followed by the step determination. The latter uses a successive approximation sequence. The detailed encoding is described in the next section.

4.4.4 Encoding Sequence

The complete PCM encoding principle is shown in Figure 4.7(a), and the voltage at the input of the comparator in (b). The encoding sequence

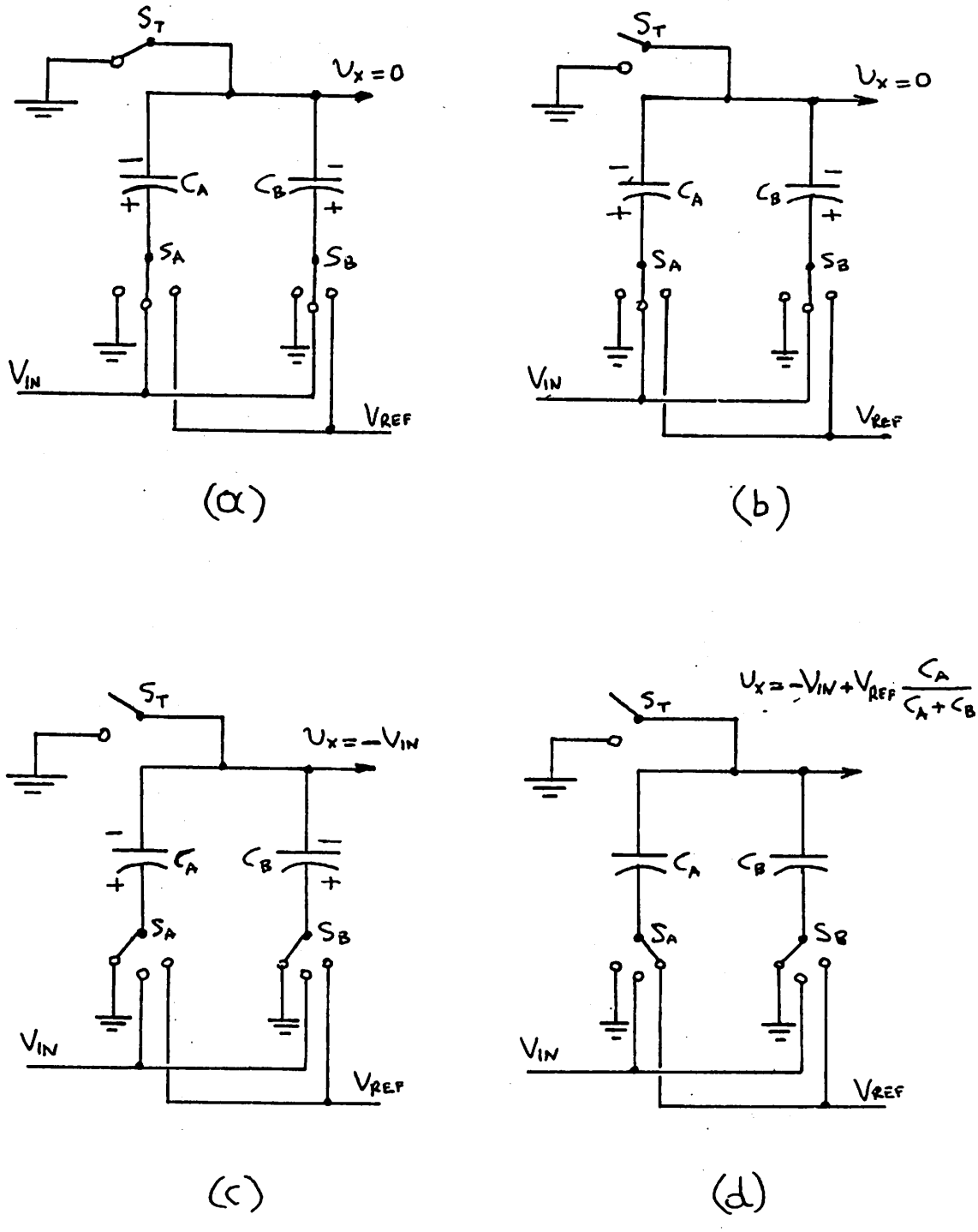
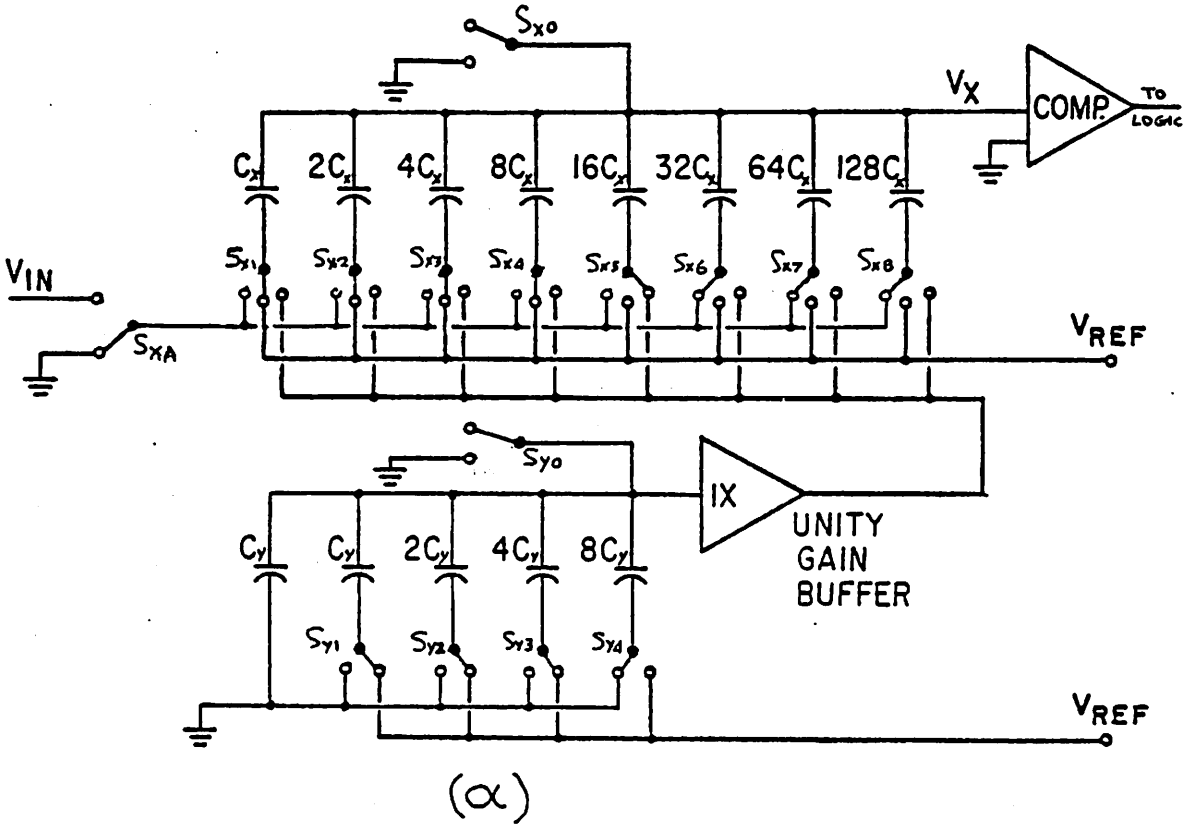
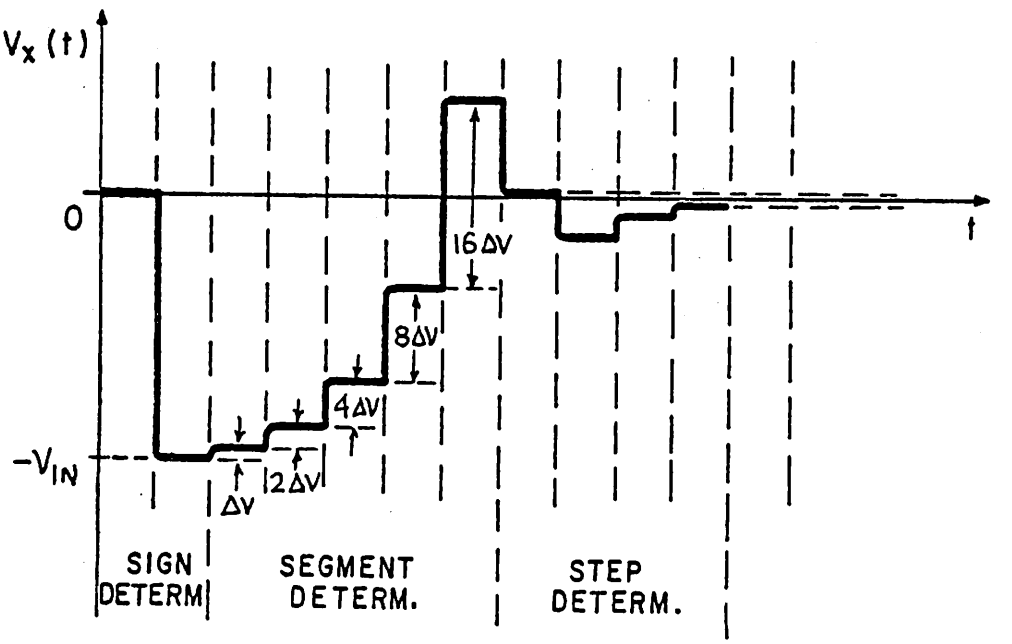


Figure 4.6: Sample-and-Hold and difference functions realization.



(a)



(b)

Figure 4.7: (a) Complete encoder principle.
(b) Comparator input waveform.

will be described by way of example. Assume that at the time of the sampling, v_{IN} is positive and lies in the 8th step of the 5th segment. This is determined by the system as follows:

a) Sampling and sign determination. Switch S_{x0} is thrown to ground, and S_{x1} through S_{x8} to the input voltage (through S_{x4}). Let v_{IN} be the value of the input at the end of this step. This value is thus sampled and stored on the x array. Next, S_{x0} is opened and S_{x4} is thrown to ground, making v_x equal to $-v_{IN}$, as shown in (b). The sign of v_x is sensed by the comparator, whose state therefore determines the sign of v_{IN}. This information is fed to the logic, which connects a positive or a negative reference voltage to the buses labeled V_{REF}, according to whether the sign of v_{IN} was sensed as positive or negative. For the particular example, a positive reference voltage is connected. The first bit of the 8-bit PCM word, corresponding to the sign of v_{IN}, has been determined at the end of this step.

b) Segment determination. Switch S_{x1} is thrown to V_{REF}, making v_x increase by an amount ΔV corresponding to the first segment, as shown in (b). Since v_x does not change sign after this, the next switch (S_{x2}) is thrown, then the third, and so on, until the comparator senses a change of sign in v_x, which happens just after S_{x5} is thrown. This information is interpreted by the logic as meaning that v_{IN} lies in the 5th segment. The logic then develops the next three bits of the PCM word, corresponding to segment # 5.

c) Step within segment determination. The system must now determine within which one of the sixteen equal steps of the 5th segment the input lies. To this end, S_{x5} is thrown to the output of the buffer, and fractions of V_{REF}, developed by the y array, are fed to the bottom plate of capacitor $16C_x$. This is done in a successive approximation sequence as

follows: Initially, all capacitors of the y array are discharged by throwing all switches to ground. Next, S_{yo} is opened, and S_{y4} is thrown to V_{REF}, thus making $V_y = V_{REF}/2$. As a consequence v_x drops, as seen in (b), but not enough to make its sign change. This is interpreted by the logic as meaning that v_{IN} must be in the first half of the segment. To check to which quarter of the segment the input corresponds, S_{y4} is thrown back to ground and S_{y3} is thrown to V_{REF}, thus making v_y equal to $V_{REF}/4$. This makes v_x change sign, meaning that v_{IN} is in the second quarter of the segment. S_{y3} is left at V_{REF}, and S_{y2} is also thrown to V_{REF}. No sign change occurs in v_x, meaning that v_{IN} is in the fourth eigth of the segment. Finally, to check in which sixteenth of the segment v_{IN} lies, S_{y3} and S_{y2} are left undisturbed and S_{y1} is thrown to V_{REF}, which does not result in a sign change in v_x. At the end of this therefore, v_{IN} has been bounded by the values $V_{REF}/2$ and $7(V_{REF}/16)$, and therefore must lie in the 8th step of the segment. The last 4 bits of the PCM word are thus determined by the logic, and the conversion is complete. For this particular example, and for the code format shown in Figure 2.15(b), the logic develops the PCM word 1 100 0111 at the output of the encoder, either in parallel form or sequentially. The final position of the switches at the end of the encoding process is as shown in Figure 4.7(a).

In the encoding scheme described, one step is needed for sampling, one for sign determination, up to eight steps for segment determination, and four steps for step determination. A maximum of fourteen steps is therefore needed for the complete encoding of each input value.

The scheme described implements an encoding law in which there are sixteen equal steps in the first segment. In the actual encoding law of Figure 2.15(a) however, there are 15 1/2 steps rather than sixteen in the first segment, the half-step being adjacent to the origin. This half-step,

along with the symmetrical half-step for negative inputs, result in a whole step which has the origin as its middle point. As will be explained in the following section, whether there are 16 or 15 1/2 steps in the first segment is of minor importance. If it is desired that the half-step detail be implemented, one can introduce an offset to the x array at the beginning of the conversion, which is equivalent to the half step. To do this, a ninth capacitor can be connected to the top plate, as shown in Figure 4.8(a). A positive or the negative voltage V_H is connected to this system according to whether the sign of the input voltage has been determined to be negative or positive, respectively, at the beginning of the conversion sequence. One particular realization, which derives V_H from V_{REF}, is shown in Figure 4.8(b).

From the description given it should be clear that v_x can be set to any value rather than zero at the beginning of the encoding, and then converged back to that value through the encoding process. This is so because the whole principle is based on changes in v_x rather than the absolute value of v_x itself.

4.5 EFFECT OF NONIDEALITIES

4.5.1 Introduction

In an implementation of the encoder scheme proposed in section 4.3, several nonidealities which can deteriorate the system performance might be present. These include parasitic capacitances, capacitor value errors, offset voltage in the comparator, offset voltage and gain error in the buffer, and mismatch between positive and negative reference voltages. In order to discuss these nonidealities, we will consider a practical encoder coupled to an ideal decoder, and we will investigate the effect of the nonidealities on the complete codec. Errors in the transfer charac-

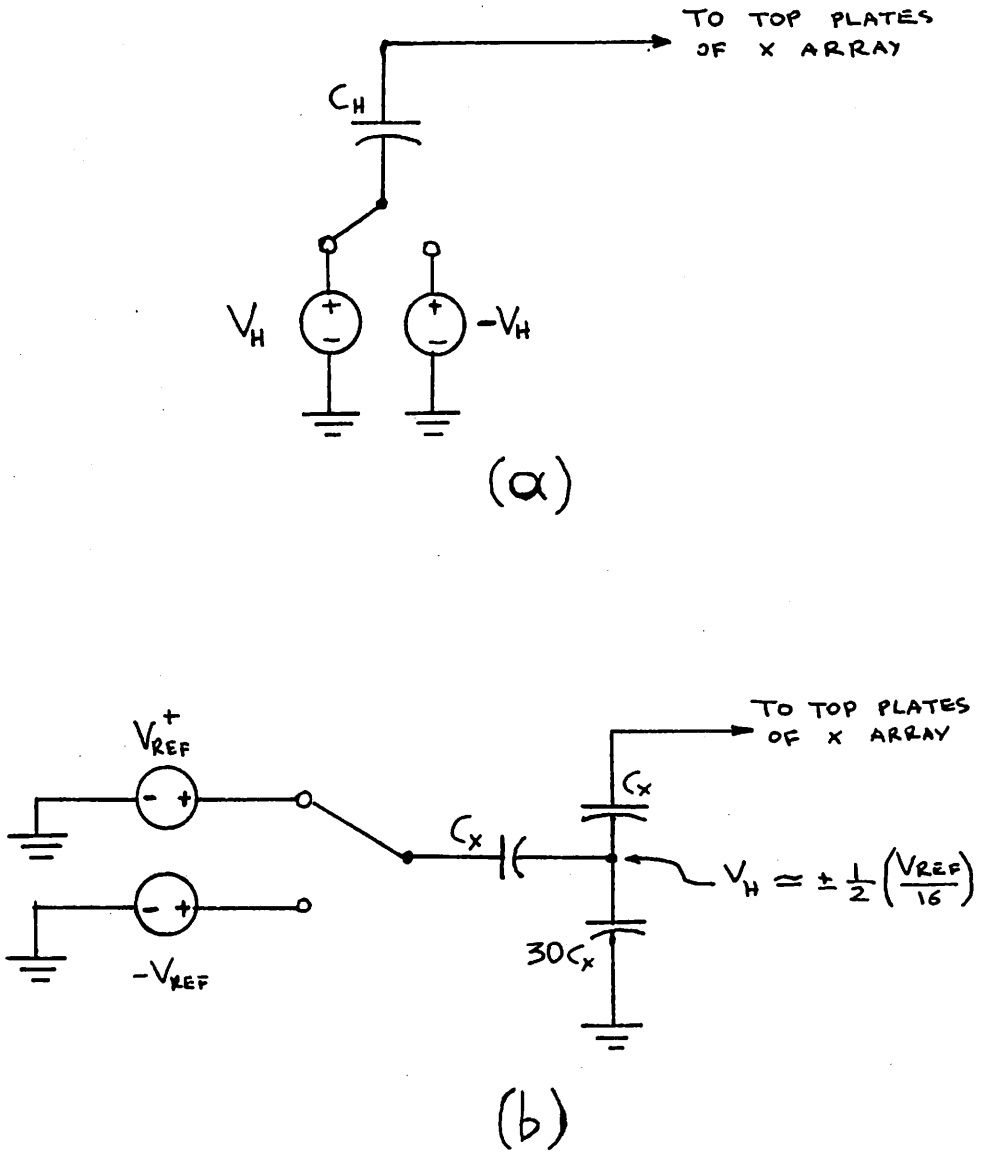


Figure 4.8: Methods for introducing a one-half step offset in the first segment.

teristic of this codec will be manifested as degradation in the signal-to-distortion and gain tracking performance. For various sets of values of the nonidealities, these parameters will be compared to the specifications set by the Bell System for their D3 Channel Bank [30]. Two of these specifications are shown in Figure 4.9.

4.5.2 Computer Simulation

The complete encoder including all important nonidealities is shown in Figure 4.10. A straightforward analysis of this circuit combined with the encoding sequence described in section 4.3, gives the set of decision levels for this encoder. A computer subroutine that calculates these decision levels was written, which is given in Appendix B. This subroutine was used as part of the simulation program XCODEC, which is discussed in Chapter 3 and Appendix A, in order to evaluate the encoder performance in conjunction with an ideal decoder, for various sets of values of the nonidealities. The effect of these nonidealities is discussed both qualitatively and in terms of the computer simulation results in the subsections that follow. A sample output of a computer run for a typical set of nonidealities is given in Appendix B.

4.5.3 Parasitic Capacitances

There are several parasitic capacitances associated with the encoder of Figure 4.7, which are due to junction capacitance, interconnect and gate overlap capacitance of the switch devices and the input devices of the comparator and the buffer. Of these, the parasitic capacitances appearing between the bottom plates of the x and y array capacitors and ground have no effect in the performance: As the bottom plates of the array capacitors are being switched between the various DC voltages required, these parasitics will only affect the shape of the voltage wave-

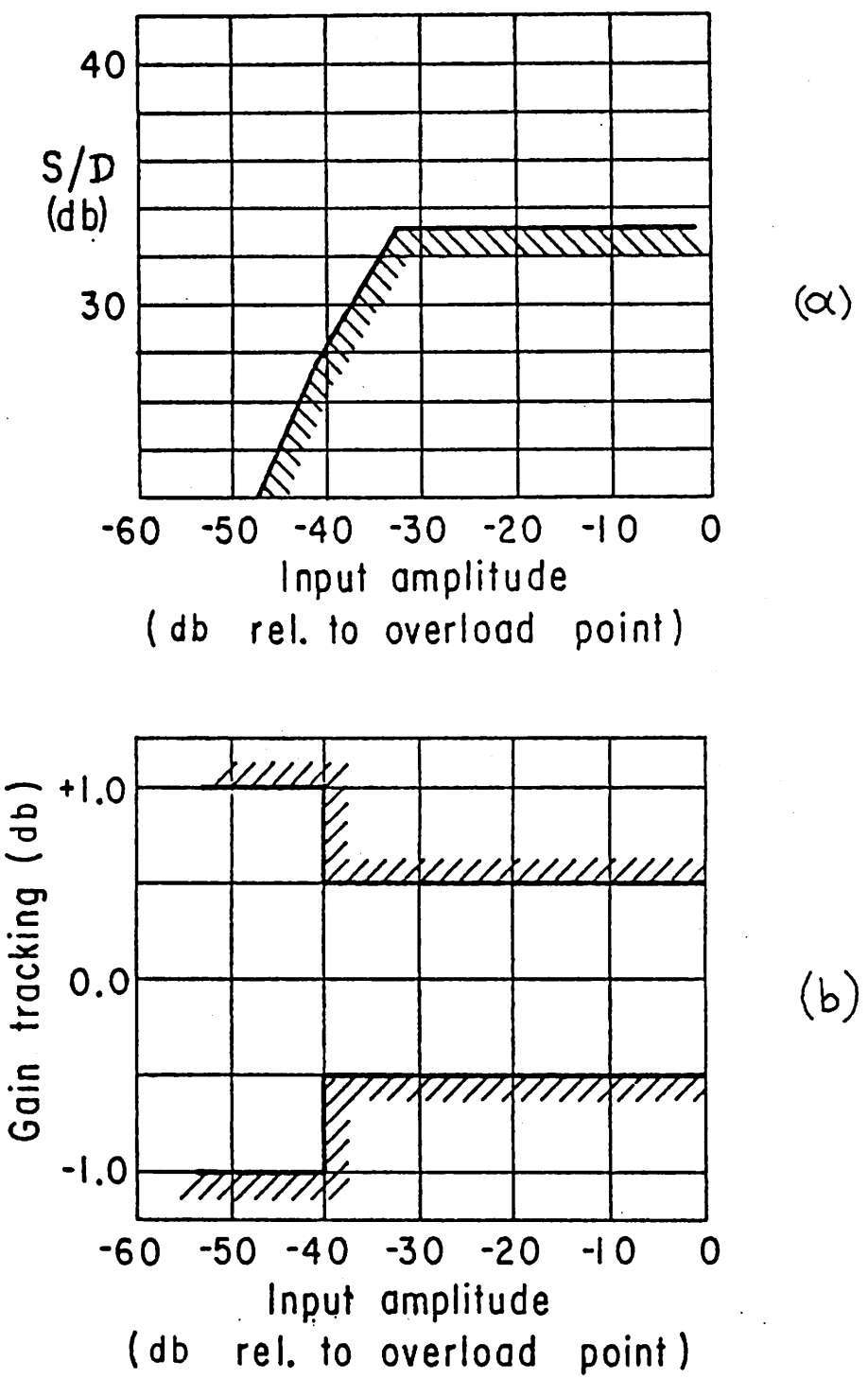


Figure 4.9: D3 Channel Bank specifications.
(a) Signal-to-distortion ratio.
(b) Gain tracking.

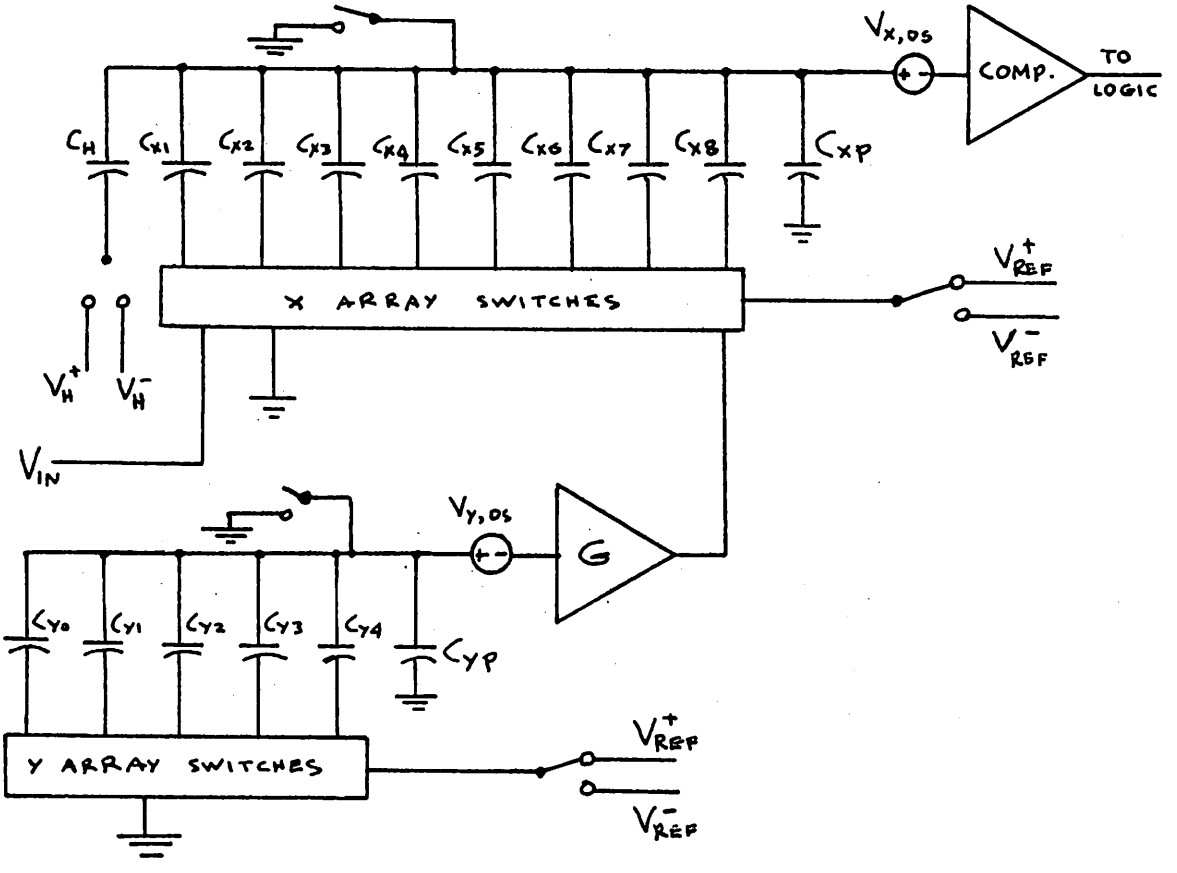


Figure 4.10: Encoder principle including important nonidealities.

forms during the transition. It is however clear that the final DC voltages at the bottom plates after the transients cannot be affected by the parasitics. Since the final values of V_x and V_y only depend on the initial and final values of these voltages, these parasitics cannot affect the performance of the system.

The parasitic capacitance between the top plates of the x array and ground does not have any significant effect for the following reason: The encoding sequence discussed in the previous section starts with $V_x = 0$ and finishes with $V_x \simeq 0$. This means that the parasitic starts and finishes with the same charge, and therefore it does not contribute a net amount of charge to the array's top plates over the encoding cycle. This will be the case even if this parasitic capacitance is nonlinear. For this reason, the value of the parasitic can be larger than C_x without affecting the encoder's performance, which is a significant feature of this scheme.

The parasitic capacitance between the top plates of the y array and ground will have the effect of reducing the values of the voltage v_y produced by that array, its effect on the encoding characteristic being as shown in Figure 4.11. If no parasitic were present, the beginning of the last step of the segment would correspond to $V_y = (15/16)V_{REF}$. If a parasitic of value KC_y is present, that value will instead be: $V_y = [15/(16 + K)]V_{REF}$. These values will be off by a quantity corresponding to half a step for a parasitic such that:

$$\frac{15}{16} V_{REF} - \frac{15}{16 + K} V_{REF} = \frac{1}{2} \frac{V_{REF}}{16} \tag{4.16}$$

This gives a value of $0.55\ C_y$ for the parasitic. All other decision levels will be off by less than half a step. Notice that this parasitic

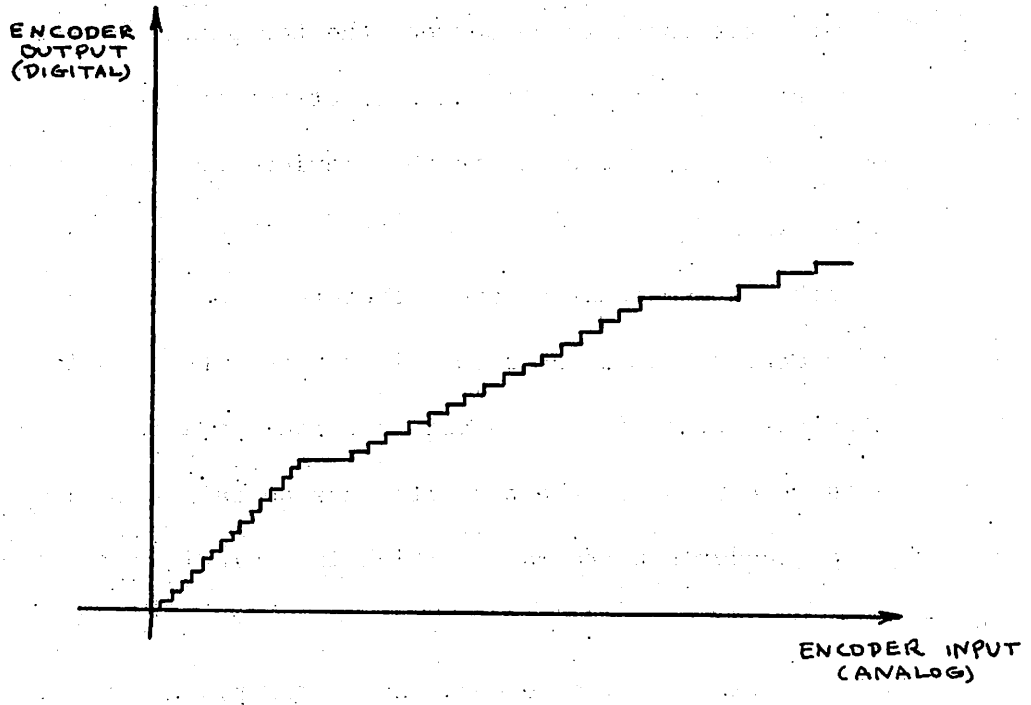


Figure 4.11: Effect of parasitic capacitance in the y array, and/or of buffer gain error.

has no effect on the boundaries between segments, the latter being determined by the x array. The effect of the parasitic on signal-to-distortion ratio and gain tracking has been investigated using XCODEC. It has been found that parasitics larger than C_y can be tolerated.

4.5.4 Buffer Gain Error

An error in the gain of the buffer will result in a characteristic like the one shown in Figure 4.11. In the absence of buffer offset, its effect is the same as that of parasitic capacitances at the top plates of the y array. Simulation shows that gain errors as high as 10% can be tolerated.

4.5.5 Buffer Offset

The effect of an input offset in the unity gain buffer is equivalent to adding to all values of V_y a constant amount equal to that offset. Since this cannot affect the values at the boundaries between segments, the resulting characteristic will be like the one in Figure 4.12. For a reference voltage of 5 volts, each step corresponds to an increment in V_y of 5/16 volts. An offset of 156 mV, therefore, would result in a displacement of all decision levels within a segment by half a step. This suggests that quite large buffer offsets can be tolerated. Simulation results show satisfactory encoder performance even in the presence of buffer offsets as high as 300 mV.

4.5.6 Comparator Offset

The effect of comparator offset on the encoder characteristic is shown in Figure 4.13. It is obviously important that this offset be kept small, since otherwise small inputs, for which high resolution is necessary, can fall in regions of more coarse resolution which will de-

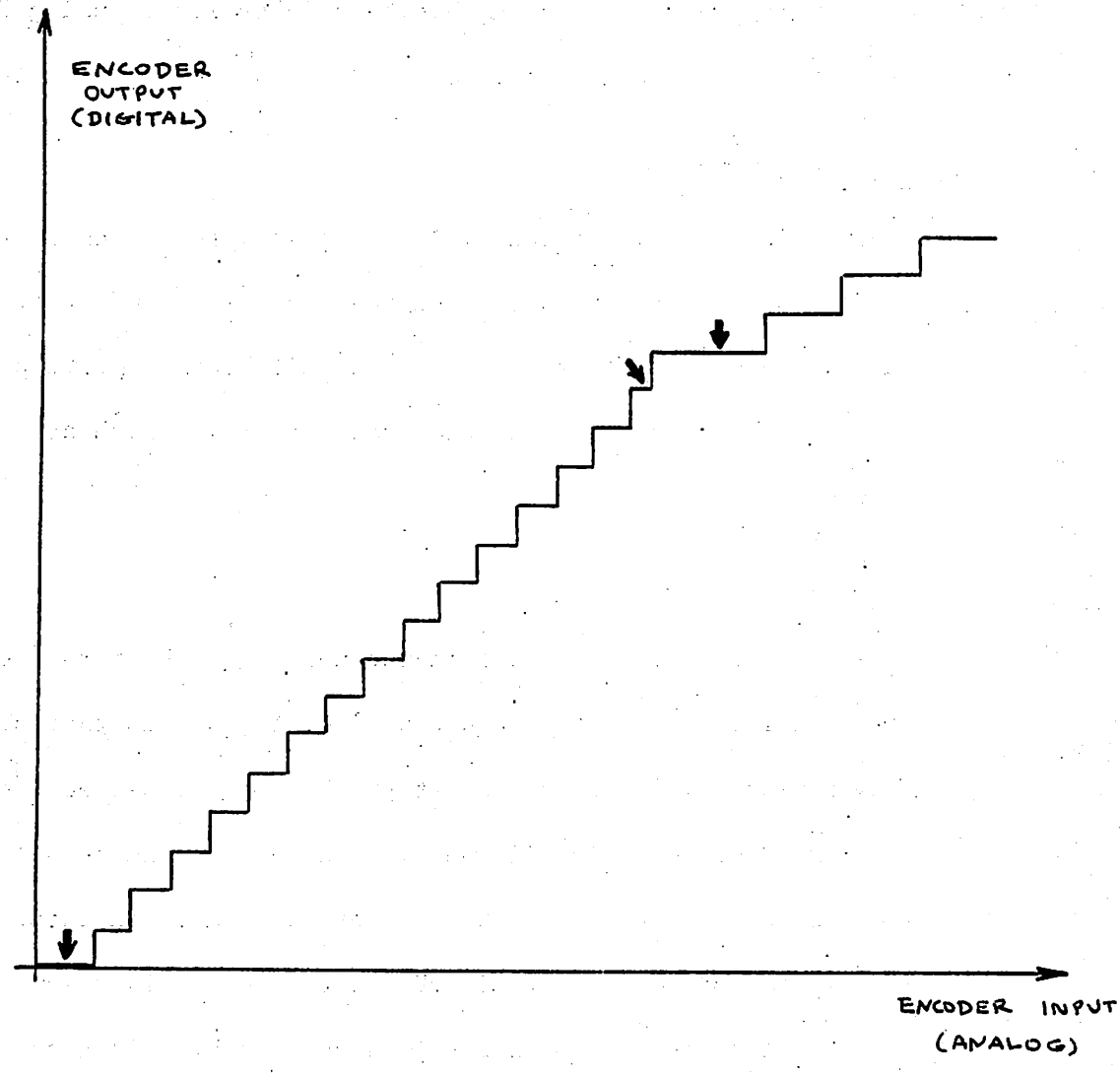


Figure 4.12: Effect of positive offset in the buffer.

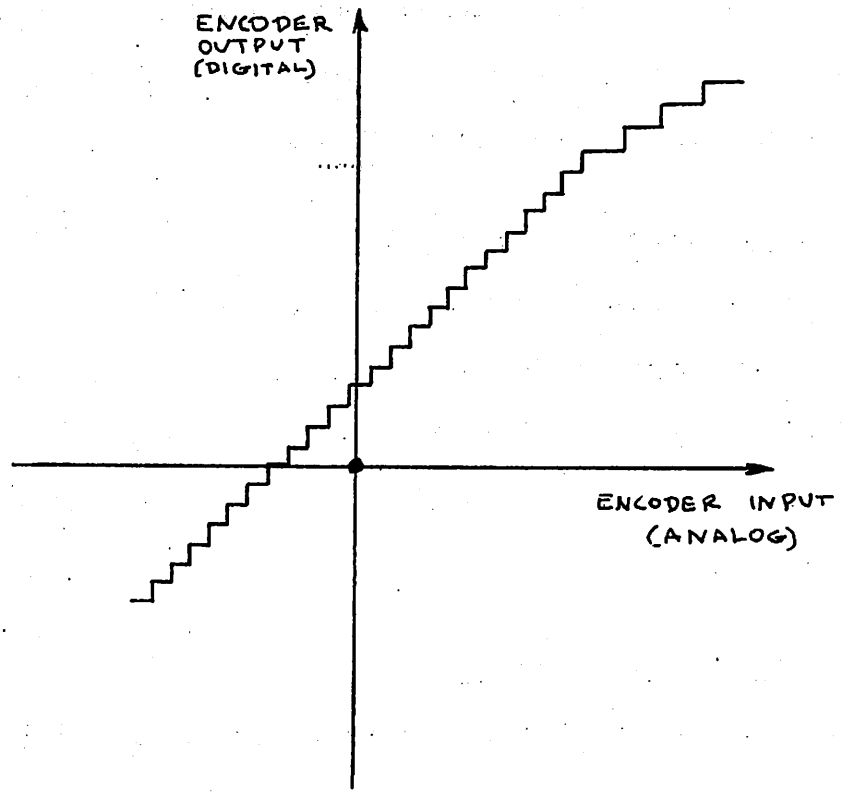


Figure 4.13: Effect of comparator offset.

grade the performance. For a 5 v reference, the length of the first segment is approximately 20 mV. Although a comparator offset of 20 mV still gives a signal-to-distortion ratio which meets the D3 specifications, the resulting gain tracking is not acceptable. In order to have good gain tracking and allow for additional nonidealities, a comparator offset of 10 mV or less is desirable. The computer predicted Signal-to-Distortion performance for an offset of 10 mV is shown in Figure 4.14.

4.5.7 Reference Sources Mismatch

Mismatch between positive and negative reference voltages will destroy the symmetry of the encoder characteristic, as shown in Figure 4.15. The different average slopes for positive and negative inputs results in signal-to-distortion degradation. Simulation shows that 2% mismatch can be tolerated.

4.5.8 Capacitor Value Errors

From the description of the encoding principle given in section 4.3, it is apparent that what is really important for accurate encoding is not the absolute values of the capacitors in the arrays, but rather the ratios between them and the total capacitance. Capacitor errors in the x array will result in average slope errors for the segments in the encoding characteristic. Errors in the y array will result in unequal step sizes for each segment.

Several different combinations of capacitor value errors have been tried using the simulation program, and it was found that for the top array errors as high as 10% for the smallest capacitor and 0.2% for the largest can be tolerated, the figures for the other capacitors of that array being between these numbers. For the lower array, the corresponding figures are 10% for the smallest and 1% for the largest capacitor.

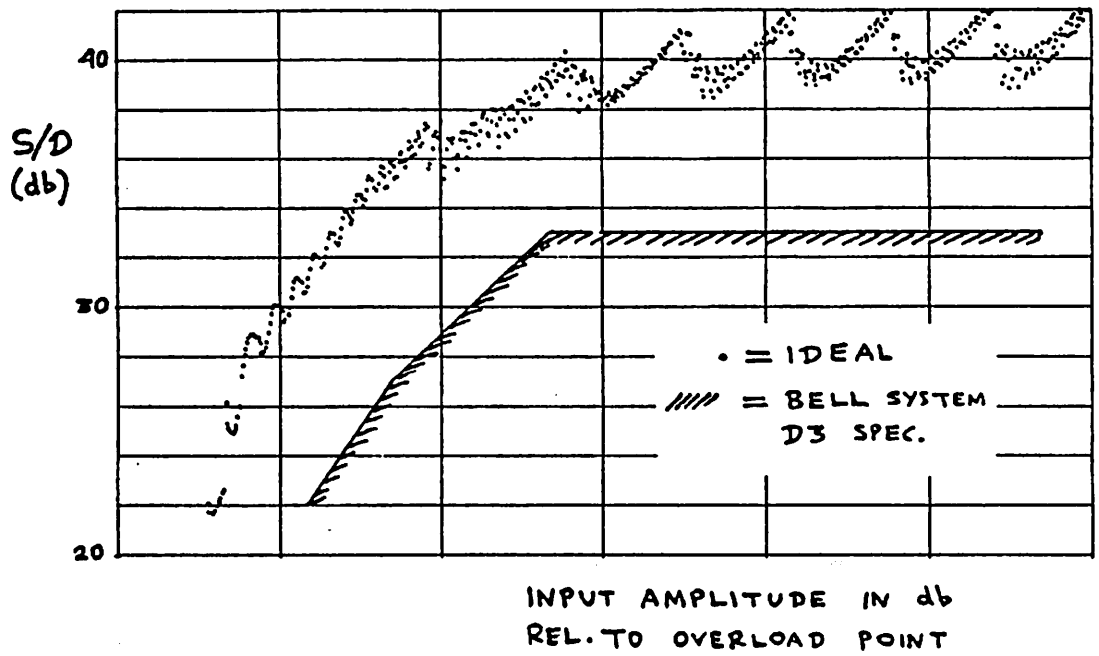


Figure 4.14: Computer simulation of S/D vs. input amplitude for a comparator offset of 10 mV and all other parameters ideal.

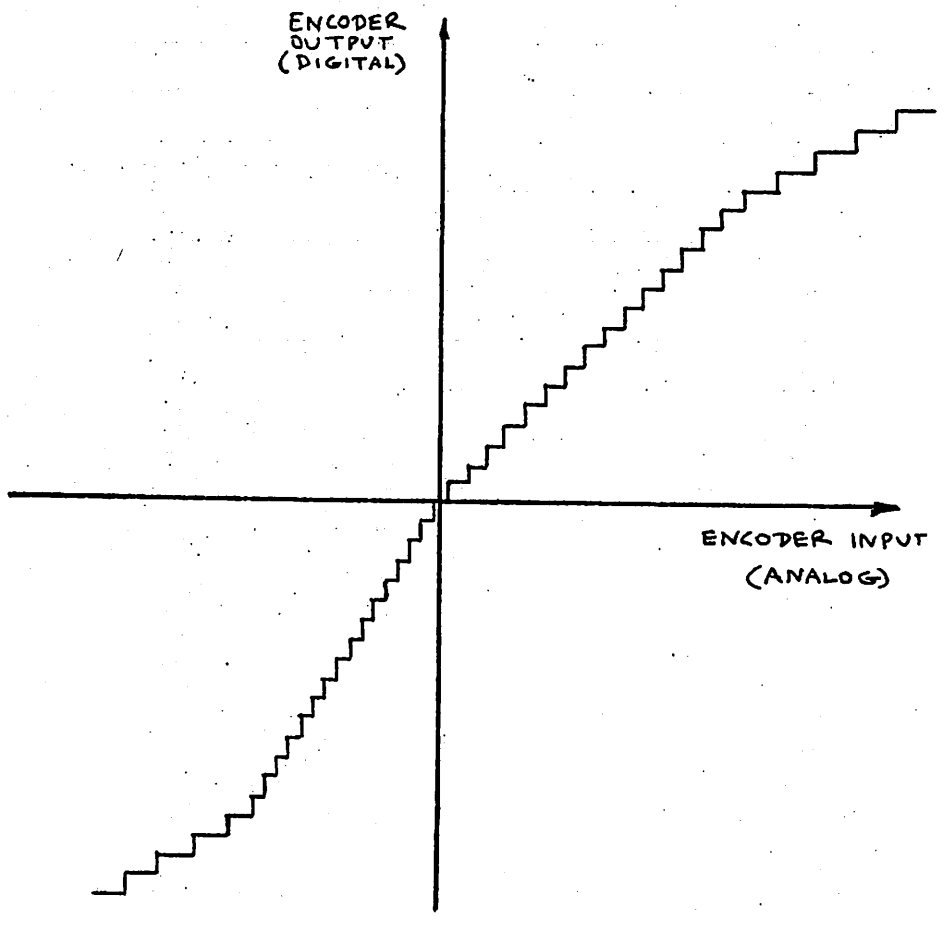


Figure 4.15: Effect of reference source mismatch.

4.5.9 Effect of the Half Step at the Origin

Simulation shows that using sixteen equal steps in the smallest segment rather than the 15 1/2 required for smooth transition at the origin, does not result in any significant degradation in the encoder performance when compared to the degradation due to other nonidealities. The signal-to-distortion ratios for the two cases differ by a fraction of a db even for low amplitudes.

4.5.10 Several Errors Combined

Simulation has been used for determining the performance of the encoder for several sets of values of the nonidealities discussed above. Although it is impossible to try all meaningful combinations of values, the numerous XCODEC runs made suggest that a reasonable design goal can be set as follows, for a reference voltage of 5 v.

a) Comparator offset: < 10 mV

b) Buffer offset: < 100 mV

c) Buffer gain error: < 2%

d) Reference sources mismatch: < 2%

e) x array capacitor value errors: 10% for smallest capacitor, 0.2% for largest.

f) y array capacitor value errors: 10% for smallest capacitor, 1% for largest.

The signal-to-distortion ratios versus input amplitude for two typical combinations of nonidealities are given in Figures 4.16 and 4.17. In each case, the circuit parameter values are given at the bottom of the figures. Although not shown in the figures, the gain tracking performance for these cases met the specifications for the D3 Channel Bank.

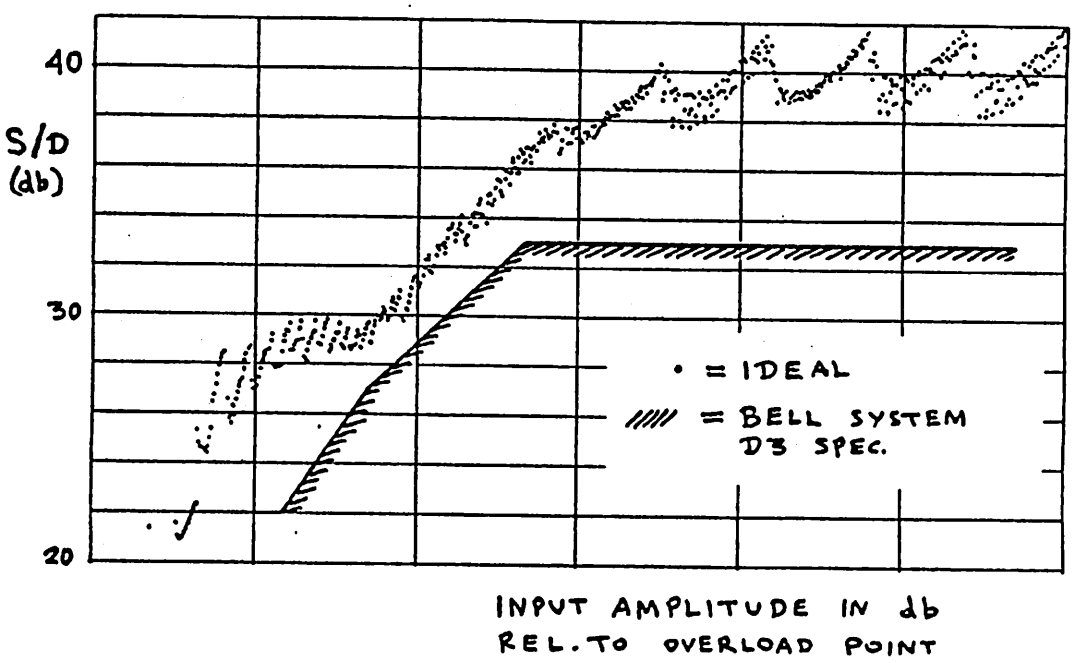


Figure 4.16: Computer simulation of S/D vs. input amplitude for the following nonidealities:

Comparator offset: 10 mV
Reference sources mismatch: 1%
Capacitor value errors with respect to nominal values (starting with smallest capacitor):
x array:
10%, -10%, 5%, -2.5%, 1%, -0.5%, 2%, -2%

y array:
8%, 8%, -4%, 2%, -2%

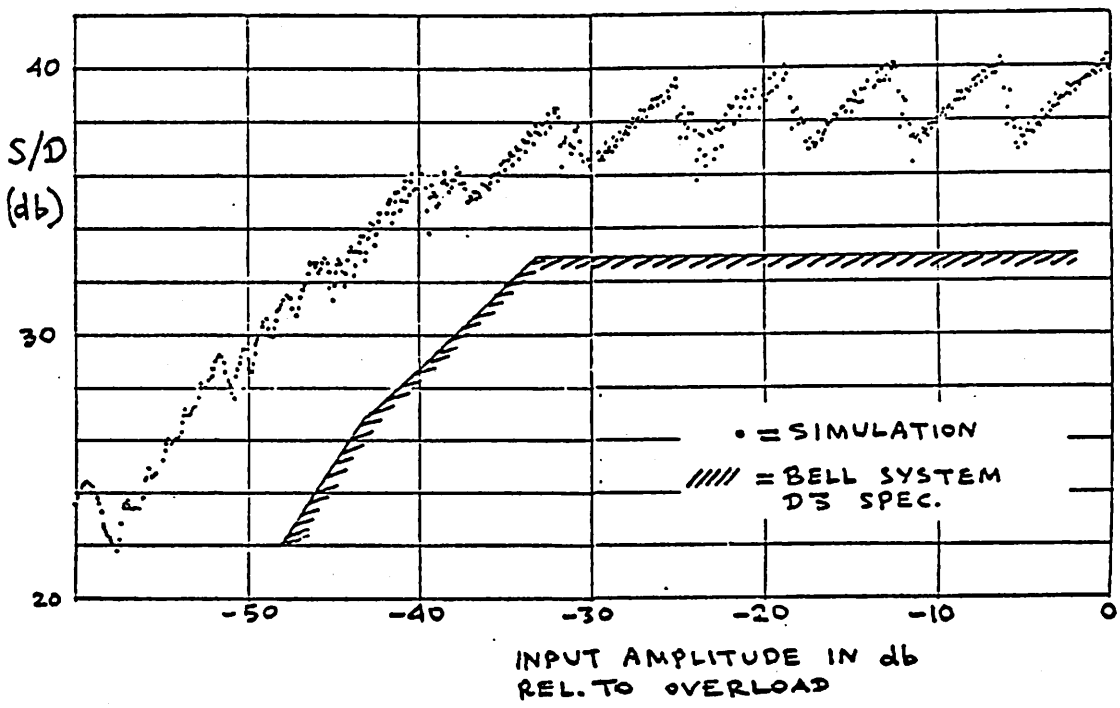


Figure 4.17: Computer simulation of S/D vs. input amplitude for the following nonidealities:

Comparator offset: 5 mV
Buffer offset: 80 mV
Buffer gain: 0.97

Parasitic capacitance in each array: 3.8% of total array capacitance.

4.6 ESTIMATES FOR AN INTEGRATED CIRCUIT IMPLEMENTATION

The circuit parameters necessary for satisfactory encoder performance, which were determined by computer simulation in the previous section, can be achieved using integrated circuit technology. An implementation using metal gate NMOS technology is proposed below. All critical parts in this implementation have been fabricated and the prototype is described in detail in Chapter 7. The experimental results, which meet the specifications for the D3 Channel Bank, are also described there.

In the proposed encoder, a comparator scheme is used which is described in detail in [28] and is given in Chapter 7. Input offset voltages of the order of 5 mV are achieved using this scheme [34], which satisfies the goals set in subsection 4.4.10. The buffer can be implemented by using an operational amplifier connected in a unity gain configuration. An amplifier has been designed and fabricated which achieves stricter goals than those set in subsection 4.5.10. This amplifier is described below.

The required capacitor accuracy can be met using an x array with a smallest capacitance of 0.25 pF, which makes the largest capacitance in that array equal to 32 pF. For the y array, these numbers are 4 pF and 32 pF respectively. Yield considerations for these capacitor arrays are given below.

An estimate of the time needed for complete encoding will now be made. The encoding sequence consists of a maximum of 14 steps, as already described. For each step, 2 μsec is alloted for the settling of the buffer (see Chapter 6), 1 μsec for comparator settling and 1 μsec for switch delays. The total encoding time calculated this way is 56 μsec.

A conservative estimate of the chip area that would be required for a

completely integrated encoder can be made as follows: The required logic consists of 150 gates and 50 flip-flops [35] which can be accommodated in an area of 3000 mil^2. The area of the switches required has been estimated as 1500 mil^2. The buffer occupies an area of 1200 mil^2, the comparator 1000 mil^2 and the two arrays 200 mil^2. This makes total area equal to 8700 mil^2, and with additional interconnect between these elements, a total chip area of 15000 mil^2 should certainly be sufficient.

The total power consumption has been estimated at 315 mW, allowing for 150 mW for the buffer, 15 mW for the logic and 150 mW for the switch drivers.

A rough estimation of the yield expected from a completely integrated encoder will now be given. As has been explained in this chapter, the requirements imposed on the buffer are very relaxed, and in fact the yield for the second version of the integrated buffer has exceeded 90% [43]. McCreary [34] has performed accurate measurements on 47 capacitor arrays on three different wafers, which show that practically 100% of these meet the requirements imposed on the y array, when the latter has a total capacitance of 64 pF. It is reasonable to assume that the encoder yield is limited by the accuracy of the x array. Computer simulation has shown that the specifications on signal-to-distortion ratio and gain tracking are exceeded for most combinations of the errors in the x array, as long as the magnitudes of the individual errors remain below certain bounds. These bounds can be defined in terms of percentages of the nominal value of each capacitor, where by nominal value is meant the ideal value the capacitor should have given the total array capacitance. One set of percentage error bounds is given below, starting with that for the smallest capacitor and proceeding towards that for the largest:

10%, 10%, 5%, 2.5%, 1%, 0.5%, 0.2%, 0.2%.

It should be noted that these by no means represent the only possible bounds. A detailed evaluation of such bounds is not feasible because it would require enumeration of all error combinations. Examination of the experimental data mentioned above showed that for a total x array capacitance of nominally 64 pF, 77% of the arrays measured showed errors within the bounds given above. This indicates that a yield of the order of 70% to 80% can be expected using the process given in Appendix F.

The partially integrated prototype is described in detail in Chapter 7, along with the experimental results.

4.7 IMPLEMENTATION OF OTHER ENCODING LAWS

The principle of charge redistribution can be used to implement other kinds of segmented encoding laws. For example, consider the 13-segment approximation to the A-law, shown in Figure 2.17. In this law, the two segments nearest to the origin for each input polarity have the same step size, and therefore the same average slope. This can be implemented by the encoder scheme described if the two smallest capacitors of the x array are made of equal value. Since the rest of the segments have average slopes related by factors of 2, with the step size doubling as one goes from one segment to the next, the values of the x-array capacitors will be C_x, C_x, $2C_x$, $4C_x$, $8C_x$, $16C_x$, $32C_x$, $64C_x$.

If a 7-bit word is desired, which corresponds to 8 steps per segment, the lower array will have to be modified. Its capacitors in that case will have values C_y, C_y, $2C_y$, $4C_y$, and the fifth capacitor will be omitted.

CHAPTER 5

REALIZATION OF ANALOG FUNCTIONS IN SINGLE CHANNEL MOS TECHNOLOGY

5.1 INTRODUCTION

Analog integrated circuits made with MOS technology are almost non-existent, in contrast to the great variety of digital MOS circuits. Completely analog chips can be made with bipolar transistor technology, which achieve a level of performance which is very difficult for MOS to reach. However, the need for analog MOS circuits still exists, mainly as part of LSI circuits that require both digital and analog functions. Logic in such systems can be designed in MOS, which offers advantages as far as both chip area and cost is concerned. However in most cases the analog functions have to be handled externally, by a separate IC which is invariably bipolar. It would thus be very desirable if some basic analog functions could be implemented in MOS allowing the realization of a complete digital-analog LSI system on a single chip.

In this chapter, the realization of analog functions in n-channel MOS technology will be discussed. However, the principles developed apply equally well to p-channel MOS technology.

5.2 NOTATION AND APPROXIMATIONS

This section is intended to establish the notation, conventions and approximations to be used in this chapter. Detailed treatments on the characteristics of the MOS transistor can be found in the references [36, 37, 38, 39].

The physical structure of a simple geometry NMOS transistor is shown in Figure 5.1(a), and its symbol and associated notation in Figure 5.1(b). Let μ be the mobility, C_o the oxide capacitance per unit area, Z the width and L the length of the channel, and V_T the threshold voltage. We will define two constants, K' and K as follows:

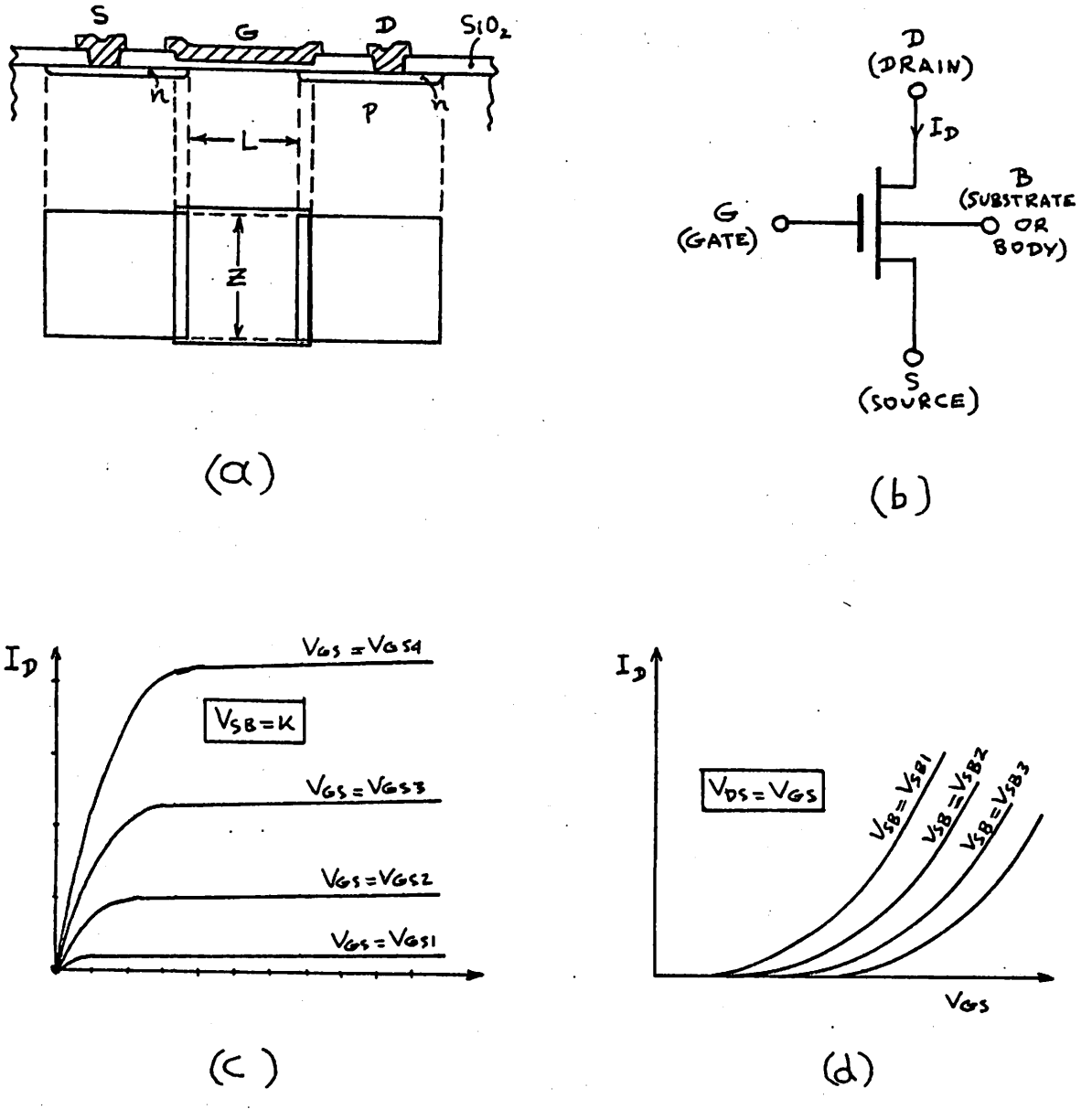


Figure 5.1: (a) Physical structure of NMOS transistor of simple geometry.
(b) Symbol and notation.
(c), (d) Typical characteristics.

$$K' = \frac{1}{2} \mu C_o \tag{5.1}$$

$$K = \left(\frac{Z}{L}\right) K' \tag{5.2}$$

The approximate equations for the MOS transistor can be derived from the Shichman-Hodges model [40] as follows:

a) Non-saturation region ($V_{DS} \leq V_{GS} - V_T$):

$$I_D = K[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \tag{5.3}$$

b) Saturation region ($V_{DS} \geq V_{GS} - V_T$):

$$I_D = K(V_{GS} - V_T)^2 \tag{5.4}$$

or:
$$V_{GS} = V_T + \sqrt{\frac{I}{K}} \tag{5.4a}$$

In the above equations the channel length modulation is not taken into account, and the mobility μ is assumed independent of V_{GS}.

The depencence of V_T on the source-to-substrate voltage will approximately be described by:

$$V_T = V_{TO} + \gamma \sqrt{V_{SB} + 2\phi} - \sqrt{2\phi} \tag{5.5}$$

where V_{TO} is the threshold voltage when $V_{SB} = 0$, ϕ is the equilibrium junction potential and γ is the body effect coefficient.

Typical plots displaying the characteristics of an MOS transistor are shown in Figures 5.1(c) and (d).

Differentiation of equation (5.4) gives, for the small signal transconductance in the saturation region:

$$g_m = 2K(V_{GS} - V_T) \tag{5.6}$$

or:

$$g_m = 2\sqrt{KI} \tag{5.6a}$$

or:

$$g_m = \frac{2I}{V_{GS} - V_T} \tag{5.6b}$$

The total gate-to-source and gate-to-drain overlap capacitances will be denoted by C_1 and C_2, respectively. The source-to-substrate and drain-to-substrate junction capacitances will be denoted by C_{SB} and C_{DB}, and the gate-to-channel capacitance by C_G.

5.3 THE MOS TRANSISTOR AS AN ANALOG CIRCUIT ELEMENT

As far as analog applications are concerned, the two basic advantages of the MOS transistor are its high input resistance and the fact that it makes a very good zero-offset analog switch. However, it is inferior to the bipolar transistor in most other respects, and this is one of the reasons that analog MOS circuits have not been developed to any extent so far. In this section the parameters of the MOS transistor, relevant to its behavior as part of analog circuits, are briefly discussed. This is intended both as an overview and to place in context the more detailed discussions of the sections to follow. Only those parameters that play an important role in most conceivable configurations will be discussed. Parameters associated with specific configurations, like the input offset voltage of a differential pair, will be discussed in the sections where these configurations are donsidered.

a) Transconductance. The low value of transconductance is one of the most serious drawbacks of MOS as an amplifier element. Using equation (5.6) and the corresponding expression for bipolar devices one can show that for a current of 100 μA, the transconductance obtained with a minimum geometry bipolar transistor can be as much as 40 times the transconductance of an MOS transistor of the same total area at the same current. Therefore, large sizes and/or large currents are needed in MOS to achieve reasonable

values of g_m. This is just opposite to the case of digital MOS IC's: There, one of the main advantages is small size.

b) Control voltage magnitude. From equation (5.4a), and for the values of K encountered in practice, it follows that considerable amounts of gate-to-source voltage are required in order to obtain reasonable amounts of drain current. This is true even in the case of depletion devices ($V_{TO} < 0$). These values are usually of the order of several volts in analog circuits, especially in the case of enhancement devices. This situation is worsened by the body effect, described in equation (5.5). In a circuit, these voltages drops add so that the power supply voltages required can be as high as $\pm$ 15 v. This is in contrast to the bipolar devices, where V_{BE} normally does not exceed 0.7 volts, and circuits operating from $\pm$ 5 volts power supplies are quite common.

c) Output resistance. The output resistance in an MOS device is limited by channel length modulation [37], [38], [39]. This effect can be reduced by increasing the channel length, but there is a limit to this if the device is to be kept at a reasonable size.

d) Input resistance. One of the few advantages of the MOS transistor relative to the bipolar is the practically infinite input resistance. It is only limited by the leakage currents of the gate, and the protection diode associated with it, for the case of an input device. Unfortunately, the only place where this can be an advantage is at the input stage of a circuit, since the configurations possible in single-channel MOS are such that at an intermediate stage, the high input resistance of a device is shunted by a much lower resistance represented by another device.

e) Parasitic capacitances. As described in the above paragraphs, a large device size is necessary if high currents and/or high transconductance is desired. This makes the parasitic capacitances large, causing

problems in the frequency response and transient performance. Many of the problems caused by these capacitances will be investigated in the sections that follow.

f) Quiescent currents. The quiescent currents in single-channel MOS analog circuits are usually high in order for the frequency response of the circuits to be adequate. This will be discussed in the sections to follow. The high currents, along with the high voltages discussed in paragraph (b) above, account for the high power consumption in MOS analog circuits.

5.4 ANALOG CIRCUIT CELLS IN NMOS TECHNOLOGY

5.4.1 Introduction

Individual cells that are available in n-channel metal-gate technology and can find use as part of analog circuits are discussed in this section. Their limitations are pointed out, and their performance when they are imbeded in an environment of other analog cells is considered. Most of these individual cells will be combined in the design of an op amp which will be discussed in Chapter 6.

5.4.2 Elements Available in N-Channel Metal-Gate MOS Technology

There are only two elements that can be used in metal-gate NMOS integrated circuits: NMOS transistors, and capacitors. Although resistors can be made using the N diffusion regions, their sheet resistance is not of a practical value. The design flexibility is therefore limited. The characteristics of the two available elements are described below.

a) NMOS transistors. The parameter K' of equation (5.1) has a value of 5 to 10 $\mu A/v^2$ for a standard n-channel metal-gate process. A value of 7 $\mu A/v^2$ is typical for the process developed at the University of California at Berkeley [28], [34]. The body effect coefficient γ in equation

1.2 for this process.

The minimum dimension used in the above process is 12 μ. Smaller dimensions are possible in the industry. Since a value of 2.5 μ is typical for lateral diffusion, an effective channel length of 7 μ is obtained for a minimum channel length device. The characteristics of the transistors obtained using this process will be given in Chapter 6.

b) Capacitors. Both thin oxide and junction capacitors are available. Thin oxide capacitance per unit area is 34600 pF/cm^2 for an oxide thickness of 1000 Å, and the capacitors obtained using the thin oxide have a typical temperature coefficient of 25 ppm/°c, which is about one tenth of that for junction capacitors. A detailed investigation of MOS capacitors has been done by McCreary [28], and McCreary and Gray [29].

5.4.3 Voltage Level Shifters

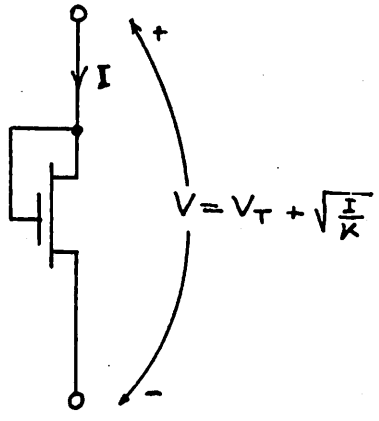
Since no resistors are available, the simplest way to obtain a voltage level shift is shown in Figure 5.2(a). Since the gate is connected to the drain, for a given current the voltage is kept constant at a value determined by equation (5.4), through negative feedback. It is easily seen that the small-signal resistance of the resulting two-terminal element is given by:

$$r = \frac{r_o}{1 + g_m r_o} \tag{5.7}$$

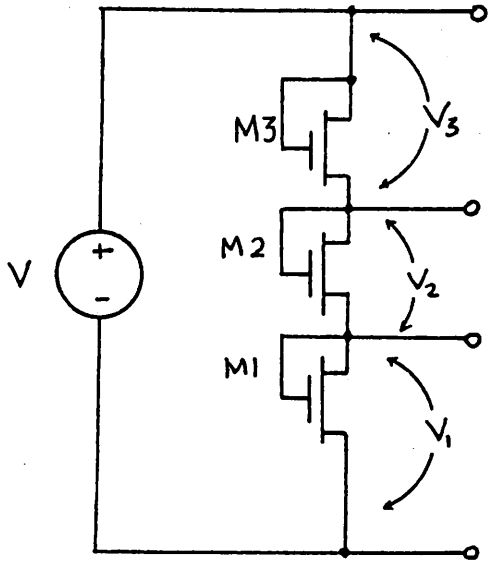
where r_o is the small-signal output resistance of the transistor. For the common case of $r_o >> 1/g_m$, this equation reduces to:

$$r \approx \frac{1}{g_m} \tag{5.8}$$

More than one voltage level shifters can be combined to form a voltage divider, as shown in Figure 5.2(b).



(a)



(b)

Figure 5.2: (a) Voltage level shifter.
(b) Voltage divider.

5.4.4 Current Mirrors

A current mirror is shown in Figure 5.3(a). Assuming that M2 is in the saturation region and that the small-signal output resistances of the devices are infinite, application of equation (5.4) gives:

$$\frac{I_2}{I_1} = \frac{(Z/L)_2}{(Z/L)_1} \tag{5.9}$$

In practice, the fact that r_o is finite makes I_2 dependent on V_{DS2}. To decrease this dependence one can increase Z_2 and L_2 at the same proportion. This will decrease the effect of channel length modulation, resulting in a higher r_o. The limitation of this method is of course the fact that the physical size and the parasitic capacitances will also increase.

Another way to increase the effective output resistance of the current mirror is as shown in Figure 5.3(b). It is easily shown that the equivalent small-signal resistance when looking into the drain of M4 is:

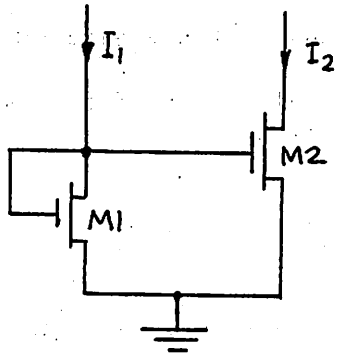
$$r_{o,eq} = r_{o4}(1 + g_{m_4} r_{o_2}) \tag{5.10}$$

The drawback of this configuration is that the minimum DC voltage allowed at the drain of M4, before the device is brought out of the saturation region, is much higher than in the case of Figure 5.3(a).

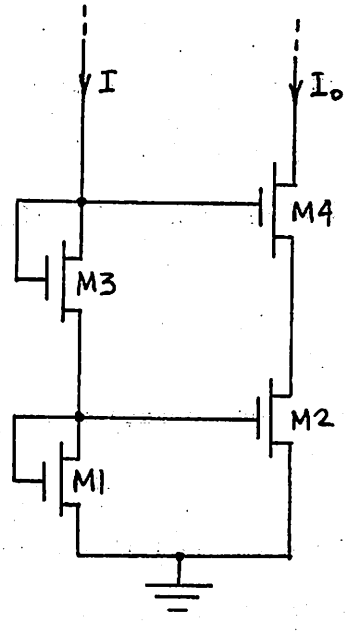
Unfortunately, the lack of complementary devices in NMOS does not allow for simple current mirrors of the opposite polarity. Thus, only current mirrors whose output is a current sink are feasible.

5.4.5 Current Sources

By combining a voltage divider and a current mirror, a current source can be formed as shown in Figure 5.4. It is to be noted that the output currents of these current sources are relatively independent on their output



(a)



(b)

Figure 5.3: Current mirrors.

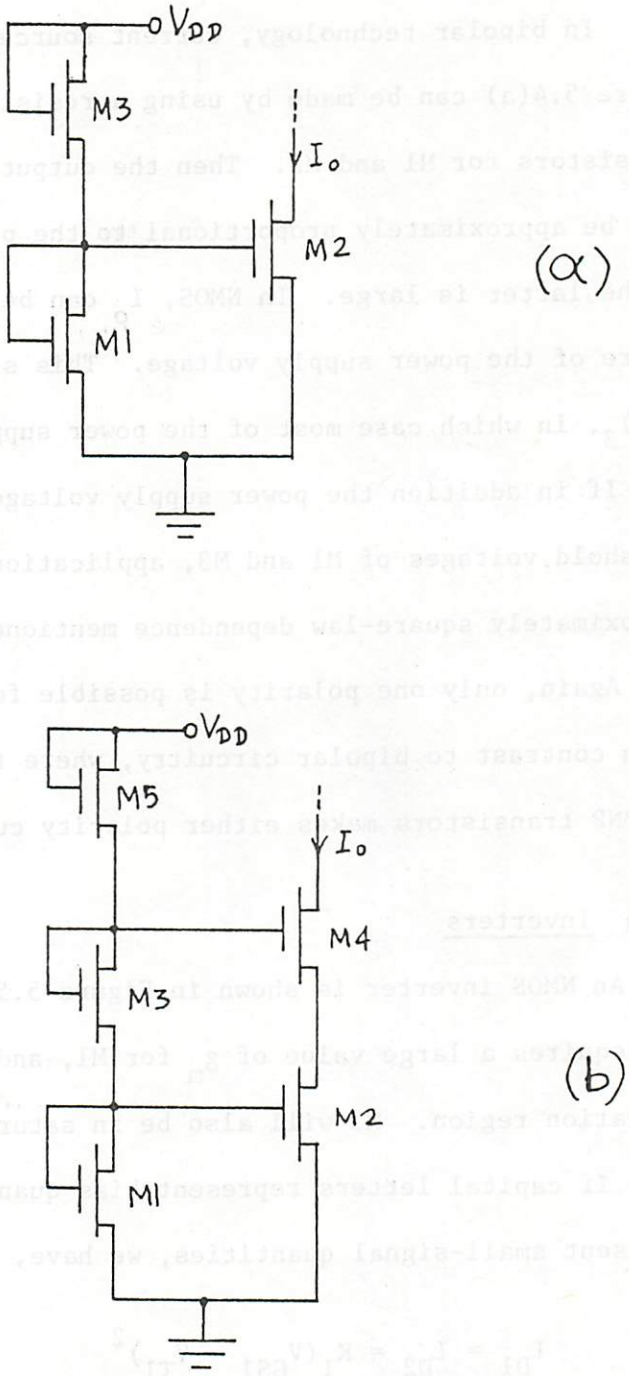


Figure 5.4: Current sources.

voltage, as long as the latter does not force the devices out of the saturation region, but they are very dependent on the power supply voltage. In bipolar technology, current sources corresponding to that in Figure 5.4(a) can be made by using a resistor in place of M3, and bipolar transistors for M1 and M2. Then the output current of the circuit, I_o, will be approximately proportional to the power supply voltage, as long as the latter is large. In NMOS, I_o can be at best proportional to the square of the power supply voltage. This situation results when $(Z/L)_1 >> (Z/L)_3$, in which case most of the power supply voltage is droped across M3. If in addition the power supply voltage is much higher than the threshold voltages of M1 and M3, application of equation (5.4) gives the approximately square-law dependence mentioned.

Again, only one polarity is possible for these current sources. This is in contrast to bipolar circuitry, where the availability of both NPN and PNP transistors makes either polarity current sources possible.

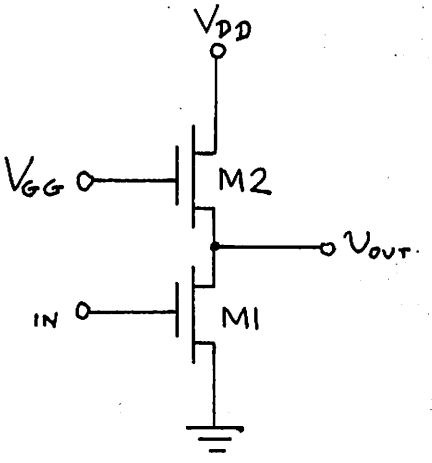
5.4.6 Inverters

An NMOS inverter is shown in Figure 5.5(a). For amplifying purposes one requires a large value of g_m for M1, and so M1 must be biased in the saturation region. M2 will also be in saturation as long as $V_{DD} > V_{GS} - V_{T2}$. If capital letters represent bias quantities and small-case letters represent small-signal quantities, we have, from equations 5.4 and 5.4(a):

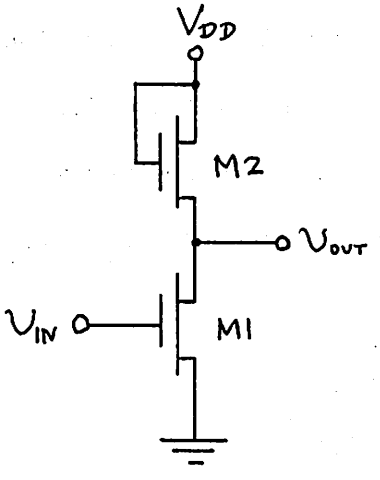
$$I_{D1} = I_{D2} = K_1(V_{GS1} - V_{T1})^2 \tag{5.11}$$

$$V_{GS2} = \sqrt{\frac{I_{D2}}{K_2}} + V_{T2} = \sqrt{\frac{K_1}{K_2}}\,(V_{GS1} - V_{T1}) + V_{T2} \tag{5.12}$$

The equivalent small-signal resistance of M2 when looking into its source is $1/g_{m_2}$. Therefore, if v_{DS1} and v_{GS1} represent small signal



(a)



(b)

Figure 5.5: NMOS inverters.

quantities, the low frequency small signal gain will be:

$$G = \frac{v_{DS1}}{v_{GS1}} = -\frac{g_{m_1}}{g_{m_2}} \tag{5.13}$$

Using equations (5.6) and (5.2) this can be written as:

$$G = -\sqrt{\frac{(Z/L)_1}{(Z/L)_2}} \tag{5.14}$$

And, from equations (5.14) and (5.4):

$$G = -\frac{V_{GS2} - V_{T2}}{V_{GS1} - V_{T1}} \tag{5.15}$$

or:

$$G = -\frac{V_{GG} - V_{DS1} - V_{T2}}{V_{GS1} - V_{T1}} \tag{5.16}$$

Assume now that the quiescent current of the inverter has been set (e.g., from power consumption considerations). We will attempt to maximize the gain of the stage for this given current. From (5.16) it can be seen that if V_{DS1} is varied, $|G|$ becomes maximum for the minimum possible value of V_{DS1}, which is equal to $V_{GS1} - V_{T1}$ if M1 is to remain in saturation. The value of G in this case is obtained from equation (5.16):

$$G = -\left[\frac{V_{GG} - V_{T2}}{V_{GS1} - V_{T1}} - 1\right] \tag{5.17}$$

Assuming that V_{DD} is the highest power supply voltage available, $|G|$ will be highest when $V_{GG} = V_{DD}$, as shown in Figure 5.5(b). For that case, (5.15) becomes:

$$G = -\left[\frac{V_{DD} - V_{T2}}{V_{GS1} - V_{T1}} - 1\right] \tag{5.18}$$

From this equation can be seen that for large $|G|$ a value of V_{GS1} close

to V_{T1} is needed. In that case however, equation (5.4) requires a large size for M1, if a reasonable quiescent current is to be maintained. Also, the closest V_{GS1} is brought to V_{T1}, the tighter the control on V_{GS1} necessary to maintain a constant quiescent current will be. There is therefore a limit to how close V_{GS1} can be brought to V_{T1}.

The maximum gain that can be obtained from an inverter will sometimes be limited by the minimum V_{GS1} possible, as explained, and sometimes by the maximum ratio of $(Z/L)_1$ to $(Z/L)_2$. If this ratio is very large, as required by equation (5.14) for high gain, not only will the total size become excessive, but the parasitic capacitances as well. Generally, gains higher than 15 or 20 are not practical for an NMOS inverter.

In the above, the conditions for maximum gain have been discussed. Another interesting subject is the minimization of the total area of the inverter when the gain desired is specified. In Appendix D, the values of the (Z/L)'s for minimum area are derived for a simple geometry inverter:

$$\left(\frac{Z}{L}\right)_1 = 0.75G \tag{5.19}$$

$$\left(\frac{Z}{L}\right)_2 = \frac{0.75}{|G|} \tag{5.20}$$

where G is the desired gain.

Choosing the Z's and L's so that the area is minimized is not always practical. For example, for a desired gain of 5, $(Z/L)_2$ must be 0.16 from equation (5.20). For a typical process, a power supply voltage of 25 volts and V_{GS} = 3v this will result in a quiescent current of the order of 0.5 mA. If this is an intolerable current drain, different Z's and L's must be used, resulting in a larger area.

The frequency response of the inverter will now be considered. The important capacitances are shown in Figure 5.6, where C_L is a load capaci-

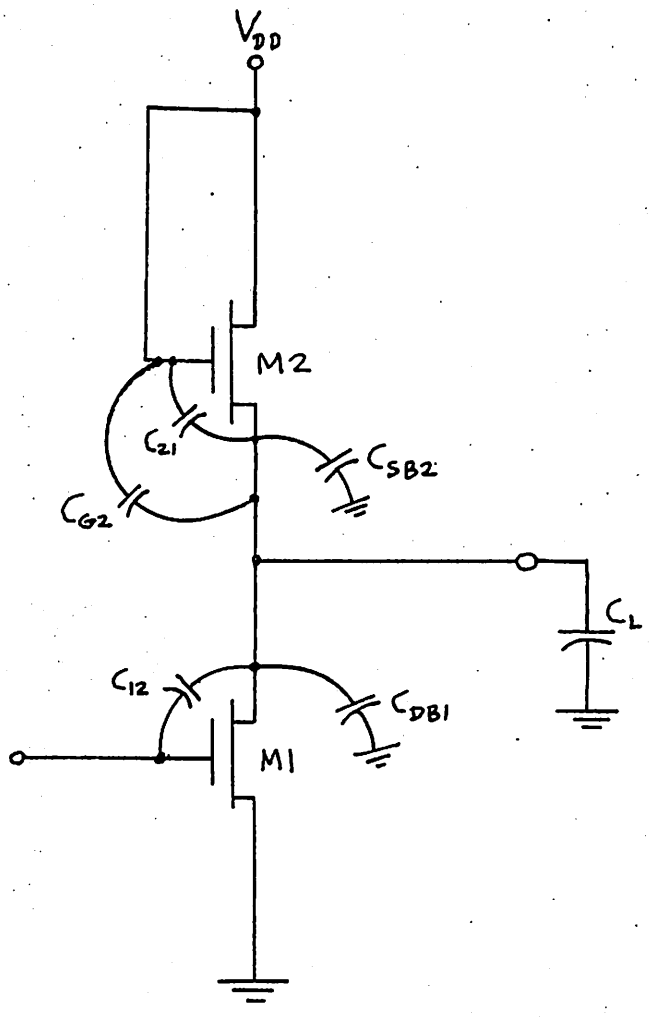


Figure 5.6: Important capacitances in an MOS inverter.

tance, and the other capacitances have been defined in section 5.3. An example for the estimation of these capacitances is given in Appendix E.

As long as the gain is sufficiently larger than unity and the stage is voltage fed, the total capacitance at the output of the inverter is given by:

$$C_{tot} \simeq C_{12} + C_{21} + C_{DB1} + C_{SB2} + C_{G2} + C_L \tag{5.21}$$

Assuming a very high small-signal output resistance for the devices, the small-signal resistance between the output of the inverter and ground is:

$$r_2 = \frac{1}{g_{m_2}} \tag{5.22}$$

From equation (5.16) it is seen that for high gain, V_{GS1} must be small. Assume that V_{GS1} has been set, and that $V_{T1} \simeq 0$, so that we can make $V_{DS1} \simeq V_{GS1}$. Then $V_{GS2} = V_{DD} - V_{GS1}$. From equations (5.22) and (5.6b) then, we get:

$$r_2 = \frac{V_{DD} - V_{GS1} - V_{T2}}{2I} \tag{5.23}$$

and a first estimate of the -3db point of the frequency response can be made from (5.21) and (5.23). However, the capacitances in (5.21) depend on the (Z/L)'s and therefore on the current desired in the stage. We will investigate the case where small power consumption is desired. For a given current I, $(Z/L)_2$ can be found from equation (5.4):

$$\left(\frac{Z}{L}\right)_2 = \frac{I}{K'(V_{GS2} - V_{T2})^2} = \frac{I}{K'(V_{DD} - V_{GS1} - V_{T2})^2} \tag{5.24}$$

From this equation is seen that for the large power supply voltages that have to be used for high gain, and for K' of the order of 5 to 10

$\mu A/v^2$, $(Z/L)_2$ will invariably be less than one. For that case, if d is the minimum dimension used, it can be seen from Figure D.1 in Appendix D that C_{G2} will be given by:

$$C_{G2} = Z_2 L_2 C_o = \frac{d^2}{(Z/L)_2} C_o \tag{5.25}$$

and using equation (5.24), this becomes:

$$C_{G2} = \frac{d^2 C_o K'(V_{DD} - V_{GS1} - V_{T2})^2}{I} \tag{5.26}$$

For a practical circuit with $K' = 6\ \mu A/v^2$, d = 0.5 mil and a power supply voltage of 30 volts (or $\pm$ 15 volts), the above expression reduces to:

$$C_{G2} \simeq \frac{100}{I} \tag{5.27}$$

where I is in μA and C_{G2} in pF. For small I, this capacitance will dominate the other terms in equation (5.21), and therefore, from equations (5.23) and (5.26), the -3db point of the frequency response is given by:

$$f_{-3db} \simeq \frac{1}{2\pi r_2 C_{G2}} \tag{5.27a}$$

or:

$$f_{-3db} = \frac{I^2}{\pi K' d^2 C_o (V_{DD} - V_{GS1} - V_{T2})^3} \tag{5.27b}$$

From this equation it can be seen that the frequency response tends to be very poor for low currents. For example, for the conditions stated above and for I = 10 μA, f_{-3db} is 15 KHz. Since the gain does not depend on the current once V_{DD} and V_{GS1} have been set (see equation 5.16), it is seen that the gain-bandwidth product also deteriorates for low currents.

This is one reason that high quiescent currents are necessary in MOS analog circuits. A method for increasing the gain-bandwidth product will be outlined in the following subsection.

5.4.7 Split Load Inverters

The reason that the frequency response of a simple inverter is so poor for low currents, is that for high gain most of the power supply voltage must be droped across the load device, as seen from equation (5.16). For small I, this means that M2 in Figure 5.6 must be a very long device, which results in large gate area and therefore large C_{G2}. This problem can be reduced if M2 is split to more than one devices in series, as shown in Figures 5.7(b) and (c).

To see this, we will compare the gain and frequency response for the inverters of Figures 5.7(a) and 5.7(b), assuming the same V_{GS1}, V_{DS1}, V_{DD} and the same small I for both circuits. The simple inverter in (a) has already been analyzed in section 5.4.6 and we have:

$$r_2 = \frac{1}{g_{m_2}} = \frac{V_{GS2} - V_{T2}}{2I} \tag{5.28}$$

$$C_{G2} = \frac{d^2 C_o K' (V_{GS2} - V_{T2})^2}{I} \tag{5.29}$$

The small-signal equivalent of the simple inverter is shown in Figure 5.7(a).

Consider now the case for which $(Z/L)_3 = (Z/L)_4$ in Figure 5.7(b). Since M3 and M4 carry the same current, equation (5.4) gives:

$$V_{GS3} - V_{T3} = V_{GS4} - V_{T4} \tag{5.30}$$

As long as $(Z/L)_3$ and $(Z/L)_4$ are significantly less than one, C_{G3} and

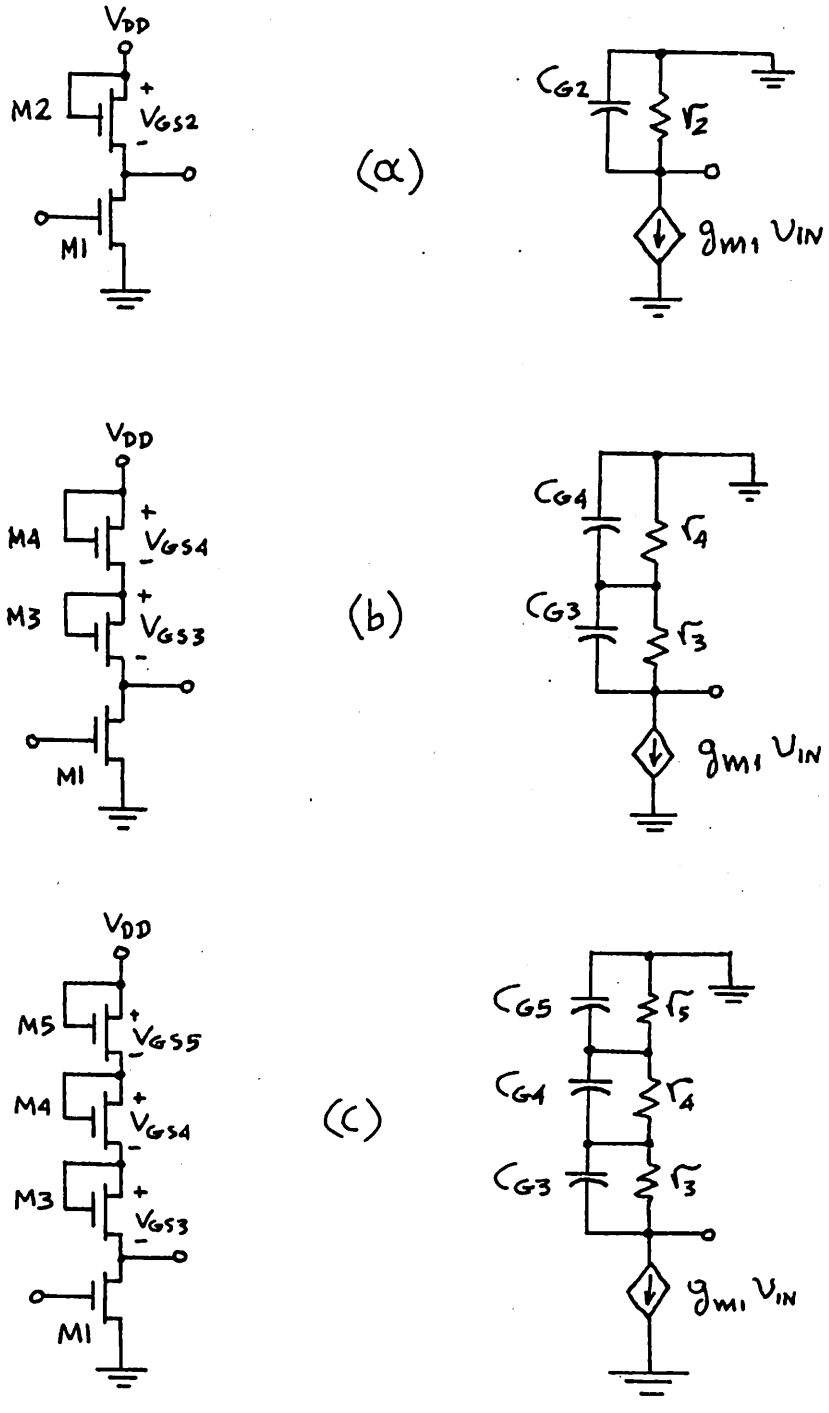


Figure 5.7: (a) Simple inverter.
(b), (c) Split load inverters.

C_{G4} will dominate the other capacitances. The resistances and capacitances for the small-signal equivalent shown in Figure 5.7(b) will be given by equations similar to (5.28) and (5.29). Taking (5.30) into account, we have:

$$r_3 = r_4 = \frac{V_{GS3} - V_{T3}}{2I} \tag{5.31}$$

$$C_{G3} = C_{G4} = \frac{d^2 C_o K' (V_{GS3} - V_{T3})^2}{I} \tag{5.32}$$

In order to compare the two circuits, we want to express these quantities in terms of r_2 and C_{G2}. To this end, define a ratio α as follows:

$$\alpha \triangleq \frac{V_{GS3} - V_{T3}}{V_{GS2} - V_{T2}} \tag{5.33}$$

Using this definition and equations (5.28), (5.29), (5.31) and (5.32) we get:

$$r_3 = r_4 = \alpha r_2 \tag{5.34}$$

$$C_{G3} = C_{G4} = \alpha^2 C_{G2} \tag{5.35}$$

Using these values for the small-signal equivalent in Figure 5.7(b), the gain G(s) of the split-load inverter is easily obtained:

$$G(s) = \frac{-2g_m \alpha r_2}{1 + s\alpha^3 r_2 C_{G2}} \tag{5.36}$$

The low frequency gain therefore, is:

$$G = -2\alpha g_m r_2 \tag{5.37}$$

And the -3db frequency is at:

$$f_{-3db} = \frac{1}{\alpha^3 r_2 C_{G2}} \tag{5.38}$$

In order to compare this performance to the simple inverter, an estimate of α for practical circuits is needed. To this end, note that in Figures 5.7(a) and (b), $V_{GS2} = V_{GS3} + V_{GS4}$. This fact and equations (5.30) and (5.33) give:

$$\alpha = \frac{1}{2}\left[1 - \frac{V_{T4}}{V_{GS2} - V_{T2}}\right] \tag{5.39}$$

Unless the body effect is really pronounced, V_{T2} and V_{T4} are much less than V_{GS2}, and α is close to 0.5. In that case, it can be seen from equation (5.37) that the low-frequency gain is the same as for the simple inverter. However, comparison of equations (5.27a) and (5.38) shows that the bandwidth of the split-load inverter is eight times higher.

Higher improvement is possible if three devices are used in the split load. However, for more than two or three devices the above analysis will not hold, since as the number of load devices is increased, their Z/L ratios also increase towards unity, if the current is to remain the same. Therefore the gate-to-channel capacitances are decreased, and they do not dominate the other capacitances, which was a basic assumption in the above calculations. Furthermore, for more than three devices, the parameter α, which can be defined in a similar manner as above, will be small, making the total load resistance also small, thus reducing the low-frequency gain.

5.4.8 Cascode Stages

In the analysis done in the previous two sections, it has been assumed that the total capacitance C_L seen as a load at the output of the inverters

was small. This can be the case, for example, if the output is connected to the input of a source follower. However, if the following stage is another gain stage, the Miller effect [43] comes into play. This is shown in Figure 5.8(a). C_2 is the gate-to-drain overlap capacitance of M3. If the output resistance of the second stage is low, and its gain is denoted by $-G_2$, the equivalent capacitance seen by the first stage is approximately equal to $(1 + G_2)\ C_2$. For a gain of 10 and a Z/L of 10 for M3, this can be as high as 2 pF. This will make the frequency response worse than that calculated in the two previous sections.

To reduce the Miller effect, a cascode stage can be used, as shown in Figure 5.8(b). To a first order approximation, the gains between the input and points A and B will be:

$$\frac{V_A}{V_{IN}} = -\frac{g_{m3}}{g_{m4}} = -\sqrt{\frac{(Z/L)_3}{(Z/L)_4}} \tag{5.40}$$

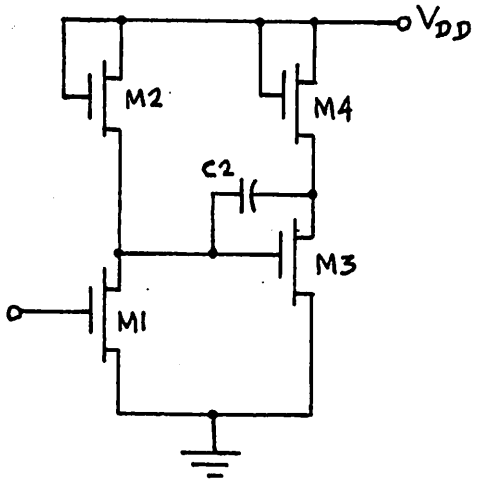
$$\frac{V_B}{V_{IN}} = -\frac{g_{m3}}{g_{m5}} = -\sqrt{\frac{(Z/L)_3}{(Z/L)_5}} \tag{5.41}$$

Therefore, the equivalent capacitance seen at the input of the stage will be:

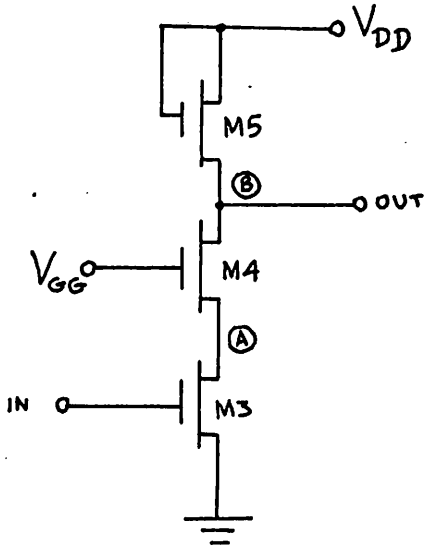
$$C_{eq} \simeq C_2\left(1 + \frac{g_{m3}}{g_{m4}}\right) \tag{5.42}$$

In order for this to be small, one must choose a large g_{m4} and therefore a large $(Z/L)_4$. This cannot be carried too far, since then the large capacitances associated with M4 will start playing a significant role. In practice, choosing $(Z/L)_4 \simeq (Z/L)_3$ gives satisfactory results.

For high gain, V_{GS3} and V_{DS3} are small, and for large $(Z/L)_4$ one also



(a)



(b)

Figure 5.8: (a) A cascade of simple inverters.
(b) A cascode stage.

can have small V_{GS4} and V_{DS4}. This allows for a large voltage drop across M5, which results in a high gain as seen from equation (5.16). In that case, and as long as the Z/L ratios of M3 and M4 are not excessively large, the dominant pole of the cascode is due to $r_5 = 1/g_{m5}$ and C_{G5}, and therefore a behavior similar to that of a simple inverter can be expected. The stage's real advantage is that it does not load the previous stage severely as would be the case for a simple inverter.

5.4.9 Differential Stages

A differential stage is shown in Figure 5.9. The low-frequency small-signal differential gain of this stage is seen to be:

$$\frac{V_{D1} - V_{D2}}{V_{G1} - V_{G2}} = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{(Z/L)_1}{(Z/L)_3}} \tag{5.43}$$

where of course we assume that $(Z/L)_1 = (Z/L)_2$ and $(Z/L)_3 = (Z/L)_4$. If r_{05} is the small signal output resistance of M5, the common mode gain when a common mode input voltage $V_{IN,CM}$ is applied is:

$$\frac{V_{D1}}{V_{IN,CM}} = \frac{V_{D2}}{V_{IN,CM}} = \frac{1}{2r_{o5}g_{m3}} \tag{5.43a}$$

For high common mode rejection, r_{o5} should be made high. To achieve this, a long channel can be used for M5, or the current source can be changed to the cascode current source shown in Figure 5.4(b).

If it is desired that the input be able to handle large common mode voltages, the design of the stage is severely restricted. The quiescent voltage drop across M3 and M4 must be small, since otherwise when there is a high common mode voltage at the input, V_{DS1} and V_{DS2} can be small enough to drive M1 and M2 out of saturation. The limited voltage drop

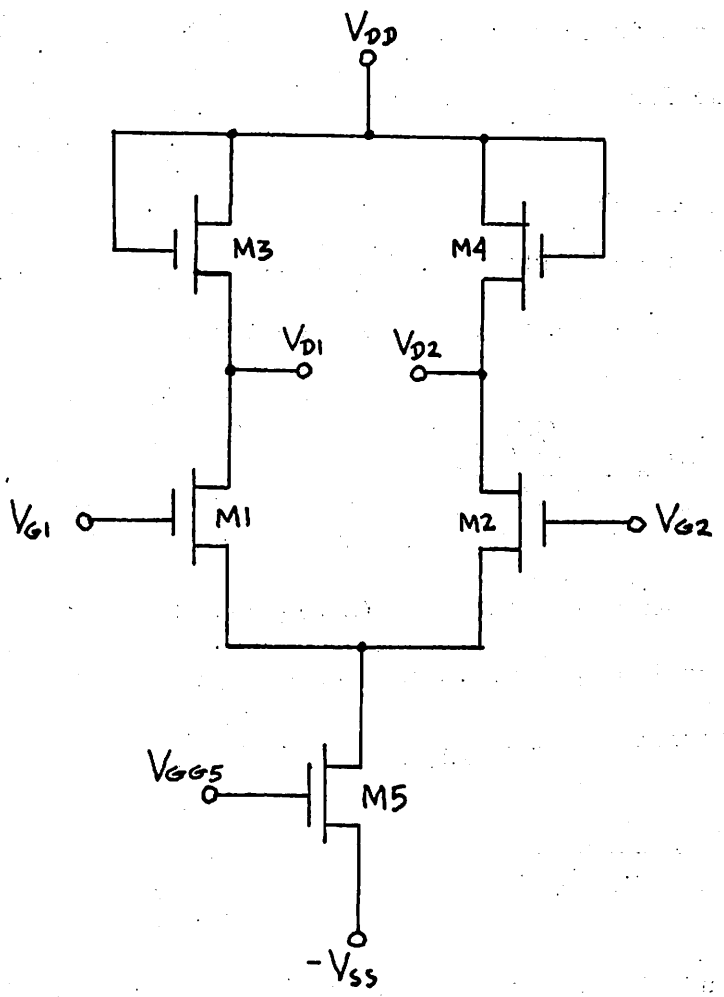


Figure 5.9: A differential stage.

allowed across M3 and M4 makes the gain of the stage small. Also, a cascode current source may have to be ruled out, since it requires a high voltage at its output, as seen in Figure 5.4(b). If the common mode input voltage of the differential stage is driven low, the voltage at the source of M1 and M2 can easily drive the output device of a cascode current source out of saturation.

A detailed investigation of the differential stage can be made by using the appropriate "half-circuits" [43]. These reduce its analysis to that of simple inverters, which have been discussed in the previous sections. The analysis therefore will not be undertaken here.

5.4.10 Source Followers

Two source followers are shown in Figure 5.10(a) and 5.10(b). Either case can be represented by the circuit of Figure 5.10(c), where g_2 represents the conductance of the bottom device in (a) or (b), and C_1 and C_2 represent the effect of capacitive parasitics and loading. For (c), it is easily shown that the gain G(s) is:

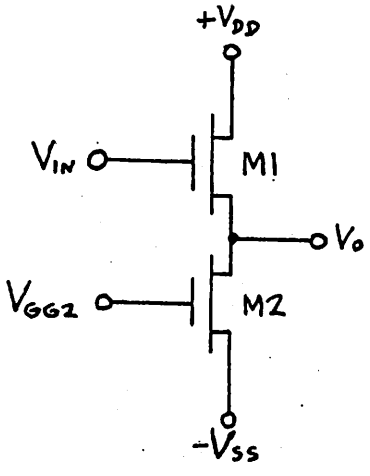
$$G(s) = \frac{v_o(s)}{v_i(s)} = \frac{g_{m1} + sC_1}{(g_{m1} + g_2) + s(C_1 + C_2)} \tag{5.44}$$

From this, the low frequency gain is:

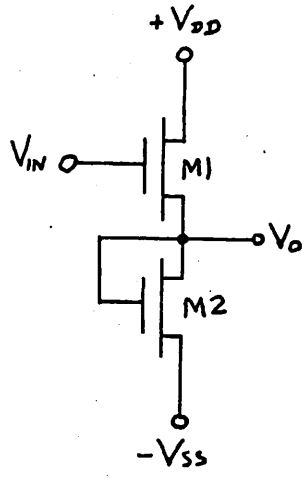
$$G = \frac{g_{m1}}{g_{m1} + g_2} \tag{5.45}$$

From G(s) in equation (5.44) it can be seen that the stage can be made extremely broadband when the zero of G(s) cancels its pole. This happens for:

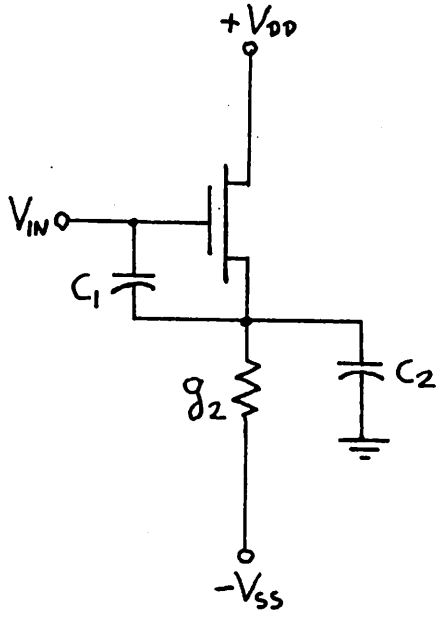
$$\frac{g_{m1}}{g_2} = \frac{C_1}{C_2} \tag{5.46}$$



(a)



(b)



(c)

Figure 5.10: (a), (b) Source followers.
(c) Equivalent circuit for (a) and (b).

Consider now the circuit in Figure 5.10(a). There, $g_2 = 1/r_{o2}$, which is usually very small, and from (5.45) it is seen that the low-frequency gain is close to unity. For pole-zero cancellation, (5.46) requires that C_2 also be small. This rules out large widths for M2, and therefore a small value for $(Z/L)_2$ is to be prefered.

The circuit of Figure 5.10(b) can be used in conjunction with current mirrors, as will be seen in section 5.4.11. For this circuit, $g_2 = g_{m2}$.

5.4.11 Output Stages

The configurations that can be used as output stages in NMOS suffer from both the lack of availability of complementary devices, and the large gate-to-source voltage drops required. Some possible output stages are shown in Figure 5.11.

In (a), a source follower is used as an output stage. The output resistance of this stage is approximately $1/g_{m1}$, which can be low if $(Z/L)_1$ and the quiescent current are large. The disadvantage of this stage is that in the case of capacitive loads between output and ground, the charging rate towards negative values is limited by the constant current of M2, which must therefore be large for fast response. Another disadvantage is that the stage must be driven from a previous stage which will invariably have a device, say M3, between V_{DD} and the gate of M1. Therefore the maximum V_{OUT} possible will be $V_{DD} - V_{T3} - V_{T1}$, and this can be quite low because of the body effect.

The circuit in (b) is not of much use, since for positive-going outputs a large amount of current will be wasted in M2.

The circuit in (c) is improved relative to those in (a) and (b), since it combines the advantages of a source follower and an inverter. Negative going output pulses have a smaller rise time than in (a). However, again

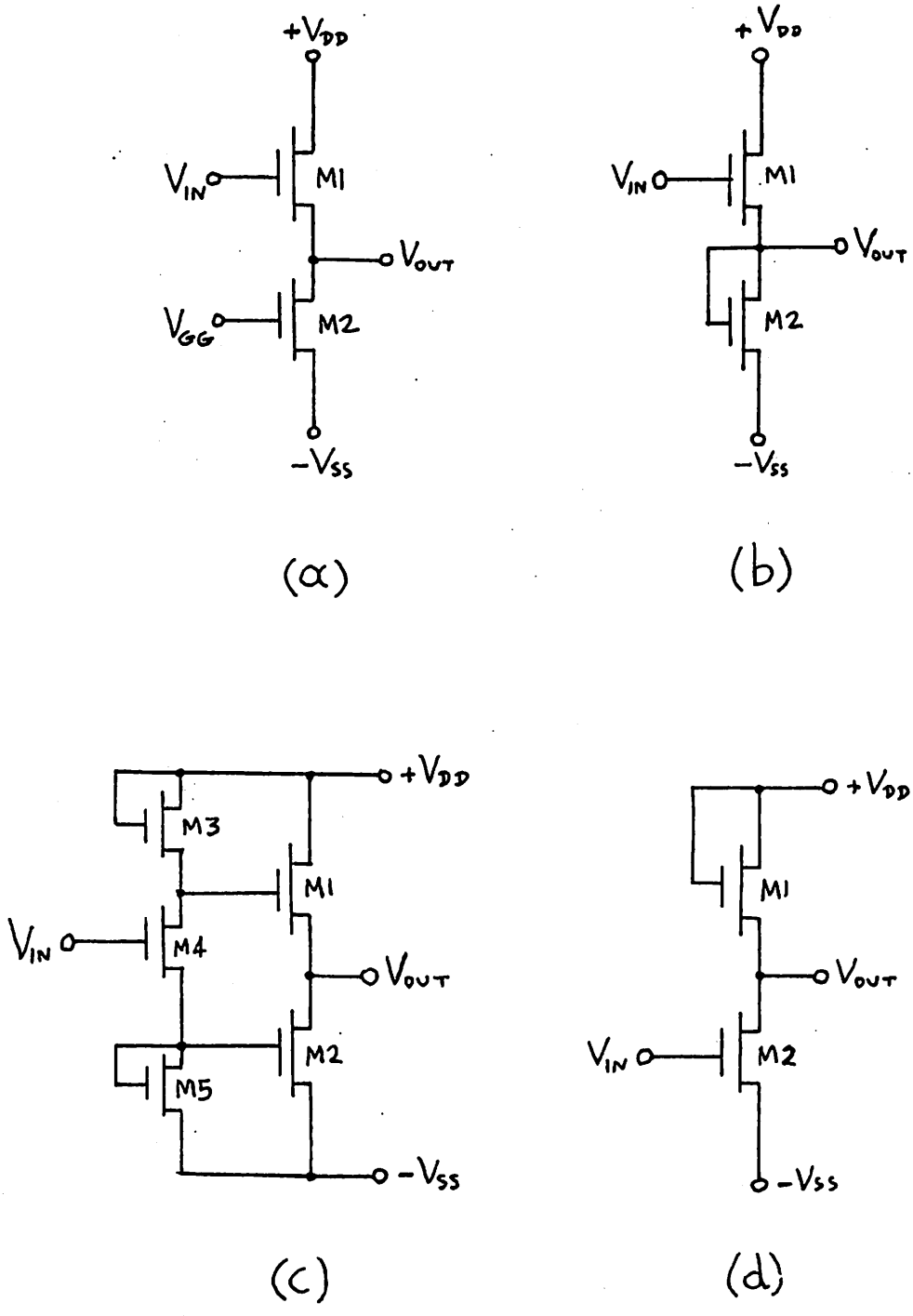


Figure 5.11: Output stages.

V_{OUT} is limited to values below $V_{DD} - V_{T3} - V_{T1}$, which is a serious drawback.

To obtain a larger output swing, one is led to the simple inverter, shown in (d). V_{OUT} can in this case swing up to $V_{DD} - V_{T1}$. However, for a capacitive load the charging time is limited by M1. Let us assume that V_{IN} goes low, so that M2 is off and the load capacitance C_L is charged through M1. An upper bound on the time t_c required to take V_{OUT} from an initial value V_{OI} to a final value V_{OF} is found easily if one assumes that during the charging process the threshold of M1 is fixed and equal to its worst-case value V_{TF}, which occurs for $V_{OUT} = V_{OF}$. This value can easily be calculated if the body effect coefficient is known. We have:

$$C_L \frac{dV_{OUT}}{dt} = K' \left(\frac{Z}{L}\right)_1 \left[V_{DD} - V_{OUT}(t) - V_{TF}\right]^2 \tag{5.47}$$

Integrating this equation gives:

$$\frac{t_c}{C_L} = \frac{V_{OF} - V_{OI}}{K'\left(\frac{Z}{1}\right)_1 (V_{DD} - V_{OF} - V_{TF})(V_{DD} - V_{OI} - V_{TF})} \tag{5.48}$$

Assume that $V_{DD} = 15$ volts, $V_{OI} = 0$ volts, $V_{OF} = 5$ volts, $K' = 7.9$ $\mu A/v^2$, and $V_{TF} = 5$ volts. Then this equation reduces to:

$$\frac{t_c}{C_L} = \frac{0.015}{(Z/L)_1} \quad \frac{\mu sec}{pF} \tag{5.49}$$

If we want to charge a capacitance of 70 pF in 1 μsec, the above equation gives $(Z/L)_1 \simeq 1$, which from equation (5.4) means that the quiescent current of the output stage must be about 1 mA, with the body effect taken into account.

Even for this large quiescent current, the output resistance of this

stage, which is approximately $1/g_{m1}$, will have a value of 6 KΩ. This output resistance, in conjunction with the 70 pF capacitive load, gives a pole corresponding to 379 KHz. This poor frequency response makes internal frequency compensation virtually impossible.

Consider now the same output stage fed from another inverter, as shown in Figure 5.12(a). To decrease the output resistance of this stage, we can use negative feedback. This can be done by connecting the gate of M3 to the output rather than V_{DD}. This modification is shown in Figure 5.12(b). A straight-forward low frequency small signal analysis of this circuit gives the following results:

$$\frac{v_o}{v_i} = \frac{g_{m4}}{g_{m3}} \times \frac{g_{m2}/g_{m1}}{1 + g_{m2}/g_{m1}} \tag{5.50}$$

$$= \sqrt{\frac{(Z/L)_4}{(Z/L)_3}} \times \frac{\sqrt{\frac{(Z/L)_2}{(Z/L)_1}}}{1 + \sqrt{\frac{(Z/L)_2}{(Z/L)_1}}} \tag{5.50a}$$

$$\frac{v_A}{v_i} = - \frac{g_{m4}}{g_{m3}} \times \frac{1}{1 + g_{m2}/g_{m1}} \tag{5.51}$$

$$= - \sqrt{\frac{(Z/L)_4}{(Z/L)_3}} \times \frac{1}{1 + \sqrt{\frac{(Z/L)_2}{(Z/L)_1}}} \tag{5.51a}$$

$$r_{OUT} = \frac{1}{g_{m1} + g_{m2}} \tag{5.52}$$

If the loop gain g_{m2}/g_{m1} is high, it is seen that the overall gain v_o/v_i is approximately equal to the gain of the inverter M3-M4, which is g_{m4}/g_{m3}. The output resistance is reduced by a factor cf $(g_{m2}/g_{m1}) + 1$.

The transfer function G(s) of this stage will now be investigated.

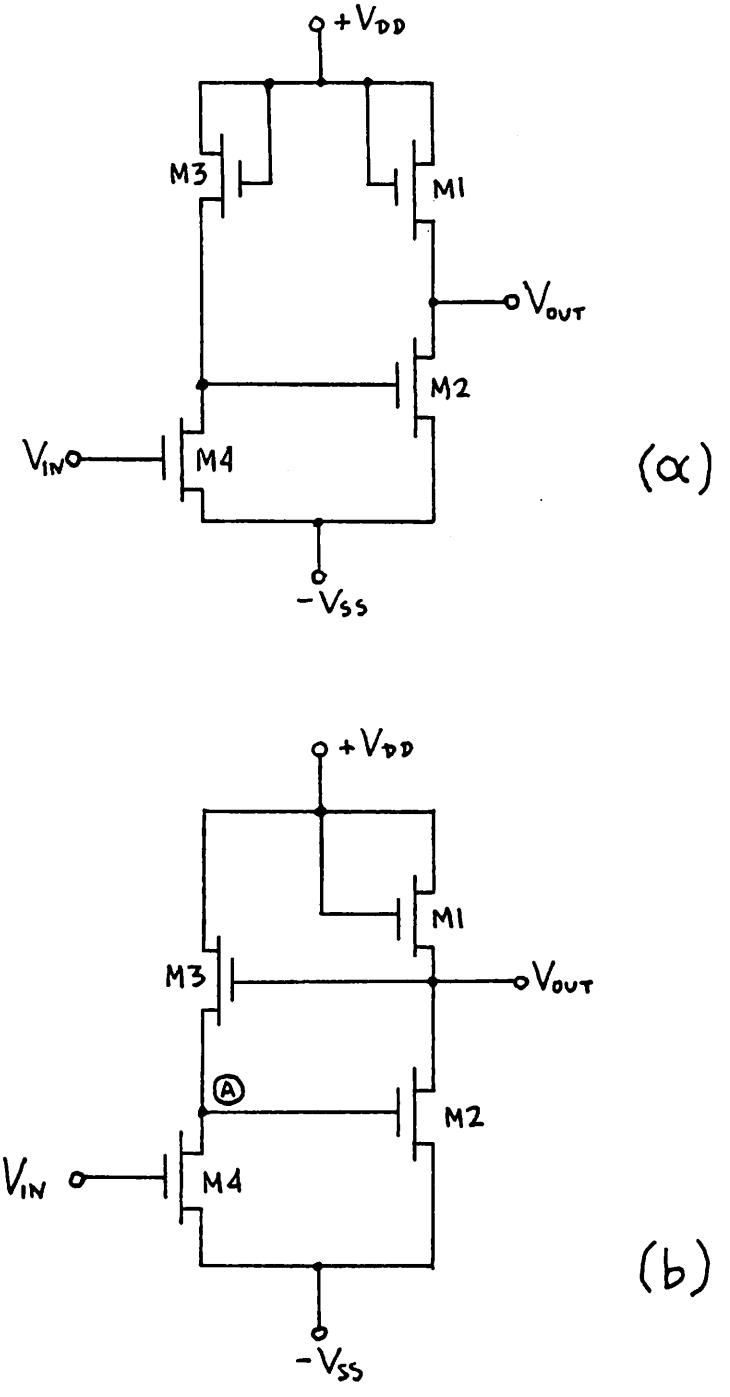


Figure 5.12: (a) Two cascaded inverters.
(b) The circuit in (a) modified to apply negative feedback.

The capacitances involved are shown in Figure 5.13(a). For clarity, the symbol C_{ov} has been used for the gate overlap capacitances. The small-signal equivalent circuit is shown in (b). By comparing (b) with (a), it is seen that the capacitances C_A, C_B AND C_C appearing in (b) are given by:

$$C_A = C_{ov2} + C_{G2} + C_{SB3} + C_{DB4} \tag{5.53}$$

$$C_B = C_{ov2} + C_{ov3} + C_{G3} \tag{5.54}$$

$$C_C = C_{ov1} + C_{G1} + C_{SB1} + C_{DB2} + C_{ov3} \tag{5.55}$$

Analysing the circuit in (b), we get:

$$G(s) = \frac{v_o(s)}{v_i(s)} = \frac{(g_{m2} - sC_B)(g_{m4} - sC_{ov4})}{\Delta(s)} \tag{5.56}$$

The network determinant $\Delta(s)$ is a second degree polynomial:

$$\Delta(s) = as^2 + bs + d \tag{5.57}$$

where:

$$a = (c_a = c_b = c_{ov4})(C_B + C_C + C_L) - C_B^2 \tag{5.58}$$

$$b = g_{m1}(C_A + C_B + C_{ov4}) + g_{m2}C_B + g_{m3}(C_L + C_C) \tag{5.59}$$

$$d = g_{m3}(g_{m1} + g_{m2}) \tag{5.60}$$

From equations (5.53) through (5.60) it is obvious that a reasonable hand analysis is not possible. Not only are the equations quite involved, but there are no clear approximations that can be made, since to investigate this circuit many combinations of quiescent current, device sizes, load capacitance etc. must be analyzed, and different parameters dominate over

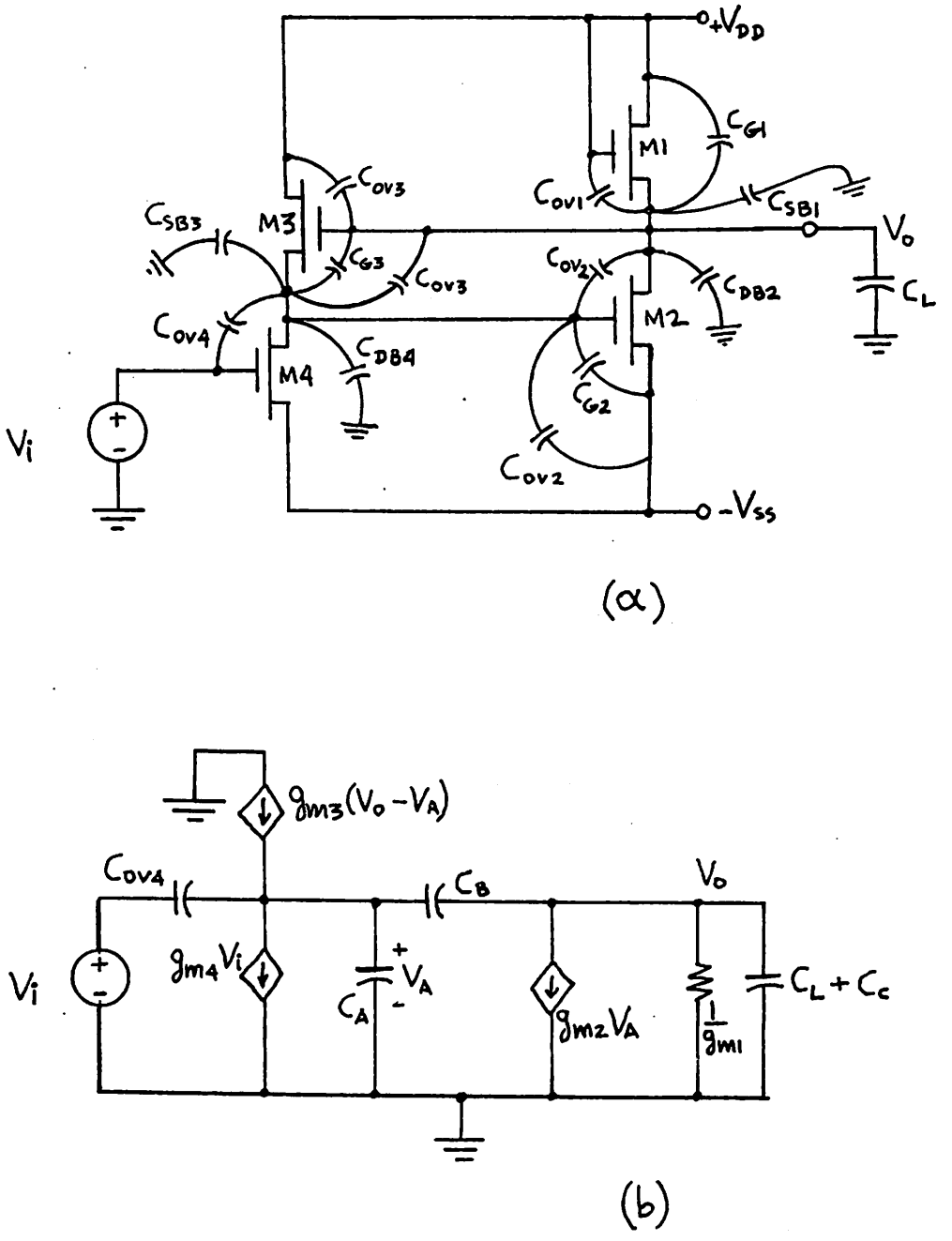


Figure 5.13: (a) Parasitic and load capacitances in the shunt-shunt feedback stage.
(b) Small-signal equivalent circuit.

the others in each case. Computer analysis is the only plausible solution here, and will be used in Chapter 6, where a further investigation of this circuit is made, and numerical values for a satisfactory output stage of this configuration are given.

5.4.12 Differential-to-Single-Ended Converters

A differential-to-single-ended converter, fed from the output of a differential pair, serves two purposes: First, it will greatly reject all common mode signals, thus improving the common mode rejection ratio (CMRR). Second, it will develop across its output a voltage which is close to the full output voltage of the differential stage, so that there is no gain reduction, as there would be if only one terminal of the differential stage output was fed directly to a following single-ended stage. This is important in MOS, where high gain stages are not feasible.

A configuration that can be used to perform the conversion is shown in Figure 5.14. There are two paths leading to the output of the stage: One, through the source follower M3-M4, is offered to v_B, and is noninverting. The other is offered to v_A and is inverting: a fraction of v_A is applied to the gate of M4, through the source follower M1-M2. This is then amplified by M4, with M3 acting as its load. The sum of the two voltages occuring due to these two paths appears at the output. Calculating the low frequency gain of each path separately, and then using superposition, we get:

$$v_{OUT} = \frac{g_{m3}r_{o4}}{1 + g_{m3}r_{o4}} \left\{ v_B - \left[\frac{g_{m1}g_{m4}}{g_{m3}(g_{m1} + g_{m2})} \right] v_A \right\} \qquad (5.61)$$

If one defines a differential input voltage $v_d \triangleq v_A - v_B$ and a common mode input voltage $v_C \triangleq (v_A + v_B)/2$, the low-frequency differential gain

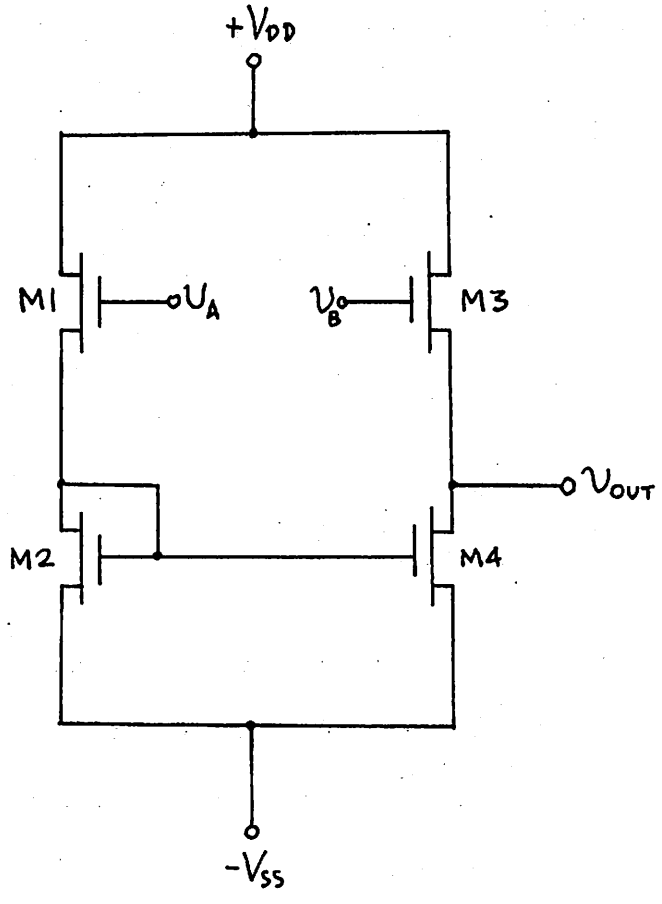


Figure 5.14: Differential-to-single-ended converter.

G_d and the low-frequency common-mode gain G_c can be derived from equation (5.6) and are as follows:

$$G_d = \frac{U_{OUT}}{U_d} = \frac{g_{m3}r_{o4}}{2(1 + g_{m3}r_{o4})}\left[1 + \frac{g_{m1}g_{m4}}{g_{m3}(g_{m1} + g_{m3})}\right] \tag{5.62}$$

$$G_c = \frac{U_{OUT}}{U_c} = \frac{g_{m3}r_{o4}}{1 + g_{m3}r_{o4}}\left[1 - \frac{g_{m1}g_{m4}}{g_{m3}(g_{m1} + g_{m2})}\right] \tag{5.63}$$

For a high common mode rejection, we want $G_c = 0$, which is achieved for:

$$\frac{g_{m1}g_{m4}}{g_{m3}(g_{m1} + g_{m2})} = 1 \tag{5.64}$$

Symmetry is very desirable in this circuit for reasons of DC voltage tracking, as will be discussed in section 5.5. We must therefore have $g_{m3} = g_{m1}$ and $g_{m4} = g_{m2}$, in which case equation (5.60b) can be satisfied only approximately, for:

$$g_{m2} >> gm_1 \tag{5.65}$$

$$g_{m4} >> gm_3 \tag{5.66}$$

Finally, simplified expressions can be obtained for G_d and G_c in terms of the Z/L ratios of the devices, using equation (5.6a). Assuming $r_{o4} >> 1/g_{m3}$, we get:

$$G_d \simeq \frac{1}{2}\left\{1 + \frac{\sqrt{(Z/L)_1(Z/L)_4}}{\sqrt{(Z/L)_3}\left[\sqrt{(Z/L)_1} + \sqrt{(Z/L)_2}\right]}\right\} \tag{5.67}$$

$$G_c \simeq 1 - \frac{\sqrt{(Z/L)_1(Z/L)_4}}{\sqrt{(Z/L)_3}\left[\sqrt{(Z/L)_1} + \sqrt{(Z/L)_2}\right]} \tag{5.68}$$

5.4.13 Frequency Compensation

In operational amplifier circuits, frequency compensation is usually used so that the circuits are stable when operated as unity gain amplifiers. This can be done by introducing a dominant pole at a frequency low enough to ensure a roll-off of 20 db per decade in the open loop frequency response, down to the unity gain frequency. In bipolar circuits, this is usually done by connecting a capacitor between the output and input of an inverting stage, to take advantage of the Miller effect, as shown in Figure 5.15(a).

Unfortunately, this configuration is not suitable for MOS circuits. To show this, we consider the case shown in Figure 5.15(a), where the inverting stage can be either a bipolar or an MOS circuit. The small-signal equivalent is shown in (b), where R_1 and C_1 represent the total resistance and capacitance at the input node, R_2 and C_2 the corresponding quantities at the output node, and $I_s(s)$ the excitation due to the previous stage. The node equations for this circuit are as follows:

$$\begin{bmatrix} G_1 + s(C_1 + C_c) & -sC_c \\ g_m - sC_c & G_2 + s(C_2 + C_c) \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} I_s(s) \\ 0 \end{bmatrix} \tag{5.69}$$

The overall transresistance of the stage can be obtained from these equations, and is:

$$\frac{V_2(s)}{I_s(s)} = \frac{g_m - sC_c}{\Delta(s)} \tag{5.70}$$

where:

$$\Delta(s) = (C_1C_c + C_2C_c + C_1C_2)s^2 +$$

$$+ \frac{C_1 + C_c}{R_2} + \frac{C_2 + C_c}{R_1} + g_m\, s +$$

$$+ \frac{1}{R_1R_2} \qquad (5.71)$$

The denominator gives the two poles of the transresistance, and it is known [44] that the spacing of these poles increases for increasing C_c, resulting in the well known "pole-splitting" effect. The frequency corresponding to the dominant pole is:

$$\omega_p \simeq \frac{1}{g_m R_1 R_2 C_c} \qquad (5.72)$$

However, as seen from equation (5.70), there is also a right-half plane zero, corresponding to a frequency ω_z given by:

$$\omega_z = \frac{g_m}{C_c} \qquad (5.73)$$

In bipolar circuits, the value of g_m is very large, and the zero corresponds to a frequency much higher than the unity gain frequency of the compensated circuit. The zero can therefore be neglected there, and the frequency response of the compensated amplifier is as shown in Figure 5.15(c). In MOS, however, the small values of g_m that can be obtained result in a small ω_z. The resulting frequency response of the amplifier is easily shown to be of the form shown in Figure 5.15(d), with the zero decreasing the phase by 90°, while at the same time preventing the magnitude from rolling off at the initial rate of 20 db per decade, and therefore the phase exceeds 180° before the magnitude becomes 1, rendering the circuit unstable when connected in a unity gain configuration.

In order to cope with this undesirable situation, the right-half-plane zero must be eliminated. To this end, consider the origin of the zero.

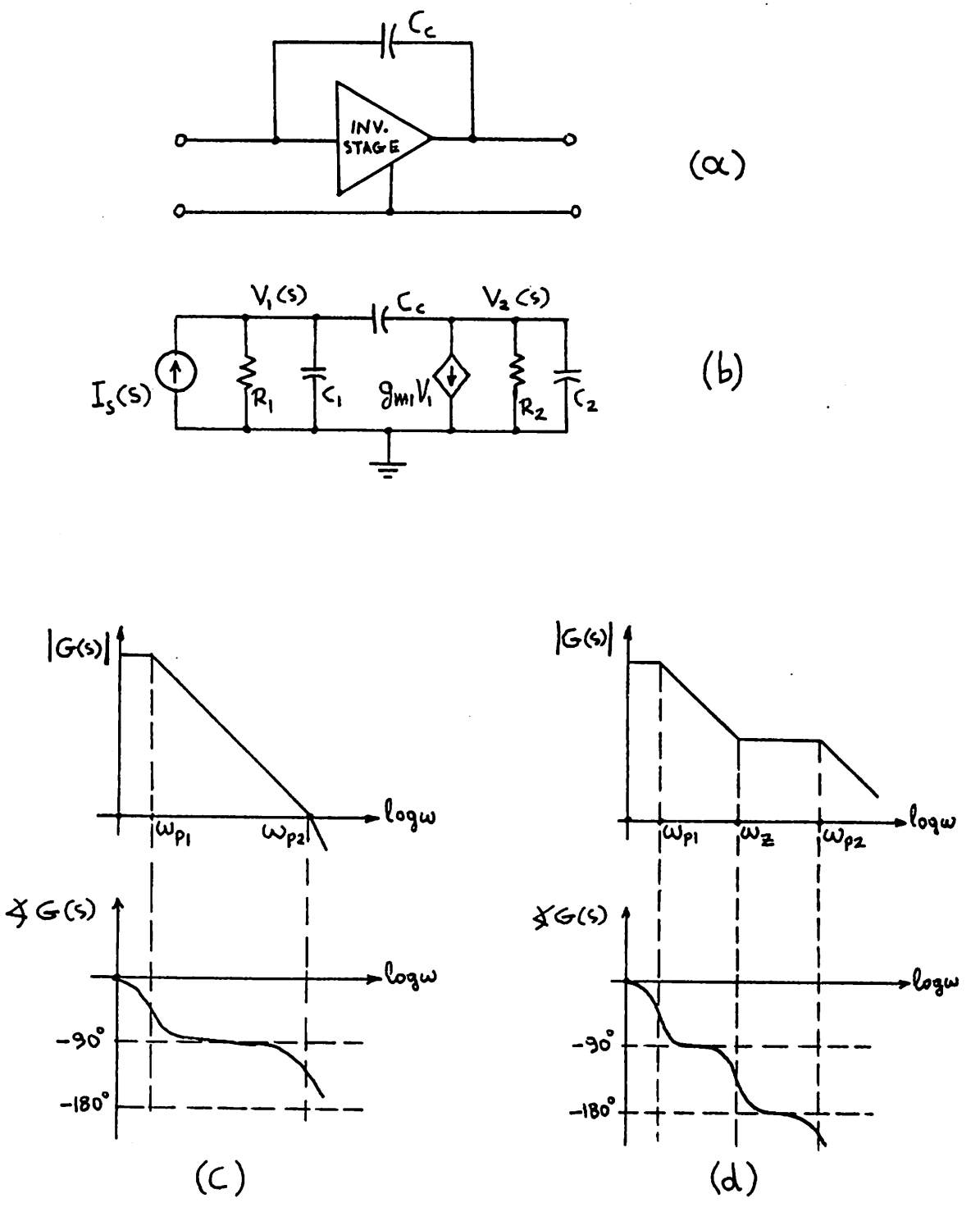


Figure 5.15: (a) An inverting stage with Miller compensation.
(b) Small signal equivalent circuit.
(c) Frequency response of complete amplifier for g_m large.
(d) Frequency response of complete amplifier for g_m small.

In the matrix equation (5.69), it occurs because of the term $g_m - sC_c$ in the second row and first column. However, this term represents the action of node 1 on node 2, part of which is the result of the direct connection of C_c between the two nodes. Physically, this action of node 1 on node 2 through C_c is the so-called "feedforward". It can easily be eliminated by isolating node 1 from node 2 through a unity gain buffer, as shown in Figure 5.16(a). The buffer allows feedback, neccessary for the Miller effect, but prevents feedforward. The small signal circuit corresponding to this situation is shown in Figure 5.16(b), from which one obtains:

$$\begin{bmatrix} G_1 + s(C_1 + C_c) & -sC_c \\ g_m & G_2 + sC_2 \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} I_s(s) \\ 0 \end{bmatrix} \tag{5.74}$$

The transresistance obtained from this equation is:

$$\frac{V_2(s)}{I_s(s)} = \frac{g_m}{\hat{\Delta}(s)} \tag{5.75}$$

where $\hat{\Delta}(s)$ is the determinant of the node admittance matrix of equation (5.74). It is seen from (5.75) that the right-half plane zero has indeed been eliminated. The dominant pole is again given by (5.72).

In practice, it has been found that a source follower performs the function of the unity gain buffer shown in Figure 5.16(a) satisfactorily.

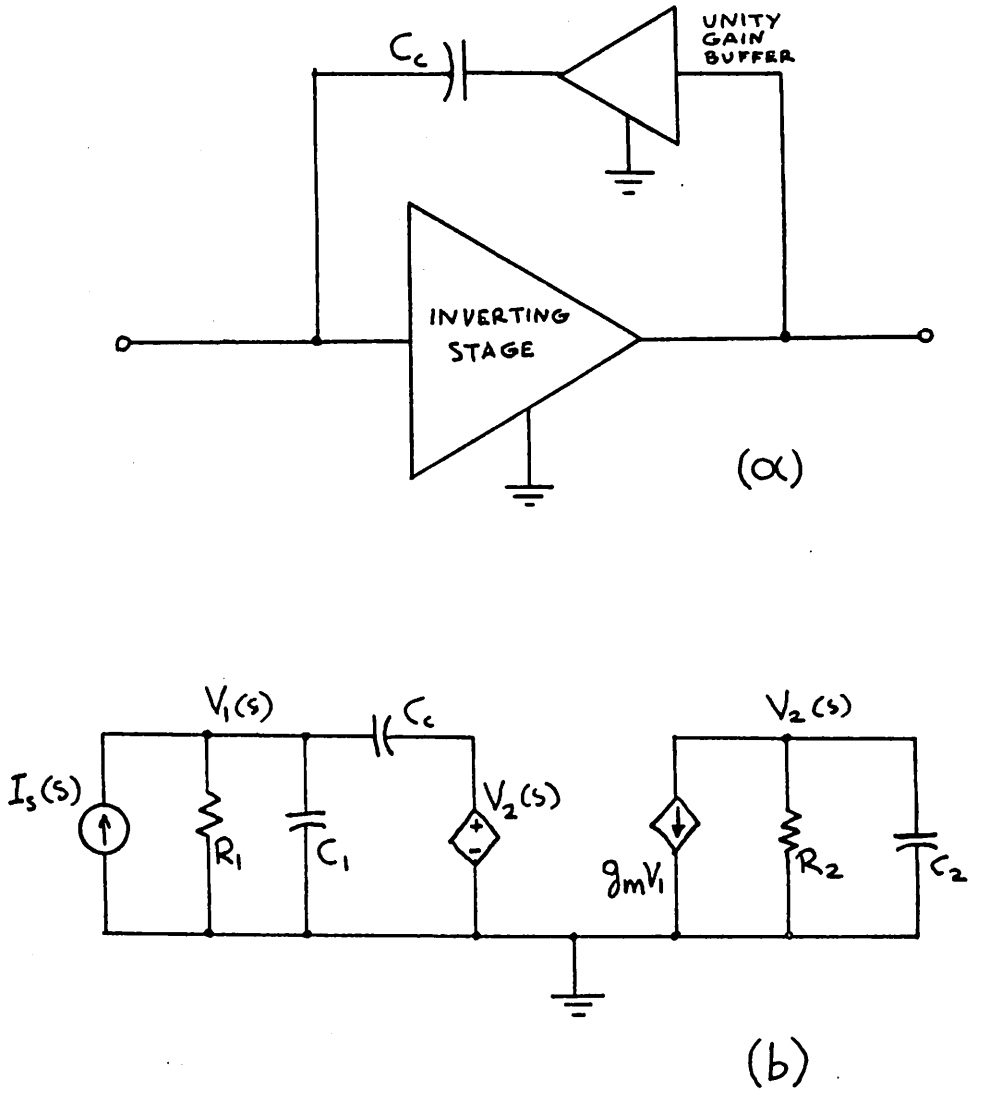


Figure 5.16: (a) Preventing feedforward by using a buffer in the feedback path.
(b) Small signal equivalent.

CHAPTER 6

AN INTERNALLY COMPENSATED NMOS OPERATIONAL AMPLIFIER

6.1 INTRODUCTION

The design, fabrication and evaluation of an N-channel MOS (NMOS) internally compensated operational amplifier has been undertaken as part of this research effort. Although the amplifier came about because of the need for a unity gain buffer in the PCM encoder described in Chapter 4, it can find several applications outside the PCM area, like in A/D and D/A converters, and Charge-Coupled Device (CCD) and Bucket-Brigade circuits.

6.2 OBJECTIVES

The requirements for the unity gain buffer required in the PCM encoder described in Chapter 4 were determined using computer simulation, and as discussed in section 4.5.10 are quite relaxed. Stricter requirements were set as objectives in designing the op amp, so that the circuit could find additional use in more demanding applications. The objectives were set as follows:

a) The open loop gain should be at least 300.

b) The output range should be at least $\pm$ 5 volts.

c) The amplifier should be internally compensated.

d) When the op amp is connected as a unity gain buffer, the 1% settling time should be no more than 2 μsec with a 5 volts input step and a load of 70 pF.

e) The input offset voltage should be less than 100 mV.

f) The design should be tolerant to process parameters. In particular, the performance should not depend critically on the value of the

threshold voltage of the transistors, as the latter is not well predictable.

It was decided that these objectives should be met without using exceedingly high power supply voltages and power consumption. However, for the several reasons discussed in Chapter 5 it was expected that both of these parameters would have to be considerably higher than those for a corresponding bipolar circuit.

6.3 CIRCUIT DESIGN

6.3.1 Overview

Since the stages of the op amp are interdependent to a large extent, the circuit of the complete op amp will be presented first. The individual stages will then be examined as parts of the whole, in the light of the background developed in Chapter 5.

The complete schematic of the op amp is shown in Figure 6.1. The input consists of the differential stage M7, M10, M6 and M9, biased by the current source. The reason that three transistors are used rather than two will be discussed below. The differential signal at the drains of M7 and M10 is converted to a single-ended signal through M4, M5, M11 and M12, and appears at the drain of M12. This signal is subsequently fed to the cascode stage M20, M19, M18. It is then level-shifted by the source follower M21, which is biased by the current source M22. The voltage divider M15, M16, M17 is used to bias M22. After level shifting, the signal is fed to a shunt-shunt feedback output stage, which consists of M23, M24, M25 and M26. Transistor M13 along with current source M17 form a buffer which is part of the frequency compansation scheme described in section 5.4.12.

In designing the amplifier, approximate hand calculations have been performed in the light of the discussion in section 5.4. The Z/L ratios

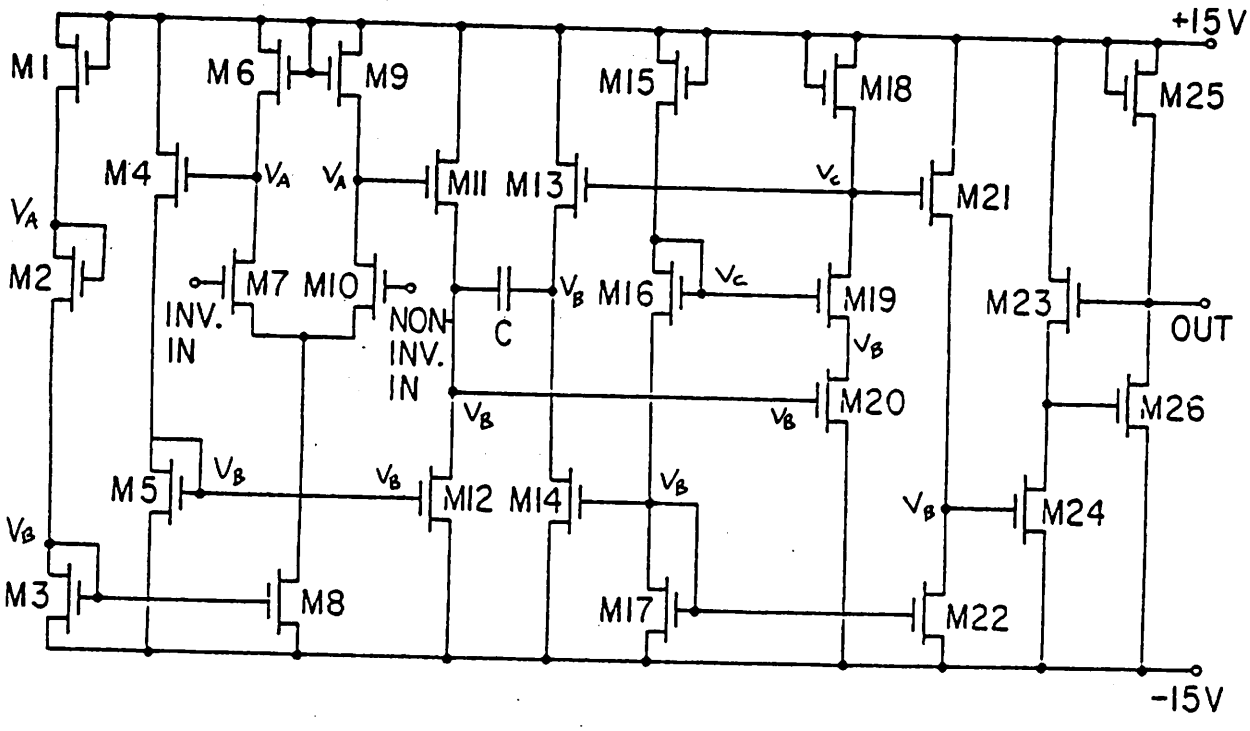


Figure 6.1: Schematic of the internally compensated NMOS operational amplifier.

obtained from these calculations were then used as a starting point, and computer simulation was used in order to refine the design. In most cases, the computer simulation results did not require a large change of the Z/L's obtained by hand calculations.

In the calculations included in the following discussion of the circuit design, the values for several quiescent currents will be needed. These values are taken from a DC analysis performed using computer simulation, which is discussed in section 6.5.2. A typical value for K' of 7 $\mu A/v^2$ is used in these calculations.

6.3.2 Quiescent Voltage Tracking

The circuit has been designed so that its operation is largely independent of the threshold voltage V_T, which is not very well predictable. If the design was based on a specific value of V_T, gross unbalances could occur when V_T would turn out to be different than the design value. Assume for example that the circuit is designed for a threshold voltage of 2 volts, in such a way that when the input differential voltage is zero, the output is also zero, which corresponds to an input offset voltage of 0 volts. If now the actual V_T obtained in processing turns out to be 1 volt, the output will in general assume a value different from zero. To bring the output back to zero, a change ΔV_{G24} of the voltage at the gate of M24 is needed, which can be achieved if the input voltage is changed by $\Delta V_{G24}/G$, where G is the gain between the input and the gate of M24. The equivalent input offset voltage is therefore $\Delta V_{G24}/G$, which will only be small if G is large. However, the fact that V_T turned out different than the design value can upset the quiescent conditions throughout the circuit, and it is possible that one or more devices among M1-M22 be driven out of the saturation region. In that case, G can have a very small value, and

the input offset voltage $\Delta V_{G24}/G$ can be quite large. To keep G large therefore, one must design the circuit so that the conditions for having M1 through M22 in the saturation region do not depend on V_T. This is done as described in the next paragraph, where for simplicity I represents I_D, and S represents the Z/L ratio.

First, note that symmetry is used in the differential pair, so that $S_7 = S_{10}$ and $S_6 = S_9$. The differential-to-single-ended converter is also symmetric, so that $S_4 = S_{11}$ and $S_5 = S_{12}$. We choose $S_8 = S_3$, so that $I_8 = I_3 = I_1$. Therefore a current equal to $I_1/2$ flows through M6, and if we choose $S_6 = S_1/2$, we have $V_{GS1} = V_{GS6}$, and, by symmetry, $V_{GS6} = V_{GS9}$. We therefore have $V_{GS2} + V_{GS3} = V_{GS4} + V_{GS5}$. If we now choose $S_4/S_5 = S_2/S_1$, we get $V_{GS4} = V_{GS2}$ and $V_{GS5} = V_{GS3}$. Since $V_{GS12} = V_{GS5}$, we have $I_{12} = I_5$ and $V_{GS11} = V_{GS4}$. Therefore $V_{DS12} = V_{DS5} = V_{GS12}$. We have therefore shown that for the Z/L ratios chosen $V_{DS12} = V_{GS12}$, and this was shown to be the case independently of the threshold voltage V_T. As long as $V_T > 0$, this guarantees that M12 will remain in the saturation region.

The two bias strings M1-M2-M3 and M15-M16-M17 have been designed so that $V_{GS17} = V_{GS3}$ for a typical value of V_T. Computer simulation shows that these two voltages remain nearly equal even if V_T changes, so we will assume that $V_{GS17} = V_{GS3}$ independently of V_T. We have chosen $S_{16}/S_{17} = S_{19}/S_{20}$, and since $V_{GS20} = V_{GS17}$, this guarantees that $V_{GS16} = V_{GS19}$. Therefore $V_{GS20} = V_{DS20}$, so that M20 is kept in the saturation region for any $V_T > 0$. In addition, we have $S_{15}/S_{16} = S_{18}/S_{19}$, and therefore $V_{GS18} = V_{GS15}$. This guarantees that $V_{DS19} = V_{GS19}$, so that M19 is also kept in the saturation region. Finally, $S_{21}/S_{22} = S_{16}/S_{17}$, and since $V_{GS21} + V_{GS22} = V_{GS16} + V_{GS17}$, we get $V_{GS21} = V_{GS19}$ and so $V_{DS22} = V_{GS22}$, keeping M22 in saturation. Similarly for M13 and M14.

The equality of the various voltages mentioned in the above discussion is indicated by the symbols V_A, V_B and V_C in Figure 6.1. Since all devices are kept in the saturation region independently of V_T, the gain G from the input to the gate of M24 remains high, and any DC unbalance, when reflected back to the input, corresponds to a small input offset voltage. In the design description that follows, the restrictions on the Z/L ratios discussed above have to be kept in mind.

6.3.3 Output Stage

The detailed discussion of the circuit design will be made starting from the output stage, which consists of M23, M24, M25, and M26. The operation and advantages of this stage have been discussed in section 5.4.11. As a starting point, it was decided that the rise time of the output when charging the maximum required load capacitance of 70 pF should be not more than 1 μsec, to allow for additional effects which would hopefully be such that the total settling time would be 2 μsec or less, as required. The Z/L ratio needed for M25 to achieve this, has been calculated in section 5.4.11 and is equal to 1.

The Z/L ratios of M23, M24 and M26 had now to be specified. M26 should be large enough to allow for fast charging of the capacitive load when the output swings negative. Also, the element values should be such that the two poles of the stage (see section 5.4.11) have values larger than the unity gain frequency of the compensated amplifier for the case of simple dominant pole compensation. In addition, these values should stay large for all capacitive loads of interest.

It was found that for some combinations of element values the position of the poles was very sensitive to the value of the capacitive load. In order to avoid such a situation as much as possible, the pole position had

to be determined for numerous combinations of the circuit element values, including Z/L ratios, quiescent current, and load capacitances. The combinations possible are so many that using circuit analysis programs such as SLIC would be laborious and extremely expensive. For this reason, a computer program was been written which simulates the performance of the stage, assuming the stage is fed by a voltage source. The data to the program are the process parameters, the power supply voltages, the overall gain required and the Z/L ratio of M25. The program then changes the Z/L ratio of M23 in specified steps, starting from a specified value, and for each value calculates the Z/L ratios of the other devices, performs a DC analysis, calculates the small-signal capacitances of the circuit taking into account geometry dependence and voltage dependence, and finally performs a small-signal analysis for each operating point, which results in a printout of the poles and zero of the gain G(s) for various values of load capacitance.

A large number of combinations of circuit parameters have been investigated using the program. It has been found that the zero of G(s) corresponds to a very high frequency and is practically independent of the load capacitance. The pole position however varies as the load capacitance is changed, and for some combinations of circuit parameters this variation is quite significant. An example is shown in Figure 6.2(a). The locus of the poles of G(s) has been plotted using the value of the load capacitance C_L as a parameter. The Z/L ratios for which this plot has been obtained are given in the figure captions. It can be seen from this plot that the frequency response of such a stage would depend heavily on the load capacitance C_L, and in fact it would be quite poor for large C_L. This would create problems in the frequency compensation of the circuit.

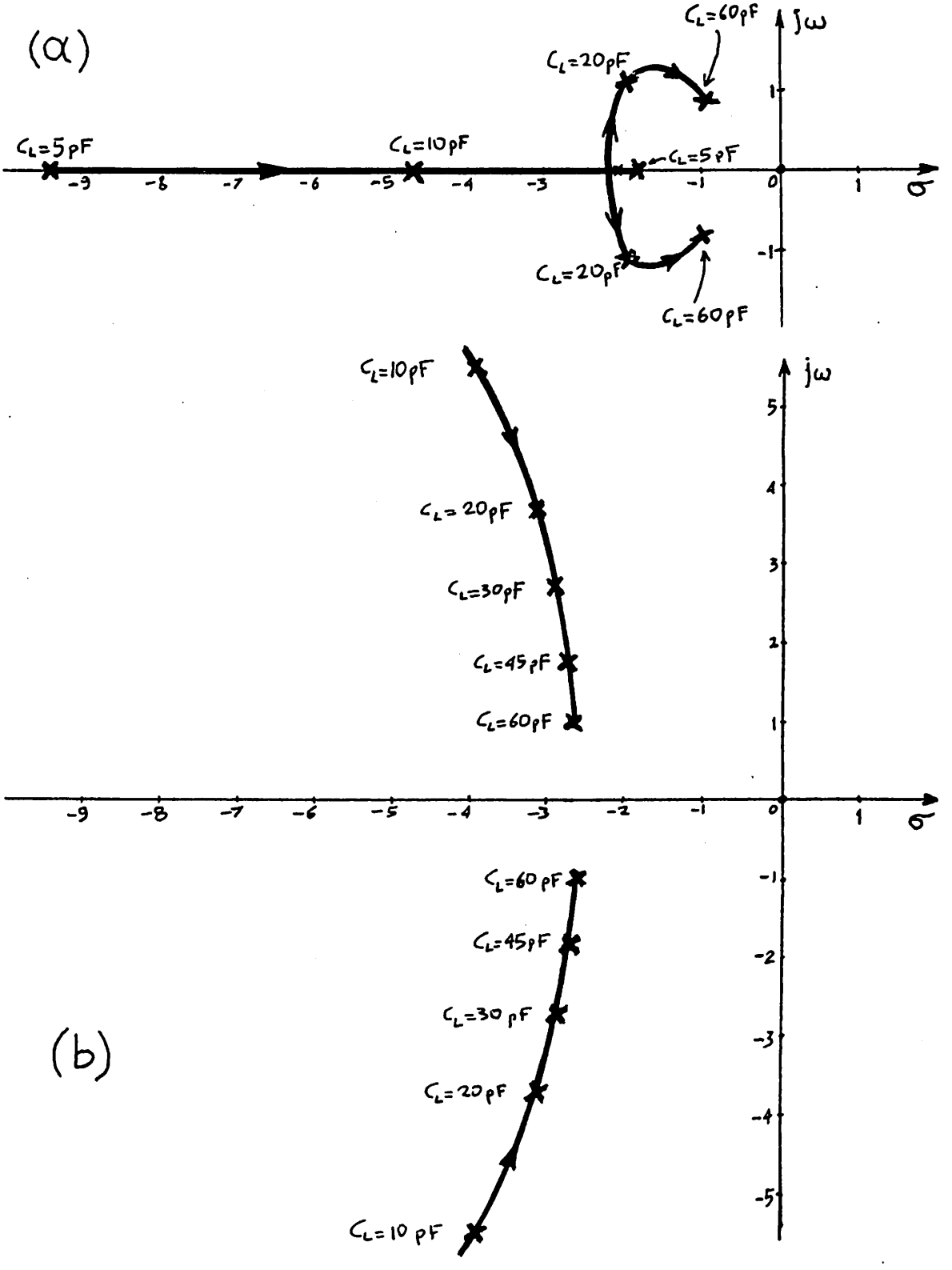


Figure 6.2: Poles of the shunt-shunt feedback output stage
(a) $(Z/L)_{23} = 0.1$, $(Z/L)_{24} = 10$, $(Z/L)_{25} = 1$, $(Z/L)_{26} = 40$
(b) $(Z/L)_{23} = 0.53$, $(Z/L)_{24} = 53$, $(Z/L)_{25} = 1$, $(Z/L)_{26} = 16$

Other combinations of circuit parameters give better results. An example is shown in Figure 6.2(b). The Z/L ratios for this case are mentioned in the figure caption, and the results shown are among the best obtained for the various combinations. Although the poles have a large imaginary part, the case in (b) was among the ones that created the less excess phase and gave the best transient response, so the final values for the Z/L ratios were picked very close to the ones for which this plot was obtained. However, even with those values it was found that the settling time goal could not be met for large capacitances connected directly across the output of the circuit. For this reason, the capacitive loads are charged through a series device, which is placed outside the feedback loop. This will be discussed in the section on experimental results.

6.3.4 Output Stage Driver

The design of the source follower feeding the output stage will now be described. The devices M21 and M22 forming the source follower were chosen equal for reasons of DC voltage tracking, as discussed above. Since the drain of M19, where the input to the source follower appears, is at a low DC voltage, the Z/L of M21 and M22 can be expected to be larger than 1 if a sufficient current through them is desired. The transfer function of the source follower is given by equation (5.44). Using the expressions for the various capacitances established in appendix E, it is easy to show that if C_{24} represents the capacitance offered by M24 to the output of the source follower, the capacitances C_1 and C_2 in Figure 5.10(c) will be approximately given by:

$$C_1 \simeq 0.032\left(\frac{Z}{L}\right)_{22} \tag{6.1}$$

$$C_2 \simeq C_{24} + 0.032\left(\frac{Z}{L}\right)_{22} \tag{6.2}$$

The output resistance of M22 is assumed infinite. Then, using equation (5.6a) for the transconductance of M21, as well as equations (6.1) and (6.2), it is easily shown that the pole of G(s) in equation (5.44) will correspond to a frequency ω_p as given below:

$$\omega_p \simeq \frac{4.86\sqrt{\left(\frac{Z}{L}\right)_{22} I}}{C_{24} + 0.064\left(\frac{Z}{L}\right)_{22}} \tag{6.3}$$

where I is the quiescent current of the source follower.

The pole given by (6.3) cannot be cancelled by the zero of the transfer function as suggested in subsection 5.4.10, since as follows from equations (6.1) and (6.2) we have $C_1 < C_2$ and therefore the required condition for cancellation, given by (5.46), cannot be satisfied. However, notice from equation (5.44) that the zero corresponds to a frequency which is sufficiently larger than that of the pole, and can be neglected. We can therefore limit our attention in maximizing ω_p. This can be done using equation (6.3). It is easily shown that ω_p is maximized when:

$$\left(\frac{Z}{L}\right)_{22} \simeq 16\ C_{24} \tag{6.4}$$

where C_{24} is in pF. The value of C_{24} can be calculated using the capacitances evaluated in Appendix E, and is approximately 2.8 pF, which, from equation (6.4), suggest Z/L ratios of 45 for M21 and M22. Unfortunately, the capacitances associated with devices of this size are large enough to create a low-frequency pole in conjunction with M18. This has not shown up in our calculations since the source follower was assumed voltage-fed. To increase the frequency of this undesired pole, the size of M21 and M22 had to be reduced, and a value of about 28 proved satisfactory.

6.3.5 Cascode Stage

For the cascode stage, consisting of M18, M9 and M20, a value of about 1 mA for the quiescent current proved to be a satisfactory compromise between the values needed for good frequency response and those for reasonable power consumption. This led to Z/L ratios of about 30 for M19 and M20, and about 0.3 for M18, which result in a gain of approximately 10 for this stage.

6.3.6 Differential-to-Single-Ended Converter

The differential-to-single-ended converter, consisting of M4, M5, M11 and M12, was designed according to equations (5.65) and (5.66). These constraints, coupled with the reasonably high currents required for good frequency response, resulted in Z/L ratios of 0.127 for M4 and M11, and 12 for M5 and M12.

6.3.7 Input Stage

The input differential pair M6, M9, M7, M10 was designed according to the discussion in section 5.4.9. The common mode input range required dictates that the voltage drop across M6 and M9 must be small. This voltage drop, combined with the high current required for good frequency response, resulted in a Z/L ratio of 2.2 for these devices. A value of 60 was chosen for M7 and M10, to make the gain of the stage about 5. Current source M8 was designed with a channel twice as long as the minimum required, to increase its small-signal output resistance. This results in improved CMRR for the input stage, as discussed in section 5.4.

6.3.8 Frequency Compensation

The frequency compensation of the circuit is achieved through a 40 pF capacitor C, which is connected between the input and the output of the

cascode stage through a source follower consisting of M13 and M14. The source follower is used in order to prevent feedforward, thus eliminating an undesirable right half-plane zero which would otherwise appear, as discussed in section 5.4.12. The Z/L ratio of M13 should be large enough in order to drive the compensation capacitor, but not so large as to present an excessive capacitance at the source of M18. A value of approximately 18 was eventually used, and M14 was made equal to M13 for reasons of DC voltage tracking, which was discussed earlier.

6.3.9 Biasing Dividers

The quiescent voltages and currents of the amplifier are set by two voltage dividers, one consisting of M1, M2, M3 and the other of M15, M16, M17. Choosing the Z/L ratios of these devices is of course not critical, and it involved a compromise between small current and small area.

6.3.10 Final Design

The approximate values for the Z/L ratios, obtained through hand calculations, were used as a starting point. Computer simulation was then used to evaluate the performance of the circuit. The circuit analysis program ISPICE was used, provided by the National CSS Company. The parameters used for the device models in this program are shown in appendix F. Using the program, and the insight provided by the approximate hand calculations as a guide, the circuit parameters were modified, in most cases not too significantly, in order to improve the overall performance. Table 6.1 shows the values of the drawn Z and L for each device, as well as the expected Z/L ratio after lateral diffusion is taken into account. The values in the table include a few small mask errors that were detected after the circuit was fabricated. Simulation shows that

TABLE 6.1

Device	Drawn Z(mil)	Drawn L(mil)	Z/L after lateral diffusion
M1	3.500	1.000	4.38
M2	0.500	10.500	0.0485
M3	3.500	1.000	4.38
M4	0.500	4.125	0.127
M5	3.725	0.500	12.46
M6	1.750	1.000	2.19
M7	18.000	0.500	60.20
M8	3.500	1.000	4.38
M9	1.750	1.000	2.19
M10	18.000	0.500	60.20
M11	0.500	4.125	0.127
M12	3.725	0.500	12.46
M13	5.500	0.500	19.23
M14	5.750	0.500	18.39
M15	0.500	8.175	0.063
M16	2.250	0.500	7.525
M17	2.250	0.500	7.525
M18	0.500	1.775	0.318
M19	8.750	0.500	29.26
M20	8.750	0.500	29.26
M21	8.500	0.500	28.43
M22	8.750	0.500	29.26
M23	0.750	1.500	0.577
M24	15.250	0.500	48.49
M25	1.500	1.675	1.017
M26	15.250	1.000	22.18

these errors should not have affected the circuit performance significantly. However, modeling inaccuracies in the simulation program have caused a significant input offset voltage. This is discussed in the section on experimental results.

6.4 APPROXIMATE CALCULATIONS

6.4.1 Gain of Individual Stages

We will now perform approximate calculations for the circuit of Figure 6.1, using the Z/L ratios given in Table 6.1. Let the subscript 1 refer to the input stage, 2 to the differential-to-single-ended converter, 3 to the cascode stage, and 4 to the shunt-shunt feedback output stage. Also, let the subscripts "dm" and "cm" stand for "differential mode" and "common mode" respectively. Assuming that the output resistances of the transistors are infinite, from equations (5.43), (5.67), (5.41) and (5.50a) we get:

$$G_{1,dm} = 5.2 \tag{6.5}$$

$$G_{2,dm} = 0.95 \tag{6.6}$$

$$G_{3} = 9.6 \tag{6.7}$$

$$G_{4} = 7.6 \tag{6.8}$$

Also, from equations (5.43a) and (5.68) we get:

$$G_{1,cm} = 0.0167 \tag{6.9}$$

$$G_{2,cm} = 0.09 \tag{6.10}$$

where $r_{o8} = 200\ K\Omega$ is assumed, a value obtained from measurements.

From equations (6.5)-(6.8), we get the differential gain of the com-

plete amplifier as follows:

$$G_{dm} = G_{1,dm}G_{2,dm}G_3G_4 = 360 \tag{6.11}$$

or:

$$G_{dm} = 51 \text{ db} \tag{6.12}$$

6.4.2 Common Mode Rejection Ratio

The Common Mode Rejection Ratio (CMRR) of the circuit will be discussed by considering its behavior between the input and the drain of M12, since the stages following M12 will amplify equaly signals of common mode or of differential origin. Two mechanisms that determine the CMRR will be considered.

Assume that a common mode voltage $U_{i,cm}$ is applied at the input of the amplifier. If no mismatches are present, the corresponding voltage at the drain of M12 will be given by:

$$U_{D12} = G_{1,cm}G_{2,cm}U_{i,cm} \tag{6.13}$$

However, if mismatches are present at the input stage, the common mode input voltage will also result in a differential voltage at the output of the first stage. If $G_{1,cm-dm}$ represents the common-mode-to-differential gain of the first stage, the corresponding voltage at the drain of M12 will include the contribution due to this second mechanism:

$$U_{D12} = \left[G_{1,cm}G_{2,cm} + G_{1,cm-dm}G_{2,dm}\right]U_{i,cm} \tag{6.14}$$

We will now discuss the relative importance of the terms in this equation. The first term of the sum inside the brackets is found from equations (6.9) and (6.10) as follows:

$$G_{1,cm}G_{2,cm} = 0.0015 \tag{6.15}$$

To estimate the magnitude of the second term, assume that a mismatch exists between the Z/L ratios of M6 and M9. This will result in a difference Δr between their small-signal resistances, and the common-mode-to-differential gain of the input stage is then easily seen to be:

$$G_{1,cm-dm} = \frac{\Delta r}{2r_{o8}} \tag{6.16}$$

For a 2% mismatch, this gain is calculated as 1.8×10^{-4} for typical process parameters, and therefore, using equation (6.6), the second term in the sum of equation (6.13) is:

$$G_{1,cm-dm}G_{2,dm} = 0.00017 \tag{6.17}$$

This is one order of magnitude smaller than the value given by equation (5.89) for the first term. Similarly, it can be found that the contribution of mismatches in other devices will also be small. We see therefore that the CMRR is not particularly sensitive to component mismatch, but is mainly determined by the common mode gains of the first two stages. Its value can be calculated from the above results:

$$CMRR \simeq \frac{G_{1,dm}G_{2,dm}}{G_{1,cm}G_{2,cm}} = 70.3 \text{ db} \tag{6.18}$$

6.4.3 Input Offset Voltage

The input offset voltage range expected in the amplifier is high compared to that of bipolar circuits. This can eventually be attributed to the poor transconductance of the MOS transistor.

The effect of Z/L ratio mismatches in M7 and M10 will be considered first. Assume that the inputs are grounded, let I be the average value of I_7 and I_{10}, and ΔI their difference. Also, let Z/L be the average value of $(Z/L)_7$ and $(Z/L)_{10}$, and $\Delta(Z/L) = (Z/L)_7 - (Z/L)_{10}$. Then, using equation

5.4, we get:

$$\frac{\Delta I}{I} = \frac{\Delta\left(\frac{Z}{L}\right)}{\left(\frac{Z}{L}\right)} \tag{6.19}$$

Assume now that a 2% mismatch exists between the Z/L ratios of M7 and M10, and an equal mismatch between those of M6 and M9. The differential output voltage of the first stage can be expressed by using equation (5.4a) as:

$$V_{GS6} - V_{GS9} = \sqrt{\frac{I_6}{K_6}} - \sqrt{\frac{I_9}{K_9}} \tag{6.20}$$

where the threshold voltages of M6 and M9 are assumed equal to a first order approximation. If we take the directions of the mismatches so as to give the worst case results, the differential output voltage of the first stage is found to be 46 mV using this equation. This, when refered back to the input by using (6.5), gives:

$$V_{in,os} = 9.2 \text{ mV} \tag{6.21}$$

There are additional sources of offset which contribute similar amounts to its value, like mismatches in the devices of the differential-to-single-ended converter. Although it is unlikely that all these sources of offset will add in the same direction, it is obvious that input offset voltages of tens of millivolts can be expected, unless the devices can be matched to better than 1%.

6.4.4 Unity Gain Bandwidth

A 40 pF capacitor has been used for compensation. At the source of M11, the small-signal resistance is $1/g_{m11}$ = 30 KΩ. The gain of the cascode

stage has been calculated in section 5.5.3 as 9.6, and therefore the frequency corresponding to the dominant pole is:

$$f_{-3db} = \frac{g_{m11}}{2\pi C_c G_3} = 13.8 \text{ KHz} \tag{6.22}$$

Using equation (6.11), the unity gain frequency is at:

$$f_{co} = G_{dm} f_{-3db} = 4.96 \text{ MHz} \tag{6.23}$$

6.4.5 Slew Rate

The slew rate can be calculated [41] as follows:

$$S_r = \frac{I_8}{C_c} \times G_4 = 18.4 \frac{V}{\mu sec} \tag{6.24}$$

6.5 COMPUTER SIMULATION

6.5.1 Modeling

The computer simulation was done using the circuit analysis program ISPICE, provided by National CSS, Inc. At the early stages of the design, the device model parameters were determined from experimental characteristics of devices that had previously been fabricated [28] using the intended process outlined in Appendix F. The characteristics were plots of I_D vs. V_{DS} with V_{GS} as a parameter, and were available for low to moderate values of V_{GS}. For this range of V_{GS}, the model parameters were picked so that the computer simulation device characteristics match the experimental ones.

After completing the design and fabrication, measurements were performed on the new devices for a large range of V_{GS}. It was found that although the devices behaved approximately as predicted for low V_{GS}, their drain currents for large V_{GS} were completely different, with discrepencies

of more than 50%. This created discrepencies between the actual amplifier performance and that predicted by computer simulation, the most important being that the input offset voltage had a mean of -65 mV, and that the total quiescent current of the amplifier was significantly higher than predicted.

In search of a better model, extensive measurements were performed on devices for large ranges of V_{GS}, and it was found that it was impossible to fit the model parameters so that the behavior of the devices be predicted over the whole range of V_{GS}'s used in the circuit. Instead, several different values for the parameter K should be used for the various transistors, depending on the value of V_{GS} of these transistors. The determination of these values of K was done by Burns [43] by matching the computer simulation device characteristics to the experimental ones, and the final models obtained are given in Appendix C.

The computer simulation results to be presented below were obtained by using the new model parameters, and they closely predict the experimental results presented in section 6.6. The computer simulation has been done for power supply voltages of $\pm$ 15 volts.

Since the threshold voltage obtained with our process is only 0.2 volts, in the experimental results to be discussed in section 6.6 a substrate bias of -5 volts with respect to V_{SS} has been used. This was done in order to approximate the situation one would encounter using a better process, in which case threshold voltages of 1 or 2 volts could be achieved without substrate bias. Although the substrate bias tends to reverse bias the junctions and reduce their capacitance, simulation has showed that the performance of the circuit is dominated by the gate-to-channel capacitances, and that the results obtained by using high threshold and no substrate bias

should not be worse than those using low threshold and substrate bias. For example, a comparison for the two cases is made in section 6.5.4 in terms of transient response. Comparisons like this have justified our use of substrate bias in the experimental measurements. In order to closely simulate these measurements, the substrate bias of -5 volts and the threshold voltage of 0.2 volts have also been used in the computer simulation.

6.5.2 DC Characteristics

The voltages and currents predicted by simulation are given in Table 6.2. It will be noted that the input differential stage is unbalanced, since the input offset had to be cancelled by an externally applied input voltage of -75 mV. The reason for this offset is given in section 6.5.1. The power supply current is 5.23 mA, which results in a power dissipation of 157 mW.

A DC transfer characteristic is shown in Figure 6.3.

6.5.3 Frequency Response

The simulated open loop gain magnitude and phase vs. frequency are given in Figures 6.4 and 6.5 for the uncompensated amplifier. The corresponding quantities when the amplifier is compensated with a 40 pF capacitor are given in Figures 6.6 and 6.7. It is seen from these last two figures that the unity gain frequency is at 11 MHz with a phase margin of 45°. The discrepancy between this value and the 5 MHz predicted by hand calculation in section 6.4.4 is that in that section a 20 db/decade roll off was assumed, whereas in Figure 6.6 there is peaking at high frequencies. If, in this figure, the 20 db/decade roll-off segment is extended to high frequencies, a unity gain frequency of 6 MHz is obtained, which is close to that predicted by hand calculation. The low frequency gain in Figure

Table 6.1

Device	V_{GS}(v)	V_{DS}(v)	V_{BS}(v)	I_D(μA)
M1	7.055	7.055	-22.945	94.53
M2	19.438	19.438	-3.506	94.53
M3	3.506	3.506	0.0	94.53
M4	19.315	26.583	-3.417	244.7
M5	3.417	3.417	0.0	244.7
M6	7.268	7.268	-22.732	64.39
M7	4.559	12.291	-10.441	64.39
M8	3.506	10.441	0.0	96.47
M9	6.831	6.831	-23.169	32.08
M10	4.476	12.728	-10.441	32.08
M11	19.395	26.226	-3.774	245.6
M12	3.417	3.774	0.0	245.6
M13	4.200	27.287	-2.713	394.7
M14	3.453	2.713	0.0	394.7
M15	22.132	22.132	-7.868	155.7
M16	4.414	4.414	-3.453	155.7
M17	3.453	3.453	0.0	155.7
M18	23.087	23.087	-6.913	908.0
M19	4.663	3.708	-3.204	908.0
M20	3.774	3.204	0.0	908.0
M21	4.192	27.279	-2.721	600.7
M22	3.453	2.721	0.0	600.7
M23	10.708	25.707	-4.293	255.2
M24	2.721	4.293	0.0	255.2
M25	14.999	14.999	-15.001	1005.0
M26	4.293	15.001	0.0	1005.0

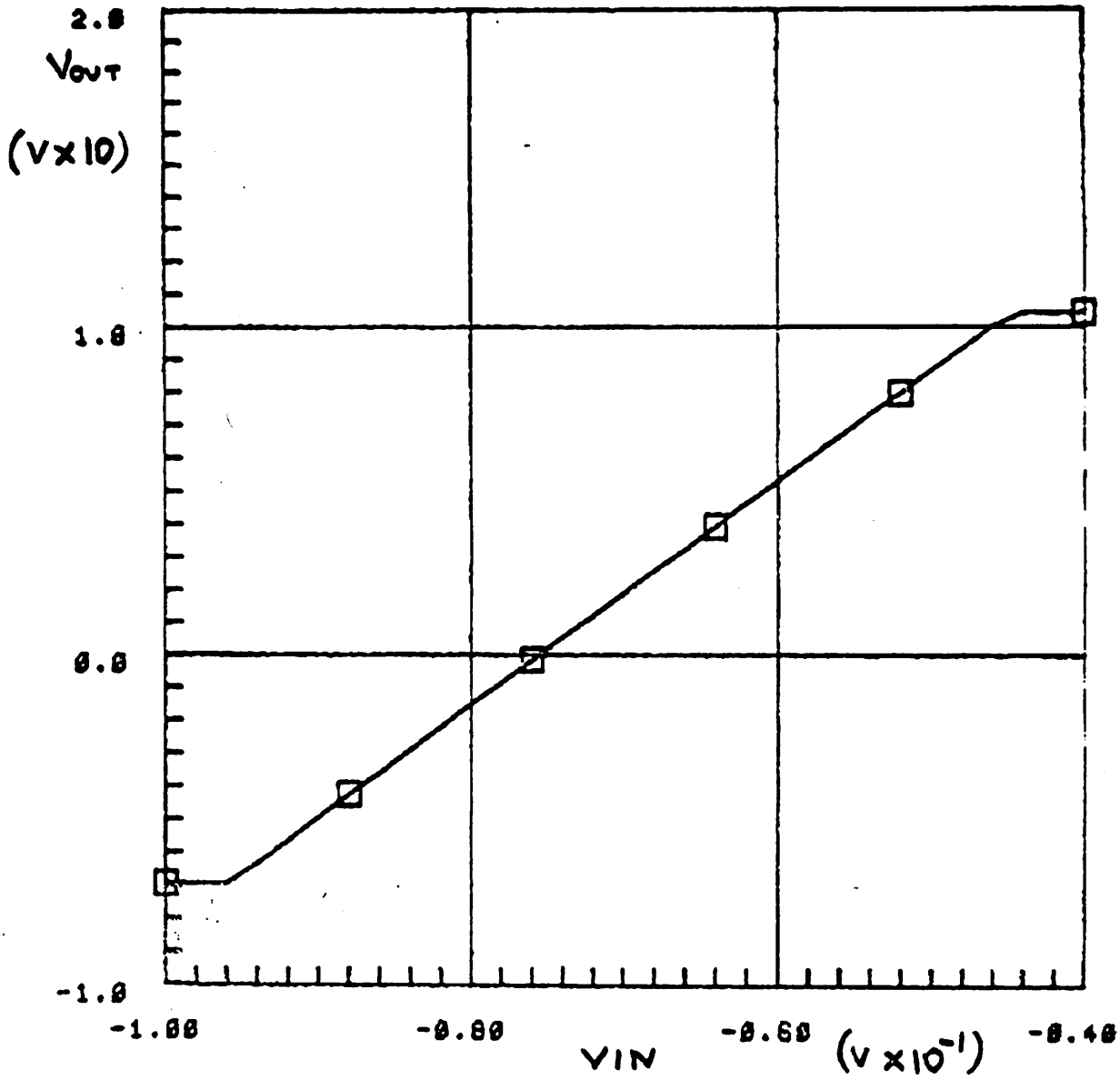


Figure 6.3: Computer simulated DC transfer characteristic.

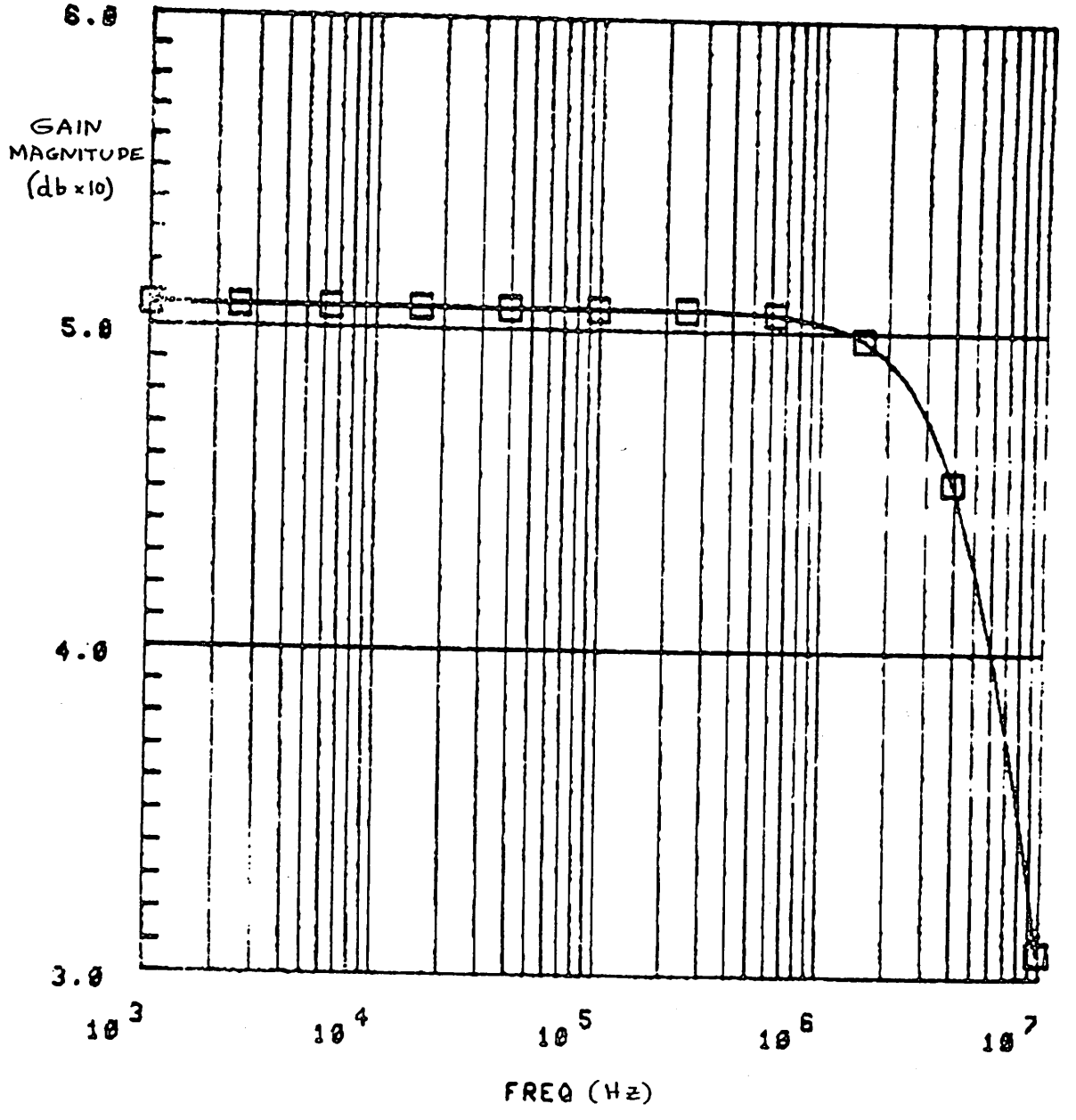


Figure 6.4: Gain magnitude in db vs. frequency for the uncompensated amplifier (computer simulation).

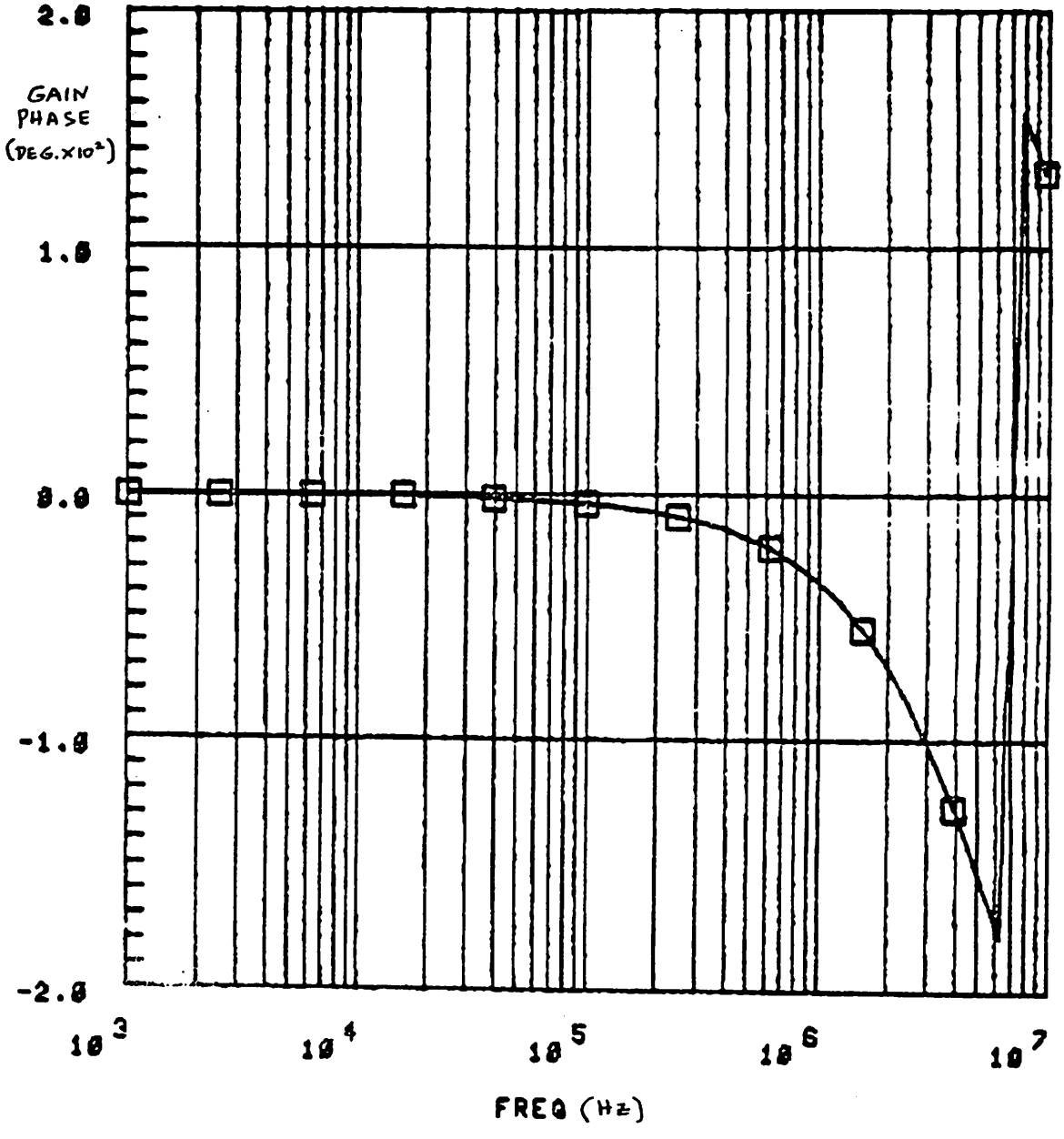


Figure 6.5: Gain phase vs. frequency for the uncompensated amplifier (computer simulation).

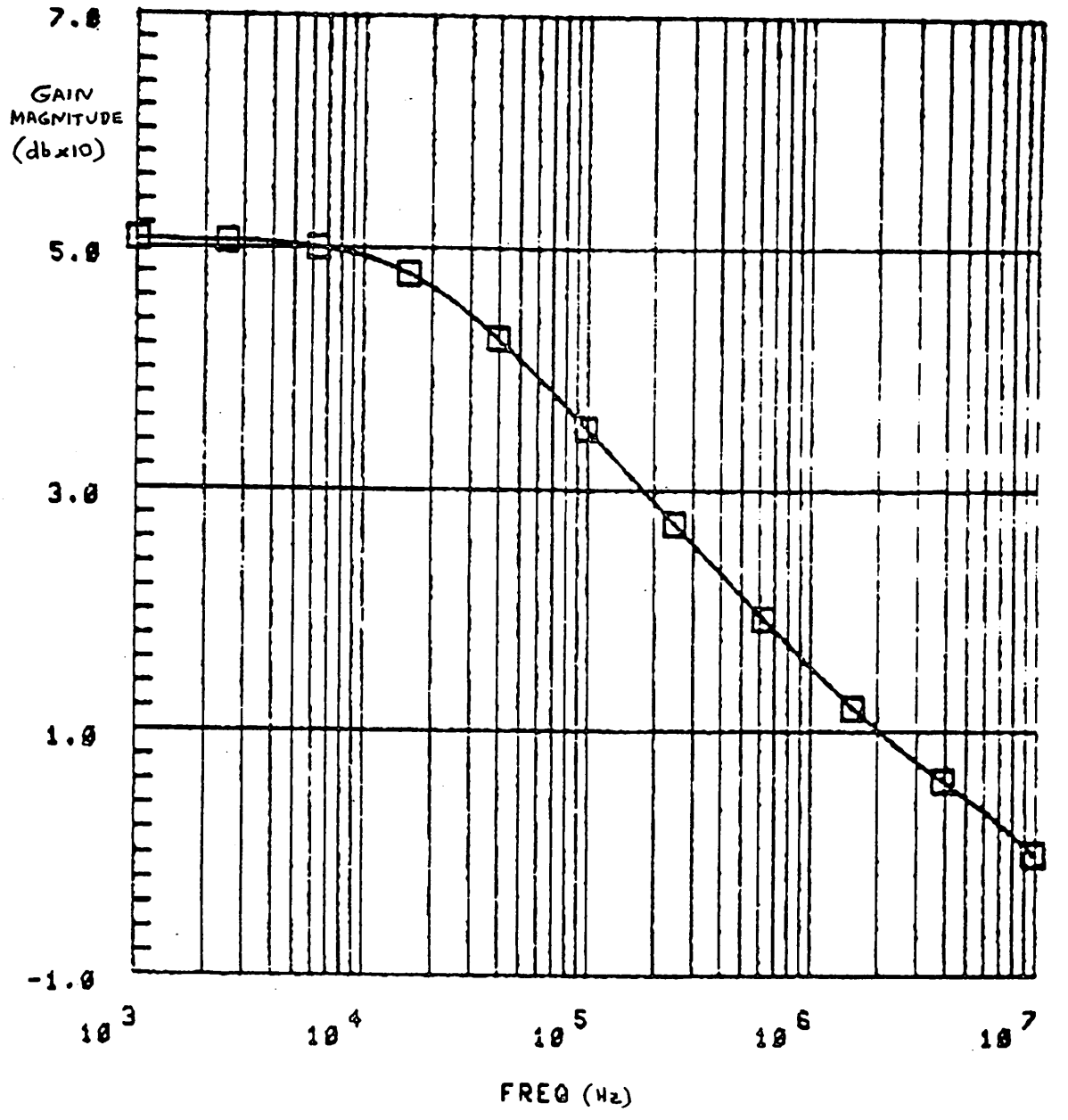


Figure 6.6: Gain magnitude in db vs. frequency for the compensated amplifier (computer simulation).

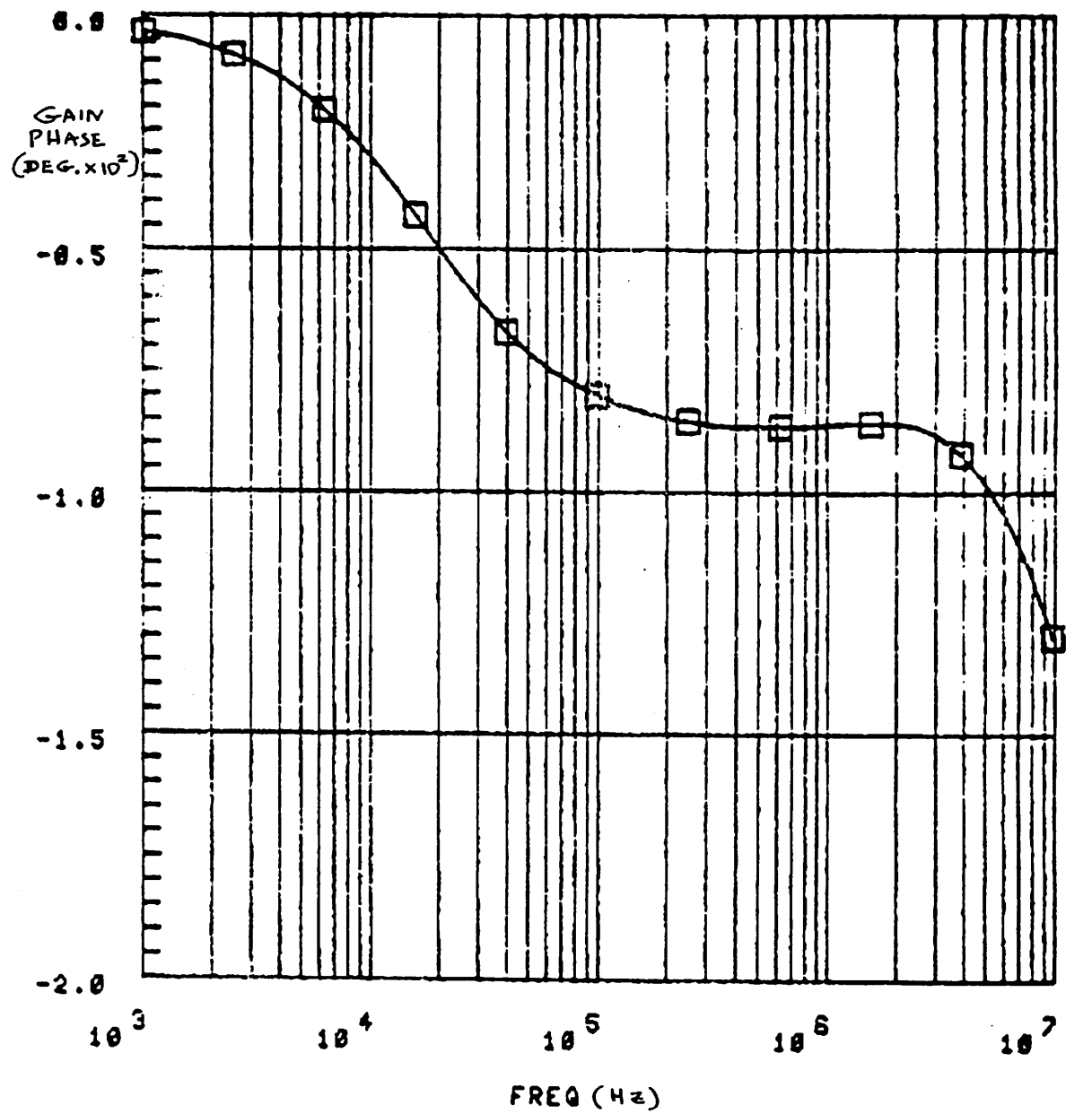


Figure 6.7: Gain phase vs. frequency for the compensated amplifier (computer simulation).

6.6 is 50.7 db, which compares well with the value of 51 db predicted in section 6.4.2.

6.5.4 Step Response

As has been discussed in section 6.3.3, the capacitive load cannot be connected directly across the amplifier's output because the frequency response then is very poor and internal compensation becomes impossible. Loads are therefore connected to the output through a transistor with a Z/L of 3, as shown in Figure 6.8, where the amplifier is shown connected in the unity gain configuration. The step response $v_c(t)$ for this circuit when the input is a +5 volt step and the capacitive load has a value of 70 pF, is shown in Figure 6.9. The 1% settling time is approximately 2 μsec, which is the goal originally set.

The step response for an input step of -5 volts is shown in Figure 6.10. Compared to Figure 6.9, less overshoot but more ringing is present.

6.6 EXPERIMENTAL RESULTS

6.6.1 Experimental Integrated Circuit Description

The amplifier of Figure 6.1 has been fabricated as an integrated circuit at the University of California, Berkeley, using n-channel metal-gate MOS technology. The process is outlined in appendix F. The dimensions used for the devices are given in Table 6.1.

A chip photograph is shown in Figure 6.11. The die is a square 64 mil on a side including the pads. However, these pads are only needed for experimentation, and if the op amp is used or part of a larger IC, so that no pads are necessary, the estimated area it would occupy is 1200 mil^2. The die photo is repeated in Figure 6.12, where each device has been identified by a number corresponding to the schematic of Figure 6.1. It

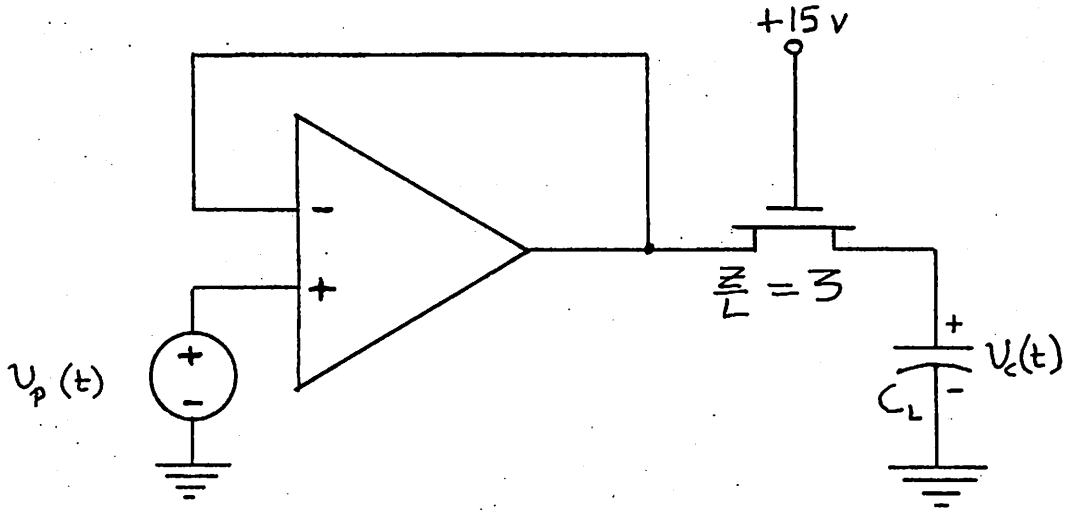


Figure 6.8: Circuit for which transient response is obtained.

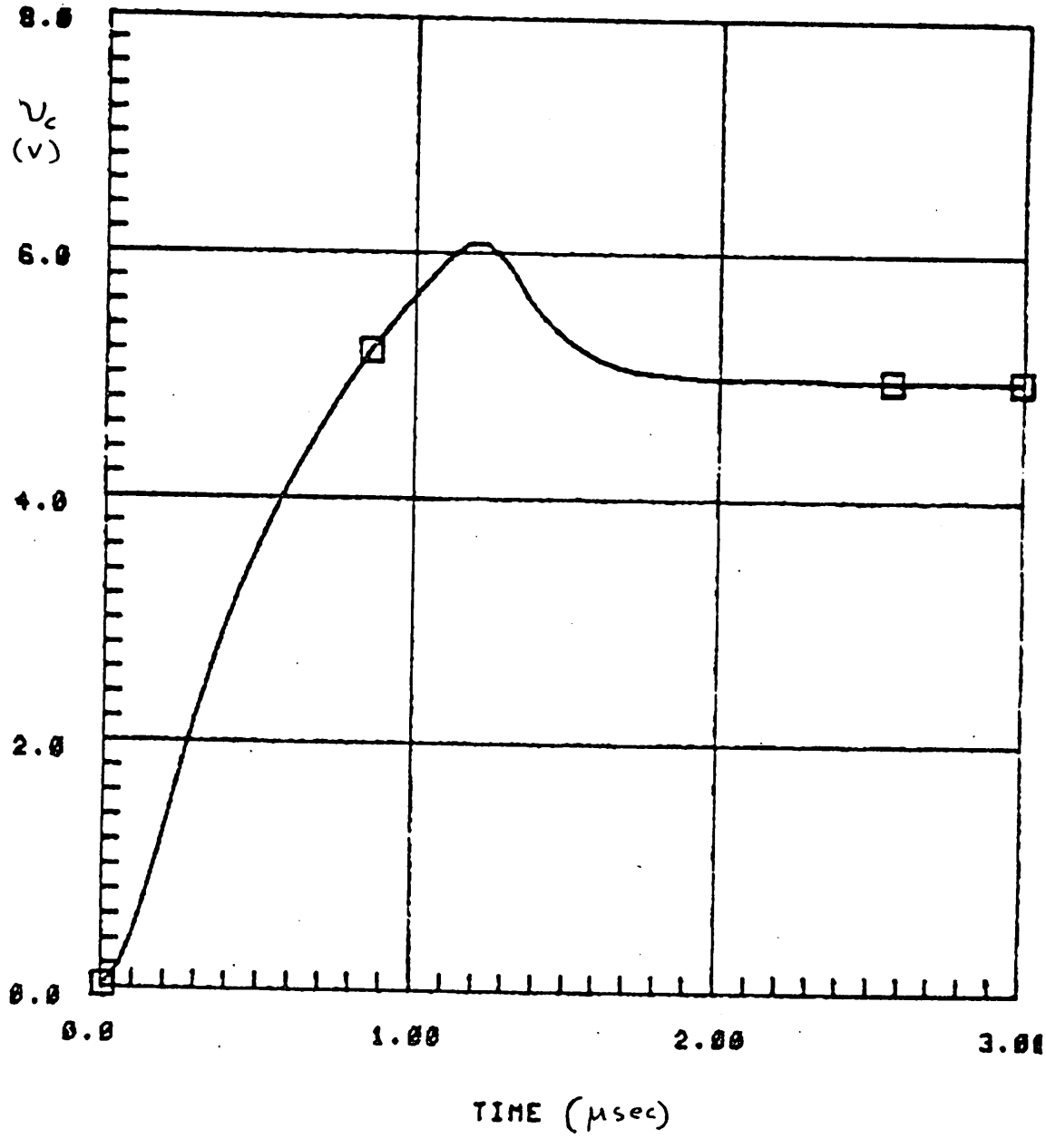


Figure 6.9: Response of the circuit in Figure 6.8 for a +5 v step input (computer simulation).

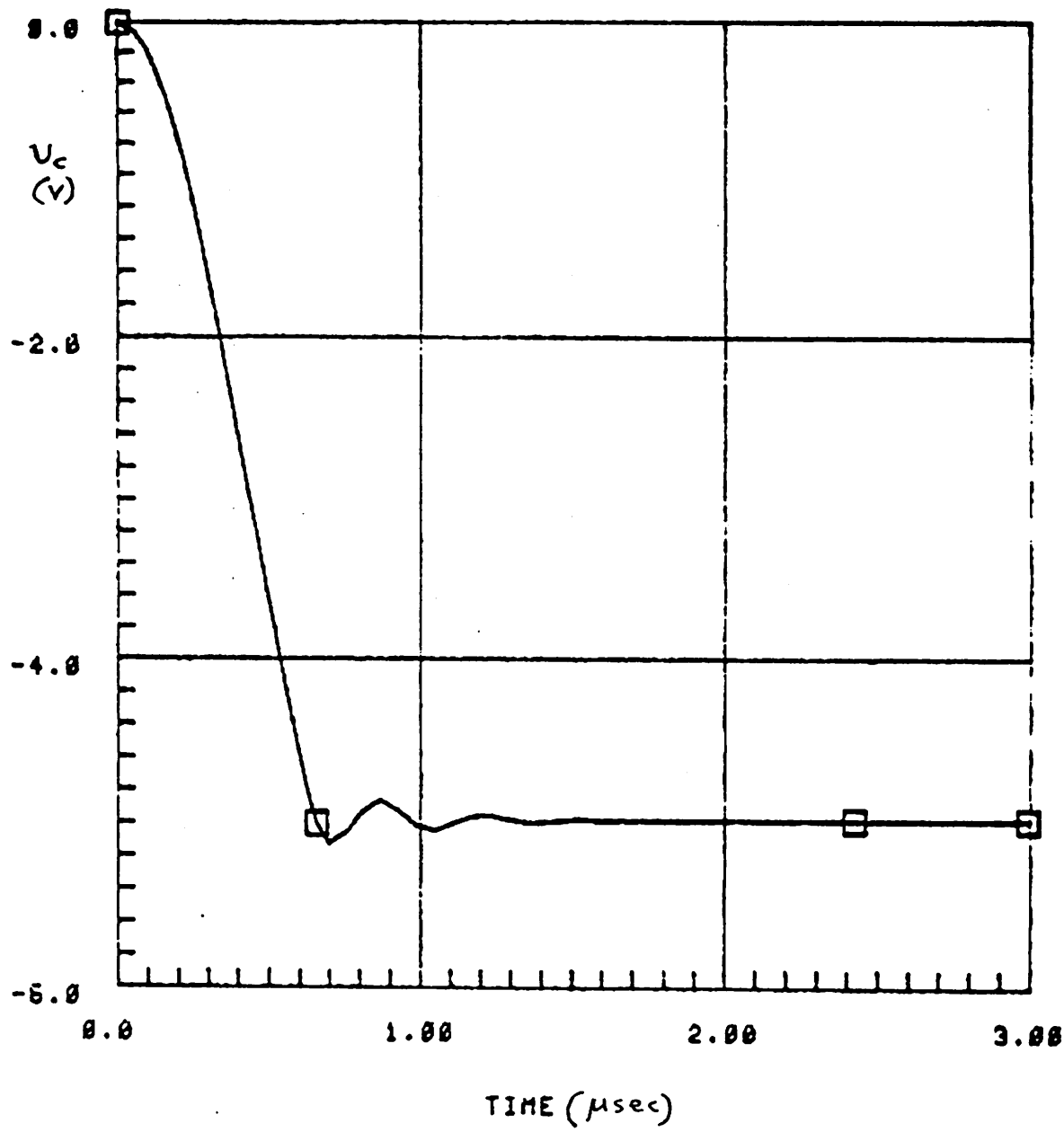


Figure 6.10: Response of the circuit in Figure 6.8 for a -5 v step input (computer simulation).

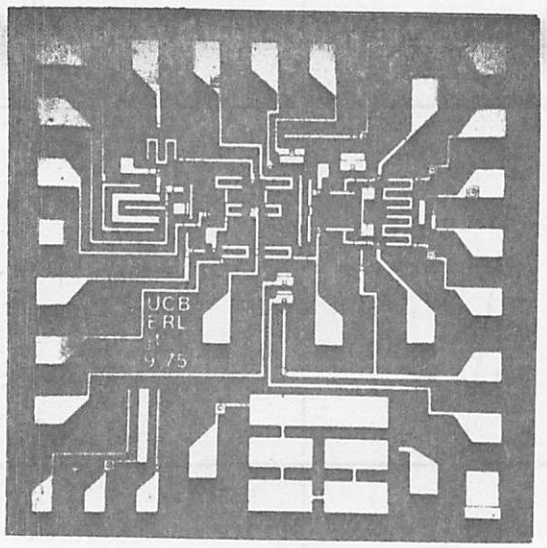


Figure 6.11: Photograph of the amplifier integrated circuit.

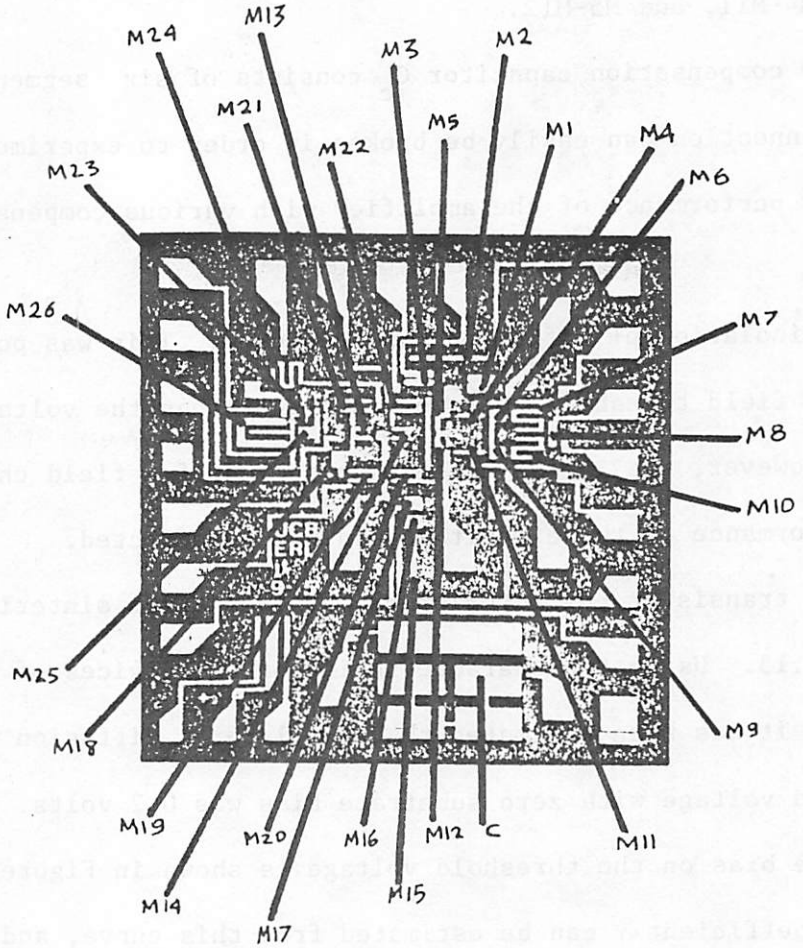


Figure 6.12: Photograph of the amplifier integrated circuit with devices identified according to the schematic in Figure 6.1.

is seen that the input devices M7 and M10 have been laid out so that their matching is not affected by x- or y- misalignment. This is also true for M6-M9, M4-M11, and M5-M12.

The compensation capacitor C_c consists of six segments in parallel, whose connection can easily be broken in order to experimentally investigate the performance of the amplifier with various compensation capacitance values.

No isolation p+ diffusion has been used. This was possible since the expected field threshold voltage was higher than the voltages in the circuit. However, the layout is such that even if a field channel is induced, the performance of the circuit should not be affected.

The transistor characteristics obtained after sintering are shown in Figure 6.13. Using the characteristics of two devices of different channel lengths, it has been estimated that the lateral diffusion was 2.55 μ. The threshold voltage with zero substrate bias was 0.2 volts. The effect of substrate bias on the threshold voltage is shown in Figure 6.14. The body effect coefficient γ can be estimated from this curve, and has a value of approximately 0.92.

6.6.2 Performance Measurements

As mentioned in the previous section, the value of the threshold voltage for zero substrate bias was 0.2 volts. This value is lower than the value assumed in the design, and certainly lower than what can be obtained by using better controlled processes and ion implantation. In order to simulate the performance of the circuit when higher threshold voltages are achieved, a substrate bias of -5 volts with respect to the negative power supply has consistently been used for all measurements, which makes the equivalent threshold voltage equal to approximately 1.5

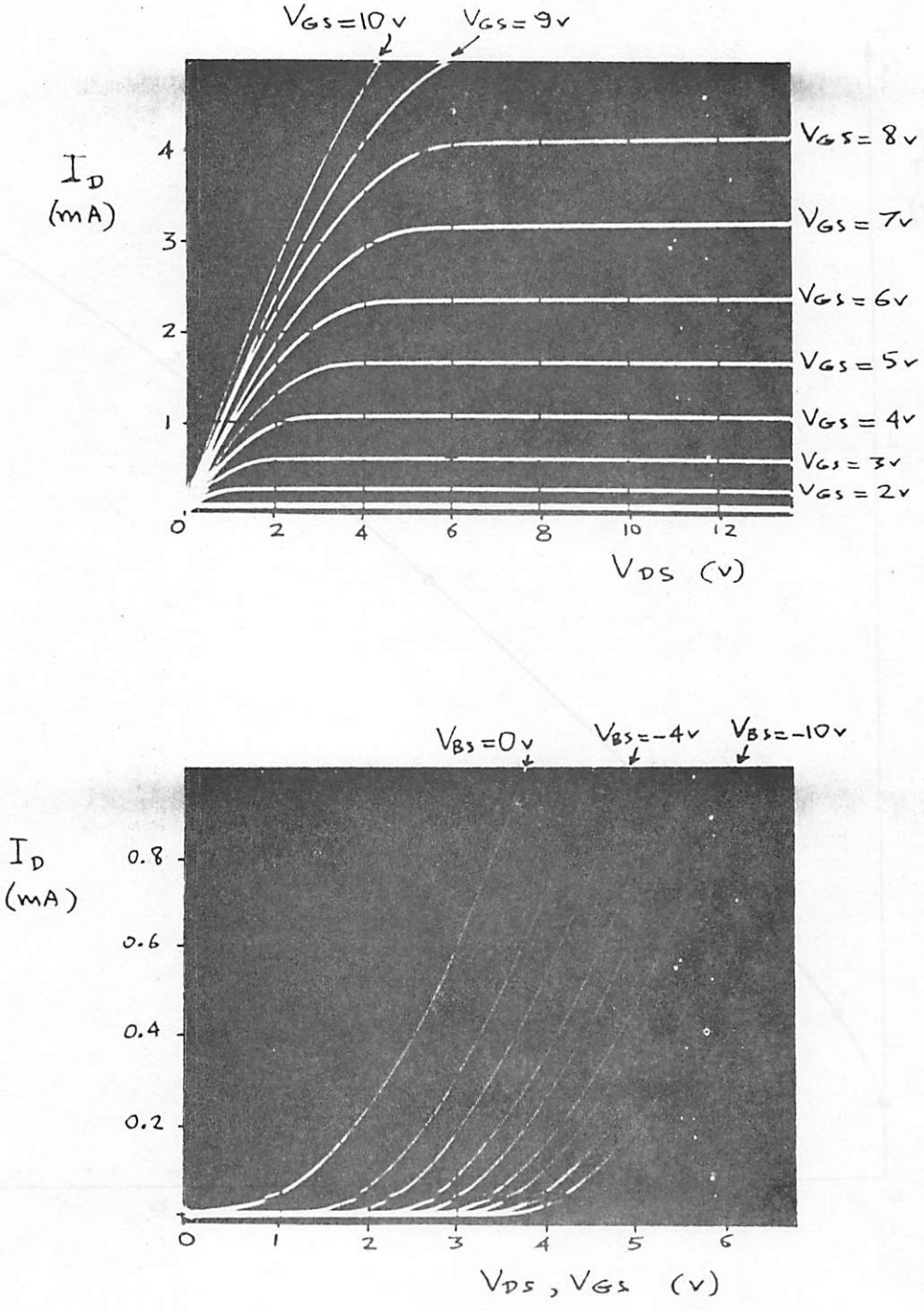


Figure 6.13: Transistor characteristics.

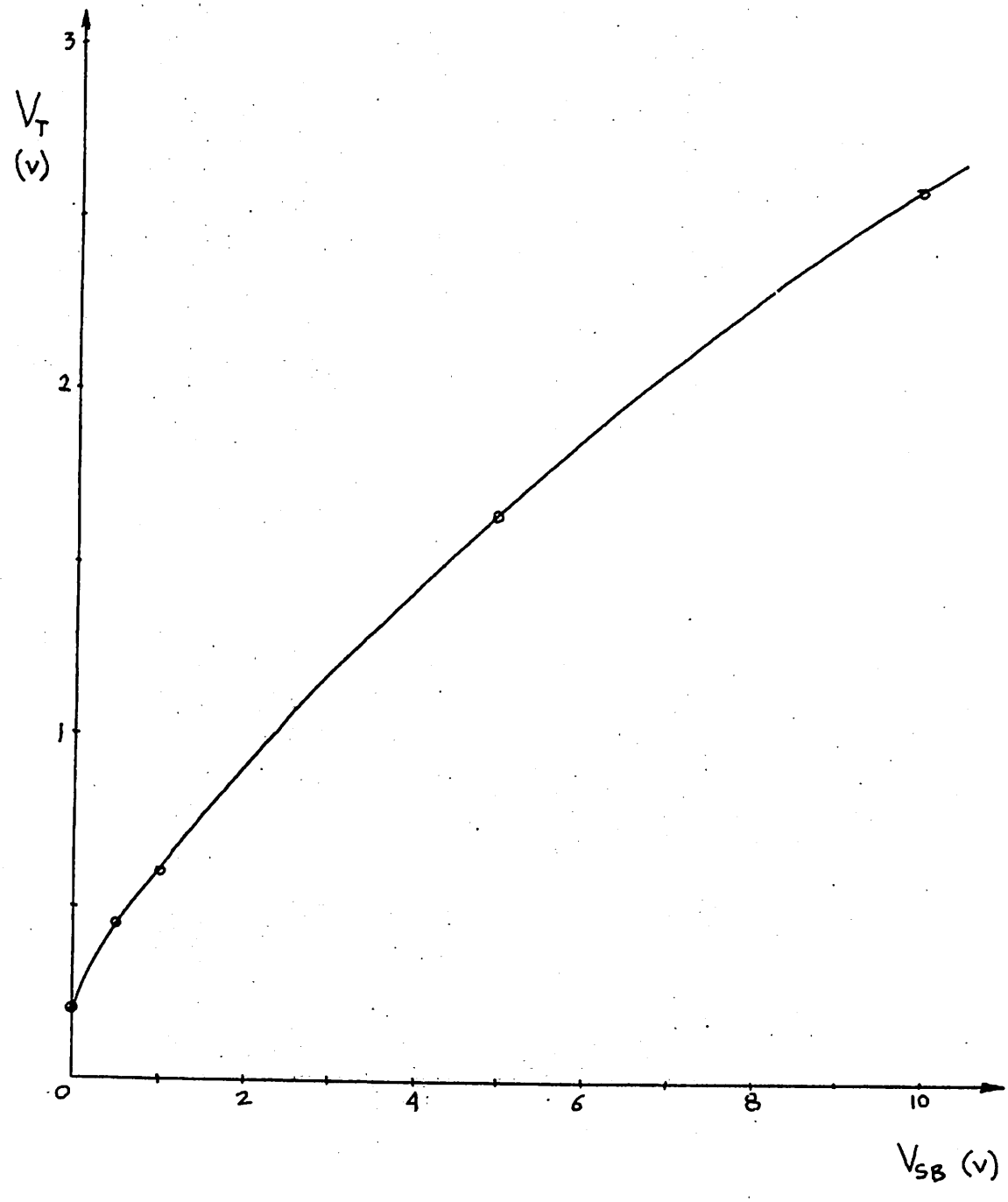


Figure 6.14: Equivalent threshold voltage versus substrate bias.

volts. Although this increases the reverse bias of the junctions so that their small signal capacitances decrease, simulation has shown that the performance of the circuit should be representative of what can be done with a threshold voltage of 1.5 volts and no substrate bias.

The DC transfer characteristic has been obtained as shown in Figure 6.15. It is seen that the +5 to -5 volt output range is certainly achieved.

The input offset voltage had a mean of -65 mV and a standard deviation of 22 mV. This has been traced to modeling problems due to insufficient device parameter data at the design stage, as explained in section 6.5.1. After the circuit was fabricated and additional data was obtained through measurements, it was possible to trim the mask and refabricate circuits whose mean offset was close to zero. This has been undertaken by Burns [43].

The effect of substrate bias on the input offset has been measured and is shown in Figure 6.16a. This data can provide indication about the independence of the offset on the threshold voltage. Similarly, the effect of power supply voltage on the offset is shown in Figure 6.16b. From this graph it follows that the power supply rejection ratio is 3.5 mV/V.

The power supply quiescent current versus substrate bias and versus power supply voltage is shown in Figures 6.17(a) and (b). The low frequency gain variation due to these parameters is shown in Figures 6.18(a) and (b).

The average value of the common mode rejection ratio was 70 db, all chips measured having CMRR's between 66 db and 72 db.

It was found that the 40 pF value suggested for the compensation capacitor by computer simulation was indeed appropriate. The frequency

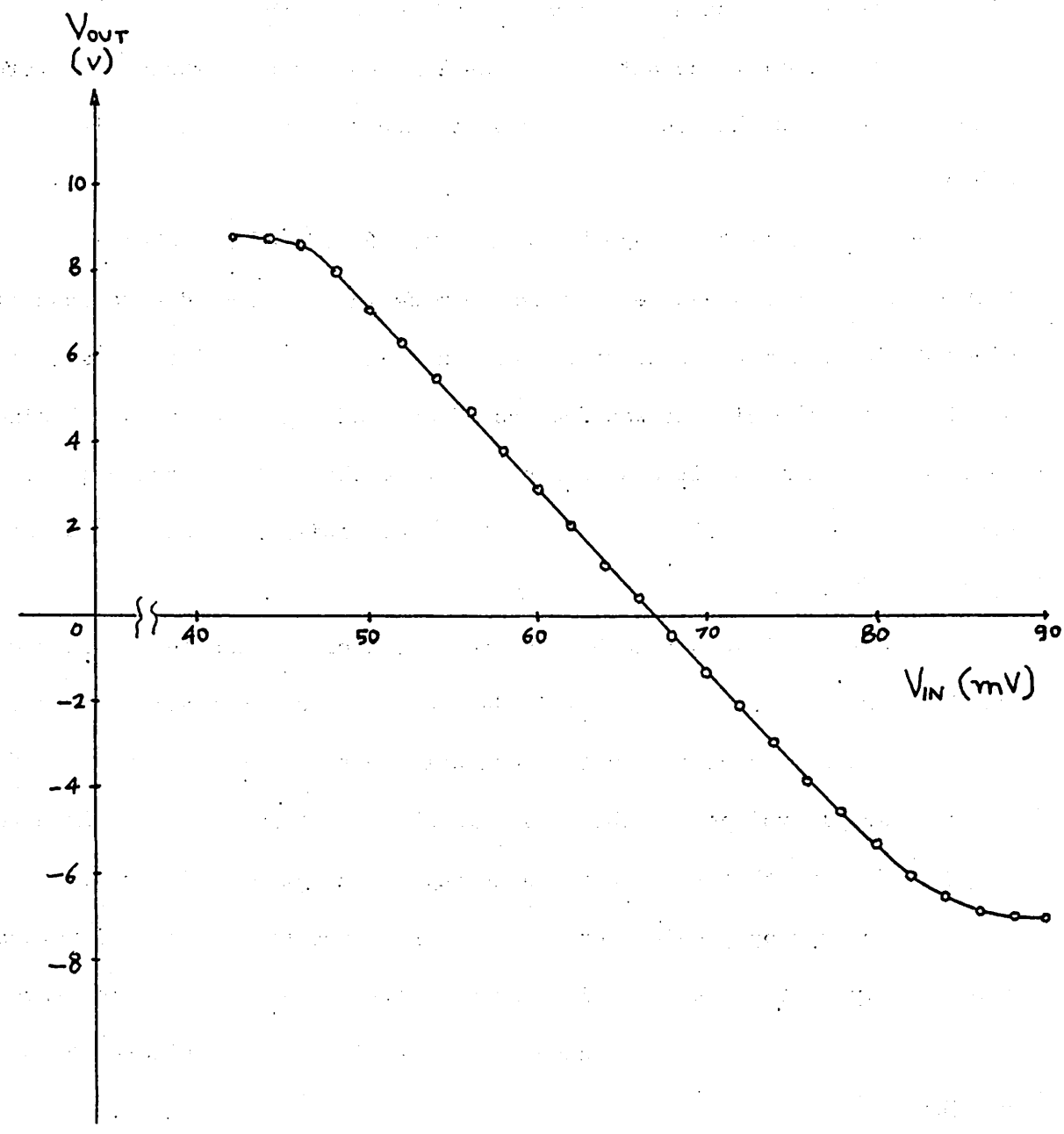


Figure 6.15: Amplifier DC transfer characteristic.

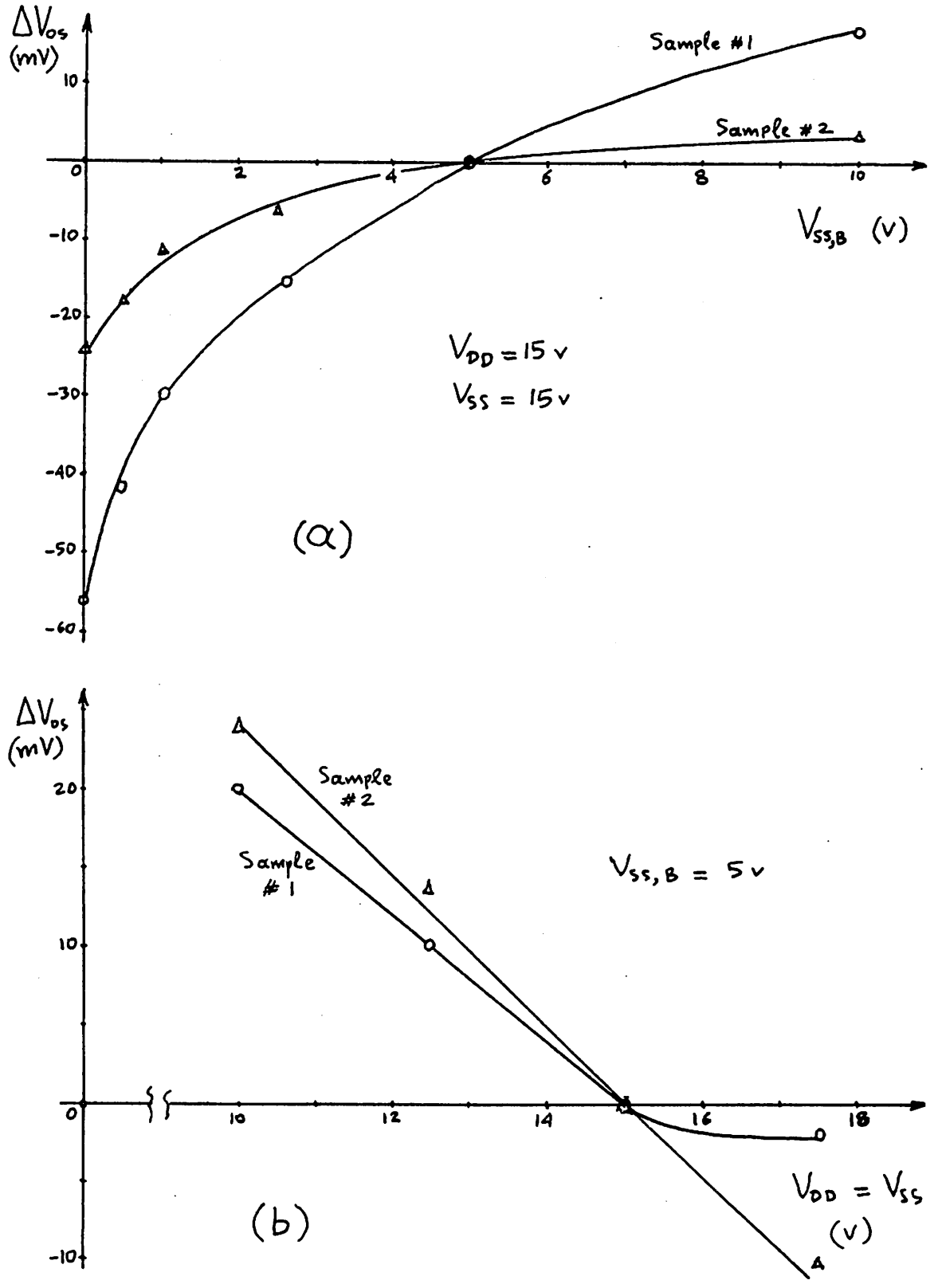


Figure 6.16: (a) Input offset voltage versus substrate bias.
(b) Input offset voltage versus power supply voltage.

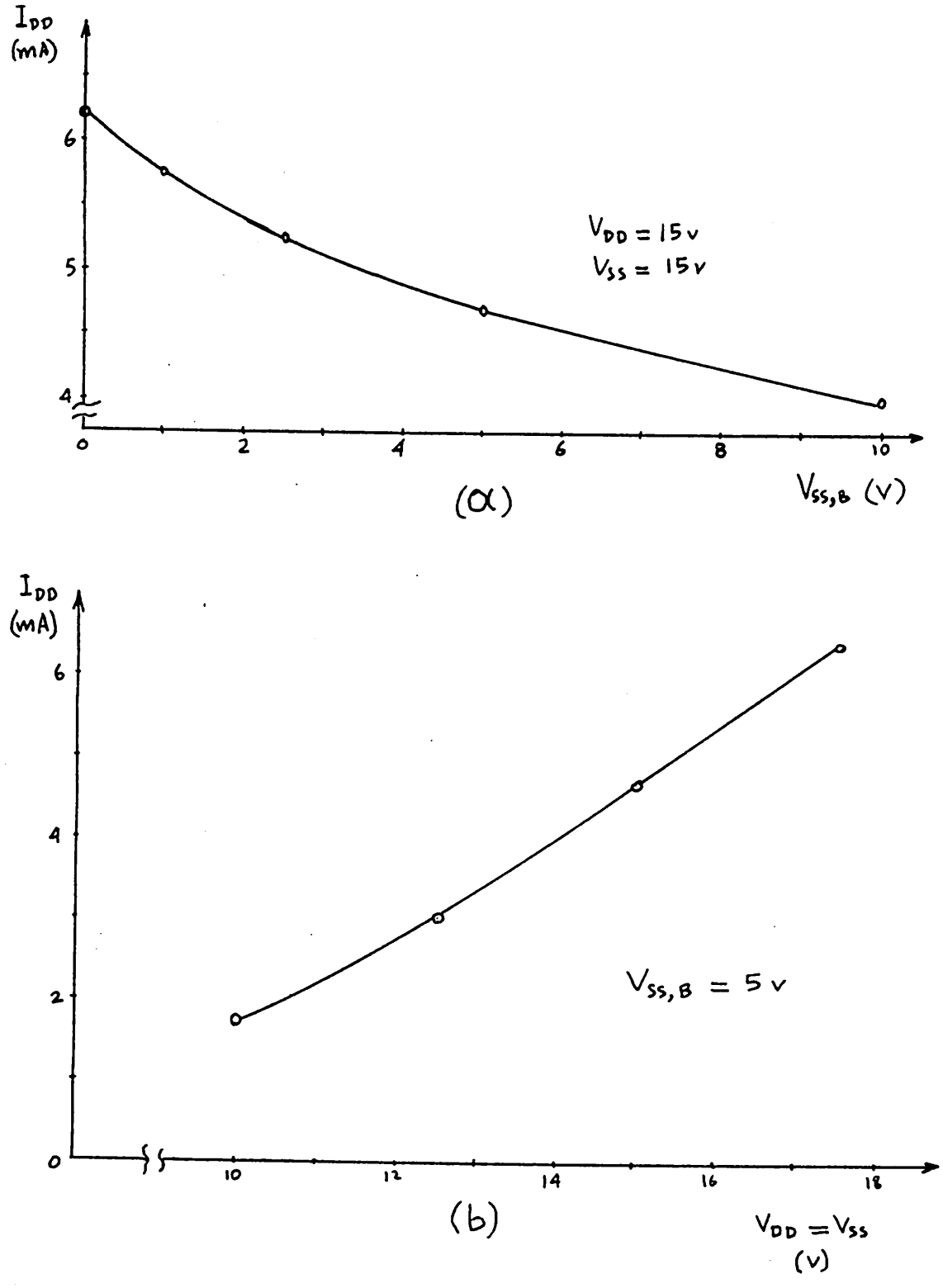


Figure 6.17: (a) Power supply quiescent current versus substrate bias.
(b) Power supply quiescent current versus power supply voltage.

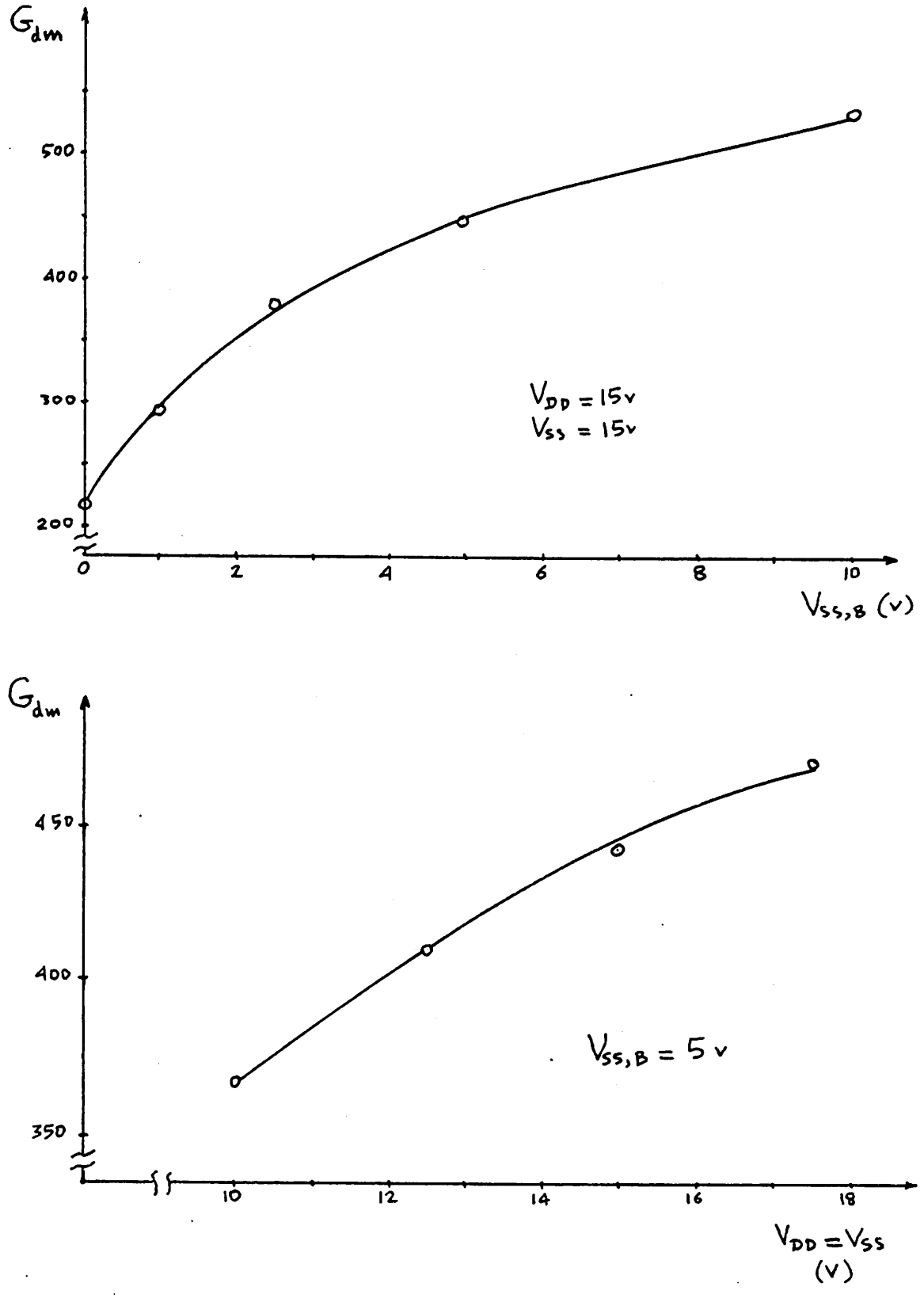


Figure 6.18: (a) Low frequency gain versus substrate bias.
(b) Low frequency gain versus power supply voltage.

response using this value is shown in Figures 6.19 and 6.20. The magnitude peaking predicted by computer simulation is indeed observed in these measurements. The unity gain frequency was 5.2 MHz. The phase margin was measured as 35°. It is believed that this value is lower than that predicted by simulation because of the loading effect of the phase measuring equipment. Simulating this loading effect on the computer showed a phase degradation of more than 10°, which should account for the discrepancy observed.

The step response of the amplifier when connected in a unity gain configuration and charging the load capacitance through a transistor, as shown in Figure 6.8 has been also experimentally investigated. The reason for this series transistor has been explained in section 6.3.3. The 1% settling time was 2.5 μsec for power supply voltages of $\pm$ 15 v. This is higher than the value of 2 μsec predicted by computer simulation, and the discrepancy has been attributed to the fact that the series transistor connected between the amplifier output and the capacitive load was off chip, and therefore excessive parasitic capacitance due to packaging and wiring appeared directly across the amplifier's output, thus reducing the phase margin. The power supply voltages were then changed to + 16 v and - 14 v. This resulted in a settling time of 2 μsec, and the waveforms obtained are shown in Figure 6.21. This improvement in the settling time can be explained by noting that although the total voltage across the amplifier remained equal to 30 v, more voltage was droped across M25. The current of the output inverter was thus increased, increasing the transconductance of M25 and M26, and the output resistance of the amplifier decreased as dictated by equation (5.52), thus reducing the effect of the parasitic capacitance mentioned above. If the series transistor shown in Figure 5.36 was on-chip, the 2 μsec settling time should have

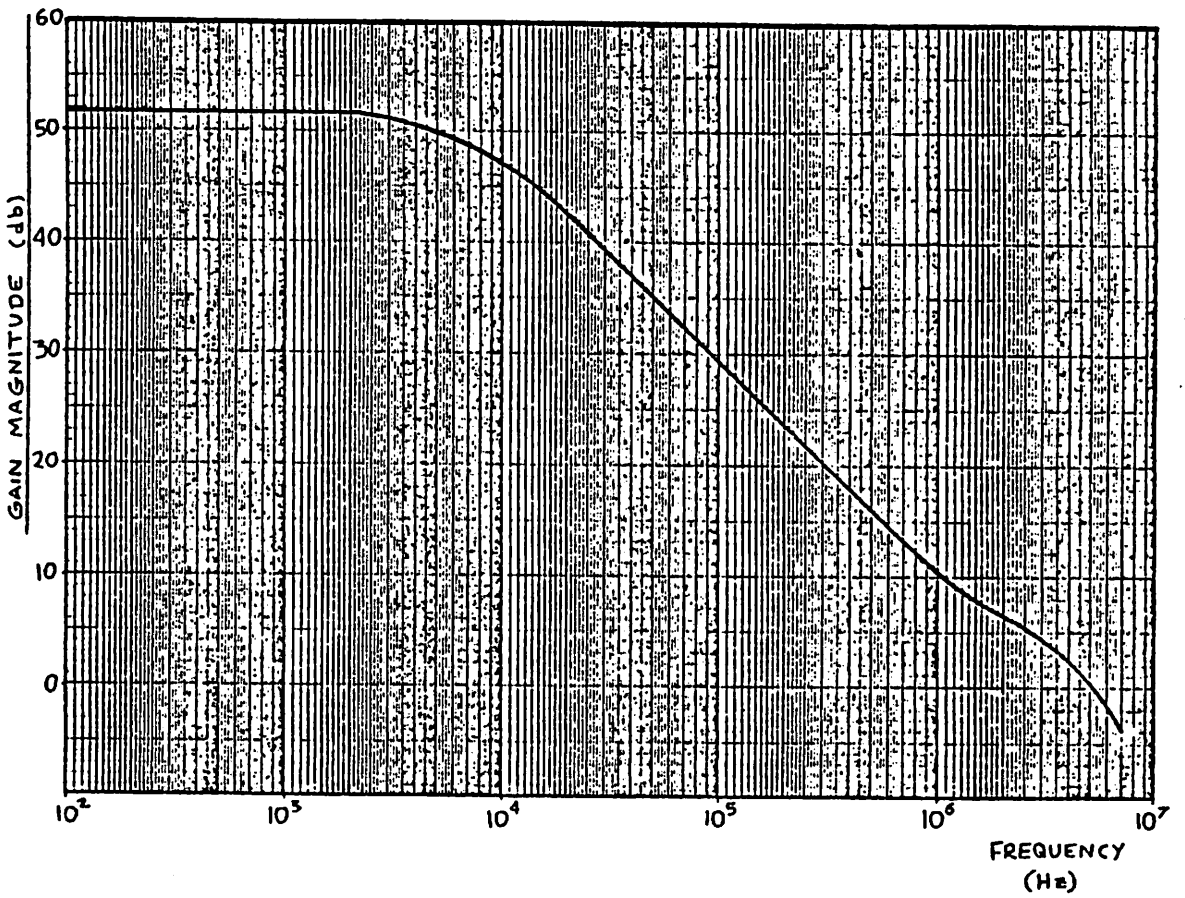


Figure 6.19: Gain magnitude vs. frequency for the compensated amplifier (experimental).

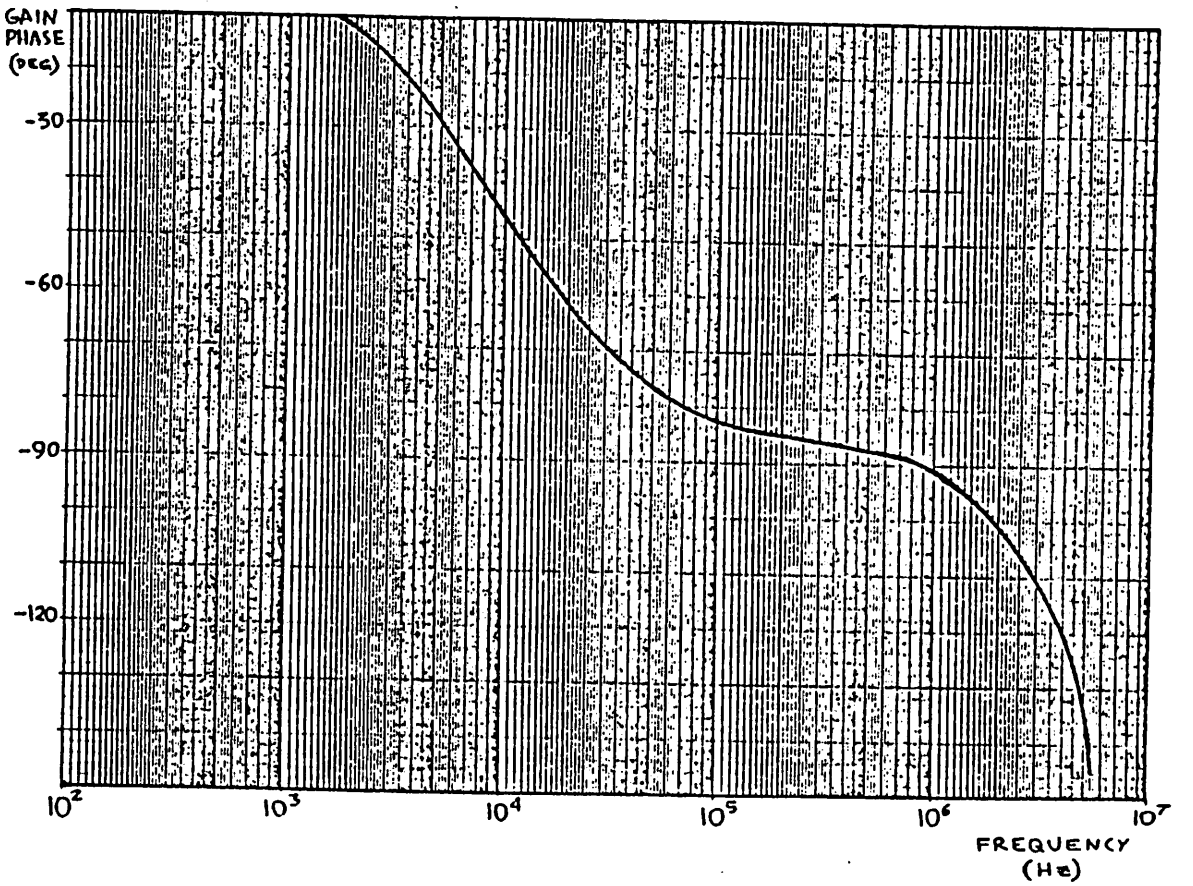


Figure 6.20: Gain phase vs. frequency for the compensated amplifier (experimental).

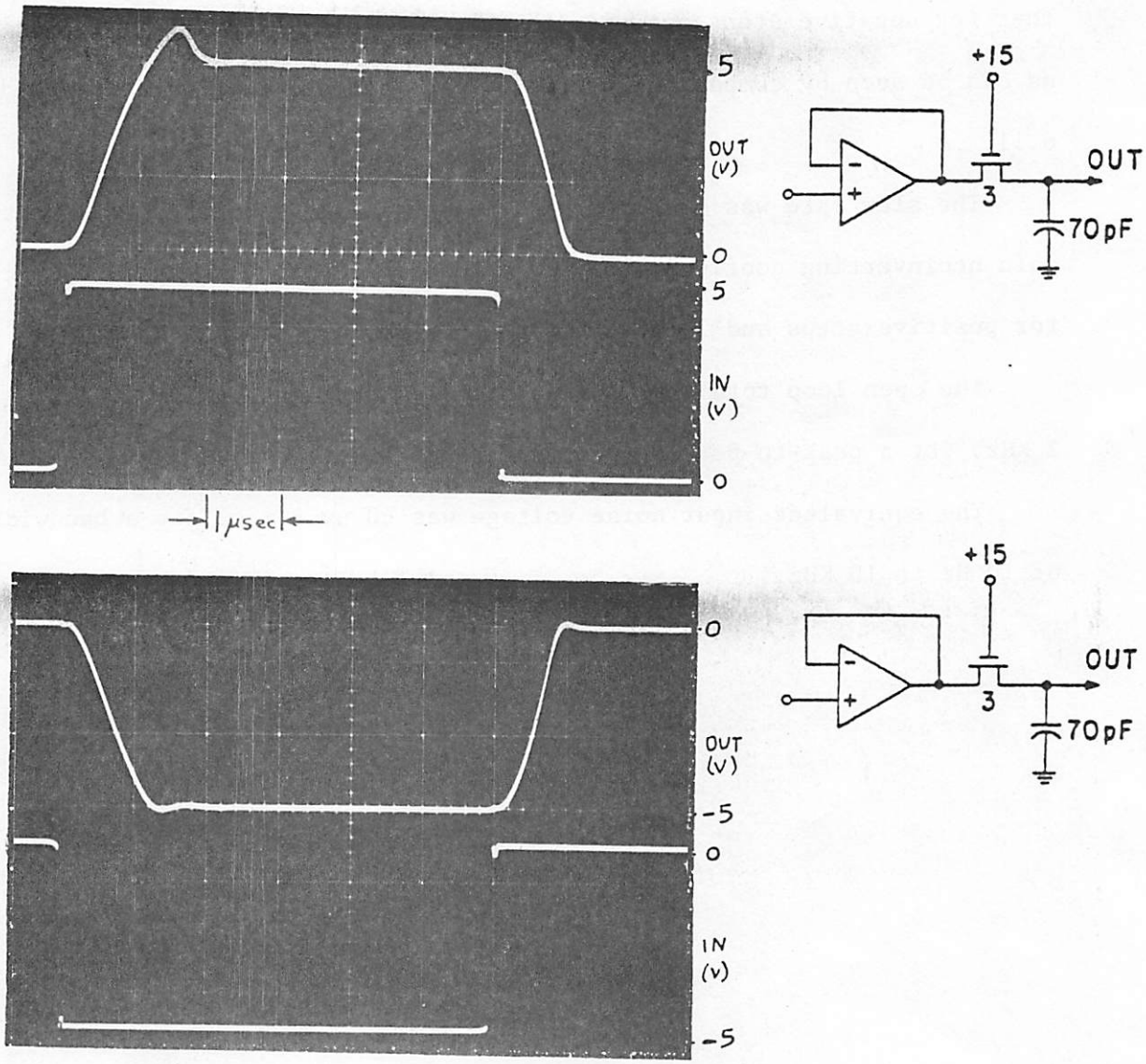


Figure 6.21: Step response.

been achieved with power supply voltages of $\pm$ 15 v, as predicted by simulation. The fact that the overshoot for positive steps is larger than that for negative steps agrees with that predicted by computer simulation, as can be seen by comparing Figures 6.22(a) and (b) to Figures 6.9 and 6.11.

The slew rate was measured with the amplifier connected in a unity gain noninverting configuration and a load of 10 pF. It was 20 v/μsec for positive steps and 12 v/μsec for negative.

The open loop total harmonic distortion was measured as 1.5% at 1 KHz, for a peak-to-peak output voltage of 10 v.

The equivalent input noise voltage was 60 μv r.m.s. for a bandwidth of 10 Hz to 10 KHz.

CHAPTER 7

PROTOTYPE PCM ENCODER SYSTEM AND EXPERIMENTAL RESULTS

7.1 INTRODUCTION

A PCM encoder scheme using the principle of charge redistribution has been described in Chapter 4. Computer simulation results given there have shown that it should be possible to implement the complete encoder as a single MOS chip. For experimental evidence of this, a PCM encoder prototype was built in which all critical parts were fabricated as n-channel aluminum gate MOS integrated circuits. The implementation of this prototype, the measurements performed on it and the results obtained will now be described. The experimental results for the operational amplifier performance are given separately in Chapter 6.

7.2 IMPLEMENTATION OF THE ENCODER

The principle of operation of the charge redistribution PCM encoding scheme has been described in Chapter 4 in conjunction with Figure 4.7. The experimental setup to implement this scheme was built by Chacko [44] The block diagram of the system is shown in Figure 7.1. Here, the logic controls the throwing of the electronic analog switches and develops the output PCM word corresponding to the input analog voltage value to be encoded. The logic is in turn controlled by the output of the comparator.

Two separate reference voltages were used in this setup (+5 v and -5 v). However, using a single reference source is possible, as described in Chapter 4.

To implement the upper and lower capacitor arrays and the comparator, two of the A/D converter chips developed by McCreary [28] have been modified and used. The capacitor matching characteristics obtained in these chips have been shown adequate for 10 bit resolution [28], which

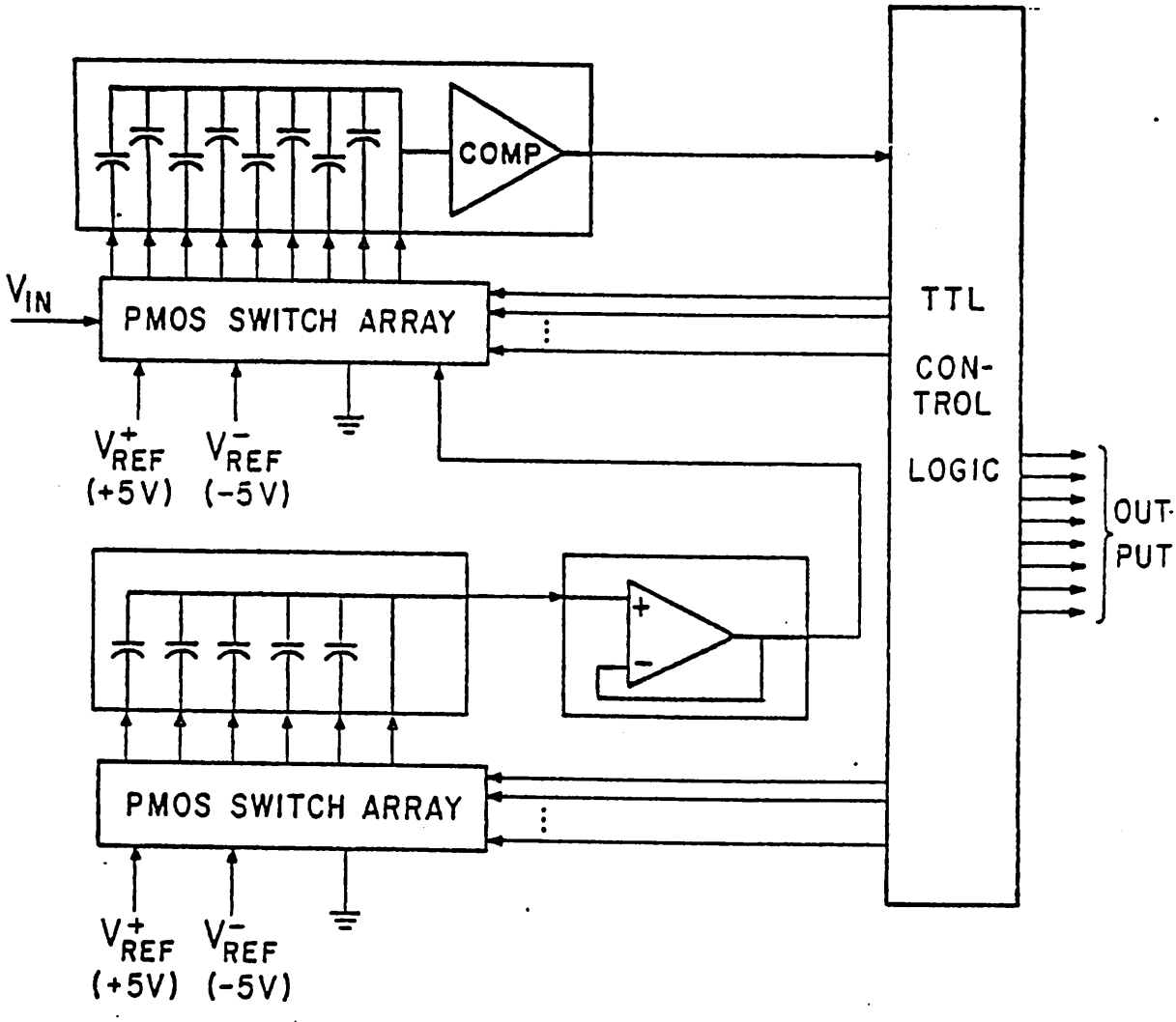


Figure 7.1: Block diagram of the experimental PCM encoder.

corresponds to much higher accuracy than what was determined necessary for 8-bit PCM in Chapter 4. A schematic of the comparator is shown in Figure 7.2(a) and a photograph of a chip containing the comparator and one capacitor array is shown in Figure 7.2(b). A detailed description of this chip is given in [28].

The op-amp used to implement the unity gain buffer was fabricated using the same technology with the one used for the comparator and capacitor array chips, and is described in detail in Chapter 6.

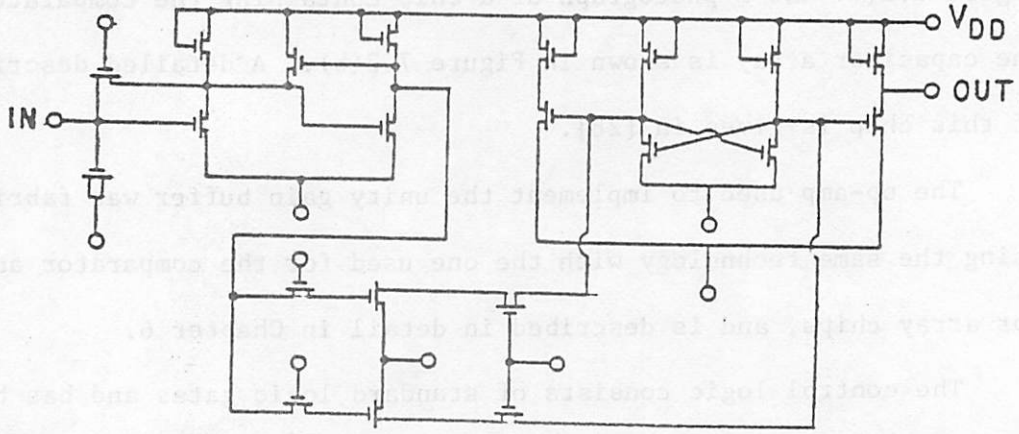
The control logic consists of standard logic gates and has been implemented using discrete TTL integrated circuits. Integrating the logic in NMOS is straight-forward and was therefore not attempted.

Although there are no problems in fabricating the analog switches required in NMOS, the number of package pins required for their connection to the rest of the system would be prohibitive, since most of them are equivalent to single-pole triple-throw types. Commercially available PMOS switches have been used, their performance being similar to that attainable in NMOS.

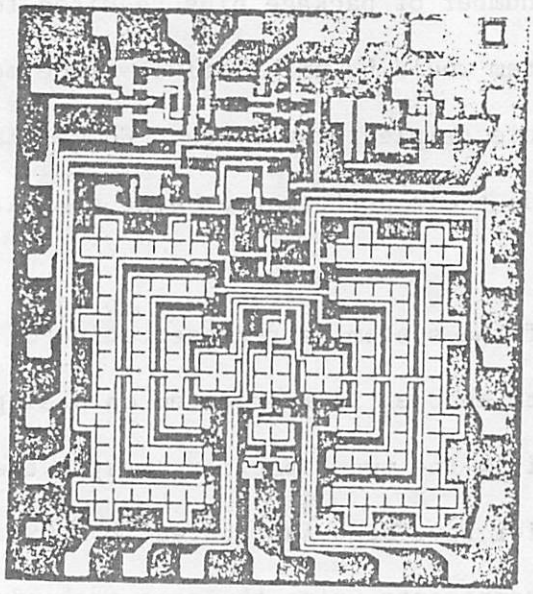
The performance of the system is representative of what can be achieved if the complete encoder is fabricated on a single chip, since all critical parts, mainly the two capacitor arrays, the comparator and the operational amplifier have been fabricated in NMOS, and the fabrication of the remaining components using the same technology is straightforward. Estimates for the size and power consumption of a single chip realization are given in Chapter 4.

7.3 SYSTEM OPERATION

The control logic and switches of Figure 7.1 are shown in more detail



(a)



(b)

Figure 7.2: McCreary's comparator.
(a) Schematic.
(b) Die photograph of comparator and one capacitor array.

in Figure 7.3. The central control circuit of the logic is a 4-bit shift register termed a state sequencer in Figure 7.3. The several control signals necessary for the comparator are generated by the comparator signal generator shown. The upper capacitor array switches are controlled by the corresponding gating logic block, which is in turn controlled by an 8-bit bidirectional shift register, termed the upper array sequencer in the figure. Similarly, another gating logic block and a 5-bit shift register, termed the lower array sequencer, control the switches of the lower capacitor array. A separate circuit with a latch is used for determining the sign of the input voltage. Upon determination of each bit of the PCM word, the latter appears at the output of the output buffer register in parallel form, but can easily be made to appear sequentially on a single output line if desired. For details on the logic circuits contained within each block of Figure 7.3 and their sequence of operation, the reader is referred to [44].

The sequence used for encoding has been described in section 4.4.4. The segments are tested sequentially, starting with the smallest. The step determination is done by successive approximation. A clock frequency of 1 MHz is used. The sampling rate is 8 KHz, and a conversion is completed in 56 μsec or less, depending on the segment in which the input lies.

7.4 TEST SETUP

The heart of the test setup used in the measurements is shown in Figure 7.4. In order that the measurement results reflect the performance of the encoder alone, a high accuracy decoder was used [45,44]. The decoder consists of two programable ROM's through which the 8-bit PCM word at the output of the encoder is converted into a 13-bit uniformly encoded

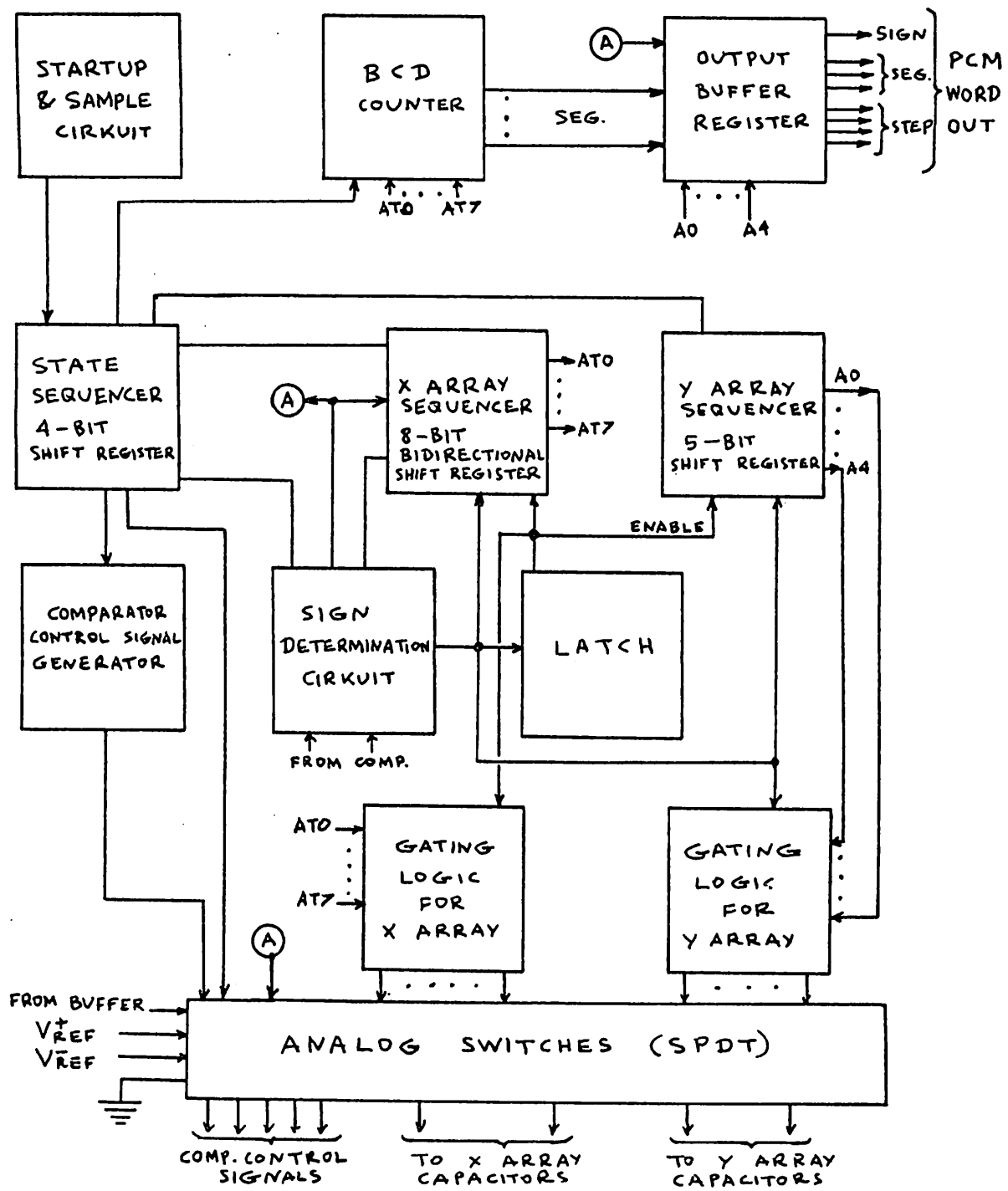


Figure 7.3: Block diagram of the encoder logic.

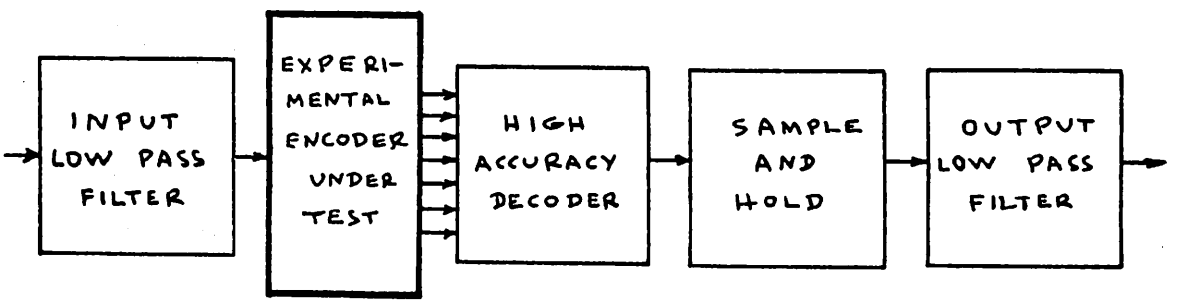


Figure 7.4: Basic test setup.

word, which is subsequently converted into an analog value by a 16-bit DAC. At the output of the encoder a sample-and-hold circuit is used which holds the signal value for a duration equal to the sampling period.

The input and output filters shown are sixth order and fourth order passive configurations respectively. The frequency response of the two filters in cascode, separated by a buffer is shown in Figure 7.5(a). The cutoff frequency is close to 3.4 KHz, and a 0.3 db peaking exists in the vicinity of 3 KHz.

The frequency response of the complete PCM system is shown in Figure 7.5(b). It is seen that it drops significantly over the passband, being 1.8 db down at 3 KHz. This can be fully explained by examining equation (2.29), from which the magnitude of the transfer function of the sample-and-hold circuit is:

$$|H(f)| = T_s|\text{sinc}fT_s| \tag{7.1}$$

where T_s is the sampling period. For the value of T_s = 1/8 KHz used, the above function is -2.1 db at 3 KHz with respect to zero frequency. Adding the +0.3 db peaking due to the filters gives 1.8 db, which is the observed drop at the 3 KHz. The frequency response can be made flat by making the hold interval extremely short, in which case $|H(f)|$ spreads in frequency and is practically flat over the passband (see Figure 2.21). Alternatively, the output filter can be designed so that its transfer function magnitude is inversely proportional to $|H(f)|$ given by equation (7.1) over the passband. Neither of these methods has been attempted, and therefore the frequency response obtained will be taken into account in interpreting the results below.

In principle, the references voltages used are the same for both capacitor arrays. In the experimental setup however, although $\pm$5v was used

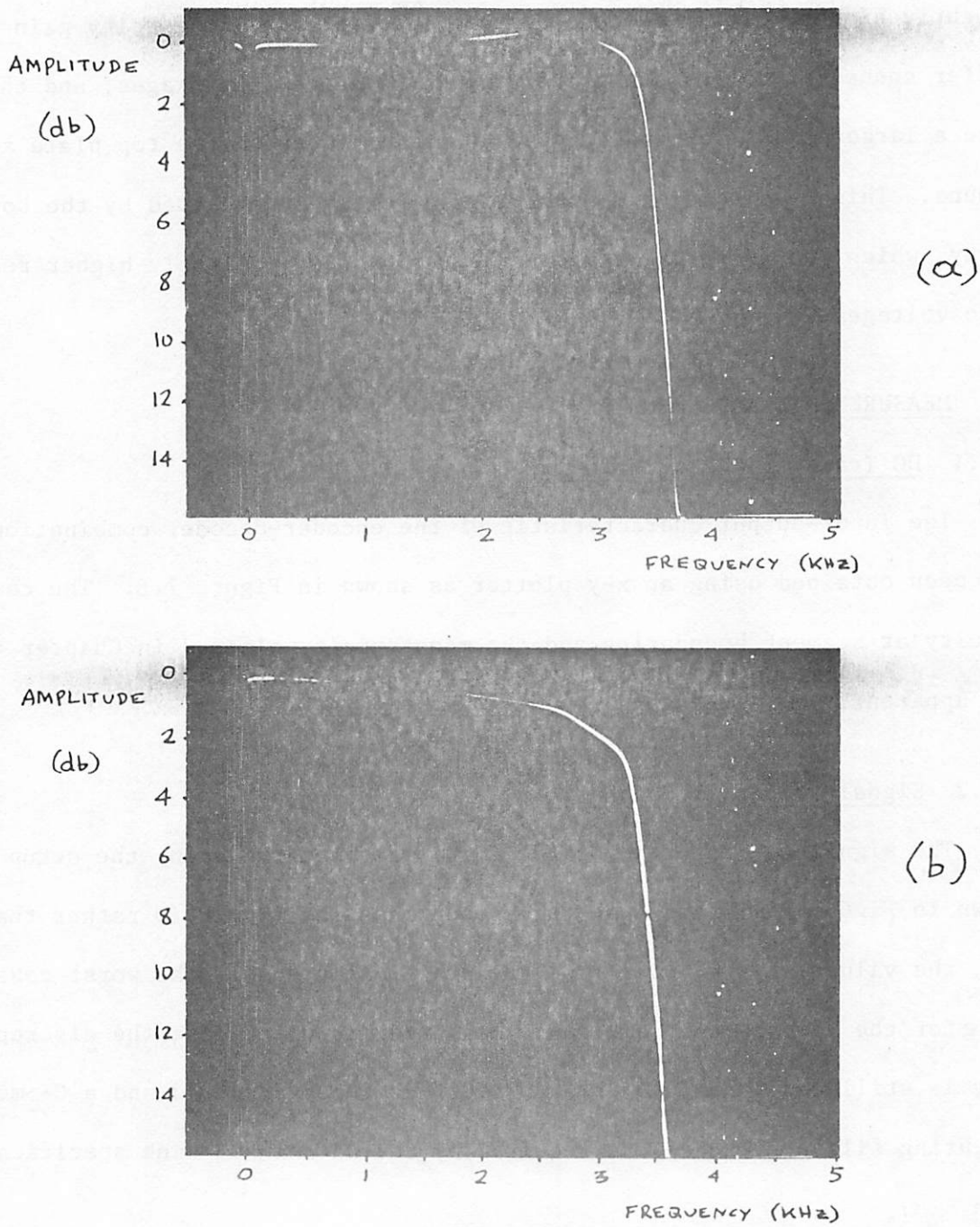


Figure 7.5: (a) Frequency response of the two filters separated by a buffer.

(b) Frequency response of the PCM system in Figure 7.4.

for the top array, the reference voltages used for the bottom array were slightly higher. This was done because that array and the unity gain buffer connected to its top plate were in separate IC packages, and therefore a large parasitic capacitance was present between the top plate and ground. This created a gain error in the voltages developed by the bottom array, which was therefore compensated for by using slightly higher reference voltages.

7.5 MEASUREMENTS AND RESULTS

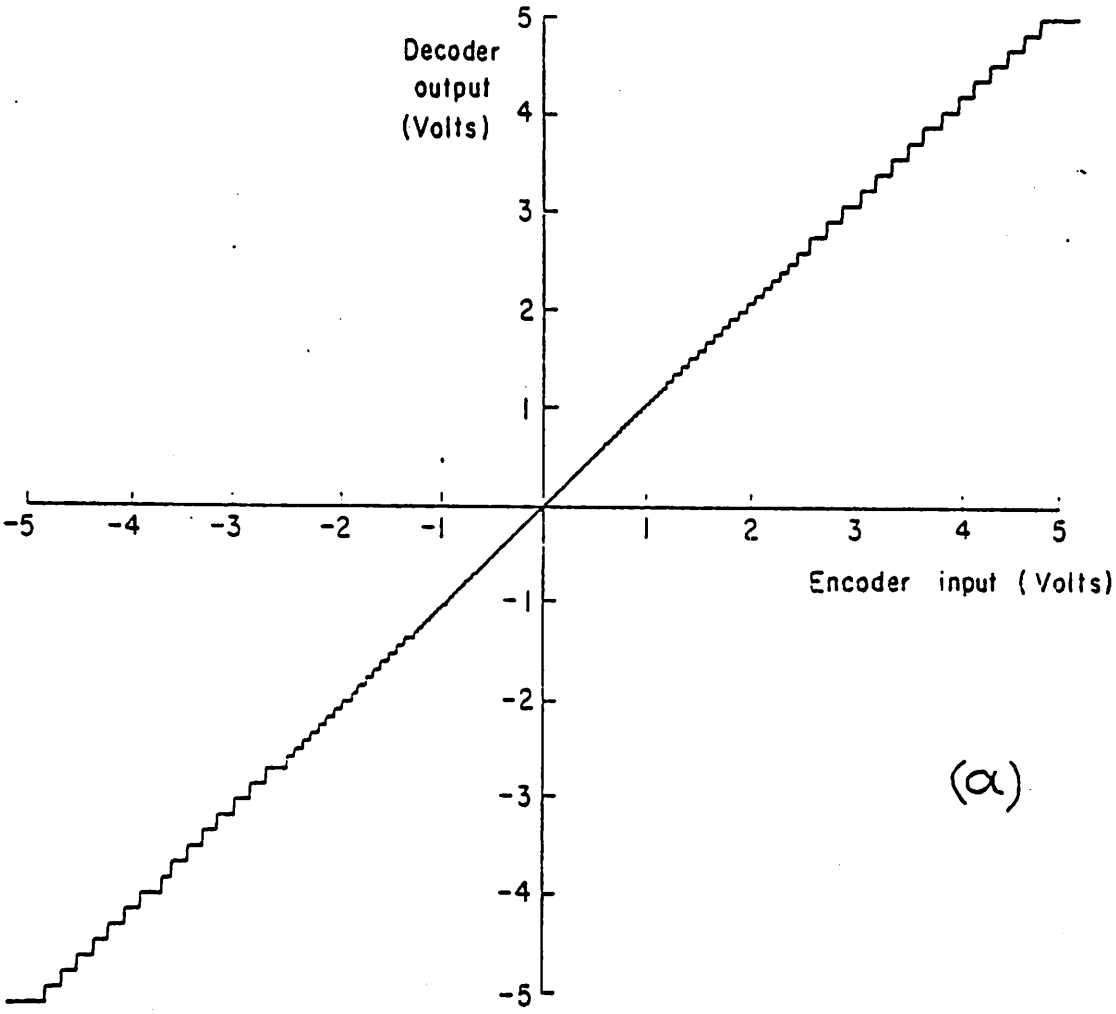
7.5.1 DC Transfer Characteristic

The input-output characteristic of the encoder-decoder combination has been obtained using an x-y plotter as shown in Figure 7.6. The continuity at segment boundaries and the monotonicity claimed in Chapter 4 are apparent.

7.5.2 Signal-to-Distortion Ratio

The signal-to-distortion ratio (S/D) was measured using the setup shown in Figure 7.7. Although this setup measures (S + D)/D rather than S/D, the values of the two ratios are practically equal, the worst case being for the lowest input amplitude measured, in which case the discrepancy is still less than 0.5 db. An 1.02 KHz input sinusoid and a C- message weighting filter are used, as required by the D3 channel bank specification

The signal-to-distortion ratio versus input amplitude is shown in Figure 7.8. The reader is cautioned that the overload point is here denoted by 0 db, and all other amplitudes refer to that. In the D3 specifications, +3 dbm is used for the overload point. The computer simulated performance of an ideal codec and the D3 specification bound are also shown for comparison.



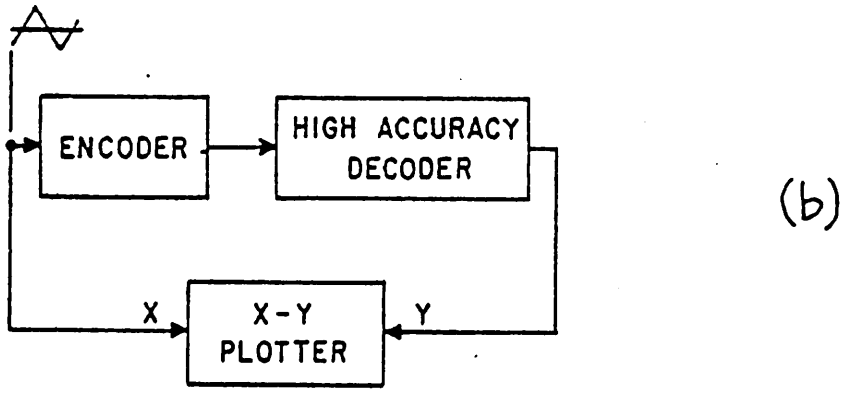


Figure 7.6: (a) DC transfer characteristic of the codec.
(b) Measurement setup.

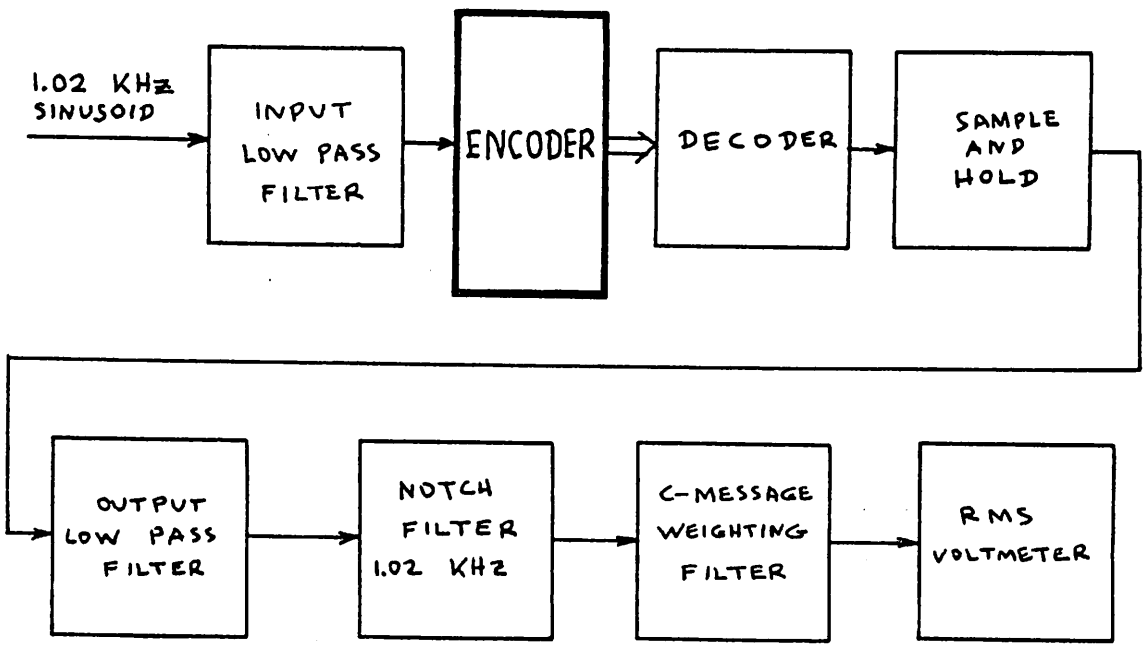


Figure 7.7: Setup for measuring signal-to-distortion ratio.

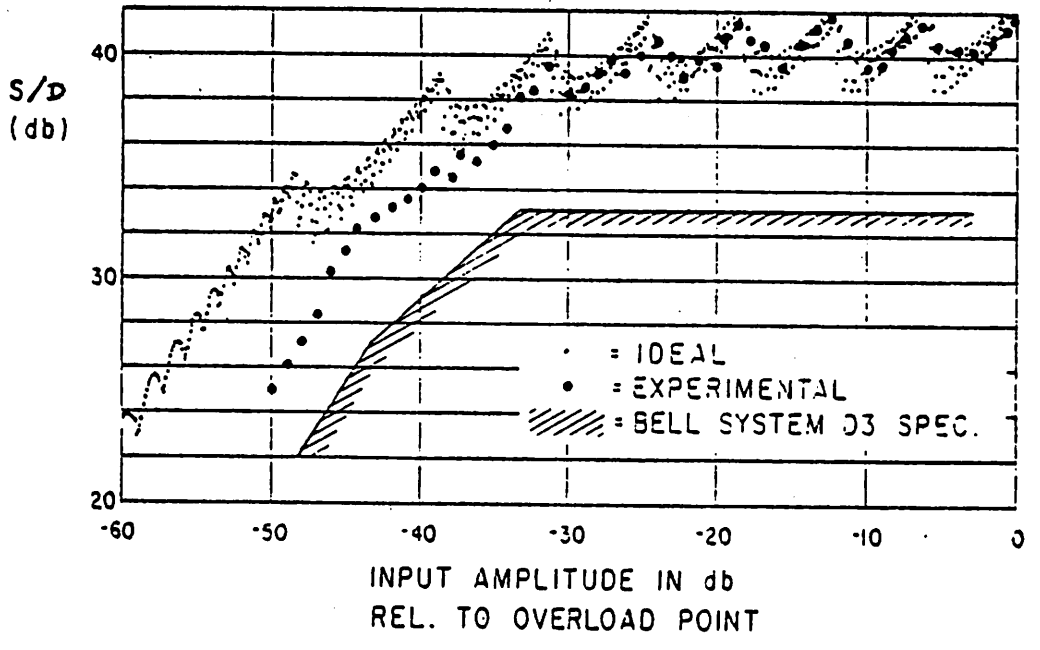


Figure 7.8: Signal-to-distortion ratio versus input amplitude.

As mentioned in section 7.4, the frequency response of the system drops within the passband due to the presence of the sample-and-hold circuit. This will tend to make the S/D measurement slightly optimistic. To estimate this effect, assume that the distortion spectrum is flat over the passband, an assumption practically justified from the considerations in Chapter 2. The effect of the sample-and-hold circuit on the signal-to-noise ratio has been evaluated in that chapter and is given by equation (2.30). For a passband of 3.4 KHz this equation gives an improvement of only 0.37 db for the S/D. The presence of the sample-and-hold circuit can therefore be ignored in interpreting the results of Figure 7.8.

It is seen that the behavior of the encoder is practically ideal for high amplitudes. At low amplitudes, S/D still exceeds the specification bound by a margin sufficient to allow for about 5 db additional degradation by the other components of a practical PCM system.

7.5.3 Idle Channel Noise

Using the setup of Figure 7.7, it was observed that the distortion (or "noise") for input amplitudes less than about -47 db was constant. This is evident in Figure 7.8, where the measured S/D values for these amplitudes lie on a straight line of slope 1 db/db. This constant noise represents idle channel noise. For equal input and output amplitudes, one can obtain its value by reading S/D off the vertical axis of Figure 7.8, and S off the horizontal. This gives an idle channel noise of -75 db relative to the overload point. For an overload point of +3 dbm then, the idle channel noise is -72 dbm, or 18 dbrnc. This is well below the 23 dbrnc allowed by the D3 specification.

7.5.4 Gain Tracking

The measurement setup for gain tracking is shown in Figure 7.9.

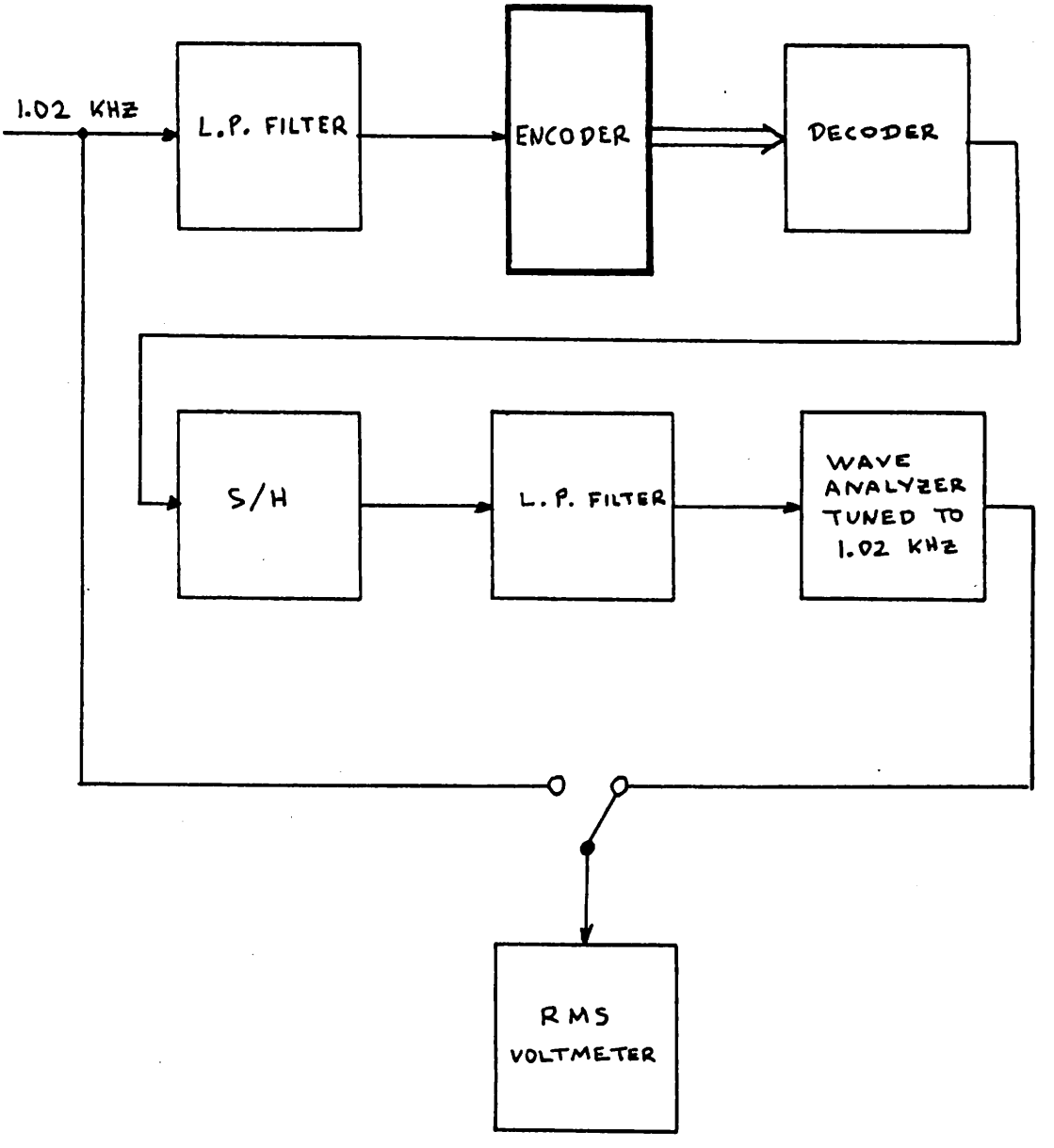


Figure 7.9: Setup for gain tracking measurement.

Since the reference point for gain tracking measurements is set at -3 db relative to overload in the D3 specifications, the input amplitude is first set at -3 db and the overall gain of the system is adjusted so that it is unity at this amplitude. For any other input amplitude then, the gain tracking will be given by the ratio of the amplitude at the wave analyzer output to that at the input, according to the definition in section 2.3.11. The results are shown in Figure 7.10, along with the D3 specification bounds.

7.5.5 Output Spectra and Single Frequency Distortion

The output spectrum was observed on a spectrum analyzer connected to the output of the system of Figure 7.5. For a sinusoidal input of frequency 1.02 KHz and an amplitude of -3 db relative to overload, the output spectrum is shown in Figure 7.11(a). The vertical scale is in db relative to the amplitude of the fundamental. It is seen that all distortion components are at -44 db or less. The D3 specification upper bound in this case is -40 db for components in the band of 0 to 4 KHz ("Single frequency distortion" specification). Figure 7.11(b) is the output spectrum under the same conditions, extended to 200 KHz. Outside the output filter passband, the only significant components occur at the sum and difference between multiples of the sampling frequency and the input frequency. These components would be present even if sampling without quantizing was used, and their reduction relies on the out-of-band rejection of the output filter.

The output spectra for any other input frequency have distortion components which are at -42 db relative to the fundamental or lower. This is well below the D3 specification upper bound of -28 db. Two cases are shown in Figures 7.12(a) and (b), for input frequencies of 100 Hz and 3 KHz re-

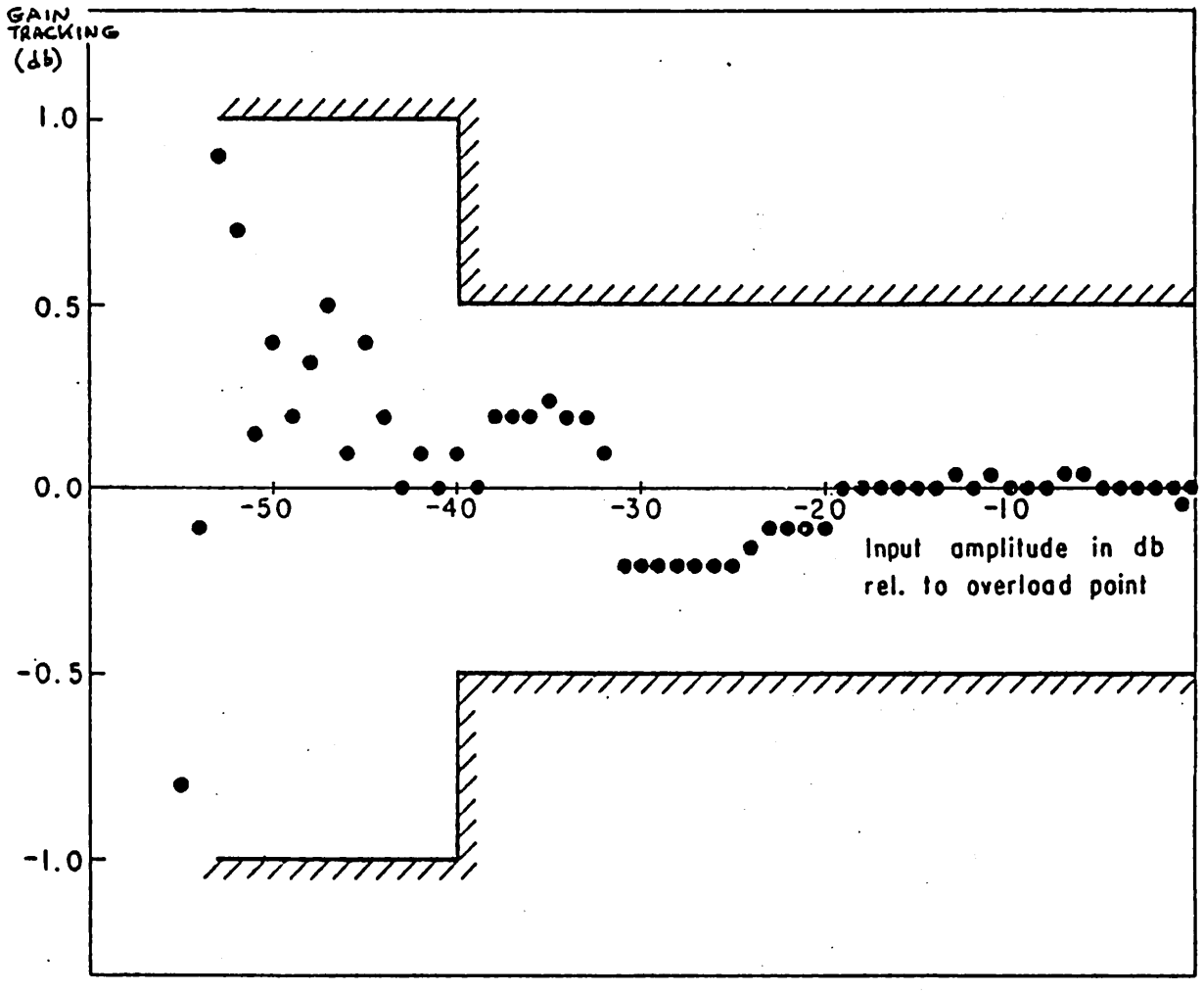


Figure 7.10: Gain tracking versus input amplitude.

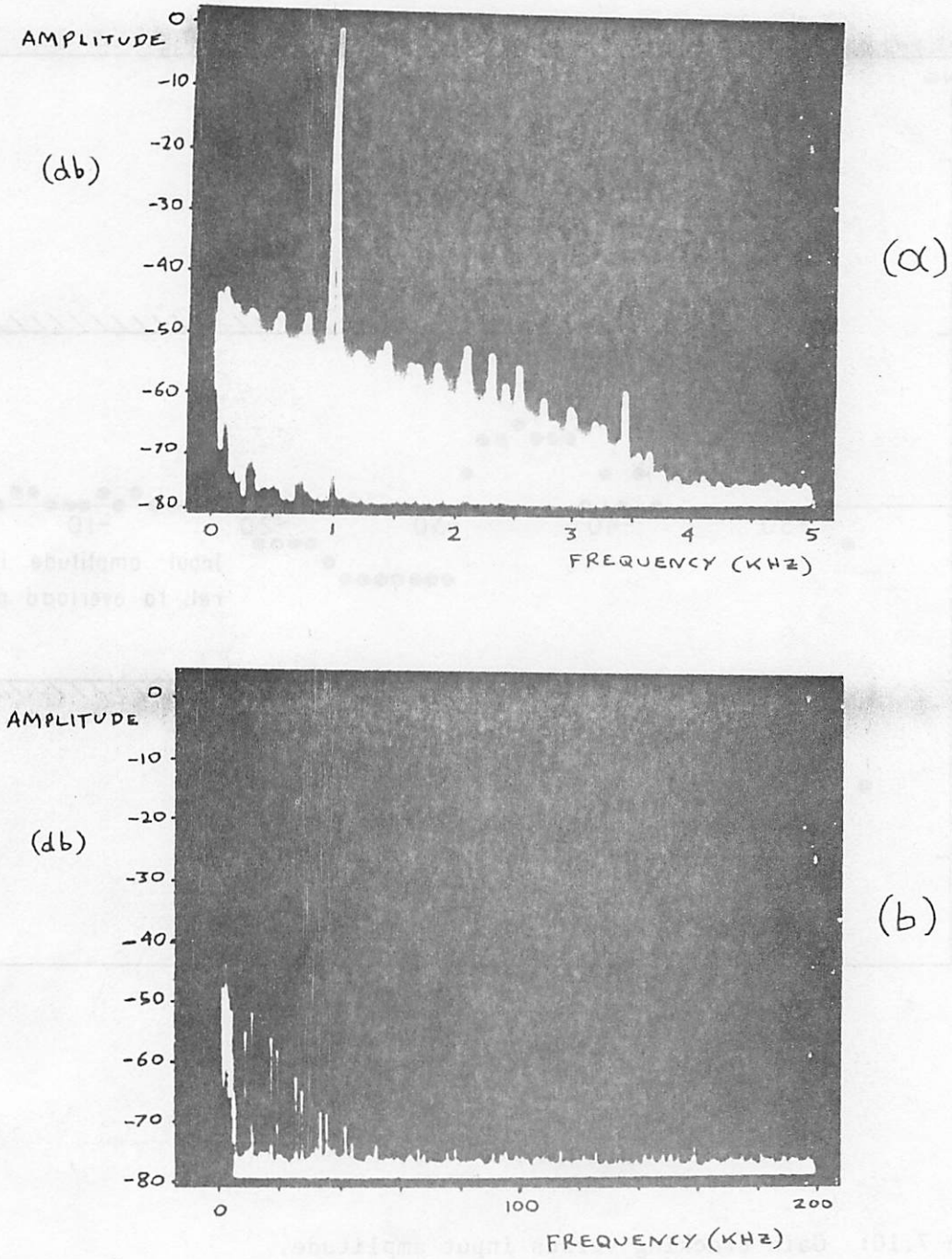


Figure 7.11: Output spectrum for a 1.02 KHz sinusoidal input of amplitude -3db relative to overload.

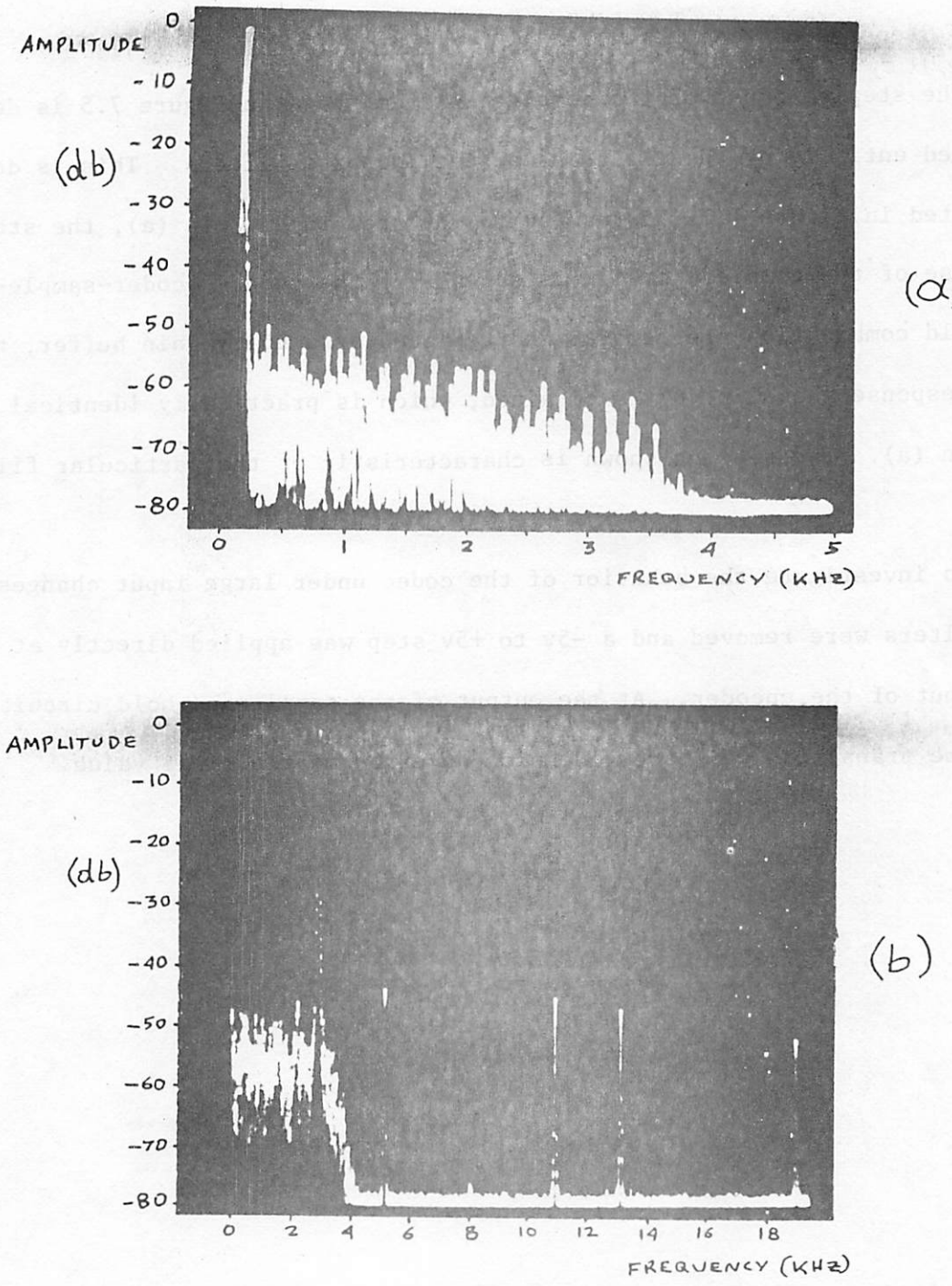


Figure 7.12: Output spectra for an input amplitude of -3db relative to overload.
(a) 100 Hz input.
(b) 3 KHz input.

spectively.

7.5.6 Step response

The step response of the complete system shown in Figure 7.5 is determined entirely by the input and output low-pass filters. This is demonstrated in Figure 7.13, for a -5v to +5v step input. In (a), the step response of the complete system is shown. If the coder-decoder-sample-and-hold combination are removed and replaced by a unity gain buffer, the step response shown in (6) is obtained, which is practically identical to that in (a). The ringing shown is characteristic of the particular filters used.

To investigate the behavior of the codec under large input changes, the filters were removed and a -5v to +5v step was applied directly at the input of the encoder. At the output of the sample-and-hold circuit the same transition was observed, with no error in the final value.

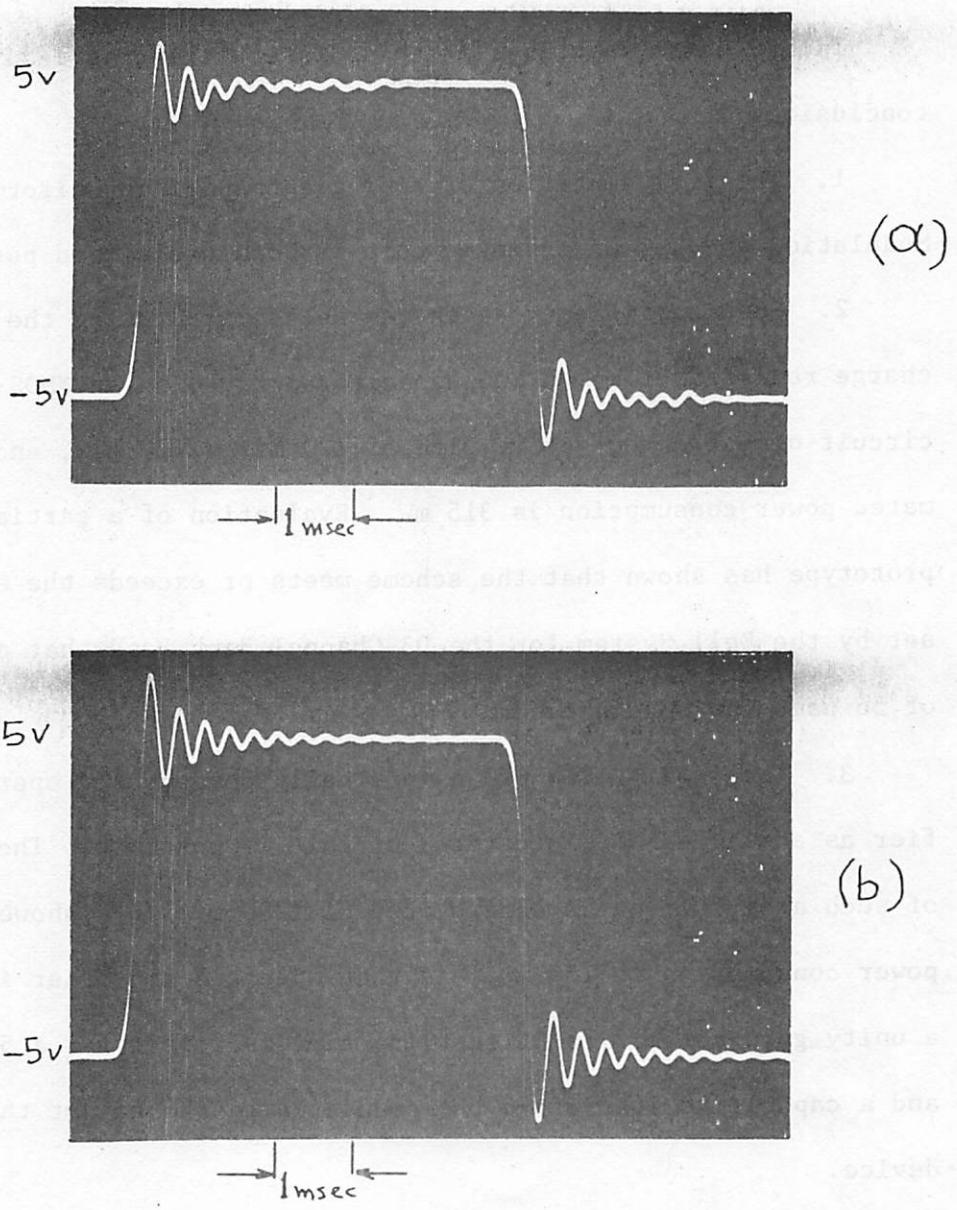


Figure 7.13: (a) Step response of the system in Figure 7.4.
(b) Step response of the filters separated by a buffer.

CHAPTER 8

CONCLUSIONS

The research described in this dissertation has lead to the following conclusions:

1. The implementation of a single-channel nonuniform Pulse Code Modulation encoder on a single chip is both useful and possible.

2. Such an implementation can be realized using the principle of charge redistribution on MOS capacitor arrays, on an NMOS integrated circuit of estimated active size of 120 mil × 120 mil, and whose estimated power consumption is 315 mW. Evaluation of a partially integrated prototype has shown that the scheme meets or exceeds the specifications set by the Bell System for the D3 Channel Bank, and that an encoding time of 56 μsec can be achieved.

3. The realization of an internally compensated operational amplifier as a single NMOS integrated circuit is possible. The fabrication of such a circuit on an active area of 1200 mil^2 has showed that the power consumption is 150 mW, and that when the amplifier is connected as a unity gain buffer its 1% settling time is 2 μsec for a 5 v input step and a capacitive load of 70 pF, connected to the output through a series device.

A P P E N D I X A

XCODEC: A CODEC SIMULATION PROGRAM

A.1 INTRODUCTION

XCODEC is a computer program that evaluates the performance of Non-uniform Pulse-Code Modulation coder-decoder combinations (Codecs), as in Fig. A.1.

The analysis performed is static, in the sense that only the effects of the DC input-output characteristics of the coder and decoder are taken into account. High frequency effects and sampling are not considered.

A.2 PROGRAM OUTPUT

After a particular coder and decoder have been specified, XCODEC generates an output containing the following:

1. Input-output characteristics of the CODEC.

For each possible digital code word, the following are listed:

a) The corresponding decoder output level (v_o).

b) The corresponding lower limit of the coder input range which is coded into that digital word (v_l).

c) The corresponding upper limit (v_u) of that range.

d) The length of that range ($v_u - v_l$).

e) The middle point of the range, $v_m = (v_l + v_u)/2$.

f) The tracking error, $(1 - \frac{v_m}{v_o})$.

2. The performance of the CODEC under sinusoidal excitation.

For each specified input amplitude, the following are listed:

a) The input amplitude in db below full-load.

b) The Signal-to-Distortion ratio (S/D) of the CODEC output (C-message weighting, see section 2.3.15)

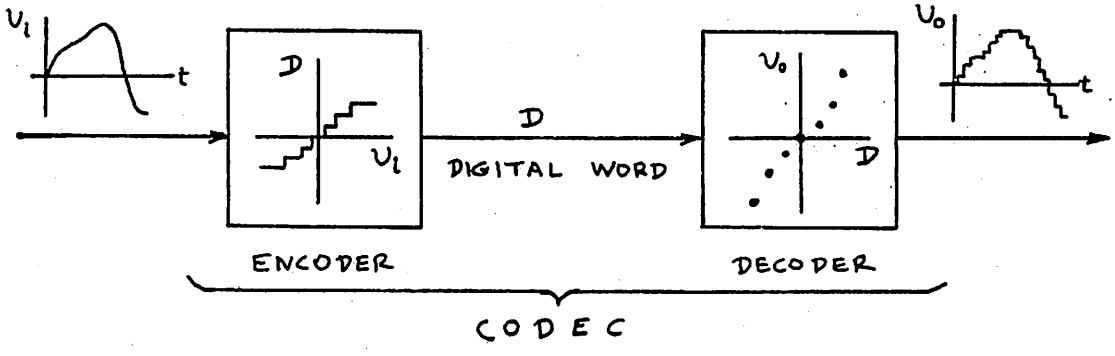


Figure A.1: A nonuniform PCM codec.

c) The Gain tracking in db (see section 2.3.12).

A.3 STRUCTURE OF THE PROGRAM

For convenience, ideal coder and decoder input-output characteristics of the standard 15-segment approximation to the 255-μ law are internally generated by the program. Input/output characteristics of other coders and decoders (e.g., a practical coder under investigation) are specified by the user. Also specified by the user is the full-load voltage of the CODEC. The program then uses that voltage as a reference, and scales the ideal characteristics so that they become compatible with the practical characteristics. For an ideal encoder, the full-load voltage correspond to the end of the last of the sixteen equal steps of the last segment. Input levels in the output of the program appear in db referenced to that full-load voltage.

The structure of the program is summarized in Figure A.2.

A.4 USING THE PROGRAM

Below, the use of XCODEC on the CDC 6400 computer at U. C. Berkeley is described, for the case where IBM cards are used.

A.4.1 Input Deck Format

The deck is of the following standard type:

Control cards

Program

7-8-9 multipunch card

Data cards

6-7-8-9 multipunch card

An input deck example is shown in Figure A.3.

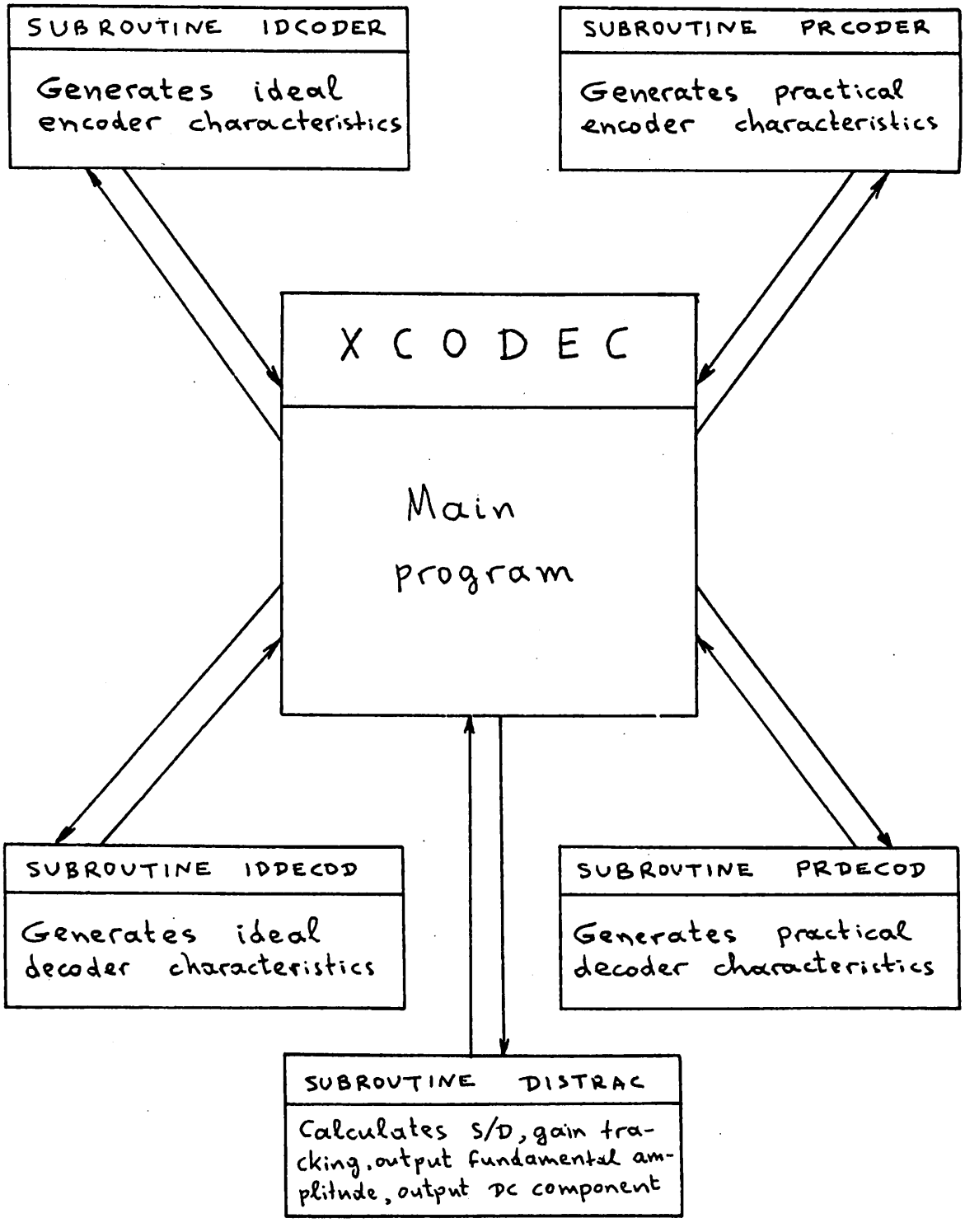


Figure A.2: Program structure.

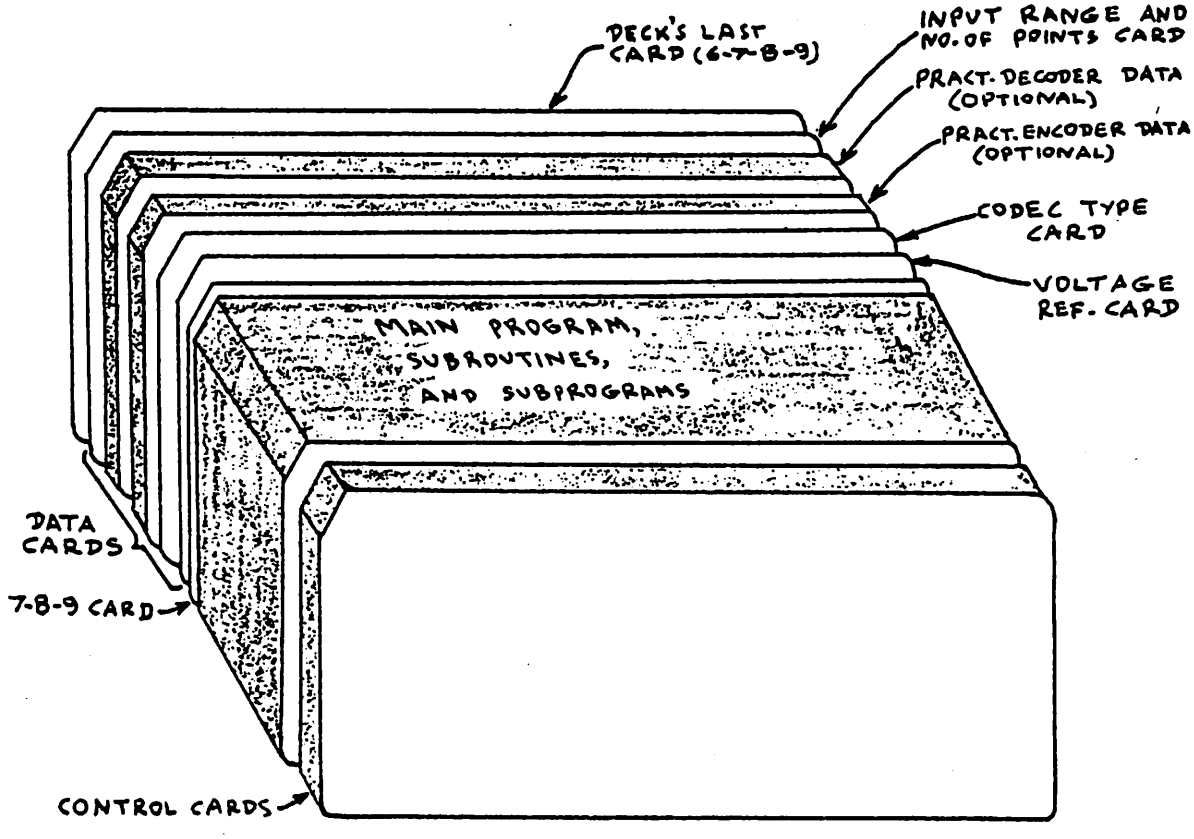


Figure A.3: Input deck.

A.4.2 Data Cards

All input data and output requests are specified through the data cards. Of these data cards, a minimum of three are necessary:

i) Voltage reference card. On this card, the full-load voltage is punched, for the reason described in section A.3. The format shown in Figure A.4(a) is used.

ii) Codec type card. This is a card with a two-digit number punched in the first two columns. This number is a code for the type of codec to be evaluated, as follows:

CODEC TO BE EVALUATED		NUMBER TO BE PUNCHED
CODER	DECODER	
IDEAL	IDEAL	11
IDEAL	PRACTICAL	12
PRACTICAL	IDEAL	21
PRACTICAL	PRACTICAL	22

The punching format is shown in Figure A.4(b).

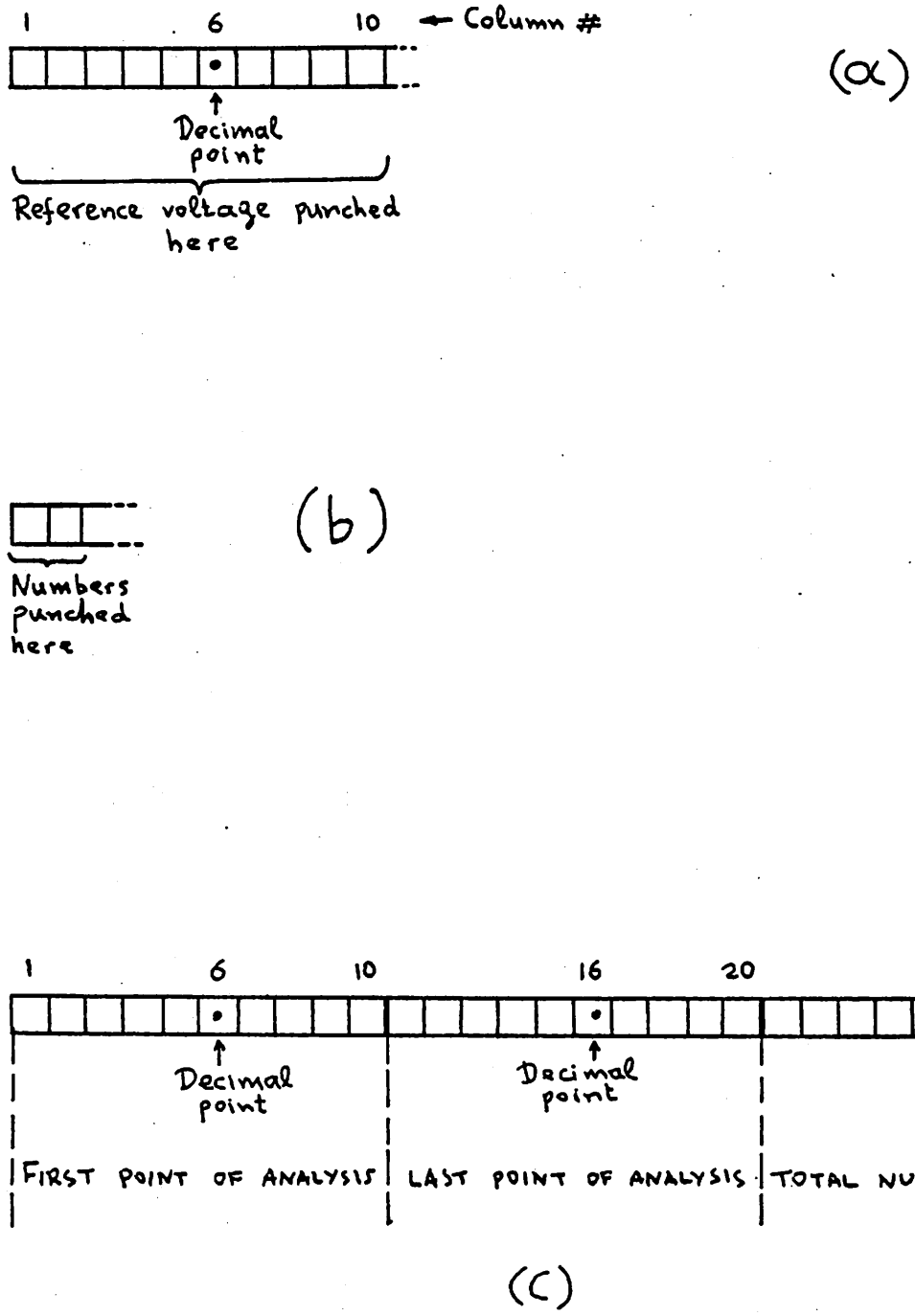


Figure A.4: Punching format for data cards.
(a) "Voltage reference" card.
(b) "Codec type" card.
(c) "Input range and no. of points" card.

More details on this are given in subsection A.4.3.

iii) "Input range and no. of points" card. This card specifies the input amplitudes for which S/D and gain tracking are to be evaluated. Three numbers are punched on this card:

* The first point of the analysis (input amplitude in db referenced to full load).
* The last point of the analysis (input amplitude in db referenced to full load).
* The total number of points.

The punching format is as shown in Figure A.4(c). Additional cards are not needed in the case where both the coder and the decoder are ideal. However, if the coder and/or the decoder are not ideal, their characteristics will have to be user-specified, and this might require additional data cards. This is described in the next section.

A.4.3 Specifying a Practical Coder or Decoder.

Since it is impossible to foresee what type of practical coder and/or decoder the user has in mind, there is no standard way for entering their characteristics into the program. For this reason complete freedom is given to the user to write his own subroutines in FORTRAN, which will then specify the characteristics of the coder or the decoder. Exactly what has to be specified in these subroutines will become clear after section A.5 is read.

The user might want to specify these characteristics as a set of numbers in the subroutine, or use "Read" statements in the subroutine and read the numbers off additional data cards. These data cards will then have to be placed in the deck in the order shown in the deck example of

Figure A.3. Better yet, the characteristics can be specified in the form of equations in the subroutine, and the various coder or decoder parameters can be introduced as variables in these equations. The values of these variables can then be read from data cards through "Read" statements. Thus, if, say, the subroutine for the practical decoder contains general expressions for the coder output levels, and these expressions are functions of different nonidealities, as, e.g., offset, capacitor mismatch, gain error etc., the values of these nonidealities can be read off data cards. By changing then only these data cards and running the program again, the effect of these nonidealities on the CODEC performance can be evaluated. The names of the subroutines are:

PRCODER (VLO,VUP,XFL) for the practical coder

PRDECOD(VOU,XFL) for the practical decoder

The symbols inside the arguments above will be understood after the section "Notation for input and output levels" is read. Finally, all the matrices used in the above two subroutines will have to be dimensioned with a dimension statement in the subroutine, and, if the computer system being used requires it, another dimension statement in the main program.

A.5 NOTATION FOR INPUT AND OUTPUT LEVELS

The digital output of the coder has the form shown in Figure 2.13(b).

Although one's and zero's are used in practice, in XCODEC integers excluding zero must be used, since integer indices in Fortran must be not less than unity. The following table summarizes the code used in this program:

Sign bit: 1 if it is 1 in the actual digital word (positive level for ideal codecs)

2 if it is 0 in the actual digital word (negative level for ideal codecs)

Segment number — 1 through 8, with 1 denoting the segment closest to the origin.

Step number within a segment — 1 through 16, with 1 denoting the step closest to the origin.

Example. Consider the step indicated by "CD" in Fig. 2.15(a). Any input voltage in the range C...D will be coded into a digital word which, for this program, is represented by:

(1, 5, 8)

The lowest point of the input range C...D, i.e. the input voltage corresponding to point C, is represented by:

VLO(1, 5, 8)

The highest point of C...D, i.e. the one corresponding to point D, is represented by:

VUP(1, 5, 8)

Finally, the output of the decoder which corresponds to the digital word generated by the coder for the above input range, is represented by:

VOU(1, 5, 8)

A complete description of a CODER is done by a set of lower limit points:

VLO(K,L,M)

and a set of upper limit points

VUP(K,L,M)

where:

K is 1 or 2

L 1 8

M 1 16

Similarly, a complete description of a DECODER is done by a set of output levels:

VOU(K,L,M)

where K,L,M are as above. These then are exactly the points that have to be specified in the subroutines for the practical coder and decoder. In SUBROUTINE PRCODER(VLO,VUP,XFL) the points VLO(K,L,M) and VUP(K,L,M) have to be specified, and in SUBROUTINE PRDECOD(VOU,XFL) the points VOU(K,L,M) have to be specified.

In practice, the circuit one is working with might be such that some digital words never occur at the output of the coder. Assume, e.g., that there is no input range for which the word corresponding to (1,6,10) occurs. However, for the purposes of the program VLO(1,6,10) and VUP (1,6,10) still have to be specified. In this case, their values will be equal indicating that VLO(1,6,10) and VUP(1,6,10) have been merged into a single point, and so there is no input range that is coded into the digital word corresponding to (1,6,10).

The last variable in the arguments of PRCODER and PRDECOD is XFL, the "full load voltage" mentioned earlier. Its value has already been read by the main program by the time these subroutines are called, and is passed to the subroutines through their argument.

A.6 COMPLETE EXAMPLE

Let us assume that we want to use XCODEC in the following situation:

a) The full-load voltage XFL is 8 volts.

b) The CODER is ideal (this will normally mean that it can accomodate analog inputs between -8 volts and 8 volts, since our full-load voltage is 8 volts).

c) Assume that we are interested in evaluating the performance of a PRACTICAL DECODER, which is such that it generates output voltages given by the following expressions (determined by analyzing the circuit under investigation).

$$\frac{XFL}{8.0}\left(L - 1 + \frac{M}{16}\right) + Vos \qquad \text{for } K = 1$$

$$-\frac{XFL}{8.0}\left(L - 1 + \frac{M}{16}\right) - Vos \qquad \text{for } K = 2$$

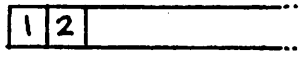
where XFL is the full-load voltage, Vos an offset voltage, and K, L, M are the variables discussed previously in section A.5.

d) We want to evaluate S/D and gain tracking for input amplitudes between -20 and +5 db below full load, at intervals of 1 db. Then:

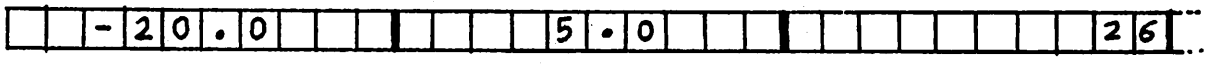
1. From (a) above, the first data card should be as shown in Figure A.5(a).
2. We have an ideal coder and a practical decoder. From the table in subsection A.4.2 it follows that the second data card should be as shown in Figure A.5(b).
3. We now have to describe the practical decoder. For this, we write the following subroutine:

```
SUBROUTINE PRDECOD(VOU,XFL)
DIMENSION VOU(2,  8,  16)
```

(α)



(b)



(c)

Figure A.5: Data cards for the example of section A.6.

```
      READ 801, VOS
801   FORMAT(F10.4)
      DO 802 L = 1,8
      DO 802 M = 1, 16
      WL = FLOAT(L)
      WM = FLOAT(M)
      VOU(1,  L,  M) = (XFL/8.)*(WL - 1. + WM/16.) + VOS
802   VOU(2, L,  M) = - VOU(1, L, M)
      RETURN
      END
```

The subroutine cards are placed in the deck as shown in Figure A.3.

4. In the above subroutine, a card containing the value of the offset VOS is read. This card is placed immediately after the card mentioned in paragraph 2 of this section, as illustrated in the input deck example in Figure A.3. (Here we use an ideal coder, and so no data cards for the coder are needed).

5. Finally, to specify the inputs for which S/D and gain tracking are to be obtained, the last data card should be as shown in Figure A.5(c). The program can now run.

A.7 PROGRAM LISTING

```
      PROGRAM XCODEC(INPUT,OUTPUT)
      ----------------------------
C     THIS PROGRAM EVALUATES THE PERFORMANCE OF COMPANDED PCM CODECS
C     *************************************************************
C
C
C
C
C
C
C
C
C
      DIMENSION VGL(2,8,16),VGL(2,8,16),VGO(2,8,16)
     1          ,VL(2,8,16),VU(2,8,16),VO(2,8,16),XL(512),XU(512),XO(512)
     1                    ,YL(2,8,16),YU(2,8,16),YO(2,8,16)
     1          ,CA(10),COS(20),VBOUT(20),VQ(10),VUP(2,8,16),
     1 VLO(2,8,16),VD(2,8,16),DVP(2,8,16)
      READ 11,XFL
   11 FORMAT(F10.4)
      PRINT 1
    1 FORMAT(10X,115(1H*),//,10X,*P R C G R A M  X C O D E C*,//,
     1 10X,115(1H*),/)
      READ 16,KC,KD
   16 FORMAT(2I1)
      IF (KC.EQ.2) GO TO 12
      CALL IDCODER(VGL,VGU,XFL)
      PRINT 13
   13 FORMAT(10X,*CODER.........IDEAL(A=0.5,B=0.5,C=0.0)*)
      GO TO 17
   12 CALL PRCODER(VGL,VGU,XFL)
      PRINT 18
   18 FORMAT(10X,*CODER.........PRACTICAL*)
   17 IF (KD.EQ.2) GO TO 14
      CALL IDDECOD(VGO,XFL)
      PRINT 3
    3 FORMAT(10X,*DECODER........IDEAL(A=0.5,B=0.5,C=0.0)*)
      GO TO 19
   14 CALL PRDECOD(VGO,XFL)
      PRINT 15
   15 FORMAT(10X,*DECODER........PRACTICAL*)
   19 CONTINUE
C
C
C     EVALUATING CODEC INPUT - OUTPUT CHARACTERISTICS
C     -----------------------------------------------
C
      PRINT 4
    4 FORMAT(/,10X,*S= SIGN BIT*,/,10X, *L= ONES COMPLEMENT OF SEGMENT W
     1ORD IN DECIMAL*,/,10X, *V= ONES COMPLCMENT OF STEP WORD IN DECIMAL
     1*,//,10X,86(1H*),//,10X,*S*,4X,
     1*L*,4X,*V*,              4X,*OUTPUT*,5X,*INPUT*,5X,*INPUT*,5X,
```

```
      1*INPUT*,6X,*STEP*,5X,*TRACKING*,/,23X,
     1      2X,*LEVEL*,6X,*LOWER*,5X,*UPPER*,5X,*STEP*,7X,*MIDDLE*,4X,
     1*ERROR*,                                  /,30X,*LIMIT*,5X,*LIMIT*,5X,*SI
     1ZE*,7X,*POINT*,//,10X,80(1H*),/)
      DO 8 KS=1,2
      DO 8 KL=1,8
      DO 8 KV=1,16
      VVGL=VGL(KS,KL,KV)
      VVGU=VGU(KS,KL,KV)
      DVG=VVGU-VVGL
      VGMID=(VVGL+VVGU)/2.0
      VVGO=VGO(KS,KL,KV)
      NS=2-KS
      NL=KL-1
      NV=KV-1
      IF (VVGO.EQ.0.0) GO TO 5
      TRER=1.0-VGMID/VVGO
      PRINT 6,NS,NL,NV,VVGO,VVGL,VVGU,DVG,VGMID,TRER
    6 FORMAT(6X,3I5,5F10.4,2X,E12.2)
      GO TO 8
    5 PRINT 7,NS,NL,NV,VVGC,VVGL,VVGU,DVG,VGMID
    7 FORMAT(6X,3I5,5F10.4,6X,*NOT DFND*)
    8 CONTINUE
C     ----------
C
      PRINT 9
    9 FORMAT(//,10X,120(1H*))
      PRINT 10
   10 FORMAT(1H1)
      PRINT 1
      IF (KC.EQ.1) 21,22
   21 PRINT 17
      GO TO 23
   22 PRINT 18
   23 IF (KD.EQ.1) 24,25
   24 PRINT 3
      GO TO 26
   25 PRINT 15
   26 CALL DISTRAC(VGL,VGU,VGO,XFL)
      STOP
      END
C
C
```

```
      SUBROUTINE DISTRAC(VL,VU,VO,XFL)
C     ----------------------------
C     CALCULATING PERFORMANCE OF CODEC
C
C     ****************************************
C
      DIMENSION VL(2,8,16),VU(2,8,16),VO(2,8,16),XL(512),XU(512),XO(512)
      MM=8
      NN=16
      NT=MM*NN
      NO=2*MM*NN
      NA=NT+1
      PRINT 509,XFL
  509 FORMAT(/,10X,*0 DB REF. IS *, F8.2,* (PEAK,FULL LOAD SINUSOID)*,/)
      PRINT 516
  516 FORMAT(/,10X,96(1H*),//,T19,*INPUT*,T32,*INPUT*,T47,*S/D*,T59,
     1*GAIN*,T72,*OUTPUT*,T87,*OUTPUT*,/,T17,*AMPLITUDE*,T31,*DB ABOVE*,
     2T47,*DB*,T57,*TRACKING*,T70,*FUNDAMENTAL*,T89,*DC*,/,T31,*FULL LOA
     3D*,T44,*C-WEIGHT*,T60,*DB*,T71,*AMPLITUDE*,T86,*COMPONENT*,//,
     4 10X,96(1H*),/)
      PI=3.1415927
C
C     ----------------------------------
C     CALCULATING INPUT AMPLITUDE LEVELS
C     ----------------------------------
C
      READ 521,DBUP,DBLOW,NPA
  521 FORMAT(2F10.4,I10)
      QN=FLOAT(NPA)-1.0
      NPB=NPA+1
      DO 515 LG=1,NPB
      IF (LG.EQ.1) 531,532
  531 XP=XFL*(10.0**(-3.0/20.0))
      GO TO 502
  532 QL=FLOAT(LG)-2.0
      DBIN=DBUP+(DBLOW-DBUP)*(QL/QN)
      XP=XFL*(10.0**(DBIN/20.0))
C
C     ---------------------------
C     CALCULATING EXPECTED VALUES
C     ---------------------------
C
  502 DO 514 KS=1,2
      DO 514 KL=1,MM
      DO 514 KV=1,NN
      I=(KS-1)*MM*NN+(KL-1)*NN+KV
      XU(I)=VU(KS,KL,KV)
      XL(I)=VL(KS,KL,KV)
  514 XO(I)=VO(KS,KL,KV)
C     END POINTS CHANGED BELOW TO SIMULATE SATURATION
      XU(NT)=999999999.0
      XL(NO)=-999999999.0
      X1=0.0
```

```
      X2=0.0
      X3=0.0
      IF (XL(1).GE.XP) GO TO 506
      DO 503 IA=1,NT
      KL1=IA
  503 IF (XL(IA).GT.(-XP)) GO TO 504
  504 DO 505 IB=1,NT
      KU1=IB-1
  505 IF (XU(IB).GT.XP) GO TO 556
  556 IF (KL1.GT.KU1) GO TO 561
      DO 510 K=KL1,KU1
      XA=XINTA(XL(K),XU(K),XP)
      XB=XINTB(XL(K),XU(K),XP)
      XC=XINTC(XL(K),XU(K),XP)
      X1=X1+XO(K)*XA
      X2=X2+(XO(K)**2)*XA
  510 X3=X3+XO(K)*XB
  561 I1=KU1+1
  513 XA=XINTA(XL(I1),XP,XP)
      XB=XINTB(XL(I1),XP,XP)
      XC=XINTC(XL(I1),XP,XP)
      X1=X1+XO(I1)*XA
      X2=X2+(XO(I1)**2)*XA
      X3=X3+XO(I1)*XB
  506 IF (XU(129).LE.(-XP)) GO TO 507
      DO 508 IC=NA,NO
      KU2=IC
  508 IF (XU(IC).LT.XP) GO TO 551
  551 DO 552 ID=NA,NO
      KL2=ID-1
  552 IF (XL(ID).LT.(-XP)) GO TO 557
  557 IF (KU2.GT.KL2) GO TO 562
      DO 512 K=KU2,KL2
      XA=XINTA(XL(K),XU(K),XP)
      XB=XINTB(XL(K),XU(K),XP)
      XC=XINTC(XL(K),XU(K),XP)
      X1=X1+XO(K)*XA
      X2=X2+(XO(K)**2)*XA
  512 X3=X3+XO(K)*XB
  562 I2=KL2+1
  517 XA=XINTA(-XP,XU(I2),XP)
      XB=XINTB(-XP,XU(I2),XP)
      XC=XINTC(-XP,XU(I2),XP)
      X1=X1+XO(I2)*XA
      X2=X2+(XO(I2)**2)*XA
      X3=X3+XO(I2)*XB
C
C     XA1=E(XO), XA2=E(XO**2), XA3=E(XI*XO), XA4=E(XI**2)
C
  507 XA1=X1/PI
      XA2=X2/PI
      XA3=X3/PI
      XA4=(XP**2)/2.0
      IF (LG.EQ.1) 534,535
```

```
  534 GOL=XA3/XA4
      GO TO 515
C
C
C     CALCULATING S/D,GAIN TRACKING,OUTPUT PARAMETERS
C     -----------------------------------------------
C
  535 R=XA1/SQRT(XA4*(XA2-XA1**2))
      G=XA3/XA4
      GTRAC=20.0*ALOG10(G/GOL)
      DOPT=XA1
      XOFUND=G*XP
      SDR=(R**2)/(1.0-R**2)
      SDRDB=10.0*ALOG10(SDR)+2.9
      IF (DBIN.GT.(-3.0)) GO TO 540
      IF ((DBIN.GE.(-33.0)).AND.(SDRDB.LT.33.0)) GO TO 529
      IF ((DBIN.GE.(-43.0)).AND.(SDRDB.LT.27.0)) GO TO 529
      IF ((DBIN.GE.(-48.0)).AND.(SDRDB.LT.22.0)) GO TO 529
  540 IF (DBIN.GT.(0.0)) GO TO 528
      IF ((DBIN.GE.(-40.0)).AND.(ABS(GTRAC).GT.0.5)) GO TO 529
      IF ((DBIN.GE.(-53.0)).AND.(ABS(GTRAC).GT.1.0)) GO TO 529
  528 PRINT 518,XP,DBIN,SDRDB,GTRAC,XOFUND,DOPT
  518 FORMAT(T12,F12.4,T25,F12.2,T39,F12.2,T51,F12.2,T66,F12.4,T82,F12.4
     1)
      GO TO 515
  529 PRINT 527,XP,DBIN,SDRDB,GTRAC,XOFUND,DOPT
  527 FORMAT(T12,F12.4,T25,F12.2,T39,F12.2,T51,F12.2,T66,F12.4,T82,F12.4
     1,5X,*D3 SPECS ARE NOT MET*)
  515 CONTINUE
      PRINT 519
  519 FORMAT(/,10X,96(1H*),/,1H1)
      RETURN
      END
C
C
```

```
      FUNCTION XINTA(YL,YU,YP)
C     ************************
C
      XINTA=ASIN(YU/YP)-ASIN(YL/YP)
      RETURN
      END
C
C
      FUNCTION XINTB(YL,YU,YP)
C     ************************
C
      XINTB=-SQRT(YP**2-YU**2)+SQRT(YP**2-YL**2)
      RETURN
      END
C
C
      FUNCTION XINTC(YL,YU,YP)
C     ************************
C
      XINTC=(YL*SQRT(YP**2-YL**2)-YU*SQRT(YP**2-YU**2)+(YP**2)*(ASIN(YU/
     1YP)-ASIN(YL/YP)))/2.0
      RETURN
      END
C
C
```

```
      SUBROUTINE IDCODER(YL,YU,XFL)
C     -----------------------------
C     EVALUATING IDEAL CODER CHARACTERISTICS(255 MU,A=0.5,B=0.5,C=0.0
C
C     ***************************************************************
C
      DIMENSION YL(2,8,16),YU(2,8,16)
      SCALING=XFL/4079.5
      DO 201 IL=1,8
      DO 201 IV=1,16
      KL=IL-1
      KV=IV-1
      GV=FLOAT(KV)
      YU(1,IL,IV)=((2.0**KL)*(GV+17.0)-16.5)*SCALING
      YL(2,IL,IV)=-YU(1,IL,IV)
      IF (IV.EQ.1) 202,203
  202 IF (IL.EQ.1) 204,205
  204 YL(1,1,1)=0.0
      GO TO 206
  205 YL(1,IL,1)=YU(1,KL,16)
      GO TO 206
  203 YL(1,IL,IV)=YU(1,IL,KV)
  206 YU(2,IL,IV)=-YL(1,IL,IV)
  201 CONTINUE
      RETURN
      END
C
C
      SUBROUTINE IDDECOD(YO,XFL)
C     --------------------------
C
C     EVALUATING IDEAL DECODER CHARACTERISTICS(255 MU,A=0.5,B=0.5,C=0.0
C
C     ***************************************************************
C
      DIMENSION YO(2,8,16)
      SCALING=XFL/4079.5
      DO 301 IL=1,8
      DO 301 IV=1,16
      KL=IL-1
      KV=IV-1
      GV=FLOAT(KV)
      YO(1,IL,IV)=((2.0**KL)*(GV+16.5)-16.5)*SCALING
  301 YO(2,IL,IV)=-YO(1,IL,IV)
      RETURN
      END
C
C
```

SUBROUTINE PRCODER(VLO,VUP,XFL)

In this space, the user is to write his own subroutine to characterize the practical coder under investigation.

SUBROUTINE PRDECOD(VOU,XFL)

In this space, the user is to write his own subroutine to characterize the practical decoder under investigation.

A.8 SAMPLE OUTPUT

The output shown in the next pages was obtained for the situation of an ideal encoder and an ideal decoder for the 15-segment approximation to the 255 μ law. The full load voltage was 5 V. S/D and gain tracking were calculated for 71 different input amplitude values between -60 db and +10 db relative to full load. The effective time for this program was 18.3 sec, and the cost on the CDC 6400 computer at the University of California, Berkeley was $2.20.

****

PROGRAM XCODEC

****

CODER.....IDEAL(A=0.5,B=0.5,C=0.0)
DECODER.....IDEAL(A=0.5,B=0.5,C=0.0)

S= SIGN BIT
L= ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V= ONES COMPLEMENT OF STEP WORD IN DECIMAL

****

S	L	V	OUTPUT LEVEL	INPUT LOWER LIMIT	INPUT UPPER LIMIT	INPUT STEP SIZE	STEP MIDDLE POINT	TRACKING ERROR
1	0	0	0.	0.	.0006	.0006	.0003	NOT DEND
1	0	1	.0012	.0006	.0018	.0012	.0012	0.
1	0	2	.0025	.0018	.0031	.0012	.0025	0.
1	0	3	.0037	.0031	.0043	.0012	.0037	0.
1	0	4	.0049	.0043	.0055	.0012	.0049	0.
1	0	5	.0061	.0055	.0067	.0012	.0061	0.
1	0	6	.0074	.0067	.0080	.0012	.0074	0.
1	0	7	.0086	.0080	.0092	.0012	.0086	0.
1	0	8	.0098	.0092	.0104	.0012	.0098	0.
1	0	9	.0110	.0104	.0116	.0012	.0110	0.
1	0	10	.0123	.0116	.0129	.0012	.0123	0.
1	0	11	.0135	.0129	.0141	.0012	.0135	0.
1	0	12	.0147	.0141	.0153	.0012	.0147	0.
1	0	13	.0159	.0153	.0165	.0012	.0159	.71E-14
1	0	14	.0172	.0165	.0178	.0012	.0172	.71E-14
1	0	15	.0184	.0178	.0190	.0012	.0184	.71E-14
1	1	0	.0202	.0190	.0214	.0025	.0202	0.
1	1	1	.0227	.0214	.0239	.0025	.0227	0.
1	1	2	.0251	.0239	.0264	.0025	.0251	0.
1	1	3	.0276	.0264	.0288	.0025	.0276	0.
1	1	4	.0300	.0288	.0313	.0025	.0300	0.
1	1	5	.0325	.0313	.0337	.0025	.0325	0.
1	1	6	.0349	.0337	.0362	.0025	.0349	0.
1	1	7	.0374	.0362	.0386	.0025	.0374	0.
1	1	8	.0398	.0386	.0411	.0025	.0398	0.
1	1	9	.0423	.0411	.0435	.0025	.0423	0.
1	1	10	.0447	.0435	.0460	.0025	.0447	0.
1	1	11	.0472	.0460	.0484	.0025	.0472	0.
1	1	12	.0496	.0484	.0509	.0025	.0496	0.
1	1	13	.0521	.0509	.0533	.0025	.0521	0.
1	1	14	.0545	.0533	.0558	.0025	.0545	0.
1	1	15	.0570	.0558	.0582	.0025	.0570	0.
1	2	0	.0607	.0582	.0631	.0049	.0607	0.
1	2	1	.0656	.0631	.0680	.0049	.0656	0.
1	2	2	.0705	.0680	.0729	.0049	.0705	0.

1	2	3	.0754	.0729	.0778	.0049	.0754	0.
1	2	4	.0803	.0778	.0827	.0049	.0803	0.
1	2	5	.0852	.0827	.0876	.0049	.0852	0.
1	2	6	.0901	.0876	.0925	.0049	.0901	0.
1	2	7	.0950	.0925	.0974	.0049	.0950	0.
1	2	8	.0999	.0974	.1023	.0049	.0999	0.
1	2	9	.1048	.1023	.1072	.0049	.1048	0.
1	2	10	.1097	.1072	.1121	.0049	.1097	0.
1	2	11	.1146	.1121	.1170	.0049	.1146	0.
1	2	12	.1195	.1170	.1220	.0049	.1195	0.
1	2	13	.1244	.1220	.1269	.0049	.1244	0.
1	2	14	.1293	.1269	.1318	.0049	.1293	0.
1	2	15	.1342	.1318	.1367	.0049	.1342	0.
1	3	0	.1416	.1367	.1465	.0098	.1416	0.
1	3	1	.1514	.1465	.1563	.0098	.1514	0.
1	3	2	.1612	.1563	.1661	.0098	.1612	0.
1	3	3	.1710	.1661	.1759	.0098	.1710	0.
1	3	4	.1808	.1759	.1857	.0098	.1808	0.
1	3	5	.1906	.1857	.1955	.0098	.1906	0.
1	3	6	.2004	.1955	.2053	.0098	.2004	0.
1	3	7	.2102	.2053	.2151	.0098	.2102	0.
1	3	8	.2200	.2151	.2249	.0098	.2200	0.
1	3	9	.2298	.2249	.2347	.0098	.2298	0.
1	3	10	.2396	.2347	.2445	.0098	.2396	0.
1	3	11	.2494	.2445	.2543	.0098	.2494	0.
1	3	12	.2592	.2543	.2641	.0098	.2592	0.
1	3	13	.2690	.2641	.2739	.0098	.2690	0.
1	3	14	.2788	.2739	.2837	.0098	.2788	0.
1	3	15	.2886	.2837	.2935	.0098	.2886	0.
1	4	0	.3033	.2935	.3132	.0196	.3033	.71E-14
1	4	1	.3230	.3132	.3328	.0196	.3230	.71E-14
1	4	2	.3426	.3328	.3524	.0196	.3426	.71E-14
1	4	3	.3622	.3524	.3720	.0196	.3622	.71E-14
1	4	4	.3818	.3720	.3916	.0196	.3818	.71E-14
1	4	5	.4014	.3916	.4112	.0196	.4014	.71E-14
1	4	6	.4210	.4112	.4308	.0196	.4210	.71E-14
1	4	7	.4406	.4308	.4504	.0196	.4406	.71E-14
1	4	8	.4602	.4504	.4700	.0196	.4602	.71E-14
1	4	9	.4798	.4700	.4896	.0196	.4798	.71E-14
1	4	10	.4994	.4896	.5093	.0196	.4994	.71E-14
1	4	11	.5191	.5093	.5289	.0196	.5191	.71E-14
1	4	12	.5387	.5289	.5485	.0196	.5387	0.
1	4	13	.5583	.5485	.5681	.0196	.5583	.71E-14
1	4	14	.5779	.5681	.5877	.0196	.5779	0.
1	4	15	.5975	.5877	.6073	.0196	.5975	.71E-14
1	5	0	.6269	.6073	.6465	.0392	.6269	.71E-14
1	5	1	.6661	.6465	.6857	.0392	.6661	.71E-14
1	5	2	.7054	.6857	.7250	.0392	.7054	.71E-14
1	5	3	.7446	.7250	.7642	.0392	.7446	.71E-14
1	5	4	.7838	.7642	.8034	.0392	.7838	.71E-14
1	5	5	.8230	.8034	.8426	.0392	.8230	.71E-14
1	5	6	.8622	.8426	.8818	.0392	.8622	.71E-14
1	5	7	.9015	.8818	.9211	.0392	.9015	.71E-14
1	5	8	.9407	.9211	.9603	.0392	.9407	.71E-14
1	5	9	.9799	.9603	.9995	.0392	.9799	.71E-14
1	5	10	1.0191	.9995	1.0387	.0392	1.0191	.71E-14

1	5	11	1.0583	1.0387	1.0780	.0392	1.0583	0.
1	5	12	1.0976	1.0780	1.1172	.0392	1.0976	.71E-14
1	5	13	1.1368	1.1172	1.1564	.0392	1.1368	0.
1	5	14	1.1760	1.1564	1.1956	.0392	1.1760	.71E-14
1	5	15	1.2152	1.1956	1.2348	.0392	1.2152	0.
1	6	0	1.2741	1.2348	1.3133	.0784	1.2741	0.
1	6	1	1.3525	1.3133	1.3917	.0784	1.3525	0.
1	6	2	1.4309	1.3917	1.4702	.0784	1.4309	0.
1	6	3	1.5094	1.4702	1.5486	.0784	1.5094	0.
1	6	4	1.5878	1.5486	1.6270	.0784	1.5878	0.
1	6	5	1.6663	1.6270	1.7055	.0784	1.6663	0.
1	6	6	1.7447	1.7055	1.7839	.0784	1.7447	0.
1	6	7	1.8231	1.7839	1.8624	.0784	1.8231	0.
1	6	8	1.9016	1.8624	1.9408	.0784	1.9016	0.
1	6	9	1.9800	1.9408	2.0192	.0784	1.9800	0.
1	6	10	2.0585	2.0192	2.0977	.0784	2.0585	0.
1	6	11	2.1369	2.0977	2.1761	.0784	2.1369	0.
1	6	12	2.2153	2.1761	2.2546	.0784	2.2153	0.
1	6	13	2.2938	2.2546	2.3330	.0784	2.2938	0.
1	6	14	2.3722	2.3330	2.4114	.0784	2.3722	0.
1	6	15	2.4507	2.4114	2.4899	.0784	2.4507	0.
1	7	0	2.5683	2.4899	2.6468	.1569	2.5683	0.
1	7	1	2.7252	2.6468	2.8037	.1569	2.7252	0.
1	7	2	2.8821	2.8037	2.9605	.1569	2.8821	0.
1	7	3	3.0390	2.9605	3.1174	.1569	3.0390	0.
1	7	4	3.1959	3.1174	3.2743	.1569	3.1959	0.
1	7	5	3.3527	3.2743	3.4312	.1569	3.3527	0.
1	7	6	3.5096	3.4312	3.5881	.1569	3.5096	0.
1	7	7	3.6665	3.5881	3.7449	.1569	3.6665	0.
1	7	8	3.8234	3.7449	3.9018	.1569	3.8234	0.
1	7	9	3.9803	3.9018	4.0587	.1569	3.9803	0.
1	7	10	4.1371	4.0587	4.2156	.1569	4.1371	0.
1	7	11	4.2940	4.2156	4.3725	.1569	4.2940	0.
1	7	12	4.4509	4.3725	4.5294	.1569	4.4509	0.
1	7	13	4.6078	4.5294	4.6862	.1569	4.6078	0.
1	7	14	4.7647	4.6862	4.8431	.1569	4.7647	0.
1	7	15	4.9216	4.8431	5.0000	.1569	4.9216	0.
0	0	0	-0.	-.0006	-0.	.0006	-.0003	NOT DEND
0	0	1	-.0012	-.0018	-.0006	.0012	-.0012	0.
0	0	2	-.0025	-.0031	-.0018	.0012	-.0025	0.
0	0	3	-.0037	-.0043	-.0031	.0012	-.0037	0.
0	0	4	-.0049	-.0055	-.0043	.0012	-.0049	0.
0	0	5	-.0061	-.0067	-.0055	.0012	-.0061	0.
0	0	6	-.0074	-.0080	-.0067	.0012	-.0074	0.
0	0	7	-.0086	-.0092	-.0080	.0012	-.0086	0.
0	0	8	-.0098	-.0104	-.0092	.0012	-.0098	0.
0	0	9	-.0110	-.0116	-.0104	.0012	-.0110	0.
0	0	10	-.0123	-.0129	-.0116	.0012	-.0123	0.
0	0	11	-.0135	-.0141	-.0129	.0012	-.0135	0.
0	0	12	-.0147	-.0153	-.0141	.0012	-.0147	0.
0	0	13	-.0159	-.0165	-.0153	.0012	-.0159	.71E-14
0	0	14	-.0172	-.0178	-.0165	.0012	-.0172	.71E-14
0	0	15	-.0184	-.0190	-.0178	.0012	-.0184	.71E-14
0	1	0	-.0202	-.0214	-.0190	.0025	-.0202	0.
0	1	1	-.0227	-.0239	-.0214	.0025	-.0227	0.
0	1	2	-.0251	-.0264	-.0239	.0025	-.0251	0.

0	1	3	-.0276	-.0288	-.0264	.0025	-.0276	0.
0	1	4	-.0300	-.0313	-.0288	.0025	-.0300	0.
0	1	5	-.0325	-.0337	-.0313	.0025	-.0325	0.
0	1	6	-.0349	-.0362	-.0337	.0025	-.0349	0.
0	1	7	-.0374	-.0386	-.0362	.0025	-.0374	0.
0	1	8	-.0398	-.0411	-.0386	.0025	-.0398	0.
0	1	9	-.0423	-.0435	-.0411	.0025	-.0423	0.
0	1	10	-.0447	-.0460	-.0435	.0025	-.0447	0.
0	1	11	-.0472	-.0484	-.0460	.0025	-.0472	0.
0	1	12	-.0496	-.0509	-.0484	.0025	-.0496	0.
0	1	13	-.0521	-.0533	-.0509	.0025	-.0521	0.
0	1	14	-.0545	-.0558	-.0533	.0025	-.0545	0.
0	1	15	-.0570	-.0582	-.0558	.0025	-.0570	0.
0	2	0	-.0607	-.0631	-.0582	.0049	-.0607	0.
0	2	1	-.0656	-.0680	-.0631	.0049	-.0656	0.
0	2	2	-.0705	-.0729	-.0680	.0049	-.0705	0.
0	2	3	-.0754	-.0778	-.0729	.0049	-.0754	0.
0	2	4	-.0803	-.0827	-.0778	.0049	-.0803	0.
0	2	5	-.0852	-.0876	-.0827	.0049	-.0852	0.
0	2	6	-.0901	-.0925	-.0876	.0049	-.0901	0.
0	2	7	-.0950	-.0974	-.0925	.0049	-.0950	0.
0	2	8	-.0999	-.1023	-.0974	.0049	-.0999	0.
0	2	9	-.1048	-.1072	-.1023	.0049	-.1048	0.
0	2	10	-.1097	-.1121	-.1072	.0049	-.1097	0.
0	2	11	-.1146	-.1170	-.1121	.0049	-.1146	0.
0	2	12	-.1195	-.1220	-.1170	.0049	-.1195	0.
0	2	13	-.1244	-.1269	-.1220	.0049	-.1244	0.
0	2	14	-.1293	-.1318	-.1269	.0049	-.1293	0.
0	2	15	-.1342	-.1367	-.1318	.0049	-.1342	0.
0	3	0	-.1416	-.1465	-.1367	.0098	-.1416	0.
0	3	1	-.1514	-.1563	-.1465	.0098	-.1514	0.
0	3	2	-.1612	-.1661	-.1563	.0098	-.1612	0.
0	3	3	-.1710	-.1759	-.1661	.0098	-.1710	0.
0	3	4	-.1808	-.1857	-.1759	.0098	-.1808	0.
0	3	5	-.1906	-.1955	-.1857	.0098	-.1906	0.
0	3	6	-.2004	-.2053	-.1955	.0098	-.2004	0.
0	3	7	-.2102	-.2151	-.2053	.0098	-.2102	0.
0	3	8	-.2200	-.2249	-.2151	.0098	-.2200	0.
0	3	9	-.2298	-.2347	-.2249	.0098	-.2298	0.
0	3	10	-.2396	-.2445	-.2347	.0098	-.2396	0.
0	3	11	-.2494	-.2543	-.2445	.0098	-.2494	0.
0	3	12	-.2592	-.2641	-.2543	.0098	-.2592	0.
0	3	13	-.2690	-.2739	-.2641	.0098	-.2690	0.
0	3	14	-.2788	-.2837	-.2739	.0098	-.2788	0.
0	3	15	-.2886	-.2935	-.2837	.0098	-.2886	0.
0	4	0	-.3033	-.3132	-.2935	.0196	-.3033	.71E-14
0	4	1	-.3230	-.3328	-.3132	.0196	-.3230	.71E-14
0	4	2	-.3426	-.3524	-.3328	.0196	-.3426	.71E-14
0	4	3	-.3622	-.3720	-.3524	.0196	-.3622	.71E-14
0	4	4	-.3818	-.3916	-.3720	.0196	-.3818	.71E-14
0	4	5	-.4014	-.4112	-.3916	.0196	-.4014	.71E-14
0	4	6	-.4210	-.4308	-.4112	.0196	-.4210	.71E-14
0	4	7	-.4406	-.4504	-.4308	.0196	-.4406	.71E-14
0	4	8	-.4602	-.4700	-.4504	.0196	-.4602	.71E-14
0	4	9	-.4798	-.4896	-.4700	.0196	-.4798	.71E-14
0	4	10	-.4994	-.5093	-.4896	.0196	-.4994	.71E-14

0	4	11	-.5191	-.5289	-.5093	.0196	-.5191	.71E-14
0	4	12	-.5387	-.5485	-.5289	.0196	-.5387	0.
0	4	13	-.5583	-.5681	-.5485	.0196	-.5583	.71E-14
0	4	14	-.5779	-.5877	-.5681	.0196	-.5779	0.
0	4	15	-.5975	-.6073	-.5877	.0196	-.5975	.71E-14
0	5	0	-.6269	-.6465	-.6073	.0392	-.6269	.71E-14
0	5	1	-.6661	-.6857	-.6465	.0392	-.6661	.71E-14
0	5	2	-.7054	-.7250	-.6857	.0392	-.7054	.71E-14
0	5	3	-.7446	-.7642	-.7250	.0392	-.7446	.71E-14
0	5	4	-.7838	-.8034	-.7642	.0392	-.7838	.71E-14
0	5	5	-.8230	-.8426	-.8034	.0392	-.8230	.71E-14
0	5	6	-.8622	-.8818	-.8426	.0392	-.8622	.71E-14
0	5	7	-.9015	-.9211	-.8818	.0392	-.9015	.71E-14
0	5	8	-.9407	-.9603	-.9211	.0392	-.9407	.71E-14
0	5	9	-.9799	-.9995	-.9603	.0392	-.9799	.71E-14
0	5	10	-1.0191	-1.0387	-.9995	.0392	-1.0191	.71E-14
0	5	11	-1.0583	-1.0780	-1.0387	.0392	-1.0583	0.
0	5	12	-1.0976	-1.1172	-1.0780	.0392	-1.0976	.71E-14
0	5	13	-1.1368	-1.1564	-1.1172	.0392	-1.1368	0.
0	5	14	-1.1760	-1.1956	-1.1564	.0392	-1.1760	.71E-14
0	5	15	-1.2152	-1.2348	-1.1956	.0392	-1.2152	0.
0	6	0	-1.2741	-1.3133	-1.2348	.0784	-1.2741	0.
0	6	1	-1.3525	-1.3917	-1.3133	.0784	-1.3525	0.
0	6	2	-1.4309	-1.4702	-1.3917	.0784	-1.4309	0.
0	6	3	-1.5094	-1.5486	-1.4702	.0784	-1.5094	0.
0	6	4	-1.5878	-1.6270	-1.5486	.0784	-1.5878	0.
0	6	5	-1.6663	-1.7055	-1.6270	.0784	-1.6663	0.
0	6	6	-1.7447	-1.7839	-1.7055	.0784	-1.7447	0.
0	6	7	-1.8231	-1.8624	-1.7839	.0784	-1.8231	0.
0	6	8	-1.9016	-1.9408	-1.8624	.0784	-1.9016	0.
0	6	9	-1.9800	-2.0192	-1.9408	.0784	-1.9800	0.
0	6	10	-2.0585	-2.0977	-2.0192	.0784	-2.0585	0.
0	6	11	-2.1369	-2.1761	-2.0977	.0784	-2.1369	0.
0	6	12	-2.2153	-2.2546	-2.1761	.0784	-2.2153	0.
0	6	13	-2.2938	-2.3330	-2.2546	.0784	-2.2938	0.
0	6	14	-2.3722	-2.4114	-2.3330	.0784	-2.3722	0.
0	6	15	-2.4507	-2.4899	-2.4114	.0784	-2.4507	0.
0	7	0	-2.5683	-2.6468	-2.4899	.1569	-2.5683	0.
0	7	1	-2.7252	-2.8037	-2.6468	.1569	-2.7252	0.
0	7	2	-2.8821	-2.9605	-2.8037	.1569	-2.8821	0.
0	7	3	-3.0390	-3.1174	-2.9605	.1569	-3.0390	0.
0	7	4	-3.1959	-3.2743	-3.1174	.1569	-3.1959	0.
0	7	5	-3.3527	-3.4312	-3.2743	.1569	-3.3527	0.
0	7	6	-3.5096	-3.5881	-3.4312	.1569	-3.5096	0.
0	7	7	-3.6665	-3.7449	-3.5881	.1569	-3.6665	0.
0	7	8	-3.8234	-3.9018	-3.7449	.1569	-3.8234	0.
0	7	9	-3.9803	-4.0587	-3.9018	.1569	-3.9803	0.
0	7	10	-4.1371	-4.2156	-4.0587	.1569	-4.1371	0.
0	7	11	-4.2940	-4.3725	-4.2156	.1569	-4.2940	0.
0	7	12	-4.4509	-4.5294	-4.3725	.1569	-4.4509	0.
0	7	13	-4.6078	-4.6862	-4.5294	.1569	-4.6078	0.
0	7	14	-4.7647	-4.8431	-4.6862	.1569	-4.7647	0.
0	7	15	-4.9216	-5.0000	-4.8431	.1569	-4.9216	0.

****

****

P R C G R A M X C O D E C

****

CODER.....IDEAL(A=0.5,B=0.5,C=0.0)
DECODER.....IDEAL(A=0.5,B=0.5,C=0.0)

0 DB REF. IS 5.00 (PEAK,FULL LOAD SINUSOID)

****

INPUT AMPLITUDE	INPUT DB ABOVE FULL LOAD	S/D DB C-WEIGHT	GAIN TRACKING DB	OUTPUT FUNDAMENTAL AMPLITUDE	OUTPUT DC COMPONENT
.0050	-60.00	23.72	.06	.0050	-.0000
.0056	-59.00	23.08	.02	.0056	-.0000
.0063	-58.00	25.63	.01	.0063	-.0000
.0071	-57.00	25.78	.10	.0071	-.0000
.0079	-56.00	26.78	-.17	.0078	-.0000
.0089	-55.00	28.39	-.04	.0089	-.0000
.0100	-54.00	29.46	.01	.0100	-.0000
.0112	-53.00	30.43	.01	.0112	-.0000
.0126	-52.00	31.33	-.02	.0125	-.0000
.0141	-51.00	31.67	-.08	.0140	-.0000
.0158	-50.00	33.07	.03	.0159	-.0000
.0177	-49.00	33.76	-.05	.0176	-.0000
.0199	-48.00	33.71	.09	.0201	-.0000
.0223	-47.00	33.09	.07	.0225	-.0000
.0251	-46.00	33.81	.04	.0252	-.0000
.0281	-45.00	34.47	-.01	.0281	-.0000
.0315	-44.00	33.83	.02	.0316	-.0000
.0354	-43.00	35.81	-.00	.0354	-.0000
.0397	-42.00	36.36	.02	.0398	-.0000
.0446	-41.00	37.13	.02	.0446	-.0000
.0500	-40.00	38.20	.00	.0500	-.0000
.0561	-39.00	38.26	.01	.0562	-.0000
.0629	-38.00	36.53	-.05	.0626	-.0000
.0706	-37.00	37.58	.02	.0708	-.0000
.0792	-36.00	37.11	.03	.0795	-.0000
.0889	-35.00	37.62	.02	.0891	-.0000
.0998	-34.00	38.87	.01	.0999	-.0000
.1119	-33.00	39.18	-.02	.1116	-.0000
.1256	-32.00	40.46	-.00	.1255	-.0000
.1409	-31.00	39.87	.04	.1415	-.0000
.1581	-30.00	37.67	.02	.1585	-.0000
.1774	-29.00	37.93	.02	.1777	-.0000
.1991	-28.00	39.15	.02	.1994	-.0000
.2233	-27.00	39.96	-.01	.2230	-.0000
.2506	-26.00	40.87	.00	.2507	-.0000

.2812	-25.00	41.56	-.00	.2811	-.0000
.3155	-24.00	38.13	.02	.3161	-.0000
.3540	-23.00	38.14	.01	.3542	-.0000
.3972	-22.00	39.20	.02	.3980	-.0000
.4456	-21.00	40.39	-.00	.4453	-.0000
.5000	-20.00	40.98	.01	.5004	-.0000
.5610	-19.00	41.75	.00	.5611	-.0000
.6295	-18.00	41.31	.02	.6309	-.0000
.7063	-17.00	40.01	.02	.7075	-.0000
.7924	-16.00	40.17	-.00	.7921	-.0000
.8891	-15.00	39.61	.01	.8904	-.0000
.9976	-14.00	40.58	-.02	.9953	-.0000
1.1194	-13.00	40.90	.00	1.1193	-.0000
1.2559	-12.00	40.33	.04	1.2612	-.0000
1.4092	-11.00	38.97	.02	1.4127	-.0000
1.5811	-10.00	39.91	.02	1.5841	-.0000
1.7741	-9.00	40.29	-.02	1.7708	-.0000
1.9905	-8.00	41.22	.00	1.9910	-.0000
2.2334	-7.00	41.83	-.00	2.2326	-.0000
2.5059	-6.00	39.84	.03	2.5138	-.0000
2.8117	-5.00	38.55	.00	2.8118	-.0000
3.1548	-4.00	39.33	.02	3.1613	-.0000
3.5397	-3.00	40.70	-.00	3.5393	-.0000
3.9716	-2.00	41.00	.01	3.9763	-.0000
4.4563	-1.00	41.80	.01	4.4592	-.0000
5.0000	-.00	41.94	-.02	4.9899	-.0000
5.6101	1.00	28.31	-.45	5.3265	-.0000
6.2946	2.00	23.01	-1.09	5.5509	-.0000
7.0627	3.00	20.02	-1.84	5.7140	-.0000
7.9245	4.00	18.02	-2.66	5.8364	-.0000
8.8914	5.00	16.56	-3.52	5.9299	-.0000
9.9763	6.00	15.43	-4.41	6.0021	-.0000
11.1936	7.00	14.54	-5.33	6.0582	-.0000
12.5594	8.00	13.80	-6.27	6.1021	-.0000
14.0919	9.00	13.20	-7.22	6.1366	-.0000
15.8114	10.00	12.69	-8.18	6.1637	-.0000

****

APPENDIX B

PRACTICAL ENCODER SIMULATION

B.1 PRACTICAL ENCODER SUBROUTINE LISTING

The subroutine "PRCODER", used to develop the decision level of the charge redistribution encoder proposed in Chapter 4, is given in this section. The inputs to the subroutine are the capacitor values for the two arrays, the parasitic capacitances, the reference voltages, the comparator offset, the buffer offset, the buffer gain, and the values of the capacitors and voltage sources of the scheme in Figure 4.8(a).

```
      SUBROUTINE PRCODER(VLO,VUP,XFL)
C     ---------------------------
C     EVALUATING PRACTICAL CODER CHARACTERISTICS
C
C     ******************************************
C
      DIMENSION CA(10),CBS(20),VBOUT(20),VO(10),VUP(2,8,16),
     1 VLO(2,8,16),VO(2,8,16),DVP(2,8,16)
      READ 401,(CA(J),J=1,5)
      READ 401,(CA(J),J=6,9),CAP
  401 FORMAT(5F10.4)
      READ 430,CB1,CB2,CB3,CB4,CB5,CBP
  430 FORMAT(6F10.4)
      READ 402,VRP,VRN,VAHP,VAHN,VAOS,VBOS,GB
  402 FORMAT(7F10.4)
C
C
C     CONSTRUCTING CIRCUIT VALUES SUMMARY
C     -----------------------------------
C
      CAT=CA(1)+CA(2)+CA(3)+CA(4)+CA(5)+CA(6)+CA(7)+CA(8)+CA(9)+CAP
      CBT=CB1+CB2+CB3+CB4+CB5+CBP
      CBS(1)=CB4
      CBS(2)=CB3
      CBS(3)=CB3+CB4
      CBS(4)=CB2
      CBS(5)=CB2+CB4
      CBS(6)=CB2+CB3
      CBS(7)=CB2+CB3+CB4
      CBS(8)=CB1
      DO 403 K=9,15
  403 CBS(K)=CB1+CBS(K-8)
      CAM=CAT-CAP-CA(9)
      PRINT 423
  423 FORMAT(10X,*PRACTICAL CODER CHARACTERISTICS*,//,10X,30(1H*),/)
      DO 432 L=1,9
  433 FORMAT(10X,*CA(*,I1,*)=*,F8.4)
  432 PRINT 433,L,CA(L)
      PRINT 434,CAP,CAT,CAM
  434 FORMAT(10X,*CAP   =*,F8.4,/,10X,*CAT   =*,F8.4,/,10X,*CAM   =*,F8.4)
      PRINT 435,CB1,CB2,CB3,CB4,CB5,CBP,CBT
  435 FORMAT(/,10X,*CB1=*,F8.4,/,10X,*CB2=*,F8.4,/,10X,*CB3=*,F8.4,/,10X
     1,*CB4=*,F8.4,/,10X,*CB5=*,F8.4,/,10X,*CBP=*,F8.4,/,10X,*CBT=*,F8.4
     1 ,/)
      PRINT 436,VRP,VRN,VAHP,VAHN,VAOS,VBOS,GB
  436 FORMAT(10X,*VRP=*,F10.4,/,10X,*VRN=*,F10.4,/,10X,*VAHP=*,F10.4,/,
     110X,*VAHN=*,F10.4,/,10X,*VAOS=*,F10.4,/,10X,*VBOS=*,F10.4,/,10X,
     1 *GB=*,F10.4,/)
C
C
C     EVALUATING H-ARRAY OUTPUT LEVELS
C     --------------------------------
C
```

```
      DO 422 IS=1,2
      KS=2-IS
      IF (KS.EQ.1) 404,405
  404 VR=VRP
      VAH=VAHP
      GO TO 406
  405 VR=VRN
      VAH=VAHN
  406 F=VR/CAM
      PRINT 438,KS
  438 FORMAT(/,10X,*S = *,I2,/,10X,8(1H*))
      DO 407 NV=1,15
      VBOUT(NV)=GB*(VR*(CBS(NV)/CBT)-VBOS)
      PRINT 437,NV,VBOUT(NV)
  437 FORMAT(10X,*VBOUT(*,I2,*)=*,F10.4)
  407 CONTINUE
C
C
C     EVALUATING INPUT STEP LIMIT POINTS
C     ----------------------------------
C
      VBOUT(16)=VR
      VQ(1)=(VAH*CA(9)-VAOS*CAT)/CAM
      DO 408 NL=2,8
  408 VQ(NL)=VQ(NL-1)+F*CA(10-NL)
      VQ(9)=VR
      DO 409 ML=1,8
      DO 409 MV=1,16
      VD(IS,ML,MV)=VQ(ML)+(VBOUT(MV)*CA(9-ML))/CAM
      IF ((IS.EQ.1).AND.(VD(IS,ML,MV).GT.VQ(ML+1))) VD(1,ML,MV)=VQ(ML+1)
      IF ((IS.EQ.2).AND.(VD(IS,ML,MV).LT.VQ(ML+1))) VD(2,ML,MV)=VQ(ML+1)
  409 CONTINUE
      IF (KS.EQ.1) 415,416
  415 DO 414 KL=1,8
      DO 414 KV=1,16
      VUP(1,KL,KV)=VD(1,KL,KV)
      IF ((KL.EQ.1).AND.(KV.EQ.1)) 410,411
  410 VLO(1,1,1)=VQ(1)
      GO TO 414
  411 IF (KV.EQ.1) 412,413
  412 VLO(1,KL,1)=VD(1,KL-1,16)
      GO TO 414
  413 VLO(1,KL,KV)=VD(1,KL,KV-1)
  414 CONTINUE
      GO TO 422
  416 DO 417 KL=1,8
      DO 417 KV=1,16
      VLU(2,KL,KV)=VD(2,KL,KV)
      IF ((KL.EQ.1).AND.(KV.EQ.1)) 418,419
  418 VUP(2,1,1)=VQ(1)
      GO TO 417
  419 IF (KV.EQ.1) 420,421
  420 VUP(2,KL,1)=VD(2,KL-1,16)
      GO TO 417
  421 VUP(2,KL,KV)=VD(2,KL,KV-1)
```

```
417 CONTINUE
422 CONTINUE
    VLO(1,1,1)=-VAUS*CAT/CAM
    VUP(2,1,1)=-VAUS*CAT/CAM
    PRINT 441
441 FORMAT(/,10X,40(1H*),/)
    RETURN
    END
```

B.2 SAMPLE OUTPUT

A sample output obtained using the subroutine given in the previous section, in conjunction with the main program, described in Appendix A, is given in this section. The circuit parameter values are summarized in the beginning of the listing.

```
**********************************************************************

P R O G R A M   X C O D E C

**********************************************************************

PRACTICAL CODER CHARACTERISTICS

*******************************

CA(1)=128.0000
CA(2)= 64.0000
CA(3)= 32.0000
CA(4)= 16.0000
CA(5)=  8.0000
CA(6)=  4.0000
CA(7)=  2.0000
CA(8)=  1.0000
CA(9)=  0.
CAP   = 10.0000
CAT   =265.0000
CAM   =255.0000

CB1=128.0000
CB2= 64.0000
CB3= 32.0000
CB4= 16.0000
CB5, 16.0000
CBP= 10.0000
CBT=266.0000

VRP=    10.0000
VRN=   -10.0000
VAHP=      0.
VAHN=      0.
VAOS=       .0100
VHOS=       .3000
GB=         .9700

S =  1
*********
VHOUT( 1)=      .2925
VHOUT( 2)=      .8759
VHOUT( 3)=     1.4594
VHOUT( 4)=     2.0428
VHOUT( 5)=     2.6263
VHOUT( 6)=     3.2098
VHOUT( 7)=     3.7932
VHOUT( 8)=     4.3767
VHOUT( 9)=     4.9601
VHOUT(10)=     5.5436
VHOUT(11)=     6.1270
VHOUT(12)=     6.7105
VHOUT(13)=     7.2940
VHOUT(14)=     7.8774
```

```
VBOUT(15)=     8.4609

S =  0
********
VBOUT( 1)=     -.8745
VBOUT( 2)=    -1.4579
VBOUT( 3)=    -2.0414
VBOUT( 4)=    -2.6248
VBOUT( 5)=    -3.2083
VBOUT( 6)=    -3.7918
VBOUT( 7)=    -4.3752
VBOUT( 8)=    -4.9587
VBOUT( 9)=    -5.5421
VBOUT(10)=    -6.1256
VBOUT(11)=    -6.7090
VBOUT(12)=    -7.2925
VBOUT(13)=    -7.8760
VBOUT(14)=    -8.4594
VBOUT(15)=    -9.0429

****************************************

CODER.........PRACTICAL
DECODER........IDEAL (A=0.5,B=0.5,C=0.0)

S= SIGN BIT
L= ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V= ONES COMPLEMENT OF STEP WORD IN DECIMAL

*****************************************************************************************

S     L     V     OUTPUT      INPUT       INPUT       INPUT       STEP        TRACKING
                  LEVEL       LOWER       UPPER       STEP        MIDDLE      ERROR
                              LIMIT       LIMIT       SIZE        POINT

*****************************************************************************************

1     0     0     0.          -.0104      -.0092      .0011       -.0098      NOT DEND
1     0     1      .0025      -.0092      -.0070      .0023       -.0081       .43E+01
1     0     2      .0049      -.0070      -.0047      .0023       -.0058       .22E+01
1     0     3      .0074      -.0047      -.0024      .0023       -.0035       .15E+01
1     0     4      .0098      -.0024      -.0001      .0024       -.0012       .11E+01
1     0     5      .0123      -.0001       .0022      .0023        .0011       .91E+00
1     0     6      .0147       .0022       .0045      .0023        .0033       .77E+00
1     0     7      .0172       .0045       .0068      .0023        .0056       .67E+00
1     0     8      .0196       .0068       .0091      .0023        .0079       .60E+00
1     0     9      .0221       .0091       .0113      .0023        .0102       .54E+00
1     0    10      .0245       .0113       .0136      .0023        .0125       .49E+00
1     0    11      .0270       .0136       .0159      .0023        .0148       .45E+00
1     0    12      .0294       .0159       .0182      .0023        .0171       .42E+00
1     0    13      .0319       .0182       .0205      .0023        .0194       .39E+00
1     0    14      .0343       .0205       .0228      .0023        .0216       .37E+00
1     0    15      .0368       .0228       .0289      .0060        .0258       .30E+00
1     1     0      .0404       .0288       .0311      .0023        .0300       .26E+00
1     1     1      .0453       .0311       .0357      .0046        .0334       .26E+00
1     1     2      .0503       .0357       .0403      .0046        .0380       .24E+00
```

1	1	3	.0552	.0403	.0448	.0046	.0426	.23E+00
1	1	4	.0601	.0448	.0494	.0046	.0471	.22E+00
1	1	5	.0650	.0494	.0540	.0046	.0517	.20E+00
1	1	6	.0699	.0540	.0586	.0046	.0563	.19E+00
1	1	7	.0748	.0586	.0632	.0046	.0609	.19E+00
1	1	8	.0797	.0632	.0677	.0046	.0654	.18E+00
1	1	9	.0846	.0677	.0723	.0046	.0700	.17E+00
1	1	10	.0895	.0723	.0769	.0046	.0746	.17E+00
1	1	11	.0944	.0769	.0815	.0046	.0792	.16E+00
1	1	12	.0993	.0815	.0860	.0046	.0837	.16E+00
1	1	13	.1042	.0860	.0906	.0046	.0883	.15E+00
1	1	14	.1091	.0906	.0952	.0046	.0929	.15E+00
1	1	15	.1140	.0952	.1073	.0121	.1012	.11E+00
1	2	0	.1213	.1073	.1118	.0046	.1095	.97E-01
1	2	1	.1311	.1118	.1210	.0092	.1164	.11E+00
1	2	2	.1409	.1210	.1301	.0092	.1256	.11E+00
1	2	3	.1508	.1301	.1393	.0092	.1347	.11E+00
1	2	4	.1606	.1393	.1485	.0092	.1439	.10E+00
1	2	5	.1704	.1485	.1576	.0092	.1530	.10E+00
1	2	6	.1802	.1576	.1668	.0092	.1622	.10E+00
1	2	7	.1900	.1668	.1759	.0092	.1713	.98E-01
1	2	8	.1998	.1759	.1851	.0092	.1805	.97E-01
1	2	9	.2096	.1851	.1942	.0092	.1896	.95E-01
1	2	10	.2194	.1942	.2034	.0092	.1988	.94E-01
1	2	11	.2292	.2034	.2125	.0092	.2079	.93E-01
1	2	12	.2390	.2125	.2217	.0092	.2171	.92E-01
1	2	13	.2488	.2217	.2308	.0092	.2262	.91E-01
1	2	14	.2586	.2308	.2400	.0092	.2354	.90E-01
1	2	15	.2684	.2400	.2641	.0241	.2520	.61E-01
1	3	0	.2831	.2641	.2733	.0092	.2687	.51E-01
1	3	1	.3027	.2733	.2916	.0183	.2824	.67E-01
1	3	2	.3223	.2916	.3099	.0183	.3007	.67E-01
1	3	3	.3420	.3099	.3282	.0183	.3191	.67E-01
1	3	4	.3616	.3282	.3465	.0183	.3374	.67E-01
1	3	5	.3812	.3465	.3648	.0183	.3557	.67E-01
1	3	6	.4008	.3648	.3831	.0183	.3740	.67E-01
1	3	7	.4204	.3831	.4014	.0183	.3923	.67E-01
1	3	8	.4400	.4014	.4197	.0183	.4106	.67E-01
1	3	9	.4596	.4197	.4380	.0183	.4289	.67E-01
1	3	10	.4792	.4380	.4563	.0183	.4472	.67E-01
1	3	11	.4988	.4563	.4746	.0183	.4655	.67E-01
1	3	12	.5184	.4746	.4929	.0183	.4838	.67E-01
1	3	13	.5381	.4929	.5113	.0183	.5021	.67E-01
1	3	14	.5577	.5113	.5296	.0183	.5204	.67E-01
1	3	15	.5773	.5296	.5778	.0483	.5537	.41E-01
1	4	0	.6067	.5778	.5962	.0184	.5870	.32E-01
1	4	1	.6459	.5962	.6328	.0366	.6145	.49E-01
1	4	2	.6851	.6328	.6694	.0366	.6511	.50E-01
1	4	3	.7244	.6694	.7060	.0366	.6877	.51E-01
1	4	4	.7636	.7060	.7426	.0366	.7243	.51E-01
1	4	5	.8028	.7426	.7792	.0366	.7609	.52E-01
1	4	6	.8420	.7792	.8158	.0366	.7975	.53E-01
1	4	7	.8812	.8158	.8525	.0366	.8342	.53E-01
1	4	8	.9205	.8525	.8891	.0366	.8708	.54E-01
1	4	9	.9597	.8891	.9257	.0366	.9074	.55E-01
1	4	10	.9989	.9257	.9623	.0366	.9440	.55E-01

1	4	11	1.0381	.9923	.9980	.0366	.9806	.55E-01
1	4	12	1.0773	.9949	1.0355	.0366	1.0172	.56E-01
1	4	13	1.1166	1.0355	1.0721	.0366	1.0538	.56E-01
1	4	14	1.1558	1.0721	1.1087	.0366	1.0904	.57E-01
1	4	15	1.1950	1.1087	1.2053	.0966	1.1570	.32E-01
1	5	0	1.2338	1.2053	1.2420	.0367	1.2236	.24E-01
1	5	1	1.3323	1.2420	1.3152	.0732	1.2786	.40E-01
1	5	2	1.4107	1.3152	1.3884	.0732	1.3518	.42E-01
1	5	3	1.4892	1.3884	1.4616	.0732	1.4250	.43E-01
1	5	4	1.5676	1.4616	1.5349	.0732	1.4983	.44E-01
1	5	5	1.6460	1.5349	1.6081	.0732	1.5715	.45E-01
1	5	6	1.7245	1.6081	1.6813	.0732	1.6447	.46E-01
1	5	7	1.8029	1.6813	1.7545	.0732	1.7179	.47E-01
1	5	8	1.8814	1.7545	1.8277	.0732	1.7911	.48E-01
1	5	9	1.9598	1.8277	1.9010	.0732	1.8644	.49E-01
1	5	10	2.0382	1.9010	1.9742	.0732	1.9376	.49E-01
1	5	11	2.1167	1.9742	2.0474	.0732	2.0108	.50E-01
1	5	12	2.1951	2.0474	2.1206	.0732	2.0840	.51E-01
1	5	13	2.2736	2.1206	2.1938	.0732	2.1572	.51E-01
1	5	14	2.3520	2.1938	2.2671	.0732	2.2304	.52E-01
1	5	15	2.4304	2.2671	2.4602	.1931	2.3636	.27E-01
1	6	0	2.5481	2.4602	2.5336	.0734	2.4969	.20E-01
1	6	1	2.7050	2.5336	2.6800	.1464	2.6068	.36E-01
1	6	2	2.8619	2.6800	2.8265	.1464	2.7533	.38E-01
1	6	3	3.0188	2.8265	2.9729	.1464	2.8997	.39E-01
1	6	4	3.1756	2.9729	3.1193	.1464	3.0461	.41E-01
1	6	5	3.3325	3.1193	3.2658	.1464	3.1926	.42E-01
1	6	6	3.4894	3.2658	3.4122	.1464	3.3390	.43E-01
1	6	7	3.6463	3.4122	3.5587	.1464	3.4854	.44E-01
1	6	8	3.8032	3.5587	3.7051	.1464	3.6319	.45E-01
1	6	9	3.9600	3.7051	3.8515	.1464	3.7783	.46E-01
1	6	10	4.1169	3.8515	3.9980	.1464	3.9247	.47E-01
1	6	11	4.2738	3.9980	4.1444	.1464	4.0712	.47E-01
1	6	12	4.4307	4.1444	4.2908	.1464	4.2176	.48E-01
1	6	13	4.5876	4.2908	4.4373	.1464	4.3641	.49E-01
1	6	14	4.7445	4.4373	4.5837	.1464	4.5105	.49E-01
1	6	15	4.9013	4.5837	4.9700	.3863	4.7769	.25E-01
1	7	0	5.1367	4.9700	5.1168	.1468	5.0444	.18E-01
1	7	1	5.4504	5.1168	5.4097	.2929	5.2632	.34E-01
1	7	2	5.7642	5.4097	5.7025	.2929	5.5561	.36E-01
1	7	3	6.0780	5.7025	5.9954	.2929	5.8490	.38E-01
1	7	4	6.3917	5.9954	6.2883	.2929	6.1419	.39E-01
1	7	5	6.7055	6.2883	6.5812	.2929	6.4347	.40E-01
1	7	6	7.0192	6.5812	6.8740	.2929	6.7276	.42E-01
1	7	7	7.3330	6.8740	7.1669	.2929	7.0205	.43E-01
1	7	8	7.6468	7.1669	7.4598	.2929	7.3134	.44E-01
1	7	9	7.9605	7.4598	7.7527	.2929	7.6062	.45E-01
1	7	10	8.2743	7.7527	8.0455	.2929	7.8991	.45E-01
1	7	11	8.5881	8.0455	8.3384	.2929	8.1920	.46E-01
1	7	12	8.9018	8.3384	8.6313	.2929	8.4848	.47E-01
1	7	13	9.2156	8.6313	8.9242	.2929	8.7777	.48E-01
1	7	14	9.5294	8.9242	9.2170	.2929	9.0706	.48E-01
1	7	15	9.8431	9.2170	9.9896	.7726	9.6033	.24E-01
0	0	0	-0.	-.0138	-.0104	.0034	-.0121	NOT DEND
0	0	1	-.0025	-.0161	-.0138	.0023	-.0150	-.51E+01
0	0	2	-.0049	-.0184	-.0161	.0023	-.0173	-.25E+01

0	0	3	-.0074	-.0207	-.0184	.0023	-.0195	-.17E+01
0	0	4	-.0098	-.0230	-.0207	.0023	-.0218	-.12E+01
0	0	5	-.0123	-.0253	-.0230	.0023	-.0241	-.97E+00
0	0	6	-.0147	-.0275	-.0253	.0023	-.0264	-.8CE+00
0	0	7	-.0172	-.0298	-.0275	.0023	-.0287	-.67E+00
0	0	8	-.0196	-.0321	-.0298	.0023	-.0310	-.5ME+00
0	0	9	-.0221	-.0344	-.0321	.0023	-.0333	-.51E+00
0	0	10	-.0245	-.0367	-.0344	.0023	-.0356	-.45E+00
0	0	11	-.0270	-.0390	-.0367	.0023	-.0378	-.40E+00
0	0	12	-.0294	-.0413	-.0390	.0023	-.0401	-.36E+00
0	0	13	-.0319	-.0436	-.0413	.0023	-.0424	-.33E+00
0	0	14	-.0343	-.0459	-.0436	.0023	-.0447	-.30E+00
0	0	15	-.0368	-.0496	-.0459	.0038	-.0477	-.30E+00
0	1	0	-.0404	-.0565	-.0496	.0069	-.0530	-.31E+00
0	1	1	-.0453	-.0610	-.0565	.0046	-.0588	-.30E+00
0	1	2	-.0503	-.0656	-.0610	.0046	-.0633	-.26E+00
0	1	3	-.0552	-.0702	-.0656	.0046	-.0679	-.23E+00
0	1	4	-.0601	-.0748	-.0702	.0046	-.0725	-.21E+00
0	1	5	-.0650	-.0793	-.0748	.0046	-.0771	-.19E+00
0	1	6	-.0699	-.0839	-.0793	.0046	-.0816	-.17E+00
0	1	7	-.0748	-.0885	-.0839	.0046	-.0862	-.15E+00
0	1	8	-.0797	-.0931	-.0885	.0046	-.0908	-.14E+00
0	1	9	-.0846	-.0977	-.0931	.0046	-.0954	-.13E+00
0	1	10	-.0895	-.1022	-.0977	.0046	-.0999	-.12E+00
0	1	11	-.0944	-.1068	-.1022	.0046	-.1045	-.11E+00
0	1	12	-.0993	-.1114	-.1068	.0046	-.1091	-.99E-01
0	1	13	-.1042	-.1160	-.1114	.0046	-.1137	-.91E-01
0	1	14	-.1091	-.1205	-.1160	.0046	-.1182	-.84E-01
0	1	15	-.1140	-.1280	-.1205	.0075	-.1243	-.90E-01
0	2	0	-.1213	-.1418	-.1280	.0137	-.1349	-.11E+00
0	2	1	-.1311	-.1509	-.1418	.0092	-.1463	-.12E+00
0	2	2	-.1409	-.1601	-.1509	.0092	-.1555	-.10E+00
0	2	3	-.1508	-.1692	-.1601	.0092	-.1646	-.92E-01
0	2	4	-.1606	-.1784	-.1692	.0092	-.1738	-.82E-01
0	2	5	-.1704	-.1875	-.1784	.0092	-.1829	-.74E-01
0	2	6	-.1802	-.1967	-.1875	.0092	-.1921	-.66E-01
0	2	7	-.1900	-.2058	-.1967	.0092	-.2012	-.59E-01
0	2	8	-.1998	-.2150	-.2058	.0092	-.2104	-.53E-01
0	2	9	-.2096	-.2241	-.2150	.0092	-.2196	-.48E-01
0	2	10	-.2194	-.2333	-.2241	.0092	-.2287	-.42E-01
0	2	11	-.2292	-.2424	-.2333	.0092	-.2379	-.38E-01
0	2	12	-.2390	-.2516	-.2424	.0092	-.2470	-.34E-01
0	2	13	-.2488	-.2607	-.2516	.0092	-.2562	-.30E-01
0	2	14	-.2586	-.2699	-.2607	.0092	-.2653	-.26E-01
0	2	15	-.2684	-.2849	-.2699	.0150	-.2774	-.33E-01
0	3	0	-.2931	-.3123	-.2849	.0274	-.2986	-.55E-01
0	3	1	-.3027	-.3306	-.3123	.0183	-.3215	-.62E-01
0	3	2	-.3223	-.3489	-.3306	.0183	-.3398	-.54E-01
0	3	3	-.3420	-.3672	-.3489	.0183	-.3581	-.47E-01
0	3	4	-.3616	-.3856	-.3672	.0183	-.3764	-.41E-01
0	3	5	-.3812	-.4039	-.3856	.0183	-.3947	-.36E-01
0	3	6	-.4008	-.4222	-.4039	.0183	-.4130	-.31E-01
0	3	7	-.4204	-.4405	-.4222	.0183	-.4313	-.26E-01
0	3	8	-.4400	-.4588	-.4405	.0183	-.4496	-.22E-01
0	3	9	-.4596	-.4771	-.4588	.0183	-.4679	-.18E-01
0	3	10	-.4792	-.4954	-.4771	.0183	-.4862	-.15E-01

0	3	11	-.4988	-.5137	-.4954	.0183	-.5045	-.11E-01
0	3	12	-.5184	-.5320	-.5137	.0183	-.5228	-.85E-02
0	3	13	-.5381	-.5503	-.5320	.0183	-.5411	-.57E-02
0	3	14	-.5577	-.5686	-.5503	.0183	-.5594	-.32E-02
0	3	15	-.5773	-.5986	-.5686	.0300	-.5836	-.11E-01
0	4	0	-.6067	-.6535	-.5986	.0547	-.6261	-.32E-01
0	4	1	-.6459	-.6901	-.6535	.0366	-.6714	-.40E-01
0	4	2	-.6851	-.7267	-.6901	.0366	-.7084	-.34E-01
0	4	3	-.7244	-.7633	-.7267	.0366	-.7450	-.29E-01
0	4	4	-.7636	-.7999	-.7633	.0366	-.7816	-.24E-01
0	4	5	-.8028	-.8365	-.7999	.0366	-.8182	-.19E-01
0	4	6	-.8420	-.8732	-.8365	.0366	-.8548	-.15E-01
0	4	7	-.8812	-.9098	-.8732	.0366	-.8915	-.12E-01
0	4	8	-.9205	-.9464	-.9098	.0366	-.9281	-.83E-02
0	4	9	-.9597	-.9830	-.9464	.0366	-.9647	-.52E-02
0	4	10	-.9989	-1.0196	-.9830	.0366	-1.0013	-.24E-02
0	4	11	-1.0381	-1.0562	-1.0196	.0366	-1.0379	.22E-03
0	4	12	-1.0773	-1.0928	-1.0562	.0366	-1.0745	.26E-02
0	4	13	-1.1166	-1.1294	-1.0928	.0366	-1.1111	.49E-02
0	4	14	-1.1558	-1.1660	-1.1294	.0366	-1.1477	.70E-02
0	4	15	-1.1950	-1.2261	-1.1660	.0601	-1.1961	-.88E-03
0	5	0	-1.2538	-1.3358	-1.2261	.1097	-1.2809	-.22E-01
0	5	1	-1.3323	-1.4090	-1.3358	.0732	-1.3724	-.30E-01
0	5	2	-1.4107	-1.4823	-1.4090	.0732	-1.4456	-.25E-01
0	5	3	-1.4892	-1.5555	-1.4823	.0732	-1.5189	-.20E-01
0	5	4	-1.5676	-1.6287	-1.5555	.0732	-1.5921	-.16E-01
0	5	5	-1.6460	-1.7019	-1.6287	.0732	-1.6653	-.12E-01
0	5	6	-1.7245	-1.7751	-1.7019	.0732	-1.7385	-.81E-02
0	5	7	-1.8029	-1.8483	-1.7751	.0732	-1.8117	-.49E-02
0	5	8	-1.8814	-1.9216	-1.8483	.0732	-1.8850	-.19E-02
0	5	9	-1.9598	-1.9948	-1.9216	.0732	-1.9582	.83E-03
0	5	10	-2.0382	-2.0680	-1.9948	.0732	-2.0314	.34E-02
0	5	11	-2.1167	-2.1412	-2.0680	.0732	-2.1046	.57E-02
0	5	12	-2.1951	-2.2144	-2.1412	.0732	-2.1778	.79E-02
0	5	13	-2.2736	-2.2877	-2.2144	.0732	-2.2510	.99E-02
0	5	14	-2.3520	-2.3609	-2.2877	.0732	-2.3243	.12E-01
0	5	15	-2.4304	-2.4810	-2.3609	.1201	-2.4209	.39E-02
0	6	0	-2.5481	-2.7005	-2.4810	.2195	-2.5907	-.17E-01
0	6	1	-2.7050	-2.8469	-2.7005	.1464	-2.7737	-.25E-01
0	6	2	-2.8619	-2.9933	-2.8469	.1464	-2.9201	-.20E-01
0	6	3	-3.0188	-3.1398	-2.9933	.1464	-3.0665	-.16E-01
0	6	4	-3.1756	-3.2862	-3.1398	.1464	-3.2130	-.12E-01
0	6	5	-3.3325	-3.4326	-3.2862	.1464	-3.3594	-.81E-02
0	6	6	-3.4894	-3.5791	-3.4326	.1464	-3.5059	-.47E-02
0	6	7	-3.6463	-3.7255	-3.5791	.1464	-3.6523	-.16E-02
0	6	8	-3.8032	-3.8719	-3.7255	.1464	-3.7987	.12E-02
0	6	9	-3.9600	-4.0184	-3.8719	.1464	-3.9452	.38E-02
0	6	10	-4.1169	-4.1648	-4.0184	.1464	-4.0916	.62E-02
0	6	11	-4.2738	-4.3113	-4.1648	.1464	-4.2380	.84E-02
0	6	12	-4.4307	-4.4577	-4.3113	.1464	-4.3845	.10E-01
0	6	13	-4.5876	-4.6041	-4.4577	.1464	-4.5309	.12E-01
0	6	14	-4.7445	-4.7506	-4.6041	.1464	-4.6773	.14E-01
0	6	15	-4.9013	-4.9908	-4.7506	.2402	-4.8707	.63E-02
0	7	0	-5.1367	-5.4297	-4.9908	.4389	-5.2103	-.14E-01
0	7	1	-5.4504	-5.7226	-5.4297	.2929	-5.5762	-.23E-01
0	7	2	-5.7642	-6.0155	-5.7226	.2929	-5.8690	-.18E-01

0	7	3	-6.0780	-6.3083	-6.0155	.2929	-6.1619	-.14E-01
0	7	4	-6.3917	-6.6012	-6.3083	.2929	-6.4548	-.99E-02
0	7	5	-6.7055	-6.8941	-6.6012	.2929	-6.7477	-.63E-02
0	7	6	-7.0192	-7.1870	-6.8941	.2929	-7.0405	-.30E-02
0	7	7	-7.3330	-7.4798	-7.1870	.2929	-7.3334	-.54E-04
0	7	8	-7.6468	-7.7727	-7.4798	.2929	-7.6263	.27E-02
0	7	9	-7.9605	-8.0656	-7.7727	.2929	-7.9192	.52E-02
0	7	10	-8.2743	-8.3585	-8.0656	.2929	-8.2120	.75E-02
0	7	11	-8.5881	-8.6513	-8.3585	.2929	-8.5049	.97E-02
0	7	12	-8.9018	-8.9442	-8.6513	.2929	-8.7978	.12E-01
0	7	13	-9.2156	-9.2371	-8.9442	.2929	-9.0906	.14E-01
0	7	14	-9.5294	-9.5300	-9.2371	.2929	-9.3835	.15E-01
0	7	15	-9.8431	-10.0000	-9.5300	.4700	-9.7650	.79E-02

PROGRAM XCODEC

CODER.....PRACTICAL
DECODER.....IDEAL (A=0.5,B=0.5,C=0.0)

0 DB REF. IS 10.00 (PEAK,FULL LOAD SINUSOID)

INPUT AMPLITUDE	INPUT DB BELOW FULL LOAD	S/D DB C-WEIGHT	GAIN TRACKING DB	OUTPUT FUNDAMENTAL AMPLITUDE	OUTPUT DC COMPONENT
10.0000	0.	36.56	0.	10.1555	.0960
7.9433	-2.00	38.38	.05	8.1137	.1169
6.3096	-4.00	36.06	-.02	6.3933	.1050
5.0119	-6.00	37.69	.04	5.1105	.0543
3.9811	-8.00	38.56	.04	4.0617	.0635
3.1623	-10.00	36.41	.01	3.2135	.0565
2.5119	-12.00	38.00	.03	2.5604	.0311
1.9953	-14.00	37.73	.05	2.0382	.0396
1.5849	-16.00	37.05	-.00	1.6094	.0331
1.2589	-18.00	37.70	.05	1.2865	.0234
1.0000	-20.00	38.07	.06	1.0225	.0243
.7943	-22.00	36.37	-.01	.8061	.0234
.6310	-24.00	37.42	-.00	.6408	.0173
.5012	-26.00	37.77	.08	.5136	.0180
.3981	-28.00	36.87	-.01	.4040	.0170
.3162	-30.00	35.34	.00	.3212	.0155
.2512	-32.00	37.95	.06	.2569	.0145
.1995	-34.00	36.16	.03	.2033	.0143
.1585	-36.00	34.11	-.04	.1602	.0138
.1259	-38.00	35.95	.04	.1284	.0125
.1000	-40.00	35.85	.06	.1022	.0128
.0794	-42.00	33.48	-.01	.0806	.0128
.0631	-44.00	32.62	-.08	.0635	.0122
.0501	-46.00	31.93	.05	.0512	.0117
.0398	-48.00	31.03	-.07	.0401	.0115
.0316	-50.00	28.18	-.15	.0316	.0116

A P P E N D I X C

MODEL PARAMETERS FOR OPERATIONAL AMPLIFIER SIMULATION

The interactive computer simulation program ISPICE, provided by National CSS, Inc., has been used.

Definition of model parameters:

VTO - zero substrate bias threshold voltage

PHI - surface potential

CO - oxide capacitance per unit area

PB - bulk junction potential

BETA - parameter K' defined in eq. (5.1)

GAMMA - body effect coefficient

LAMBDA - channel length modulation parameter

C1 - gate-source overlap capacitance per unit channel width

C2 - gate-drain overlap capacitance per unit channel width

CBD - drain-substrate zero-bias capacitance per unit channel width

CBS - source-substrate zero-bias capacitance per unit channel width

All parameters except BETA have the same values for all devices. These values are given below:

VTO = 0.2 v

PHI = 0.7 v

CO = 3.46E-8 F/cm^2

PB = 0.85 v

GAMMA = 0.91 $v^{1/2}$

LAMBDA = 3.3E-5 $cm/v^{1/2}$

C1 = 15 pF/cm

C2 = 15 pF/cm

CBD = 45 pF/cm

CBS = 45 pF/cm

The values of parameter BETA were as given below. Device numbers refer to Figure 6.1.

Device #	BETA(A/v^2)
M2, M4, M11, M15, M18	8.35E-6
M23	9.0E-6
M25	10.3E-6
M1, M6, M9	11.8E-6
M3, M5, M7, M8, M10, M12, M13, M14, M16, M17, M19, M20, M21, M-2, M24, M26	13.55E-6

For details on how the values of these parameters were assigned, see [43].

A P P E N D I X D

MINIMIZATION OF THE AREA OF AN INVERTER OF SIMPLE GEOMETRY

Consider the inverter shown in Figure D.1(a), realized by the geometry shown in Figure D.1(b), where $(Z/L)_1 > 1$ and $(Z/L)_2 < 1$. For a given gain G, equation (5.14) gives:

$$\frac{(Z/L)_1}{(Z/L)_2} = G^2 \tag{D.1}$$

If minimum dimensions are assumed and lateral diffusion is taken into account, we will have:

$$L_1 = 0.3 \text{ mil} \tag{D.2}$$

$$Z_1 = 0.3\left(\frac{Z}{L}\right)_1 \text{ mil} \tag{D.3}$$

$$Z_2 = 0.5 \text{ mil} \tag{D.4}$$

$$L_2 = \frac{Z_2}{(Z/L)_2} = \frac{0.5}{(Z/L)_2} \text{ mil} \tag{D.5}$$

From these expressions and Figure D.1(b) we get for the areas involved:

$$A_{M1} = \left(\frac{Z}{L}\right)_1 \times 0.3 \times 1.5 \text{ mil}^2 + A_{M1,\text{contacts}} \tag{D.6}$$

$$A_{M2} = 0.5 \times \frac{0.5}{(Z/L)_2} \text{ mil}^2 + A_{M2,\text{contacts}} \tag{D.7}$$

As the channel sizes are varied, the areas due to the contacts remain unchanged, and therefore the only variable area is, from (D.6) and (D.7):

$$A = \left[0.45\left(\frac{Z}{L}\right)_1 + \frac{0.25}{(Z/L)_2}\right] \text{mil}^2 \tag{D.8}$$

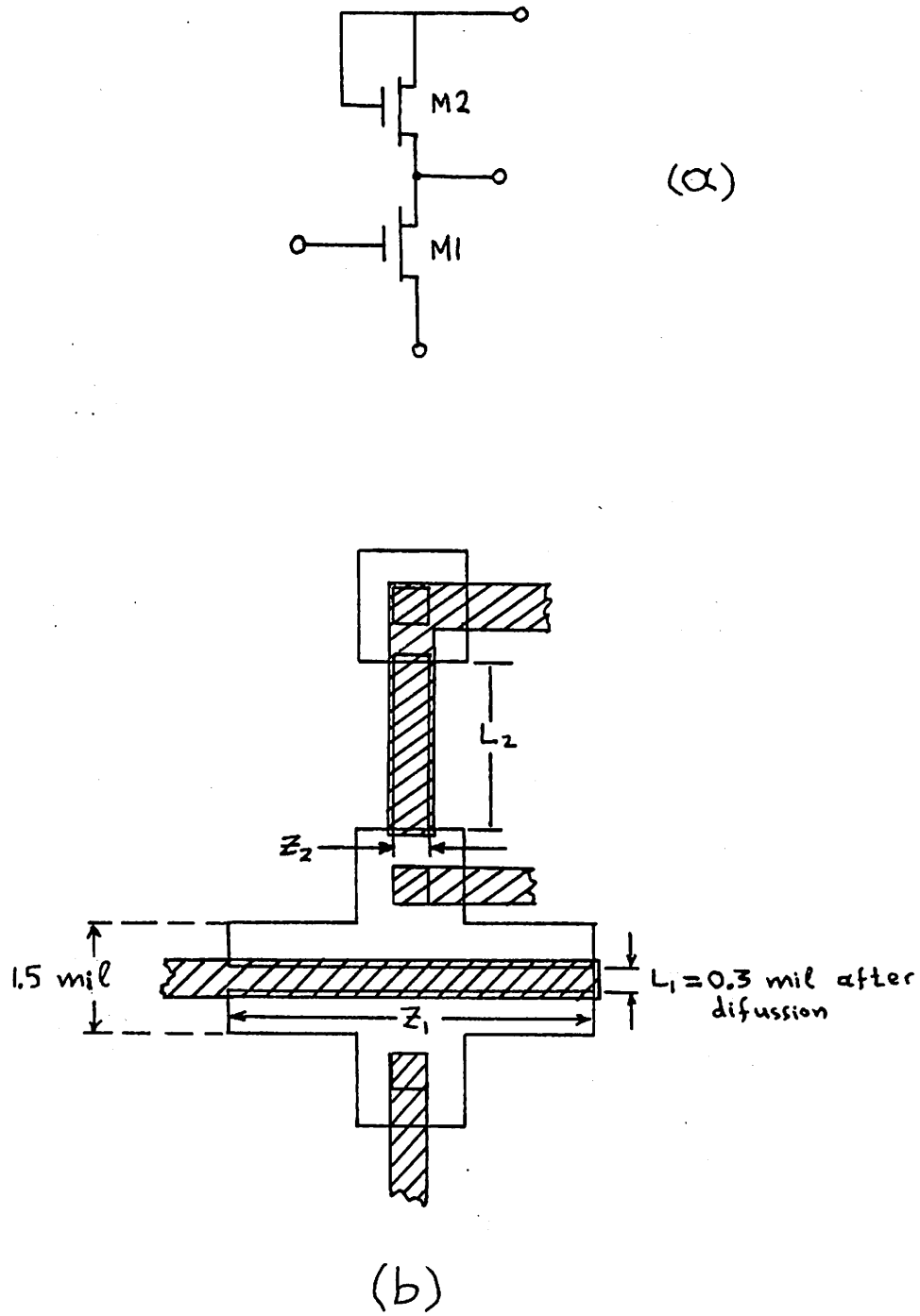


Figure D.1: An inverter of simple geometry.

Equation (D.8) can now be minimized subject to the constraint imposed by equation (D.1). The result is easily derived, and is:

$$\left(\frac{Z}{L}\right)_1 = 0.75G \tag{D.9}$$

$$\left(\frac{Z}{L}\right)_2 = \frac{0.75}{G} \tag{D.10}$$

APPENDIX E

CALCULATION OF SMALL-SIGNAL CAPACITANCES IN MOS TRANSISTORS

The accurate calculation of capacitances in MOS transistors is very involved [36]. Here we will use approximations that make possible a first order estimate of these capacitances.

The capacitances for an MOS transistor in the saturation region are shown in Figure E.1. C_1 and C_2 are gate overlap capacitances, C_{SB} and C_{DB} are junction capacitances and C_G is the capacitance between the gate and the well formed channel. C_1, C_2, C_{SB} and C_{DB} will be assumed proportional to the channel width for simplicity, and the numerical values that will be used represent reasonable averages for the geometries and processes usually used. For the overlap capacitances, these values are:

$$\frac{C_1}{Z} = \frac{C_2}{Z} = 15 \frac{pF}{cm} \tag{E.1}$$

For the simple inverter of Figure 5.5(b) it can be seen that as far as small-signal analysis is concerned, C_{SB1} and C_{DB2} are shorted out. The remaining junctions will be assumed to be reversed biased at 9 volts. This is close to actual bias values that are used in the design of the operational amplifier in Chapter 6. For this bias value, the junction capacitances of interest have been estimated as:

$$\frac{C_{DB1}}{Z_1} = \frac{C_{SB2}}{Z_2} = 13.3 \frac{pF}{cm} \tag{E.2}$$

since the bias is the same for the two junctions.

Consider now the calculation of capacitances for $Z/L > 1$ and $Z/L < 1$.

a) Capacitances for $Z/L > 1$. This case is shown in Figure E.2(a). After diffusion, a channel length of 0.3 mil is assumed. For an oxide

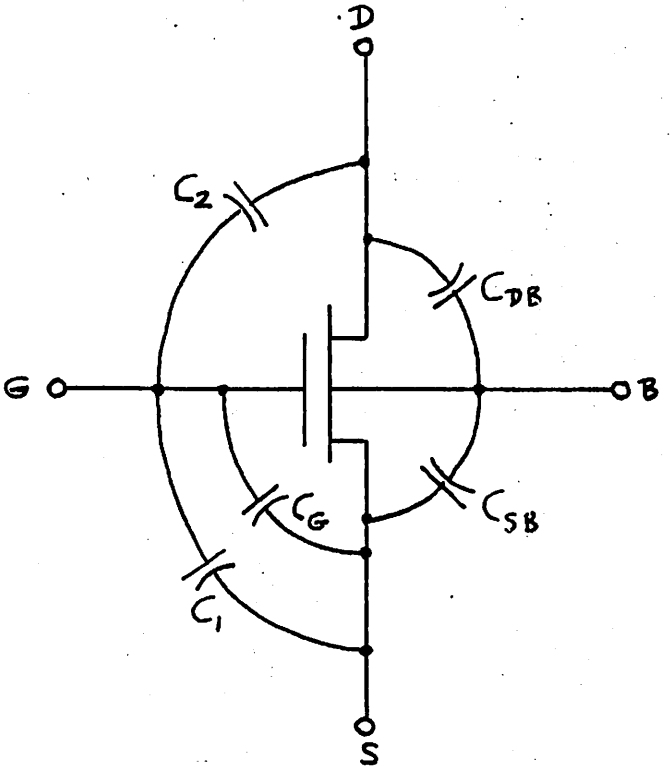
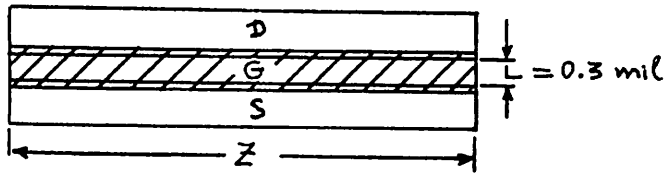
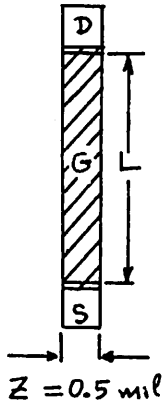


Figure E.1: Capacitances in an MOS transistor.



(a)



(b)

Figure E.2: Simple geometry layouts for approximate small-signal capacitance calculations.

(a) $\frac{Z}{L} > 1$

(b) $\frac{Z}{L} < 1$

thickness of 1000 Å and using equations (E.1) and (E.2) we get:

$$C_{DB} = Z \times 13.3 \frac{pF}{cm} = 0.3 \text{ mil} \times \left(\frac{Z}{L}\right) \times 13.3 \frac{pF}{cm} = 0.01 \left(\frac{Z}{L}\right) \text{ pF} \qquad \text{(E.3)}$$

$$C_1 = C_2 = Z \times 15 \frac{pF}{cm} = 0.3 \text{ mil} \times \left(\frac{Z}{L}\right) \times 15 \frac{pF}{cm} = 0.012 \left(\frac{Z}{L}\right) pF \qquad \text{(E.4)}$$

$$C_G = ZLC_o = \left(0.3 \text{ mil} \times \frac{Z}{L}\right) \times (0.3 \text{ mil}) \times \left(3.46 \times 10^{-8} \frac{F}{cm^2}\right) =$$
$$= 0.02 \left(\frac{Z}{L}\right) \text{ pF} \qquad \text{(E.5)}$$

b) Capacitances for $Z/L < 1$. This case is shown in Figure E.2(b). We have:

$$C_{SB} = 0.5 \text{ mil} \times 13.3 \frac{pF}{cm} = 0.017 \text{ pF} \qquad \text{(E.6)}$$

$$C_1 = C_2 = 0.5 \text{ mil} \times 15 \frac{pF}{cm} = 0.02 \text{ pF} \qquad \text{(E.7)}$$

$$C_G = ZLC_o = (0.5 \text{ mil}) \times \left[\frac{0.5 \text{ mil}}{(Z/L)}\right] \times \left(3.46 \times 10^{-8} \frac{F}{cm^2}\right) =$$
$$= \frac{0.056}{(Z/L)} \text{ pF} \qquad \text{(E.8)}$$

Notice that the junction and gate overlap capacitances do not depend on Z/L, as long as the later is less than unity. They only depend on the minimum dimension used for the channel width, which here is assumed to be 0.5 mil.

APPENDIX F

N-CHANNEL MOS ALUMINUM GATE FABRICATION PROCESS

A description of the process used to fabricate the operational amplifier described in Chapter 5 will be given below, which has evolved in its present form through previous efforts [28, 34]. Although the steps necessary for p+ isolation diffusion are included for completeness, such diffusion has not been used in fabricating the op amp, since they were found unnecessary, as explained in Chapter 6. The substrate used was p-type, 100 orientation, and 3-5 Ω-cm resistivity. In the sequence below, the abbreviation "DI" stands for deionized water.

Fabrication sequence

1. Initial wafer cleaning:
   - a) DI: HF (9:1), room temperature, dip
   - b) TCE, 60°C, 10 min
   - c) Acetone, room temperature, 2 min
   - d) DI, rinse
   - e) RCA1 cleaning:

     NH_4OH: H_2O_2: DI, (1:1:5), 75°C, 15 min

     DI, rinse
   - f) RCA2 cleaning:

     HCL: H_2O_2: DI, (1:1:6), 75°C, 15 min

     DI, rinse

     N_2, blow dry

2. Initial oxidation: Initial oxidation furnace, growth of 0.92 μ wet oxide.
   - a) Wet O_2, 0.5 ℓ/min, 1150°C, 90 min

b) Dry N_2, 0.65 ℓ/min, 850°C, 10 min

3. Photoresist step (p+ isolation diffusion mask)

a) Apply Kodak 747 (Micro neg) photoresist; 50 c.s.; 500 rpm, 30 sec, single coat

b) Air dry, 15 min

c) Prebake, 90°C, 10 min

d) Expose mask, 3.5 sec

e) Spray develop, 30 sec

f) Spray rinse, 20 sec

g) Postbake, 125°C, 30 min

h) Oxide etch, NH_4F: HF (5:1), room temperature, 9.5 min

i) Photoresist strip, H_2SO_4: H_2O_2 (4:1), 90°C (self-heating), 5 min

4. RCA1 & RCA2 cleaning (see steps 2e, 2f)

5. p + predeposition: p-type predeposition furnace 950°C

B_2H_6, 0.26 ℓ/min
O_2, 0.013 ℓ/min } Simultaneous flow, 15 min
N_2, 1.3 ℓ/min

6. Etch boron glass, 12% HF, dip, 1.5 min

7. RCA1 & RCA2 cleaning (see steps 2e, 2f)

8. Oxide growth over p+: p-type drive-in furnace, 1150°C

a) Wet O_2, 0.5 ℓ/min, 16 min

b) Dry N_2, 1.0 ℓ/min, 10 min

9. Photoresist step (n+ diffusion mask)

Same as step 3, except (b), where drying under infrared lamp is used.

10. RCA1 & RCA2 cleaning (see steps 2e, 2f)

11. n+ predeposition: n-type predeposition furnace, 1050°C; $POCℓ_3$, 0°C.

a) O_2, 0.1 ℓ/min
   N_2, 1.25 ℓ/min } 5 min (dry)

b) O_2, 0.1 ℓ/min
   N_2, 1.25 ℓ/min
   N_2/POQ_3 0.096 ℓ/min } 20 min (wet)

c) O_2, 0.1 ℓ/min
   N_2, 1.25 ℓ/min } 2 min (dry)

12. Etch phosphorous glass, 12% HF, dip

16. RCA1 & RCA2 cleaning (see steps 2e, 2f)

17. Oxide growth over n+: n-type drive-in furnace

    a) Wet O_2, 0.5 ℓ/min, 1100°C, 34 min

    b) Dry N_2, 1.0 ℓ/min, 900°C, 10 min

18. Photoresist step (gate oxide mask)

    Same as step 9, except (h), for which time is 6.5 min

19. RCA1 & RCA2 cleaning. (see steps 2e, 2f)

20. Gate oxide growth: n-type drive-in furnace, wafer horizontal on boat.

    a) Dry O_2, 1.5 ℓ/min, 1000°C, 110 min total time. For uniform oxide thickness, wafer is rotated according to the following schedule:

Rotation angle	Time
0°	10 min
180°	22 min
90°	33 min
270°	45 min

    b) N_2, 1.0 ℓ/min, 900°, 5 min

21. Photoresist step (contact mask)

    Same as step 9, except (d), where mask is exposed 2.5 sec, then shifted one row, and again exposed 2.5 sec. This eliminates pinholes.

Also, in (h) 1.5 min etch.

22. RCA1 & RCA2 cleaning (see steps 2e, 2f)

23. Dry under infrared lamp, 10 min

24. Evaporate aluminum, 0.3 μ to 0.4 μ thickness

24. Photoresist step (metallization mask)

    a) Heat under infrared lamp, 10 min

    b) Apply AZ1350J photoresist, 8000 rpm, 30 sec, single coat

    c) Prebake, 90°C, 45 min

    d) Expose mask, 12.5 sec

    e) Develop with MF312 or AZ1350J developer, developer: DI, (1:1), 45 sec

    f) DI, rinse

    g) Postbake, 90°C, 30 min

    h) Etch aluminum with aluminum etchant type A, 45°-50°C with ultrasonic agitation, 30 sec-45 sec

    i) DI, rinse

    j) Strip photoresist with 1112 photoresist stripper, 50°-60°C, 2-3 min

    k) DI, rinse

    ℓ) N_2, blow dry

25. Heat treatment: Sintering oven, 200°C

    N_2: H_2 (9:1), 1ℓ/min, 5 min

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