TOPOLOGICAL GENERATION AND ANALYSIS OF VOLTAGE MULTIPLIER CIRCUITS

by

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ABSTRACT

Voltage multipliers are used for transformerless conversion of an ac input voltage $v_i(t) = E \sin \omega t$ into a dc output voltage $V_{out} = nE$, where $n \geq 2$. This paper investigates the topological properties of voltage multiplier circuits and presents a unified approach for generating new voltage-multiplier circuit structures. In particular, an algorithm is presented for generating n-fold voltage multipliers with n capacitors and n diodes. A theorem is presented for finding the dc capacitor voltage by inspection when no load current is drawn. For the case with load, explicit formulas for the output dc voltage and the output resistance are given. Using the algorithm developed in this paper, three new voltage quadrupler circuits are generated and shown to have an output resistance only one-half of the conventional ladder quadrupler circuit.

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1. Introduction

A voltage multiplier (abbreviated VM) is a capacitor-diode[1] network capable of converting an ac input voltage $v_i(t) = E \sin \omega t$ into a dc output voltage $V_{out} = nE$, where $n \geq 2$. Several commonly used voltage multiplier circuit configurations (n=2,3,4) are shown in Fig. 1. Voltage multipliers have been used extensively in the high-voltage power supply of television sets and in many other applications requiring an ac-to-dc conversion [1-3]. Figure 2(a) shows a C-D ladder network with the diodes forming the "rungs," and with $v_i(t)$ applied to one end of the ladder [4,p.822]. A dc capacitor voltage $V_o = nE$ may be obtained by connecting the output circuit of Fig. 2(b) across an appropriate pair of nodes of the ladder network. The output circuit consists of a diode in series with a capacitor (called the output capacitor) and will henceforth be referred to as the "output tank" to emphasize the fact that in practice, the output capacitor has a much larger capacitance than the others in the ladder. Two tank connections for realizing an even order and an odd order multipliers are shown in Figs. 3(a) and (b), respectively [5].

As an aid for understanding the operating mechanisms of voltage multiplier circuits, let us first review some basic properties of the simple rectifier circuit shown in Fig. 4. If the capacitor is initially uncharged i.e., $v_C(0) = 0$, then the steady-state capacitor voltage is

$$V_C \triangleq v_C(\infty) = \begin{cases} E_o + E, & \text{if } E_o + E \geq 0 \\ 0, & \text{if } E_o + E < 0 \end{cases} \tag{1}$$

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[1] We assume all diodes are ideal throughout this paper, i.e., the diode voltage V_D and the diode current i_D satisfy the constraints $v_D \leq 0$, $i_D \geq 0$, and $v_D i_D = 0$.

In other words, if the input voltage at any time forward biases the diode, then the capacitor will be charged to the peak forward biasing voltage and will retain that voltage forever. Furthermore, if any passive load is now connected across the capacitor such that it draws only a finite amount of charge from the capacitor for all $t \geq 0$, then it is intuitively clear that the lost charge will eventually be replenished by the source during the subsequent forward biasing intervals of $v_i(t)$. Therefore $v_C(\infty)$ is again equal to $E_o + E$. Thus, in steady state, the capacitor is equivalent to a dc voltage source of value $E_o + E$, provided that the passive load draws only a finite amount of charge.

Using the preceding equivalent voltage-source concept, we can now find the steady-state solution of the VM circuits of Figs. 2 and 3 via an intuitive method, provided the following requirement is satisfied by these circuits:

Assumption 1. The steady-state solution of the initially relaxed C-D-1E_{ac} network is the same as the solution obtained by connecting the diodes to the initially relaxed C-1E_{ac} subnetwork, one at a time, in any order, provided that a steady state is reached before each new diode is connected.[2]

As a specific example, consider the C-D-1E_{ac} ladder network of Fig. 3(a). The associated C-1E_{ac} network is obtained by disconnecting all diodes. Assuming that all capacitors are initially uncharged at $t = 0$ when the diode D_1 is re-connected, then it follows from Eq. (1) that $V_{C1} = E$.

[2]For simplicity, we use the abbreviation "C-D-1E_{ac} network" to denote any network containing capacitors, diodes, and exactly one sinusoidal voltage source. Similarly, a C-1E_{ac} network contains only capacitors and exactly one voltage source. A network is said to be initially relaxed if the initial voltages on the capacitors are equal to zero prior to the application of the voltage source.

We now treat C_1 as if it is a voltage source $V_{C1} = E$. Looking to the left of nodes 1 and 2, we see an equivalent voltage source $v_{21}(t) = E + E \sin \omega t$. Hence if we re-connect diode D_2 after C_1 has reached steady state, we would obtain $V_{C2} = 2E$ in accordance with Eq. (1). Continuing this diode re-connection procedure, the following steady-state voltages for the circuits of Figs. 3(a) and (b) are easily obtained:

$$V_{C1} = E$$
$$V_{C2} = V_{C3} = \cdots = V_{C,n-1} = 2E$$
$$V_{Cn} = nE$$

The preceding method is simple and gives correct results (as will be proved in Section 3) for these circuits. Unfortunately, its validity depends on whether Assumption 1 is satisfied, or not. To demonstrate that not all capacitor-diodes networks satisfy the property stipulated in Assumption 1, consider the circuit shown in Fig. 5, where both capacitors are assumed to be initially uncharged. If D_1 is re-connected at $t = 0$ (D_2 not connected yet) then $v_{C1}(t) = v_{C2}(t) = 10$ for $t \geq \frac{1}{4} T$, where $T = 2\pi/\omega$. Now suppose that D_2 is re-connected at $t = T$, then D_2 will be reversed biased at all times since $v_{D2}(t) = 4 \sin \omega t - 10 < 0$ for all $t \geq T$. Thus the steady-state solution is $V_{C1} = V_{C2} = 10$. On the other hand, if we re-connect D_2 first at $t = 0$, and subsequently re-connect D_1 at $t = T$, then a straightforward analysis gives the steady-state solution $V_{C1} = 8$ and $V_{C2} = 12$. This example shows that different orders of re-connecting the diodes could lead to different steady-state solutions. Consequently the property stipulated in Assumption 1 is certainly not true in general.

Even assuming that Assumption 1 is satisfied for the time being, the preceding Intuitive Method still has a serious drawback: It is not applicable to all C-D-1E_{ac} voltage multiplier circuits, such as the one shown in Fig. 11.

One objective of this paper is therefore to present a rigorous theory and a reasonably simple method for computing the steady-state solution of voltage-multiplier circuits.

Another objective is to provide answers to the following practical questions:

Is the ladder network of Fig. 3 the only general voltage multiplier circuit configuration? If not, what other general configurations are there? How does one choose among different configurations? What is the effect of the load on the dc output voltage? In Section 2 we present a topological procedure for constructing a variety of n-fold voltage multiplier configurations using n capacitors and n diodes. It will be clear that the conventional ladder voltage multiplier circuit is just a special case generated by our topological algorithm. In Section 3 we present a rigorous theory for determining the steady-state capacitor voltages of the voltage multiplier circuits generated in Section 2, under no load condition. The result of this section actually gives a justification for the Intuitive Method described earlier. The effect of load current on the dc output voltage is analyzed in Section 4. The resulting analysis will enable one to choose the best among several n-fold voltage multiplier configurations, when voltage regulation is the primary concern.

2. A Topological Method for Generating Voltage Multiplier Circuits

The problem at hand is to construct a network N made up of ideal capacitors, ideal diodes, and one sinusoidal voltage source (abbreviated

C-D-1E_{ac}) that will possibly perform as a voltage multiplier. Since a general theory of C-D-1E_{ac} networks does not currently exist, we shall not attempt to investigate the most general network configuration in which the diodes and the capacitors can be connected in an arbitrary fashion. Instead, we shall first identify the features of the conventional ladder voltage multiplier circuit which are fundamental to the operation of the circuit and then develop a topological method for generating other configurations possessing the same fundamental features. The following two conditions on the C-D-1E_{ac} networks are two such features which we will henceforth assume to hold for all networks to be investigated in this paper:

(1) C-E tree Hypothesis: The capacitors and the voltage source form a tree of the network.

(2) D-E tree Hypothesis: The diodes and the voltage source form a tree of the network.

In Section 3 we shall describe a rigorous and yet simple method for finding the steady-state solution of any C-D-1E_{ac} network satisfying the C-E tree and the D-E tree hypotheses. Although our original motivation for imposing these two hypotheses was to preserve partly the conventional ladder voltage multiplier circuit configuration, several subsequent considerations have indicated that these two hypotheses are in fact desirable for the design of any practical voltage multipliers. For example, if there is a loop consisting of the voltage source and some capacitors, and hence violating the C-E tree hypothesis, then the capacitor voltages in the loop will no longer remain constant even in steady state. If there are two diodes connected in series, and hence violating the C-E tree hypothesis, then either one diode may be shorted, or both diodes may be

removed without affecting the solution. If there are two diodes connected in parallel, and hence violating the D-E tree hypothesis, then either one diode may be removed, or both diodes may be shorted without affecting the solution. If there are two capacitors connected in series (and hence violating the D-E tree hypothesis), or in parallel (and hence violating the C-E tree hypothesis), then the two capacitors can be replaced by an equivalent capacitor.

One immediate consequence of hypotheses (1) and (2) is that if the network N has n+2 nodes, then

total number of capacitors
= total number of diodes = n

Given n, we can construct all nC-nD-1E networks (containing n capacitors, n diodes, and one voltage source), satisfying the C-E tree and D-E tree hypotheses. The conventional voltage multiplier circuits in Figs. 2 and 3 are rather special cases where the voltage source and (n-1) capacitors form a path in the network. Upon eliminating the (n-1)C-1E path constraint, we immediately have a new realm of nC-nD-1E networks which can possibly perform as voltage multipliers. Figure 6 shows three networks that satisfy hypotheses (1) and (2), but do not have (n-1)C-1E paths. The steady-state capacitor voltage are indicated in the figure.

We shall now examine the number of nC-1E trees that can be constructed, given the number n. As an illustration, consider first the special case n=3. There are six distinct 3C-1E trees as shown in Fig. 7. Label the nodes of the voltage source E as nodes 0 and 1. If the E-branch is removed from each of these graphs, the resulting graph separates into two sut-trees T_{C0} and T_{C1}, with n_0 and n_1 C-branches, respectively, where

$n_0 \geq 0$, $n_1 \geq 0$ and $n_0 + n_1 = n$. Now in the enumeration of all T_{C0} and T_{C1} subtrees, the nodes 0 and 1 are different from the rest because they serve as reference nodes and will henceforth be called the roots of T_{C0} and T_{C1}, respectively. Given any n_0 and n_1 such that $n = n_0+n_1$, our problem is to find all distinct combinations of rooted trees T_{C0} containing n_0 branches, and all rooted trees T_{C1} containing n_1 branches. This problem can therefore be identified with the problem of enumerating "unlabeled rooted trees" for which well-known methods exist [6,p.246]. In particular, if w_k denotes the number of unlabeled rooted, trees of k branches, then the value of w_k corresponding to the first 9 values of k are listed below.

k	1	2	3	4	5	6	7	8	9
w_k	1	2	4	9	20	48	115	286	719

Applying this table to Fig. 7, we see that we have 1 rooted tree T_{C0} of 1 branch, 2 rooted trees T_{C1} of 2 branches, and 4 rooted trees T_{C1} of 3 branches. The value of w_k for any k can be calculated by the use of a counting series [6,p.247] which we will not elaborate here. The above list should suffice for our present discussions.

To get the total number of nC-1E trees we should:

(1) consider all possible ways of partitioning n into $n = n_0+n_1$;

(2) for each (n_0,n_1) pair, enumerate the unlabeled rooted trees T_{C0} and T_{C1};

(3) consider all possible combinations of T_{C0} and T_{C1} which, together with E, form a C-E tree, and take care to avoid duplications.

It can be shown that the result is:

$t_n \triangleq$ number of distinct nC-1E trees

$$= \begin{cases} w_n + w_1 w_{n-1} + \cdots + w_{\frac{n-1}{2}} \cdot w_{\frac{n+1}{2}}, & \text{for odd } n \\ w_n + w_1 w_{n-1} + \cdots + w_{(\frac{n}{2}-1)} w_{(\frac{n}{2}+1)} + \frac{1}{2} w_{\frac{n}{2}} (w_{\frac{n}{2}} + 1) & \text{for even } n \end{cases} \quad (2)$$

The first seven values of t_n are listed below.

n	1	2	3	4	5	6	7
t_n	1	3	6	16	37	96	237

Observe that for the example in Fig. 7, we have n=3 and hence we expect to have 6 distinct 3C-1E trees. Once a particular C-E tree configuration has been selected, there are still many ways to connect the n diodes to form a D-E tree. The combinatorial problem becomes extremely complicated. Fortunately some practical considerations described below will further restrict the class of C-E trees and D-E trees for our purpose.

Consider the three circuits shown in Fig. 6, each of which uses 4 capacitors and 4 diodes. Figure 6(a) is a voltage quadrupler whereas the other two circuits can at most function as voltage doublers. Naturally, we are only interested in voltage multiplier circuits which produce the highest dc output voltage possible with the given number of components. With this practical consideration in mind, we see that the diode D_1 in Fig. 6(c) is poorly located because its fundamental loop relative to the C-E tree contains only capacitors (and D_1 of course). Since the ac voltage source is not included in the loop, we have a situation of charging some capacitors by other capacitors. We can not expect the highest dc voltage to be enhanced by such a mechanism. Therefore, it is reasonable to connect

every diode only from one node of T_{C0} to another node of T_{C1}. In this way, every fundamental loop associated with the diodes relative to the C-E tree will contain the voltage source. This procedure further implies that the fundamental cutset defined by the voltage source relative to the C-E tree will contain all the diodes [7]. Therefore, we have now justified the imposition of a third hypothesis:

(3) D-E cutset Hypothesis. The diodes and the voltage source form a cutset of the network.

Next, let us review the action of the voltage multiplier of Fig. 3(a). When D_1 alone is connected to the C-E ladder, C_1 will be charged to $V_{C1}=E$. At this time, the voltage drop from node 2 to node 1 is

$$v_{21}(t) = E + E \sin \omega t$$

which has positive peak of 2E. By connecting D_2 from node 2 to node 3. we utilize the 2E peak voltage to charge C_2 and obtain $V_{C2} = 2E$. At this point in time, if we connect another diode from node 2 to some other capacitor, the voltage available for charging the capacitor is at most 2E. Hence, nothing is to be gained by connecting more diodes to node 2. Thus, in order to make the best use of every diode; it is advisable not to have more than two diodes connected to every node. This, together with the D-E cutset hypothesis, suggests that (a) The number of the capacitors in the two subtrees T_{C0} and T_{C1} differ by no more than 1. (b) The diodes are contained in a path. We have therefore justified the imposition of still another topological constraint:[3]

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[3] Hypotheses (1) through (4) imply that at most two diodes are connected to each node.

(4) Aligned D-path Hypothesis. The diodes, possibly with the voltage source, form a path and are forward biased in the same direction in the path.

A network satisfying hypotheses (1)-(4) can be depicted as shown in Fig. 8. We wish to emphasize that all four hypotheses have been imposed through practical considerations rather than theoretical development. The C-E tree and D-E tree hypotheses are introduced so that the fundamental features of the conventional ladder voltage multiplier are preserved, and such that the steady-state solution can be found by simple and rigorous method (Section 3). The D-E cutset and the aligned D-path hypotheses are introduced in order that an n-fold voltage multiplier with only n capacitors and n diodes may be developed. The D-E cutset and D-path hypotheses can also be justified mathematically once the C-E tree and D-E tree hypotheses have been imposed. This will be done in Section 3 after a general steady-state analysis method is developed. Observe that the conventional ladder circuits of Figs. 2 and 3 satisfy all four hypotheses. In contrast, the circuits shown in Figs. 6(b) and (c), which fail to function as voltage quadruplers violate the D-E path hypotheses.

Taking into consideration the four hypotheses stated above, we shall now describe an algorithm for producing an n-fold voltage multiplier with n capacitors and n diodes. For the purpose of our subsequent analysis of the circuit (Section 3), the algorithm also includes a scheme for labeling the nodes the capacitors, and the diodes.

Algorithm VM (Voltage Multipliers):

Step 1. C-E tree construction. Construct two rooted trees T_{C0} and T_{C1} with $\frac{n}{\lfloor 2 \rfloor}$ and $\frac{\lceil n \rceil}{2}$ capacitors, respectively.[4] Connect the voltage source across the two roots of T_{C0} and T_{C1}.

Step 2. Node Labeling.

Case 1. n is even. For T_{C1}, select any capacitor as the output capacitor and label its nodes with 1 and n+1. Label the remaining nodes of T_{C1} with odd integers (3,5,...,n-1). For T_{C0}, label the root with 0, and the remaining nodes with even integers (2,4,...,n).

Case 2. n is odd. For T_{C1}, select any capacitor as the output capacitor and label its nodes with 1 and n+2. Label the remaining nodes of T_{C1} with odd integers (3,5,...,n). For T_{C0}, label the nodes with even integers (2,4,...,n+1), taking care that roots of T_{C0} and T_{C1} are labeled with consecutive integers.

Step 3. Diode connection and labeling.

Case 1. n is even. Connect a string of n diodes to node pairs (1,2),(2,3),...,(n,n+1), with each diode forward biased from node j to node k, j < k. Label the diodes consecutively as $D_1, D_2, \ldots, D_n$.

Case 2. n is odd. Connect n diodes to the node pairs (1,2),(2,3), ...,(n,n+1),(n+1,n+2) disregarding the pair associated with the nodes of the voltage source, with each diode biased from node j to node k, j < k. Label the diodes consecutively as $D_1, D_2, \ldots, D_n$.

Step 4. Capacitor labeling.

Label the output capacitor as C_n, which is between the node pair (1,n+1) for the case n is even, or between the node pair (1,n+2) for the case n is odd. Label the remaining capacitors as $C_1, C_2, \ldots, C_{n-1}$ in any order.

[4] We use the symbol $\lfloor x \rfloor$ (floor of x) to denote the greatest integer equal to or less than x and the symbol $\lceil x \rceil$ (ceiling of x) to denote the least integer equal to or greater than x.

Observe that the fundamental loop defined by C_n with respect to the C-E tree contains n diodes. It will be shown rigorously in Section 3 that $V_{Cn} = nE$ if $v_i = E \sin \omega t$.

As examples, the conventional voltage multiplier circuits of Fig. 3 and the new quadrupler circuit of Fig. 6(a) have been generated and labeled according to the algorithm. Observe that Algorithm VM has been presented as one possible way of constructing voltage multiplier circuits. There may exist other voltage multiplier circuits that cannot be generated by algorithm VM. However, we conjecture that all nC-nD-1E_{ac}, n-fold voltage multipliers can be generated by Algorithm VM, provided that the positions of any two series-connected elements may be interchanged, if necessary. In the conjecture, it is understood that the output voltage $V_0 = nE$ must appear across a capacitor. Consider n=4 for example. Algorithm VM generates 9 distinct configurations which are listed in Fig. 14. For this simple case, one can exhaust all possible connections of 4C-4D-1E elements and show that there are only 9 distinct voltage quadruplers and that all of them are generated by Algorithm VM.

3. Steady-State Analysis -- Without Load

Consider an nC-nD-1E_{ac} network N which satisfies the C-E tree and D-E tree hypotheses. To facilitate the formulation of the equilibrium equations for N, we construct G_d, the directed graph associated with N. In G_d, let each diode branch direction be the same as the forward current direction. Branch directions for the capacitors and the voltage source may be arbitrarily assigned. Then the fundamental loop matrix with respect to the C-E tree may be partitioned as follows (see [7] for notation):

$$\underset{\sim}{B} = \begin{array}{c} \begin{array}{cccc} E & C_1 & \ldots, C_n & D_1, \ldots, D_n \end{array} \\ \left[\begin{array}{c|ccc|c} & & & & \\ \underset{\sim}{B}_E & & \underset{\sim}{B}_C & & \underset{\sim}{1}_n \\ & & & & \end{array}\right] \\ \underbrace{\qquad\qquad\qquad}_{\text{C-E tree}} \quad \underbrace{\qquad}_{\text{D-cotree}} \end{array} \tag{3}$$

The current and voltage vectors are denoted by $\underset{\sim}{i}_E$, $\underset{\sim}{i}_C$, $\underset{\sim}{i}_D$, v_E, $\underset{\sim}{v}_C$, and v_D respectively. Throughout the remaining sections, we use small letters for functions of time, and capital letters for constants. The network is governed by three laws which are expressed by matrix equations as follows:

Kirchhoff voltage law (KVL):

$$\underset{\sim}{B}_E v_E + \underset{\sim}{B}_C \underset{\sim}{v}_C + v_D = Q \tag{4}$$

Kirchhoff current law (KCL) [7,p.145]:

$$\begin{bmatrix} \underset{\sim}{i}_E \\ \underset{\sim}{i}_C \end{bmatrix} = \begin{bmatrix} \underset{\sim}{B}_E^T \\ \underset{\sim}{B}_C^T \end{bmatrix} \underset{\sim}{i}_D \tag{5}$$

Branch v-i relationships:[5]

$$\underset{\sim}{i}_C = \underset{\sim}{C} \frac{d\underset{\sim}{v}_C}{dt} \tag{6}$$

$$\underset{\sim}{v}_D \leq \underset{\sim}{0},\ \underset{\sim}{i}_D \geq \underset{\sim}{0},\ \underset{\sim}{v}_D^T \underset{\sim}{i}_D = 0 \tag{7}$$

Equations (4)-(7) must be satisfied for all t, although we are looking only at $t \to \infty$. Assume that the steady-state capacitor voltages are constant, i.e., $\underset{\sim}{v}_C(\infty) = \underset{\sim}{V}_C$. We shall outline a procedure for finding $\underset{\sim}{V}_C$. From Eq. (6), we have $\underset{\sim}{i}_C(\infty) = \underset{\sim}{0}$. Since the D-E elements also form a tree T_{DE}, we can express $\underset{\sim}{i}_E$ and $\underset{\sim}{i}_D$ in terms of the link (for T_{D-E}) currents $\underset{\sim}{i}_C$. Then, $\underset{\sim}{i}_C = \underset{\sim}{0}$ implies $\underset{\sim}{i}_E = \underset{\sim}{0}$ and $\underset{\sim}{i}_D = \underset{\sim}{0}$. It follows that all currents are zero in steady state, a result that obviously satisfies KCL.

Letting $\underset{\sim}{v}_C = \underset{\sim}{V}_C$, $v_E = E \sin \omega t$ (E>0), we have from Eqs. (4) and (7)

$$\underset{\sim}{v}_D(t) = -\underset{\sim}{B}_E E \sin \omega t - \underset{\sim}{B}_C \underset{\sim}{V}_C \leq 0, \text{ for all } t \tag{8}$$

It is easy to see that the inequality (8) holds for all t if, and only if,

$$\underset{\sim}{U} E - \underset{\sim}{B}_C \underset{\sim}{V}_C \leq \underset{\sim}{0}$$

or

$$\boxed{\underset{\sim}{B}_C \underset{\sim}{V}_C \geq \underset{\sim}{U} E} \tag{9}$$

where $\underset{\sim}{U}$ is an n-vector with 1's and 0's as its elements; namely,

$$u_j = \begin{cases} 1 & \text{if the j-th element of } \underset{\sim}{B}_E \text{ is either 1 or -1.} \\ 0, & \text{otherwise} \end{cases}$$

We have succeeded in obtaining an inequality devoid of the time variable t. We will show that inequality (9) is the crux to the steady-state analysis

[5] In the paper, $\underset{\sim}{a} \geq \underset{\sim}{b}$ means $a_i \geq b_i$ for all i.

of N.

The matrix $\underset{\sim}{B}_C$ is a square matrix of order n. Since the capacitors form a cotree for the D-E tree, $\underset{\sim}{B}_C$ is nonsingular [8,p.93]. At this point, it is rather tempting to ignore the ">" sign in Inequality (9) and then find $\underset{\sim}{V}_C$ by solving $\underset{\sim}{B}_C\underset{\sim}{V}_C = \underset{\sim}{U}E$ and accepting the result as the steady-state solution. Unfortunately, such a procedure has no theoretical foundation. It may or may not give the correct answers, as the following two simple examples will demonstrate.

Example 1. Consider the voltage doubler shown in Fig. 1. We have

$$\underset{\sim}{B} = \left[\underset{\sim}{B}_E \quad \underset{\sim}{B}_C \quad \underset{\sim}{1}_n\right] = \left[\begin{array}{c|cc|cc} 1 & 1 & 0 & 1 & 0 \\ \hline -1 & -1 & 1 & 0 & 1 \end{array}\right]$$

Then $\underset{\sim}{U} = [1 \quad 1]^T$, and $\hat{\underset{\sim}{V}}_C \triangleq \underset{\sim}{B}_C^{-1}\underset{\sim}{U}E = [E, 2E]^T$ which is indeed the correct solution for $\underset{\sim}{V}_C$.

Example 2. Consider the circuit shown in Fig. 9. We have

$$\underset{\sim}{B} = \left[\underset{\sim}{B}_E \quad \underset{\sim}{B}_C \quad \underset{\sim}{1}_n\right] = \left[\begin{array}{c|cc|ccc} 1 & 1 & 0 & 1 & 0 & 0 \\ \hline -1 & -1 & 1 & 0 & 1 & 0 \\ -1 & 0 & 1 & 0 & 0 & 1 \end{array}\right]$$

Then $\underset{\sim}{U} = [1 \quad 1 \quad 1]^T$, and $\hat{\underset{\sim}{V}}_C \triangleq \underset{\sim}{B}_C^{-1}\underset{\sim}{U}E = [E, \ 2E, \ -E]^T$, which is obviously not a solution, as V_{C3} can never be negative in Fig. 9.

In view of these examples, it is clear that we should use Inequality (9) as the basis for the steady-state analysis. Observe that Inequality (9) is only a necessary, but not a sufficient condition for $\underset{\sim}{V}_C$ to be the steady-state solution of N. A general inequality of the form $\underset{\sim}{A}\underset{\sim}{X} \geq \underset{\sim}{K}$ may have no solution, a unique solution, or infinitely many solutions. For the case of infinitely many mathematical solutions, further information

must be used to determine which can be accepted as the solution to a physical problem. To see the significance of the above observation, consider the voltage doubler circuit of Fig. 1 again. The equation corresponding to (9) is given by:

$$\begin{bmatrix} 1 & 0 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \end{bmatrix} \geq \begin{bmatrix} E \\ E \end{bmatrix}$$

One obvious solution is $\underset{\sim}{V}_C = [E, 2E]^T$. But another solution is $\underset{\sim}{V}_C = [4E, 6E]^T$, among infinitely many others. Consider now the actual operation of the circuit. $V_{C1} = 4E$, $V_{C2} = 6E$ is possible only if we charge C_1 and C_2 up to 4E and 6E, respectively, before the ac source is applied. If the circuit starts with uncharged capacitors, then a transient analysis will reveal that the voltage finally approach $v_{C1}(\infty) = V_{C1} = E$, and $v_{C2}(\infty) = V_{C2} = 2E$. Therefore, we will reject $[4E, 6E]^T$, but accept $[E, 2E]^t$ as the steady-state solution of $\underset{\sim}{V}_C$.

Except for some extremely simple circuits, finding the steady-state solutions of C-D-1E_{ac} networks through transient analysis is not a practical approach. Therefore, we should try to find some features that will distinguish the steady-state solution (for initially relaxed networks) from all other feasible solutions of (9). Fortunately this is possible with the aid of some physical reasoning. Consider again the doubler circuit of Fig. 1. Suppose that we have capacitors initially charged to $v_{C1}(0) = 4E$, $v_{C2}(0) = 6E$. Then $\underset{\sim}{V}_C = [4E,6E]^T$ is a solution to Inequality (9). But now imagine that due to some temporary leakage the capacitor voltages drop to[3.9E,5.9E] . These reduced voltages also satisfy Inequality (9). Since the ac voltage source v_i=E sin ωt does not have the capability to restore the

capacitor voltages to their previous values [4E,6E] . We shall say that the solution voltages [4E,6E] are not maintainable. Next, consider the solution $\underset{\sim}{V}_C = [E,2E]^T$ which, by transient analysis, has been found to be the steady-state solution if the network is initially relaxed. Imagine again that due to some temporary leakage, the capacitor voltages drop to $\underset{\sim}{V}_C = [0.9E,1.9E]^T$. It can immediately be shown that these lower capacitor voltages cannot satisfy Inequality (9). The consequence of violating Inequality (9) is that the diodes begin to conduct ($i_D > 0$), and charges will be restored to the capacitors until $\underset{\sim}{V}_C = [E,2E]^T$ is again reached. Consequently, in this case we shall say that the voltages [E,2E] are maintainable.

Thus, one feature that distinguishes the steady-state solution of an initially relaxed network from the other feasible solutions of Inequality (9) is their "maintainability". The mathematical counterpart of this observation will now be defined precisely.

Definition. Let $\underset{\sim}{X}=\underset{\sim}{X}^*$ be a solution of $\underset{\sim}{A}\underset{\sim}{X} \geq \underset{\sim}{K}$, where $\underset{\sim}{A}$ and $\underset{\sim}{K}$ are m×n and n×1 real matrices, respectively. $\underset{\sim}{X}^*$ is called a reducible solution if there exists another solution $\underset{\sim}{X}=\underset{\sim}{\tilde{X}}\neq\underset{\sim}{X}^*$ such that for i=1,2,...n, the following is true:

$$\begin{cases} x_i^* \geq \tilde{x}_i \geq 0 & \text{if } x_i^* > 0 \\ x_i^* \leq \tilde{x}_i \leq 0 & \text{if } x_i^* < 0 \\ \tilde{x}_i = 0 & \text{if } x_i^* = 0 \end{cases}$$

Otherwise, the solution is said to be irreducible.

For the two-dimensional case, this definition can be illustrated geometrically. In Fig. 10, the feasible solutions of $\underset{\sim}{A}\underset{\sim}{X}=\underset{\sim}{K}$

are indicated by the hatched areas. For Fig. 10(a), $\underset{\sim}{X}^* = [1,2]^T$ is the only irreducible solution, and $\underset{\sim}{X}^*$ is also the solution of $\underset{\sim}{\underset{\sim}{A}}\underset{\sim}{X}=\underset{\sim}{K}$. In Fig. 10(b), $\underset{\sim}{X}=\underset{\sim}{\underset{\sim}{A}}^{-1}\underset{\sim}{K} = [1\ -1]^T$ is a solution of $\underset{\sim}{\underset{\sim}{A}}\underset{\sim}{X} \geq \underset{\sim}{K}$, but it is reducible. The only irreducible solution in Fig. 10(b) is $\underset{\sim}{X} = [1\ 0]^T$ which is not a solution of $\underset{\sim}{\underset{\sim}{A}}\underset{\sim}{X}=\underset{\sim}{K}$. To show that a irreducible solution need not be unique, observe that all points along the solid bold line segment in Fig. 10(c) are irreducible solutions. A moment's reflection will reveal that for the Inequality (9), a reducible solution corresponds to a non-maintainable set of capacitor voltages, while a irreducible solution corresponds to a maintainable set of capacitor voltages. Clearly, the correct steady-state solution must be a irreducible solution of Inequality (9). For the general case of $\underset{\sim}{\underset{\sim}{A}}\underset{\sim}{X} \geq \underset{\sim}{K}$, finding the irreducible solution, or solutions, is a complicated problem. However, there are some special cases that can be solved quite easily. The following lemma is of great usefulness in the present study.

Lemma 1. Let $\underset{\sim}{\underset{\sim}{A}}$ be an n×n non-singular matrix, and $\underset{\sim}{K}$ an n-vector where $\underset{\sim}{K} \geq \underset{\sim}{0}$. If for each row of $\underset{\sim}{\underset{\sim}{A}}^{-1}$, all non-zero elements have the same sign, then the inequality $\underset{\sim}{\underset{\sim}{A}}\underset{\sim}{X} \geq \underset{\sim}{K}$ has one, and only one, irreducible solution given by $\underset{\sim}{X}=\underset{\sim}{\underset{\sim}{A}}^{-1}\underset{\sim}{K}$.

Proof: See Appendix.

We shall now illustrate the use of Inequality (9) and Lemma 1 with an example.

Example 3. Find the steady-state capacitor voltages for the circuit shown in Fig. 11.

Solution:

For Eq. (3), we have

$$\underset{\sim}{B} = [B_E B_C 1_n] = \begin{array}{c} \begin{matrix} E & C_1 & C_2 & C_3 & D_1 & D_2 & D_3 \end{matrix} \\ \left[\begin{array}{c|ccc|ccc} 1 & 0 & -1 & 1 & 1 & 0 & 0 \\ -1 & -1 & 1 & -1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{array}\right] \end{array}$$

The matrix $\underset{\sim}{B}_C$ and vector $\underset{\sim}{U}$ associated with the Inequality (9) can now be identified as follows:

$$\underset{\sim}{B}_C = \begin{bmatrix} 0 & -1 & 1 \\ -1 & 1 & -1 \\ 1 & 0 & 1 \end{bmatrix}, \qquad \underset{\sim}{U} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

The inverse of $\underset{\sim}{B}_C$ is

$$\underset{\sim}{B}_C^{-1} = \begin{bmatrix} -1 & -1 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

Since the non-zero elements in each row of $\underset{\sim}{B}_C^{-1}$ have the same sign, it follows from Lemma 1 that the unique irreducible solution, is given by

$$\underset{\sim}{V}_C = \underset{\sim}{B}_C^{-1} \underset{\sim}{U} E = [-2E, 2E, 3E]$$

and this solution is the steady-state solution of this circuit. We see that the circuit is a voltage tripler. Observe that it is not possible to find the steady-state voltages of this circuit by the intuitive reasoning described in Section 1.

We shall now present a theorem which will once again make it possible for us to obtain the steady-state solution by inspection. The theorem is a major result of this paper, and therefore will be stated clearly in words.

Theorem 1. Let N be an nC-nD-1E_{ac} network which satisfies the following topological constraints:

(a) the capacitors and the voltage source form a tree

(b) the diodes and the voltage source form a tree

(c) the diodes and the voltage source from a cutset

(d) the diodes, possibly with the voltage source, form a path and are forward biased in the same direction in the path

If $v_i(t)=E \sin \omega t$, $E>0$ and the capacitors are intially uncharged, then in steady state the capacitor voltages are constant, and are given by

$$V_{C_j} = \pm k_j E$$

where k_j denotes the number of diodes contained in the fundamental loop defined by the capacitor C_j with respect to the diodes-voltage-source tree, and where the positive sign holds when the reference direction of V_{Cj} is aligned with the diode's forward directions, and is negative otherwise.

Proof: Let $\underset{\sim}{B}$ and $\hat{\underset{\sim}{B}}$ be the fundamental loop matrices with respect to the C-E tree and the D-E tree, respectively. Let $\underset{\sim}{Q}$ be the fundamental cutset matrix with respect to the C-E tree. These three matrices may be partitioned as follows (assuming, of course, columns are ordered correspondingly in all matrices):

$$\underset{\sim}{B} = \begin{array}{c} \begin{matrix} C_1 & \cdots & C_n & E & D_1 & \cdots & D_n \end{matrix} \\ \left[\begin{array}{ccc|c|ccc} & & & & & & \\ & \underset{\sim}{B}_C & & \underset{\sim}{B}_E & & \underset{\sim}{1}_n & \\ & & & & & & \end{array}\right] \\ \underbrace{\qquad\qquad\qquad\qquad}_{\text{C-E tree}} \quad \underbrace{\qquad\qquad}_{\text{D-cotree}} \end{array} \tag{10}$$

$$\underset{\sim}{Q} = \left[\begin{array}{c|c|c} \underset{\sim}{1}_n & \underset{\sim}{0} & \underset{\sim}{Q}_{CD} \\ \hline \underset{\sim}{0} & 1 & \underset{\sim}{Q}_{ED} \end{array}\right] \qquad (11)$$

C-E tree D-cotree

$$\hat{\underset{\sim}{B}} = \left[\begin{array}{c|c|c} \underset{\sim}{1}_n & \hat{\underset{\sim}{B}}_E & \hat{\underset{\sim}{B}}_D \end{array}\right] \qquad (12)$$

C-cotree D-E tree

From $\underset{\sim}{B}\underset{\sim}{Q}^T = \underset{\sim}{0}$ [5,p.97], we obtain

$$\underset{\sim}{B}_C + \underset{\sim}{Q}_{CD}^T = \underset{\sim}{0} \qquad (13)$$

and

$$\underset{\sim}{B}_E + \underset{\sim}{Q}_{ED}^T = \underset{\sim}{0} \qquad (14)$$

From $\hat{\underset{\sim}{B}}\underset{\sim}{Q}^T = \underset{\sim}{0}$, we obtain

$$\underset{\sim}{1}_n + \hat{\underset{\sim}{B}}_D\underset{\sim}{Q}_{CD}^T = \underset{\sim}{0} \qquad (15)$$

Substituting $\underset{\sim}{Q}_{CD}^T$ from (13) into (15), we obtain

$$\underset{\sim}{1}_n - \hat{\underset{\sim}{B}}_D\underset{\sim}{B}_C = \underset{\sim}{0} \qquad (16)$$

Since $\underset{\sim}{B}_C$ is nonsingular [8,p.93], Eq. (16) yields

$$\boxed{\hat{\underset{\sim}{B}}_D = \underset{\sim}{B}_C^{-1}} \qquad (17)$$

Now consider any jth row of $\hat{\underset{\sim}{B}}_D$, which corresponds to the fundamental loop defined by C_j with respect to the D-E tree. Due to the Aligned diode path hypothesis, the nonzero elements in the jth row of $\hat{\underset{\sim}{B}}_D$ and hence the jth row of $\underset{\sim}{B}_C^{-1}$, must all be equal to +1 or -1. Since $\underset{\sim}{B}_C^{-1}$ satisfies the conditions of Lemma 1, it follows that Inequality (9) has a unique

irreducible solution given by $\underset{\sim}{V}_C = \underset{\sim}{B}_C^{-1}\underset{\sim}{U}E$. Hence the steady-state voltage is given by

$$\underset{\sim}{V}_C = \underset{\sim}{B}_C^{-1}\underset{\sim}{U}E = \hat{\underset{\sim}{B}}_D\underset{\sim}{U}E \tag{18}$$

Let us next observe that the D-E cutset constraint (c) implies each element of $\underset{\sim}{Q}_{ED}$ in Eq. (11) is equal to either +1 or -1. It follows from Eq. (14) that every element of $\underset{\sim}{B}_E$ is either +1 or -1. According to the definition of $\underset{\sim}{U}$ in Inequality (9), we see that all elements of $\underset{\sim}{U}$ are equal to 1. Therefore, the steady-state solution (18) may be rewritten as

$$\underset{\sim}{V}_C = \hat{\underset{\sim}{B}}_D\underset{\sim}{E} \tag{19}$$

where $\underset{\sim}{E} \triangleq [E,E,\ldots,E]^T$.

Since for any jth row of $\hat{\underset{\sim}{B}}_D$, the nonzero elements are all 1, or all -1, it is clear from Eq. (19) that

$$V_{Cj} = \pm k_j E \tag{20}$$

where k_j is the total number of nonzero elements in the jth row of $\hat{\underset{\sim}{B}}_D$, which is simply the number of diodes in the fundamental loop defined by C_j with respect to the D-E tree.

Now if we redefine the reference polarity of each capacitor voltage V_{Cj} so that V_{Cj} is aligned with the forward bias direction of the diodes, then Eq. (20) reduces to:

$$V_{Cj} = k_j E \tag{21}$$

This completes the proof of Theorem 1. ¤

Corollary 1. For each voltage multiplier network N_{VM} generated by Algorithm VM of Section 2, if $v_i = E \sin \omega t$, $E > 0$, then the output voltage under no load condition is given precisely by

$$V_{Cn} = nE$$

Proof: Observe that N_{VM} satisfies all hypotheses of Theorem 1. Moreover, since the reference polarity of the output voltage is chosen, by assumption, so that it is positive, it follows that $V_{Cn} = k_n E$. An examination of Steps 3 and 4 shows that the fundamental loop defined by C_n with respect to the D-E tree contains all n diodes, therefore $V_{Cn} = nE$. □

With the aid of Theorem 1, the conventional voltage multiplier circuits of Figs. 2 and 3, as well as the new circuits of Fig. 6(a) and Fig. 11 can now all be solved by inspection. The solutions of the steady-state voltage are indicated in the figures. Observe that the answers obtained earlier in Section 1 for the circuits of Figs. 2 and 3 using the Intuitive Method are in fact correct. However, for the circuit of Fig. 11, this intuitive method cannot be applied. In any event, since Theorem 1 is much easier to use, there is no reason to resort to the intuitive method of Section 1, even if it is applicable.

Remarks:

(1) Theorem 1 remains valid for any periodic function $v_i(t)$ as long as $E \triangleq \max[v_i(t)] > 0$, and $\min[v_i(t)] = -E$.

(2) It follows from Eq. (18) that in order to attain the highest capacitor voltage, we should make all elements of $\underset{\sim}{U}$ nonzero. This in turn requires that all elements in $\underset{\sim}{B}_E$ and $\underset{\sim}{Q}_{ED}$ be nonzero [see Eqs. (9) and (14)]. From Eq. (11), a $\underset{\sim}{Q}_{ED}$ with all nonzero elements is equivalent to the requirement

that all diodes and the voltage source form a cutset, a condition introduced earlier in Section 2 through intuitive reasoning, and which serves as a hypothesis for Theorem 1:

(3) It follows from Eq. (19) that the maximum capacitor voltage magnitude $|V_C| = nE$ can be attained only with a row of $\hat{B}_D$ having all elements nonzero and of the same sign. This immediately leads to the "aligned-diode path" constraint introduced in Section 2, and which serves also as a hypothesis for Theorem 1.

(4) If all diodes have a cut-in voltage $V_r > 0$ (i.e., the diode is characterized by $i_D \leq 0$, $v_D - V_r \leq 0$, and $i_D(v_D - V_r) = 0$), then the basic Inequality (9) becomes $B_C V_C \geq U(E-V_r)$, and Theorem 1 is easily extended to give $V_{Cj} = \pm k_j(E-V_r)$. Hence, for an n-fold voltage multiplier, the output voltage will be actually lower than the ideal output voltage $V_o = nE$ by nV_r volts.

(5) From Eqs. (4) and (18), it is easily seen that the peak reverse voltage experienced by every diode is 2E.

4. Steady-State Analysis -- With Load

In the previous sections, we have considered two voltage quadruplers [Fig. 1(c) and 6(a)]. We now ask which is the better circuit? To answer this question, we must first define some criteria for "goodness." For example, if we are most concerned with the capacitor dielectric breakdown requirements, then Fig. 1(c) might be selected because its four capacitors are charged to [E,2E,2E,4E] , whereas the corresponding capacitor voltages for Fig. 6(a) are [E,2E,3E,4E] . But in many cases we may be more concerned with the voltage regulation, i.e., the drop in the output voltage when a load is present, in the form of an equivalent resistor R_L connected in parallel with the output capacitor C_n (see Fig. 12(a)). In order to derive

a quantitative comparison of such voltage drops, we shall extend the concept of output resistance of a linear circuit to voltage multipliers. This will be done after we make some simplifying assumptions concerning loaded voltage multipliers.

For a given value of R_L, the steady-state output voltage $v_o(t)$ and load current $i_L(t)$ will be periodic with the same period $T = 1/f$ of the input waveform. Since our objective is to obtain a dc output voltage, it is desirable to choose as large a value of the capacitance C_n as possible in order to reduce the ripple components in $v_o(t)$ and $i_L(t)$. For the purpose of carrying out a quantitative analysis, we will assume that $C_n \to \infty$ so that the output voltage becomes a constant dc voltage $v_o(\infty) = V_o = V_{Cn}$ in <u>steady state</u>. The exact value of $v_o(\infty)$ of course depends on the amplitude E and frequency $f = \omega/2\pi$ of $v_i(t)$, as well as on the load current I_L drawn by the equivalent load resistor R_L, and the values of the remaining capacitors; namely,

$$v_o(\infty) = V_o(E,\omega;I_L,C_1,C_2,\ldots,C_{n-1}) \tag{22}$$

The voltage regulation of the multiplier depends on the <u>sensitivity</u> of V_o relative to I_L, and a convenient measure of this sensitivity is therefore given by

$$R_o \triangleq -\frac{\partial V_o}{\partial I_L} \tag{23}$$

where R_o has the unit of resistance and will henceforth be called the <u>output resistance</u> of this voltage multiplier. Notice that the negative sign in Eq. (23) is due to our reference direction of I_L in Fig. 12(b) which is out of the one-port seen by the load resistor R_L. Note also that Eq. (23) implicitly assumes $C_n \to \infty$.

We shall now describe a method for calculating R_o for any voltage multiplier N_{VM} generated by Algorithm VM. To facilitate the discussions we shall assume without loss of generality that the reference polarity of the input voltage $v_i(t)$ has been assigned in such a way that D_n -- the diode in series with the output capacitor C_n -- conducts during positive peaks of $v_i(t) = E \sin \omega t$. We will let t_p and t_n denote the positive peak and negative peak instants of $v_i(t)$, i.e., $v_i(t_p) = E$ and $v_i(t_n) = -E$. The calculation of R_o is accomplished in two stages.

Stage 1. Calculation of Surge Charges.

During each period $T = \frac{2\pi}{\omega}$, the charge passing through the load R_L is given by

$$\Delta q_L = I_L \cdot T = I_L/f \tag{24}$$

where I_L is a constant current in view of our assumption that $C_n \to \infty$. It was shown in Section 3 that when there is no load ($I_L=0$), all currents in N_{VM} are zero in steady state. However, when a load current is drawn ($I_L \neq 0$) thereby causing the output voltage to drop slightly, currents will also be flowing in the other branches of the network for short time intervals Δt just before the positive and negative peaks of $v_i(t)$. The surge charges through a branch with current $i(t)$ are therefore given, respectively, by

$$\Delta q^+ \triangleq \int_{t_p-\Delta t}^{t_p} i(\tau)d\tau \tag{25}$$

and

$$\Delta q^- \triangleq \int_{t_n-\Delta t}^{t_n} i(\tau)d\tau \tag{26}$$

The diodes $D_n, D_{n-2}, \ldots$ will be collectively denoted by D_+ to emphasize that they conduct near the positive peak of $v_i(t)$ from $t_p-\Delta t$ to t_p. Similarly, the diodes $D_{n-1}, D_{n-3}, \ldots$ will be denoted by D_- to emphasize that they conduct near the negative peaks of $v_i(t)$. Since the diodes belonging to D_- (resp; D_+) are cut off during the time interval $(t_p-\Delta t, t_p)$ (resp., $(t_n-\Delta t, t_n)$), it follows that:

$$\Delta \underset{\sim}{q}^{+}_{D_-} = \underset{\sim}{0} \tag{27}$$

$$\Delta \underset{\sim}{q}^{-}_{D_+} = \underset{\sim}{0}$$

Our next task is to determine the remaining surge charges $\Delta \underset{\sim}{q}^{+}_{C}$, $\Delta \underset{\sim}{q}^{-}_{C}$, $\Delta \underset{\sim}{q}^{+}_{D_+}$, and $\Delta \underset{\sim}{q}^{-}_{D_-}$ in terms of $\Delta \underset{\sim}{q}_L$. Consider a typical node "m" as shown in Fig. 12. Kirchhoff current law requires that

$$i_{C1}(t) - i_{D1}(t) - i_{C2}(t) = 0 \quad \text{for all } t \tag{28}$$

If we integrate both sides of Eq. (28) from $t_p-\Delta t$ to t_p, we obtain

$$\Delta q^{+}_{C1} - \Delta q^{+}_{D1} - \Delta q^{+}_{C2} = 0 \tag{29}$$

Equation (29) is exactly of the same form as Eq. (28). This means that KCL must be satisfied by the surge charges, provided they are referred to the same time interval.

Although the capacitor voltages $v_{C1}, v_{C2}, \ldots, v_{Cn-1}$ now vary as a function of time, they must nevertheless have constant average values in steady state. This implies that

$$\Delta q^{+}_{C,j} + \Delta q^{-}_{C,j} = 0, \quad j = 1,\ldots,n-1$$

or

$$\Delta q^{-}_{C,j} = -\Delta q^{+}_{C,j}, \qquad j = 1,\ldots,n-1 \tag{30}$$

The condition prevailing at the output tank -- consisting of the output capacitor C_n and the load resistor R_L, Fig. 13(a) -- requires special attention. Refer to Figs. 13(b)-(d), and observe that when the diode D_n conducts near t_p, a surge current flows into C_n. But immediately after t_p, the diode D_n is cut-off. Since C_n is assumed to be infinite, the voltage v_{Cn} is equal to a constant V_{Cn} (the steady-state voltage). This voltage maintains the constant load current $I_L = -i_{Cn} = V_{Cn}/R_L$ throughout the whole period. Since there should be no net increase or decrease of the charge on C_n in steady state, it follows from Fig. 13(a) that whatever surge charge Δq^+_{Cn} injected into C_n during the short interval Δt near the positive peak t_p must be transferred to the load resistor R_L; namely:

$$\Delta q^+_{Cn} = I_L \cdot T = \Delta q_L \tag{31}$$

Since D_n is connected in series with C_n, KCL requires that

$$\Delta q^+_{Dn} = \Delta q^+_{Cn} = \Delta q_L \tag{32}$$

To determine other diode surge charges, consider first the case n is even. The network N_{VM} has an aligned diode path starting from node 1 and terminating at node n+1. Thus for each node j = 2,3,...,n-1, there are exactly two diodes connected to it, with one directed toward node j, and the other away from node j. Besides, there are two or more capacitors (the number of capacitors is unimportant in the argument) connected to node j. By way of illustration, consider node 3 in Fig. 3(b). We have,

$$\text{near } t_p: \quad \Delta q^+_{D1} - \Delta q^+_{C1} + \Delta q^+_{C3} = 0 \tag{33}$$

$$\text{near } t_n: \quad -\Delta q^-_{D2} - \Delta q^-_{C1} + \Delta q^-_{C3} = 0 \tag{34}$$

Adding Eqs. (33) and (44) and invoking Eq. (30) we obtain

$$\Delta q^{+}_{D1} = \Delta q^{-}_{D2}$$

Thus the two diode surge charges have the same magnitude although they occur at different time intervals. Similar situation applies at nodes 3,4,...,n-1and also for the case n is odd. Therefore we conclude that for N_{VM}, all diode surge charges are equal to Δq_L, i.e., if we define $\Delta \underset{\sim}{q}^{+}_{D_+} \triangleq [\Delta q^{+}_{Dn}, \Delta q^{+}_{Dn-2}, \ldots]^T$ and $\Delta \underset{\sim}{q}^{-}_{D_-} \triangleq [\Delta q^{-}_{Dn-1}, \Delta q^{-}_{Dn-3}, \ldots]^T$, then we have

$$\Delta \underset{\sim}{q}^{+}_{D_+} = \Delta \underset{\sim}{q}^{-}_{D_-} = \Delta \underset{\sim}{q}_L \tag{35}$$

where $\Delta \underset{\sim}{q}_L \triangleq [\Delta q_L, \Delta q_L, \ldots, \Delta q_L]^T$.

We shall now turn our attention to the calculation of $\underset{\sim}{q}^{+}_{cn}$. This is easily done by applying KCL to N_{VM} near $t = t_p$. During this time interval, all diodes in the D_- group $\{D_{n-1}, D_{n-3}, \ldots\}$ are cut-off, whereas each diode belonging to the D_+ group $\{D_n, D_{n-2}, \ldots\}$ behaves as a current source. The capacitor surge charges $\Delta \underset{\sim}{q}^{+}_{C}$ can be expressed in terms of $\Delta \underset{\sim}{q}^{+}_{D_+}$ through a relationship similar to Eq. (5). An explicit formula for $\Delta \underset{\sim}{q}^{+}_{C}$ will now be derived.

Further partition the fundamental loop matrix given by Eq. (3) as follows:

$$\underset{\sim}{B} = [\underset{\sim}{B}_C \; \underset{\sim}{B}_E \; \underset{\sim}{1}_n] = \begin{array}{c} \overbrace{}^{C} \; \overbrace{}^{E} \; \overbrace{}^{D_+} \; \overbrace{}^{D_-} \\ \left[\begin{array}{cc|cc} \underset{\sim}{B}^{+}_{C} & \underset{\sim}{B}^{+}_{E} & \underset{\sim}{1} & \underset{\sim}{0} \\ \hline \underset{\sim}{B}^{-}_{C} & \underset{\sim}{B}^{-}_{E} & \underset{\sim}{0} & \underset{\sim}{1} \end{array}\right] \\ \underbrace{}_{\text{C-E tree}} \quad \underbrace{}_{\text{D-cotree}} \end{array} \tag{36}$$

The associated fundamental cutset matrix is given by:

$$\underset{\sim}{Q} = \begin{array}{c} \overbrace{}^{C} \overbrace{}^{E} \overbrace{}^{D_+} \overbrace{}^{D_-} \\ \left[\begin{array}{c|c|c|c} \underset{\sim}{1}_n & \underset{\sim}{0} & -(\underset{\sim}{B}_C^+)^T & -(\underset{\sim}{B}_C^-)^T \\ \hline \underset{\sim}{0} & 1 & -(\underset{\sim}{B}_E^+)^T & -(\underset{\sim}{B}_E^-)^T \end{array}\right] \\ \underbrace{}_{\text{C-E tree}} \quad \underbrace{}_{\text{D-cotree}} \end{array}$$

Let the surge charge vector $\Delta\underset{\sim}{q}$ be similarly partitioned. Using $\underset{\sim}{Q}\cdot\Delta\underset{\sim}{q}^+ = \underset{\sim}{0}$ and $\Delta\underset{\sim}{q}_{D_-}^+ = \underset{\sim}{0}$ from Eq. (27), we obtain

$$\Delta\underset{\sim}{q}_C^+ - (\underset{\sim}{B}_C^+)^T\Delta\underset{\sim}{q}_{D_+}^+ = \underset{\sim}{0} \tag{37}$$

Substituting Eq. (35) for $\Delta\underset{\sim}{q}_{D_+}^+$ in Eq. (37), we obtain

$$\boxed{\Delta\underset{\sim}{q}_C^+ = (\underset{\sim}{B}_C^+)^T\cdot\Delta\underset{\sim}{q}_{D_+}^+ = (\underset{\sim}{B}_C^+)^T\cdot\underset{\sim}{q}_L} \tag{38}$$

Finally, we observe from Eq. (30) that $\Delta\underset{\sim}{q}_C^-$ in simply equal to $-\Delta\underset{\sim}{q}_C^+$. Note that Δq_{Cn}^- does not appear as a surge (see Fig. 13(d)).

Example 4. Consider the voltage quadrupler circuit of Fig. 6(a) with a load resistor connected across C_4. The fundamental loop matrix for this circuit is given by

$$\underset{\sim}{B} = \begin{array}{c} \overbrace{}^{\text{C-E tree}} \overbrace{}^{D_+} \overbrace{}^{D_-} \\ \left[\begin{array}{ccccc|c|cc|cc} C_1 & C_2 & C_3 & C_4 & E & D_4 & D_2 & D_3 & D_1 \\ \hline 0 & 0 & -1 & 1 & -1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \end{array}\right] \end{array} \tag{39}$$

Hence we identify

$$\underset{\sim}{B}_C^+ = \begin{bmatrix} 0 & 0 & -1 & 1 \\ -1 & 1 & 0 & 0 \end{bmatrix}$$

From Eq. (35): $\Delta q_{D1}^- = q_{D2}^+ = \Delta q_{D3}^- = \Delta q_{D4}^+ = \Delta q_L$

From Eq. (38): $\Delta \underset{\sim}{q}_C^+ = (\underset{\sim}{B}_C^+)^T \Delta \underset{\sim}{q}_L = [-\Delta q_L, \Delta q_L, -\Delta q_L, \Delta q_L]^T$.

From Eq. (30): $\Delta \underset{\sim}{q}_C^- = [\Delta q_L, -\Delta q_L, \Delta q_L, -\Delta q_L]^T$.

Stage 2. Calculation of Capacitor Voltages

In Section 3, we have shown that the steady-state solution of N_{VM} when $I_L = 0$ must satisfy Eq. (18); namely,

$$\underset{\sim}{B}_C \underset{\sim}{V}_C = \underset{\sim}{U}\underset{\sim}{E} \tag{40}$$

Substituting this equation into Eq. (8), we observe that in every scalar equation of Eq. (8), the equality sign will be reached periodically, at positive peaks or at negative peaks of $v_i(t)$. The physical meaning is that for this class of networks, each diode reach the breakpoint ($i_D = 0$, $v_D = 0$) periodically in steady state. Now when a load is connected across C_n to draw current I_L, the diodes will not only reach the breakpoint, but will actually be forward biased for a brief time interval. In particular, the diodes in the D_+ group $\{D_n, D_{n-2}, \ldots\}$ will be conducting currents from $t_p - \Delta t$ to t_p, while the diodes in the D_- group $\{D_{n-1}, D_{n-3}, \ldots\}$ will be conducting currents from $t_n - \Delta t$ to t_n. Therefore, in applying Eq. (40), the scalar equations should be separated into two groups, one applicable at $t = t_p$, while the other applicable at $t = t_n$. The matrix $\underset{\sim}{B}$ in Eq. (36) has already been partitioned for this purpose. Hence, Eq. (40) decomposes into two equations:

$$\underset{\sim}{B}_C^+ \underset{\sim}{V}_C^+ = \underset{\sim}{U}^+ E \tag{41}$$

$$\underset{\sim}{B}_C^- \underset{\sim}{V}_C^- = \underset{\sim}{U}^- E \tag{42}$$

where $\underset{\sim}{U}^+$ and $\underset{\sim}{U}^-$ are associated with $\underset{\sim}{B}_E^+$ and $\underset{\sim}{B}_E^-$ in Eq. (40), respectively. See the explanatory note in Inequality (9) for the construction of $\underset{\sim}{U}^+$ and $\underset{\sim}{U}^-$ from $\underset{\sim}{B}_E^+$ and $\underset{\sim}{B}_E^-$, respectively.

For each capacitor C_j, the surge charge Δq_{Cj}^+ has been found earlier by the use of Eq. (38). The voltage difference $V_{Cj}^+ - V_{Cj}^-$ is therefore given by

$$V_{Cj}^+ - V_{Cj}^- = \Delta q_{Cj}^+ / C_j, \quad j = 1,2,\ldots,n \tag{43}$$

Again, the output capacitor C_n requires special attention. Since C_n is assumed to be infinitely large, we have $V_{Cn}^+ = V_{Cn}^- = V_o$. Equation (43) may be expressed more compactly as

$$\underset{\sim}{V}_C^+ - \underset{\sim}{V}_C^- = \underset{\sim}{S}\, \Delta \underset{\sim}{q}_C^+ \tag{44}$$

where $\underset{\sim}{S} \triangleq \text{diag.}\left(\frac{1}{C_1}, \frac{1}{C_2}, \ldots, \frac{1}{C_n} \right)$.

From Eqs. (42), (44), and (38), we can eliminate $\underset{\sim}{V}_C^-$ and $\Delta \underset{\sim}{q}_C^+$ to obtain

$$\underset{\sim}{B}_C^- \underset{\sim}{V}_C^+ = \underset{\sim}{U}^- E + \underset{\sim}{B}_C^- \underset{\sim}{S} (\underset{\sim}{B}_C^+)^T \Delta \underset{\sim}{q}_L \tag{45}$$

Equation (41) and (45) can be combined into a single equation

$$\underset{\sim}{B}_C \underset{\sim}{V}_C^+ = \begin{bmatrix} \underset{\sim}{B}_C^+ \\ \underset{\sim}{B}_C^- \end{bmatrix} \underset{\sim}{V}_C^+ = \begin{bmatrix} \underset{\sim}{U}^+ \\ \underset{\sim}{U}^- \end{bmatrix} \underset{\sim}{E} + \begin{bmatrix} \underset{\sim}{0} \\ \underset{\sim}{B}_C^- \underset{\sim}{S} (\underset{\sim}{B}_C^+)^T \Delta \underset{\sim}{q}_L \end{bmatrix} \tag{46}$$

Since $\underset{\sim}{B}_C$ is nonsingular, and its inverse is given by $\underset{\sim}{B}_C^{-1} = \hat{\underset{\sim}{B}}_D$ [see Eq. (17)], we obtain the following explicit formula for $\underset{\sim}{V}_C^+$:

$$\boxed{\underset{\sim}{V}_C^+ = \hat{\underset{\sim}{B}}_D \underset{\sim}{U} E + \hat{\underset{\sim}{B}}_D \begin{bmatrix} \underset{\sim}{0} \\ \underset{\sim}{B}_C^- \underset{\sim}{S} (\underset{\sim}{B}_C^+)^T \Delta \underset{\sim}{q}_L \end{bmatrix}} \tag{47}$$

where

$\underset{\sim}{B}_C^+$ and $\underset{\sim}{B}_C^-$ are defined in Eq. (36);

$\underset{\sim}{U}$ is defined in Eq. (9)

$\underset{\sim}{S}$ is defined in Eq. (44)

$\Delta \underset{\sim}{q}_L$ is defined by Eq. (35) and (24)

$\hat{\underset{\sim}{B}}_D$ is defined in Eq. (12)

If $V_o = V_{Cn}^+$ is the only information desired, the calculation of Eq. (47) should be carried out without the full effort of finding $\underset{\sim}{V}_C^+$. For the voltage multipliers generated by Algorithm VM, we have $\underset{\sim}{U} = [1,1,\ldots,1]^T$, $V_0 = V_{Cn}^+$, and the n-th row of $\hat{\underset{\sim}{B}}_D = [1,1,1,\ldots,1]$. Define $\underset{\sim}{W} \triangleq [1,1,\ldots,1]^T$, then Eq. (47) leads to

$$\boxed{V_o = nE + \underset{\sim}{W}^T \underset{\sim}{B}_C^- \underset{\sim}{S} (\underset{\sim}{B}_C^+) \Delta \underset{\sim}{q}_L} \tag{48}$$

Substituting Eq. (24) for $\Delta \underset{\sim}{q}_L$ in Eq. (48) and using Eq. (23), we obtain the following explicit formula for the output resistance:

$$\boxed{R_o = \left(\underset{\sim}{W}^T \underset{\sim}{B}_C^- \underset{\sim}{S} \underset{\sim}{B}_C^+ \underset{\sim}{W} \right) / f} \tag{49}$$

The explicit formulas (48) and (49) have been derived for VM circuits where the output capacitor C_n is in series with a diode D_n. Voltage multiplier circuits generated by Algorithm VM may or may not have a series-connected C_n-D_n output tank (see the tripler of Fig. 11 for an example of the latter case). It can be shown that Eqs. (48) and (49) are also valid for the latter case, and even for the case of finite (but

large) C_n, provided that we consider V_o to be V^+_{Cn}.

We shall now illustrate the use of the explicit formulas (48) and (49) with an example.

Example 5. Let us continue with the voltage quadrupler circuit of Example 4 [Fig. 6(a)]. Suppose that $C_1 = C_2 = C_3 = C$ and $C_4 \to \infty$.

$$\underset{\sim}{S} = \text{diag}\left(\frac{1}{C}, \frac{1}{C}, \frac{1}{C}, 0\right)$$

From Eq. (39), we obtain

$$\underset{\sim}{B}^+_C = \begin{bmatrix} 0 & 0 & -1 & 1 \\ -1 & 1 & 0 & 0 \end{bmatrix}$$

$$\underset{\sim}{B}^-_C = \begin{bmatrix} 0 & -1 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

Substituting the above matrices into Eqs. (48) and (49), we obtain

$$V_o = 4E - \frac{3I_L}{fC} \tag{50}$$

and

$$R_o = \frac{3}{fC} \tag{51}$$

By the same method, we find the output resistance for the voltage quadrupler circuit of Fig. 1(c) to be $R_o = 6/fC$. The output resistance of Fig. 1(c) can also be obtained from the equation given in [5,Eq.(3)] by letting n=4. It is important to note that R_o for the new voltage quadrupler circuit of Fig. 6(a) is only one-half of the conventional quadrupler of Fig. 1(c).

Using Eq. (49), we can prove the following theorem which constitutes the second major result of this paper.

Theorem 2. For any network generated by Algorithm VM (i.e., an nC-nD-1E network which, besides satisfying the four conditions of Theorem 1, has the D-path or D-E-path terminated in C_n), if the output capacitor $C_n \to \infty$, then the output resistance is given by

$$R_o = \frac{1}{f} \sum_{j=1}^{n-1} \frac{\left(\frac{m_j}{2}\right)^2}{C_j} \tag{52}$$

where m_j is the number of diodes contained in the cutset defined by C_j with respect to the C-E tree.

Proof: In the derivation of Eq. (32), we have assumed that the output capacitor C_n is in series with the diode D_n. This condition can be relaxed. By a reasoning similar to that given in Eqs. (33)-(34), we can easily see that $\Delta q_{Dn}^{+} = \Delta q_L$, as long as one node of C_n has only one diode D_n, and possibly several other capacitors connected to it. Since this is true for all circuits generated by Algorithm VM, we can repeat the derivation of the subsequent equations (33)-(49). Therefore the explicit formulas (48) and (49) are valid for all circuits generated Algorithm VM.

Equation (49) has a topological interpretation. First, note that from Eq. (49)

$$R_o = -\frac{1}{f} \sum \left[\text{all elements of } \underset{\sim}{B}_C^{-} \underset{\sim}{S} (\underset{\sim}{B}_C^{+})^T\right] \tag{53}$$

Since $\underset{\sim}{S}$ is a diagonal matrix [see Eq. (44)], the triple product $\underset{\sim}{B}_C^{-1} \underset{\sim}{S} (\underset{\sim}{B}_C^{+})^T$ can be expanded quite easily to give the contribution of $1/C_j$ in the output resistance. We have

$\frac{1}{C_j}$ term in Eq. (53)

$$= -\frac{1}{fC_j}\left[\text{j-th column of } B_{\tilde{C}}^{-}\right]\left[\text{j-th row of } (B_{\tilde{C}}^{+})^T\right]$$

$$= \frac{1}{fC_j}\left[\text{No. of diodes in } D_- \text{ group whose f-loops contain } C_j\right]$$

$$\cdot \left[\text{No. of diodes in } D_+ \text{ group whose f-loops contain } C_j\right]$$

$$= \frac{1}{fC_j}\left[\text{No. of diodes in } D_- \text{ group contained in the cutset defined by } C_j \text{ w.r.t. the C-E tree}\right]$$

$$\cdot \left[\text{No. of diodes in } D_+ \text{ group contained in the cutset defined by } C_j \text{ w.r.t. the C-E tree}\right] \qquad (54)$$

Summing up all of such terms in the expansion of (53) one obtain

$$R_o = \frac{1}{f}\sum_{j=1}^{n-1}\frac{1}{C_j}m_j^+m_j^- \qquad (55)$$

where m_j^+ and m_j^- are the number of diodes in the D_+ group and D_- group, respectively, which are contained in the fundamental cutset defined by C_j with respect to the C-E tree.

Now for any circuit generated by Algorithm VM, we shall show that

$$m_j^+ = m_j^- = \frac{m_j}{2}, \qquad j = 1,2,\ldots,n-1 \qquad (56)$$

Recall that (a) C_n has D_n connected to one node and D_1 connected to the other, with D_n in the D_+ group and D_1 in the D_- group (or vice versa); (b) node labeled 0; if present, has no diode connected to it; (c) each of the other nodes has exactly two diodes connected to it, one in the D_+

group, and the other in the D_- group. Now consider the formation of a cutset defined by C_j, $j \neq n$, with respect to the C-E tree. Removal of C_j from the C-E tree produces two subtrees, which we shall denote by $T_{S,C}$ and $T_{S,C-E}$, with the voltage source in the latter subtree. Now consider the subtree $T_{S,C}$. The fundamental cutset defined by C_j simply consists of all diodes connected between one node of $T_{S,C}$ and another node of $T_{S,C-E}$. Upon reviewing the properties (a)-(c) described above, we immediately conclude that the number of diodes connected to T_{S-C} is even, and are equally divided in the D_+ and D_- groups. Thus, Eq. (56) is valid. As an example, consider Fig. 1(c). For C_1, the fundamental cutset contains all four diodes, with $m_1^+ = 2$, $m_1^- = 2$, and $m_1 = 4$.

Putting Eq. (56) into Eq. (55), we have Eq. (52). This completes the proof of Theorem 2. ¤

We observe that the expressions for the output resistance as shown in Eqs. (1) and (2) of [5] are just special cases of Theorem 2. With Theorem 2, the problem of determining the output resistance is reduced to that of finding the fundamental cutsets defined by the capacitors (with respect to the C-E tree) and counting the diodes in the cutsets. In particular, if we assume $C_1 = C_2 = \ldots = C_{n-1} = C$, then Theorem 2 leads to (see also Eqs. (3) and (4) of [5]) the following expressions for the conventional ladder voltage multipliers:

$$R_o = \begin{cases} \frac{n}{6}\left(\frac{n^2}{2} + 1\right)\frac{1}{fC} & , \text{ for n even, Fig. 3(a)} \\ \frac{n}{12}\left(n^2-1\right)\frac{1}{fC} & , \text{ for n odd, Fig. 3(b)} \end{cases} \tag{57}$$

Since $R_o \propto n^3$, for large n, the voltage regulation is a serious problem

in voltage multipliers of large n. As pointed out earlier, the capacitor voltages for the conventional ladder voltage multiplier are

$$[E,2E,2E,\ldots,2E,nE]$$

The output resistance can be greatly reduced by choosing T_{C0} and T_{C1} to be rooted "star" subtrees (see Fig. 6(a) for example). For such voltage multipliers, Theorem 2 leads to

$$R_o = \frac{(n-1)}{fC} \tag{58}$$

which varies only linearly with n for large n. It can be shown that $R_o = (n-1)/fC$ is the smallest output resistance obtainable with the circuits generated by Algorithm VM. This smallest output resistance is achieved at the expense of more costly capacitors, because the capacitor voltages for this case are $[E,2E,3E,\ldots,(n-1)E,nE]$, instead of $[E,2E,2E,\ldots,2E,nE]$.

5. Conclusion

We have described an algorithm for generating n-fold voltage multiplier circuits with n capacitors and n diodes. It is shown that the conventional ladder VM circuit [4,5] is just a special case generated by our Algorithm VM. A rigorous steady-state analysis for N_{VM} is presented both without load and with load. For the unloaded case, Theorem 1 makes it possible to determine the capacitor voltages by inspection.

Three important factors to be considered in selecting different voltage multiplier circuits are the capacitor voltage ratings, the output resistance, and the common-ground requirement. Consider the voltage

quadruplers for example. Algorithm VM generates a total of 9 distinct quadruplers whose C-E trees and labeling of nodes are shown in Fig. 14(a)-(i). The connection of diodes is shown in Fig. 14(j). After connecting the diodes, Figs. 14(a) and (b) result in the quadruplers of Figs. 1(c) and 6(a), respectively. Figs. 14(c) and (d) lead to two more quadruplers shown in Figs. 15(a) and (b), respectively, both having $R_o=3/fC$ (assuming $C_1=C_2=C_3=C$, and $C_4\to\infty$). The quadruplers derived from Fig. 14(e)-(i) all have $R_o=6/fC$. The following table gives a comparison of the voltage quadruplers based on Fig. 14.

properties / Fig. 14	$R_o \cdot fC$	Capacitor voltages, multiples of E	common-ground
(a), also Fig. 1(c)	6	1,2,2,4	yes
(b), also Fig. 6(a)	3	1,2,3,4	yes
(c), also Fig. 15(a)	3	1,2,3,4	yes
(d), also Fig. 15(b)	3	1,1,2,4	no
(e)	6	1,2,2,4	yes
(f)	6	2,2,3,4	yes
(g)	6	1,2,2,4	no
(h)	6	1,2,2,4	no
(i)	6	2,2,3,4	yes

The properties indicated in the table have also been experimentally verified. From the table, it is seen that Fig. 15(b) is the best voltage quadruplers as far as the output resistance and capacitor voltages are concerned. But this circuit has no common terminal between the input and the output, which makes it unsuitable for some

applications. The quadruplers of Fig. 6(a) and 15(a) are better than the conventional quadrupler of Fig. 1(c) as far as the output resistance is concerned. But the capacitor voltages for the former are [E,2E,3E,4E], whereas those for the latter are [E,2E,2E,4E]. In other words, the third capacitor has E volts higher steady-state voltage across it.

Our conclusion about the selection of voltage multipliers is that the conventional ladder configuration of Fig. 3 is among the best, if the capacitor voltage is the primary concern, and the common ground is a requirement. On the hand, if one can tolerate the use of capacitors with higher voltage ratings, then other voltage multiplier circuits generated by Algorithm VM should be considered as some of them have output resistance smaller than the conventional ladder configuration of Fig. 3.

APPENDIX

Proof of Lemma 1:

Case 1. All non-zero elements of $\underset{\sim}{A}^{-1}$ are positive. The inequality

$$\underset{\sim}{A}\underset{\sim}{X} \geq \underset{\sim}{K} \quad \text{with } \underset{\sim}{K} \geq 0 \tag{59}$$

may be expressed in equivalent form

$$\underset{\sim}{A}\underset{\sim}{X} = \underset{\sim}{K}+\underset{\sim}{S}, \quad \underset{\sim}{S} \geq \underset{\sim}{0} \tag{60}$$

where $\underset{\sim}{S}$ is called the slack vector. Any feasible solution of Eq. (59) may be expressed as

$$\underset{\sim}{X} = \underset{\sim}{A}^{-1}\underset{\sim}{K}+\underset{\sim}{A}^{-1}\underset{\sim}{S}, \quad \underset{\sim}{S} \geq \underset{\sim}{0} \tag{61}$$

Since all non-zero elements of $\underset{\sim}{A}^{-1}$ are positive, then $\underset{\sim}{A}^{-1}\underset{\sim}{K} \geq \underset{\sim}{0}$, and $\underset{\sim}{A}^{-1}\underset{\sim}{S} \geq 0$. The smallest magnitude of each x_i is achieved if, and only if, $\underset{\sim}{S}=\underset{\sim}{0}$. Thus $\underset{\sim}{X} = \underset{\sim}{A}^{-1}\underset{\sim}{K}$ is a irreducible solution, since every x_i has the smallest magnitude possible. To see that any other solution $\underset{\sim}{X}^*(\underset{\sim}{X}^* \neq \underset{\sim}{A}^{-1}\underset{\sim}{K})$ is reducible, refer to the definition and simply let $\tilde{\underset{\sim}{X}} = \underset{\sim}{A}^{-1}\underset{\sim}{K}$. Since $\underset{\sim}{X}^* \geq \underset{\sim}{0}$ and $\tilde{\underset{\sim}{X}} \geq \underset{\sim}{0}$, but $\underset{\sim}{X}^* \geq \tilde{\underset{\sim}{X}}$, then $\underset{\sim}{X}^*$ is a reducible solution.

Case 2. The non-zero elements of some m ($1 \leq m \leq n$) rows of $\underset{\sim}{A}^{-1}$ are negative. Without loss of generality, we assume these to be the first m rows.

Rewrite Eq. (60) as

$$\underset{\sim}{A}\underset{\sim}{X} = [\underset{\sim}{A}_1, \underset{\sim}{A}_2] \begin{bmatrix} \underset{\sim}{X}_1 \\ \underset{\sim}{X}_2 \end{bmatrix} = \underset{\sim}{K}+\underset{\sim}{S}, \quad \underset{\sim}{S} \geq 0 \tag{62}$$

where $\underset{\sim}{A}_1$ has m columns, and $\underset{\sim}{X}_1$ is an m-vector.

Then,

$$\begin{bmatrix} \underset{\sim}{X}_1 \\ \underset{\sim}{X}_2 \end{bmatrix} = \underset{\sim}{A}^{-1}(\underset{\sim}{K}+\underset{\sim}{S})$$

Since $(\underset{\sim}{K}+\underset{\sim}{S})\geq 0$, it follows from the hypothesis concerning the signs of the elements of $\underset{\sim}{A}^{-1}$ that

$$\underset{\sim}{X}_1 \leq \underset{\sim}{0} \ , \quad \underset{\sim}{X}_2 \geq \underset{\sim}{0} \tag{63}$$

Construct another system

$$[-\underset{\sim}{A}_1, \underset{\sim}{A}_2] \begin{bmatrix} \underset{\sim}{Y}_1 \\ \underset{\sim}{Y}_2 \end{bmatrix} = \underset{\sim}{K}+\underset{\sim}{S}, \ \underset{\sim}{S} \geq 0 \tag{64}$$

Then there is a one-to-one correspondence between the solutions of (62) and Eq. (64), namely

$$\underset{\sim}{Y}_1 = -\underset{\sim}{X}_1 \text{ and } \underset{\sim}{Y}_2 = \underset{\sim}{X}_2 \tag{65}$$

With Eq. (65), it is easy to see that two corresponding solutions of Eqs. (62) and (64) are either both reducible, or both irreducible.

For Eq. (64), let us calculate the inverse of the coefficient matrix

$$[-\underset{\sim}{A}_1 \ \underset{\sim}{A}_2]^{-1} = \left\{ [\underset{\sim}{A}_1 \ \underset{\sim}{A}_2] \begin{bmatrix} -\underset{\sim}{1}_m & \underset{\sim}{0} \\ \underset{\sim}{0} & \underset{\sim}{1}_{n-m} \end{bmatrix} \right\}^{-1} = \begin{bmatrix} -\underset{\sim}{1}_m & \underset{\sim}{0} \\ \underset{\sim}{0} & \underset{\sim}{1}_{n-m} \end{bmatrix} \underset{\sim}{A}^{-1}$$

Since by hypothesis the non-zero elements in the first m rows of $\underset{\sim}{A}^{-1}$ are negative, a premultiplication of $\underset{\sim}{A}^{-1}$ by diag. $[-\underset{\sim}{1}_m, \underset{\sim}{1}_{n-m}]$ results in $[-\underset{\sim}{A}_1 \ \underset{\sim}{A}_2]^{-1}$ whose non-zero elements are all positive. It follows from our result in Case 1 that the system defined by Eq. (64) has one, and only one, irreducible solution given by

$$\underset{\sim}{Y} = [-\underset{\sim}{A}_1 \; \underset{\sim}{A}_2]^{-1}\underset{\sim}{K}$$

Hence the system (62) has one, and only one, irreducible solution given by

$$\underset{\sim}{X} = \begin{bmatrix} \underset{\sim}{X}_1 \\ \underset{\sim}{X}_2 \end{bmatrix} = \begin{bmatrix} -\underset{\sim}{Y}_1 \\ \underset{\sim}{Y}_2 \end{bmatrix} = \begin{bmatrix} -\underset{\sim}{1}_m & 0 \\ 0 & \underset{\sim}{1}_{n-m} \end{bmatrix} \cdot [-\underset{\sim}{A}_1 \; \underset{\sim}{A}_2]^{-1} \cdot \underset{\sim}{K}$$

$$= \left\{ [-\underset{\sim}{A}_1 \; \underset{\sim}{A}_2] \begin{bmatrix} -\underset{\sim}{1}_m & \underset{\sim}{0} \\ \underset{\sim}{0} & \underset{\sim}{1}_{n-m} \end{bmatrix} \right\}^{-1} \underset{\sim}{K} = [\underset{\sim}{A}_1 \; \underset{\sim}{A}_2]^{-1}\underset{\sim}{K} = \underset{\sim}{A}^{-1}\underset{\sim}{K}$$

This completes the proof of Lemma 1.

Q.E.D.

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Figure Captions

Fig. 1. A voltage doubler, tripler, and quadrupler.

Fig. 2. (a) A ladder C-D network. (b) output tank.

Fig. 3. An N-fold voltage multipliers derived from a C-D ladder network.

Fig. 4. A simple rectifier circuit.

Fig. 5. An example showing the steady-state voltages depend on the order where the diodes are connected.

Fig. 6. Networks with C-E tree and D-E tree.

Fig. 7. Enumeration of distinct 3C-1E trees.

Fig. 8. A general voltage multiplier configuration.

Fig. 9. An example showing that $\underset{\sim}{B}_C\underset{\sim}{V}_C=\underset{\sim}{U}\underset{\sim}{E}$ gives an incorrect solution.

Fig. 10. Examples and geometrical interpretations for illustrating the concept of irreducible solutions of $\underset{\sim}{A}\underset{\sim}{X} \geqq \underset{\sim}{K}$.

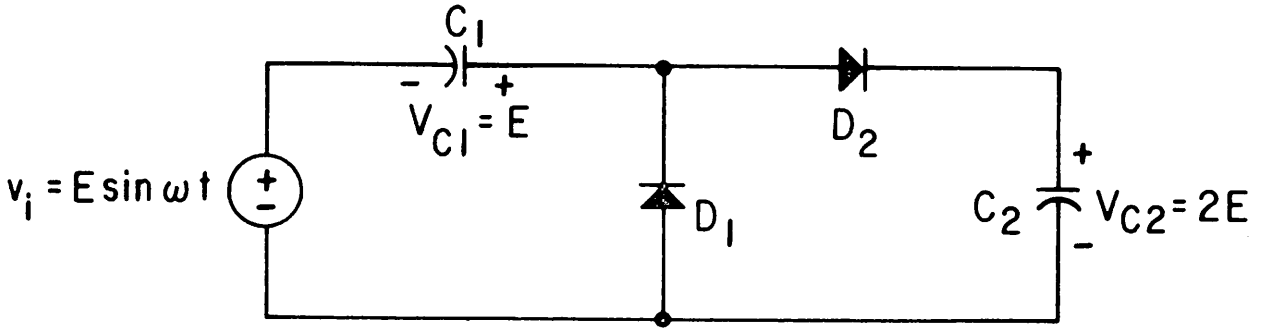
Fig. 11. A voltage tripler defying the intuitive method of solution.

Fig. 12. A voltage multiplier with load connected.

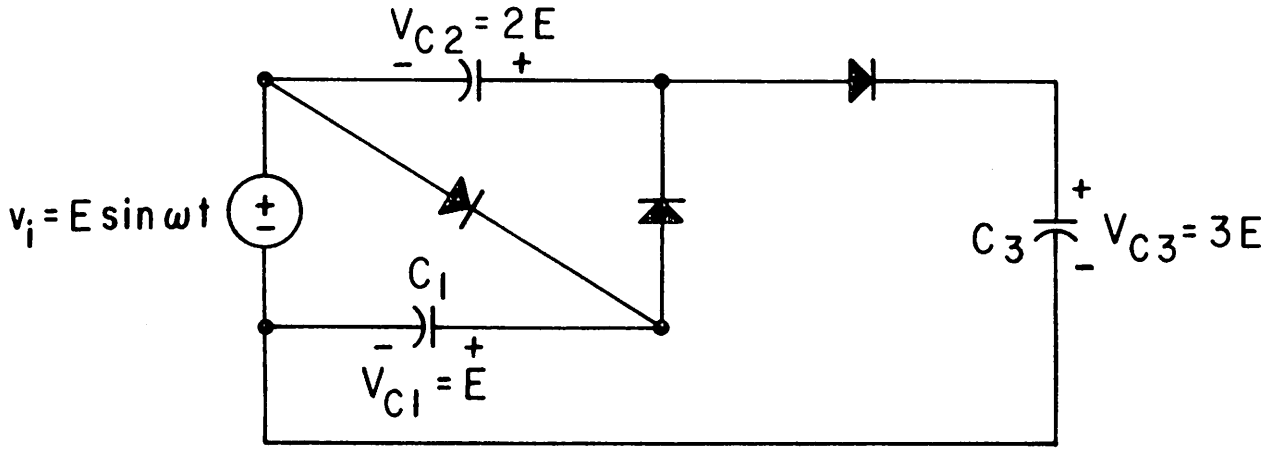
Fig. 13. Current waveforms in the output circuit.

Fig. 14. Generation of voltage quadruplers by Algorithm VM.

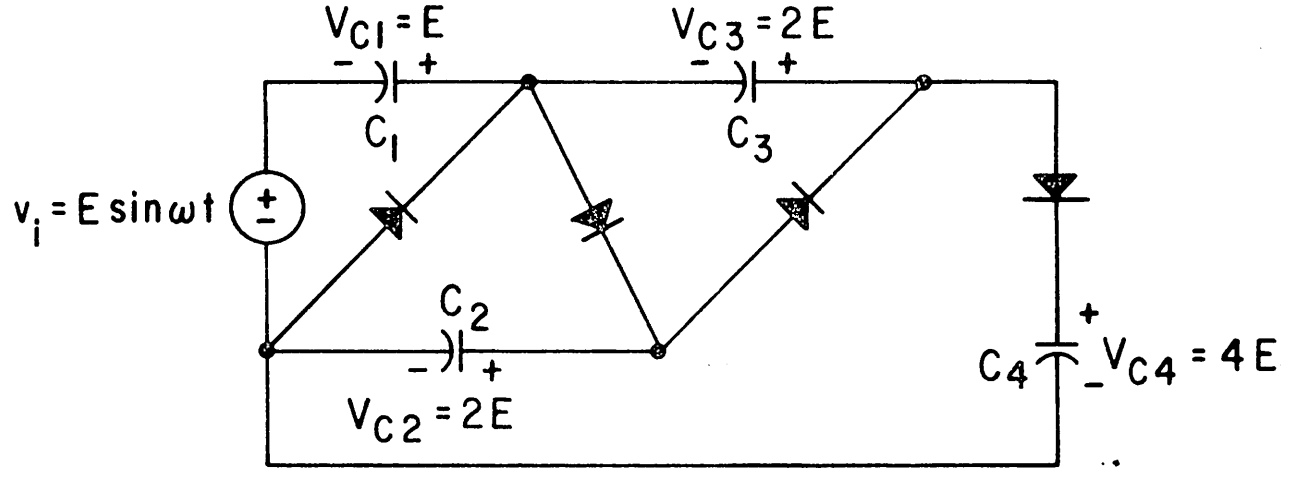
Fig. 15. These two voltage quadruplers, as well as Fig. 6(a), have output resistance $R_o = 3/fC$.


C1
V_C1 = E
D2
D1
v_i = E sin ωt
C2
V_C2 = 2E

(a)


V_C2 = 2E
v_i = E sin ωt
C3
V_C3 = 3E
C1
V_C1 = E

(b)


V_C1 = E
V_C3 = 2E
C1
C3
v_i = E sin ωt
C2
V_C2 = 2E
C4
V_C4 = 4E

(c)

Fig. 1

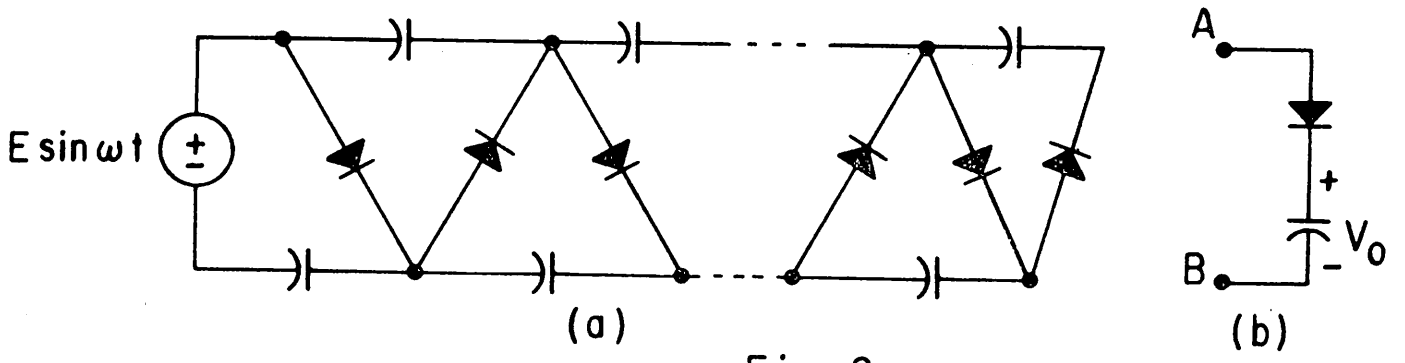
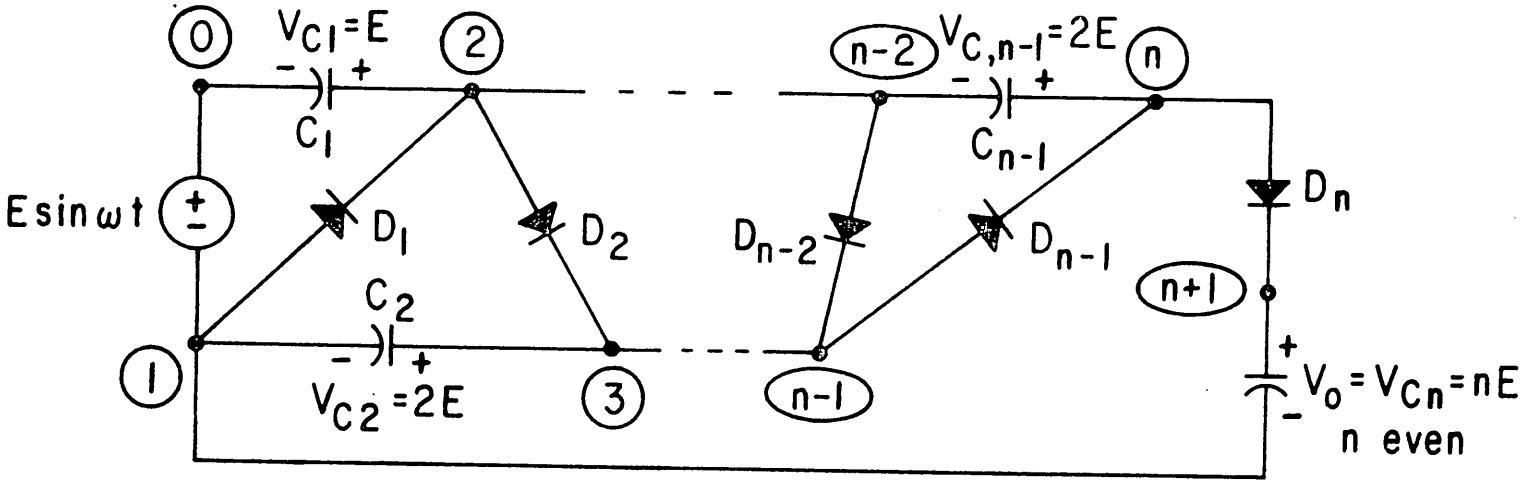
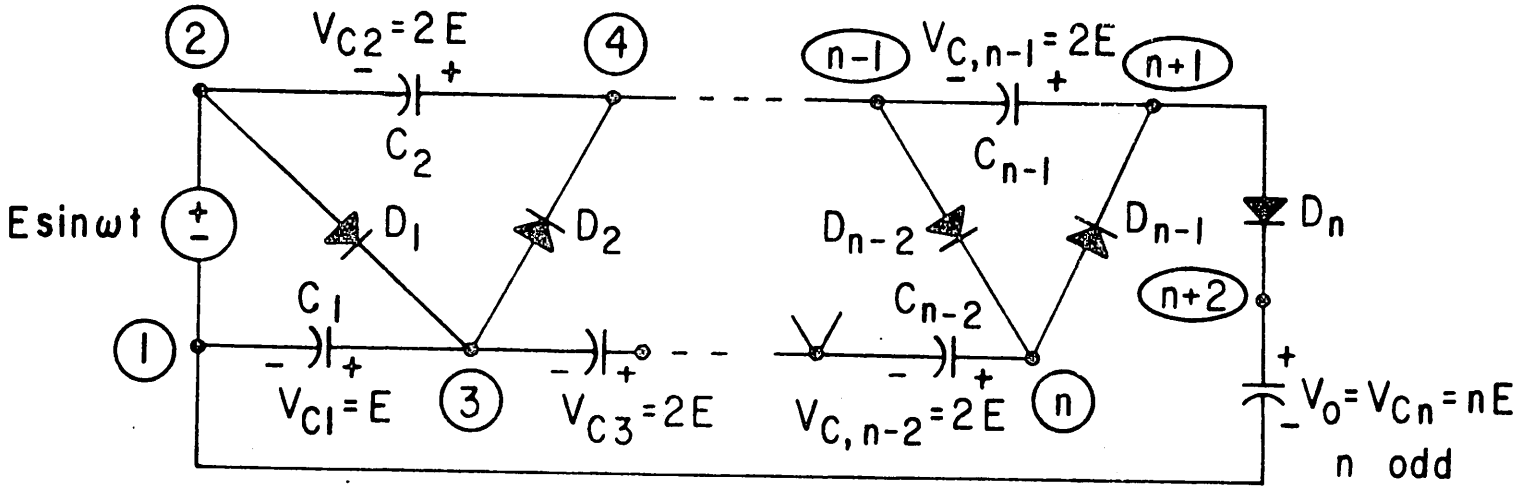

Esinωt
A
B
+
V_o
(a)
(b)

Fig. 2


0
$V_{C1}=E$
2
n-2
$V_{C,n-1}=2E$
n
C_1
C_{n-1}
Esinωt
D_1
D_2
D_{n-2}
D_{n-1}
D_n
n+1
C_2
1
$V_{C2}=2E$
3
n-1
$V_o=V_{Cn}=nE$
n even

(a)


2
$V_{C2}=2E$
4
n-1
$V_{C,n-1}=2E$
n+1
C_2
C_{n-1}
Esinωt
D_1
D_2
D_{n-2}
D_{n-1}
D_n
n+2
C_1
C_{n-2}
1
$V_{C1}=E$
3
$V_{C3}=2E$
$V_{C,n-2}=2E$
n
$V_o=V_{Cn}=nE$
n odd

(b)

Fig. 3

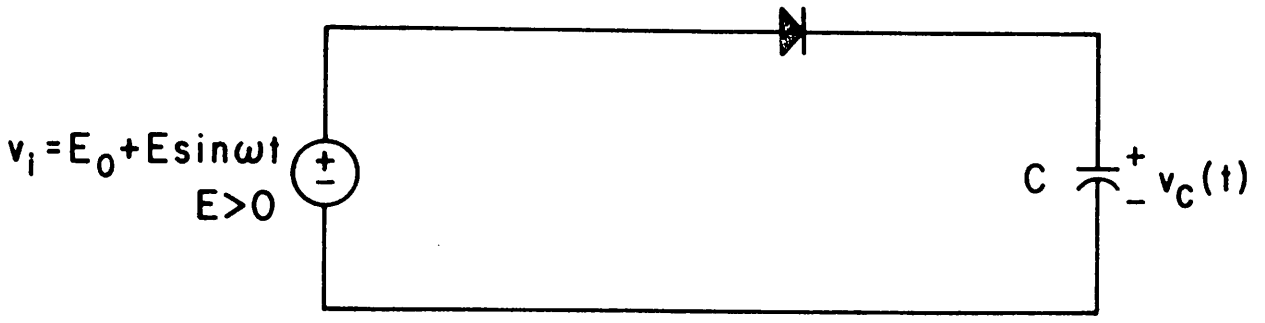

$v_i = E_0 + E\sin\omega t$
$E > 0$
C
$v_c(t)$

Fig. 4

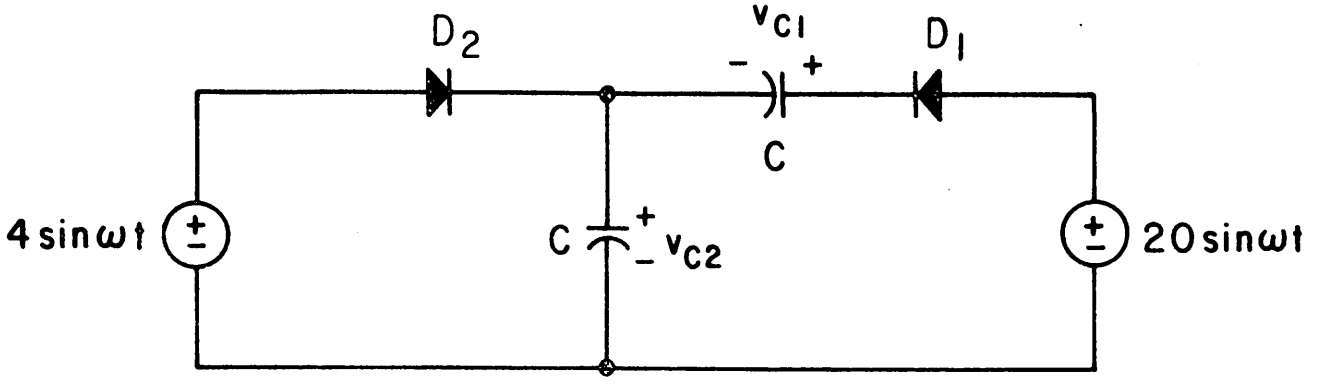
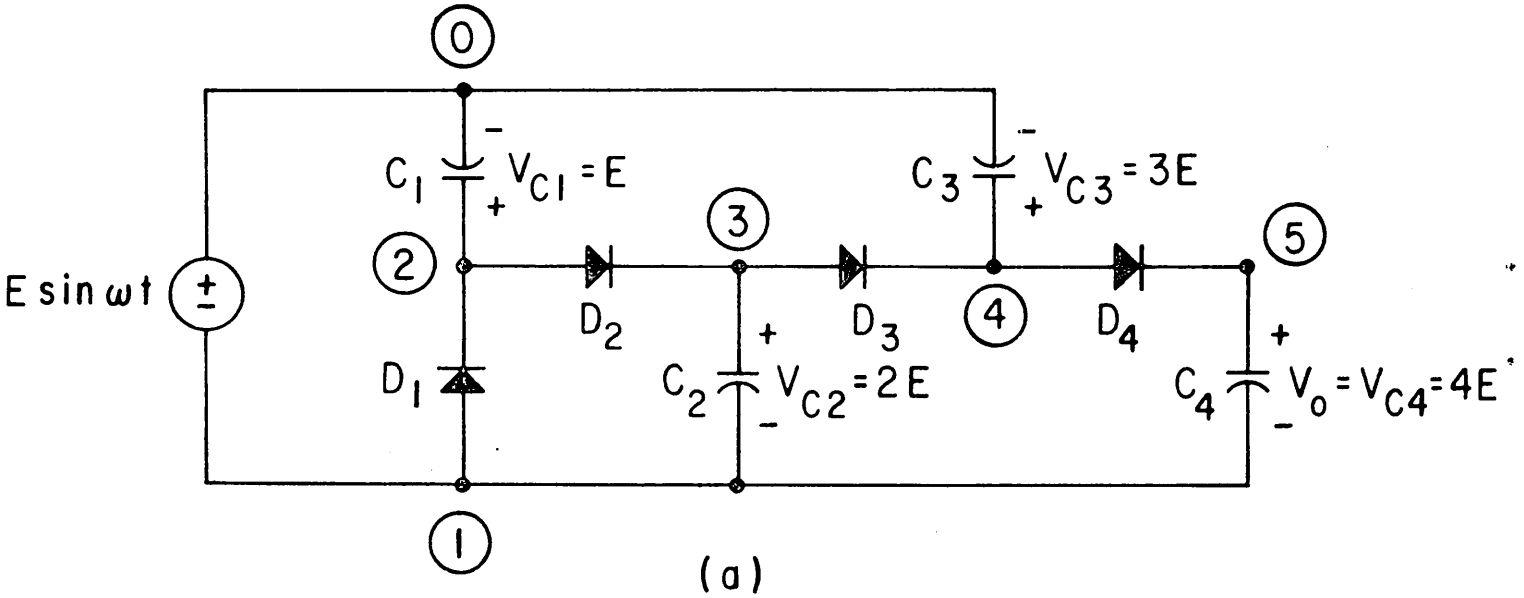
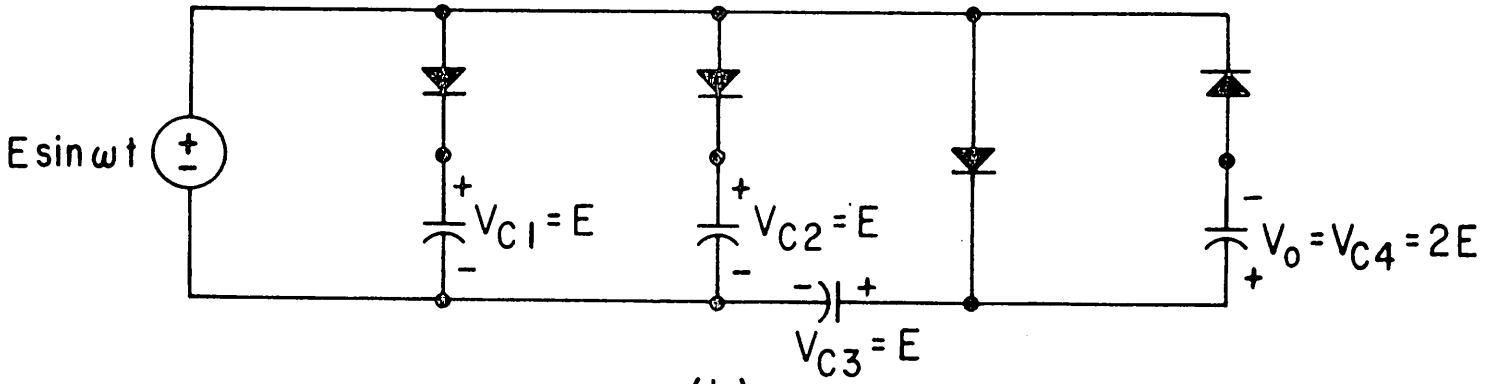

D_2
v_{C1}
D_1
C
$4\sin\omega t$
C
v_{C2}
$20\sin\omega t$

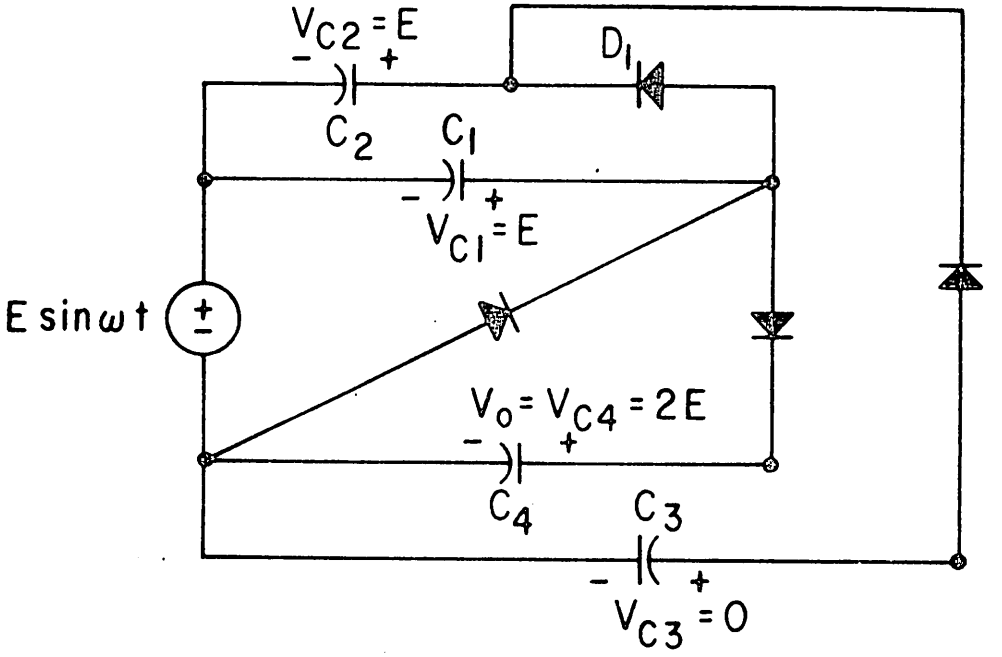
Fig. 5


0
C1
VC1 = E
C3
VC3 = 3E
3
5
2
E sin ωt
D2
D3
4
D4
D1
C2
VC2 = 2E
C4
Vo = VC4 = 4E
1

(a)


E sin ωt
VC1 = E
VC2 = E
Vo = VC4 = 2E
VC3 = E

(b)


VC2 = E
D1
C2
C1
VC1 = E
E sin ωt
Vo = VC4 = 2E
C4
C3
VC3 = 0

(c)

Fig. 6

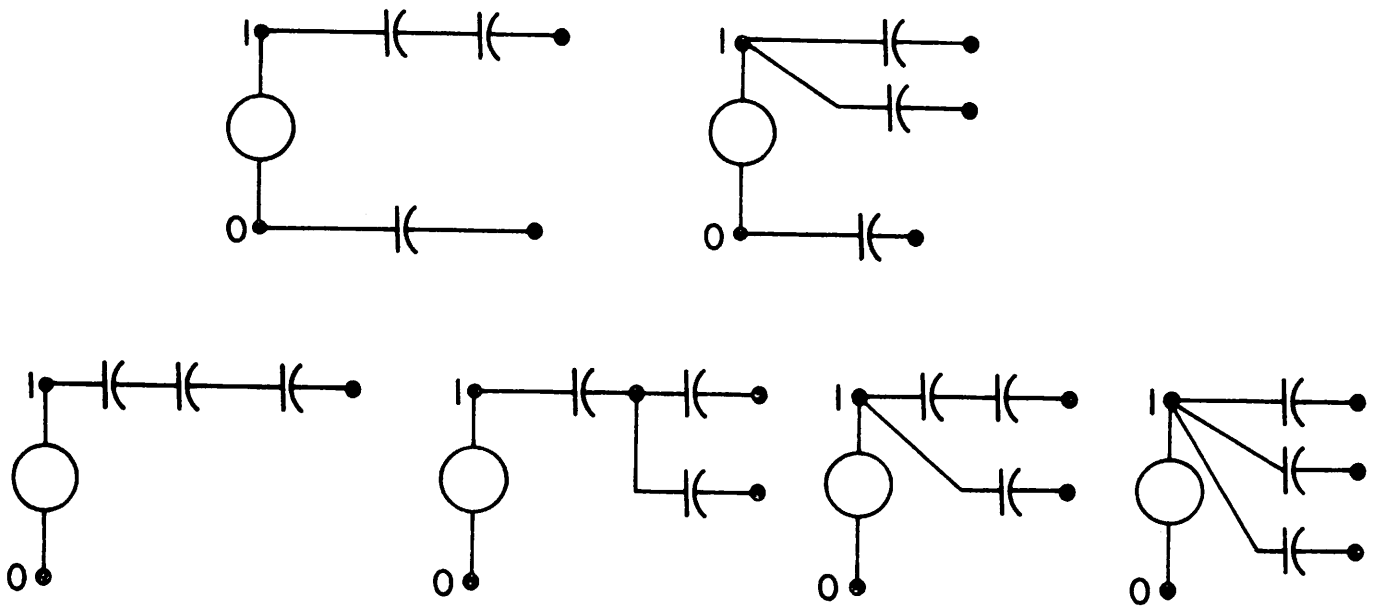


Fig. 7

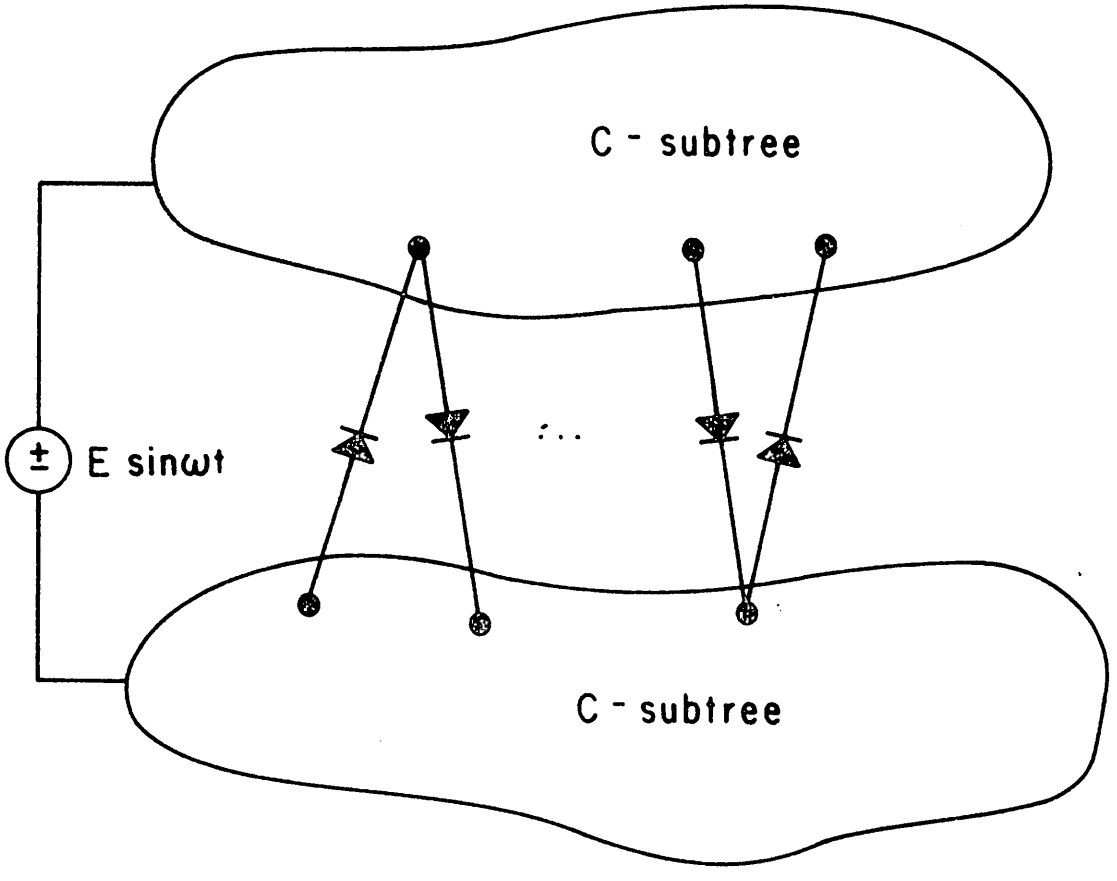


Fig. 8

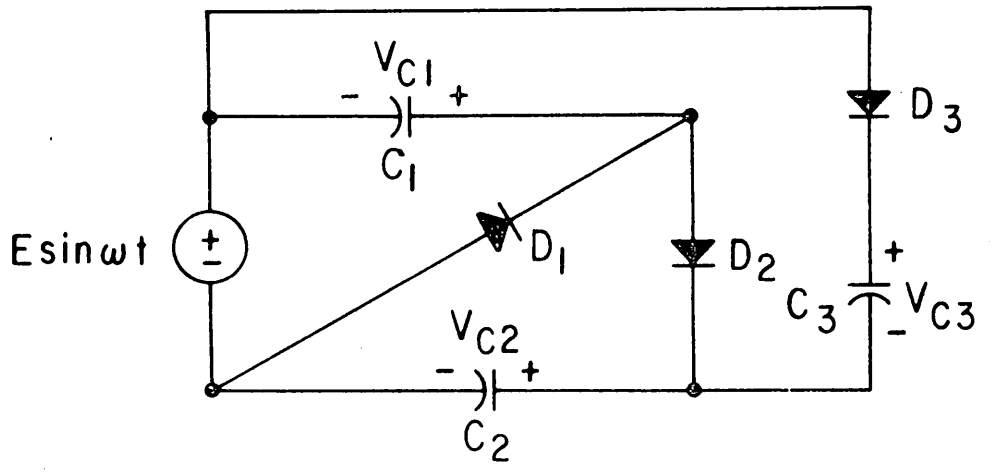

V_{C1}
C_1
D_3
$E\sin\omega t$
D_1
D_2
C_3
V_{C3}
V_{C2}
C_2

Fig. 9

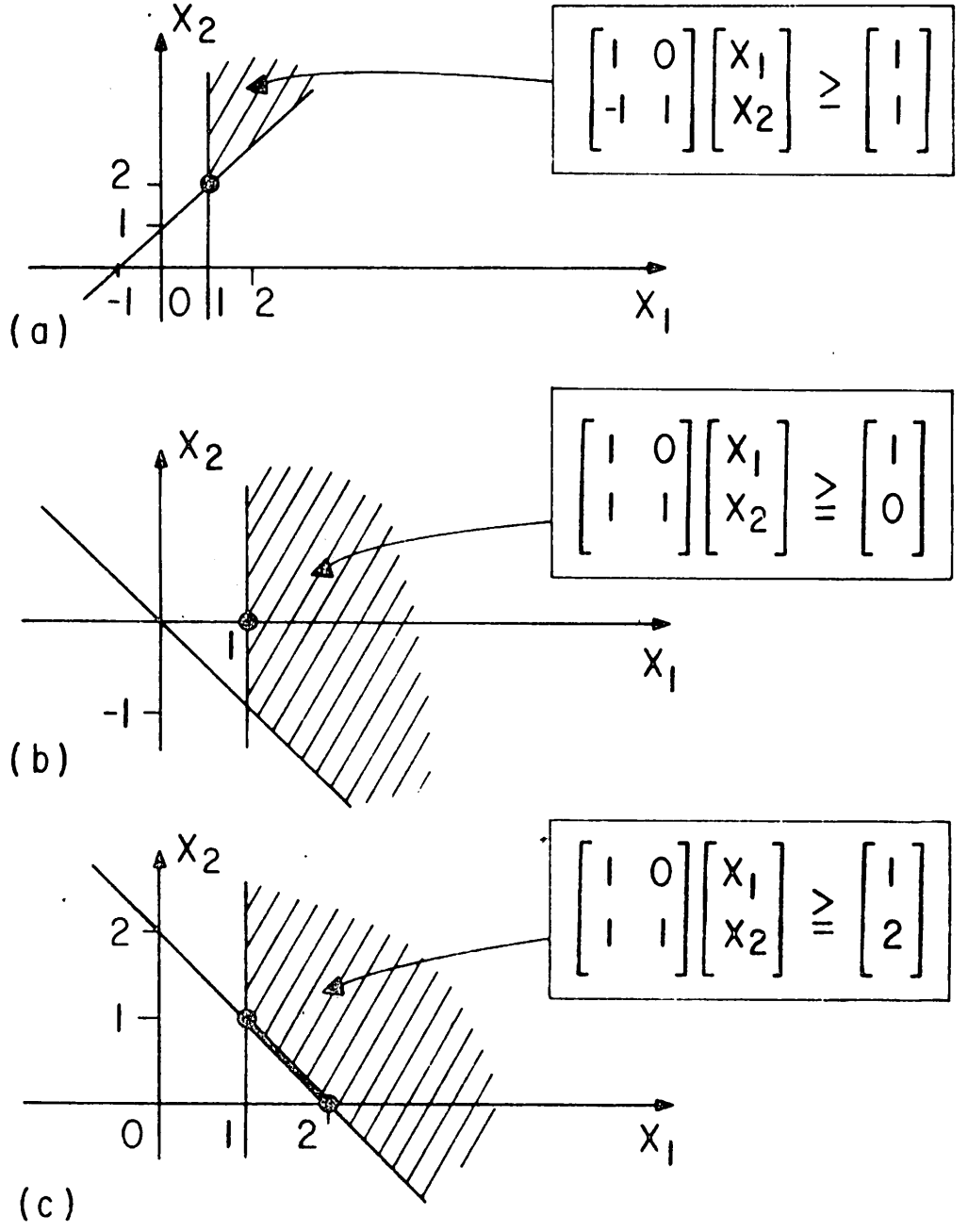

X_2
X_1
$\begin{bmatrix} 1 & 0 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \geq \begin{bmatrix} 1 \\ 1 \end{bmatrix}$
(a)
$\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \geq \begin{bmatrix} 1 \\ 0 \end{bmatrix}$
(b)
$\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \geq \begin{bmatrix} 1 \\ 2 \end{bmatrix}$
(c)

Fig. 10

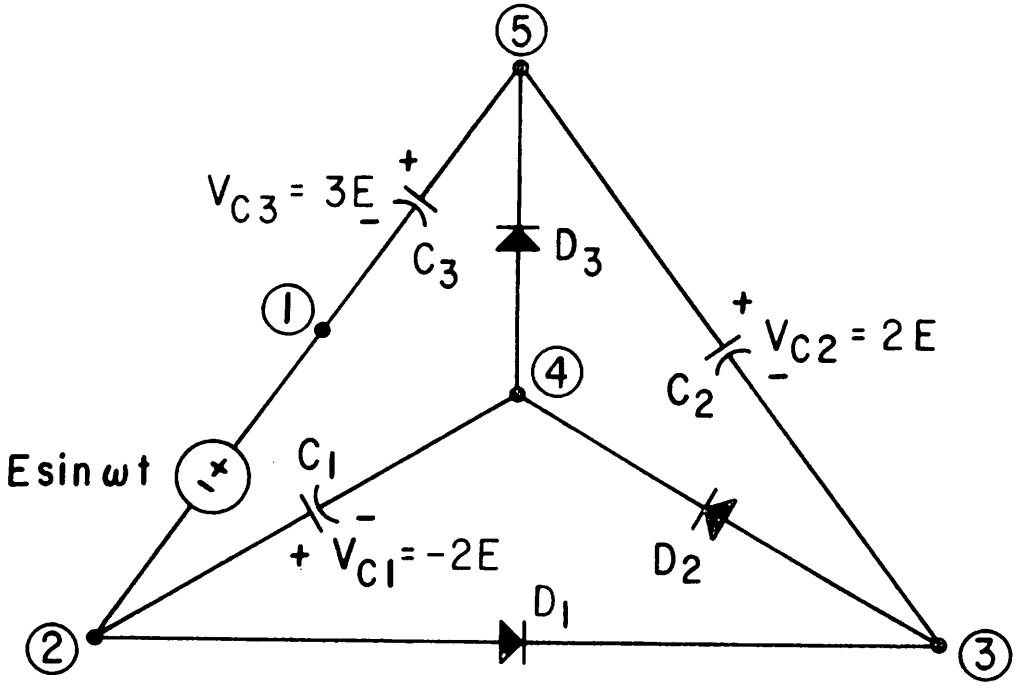

5
$V_{C3} = 3E$
+
−
C_3
D_3
1
4
+
$V_{C2} = 2E$
−
C_2
$E \sin \omega t$
C_1
−
+ $V_{C1} = -2E$
D_2
D_1
2
3

Fig. 11

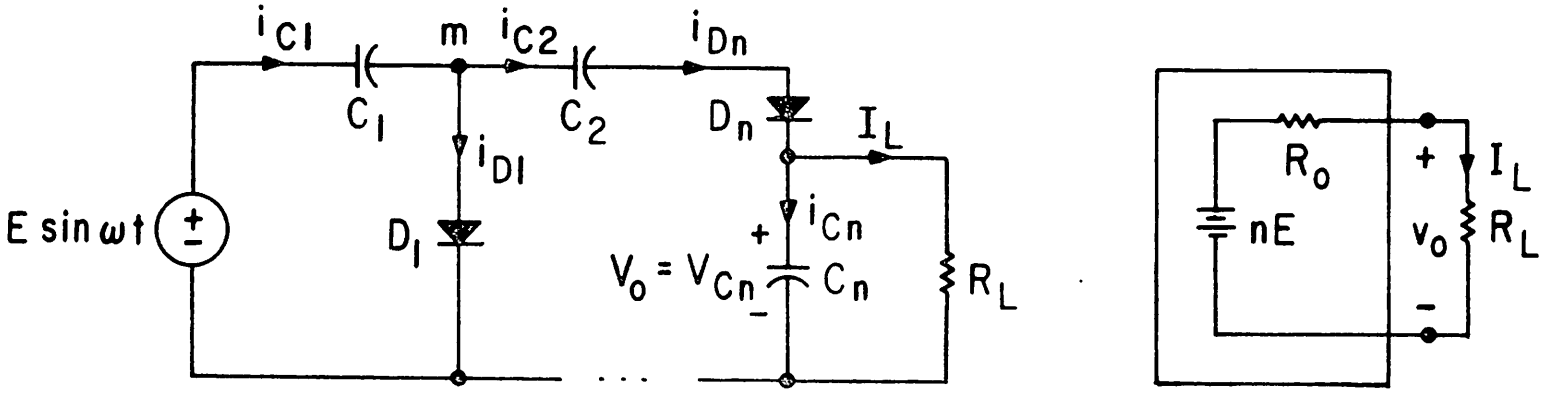
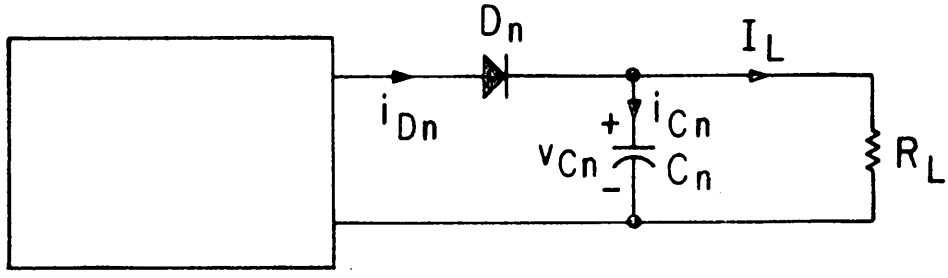
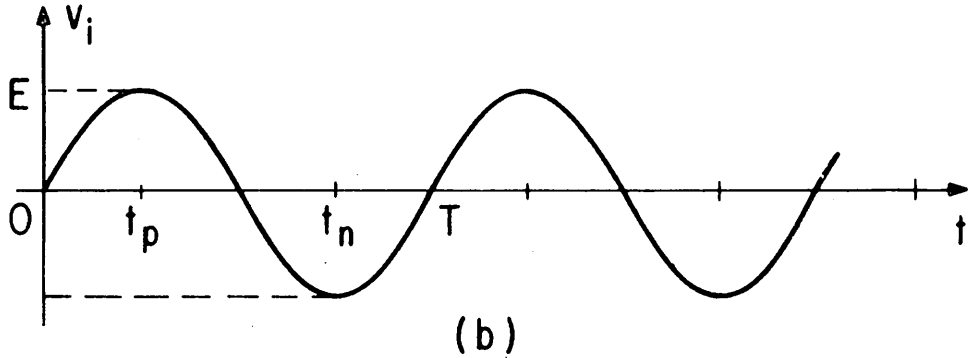

i_{C1}
m
i_{C2}
i_{Dn}
C_1
C_2
D_n
I_L
i_{D1}
$E \sin \omega t$
D_1
+
i_{Cn}
$V_o = V_{Cn}$
−
C_n
R_L
(a)
R_o
+
I_L
nE
v_o
R_L
−
(b)

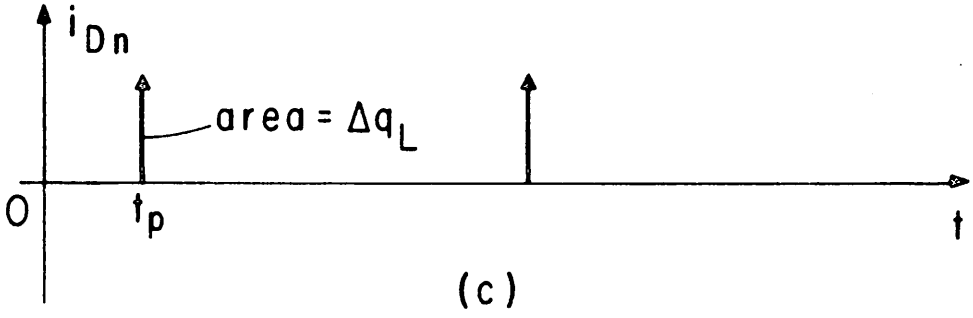
Fig. 12


Dn
I_L
i_{Dn}
+
i_{Cn}
v_{Cn}
−
C_n
R_L

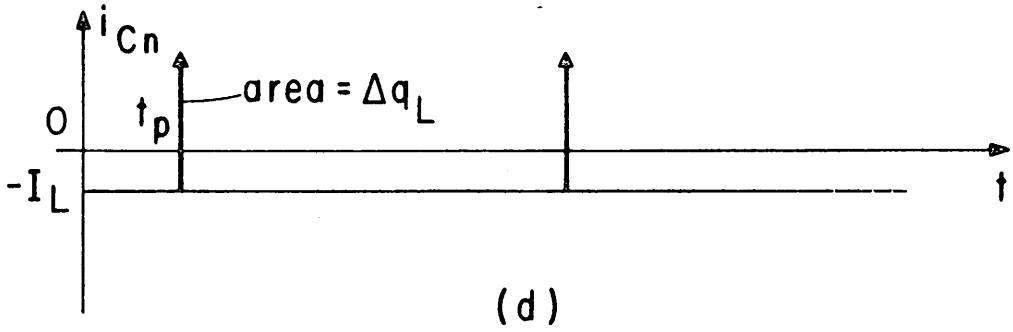
(a)


v_i
E
O
t_p
t_n
T
t

(b)


i_{Dn}
area = Δq_L
O
t_p
t

(c)


i_{Cn}
area = Δq_L
O
t_p
$-I_L$
t

(d)

Fig.13

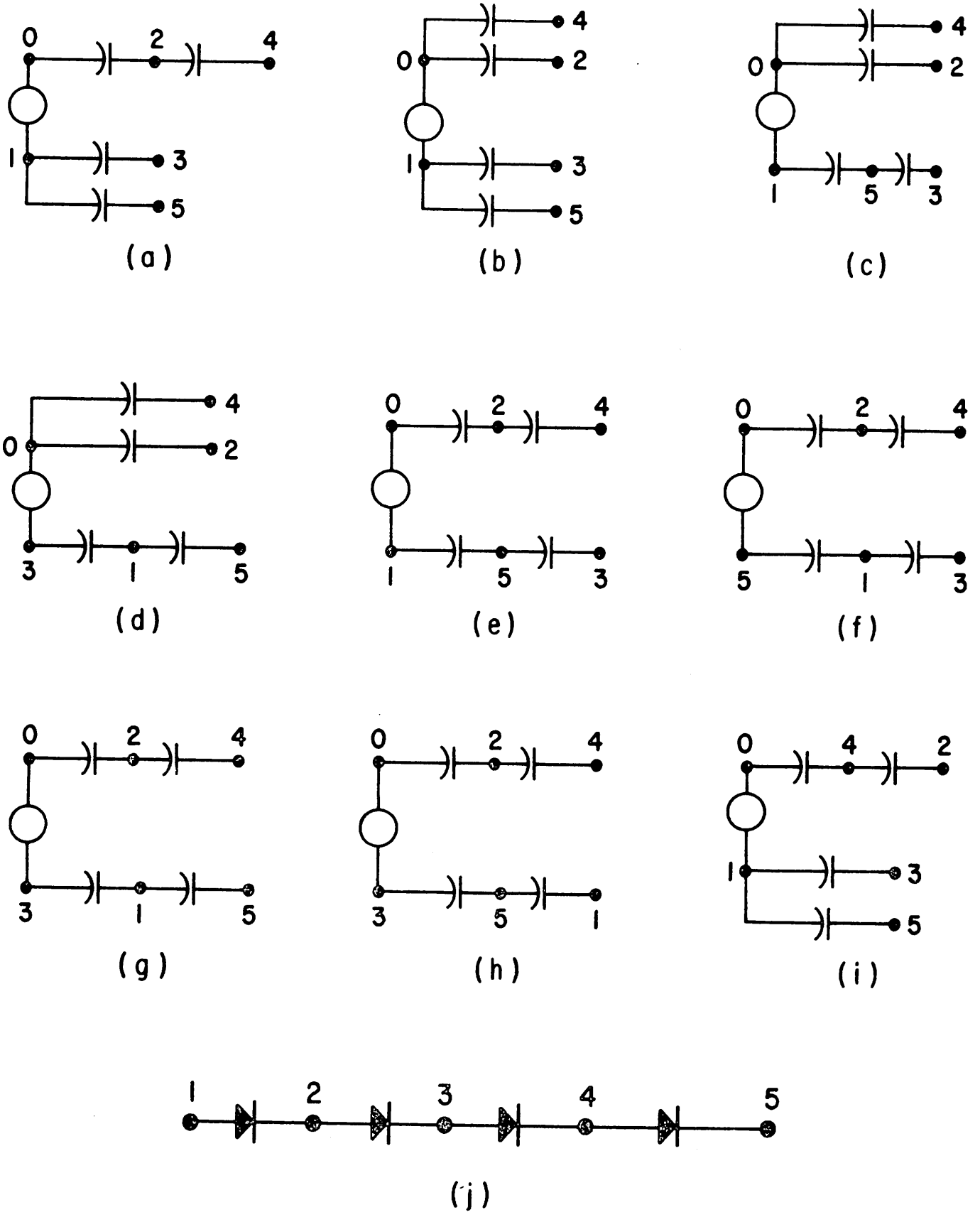
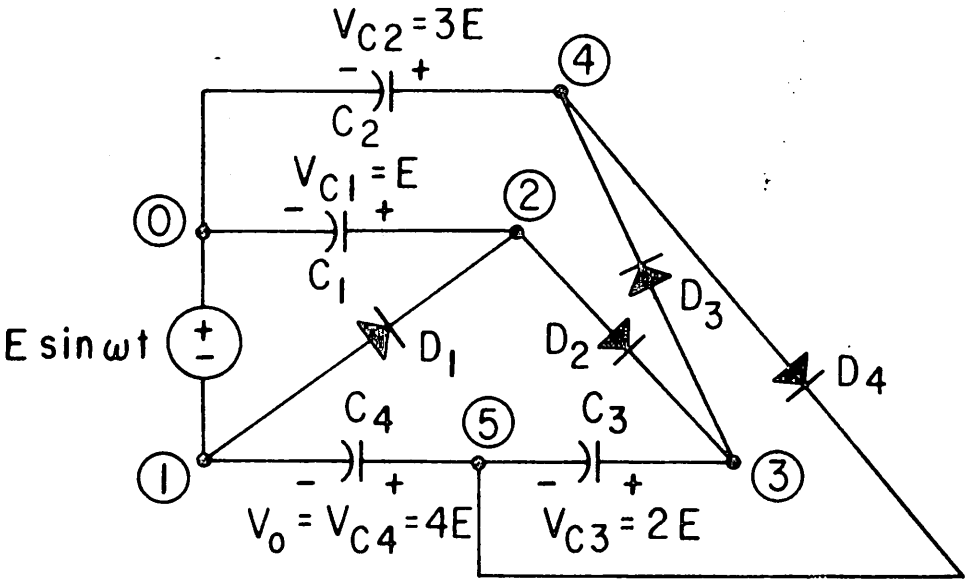
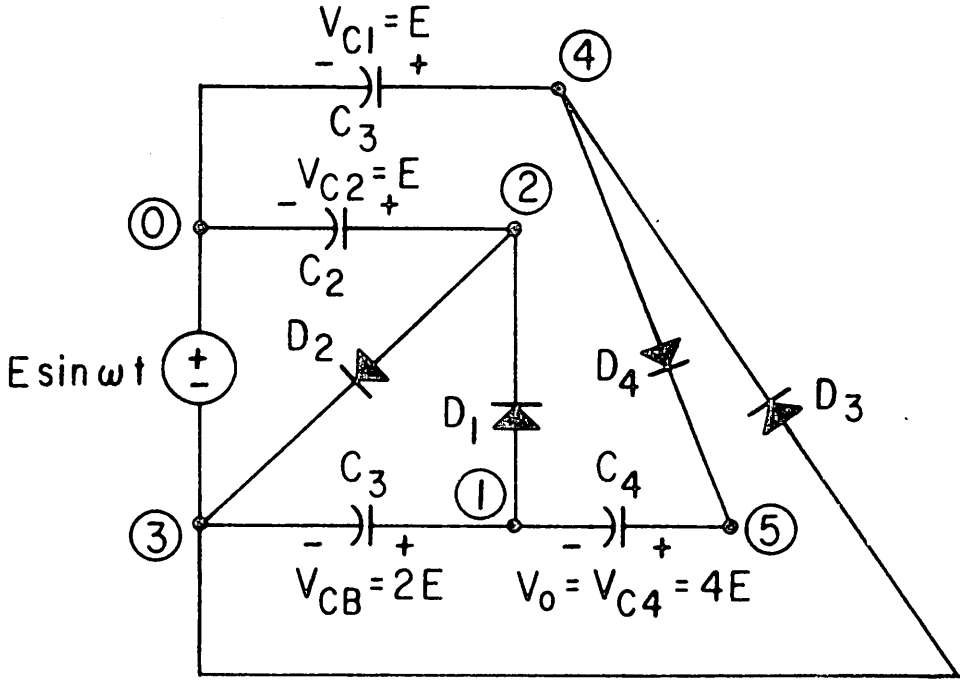

0
2
4
1
3
5
(a)
0
4
2
1
3
5
(b)
0
4
2
1
5
3
(c)
0
4
2
3
1
5
(d)
0
2
4
1
5
3
(e)
0
2
4
5
1
3
(f)
0
2
4
3
1
5
(g)
0
2
4
3
5
1
(h)
0
4
2
1
3
5
(i)
1
2
3
4
5
(j)

Fig. 14


$V_{C2}=3E$
C_2
$V_{C1}=E$
C_1
$E\sin\omega t$
D_1
D_2
D_3
D_4
C_4
C_3
$V_o=V_{C4}=4E$
$V_{C3}=2E$
0
1
2
3
4
5

(a)


$V_{C1}=E$
C_3
$V_{C2}=E$
C_2
$E\sin\omega t$
D_2
D_1
D_4
D_3
C_3
C_4
$V_{CB}=2E$
$V_o=V_{C4}=4E$
0
1
2
3
4
5

(b)

Fig. 15