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COMPUTER SIMULATION

OF MONOLITHIC CIRCUIT PERFORMANCE

IN THE PRESENCE OF ELECTRO-THERMAL INTERACTIONS

by

K. Fukahori

Memorandum No. UCB/ERL M77/18

24 March 1977

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TABLE OF CONTENTS

Page

ACKNOWLEDGMENT. i

LIST OF FIGURES v

LIST OF TABLES. x

CHAPTER

1 INTRODUCTION. 1

2 THE SIGNIFICANCE OF ELECTRO-THERMAL INTERACTIONS IN INTEGRATED CIRCUITS 6

2-1. Introduction. 6
2-2. Temperature dependence of bulk properties . . . 6

2-2-1. Intrinsic carrier concentration 6
2-2-2. Carrier mobility. 11
2-2-3. Breakdown voltage 16
2-2-4. Other temperature dependent properites. 20

2-3. The significance of the electro-thermal interactions as a design problem 20

2-3-1. The effect of thermal feedback on dc transfer curve of 741 operational amplifier 20

2-4. Electro-thermal interaction as a design degree of freedom. 31

2-4-1. Temperature stabilized substrate integrated circuit. 31
2-4-2. Thermal shutdown circuit. 38

3 LUMPED MODELING OF DIE-PACKAGE STRUCTURE. 41

3-1. Introduction. 41
3-2. Typical die-package structures. 41
3-3. The symmetrical finite difference approach. . . 47
3-4. Asymmetrical finite difference approach 53
3-5. Error analysis of the finite difference approximation 66

		Page
4	THE MATHEMATICAL FORMULATION AND NUMERICAL METHODS	75
4-1.	Introduction	75
4-2.	General formulation of the coupled system	75
4-3.	Newton-Raphson's method	80
4-3-1.	General description	80
4-3-2.	Branch relations in the electro-thermal system	81
4-3-3.	Update logic	89
4-3-4.	Transient analysis	94
4-3-5.	Computational effort involved in the Newton-Raphson algorithm	102
4-4.	Modified functional iteration	104
4-4-1.	Introduction	104
4-4-2.	Computational advantages and disadvantages of the modified functional iteration method	105
4-4-3.	Convergence of the modified functional iteration method	109
4-4-4.	Transient analysis using modified functional iteration method	116
4-5.	Conclusion	119
5	EXPERIMENTAL RESULTS	121
5-1.	Introduction	121
5-2.	Operational amplifiers	121
5-3.	Voltage regulators	133
5-4.	Temperature stabilized substrate integrated circuit system	146
6	CONCLUSION	153
6-1.	Summary	153
6-2.	Recommendation for further work	154
APPENDIX		
1	USER'S GUIDE	157
2	BENCH MARK CIRCUITS	178
A2-1.	Simple differential active load amplifier	178
A2-2.	Simple inverter	189
A2-3.	dc transfer curve analysis of a simple operational amplifier	198
A2-4.	dc transfer curve of a 741 operational amplifier	211

		Page
A2-5.	Transient analysis of LM140d voltage regulator	220
A2-6.	dc transfer curve of LM199 TSS circuit	234
A2-7.	How to use T-SPICE2C	251
3	THE T-SPICE PROGRAM	259
A3-1.	Introduction	259
A3-2.	T-SPICE2A, T-SPICE2B root segment	259
A3-3.	The main analysis loop	264
A3-4.	The FRMGD1, 2, 3 and 4 overlays	264
A3-5.	The RCVGRD overlay	273
A3-6.	The FRMGTH overlay	273
A3-7.	The SETUP overlay	273
A3-8.	The JAGTH overlay	273
A3-9.	The THLOAD overlay	274
A3-10.	The DCTRAN overlay	274
A3-10-1.	The DCTRAN overlay in T-SPICE2A	274
A3-10-2.	The DCTRAN overlay in T-SPICE2B	287
A3-11.	The T-SPICE2C program	287
4	LINKED LIST BEAD STRUCTURE	295
A4-1.	Resistors	295
A4-2.	Capacitors	298
A4-3.	Inductors	299
A4-4.	Mutual inductors	300
A4-5.	Voltage controlled current source	301
A4-6.	Non-linear voltage controlled current source	302
A4-7.	Independent voltage sources	303
A4-8.	Independent current source	304
A4-9.	BJT	305
A4-10.	Thermal capacitors	311
A4-11.	Thermal parameters	311
A4-12.	Zener diode	313
A4-13.	BJT model	314
A4-14.	.PRINT/.PLOT	316
5	LIST OF THE T-SPICE PROGRAM	317
REFERENCES		318

LIST OF FIGURES

FIGURE — Page

2.1 Intrinsic carrier concentration as a function of reciprocal temperature. 9

2.2 Temperature sensor using a diode. 12

2.3 Electron and hole drift mobilities in Si as a function of temperature and impurity concentration. . 14

2.4 Normalized temperature sensitivity $\delta_R/\delta_{R(27°C)}$ for base and emitter resistors. 18

2.5 Normalized temperature sensitivity $\delta_R/\delta_{R(27°C)}$ for base-pinch and collector resistors. 19

2.6 Temperature coefficient γ_z as a function of breakdown voltage. 21

2.7 dc transfer curve of a 741 op. amp.. 23

2.8 Simplified circuit schematic and its layout 24

2.9 Thermally induced offset voltage as a function of output voltage under no load condition. 27

2.10 Actual dc transfer curve with no load 28

2.11 Power dissipation in Q14 and Q20 vs. V_{out} 30

2.12 Thermally induced offset voltage due to Q14, Q20 vs. V_{out}. 31

2.13 Actual dc transfer curve under loaded condition 33

2.14 Example TSS system. 34

2.15 Band gap reference source 36

2.16 Diode compensated zener voltage reference source. . . . 37

2.17 Simplified schematic of μa 7805 15 watt monolithic voltage regulator 39

Page

3.1(a) Exploded view of TO-type package. 42

3.1(b) Exploded view of flat package 43

3.1(c) Exploded view of DIP package. 44

3.2(a) Physical structure. 46

3.2(b) Simplified model. 46

3.3(a) Solid subdivided into rectangular blocks. 48

3.3(b) One subregion expanded. 48

3.4 Equivalent circuit model for a subregion. 50

3.5 Complete circuit model for a subregion. 52

3.6 Asymmetrical thermal network with arbitrarily defined common boundary 55

3.7 Asymmetrical thermal network. 57

3.8(a) Asymmetrical thermal network in three dimensions. . . . 58

3.8(b) An expanded subregion 58

3.9(a) Example of asymmetrical network 62

3.9(b) Lumped model for a subregion. 62

3.10 A typical subregion of the die-header sandwich. 63

3.11 One method to suppress the creation of an extra node when the node is chosen in the middle of the subregion 73

4.1 A thermal lumped model associated with a node 79

4.2 Flow graph for the Newton-Raphson's method. 82

4.3 Equivalent circuit model for a current defined element. 84

4.4 Circuit model for a voltage defined element 86

4.5 Circuit model for a current defined element that depends on voltage and temperature. 88

4.6 Circuit model for a non-linear thermal resistor 90

4.7 Circuit model for a linear thermal resistor 90

4.8 Flow chart for the temperature limiting algorithm . . . 91

		Page
4.9	Flow chart of junction voltage limiting algorithm.	93
4.10	Flow chart of junction voltage limiting algorithm to limit power dissipation	95
4.11	Circuit model for a capacitor.	99
4.12(a)	A simple example circuit	100
4.12(b)	Equivalent circuit	100
4.12(c)	The resulting admittance matrix.	101
4.13	Illustration of iterative solution	106
4.14	Flow chart for a modified functional method.	107
4.15	Three examples of iterative solution	113
4.16	Illustration of convergence criteria for the functional iteration method.	115
4.17	A simple TSS example circuit to illustrate how to calculate thermal loop gain.	117
4.18	Circuit model employing modified function iteration method for the example of Fig. 4.12(a)	118
5.1	Computer predicted and experimentally observed dc transfer characteristic of 741 #1.	122
5.2	Schematic of 741 #1 and #2	123
5.3	Die photograph of 741 #1	124
5.4	Die photograph of 741 #2	127
5.5	Computer predicted and experimentally observed dc transfer characteristic of 741 #2.	128
5.6	Die photograph of 741 #3	129
5.7	Schematic of 741 #3 showing 100Ω buffering resistors in the output lead	130
5.8	Computer predicted and experimentally observed dc transfer characteristic of 741 #3.	132
5.9	Computer predicted and experimentally observed dc transfer characteristic of Fairchild 7118 op. amp.	134

		Page
5.10(a)	Block diagram of a typical three-terminal voltage regulator.	138
5.10(b)	Typical output voltage waveform in response to a step increase in input current	138
5.11	Simplified schematic of LM140d voltage regulator	139
5.12	Die photograph of the LM140d	141
5.13	Observed and computer predicted output voltage waveform for two versions of the LM140d in response to a 1.5A output current step	142
5.14	Photo of revised LM140d chip	144
5.15	Computer predicted and experimentally observed transient response of revised chip	145
5.16	Temperature distribution within a TSS system	148
5.17	LM199 temperature-stabilized substrate voltage reference.	149
5.18	Die photograph of the LM199 showing lines of constant temperature.	151
A2.1	Active load differential amplifier	180
A2.2	Simple inverter.	191
A2.3	Simplified 741 op. amp.	200
A2.4	Complete schematic of 741 operational amplifier.	214
A2.5	Simplified schematic of LM140d voltage regulator	226
A2.6	Schematic of LM199 TSS system.	239
A2.7	Example of thermal network formation	254
A3.1	T-SPICE2A, B overlay structure	260
A3.2	Flow chart of modified functional iteration method	262
A3.3	Flow chart of Newton-Raphson's method.	263
A3.4	dc transfer curve flow chart	265
A3.5	dc operating point analysis flow chart	266

		Page
A3.6	Transient analysis flow chart	267
A3.7	FORMGRID flow chart	269
A3.8	Example of rectangle formation	270
A3.9	Examples of first order check	271
A3.10	dc transfer curve analysis employing modified functional method	275
A3.11	Flow chart of dc operating point analysis employing modified functional method	278
A3.12	Flow chart of initial transient analysis employing modified functional method	279
A3.13	Flow chart of transient analysis employing modified functional method	280
A3.14	ITER8 flow chart	282
A3.15	ITER8 flow chart	284
A3.16	LOAD flow chart	285
A3.17	LUDCMP flow chart	286
A3.18	Temperature update scheme	288
A3.19	Flow chart of thermal network formation in T-SPICE2C	290
A3.20(a)	Node "D" acceptable	291
A3.20(b)	Node "D" not acceptable	291
A3.22	Perimeter tables before and after the triangle ABD formation	292
A3.23	A case where the outer angle of the perimeter is less than 180 degrees	294
A4.1	Integral charge model for an intrinsic BJT	310

LIST OF TABLES

TABLE		Page
2.1	Temperature Coefficient for Several Types of Resistors	17
5.1	CPU Time on CDC 6400 Spent by Analysis Portion of the Simulation	135
5.2	Comparison of Number of Iterations in the Newton-Raphson's Method for dc Operating Analysis when the Junction Initializing Scheme Is and Is Not Used	136
A4.1	The Linked List Structure of Resistors in T-SPICE2A	296
A4.2	The Linked List Structure of Resistors in T-SPICE2B	297
A4.3	The Linked List Structure for Capacitors	298
A4.4	Linked List Structure for Inductors	299
A4.5	Linked List Structure for Mutual Inductors	300
A4.6	Linked List Structure for Voltage Controlled Current Source	301
A4.7	Linked List Structure for Non-Linear Voltage Controlled Current Source	302
A4.8	Linked List Structure for Independent Voltage Source	303
A4.9	Linked List Structure for Independent Current Source	304
A4.10	The Linked List Structure of BJT in T-SPICE2A	305
A4.11	The Linked List Structure of BJT in T-SPICE2B	306
A4.12	Linked List Structure of Thermal Capacitors	311
A4.13	Linked List Structure for Thermal Parameters	312
A4.14	Linked List Structure of Zener Diode in T-SPICE2A	313
A4.15	Linked List Structure of Zener Diode in T-SPICE2B	314

Page

A4.16 Linked List Structure of BJT Model. 314

A4.17 Linked List Structure of dc Analysis Output Variable. . 316

CHAPTER 1

INTRODUCTION

The use of electronic circuit simulation programs has become widespread in the past decade or so. The major reasons for the continued development of such programs are threefold. First, in many cases, the performance of integrated circuits in monolithic form cannot be simulated with sufficient accuracy by bread-boarding of the circuit. This is largely due to parasitic components inherent in integrated circuits which cannot be accurately modeled with discrete components. Second, as the result of extensive research effort which resulted in better understanding of how semiconductor devices work, it has become possible to mathematically model the devices quite accurately and reliably. Third, with the reduction in the cost of simulation the time period involved in the design cycle of integrated circuits can be shortened. The simulation programs such as SPICE2 [1] have made significant contribution as a reliable, accurate and efficient vehicle in the design of integrated circuits.

The simulation programs developed to date have had one major limitation as a design tool in that they did not take into consideration the effect of temperature variation on the top surface of the chips due to internal heat dissipation of the circuits. Indeed, the localized power dissipation within the elements of the circuit cause chip temperature gradients and variations which strongly affect the performance of the circuits, particularly in cases where very high

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by

Kiyoshi Fukahori

ABSTRACT

This research effort has been directed toward the development of an efficient and accurate computer simulation program which predicts the dc and transient performance of integrated circuits in the presence of electro-thermal interactions on the monolithic die.

First, an efficient and effective lumped modeling of the die-package structure is developed which can accurately represent the thermal behavior of a wide variety of commonly used integrated circuit die-package combinations.

Second, the mathematical formulation of the coupled electro-thermal system is carried out and two algorithms useful for the solution of the system are developed. The advantages and disadvantages of the two algorithms are investigated under both dc and transient conditions.

Third, a computer program called T-SPICE has been developed and used to predict the performance of a group of monolithic operational amplifiers, voltage regulators, temperature stabilized substrate systems. Comparison is made between the experimentally observed and the simulated performances of these circuits. Experimental agreement in all cases is good.

accuracy is required or where large power dissipation occurs on a chip. In these two types of circuits, the capability of simultaneously simulating both thermal and electrical behavior becomes essential. In fact, in some classes of circuits, the simulation of electrical effects only becomes meaningless because the proper performance of the circuits depends upon the actual electro-thermal interactions. Although the electro-thermal interactions are not of importance in every new monolithic circuit design, the frequency of cases in which their influence must be considered is constantly increasing because of the requirements for increasing precision on the one hand, and for increasing power levels, on the other, in analog integrated circuits.

Previous work on electro-thermal circuits has been concentrated on the relationship between the two-dimensional geometrical layout of the distributed heat sources and temperature sensors, and the resulting thermal frequency response. In recent work [2], the header was represented as a rectangular block under the die and a finite Fourier transform solution of the heat flow equation

$$k\nabla^2 T = \rho c \frac{dT}{dt} \qquad (1\text{-}1)$$

where k is the thermal conductivity of the material and ρc is the specific heat, was carried out in both the silicon and the header.

A computer program [3] has been written which performs this calculation. However, the program was of limited usefulness because of the following limitations [4]:

1. The finite transform solution is feasible only for simple rectangular die structures with uniform boundary conditions. Thus, accurate representation of the effects of bonding wires, and the

effects of the thermal behavior of a large header are cumbersome. This is particularly important in the analysis of thermal shutdown circuits, where the thermal behavior of the header-heatsink combination plays an important role.

2. The analysis of the circuit to determine the dependence of the parameter of interest on the temperature of each circuit element must be carried out by hand, and this information inserted into the program. This process becomes very laborious for circuits containing a sensor circuit which consists of many temperature-sensitive elements.
3. The approach rests on assumptions of linearity both in the electronic and thermal parts of the circuit. Thus a piecewise linear approach must be used for a nonlinear case such as thermal shutdown circuits.

As a result of these limitations, no general simulation tool has come into wide use in the design of electro-thermal circuits. If full advantage is to be taken of the design degrees of freedom offered, then a more powerful simulator is needed.

The research effort described in this dissertation has been directed toward the development of more powerful general-purpose electro-thermal simulator with the following objectives in mind:

a) It must be capable of accurately modeling the thermal behavior of chip-package structure under dc and transient conditions.
b) The thermal parameters which must be specified by the user for use in the program must be either easily measured or calculated.
c) The temperature sensitivity of electrical circuit elements within the integrated circuit must be accurately modeled in the program.

d) The capability for simulating the different aspects of electronic circuit behavior must be similar to that of the existing programs.
e) The program should be capable of simulating such anamolies as die-attach voids, flip chip attach bonding, etc.

In Chapter 2 of this dissertation, the importance of electro-thermal interaction is illustrated in two classes of circuits, one in which the thermal interaction degrades the performance of integrated circuit, and the other in which the thermal interaction is utilized as design degree of freedom to enhance the performance of certain types of integrated circuits.

In Chapter 3, the lumped modeling of die-package structure for typical integrated circuits is developed from the general heat flow equation. A generalization of symmetrical finite difference approximation is employed for an efficient and accurate representation of the die-package structure.

In Chapter 4, the equations governing the coupled electro-thermal system are formulated and two numerical methods relating to the solution of the system are presented. The first method involves the use of the Newton-Raphson's method to the coupled system as a whole. The second method uses the Newton-Raphson's method for the solution of electrical system, but functional iteration is employed between the electrical and thermal systems until convergence is obtained. The two methods are analyzed and compared in detail, and the advantages and disadvantages and their respective applicabilities are presented. Also, the application of the two methods for the solution of the coupled system under transient condition is presented.

In Chapter 5, the simulation results are compared to those

experimentally observed. It is shown that the agreement is very good. The relative merits of the two methods are concluded from the result of several simulations.

In Chapter 6, the summary of this research is given and recommendations for further work are given along with some ideas on how to implement them.

In the appendices, the specifics of the program are described in detail.

CHAPTER 2

THE SIGNIFICANCE OF ELECTRO-THERMAL INTERACTIONS IN INTEGRATED CIRCUITS

2-1. Introduction

The electro-thermal interactions arise from the temperature variations in the die-package structure. In this chapter, the temperature dependence of some of the important bulk properties are first discussed. Then the significance of electro-thermal interactions arising from this dependence are demonstrated in two different classes of integrated circuits.

In one class of integrated circuits, the electro-thermal interaction causes the degradation of circuit performance while in the other class of integrated circuits, the electro-thermal interaction is utilized to improve the performance of integrated circuits. A few examples of circuit performance are given for both classes of integrated circuits.

2-2. Temperature dependence of bulk properties

Since the integrated circuits are typically built on silicon substrates,some of the properties of silicon whose temperature dependences play important roles in the performance of integrated circuits are briefly mentioned in this section.

2-2-1. Intrinsic carrier concentration

One of the most important temperature dependent bulk properties

of silicon is that of intrinsic carrier concentration, n_i^2. In an intrinsic material the number of electrons n_i is equal to the number of holes p_i and given by [5]:

$$n_i = p_i = 2\left(\frac{kT}{2\pi h^2}\right)^{\frac{3}{2}} (m_e m_h)^{\frac{3}{4}} e^{-Eg_o/2kT}$$

or

$$n_i p_i = n_i^2 = 4\left(\frac{kT}{2\pi h^2}\right)^3 (m_e m_h)^{\frac{3}{2}} e^{-Eg_o/kT} \qquad (2\text{-}1)$$

where k is a Boltzman's constant,

T is temperature,

h is a Plank's constant,

m_e, m_h are effective mass of an electron and a hole,

Eg_o is an energy gap of silicon extrapolated to absolute zero.

Eq. (2-1) can be rewritten to emphasize its temperature dependence as

$$n_i^2 = KT^3 e^{-Eg_o/kT} \qquad (2\text{-}2)$$

where

$$K = 4\left(\frac{k}{2\pi h^2}\right)^3 (m_e m_h)^{\frac{3}{2}}$$

The immediate consequence of this phenomenon is quite significant and manifests itself in the temperature dependence of diode characteristic, whose ideal relation is given by

$$I_d = I_s\left(e^{\frac{qV_d}{kT}} - 1\right) \qquad (2\text{-}3)$$

where I_d and V_d are the current and voltage of the diode. I_s is called saturation current and is given by [6]:

$$I_s = Aqn_i^2\left(\frac{D_h}{N_D L_h} + \frac{D_e}{N_A L_e}\right) \qquad (2\text{-}4)$$

where A is the cross-sectional area of the diode junction,

q is the charge of an electron,

D_h, D_e are the hole and electron diffusion constants,

N_A, N_D are doping concentration of p type and n type materials, respectively,

L_h, L_e are hole and electron diffusion lengths.

The temperature dependence of I_s is dominated by that of n_i^2 because the factor in parentheses in Eq. (2-4) is not strongly temperature dependent. The temperature dependence of n_i^2 is more clearly seen if we take the logarithm of Eq. (2-2):

$$\ln(n_i^2) = \ln(KT^3) - \frac{Eg_o}{kT} \qquad (2\text{-}5)$$

The first term on the right-hand side of Eq. (2-5) is a very weak function of T about room temperatures. Thus the plot of $\ln(n_i^2)$ versus $\frac{1}{T}$ will be linear with its slope approximately equal to $-\frac{Eg_o}{k}$ as shown in Fig. 2.1. The fractional change in n_i^2 is from Eq. (2-2)

$$\frac{1}{n_i^2}\frac{dn_i^2}{dT} = \frac{3}{T} + \frac{Eg_o}{kT^2} \qquad (2\text{-}6)$$

For silicon, Eg_o = 1.1 eV and at room temperature (T = 300°K), $kT \cong 26$ meV. Therefore

$$\frac{1}{n_i^2}\frac{dn_i^2}{dT} = \frac{3}{300} + \frac{1.1\ \text{eV}}{(26\text{meV})(300)} = 0.01 + 0.16 = 17\%$$

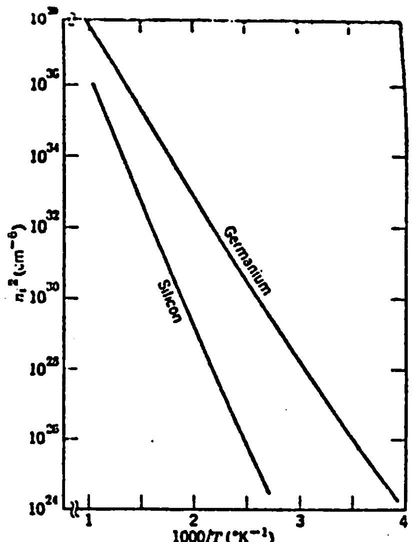


Fig. 2-1

Intrinsic carrier concentration as a function of reciprocal temperature.

(After Gray, Ref. [7])

Thus n_i^2 (or I_s) doubles approximately every 6°C. The temperature dependence of diode current at a given V_d is from Eq. (2-2),

$$\left.\frac{dI_d}{dT}\right|_{V_d} = \left.\frac{dI_s}{dT}\right|_{V_d} \left(e^{\frac{qV_d}{kT}} - 1\right) - \frac{I_s}{T}\frac{qV_d}{kT} e^{\frac{qV_d}{kT}} \qquad (2\text{-}7)$$

If the diode is sufficiently forward biased (i.e., $V_d >> \frac{kT}{q}$)

$$\left.\frac{dI_d}{dT}\right|_{V_d} \cong \left(\left.\frac{dI_d}{dT}\right|_{V_d} - I_s \frac{qV_d}{kT^2}\right)\left(e^{\frac{qV_d}{kT}}\right) \qquad (2\text{-}8)$$

Therefore

$$\frac{1}{I_d}\left.\frac{dI_d}{dT}\right|_{V_d} \cong \frac{1}{I_s}\left.\frac{dI_s}{dT}\right|_{V_d} - \frac{qV_d}{kT^2} \qquad (2\text{-}9)$$

For $V_d \cong 0.7$,

$$\frac{1}{I_d}\left.\frac{dI_d}{dT}\right|_{V_d=.6V} = 0.17 - \frac{0.7}{26m}\frac{1}{300} \cong 8\%$$

Thus the diode current for silicon at a fixed voltage will double for roughly 10°C change in temperature. The change in the voltage drop across the diode at a constant current level I_d is obtained by first rewriting Eq. (2-3) as

$$V_d = \frac{kT}{q}\ln\left(1 + \frac{I_d}{I_s}\right) \cong \frac{kT}{q}\ln\frac{I_d}{I_s} \qquad (2\text{-}10)$$

for $V_d >> \frac{kT}{q}$, and differentiating this with respect to T to get

$$\left.\frac{dV_d}{dT}\right|_{I_d} = \frac{V_d}{T} - \frac{kT}{q}\frac{1}{I_s}\left.\frac{dI_s}{dT}\right|_{I_d} \qquad (2\text{-}11)$$

At room temperature ($T = 300°K$) and I_d = 1ma, and $I_s = 10^{-14}A$,

$$V_d \cong (26m)\ln\frac{1ma}{10^{-14}} \cong 0.66^V$$

and

$$\left.\frac{dV_d}{dT}\right|_{I_d=1ma} = \frac{0.66}{300} - 26m^V(0.17\%) \cong -2.2mV/deg.C.$$

In general the diode voltage for a fixed current would show negative temperature coefficient of about -2mV/deg.C.

If we bias a diode with a constant current source as shown in Fig. 2.2, and measure the voltage drop V_d, we can sense the temperature at which the diode is operating. This is typically the way in which the temperature sensing is done on an integrated circuit chip.

2-2-2. Carrier mobility

Another important temperature dependent property of silicon is that of carrier mobility. The carrier mobility μ is defined as the magnitude of the drift velocity, $|V_d|$ per unit electric field, $|E|$:

$$\mu = \left|\frac{V_d}{E}\right| \qquad (2\text{-}12)$$

The mobility is related to collisions of carriers with lattice impurities and phonons and given by [7]

$$\mu = \frac{q\tau}{m^*} \qquad (2\text{-}13)$$

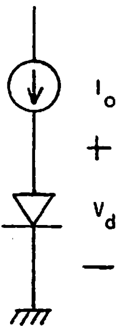


Fig. 2.2 - Temperature sensor using a diode

Where m^* is the effective mass of a carrier, τ is a collision time.

When the mobility is dominated by acoustic mode phonon scattering, it shows temperature dependence given by [8]:

$$\mu_l \propto T^{-3/2} \qquad (2\text{-}14)$$

When the mobility is dominated by ionized impurities scattering, it shows temperature dependence given by

$$\mu_i \propto T^{3/2} \qquad (2\text{-}15)$$

The combined mobility μ is to a good approximation given by

$$\frac{1}{\mu} = \frac{1}{\mu_l} + \frac{1}{\mu_i} \qquad (2\text{-}16)$$

Typically at low temperatures the scattering mechanism due to ionized impurity dominates and shows the temperature dependence as given by Eq. (2-15), while at high temperature range where transistors typically operate, the scattering mechanism due to phonon dominates as given by Eq. (2-14). For pure materials at room temperature [8], it is found that the mobility varies as $T^{-2.5}$ and $T^{-2.7}$ for n- and p-type silicon materials. Electron and hole mobilities in silicon as a function of temperature and impurity concentration is given in Fig. 2.3.

The practical effect of the temperature dependence of mobility is that the diffused resistor has a positive temperature coefficient. The resistivity ρ for n-type and p-type semiconductor materials are given respectively by

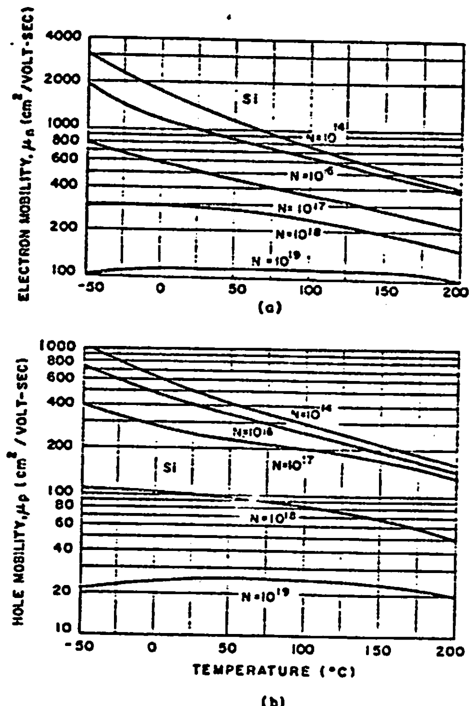


Fig. 2-3

Electron and hole drift mobilities in Si as a function of temperature and impurity concentration.

(After Sze Ref. [8])

$$\rho_n = \frac{1}{q\mu_n n} \propto T^{\eta 1} \qquad (2\text{-}17)$$

$$\rho_n = \frac{1}{q\mu_p p} \propto T^{\eta 2} \qquad (2\text{-}18)$$

where η_1 and η_2 are constants.

A resistor made in uniformly doped material of length L with cross-sectional area of A will have the resistance value R given by

$$R(T) = \rho\frac{L}{A} \propto T^{\eta} \qquad (2\text{-}19)$$

where η is a constant.

For a large temperature variation, Eq. (2-19) must be used. However, for a typical integrated circuit, the variation is rather small. In these cases, one can approximate Eq. (2-19) by specifying effective temperature coefficient, γ_R [9]. When R(T) is expanded about the operating temperature T_o, we get

$$R(T) = R(T_o) + \left.\frac{dR}{dT}\right|_{T_o} (T - T_o) + \frac{1}{2}\left.\frac{d^2R}{dT^2}\right|_{T_o}(T - T_o)^2 + \ldots$$

$$= R(T_o)[1 + \frac{1}{R(T_o)}\left.\frac{dR}{dT}\right|_{T_o} (T - T_o) + \ldots \qquad (2\text{-}20)$$

If we define

$$\gamma_R \equiv \frac{1}{R(T_o)}\left.\frac{dR}{dT}\right|_{T_o} \qquad (2\text{-}21)$$

Then,

$$R(T) \cong R(T_o)[1 + \gamma_R(T - T_o)] \qquad (2\text{-}22)$$

for small temperature variation.

Typically, γ_R is obtained empirically and used in place of η to specify the temperature coefficience of R.

Typical values of γ_R for several types of resistors are given in Table 2-1, Fig. 2.4, Fig. 2.5.

2-2-3. Breakdown voltage

When a sufficiently high field is applied to a p-n junction, the junction breaks down and conducts a very large current. The voltage at which the breakdown occurs is a function of temperature and this dependence gives rise to another important temperature dependent property of silicon.

Typically the breakdown voltage increases as temperature rises. The hot carriers passing through the high field depletion layer lose part of their energy to optical phonons after traveling each electron phonon mean free path λ. The value of λ decreases with temperature [8]. Thus the carriers lose more energy to the phonon along a given distance at constant field. Hence the carriers must pass through a greater potential difference before they can acquire sufficient energy to break down.

The practical significance of this property in integrated circuits is the temperature dependence of zener diode, often used as a reference source. Just as with the temperature dependence of resistors, the breakdown voltage V_B may be most conveniently expressed as

$$V_B = V_B(T_o) + \gamma_B(T - T_o) \qquad (2\text{-}23)$$

Table 2.1 TEMPERATURE COEFFICIENT FOR SEVERAL TYPES OF RESISTORS

(After Hamilton, Ref. [10])

Region and type of material	Sheet resistance Ω/sq or concentration, cm^{-3}	at $300^{o}K$ ppm
Emitter, n	5	1500
	15	2500
Base, p	100	1000
	200	2500
Collector, n	10^{15}	8000
	10^{16}	4000
	10^{17}	3500
Base pinch, p	...	8000

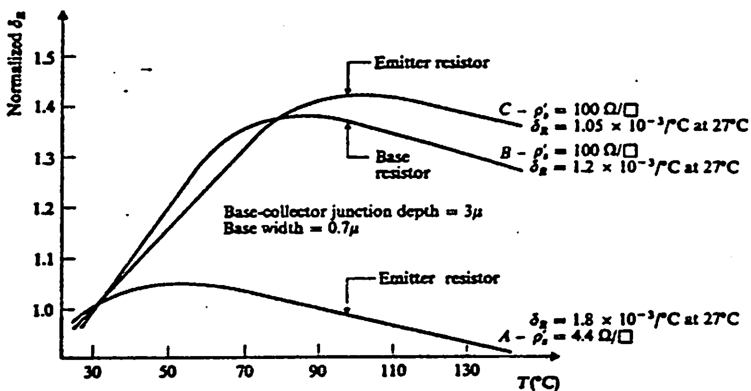


Fig. 2.4

Normalized temperature sensitivity $\delta_R/\delta_{R(27°C)}$ for base and emitter resistors.

(After Hamilton, Ref. [10])

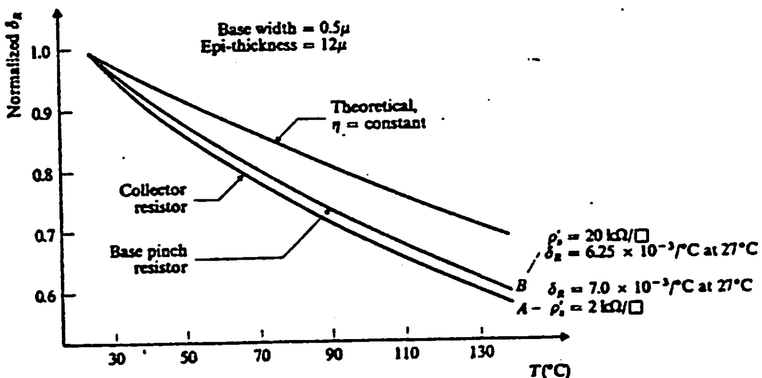


Fig. 2.5

Normalized temperature sensitivity $\delta_R/\delta_{R(27°C)}$ for base-pinch and collector resistors.

(After Hamilton, Ref. [10])

where γ_B is the temperature coefficient of the breakdown in units of (V/°C). γ_B is a function of the breakdown voltage and this relation is shown in Fig. 2.6. For a zener breakdown voltage of about six volts, γ_B is around $+2m^V/°C$.

2-2-4. Other temperature dependent properties

There are other bulk properties whose temperature dependence affects the performance of integrated circuits. Good examples are the temperature dependence of current gain of bipolar transistors [9], and that of the threshold voltages of both metal-oxide-semiconductor field effect transistors and junction field effect transistors. In all these cases one can simply express these parameters in terms of temperature coefficients obtained empirically.

In the program developed only the temperature dependence of saturation current, breakdown voltage, and diffused resistors are considered. The program can be easily modified to accommodate other temperature dependent parameters.

2-3. The significance of the electro-thermal interactions as a design problem

The temperature dependence of the silicon material as mentioned in the previous section affects the performance of integrated circuits in two different ways. In this section, the aspect of the electro-thermal interaction as a design problem is presented.

2-3-1. The effect of thermal feedback on dc transfer curve of 741 operational amplifier

The significance of the electro-thermal interactions as a

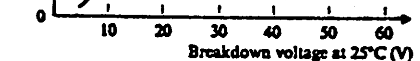


Fig. 2.6

Temperature coefficient γ_z as a function of breakdown voltage.

(After Hamilton, Ref. [10])

design problem is best illustrated by the dc transfer characteristic of a commercially available operational amplifier 741 as shown in Fig. 2.7 [10], [11]. A heavily distorted dc transfer curve is observed for the amplifier when a load resistor of 1 KΩ is attached from the output to ground, resulting in power dissipation in the output transistors. The figure also shows this observed dc transfer characteristic for the case of output left open. Notice that the gain has about the right magnitude but the wrong polarity. This results from undesirable thermal feedback from elements in the circuit other than the output transistors. The computer predicted dc transfer characteristic which does not take the thermal interaction into account is also shown in Fig. 2.7.

Let us explore the origin of this heavy distortion on dc transfer curve. To facilitate the understanding of this phenomenon, a simplified version of the 741 circuit is shown in Fig. 2.8, along with a simplified drawing of the die layout of this particular 741 operational amplifier. The power dissipation in Q_{13A}, which acts as the load for common emitter stage Q_{17} and also biases the output stage, varies linearly with output voltage, V_{out}. More specifically, the power dissipation in Q_{13A}, $P(Q_{13A})$, is given by

$$P(Q_{13A}) \cong I_{CQ13A} \cdot (V_{CC} - (V_{out} - 2V_{BE})) \qquad (2\text{-}24)$$

where I_{CQ13A} is the collector currents of Q_{13A},

V_{CC} is the positive power supply voltage,

V_{BE} is the base-emitter junction voltage.

The same is true of the power dissipation in Q_{17}, and

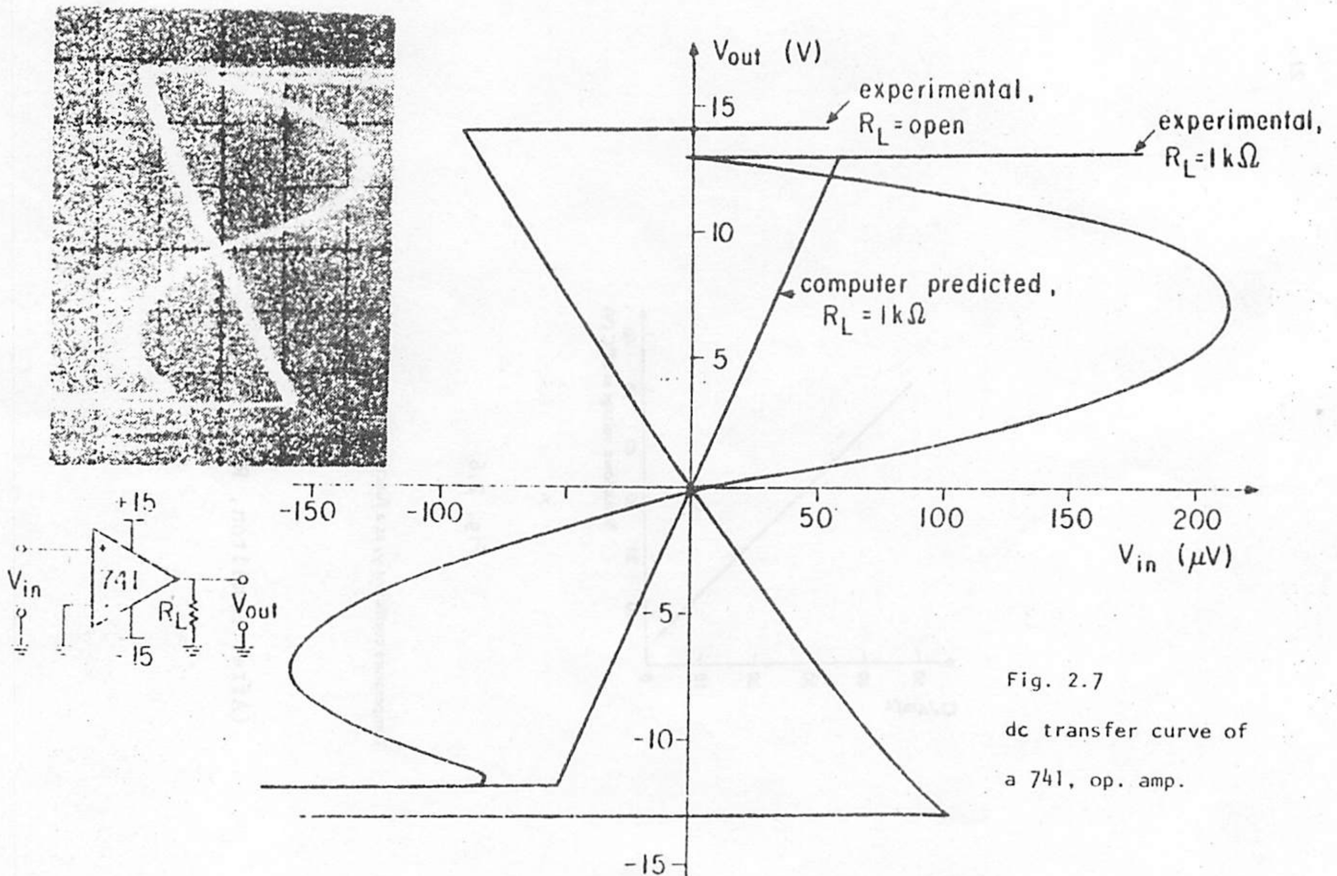


Fig. 2.7

dc transfer curve of

a 741, op. amp.

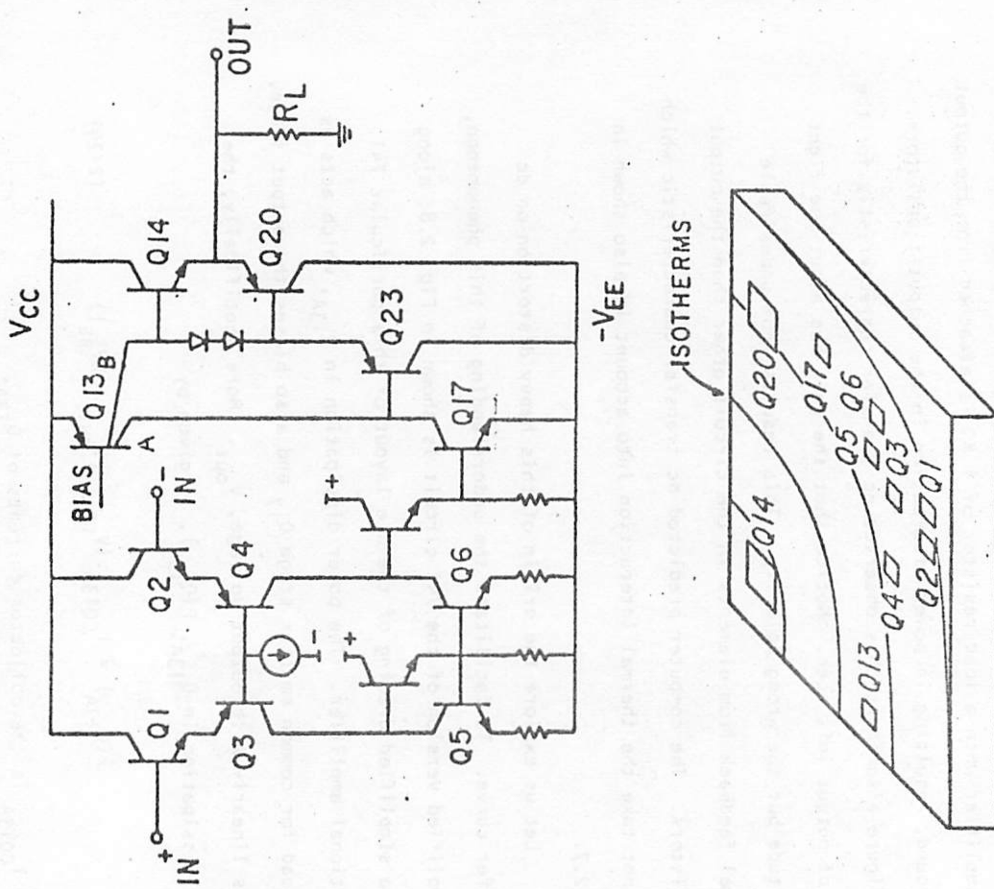


Fig 2.8 Simplified circuit schematic and its layout

$$P(Q_{17}) \cong I_{CQ13A} \cdot (V_{out} - 2V_{BE} + V_{EE}) \tag{2-25}$$

where V_{EE} is the negative power supply voltage. If there is no load attached to the output, the power dissipation in Q_{13B}, Q_{23} are given by

$$P(Q_{13B}) = I_{CQ13B} \cdot (V_{CC} - (V_{out} + V_{BE})) \tag{2-26}$$

$$P(Q_{23}) = I_{CQ13B} \cdot (V_{out} - V_{BE} + V_{EE}) \tag{2-27}$$

The power dissipation in other transistors of the circuit are not directly related to the output voltage, and they do not have any significant effect on the distortion of dc transfer characteristic.

Each component given by Eq. (2-24) through Eq. (2-27) will in general create temperature gradients between Q_1-Q_2, Q_3-Q_4, and Q_5-Q_6. However the magnitude and the direction of thermal gradients depend on how the power dissipating transistors are laid out with respect to the input pairs. For example, the power dissipation in Q_{13} will make Q_2, Q_4, and Q_5 hotter than Q_1, Q_3, and Q_6 respectively. If the unit amount of power dissipation in $Q_{13A,B}$ results in temperature difference ΔT between Q_2 and Q_1 of the amount $\delta_T Pd(Q_{13A,B})$, where δ_T is a measure of coupling between $Q_{13A,B}$ and Q_1-Q_2 pair, and has a unit of °C/watt, the effective change in offset voltage is given by

$$V_{os} = K.\Delta T = K\delta_T Pd(Q_{13A,B}) \tag{2-28}$$

where from Eq. (2-11),

$$K = \left.\frac{dV_{BE}}{dT}\right|_{I=const} \cong -2mV/°C.$$

The effect of power dissipation in $Q_{13A,B}$ on Q_3-Q_4, Q_5-Q_6 can be expressed similarly. Thus the total thermally induced offset voltage $V_{osQ13A,B}$ may be written as

$$V_{osQ13A,B} = \gamma_{Q13} \cdot Pd(Q_{13A,B}) \tag{2-29}$$

where

$$\gamma_{Q13} = K\delta_T$$

is a constant.

From Eq. (2-24), Eq. (2-26), we see that the power dissipation in $Q_{13A,B}$ is linearly related to the output voltage. Thus V_{os} is linear with V_{out}. The plot of V_{os} versus V_{out} is shown in Fig. 2.9.

Similarly, the effects of power dissipation in Q_{17}, Q_{23} on the offset voltage can be written as

$$V_{osQ17} = \gamma_{Q17} \cdot P_d(Q17) \tag{2-30}$$

$$V_{osQ23} = \gamma_{Q23} \cdot P_d(Q23) \tag{2-31}$$

where γ_{Q17}, γ_{Q23} are constants indicating the measure of coupling between Q17, Q23 and input pairs.

Since P(Q17) and P(Q23) are linear with V_{out}, V_{osQ17} and V_{osQ23} also show linear relationship with V_{out}. This is shown also in Fig. 2.9. The dark line indicates the thermally induced total offset voltage which must be added to the ideal characteristic to achieve accurate dc transfer characteristic. This is done in Fig. 2.10. The dark line shows actual dc transfer characteristic.

The linear relationship between thermally induced offset

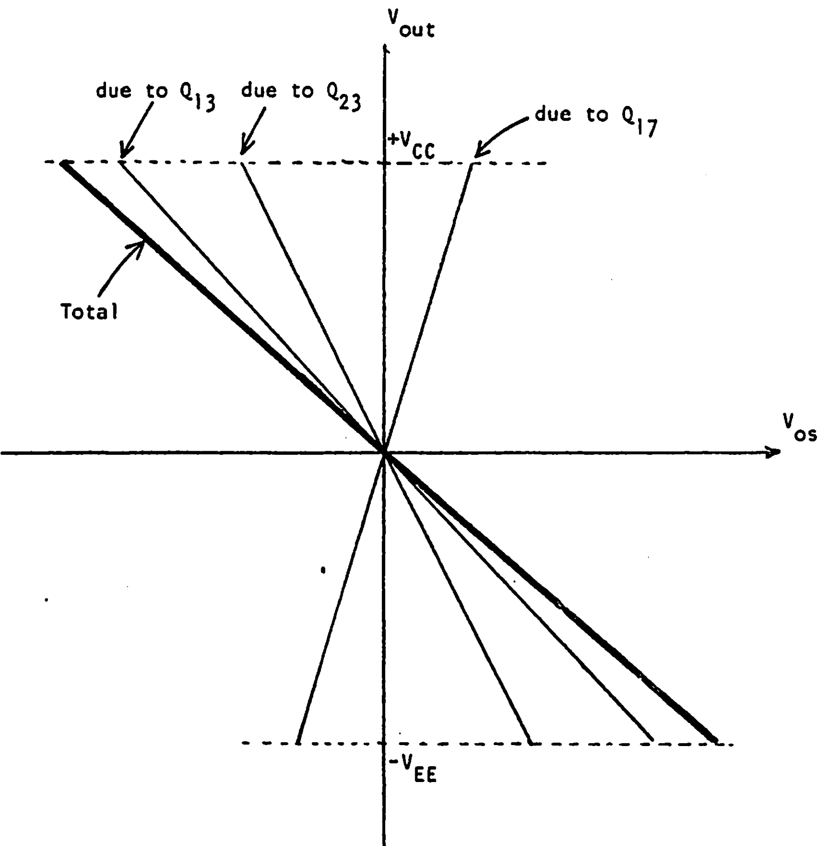


Fig. 2.9

Thermally induced offset voltage as a function of output voltage under no load condition

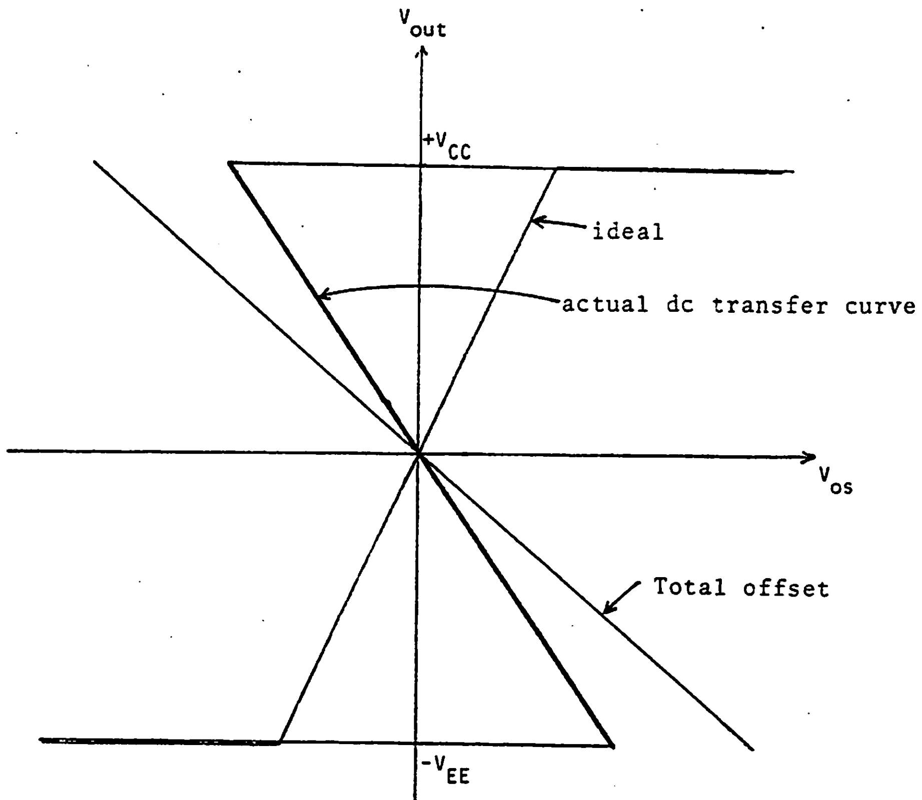


Fig. 2.10

Actual dc transfer curve with no load

voltage and the output voltage is altered when the load is attached to the output of the amplifier. In addition to the power dissipation in Q_{13}, Q_{17}, Q_{23}, that of Q_{14} and Q_{20} must be considered. The power dissipation in Q_{14} and Q_{20} are given as follows:

$$\text{For } V_{out} \geq 0,\quad P(Q14) \cong \left(\frac{V_{out}}{R_L}\right)(V_{CC} - V_{out}) \qquad P(Q20) \cong 0 \qquad (2\text{-}32a,b)$$

and for

$$V_{out} \leq 0,\quad P(Q14) \cong 0 \qquad P(Q20) = \frac{-V_o}{R_L}(V_{out} + V_{EE}) \qquad (2\text{-}33a,b)$$

The relationship between V_{out} and the power dissipation in Q_{14} and Q_{20} is shown in Fig. 2.11.

Since the thermally induced offset voltage is proportional to P(Q14), P(Q20), we may write

$$V_{osQ14} = \gamma_{Q14}P(Q14) = \gamma_{Q14}\left(\frac{V_{out}}{R_L}(V_{CC} - V_{out})\right) \qquad (2\text{-}34)$$

$$V_{osQ20} = \gamma_{Q20}P(Q20) = \gamma_{Q20}\left(-\frac{V_{out}}{R_L}\right)(V_o + V_{EE}) \qquad (2\text{-}35)$$

where γ_{Q14}, γ_{Q20} indicate the measure of coupling between Q14, Q20 and input pairs. Obviously the sign and magnitude of γ_{Q14} and γ_{Q20} will depend on their positions relative to the critical input pairs. In the case of this particular lay-out in Fig. 2.8, the sign of γ_{Q14} is opposite to that of γ_{Q20}. V_{osQ14} and V_{osQ20} are plotted in Fig. 2.12

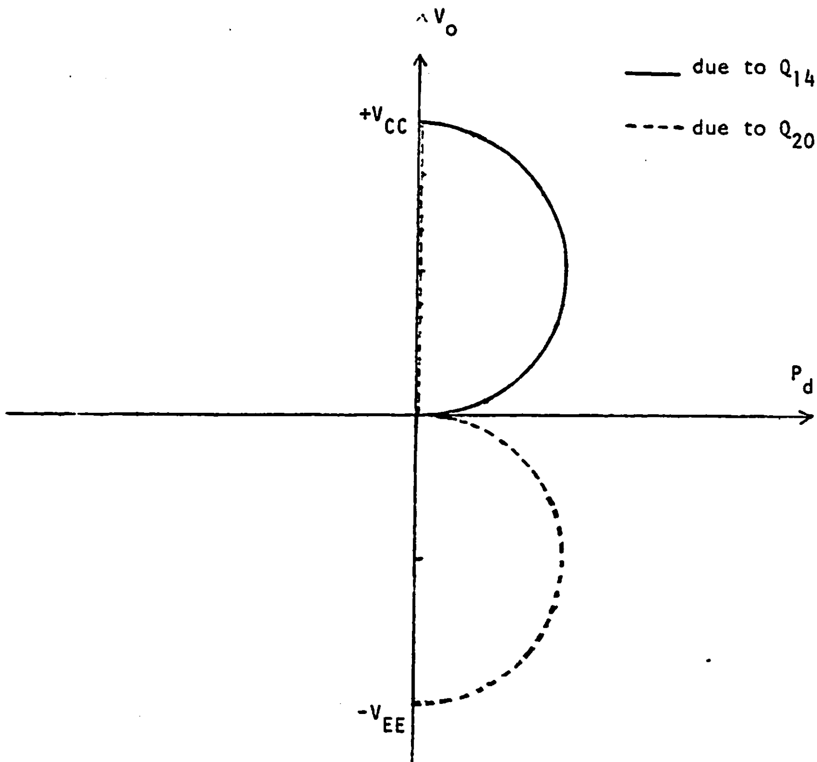


Fig. 2.11

Power dissipation in Q14 and Q 20 vs. V_{out}

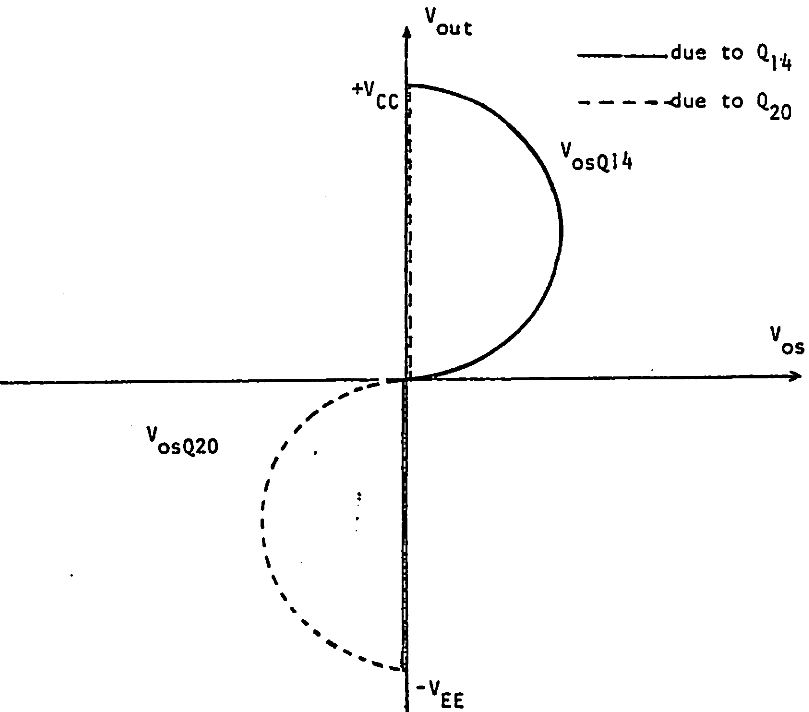


Fig. 2.12

Thermally induced offset voltage due to Q14, Q20 vs. V_{out}

as a function of V_{out}.

The total dc transfer characteristic under loaded condition is obtained by adding V_{osQ14}, V_{osQ20}, V_{osQ13}, V_{osQ23}, V_{osQ17} to the ideal characteristic. This is shown in Fig. 2.13.

The practical effects [12] of the thermal feedback in operational amplifiers are that (1) the effective value of dc open loop gain must be specified at a lower value than that which would be realizable considering electrical effects only; (2) when the amplifier is operated at low frequencies, the distortion due to this undesirable thermal feedback must be taken into consideration. Other types of circuits which are subject to these effects are those circuits which require high precision such as D/A converters, instrumentation amplifiers, analog multipliers, and precision voltage references, and those types of circuits which experience large amount of power dissipation such as voltage regulators, audio and servo amplifiers, etc.

2-4. Electro-thermal interaction as a design degree of freedom

Electro-thermal interactions are important as a design problem but can also be utilized as a design degree of freedom in certain types of integrated circuits. In this section, two such examples are given to demonstrate this utility.

2-4-1. Temperature stabilized substrate integrated circuit

A good example of the utilization of electro-thermal interactions to improve the performance of integrated circuit is that of temperature stabilized substrate system [13], shown in Fig. 2.14. The objective of the temperature stabilization system is to hold the chip temperature constant at an elevated value independent of the

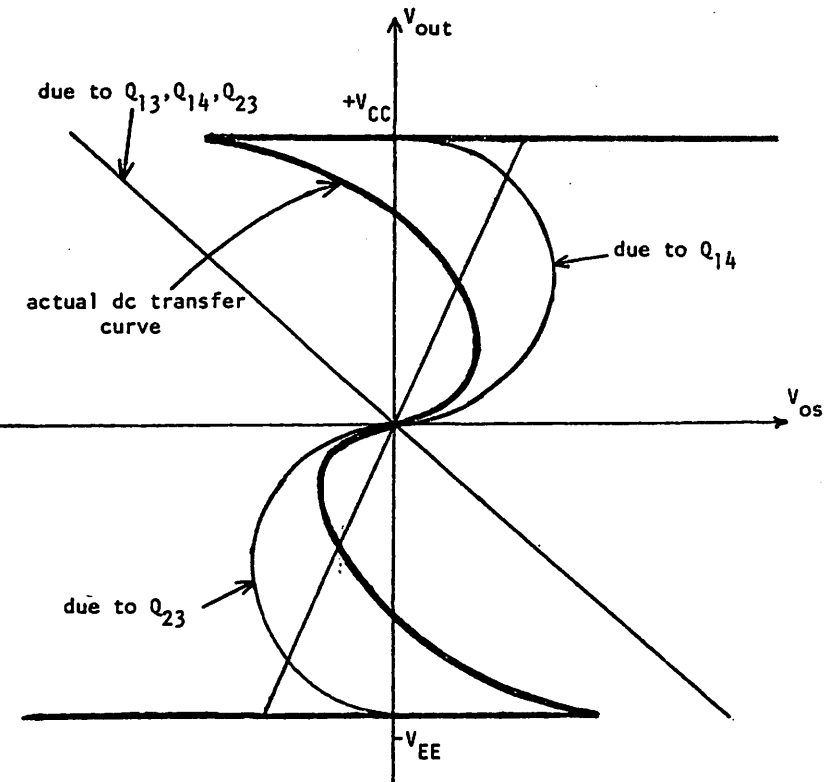


Fig. 2.13
Actual dc transfer curve under loaded condition

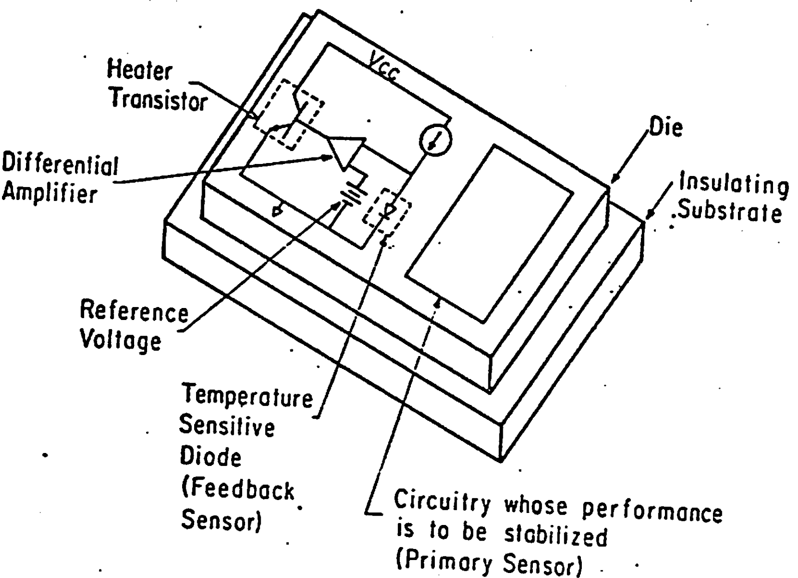


Fig. 2.14. Example TSS system

variations in ambient temperature so that the effective temperature sensitivity of the circuitry on the chip is reduced below that of an unstabilized chip. The stabilization is accomplished by including temperature sensor, reference source, error amplifier, and controlled heat source on the chip itself and by isolating the chip from its surrounding environment as shown in Fig. 2.14. Typically the temperature sensor consists of a diode which senses the temperature of the die by the change in its forward voltage drop as mentioned earlier in this chapter. Reference source is made of either band gap circuitry [14] or a diode compensated zener. The former uses the negative temperature coefficient of emitter base junction voltage in conjunction with the positive temperature coefficient developed in the emitter-base voltage differential of two transistors operating at different current densities to make a zero temperature coefficient reference, as shown in Fig. 2.15. The latter makes use of the positive temperature coefficient of breakdown voltage of zener diode and the negative temperature coefficient of diode as shown in Fig. 2.16.

An important consideration in the layout of such circuits is that when the ambient temperature varies, the power dissipation in the controlled heat source may vary. As a result temperature gradients across the surface of the chip vary as the ambient temperature changes. These varying gradients would in general cause a non-uniform temperature distribution among devices, for example, making up the reference sources. Consequently, the performance of the circuitry whose performance is to be stabilized can be severely degraded and cause the sensitivity of that circuitry to be much larger than otherwise expected.

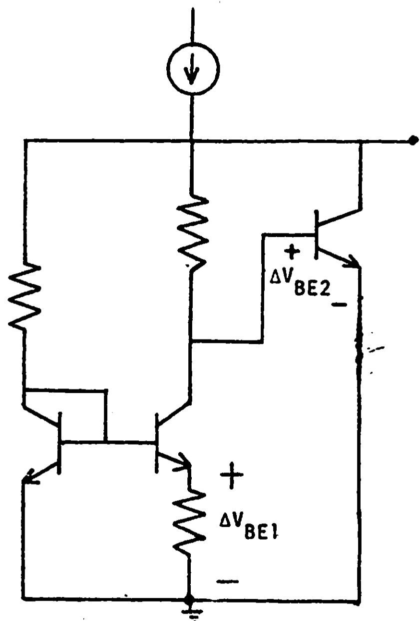


Fig. 2.15

Band Gap Reference Source

$$V_o = V_d(0) + V_z(0) + (\gamma_1 + \gamma_2)(T - T_o)$$

If $\gamma_1 + \gamma_2 = 0$, $V_o \neq f(T)$

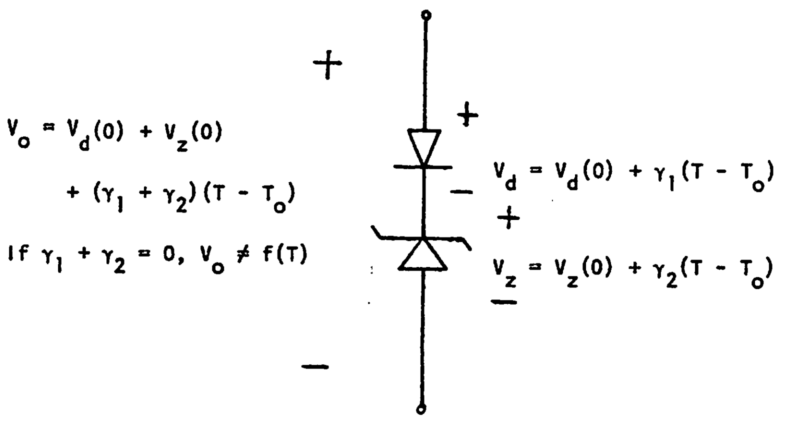


Fig. 2.16

Diode compensated zener voltage reference source

2-4-2. Thermal shutdown circuit

Another example of the use of electro-thermal interaction to improve circuit performance is the thermal shutdown circuit for power voltage regulators and power amplifiers [15]. These circuits must usually withstand load faults, such as short circuits, which cause an internal power dissipation of two to three times the rated power output. Unless the package is capable of dissipating this amount of power, the result is excessive chip temperature and device failure. The package dissipation requirements, and hence cost, can be greatly alleviated by including a circuit which, when the chip temperature exceeds a set maximum value, limits the output current of the circuit avoiding catastrophe failure. A simplified schematic of such a circuit contained in the µA7805 15 watt monolithic voltage regulator [16] is shown in Fig. 2.17.

As the temperature of the die rises, the voltage drop across the two diodes in series decreases, thereby further forward-biasing the transistor. At some threshold temperature Q_1 will turn on, diverting the current from the power transistor Q_2.

In attempting to arrive at an optimum shutdown circuit and layout, the problem is encountered that, when the circuit is activated, a feedback loop is closed which includes the thermal path from the output power transistor to the thermal sensor. Since the thermal capacitance of the chip is distributed, this thermal transfer function is irrational and will have large phase shift at high frequencies, depending on the separation of heat source and temperature sensor. From an application point of view, the loop must be stable as the output current is limited. Further, localized dissipation of 15 watts

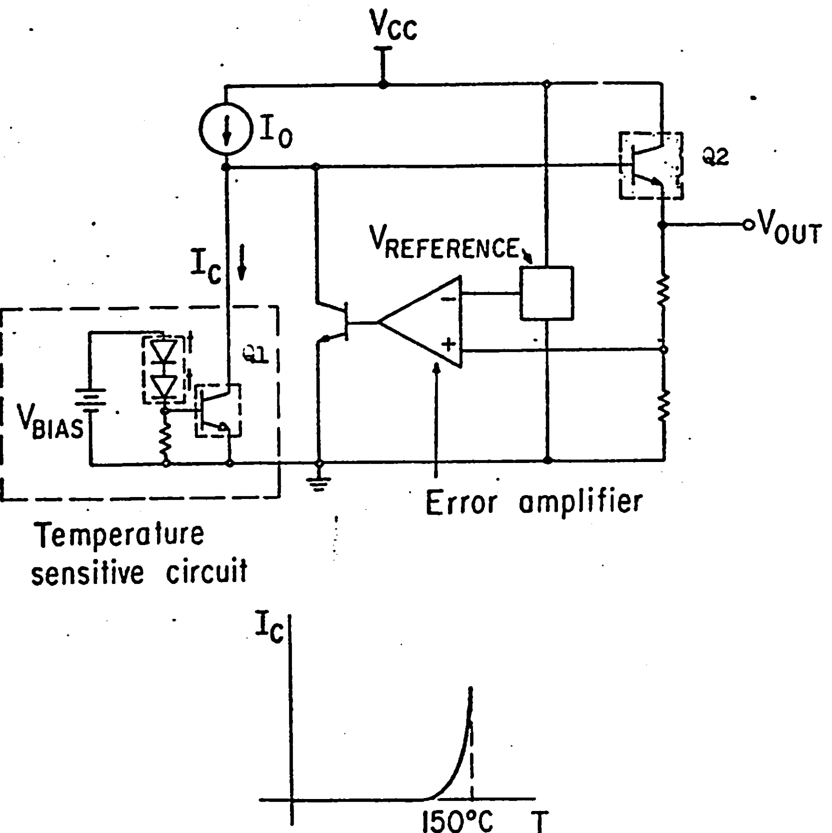


Fig. 2.17. Simplified schematic of μa 7805 15 watt monolithic voltage regulator.

or more can cause temperature difference of 10°C-50°C across the die. Thus the temperature sensor is not at the same temperature as the power transistors. This must be taken into account in setting the temperature threshold.

Other applications of electro-thermal interactions to improve circuit performance include thermal shutdown circuits for electro-thermal multi-vibrators and electro-thermal low frequency filters [17].

CHAPTER 3

LUMPED MODELING OF DIE-PACKAGE STRUCTURE

3-1. Introduction

One of the most important problems in the development of a generally useful electro-thermal simulation program is that of adequately modeling the thermal behavior of the die-package structure with an effective compromise between accuracy in simulation on the one hand and economy in computer simulation time on the other. In this chapter some of the widely used die-package structures are considered. Reasonable assumptions are made, and consequently, a simplified physical model is obtained. Then the finite difference approximation of the flow equation is used to derive a lumped model of the die-package structure which gives reasonable level of complexity in terms of accuracy, yet provides economical node count. At the end of the chapter, error introduced by the finite difference approximation is analyzed.

3-2. Typical die-package structures

There are three types of well-established integrated circuit packages in common use. They are the TO-type package, the ceramic flat package and the ceramic and plastic dual in-line packages. Shown in Fig. 3.1 are the physical structures of TO package, flat package and the plastic dual in-line package [18].

In all three of them, the die is mounted on an underlying

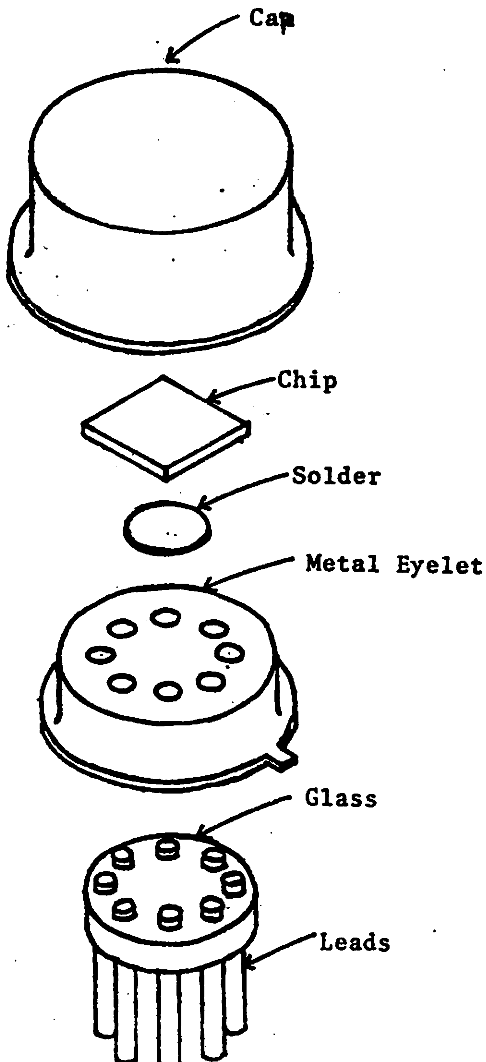


Fig. 3.1(a)

Exploded view of TO-type package

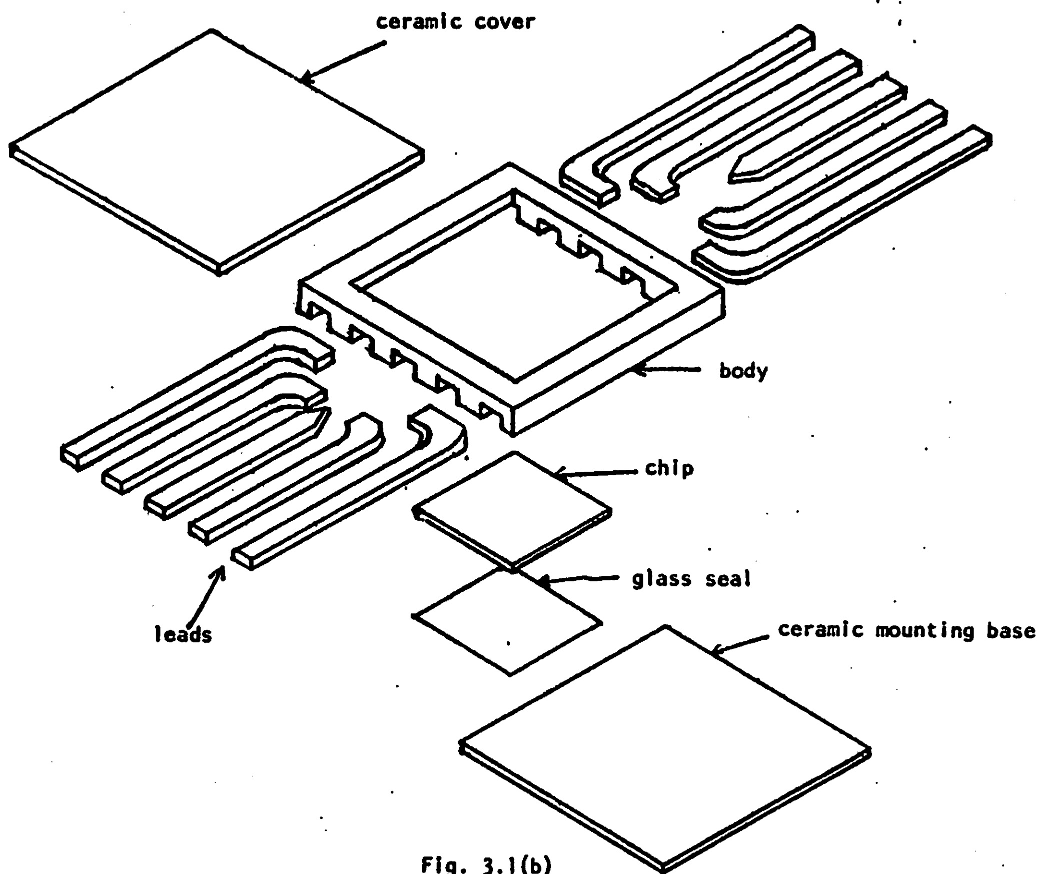


Fig. 3.1(b)

Exploded view of flat package

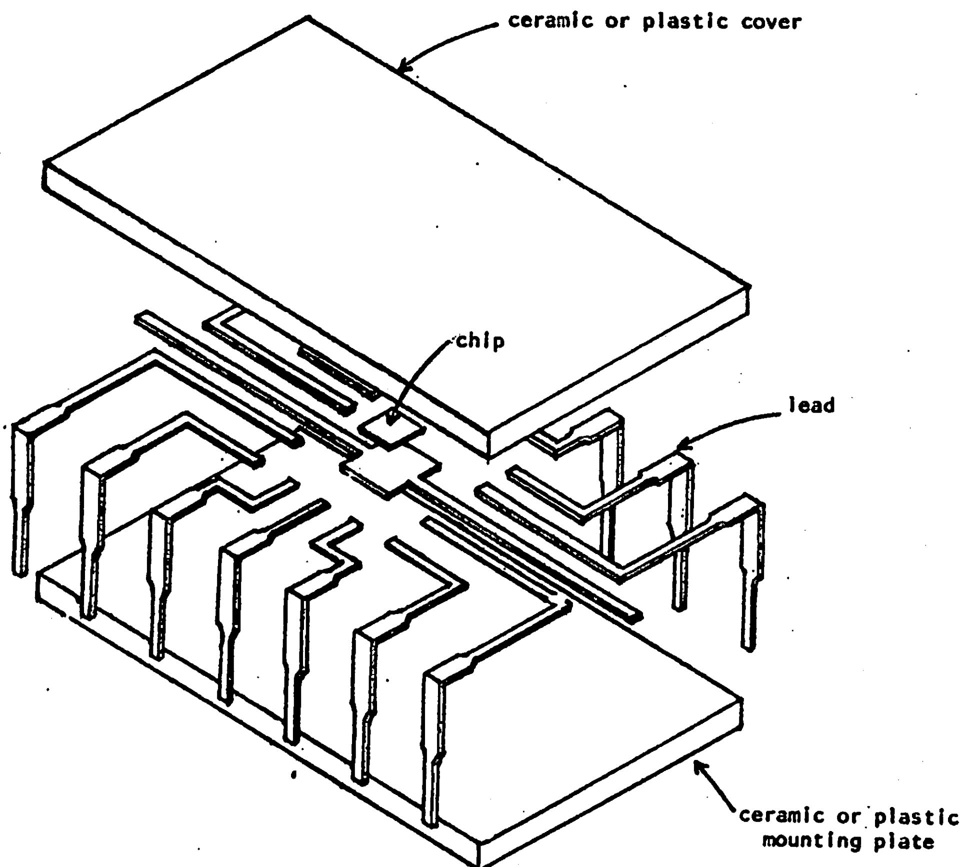


Fig. 3.1(c)

Exploded view of DIP package

package material (called header) with which it is in intimate thermal contact. The package in turn is subject to a complex set of thermal boundary conditions. The aspects of the thermal behavior of the package which are important to the electrical behavior of the circuit are two-fold. First, the package dictates the total thermal resistance between the top surface of the chip and the ambient atmosphere. Second, the presence of the header material underneath the die and in intimate thermal contact with it affects the temperature distribution on the top surface of the die because of a lateral thermal conductance in the header material. On the other hand, the regions remote from the die have little effect on the performance of the integrated circuit. In order to properly model those two effects without introducing unnecessary complexity in the modeling of the remote regions, a simplified model was adapted as shown in Fig. 3.2.

This simplified physical model consists of the die and a piece of the underlying header material. The rectangular piece of header material is in turn mounted on an isothermal substrate. In order to adjust the net junction to ambient thermal resistance to the proper value, a thermally conducting interface is included between the header material and the isothermal surface. In addition, the thermal capacitance of the remainder of the package structure outside of the rectangular piece may be included in lumped form in a strip around the outside edge of the rectangular block. With this model, the lumped modeling of the die-package structure employing finite difference approximation can be easily carried out without incurring excessive number of thermal nodes as will be shown later in this chapter. At the same time the important thermal behavior on the top surface of the

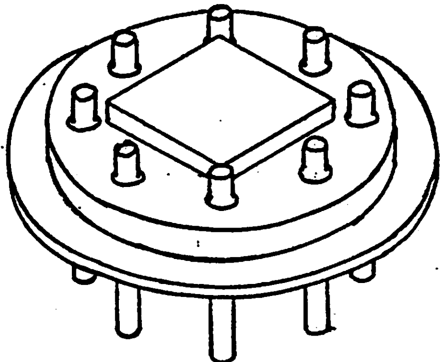


Fig. 3.2(a)

Physical structure

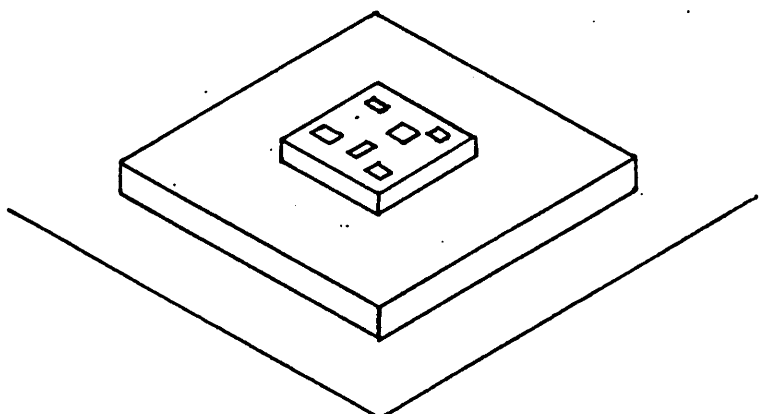


Fig. 3.2(b)

Simplified model

chip is adequately modeled without introducing unnecessary complexity in the modeling of the remote regions. This will also be explained later. Thus this simplified physical model provides an adequate compromise between accuracy in simulation and efficient use of computer time.

3-3. The symmetrical finite difference approach

With the selection of the simplified physical model, the next problem is the generation of lumped representation of this physical structure. The usual approach to the lumped modeling of such a rectangular structure is the symmetrical finite difference approach [3]. With this technique the solid which is to be modeled is subdivided into subregions which have a rectangular plain view shown in Fig. 3.3(a). Each subregion can be represented by a set of six thermal resistors and one thermal capacitor as will be shown. One subregion of Fig. 3.3(a) is shown in Fig. 3.3(b). For this subregion, the heat, $P_{x=x_2}$ flowing out through the cross section at $x = x_2$ is

$$P_{x=x_2} = -\int_{z_1}^{z_2}\int_{y_1}^{y_2} k \left.\frac{dT}{dx}\right|_{x=x_2} dydz = -k\int_{z_1}^{z_2}\int_{y_1}^{y_2} \left.\frac{dT}{dx}\right|_{x=x_2} dydz \quad (3\text{-}1)$$

where k is the thermal conductivity of the material. If we approximate

$$\left.\frac{dT}{dx}\right|_{x_2}$$

as

$$\left.\frac{dT}{dx}\right|_{x_2} = \frac{T_{200} - T_{000}}{x_2 - x_o}$$

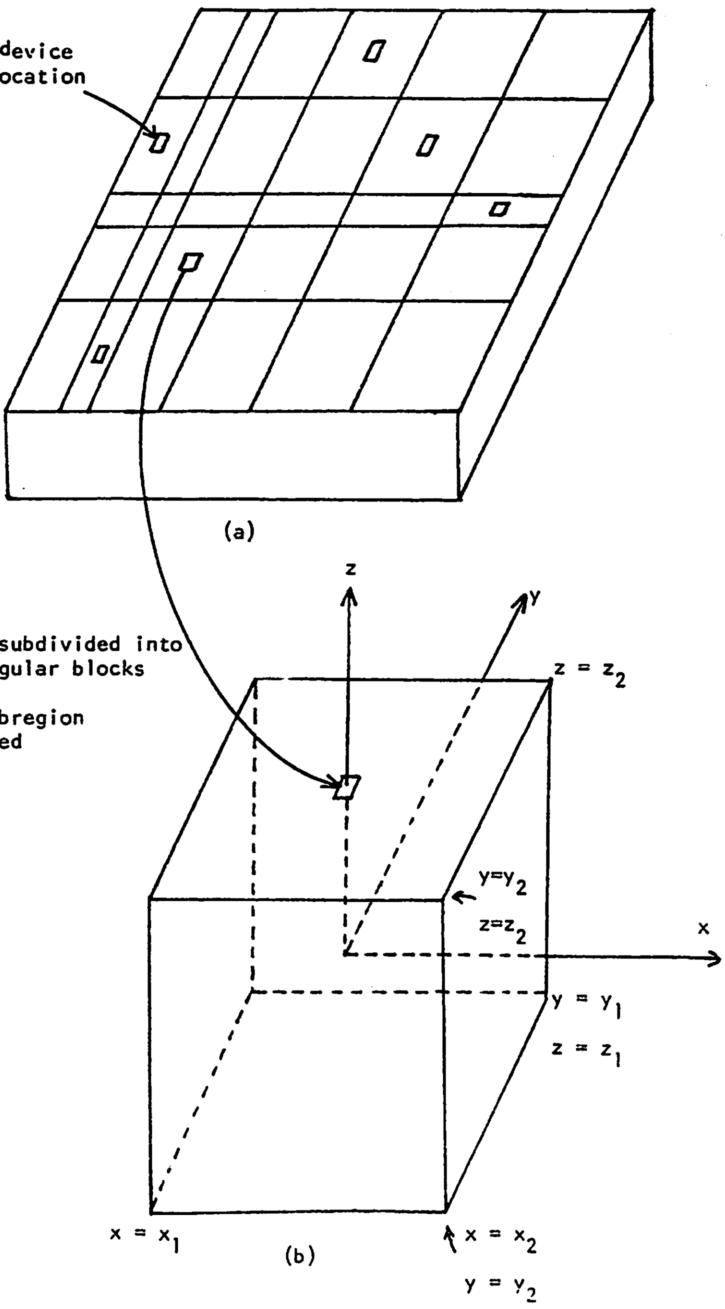


Fig. 3.3

(a) Solid subdivided into rectangular blocks

(b) One subregion expanded

where $T_{200} = T(x_2, 0, 0)$

$T_{000} = T(0, 0, 0)$

and assume that $\left.\frac{dT}{dx}\right|_{x_2}$ is constant over the plane bounded by $x = x_2$, $y_1 < y < y_2$, $z_1 < z < z_2$, then we can write

$$P_{x=x_2} = -k\int_{z_1}^{z_2}\int_{y_1}^{y_2} \left.\frac{dT}{dx}\right|_{x_2} dydz = k\left(\frac{T_{000} - T_{200}}{x_2 - x_o}\right)(y_2 - y_1)(z_2 - z_1)$$

$$= \frac{k(y_2 - y_1)(z_2 - z_1)}{x_2 - x_o}(T_{000} - T_{200}) \qquad (3\text{-}2)$$

At this point we can construct an analog model for the thermal system in which current, voltage, and conductance in electrical system correspond to power, temperature, and thermal conductance. When this is done one can easily recognize that the equivalent thermal conductance G_{TH} is given by

$$G_{TH} = \frac{k(y_2 - y_1)(z_2 - z_1)}{x_2 - x_o} \qquad (3\text{-}3)$$

and

$$P_{x=x_2} = G_{TH}\cdot(T_{000} - T_{200})$$

Similarly, we can calculate thermal conductance in other directions. The resulting equivalent circuit model for the subregion is shown in Fig. 3.4.

The thermal storance associated with a subregion can be obtained from continuity equation. Referring to Fig. 3.4 the total power flowing out of the node N_o is

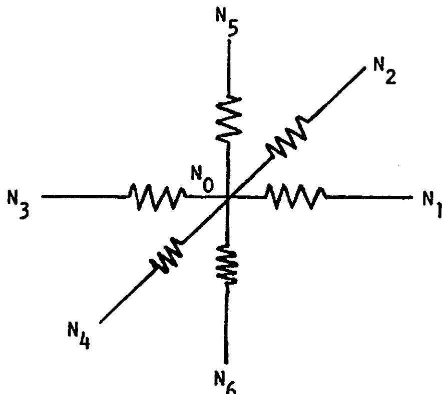


Fig. 3.4

Equivalent circuit model for a subregion

$$P_{out} = \sum_{i=1}^{6} G_i(T_o - T_i)$$

where T_i is the temperature of the surrounding nodes,

G_i is the conductance between nodes N_o and N_i.

The net power $(P_{in} - P_{out})$ is the heat energy stored per unit time. Thus we can write

$$P_{in} - P_{out} = \frac{d}{dt}\int_V \rho c T dV \qquad (3\text{-}5)$$

where ρc is the specific heat of the material,

$dV = dxdydz$, and

V corresponds to the volume of the subregion.

If we assume that T is constant within the volume element, then we can write

$$P_{in} - P_{out} = V\rho c \frac{dT}{dt} = C_{TH}\frac{dT}{dt} \qquad (3\text{-}6)$$

where $C_{TH} = V\rho c$.

Thus we obtain the thermal capacitance associated with this node:

$$C_{TH} = V\rho_s c_s \qquad (3\text{-}7)$$

The completed model for this subregion is shown in Fig. 3.5.

The finite difference approximation approach is attractive in that the thermal network algorithm can be implemented very easily. However, this approach presents a difficult problem for typical integrated circuit layouts. Proper matching of the boundary conditions on the top surface of the chip requires that each active

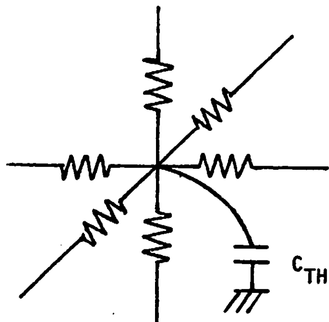


Fig. 3.5

Complete circuit model for a subregion

electrical circuit element on the die have one subregion associated with it. This requirement results in the formation of a number of nodes which is greatly in excess of the number of electrical elements on the surface of the die as illustrated in the example of Fig. 3.3(a). For N device locations on a chip it will in general create N^2 thermal nodes. Even for a simple operational amplifier, N can be easily over 30, which causes the total number of thermal nodes to be 900! This excessive number of thermal nodes results in high cost in the computation and large memory space requirements.

3-4. Asymmetrical finite difference approach

With the symmetrical finite difference approach, one node is associated with every rectangular subregion. A better approach that can be used to avoid this problem is a generalization of the symmetrical finite difference approach. In this method a network of triangles is formed by connecting the thermal nodes corresponding to device locations and some internally created nodes necessary to insure that none of the interior angles of triangles are obtuse. By employing the finite difference approximation to the network thus formed, the values of the thermal resistance and capacitances are easily evaluated. The detail of the theory behind this approach is now presented in a slightly different fashion from the original derivation by Mr. McNeal [19].

Our objective can be stated as follows: Given randomly distributed nodes we wish to connect every node to its adjacent nodes with an equivalent thermal resistance in order that the temperatures at the nodes will be as near as possible the correct solution of the general

heat flow equation. Suppose we pick for any triangles a point interior to the triangle and connect it to its three adjacent points chosen in like manner in an arbitrary fashion, as shown by the dark lines in Fig. 3.6. Now let us define the current flowing through the common boundary c-d as the current flowing through the resistor connecting nodes A and B. This current I_{AB} is given by

$$I_{AB} = -\int_c^d k\vec{\nabla}T.\vec{dr} \qquad (3\text{-}8)$$

where $\vec{dr}$ is along the common boundary c-d. The voltage (temperature) difference between A and B is given by

$$V_{AB} = \int_A^B -\vec{\nabla}T.\vec{dl} \qquad (3\text{-}9)$$

where $\vec{dl}$ is along the line segment connecting nodes A and B.

Thus the equivalent resistance R_{AB} between nodes A and B is given by

$$R_{AB} = \frac{V_{AB}}{I_{AB}} = \frac{\int_A^B - \vec{\nabla}T.\vec{dl}}{k\int_C^D - \vec{\nabla}T.\vec{dr}} \qquad (3\text{-}10)$$

The resistance value evaluated above is of no significance since it depends on a particular temperature distribution. If we can make R_{AB} independent of temperature distribution by suitably choosing points c to d, then we will have succeeded in forming equivalent circuit representation of the thermal behavior. In general this is not possible. Suppose we choose c and d in their respective triangles such that the perpendicular bisectors of the three line segments

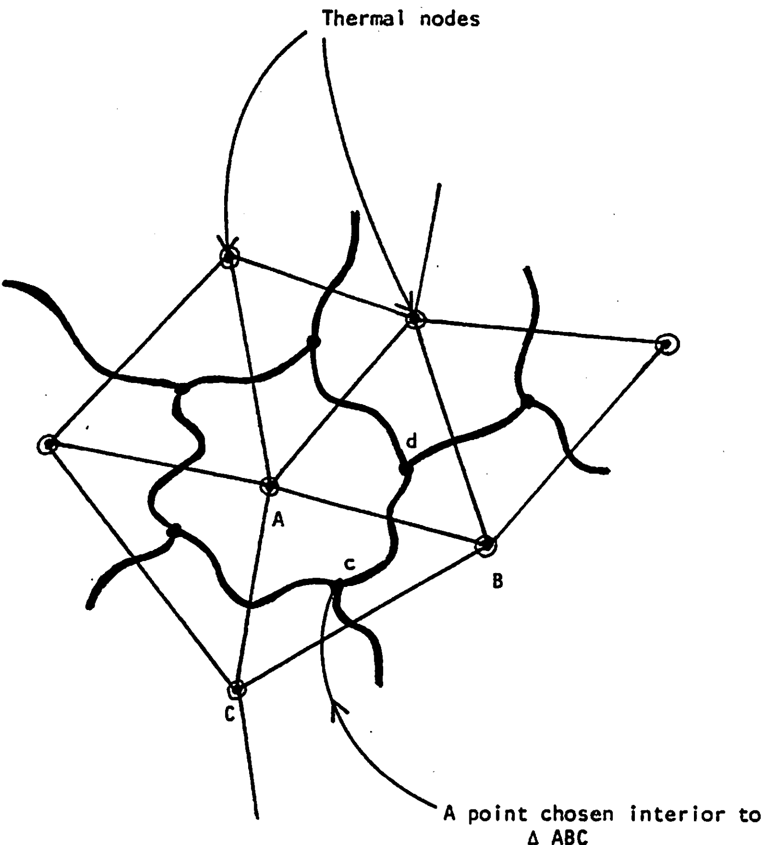


Fig. 3.6

Asymmetrical thermal network with arbitrarily defined common boundary

comprising the triangles meet at c and d, and define the integration path along the straight lines connecting c and d, as shown in Fig. 3.7. As long as all the inner angles of triangles are not obtuse, the three bisecting lines will meet at one point inside the triangle. With this particular choice of c and d the integration path has a special attractive feature that if $\vec{\nabla T}$ = constant, then

$$V_{AB} = \int_A^B -\vec{\nabla T}.\vec{dl} = -\nabla T l_{AB} \cos\alpha \qquad (3\text{-}11)$$

$$I_{AB} = \int_A^B -k\vec{\nabla T}\vec{dr} = -kr_{cd} \cos\alpha \qquad (3\text{-}12)$$

Thus

$$R_{AB} = \frac{l_{AB}}{kr_{cd}} \qquad (3\text{-}13)$$

where α is the angle between $\vec{dl}$ and $\vec{\nabla T}$.

R_{AB} is now dependent only upon the physical property of the material and the manner in which the region is subdivided. This concept is now carried out for three-dimensional case and error analysis will follow in the next section.

For three-dimensional case, the block of material can be subdivided in the similar manner as shown in Fig. 3.8. In this case

$$V_{AB} = -\int_A^B \vec{\nabla T}.\vec{dl} \qquad (3\text{=}14)$$

$$I_{AB} = -\int_S k(\vec{\nabla T}).\vec{ds} \qquad (3\text{-}15)$$

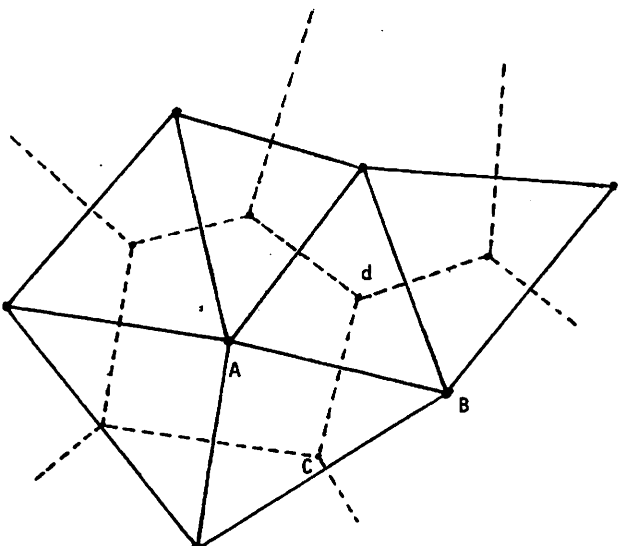
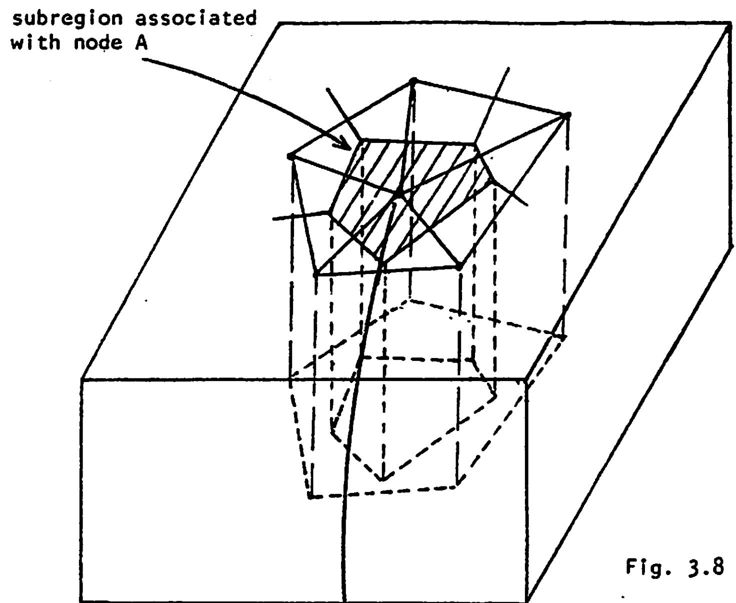


Fig. 3.7

Asymmetrical thermal network



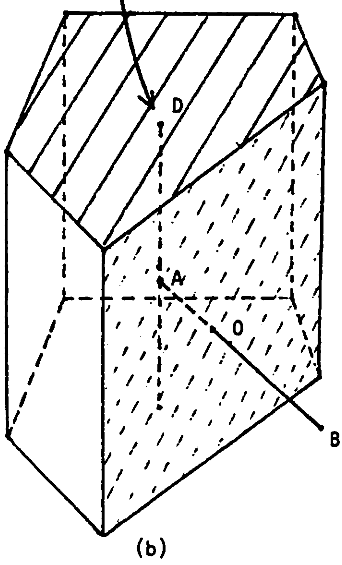


Fig. 3.8

(a) Asymmetrical thermal network in three dimensions

(b) An expanded subregion

where S is the plane denoted by dashed lines in Fig. 3.8. If we assume that

$$\vec{\nabla}T \cong (\vec{\nabla}T)_0 = \text{constant along the line segment } \overline{AB} \text{ and over the area S} \quad (3\text{-}16)$$

where $(\vec{\nabla}T)_0$ is $\vec{\nabla}T$ evaluated at node 0, then

$$V_{AB} \cong -(\vec{\nabla}T)_0 l_{AB} \cdot \cos\alpha \quad (3\text{-}17)$$

$$I_{AB} \cong -k(\vec{\nabla}T)_0 r_{cd} \cdot \Delta z . \cos\alpha \quad (3\text{-}18)$$

where α is the angle between the line segment $\overline{AB}$ and $(\vec{\nabla}T)_0$. Thus

$$R_{AB} = \frac{V_{AB}}{I_{AB}} = \frac{l_{AB}}{k \Delta z \ r_{cd}} \quad (3\text{-}19)$$

In the identical manner all the thermal resistance to the adjacent nodes in horizontal plane are evaluated. The thermal resistor between A and D is calculated as follows:

$$V_{AD} = -\int_A^D \vec{\nabla}T . d\vec{a} \quad (3\text{-}20)$$

$$I_{AD} = -k \int_{S_{top}} \vec{\nabla}T . d\vec{s} \quad (3\text{-}21)$$

where S_{top} is the area of polygon on the top surface. If we assume that

$$\vec{\nabla}T \cong (\vec{\nabla}T)_D = \text{constant} \quad (3\text{-}22)$$

along the line segment $\overline{DA}$ and over S_{top}, then

$$V_{AD} \cong -(\vec{\nabla}T)_D \cdot l_{AD} \cos\alpha \quad (3\text{-}23)$$

$$I_{AD} \cong -k(\vec{\nabla}T)_D \cdot S_{top} \cos\alpha \quad (3\text{-}24)$$

where α is the angle between $(\vec{\nabla}T)_D$ and $\overline{DA}$. Thus

$$R_{AD} \cong \frac{\ell_{AD}}{kS_{top}} \quad (3\text{-}25)$$

Similarly

$$R_{AC} \cong \frac{\ell_{AC}}{kS_{top}} \quad (3\text{-}26)$$

The thermal capacitance associated with each subregion is evaluated in the same way as the symmetrical finite difference method. Since each node has a volume element associated exclusively with itself, one can attribute the heat stored in that volume element to that node. (See Fig. 3.8(b).) The continuity equation gives the following equation:

$$P_{in} - P_{out} = P_{in} - \sum_{i=1}^{N} (T_A - T_i)/R_{Ai}$$
$$= \frac{d}{dt} \int_V \rho_s c_s T dV \quad (3\text{-}27)$$

where T_A is the temperature of the node A,

R_{Ai} is the thermal resistance between node A and its adjacent node i,

N is the total number of nodes connected to node A.

If we assume that

$$T = T_A = \text{constant}$$

within this volume element, then

$$P_{in} - P_{out} = \rho c V \frac{dT}{dt} \qquad (3\text{-}28)$$

Therefore

$$C_{TH} = \rho c V \qquad (3\text{-}29)$$

The resulting equivalent circuit employing asymmetrical approach for the example of Fig. 3.9(a) is shown in Fig. 3.9(b). The identical thermal network is formed for the portion of the header directly underneath the die. In addition to these thermal nodes, several additional nodes are created along the outside edges of the rectangular header as shown in Fig. 3.9(a). Obviously the density of thermal nodes in the header region not directly underneath the die is sparse. However this arrangement is adequate to model the thermal behavior of the region remote from the active device locations. A typical subregion of the die-header sandwich is shown in Fig. 3.10. The resistance leading to the ambient represents a portion of the junction-to-ambient thermal resistance. Each subregion has one thermal resistance leading to the ambient and its conductance is scaled according to the bottom area of the subregion. Therefore the values of these resistances must be obtained numerically so as to adjust the total junction to ambient thermal resistance to a user-specified value. In the program developed the temperature is calculated twice on the top surface of the chip at

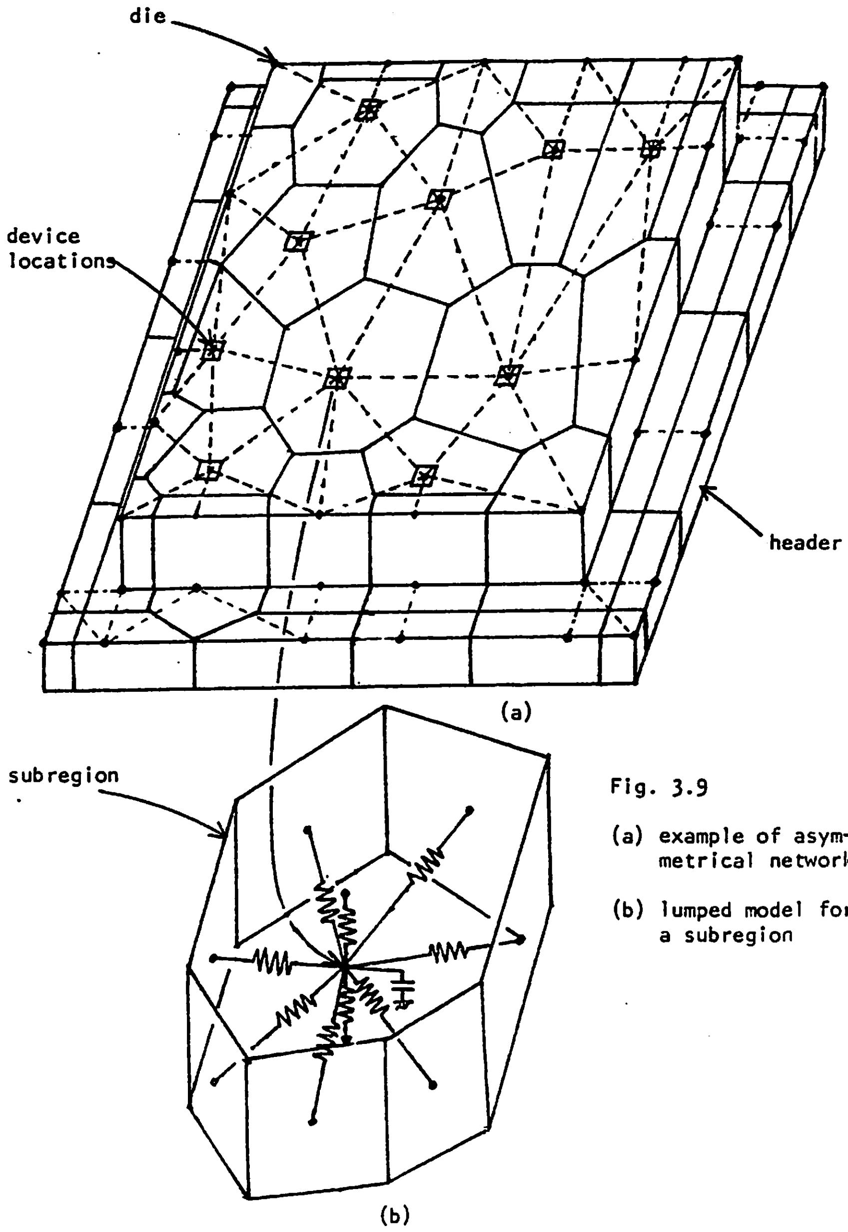


Fig. 3.9

(a) example of asymmetrical network

(b) lumped model for a subregion

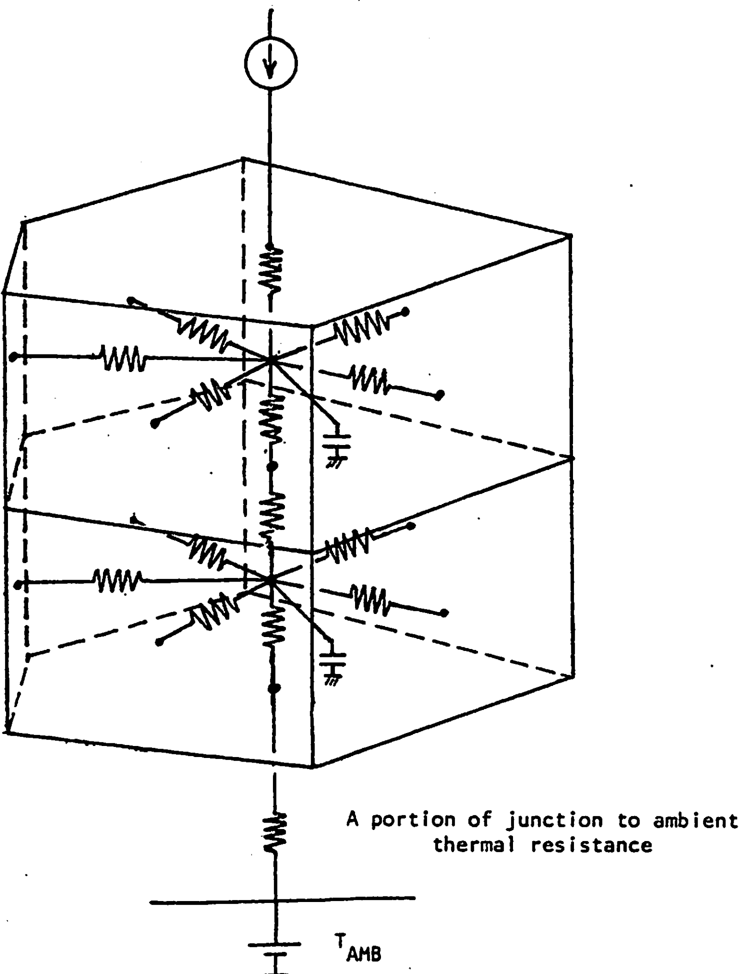


Fig. 3.10

A typical subregion of the die-header sandwich

two different sets of this interface conductance, $1.5G_{TH}$ and $2.0G_{TH}$, where G_{TH} is the user-specified junction-to-ambient thermal conductance. (That is, the thermal conductance of $1.5G_{TH}$ and $2.0G_{TH}$ are distributed over the bottom surface of the header, in proportion to the bottom area.) The final value of this interface conductance is linearly interpolated. If the exact value is desired several iterations will be necessary.

Two thermal network formation algorithms were written to implement this approach. The first algorithm forms a triangular thermal network formation at the expense of large thermal node count. The second algorithm forms the network in a different manner from that of the first algorithm typically resulting in smaller thermal node count. However, this algorithm does not always complete the network formation successfully. To ensure its success some extra data must be entered. The first algorithm was incorporated into programs T-SPICE2A and T-SPICE2B. The second algorithm is separately written in the program T-SPICE2C. (T-SPICE2A and T-SPICE2B are introduced in the next chapter. For the detail of the two algorithms see Appendix 3.) Since the devices are not always located so as to form a network of triangles whose inner angles are all less than 90 degrees, some additional nodes have to be created to ensure this requirement is met. In addition to this, a proper matching of boundary conditions around the edges of the rectangular structure requires that more nodes be created along the outside edges. Due to these difficulties, the algorithms typically create three to five times the number of total device locations for each layer. Note that there does not exist a unique way of forming thermal networks. Although this is considerably better

than the symmetrical finite approximation method, more improvement can be made. The total number of nodes created on the header layer is slightly greater than that for chip plane.

Three important limitations arise from this modeling approach [12]. The first is that in circuits which contain only a few circuit elements which are widely spaced physically, the thermal model will not contain enough thermal nodes to predict accurately the chip temperature distribution. To avoid this problem, the user must introduce additional nodes to insure that no point on the surface of the chip is separated from its adjacent node by more than Δl where Δl is to be chosen consistent with the accuracy desired. This point will be discussed more in detail in the next section.

A second important limitation is that the heat sources are represented as point sources, and the temperature sensitivity of any element is localized at one point. Device structures are often encountered which are distributed over a large area, large resistors and power resistors being the best examples. These structures can be accurately modeled by the user of the program by representing them as being composed of a number of individual devices connected in parallel or series as appropriate. Each of the individual devices has a different physical location. Such an approach is particularly important in the modeling of power transistors where nonuniform current distribution in the device is an important thermal effect.

A third important limitation is that since the thermal nodes are separated by a distance on the order of the electrical device separation, thermal phenomenon which take place over distances shorter than this are not well modeled. Thus, for example, certain self-

heating effects which occur in very small geometry devices operated at high power densities with short pulse widths will not be accurately predicted. Such phenomenon depend heavily on the temperature distribution with a few tens of microns of the device in the vertical and horizontal directions.

Thermal capacitance associated with the die-package structure other than those already mentioned can be included in a lumped form around the outside edges of the header. However this was not done in an actual analysis of the program due to the following reasons:

(1) In most cases the thermal time constant associated with this portion of the structure is very large and the details of thermal behavior in this order of time scale is of no interest.

(2) When widely separated time constants are involved in the transient analysis, the cost of computation becomes excessive. This is particularly true in the light of the fact that the ratio of the smallest electrical time constant and the largest thermal time constant could be as large as 10^{10}.

If one is interested in the thermal behavior in the time scale of thermal time constant energy storage elements of the system, one can simply neglect the electrical energy storage elements.

The effects of bonding wires and voids are not included in the present program but ground work is laid out in such a way that their inclusion is straightforward.

3-5. Error analysis of the finite difference approximation

The error introduced by the finite difference approximation in three-dimensional case is in general difficult to evaluate. We will

first reduce this error analysis to a two-dimensional problem by making a physically reasonable assumption that the temperature variation in vertical direction is linear. That is,

$$\left.\frac{\partial T}{\partial z}\right|_{x=y=constant} = \text{constant} \qquad (3\text{-}30)$$

This assumption is reasonable because a silicon chip is a highly thermal conductivity material and usually very thin. Any heat generated on the top surface of the chip will flow mainly in vertical direction. Obviously if the heat generated is uniform over the entire surface of the chip, this is a correct assumption aside from slight deviation around the edges of the chip. The validity of this assumption may be violated if

(1) the heat source on the top surface of the chip is narrowly confined in an area smaller compared to mesh size;

(2) the header material is made of a material of high thermal conductivity.

With this assumption the error analysis is made essentially two dimensional.

First we calculate the error in temperature introduced by the finite difference approximation. Let us assume that the temperature distribution is given by T(x, y, z). Referring to Fig. 3.8, choose the point "O" as the origin of X and Y rectangular coordinates and let the line segment $\overline{AB}$ be the X axis. If we Taylor expand the temperature distribution T along X axis about the origin, we obtain

$$T(x, 0, 0) = T(0, 0, 0) + \left.\frac{dT}{dx}\right|_{x=y=z=0} x + \frac{1}{2!}\left.\frac{d^2T}{dx^2}\right|_{x=y=z=0} x^2$$

$$+ \frac{1}{3!}\left.\frac{d^3T}{dx^3}\right|_{x=y=z=0} x^3 + \ldots \qquad (3\text{-}31)$$

The exact temperature difference $(T_{AB})_{EXACT}$ between two nodes at $x = x_1$ and $x = x_2$ is given by

$$(T_{AB})_{EXACT} = T_A - T_B = T(x_1, 0, 0) - T(x_2, 0, 0)$$

$$\cong - \left.\frac{dT}{dx}\right|_{x=y=z=0} \Delta x - \frac{1}{6}\left.\frac{d^3T}{dx^3}\right|_{x=y=z=0} \cdot \frac{\Delta x^3}{4} \qquad (3\text{-}32)$$

where $\Delta x = x_2 - x_1$, and we used the fact that

$$|x_1| = |x_2|$$

The finite difference approximation gives, from Eq. (3-17)

$$(T_{AB})_{APPROX} = -|\vec{\nabla} T_o|\ x.\cos\alpha = - \left.\frac{dT}{dx}\right|_{x=y=z=0} \Delta x \qquad (3\text{-}33)$$

Therefore the first order error ΔT_{AB} is

$$\Delta T_{AB} = |(T_{AB})_{EXACT} - (T_{AB})_{APPROX}| = \frac{1}{6}\left.\frac{d^3T}{dx^3}\right|_{x=y=z=0} \cdot \frac{\Delta x^3}{4}$$

$$= \frac{\Delta x^3}{24}\left.\frac{d^3T}{dx^3}\right|_{x=y=z=0} \qquad (3\text{-}34)$$

Now we calculate the error in heat flow. Let us first define

$$f(y, z) \equiv \left.\frac{dT}{dx}\right|_{x=0} \qquad (3\text{-}35)$$

Then, the exact amount of heat flow $(P_{AB})_{EXACT}$ from node A to node B is given by

$$(P_{AB})_{EXACT} = -k\int_{z_1}^{z_2}\int_{y_1}^{y_2} f(y, z)\,dydz \qquad (3\text{-}36)$$

If we Taylor expand f in the y and z directions about the origin we obtain,

$$f(y, z) = f(0, 0) + \left(y \left.\frac{\partial f}{\partial y}\right| + z \left.\frac{\partial f}{\partial z}\right|\right) + \frac{1}{2}\left(y^2 \left.\frac{\partial^2 f}{\partial y^2}\right| + 2yz \left.\frac{\partial^2 f}{\partial y \partial z}\right|\right.$$

$$\left. + z^2 \left.\frac{\partial^2 f}{\partial z^2}\right|\right) + \frac{1}{3!}\left(\left.\frac{\partial^3 f}{\partial y^3}\right| + 3y^2 z \left.\frac{\partial^3 f}{\partial y^2 \partial z}\right|\right.$$

$$\left. + 3yz^2 \left.\frac{\partial^3 f}{\partial y \partial z^2}\right|\right) + \ldots \qquad (3\text{-}37)$$

where all the derivatives are evaluated at y = z = 0. Thus we obtain,

$$(P_{AB})_{EXACT} = -k\int_{z_1}^{z_2}\int_{y_1}^{y_2} f(y, z)\,dydz = -k\{f(0, 0)\Delta y \Delta z$$

$$+ \frac{1}{2}\left.\frac{\partial f}{\partial y}\right| \left[y^2 \Delta z\right]_{y_1}^{y_2} + \frac{1}{2}\left.\frac{\partial f}{\partial z}\right| \left[z^2 \Delta y\right]_{z_1}^{z_2}$$

$$+ \frac{1}{2}\left(\frac{1}{3} y^3 \left.\frac{\partial^2 f}{\partial y^2}\right| \Delta z\right]_{y_1}^{y_2} + \frac{1}{2} y^2 z^2 \left.\frac{\partial^2 f}{\partial y \partial z}\right]_{y_1}^{y_2}\Big]_{z_1}^{z_2}$$

$$+ \frac{1}{3} z^3 \left.\frac{\partial^2 f}{\partial z^2}\right| \Delta y\Big]_{z_1}^{z_2}\Big) + \ldots\} \qquad (3\text{-}38)$$

where $\Delta z = z_2 - z_1$, $\Delta y = y_2 - y_1$

Now if we use the assumption Eq. (3-30), the third, fifth and sixth terms on the right-hand side vanish. Obviously if "0" is the midpoint of the line segment $\overline{z_1 z_2}$, the third and fifth terms vanish independent of the assumption Eq. (3-30). If we further assume that "0" is the midpoint of $\overline{y_1 y_2}$, then the second term also vanishes. In general, this will not be the case. However, for most cases, $|y_1| \cong |y_2|$ and thus the second term when evaluated will be small. In addition to this, the fourth term is maximized when we set $|y_1| = |y_2|$. For these reasons we let $|y_1| = |y_2|$ in Eq. (3-38) to obtain

$$(P_{AB})_{EXACT} = -k\left[f(0, 0)\Delta y \Delta z + \frac{\Delta y^3 \Delta z}{4} \left.\frac{\partial^2 f}{\partial y^2}\right|_{y_1}^{y_2}\right] + \ldots \qquad (3\text{-}39)$$

The finite difference approximation on the other hand gives from Eq. (3-18)

$$(P_{AB})_{APPROX} = -k|\vec{\nabla} T|_o \Delta y \Delta z . \cos\alpha = -k \left.\frac{\partial T}{\partial x}\right|_{x=y=z=0} \Delta y \Delta z$$

$$= -kf(0, 0)\Delta y \Delta z \qquad (3\text{-}40)$$

Therefore the first order error ΔP_{AB} is given by

$$\Delta P_{AB} = |(P_{AB})_{EXACT} - (P_{AB})_{APPROX}| \cong \frac{k\Delta y^3 z}{4} \left.\frac{\partial^2 f}{\partial y^2}\right|_{y_1}^{y_2} \qquad (3\text{-}41)$$

The exact R_{AB} is given by

$$(R_{AB})_{EXACT} = \frac{(T_{AB})_{APPROX} + \Delta T_{AB}}{(P_{AB})_{APPROX} + \Delta P_{AB}}$$

$$= \frac{(T_{AB})_{APPROX}\left(1 + \frac{\Delta T_{AB}}{(T_{AB})_{APPROX}}\right)}{(P_{AB})_{APPROX}\left(1 + \frac{\Delta P_{AB}}{(P_{AB})_{APPROX}}\right)}$$

$$\cong (R_{AB})_{APPROX}\left[1 + \frac{\Delta T_{AB}}{(T_{AB})} - \frac{\Delta P_{AB}}{(P_{AB})_{APPROX}}\right] \qquad (3\text{-}42)$$

where

$$(R_{AB})_{APPROX} = \frac{(T_{AB})_{APPROX}}{(P_{AB})_{APPROX}} = \frac{\Delta x}{k\Delta y\Delta z}$$

and we used

$$\frac{1}{1+\gamma} \cong 1 - \gamma \qquad \text{for} \qquad \gamma << 1$$

and

$$(1+\varepsilon)(1+\gamma) \cong 1 + \varepsilon + \gamma \qquad \text{for } \varepsilon, \gamma << 1.$$

Substituting Eq. (3-34), (3-41) in (3-42), we obtain

$$(R_{AB})_{EXACT} = (R_{AB})_{APPROX}\left(1 + \frac{1}{24}\left(\Delta x^2 \left.\frac{\partial^3 T}{\partial x^3}\right| - \Delta y^2 \left.\frac{\partial^3 T}{\partial x \partial y^3}\right|\right)/\left(\left.\frac{\partial T}{\partial x}\right|\right)\right) \qquad (3\text{-}43)$$

Thus the percentage error in R_{AB}, denoted as $(R_{AB})_{\%}$ introduced by the finite difference approximation is given by

$$(\Delta R_{AB})_{\%} = \frac{1}{24}\left(\Delta x^2 \left.\frac{\partial^3 T}{\partial x^3}\right| - \Delta y^2 \left.\frac{\partial^3 T}{\partial x \partial y^2}\right|\right)/\left(\left.\frac{\partial T}{\partial x}\right|\right) \qquad (3\text{-}44)$$

Obviously as Δx, $\Delta y \to 0$, $(\Delta R_{AB})_{\%} \to 0$. Thus the $(\Delta R_{AB})_{\%}$ decreases as the square of the mesh size Δx, Δy. The precise evaluation of error is difficult to make since we do not know

$$\left.\frac{\partial^3 T}{\partial x^3}\right|, \left.\frac{\partial^3 T}{\partial x \partial y z}\right|.$$

A percentage error in R_{AB} will directly translate to a percentage error in temperature distribution because power dissipation within elements on the top surface of the chip is to a first order dictated by the electrical nodal voltages and a very weak function of temperature. Thus the power dissipation is known very accurately.

Additional thermal nodes created on the top surface of the chip do not necessarily add to the total number of thermal nodes for actual analysis. In an actual analysis, referring to Fig. 3.11, one can first ignore the thermal resistances R_A from the top surface of the chip to the heat source and solve for the temperature T_A', at node A'. In order to obtain the correct device temperature T_A, one only needs to add the temperature drop across the resistor R_A, that is

$$T_A = T_A' + R_A P_0$$

This scheme works well with the functional iteration. (See the next chapter.) However, it causes some difficulty in convergence in the Newton-Raphson method. In addition to this

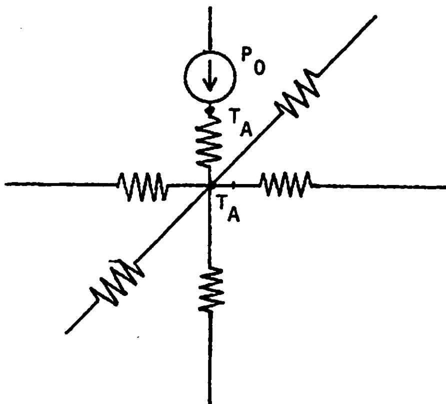


Fig. 3.11

One method to suppress the creation of an extra node when the node is chosen in the middle of the subregion

extra layer of nodes from a view point of economical use of computer time. Thus in the program developed, a node is chosen on the top surface of the chip. With a node chosen on a top surface of the chip, the same procedure can be followed to obtain the same result as given by Eq. (3-44) for the percentage error in temperature distribution. This is due to the assumption of Eq. (3-30).

The error analysis made in this section is essentially 2 1/2 dimensional in a sense that the temperature distribution in z direction is constrained by the assumption of Eq. (3-30). Therefore the dependence of $(\Delta R)_{\%}$ on mesh size as Δx^2, Δy^2 will not be correct if this assumption is violated. In such cases, the dependence of $(\Delta R)_{\%}$ will involve linear relation with Δx, Δy, Δz. Thus for a particular die-package structure in which Eq. (3-30) cannot be assumed, one must create an extra layer of nodes on the top surface of the chip to obtain a more accurate result. For many integrated circuits, Eq. (3-30) is reasonable and the comparison of the two thermal networks did not show any difference in the response of many integrated circuit performances aside from the small fixed amount of dc shift in temperature distribution.

CHAPTER 4

THE MATHEMATICAL FORMULATION AND NUMERICAL METHODS

4-1. Introduction

With the development of a circuit model for the die-package structure, the next task is to combine this with the electrical system and formulate a mathematical description of the coupled system. In this chapter, the technique for equation formulation of the electro-thermal system is presented first and two numerical methods pertinent to the solution of the equations are investigated. Advantages and disadvantages associated with the two methods are also given.

4-2. General formulation of the coupled system

The coupled system must be modeled subject to three basic laws: Kirchoff's voltage law (KVL), Kirchoff's current law (KCL), and the element law (branch characteristic). The first two laws KVL, KCL are linear algebraic constraints on branch voltages (temperatures for the thermal system) and current (heat flow in thermal system) arising from the interconnection of branches and are independent of the branch characteristics. Thus, they imply a topological linear system of equations [20]:

$$\underset{\sim}{A}\underset{\sim}{x} = \underset{\sim}{0} \tag{4-1}$$

where the matrix A contains coefficients that are +1, -1, 0 and $\underset{\sim}{x}$ is the vector consisting of both electrical and thermal variables.

The third constraint that each branch relation be satisfied at each instant of time implies a system of algebraic differential equations of the form,

$$\underset{\sim}{B}(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, t) = [B_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, t), B_2(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, t) \ldots]^{T\gamma} \tag{4-2}$$

where $\dot{\underset{\sim}{x}}$ is the time derivative of $\underset{\sim}{x}$ and $\underset{\sim}{B}$ are in general non-linear functions of $\dot{\underset{\sim}{x}}$, $\underset{\sim}{x}$, t. Combining Eq. (4-1) with Eq. (4-2), we obtain

$$\underset{\sim}{F}(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, t) = \underset{\sim}{0} \tag{4-3}$$

This is the most general form of equations describing the coupled system, and Eq. (4-3) must be solved under dc, transient and ac conditions.

One can formulate the coupled system more specifically so as to attach a more physical interpretation to the equations. The electrical system must have KVL and KCL satisfied independent of the thermal behavior of the coupled system. Thus, we can write

$$\underset{\sim}{A}'x = \underset{\sim}{0} \tag{4-4}$$

where $\underset{\sim}{x}$ is now a vector consisting of electrical branch voltages and currents only. The third constraint gives a system of algebraic differential equations of the form

$$\underset{\sim}{B}'(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \tag{4-5}$$

where T is a vector of thermal variables. If the number of electrical branches is equal to N_E, Eq. (4-4) and Eq. (4-5) each give N_E number of equations. Thus, when Eq. (4-4) and Eq. (4-5) are combined to form

$$\underset{\sim}{F}_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \qquad (4\text{-}6)$$

it will involve $2N_E$ differential equations. $\underset{\sim}{F}_1$ is a non-linear operator on $\dot{\underset{\sim}{x}}$, $\underset{\sim}{x}$, $\dot{\underset{\sim}{T}}$, $\underset{\sim}{T}$, t.

Similarly for the thermal system, we can write to satisfy KVL, KCL

$$\underset{\sim}{A}''\underset{\sim}{T} = \underset{\sim}{0} \qquad (4\text{-}7)$$

and to satisfy the third constraint

$$\underset{\sim}{B}''(\dot{x}, x, \dot{T}, T, t) = \underset{\sim}{0} \qquad (4\text{-}8)$$

If the number of thermal branches is equal to N_T, then, when Eq. (4-7) and Eq. (4-8) are combined we have $2N_T$ differential equations:

$$\underset{\sim}{H}_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \qquad (4\text{-}9)$$

$\underset{\sim}{H}_1$ is a non-linear operator on $\dot{\underset{\sim}{x}}$, $\underset{\sim}{x}$, $\dot{\underset{\sim}{T}}$, $\underset{\sim}{T}$, t.
Thus, we have derived another form of equations describing the coupled system:

$$\underset{\sim}{F}_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \qquad (4\text{-}10a)$$

$$\underset{\sim}{H}_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \qquad (4\text{-}10b)$$

When a particular integration method is employed, Eq. (4-10) reduces to

$$\underset{\sim}{F}(\underset{\sim}{x}, \underset{\sim}{T}) = \underset{\sim}{0} \qquad (4\text{-}11a)$$

$$\underset{\sim}{H}(\underset{\sim}{x}, \underset{\sim}{T}) = \underset{\sim}{0} \qquad (4\text{-}11b)$$

where $\underset{\sim}{F}$ and $\underset{\sim}{H}$ are non-linear operators on $\dot{\underset{\sim}{x}}$, $\underset{\sim}{x}$, $\dot{\underset{\sim}{T}}$, $\underset{\sim}{T}$, t.

We can further simplify Eq. (4-10b) from the actual physical model developed in Chapter 3. There is one thermal capacitor

associated with every node as shown in Fig. 4.1. Thus, if we assume that the thermal capacitors and resistors are linear with temperature and independent of electrical variables, then we can write, for each capacitor current, by inspection,

$$C_{TH}\frac{dT_i}{dt} = P_i(\underset{\sim}{x}, \underset{\sim}{T}) - \sum_k Y_{ik}(T_i - T_k) \qquad (4\text{-}12)$$

where Y_{ik} is the thermal conductance between node i and k,

T_i and T_k are the node temperatures at node i and k, and

P_i is the power generated at node i.

Thus, if the number of non-datum thermal nodes is equal to N_T, then Eq. (4-12) suggests N_T set of differential equations, and they are expressed as

$$\dot{\underset{\sim}{T}} = Y_{TH}\underset{\sim}{T} + \underset{\sim}{P}(\underset{\sim}{x}, \underset{\sim}{T}) \qquad (4\text{-}13)$$

where Y_{TH} is thermal admittance matrix and $\underset{\sim}{P}$ indicates the dependence of power dissipation on $\underset{\sim}{x}$ and $\underset{\sim}{T}$.

Thus, the alternate form of equations that describe the system is

$$\underset{\sim}{F}_1(\dot{\underset{\sim}{x}}, \underset{\sim}{x}, \dot{\underset{\sim}{T}}, \underset{\sim}{T}, t) = \underset{\sim}{0} \qquad (4\text{-}14a)$$

$$\dot{\underset{\sim}{T}} = Y_{TH}\underset{\sim}{T} + \underset{\sim}{P}(\underset{\sim}{x}, \underset{\sim}{T}) \qquad (4\text{-}14b)$$

Although we have elaborated on the formulation of the coupled system in a general manner, in practice, the system equations are never formulated in the form of state variable as in Eq. (4-14). Instead, as we shall see later, the branch relations are replaced by

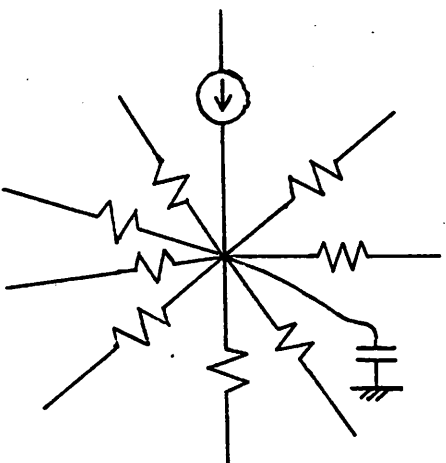


Fig. 4.1

A thermal lumped model associated with a node

an equivalent system of linear equations at each iteration in a dc analysis, and at each iteration of each time point in a transient analysis. When this is done, and the modified nodal analysis method of equation formulation is employed, the general expression for the coupled system reduces to a linear system of equations

$$A\underset{\sim}{x} = \underset{\sim}{j} \qquad (4\text{-}15)$$

where $\underset{\sim}{x}$ is the vector of unknown variable and $\underset{\sim}{j}$ is the excitation vector of the system. The dimension of the matrix A is related to the total number of electrical nodes, thermal nodes, inductors, independent voltage sources, temperature sources and temperature controlled voltage sources. (A typical example of temperature controlled voltage sources is a zener diode.)

In the next two sections, two methods relevant to the solution of Eq. (4-14) are presented.

4-3. Newton-Raphson's method

4-3-1. General description

The first method proposed is the Newton-Raphson method applied to the entire coupled system.

Any electrical branch relations can be written as

$$f(x, T) = 0 \qquad (4\text{-}16)$$

where we assumed that the branch relations depend on branch voltage and its temperature and do not directly depend upon the actual heat flow.

The straightforward application of the Newton-Raphson algorithm

to individual branches results in an iteration scheme as follows:

$$x^{n+1} = x^n + \left.\frac{\partial f}{\partial x}\right|_n (x^{n+1} - x^n) + \left.\frac{\partial f}{\partial T}\right|_n (T^{n+1} - T^n) \qquad (4\text{-}17)$$

where n corresponds to iteration count and $\left.\frac{\partial f}{\partial x}\right|_n$, $\left.\frac{\partial f}{\partial T}\right|_n$ are the partial derivatives of f with respect to x and T, evaluated at the nth iterations. The resulting admittance matrix will take a form as shown in Fig. 4.2, where the elements in the submatrix $\frac{\partial I}{\partial T}$ are temperature controlled current sources corresponding to the effects of temperature on the electrical performance of the circuit and the elements in $\frac{\partial P}{\partial v}$ are electrically controlled power sources which indicate the dependence of power dissipation in the circuit on the electrical node voltages.

Once the linearization process is completed, and the update logic employed to limit power, temperature, voltage, and current excursions from one iteration to the next, the Newton-Raphson method proceeds in a straightforward manner. This iteration scheme is illustrated in Fig. 4.2. One of the programs developed employs the Newton-Raphson method, and this program is called T-SPICE2B.

4-3-2. Branch relations in the electro-thermal system

Unlike an electrical system, the coupled system requires a few additional types of branch elements. Basically, the following three different branch relations are encountered in typical electro-thermal systems.

(1) Current defined elements which depend on both its terminal voltage, V, and temperature, T.

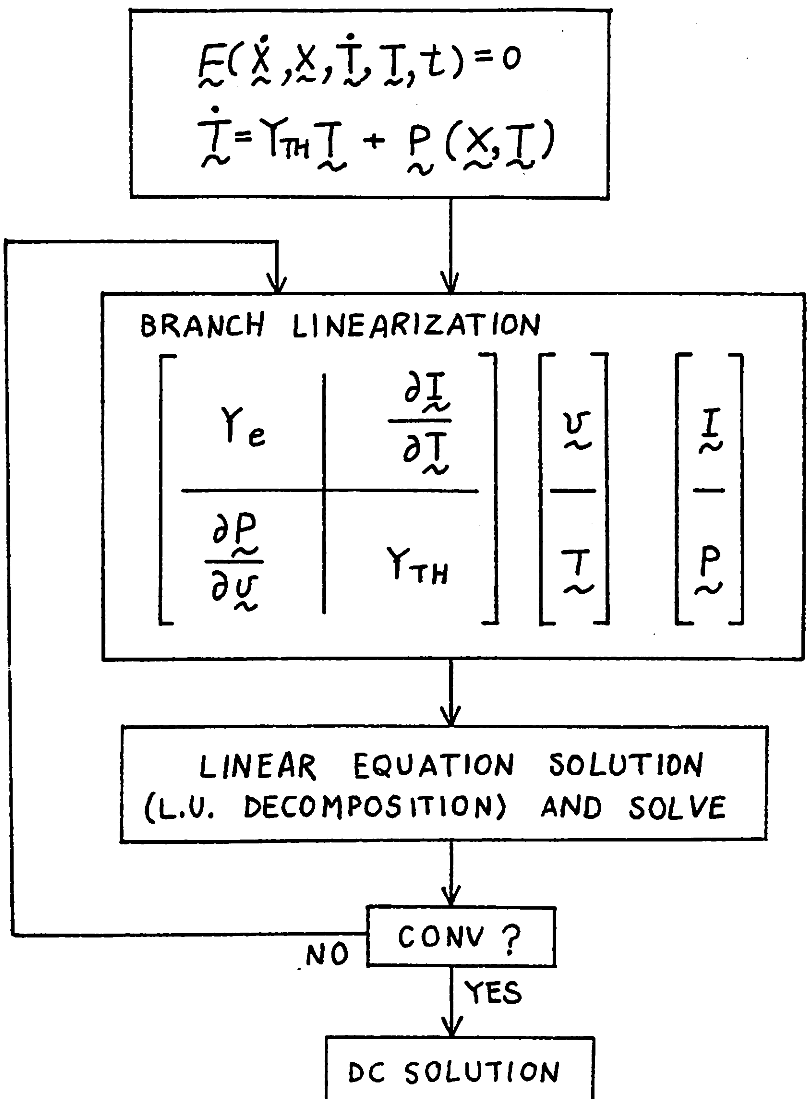


Fig. 4.2

Flow graph for the Newton-Raphson's method

$$I = f(V, T) \qquad (4\text{-}18)$$

For this element, the branch linearization employing Newton-Raphson method gives the following iteration scheme:

$$I^{n+1} = I^n + \frac{\partial f}{\partial V}\bigg|_n (x^{n+1} - x^n) + \frac{\partial f}{\partial T}\bigg|_n (T^{n+1} - T^n)$$

$$= I_o + \frac{\partial f}{\partial V}\bigg|_n V^{n+1} + \frac{\partial f}{\partial T}\bigg|_n T^{n+1} \qquad (4\text{-}19)$$

where

$$I_o = I^n - \frac{\partial f}{\partial V}\bigg|_n x^n - \frac{\partial f}{\partial T}\bigg|_n T^n$$

and n corresponds to iteration count.

The equivalent circuit model for this element is shown in Fig. 4.3. In Fig. 4.3, I_o is a constant current source, $\frac{\partial f}{\partial T}\big|_n T^{n+1}$ is a temperature dependent current source, G is an equivalent conductance of the element.

A good example of this type of element is a diode whose voltage, current and temperature relationship is given by

$$I_d = I_o T^3 e^{-Eg/kT}(e^{qV_D/kT} - 1)$$

where I_o is a constant, Eg is energy gap of the silicon, and k is a Boltzmann's constant.

(2) Voltage defined element which depends upon both its branch current, I, and temperature, T.

$$V = f(I, T) \qquad (4\text{-}20)$$

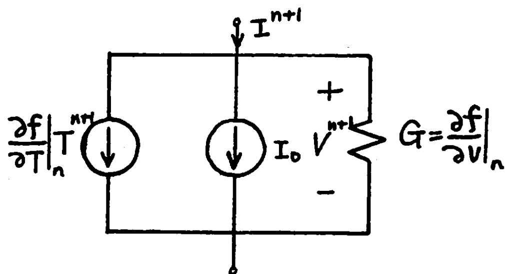


Fig. 4.3

Equivalent circuit model for a current defined element

A similar procedure to (1) gives the following relation and its element model as shown in Fig. 4.4.

$$V^{n+1} = V_o + \left.\frac{\partial f}{\partial I}\right|_n I^{n+1} + \left.\frac{\partial f}{\partial T}\right|_n T^{n+1} \qquad (4\text{-}21)$$

where

$$V_o = V^n - \left.\frac{\partial f}{\partial I}\right|_n I^n - \left.\frac{\partial f}{\partial T}\right|_n T^n$$

In Fig. 4.4, V_o is a constant voltage source, $\left.\frac{\partial f}{\partial T}\right|_n T^{n+1}$ is a temperature dependent voltage source, R is an equivalent resistance of the element.

A good example of this type of element is a zener diode whose voltage V_z and temperature, T, is given by

$$V_z(T) = V_{z_o} + TC*(T - T_o) + I_z \cdot R_z$$

where V_{z_o} is a voltage drop across the zener at a nominal temperature T_o, TC is the temperature coefficient, I_z is the current through the zener, and R_z is its series resistance.

(3) Thermal-current defined element which depends upon its branch voltage, V, and temperature, T.

In this particular element, we can write:

$$P = f(V, T) \qquad (4\text{-}22)$$

There are two different kinds of thermal-current defined elements. One is the heat source where T is the temperature of the element generating heat. The other is the thermal resistor, where T is the temperature difference between two thermal nodes. The heat

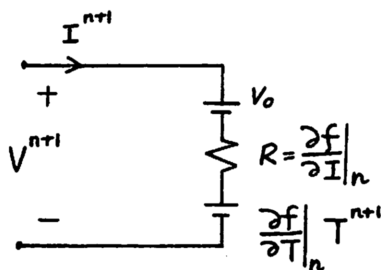


Fig. 4.4

Circuit model for a voltage defined element

flow through it is defined by the temperature difference across the thermal resistor.

For the first kind, we have

$$P^{n+1} = P_o + \frac{\partial f}{\partial V}\Big|_n V^{n+1} + \frac{\partial f}{\partial T}\Big|_n T^{n+1} \qquad (4\text{-}23)$$

where

$$P_o = P^n - \frac{\partial f}{\partial V}\Big|_n V^n - \frac{\partial f}{\partial T}\Big|_n T^n$$

The element model is shown in Fig. 4.5. In Fig. 4.5, I_o is a constant heat source, $-\frac{\partial f}{\partial T}\Big|_n$ is an equivalent thermal resistance shunting the thermal node to the ground. $\frac{\partial f}{\partial V}\Big|_n T^{n+1}$ is a voltage dependent heat source and it indicates the effect of electrical nodal voltage on power dissipation. A good example of this kind of element is power dissipated in a diode whose relationship is given below:

$$P = I_d V_d = I_o T^3 e^{-Eg/kT}(e^{qV_d/kT} - 1)V_d$$

For the second kind, we have

$$P = f(T) \qquad (4\text{-}24)$$

We can write

$$P^{n+1} = P^n + \frac{\partial f}{\partial T}\Big|_n (T^{n+1} - T^n) = P_o + \frac{\partial f}{\partial T}\Big|_n T^{n+1} \qquad (4\text{-}25)$$

where

$$P_o = P^n - \frac{\partial f}{\partial T}\Big|_n T^n$$

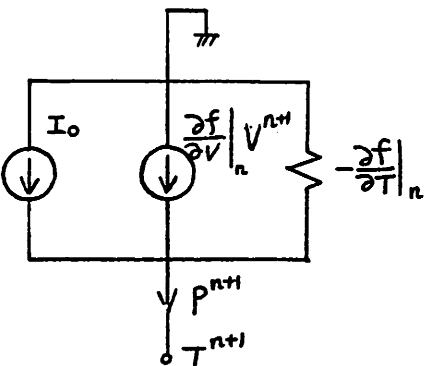


Fig. 4.5

Circuit model for a current defined element that depends on voltage and temperature

The element model is shown in Fig. 4.6.

If in particular, the heat flow through the resistor is linear with temperature difference, then Eq. (4-25) reduces to

$$P^{n+1} = GT^{n+1}$$

where G is a constant linear thermal conductance. The element model also reduces to that shown in Fig. 4.7.

4-3-3. Update logic

The straightforward application of the Newton-Raphson algorithm results in numerical convergence problems in typical electronic circuit when the iterate solution is not sufficiently close to a correct solution. These problems occur due to numerical overflow and/or numerical oscillations. In the past, basically three different algorithms have been employed to eliminate these problems [1]. In the case of electrothermal simulation, the problems are more complicated because a scheme must be developed so as to properly limit not only voltages and currents but also temperatures and heat flow. In the program T-SPICE2B, a modified version of simple limiting process with alternating bases has been employed as follows:

First, for a given T_n and an iterate solution $\hat{T}_{n+1}$, the new temperatures T^{n+1} are updated according to a simple criterion in which their temperature excursion is limited to $\pm\Delta T$ which can be user-specified or defaulted at 1°C. The flow chart for this temperature limiting algorithm is shown in Fig. 4.8.

Secondly, non-linear elements must be treated properly. For a bipolar transistor, for example, the question is the following:

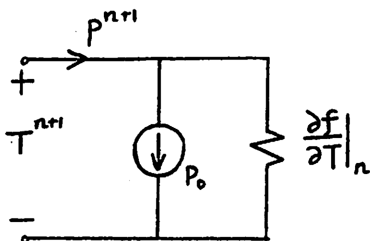


Fig. 4.6

Circuit model for a non-linear thermal resistor

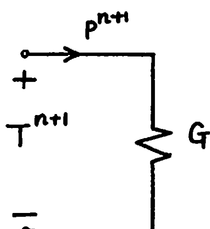


Fig. 4.7

Circuit model for a linear thermal resistor

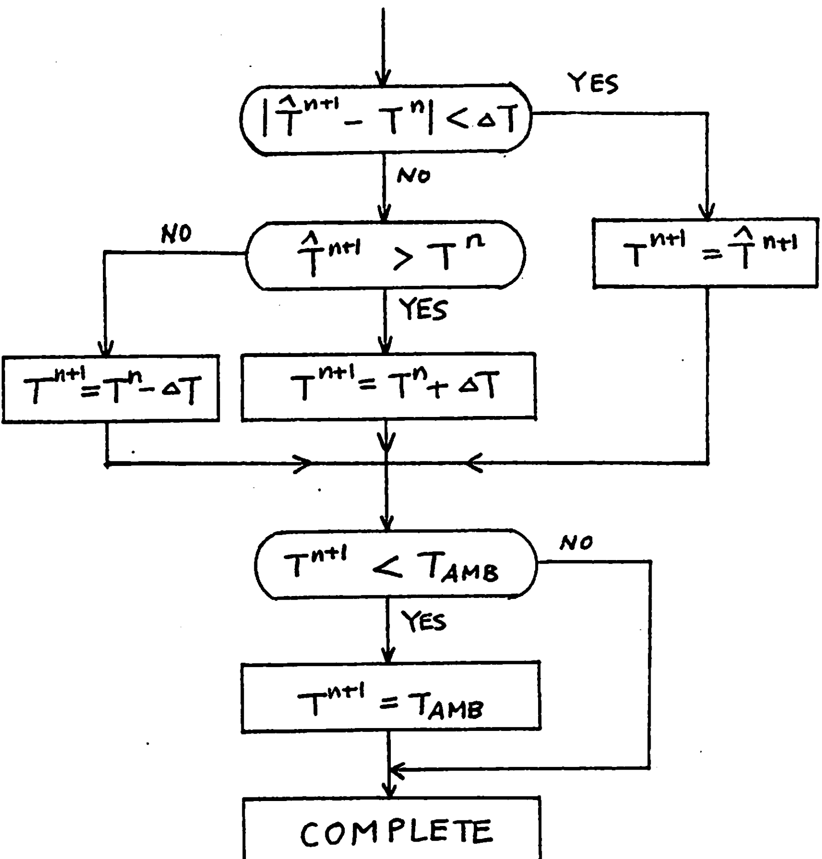


Fig. 4.8

Flow chart for the temperature limiting algorithm

Given (V_{BE}^{n}, I_{CBE}^{n}, V_{BC}^{n}, I_{CBC}^{n}, P^{n}) and iterate solution ($\hat{V}_{BE}^{n+1}$, $\hat{I}_{CBE}^{n+1}$, $\hat{V}_{BC}^{n+1}$, $\hat{I}_{CBC}^{n+1}$, $\hat{P}^{n+1}$), how shall we best choose (V_{BE}^{n+1}, V_{BC}^{n+1}, I_{CBE}^{n+1}, I_{CBC}^{n+1}, P^{n+1}) so that the next iterate solution be as nearly close to the correct solution as possible? I_{CBE} and I_{CBC} are that portion of the collector current due to base to emitter, V_{BE}, base to collector V_{BC} junction voltages respectively. P is the power dissipation of the device and n is an iterate count. First, two junction voltages, V_{BE}, V_{BC} are updated individually according to the rule as indicated in the flow chart of Fig. 4.9. Basically in this scheme, the junction voltage excursions of forward (reversed) biased junction from one iteration to the next is limited to an empirical factor of $2V_T(V_{RLIM})$. V_T is the thermal voltage at temperature T, and given by kT/q. V_{RLIM} is a user-specifiable constant.

One significant difference in this update logic is the introduction of V_{RLIM} (defaulted at one volt) which is used to limit the excursion in the reverse biased junction voltage. This becomes necessary due to the fact that a large excursion in reverse biased junction voltage, for example, could result in a large increase in power dissipation of a bipolar transistor. For an electrical circuit alone, it was not necessary because the reverse biased junction voltage, however large, did not change the currents within the circuit very much.

After V_{BE}^{n+1} and V_{BC}^{n+1} have been chosen according to the flow chart of Fig. 4.10, a new power dissipation is computed as

$$P^{n+1} = V_{BE}^{n+1} \cdot I_B^{n+1} + V_{CE}^{n+1} \cdot I_C^{n+1}$$

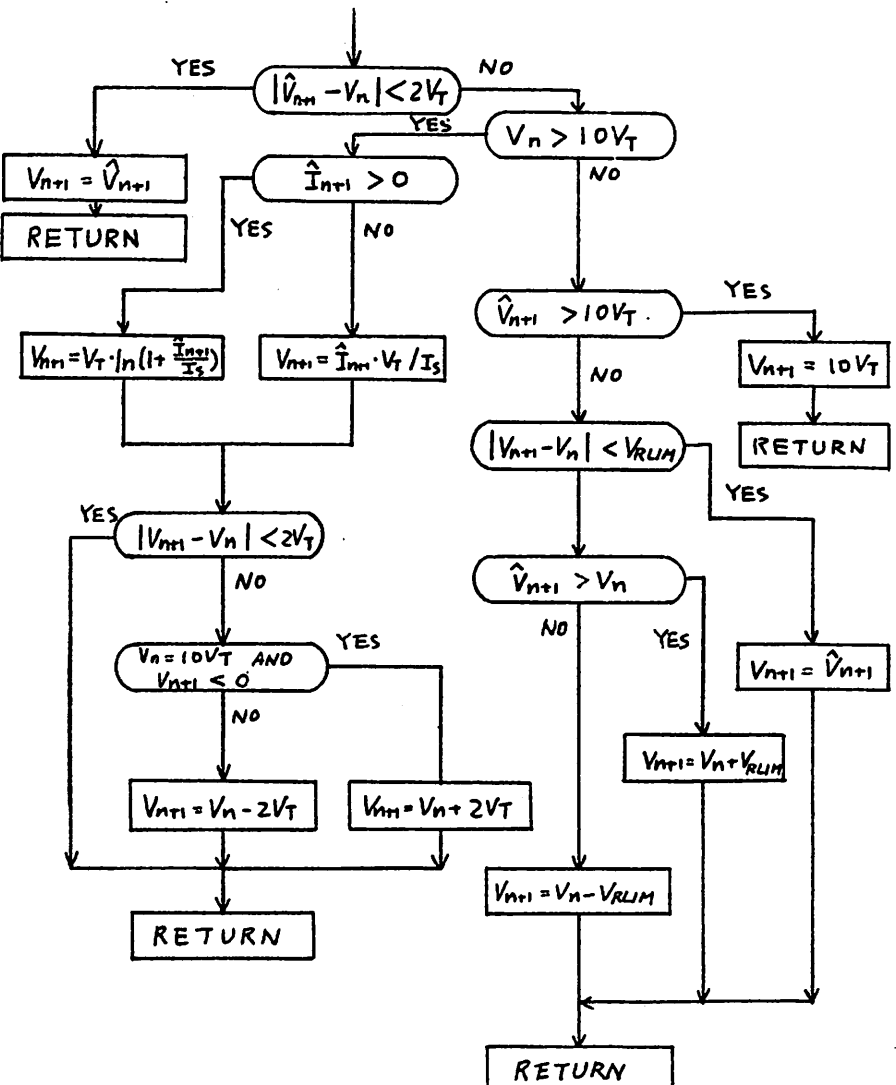


Fig. 4.9

Flow chart of junction voltage limiting algorithm

The new power dissipation is limited to less than four times the power dissipation at the previous iteration and V_{BE}, V_{BC} are recomputed according to the following rule shown in Fig. 4.10.

The convergence in the Newton-Raphson iterations can be greatly facilitated when the electrical circuit is individually solved, and the resulting nodal voltages are used as an initial guess of all the junction voltages for all non-linear elements at the onset of the iteration process of the electro-thermal system. This junction initializing scheme results in a large saving in the cost of simulation as will be presented in Chapter 5.

The same convergence criterion as in SPICE2 [1] was used to determine if the iterative sequence of solutions has converged, and is rewritten here for completeness.

For all the current defined branches

$$|\hat{I}_{n+1} - I_n| < \varepsilon a + \varepsilon r.\mathrm{Min}\{|I_{n+1}| \cdot |I_n|\}$$

and for all the voltage defined branches

$$|V_{n+1} - V_n| < \varepsilon a + \varepsilon r.\mathrm{Min}\{|\hat{V}_{n+1}|, |V_n|\}$$

with $\varepsilon a = 10^{-12}$ and $\varepsilon r = 0.1\%$, and $\mathrm{Min}[x_1, x_2] \equiv$ the smaller of x_1 and x_2.

No separate criterion was found necessary to insure the convergence of temperatures.

4-3-4. Transient analysis

One important consideration in the transient analysis of electrothermal circuit is the large spread between electrical time constants

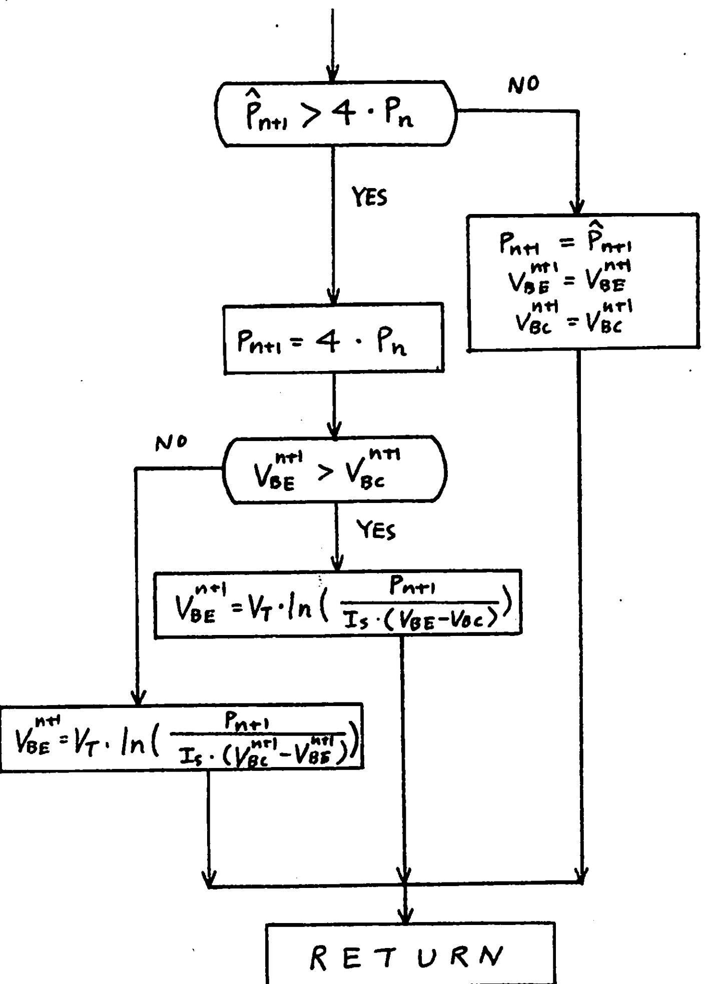


Fig. 4.10

Flow chart of junction voltage limiting algorithm to limit power dissipation

(microseconds) and thermal time constants (milliseconds). In order to cope with this problem, a stiffly stable Trapezoidal Integration technique with automatic timestep control has been chosen for transient analysis. The implicit second-order Trapezoidal algorithm uses the following rule to compute x_{n+1} from x_n.

$$x_{n+1} = x_n + \frac{h_n}{2}(\dot{x}_{n+1} + \dot{x}_n) \tag{4-27}$$

where n corresponds to time point and h_n the time step from n to n + 1.

The truncation error associated with this integration technique is given by

$$-\frac{h^3}{12}\frac{d^3x}{dt^3}\bigg|_\xi \tag{4-28}$$

where ξ is somewhere between t_n and t_{n+1}.

In SPICE2, in order to avoid the numerical oscillation problem often encountered in the Trapezoidal Integration method, the time step was adjusted such that local truncation error is maintained within a certain amount. This is done as follows [1]:

$$h_{n+1} = \sqrt[3]{\frac{\varepsilon r\,|x_{n+1}| + \varepsilon a}{DD_3(t_{n+1})}} \tag{4-29}$$

where $\varepsilon r = 10^{-3}$ relative error tolerance

$\varepsilon a = 10^{-2}$ absolute tolerance

$$DD_3(t_{n+1}) = \frac{DD_2(t_{n+1}) - DD_2(t_n)}{(h_n + h_{n-1} + h_{n-2})}$$

$$DD_2(t_{n+1})_r = \frac{\frac{X_{n+1} - X_n}{h_n} - \frac{X_n - X_{n-1}}{h_{n-1}}}{h_n \, h_{n-1}}$$

The identical method was carried on to T-SPICE.

If the energy storage element has a temperature dependence, branch linearization employing the Newton-Raphson method would take a form slightly different from those involving electrical dependence only. If, for example, charge q on a capacitor plate is a function of its terminal voltage as well as its temperature, we can write

$$q = f(V, T) \tag{4-30}$$

The Trapezoidal Integration algorithm gives

$$q_{n+1} = q_n + \frac{h_n}{2}(\dot{q}_n + \dot{q}_{n+1}) \tag{4-31}$$

$$= q_n + \frac{h}{2}(i_n + i_{n+1}) \tag{4-32}$$

Solving Eq. (4-32) for i_{n+1}, we get

$$i_{n+1} = 2\,\frac{q_{n+1} - q_n}{h} - i_n = \frac{2}{h}\,q_{n+1} - \left(\frac{2q_n}{h} + i_n\right) \tag{4-33}$$

The last term in the parenthesis above is known from the previous time point solution and is constant. Since q is a function of V and T, Eq. (4-33) is in general a non-linear equation involving V_{n+1}, T_{n+1}. If we Taylor expand Eq. (4-33) we obtain

$$i^{m+1}_{n+1} = \frac{2}{h}\left\{q^m_{n+1} + \left.\frac{\partial q}{\partial V}\right|_{m \atop n+1}(V^{m+1}_{n+1} - V^m_{n+1}) + \left.\frac{\partial q}{\partial T}\right|_{m \atop n+1}(T^{m+1}_{n+1} - T^m_{n+1}) + \ldots\right\} - \left(\frac{2q_n}{h} + i_n\right)$$

$$= \frac{2}{h}\left(q^m_{n+1} - \left.\frac{\partial q}{\partial V}\right|_{m \atop n+1} V^m_{n+1} - \left.\frac{\partial q}{\partial T}\right|_{m \atop n+1} T^m_{n+1} - q_n\right) - i_n$$

$$+ \frac{2}{h}\left.\frac{\partial q}{\partial V}\right|_{m \atop n+1} V^{m+1}_{n+1} + \frac{2}{h}\left.\frac{\partial q}{\partial T}\right|_{m \atop n+1} T^{m+1}_{n+1} \tag{4-34}$$

$$= I_o + \frac{2}{h}\left.\frac{\partial q}{\partial V}\right|_{m \atop n+1} V^{m+1}_{n+1} + \frac{2}{h}\left.\frac{\partial q}{\partial T}\right|_{m \atop n+1} T^{m+1}_{n+1} \tag{4-35}$$

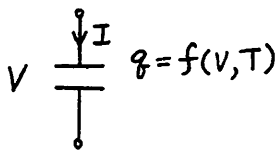
where m corresponds to Newton-Raphson iteration count, and

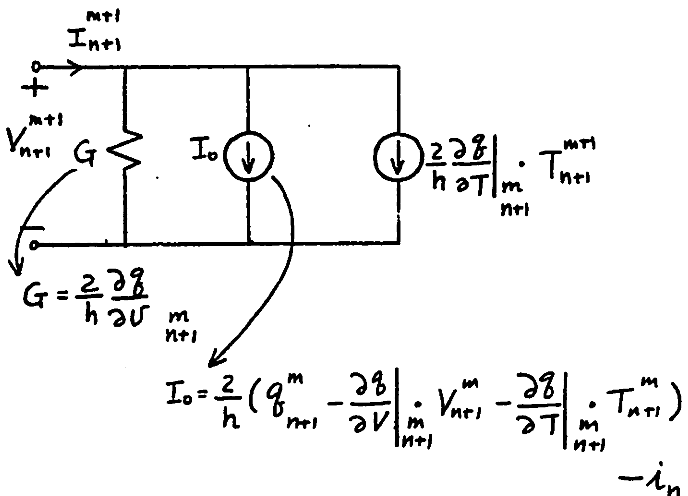
$$I_o = \frac{2}{h}\left(q^m_{n+1} - \left.\frac{\partial q}{\partial V}\right|_{m \atop n+1} V^m_{n+1} - \left.\frac{\partial q}{\partial T}\right|_{m \atop n+1} T^m_{n+1} - q_n\right) - i_n$$

The companion model for Eq. (4-35) is shown in Fig. 4.11.

Obviously for thermal capacitors, i corresponds to the heat flow P and q corresponds to thermal energy. Clearly the transient analysis has been reduced to dc analysis by means of Trapezoidal Integration method.

The circuit model for a simple circuit shown in Fig. 4.12(a), containing non-linear element (diode), non-linear electrical capacitor that depends on terminal voltage and temperature, non-linear thermal resistor and a linear thermal capacitor is shown in Fig. 4.12(b).



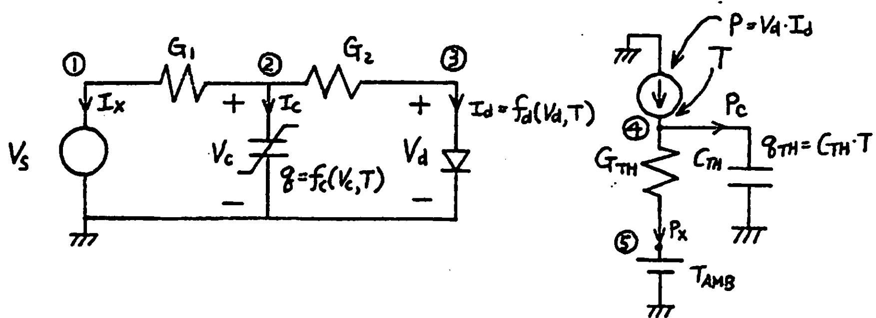


$$G = \frac{2}{h}\frac{\partial q}{\partial V}\Big|^{m}_{n+1}$$

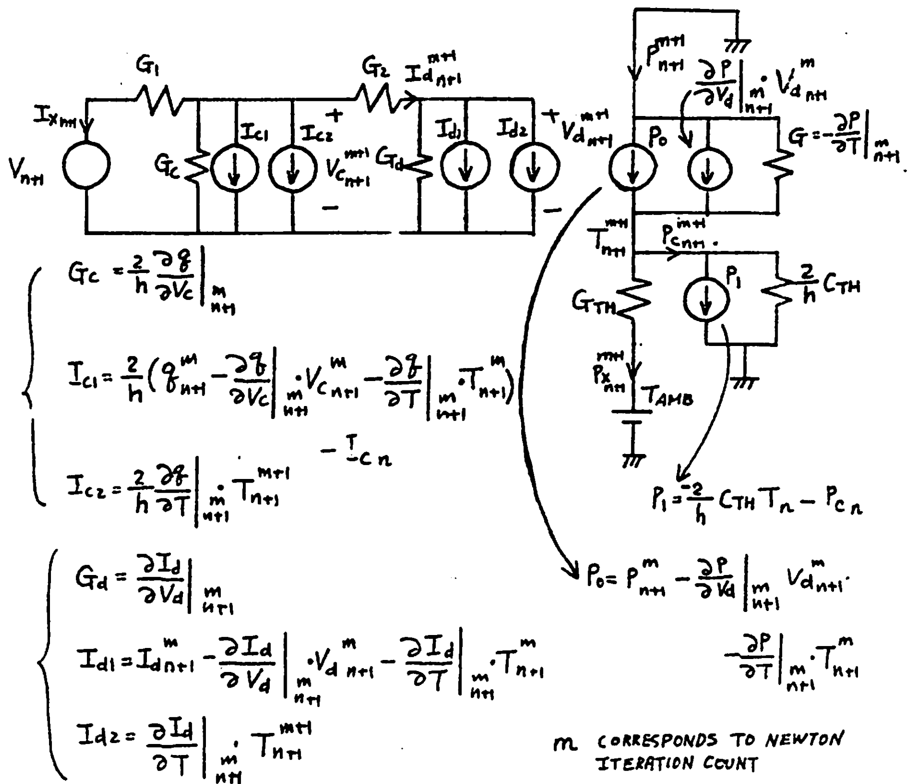
$$I_o = \frac{2}{h}\left(q^{m}_{n+1} - \frac{\partial q}{\partial V}\Big|^{m}_{n+1} \cdot V^{m}_{n+1} - \frac{\partial q}{\partial T}\Big|^{m}_{n+1} \cdot T^{m}_{n+1}\right) - i_n$$

Fig. 4.11

Circuit model for a capacitor



(a)



$$G_c = \frac{2}{h}\frac{\partial q}{\partial V_c}\Big|^{m}_{n+1}$$

$$I_{c1} = \frac{2}{h}\left(q^{m}_{n+1} - \frac{\partial q}{\partial V_c}\Big|^{m}_{n+1} \cdot V^{m}_{c_{n+1}} - \frac{\partial q}{\partial T}\Big|^{m}_{n+1} \cdot T^{m}_{n+1}\right) - I_{c_n}$$

$$I_{c2} = \frac{2}{h}\frac{\partial q}{\partial T}\Big|^{m}_{n+1} \cdot T^{m+1}_{n+1}$$

$$G_d = \frac{\partial I_d}{\partial V_d}\Big|^{m}_{n+1}$$

$$I_{d1} = I^{m}_{d_{n+1}} - \frac{\partial I_d}{\partial V_d}\Big|^{m}_{n+1} \cdot V^{m}_{d_{n+1}} - \frac{\partial I_d}{\partial T}\Big|^{m}_{n+1} \cdot T^{m}_{n+1}$$

$$I_{d2} = \frac{\partial I_d}{\partial T}\Big|^{m}_{n+1} \cdot T^{m+1}_{n+1}$$

$$P_1 = \frac{2}{h} C_{TH} T_n - P_{c_n}$$

$$P_o = P^{m}_{n+1} - \frac{\partial P}{\partial V_d}\Big|^{m}_{n+1} V^{m}_{d_{n+1}} - \frac{\partial P}{\partial T}\Big|^{m}_{n+1} \cdot T^{m}_{n+1}$$

m CORRESPONDS TO NEWTON ITERATION COUNT

n CORRESPONDS TO TIME POINT

(b)

$$
\begin{pmatrix}
G_1 & -G_1 & & & & +1 & \\
-G_1 & G_1+G_c+G_2 & -G_2 & \frac{2}{h}\frac{\partial q}{\partial T}\Big|_{n+1}^{m} & & & \\
 & -G_2 & G_2+G_d & \frac{\partial I_d}{\partial T}\Big|_{n+1}^{m} & & & \\
 & & -\frac{\partial P}{\partial V_d}\Big|_{n+1}^{m} & G_{TH}-\frac{\partial P}{\partial T}\Big|_{n+1}^{m} & -G_{TH} & & \\
 & & & -G_{TH} & G_{TH}+\frac{2}{h}C_{TH} & & +1 \\
+1 & & & & & & \\
 & & & & +1 & &
\end{pmatrix}
\cdot
\begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ T_4 \\ T_5 \\ I_x \\ P_x \end{pmatrix}
=
\begin{pmatrix} 0 \\ -I_{c1} \\ -I_{d1} \\ -P_1 \\ P_1 \\ V_S \\ T_{AMB} \end{pmatrix}
$$

(c)

Fig. 4.12

(a) a simple example circuit

(b) equivalent circuit

(c) the resulting admittance matrix

Shown in Fig. 4.12(c) is the electro-thermal admittance matrix for this circuit.

4-3-5. <u>Computational effort involved in the Newton-Raphson algorithm</u>

The use of Newton-Raphson algorithm appears attractive in that it would always converge as long as one can start sufficiently close to the correct solution. With the adoption of proper update logic as described in 4-3-3, indeed the algorithm does show very good convergence properties. However, the computational effort involved in this method is quite large.

Nagel [1] reported that for typical integrated circuits,

(1) 10 ∿ 20% of the computational cost of analysis portion of simulation, using Markowitz sparse matrix technique is expended for the LU decomposition of the matrix and the rest for the loading (that is, the evaluation of matrix coefficients).

(2) The cost of analysis portion of simulation increases $N^{1.24}$ (Eq. 4-36), where N is the dimension of the matrix.

Assume that for a given circuit the number of electrical nodes is N_E and that three times as many thermal nodes as electrical nodes are generated for each layer of thermal network. If we assume that the proportion of computational cost for LU decomposition and loading is maintained in the solution process of the electro-thermal admittance matrix, then the cost of simulation for electro-thermal system will be, using this empirical formula,

$$\frac{(7N_E)^{1.24}}{(N_E)^{1.24}} = 7^{1.24} \cong 10 \text{ times as expensive as the electrical}$$

circuit alone. The assumption above may not be exactly correct because

the computational effort spent for the loading of the electro-thermal matrix may not increase in proportion to the dimension of the matrix. In reality, the cost increases at least as much as the simple calculation above suggests. There are two basic reasons for this. First, for typical integrated circuits, the number of off-diagonal entries is 2 ~ 3 [21] and Eq. (4-36) applies only in such cases. The sparsity of the electro-thermal network however is much worse. Consider for example an electro-thermal network matrix as shown below:

$$\begin{bmatrix} Y_E & \frac{\partial \underset{\sim}{I}}{\partial \underset{\sim}{T}} \\ \frac{\partial \underset{\sim}{P}}{\partial \underset{\sim}{V}} & Y_{TH} \end{bmatrix} \begin{bmatrix} \underset{\sim}{V} \\ \underset{\sim}{T} \end{bmatrix} = \begin{bmatrix} \underset{\sim}{I} \\ \underset{\sim}{P} \end{bmatrix} \qquad (4\text{-}37)$$

The number of off-diagonal entries in submatrix Y_E (electrical admittance submatrix) is typically equal to 2 ~ 3. However, the number of off-diagonal entries in submatrix Y_{TH} (thermal admittance submatrix) is at least six, and typically eight because every thermal node is connected to its adjacent nodes in horizontal plane as well as in vertical direction. Furthermore, the sparsity of the submatrices $\frac{\partial \underset{\sim}{I}}{\partial \underset{\sim}{T}}$ and $\frac{\partial \underset{\sim}{P}}{\partial \underset{\sim}{V}}$ is very low. Consider for example a bipolar transistor. On a row in the submatrix $\frac{\partial \underset{\sim}{P}}{\partial \underset{\sim}{V}}$, corresponding to the temperature of the bipolar transistor, there will be at least three off-diagonal entries. Similarly the corresponding column in $\frac{\partial \underset{\sim}{I}}{\partial \underset{\sim}{T}}$ will have three off-diagonal entries. Resistors will make two off-diagonal entries in $\frac{\partial \underset{\sim}{I}}{\partial \underset{\sim}{T}}$ and $\frac{\partial \underset{\sim}{P}}{\partial \underset{\sim}{V}}$ submatrices. Thus, the large sparsity typically characterized by 2 ~ 3 off-diagonal entries in electricl system matrix cannot be maintained in the electro-thermal matrix. Thus the portions of time spent for LU decomposition can become as much as 50%.

Second, the computational effort expended in the evaluation of the coupling submatrices $\frac{\partial \underset{\sim}{I}}{\partial \underset{\sim}{T}}$ and $\frac{\partial \underset{\sim}{P}}{\partial \underset{\sim}{V}}$ can be quite large. This is particularly true of circuit involving exponential non-linearities.

When the above considerations have been included it is easy to see that the cost of simulation can be <u>at least</u> ten times greater than when electrical effects only are considered. In some way, however, it is not fair to say that electro-thermal simulation costs at least ten times as much as electrical simulation alone. For example, in a temperature stabilized substrate integrated circuit system, a simulation of electrical effect alone does not have any physical meaning. In this class of circuit the simulation cannot be done without considering thermal effect.

Before the close of this section, one advantage should be mentioned of the Newton-Raphson method in addition to its convergence property. That is, the Newton-Raphson method can be easily adopted to a non-linear thermal network. It is an easy matter to re-evaluate thermal resistance after every iteration. The same can be said about the energy storage element that depends not only on electrical variable but also its temperature.

4-4. Modified functional iteration

4-4-1. Introduction

The high cost of computation typical of the Newton-Raphson method can be reduced by a method which may be termed a "modified functional iteration method." It proceeds in the following manner. Rewriting Eq. (4-11)

$$\underset{\sim}{F}(\underset{\sim}{x}, \underset{\sim}{T}) = 0 \qquad (4\text{-}37a)$$

$$\underset{\sim}{H}(\underset{\sim}{x}, \underset{\sim}{T}) = 0 \qquad (4\text{-}37b)$$

first a set of initial temperature guesses $\underset{\sim}{T}^{o}$ are made. For a given $\underset{\sim}{T}^{o}$, Eq. (4-37a) is solved for $\underset{\sim}{x}^{o}$, using the Newton-Raphson method. With $\underset{\sim}{x}^{o}$, Eq. (4-37b) is solved for $\underset{\sim}{T}^{1}$. This process is repeated until $\underset{\sim}{x}$, $\underset{\sim}{T}$ converges. The process of solution for one-dimensional case is shown graphically in Fig. 4.13. Shown in Fig. 4.14 is a flow graph describing the process of the modified functional iteration. This method is used in one of the programs developed and called T-SPICE2A.

In this section, the advantages, disadvantages and the convergence property of this method are presented.

4-4-2. Computational advantages and disadvantages of the modified functional iteration method

The computational advantages of this method are many-fold. Consider the linearized system of equations for both electrical and thermal systems as shown below.

$$[Y_E][\underset{\sim}{V}] = [\underset{\sim}{I}] \qquad (4\text{-}38a)$$

$$[Y_{TH}][\underset{\sim}{T}] = [\underset{\sim}{P}(\underset{\sim}{V}, \underset{\sim}{T})] \qquad (4\text{-}38b)$$

Eq. (4-38a) and Eq. (4-38b) correspond to Eq. (4-37a) and Eq. (4-37b) respectively. In terms of these equations, the modified functional iteration proceeds as follows: With an initial temperature guess $\underset{\sim}{T}^{o}$, the branch linearized admittance matrix Y_E is formed. Then Eq. (4-38a) is solved for $\underset{\sim}{V}^{o}$. With $\underset{\sim}{V}^{o}$ and $\underset{\sim}{T}^{o}$, $\underset{\sim}{P}(\underset{\sim}{V}^{o}, \underset{\sim}{T}^{o})$ is calculated and inserted to the right-hand side of Eq. (4-38b). Strictly speaking, Eq. (4-38b) must be solved iteratively because it is a non-linear equation.

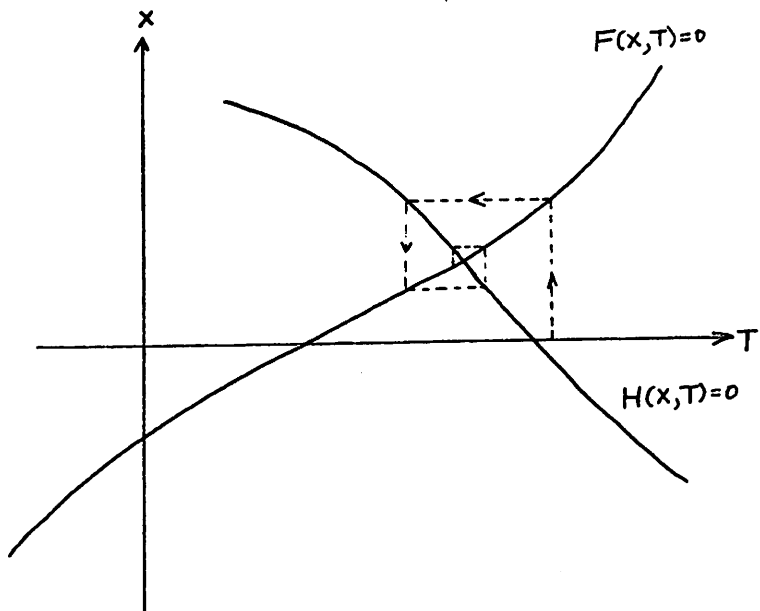


Fig. 4.13

Illustration of iterative solution

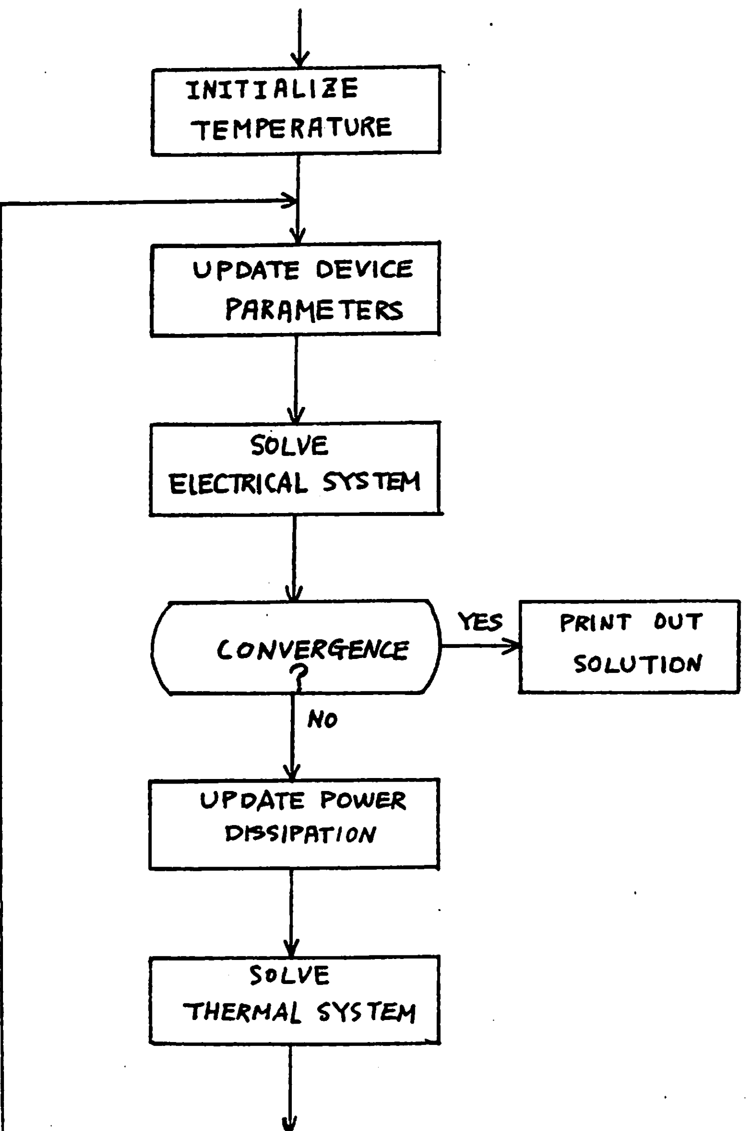


Fig. 4.14

Flow chart for a modified functional method

However, in order to avoid this expensive iterative process, $P(\underset{\sim}{V}^o, \underset{\sim}{T}^o)$ is used as an approximation. (To solve Eq. 4-38b exactly, one may do a straight functional iteration to obtain $\underset{\sim}{T}_1$.) Eq. (4-38b) is then solved for $\underset{\sim}{T}^1$. With $\underset{\sim}{T}^1$, Y_E is recalculated and this process is repeated until convergence. Thus the first major advantage of this method is obvious: In the solution of Eq. (4-38b), only one LU decomposition is necessary for dc analysis. Even for transient analysis, only one LU decomposition is necessary at each time point provided the thermal energy storage element is linear with T. Therefore the computational cost associated with the LU decomposition of the thermal admittance matrix is negligibly small. Since only one LU decomposition is necessary for dc analysis, and one LU decomposition at each time point in transient analysis, the cost of simulation is very insensitive to the size of the thermal system. Compared to the case of Newton-Raphson method in which LU decomposition time is as much as 50% of the total computation time, the saving in computation effort is tremendous. The actual simulation results show that the cost of this method is one-half of the Newton-Raphson method. Furthermore, one does not have to evaluate derivatives associated with submatrices inherent in the Newton-Raphson method. Another minor advantage is that no limiting process is necessary.

There exist however several disadvantages to this method. The most serious one is its convergence property. In the next section, the convergence property of the modified functional iteration method will be carefully investigated. The other disadvantages are: (1) if the thermal model is not linear, the LU decomposition must be carried out at every iteration and the saving associated with this process as

mentioned earlier will be lost. (2) For this method to be readily adaptable to the existing programs such as SPICE 2, the memory allocation scheme must be carefully executed. These problems are however minor and the only significant disadvantage of this method is presented next.

4-4-3. Convergence of the modified functional iteration method

The most serious disadvantage of the method is that it fails to converge for a certain class of circuits. The problem associated with this non-convergence is now shown below:

First we can rewrite Eq. (4-37a) as

$$\underset{\sim}{x} = \underset{\sim}{f}(\underset{\sim}{T}) = [f_1(\underset{\sim}{T}),\ f_2(\underset{\sim}{T})\ .\ .\ .\ f_N(\underset{\sim}{T})]^{T\gamma} \qquad (4\text{-}39a)$$

where $\underset{\sim}{f}$ is a non-linear function of $\underset{\sim}{T}$, and N is the dimension of vector $\underset{\sim}{x}$. One can do this according to the physical reasoning that if the temperature distribution is known to be $\underset{\sim}{T}$, then only one unique solution $\underset{\sim}{x}$ is possible. Thus we can define $f_1,\ f_2\ .\ .\ .\ f_N$, each of which may be considered to define a surface in M dimensional space, where M is the dimension of the temperature vector $\underset{\sim}{T}$.

Eq. (4-38b) can be from the same physical reasoning as for $\underset{\sim}{f}$ rewritten as

$$\underset{\sim}{T} = \underset{\sim}{g}(\underset{\sim}{x}) \qquad (4\text{-}39b)$$

Thus we have, combining Eq. (4-39a) and Eq. (4-39b)

$$\underset{\sim}{x} = \underset{\sim}{f}(\underset{\sim}{T}) \qquad (4\text{-}40a)$$

$$\underset{\sim}{T} = \underset{\sim}{g}(\underset{\sim}{x}) \qquad (4\text{-}40b)$$

More specifically Eq. (4-40) are rewritten as

$$x_i = f_i(\underset{\sim}{T}) \qquad \text{for } i = 1,\ 2\ .\ .\ .\ N \qquad (4\text{-}41a)$$

$$T_i = g_i(\underset{\sim}{x}) \qquad \text{for } i = 1,\ 2\ .\ .\ .\ M \qquad (4\text{-}41b)$$

The functional iterations imply

$$\underset{\sim}{x}^{n+1} = \underset{\sim}{f}(\underset{\sim}{T}^{n+1}) \qquad \text{and} \qquad \underset{\sim}{T}^{n+1} = \underset{\sim}{g}(\underset{\sim}{x}^n)$$

Therefore

$$\underset{\sim}{x}^{n+1} = \underset{\sim}{f}(\underset{\sim}{T}^{n+1}) = \underset{\sim}{f}(\underset{\sim}{g}(\underset{\sim}{x}^n)) \equiv \underset{\sim}{G}(\underset{\sim}{x}^n) \qquad (4\text{-}42)$$

or

$$x_i^{n+1} = G_i(\underset{\sim}{x}^n) \qquad \text{for } i = 1,\ 2\ .\ .\ .\ N \qquad (4\text{-}42)$$

Assume [22] that Eq. (4-42) has a solution at x_{op}, and that all the components G_i have continuous first partial derivatives. For any two points $\underset{\sim}{x}_a$, $\underset{\sim}{x}_b$ in

$$||\underset{\sim}{x} - \underset{\sim}{x}_{op}||_\infty \le \rho \qquad (4\text{-}43)$$

where $||\underset{\sim}{x}||_\infty = \max_j |x_j|$ and ρ is a real number.

We can write

$$G_i(\underset{\sim}{x}_a) - G_i(\underset{\sim}{x}_b) = \sum_{j=1}^{N} \frac{\partial G_i}{\partial x_j}(\xi^i)\ (x_{aj} - x_{bj}),$$

$$\text{for } i = 1,\ 2\ .\ .\ .\ n \qquad (4\text{-}44)$$

where x_{aj}, x_{bj} are <u>jth</u> components of $\underset{\sim}{x}_a$, $\underset{\sim}{x}_b$ respectively, ξ^i is a point on the open line segment joining $\underset{\sim}{x}_a$, $\underset{\sim}{x}_b$. Thus

$$|G_i(\underset{\sim}{x}_a) - G_i(\underset{\sim}{x}_b)| \leq \sum_{j=1}^{N} \left|\frac{\partial G_i}{\partial x_j}\right| \cdot \left|x_{aj} - x_{bj}\right|$$

$$\leq ||\underset{\sim}{x}_a - \underset{\sim}{x}_b||_\infty \sum \left|\frac{\partial G_i}{\partial x_j}(\xi^i)\right| \qquad (4\text{-}45)$$

If we assume that

$$\left|\frac{\partial G_i(\underset{\sim}{x})}{\partial x_j}\right| \leq \frac{\lambda}{N} \qquad \lambda < 1 \quad \text{for } i = 1, 2 \ldots N \qquad (4\text{-}46)$$

then, Eq. (4-45) reduces to

$$|G_i(\underset{\sim}{x}_a) - G_i(\underset{\sim}{x}_b)| < \lambda||\underset{\sim}{x}_a - \underset{\sim}{x}_b||_\infty \qquad (4\text{-}47)$$

Since the inequality holds for each i, we have

$$||G(\underset{\sim}{x}_a) - G(\underset{\sim}{x}_b)||_\infty < \lambda||\underset{\sim}{x}_a - \underset{\sim}{x}_b||_\infty \qquad (4\text{-}48)$$

In particular

$$||\underset{\sim}{x}' - x_{op}|| = ||\underset{\sim}{G}(\underset{\sim}{x}^o) - G(x_{op})||_\infty$$

$$\leq \lambda||\underset{\sim}{x}^o - \alpha||_\infty$$

$$\leq \lambda\,\rho \qquad (4\text{-}49)$$

Thus,

$$||\underset{\sim}{x}^n - \underset{\sim}{x}_{op}||_\infty = ||\underset{\sim}{G}(\underset{\sim}{x}^{n-1}) - G(\underset{\sim}{x}_{op})||_\infty$$

$$\leq \lambda||\underset{\sim}{x}^{n-1} - \underset{\sim}{x}_{op}||_\infty$$

$$\leq \lambda^n \rho \qquad (4\text{-}50)$$

Thus it is shown that under the condition of Eq. (4-46), the iteration would converge. Since

$$\frac{\partial G_i}{\partial x_j} = \frac{\partial G_i}{\partial T_1}\frac{\partial T_1}{\partial x_j} + \frac{\partial G_i}{\partial T_2}\frac{\partial T_2}{\partial x_j} + \ldots + \frac{\partial G_i}{\partial T_M}\frac{\partial T_M}{\partial x_j} = \sum_{k=1}^{M}\frac{\partial G_i}{\partial T_k}\frac{\partial T_k}{\partial x_j} \qquad (4\text{-}51)$$

Eq. (4-46) implies

$$\left|\sum_{k=1}^{M}\frac{\partial G_i}{\partial T_k}\frac{\partial T_k}{\partial x_j}\right| \leq \frac{\lambda}{N}, \ \lambda < 1 \qquad (4\text{-}52)$$

Thus if

$$\max_k \left|\frac{\partial G_i}{\partial T_k}\frac{\partial T_k}{\partial x_j}\right| < \frac{\lambda}{NM} \qquad (4\text{-}53)$$

the condition of Eq(4-46) would be always satisfied. For one-dimensional case (that is, N = M = 1), Eq. (4-53) translates to

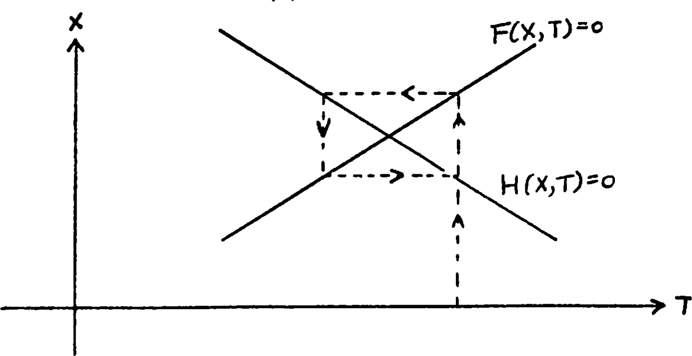
$$\left|\frac{df}{dT}\right| \cdot \left|\frac{dg}{dx}\right| < 1$$

or

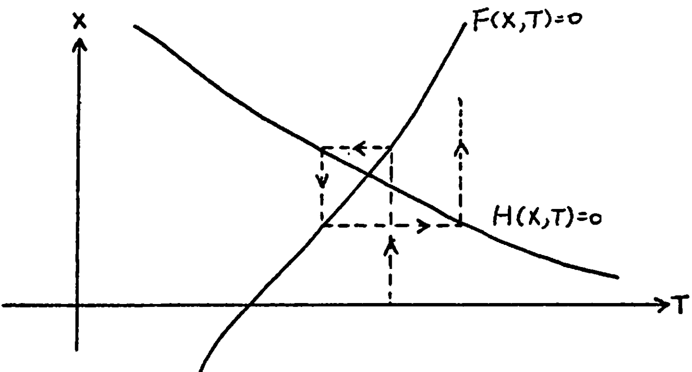
$$\left|\frac{df}{dT}\right| < \left|\frac{dx}{dg}\right| \qquad (4\text{-}54)$$

Fig. 4.15 shows three examples for one-dimensional case. In Fig. 4.15(a), f(T) and g(x) are both weak functions of T and x respectively and $\left|\frac{df}{dT}\right| < \left|\frac{dx}{dg}\right|$. Thus, the iteration would converge rapidly.

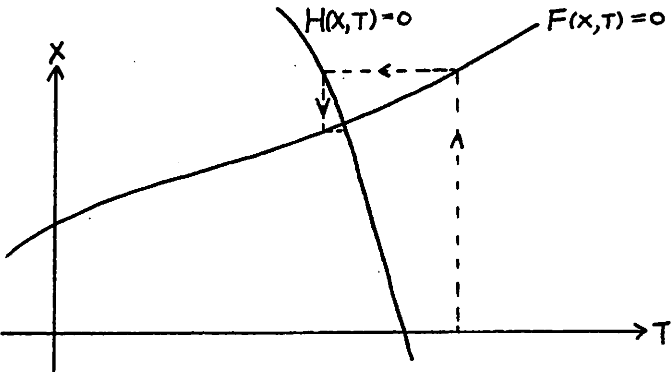
In Fig. 4.15(b), both f(T) and g(x) are strong functions of T and x respectively and $\left|\frac{df}{dT}\right| > \left|\frac{dx}{dg}\right|$. Thus, the iteration would not converge. If in particular, $\left|\frac{df}{dx}\right| = \left|\frac{dx}{dg}\right|$, this would lead to a numerical oscillation as shown in Fig. 4.15(c). To express more



(a)



(b)



(c)

Fig. 4.15

Three examples of iterative solution

clearly the conditions imposed by Eq. (4-54), the dependence of electrical behavior on temperature must be weaker than the dependence of thermal behavior or electrical voltages. Thus we can expect convergence difficulty in a simulation of a circuit in which a strong thermal interaction occurs.

The condition imposed by Eq. (4-53) may be too stringent and physical interpretation is rather difficult to make. The concept of thermal loop gain may be introduced to facilitate this problem. Referring to Fig. 4.16, the significance of convergence property can be seen graphically. Suppose that the initial guess T_o for temperature was different from the correct value by ΔT_o. After one iteration the resulting temperature T_1 will be away from the correct solution by ΔT_1. For the functional iteration to converge we must have $\left|\frac{\Delta T_1}{\Delta T_o}\right| < 1$. That is, the incremental thermal loop gain must be less than 1 for the convergence of the method. To apply this concept to a circuit, we may calculate the most significant thermal loop gain of the circuit. Although this is not sufficient to guarantee that the method converges, it does give a fairly good idea. (To use Eq. (4-52) strictly, we require that the thermal loop gain is less than $\frac{1}{N}$.) A typical example of the class of circuit for which the loop gain may be greater than unity is the temperature stabilized substrate integrated circuit mentioned in Chapter 2. For the system in Fig. 4.17, the thermal loop gain can be calculated as follows: Suppose that the temperature of the diode sensor dropped by ΔT_o from its stabilized temperature. Then the voltage drop across the sensor is

$$\Delta V_d \cong \gamma_T \Delta T_o \qquad \text{(typically, } \gamma_T \cong -2\text{mV/°C)}$$

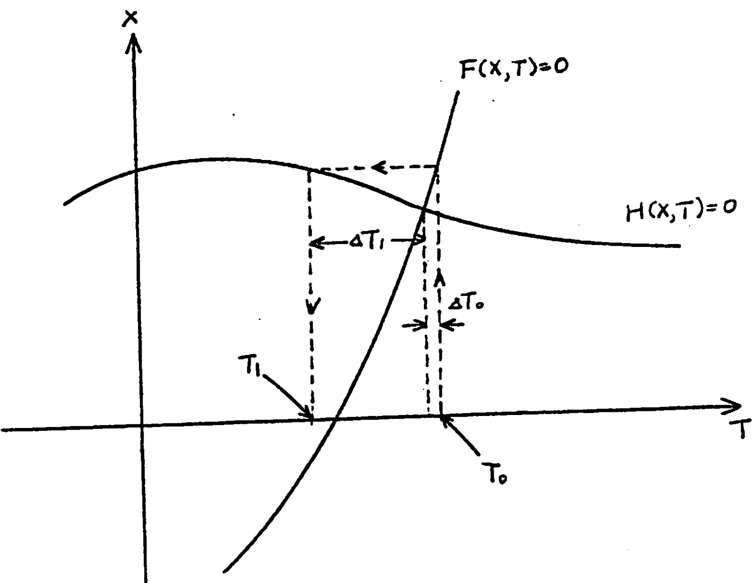


Fig. 4.16

Illustration of convergence criteria for the functional iteration method

If the gain of the amplifier is A_ν and the transconductance of the heater Q_1 is g_m, the resulting increase in power dissipation is

$$\Delta P \cong (\gamma_T \Delta T) A_\nu g_m V_{cc}$$

If the junction to ambient thermal resistance is R_{TH}, the net increase in temperature is

$$\Delta T_1 = \Delta P . R_{TH} = \gamma_T A_\nu g_m V_{cc} R_{TH} \cdot \Delta T_o$$

Thus the thermal loop gain is

$$\frac{\Delta T_1}{\Delta T_o} = \gamma_T A_\nu g_m V_{cc} R_{TH}$$

If $\left|\frac{\partial T_1}{\partial T_o}\right| > 1$, the functional iteration is guaranteed to diverge. For a typical temperature stabilized substrate integrated circuit the loop gain is much greater than one and the convergence difficulty in the modified functional iteration method is expected.

4-4-4. Transient analysis using modified functional iteration method

Transient analysis employing Trapezoidal Integration technique can be easily adapted to the modified functional iteration method. For the simple circuit shown in Fig. 4.11(a), the circuit model is shown in Fig. 4.18.

If the q_{th} is a linear function of T, then the term $\frac{2}{h}\frac{dq_{th}}{dT}$ is a constant (= C_{TH}) for a given time step h. Therefore only one LU decomposition is necessary for each time point. The solution of the method proceeds as follows:

From the given $\underset{\sim}{T}_n$, $\underset{\sim}{V}_n$ at time t_n, the electrical system is first

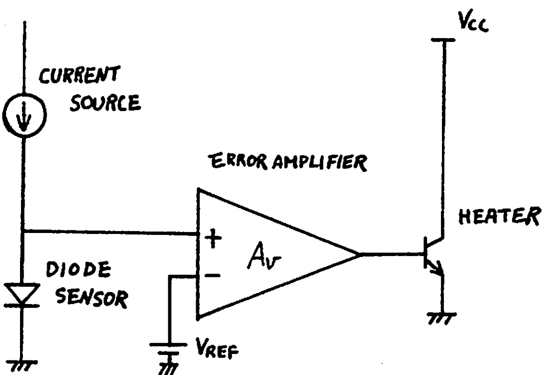
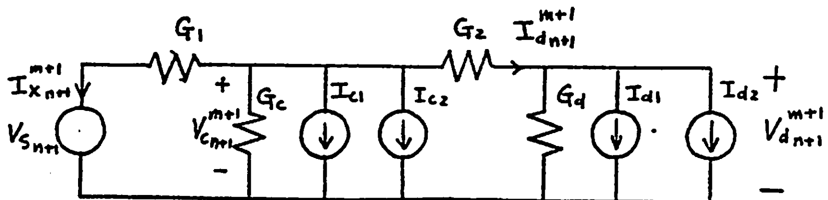


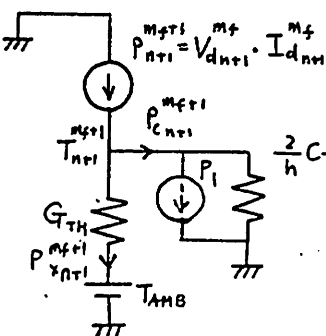
Fig. 4.17

A simple TSS example circuit to illustrate how to calculate thermal loop gain



$$\begin{cases} G_c = \dfrac{2}{h}\dfrac{\partial q}{\partial V_c}\Big|_{n+1}^{m} \\ I_{c1} = \dfrac{2}{h}\left(q_{n+1}^{m} - \dfrac{\partial q}{\partial V_c}\Big|_{n+1}^{m} - \dfrac{\partial q}{\partial T}\Big|_{n+1}^{m_f} \cdot T_{n+1}^{m_f}\right) \\ I_{c2} = \dfrac{2}{h}\left(\dfrac{\partial q}{\partial T}\Big|_{n+1}^{m_f} \cdot T_{n+1}^{m_f}\right) \end{cases}$$

$$\begin{cases} G_d = \dfrac{\partial I_d}{\partial V_d}\ {}_{n+1}^{m} \\ I_{d1} = I_{d_{n+1}}^{m} - \dfrac{\partial I_d}{\partial V_d}\Big|_{n+1}^{m} \cdot V_{d_{n+1}}^{m} - \dfrac{\partial I_d}{\partial T}\Big|_{n+1}^{m_f} \cdot T_{n+1}^{m_f} \\ I_{d2} = \dfrac{\partial I_d}{\partial T}\Big|_{n+1}^{m_f} \cdot T_{n+1}^{m_f} \end{cases}$$



$$P_1 = -\frac{2}{h} C_{TH} \cdot T_n - P_{c\,n}$$

n CORRESPONDS TO TIME STEP
m CORRESPONDS TO NEWTON ITERATION COUNT
m_f CORRESPONDS TO FUNCTIONATL ITERATION COUNT

Fig. 4.18

Circuit model employing modified function iteration method for the example of Fig. 4.12(a)

solved for $\underset{\sim}{V}^{o}_{n+1}$ by the Newton-Raphson method. With $\underset{\sim}{V}^{o}_{n+1}$, $\underset{\sim}{P}^{o}_{n+1}$ is calculated and inserted to the thermal network. The resulting $\underset{\sim}{T}^{1}_{n+1}$ is used to calculate $\underset{\sim}{V}^{1}_{n+1}$, and this process is repeated until $\underset{\sim}{T}_{n+1}$, $\underset{\sim}{V}_{n+1}$ converge. After the convergence is obtained, the next time step, h_{n+1} is calculated according to Eq. (4-29) for both electrical and thermal capacitors. The smallest h_{n+1} is used as the next time step.

If the solution does not functionally converge for a given step size h_n one can reduce the step size so as to cut down the effective thermal loop gain. This would help the convergence of the method under the transient condition. In T-SPICE2A, the step size is reduced by a factor of eight if no convergence in functional iteration is obtained.

One possible advantage of the method in the solution of stiff equations such as the ones we are concerned with is that one might save a considerable amount of computational effort by skipping the analysis of thermal system while the fast electrical behavior associated with small time constants settles. This is not possible with the Newton-Raphson method.

4-5. Conclusion

It has been shown that both the Newton-Raphson's method and the modified functional iteration method can be used for the solution of electro-thermal system. It appears that despite its good convergence property, Newton-Raphson's method seriously suffers from its high cost of computation. The modified functional iteration method, on the other hand, shows an economical alternative. However, it seems that the numerical non-convergence problem may arise in the class of circuits

which enclose a thermal path within a high-gain feedback loop, such as temperature-stabilized substrates integrated systems and thermal multivibrators. Thus it appears that the combined use of two methods is necessary depending upon the particular applications.

CHAPTER 5

EXPERIMENTAL RESULTS

5-1. Introduction

Two programs have been developed. In the first program (referred to as T-SPICE2A subsequently) the modified functional iteration has been used and in the second program (referred to as T-SPICE2B) the Newton-Raphson method is used. The two programs have been used to simulate the performance of several different integrated circuits. The specific user-oriented features of the program are described in the appendix.

In this chapter the comparison will be made between the experimentally observed circuit performance and the computer predicted simulation results. The relative merits of the two algorithms as used in three different types of circuits with respect to the cost of simulation and convergence property are presented.

5-2. Operational amplifiers

The program was first used to predict the dc transfer characteristics of the three 741 operational amplifiers fabricated by three different manufacturers. Shown in Fig. 5.1 are the experimentally observed and the computer predicted characteristics of the first 741 operational amplifier. This integrated circuit schematic and die photo are shown in Fig. 5.2 and Fig. 5.3, respectively. Notice that two external resistors RFB1 and RFB2 are used to place the amplifier

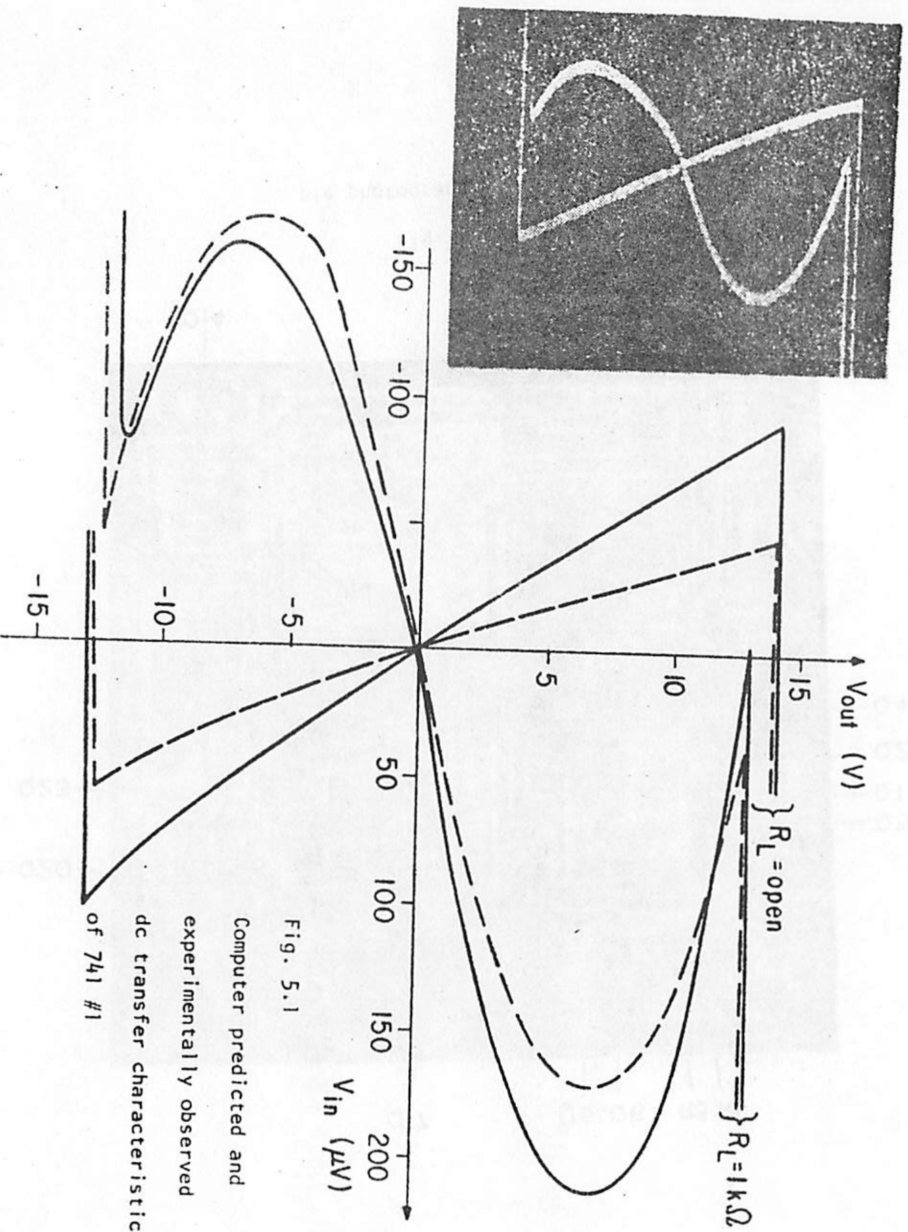


Fig. 5.1

Computer predicted and experimentally observed dc transfer characteristic of 741 #1

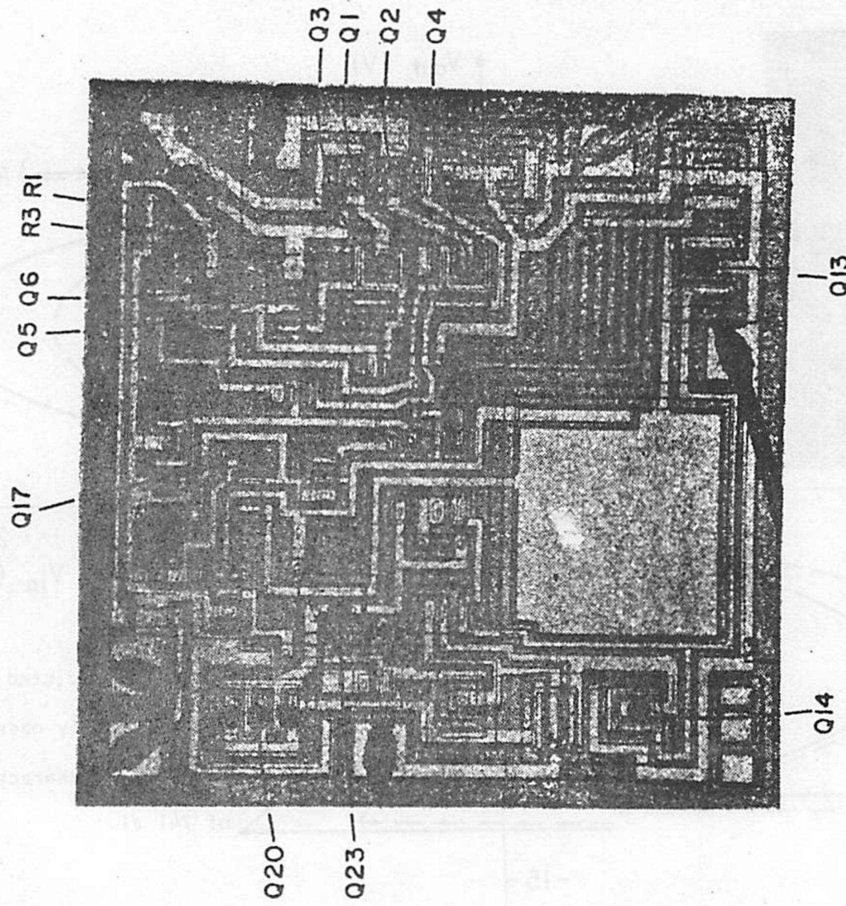


Fig. 5.3

Die photograph of 741 #1

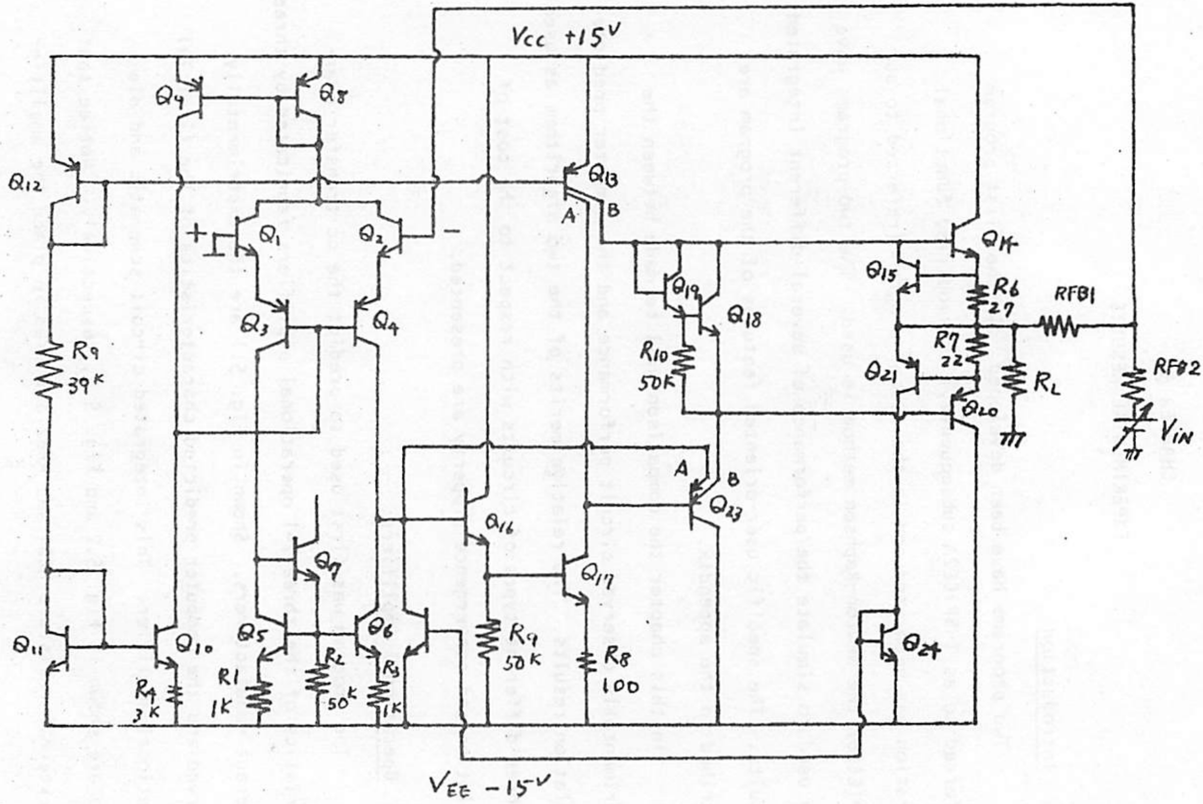


Fig. 5.2

Schematic of 741 #1 and #2

in a negative feedback configuration. This is necessary because most operational amplifiers suffer from a severe thermal feedback effect and the output of the amplifier becomes multi-valued function of input voltage. Notice that agreement between experimentally observed and computer predicted performance is good.

The severe distortion in the dc transfer characteristic is quite understandable when one examines this rather poorly laid out amplifier. The current source Q_{13} as well as the p-n-p emitter follower stage Q_{23} are not laid out symmetrically with respect to the input pairs, Q_1- Q_2, Q_3-Q_4 and Q_5-Q_6. As the output voltage rises, the power dissipation in Q_{23}(Q13) increases (decreases) linearly with output voltage. The combined effect, as the output voltage rises, is to make Q_1, Q_3 and Q_5 hotter than Q_2, Q_4 and Q_6 respectively. When Q_1 and Q_3 get hotter than Q_2 and Q_4 one must apply negative offset voltage which varies linearly with output voltage to the non-inverting terminal to restore the same output voltage that existed when no thermal gradients are present. When Q_5 gets hotter than Q_6, one must apply positive offset voltage to cancel this thermal imbalance. However, the effects of Q_1-Q_2, Q_3-Q_4 pairs dominate over that of Q_5-W_6. Thus under no load condition the power dissipation in Q_{13} and Q_{23} results in the dc transfer characteristic which is tilted to the left on a V_{in} vs. V_{out} plot, as shown in Fig. 5.1.

When the load is attached to the output of the amplifier and the output voltage is positive the power dissipation in Q_{14} makes the temperature of Q_2, Q_4, Q_5 hotter than Q_1, Q_3, Q_6 respectively. In this case the three individual pairs all contribute to increase the offset in positive direction. Thus the dc transfer curve deviates to the

right on a V_{in} vs. V_{out} plot. When the output voltage is negative, a large power dissipation in Q_{20} occurs and makes Q_1, Q_3, Q_5 hotter than Q_2, Q_4, Q_6. However in this case the effect of power dissipation in Q_{20} on Q_1-Q_2, Q_3-Q_4 is opposite to that of Q_5-Q_6 and some cancellation occurs. Consequently the distortion when the output is negative is not quite as bad as the case of output voltage positive.

The program was next applied to a second 741 amplifier which was made by a different manufacturer and had the same electrical circuit but a different layout. The die is shown in Fig. 5.4, and computer predicted and experimentally observed characteristics are shown in Fig. 5.5. Again, the agreement is good. This device was contained in a TO-5 metal package.

The program was used on a third layout of the same 741 circuit fabricated by the third manufacturer. A photograph of this die is shown in Fig. 5.6. The circuit schematic for this amplifier is slightly different from the earlier two just mentioned and shown in Fig. 5.7. At first glance, this circuit appears to be one which is much more optimal than the first two in terms of susceptibility to the thermal feedback effects. The output transistors Q14 and Q20 are located symmetrically along the center line of the die as are the critical input pairs Q1-Q2, Q3-Q4, and Q5-Q6, and indeed there is very little thermal interaction between the output transistors and input pairs. However, this circuit is a good example of a case in which a simple symmetrical layout of the obvious large power dissipating elements does not necessarily yield ideal thermal performance. Notice that current source Q13 is placed so that power dissipation within it can cause temperature differences between the input transistor. As a result, dc transfer

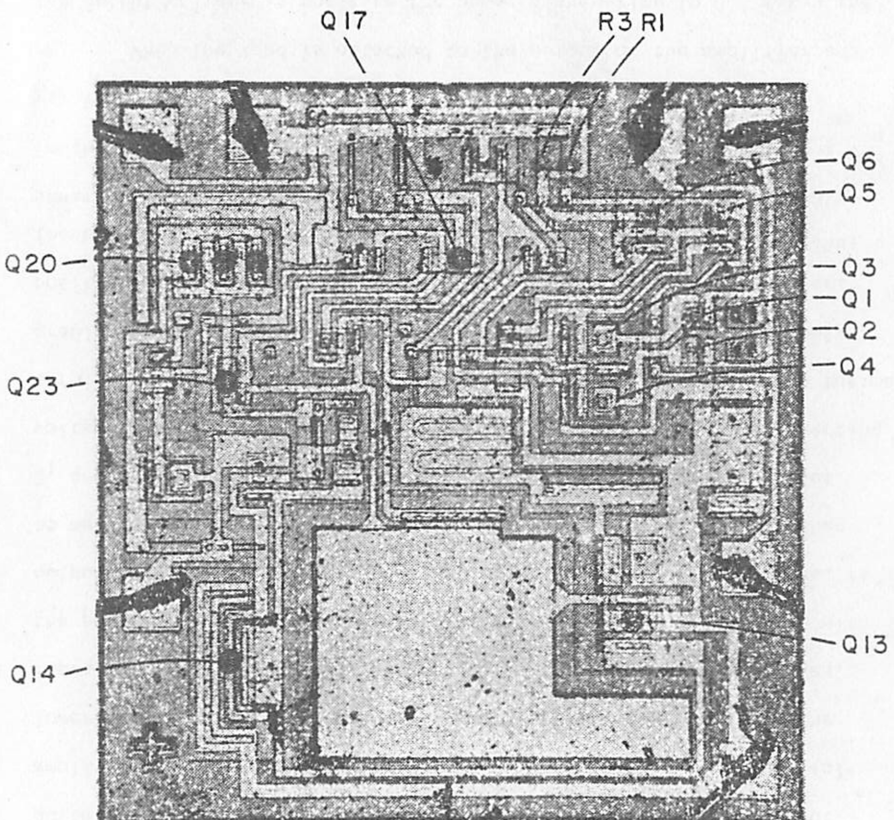


Fig. 5.4

Die photograph of 741 #2

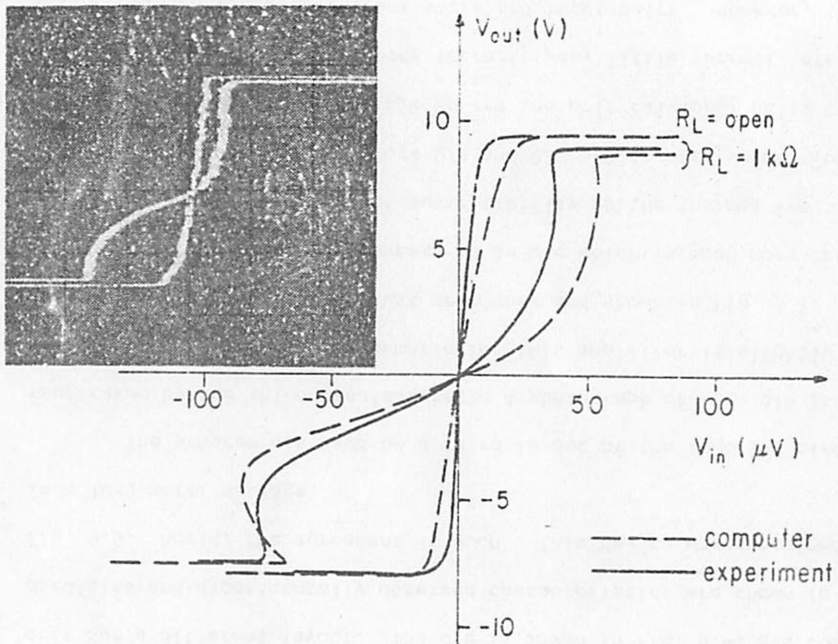


Fig. 5.5

Computer predicted and experimentally observed dc transfer characteristic of 741 #2

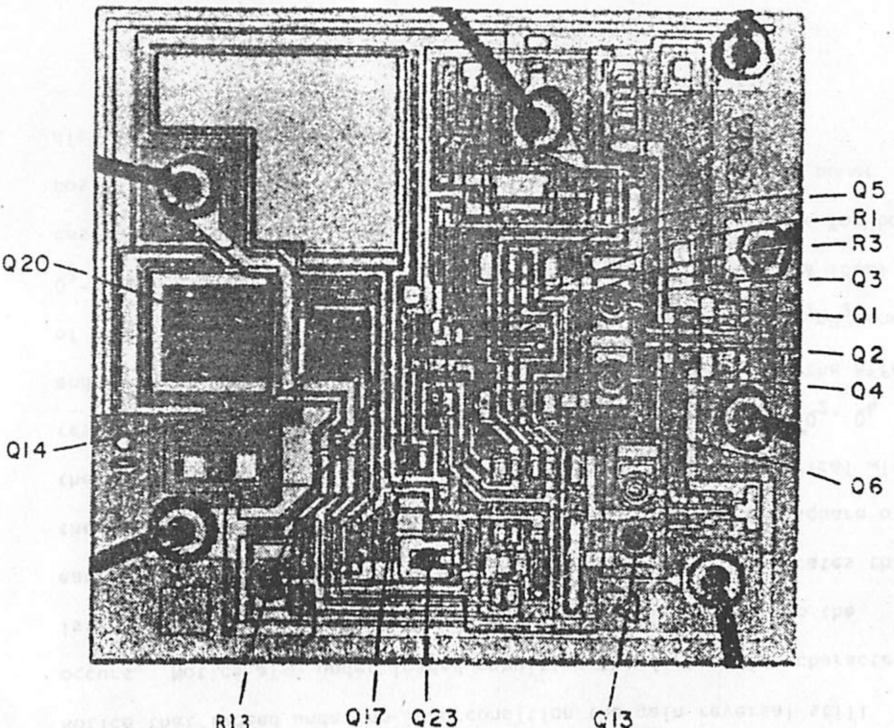


Fig. 5.6

Die photograph of 741 =3

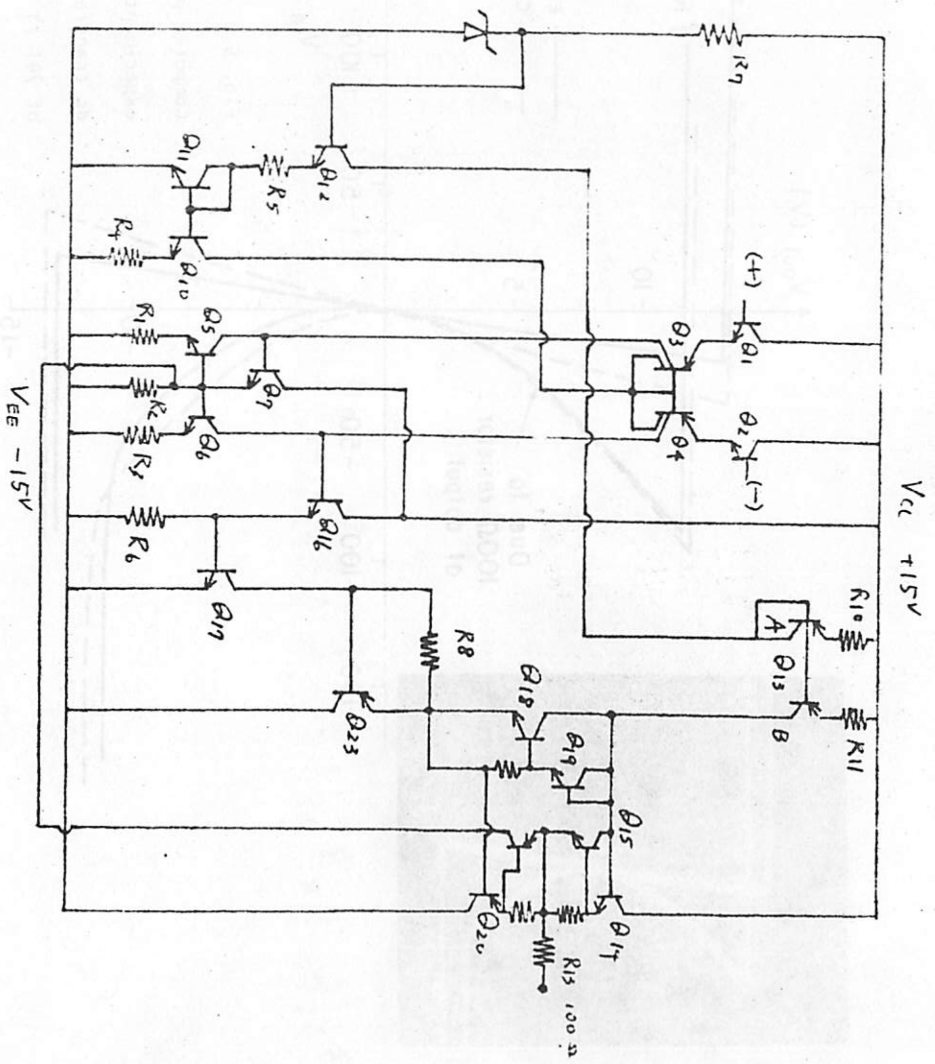


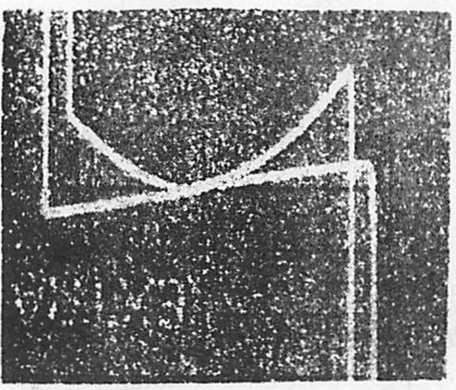
Fig. 5.7

curve still shows a gain reversal in the no load condition. In addition, the 100-Ω resistor R13 shown in Fig. 5.7 which appears in series with output lead for buffering purposes is not located along the die centerline, and its dissipation can cause temperature differences between the input devices. The power dissipation in this resistor can be very significant under heavy load conditions. The observed and computer predicted dc transfer characteristics are shown in Fig. 5.8. Notice that indeed under no load condition the gain reversal still occurs. Notice also under loaded condition the dc transfer characteristic is distorted with a shape which is quite different from the earlier two circuits. The distortion has a shape which indicates that the thermally induced offset voltage is proportional to the square of the output current. Since the location of R13 is not symmetrical with respect to the input pairs, its power dissipation would make Q_2, Q_4 and Q_6 hotter than Q_1, Q_3 and Q_5 respectively. In this case the effect of power dissipation in R13 on Q_5-Q_6 dominates over that on Q_1-Q_2 and Q_3-Q_4 and the deviation of dc transfer characteristic from its ideal case would be in the direction of more negative offset voltage for both positive and negative output voltage. Furthermore, since the power dissipation in R13 varies as

$$R_{13} \cdot I_o^{\,2} = R_{13} \cdot \left(\frac{V_o}{R_L}\right)^2 ,$$

where I_o and V_o are the output current and voltages and R_L is the load resistor, the shape of the deviation will be quadratic with respect to V_o.

The program was also used to predict the dc transfer



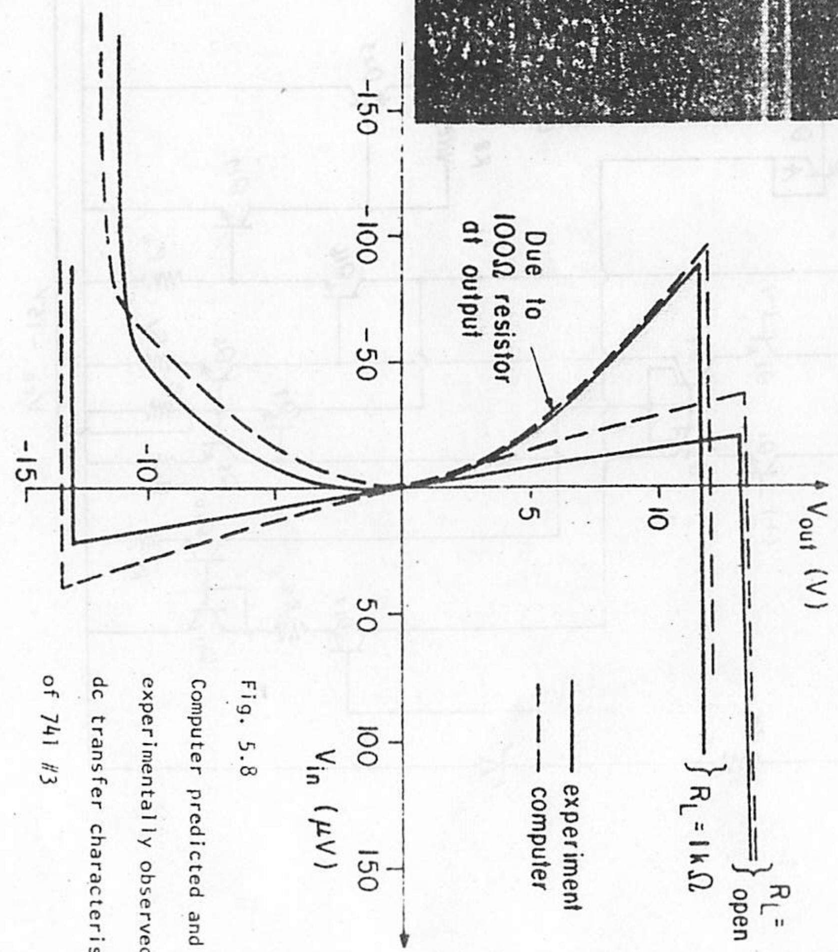


Fig. 5.8
Computer predicted and experimentally observed dc transfer characteristic of 741 #3

characteristics of Fairchild 7118 operational amplifier. Fig. 5.9 shows the experimentally observed and computer predicted dc transfer characteristics. Again the agreement is good.

For the first three circuits, both Newton-Raphson method and modified functional iteration method converged. The fourth circuit failed to converge at several points. Shown in Table 5.1 is the comparison of the CPU time needed for the analysis portion of the program. Notice a rather dramatic reduction in the cost of simulation when the modified functional iteration is used. The ratio in CPU time of the two methods is approximately two to three. Table 5.2 indicates the saving achieved in the number of iterations in the Newton-Raphson algorithm for an operating point analysis when a scheme is employed in which the electrical network is solved separately at a user-specified guess temperature and the resulting voltages are used as an initial junction voltage guess for the coupled electro-thermal network. Again a tremendous saving in iteration counts of anywhere between 70 to 90% occurs at the expense of small amount of computational effort at the onset of the analysis. This involves the setup of the matrix for electrical network as well as the solution of the electrical network. (The CUP time indicated in Table 5-1 for the Newton-Raphson method is obtained when the junction initializing scheme is employed.)

5-3. Voltage regulators

As mentioned in the first chapter, the undesired effects of thermal feedback can be most significant in integrated circuits which experience large power dissipation. A good example of such a circuit is a three-terminal voltage regulator illustrated schematically in

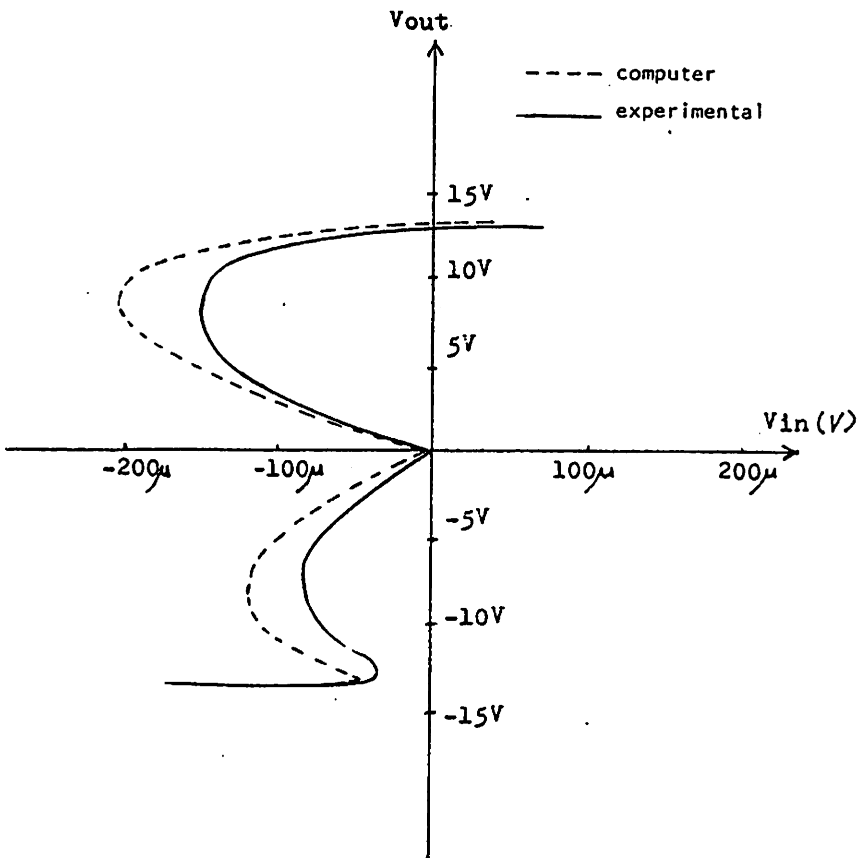


Fig. 5.9

Computer predicted and experimentally observed dc transfer characteristic of Fairchild 7118 op. amp

TABLE 5.1

CPU Time on CDC 6400 Spent by Analysis Portion of the Simulation

Circuit Name	Newton-Raphson Method	Modified Functional Iteration Method
741 op. amp. #1	328.3 sec	118.5 sec
741 op. amp. #2	898.3 sec	102.64 sec
741 op. amp. #3	211.1 sec	119.5 sec
µA 7118	158.2 sec	353 sec
LM140d #1	573.7 sec	200 sec
LM140d #2	692.9 sec	174.9 sec
LM140d #3 new layout	464.2 sec	123.2 sec
LM Negative Regulator #1	199.9 sec	74.7 sec
LM Negative Regulator #2	182.7 sec	71.6
LM40E TSS	408.4 sec	no convergence

TABLE 5.2

Comparison of Number of Iterations in the Newton-Raphson's Method for dc Operating Analysis when the Junction Initializing Scheme Is and Is Not Used

Circuit Name	With	Without
741 op. amp. #1	34	6
741 op. amp. #2	25	6
741 op. amp. #3	40	9
µA 7118	40	11
LM140d #1	30	3
LM140d #2	30	3
LM140d #3 new layout	41	3
LM Negative Regulator #1	93	4
LM Negative Regulator #2	24	4
LM40E TSS	34	42

Fig. 5.10(a). The circuit usually consists of a reference voltage source, error amplifier, and series pass transistor. When a load resistor is suddenly attached to the output of the regulator the load current increases to a large value and the power dissipation in the pass transistor increases suddenly. As a result, die temperature increases and thermal gradients are generated which propagate from the power transistor across the die. These thermal gradients affect the circuit performance in two important ways. An output waveform which might be observed as a function of time after the application of the load at t = 0 is illustrated in Fig. 5.10(b). First, after the thermal gradients have settled to their steady state value the resulting temperature differences between critical circuit elements can cause the stady-state output voltage to be different from that which existed under no load condition. Secondly, in addition to this phenomenon, when the load is applied at t = 0, the thermal gradients which are generated do not necessarily reach all the devices within the circuit at the same time. As a result a non-monotonic transient output waveform can occur due to the resulting transient thermal imbalance. In the frequency domain these time varying thermal gradients have the effect of producing humps and dips in the output impedance and line regulation as a function of frequency. Because of the thermal natural frequencies of the die package structure, they tend to occur at the undesirable values near 60 Hz, 120 Hz and 180 Hz.

A typical monolithic voltage regulator circuit, the National LM-140 [23], is shown in simplified form in Fig. 5.11. The circuit consists of series pass transistor Q16 and the band gap circuitry composed of transistor Q1 through Q8. The output voltage can be seen to

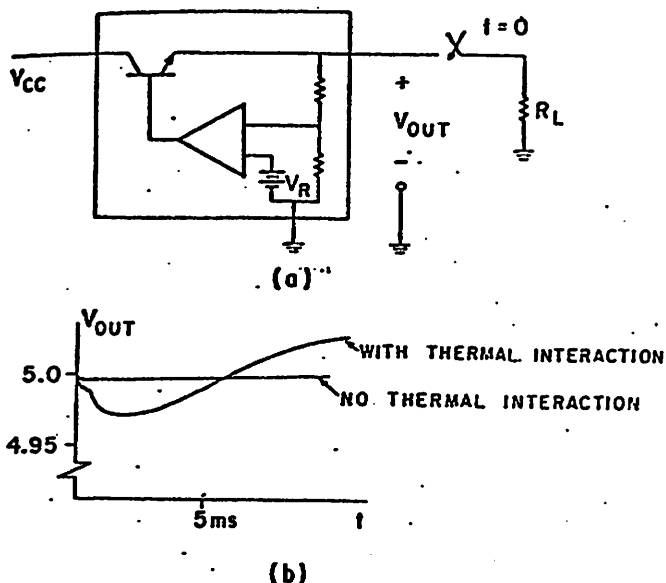


Fig. 5.10

(a) block diagram of a typical three-terminal voltage regulator

(b) typical output voltage waveform in response to a step increase in input current

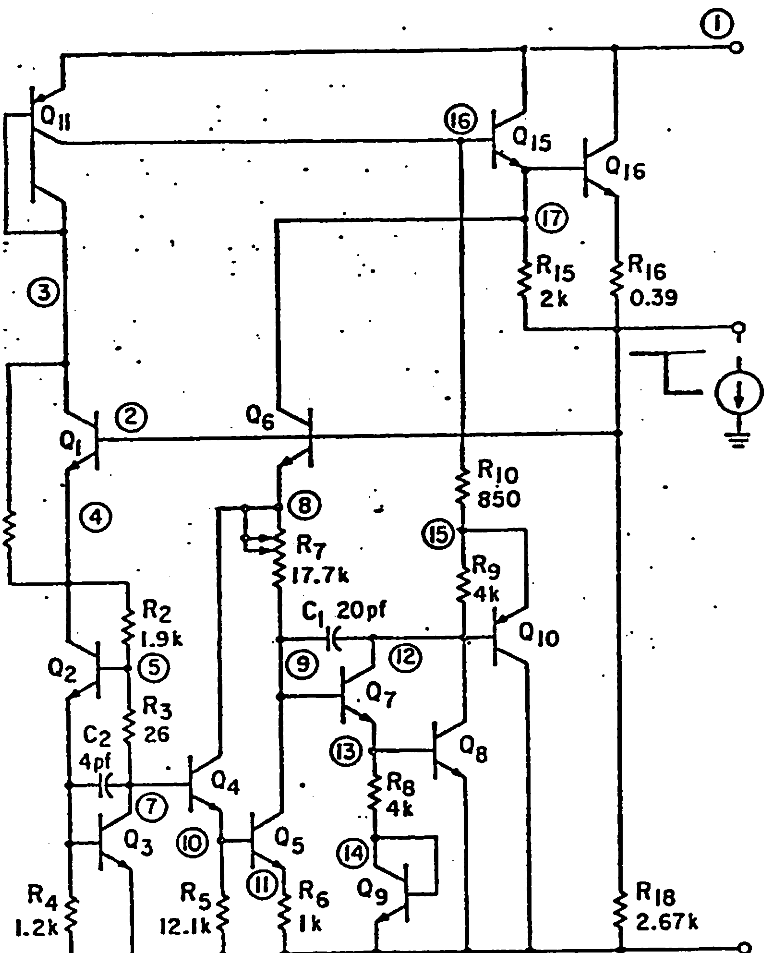


Fig. 5.11

Simplified schematic of LM140d voltage regulator

be the sum of the base-emitter diodes drops in Q6, Q7 and Q8 plus the voltage drop across R_7. The voltage drop in R_7 is proportional to the voltage $(V_{BE3} + V_{BE2}) - (V_{BE4} + V_{BE5})$ multiplied by a constant which is approximately equal to 17. Thus if any temperature differences exist between transistors Q2-Q3 and transistors in Q4-Q5, a large change in output voltage will occur. In addition, any difference in temperature between the group of transistors Q6, Q7, Q8, and that of the second group Q2, Q3, Q4, Q5 will result in a significant but smaller change in output voltage.

The die photo of one layout of this particular regulator circuit is shown in Fig. 5.12. The elements associated with the band gap reference are located down the left side of the die while the large structure on the right side is the output power transistor. The behavior of two different versions of this circuit was simulated using the program described above. In the first version, only the center emitter of the three-emitter transistor Q2 was electrically connected so that all of the devices associated with the band gap reference were distributed in a straight line along the left edge of the die. Because the isothermal lines which result from dissipation in the output transistor are curved, it is clear that transistors Q6, Q5, Q4 get hotter than Q2 and Q3. As a result this circuit displays a large change in the steady-state output voltage when power is dissipated in the output transistor. Fig. 5.13 shows the observed and predicted output voltage waveform, labeled version 1, when a 1.5 A current pulse is applied to the output of the regulator. The solid line is the experimentally observed response and the dotted line is the computer predicted response.

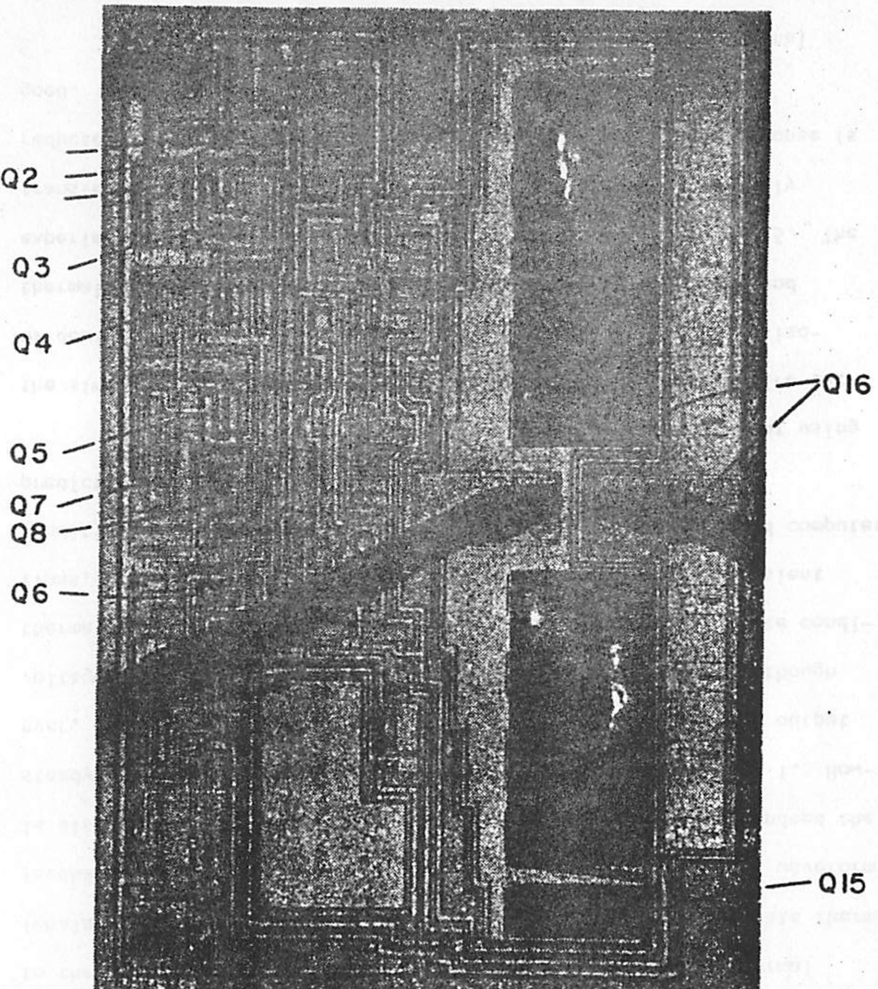


Fig. 5.12

Die photograph of the LM140d

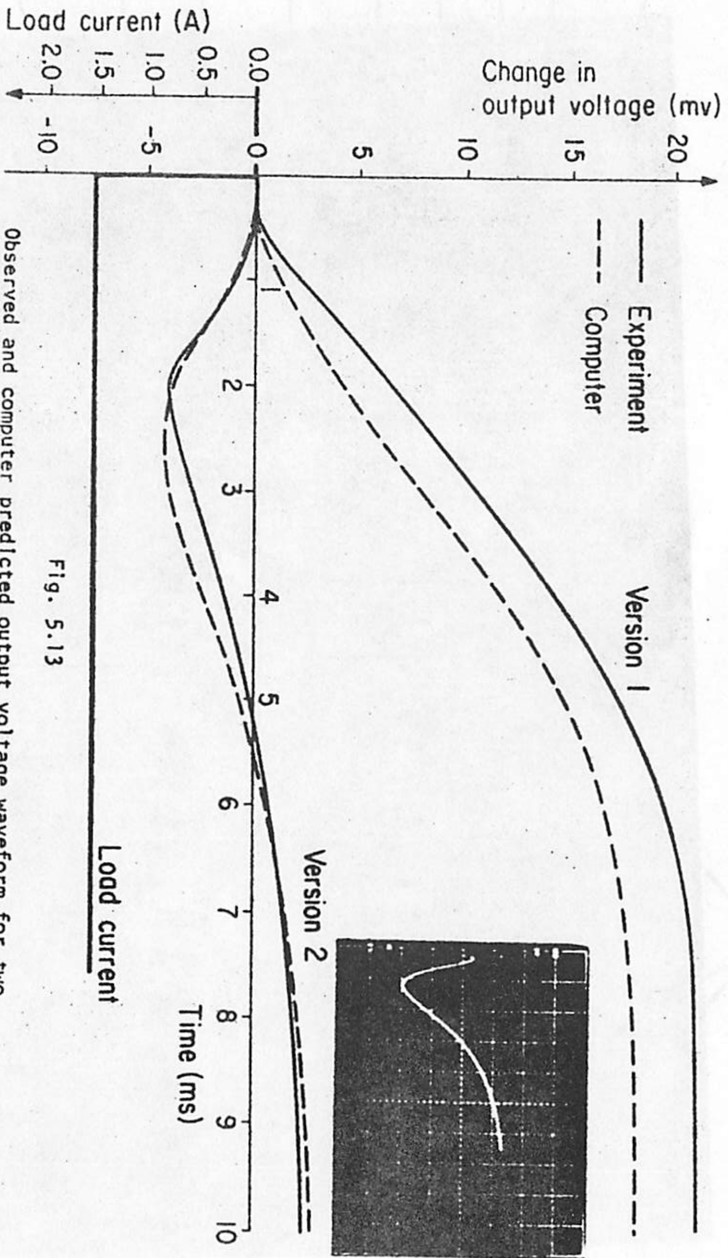


Fig. 5.13

Observed and computer predicted output voltage waveform for two versions of the LM140d in response to a 1.5A output current step.

A second, modified version of this chip was fabricated in order to attempt to correct this problem in which the emitter of Q2 which is closer to the power transistor than in the first version was electrically connected. This was done in an effort to counterbalance the thermal imbalance between the group Q2, Q3, Q4, and Q5 with reference to the group Q6, Q7, and Q8 by introducing a compensating thermal imbalance between Q2 and Q3. By doing this the net steady-state thermal feedback could hopefully be reduced. The resulting transient waveform is also shown in Fig. 5.13, labeled version 2. Notice that indeed the steady-state output voltage change is smaller than in version 1. However, the change introduced a negative going transient to the output voltage which did not exist before. This results because, although thermal coupling mechanism has been canceled under steady-state conditions, the thermal imbalance has not been canceled under transient conditions. The agreement between experimentally observed and computer predicted response is good.

A complete relayout of the circuit was next carried out using the simulator as a tool to check each layout change. The entire set of devices Q2, Q3, Q4, Q5, Q6, Q7, and Q8 was placed along an isothermal line as shown in Fig. 5.14. The resulting simulated and experimentally observed output waveforms are shown in Fig. 5.15. The transient and steady-state output voltage variations are greatly reduced, and the agreement between predicted and observed response is good.

Both the Newton-Raphson algorithm and modified functional iteration showed convergence and their respective CPU time involved in the analysis are listed in Table 5.1. Also shown are the similar

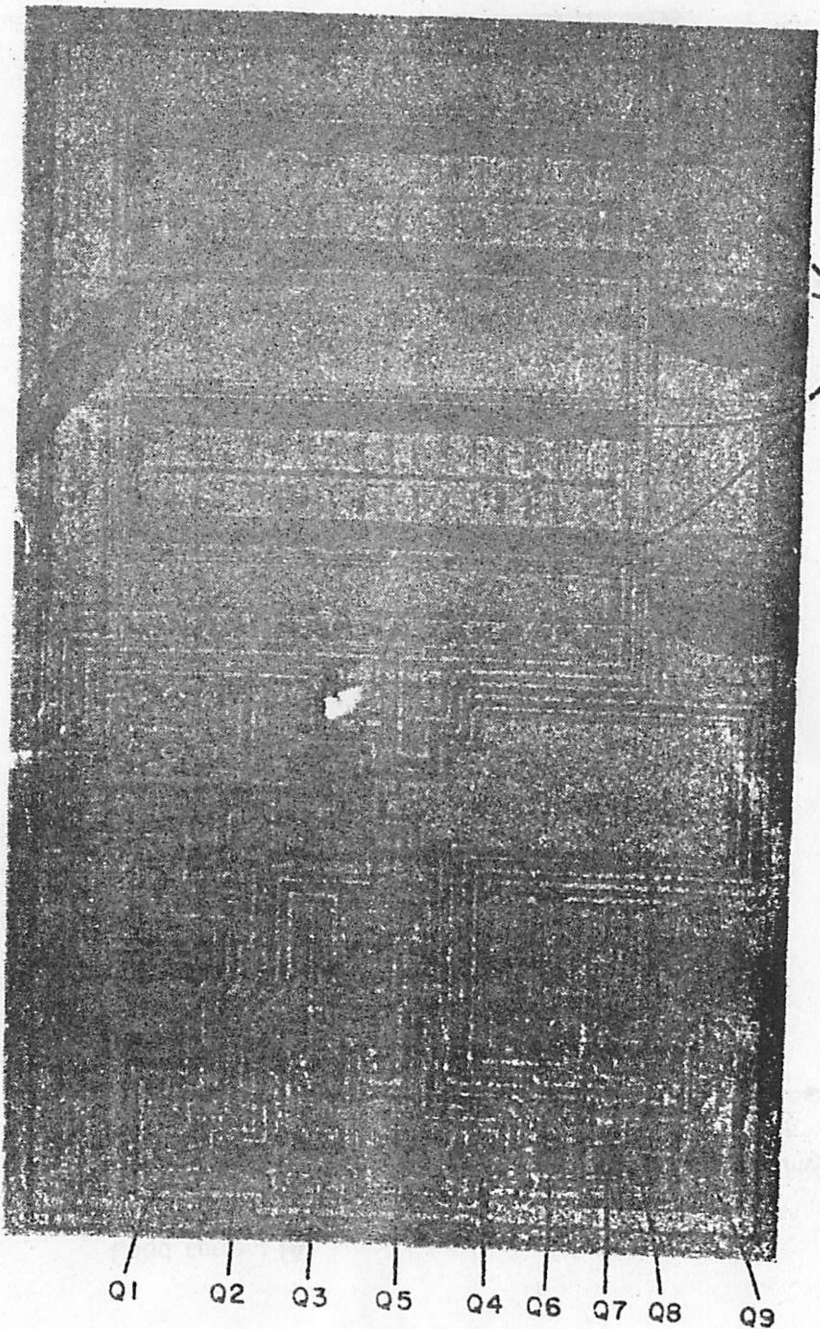


Fig. 5.14

Photo of revised LM140d chip

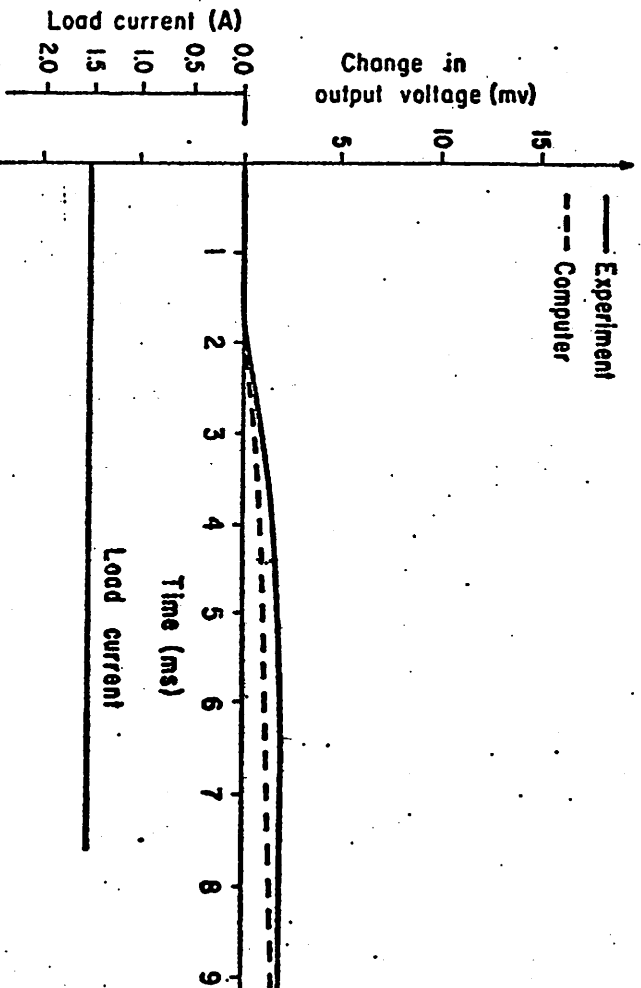


Fig. 5.15

Computer predicted and experimentally observed transient response of revised chip

results for LM120ML [22] negative voltage regulators. Table 5.2 shows the number of iterations required by Newton-Raphson method when the junction initializing scheme is and is not used. Notice for these transient runs the ratio of CPU time of the two methods is roughly three. The junction initializing scheme is quite effective and shows approximately 90% saving in CPU time in the operating point analysis.

In all three transient runs, the electrical energy storage elements have been removed from the circuit. This was done to avoid excessive cost in simulation run caused by the large spread in time constants. This is probably acceptable for most transient simulation because when there exists a large spread in electrical and thermal constants, one really does not need thermal simulation capability to determine the circuit behavior that occurs in the order of small electrical time constants. Of course when the two sets of time constants are comparable one must include electrical energy storage elements for the complete simulation of the program.

5-4. Temperature stabilized substrate integrated circuit system

The program was next applied to a temperature-stabilized substrate integrated circuit system. The objective of this system, illustrated in Fig. 5.16 [3], is the reduction of effective temperature sensitivity of the integrated circuit by stabilizing the die temperature at constant value independent of the ambient temperature variations. The problem which occurs in the actual behavior of the circuit is that as the ambient temperature varies the heater transistor power must vary which gives rise to the chip temperature variation. In Fig. 5.16(a) the chip temperature distribution which results when the

ambient temperature is kept constant and the heater power is varied is illustrated. Notice that the temperature differences between one end of the chip and the other increases as the heater power is increased. If the feedback loop is then closed with a large amount of loop gain, the effect will be to keep the temperature at the feedback sensor constant. However, the temperature variation from one end of the chip to the other as a function of heater power results in a family of temperature curves across the chip as illustrated in Fig. 5.16(b). All of the devices located along the dotted line passing through the feedback sensor will not experience any temperature variation as the ambient temperature varies. The other locations of the chip will experience either positive or negative temperature variations. In practice a rather moderate amount of loop gain must be used for stability reasons. Because of this the point of zero temperature variation moves closer to the heat source. For optimum performance, the critical elements of the stabilized circuit should be located on this locus or zero temperature variation.

The program was used to simulate the performance of the LM199 temperature-stabilized voltage reference source [24]. The schematic diagram of this circuit is shown in Fig. 5.17. The upper portion of the circuit is the temperature regulator; Q11 is the controlled heat source and Q13 is the temperature sensing device. The lower portion of the circuit is the circuit to be stabilized. Zener diode Z1 and diode Q4 together form a temperature-compensated reference diode. The rest of the circuitry is a shunt regulator for the zener to reduce its incremental impedance. The regulator circuit is set up to stabilize the chip at approximately 90°C.

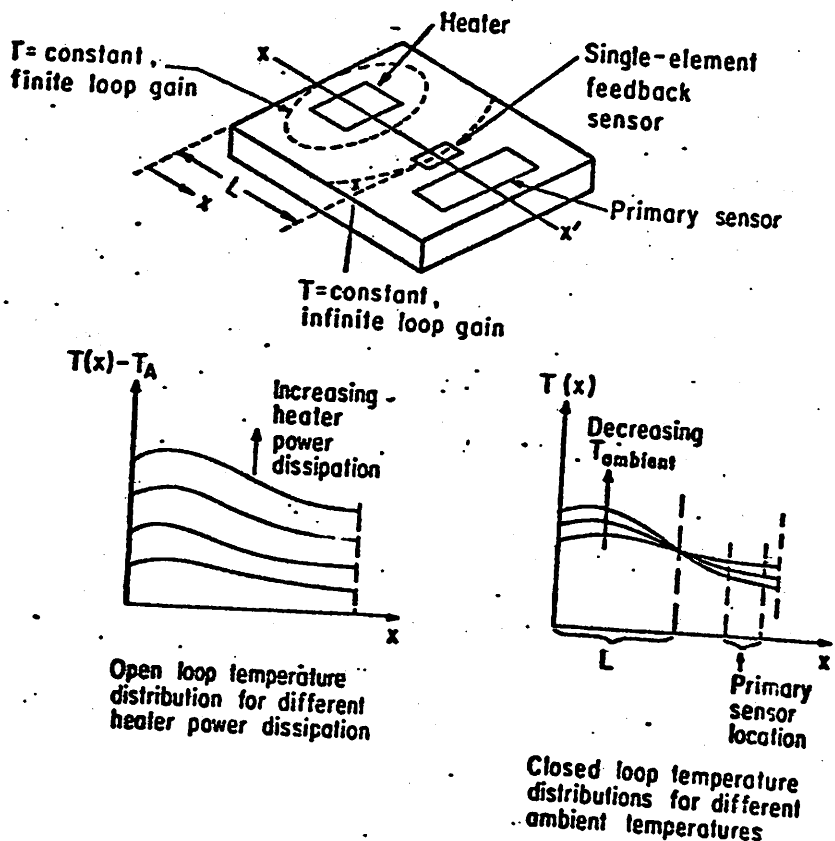


Fig. 5.16

Temperature distribution within a TSS system

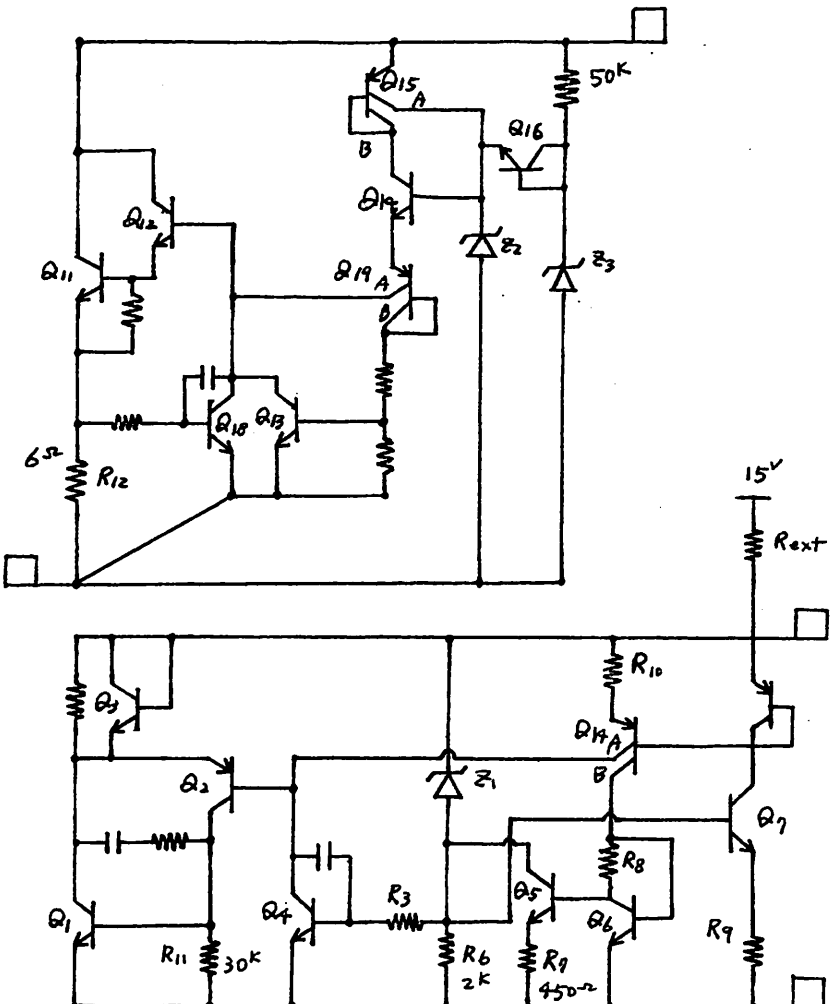


Fig. 5.17

LM199 temperature-stabilized substrate voltage reference

The LM199 die is shown in Fig. 5.18. The heater, sensor, and reference diode are labeled. The dark lines on the photograph are TSPICE predicted lines of constant temperature for an ambient temperature variation of -40°C to 90°C. As expected, a line of zero temperature variation does exist, and passes within about two mils of the feedback sensor. The regions close to the heater experience a negative shift in temperature as the ambient temperature increases, while the regions far from the heater experience a positive shift in temperature. According to the simulation, the feedback sensor, the zener and its compensating diode all experience a positive shift of about 1°C. Direct measurement of the zener diode temperature by measurement of its forward voltage shows that the actual temperature variation is very close to this value. Movement of the zener diode and the compensating diode closer to the heater would result in smaller voltage drop so that the unstabilized temperature coefficient of forward drop in the combination is nominally zero with some statistical deviation about this nominal value from unit to unit. The amount of temperature variation at the zener and compensating diode will determine the amount of deviation from zero temperature coefficient in a sample of stabilized units. Thus the effect of moving the zener and the compensating diodes closer to the heater would be to tighten the distribution of observed TCs in stabilized units, without affecting the nominal value of zero temperature coefficient.

For this circuit, the Newton-Raphson method did converge but the modified functional iteration method failed to converge. This result is in accordance with the earlier prediction that in a circuit where a strong thermal interaction occurs, the modified functional

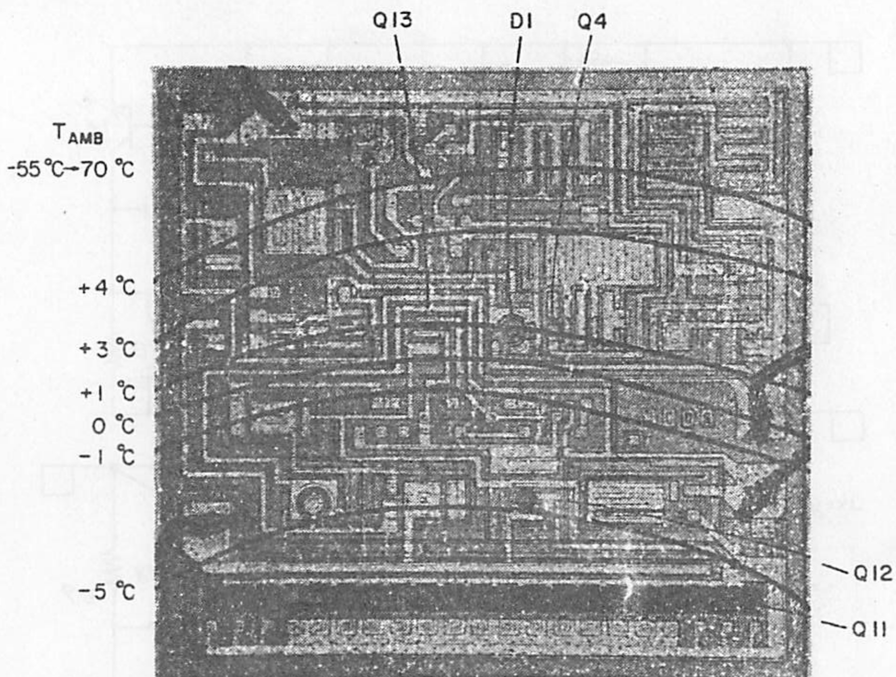


Fig. 5.18

Die photograph of the LM199 showing lines of constant temperature. The indicated temperatures on the isotherms are the variation in temperature experienced by points on the line for an ambient change from -40°C to 70°C.

iteration will fail to converge. The reason for the convergence failure of the modified functional iteration method can be deduced from the actual operating point of the circuit obtained by the Newton-Raphson method. Referring to Fig. 5.17, the sensor Q13 stabilizes at 105°C, V_{BE} = 0.514V, I_c = 0.4 ma. Now if the temperature of Q13 changes by -1°C, then the base current of the driver transistor Q12 increases by (0.4 ma) (8%) = 32 ua. Correspondingly the power dissipation of the heater increases by roughly

$$\Delta I_c = V_{CE} \cdot \Delta I_B \cdot \beta^2 = 9.6 \text{ watts},$$

where V_{CE} is the collector to emitter voltage,

ΔI_c is the increase in collector current,

$\Delta I_c = I_B \beta^2$ where β is the current gain of the transistors.

For this particular die package structure, the junction to ambient thermal resistance is 200°C/W. Thus this increase in power dissipation would raise the chip temperature by about 1920°C. Thus the incremental thermal loop gain at this operating condition is 1920. As mentioned earlier if thermal loop gain is greater than one, then the modified functional iteration would not converge.

Table 5.1 lists the CPU time required on CDC 6400 by the Newton-Raphson method. Table 5.2 shows the comparison in the number of iteration when the junction initializing scheme is and is not used. In this class of circuits however there is no saving in iteration number and in fact one is better off not employing the junction initializing scheme.

CHAPTER 6
CONCLUSION

6-1. Summary

The objectives of this dissertation have been accomplished as follows:

(1) A new general purpose electro-thermal program that predicts the dc and transient performance of integrated circuits in the presence of electro-thermal interactions on the integrated circuit die has been developed.

(2) Two associated numerical methods have been developed and investigated. It has been mathematically proven and clearly demonstrated that the combined use of the two methods is necessary for the economical simulation of electro-thermal behavior depending upon the particular application.

(3) An accurate physical model of the die package structure has been developed.

(4) The asymmetrical finite difference method has been introduced to form a lumped thermal network that represents the thermal behavior of the die package structure accurately and efficiently. This resulted in a significant reduction of thermal nodes compared to a straightforward finite difference method.

(5) The program is written in such a way that the simulation of such anamolies as die-attach voids, flip chip attach bonding, etc., could be easily adopted in a lumped form.

6-2. Recommendation for further work

Further research should concentrate first in two areas. One would be the development of more efficient algorithms to reduce the cost of simulation. The other is to extend the usefulness of the program by including the simulation capabilities other than those already done in this research.

For the first category the following may be suggested:

(1) The development of an algorithm that would generate a lumped model for the die package structure with efficiency and accuracy yet with fewer number of thermal nodes.

(2) The development of proper criteria in modified functional iteration for skipping the transient analysis of slowly changing thermal behavior while the fast changing electrical variables settle down.

(3) The development of a scheme for controlling the step size in the transient analysis using the modified functional iteration so as to assure convergence and accuracy as mentioned in Chapter 4.

For the second category, the following additional features would be generally useful:

(1) the small-signal ac analysis

(2) Pole-zero calculation

(3) Thermal distortion analysis

The small-signal ac analysis can be done in a straightforward manner. This would involve linearizing both the electrical and thermal elements about some operating point in the same manner as in Chapter 4. The pole-zero analysis will provide invaluable data for the design of electro-thermal filters. The thermal distortion may become very important in a design of high quality low frequency amplifier. The

thermal distortion analysis may be carried out using a perturbation method as follows [25]:

a) First apply an electrical excitation of frequency to the electrical network and obtain the resulting small signal response $\underset{\sim}{x}_a$ at ω_o. In a more mathematical form, we start from

$$\dot{\underset{\sim}{x}} = \underset{\sim}{f}(\underset{\sim}{x}, \underset{\sim}{T}) + \underset{\sim}{g}(t) \tag{6-1}$$

$$\dot{\underset{\sim}{T}} = \underset{\sim}{H}\underset{\sim}{T} + \underset{\sim}{P}(\underset{\sim}{x}, \underset{\sim}{T}) \tag{6-2}$$

Taylor expansion of Eq. (6-1) gives

$$\begin{aligned} \dot{\underset{\sim}{x}} &= \underset{\sim}{f}_o(\underset{\sim}{x}_o, \underset{\sim}{T}_o) + g_o(t) + \frac{d\underset{\sim}{f}}{d\underset{\sim}{x}}(\underset{\sim}{x} - \underset{\sim}{x}_o) \\ &+ \frac{1}{2!}\frac{d^2\underset{\sim}{f}}{d\underset{\sim}{x}^2}(\underset{\sim}{x} - \underset{\sim}{x}_o)^2 + \ldots + \frac{d\underset{\sim}{f}}{d\underset{\sim}{T}}(\underset{\sim}{T} - \underset{\sim}{T}_o) \\ &+ \frac{1}{2!}\frac{d^2\underset{\sim}{f}}{d\underset{\sim}{T}^2}(T - T_o)^2 + \ldots \end{aligned} \tag{6-3}$$

Take only the first three terms on the right-hand side and remove the dc components to arrive at

$$\dot{\underset{\sim}{x}}_a = \underset{\sim}{g}_o(t) + \frac{d\underset{\sim}{f}}{d\underset{\sim}{x}}\underset{\sim}{x}_a \tag{6-4}$$

where $\underset{\sim}{x}_a = \underset{\sim}{x} - \underset{\sim}{x}_o$ and $\dot{\underset{\sim}{x}}_a = \dot{\underset{\sim}{x}}$, and x_o, T_o correspond to dc operating point. For a given excitation $g_o(t)$, one can solve for $\underset{\sim}{x}_a$. $\underset{\sim}{x}_a$ is the small-signal variations.

b) Using the resulting small signal response x_a, obtain power

dissipation at the frequency of $2\omega_o$. Apply this excitation to the thermal network and obtain small-signal temperature variation $\Delta\underset{\sim}{T}_a$ at $2\omega_o$. That is, first Taylor expand Eq. (6-2) to get

$$\dot{\underset{\sim}{T}}_a = \underset{\sim}{H}\underset{\sim}{T}_a + \frac{d\underset{\sim}{P}}{d\underset{\sim}{x}}\underset{\sim}{x}_a + \frac{1}{2}\frac{d^2\underset{\sim}{P}}{d\underset{\sim}{x}^2}\underset{\sim}{x}_a^2 + \ldots \tag{6-5}$$

where $\underset{\sim}{T}_a = \underset{\sim}{T} - \underset{\sim}{T}_o$ and $\dot{\underset{\sim}{T}}_a = \dot{\underset{\sim}{T}}$. Then use $\underset{\sim}{x}_a$ obtained in part (a) to obtain $\underset{\sim}{T}_a$ at $2\omega_o$.

c) Substitute the small-signal temperature variation $\underset{\sim}{T}_a$ at $2\omega_o$ in Eq. (6-3) and solve for $\underset{\sim}{x}_a$ at $2\omega_o$. That is, solve

$$\dot{\underset{\sim}{x}}_a = \frac{d\underset{\sim}{f}}{d\underset{\sim}{x}}\underset{\sim}{x}_a + \frac{d\underset{\sim}{f}}{d\underset{\sim}{T}}\underset{\sim}{T}_a \qquad \text{for } \underset{\sim}{x}_a.$$

Thus it appears that this perturbation method could easily be adopted to the modified functional method.

APPENDIX I

USER'S GUIDE

UNIVERSITY OF CALIFORNIA
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING
AND COMPUTER SICIENCES

KIYOSHI FUKAHORI
PAUL R. GRAY

USER*S GUIDE FOR T-SPICE

T-SPICE IS A GENERAL-PURPOSE CIRCUIT SIMULATION PROGRAM FOR NONLINEAR
DC AND NONLINEAR TRANSIENT ANALYSES. CIRCUITS MAY CONTAIN RESISTORS,
CAPACITORS, INDUCTORS, MUTUAL INDUCTORS, INDEPENDENT VOLTAGE AND CURRENT SOURCES,
LINEAR, AND NONLINEAR VOLTAGE CONTROLLED CURRENT SOURCES, BJTS, AND ZENER DIODES.
THE SPECIAL FEATURE OF T-SPICE IS THAT IT TAKES INTO ACCOUNT THE EFFECT OF CHIP
TEMPERATURE GRADIENTS AND VARIATIONS DUE TO LOCALIZED POWER DISSIPATION WITHIN
THE ELEMENTS OF THE INTEGRATED CIRCUITS IN DETERMINING THE BEHAVIOR OF THE
CIRCUITS.

TWO PROGRAMS, T-SPICE2A AND T-SPICE2B ARE AVAILABLE FOR SIMULATING ELECTRO-
THERMAL CIRCUIT PERFORMANCE. THE FORMER USES THE MODIFIED FUNCTIONAL ITERATION
METHOD WHILE THE LATTER USES THE NEWTON-RAPHSON METHOD. THE PGOGRAM T-SPICE2A
SHOULD BE USED FOR ALL TYPES OF INTEGRATED CIRCUIT SIMULATIONS EXCEPT THOSE
INVOLVING STRONG THERMAL INTERACTIONS SUCH AS TEMPERATURE STABILIZED SUBSTRATE
INTEGRATED CIRCUITS. FOR THIS TYPES OF CIRCUITS AND OTHERS THAT HAVE CONVER-
GENCE PROBLEMS IN T-SPICE2A, THE PROGRAM T-SPICE2B MAY BE USED. TYPICALLY THE
COST OF SIMULATION ASSOCIATED WITH T-SPICE2A IS ONE HALF OF THAT ASSOCIATED
WITH T-SPICE2B.

T-SPICE USES DYNAMIC MEMORY MANAGEMENT TO STORE ELEMENTS, MODELS, AND
OUTPUT VALUES. THUS, THE ONLY LIMITATION IMPOSED BY THE PROGRAM ON THE SIZE OR
THE COMPLEXITY OF THE CIRCUIT TO BE SIMULATED IS THAT ALL NECESSARY DATA FIT
IN MEMORY. THE AMOUNT OF MEMORY SPACE REQUIRED FOR SIMULATION DEPENDS ON THE
SIZE OF THE CIRCUIT AND THE TOTAL NUMBER OF THERMAL NODES THAT WILL BE CREATED
BY THE PROGRAM. THE TOTAL NUMBER OF THERMAL NODES THAT WILL BE CREATED BY THE
PROGRAM IS A STRONG FUNCTION OF THE DISCRETE NUMBER OF X AND Y COORDINATES. IN
ORDER TO MINIMIZE THE COST OF SIMULATION CARE SHOULD BE TAKEN SO AS TO LIMIT
THE DISCRETE NUMBER OF X AND Y COORDINTAES WITHIN 15 EACH. FOR EXAMPLE A 50
POINT DC TRANSFER CURVE ANALYSIS OF THE UA741 OPERATIONAL AMPLIFIER WITH 15
DISCRETE X COORDINATES AND 15 DISCRETE Y COORDINATES REQUIRES APPROXIMATELY

110000(OCTAL) WORDS. IF IN RUNNING EITHER OF THESE PROGRAMS, THE MEMORY NEEDED FOR ANALYSIS EXCEEDS THE MAXIMUM MEMORY AVAILABLE AN AUXILLIARY PROGRAM T-SPICE2C IS AVAILABLE. SEE THE DESCRIPTION OF T-SPICE2C AT THE END OF THIS MANUAL.

AS FAR AS THE INPUT DATA IS CONCERNED THREE PROGRAMS HAVE THE SAME FORMAT. WHENEVER THE TERMINOLOGY T-SPICE IS USED IT IS UNDERSTOOD TO MEAN ALL THREE PROGRAMS UNLESS OTHERWISE INDICATED. INPUT FORMAT OF T-SPICE IS QUITE SIMILAR TO THAT OF SPICE2. THE ADDITION OVER AND ABOVE THE STANDARD SPICE2 DECK INCLUDE X AND Y LOCATIONS OF EACH DEVICE WRITTEN IN THE ELEMENT CARD ITSELF AND SINGLE THERMAL CARD WHICH SPECIFIES THERMAL DATA REQUIRED. THIS USER'S GUIDE SHOULD BE USED WITH THAT OF SPICE2. ONLY THE PORTION OF THE INPUT FORMAT THAT IS UNIQUE TO T-SPICE IS DESCRIBED HERE.

ELEMENT CARD

WHEN X AND Y COORDINATES ARE NOT SPECIFIED, THAT TLEMENT IS CONSIDERED OFF CHIP AND RESIDES AT AMBIENT TEMPERATURE.

*****RESISTORS

```
GENERAL FORM: RXX N1 N2 VAL   TC=TC1   X=X1    Y=Y1
EXAMPLE:      R1  1  2  100K  TC=1M    X=12.5  Y=13.5
```

TC IS THE TEMPERATURE COEFFICIENT OF THE RESISTOR. X AND Y INDICATE THE RESISTOR LOCATION AS MEASURED FROM THE LOWER LEFT CORNER OF A RECTANGULAR CHIP. THE VALUE OF THE RESISTOR AS A FUNCTION OF TEMPERATURE IS GIVEN BY:

```
VALUE(T)=VALUE(27.0)*(1.0+TC*(T-27.0))
WHERE T IS IN DEGREE-C.
```

IF TC IS NOT SPECIFIED, DEFAULT IS TC=0.0

*****ZENER DIODES

```
GENERAL FORM:  ZXX  N1  N2  VAL  TC=TC1  X=X1    Y=Y1
EXAMPLE :      Z1   2   4   6.3  TC=2M   X=18.0  Y=12.8
```

N1 AND N2 ARE TWO ELEMENT NODES. VAL IS THE VOLTAGE DROP ACROSS THE ZENER FROM N1 TO N2. TC IS THE TEMPERATURE COEFFICIENT OF THE ZENER

VOLTAGE IN UNIT OF V/DEG-C. X AND Y INDICATE THE DEVICE LOCATION OF THE ZENER DIODES.

```
VAL(T)=VAL(27.0)+TC*(T-27.0)
```

IF TC IS NOT SPECIFIED, DEFAULT IS TC=0.0

*****BJT

```
GENERAL FORM:  QXX  NC  NB  NE  MNAME  AREA  X=X1    Y=Y1
EXAMPLE :      Q13  4   3   1   MODN   2.5   X=23.5  Y=16.2
```

X AND Y INDICATE THE DEVICE LOCATION.

JFET, DIODE, AND MOS DEVICES ARE NOT TREATED AS YET IN T-SPICE.

*****BJT MODEL

IS, RB,RC,AND RE ARE CONSIDERED TEMPERATURE DEPENDENT AND MODELLED AS FOLLOWS:

```
IS=I0*T↑(PT/N)*EXP(-EG/KT)
RC(T)=RC(27.0)*(1.0+TC1C*(T-27.0))
RB(T)=RB(27.0)*(1.0+TC1B*(T-27.0))
RE(T)=RE(27.0)*(1.0+TC1E*(T-27.0))
```

TC1C,TC1B, AND TC1E ARE TEMPERATURE COEFFICIENTS OF THE COLLECTOR, BASE EMITTER RESISTANCES. IF LEFT UNSPECIFIED, THEY ARE CONSIDERED TEMPERATURE INDEPENDENT. T IS IN DEG-C.

*****.THRML CARD

THIS CARD SPECIFIED THE THERMAL DATA REGARDING THE DIE/PACKAGE STRUCTURE.

```
GENERAL FORM: .THRMAL LX=VAL1 LY=VAL2 LXHDR=VAL3 LYHDR=VAL4 AO=VAL5
              BO=VAL6 KS=VAL7 KH=VAL8 GH=VAL9 TCS=VAL10 TCH=VAL11
```

```
EXAMPLE: LX=50 LY=50 A0=10 B0=10 KS=.00223 KH=.00045 GH=.01
         +TCS=27.0E-9 TCH=27.0E-9 LXHDR=200.0 LYHDR=200.0
```

NOTE THE VALUES OF LX AND LY MUST BE SPECIFIED. THE OTHER PARAMETERS ARE DEFAULTED AS INDICATED IN THE EXAMPLE.

LX,LY:THE LENGTH OF THE RECTANGULAR CHIP IN X AND Y DIRECTIONS(MIL)
A0,B0: THE THICKNESS OF CHIP AND HEADER (MIL)
LXHDR,LYHDR: THE LENGTH OF THE RECTANGULAR HEADER IN X AND Y DIRECTIONS (MIL)
KS,KH: THERMAL CONDUCTIVITY OF CHIP AND HEADER IN (MW/DEG-C-MIL)
TCS,TCH: THERMAL CAPACITANCE OF CHIP AND HEADER IN (MW-SEC)/(DEG-C-MIL+3)
GH:JUNCTION TO AMBIENT THERMAL CONDUCTANCE IN (W/DEG-C)

*****.DC CARD

T-SPICE ALLOWS THE AMBIENT TEMPERATURE TO BE VARIED.

```
GENERAL FORM: .DC TAMB TMIN TMAX TDELTA
EXAMPLE:      .DC TAMB -50  100  10
```

TMIN IS THE STARTING AMBIENT TEMPERATURE IN DEG-C. TMAX IS THE FINAL TEMPERATURE IN DEG-C. TDELTA IS THE TEMPERATE STEP IN DEG-C. FOR THE DC TRANSFER CURVE COMPUTATION OF OPERATIONAL AMPLIFIERS, A NEGATIVE FEED-BACK CONFIGURATION MUST BE USED. THIS IS ESSENTIAL BECAUSE MOST OPERATIONAL AMPLIFIERS SUFFER FROM THERMAL FEEDBACK EFFECTS AND CONSEQUENTLY THE OUTPUT BECOMES MULTI-VALUED FUNCTION OF DIFFERENTIAL INPUT VOLTAGE.

*****.PRINT/.PLOT CARD

T-SPICE ALLOWS THE TEMPERATURES OF ANY DEVICE ON A CHIP OR TEMPERATURE DIFFERENCES BETWEEN AY TWO DEVICES TO BE PRINTED OR PLOTTED AS A FUNCTION OF INPUT VOLTAGE OR AMBIENT TEMPERATURE FOR THE CASE OF THE DC TRANSFER CURVE AND TIME FOR THE CASE OF TRNASIENT ANALYSIS.


```
GENERAL FORM : .PRINT PRTYPE V(N1) V(N1,N2) T(NAME1,NAME2)
EXAMPLE:       .PRINT DC V(1) V(2,4) T(Q1,Q2) T(Z1,R2)
```

PRTYPE IS THE TYPE OF THE ANALYSIS(DC OR TRAN)
T(NAME1,NAME2) SPECIFIES THE TEMPERATURE DIFFERENCE BETWEEN DEVICES NAMED NAME1 AND NAME2.

*****.TRAN CARD

IN THE TRANSIENT ANALYSIS OF A ELECTRO-THERMAL INTERACTIONS IT IS STRONGLY RECOMMENDED THAT ALL THE ELECTRICAL ENERGY STORAGE ELEMENTS BE REMOVED FROM THE INPUT. THE INCLUSION WILL RESULT IN A VERY EXPENSIVE SIMULATION. IF ONE IS INTERESTED IN THE CIRCUIT TRANSIENT BEHAVIOR THAT TAKES PLACE IN THE ORDER OF THERMAL TIME CONSTANTS THE INCLUSION OF ELECTRICAL ENERGY STORAGE ELEMENT WHOSE TIME CONSTANT IS MUCH SMALLER THAN THE THERMAL TIME CONSTANTS WILL BE MEANINGLESS.

*****.OPTION CARD

OPTION	EFFECT
TROOM=X	X IS THE AMBIENT ROOM TEMPERATURE. DEFAULT IS 27.0DEG-C.
TOP=X	X IS THE GUESS FOR THE OPERATING TEMPERATURE OF ALL THE DEVICES. IN SOME CASES THE SPECIFICATION HELPS THE NUMERICAL CONVERGENCE. THE SPECIFICATION IS CRITICAL FOR TEMPERATURE STABILIZED SUBSTRATE CIRCUITS. IN GENERAL IT IS NOT NECESSARY TO SPECIFY. DEFAULT IS 27.0DEG-C.
PDMAX=X	X IS THE MAXIMUM POWER DISSIPATION FROM ANY DEVICE ON A CHIP. IN T-SPICE2B A PROPER SPECIFICATION OF THIS VALUE AIDS A FAST CONVERGENCE.
ISKIP=N	THIS OPTION SPECIFICATION DOES NOT HAVE ANY EFFECT ON T-SPICE2A. IN T-SPICE2B IF N=1 THE JUNCTION INITIALIZING SCHEME WILL BE SKIPPED. THIS OPTION SHOULD BE USED ONLY IN THE TEMPERATURE STABILIZED SUBSTRATE CIRCUITS.
IGRID=N	IF N=1, IT INDICATES THE PRESENCE OF THE DECK FOLLOWING THE .END CARD THAT CONTAINS DATA REGARDING THE THERMAL

```
                NETWORK FORMED BY T-SPICE2C. CONSEQUENTLY THIS ADDITIONAL
                DECK IS READ IN AND THE THERMAL NETWORK FORMATION ROUTINE
                IS SKIPPED. IF N=0 THE THERMAL NETWORK FORMATION
                ROUTINE BUILT IN T-SPICE2A,AND B WILL BE CALLED AND USED.
                DEFAULT IS N=0.
   IDBUG1=N     IF N=1 THE PROGRAM WILL PRINT OUT THE THE PROCESS OF
                THERMAL NETWORK FORMATION.
   IDBUG2=N     IF N=1 THE PROGRAM WILL PRINT OUT THE FINAL STEPS OF
                THERMAL NETWORK FORMATION PROCESS.
   IDBUG3=N     IF N=1 THE PROGRAM PRINTS OUT THE ACTUAL EVALUATION
                PROCESS OF THERMAL RESISTANCES AND CAPACITANCES.
   IDBUG4=N     IF N=1 THE PROGRAM PRINTS OUT THE PROCESS OF SETUP.
   IDBUG5=N     IF N=1 THE PROGRAM PRINTS OUT THE SOLUTION OF CIRCUIT
                AFTER EVERY ITERATION.
   IDBUG6=N     IF N=1 THE PROGRAM PRINTS OUT THE SOLUTION AFTER EVERY
                FUNCTIONAL ITERATION (APPLICABLE ONLY TO T-SPICE2A)
   IDBUG7=N     IF N=1 THE PROGRAM PRINTS OUT THE SOLUTION AT THE
                END OF EVERY DC POINT OR TIME POINT.
   IDBUG8=N     IF N=1 THE PROGRAM PRINTS OUT THE LINEARIZED BJT
                PARAMETER AT EVERY ITERATION.
```


APPENDIX A: EXAMPLE DATA DECK

THE FOLLOWING DECK DETERMINES THE DC TRANSFER CURVE OF A SIMPLE ACTIVE LOAD DIFFERENTIAL AMPLIFIER AS THE AMBIENT TEMPERATURE IS VARIED FROM 30 DEGREE-C TO 100 DEGREE-C WITH TEMPERATURE STEP OF 10 DEGREE-C.

```
SIMPLE ACTIVE LOAD DIFFERENTIAL AMPLIFIER
Q1 4 2 3 MODN                   X=10.0     Y=10.0
Q2 5 0 3 MODN                   X=30.0     Y=10.0
Q3 4 4 6 MODP                   X=30.0     Y=30.0
Q4 L K M MODN                   X=22.0     Y=22.0
RL 7 0 100K
Z1 6 8 7.3 TC=3.0E-03           X=40.0     Y=18.666
RS 8 0 500.0
IEE 3 0 2.0M
VCC 6 0 15.0
.MODEL MODN NPN BF=100.0 IS=1.E-18 VA=100.
.MODEL MODP PNP BF=100. IS=1.E-18 VA=[illegible]0.0
VIN 2 0 0.0
.PRINT DC V(7)
.PLOT DC V(7)
.PLOT DC T(Q1,Q2)
.DC TAMB 30 100 10
.OP
.THRML LX=40. LY=40. A0=10. B0=10. KS=.00223 KH=.0002 GH=.01
+TCS=27.7E-9 TCH=30.0E-09 LXHDR=100. LYHDR=100.
.OPTION ACCT TROOM=27.0 TOP=28.0 PDMAX=.2 IDBUG7=1
.END
```

THE FOLLOWING DECK DETERMINES THE DC TRANSFER CURVE OF A COMMERCIALLY AVAILABLE 741 OPERATIONAL AMPLIFIER. NOTICE THAT IGRID IS NOT SPECIFIED IN THE OPTION CARD. THUS THE ROUTINE BUILT IN TO T-SPICE2A,B WILL BE USED.

```
DC TRANSFER CURVE OF FAIRCHILD 741
Q1 10 1 3 MODN                  X=37.5     Y=8.0
Q2 10 2 4 MODN                  X=34.5     Y=8.
Q3 5 11 3 MODP                  X=32.5     Y=12.8
Q4 9 11 4 MODP                  X=26.0     Y=12.8
Q5 5 6 7 MODN                   X=39.2     Y=16.5
Q6 9 6 8 MODN                   X=46.0     Y=16.5
Q7 23 5 6 MODN                  X=32.5     Y=22.5
Q8A 10 10 23 MODP .2            X=13.0     Y=6.5
```

```
Q9B 10 10 23 MODP .8                X=26.0    Y=6.5
Q9A 11 10 23 MODP .4                X=32.5    Y=6.5
Q9B 11 10 23 MODP .6                X=26.0    Y=6.5
Q10 11 12 14 MODN                   X=39.2    Y=22.5
Q11 12 12 24 MODN                 X=45.0    Y=28.0
Q12 13 13 23 MODP                   X=8.0     Y=6.5
Q13A 15 13 23 MOD1                  X=8.0     Y=12.8
Q13B 17 13 23 MOD2                 X=8.0     Y=12.8
Q14 23 17 20 MODA                  X=13.0    Y=47.0
Q15A 17 20 21 MODN .35              X=32.5    Y=38.0
Q15B 17 20 21 MODN .65              X=26.0    Y=38.0
Q16 23 9 16 MODN                  X=37.5    Y=28.0
Q17A 15 16 25 MODN .35                X=45.0    Y=28.0
Q17B 15 16 25 MODN .65               X=41.0    Y=28.0
Q18A 17 18 19 MODN .75              X=32.5    Y=31.3
Q18B 17 18 19 MODN .25             X=26.0    Y=31.3
Q19A 17 17 18 MODN .65             X=26.0    Y=31.3
Q19B 17 17 18 MODN .35              X=32.5    Y=31.3
Q20 24 19 22 MODP                 X=41.0    Y=47.0
Q21 26 22 21 MODP                    X=26.0    Y=47.0
Q22 9 26 24 MODN                    X=41.0    Y=38.0
Q23A 24 15 9 MOD3                   X=37.5    Y=38.0
Q23B 24 15 19 MOD4                  X=37.5    Y=31.3
Q24A 26 26 24 MODN .25              X=32.5    Y=38.0
Q24B 26 26 24 MODN .75              X=32.5    Y=47.0
R1 7 24 1K
R2 6 24 50K
R3 8 24 1K
R4 14 24 3K
R5 13 12 39K
R6 20 21 27
R7 21 22 22.0
R8 25 24 100.0
R9 16 24 50K
R10 18 19 40K
R11 26 24 50K
RFB1 21 2 100K
RFB2 2 30 50.0
RL 21 0 1.0K
VIN1 1 0 0.0
VCC 23 0 15.0
VEE 24 0 -15.0
VIN 0 30 -8M
.MODEL MODN NPN IS=1.E-14 VA=100
.MODEL MODP PNP IS=1.E-14 VA=75.0
.MODEL MOD1 PNP IS=2.25E-15 VA=75
.MODEL MOD2 PNP IS=.9E-15 VA=75.
.MODEL MOD3 PNP IS=.0063E-15 VA=75
```



```
.MODEL MOD4 PNP IS=.79E-15 VA=75
.MODEL MODA NPN IS=1.E-14  VA=100 BF=200
.THRML LX=55 LY=55 A0=10 B0=10 KS=2.23E-03 KH=4.5E-04 GH=1.E-02
+TCS=.02 TCH=.02 LXHDR=110 LYHDR=110
.PRINT DC V(2) V(21)
.PRINT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.PLOT DC V(2) (-.4M,.4M) V(21)
.PLOT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.DC VIN -8M 6.4M .4M
.OPTION ACCT IDBUG7=1 PDMAX=.15
.END
```

THE FOLLOWING DECK DETERMINES THE TRANSIENT RESPONSE OF A COMMONLY USED VOLTAGE REGULATOR. NOTICE IN THIS CASE IGRID=1 IS SPECIFIED IN THE OPTION CARD. THE PORTION OF INPUT DATA FOLLOWING .END CARD IS OBTAINED BY RUNNING T-SPICE2C.

```
TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL     NEWTON-RAPHSON
Q1 3 2 4 MODN 2.25                  X=5.00      Y=16.8
Q2 4 5 6 MODN 2.0                   X=12.2      Y=14.6
Q3 7 6 0 MODN 6.0                   X=20.0      Y=11.3
Q4 8 7 10 MODN 6.0                  X=26.0      Y=11.30
Q5 9 10 11 MODN 7.0                 X=35.6      Y=11.3
Q6 17 2 8 MODN 2.25                 X=51.0 Y=10.0
Q7 12 9 13 MODN 2.25                X=40.8      Y=11.3
Q8 12 13 0 MODN 2.25                X=43.3      Y=11.3
Q9 14 14 0 MODN 2.25                X=48.0      Y=6
Q10 0 12 15 MODVP 6.15              X=62.0      Y=27.3
Q11 16 3 1 MODLP 3.0                X=50.7      Y=21.0
Q12 3 3 1 MODLP 3.0                 X=46.4      Y=21.0
Q15 1 16 17 MODN 17.5               X=77.4      Y=42.0
Q1601 1 17 18 MODN 18.0             X=9.3       Y=42.0
Q1603 1 17 20 MODN 18.0             X=15.8      Y=42.0
Q1605 1 17 22 MODN 18.0             X=22.5      Y=42.0
Q1607 1 17 24 MODN 18.0             X=29.0      Y=42.0
Q1609 1 17 26 MODN 18.0             X=35.6      Y=42.0
Q1611 1 17 28 MODN 18.0             X=51.0      Y=42.0
Q1613 1 17 30 MODN 18.0             X=57.5      Y=42.0
Q1615 1 17 32 MODN 18.0             X=64.1      Y=42.0
Q1617 1 17 34 MODN 18.0             X=70.8      Y=42.0
R1 3 4 30K                          X=10.0      Y=21.0
R2 4 5 1.9K                         X=7.5       Y=11.0
R3 5 7 26.0                         X=16.4      Y=11.0
R4 6 0 1.2K                         X=20.5      Y=8.5
R5 10 0 12.1K                       X=39.0      Y=7.0
```

```
R6 11 0 1K                              X=38.0     Y=4.7
R7 8 9 17.7K                            X=28.0     Y=7.0
R8 13 14 4K                             X=48.0     Y=6.0
R9 15 12 4K                             X=53.5     Y=16.0
R10 16 15 850                           X=55.0     Y=20.0
R15 17 2 2K                             X=25.0     Y=26.5
R1601 18 2 3.5                          X=9.3      Y=42.0
R1603 20 2 3.5                          X=15.8     Y=42.0
R1605 22 2 3.5                          X=22.5     Y=42.0
R1607 24 2 3.5                          X=29.0     Y=42.0
R1609 26 2 3.5                          X=35.6     Y=42.0
R1611 28 2 3.5                          X=51.0     Y=42.0
R1613 30 2 3.5                          X=57.5     Y=42.0
R1615 32 2 3.5                          X=64.1     Y=42.0
R1617 34 2 3.5                          X=70.8     Y=42.0
R18 2 0 2.67K                           X=69.0     Y=6.7
VCC 1 0 10
.MODEL MODN NPN BF=100 IS=1.E-15 RB=300 RC=260 VA=200 PE=.65 ME=.5 PC=.5 MC=.3
.MODEL MODLP PNP BF=15 IS=1.5E-15 RB=200 RC=25 RE=270 VA=50 PE=.65 ME=.3 PC=.5
+ MC=.3
.MODEL MODVP PNP BF=50 IS=1.5E-15 RB=100 RC=100 RE=270 VA=80 PE=.65 ME=.3 PC=.5
+ MC=.3
IOUT 2 0 PULSE(1M 1.5 0US 10US 10US 10MS 20MS)
.PRINT TRAN V(2) V(8,9) V(11)
.PRINT TRAN V(5,6) V(6) V(7,10) V(10,11) V(2,8) V(9,13) V(13)
.PRINT TRAN T(Q3) T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.PLOT TRAN V(2) V(9) V(7) V(11)
.PLOT TRAN T(Q3) T(Q2) T(Q2,Q3)
.PLOT TRAN T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.TRAN 100US 10MS
.THRML LX=86 LY=58 A0=7 B0=100 KS=.00223 KH=0.00800 GH=.02857
+TCS=27.7E-9 TCH=56.33E-9 LXHDR=500.0 LYHDR=500.0
.OPTION ACCT PDMAX=2.0 IDBUG7=1 IGRID=1
.END
  26   88
  38     1.58000E+01     5.80000E+01
  39     2.90000E+01     5.80000E+01
  40     4.35000E+01     5.80000E+01
  41     5.75000E+01     5.80000E+01
  42     7.08000E+01     5.80000E+01
  43     8.60000E+01     3.87000E+01
  44     8.60000E+01     2.00000E+01
  45     6.90000E+01     0.
  46     6.30000E+01     0.
  47     5.60000E+01     0.
  48     1.58000E+01     3.60000E+01
  49     2.28000E+01     3.58000E+01
  50     3.20000E+01     3.60000E+01
```



```
  51     4.00000E+01     3.40000E+0
  52     1.00000E+01     3.00000E+01
  53     1.77000E+01     2.58000E+01
  54     3.80000E+01     3.00000E+01
  55     5.00000E+01     2.60000E+01
  56     5.45000E+01     2.65000E+01
  57     7.08000E+01     2.73000E+01
  58     6.22000E+01     2.08000E+01
  59     6.20000E+01     1.42000E+01
  60     4.79000E+01     1.59000E+01
  61     4.20000E+01     1.70000E+01
  62     3.57000E+01     1.77000E+01
  63     2.83000E+01     1.43000E+01
  64     2.07000E+01     1.62000E+01
  65     1.64000E+01     1.62000E+01
  66     1.22000E+01     8.50000E+00
  67     1.73000E+01     8.20000E+00
  68     3.34000E+01     7.50000E+00
  69     4.13000E+01     3.90000E+00
  70     4.26000E+01     6.20000E+00
  71     4.60000E+01     1.90000E+00
  72     5.60000E+01     2.00000E+00
  73     9.90000E+00     3.61000E+01
  74     0.              3.80000E+01
  75     0.              3.00000E+01
  76     0.              1.60000E+01
  77     2.00000E+00     1.00000E+01
  78     0.              1.00000E+01
  79     7.20000E+00     0.
  80     1.60000E+01     0.
  81     2.00000E+01     0.
  82     3.00000E+01     0.
  83     4.02000E+01     0.
  84     4.60000E+01     0.
  85     6.00000E+01     7.50000E+00
  86     7.30000E+01     1.58000E+01
  87     8.33081E+01     3.20143E+01
  88     8.60000E+01     3.20143E+01
   1   74    2   75    3   76    4   78    5   34    6   79    7   80    8   81    9   82   10    8
  11   84   12   47   13   46   14   45   15   35   16   44   17   88   18   43   19   36   20    4
  21   41   22   40   23   39   24   38   25   37   26   74
   6    5    5    5    6    5    5    5    6    5
   7    5    5    6    5    6    7    5    6    4
   6    6    6    6    6    5    6    6    6    5
   6    5    6    3    4    3    3    5    5    4
   5    5    4    5    3    5    4    6    6    6
   5    5    7    7    6    7    8    6    6    6
   6    6    6    6    6    6    6    7    5    6
```

7	6	6	4	6	4	6	3	5	4
5	5	5	3	6	6	5	3		
65	23	53	52	22	75				
23	66	22	79	77					
24	67	65	66	23					
7	25	81	24	67					
28	26	70	69	6	68				
69	5	68	83	82					
25	68	82	4	81					
71	70	29	27	72					
60	31	27	85	10	59				
9	31	56	59	58					
63	64	62	54	53	50	49			
13	73	74	36	37					
14	48	73	12	38					
15	49	48	13	38	39				
16	50	49	14	39					
51	50	17	15	39	40				
55	51	56	16	18	40	41			
56	17	30	19	41					
30	18	57	20	41	42				
57	19	33	42						
46	85	59	86	45	35				
1	23	2	75	77	76				
65	3	66	1	2	22				
25	4	64	67	3	65				
68	63	7	4	24	64				
28	62	5	68	63					
8	29	60	72	9	85				
61	62	29	26	5	70				
61	28	70	8	27	60				
58	56	18	57	19					
60	32	9	55	10	56				
60	61	54	31	55					
57	20	87	43	42	36				
77	79	78							
45	21	86	44						
33	42	43							
38	12	74							
12	13	14	39	37					
14	38	15	16	40					
16	39	17	41						
17	40	18	19	42					
19	41	20	33	36					
33	87	88	36						
35	86	57	87	88					
21	46	35							
72	85	47	21	45					

71	72	84	46				
49	53	52	14	73	13		
50	11	53	15	48	14		
54	11	51	49	16	15		
55	54	17	50	16			
48	53	1	75	73			
11	64	65	49	1	48	52	
62	11	61	32	55	51	50	
31	32	54	56	51	17		
31	55	10	58	17	30	18	
58	30	86	19	44	20	33	87
59	10	56	86	30	57		
85	9	10	58	21	86		
27	29	61	32	31	9		
62	28	29	60	54	32		
61	28	26	63	11	54		
62	26	68	25	64	11		
25	24	63	11	65	53		
64	24	3	53	23	1		
3	67	80	23	2	79		
4	81	24	3	80	66		
26	5	6	63	25	82	7	
70	5	6	83	71			
5	28	29	69	71	8		
83	69	70	8	72	84	47	
8	27	71	47	85	46		
48	52	75	13	12	74		
73	75	12	37				
52	1	22	73	76	74		
22	77	75	78				
22	2	79	76	78	34		
77	76	34					
66	80	2	77	34			
81	67	66	79				
7	82	4	67	80			
68	6	83	7	81			
69	6	82	71	84			
83	71	47					
72	27	9	46	59	21		
21	59	58	57	35	44		
44	57	33	43	88			
44	87	43					

T-SPICE2C IS AN AUXILIARY PROGRAM AND FORMS A THERMAL NETWORK IN A MANNER QUITE DIFFERENT FROM THE ROUTINE IN T-SPICE2A AND T-SPICE2B. THE TOTAL NUMBER OF THERMAL NODES CREATED BY THIS PROGRAM IS TYPICALLY SMALLER THAN THAT OF T-SPICE2A AND T-SPICE2B. IN ORDER TO USE T-SPICE2C A USER MUST ENTER THE NUMBER OF EXTRA THERMAL NODES AND THEIR LOCATIONS THAT ARE CREATED BY THE USER IN SUCH A WAY THAT NONE OF THE INNER ANGLES OF TRIANGLES IN THE ASYMMETRICAL TRIANGULAR THERMAL NETWORK ARE OBTUSE. THE RESULTING DATA IS PUNCHED INTO CARDS. THE PUNCHED DECK MUST BE PLACED AFTER THE .END CARD IN T-SPICE2A OR T-SPICE2B AND IGRID=1 MUST BE SPECIFIED IN THE OPTION CARD FOR ACTUAL ANALYSIS. THE SEQUENCE OF THE ORIGINAL INPUT DECK MUST NOT BE CHANGED BECAUSE THE THREE PROGRAMS DEFINE THE THERMAL NODE NUMBER OF ALL THE DEVICES ON THE CHIP IN A SEQUENCE IN WHICH THE INPUT DECK HAS BEEN READ IN. THE ADDITIONAL DATA MUST BE ENTERED IN A FIXED FORMAT AS SHOWN BELOW. FOR AN INSTRUCTION ON HOW TO FORM THIS TRIANGULAR THERMAL NETWORK SEE THE ERL REPORT.

THE FOLLOWING IS AN EXAMPLE ON THE USE OF T-SPICE2C. NOTICE THE PART OF INPUT DATA FOLLOWING .END CARD IS THE ADDITIONAL INFORMATION NECESSARY TO CREATE A THERMAL NETWORK. THE FIRST CARD FOLLOWING .END CARD DEFINES THE NUMBER OF ADDITIONAL NODES CREATED BY A USER. THE REMAINING DATA ARE USED TO DEFINE THE LOCATIONS OF THOSE USER CREATED THERMAL NODES LOCATIONS. THUS THE NUMBER OF THESE CARDS MUST BE EQUAL TO WHAT IS SPECIFIED BY THE FIRST CARD FOLLOWING .END.

```
TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL     NEWTON-RAPHSON
Q1 3 2 4 MODN 2.25                X=5.00     Y=16.8
Q2 4 5 6 MODN 2.0                 X=12.2     Y=14.6
Q3 7 6 0 MODN 6.0                 X=20.0     Y=11.3
Q4 8 7 10 MODN 6.0                X=26.0     Y=11.30
Q5 9 10 11 MODN 7.0               X=35.6     Y=11.3
Q6 17 2 8 MODN 2.25               X=51.0 Y=10.0
Q7 12 9 13 MODN 2.25              X=40.8     Y=11.3
Q8 12 13 0 MODN 2.25              X=43.5     Y=11.3
Q9 14 14 0 MODN 2.25              X=48.0     Y=6
Q10 0 12 15 MODVP 6.15            X=62.0     Y=27.3
Q11 16 3 1 MODLP 3.0              X=60.7     Y=21.0
Q12 3 3 1 MODLP 3.0               X=46.4     Y=21.0
Q15 1 16 17 MCON 17.5             X=77.4     Y=42.0
Q1601 1 17 18 MODN 18.0           X=9.3      Y=42.0
Q1603 1 17 20 MODN 18.0           X=15.8     Y=42.0
Q1605 1 17 22 MODN 18.0           X=22.5     Y=42.0
Q1607 1 17 24 MODN 18.0           X=29.0     Y=42.0
Q1609 1 17 26 MODN 18.0           X=35.6     Y=42.0
Q1611 1 17 28 MODN 18.0           X=51.0     Y=42.0
Q1613 1 17 30 MODN 18.0           X=57.5     Y=42.0
Q1615 1 17 32 MODN 18.0           X=64.1     Y=42.0
```



```
Q1617 1 17 34 MODN 18.0           X=70.8     Y=42.0
R1 3 4 30K                        X=10.0     Y=21.0
R2 4 5 1.9K                       X=7.5      Y=11.0
R3 5 7 26.0                       X=16.4     Y=11.0
R4 6 0 1.2K                       X=20.5     Y=8.5
R5 10 0 12.1K                     X=39.0     Y=7.0
R6 11 0 1K                        X=38.0     Y=4.7
R7 8 9 17.7K                      X=25.0     Y=7.0
R8 13 14 4K                       X=48.0     Y=6.0
R9 15 12 4K                       X=53.5     Y=16.0
R10 16 15 850                     X=56.0     Y=20.0
R15 17 2 2K                       X=25.0     Y=26.5
R1601 18 2 3.5                    X=9.3      Y=42.0
R1603 20 2 3.5                    X=15.8     Y=42.0
R1605 22 2 3.5                    X=22.8     Y=42.0
R1607 24 2 3.5                    X=29.0     Y=42.0
R1609 26 2 3.5                    X=35.6     Y=42.0
R1611 28 2 3.5                    X=51.0     Y=42.0
R1613 30 2 3.5                    X=57.6     Y=42.0
R1615 32 2 3.5                    X=64.1     Y=42.0
R1617 34 2 3.5                    X=70.8     Y=42.0
R18 2 0 2.67K                     X=69.0     Y=6.7
VCC 1 0 10
.MODEL MODN NPN BF=100 IS=1.E-15 RB=300 RC=260 VA=200 PE=.65 ME=.5 PC=.5 MC=.3
.MODEL MODLP PNP BF=15 IS=1.5E-15 RB=200 RC=25 RE=270 VA=60 PE=.65 ME=.3 PC=.5
+ MC=.3
.MODEL MODVP PNP BF=50 IS=1.5E-15 RB=100 RC=100 RE=270 VA=80 PE=.65 ME=.3 PC=.5
+ MC=.3
IOUT 2 0 PULSE(1M 1.5 0US 10US 10US 10MS 20MS)
.PRINT TRAN V(2) V(8,9) V(11)
.PRINT TRAN V(5,6) V(6) V(7,10) V(10,11) V(2,8) V(9,13) V(13)
.PRINT TRAN T(Q3) T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.PLOT TRAN V(2) V(9) V(7) V(11)
.PLOT TRAN T(Q3) T(Q2) T(Q2,Q3)
.PLOT TRAN T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.TRAN 100US 10MS
.THRML LX=86 LY=58 A0=7 B0=100 KS=.00223 KH=0.00800 GH=.02857
+TCS=27.7E-9 TCH=56.33E-9 LXHDR=500.0 LYHDR=500.0
.OPTION ACCT PDMAX=2.0 IDBUG7=1 IGRID=1
.END
49
+1.580E+01+5.800E+01
+2.900E+01+5.800E+01
+4.350E+01+5.800E+01
+5.750E+01+5.800E+01
+7.080E+01+5.800E+01
+8.600E+01+3.870E+01
+8.600E+01+2.000E+01
```

```
+6.900E+01+0.000E+00
+6.300E+01+0.000E+00
+5.600E+01+0.000E+00
+1.580E+01+3.600E+01
+2.280E+01+3.580E+01
+3.200E+01+3.600E+01
+4.000E+01+3.400E+01
+1.000E+01+3.000E+01
+1.770E+01+2.580E+01
+3.800E+01+3.000E+01
+5.000E+01+2.600E+01
+5.450E+01+2.650E+01
+7.080E+01+2.730E+01
+6.220E+01+2.080E+01
+6.200E+01+1.420E+01
+4.790E+01+1.590E+01
+4.200E+01+1.700E+01
+3.570E+01+1.770E+01
+2.830E+01+1.430E+01
+2.070E+01+1.620E+01
+1.640E+01+1.620E+01
+1.220E+01+8.500E+00
+1.730E+01+8.200E+00
+3.340E+01+7.500E+00
+4.130E+01+3.900E+00
+4.260E+01+6.200E+00
+4.600E+01+1.900E+00
+5.600E+01+2.000E+00
+9.900E+00+3.610E+01
+0.000E+00+3.800E+01
+0.000E+00+3.000E+01
+0.000E+00+1.600E+01
+2.000E+00+1.000E+01
+0.000E+00+1.000E+01
+7.200E+00+0.000E+00
+1.600E+01+0.000E+00
+2.000E+01+0.000E+00
+3.000E+01+0.000E+00
+4.020E+01+0.000E+00
+4.600E+01+0.000E+00
+6.000E+01+7.500E+00
+7.300E+01+1.580E+01
```

THE FOLLOWING SHOWS THE RESULTANT PUNCHED DECK. IN ORDER TO ACTUALLY SIMULATE THE CIRCUIT PERFORMANCE THIS PUNCHED DECK MUST BE ATTACHED TO THE ORIGINAL INPUT DECK FOLLOWING .END CARD IN EITHER T-SPICE2A OR T-SPICE2B. NOTICE THE FOLLOWING PUNCHED DECK WAS USED IN THE EXAMPLE CIRCUIT OF VOLTAGE REGULATOR MENTIONED EARLIER.


```
26   88
38     1.58000E+01      5.80000E+01
39     2.90000E+01      5.80000E+01
40     4.35000E+01      5.80000E+01
41     5.75000E+01      5.80000E+01
42     7.08000E+01      5.80000E+01
43     8.60000E+01      3.87000E+01
44     8.60000E+01      2.00000E+01
45     6.90000E+01      0.
46     6.30000E+01      0.
47     5.60000E+01      0.
48     1.58000E+01      3.60000E+01
49     2.28000E+01      3.58000E+01
50     3.20000E+01      3.60000E+01
51     4.00000E+01      3.40000E+01
52     1.00000E+01      3.00000E+01
53     1.77000E+01      2.58000E+01
54     3.80000E+01      3.00000E+01
55     5.00000E+01      2.60000E+01
56     5.45000E+01      2.65000E+01
57     7.08000E+01      2.73000E+01
58     6.22000E+01      2.08000E+01
59     6.20000E+01      1.42000E+01
60     4.79000E+01      1.59000E+01
61     4.20000E+01      1.70000E+01
62     3.57000E+01      1.77000E+01
63     2.83000E+01      1.43000E+01
64     2.07000E+01      1.62000E+01
65     1.64000E+01      1.62000E+01
66     1.22000E+01      8.50000E+00
67     1.73000E+01      8.20000E+00
68     3.34000E+01      7.50000E+00
69     4.13000E+01      3.90000E+00
70     4.26000E+01      6.20000E+00
71     4.60000E+01      1.90000E+00
72     5.60000E+01      2.00000E+00
73     9. 0000E+00      3.61000E+01
74     0.               3.80000E+01
75     0.               3.00000E+01
76     0.               1.60000E+01
77     2.00000E+00      1.00000E+01
78     0.               1.00000E+01
79     7.20000E+00      0.
80     1.60000E+01      0.
81     2.00000E+01      0.
82     3.00000E+01      0.
```

```
83      4.02000E+01      0.
84      4.60000E+01      0.
85      6.00000E+01      7.50000E+00
86      7.30000E+01      1.58000E+01
87      8.33081E+01      3.20143E+01
88      8.60000E+01      3.20143E+01
 1   74    2   75    3   76    4   78    5   34    6   79    7   80    8   81    9   82   10    8
11   84   12   47   13   46   14   45   15   35   16   44   17   88   18   43   19   36   20    4
21   41   22   40   23   39   24   38   25   37   26   74
 6    5    5    5    6    5    5    5    6    5
 7    5    5    6    5    6    7    5    6    4
 5    6    6    6    6    5    6    6    6    5
 6    5    6    3    4    3    3    5    5    4
 5    5    4    5    3    5    4    6    6    6
 5    5    7    7    6    7    8    6    6    6
 6    6    6    6    6    6    6    7    5    6
 7    6    6    4    6    4    6    3    5    4
 5    5    5    3    6    6    5    3
65   23   53   52   22   75
23   66   22   79   77
24   67   65   66   23
 7   25   81   24   67
28   26   70   69    6   68
69    5   68   83   82
25   68   82    4   81
71   70   29   27   72
60   31   27   85   10   59
 9   31   56   59   58
63   64   62   54   53   50   49
13   73   74   38   37
14   48   73   12   38
15   49   48   13   38   39
16   50   49   14   39
51   50   17   15   39   40
55   51   56   16   18   40   41
56   17   30   19   41
30   18   57   20   41   42
57   19   33   42
46   85   59   86   45   35
 1   23    2   78   77   76
65    3   66    1    2   22
25    4   64   67    3   65
68   63    7    4   24   64
28   62    5   68   63
 8   29   60   72    9   85
61   62   29   26    5   70
61   28   70    8   27   60
58   56   18   57   19
```



```
60   32    9   55   10   56
60   61   54   31   55
52   20   87   43   42   36
77   79   78
45   21   86   44
33   42   43
38   12   74
12   13   14   39   37
14   38   15   16   40
16   39   17   41
17   40   18   19   42
19   41   20   33   36
33   87   88   36
35   86   57   87   88
21   46   35
72   85   47   21   45
71   72   84   46
49   53   52   14   73   13
50   11   53   15   48   14
54   11   51   49   16   15
55   54   17   50   16
48   53    1   75   73
11   64   65   49    1   48   52
62   11   61   32   55   51   50
31   32   54   56   51   17
31   55   10   58   17   30   18
58   30   86   19   44   20   33   87
59   10   56   86   30   57
85    9   10   58   21   86
27   29   61   32   31    9
62   28   29   60   54   32
61   28   26   63   11   54
62   26   68   25   64   11
25   24   63   11   65   53
64   24    3   53   23    1
 3   67   80   23    2   79
 4   81   24    3   80   66
26    9    6   63   25   82    7
70    5    6   83   71
 5   29   29   69   71    8
83   69   70    8   72   84   47
 8   27   71   47   85   46
48   52   75   13   12   74
73   75   12   37
52    1   22   73   76   74
22   77   75   78
22    2   79   76   78   34
77   76   34
```

```
66  80   2  77  34
81  67  66  79
 7  82   4  67  80
68   6  83   7  81
69   6  82  71  84
83  71  47
72  27   9  46  59  21
21  59  58  57  35  44
44  57  33  43  88
44  87  43
```

PLEASE NOTE THAT THE DEPARTMENT OF EECS, UNIVERSITY OF CALIFORNIA, BERKELEY CAN NOT ASSUME ANY RESPONSIBILITY FOR ANY PROBLEMS ARISING FROM THE USE OF THE PROGRAM.

APPENDIX 2

BENCH MARK CIRCUITS

In order to familiarize the user with the use of T-SPICE, several bench mark circuits are listed in this appendix.

A2-1. Simple differential active load amplifier

The following deck shown below performs a dc transfer curve analysis and dc operating point analysis of a simple differential active load amplifier whose circuit schematic is shown in Fig. A2.1.

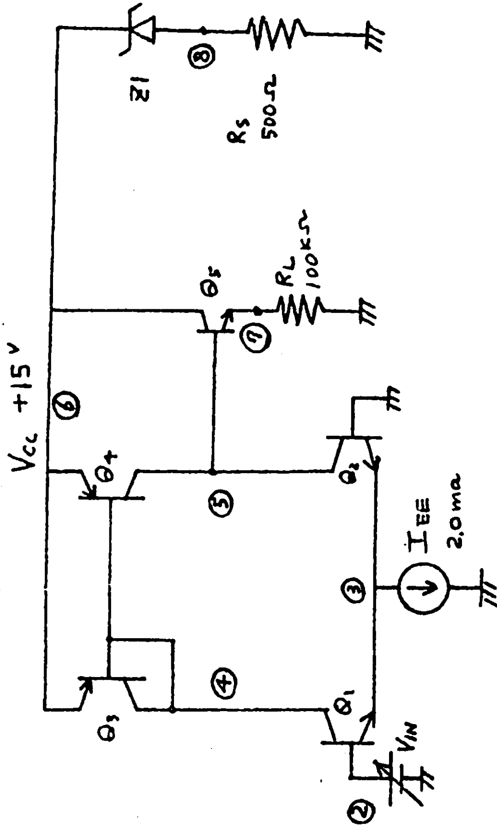


Fig. A2.1

Active load differential amplifier

```
DC TRANSFER CURVE OF A SIMPLE DIFFERENTIAL ACTIVE LOAD AMPLIFIER
Q1 4 2 3 MODN                          X=10.     Y=10.
Q2 5 0 3 MODN                          X=30.     Y=10.
Q3 4 4 6 MODP                          X=30.     Y=30.
Q4 5 4 6 MODP                          X=10.     Y=30.
Q5 6 5 7 MODN                          X=22.     Y=22.
RL 7 0 100K
Z1 6 8 7.3 TC=3.E-03   X=40.  Y=18.666
RS 8 0 500.
IEE 3 0 2.0M
VCC 6 0 15.0
.MODEL MODN NPN BF=100 IS=1.E-15 VA=100.
.MODEL MODP PNP BF=100 IS=1.E-15 VA=50.
VIN 2 0 0.0
.PLOT DC V(7) V(5)
.PRINT DC V(7) V(5)
.PLOT DC T(Q1) T(Q2) T(Q1,Q2)
.DC VIN -10M 10M .5M
.THRML LX=40 LY=40 A0=10 B0=10 KS=.00223 KH=.0002 GH=.01
+TCS=27.7E-9 TCH=30.E-09 LXHDR=100 LYHDR=100
.OPTION ACCT      TROOM=27.0 TOP=28.0 PDMAX=.2
.OP
.END
```

*************** 8 JAN 77 ********************************T-SPICE 2A ******************************** 14:20:14 ***************

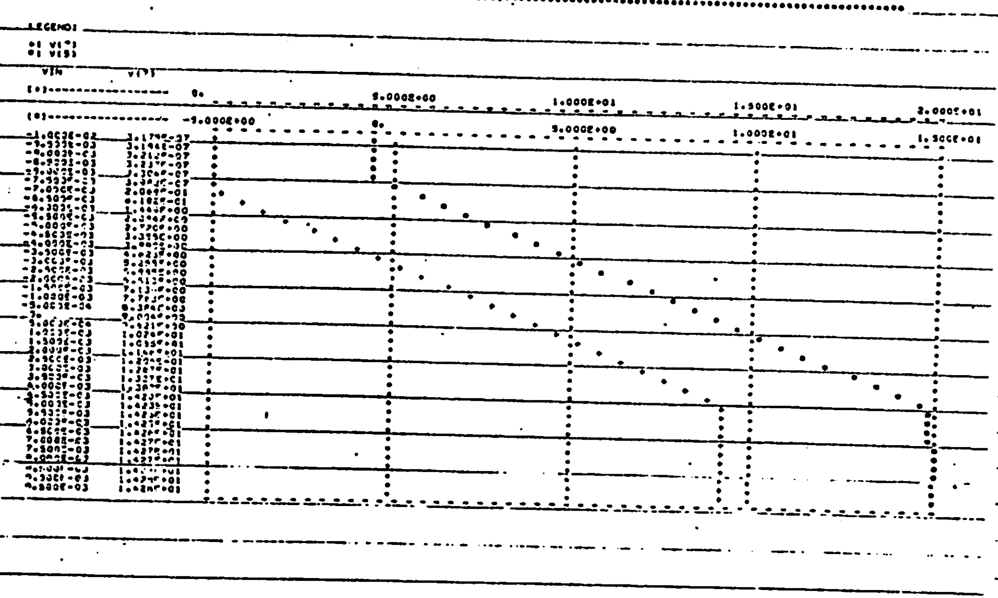
DC TRANSFER CURVE OF A SIMPLE DIFFERENTIAL ACTIVE LOAD AMPLIFIER

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

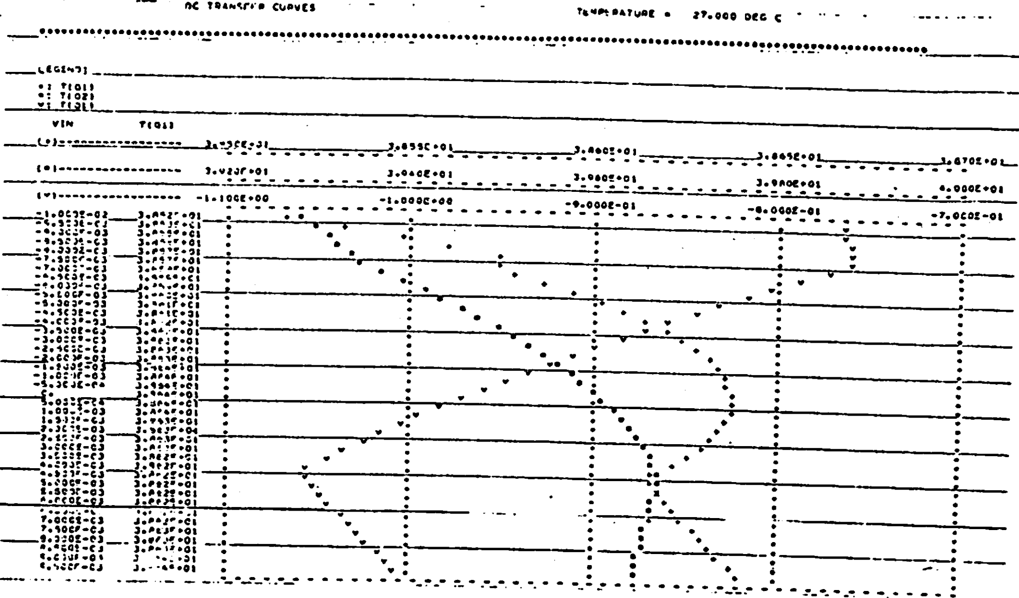
****

VIN	V(7)	V(5)
-1.000E-02	3.179E-07	-6.091E-01
-9.500E-03	3.194E-07	-6.012E-01
-9.000E-03	3.212E-07	-5.902E-01
-8.500E-03	3.237E-07	-5.718E-01
-8.000E-03	3.304E-07	-5.087E-01
-7.500E-03	3.902E-07	8.009E-02
-7.000E-03	2.068E-01	7.320E-01
-6.500E-03	8.192E-01	1.390E+00
-6.000E-03	1.449E+00	2.027E+00
-5.500E-03	2.084E+00	2.672E+00
-5.000E-03	2.720E+00	3.315E+00
-4.500E-03	3.355E+00	3.956E+00
-4.000E-03	3.990E+00	4.595E+00
-3.500E-03	4.623E+00	5.233E+00
-3.000E-03	5.255E+00	5.868E+00
-2.500E-03	5.885E+00	6.501E+00
-2.000E-03	6.513E+00	7.132E+00
-1.500E-03	7.139E+00	7.761E+00
-1.000E-03	7.763E+00	8.387E+00
-5.000E-04	8.384E+00	9.011E+00
0.	9.004E+00	9.632E+00
5.000E-04	9.621E+00	1.025E+01
1.000E-03	1.024E+01	1.087E+01
1.500E-03	1.085E+01	1.148E+01
2.000E-03	1.146E+01	1.209E+01
2.500E-03	1.206E+01	1.270E+01
3.000E-03	1.267E+01	1.331E+01
3.500E-03	1.327E+01	1.391E+01
4.000E-03	1.387E+01	1.451E+01
4.500E-03	1.420E+01	1.484E+01
5.000E-03	1.421E+01	1.487E+01
5.500E-03	1.425E+01	1.489E+01
6.000E-03	1.425E+01	1.490E+01
6.500E-03	1.426E+01	1.490E+01
7.000E-03	1.427E+01	1.491E+01
7.500E-03	1.427E+01	1.491E+01
8.000E-03	1.427E+01	1.492E+01
8.500E-03	1.428E+01	1.492E+01
9.000E-03	1.428E+01	1.492E+01
9.500E-03	1.428E+01	1.493E+01

The following is a part of the resultant output file when the above-mentioned deck is run on the program T-SPICE2A.



DC TRANSFER CURVE OF A SIMPLE DIFFERENTIAL ACTIVE LOAD AMPLIFIER
DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C
LEGEND:
VIN



DC TRANSFER CURVE OF A SIMPLE DIFFERENTIAL ACTIVE LOAD AMPLIFIER
DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C
LEGEND:
VIN

**** BIPOLAR JUNCTION TRANSISTOR OPERATING POINTS

	Q1	Q2	Q3	Q4	Q5
MODEL	MQDN ONCHIP	MQDN ONCHIP	MQDP ONCHIP	MQDP ONCHIP	MQDN ONCHIP
IB	8.61E-06	9.11E-06	-9.65E-06	-9.14E-06	8.46E-07
IC	9.84E-04	9.99E-04	-9.65E-04	-1.00E-03	8.92E-05
VBE	.692	.692	-.694	-.694	.629
VBC	-14.306	-9.633	0.	4.673	-5.367
VCE	14.998	10.325	-.694	-5.367	5.996
BETADC	114.306	109.629	100.000	109.384	105.372
TEMP-C	38.638	39.610	39.315	38.417	39.122
WATTS	.015	.010	.001	.005	.001
GM	3.66E-02	3.71E-02	3.58E-02	3.72E-02	3.31E-03
RPI	3.12E+03	2.96E+03	2.79E+03	2.93E+03	3.18E+04
RO	1.16E+05	1.10E+05	5.19E+04	5.47E+04	1.18E+06
CPI	0.	0.	0.	0.	0.
CMU	0.	0.	0.	0.	0.
BETAAC	114.279	109.602	99.946	109.300	105.344
FT	5.83E+17	5.90E+17	5.70E+17	5.93E+17	5.27E+16

**** ZENER DIODES OPERATING POINTS

	Z1 ONCHIP
VOLTS	7.346
AMPS	1.53E-02
TEMP-C	42.185
WATTS	1.12E-01

**** BIPOLAR JUNCTION TRANSISTOR OPERATING POINTS

	Q1	Q2	Q3	Q4	Q5
MODEL	MQDN ONCHIP	MQDN ONCHIP	MQDP ONCHIP	MQDP ONCHIP	MQDN ONCHIP
IB	8.61E-06	9.11E-06	-9.65E-06	-9.14E-06	8.46E-07
IC	9.84E-04	9.99E-04	-9.65E-04	-1.00E-03	8.92E-05
VBE	.692	.692	-.694	-.694	.629
VBC	-14.306	-9.633	0.	4.673	-5.367
VCE	14.998	10.325	-.694	-5.367	5.996
BETADC	114.306	109.629	100.000	109.384	105.372
TEMP-C	38.638	39.610	39.315	38.417	39.122
WATTS	.015	.010	.001	.005	.001
GM	3.66E-02	3.71E-02	3.58E-02	3.72E-02	3.31E-03
RPI	3.12E+03	2.96E+03	2.79E+03	2.93E+03	3.18E+04
RO	1.16E+05	1.10E+05	5.19E+04	5.47E+04	1.18E+06
CPI	0.	0.	0.	0.	0.
CMU	0.	0.	0.	0.	0.
BETAAC	114.279	109.602	99.946	109.300	105.344
FT	5.83E+17	5.90E+17	5.70E+17	5.93E+17	5.27E+16

**** ZENER DIODES OPERATING POINTS

	Z1 ONCHIP
VOLTS	7.346
AMPS	1.53E-02
TEMP-C	42.185
WATTS	1.12E-01

***** 8 JAN 77 ************** T-SPICE 2A ************** 14:20:14 *****

DC TRANSFER CURVE OF A SIMPLE DIFFERENTIAL ACTIVE LOAD AMPLIFIER

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(2)	-5.0073E-16	(3)	-6.9183E-01	(4)	1.4306E+01	(5)	9.5327E+00	(6)	1.5000E+01
(7)	9.0040E+00	(8)	7.6544E+00						

NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE
(1)	3.8638E+01	(2)	3.9610E+01	(3)	3.9315E+01	(4)	3.8417E+01	(5)	3.9122E+01
(6)	4.2185E+01	(7)	3.7997E+01	(8)	3.9270E+01	(9)	3.8675E+01	(10)	3.7839E+01
(11)	3.8243E+01	(12)	4.0095E+01	(13)	4.0890E+01	(14)	3.8231E+01	(15)	3.8533E+01
(16)	3.9797E+01	(17)	3.8914E+01	(18)	3.8108E+01	(19)	3.8372E+01	(20)	3.8675E+01
(21)	3.9196E+01	(22)	3.7676E+01	(23)	3.8494E+01	(24)	3.8260E+01	(25)	3.7510E+01
(26)	3.8307E+01	(27)	3.9003E+01	(28)	3.6261E+01	(29)	3.7242E+01	(30)	3.6931E+01
(31)	3.6182E+01	(32)	3.6925E+01	(33)	3.8383E+01	(34)	3.8832E+01	(35)	3.6994E+01
(36)	3.7711E+01	(37)	3.8672E+01	(38)	3.7397E+01	(39)	3.6434E+01	(40)	3.7114E+01
(41)	3.8024E+01	(42)	3.7755E+01	(43)	3.2602E+01	(44)	3.3734E+01	(45)	3.4266E+01
(46)	3.4114E+01	(47)	3.3075E+01	(48)	3.4327E+01	(49)	3.4780E+01	(50)	3.4143E+01
(51)	3.2943E+01	(52)	3.3984E+01	(53)	3.3887E+01	(54)	3.3583E+01	(55)	3.2520E+01
(56)	3.3535E+01	(57)	3.3818E+01	(58)	3.3579E+01	(59)	2.7144E+01	(60)	2.7000E+01

AMBIENT TEMPERATURE(DEG-C) TOTAL POWER DISSIPATION ON CHIP

27.000 1.44E-01WATTS

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VCC	-1.738E-02
VIN	-8.602E-06

TOTAL POWER DISSIPATION OF THE ENTIRE CIRUIT 2.62E-01WATTS

**** RESISTORS OPERATING POINTS

	RL OFCHIP	RS OFCHIP
VOLTS	9.004	7.654
AMPS	9.00E-05	1.53E-02
OHMS	1.00E+05	5.00E+02
TEMP-C	27.000	27.000
WATTS	8.11E-04	1.17E-01

A2-2. Simple inverter

The following deck shown below performs a transient analysis of a simple inverter whose circuit schematic is shown in Fig. A2.2.


```
SIMPLE INVERTER EXAMPLE CIRCUIT   FUNCTIONAL ITERATION
Q1 4 3 0 MOD1      X=20.    Y=20.
RL 5 4 1K
RS 2 3 10K     X=30.0   Y=30.0
VCC 5 0 20.0
VIN 2 0 PULSE(10.0 1.0 0US 100US 100US 20MS 30MS)
.MODEL MOD1 NPN BF=200 BR=2 IS=5.E-15 RB=200 RC=200 VA=130 PE=.7 PC=.55
.THRML LX=40 LY=40 A0=10 B0=10 KS=.00223 KH=.0002 GH=.01
+TCS=27.7E-9 TCH=30.E-9 LXHDR=100. LYHDR=100
.PLOT TRAN V(4)
.PLOT TRAN T(Q1)
.TRAN 100US 10MS
.END
```

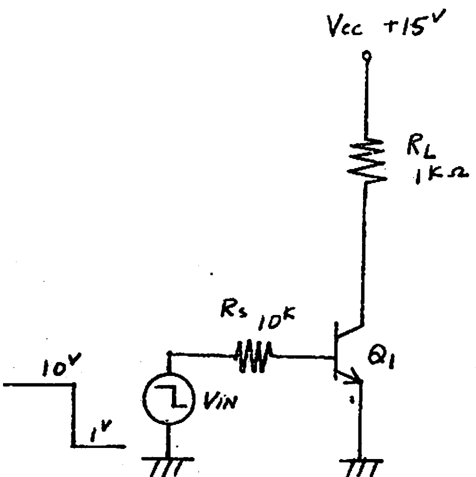


Fig. A2.2

Simple inverter

The following is a part of the resultant output file when the above-mentioned deck is run on the program T-SPICE2A.

***** 6 JAN 77 ************** T-SPICE 2A ************** 14120114 *****

SIMPLE INVERTER EXAMPLE CIRCUIT   FUNCTIONAL ITERATION

INITIAL TRANSIENT SOLUTION   TEMPERATURE = 27.000DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(2)	1.0000E+01	(3)	9.2182E-01	(4)	3.3876E+00	(8)	2.0000E+01		

NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE
(1)	3.2796E+01	(2)	3.3177E+01	(3)	3.2234E+01	(4)	3.2278E+01	(5)	3.2485E+01
(6)	3.2309E+01	(7)	3.2557E+01	(8)	3.2799E+01	(9)	3.2605E+01	(10)	3.2627E+01
(11)	3.2521E+01	(12)	3.2303E+01	(13)	3.2684E+01	(14)	3.1657E+01	(15)	3.1670E+01
(16)	3.1165E+01	(17)	3.1729E+01	(18)	3.2059E+01	(19)	3.2365E+01	(20)	3.1995E+01
(21)	3.2023E+01	(22)	3.2025E+01	(23)	2.9906E+01	(24)	3.0415E+01	(25)	3.0419E+01
(26)	2.9907E+01	(27)	3.0419E+01	(28)	3.0419E+01	(29)	2.9917E+01	(30)	3.0441E+01
(31)	3.0396E+01	(32)	2.9909E+01	(33)	3.0447E+01	(34)	3.0422E+01	(35)	2.7065E+01
(36)	2.7000E+01								

AMBIENT TEMPERATURE(DEG-C)   TOTAL POWER DISSIPATION ON CHIP
27.000   6.54E-02WATTS

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VCC	-1.661E-02
VIN	-9.078E-04

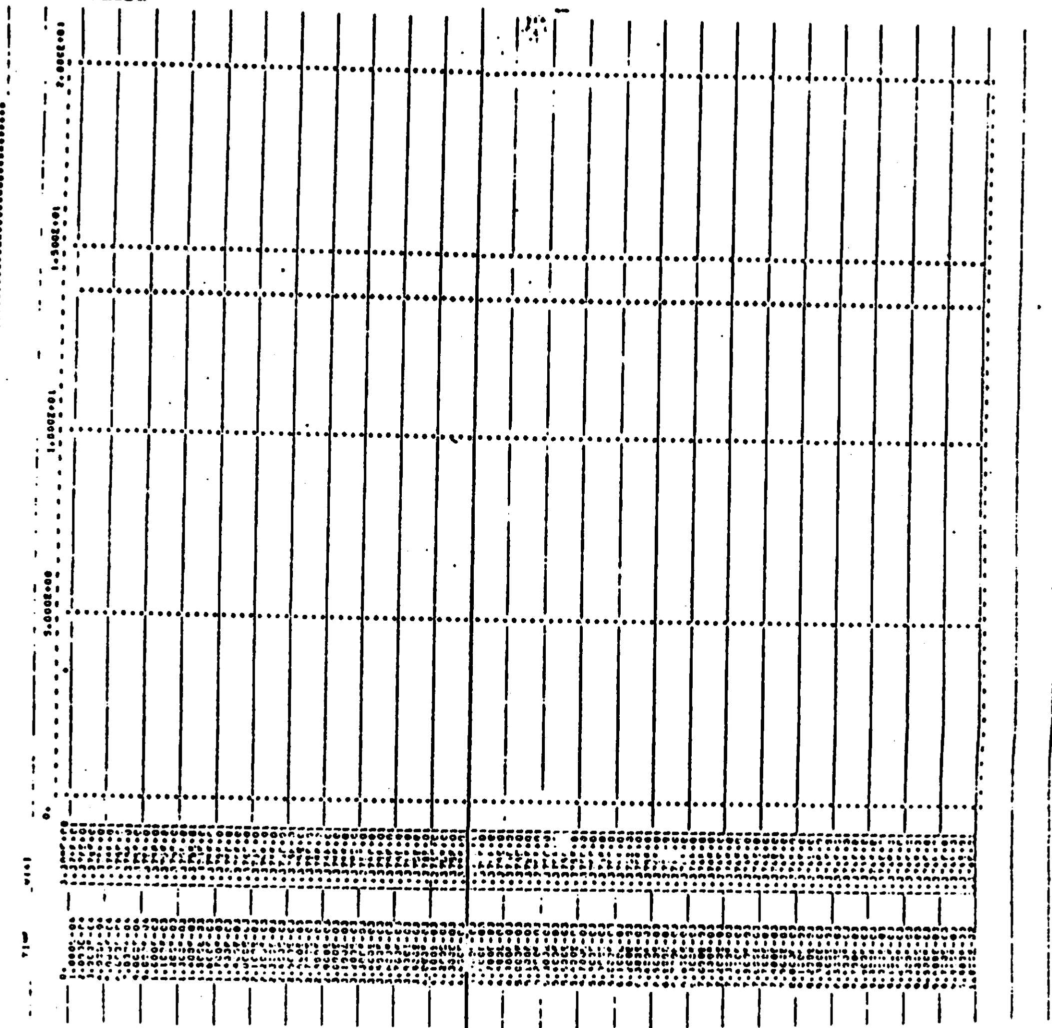
TOTAL POWER DISSIPATION OF THE ENTIRE CIRUIT 3.41E-01WATTS

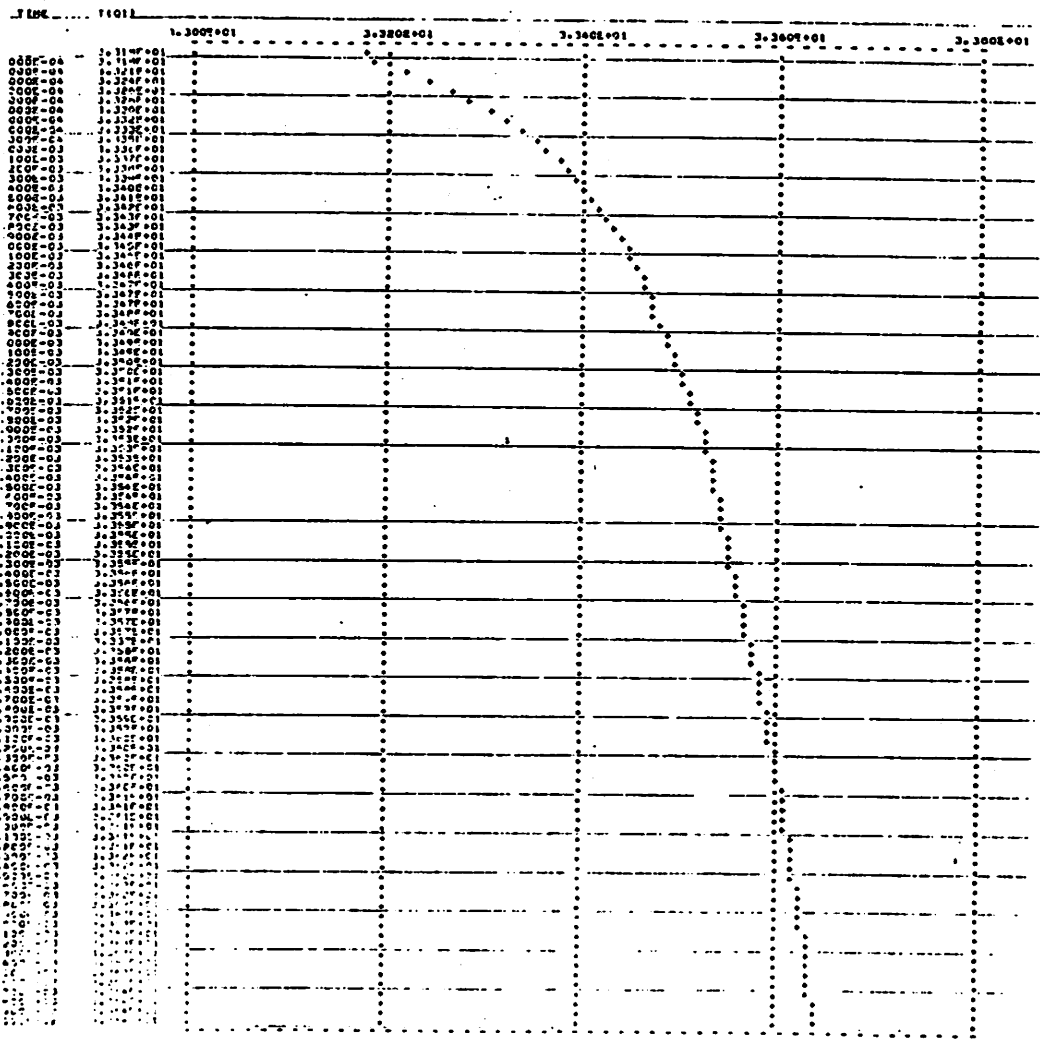
**** RESISTORS OPERATING POINTS

	PL OFCHIP	RS ONCHIP
VOLTS	16.612	9.078
AMPS	1.66E-02	9.08E-04
OHMS	1.00E+03	1.00E+04
TEMP-C	27.000	32.796
WATTS	2.76E-01	9.24E-03

**** BIPOLAR JUNCTION TRANSISTOR OPERATING POINTS

	Q1
MODEL	MOD1 ONCHIP
IB	9.08E-06
IC	1.06E-02
VBE	.922
VBC	-2.466
VCE	3.388
BETADC	18.298
TEMP-C	13.177
WATTS	.097





A2-3. dc transfer curve analysis of a simple operational amplifier

The following deck performs a dc transfer curve analysis for a simplified 741 operational amplifier sh[illegible]n in Fig. A2.3.

```
EXAMPLE 741
Q1 10 0 2 MODN                         X=31.0  Y=2.0
Q2 10 1 3 MODN                         X=26.0   Y=2.0
Q3 5 4 2 MODP                          X=31.0     Y=4.0
Q4 6 4 3 MODP            X=22.0     Y=4.0
I4 4 0 .3U
R411 4 11 100MEG
Q7 10 5 7 MODN
Q5 5 7 8 MODN                          X=30.0   Y=11.0
Q6 6 7 9 MODN                          X=37.0    Y=11.0
R1 8 11 1K
R2 7 11 50K
R3 9 11 1K
Q8 10 6 12 MODN
R4 12 11 50K
Q17 13 12 11 MODN                      X=39.0    Y=19.0
I14 14 0 .3M
Q13A 14 14 10 MODP                     X=3.0     Y=11.0
Q13B 13 14 10 MODP                     X=3.0     Y=11.0
Q13C 15 14 10 MODP .75                 X=3,0     Y=11.0
Q21 15 15 16 MODN
Q22 16 16 17 MODN
Q23 11 13 17 MODP                      X=26.0    Y=18.0
Q14 10 15 18    MODN                   X=10.0     Y=35.0
Q20 11 17 18 MODP         X=39.0    Y=35.0
RL 18 0 1K
VIN 0 19 0.0
VCC 10 0 15
VEE 11 0 -15
RF2 18 1 100K
RF1 1 19 50
.THRML  LX=50 LY=40 A0=10 B0=10 KS=.00223 KH=.0002 GH=.01
+TCS=27.0E-9 TCH=30.E-9 LXHDR=100. LYHDR=100.
.MODEL MODN NPN BF=100 VA=100
.MODEL MODP PNP BF=100 VA=50
.PRINT DC V(18) V(1)
.PRINT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.PLOT DC V(19) V(1)
.PLOT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.DC VIN -10M 10M 1M
.OPTION ACCT PDMAX=.2 IDBUG7=1
.END
```

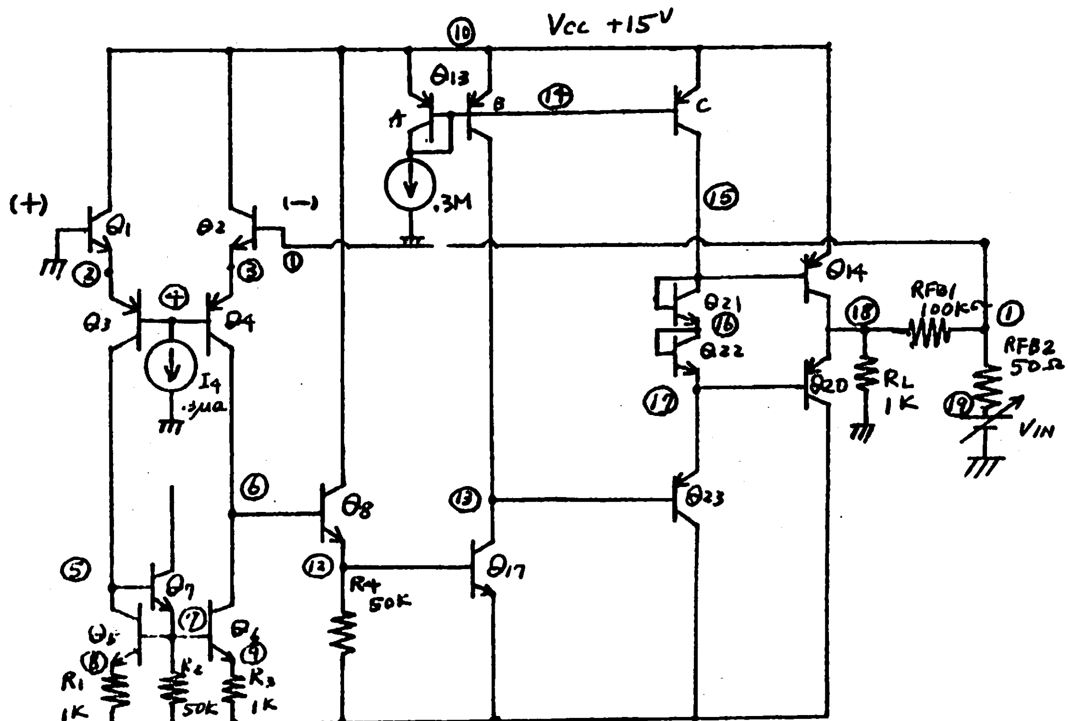



Fig. A2.3

Simplified 741 op. amp.

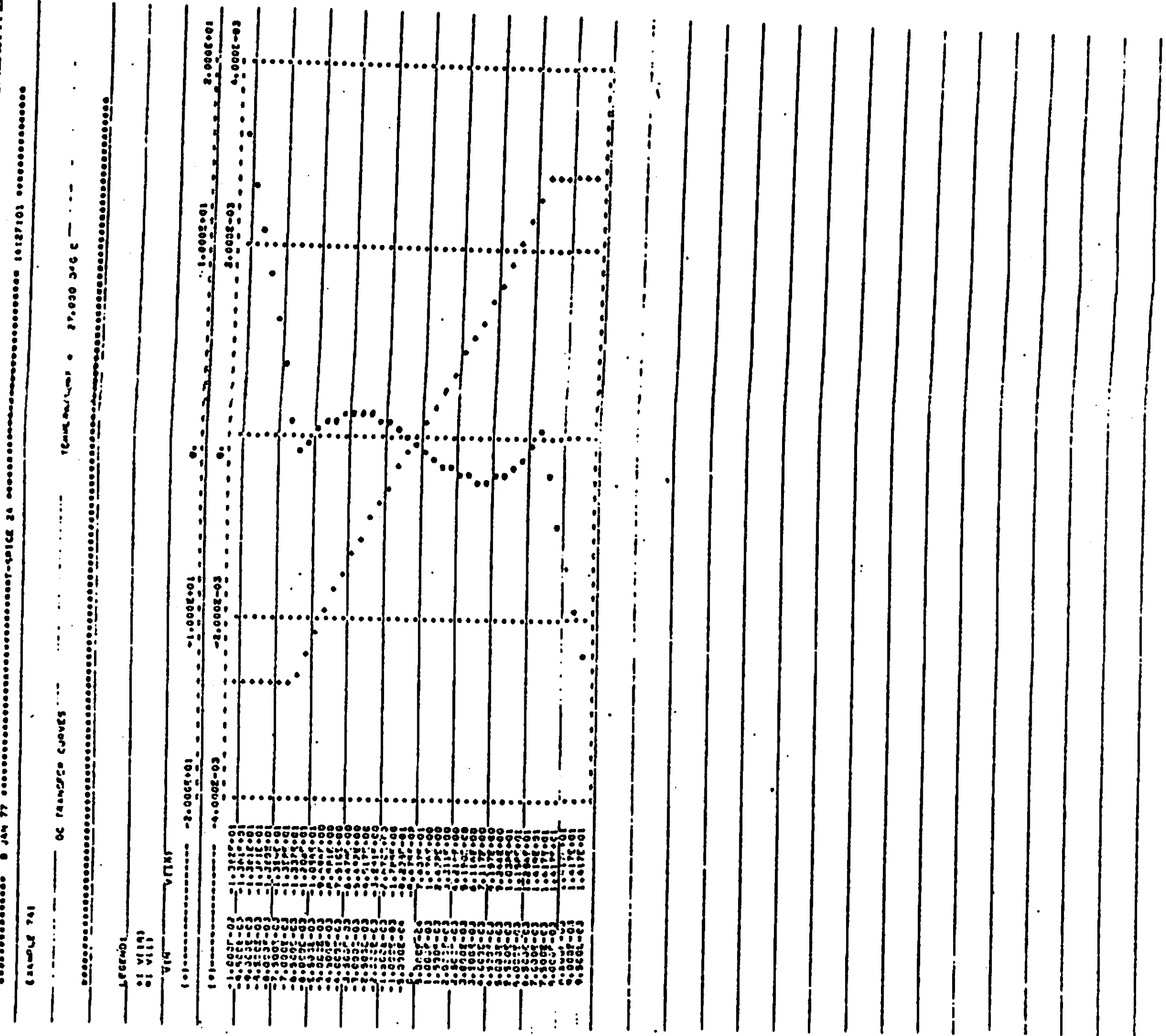
**************** 8 JAN 77 ********************************T-SPICE 2A ********************************* 14:27:01 ***************

EXAMPLE 741

DC TRANSFER CURVES　　　　TEMPERATURE = 27.000 DEG C

VIN	V(18)	V(1)
-1.000E-02	-1.362E+01	3.178E-03
-9.500E-03	-1.361E+01	2.679E-03
-9.000E-03	-1.361E+01	2.191E-03
-8.500E-03	-1.361E+01	1.683E-03
-8.000E-03	-1.360E+01	1.186E-03
-7.500E-03	-1.359E+01	6.907E-04
-7.000E-03	-1.358E+01	1.997E-04
-6.500E-03	-1.337E+01	-1.946E-04
-6.000E-03	-1.208E+01	-5.100E-05
-5.500E-03	-1.086E+01	5.874E-05
-5.000E-03	-9.696E+00	1.401E-04
-4.500E-03	-8.581E+00	1.976E-04
-4.000E-03	-7.510E+00	2.328E-04
-3.500E-03	-6.478E+00	2.487E-04
-3.000E-03	-5.482E+00	2.471E-04
-2.500E-03	-4.517E+00	2.292E-04
-2.000E-03	-3.581E+00	1.977E-04
-1.500E-03	-2.670E+00	1.527E-04
-1.000E-03	-1.785E+00	9.523E-05
-5.000E-04	-9.238E-01	2.611E-05
0.	-8.479E-02	-5.432E-05
5.000E-04	7.407E-01	-1.416E-04
1.000E-03	1.576E+00	-2.238E-04
1.500E-03	2.432E+00	-2.958E-04
2.000E-03	3.311E+00	-3.562E-04
2.500E-03	4.216E+00	-4.040E-04
3.000E-03	5.150E+00	-4.367E-04
3.500E-03	6.116E+00	-4.536E-04
4.000E-03	7.117E+00	-4.513E-04
4.500E-03	8.157E+00	-4.332E-04
5.000E-03	9.244E+00	-3.897E-04
5.500E-03	1.038E+01	-3.221E-04
6.000E-03	1.158E+01	-2.236E-04
6.500E-03	1.284E+01	-9.138E-05
7.000E-03	1.419E+01	8.120E-05
7.500E-03	1.417E+01	-4.291E-04
8.000E-03	1.417E+01	-9.288E-04
8.500E-03	1.417E+01	-1.429E-03
9.000E-03	1.417E+01	-1.928E-03
9.500E-03	1.417E+01	-2.428E-03

The following is a part of output file when the above-mentioned deck is run on the program T-SPICE2A.



*************** 8 JAN 77 ******************************T-SPICE 2A ****************************** 14:27:01 ***************

EXAMPLE 741

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

VIN	I(Q1)	I(Q3)	I(Q8)
-1.000E-02	-4.189E-02	-7.425E-02	4.608E-02
-9.500E-03	-4.181E-02	-7.419E-02	4.612E-02
-9.000E-03	-4.165E-02	-7.397E-02	4.607E-02
-8.500E-03	-4.155E-02	-7.387E-02	4.609E-02
-8.000E-03	-4.144E-02	-7.373E-02	4.608E-02
-7.500E-03	-4.130E-02	-7.353E-02	4.602E-02
-7.000E-03	-4.101E-02	-7.303E-02	4.579E-02
-6.500E-03	-3.803E-02	-6.712E-02	4.195E-02
-6.000E-03	-2.198E-02	-3.466E-02	2.061E-02
-5.500E-03	-9.281E-03	-9.354E-03	4.168E-03
-5.000E-03	9.844E-05	9.460E-03	-7.841E-03
-4.500E-03	6.872E-03	2.301E-02	-1.625E-02
-4.000E-03	1.119E-02	3.162E-02	-2.127E-02
-3.500E-03	1.342E-02	3.600E-02	-2.339E-02
-3.000E-03	1.372E-02	3.651E-02	-2.208E-02
-2.500E-03	1.224E-02	3.343E-02	-1.983E-02
-2.000E-03	9.267E-03	2.735E-02	-1.472E-02
-1.500E-03	4.828E-03	1.833E-02	-7.559E-03
-1.000E-03	-9.877E-04	6.570E-03	1.678E-03
-5.000E-04	-8.078E-03	-7.624E-03	1.267E-02
0.	-1.638E-02	-2.375E-02	2.619E-02
5.000E-04	-2.531E-02	-3.999E-02	4.240E-02
1.000E-03	-3.368E-02	-5.462E-02	5.840E-02
1.500E-03	-4.097E-02	-6.718E-02	7.259E-02
2.000E-03	-4.700E-02	-7.788E-02	8.457E-02
2.500E-03	-5.170E-02	-8.594E-02	9.409E-02
3.000E-03	-5.483E-02	-9.076E-02	1.007E-01
3.500E-03	-5.630E-02	-9.304E-02	1.043E-01
4.000E-03	-5.595E-02	-9.213E-02	1.045E-01
4.500E-03	-5.354E-02	-8.759E-02	1.008E-01
5.000E-03	-4.859E-02	-7.872E-02	9.267E-02
5.500E-03	-4.126E-02	-6.541E-02	7.981E-02
6.000E-03	-3.060E-02	-4.638E-02	6.093E-02
6.500E-03	-1.639E-02	-2.111E-02	3.547E-02
7.000E-03	2.088E-03	1.144E-02	1.115E-03
7.500E-03	-1.148E-02	-1.529E-02	2.619E-02
8.000E-03	-1.158E-02	-1.558E-02	2.640E-02
8.500E-03	-1.150E-02	-1.550E-02	2.642E-02
9.000E-03	-1.141E-02	-1.542E-02	2.642E-02
9.500E-03	-1.132E-02	-1.533E-02	2.642E-02

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

LEGEND:

The following is a part of output file when the same deck is run on the program T-SPICE2B. Notice there exists hardly any difference between the two results.

EXAMPLE 741

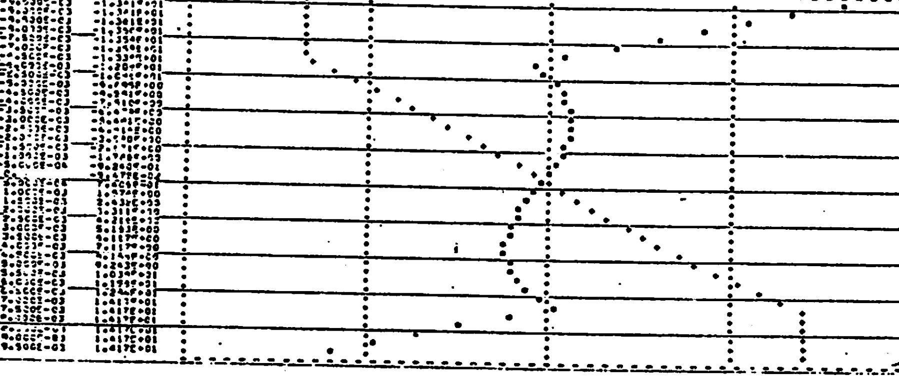
DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

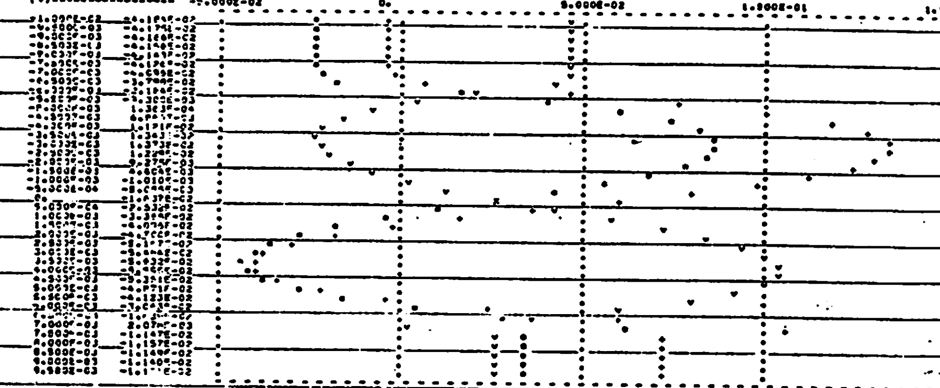
VIN	V(10)	V(1)
-1.000E-02	-1.362E+01	3.178E-03
-9.500E-03	-1.361E+01	2.679E-03
-9.000E-03	-1.361E+01	2.181E-03
-8.500E-03	-1.361E+01	1.683E-03
-8.000E-03	-1.360E+01	1.186E-03
-7.500E-03	-1.359E+01	6.907E-04
-7.000E-03	-1.358E+01	1.997E-04
-6.500E-03	-1.336E+01	-1.942E-04
-6.000E-03	-1.208E+01	-5.156E-05
-5.500E-03	-1.086E+01	5.872E-05
-5.000E-03	-9.695E+00	1.404E-04
-4.500E-03	-8.581E+00	1.976E-04
-4.000E-03	-7.510E+00	2.330E-04
-3.500E-03	-6.479E+00	2.486E-04
-3.000E-03	-5.481E+00	2.473E-04
-2.500E-03	-4.516E+00	2.297E-04
-2.000E-03	-3.590E+00	1.977E-04
-1.500E-03	-2.671E+00	1.525E-04
-1.000E-03	-1.786E+00	9.503E-05
-5.000E-04	-9.240E-01	2.602E-05
0.	-8.475E-02	-5.432E-05
5.000E-04	7.406E-01	-1.416E-04
1.000E-03	1.576E+00	-2.238E-04
1.500E-03	2.432E+00	-2.959E-04
2.000E-03	3.311E+00	-3.563E-04
2.500E-03	4.216E+00	-4.037E-04
3.000E-03	5.153E+00	-4.354E-04
3.500E-03	6.117E+00	-4.531E-04
4.000E-03	7.117E+00	-4.530E-04
4.500E-03	8.158E+00	-4.329E-04
5.000E-03	9.243E+00	-3.901E-04
5.500E-03	1.038E+01	-3.218E-04
6.000E-03	1.155E+01	-2.239E-04
6.500E-03	1.284E+01	-9.138E-05
7.000E-03	1.419E+01	8.111E-05
7.500E-03	1.417E+01	-4.291E-04
8.000E-03	1.417E+01	-9.288E-04
8.500E-03	1.417E+01	-1.429E-03
9.000E-03	1.417E+01	-1.928E-03
9.500E-03	1.417E+01	-2.428E-03

EXAMPLE 741

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

VIN	I(Q1)	I(Q3)	I(Q5)
-1.000E-02	-4.184E-02	-7.416E-02	4.603E-02
-9.500E-03	-4.175E-02	-7.409E-02	4.606E-02
-9.000E-03	-4.166E-02	-7.399E-02	4.609E-02
-8.500E-03	-4.156E-02	-7.388E-02	4.609E-02
-8.000E-03	-4.143E-02	-7.371E-02	4.607E-02
-7.500E-03	-4.126E-02	-7.345E-02	4.598E-02
-7.000E-03	-4.096E-02	-7.295E-02	4.573E-02
-6.500E-03	-3.798E-02	-6.703E-02	4.189E-02
-6.000E-03	-2.184E-02	-3.459E-02	2.057E-02
-5.500E-03	-9.300E-03	-9.394E-03	4.193E-03
-5.000E-03	1.363E-04	9.533E-03	-7.894E-03
-4.600E-03	6.869E-03	2.301E-02	-1.625E-02
-4.000E-03	1.121E-02	3.166E-02	-2.130E-02
-3.500E-03	1.343E-02	3.603E-02	-2.341E-02
-3.000E-03	1.373E-02	3.653E-02	-2.286E-02
-2.500E-03	1.224E-02	3.353E-02	-1.989E-02
-2.000E-03	9.275E-03	2.737E-02	-1.473E-02
-1.500E-03	4.904E-03	1.828E-02	-7.525E-03
-1.000E-03	-1.010E-03	6.531E-03	1.611E-03
-5.000E-04	-8.095E-03	-7.642E-03	1.268E-02
0.	-1.637E-02	-2.375E-02	2.619E-02
5.000E-04	-2.532E-02	-4.000E-02	4.240E-02
1.000E-03	-3.368E-02	-5.462E-02	5.840E-02
1.500E-03	-4.096E-02	-6.720E-02	7.261E-02
2.000E-03	-4.700E-02	-7.756E-02	8.458E-02
2.500E-03	-5.167E-02	-8.548E-02	9.403E-02
3.000E-03	-5.484E-02	-9.076E-02	1.007E-01
3.500E-03	-5.632E-02	-9.308E-02	1.043E-01
4.000E-03	-5.595E-02	-9.213E-02	1.045E-01
4.500E-03	-5.351E-02	-8.753E-02	1.008E-01
5.000E-03	-4.871E-02	-7.881E-02	9.276E-02
5.500E-03	-4.123E-02	-6.535E-02	7.976E-02
6.000E-03	-3.063E-02	-4.643E-02	6.099E-02
6.500E-03	-1.639E-02	-2.110E-02	3.547E-02
7.000E-03	2.078E-03	1.142E-02	1.137E-03
7.500E-03	-1.147E-02	-1.528E-02	2.613E-02
8.000E-03	-1.157E-02	-1.554E-02	2.638E-02
8.500E-03	-1.149E-02	-1.549E-02	2.640E-02
9.000E-03	-1.140E-02	-1.540E-02	2.640E-02
9.500E-03	-1.131E-02	-1.531E-02	2.640E-02


6 JAN 77 T-SPICE 2B 15:18:01
EXAMPLE 741
DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C
LEGEND:
VIN
-2.000E+01
-1.000E+01
0.
1.000E+01
2.000E+01
-4.000E-03
-2.000E-03
2.000E-03
4.000E-03


6 JAN 77 T-SPICE 2B 15:18:01
EXAMPLE 741
DC TRANSFER CURVES
TEMPERATURE = 27.000 DEG C
LEGEND:
VIN
-1.000E-01
5.000E-02
1.000E-01
-5.000E-02
0.
1.500E-01

A2-4. <u>dc transfer curve of a 741 operational amplifier</u>

The following deck performs a dc transfer curve analysis for a commercially available 741 operational amplifier shown in Fig. A2.4.


```
DC TRANSFER CURVE OF FAIRCHILD 741
Q1 10 1 3 MODN                       X=37.5    Y=8.0
Q2 10 2 4 MODN                       X=34.5    Y=8.
Q3 5 11 3 MODP                       X=32.5    Y=12.8
Q4 9 11 4 MODP                       X=.6.0    Y=12.8
Q5 5 6 7 MODN                        X=39.2    Y=16.5
Q6 9 6 8 MODN                        X=45.0    Y=16.5
Q7 23 5 6 MODN                       X=32.5    Y=22.5
Q8A 10 10 23 MODP .2                 X=13.0    Y=6.5
Q8B 10 10 23 MODP .8                 X=26.0    Y=6.5
Q9A 11 10 23 MODP .4                 X=32.5    Y=6.5
Q9B 11 10 23 MODP .6                 X=26.0    Y=6.5
Q10 11 12 14 MODN                    X=39.2    Y=22.5
Q11 12 12 24 MODN                    X=45.0    Y=28.0
Q12 13 13 23 MODP                    X=8.0     Y=6.5
Q13A 15 13 23 MOD1                   X=8.0     Y=12.8
Q13B 17 13 23 MOD2                   X=8.0     Y=12.8
Q14 23 17 20 MODA                    X=13.0    Y=47.0
Q15A 17 20 21 MODN .35               X=32.5    Y=38.0
Q15B 17 20 21 MODN .65               X=26.0    Y=38.0
Q16 23 9 16 MODN                     X=37.5    Y=28.0
Q17A 15 16 25 MODN .35               X=45.0    Y=28.0
Q17B 15 16 25 MODN .65               X=41.0    Y=28.0
Q18A 17 18 19 MODN .75               X=32.5    Y=31.3
Q18B 17 18 19 MODN .25               X=26.0    Y=31.3
Q19A 17 17 18 MODN .65               X=26.0    Y=31.3
Q19B 17 17 18 MODN .35               X=32.5    Y=31.3
Q20 24 19 22 MODP                    X=41.0    Y=47.0
Q21 26 22 21 MODP                    X=26.0    Y=47.0
Q22 9 26 24 MODN                     X=41.0    Y=38.0
Q23A 24 15 9 MOD3                    X=37.5    Y=38.0
Q23B 24 15 19 MOD4                   X=37.5    Y=31.3
Q24A 26 26 24 MODN .25               X=32.5    Y=38.0
Q24B 26 26 24 MODN .75               X=32.5    Y=47.0
R1 7 24 1K
R2 6 24 50K
R3 8 24 1K
R4 14 24 3K
R5 13 12 39K
R6 20 21 27
R7 21 22 22.0
R8 25 24 100.0
R9 16 24 50K
R10 18 19 40K
R11 26 24 50K
RFB1 21 2 100K
RFB2 2 30 50.0
RL 21 0 1.0K
```

```
VIN1 1 0 0.0
VCC 23 0 15.0
VEE 24 0 -15.0
VIN 0 30 -8M
.MODEL MODN NPN IS=1.E-14 VA=100
.MODEL MODP PNP IS=1.E-14 VA=75.0
.MODEL MOD1 PNP IS=2.25E-15 VA=75
.MODEL MOD2 PNP IS=.9E-15 VA=75.
.MODEL MOD3 PNP IS=.0063E-15 VA=75
.MODEL MOD4 PNP IS=.79E-15 VA=75
.MODEL MODA NPN IS=1.E-14  VA=100 BF=200
.THRML LX=55 LY=55 A0=10 B0=10 KS=2.23E-03 KH=4.5E-04 GH=1.E-02
+TCS=.02 TCH=.02 LXHDR=110 LYHDR=110
.PRINT DC V(2) V(21)
.PRINT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.PLOT DC V(2) (-.4M,.4M) V(21)
.PLOT DC T(Q1,Q2) T(Q3,Q4) T(Q5,Q6)
.DC VIN -8M 6.4M .4M
.OPTION ACCT IDBUG7=1 PDMAX=.15
.END
```

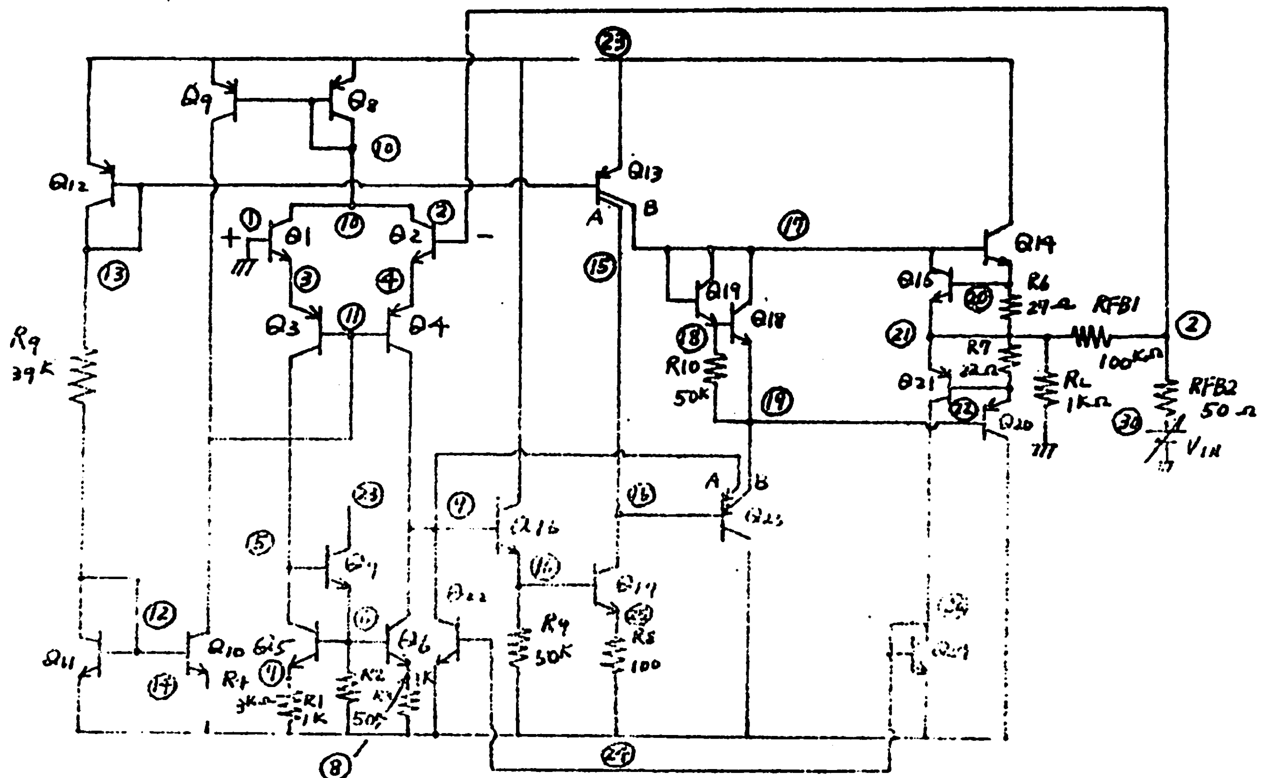


Fig. A2.4

Complete schematic of 741 operational amplifier

The following is a part of output file when the above-mentioned deck is run on the program T-SPICE2A.

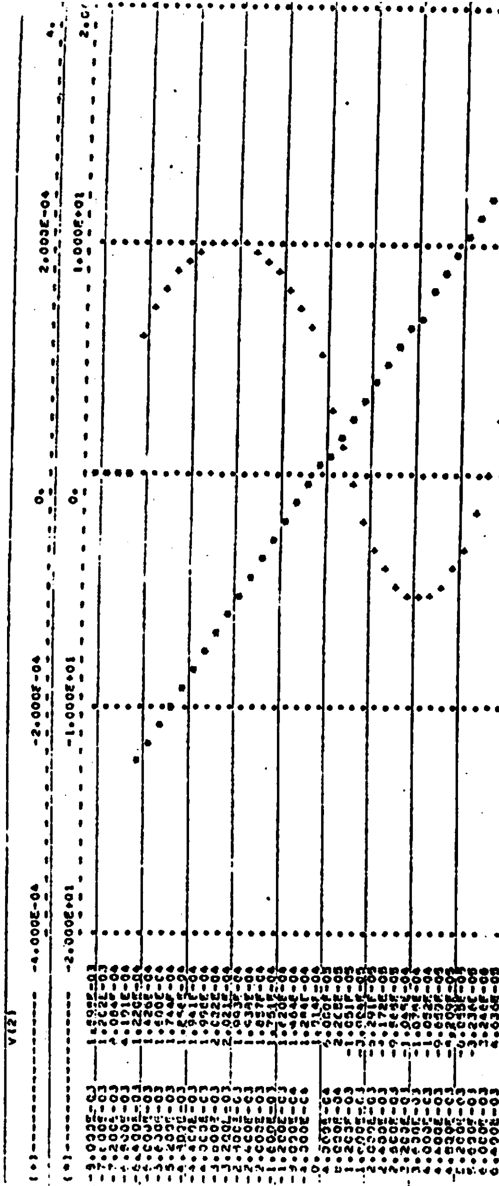
```
***************  8 JAN 77 ********************************T-SPICE 2A ******************************* 14:27:01 ***************

DC TRANSFER CURVE OF FAIRCHILD 741

                    DC TRANSFER CURVES                                    TEMPERATURE =   27.000 DEG C

****************************************************************************************************************
```

	V(2)	V(21)
-8.000E-03	1.598E-03	-1.279E+01
-7.600E-03	1.202E-03	-1.278E+01
-7.200E-03	8.094E-04	-1.277E+01
-6.800E-03	4.191E-04	-1.275E+01
-6.400E-03	1.220E-04	-1.285E+01
-6.000E-03	1.426E-04	-1.170E+01
-5.600E-03	1.600E-04	-1.087E+01
-5.200E-03	1.744E-04	-1.004E+01
-4.800E-03	1.856E-04	-9.218E+00
-4.400E-03	1.941E-04	-8.401E+00
-4.000E-03	1.996E-04	-7.590E+00
-3.600E-03	2.022E-04	-6.785E+00
-3.200E-03	2.021E-04	-5.985E+00
-2.800E-03	1.993E-04	-5.191E+00
-2.400E-03	1.938E-04	-4.402E+00
-2.000E-03	1.857E-04	-3.618E+00
-1.600E-03	1.751E-04	-2.839E+00
-1.200E-03	1.620E-04	-2.065E+00
-8.000E-04	1.464E-04	-1.296E+00
-4.000E-04	1.284E-04	-5.325E-01
[illegible]	1.014E-04	2.134E-01
4.000E-04	6.000E-05	9.308E-01
8.000E-04	2.265E-05	1.656E+00
1.200E-03	-1.051E-05	2.390E+00
1.600E-03	-3.904E-05	3.133E+00
2.000E-03	-6.291E-05	3.885E+00
2.400E-03	-8.172E-05	4.647E+00
2.800E-03	-9.568E-05	5.419E+00
3.200E-03	-1.045E-04	6.202E+00
3.600E-03	-1.078E-04	6.995E+00
4.000E-03	-1.052E-04	7.800E+00
4.400E-03	-9.699E-05	8.617E+00
4.800E-03	-8.209E-05	9.446E+00
5.200E-03	-6.055E-05	1.029E+01
5.600E-03	-3.236E-05	1.115E+01
6.000E-03	3.246E-06	1.202E+01
6.400E-03	4.636E-05	1.290E+01

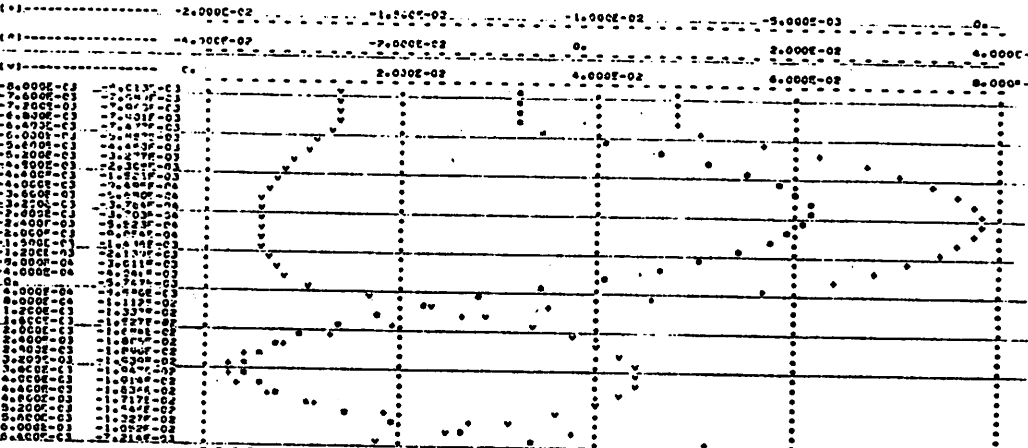


************** 8 JAN 77 *********************************T-SPICE 2A ******************************** 14:27:01 ***************

DC TRANSFER CURVE OF FAIRCHILD 741

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

	T(01)	T(03)	T(05)
-8.000E-03	-8.013E-03	-8.136E-03	1.330E-02
-7.600E-03	-7.989E-03	-8.041E-03	1.329E-02
-7.200E-03	-7.963E-03	-7.949E-03	1.328E-02
-6.800E-03	-7.901E-03	-7.739E-03	1.323E-02
-6.400E-03	-7.477E-03	-5.967E-03	1.285E-02
-6.000E-03	-5.857E-03	7.809E-04	1.134E-02
-5.600E-03	-4.460E-03	6.519E-03	1.001E-02
-5.200E-03	-3.277E-03	1.130E-02	8.867E-03
-4.800E-03	-2.308E-03	1.513E-02	7.904E-03
-4.400E-03	-1.525E-03	1.809E-02	7.092E-03
-4.000E-03	-9.495E-04	2.010E-02	6.449E-03
-3.600E-03	-5.680E-04	2.124E-02	5.971E-03
-3.200E-03	-3.744E-04	2.153E-02	5.652E-03
-2.800E-03	-3.703E-04	2.098E-02	5.490E-03
-2.400E-03	-5.523E-04	1.957E-02	5.485E-03
-2.000E-03	-9.054E-04	1.739E-02	5.623E-03
-1.600E-03	-1.436E-03	1.439E-02	5.906E-03
-1.200E-03	-2.139E-03	1.062E-02	6.338E-03
-8.000E-04	-3.011E-03	6.085E-03	6.912E-03
-4.000E-04	-4.046E-03	8.137E-04	7.629E-03
0.	-5.747E-03	-5.257E-03	1.037E-02
4.000E-04	-8.580E-03	-1.167E-02	1.717E-02
8.000E-04	-1.112E-02	-1.741E-02	2.331E-02
1.200E-03	-1.337E-02	-2.245E-02	2.874E-02
1.600E-03	-1.527E-02	-2.671E-02	3.340E-02
2.000E-03	-1.684E-02	-3.019E-02	3.727E-02
2.400E-03	-1.805E-02	-3.283E-02	4.030E-02
2.800E-03	-1.890E-02	-3.465E-02	4.253E-02
3.200E-03	-1.939E-02	-3.561E-02	4.389E-02
3.600E-03	-1.947E-02	-3.564E-02	4.432E-02
4.000E-03	-1.914E-02	-3.471E-02	4.378E-02
4.400E-03	-1.836E-02	-3.276E-02	4.223E-02
4.800E-03	-1.717E-02	-2.983E-02	3.969E-02
5.200E-03	-1.546E-02	-2.573E-02	3.597E-02
5.600E-03	-1.327E-02	-2.049E-02	3.114E-02
6.000E-03	-1.052E-02	-1.394E-02	2.505E-02
6.400E-03	-7.214E-03	-6.082E-03	1.768E-02



A2.5. Transient analysis of LM140d voltage regulator

The following deck performs a transient analysis of a commercially available LM140d voltage regulator whose amplified circuit schematic is shown in Fig. A2.5.

```
TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL     NEWTON-RAPHSON
Q1 3 2 4 MODN 2.25                X=5.00     Y=16.8
Q2 4 5 6 MODN 2.0                 X=12.2     Y=14.6
Q3 7 6 0 MODN 6.0                 X=20.0     Y=11.3
Q4 8 7 10 MODN 6.0                X=26.0     Y=11.30
Q5 9 10 11 MODN 7.0               X=35.6     Y=11.3
Q6 17 2 8 MODN 2.25               X=51.0 Y=10.0
Q7 12 9 13 MODN 2.25              X=40.8     Y=11.3
Q8 12 13 0 MODN 2.25              X=43.3     Y=11.3
Q9 14 14 0 MODN 2.25              X=48.0     Y=6
Q10 0 12 15 MODVP 6.15            X=62.0     Y=27.3
Q11 16 3 1 MODLP 3.0              X=50.7     Y=21.0
Q12 3 3 1 MODLP 3.0               X=46.4     Y=21.0
Q15 1 16 17 MODN 17.5             X=77.4     Y=42.0
Q1601 1 17 18 MODN 18.0           X=9.3      Y=42.0
Q1603 1 17 20 MODN 18.0           X=15.8     Y=42.0
Q1605 1 17 22 MODN 18.0           X=22.5     Y=42.0
Q1607 1 17 24 MODN 18.0           X=29.0     Y=42.0
Q1609 1 17 26 MODN 18.0           X=35.6     Y=42.0
Q1611 1 17 28 MODN 18.0           X=51.0     Y=42.0
Q1613 1 17 30 MODN 18.0           X=57.5     Y=42.0
Q1615 1 17 32 MODN 18.0           X=64.1     Y=42.0
Q1617 1 17 34 MODN 18.0           X=70.8     Y=42.0
R1 3 4 30K                        X=10.0     Y=21.0
R2 4 5 1.9K                       X=7.5      Y=11.0
R3 5 7 26.0                       X=16.4     Y=11.0
R4 6 0 1.2K                       X=20.5     Y=8.5
R5 10 0 12.1K                     X=39.0     Y=7.0
R6 11 0 1K                        X=38.0     Y=4.7
R7 8 9 17.7K                      X=25.0     Y=7.0
R8 13 14 4K                       X=48.0     Y=6.0
R9 15 12 4K                       X=53.5     Y=16.0
R10 16 15 850                     X=55.0     Y=20.0
R15 17 2 2K                       X=25.0     Y=26.5
R1601 18 2 3.5                    X=9.3      Y=42.0
R1603 20 2 3.5                    X=15.8     Y=42.0
R1605 22 2 3.5                    X=22.5     Y=42.0
R1607 24 2 3.5                    X=29.0     Y=42.0
R1609 26 2 3.5                    X=35.6     Y=42.0
R1611 28 2 3.5                    X=51.0     Y=42.0
R1613 30 2 3.5                    X=57.5     Y=42.0
R1615 32 2 3.5                    X=64.1     Y=42.0
R1617 34 2 3.5                    X=70.8     Y=42.0
R18 2 0 2.67K                     X=69.0     Y=6.7
VCC 1 0 10
.MODEL MODN NPN BF=100 IS=1.E-15 RB=300 RC=260 VA=200 PE=.65 ME=.5 PC=.5 MC=.3
.MODEL MODLP PNP BF=15 IS=1.5E-15 RB=200 RC=25 RE=270 VA=50 PE=.65 ME=.3 PC=.5
+ MC=.3
```



```
.MODEL MODVP PNP BF=50 IS=1.5E-15 RB=100 RC=100 RE=270 VA=80 PE=.65 ME=.3 PC=.5
+ MC=.3
IOUT 2 0 PULSE(1M 1.5 0US 10US 10US 10MS 20MS)
.PRINT TRAN V(2) V(8,9) V(11)
.PRINT TRAN V(5,6) V(6) V(7,10) V(10,11) V(2,8) V(9,13) V(13)
.PRINT TRAN T(Q3) T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.PLOT TRAN V(2) V(9) V(7) V(11)
.PLOT TRAN T(Q3) T(Q2) T(Q2,Q3)
.PLOT TRAN T(Q2,Q3) T(Q4,Q3) T(Q5,Q3) T(Q7,Q3) T(Q8,Q3) T(Q6,Q3)
.TRAN 100US 10MS
.THRML LX=86 LY=58 A0=7 B0=100 KS=.00223 KH=0.00800 GH=.02857
+TCS=27.7E-9 TCH=56.33E-9 LXHDR=500.0 LYHDR=500.0
.OPTION ACCT PDMAX=2.0 IDBUG7=1 IGRID=1
.END
  26    88
   38     1.58000E+01      5.80000E+01
   39     2.90000E+01      5.80000E+01
   40     4.35000E+01      5.80000E+01
   41     5.75000E+01      5.80000E+01
   42     7.08000E+01      5.80000E+01
   43     8.60000E+01      3.87000E+01
   44     8.60000E+01      2.00000E+01
   45     6.90000E+01      0.
   46     6.30000E+01      0.
   47     5.60000E+01      0.
   48     1.58000E+01      3.60000E+01
   49     2.28000E+01      3.58000E+01
   50     3.20000E+01      3.60000E+01
   51     4.00000E+01      3.40000E+01
   52     1.00000E+01      3.00000E+01
   53     1.77000E+01      2.58000E+01
   54     3.80000E+01      3.00000E+01
   55     5.00000E+01      2.60000E+01
   56     5.45000E+01      2.65000E+01
   57     7.08000E+01      2.73000E+01
   58     6.22000E+01      2.08000E+01
   59     6.20000E+01      1.42000E+01
   60     4.79000E+01      1.59000E+01
   61     4.20000E+01      1.70000E+01
   62     3.57000E+01      1.77000E+01
   63     2.83000E+01      1.43000E+01
   64     2.07000E+01      1.62000E+01
   65     1.64000E+01      1.62000E+01
   66     1.22000E+01      8.50000E+00
   67     1.73000E+01      8.20000E+00
   68     3.34000E+01      7.50000E+00
   69     4.13000E+01      3.90000E+00
   70     4.26000E+01      6.20000E+00
```

```
71      4.60000E+01     1.90000E+00
72      5.60000E+01     2.00000E+00
73      9.90000E+00     3.61000E+01
74      0.              3.80000E+01
75      0.              3.00000E+01
76      0.              1.60000E+01
77      2.00000E+00     1.00000E+01
78      0.              1.00000E+01
79      7.20000E+00     0.
80      1.60000E+01     0.
81      2.00000E+01     0.
82      3.00000E+01     0.
83      4.02000E+01     0.
84      4.60000E+01     0.
85      6.00000E+01     7.50000E+00
86      7.30000E+01     1.58000E+01
87      8.33081E+01     3.20143E+01
88      8.60000E+01     3.20143E+01
 1   74    2   75    3   76    4   78    5   34    6   79    7   80    8   81    9   82   10   83
11   84   12   47   13   46   14   45   15   35   16   44   17   88   18   43   19   36   20   42
21   41   22   40   23   39   24   38   25   37   26   74
 6    5    5    5    6    5    5    5    6    5
 7    5    5    6    5    6    7    5    6    4
 6    6    6    6    6    5    6    6    6    5
 6    5    6    3    4    3    3    5    5    4
 5    5    4    5    3    5    4    6    6    6
 5    5    7    7    6    7    8    6    6    6
 6    6    6    6    6    6    6    7    5    6
 7    6    6    4    6    4    6    3    8    4
 5    5    5    3    6    6    5    3
65   23   53   52   22   75
23   66   22   79   77
24   67   65   66   23
 7   25   81   24   67
28   26   70   69    6   68
69    5   68   83   82
25   68   82    4   81
71   70   29   27   72
60   31   27   85   10   59
 9   31   56   59   58
63   64   62   54   53   50   49
13   73   74   38   37
14   48   73   12   38
15   49   48   13   38   39
16   50   49   14   39
51   50   17   15   39   40
55   51   56   16   18   40   41
56   17   30   19   41
```



```
30   18   57   20   41   42
57   19   33   42
46   85   59   86   45   35
 1   73    2   75   77   76
65    3   66    1    2   22
25    4   64   67    3   65
68   63    7    4   24   64
28   62    5   68   63
 8   29   60   72    9   85
61   62   29   26    5   70
61   28   70    8   27   60
58   56   18   57   19
60   32    9   55   10   56
60   61   54   31   55
57   20   87   43   42   36
77   79   78
45   21   86   44
33   42   43
38   12   74
12   13   14   39   37
14   38   15   16   40
16   39   17   41
17   40   18   19   42
19   41   20   33   36
33   87   88   36
35   86   57   87   88
21   46   35
72   85   47   21   45
71   72   84   46
49   53   52   14   73   13
50   11   53   15   48   14
54   11   51   49   16   15
55   54   17   50   16
48   53    1   75   73
11   64   65   49    1   48   52
62   11   61   32   55   51   50
31   32   54   56   51   17
31   55   10   58   17   30   18
58   30   86   19   44   20   33   87
59   10   56   86   30   57
85    9   10   58   21   86
27   29   61   32   31    9
62   28   29   60   54   32
61   28   26   63   11   54
62   26   68   25   64   11
25   24   63   11   65   53
64   24    3   53   23    1
 3   67   80   23    2   79
```

4	81	24	3	80	66	
26	5	6	63	25	82	7
70	5	6	83	71		
5	28	29	69	71	8	
83	69	70	8	72	84	47
8	27	71	47	85	46	
48	52	75	13	12	74	
73	75	12	37			
52	1	22	73	76	74	
22	77	75	78			
22	2	79	76	78	34	
77	76	34				
66	80	2	77	34		
81	67	66	79			
7	82	4	67	80		
68	6	83	7	81		
69	6	82	71	84		
83	71	47				
72	27	9	46	59	21	
21	59	58	57	35	44	
44	57	33	43	88		
44	87	43				

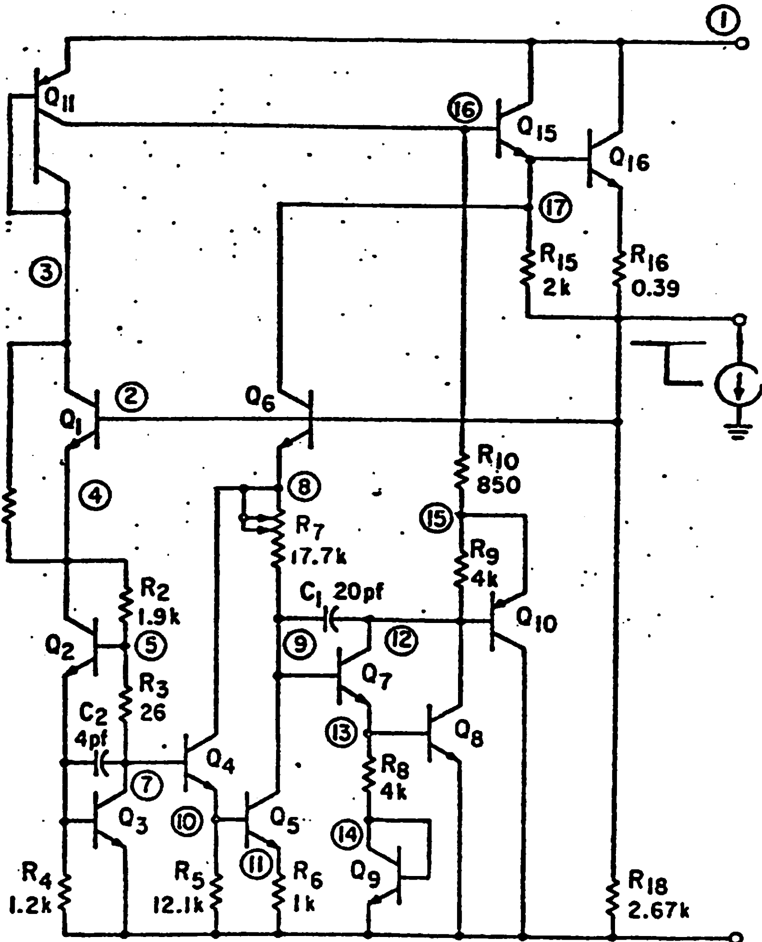
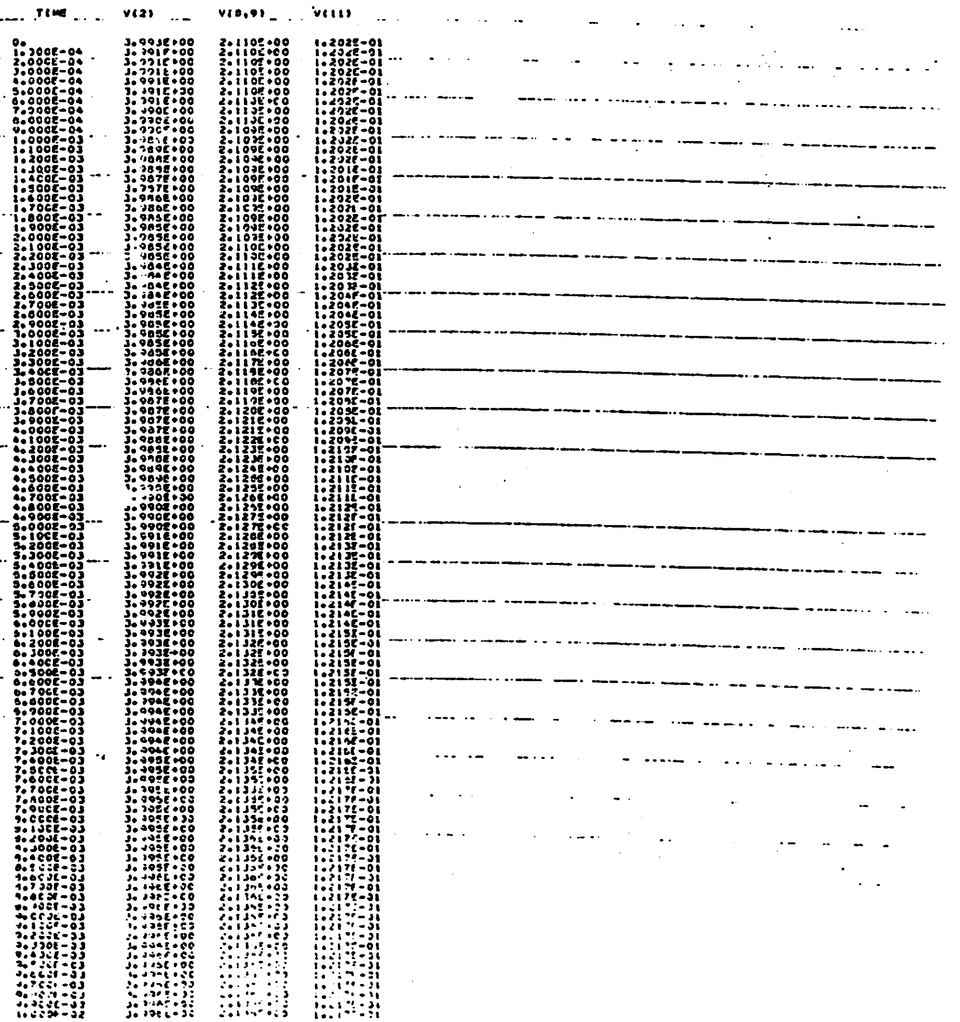


Fig. 2A.5

Simplified schematic of LM140d voltage regulator

The following is a part of the resultant output file when the above-mentioned deck is run on the program T-SPICE28.



*************** 30 NOV 76 ******************************T-SPICE 2) ********************************** 04:15:32 ***********

TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL   NEWTON-RAPHSON

TRANSIENT ANALYSIS   TEMPERATURE = 27.000 DEG C

TIME	V(2)	V(8,9)	V(11)
0.	3.993E+00	2.110E+00	1.202E-01
1.000E-04	3.991E+00	2.110E+00	1.202E-01
2.000E-04	3.991E+00	2.110E+00	1.202E-01
3.000E-04	3.991E+00	2.110E+00	1.202E-01
4.000E-04	3.991E+00	2.110E+00	1.202E-01
5.000E-04	3.991E+00	2.110E+00	1.202E-01
6.000E-04	3.991E+00	2.113E+00	1.202E-01
7.000E-04	3.990E+00	2.110E+00	1.202E-01
8.000E-04	3.990E+00	2.110E+00	1.202E-01
9.000E-04	3.990E+00	2.109E+00	1.202E-01
1.000E-03	3.989E+00	2.109E+00	1.202E-01
1.100E-03	3.989E+00	2.109E+00	1.202E-01
1.200E-03	3.988E+00	2.109E+00	1.202E-01
1.300E-03	3.989E+00	2.109E+00	1.201E-01
1.400E-03	3.987E+00	2.109E+00	1.201E-01
1.500E-03	3.987E+00	2.109E+00	1.201E-01
1.600E-03	3.986E+00	2.109E+00	1.202E-01
1.700E-03	3.986E+00	2.109E+00	1.202E-01
1.800E-03	3.985E+00	2.109E+00	1.202E-01
1.900E-03	3.985E+00	2.109E+00	1.202E-01
2.000E-03	3.985E+00	2.109E+00	1.202E-01
2.100E-03	3.985E+00	2.110E+00	1.202E-01
2.200E-03	3.985E+00	2.110E+00	1.202E-01
2.300E-03	3.984E+00	2.111E+00	1.203E-01
2.400E-03	3.984E+00	2.111E+00	1.203E-01
2.500E-03	3.984E+00	2.112E+00	1.203E-01
2.600E-03	3.984E+00	2.112E+00	1.204E-01
2.700E-03	3.985E+00	2.113E+00	1.204E-01
2.800E-03	3.985E+00	2.114E+00	1.204E-01
2.900E-03	3.985E+00	2.114E+00	1.205E-01
3.000E-03	3.985E+00	2.115E+00	1.205E-01
3.100E-03	3.985E+00	2.116E+00	1.206E-01
3.200E-03	3.985E+00	2.116E+00	1.206E-01
3.300E-03	3.986E+00	2.117E+00	1.206E-01
3.400E-03	3.986E+00	2.118E+00	1.207E-01
3.500E-03	3.986E+00	2.118E+00	1.207E-01
3.600E-03	3.986E+00	2.119E+00	1.207E-01
3.700E-03	3.987E+00	2.119E+00	1.208E-01
3.800E-03	3.987E+00	2.120E+00	1.208E-01
3.900E-03	3.987E+00	2.121E+00	1.209E-01
4.000E-03	3.987E+00	2.121E+00	1.209E-01
4.100E-03	3.988E+00	2.122E+00	1.209E-01
4.200E-03	3.989E+00	2.123E+00	1.210E-01
4.300E-03	3.988E+00	2.123E+00	1.210E-01
4.400E-03	3.989E+00	2.124E+00	1.210E-01
4.500E-03	3.989E+00	2.125E+00	1.211E-01
4.600E-03	3.990E+00	2.125E+00	1.211E-01
4.700E-03	3.990E+00	2.126E+00	1.211E-01
4.800E-03	3.990E+00	2.126E+00	1.212E-01
4.900E-03	3.990E+00	2.127E+00	1.212E-01
5.000E-03	3.990E+00	2.127E+00	1.212E-01
5.100E-03	3.991E+00	2.128E+00	1.212E-01
5.200E-03	3.991E+00	2.128E+00	1.213E-01
5.300E-03	3.991E+00	2.129E+00	1.213E-01
5.400E-03	3.991E+00	2.129E+00	1.213E-01
5.500E-03	3.992E+00	2.129E+00	1.213E-01
5.600E-03	3.992E+00	2.130E+00	1.214E-01
5.700E-03	3.992E+00	2.130E+00	1.214E-01
5.800E-03	3.992E+00	2.130E+00	1.214E-01
5.900E-03	3.992E+00	2.131E+00	1.214E-01
6.000E-03	3.993E+00	2.131E+00	1.214E-01
6.100E-03	3.993E+00	2.131E+00	1.215E-01
6.200E-03	3.993E+00	2.132E+00	1.215E-01
6.300E-03	3.993E+00	2.132E+00	1.215E-01
6.400E-03	3.993E+00	2.132E+00	1.215E-01
6.500E-03	3.993E+00	2.132E+00	1.215E-01
6.600E-03	3.994E+00	2.133E+00	1.215E-01
6.700E-03	3.994E+00	2.133E+00	1.215E-01
6.800E-03	3.994E+00	2.133E+00	1.215E-01
6.900E-03	3.994E+00	2.133E+00	1.215E-01
7.000E-03	3.994E+00	2.134E+00	1.215E-01
7.100E-03	3.994E+00	2.134E+00	1.216E-01
7.200E-03	3.994E+00	2.134E+00	1.216E-01
7.300E-03	3.994E+00	2.134E+00	1.216E-01
7.400E-03	3.995E+00	2.134E+00	1.216E-01
7.500E-03	3.995E+00	2.135E+00	1.216E-01
7.600E-03	3.995E+00	2.135E+00	1.216E-01
7.700E-03	3.995E+00	2.135E+00	1.217E-01
7.800E-03	3.995E+00	2.135E+00	1.217E-01
7.900E-03	3.995E+00	2.135E+00	1.217E-01
8.000E-03	3.995E+00	2.135E+00	1.217E-01
8.100E-03	3.995E+00	2.135E+00	1.217E-01
8.200E-03	3.995E+00	[illegible]	1.217E-01
8.300E-03	3.995E+00	[illegible]	1.217E-01
8.400E-03	3.995E+00	2.135E+00	1.217E-01
8.500E-03	3.995E+00	[illegible]	1.217E-01
8.600E-03	3.996E+00	[illegible]	1.217E-01
8.700E-03	[illegible]	[illegible]	1.217E-01
8.800E-03	[illegible]	[illegible]	1.217E-01
8.900E-03	[illegible]	[illegible]	[illegible]
9.000E-03	[illegible]	[illegible]	[illegible]
9.100E-03	[illegible]	[illegible]	[illegible]
9.200E-03	[illegible]	[illegible]	[illegible]
9.300E-03	[illegible]	[illegible]	[illegible]
9.400E-03	[illegible]	[illegible]	[illegible]
9.500E-03	[illegible]	[illegible]	[illegible]
9.600E-03	[illegible]	[illegible]	[illegible]
9.700E-03	[illegible]	[illegible]	[illegible]
9.800E-03	[illegible]	[illegible]	[illegible]
9.900E-03	[illegible]	[illegible]	[illegible]
1.000E-02	[illegible]	[illegible]	[illegible]

*************** 30 NOV 76 ********************************T-SPICE 2D ******************************** 04:35:32 ******

TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL   NEWTON-RAPHSON

TRANSIENT ANALYSIS   TEMPERATURE = 27.300 DEG C

TIME	V(5,6)	V(6)	V(7,10)	V(10,11)	V(2,6)	V(9,13)	V(13)
0.	6.806E-01	6.675E-01	5.937E-01	6.075E-01	6.475E-01	5.871E-01	6.481E-01
1.000E-04	6.806E-01	6.675E-01	5.939E-01	6.075E-01	6.474E-01	5.866E-01	6.472E-01
2.000E-04	6.806E-01	6.675E-01	5.939E-01	6.075E-01	6.474E-01	5.865E-01	6.472E-01
3.000E-04	6.806E-01	6.675E-01	5.939E-01	6.075E-01	6.474E-01	5.865E-01	6.472E-01
4.000E-04	6.806E-01	6.674E-01	5.938E-01	6.075E-01	6.474E-01	5.865E-01	6.471E-01
5.000E-04	6.806E-01	6.674E-01	5.938E-01	6.075E-01	6.474E-01	5.865E-01	6.471E-01
6.000E-04	6.805E-01	6.674E-01	5.938E-01	6.075E-01	6.474E-01	5.865E-01	6.471E-01
7.000E-04	6.805E-01	6.674E-01	5.938E-01	6.074E-01	6.473E-01	5.865E-01	6.470E-01
8.000E-04	6.804E-01	6.673E-01	5.937E-01	6.074E-01	6.473E-01	5.864E-01	6.469E-01
9.000E-04	6.803E-01	6.672E-01	5.936E-01	6.073E-01	6.473E-01	5.863E-01	6.468E-01
1.000E-03	6.802E-01	6.672E-01	5.935E-01	6.072E-01	6.472E-01	5.862E-01	6.467E-01
1.100E-03	6.800E-01	6.671E-01	5.934E-01	6.071E-01	6.471E-01	5.861E-01	6.466E-01
1.200E-03	6.799E-01	6.670E-01	5.933E-01	6.070E-01	6.470E-01	5.859E-01	6.465E-01
1.300E-03	6.797E-01	6.669E-01	5.932E-01	6.068E-01	6.469E-01	5.858E-01	6.463E-01
1.400E-03	6.795E-01	6.667E-01	5.930E-01	6.067E-01	6.468E-01	5.856E-01	6.462E-01
1.500E-03	6.794E-01	6.666E-01	5.927E-01	6.066E-01	6.467E-01	5.854E-01	6.460E-01
1.600E-03	6.792E-01	6.665E-01	5.927E-01	6.064E-01	6.465E-01	5.853E-01	6.459E-01
1.700E-03	6.790E-01	6.663E-01	5.925E-01	6.062E-01	6.464E-01	5.851E-01	6.457E-01
1.800E-03	6.789E-01	6.662E-01	5.924E-01	6.061E-01	6.463E-01	5.849E-01	6.455E-01
1.900E-03	6.785E-01	6.660E-01	5.922E-01	6.059E-01	6.461E-01	5.846E-01	6.453E-01
2.000E-03	6.784E-01	6.659E-01	5.920E-01	6.057E-01	6.460E-01	5.844E-01	6.451E-01
2.100E-03	6.782E-01	6.657E-01	5.919E-01	6.055E-01	6.458E-01	5.842E-01	6.449E-01
2.200E-03	6.780E-01	6.656E-01	5.916E-01	6.053E-01	6.457E-01	5.840E-01	6.447E-01
2.300E-03	6.778E-01	6.654E-01	5.914E-01	6.051E-01	6.455E-01	5.838E-01	6.446E-01
2.400E-03	6.777E-01	6.653E-01	5.912E-01	6.050E-01	6.454E-01	5.836E-01	6.444E-01
2.500E-03	6.775E-01	6.651E-01	5.910E-01	6.048E-01	6.452E-01	5.834E-01	6.442E-01
2.600E-03	6.773E-01	6.650E-01	5.909E-01	6.046E-01	6.451E-01	5.832E-01	6.440E-01
2.700E-03	6.771E-01	6.648E-01	5.906E-01	6.044E-01	6.449E-01	5.830E-01	6.439E-01
2.800E-03	6.769E-01	6.647E-01	5.905E-01	6.043E-01	6.448E-01	5.829E-01	6.436E-01
2.900E-03	6.768E-01	6.645E-01	5.903E-01	6.041E-01	6.446E-01	5.826E-01	6.435E-01
3.000E-03	6.766E-01	6.644E-01	5.901E-01	6.039E-01	6.445E-01	5.824E-01	6.433E-01
3.100E-03	6.765E-01	6.643E-01	5.899E-01	6.037E-01	6.443E-01	5.822E-01	6.431E-01
3.200E-03	6.763E-01	6.641E-01	5.897E-01	6.036E-01	6.442E-01	5.820E-01	6.430E-01
3.300E-03	6.762E-01	6.640E-01	5.896E-01	6.034E-01	6.441E-01	5.818E-01	6.428E-01
3.400E-03	6.760E-01	6.639E-01	5.894E-01	6.033E-01	6.440E-01	5.817E-01	6.427E-01
3.500E-03	6.759E-01	6.638E-01	5.893E-01	6.032E-01	6.439E-01	5.815E-01	6.425E-01
3.600E-03	6.758E-01	6.637E-01	5.892E-01	6.030E-01	6.437E-01	5.814E-01	6.424E-01
3.700E-03	6.757E-01	6.636E-01	5.890E-01	6.029E-01	6.436E-01	5.812E-01	6.423E-01
3.800E-03	6.755E-01	6.635E-01	5.889E-01	6.028E-01	6.435E-01	5.811E-01	6.421E-01
3.900E-03	6.755E-01	6.634E-01	5.888E-01	6.027E-01	6.434E-01	5.809E-01	6.420E-01
4.000E-03	6.754E-01	6.633E-01	5.887E-01	6.026E-01	6.433E-01	5.808E-01	6.419E-01
4.100E-03	6.753E-01	6.632E-01	5.885E-01	6.024E-01	6.432E-01	5.807E-01	6.418E-01
4.200E-03	6.752E-01	6.631E-01	5.884E-01	6.023E-01	6.431E-01	5.806E-01	6.417E-01
4.300E-03	6.751E-01	6.631E-01	5.883E-01	6.022E-01	6.430E-01	5.804E-01	6.416E-01
4.400E-03	6.750E-01	6.630E-01	5.882E-01	6.021E-01	6.430E-01	5.803E-01	6.415E-01
4.500E-03	6.749E-01	6.629E-01	5.881E-01	6.021E-01	6.429E-01	5.802E-01	6.414E-01
4.600E-03	6.749E-01	6.628E-01	5.880E-01	6.020E-01	6.428E-01	5.801E-01	6.413E-01
4.700E-03	6.748E-01	6.628E-01	5.879E-01	6.019E-01	6.427E-01	5.800E-01	6.412E-01
4.800E-03	6.747E-01	6.627E-01	5.878E-01	6.019E-01	6.426E-01	5.799E-01	6.411E-01
4.900E-03	6.746E-01	6.626E-01	5.877E-01	6.017E-01	6.426E-01	5.798E-01	6.410E-01
5.000E-03	6.746E-01	6.626E-01	5.877E-01	6.016E-01	6.425E-01	5.797E-01	6.409E-01
5.100E-03	6.745E-01	6.625E-01	5.876E-01	6.016E-01	6.424E-01	5.796E-01	6.409E-01
5.200E-03	6.745E-01	6.625E-01	5.875E-01	6.015E-01	6.424E-01	5.796E-01	6.408E-01
5.300E-03	6.744E-01	6.624E-01	5.874E-01	6.014E-01	6.423E-01	5.795E-01	6.407E-01
5.400E-03	6.743E-01	6.624E-01	5.874E-01	6.014E-01	6.423E-01	5.794E-01	6.406E-01
5.500E-03	6.743E-01	6.623E-01	5.873E-01	6.013E-01	6.422E-01	5.793E-01	6.406E-01
5.600E-03	6.743E-01	6.623E-01	5.873E-01	6.012E-01	6.422E-01	5.793E-01	6.405E-01
5.700E-03	6.742E-01	6.622E-01	5.872E-01	6.012E-01	6.421E-01	5.792E-01	6.405E-01
5.800E-03	6.742E-01	6.622E-01	5.871E-01	6.011E-01	6.421E-01	5.792E-01	6.404E-01
5.900E-03	6.741E-01	6.622E-01	5.871E-01	6.011E-01	6.420E-01	5.791E-01	6.404E-01
6.000E-03	6.741E-01	6.621E-01	5.871E-01	6.011E-01	6.420E-01	5.791E-01	6.403E-01
6.100E-03	6.741E-01	6.621E-01	5.870E-01	6.010E-01	6.419E-01	5.790E-01	6.403E-01
6.200E-03	6.741E-01	6.621E-01	5.870E-01	6.010E-01	6.419E-01	5.790E-01	6.402E-01
6.300E-03	6.740E-01	6.621E-01	5.870E-01	6.010E-01	6.419E-01	5.790E-01	6.402E-01
6.400E-03	6.740E-01	6.621E-01	5.869E-01	6.009E-01	6.419E-01	5.789E-01	6.402E-01
6.500E-03	6.740E-01	6.620E-01	5.869E-01	6.009E-01	6.418E-01	5.789E-01	6.402E-01
6.600E-03	6.740E-01	6.620E-01	5.869E-01	6.009E-01	6.418E-01	5.789E-01	6.401E-01
6.700E-03	6.740E-01	6.620E-01	5.869E-01	6.009E-01	6.418E-01	5.788E-01	6.401E-01
6.800E-03	6.740E-01	6.620E-01	5.868E-01	6.009E-01	6.418E-01	5.788E-01	6.401E-01
6.900E-03	6.740E-01	6.620E-01	5.868E-01	6.008E-01	6.418E-01	5.788E-01	6.401E-01
7.000E-03	6.739E-01	6.620E-01	5.868E-01	6.008E-01	6.417E-01	5.788E-01	6.400E-01
7.100E-03	6.739E-01	6.619E-01	5.868E-01	6.008E-01	6.417E-01	5.787E-01	6.400E-01
7.200E-03	6.739E-01	6.619E-01	5.867E-01	6.007E-01	6.417E-01	5.787E-01	6.400E-01
7.300E-03	6.739E-01	6.619E-01	5.867E-01	6.007E-01	6.417E-01	5.787E-01	6.400E-01
7.400E-03	6.739E-01	6.619E-01	5.867E-01	6.007E-01	6.417E-01	5.787E-01	6.399E-01
7.500E-03	6.738E-01	6.619E-01	5.867E-01	6.007E-01	6.416E-01	5.786E-01	6.399E-01
7.600E-03	6.738E-01	6.619E-01	5.866E-01	6.006E-01	6.416E-01	5.786E-01	6.399E-01
7.700E-03	6.738E-01	6.618E-01	5.866E-01	6.006E-01	6.416E-01	5.786E-01	6.399E-01
7.800E-03	6.738E-01	6.618E-01	5.866E-01	6.006E-01	6.415E-01	5.785E-01	6.398E-01
7.900E-03	6.737E-01	6.618E-01	5.865E-01	6.006E-01	6.415E-01	5.785E-01	6.398E-01
8.000E-03	6.737E-01	6.618E-01	5.865E-01	6.006E-01	6.415E-01	5.785E-01	6.398E-01
8.100E-03	6.737E-01	6.618E-01	5.865E-01	6.005E-01	6.415E-01	5.785E-01	6.398E-01
8.200E-03	6.737E-01	6.618E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.300E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.400E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.500E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.600E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.700E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.800E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.900E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.000E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.100E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.200E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.300E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.400E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.500E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.600E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.700E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.800E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.900E-03	6.737E-01	6.617E-01	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.000E-02	6.737E-01	6.617E-01	5.860E-01	[illegible]	6.414E-01	[illegible]	[illegible]

*************** 30 NOV 76 ********************************T-SPICE 2D ******************************** 04:35:32 ******

TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL   NEWTON-RAPHSON

TRANSIENT ANALYSIS   TEMPERATURE = 27.000 DEG C

TIME	T(03)	T(02)	T(04)	T(05)	T(07)	T(08)	T(06)
0.	2.778E+01	4.984E-02	-3.964E-02	-4.779E-02	-3.324E-02	-2.140E-02	-1.217E-02
1.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.000E-04	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
4.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
5.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
7.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.000E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.100E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.200E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.300E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.400E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.500E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.600E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.700E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.800E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
9.900E-03	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.000E-02	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

************** 30 NOV 76 ****************************T-SPICE 2D **************************** 04135132 **************

TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL NEWTON RAPHSON

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

LEGEND:
*: V(2)
+: V(9)
=: V(7)
<: V(11)

TIME V(2)

(*)---------- 3.980E+00 3.985E+00 3.990E+00 3.995E+00 4.000E+00

(+)---------- 1.210E+00 1.220E+00 1.230E+00 1.240E+00 1.250E+00

(=)---------- 1.305E+00 1.310E+00 1.315E+00 1.320E+00 1.325E+00

(<)---------- 1.200E-01 1.205E-01 1.210E-01 1.215E-01 1.220E-01

************** 30 NOV 76 ****************************T-SPICE 2D **************************** 04135132 **************

TRANSIENT ANALYSIS OF VOLTAGE REGULATOR ---NATIONAL NEWTON-RAPHSON

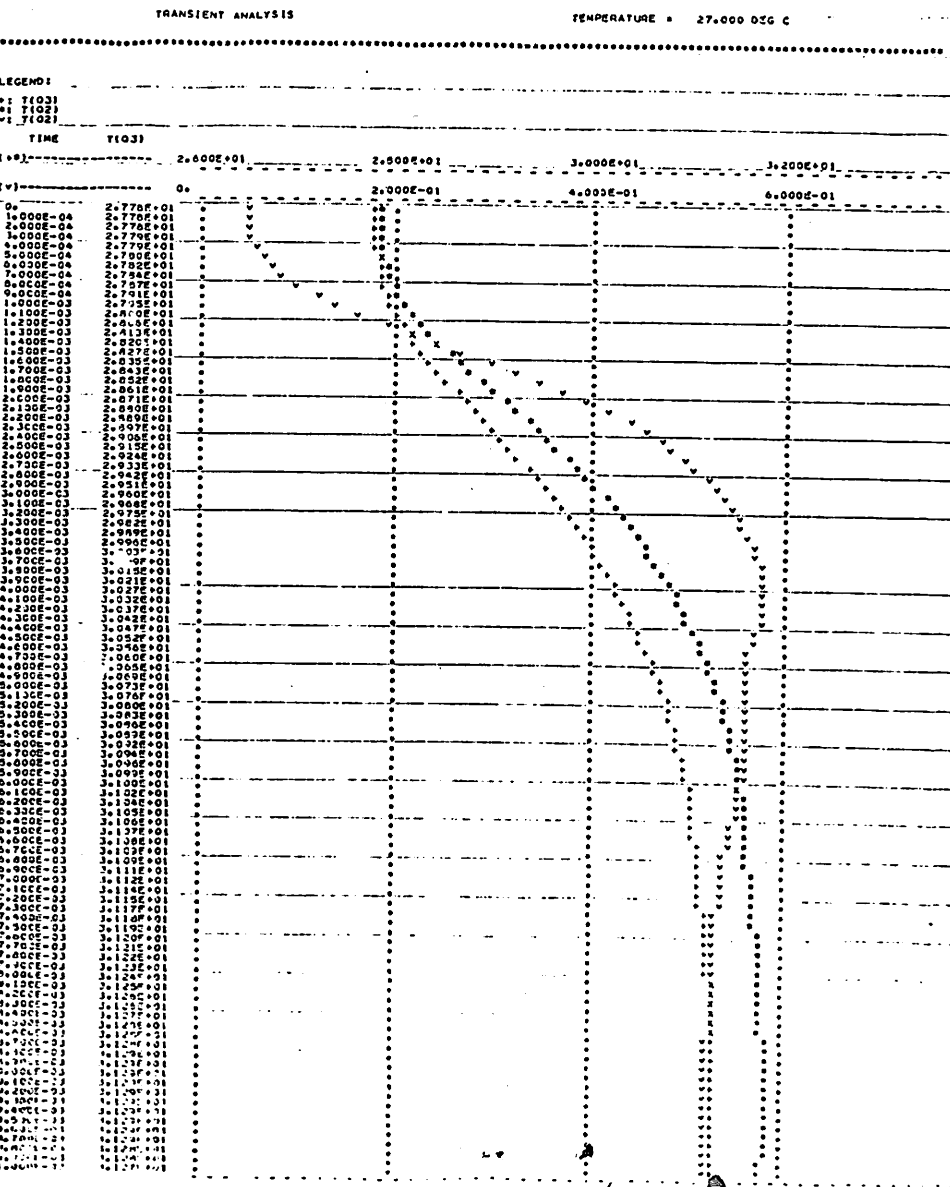
TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

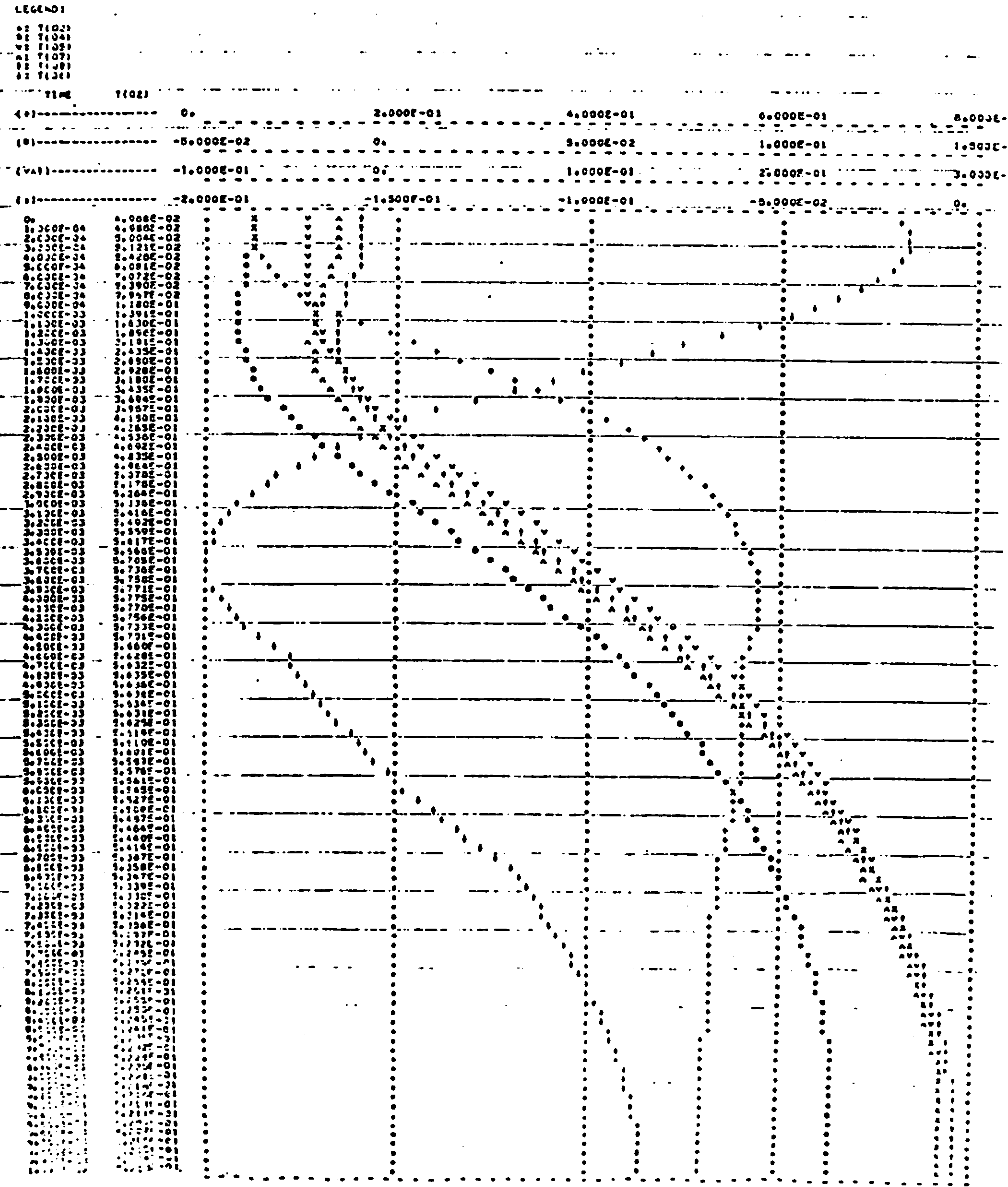
LEGEND:
*: T(03)
+: T(02)
=: T(02)

TIME T(03)

(*)---------- 2.600E+01 2.800E+01 3.000E+01 3.200E+01 3.400E+01

(=)---------- 0. 2.000E-01 4.000E-01 6.000E-01 8.000E-01





A2-6. dc transfer curve of LM199 TSS circuit

The following deck performs a dc transfer curve analysis of a temperature stabilized substrate circui as an ambient temperature is changed from -50°C to 100°C with a temperature step of 10°C. The schematic of the circuit is shown in Fig. A2.6. Notice in this case IGRID = 1 is specified in the option card. The data following .END card is t e deck punched by T-SPICE2C and contains information concerning thermal network formed by T-SPICE2C.

```
DC TRANSFER CURVE OF TSS LM400
Q1 1 3 0 MODN 9.0                        X=51.0     Y=45.0
Q2 3 2 1 MODP 1.0                        X=45.0    Y=28.0
Q3 11 11 1 MODN 1.0                      X=45.0    Y=28.0
Q4 2 4 0 MODN 1.0                        X=33.35    Y=30.25
Q5 6 7 13 MODN 14.5                      X=33.0     Y=42.0
Q6 7 8 0 MODN 1.0                        X=25.2     Y=44.0
Q7 9 6 12 MODN 2.0                       X=16.9     Y=30.2
Q9 9 9 11 MODP 1.0                       X=5.0      Y=40.0
Z1 11 6 6.3      TC=2M                   X=30.0      Y=30.2
R3 4 6 20K                               X=25.2     Y=39.3
R6 6 0 2K                                X=25.2     Y=39.3
R7 13 0 450.                             X=20.0     Y=48.0
R8 8 7 2.4K                              X=25.2      Y=44.0
R9 12 0 2.6K                             X=16.9     Y=30.2
R10 10 11 10K                            X=7.0      Y=48.0
Q14A 2 9 10 MODP 5.0                     X=17.0     Y=40.0
Q14B 8 9 10 MODP 3.0                     X=17.0     Y=40.0
R11 3 0 30K                              X=50.0    Y=35.3
Q12 25 16 14 MODN 2.0                    X=31.1        Y=16.3
Q13 16 18 24 MODN 2.0                   X=23.1     Y=31.0
Q14 21 22 20 MODN 1.0                    X=23.1    Y=16.1
Q15A 22 21 25 MODP .5                     X=23.1     Y=16.1
Q15B 21 21 25 MODP .5                     X=23.1     Y=16.1
Q16 23 23 22 MODN 1.0                     X=5.75     Y=30.75
Q18 16 17 24 MODN 1.0                   X=45.0     Y=16.0
Q19A 16 19 20 MODP 1.0                  X=10.5     Y=23.0
Q19B 19 19 20 MODP 1.0                  X=10.5     Y=23.0
Z2 22 24 6.3     TC=2M                   X=14.3     Y=15.8
Z3 23 24 6.3     TC=2M                   X=5.75     Y=30.75
R12 15 24 6.0                            X=49.5        Y=12.2
R13 15 17 10K                            X=49.5        Y=12.2
R14 18 24 1.15K                          X=27.0      Y=23.0
R15 18 19 10.5K                          X=27.0      Y=23.0
RSET 25 23 50K
REXT 25 11 20K
Q1101 25 14 15 MODN 4.0                   X=5.5      Y=7.8
Q1103 25 14 15 MODN 4.0                    X=9.9     Y=7.8
Q1105 25 14 15 MODN 4.0                    X=14.3    Y=7.8
Q1107 25 14 15 MODN 4.0                    X=18.7    Y=7.8
Q1109 25 14 15 MODN 4.0                    X=23.1    Y=7.8
Q1111 25 14 15 MODN 4.0                    X=27.5    Y=7.8
Q1113 25 14 15 MODN 4.0                    X=31.9    Y=7.8
Q1115 25 14 15 MODN 4.0                    X=36.3    Y=7.8
Q1117 25 14 15 MODN 4.0                    X=40.7    Y=7.8
Q1119 25 14 15 MODN 4.0                    X=45.1    Y=7.8
Q1121 25 14 15 MODN 4.0                    X=49.5    Y=7.8
VCC 25 0 15.0

VEE 24 0 -15.0
.MODEL MODN NPN BF=100 IS=1.E-15 RB=300 RC=250 VA=200
.MODEL MODP PNP BF=15 IS=1.E-15 RB=200 RC=25 RE=270 VA=50
.THRML LX=55 LY=53 A0=10. B0=50 KS=2.23E-03 KH=4.5E-04 TCS=2.E-09
+TCH=2.E-09 GH=.005 LXHDR=110 LYHDR=106
.OP
.PRINT DC V(11) V(11,6) V(6) V(18) V(22)
.PRINT DC T(Z1) T(Q4) T(Q13) T(Q1101) T(Q1111) T(Q1121)
.PLOT DC V(11) V(11,6) V(6) V(18) V(22)
.PLOT DC T(Z1) T(Q4) T(Q13) T(Q1101) T(Q1111) T(Q1121)
.DC TAMB -50 100 10
.OPTION ACCT IDBUG7=1 IGRID . PDMAX=.1 TOP=107
.END
   23   62
   38      8.00000E+00      5.30000E+01
   39      2.10000E+01      5.30000E+01
   40      3.90000E+01      5.30000E+01
   41      5.00000E+01      5.30000E+01
   42      2.80000E+01      5.00000E+01
   43      3.90000E+01      5.00000E+01
   44      5.50000E+01      4.60000E+01
   45      5.50000E+01      3.70000E+01
   46      4.50000E+01      3.80000E+01
   47      0.               4.20000E+01
   48      0.               3.28000E+01
   49      0.               2.08000E+01
   50      2.00000E+01      2.30000E+01
   51      3.30000E+01      2.30000E+01
   52      5.50000E+01      2.50000E+01
   53      3.63000E+01      1.60000E+01
   54      7.00000E+00      1.60000E+01
   55      0.               1.10000E+01
   56      5.50000E+01      1.10000E+01
   57      4.51000E+01      0.
   58      3.63000E+01      0.
   59      2.75000E+01      0.
   60      1.87000E+01      0.
   61      9.90000E+00      0.
   62      2.80000E+01      5.30000E+01
    1   47    2   48    3   49    4   55    5   34    6   61    7   60    8   59    9   58   10   5
   11   35   12   56   13   52   14   45   15   44   16   36   17   41   18   40   19   62   20   3
   21   38   22   37   23   47
    5    6    5    5    6    5    5    6    6    7
    5    7    5    8    6    6    7    6    6    5
    6    5    5    5    5    5    6    4    6    5
    6    6    7    3    3    2    3    4    4    4
    5    7    6    4    4    6    4    4    5    6
    6    6    7    6    4    4    5    5    5    5
```

```
 5    3
16   14   32   12    3
 3   14    5   42   39   38
12    1   14    2   42
50   16   20   18   14
14   13    2   47   38   37
10   46   52    9   45
19   30   52   31   56
51   15   17   50   32   16
46   43    6   45   41   44
51   11   53   19   52   46    6
32   51   10   12   46
32    1   11   46    3   42   43
18   48   14    5   47
 4   18   13   16    1    3    2    5
51    8   53   17   26   27
32    8   50    4   14    1
15    8   50   33   24   25   26
20   49    4   48   13   14
10   53   29   30    7   52
50   33    4   54   49   18
22   54   55   61   34
33   54   23   21   61
22   33   24   60   61
23   33   17   25   60
24   17   26   59   60
25   17   15   27   59
26   15   53   28   58   59
27   53   29   58
28   53   19   30   57   58
19   29    7   31   57
 7   30   56   57   35
 8   51   16   11    1   12
17   50   20   54   22   23   24
21   61   55
57   31   56
41   44
38    5   47
 2    5   39   37
 2   42   38   62
42   43   41   62
 9   43   40   44   36
 3    2   12   43   40   39   62
12   42   46    9   40   41
45    9   41   36
 6    9   52   44
10   11   12    6   43    9
13   48    5   37
```



```
49   18   13   47
54   55   20   18   48
17    8   16    4   33   20
 8   15   53   32   11   10
19   10    7   56    6   45
51   15   10   19   27   28   29
33   20   22   21   55   49
21   54   49   34
31    7   52   35
30   29   31   58   35
29   57   28   27   59
27   58   26   25   60
25   59   24   23   61
23   60   22   21   34
40   42   39
```

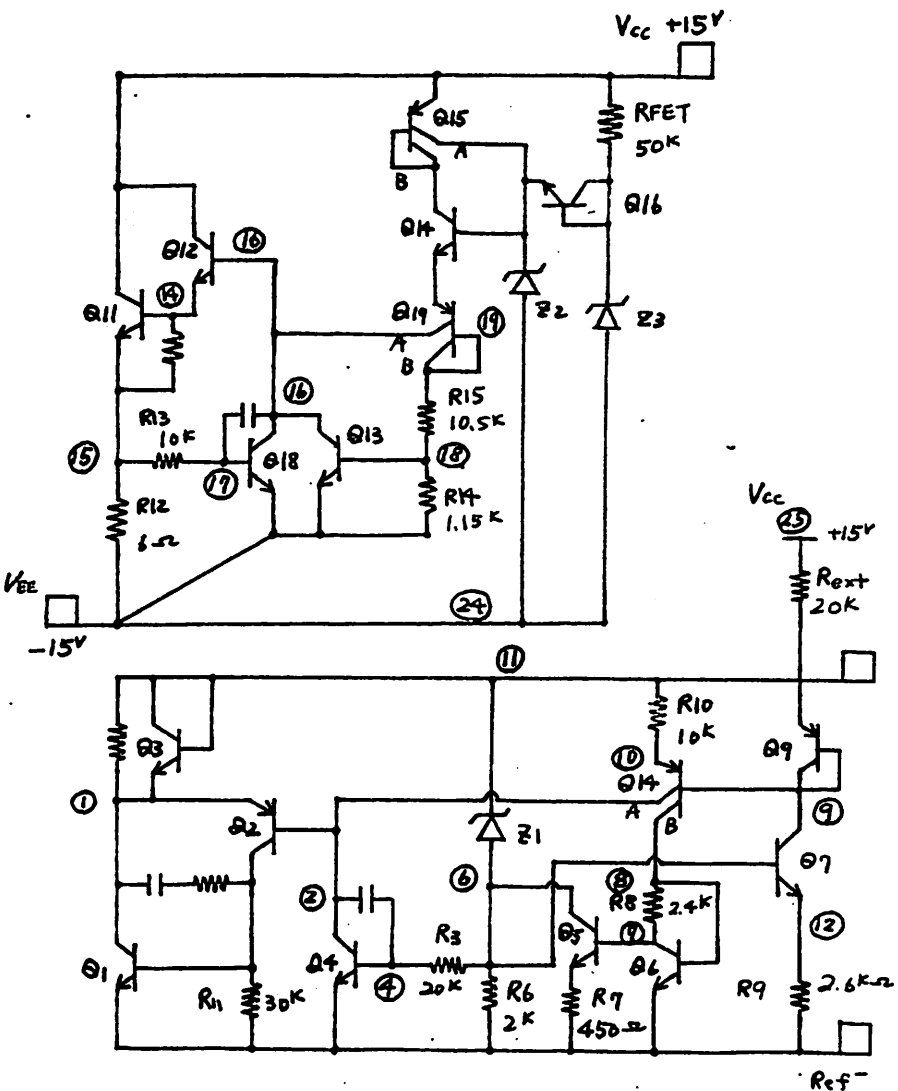


Fig. A2.6

Schematic of LM199 TSS system

The following is a part of resultant output file when the above-mentioned deck is run on the program T-SPICE2B.

**************** 22 NOV 75 ********************************T-SPICE 2B **

DC TRANSFER CURVE OF TSS LM400

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

TAMB	V(11)	V(11,4)	V(C)	V(18)	V(22)
-5.000E+01	6.870E+00	6.340E+00	1.017E-01	-1.448E+01	-9.512E+00
-4.000E+01	[illegible]	6.440E+00	3.897E-01	-1.449E+01	[illegible]
-3.000E+01	[illegible]	6.440E+00	3.895E-01	-1.449E+01	[illegible]
-2.000E+01	[illegible]	6.440E+00	3.894E-01	-1.448E+01	[illegible]
-1.000E+01	[illegible]	6.440E+00	3.883E-01	-1.449E+01	[illegible]
0.	[illegible]	6.440E+00	3.892E-01	-1.448E+01	[illegible]
1.000E+01	[illegible]	6.440E+00	1.884E-01	-1.448E+01	[illegible]
2.000E+01	[illegible]	6.440E+00	1.990E-01	-1.448E+01	[illegible]
3.000E+01	[illegible]	6.440E+00	1.840E-01	-1.448E+01	[illegible]
4.000E+01	[illegible]	6.440E+00	[illegible]	-1.449E+01	[illegible]
5.000E+01	[illegible]	6.440E+00	[illegible]	-1.449E+01	[illegible]
6.000E+01	[illegible]	6.440E+00	[illegible]	-1.448E+01	[illegible]
7.000E+01	[illegible]	6.440E+00	[illegible]	-1.448E+01	[illegible]
8.000E+01	[illegible]	6.440E+00	[illegible]	-1.448E+01	[illegible]
9.000E+01	[illegible]	6.440E+00	[illegible]	-1.448E+01	[illegible]
1.000E+02	[illegible]	6.440E+00	[illegible]	-1.448E+01	[illegible]

241

**************** 22 NOV 76 ********************************T-SPICE 2B **

DC TRANSFER CURVE OF TSS LM400

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

TAMB	T(Z1)	T(Q4)	T(Q13)	T(Q110)	T(Q111)	T(Q112)
-5.000E+01	1.169E+02	1.169E+02	1.164E+02	1.229E+02	1.255E+02	1.226E+02
-4.000E+01	1.170E+02	1.160E+02	1.166E+02	1.225E+02	1.250E+02	1.223E+02
-3.000E+01	1.173E+02	1.169E+02	1.168E+02	1.221E+02	1.243E+02	1.220E+02
-2.000E+01	1.171E+02	1.170E+02	1.169E+02	1.214E+02	1.240E+02	1.215E+02
-1.000E+01	1.171E+02	1.170E+02	1.170E+02	1.215E+02	1.235E+02	1.213E+02
0.	1.171E+02	1.171E+02	1.170E+02	1.212E+02	1.210E+02	1.210E+02
1.000E+01	1.171E+02	1.171E+02	1.171E+02	1.209E+02	1.225E+02	1.206E+02
2.000E+01	1.172E+02	1.171E+02	1.171E+02	1.205E+02	1.220E+02	1.203E+02
3.000E+01	1.173E+02	1.172E+02	1.172E+02	1.202E+02	1.215E+02	1.200E+02
4.000E+01	1.171E+02	1.172E+02	1.172E+02	1.199E+02	1.210E+02	[illegible]
5.000E+01	1.171E+02	1.173E+02	1.173E+02	1.196E+02	1.205E+02	1.193E+02
6.000E+01	1.172E+02	1.173E+02	1.174E+02	1.192E+02	1.201E+02	[illegible]
7.000E+01	1.174E+02	1.174E+02	1.174E+02	1.189E+02	1.196E+02	1.197E+02
8.000E+01	1.175E+02	1.174E+02	1.175E+02	1.186E+02	1.191E+02	1.191E+02
9.000E+01	1.175E+02	1.175E+02	1.177E+02	1.183E+02	1.185E+02	1.180E+02
1.000E+02	1.175E+02	1.175E+02	1.176E+02	1.179E+02	1.182E+02	1.177E+02

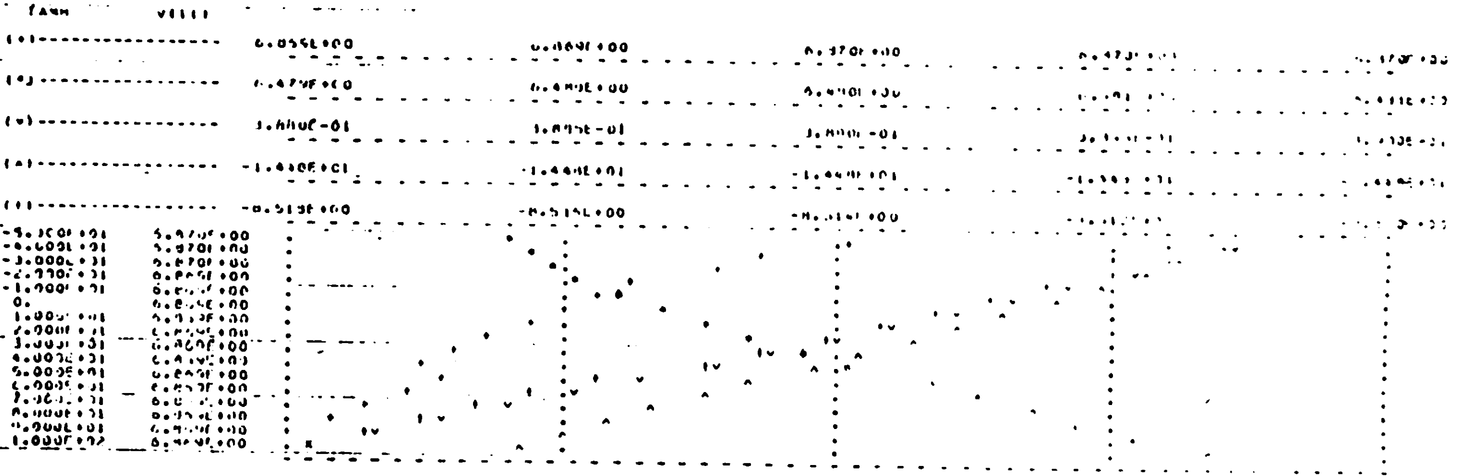
22 NOV 78 SPICE 20

DC TRANSFER CURVE OF TSS L4400

DC TRANSFER CURVES

LEGEND:

V(11)
V(11,9)
V(5)
V(14)
V(22)



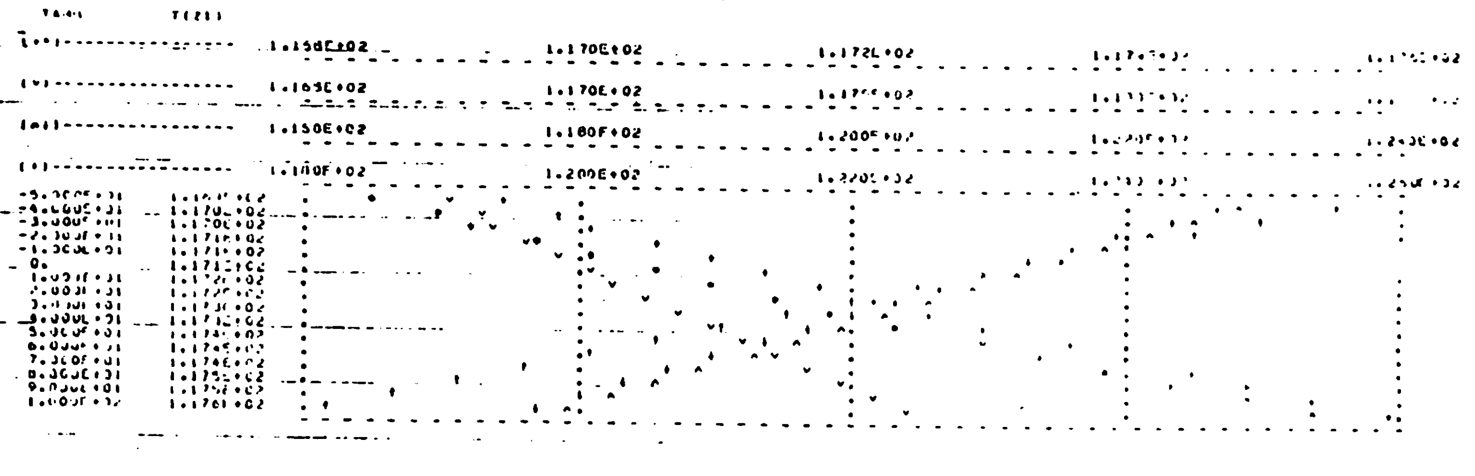
22 NOV 78 SPICE 20

DC TRANSFER CURVE OF TSS L4400

DC TRANSFER CURVES

LEGEND:

T(21)
T(Q1)
T(Q13)
T(Q110)
T(Q111)
T(Q112)



***** 27 NOV 76 ************** I-SPICE 2D ************** 21:21:41 *****

DC TRANSFER CURVE OF TSS L4400

SMALL SIGNAL BIAS SOLUTION   TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	5.1592E+00	(2)	5.9270E+00	(3)	4.3618E-01	(4)	3.6911E-01	(6)	[illegible]
(7)	3.6159E-01	(8)	3.6810E-01	(9)	6.4715E+00	(10)	[illegible]	(11)	[illegible]
(12)	1.5236E-02	(13)	9.7001E-03	(14)	-1.4389E+01	(15)	-1.4911E+01	(16)	-1.3122E+01
(17)	-1.4911E+01	(18)	-1.4484E+01	(19)	-9.7294E+00	(20)	[illegible]	(21)	[illegible]
(22)	-8.5148E+00	(23)	-8.5203E+00	(24)	-1.5000E+01	(25)	1.5000E+01		

NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE
(1)	1.1626E+02	(2)	1.1560E+02	(3)	1.1588E+02	(4)	1.1722E+02	(5)	[illegible]
(6)	1.1519E+02	(7)	1.1931E+02	(8)	1.1850E+02	(9)	[illegible]	(10)	1.1711E+02
(11)	1.1713E+02	(12)	1.1557E+02	(13)	1.1585E+02	(14)	[illegible]	(15)	1.1472E+02
(16)	1.1719E+02	(17)	1.2023E+02	(19)	1.1605E+02	(19)	[illegible]	(20)	[illegible]
(21)	1.2033E+02	(22)	1.2087E+02	(23)	1.2126E+02	(24)	[illegible]	(25)	[illegible]
(26)	1.2163E+02	(27)	1.2154E+02	(28)	1.2131E+02	(29)	[illegible]	(30)	[illegible]
(31)	1.2004E+02	(32)	1.1726E+02	(33)	1.1961E+02	(34)	[illegible]	(35)	[illegible]
(36)	1.1495E+02	(37)	1.1494E+02	(38)	1.1516E+02	(39)	[illegible]	(40)	[illegible]
(41)	1.1503E+02	(42)	1.1555E+02	(43)	1.1542E+02	(44)	1.1521E+02	(45)	[illegible]
(46)	1.1604E+02	(47)	1.1553E+02	(48)	1.1640E+02	(49)	[illegible]	(50)	[illegible]
(51)	1.1831E+02	(52)	1.1709E+02	(53)	1.1344E+02	(54)	[illegible]	(55)	[illegible]
(56)	1.1917E+02	(57)	1.1992E+02	(58)	1.2057E+02	(59)	[illegible]	(60)	[illegible]
(61)	1.2015E+02	(62)	1.1546E+02	(63)	1.1171E+02	(64)	[illegible]	[illegible]	[illegible]

NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE	NODE	TEMPERATURE
(66)	1.1200E+02	(67)	1.1117E+02	(68)	1.1154E+02	(69)	[illegible]	(70)	[illegible]
(71)	1.1117E+02	(72)	1.1191E+02	(73)	1.1203E+02	(74)	[illegible]	(75)	[illegible]
(76)	1.1163E+02	(77)	1.1246E+02	(78)	1.1203E+02	(79)	1.1249E+02	(80)	[illegible]
(81)	1.1222E+02	(82)	1.1212E+02	(83)	1.1210E+02	(84)	1.1233E+02	(85)	[illegible]
(86)	1.1252E+02	(87)	1.1256E+02	(88)	1.1257E+02	(89)	1.1255E+02	(90)	[illegible]
(91)	1.1240E+02	(92)	1.1229E+02	(93)	1.1213E+02	(94)	1.1205E+02	(95)	[illegible]
(96)	1.1187E+02	(97)	1.1181E+02	(98)	1.1077E+02	(99)	1.1094E+02	(100)	[illegible]
(101)	1.1113E+02	(102)	1.1106E+02	(103)	1.1099E+02	(104)	1.1127E+02	(105)	[illegible]
(106)	1.1101E+02	(107)	1.1134E+02	(108)	1.1156E+02	(109)	1.1122E+02	(110)	[illegible]
(111)	1.1196E+02	(112)	1.1228E+02	(113)	1.1227E+02	(114)	1.1170E+02	(115)	[illegible]
(116)	1.1218E+02	(117)	1.1158E+02	(118)	1.1191E+02	(119)	1.1214E+02	(120)	1.1234E+02
(121)	1.1246E+02	(122)	1.1240E+02	(123)	[illegible]	(124)	1.1111E+02	(125)	[illegible]
(126)	1.1120E+02	(127)	1.1146E+02	(128)	1.1145E+02	(129)	1.1110E+02	(130)	1.1073E+02
(131)	1.1073E+02	(132)	1.1078E+02	(133)	1.1036E+02	(134)	[illegible]	(135)	[illegible]
(136)	1.1011E+02	(137)	1.1026E+02	(138)	1.1031E+02	(139)	1.1013E+02	(140)	[illegible]
(141)	1.1026E+02	(142)	1.1069E+02	(143)	1.1097E+02	(144)	1.1097E+02	(145)	[illegible]
(145)	2.7000E+01								

AMBIENT TEMPERATURE(DEG-C)   TOTAL POWER DISSIPATION ON CHIP
27.000   5.02E-01WATTS

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VCC	-1.745E-02
VEE	1.705E-02

TOTAL POWER DISSIPATION OF THE ENTIRE CIRCUIT 5.17E-01WATTS

**** RESISTORS OPERATING POINTS

	[illegible]	R6	R7	R8	R9	R10	R11	[illegible]	[illegible]	[illegible]
	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP	ONCHIP
VOLTS	-.001	.349	.010	.006	.016	-.068	.436	[illegible]	[illegible]	[illegible]
AMPS	-3.99E-08	1.94E-04	2.15E-05	2.56E-06	6.15E-06	-6.79E-06	1.45E-05	[illegible]	[illegible]	[illegible]
OHMS	2.00E+04	2.00E+03	4.90E+02	2.40E+03	2.60E+03	1.00E+04	3.00E+04	[illegible]	[illegible]	[illegible]
TEMP-C	116.256	116.296	115.604	115.879	117.201	115.343	116.144	[illegible]	[illegible]	[illegible]
WATTS	3.03E-11	7.56E-05	2.09E-07	1.57E-08	9.84E-08	4.59E-07	6.34E-06	[illegible]	[illegible]	[illegible]

	R15	RECT	REXT
	ONCHIP	OFCHIP	OFCHIP
VOLTS	-9.255	23.520	8.131
AMPS	-4.53E-04	4.70E-04	4.07E-04
OHMS	1.09E+04	5.00E+04	2.00E+04
TEMP-C	118.495	27.000	27.000
WATTS	2.15E-03	1.11E-02	3.31E-03

**** BIPOLAR JUNCTION TRANSISTOR OPERATING POINTS

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q14A	[illegible]
MODEL	MOON ONCHIP	MCOP ONCHIP	MCON ONCHIP	MOON ONCHIP	MCON ONCHIP	MOON ONCHIP	MOON ONCHIP	MOOP ONCHIP	MOOP ONCHIP	[illegible]
IB	1.50E-06	-9.55E-07	1.76E-06	3.89E-08	2.13E-07	2.35E-09	4.27E-08	-3.59E-07	-2.44E-07	-1.23E-07
IC	1.61E-04	-1.60E-05	1.76E-04	4.77E-06	2.13E-05	2.35E-06	6.11E-06	-5.37E-0[illegible]	[illegible]	[illegible]
VBE	.416	-.431	.511	.368	.352	.368	.373	[illegible]	-.132	[illegible]
VBC	-5.922	5.491	0.	-5.539	-.027	.006	-6.093	0.	.543	6.134
VCE	6.350	-5.922	.511	5.927	.379	.362	6.456	[illegible]	[illegible]	[illegible]
BETADC	102.173	16.791	99.971	122.719	100.236	99.956	143.033	15.000	15.341	[illegible]
TEMP-C	115.404	117.110	117.110	117.186	115.967	115.879	117.201	[illegible]	[illegible]	[illegible]
WATT	.001	.000	.000	.000	.000	.000	.000	.000	.000	[illegible]
GM	4.81E-01	4.76E-04	9.25E-03	1.41E-04	6.37E-04	7.01E-05	1.91E-04	[illegible]	[illegible]	[illegible]
RPI	2.14E+08	3.49E+04	1.91E+04	7.26E+05	1.57E+05	1.43E+06	5.70E+05	[illegible]	[illegible]	[illegible]
RO	1.27E+05	1.44E+06	1.13E+06	4.07E+07	8.05E+06	7.57E+07	[illegible]	[illegible]	[illegible]	[illegible]
CPI	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
CMU	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
BETAAC	102.942	16.637	99.961	102.751	99.994	99.978	103.023	14.9[illegible]0	[illegible]	[illegible]
FT	7.66E+16	7.58E+15	8.35E+16	2.29E+15	1.01E+16	1.12E+15	2.07E+15	[illegible]	[illegible]	1.20E+1[illegible]

247.

248.

MODEL	Q12 MODN ONCHIP	Q13 MODN ONCHIP	Q14 MODN ONCHIP	Q16A MODP ONCHIP	Q16B MODP ONCHIP	Q16 MODN ONCHIP	Q18 MODN ONCHIP	Q19A MODP ONCHIP	[illegible] MODP ONCHIP	[illegible] MODN ONCHIP
IB	9.98E-07	4.08E-06	7.66E-06	-3.23E+05	-5.12E-06	-7.70E-14	-1.54E-09	-2.52E-05	-2.57E-05	1.11E-05
IC	1.28E-04	4.10E-04	8.56E-04	-8.11E-04	-7.67E-04	-7.15E-12	3.79E-09	-4.10E-04	-1.01E-04	[illegible]
VBE	.467	.616	.587	-1.041	-1.041	-.000	.089	-.657	-.657	.522
VBC	-28.922	-.862	-22.474	22.474	0.	0.	-.986	4.193	0.	-29.341
VCE	29.389	1.079	23.031	-23.515	-1.041	-.006	1.076	-4.850	-.657	[illegible]
BETADC	125.784	100.230	111.708	21.747	14.985	92.835	-2.467	16.260	14.949	115.432
TEMP-C	119.498	117.178	120.235	120.235	120.235	118.849	118.937	118.082	118.082	120.327
WATTS	.004	.000	.020	.019	.001	.000	.000	.002	.000	.039
GM	3.70E-03	1.22E-02	2.52E-02	2.39E-02	2.26E-02	3.58E-14	2.06E-08	1.22E-02	1.19E-02	3.41E-02
RPI	3.09E+04	8.23E+03	4.40E+03	9.08E+02	6.62E+02	7.16E+10	4.50E+09	1.33E+03	1.26E+03	3.31E+03
RO	1.81E+06	4.88E+05	2.60E+05	8.93E+04	6.51E+04	7.71E+09	6.32E+08	1.32E+05	1.23E+03	1.77E+05
CPI	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
CMU	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
BETAAC	114.436	100.239	111.114	21.724	14.984	.003	92.923	16.245	14.954	114.619
FT	5.89E+16	1.94E+17	4.02E+17	3.81E+12	3.80E+12	5.69E+05	3.29E+11	1.94E+17	1.89E+17	6.07E+17

MODEL	Q1103 MODN ONCHIP	Q1105 MODN ONCHIP	Q1107 MODN ONCHIP	Q1109 MODN ONCHIP	Q1111 MODN ONCHIP	Q1113 MODN ONCHIP	Q1115 MODN ONCHIP	Q1117 MODN ONCHIP	Q1119 MODN ONCHIP	Q1121 MODN ONCHIP
IB	1.14E-05	1.16E-05	1.18E-05	1.19E-05	1.18E-05	1.18E-05	1.16E-05	1.13E-05	1.12E-05	[illegible]
IC	1.33E-03	1.36E-03	1.38E-03	1.39E-03	1.38E-03	1.37E-03	1.36E-03	1.34E-03	1.31E-03	[illegible]
VBE	.522	.522	.522	.522	.522	.522	.522	.522	.522	.522
VBC	-29.389	-29.389	-29.389	-29.389	-29.389	-29.389	-29.389	-29.389	-29.389	-29.389
VCE	29.911	29.911	29.911	29.911	29.911	29.911	29.911	29.911	29.911	29.911
BETADC	116.887	116.920	116.944	116.957	116.955	115.943	116.923	116.897	116.865	115.922
TEMP-C	120.869	121.264	121.551	121.701	121.680	121.536	121.314	121.005	120.727	120.342
WATTS	.040	.041	.041	.041	.041	.041	.041	.040	.039	.039
GM	3.91E-02	3.94E-02	4.04E-02	4.07E-02	4.07E-02	4.04E-02	4.00E-02	3.94E-02	3.87E-02	3.77E-02
RPI	2.93E+03	2.87E+03	2.84E+03	2.82E+03	2.82E+03	2.84E+03	2.87E+03	2.91E+03	2.96E+03	3.04E+03
RO	1.72E+05	1.69E+05	1.67E+05	1.65E+05	1.65E+05	1.67E+05	1.69E+05	1.71E+05	1.74E+05	[illegible]
CPI	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
CMU	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
BETAAC	114.636	114.636	114.635	114.635	114.635	114.635	114.635	114.636	114.637	114.634
FT	6.23E+17	6.35E+17	6.43E+17	6.48E+17	6.47E+17	6.43E+17	6.37E+17	6.27E+17	[illegible]	[illegible]

**** ZENER DIODES OPERATING POINTS

	Z1 OFCHIP	Z2 OFCHIP	Z3 OFCHIP
VOLTS	6.481	6.495	6.480
AMPS	2.10E-03	8.03E-04	4.70E-04
TEMP-C	27.000	27.000	27.000
WATTS	1.40E-03	5.21E-03	3.05E-03

A2.7 How to use T-SPICE2C

The following deck illustrates how to use the auxiliary program T-SPICE2C. The deck following .END card contains data regarding the number of user-created extra thermal nodes and their locations as shown in Fig. A2.7. The nodes indicated by "X" correspond to device locations and those indicated by "O" to user-created extra nodes. They are created to insure that all inner angles of triangles are less than 90 degrees. Note there are many ways of triangular network formation and this is only one of them. The first card following .END gives the number of user-created extra nodes and the remainder of the deck simply defines the x and y coordinates of these nodes. (Obviously the number of these cards is equal to the number of extra nodes specified by the first card.) In this example there are 24 user-created thermal nodes and their locations are entered as shown below. The four corners are automatically taken to be thermal nodes and they need not be included in the user-created thermal nodes. If all the inner angles of triangles are less than 90 degrees, the program punches out a deck that contains information regarding thermal network formed.

In general a user need not complete the triangle network as given in this example. The program can automatically create nodes around the edges of the chip quite reliably. Therefore only a few extra nodes interior to the chip need to be specified. However, to be absolutely sure, the user may wish to complete the triangular network as done in this example and enter all the necessary extra thermal nodes.

```
DC TRANSFER CURVE OF TSS LM4UD
Q1 1 3 0 MODN 9.0                    X=51.0     Y=45.0
Q2 3 2 1 MODP 1.0                    X=45.0     Y=28.0
Q3 11 11 1 MODN 1.0                  X=45.0     Y=28.0
Q4 2 4 0 MODN 1.0                    X=33.35    Y=30.25
Q5 6 7 13 MODN 14.5                  X=33.0     Y=42.0
Q6 7 8 0 MODN 1.0                    X=25.2     Y=44.0
Q7 9 6 12 MODN 2.0                   X=16.9     Y=30.2
Q9 9 9 11 MODP 1.0                   X=5.0      Y=40.0
Z1 11 6 6.3     TC=2M                X=30.0     Y=30.2
R3 4 6 20K                           X=25.2     Y=39.3
R6 6 0 2K                            X=25.2     Y=39.3
R7 13 0 450.                         X=20.0     Y=48.0
R8 8 7 2.4K                          X=25.2     Y=44.0
R9 12 0 2.6K                         X=16.9     Y=30.2
R10 10 11 10K                        X=7.0      Y=48.0
Q14A 2 9 10 MODP 5.0                 X=17.0     Y=40.0
Q14B 8 9 10 MODP 3.0                 X=17.0     Y=40.0
R11 3 0 30K                          X=80.0     Y=35.3
Q12 25 16 14 MODN 2.0                X=31.1     Y=16.3
Q13 16 18 24 MODN 2.0                X=23.1     Y=31.0
Q14 21 22 20 MODN 1.0                X=23.1     Y=16.1
Q15A 22 21 25 MODP .5                X=23.1     Y=16.1
Q15B 21 21 25 MODP .5                X=23.1     Y=16.1
Q16 23 23 22 MODN 1.0                X=5.75     Y=30.75
Q19 16 17 24 MODN 1.0                X=45.0     Y=16.0
Q19A 16 19 20 MODP 1.0               X=10.5     Y=23.0
Q19B 19 19 20 MODP 1.0               X=10.5     Y=23.0
Z2 22 24 6.3    TC=2M                X=14.3     Y=15.8
Z3 23 24 6.3    TC=2M                X=5.75     Y=30.75
R12 15 24 6.0                        X=49.8     Y=12.2
R13 15 17 10K                        X=49.5     Y=12.2
R14 18 24 1.15K                      X=27.0     Y=23.0
R15 18 19 10.5K                      X=27.0     Y=23.0
RFFT 25 23 50K
REXT 25 11 20K
Q1101 25 14 15 MODN 4.0              X=5.5      Y=7.8
Q1103 25 14 15 MODN 4.0              X=9.9      Y=7.8
Q1105 25 14 15 MODN 4.0              X=14.3     Y=7.8
Q1107 25 14 15 MODN 4.0              X=18.7     Y=7.8
Q1109 25 14 15 MODN 4.0              X=23.1     Y=7.8
Q1111 25 14 15 MODN 4.0              X=27.5     Y=7.8
Q1113 25 14 15 MODN 4.0              X=31.9     Y=7.8
Q1115 25 14 15 MODN 4.0              X=36.3     Y=7.8
Q1117 25 14 15 MODN 4.0              X=40.7     Y=7.8
Q1119 25 14 15 MODN 4.0              X=45.1     Y=7.8
Q1121 25 14 15 MODN 4.0              X=49.5     Y=7.8
VCC 25 0 15.0
```

18	48	14	5	47			
4	18	13	16	1	3	2	5
51	8	53	17	26	27		
32	8	50	4	14	1		
15	8	50	33	24	25	26	
20	49	4	48	13	14		
10	53	29	30	7	52		
50	33	4	54	49	18		
22	54	55	61	34			
33	54	23	21	61			
22	33	24	60	61			
23	33	17	25	60			
24	17	26	59	60			
25	17	15	27	59			
26	15	53	28	58	59		
27	53	29	58				
28	53	19	30	57	58		
19	29	7	31	57			
7	30	56	57	35			
8	51	16	11	1	12		
17	50	20	54	22	23	24	
21	61	55					
57	31	56					
41	44						
38	5	47					
2	5	39	37				
2	42	38	62				
42	43	41	62				
9	43	40	44	36			
3	2	12	43	40	39	62	
12	42	46	9	40	41		
45	9	41	36				
6	9	52	44				
10	11	12	6	43	9		
13	48	5	37				
49	18	13	47				
54	55	20	18	48			
17	8	16	4	33	20		
8	15	53	32	11	10		
19	10	7	56	6	45		
51	15	10	19	27	28	29	
33	20	22	21	55	49		
21	54	49	34				
31	7	52	35				
30	29	31	58	35			
29	57	28	27	59			
27	58	26	25	60			
25	59	24	23	61			

23	60	22	21	34
40	42	39		

APPENDIX 3

THE T-SPICE PROGRAM

A3-1. Introduction

The programs T-SPICE2A, T-SPICE2B, and T-SPICE2C have evolved from SPICE2 and therefore the basic structure of the three programs is no different from that of SPICE2. However, the majority of the routines have been modified to suit the task required for electro-thermal simulation. Also, several new overlays have been added.

T-SPICE2A employs the modified functional method to obtain convergence in the analysis and T-SPICE2B, the Newton-Raphson method. The above two programs are quite similar in every other respect. T-SPICE2C is an auxilliary program that forms the thermal network for the die in an entirely different manner from that built in T-SPICE2A and T-SPICE2B.

In this appendix, the detail of the programs will be given with particular emphasis on those portions of the program which are different from SPICE2.

A3-2. T-SPICE2A, T-SPICE2B root segment

The programs T-SPICE2A and T-SPICE2B consist of fourteen major overlays as shown in Fig. A3.1. The root segments T-SPICE2A, T-SPICE2B are the main control portion of the programs and call in the various overlays that are required for the specific simulation. The main control flow graphs of T-SPICE2A and T-SPICE2B are shown in Fig. A3.2,

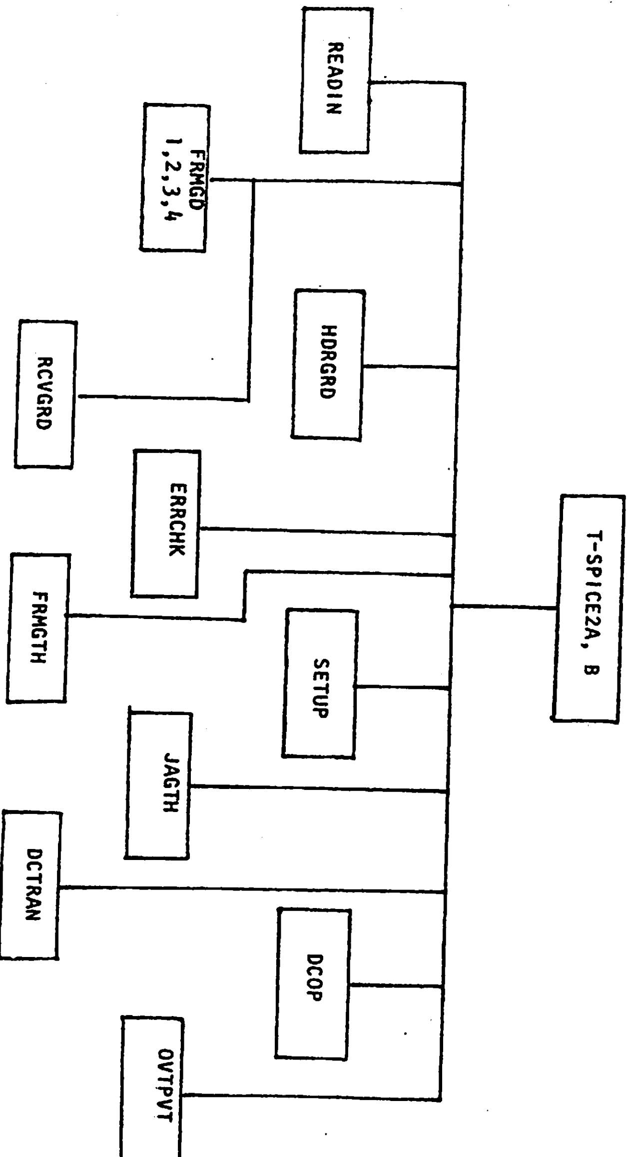


Fig. A3.1

T-SPICE2A, B overlay structure

A3.3 respectively.

In T-SPICE2A, the main program first calls READIN overlay which reads the input file and constructs the circuit data structure. It then checks if the thermal network has been constructed (by T-SPICE2C) and its data are available as a part of input data. If so (i.e., IGRID = 1), it skips the overlays FRMGD1, 2, 3, and 4 and reconstructs the thermal network from the input data through the overlay RCVGRD. Otherwise it calls the overlays FRMGD1, 2, 3, and 4 and constructs the thermal network from the device locations and the chip dimensions. Then the HDRGRD overlay is called to form the thermal network for the header. After the entire thermal network is formed, the overlay ERRCHK is called. The next overlay FRMGTH actually evaluates the thermal resistances and capacitances. The SETUP overlay with INTL = 1 constructs the integer pointer structure for the thermal circuit that is used by the DCTRAN overlay. The next overlay JAGTH calculates what the header to ambient thermal resistance should be so as to make the net junction to ambient thermal resistance equal to what the user specifies. The overlay THLOAD creates tables concerning all the matrix coefficients and their locations that are caused by the thermal resistances so that only the copy function is necessary to load the thermal conductances into the thermal admittance matrix. The next call to SETUP with INTL = 2 constructs the integer pointer structure for the electrical circuit. After this call to SETUP, the circuit analysis can proceed. The main analysis consists of three parts: the dc transfer curve analysis, dc operating point analysis, and the transient analysis. After the desired analysis is performed, the overlay OUTPUT prints out the output and returns to begin the next job.

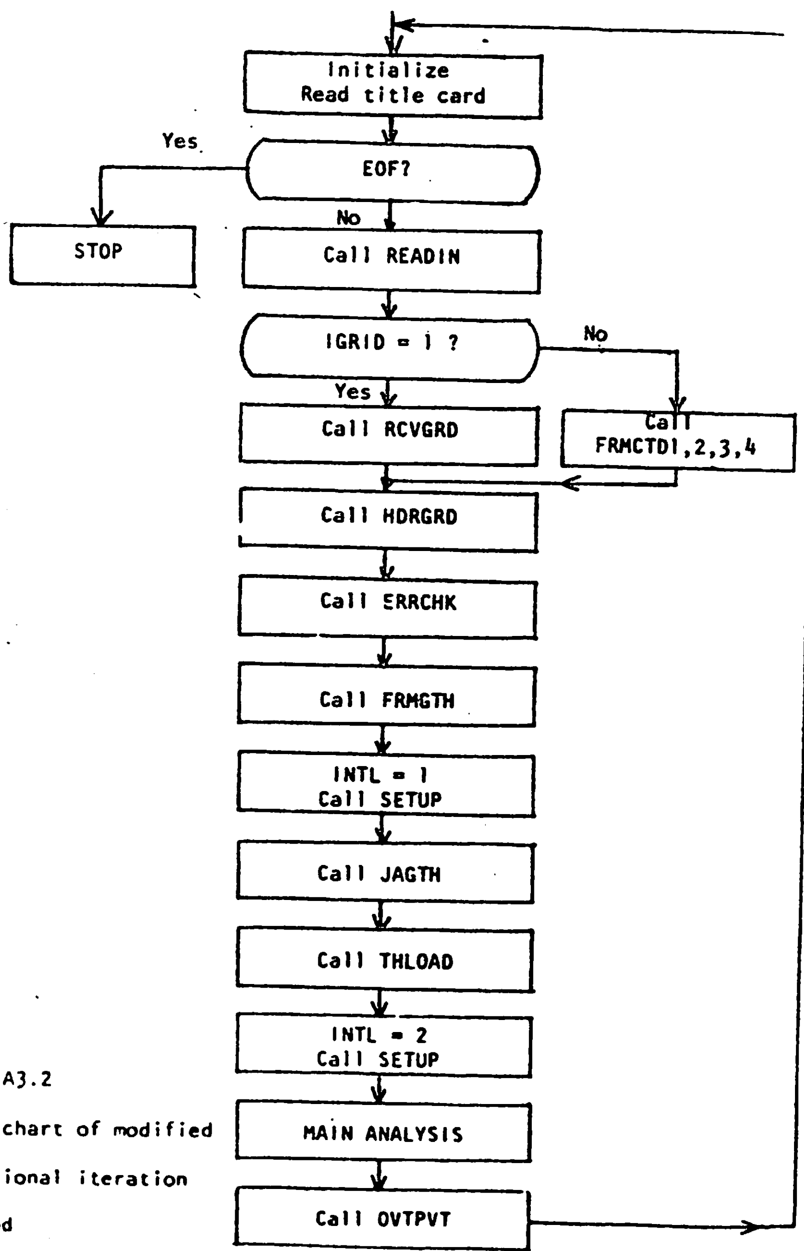


Fig. A3.2
Flow chart of modified functional iteration method

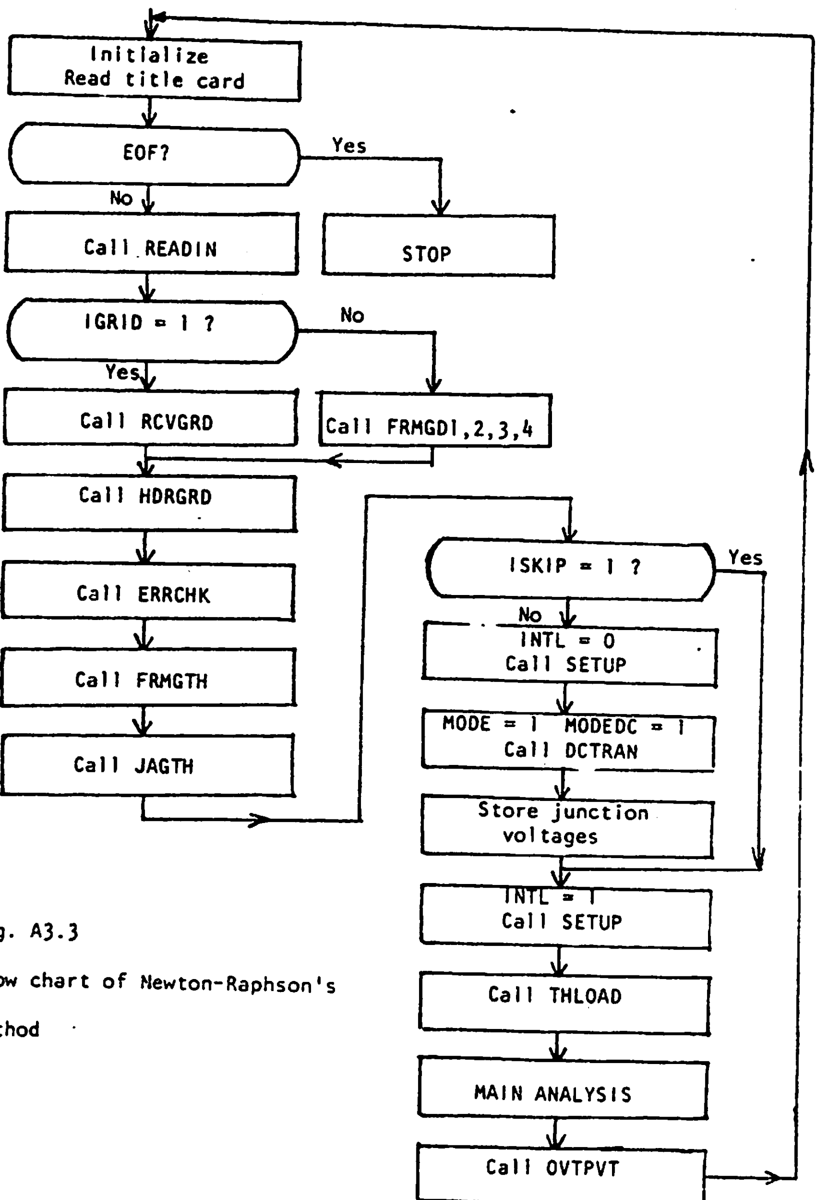


Fig. A3.3

Flow chart of Newton-Raphson's method

T-SPICE2B proceeds in the identical fashion up to the overlay FRMGTH. The next overlay JAGTH is slightly different from that in T-SPICE2A and it first sets up the integer pointer structure for the thermal network and calculates the header to ambient thermal resistance. The main program then checks if the flag ISKIP is set one or zero. ISKIP = 1 indicates that junction initializing scheme as discussed in Chapter 4 is to be skipped. If the flag is zero, then the overlay SETUP is called with INTL = 0 which sets up the integer pointer structure for the electrical circuit. The overlay DCTRAN is called with MODE = 1 and MODEDC = 1, which does the operating point analysis for the electrical circuit. From the resulting nodal voltages, all the voltages across the non-linear electrical elements are retained as an initial guess for the electro-thermal analysis. The next call to the overlay SETUP with INTL = 0 establishes the integer pointer structure for the entire electro-thermal network. The overlay THLOAD, main analysis overlay and OVTPVT overlay are called in that sequence to complete the job.

A3-3. The main analysis loop

The dc transfer curve analysis loop, the operating point analysis loop and the transient analysis loop for both T-SPICE2A and T-SPICE2B have the same structure as in SPICE2 and repeated here for completeness in Fig. A3.4, A3.5, A3.6.

A3-4. The FRMGD1, 2, 3 and 4 overlays

These overlays are identical in both T-SPICE2A and T-SPICE2B. It consists of numerous subroutines and its basic function is to construct the asymmetrical thermal network as mentioned in Chapter 3.

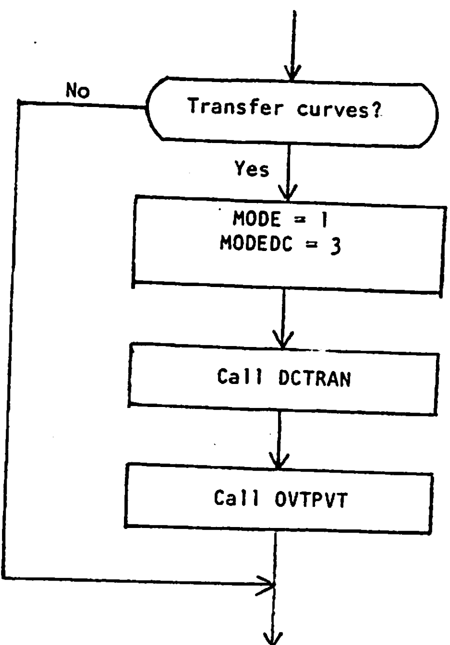


Fig. A3.4

dc transfer curve flow chart

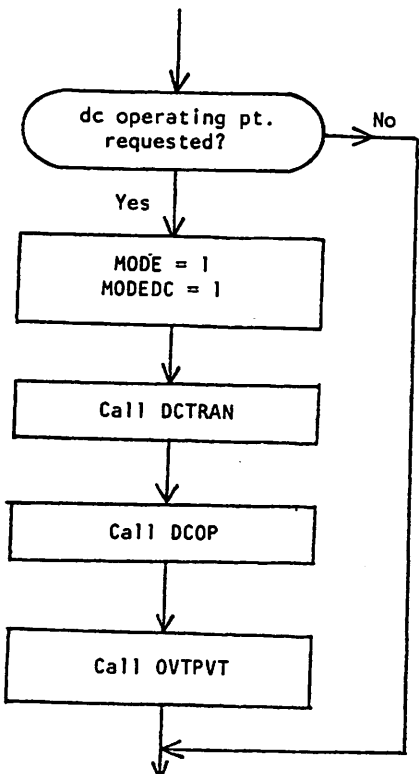


Fig. A3.5

dc operating point analysis flow chart

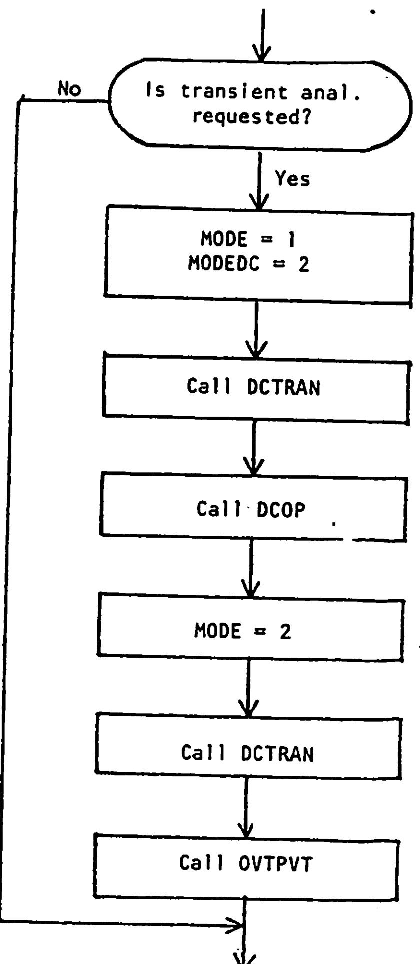


Fig. A3.6

Transient analysis flow chart

The flow graph for this task is shown in Fig. 3A.7. The overlay FRMGD1 defines a thermal node number for all the devices on a chip, and discretizes the X and Y coordinates in an increasing order. Thus any thermal node is alternately expressed by a set of two integers, one corresponding to X coordinates and the other to Y coordinates. The overlays FRMGD2 and FRMGD3 construct a set of rectangles so that all the thermal nodes are located around the edges of the rectangles. An example is shown in Fig. A3.8. A rectangle is defined by a set of four integers, two corresponding to X coordinates, and the other two to Y coordinates. The task of the overlay FRMGD4 is to form an asymmetrical triangular thermal network in such a way that no triangle would have an obtuse inner angle. The overlay FRMGD4 first does the first order check for every rectangle to insure all the nodes around the edges of a rectangle are not in conflict with any line segments connecting two adjacent nodes. Referring to Fig. A3.9(a), one might try to form a triangular network as shown by dashed lines. However, one finds that the node "A" is a problem node because $\measuredangle BAC$ is greater than 90 degrees. Thus the node "A" is in conflict with the line segment $\overline{BC}$. In this case the overlay FRMGD4 creates the node "D" as shown in Fig. A3.9(b). This first order check is done with relative ease as follows: A circle is drawn for every line segment around the edges of a rectangle as shown in Fig. A3.9(c). If there exists a node interior to a circle then that node is in conflict with the line segment which is used to define that circle. In this example the node "A" is within the circle that has $\overline{BC}$ as its diameter. The subroutine FSTODR handles most of this first order check.

After the first order check is completed, the second order

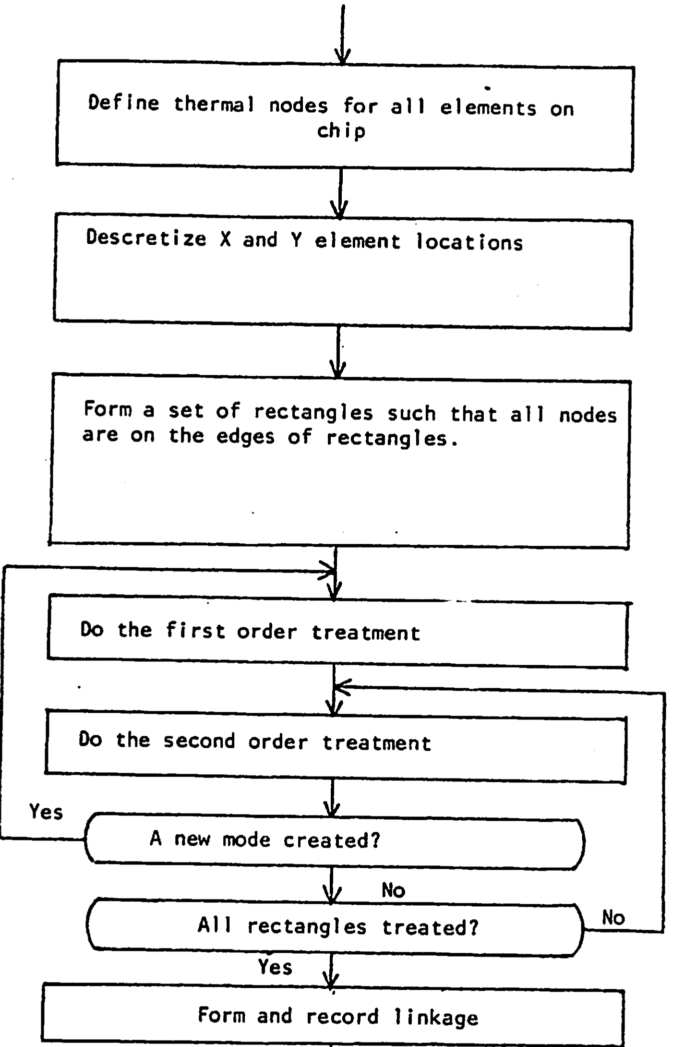
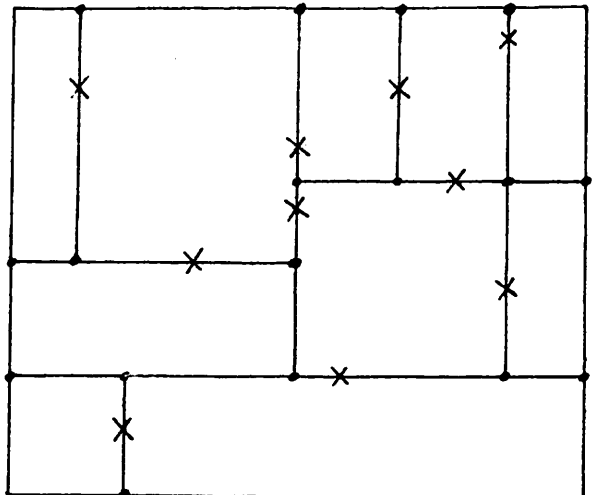


Fig. A3.7

FORMGRID flow chart

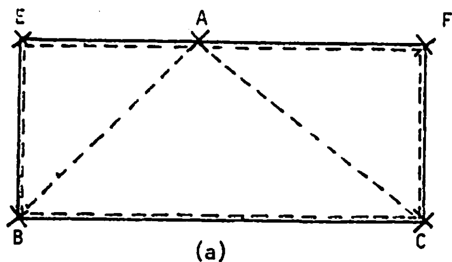


× device locations

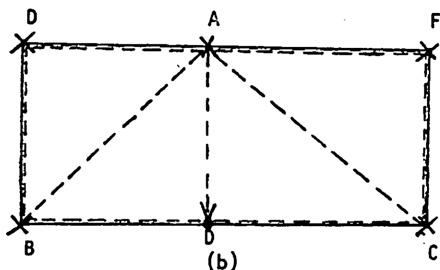
• created nodes

Fig. A3.8

Example of rectangle's formation



(a)



(b)

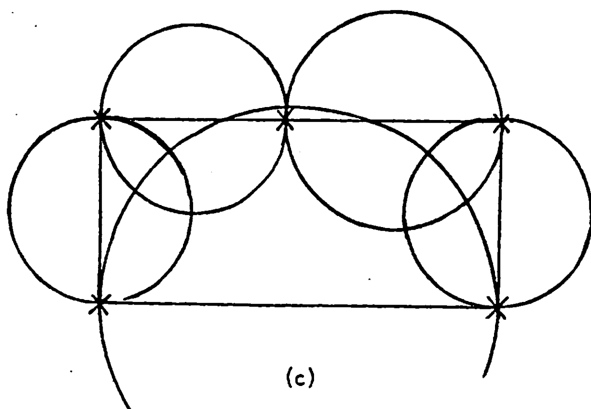

(c)

Fig. A3.9

Examples of first order check

check starts. The basic objective of the second order check is to form an asymmetrical thermal network for every rectangle without creating nodes around the edges of the rectangle. If a node is created around the edges of the rectangle then it affects the thermal network of the adjacent rectangle which it shares the line segment containing the node created. The overlay tries to first complete this triangular thermal network for a rectangle without creating nodes around the outside edges of the rectangle. In this process, a few nodes interior to the rectangle may be created. If a node is created on the outside edges, then it goes back to the first order check and this process is repeated until every rectangle has its own triangular network in accordance with the requirement. The subroutines FRMTRI and INDTRI are devoted to the second order check. When the second order treatment is finished it goes to the final linkage formation step.

The overlay returns to the main program with six tables labeled IPNTX, IPNTY, NOFFTH, IURTH, LINKTH and IPERIM. Nth entry into IPNTX and IPNTY tables give X and Y coordinates of node N. Nth entry into NOFFTH gives the number of nodes connected to node N. Tables IURTH, LINKTH contain data regarding node connections and these data are stored in a linked list bead structure in NODPLC array. NODPLC(IURTH+N)(=IPTR) is a pointer to LINKTH table and NODPLC(LINKTH+IPTR+1)(=N1) is a node connected to node N. NODPLC(LINKTH+IPTR) is another pointer to the next bead. If IPTR = 0, it indicates the end of the bead. Table IPERIM gives all the nodes on the edges of the chip sequentially, starting from the lower left corner in a counterclockwise direction. The number of entries, IPRM in IPERIM table is equal to the number of nodes along the outside edges plus one, and

NODPLC(IPERIM+1) = NODPLC(IPERIM+IPRM).

A3-5. The RCVGRD overlay

This overlay simply reads in data concerning the asymmetrical network previously formed and available in punched form and reconstructs the six tables mentioned in FRMGD1, 2, 3, 4 overlays.

A3-6. The FRMGTH overlay

This overlay calculates the values of all the thermal resistances and capacitors for both chip and header as shown in Chapter 3.

A3-7. The SETUP overlay

In T-SPICE2A, the SETUP overlay with the flag 'INTL' set at 1 or 2 establishes the integer pointer structure for the thermal or electrical circuit respectively.

In T-SPICE2B, the SETUP overlay with the flag 'INTL' set at -1, 0, +1 establishes the integer pointer structure for the thermal, electrical, and overall electro-thermal circuits, respectively.

A3-8. The JAGTH overlay

The JAGTH routine is the control routine for the overlay. It calculates the chip temperature for a unit power input on the top surface of the chip with two sets of thermal conductances 1.5 GH and 2.0 GH distributed from the bottom surface of the header to the ambient, where GH is the user-specified junction to ambient conductance. From these two results the header to ambient thermal resistance is linearly interpolated to give user-specified junction to ambient thermal resistance.

A3-9. The THLOAD overlay

This overlay calculates all the admittance-matrix coefficients associated with the thermal resistances and their locations in the matrix. The matrix coefficients and their locations are stored in NDTPC and NTHVAL tables respectively. The content of these two tables is copied into the Y-matrix later when the actual analysis begins and the loading of admittance matrix becomes necessary at every iteration.

A3-10. The DCTRAN overlay

This overlay in T-SPICE2A is different from that in T-SPICE2B. First the DCTRAN overlay as implemented in T-SPICE2A is presented and then the DCTRAN as implemented in T-SPICE2B is presented.

A3-10-1. The DCTRAN overlay in T-SPICE2A

The DCTRAN overlay is the control routine and performs the dc operating analysis, the transient initial conditions analysis, dc transfer curve analysis and transient analysis. It consists of the following subroutines: DCTRAN, TRUNC, TERR, SORUPD, LUDCMP, FITER8, ITER8, CHKCON, UPDPWR, UPDVAL, LMTPWR, DCDCMP, DCSOL, LOAD, COPYTH, INTGR8 and BJT.

In dc transfer curve analysis as shown in Fig. A3.10, the program first updates source values at time zero and does the LU decomposition of the thermal admittance matrix through the subroutine call to LUDCMP. The LU decomposed Y-matrix is stored in the LVNTH table and later used during the loading of the thermal matrix. The INITF flag is then set to two. The subroutine FITER8 is called to actually obtain the first point solution. If the solution does functionally converge, the values of the specified output variables are stored in

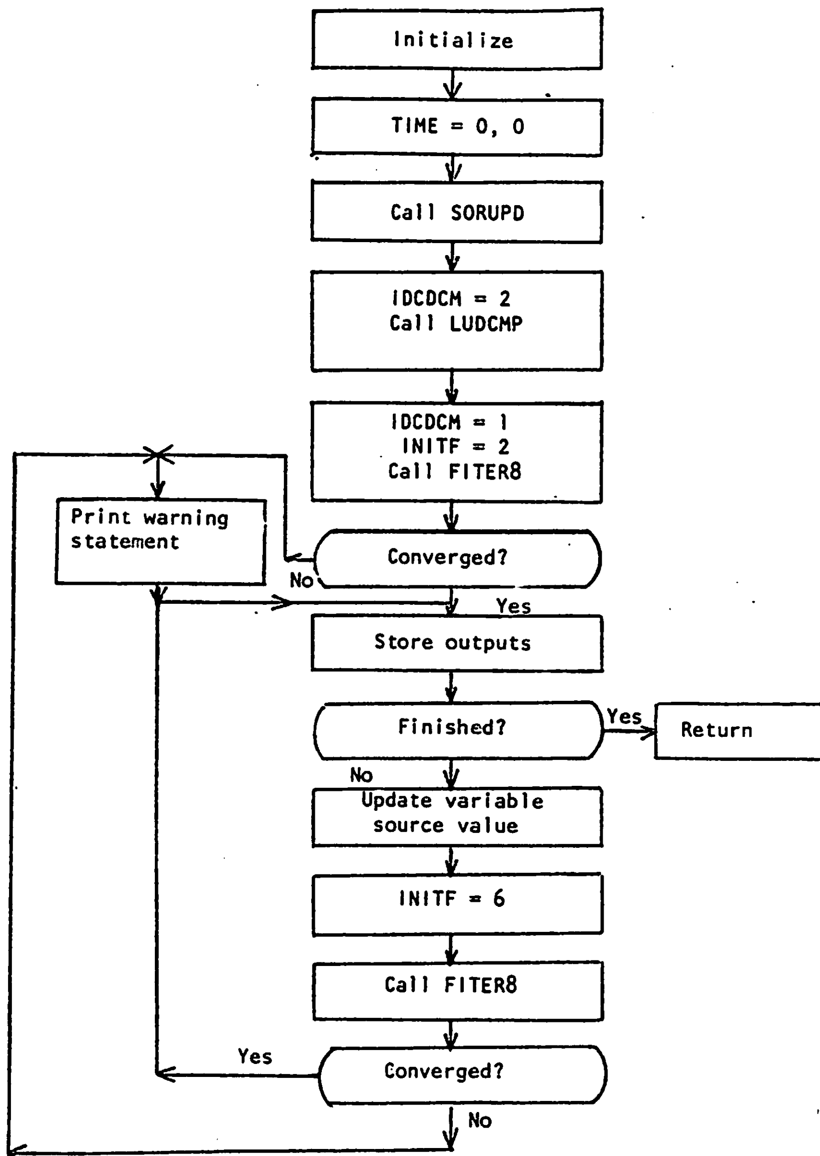


Fig. A3.10

dc transfer curve analysis employing modified functional method

central memory. If the solution does not functionally converge, then the warning statement is printed out and the analysis proceeds to store the last result of the solution. Then the variable source is incremented and the INITF flag is set to six. This process continues until the required number of dc transfer curve points has been computed.

The dc operating point analysis as shown in Fig. 3A.11 is less complicated than the dc transfer curve analysis. It proceeds in the same manner as in the dc transfer curve analysis and after the solution is converged the INITF flag is set to four. Then the device model routine BJT is called to compute the linearized, small-signal value of the non-linear capacitors in the device model.

The initial transient point analysis is almost identical to the dc operating point analysis and shown in Fig. 3A.12. The only difference is that in the initial transient point analysis, the linearized capacitances are not computed after the solution converges.

The transient analysis loop is shown in Fig. A3.13. Since the time-zero solution has been computed by the initial transient point analysis, it first stores the values of the output variables. After the proper time step is chosen, the thermal admittance matrix is decomposed by the subroutine LUDCMP. The decomposed matrix is stored in the LVNTH table and the first time point solution is obtained by calling the subroutine FITER8 with the INITF flag set equal to five. If the time point does not functionally converge, the time step is reduced by a factor of 8 and the time point is re-attempted. If the time point does converge, then the subroutine TRUNC is called twice with the INTL flag set to one and two, to calculate the smallest time step from both electrical and thermal circuits respectively. The smaller of the two

for number sequence only

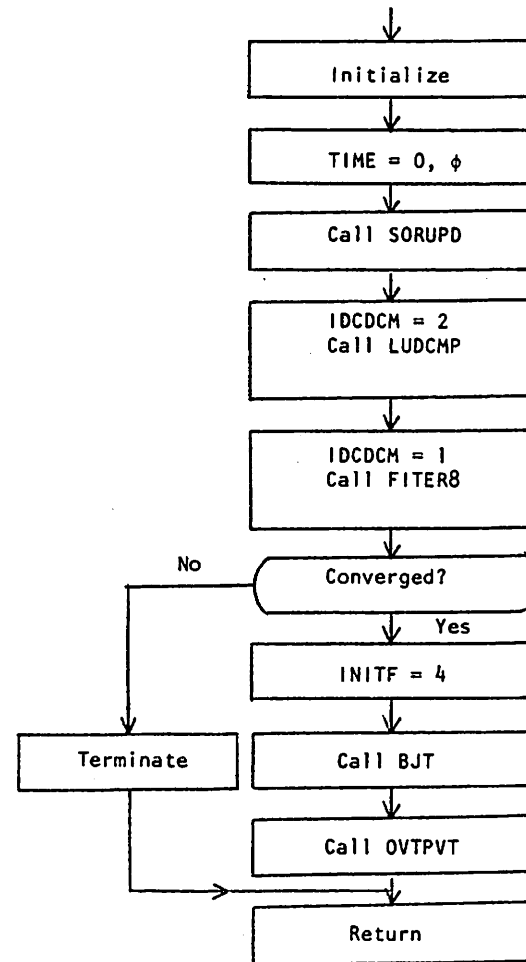


Fig. A3.11

Flow chart of dc operating point analysis employing modified functional method

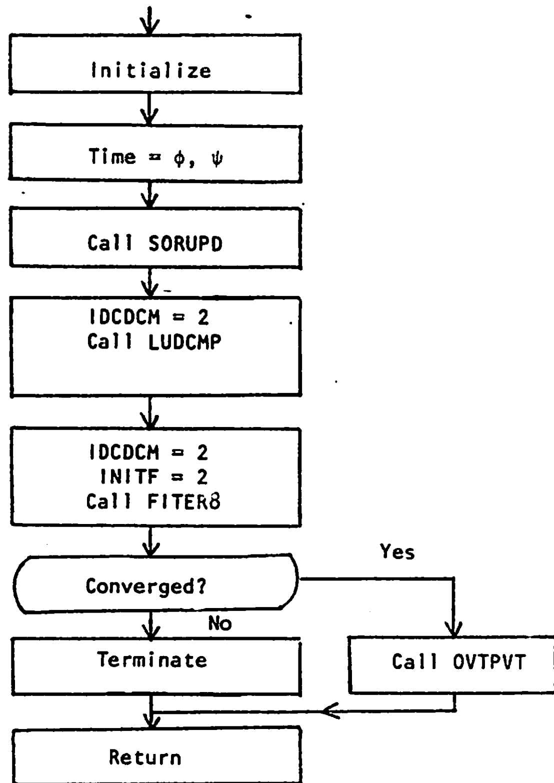


Fig. A3.12

Flow chart of initial transient analysis employing modified functional method

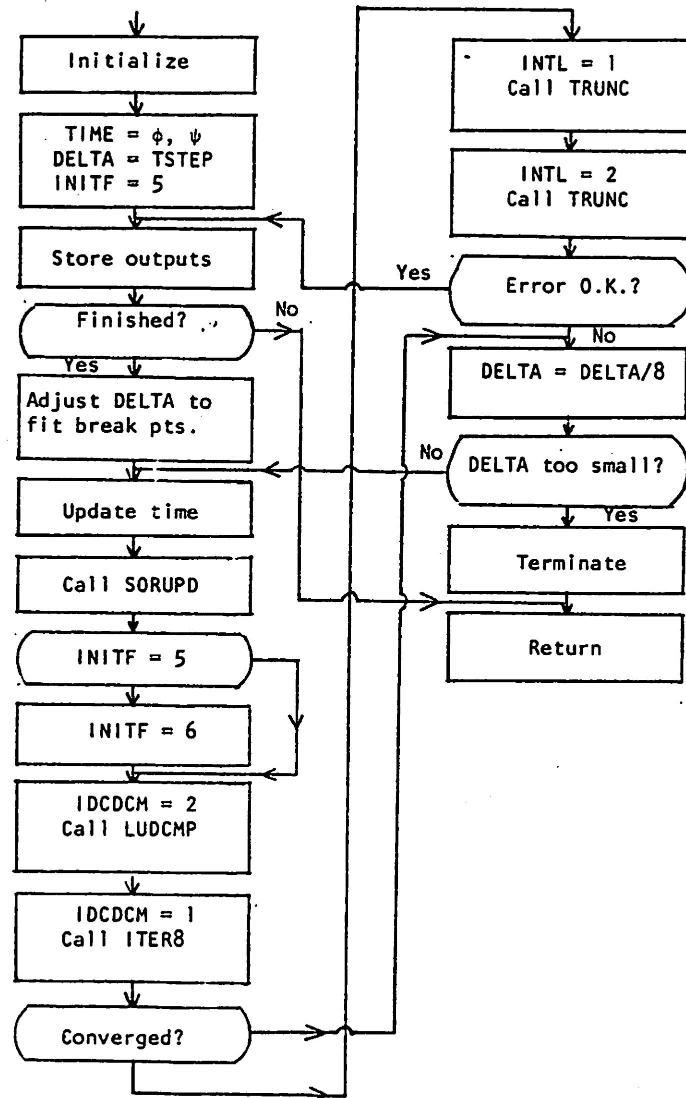


Fig. A3.13

Flow chart of transient analysis employing modified functional method

is chosen as a next time step. As long as the chosen time step is greater than 90 per cent of the present time step, then the time point is accepted and the output variables are stored. Otherwise, the time point is rejected and re-attempted with the smaller time step. The LU decomposition is necessary prior to each call to FITER8 because the thermal admittance matrix coefficients vary with the size of the time step chosen.

All four of the analysis procedures in the DCTRAN overlay use the subroutines FITER8 , ITER8 , LUDCMP, and LOAD.

The subroutine FITER8 as shown in Fig. A3.14 calls ITER8 with the INTL flag set to one and two alternately until both the electrical and thermal solutions converge functionally. ITNUM that indicates the number of functional iterations is first set to zero and the subroutine UPDVAL is called to update the non-linear device parameters according to guess temperatures. The integer pointer structure for the electrical system stored in the table IUR1, IUC1, and IODR1 are copied onto the IUR, IUC, and IORDER tables. The subroutine ITER8 is called with INTL =1 and it returns with the solution of the electrical nodal voltages. The subroutine CHKCON next checks for the functional convergence between the current functional iterate solution and the previous iterate solution with respect to the electrical nodal voltage, temperatures, and electrical currents through all the non-linear electrical elements. If the functional convergence is obtained, it returns to the subroutine DCTRAN. Otherwise, the subroutine UPDPWR is called and the new power dissipation vector is created according to the latest electrical solution and the integer pointer structure for the thermal system stored in the tables IUR2, IUC2, and IODR2 are copied onto the IUR, IUC, and

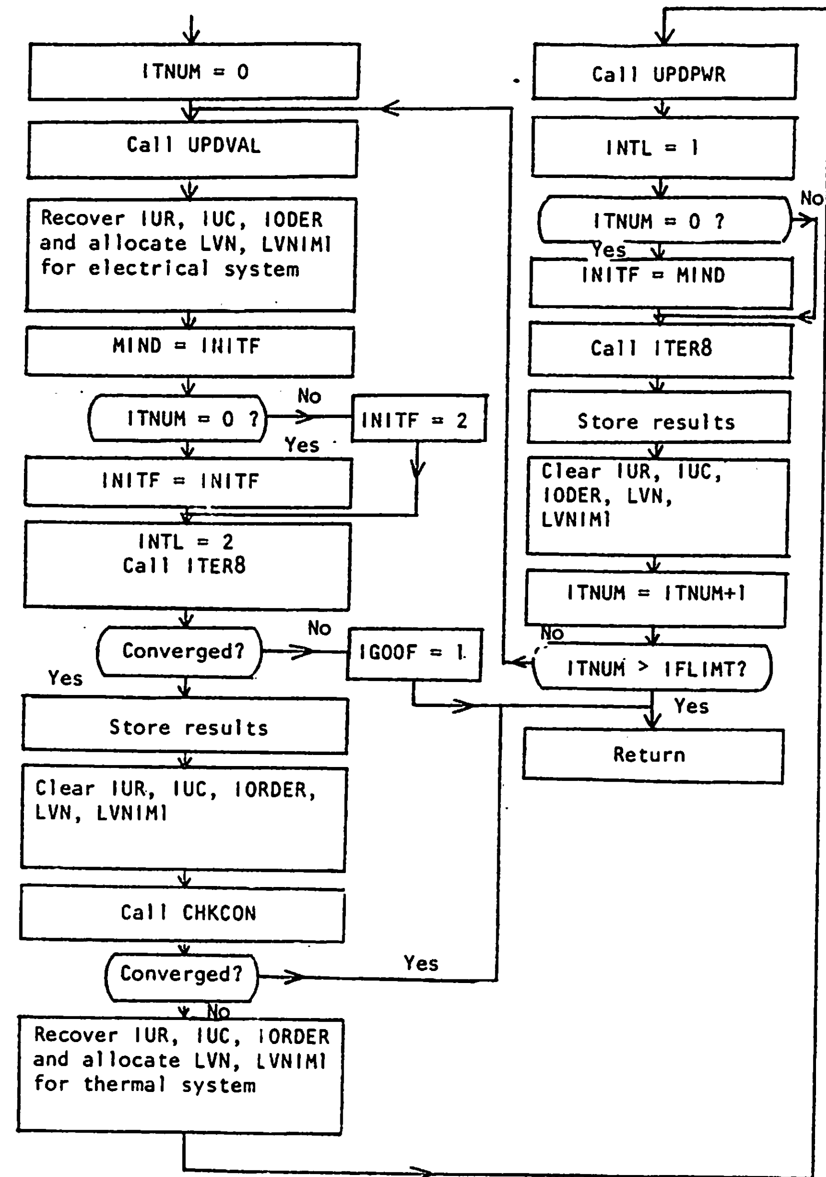


Fig. A3.14

ITER8 flow chart

IORDER tables. The subroutine ITER8 is called with INTL=2, and it returns with the nodal temperature solution. This process continues until the functional convergence is obtained.

The flow graph of ITER8 is slightly different from that in SPICE 2 and shown in Fig. A3.15. When the flag IDCDCM is equal to one, it indicates that the LU decomposition of the thermal admittance matrix has been performed previously and the decomposed matrix is stored in the LVNTH table. Thus the call to DCDCMP is skipped.

The flow graph of LOAD is shown in Fig. A3.16. When the flags INTL=1 and IDCDCM=2, they indicate that the thermal admittance matrix is to be loaded and LU decomposed. In this case, the excitation vector will not be loaded since it is not needed for LU decomposition. When the flag IDCDCM=1, it indicates that the LU decomposition of the thermal admittance matrix has been performed and LU decomposed matrix is available in LVNTH table. Thus the content of the LVNTH table is copied onto the LVN table and the excitation vector is also loaded. If the flag INTL=2, it indicates that the electrical admittance matrix is to be loaded.

The flow graph of LUDCMP is given in Fig. A3.17. The function of this routine is to perform LU decomposition for the thermal admittance matrix and store the LU decomposed matrix in the LVNTH table. To this end, it first copies the integer pointer structure for the thermal system stored in the IUR1, IUC1, and IODR1 tables into the IUR, IUC, and IORDER tables. Then with the flag INTL=1, the subroutine LOAD is called and then the thermal admittance matrix is LU decomposed through the subroutine DCDCMP. The LU decomposed matrix is stored in the LVNTH table.

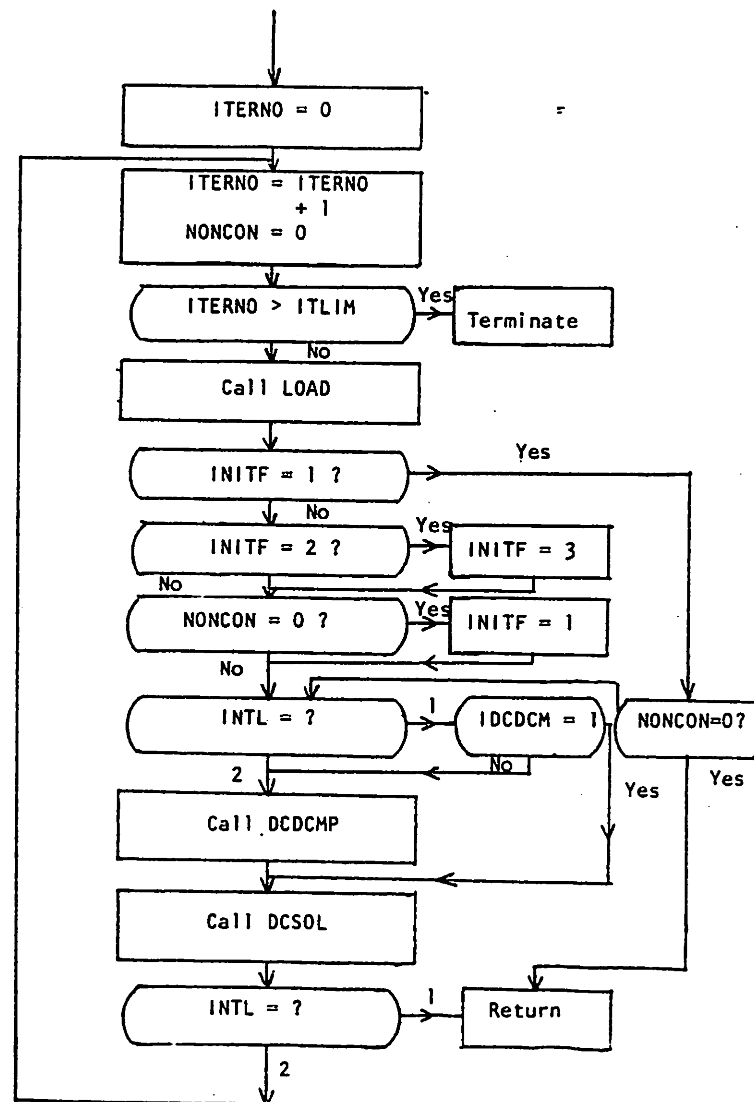


Fig. A3.15

ITER8 flow chart

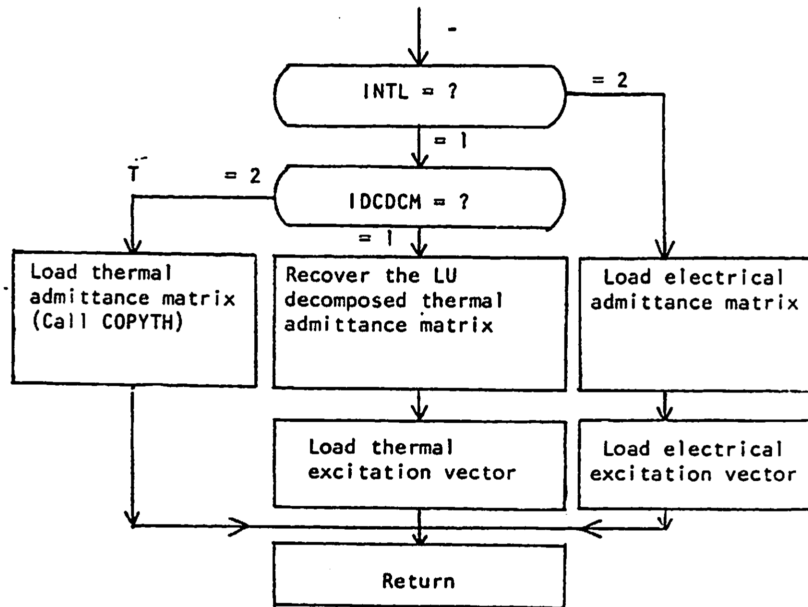


Fig. A3.16

LOAD flow chart

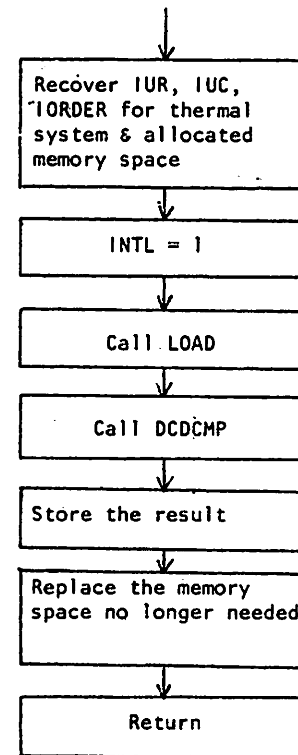


Fig. A3.17

LUDCMP flow chart

A3-10-2. <u>The DCTRAN overlay in T-SPICE2B</u>

The structure of the DCTRAN overlay for the four modes of analysis is very much like that of SPICE2. This is largely due to the fact that the program T-SPICE2B employs structurally the same Newton-Raphson method for the solution of the system. The flow graphs for the four modes of analysis procedures are not shown. The only difference between T-SPICE2B and SPICE2 in terms of the structure is that in T-SPICE2B, the subroutine UPDTMP is called at the end of each iteration so as to properly limit the temperature excursion between iterations. The flow chart for the subroutine UPDTMP is shown in Fig. A3.18.

A3-11. <u>The T-SPICE2C program</u>

The program T-SPICE2C is an auxilliary program that forms the thermal asymmetrical network for the die from its dimensions and the device locations in a manner different from that in T-SPICE2A and T-SPICE2B. The data concerning the network formed that are stored in the six tables, IPNTX, IPNTY, IPERIM, NOFFTH, IURTH, and LINKTH are punched into cards and used by T-SPICE2A and T-SPICE2B in reconstructing the thermal network. The punched deck must be added to the original input deck following .END card and the option flag IGRID must be set to one for the actual analysis in T-SPICE2A and T-SPICE2B.

T-SPICE2C employs a slightly more complicated strategy in forming the thermal network and typically it results in the total number of thermal nodes that is smaller than that created by the thermal network formation routine built into T-SPICE2A and T-SPICE2B. There is, however, a drawback in that it does not always form an asymmetrical

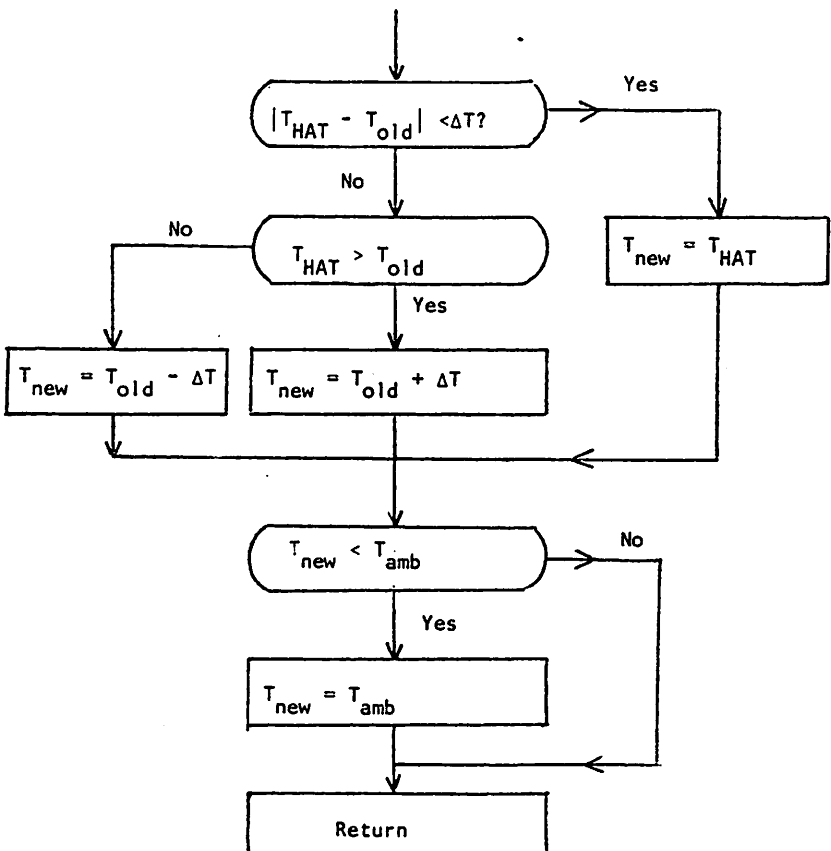


Fig. A3.18

Temperature update scheme

thermal network successfully. In order to insure the success of the thermal network formation, the user must first create his own triangular thermal network making sure that all the interior angles of triangles are less than 90 degrees, and enter these extra node locations as a part of input data.

The flow graph of T-SPICE2C is shown in Fig. A3.19. The program works in the following way. It first chooses a node A on a chip plane and another node B closest to it. Then it checks if there exists a node with which A and B can create a triangle without inflicting any difficulty. Node C in Fig. A3.20(a) is acceptable but node C in Fig. A3.20(b) is not because of the presence of a node D.

If no appropriate node exists, then the program creates a node C and forms a triangle ABC. Now at this point the three nodes A, B, and C are considered to form a perimeter which will eventually be expanded until it coincides with the outside edges of the rectangular chip. Thus we can make a perimeter table whose entries are sequentially A, B, C, and back to A.

The next step is to find a node for every line segment along the perimeter, which lies within the region defined by two straight lines drawn perpendicular to the line segment at two ends and closest to that line segment as shown in Fig. A3.21. A line segment which has the closest node is then chosen and the line segment and its closest node D are used to form a triangle, ABD. If no such nodes exist, an appropriate node D is created to form a triangle with one of the line segments along the perimeter. At the end of this process the perimeter table will be expanded to cover this node. Fig. A3.22 shows a case of this example.

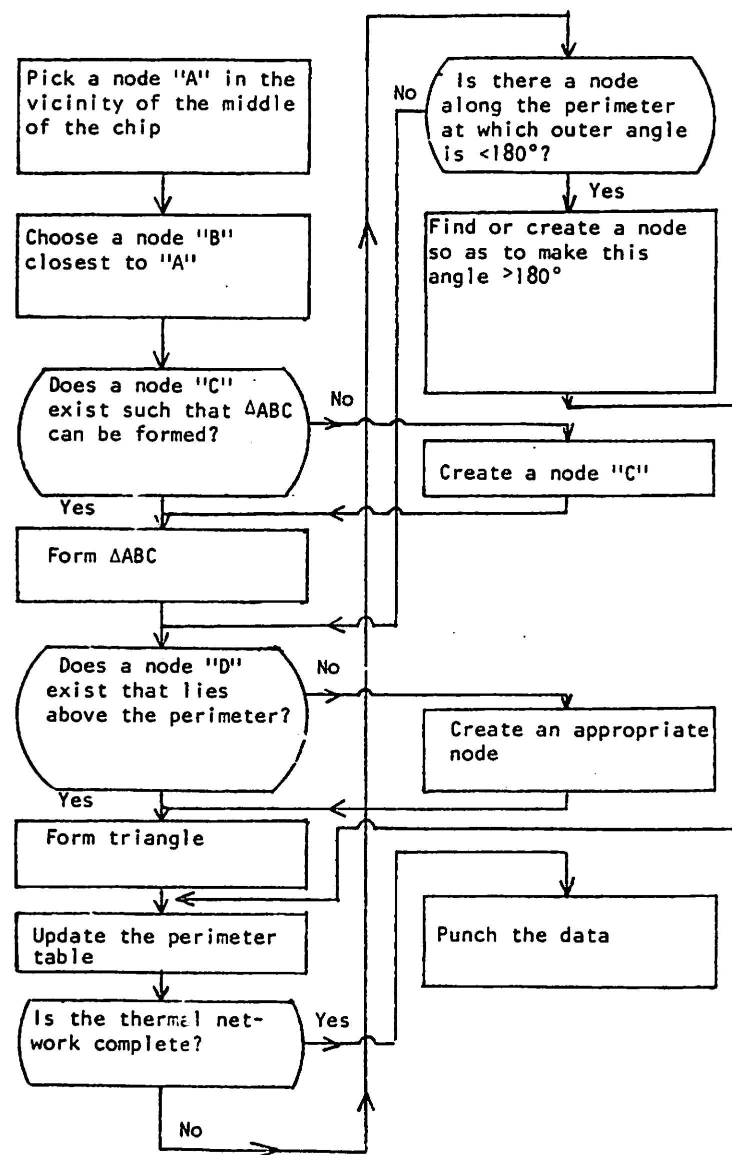
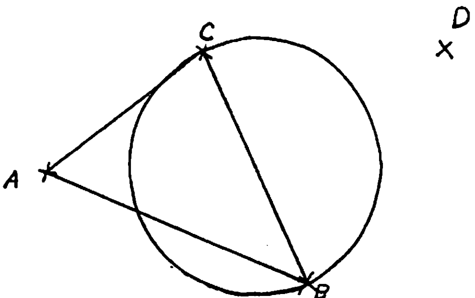
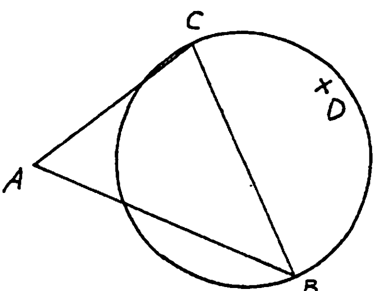


Fig. A3.19

Flow chart of thermal network formation in T-SPICE2C



(a) node "D" acceptable



(b) node "D" not acceptable

Fig. A3.20

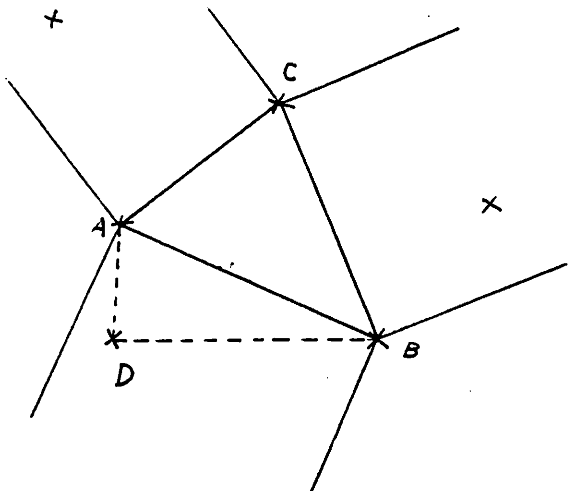
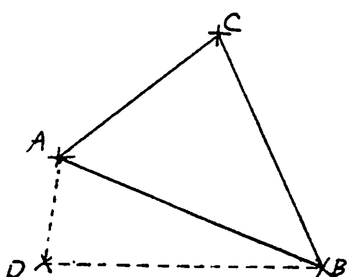


Fig. A3.21

A node "O" closest to the perimeter A-B-C is chosen



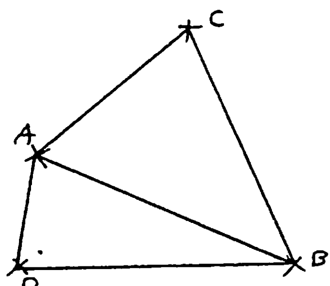


Fig. A3.22

Perimeter tables before and after the triangle ABD formation

This process continues until the entire plane of the die is bounded by the perimeter. Should it happen that an outer angle at any node along the perimeter is less than 180 degrees, then a node is found or created about this node and triangles are formed in such a way that the updated perimeter will no longer have an outer angle that is less than 180 degrees. This is shown in Fig. A3.23. In this example angle $\angle DEF$ is less than 180 degrees. Thus an appropriate node G is either found or created and the two triangles FEG and DEG are formed. The new perimeter represented by nodes A-B-C-D-G-F-A no longer have an outer angle less than 180 degrees. When the perimeter coincides with the outside edges of the chip, the program punches out the data concerning the thermal network formed.

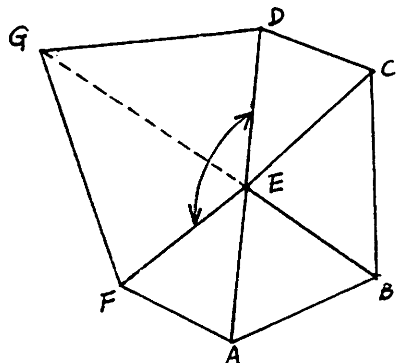


Fig. A3.23

A case where the outer angle of the perimeter is less than 180 degrees

APPENDIX 4

LINKED LIST BEAD STRUCTURE [26]

All integer data are referenced using the array NODPLC and all real data accessed using the array VALUE. The VALUE subscript for the first real value is stored in the integer part of the list element and is called LOCV (LOCM for device models); the NODPLC subscript is called LOC. The same notation as described by Cohen [26] is used here and only those notations unique to T-SPICE are presented.

A4-1. Resistors

The linked list structure of resistors as used in T-SPICE2A and T-SPICE2B are shown in Tables A4.1 and A4.2 respectively.

TABLE A4.1

The Linked List Structure of Resistors in T-SPICE2A

ID = 1

LOC		LOCV	
LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	r(T nom)
+ 2:	n1	+ 2:	TC
+ 3:	n2	+ 3:	X Loc
+ 4:	(n1, n2)	+ 4:	Y Loc
+ 5:	(n2, n1)	+ 5:	T
+ 6:	Lxi offset	+ 6:	r(T)
+ 7:	INDT	+ 7:	PWR
+ 8:	NT		

Comments:

(1) INDT: If INDT = 1, the element is on chip
If INDT = 0, the element is off chip

(2) NT: The thermal node number of the element

(3) TC: The temperature coefficient of the element

(4) X Loc: X coordinate of the element

(5) Y Loc: Y coordinate of the element

(6) T: The temperature of the element at the current iterate

(7) r(T): The value of the resistor at the current iterate temperature T

(8) PWR: The power dissipation within the element at the current iterate

(9) r(T nom): The value of the resistor at room temperature (27°C)

TABLE A4.2

The Linked List Structure of Resistors in T-SPICE2B

ID = 1

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	r(T nom)
+ 2:	n1	+ 2:	TC
+ 3:	n2	+ 3:	X Loc
+ 4:	(n1, n2)	+ 4:	Y Loc
+ 5:	(n2, n1)		
+ 6:	(n1, NT)		
+ 7:	(n2, NT)		
+ 8:	(NT, n1)		
+ 9:	(NT, n2)		
+10:	Lxi offset		
+11:	INDT		
+12:	NT		

A4-2. Capacitors

In T-SPICE2A, all the electrical capacitors are stored in the linked list under ID (identification number) = 2, while the thermal capacitors are stored under ID = 13. In T-SPICE2B both the electrical and thermal capacitors are stored under ID = 2. The linked list structure for capacitors under ID = 2 are identical in both T-SPICE2A and T-SPICE2B and shown in Table A4.3.

TABLE A4.3

The Linked List Structure for Capacitors

ID = 2

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	computed element value
+ 2:	n1		
+ 3:	n2		
+ 4:	(n1, n2)		
+ 5:	(n2, n1)	Lxi + 0:	q (capacitor)
+ 6:	Lxi offset	+ 1:	i (capacitor)

A4-3. Inductors

The linked list structure for inductors is identical in both T-SPICE2A and T-SPICE2B and is shown in Table A4.4.

TABLE A4.4

Linked List Structure for Inductors

ID = 3

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	computed value
+ 2:	n1		
+ 3:	n2		
+ 4:	IBR		
+ 5:	(n1, IBR)		
+ 6:	(n2, IBR)		
+ 7:	(IBR, n1)		
+ 8:	(IBR, n2)	Lxi + 0:	phi (inductor)
+ 9:	Lxi offset	+ 1:	V (inductor)

A4-4. Mutual inductors

The linked list structure for mutual inductors in both T-SPICE2A and T-SPICE2B is shown in Table A4.5.

TABLE A4.5

Linked List Structure for Mutual Inductors

ID = 4

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	value
+ 2:	ptr(L1)		
+ 3:	ptr(L2		
+ 4:	(L1, L2)		
+ 5:	(L2, L1)		

A4-5. Voltage controlled current source

The linked list structure for voltage controlled current source in both T-SPICE2A and T-SPICE2B is shown in Table A4.6.

TABLE A4.6

Linked List Structure for Voltage Controlled Current Source

ID = 5

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	value
+ 2:	n1	+ 2:	delay
+ 3:	n2		
+ 4:	n3		
+ 5:	n4		
+ 6:	(n1, n3)		
+ 7:	(n1, n4)		
+ 8:	(n2, n3)		
+ 9:	(n2, n4)		

A4-6. Non-linear voltage controlled current source

The linked list structure for non-linear voltage controlled current source in both T-SPICE2A and T-SPICE2C is shown in Table A4.7.

TABLE A4.7

Linked List Structure for Non-Linear Voltage Controlled Current Source

ID = 6

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	p1
+ 2:	n1	+ 2:	p2
+ 3:	n2	.	
+ 4:	n3	.	
+ 5:	n4	.	
+ 6:	(n1, n3)	+21:	p21
+ 7:	(n1, n4)		
+ 8:	(n2, n3)		
+ 9:	(n2, n4)	Lxi + 0:	V old
+10:	NPAR	+ 1:	G eq
+11:	Lxi offset	+ 2:	i old

A4-7. Independent voltage sources

The linked list structure for independent voltage sources in both T-SPICE2A and T-SPICE2B is shown in Table A4.8.

TABLE A4.8

Linked List Structure for Independent Voltage Source

ID = 7

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	dc/transient value
+ 2:	n1		
+ 3:	n2		
+ 4:	tp (function coefficient)	LOCP + 1:	V1
+ 5:	LOCP	+ 2:	V2
+ 6:	IBR	+ 3:	T1
+ 7:	(n1, IBR)	+ 4:	T2
+ 8:	(n2, IBR)	+ 5:	T3
+ 9:	(IBR, n1)	+ 6:	T4
+10:	(IBR, n2)	+ 7:	Period

A4-8. Independent current source

The linked list structure for independent current sources in both T-SPICE2A and T-SPICE2B is shown in Table A4.9.

TABLE A4.9

Linked List Structure for Independent Current Source

ID = 8

LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	dc/transient value
+ 2:	n1		
+ 3:	n2	LOCP + 1:	V1
+ 4:	tp (function coefficient)	+ 2:	V2
+ 5:	LOCP	+ 3:	T1
		+ 4:	T2
		+ 5:	T3
		+ 6:	T4
		+ 7:	Period

A4-9. BJT

The linked list structures of BJT in T-SPICE2A and T-SPICE2B are shown in Table A4.10 and Table A4.11 respectively.

TABLE A4.10

The Linked List Structure of BJT in T-SPICE2A

ID = 10

LOC		LOCV	
LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	area factor
+ 2:	nc	+ 2:	X Loc
+ 3:	nb	+ 3:	Y Loc
+ 4:	ne	+ 4:	T
+ 5:	nc'	+ 5:	Is(T)
+ 6:	nb'	+ 6:	RB(T)
+ 7:	ne'	+ 7:	RC(T)
+ 8:	mp	+ 8:	RE(T)
+ 9:	off	+ 9:	VT
+10:	(nc, nc')	+10:	PWR
+11:	(nb, nb')		
+12:	(ne, ne')	Lxi + 0:	Vbe
+13:	(nc', nc)	+ 1:	Vbc
+14:	(nc', nb')	+ 2:	ic
+15:	(nc', ne')	+ 3:	ib
+16:	(nb', nb)	+ 4:	g_{pi}
+17:	(nb', nc)	+ 5:	g_{mu}
+18:	(nb', ne')	+ 6:	g_{mo}

LOC		Lxi	
+ 19:	(ne', ne)	+ 7:	g_o
+ 20:	(ne', nc')	+ 8:	g(cbe)
+ 21:	(ne', nb')	+ 9:	i(cbe)
+ 22:	Lxi offset	+10:	g(cbc)
+ 23:	INDT	+11:	i(cbc)
+ 24:	NT	+12:	g(ccs)
		+13:	i(ccs)

Comments:

(1) Is(T) is the saturation current at the current iterate temperature T.

(2) RB(T), RC(T), RE(T) are extrinsic base, collector and emmiter resistances at the current iterate temperature T.

TABLE A4.11

The Linked List Structure of BJT in T-SPICE2B

ID = 10

LOC		LOCV	
LOC + 0:	next-pointer	LOCV + 0:	element name
+ 1:	LOCV	+ 1:	area factor
+ 2:	nc	+ 2:	X Loc (V_{BEINL})
+ 3:	nb	+ 3:	Y Loc (V_{BCINL})
+ 4:	ne		
+ 5:	nc'	Lxi + 0:	V_{be}
+ 6:	nb'	+ 1:	V_{bc}
+ 7:	ne'	+ 2:	ic
+ 8:	mp	+ 3:	ib
+ 9:	off	+ 4:	g_{pi}
+10:	(nc, nc')	+ 5:	g_{mu}

+ 11: (nb, nb')

+ 12: (ne, ne')

+ 13: (nc', nc)

+ 14: (nc', nb')

+ 15: (nc', ne')

+ 16: (nb', nb)

+ 17: (nb', nc)

+ 18: (nb', ne')

+ 19: (ne', ne)

+ 20: (ne', nc')

+ 21: (ne', nc')

+ 22: (nc', NT)

+ 23: (nb', NT)

+ 24: (ne', NT)

+ 25: (NT, nc')

+ 26: (NT, nb')

+ 27: (NT, ne')

+ 28: Lxi offset

+ 29: INDT

+ 30: NT

+ 6: g_{mo}

+ 7: g_o

+ 8: g(cbe)

+ 9: i(cbe)

+10: g(cbc)

+11: i(cbc)

+12: c(ccs)

+13: i(ccs)

+14: dIF/dT

+15: dIB1/dT

+16: dIB2/dT

+17: T

+18: CBEQB

+19: CBCQB

+20: dIC1/dT

+21: dIC2/dT

+22: dP/dVbe

+23: dP/dVce

+24: dP/dT

Comments:

(1) The contents of LOCV + 2, 3 are changed to initial base-to-emitter and base-to-collector or junction voltage guesses after the junction initializing scheme.

(2) Notations in linearized BJT model as used in T-SPICE2B are defined in the following:

The integral charge model proposed by Gummel and Poon [27] for

an intrinsic BJT and adapted to T-SPICE may be characterized by the following equations:

$$I_C = (CBE - CBC)/QB - CBC/BR - CBCN$$

$$I_B = CBE/BF + CBC/BR + CBCN$$

where $CBE = I_s.[\exp(qV_{BE}/kT) - 1]$ if forward biased,

$= (I_s/V_T).V_{BE}$ if reverse biased.

$CBEN = C_2 I_s.[\exp(qV_{BE}/n_{ekT}) - 1]$ if forward biased,

$= (C_2 I_s/n_{eVT}).V_{BE}$ if reverse biased.

$CBC = I_s.[\exp(qV_{BC}/kT) - 1]$ if forward biased,

$= (I_s/V_T)$ if reverse biased.

$CBCN = C_4.I_s[\exp(qV_{BC}/n_{ckT}) - 1]$ if forward biased,

$= (C_4.I_s/n_{cVT}).V_{BC}$ if reverse biased.

I_C: collector current

I_B: base current

BF: ideal forward current gain

BR: ideal reverse current gain

V_{BE}: base-to-emitter junction voltage

V_{BC}: base=to-collector junction voltage

k: Boltzman's constant

T: temperature in degrees K

I_s: saturation curren.

C_2: forward non-ideal base current coefficient

C_4: reverse non-ideal base current coefficient

n_e: non-ideal base-to-emitter emission coefficient

nc: non-ideal base-to-emitter emission coefficient

The circuit model describing these equations is shown in Fig. A4.1. Referring to Fig. A4.1,

$I_1 = CBE/BF + CBEN$

$I_2 = CBC/BR + CBCN$

$I_B = I_1 + I_2$

$I_{C1} = C_{BE}/QB$

$I_{C2} = C_{BC}/QB$

$I_F = I_{C1} - I_{C2}$

$I_C = I_F - I_2$

In terms of these quantities, the notations as used in the subroutine BJT are defined as follows:

DISOT = dI_s/dT

DBEOT = dC_{BE}/dT

DBENOT = dC_{BEN}/dT

DBCDT = dC_{BC}/dT

DBCNDT = dC_{BCN}/dT

DQ2DT = dQ_2/dT

DQBDT = dQ_B/dT

CBEQB = C_{BE}/QB

CBCQB = C_{BC}/QB

DCIDT = dI_{C1}/dT

DC2DT = dI_{C2}/dT

DIFDT = dI_F/dT

DPIDBE = dP/dV_{BE}

DPIDBC = dP/dV_{BC}

DPDT = dP/dT

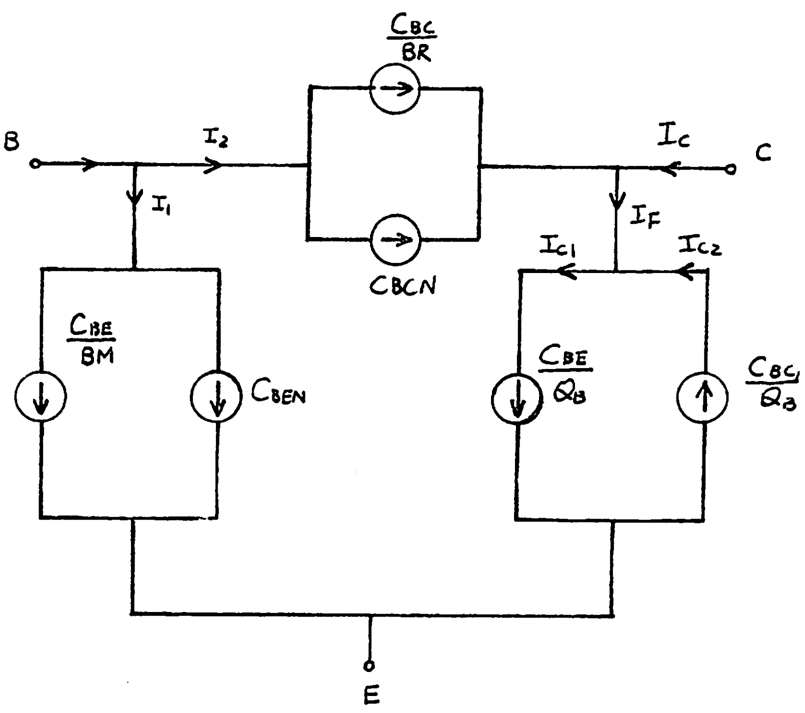


Fig. A4.1

Integral charge model for an intrinsic BJT

where $\dot{P} = V_{BE} \cdot I_B + V_{CE} \cdot I_C$

A4-10. Thermal capacitors

In T-SPICE2A, thermal capacitors are treated differently from electrical capacitors, while in T-SPICE2B both are stored under ID = 2. Thermal capacitors in T-SPICE2A are grouped under ID = 13 and its linked list structure is shown in Table A4.12.

TABLE A4.12

Linked List Structure of Thermal Capacitors

LOC		LOCV	
+ 0:	next-pointer	+ 0:	element name
+ 1:	NT	+ 1:	value
+ 2:	Lxi offset		

Comment:

(1) Since all the thermal capacitors have one node at ground, only one node needs to be specified.

A4-11. Thermal parameters

All the thermal parameters are stored under ID = 15 and are shown in Table A4.13.

TABLE A4.13

Linked List Structure for Thermal Parameters

ID = 15

LOC		LOCV	
+ 0:		+ 0:	
+ 1:	LOCV	+ 1:	LX
		+ 2:	LY
		+ 3:	Aϕ
		+ 4:	BO
		+ 5:	KS
		+ 6:	KH
		+ 7:	TCS
		+ 8:	TCH
		+ 9:	GH
		+10:	CXHDR
		+11:	CYHDR

Comment:

(1) For the meanings of the notations, see Appendix 1.

A4-12. Zener diode

The linked list structures of zener diodes in T-SPICE2A and T-SPICE2B are shown in Tables A4.14 and A4.15, respectively.

TABLE A4.14

Linked List Structure of Zener Diode in T-SPICE2A

ID = 18

LOC		LOCV	
+ 0:	next-pointer	+ 0:	element name
+ 1:	LOCV	+ 1:	value (T nom)
+ 2:	n1	+ 2:	TC
+ 3:	n2	+ 3:	X Loc
+ 4:	IBR	+ 4:	Y Loc
+ 5:	(n1, IBR)	+ 5:	T
+ 6:	(n2, IBR)	+ 6:	Value (T)
+ 7:	(IBR, n1)	+ 7:	PWR
+ 8:	(IBR, n2)		
+ 9:	INDT		
+10:	NT		

Comments:

(1) Value (T nom) is the zener voltage at nominal temperature (27°C).

(2) Value (T) is the zener voltage at the current iterate temperature T.

TABLE A4.15

Linked List Structure of Zener Diode in T-SPICE2B

ID = 18

LOC		LOCV	
+ 0:	next-pointer	+ 0:	element name
+ 1:	LOCV	+ 1:	Value (T nom)
+ 2:	n1	+ 2:	TC
+ 3:	n2	+ 3:	X Loc
+ 4:	IBR	+ 4:	Y Loc
+ 5:	(n1, IBR)		
+ 6:	(n2, IBR)		
+ 7:	(IBR, n1)		
+ 8:	(IBR, n2)		
+ 9:	INDT		
+10:	NT		

A4-13. BJT model

The linked list structure of BJT model for both T-SPICE2A and T-SPICE2B is shown in Table A4.16.

TABLE A4.16

Linked List Structure of BJT Model

ID = 22

LOC		LOCV	
+ 0:	next-pointer	+ 0:	model name
+ 1:	LOCV	+ 1:	BF
+ 2:	model type	+ 2:	BR
		+ 3:	IS

+ 4: RB

+ 5: RC

+ 6: RE

+ 7: VA

+ 8: VB

+ 9: IK

+10: C2

+11: NE

+12: IKR

+13: C4

+14: NC

+15: TF

+16: TR

+17: CCS

+18: CJE

+19: PE

+20: ME

+21: CJC

+22: PC

+23: MC

+24: EG

+25: PT

+26: KF

+27: AF

+28: TCIC

+29: TCIB

+30: TCIE

Comments:

(1) TCIC, TCIB, TCIE are the temperature coefficients of the extrinsic collector, base, and emitter resistances.

A4-14. .PRINT/.PLOT

The linked list structures for elements defined under ID = 31 through 42 are identical to that of SPICE 2. The linked lists represented by ID = 43, 44 are added for temperature outputs under dc and transient simulations. The linked structure of dc analysis output is shown in Table A4.17.

TABLE A4.17

Linked List Structure of dc Analysis Output Variable

ID = 43

LOC + 0: next-pointer

+ 1: LOCV

+ 2: Name1(N1)

+ 3: Name2(N2)

+ 4: ISEQ

+ 5: unused

LOCV + 0: variable name

Comments:

(1) Name 1 and Name 2 are the names of the devices whose temperature difference is the desired output. The names are changed to corresponding thermal node numbers N1 and N2 in the subroutine DEFTHN.

(2) The linked list entries for ID = 44 are exactly the same as for ID = 43 except that the output variables are for transient.

APPENDIX 5

LIST OF THE T-SPICE PROGRAM

Persons who wish to obtain the T-SPICE program should write to the Electronics Research Laboratory, University of California, Berkeley, California 94720. The laboratory charges only a nominal handling charge for any of the programs that it has available.

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