A LOW NOISE OUTPUT STAGE FOR A CCD TRANSVERSAL FILTER

by

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OUTLINE

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I. INTRODUCTION

A transversal filter used in discrete time signal processing has the form $V_{out}(kT)=h_0V_{in}(kT)+h_1V_{in}((k-1)T)+h_2V_{in}((k-2)T)+\ldots+h_mV_{in}((k-m)T)$, which corresponds to a series of delays and multiplying constants and a summer, as shown in Figure 1. This structure can be conveniently implemented using a CCD (charge-coupled device).

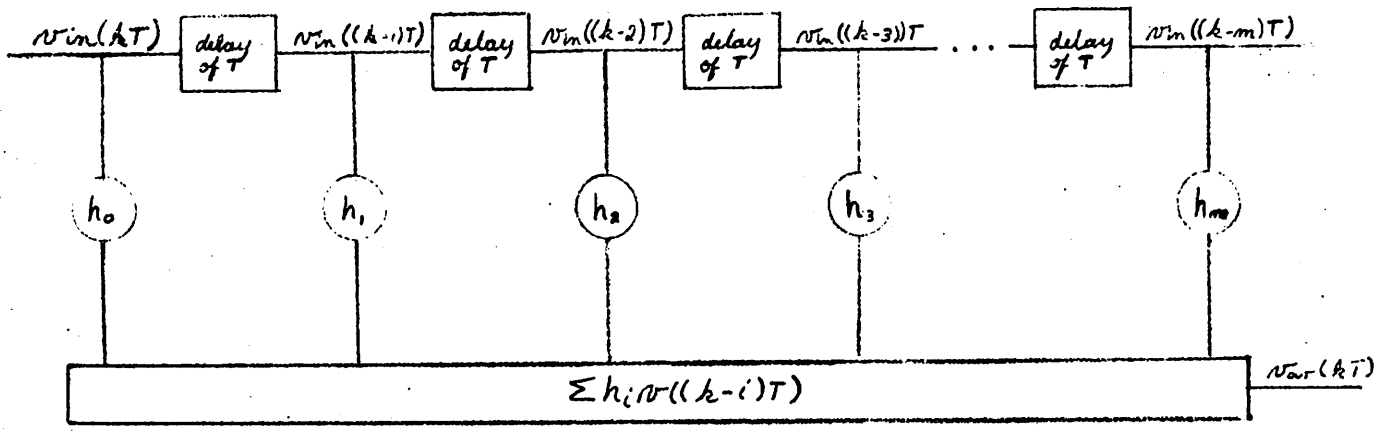


Figure 1. Block Diagram of a Transversal Filter

A CCD is built on a substrate of p-type silicon on which a thin layer of oxide has been grown and over which a series of polysilicon or aluminum gates has been laid. The voltage on each gate can be controlled such that the charge is transferred from one gate to the next.

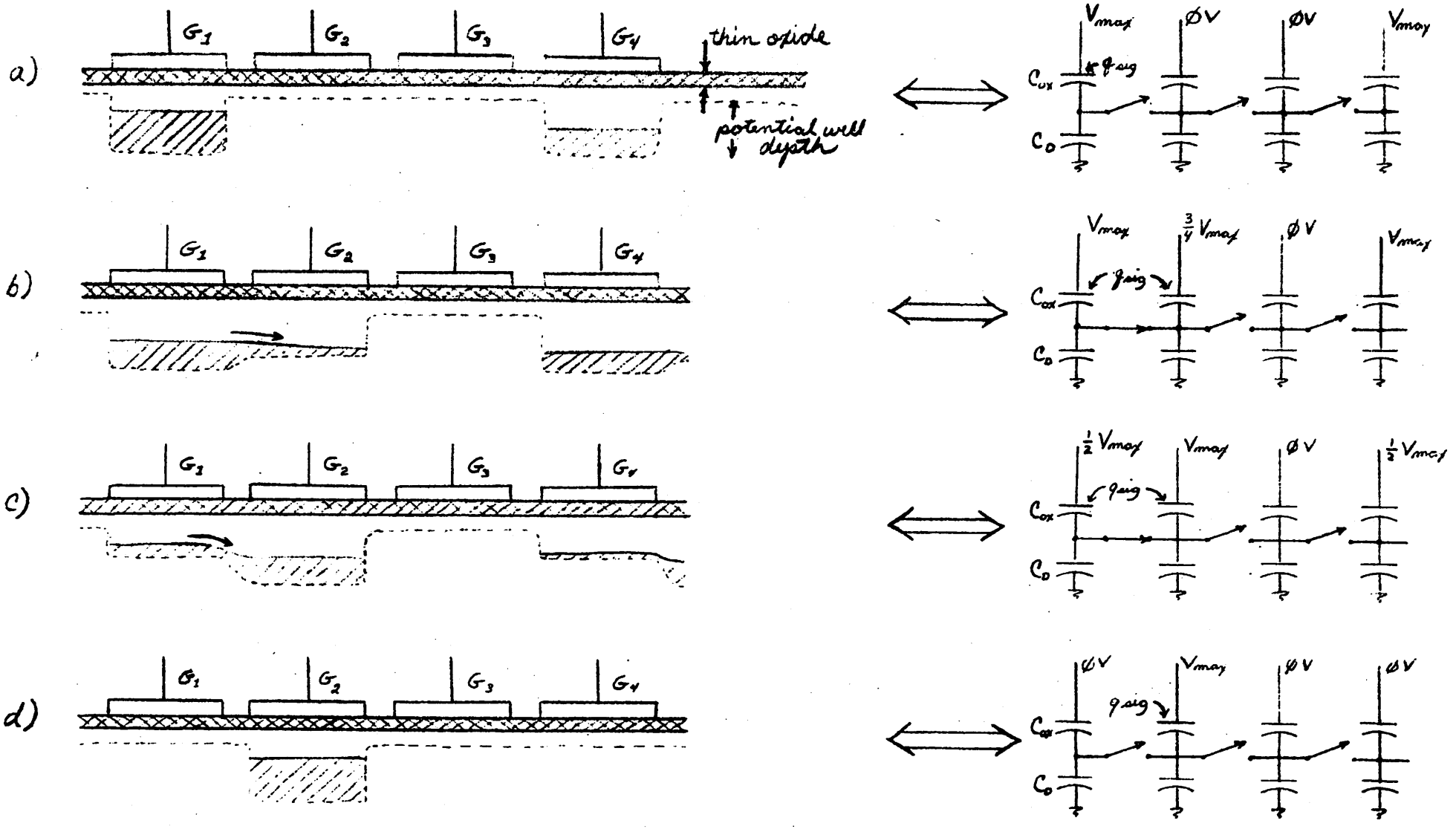


Figure 2. Charge Transfer in a CCD

In Figure 2, the voltage on gates two and three (G_2 and G_3) is the same as that of the substrate and therefore, gates two and three have zero volts across their oxide capacitance. But, gate one is at its maximum voltage, V_{max} (normally 15 volts), so a charge may be introduced onto C_{ox}, which can potentially be as large as $C_{ox}\ V_{max}$. In Figure 2 this is represented by a potential well depth under gate 1. The amount of charge which is actually on C_{ox} (q_{sig}) is signified by the level to which the potential well has been "filled." Now, if the voltage on gate two is raised, its charge-holding potential is increased and some of the charge on gate 1 is transferred to gate 2 (Figure 2b). When the voltage on gate 1 is reduced to zero, all the charge will have been transferred to gate 2 (Figure 2d). This then is an analog delay line.

The next stage in making a transversal filter is to tap the signal in the delay line. This can be accomplished by splitting every third electrode into two parts and connecting the parts as shown in Figure 3.

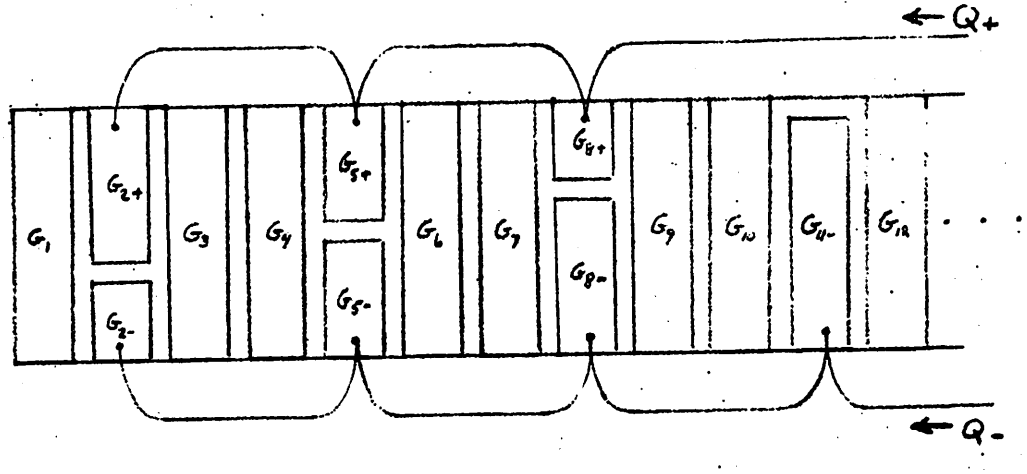


Figure 3. Tap Weights on a CCD Transversal Filter

Now imagine there is some charge q_{sig} under gate 1. When that charge is transferred to gate 2, two thirds of it will go under G_{2+} and one third under G_{2-}. Meanwhile, an opposite, matching charge will be drawn through the connecting wire attached to the top side of G_{2+} and G_{2-} (Kirchoff's current law). If the output is defined as the difference between the charge in positive line, Q_+, and that in the negative line, Q_-, then in this example $Q_{out}=Q_+-Q_-=\frac{2}{3}q_{sig}-\frac{1}{3}q_{sig}=\frac{1}{3}q_{sig}$. The other tap weights shown give an output signal of $0q_{sig}$, $-\frac{1}{3}q_{sig}$, and $-1q_{sig}$ respectively. Now define a_i as the fraction of the ith electrode which is connected to the Q_- line and $(1-a_i)$ as the fraction which is connected to the Q_+ line. Then the fact that all the gates are connected on the top side means that the total value of Q_{out} is calculated by:

$$Q_-=a_0q_{sig}(kT)+a_1q_{sig}((k-1)T)+a_2q_{sig}((k-2)T)+\ldots$$

$$Q_+=(1-a_0)q_{sig}(kT)+(1-a_1)q_{sig}((k-1)T)+(1-a_2)q_{sig}((k-2)T)+\ldots$$

$$Q_{out}=(1-2a_0)q_{sig}(kT)+(1-2a_1)q_{sig}((k-1)T)+(1-2a_2)q_{sig}((k-2)T)+\ldots$$

This is exactly the form needed for a discrete time transversal filter with $h_i \underline{\Delta} (1-2a_i)$.

It is clearly desirable to introduce a q_{sig} which is linearly dependent on the input voltage V_{sig}. This can be handled most satisfactorily by using the voltage input method shown in Figure 4.

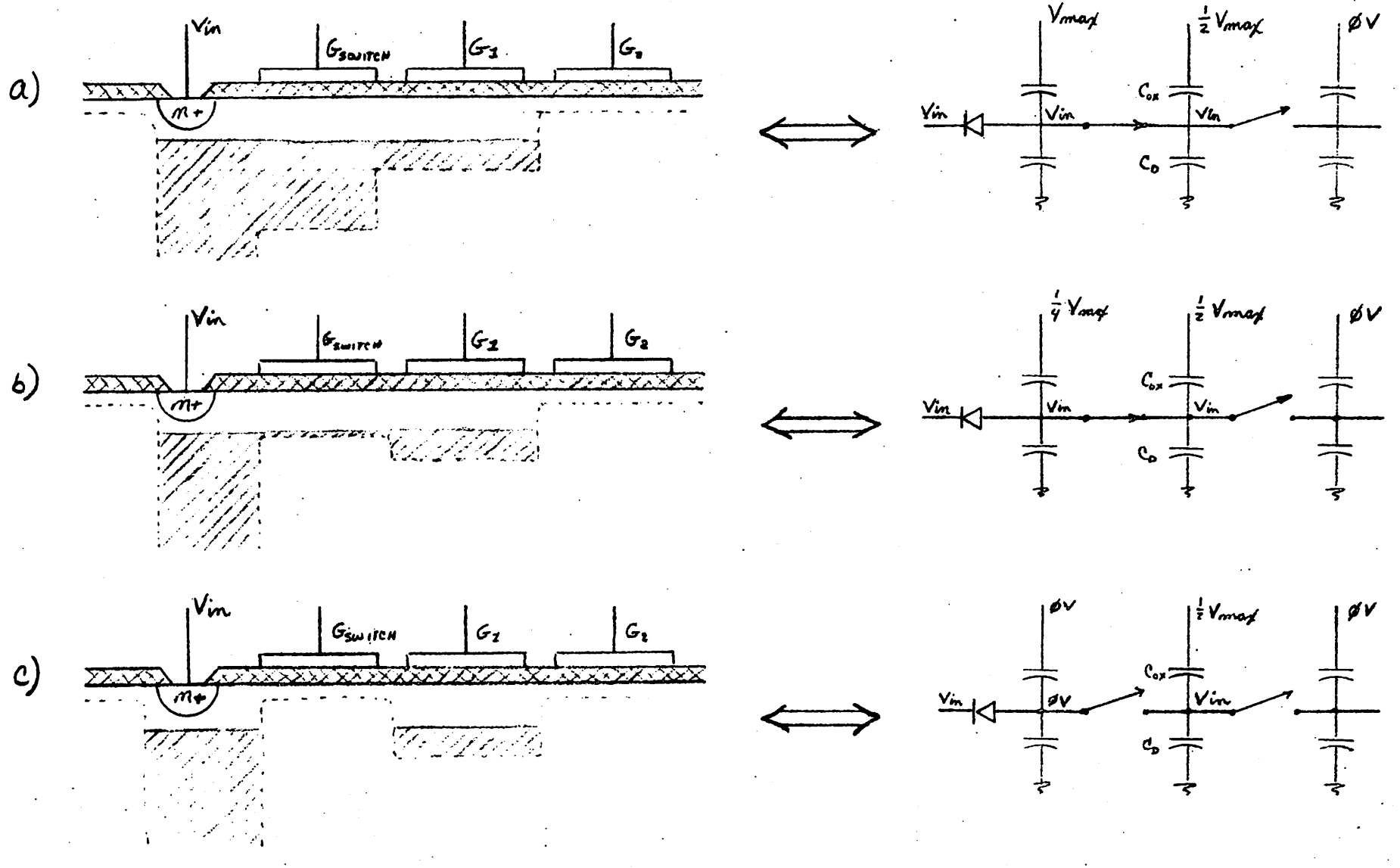


Figure 4. Voltage Input Method for a CCD

Here the input voltage is applied to an n+ diffusion, while the voltage on the adjacent gate (G_{switch}) is at V_{max} and the voltage on the next gate (G_2) is held at 1/2 V_{max}. When the switch gate is turned off, the charge on C_{ox} will be C_{ox} (V_{in} - 1/2 V_{max}) and the charge on C_D will be C_D (V_{in}). When this charge is transferred to the next gate, the charge through the output lines will be 1/2 C_{ox} (V_{sig} - 1/2 V_{max}). The depletion capacitance will discharge through ground. Then as long as the voltage on the following split electrodes is held at 1/2 V_{max}, the output charge will be linearly dependent on V_{in}. However, if the voltage is not held at V_{max}, the capacitors will make up the difference by transferring some of the charge which is on C_{ox} to C_D. Unfortunately, C_D is a nonlinear capacitor, so the amount of charge transferred will not be proportional to the voltage difference and some distortion will be introduced. This effect is small, however, since $C_D \ll C_{ox}$ and therefore the amount of charge transferred is small.[1]

Finally, the CCD needs an output stage which will convert Q_{out} to V_{out}. That is the major topic of this paper.

II. CHOICE OF AN OUTPUT STAGE

In the specific application for which this output stage has been designed, it is not necessary to take the difference of Q_+ and Q_-

[1]For more information on the basic operation of CCD's, see Kosonocky and Carnes, "Basic Concepts of Charge-Coupled Devices".

since the next stage will do this automatically. It is necessary, however, that the gains and DC levels be carefully matched. Matching the gains is a simple matter of matching feedback capacitors (if an op-amp is used), but matching the DC levels is not as easy. The configuration shown in Figure 5 has four problems with setting the DC level.

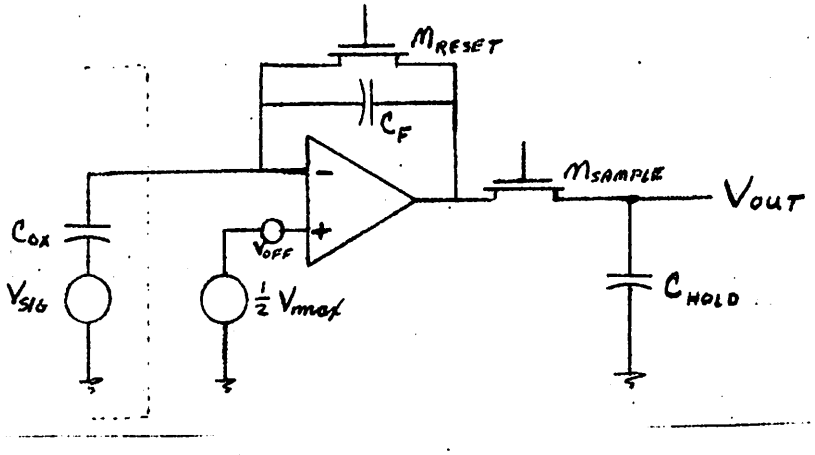


Figure 5. Simple CCD Output Stage

The first is the problem of amplifier offset voltage. The DC level of the output is set when the reset transistor is closed, and will have a value of 1/2 V_{max} + V_{offset}. Since offset voltages can easily differ by as much as 50mV, and the total output signal may only be 500mV, this can be a significant limitation to the accuracy

of the output signal. Another potential source of offset comes from the CCD and is called clock noise. It is caused by capacitive coupling of the clock transition on adjacent electrodes into the signal electrodes (Figure 6).

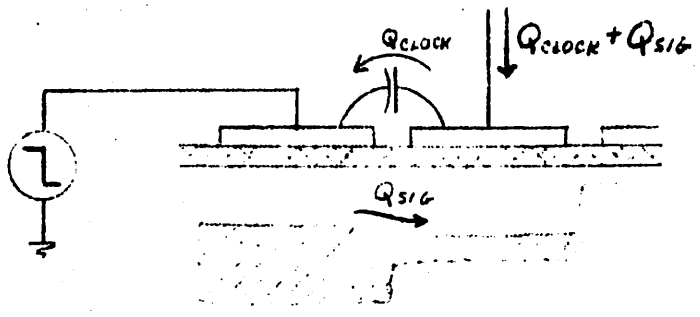


Figure 6. CCD Clock Noise

The size of this offset depends on the size of the coupling capacitor, but in poorly designed CCD filters, it can be two to three times larger than the signal size. However, in well designed CCD's, this clock feedthrough is balanced so that the same level is received on the two signal lines. It can then be treated as a common mode signal and rejected. On other CCD's (including the one for which this output stage has been designed), the signal is not only balanced, but also small. So even if the balance is not perfect, the total effect will be negligible.

The next problem comes with the resetting of the feedback capacitor. When the reset transistor is turned off, there is some charge transferred to the feedback capacitor due to the capacitive coupling between the gate and source of the reset transistor (Figure 7).

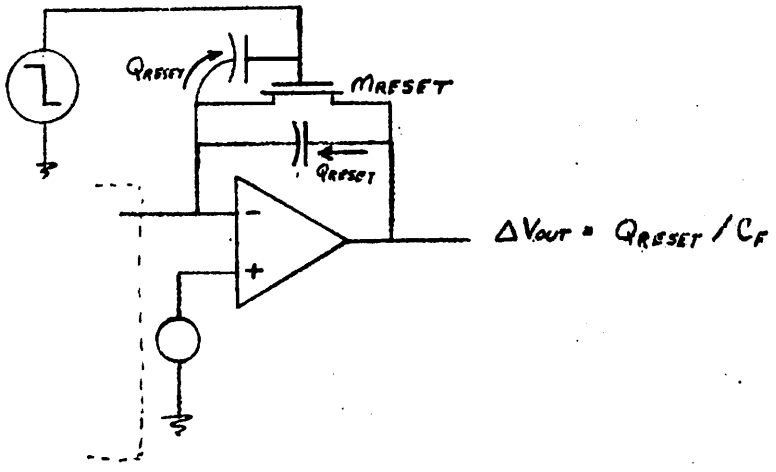


Figure 7. Effect of Resetting C_F

The last problem is a culmination of the previous three, namely that even if everything is perfectly balanced and the DC levels of both the positive and negative outputs match, the circuit designer has not been able to chose that level.

All these problems can be handled by introducing a coupling capacitor and careful timing to the output stage. The circuit and timing are shown in Figure 8. The important points to notice are that the DC level of V_{out} is set periodically by shorting it to an arbitrary V_{DC} and it is therefore not determined by $\frac{1}{2} V_{max}$ or the offset voltage. Furthermore, M_{DC} is not opened until after the resetting of the feedback capacitor is complete, so that level does not affect it either. It is affected slightly by the opening of M_{DC} and M_{sample}, but these effects can be made sufficiently small and sufficiently predictable to cause no problem. This type of output stage is called a correlated double sampler and will be discussed in more detail later.

If a single output is desired, the circuit shown in Figure 8 can be modified to that shown in Figure 9.

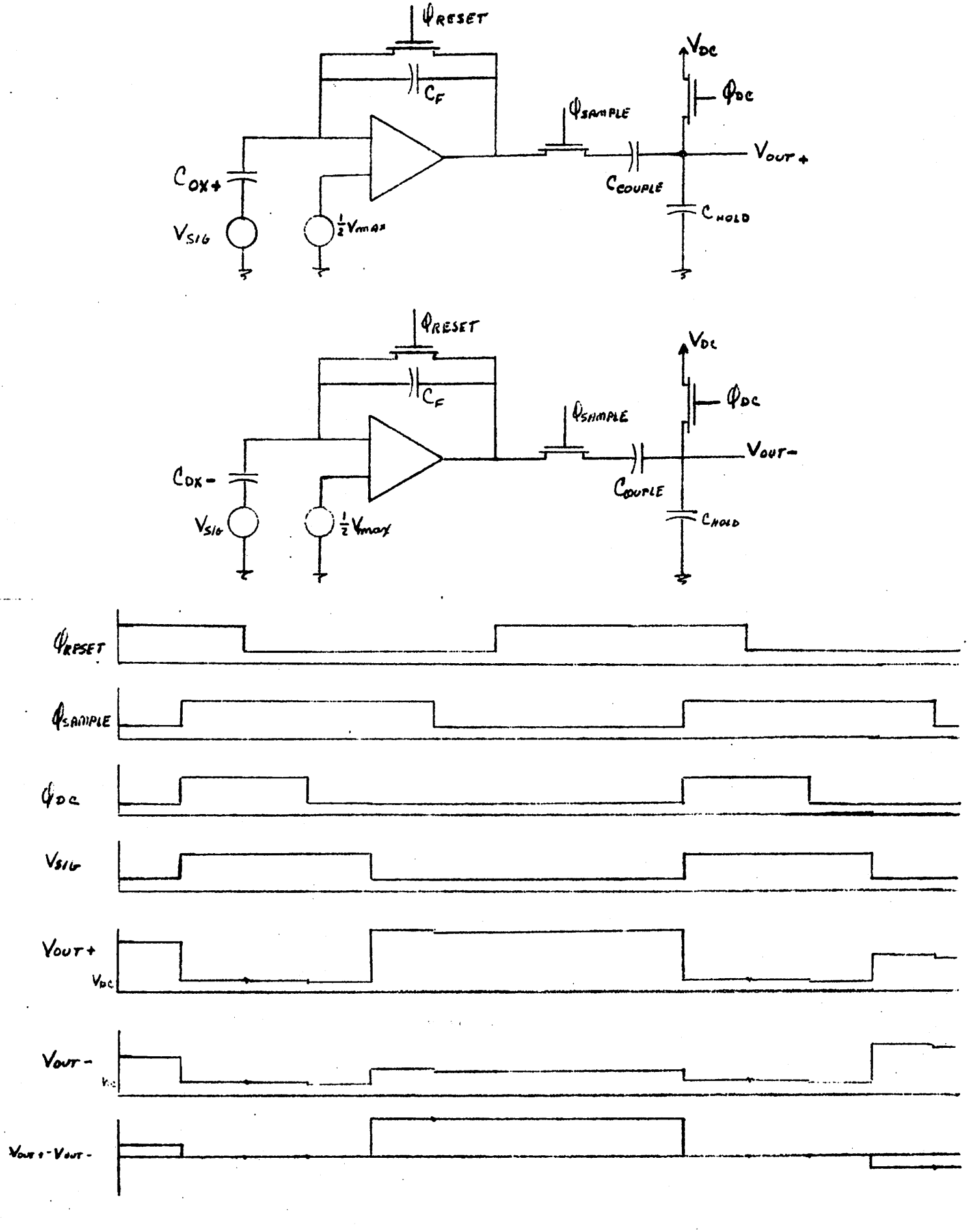


Figure 8. Output Stage with Correlated Double Sampler

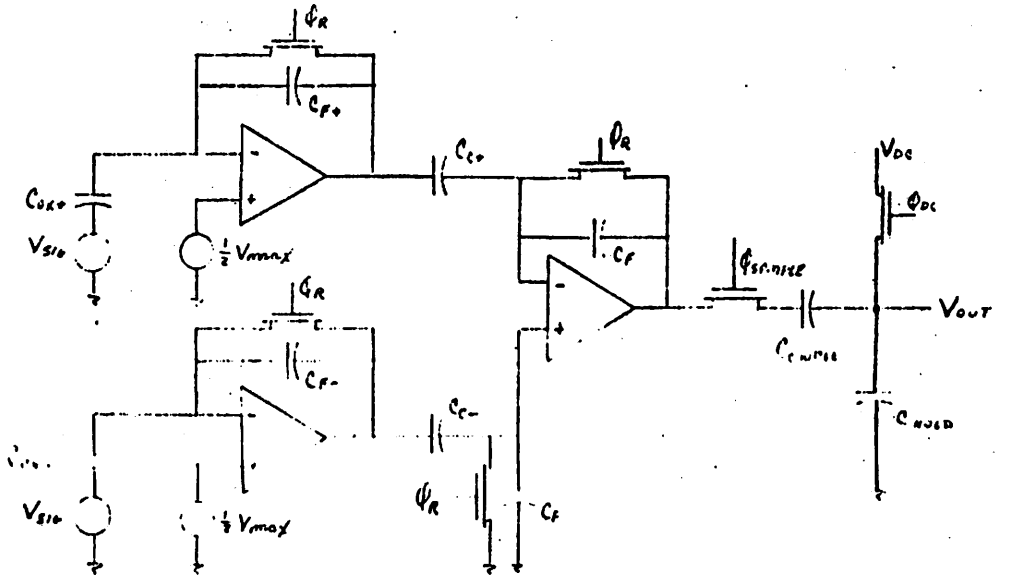


Figure 9. A Single-Ended Output Stage

This has the same timing as the first circuits and the same elements with the addition of one op-amp and two capacitors. The same function can also be achieved by the circuit in Figure 10, but although less complex, this has trouble with the stray capacitances in the CCD (they must be perfectly matched), has less gain than the circuit shown in Figure 9, and will introduce the distortion effect discussed earlier.

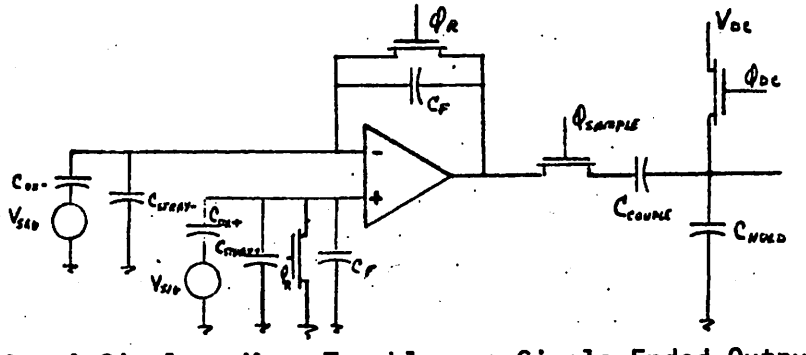


Figure 10. A Simpler, More Troublesome Single-Ended Output Stage

When a discrete prototype of the output stage shown in Figure 11 was built, it was found to behave about as expected[2] with one major difference - it was extremely noisy. Although this noise could not be measured accurately, it appeared to have an RMS value between 1 and 3mV. It was decided that the noise must be coming from the op-amp for the following reasons:

[2]For more details, see Appendix B.

1. Thoroughly bypassing and low pass filtering all supplies did not help.

2. Completely separating the analog portion of the circuitry from the noisy digital clocking circuitry did not help.

3. Shielding the circuitry did not help, besides which the 60 cycle noise was frequently visible with the other noise superimposed upon it.

4. If C_{stray} was increased, the noise seemed to increase.

5. If C_F was increased, the noise decreased proportionally.

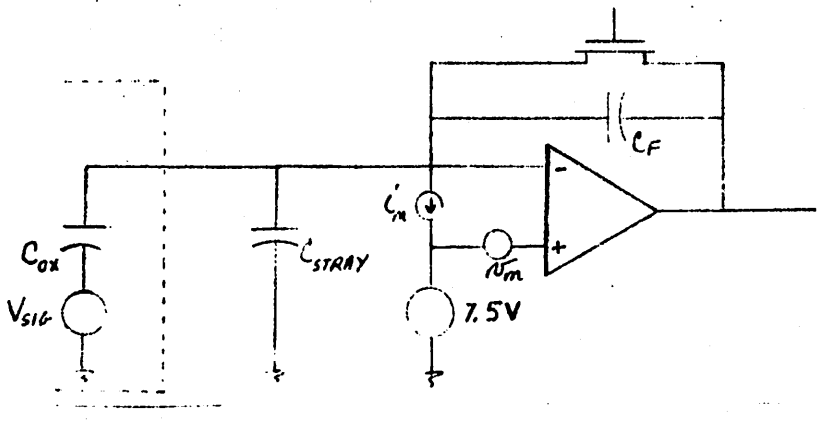


Figure 11. Partial Output Stage, Showing Op-amp's Equivalent Input Noise Sources

The first three points seemed to eliminate the possibility that the noise was being generated externally, the fourth point implied the noise was not coming from the CCD, and the fourth and fifth points together implied that the noise was from the op-amp since:

$$v_{out} = \left(1 + \frac{C_{stray}}{C_F}\right) v_n + \frac{i_n}{j\omega C_F}$$

Therefore, the noise of the 536 operational amplifier used was measured and was found to have an equivalent input current noise of $i_n = 6 \times 10^{-13} A$.

This would yield an output voltage noise of:

$$v_{out} = \left[\int_{1KHZ}^{\infty} \left(\frac{i_n}{2\pi f C} \right)^2 df \right]^{\frac{1}{2}} = \frac{6 \times 10^{-13}}{(2 \times 3.14)\ (10^3)^{\frac{1}{2}}\ (3 \times 10^{-12})} = 1mV,$$

where the lower limit of integration was chosen as 1KHZ since anything lower would have looked more like a DC offset than noise. Clearly, this is about the right level and is probably the major cause of the output noise seen.

Although an MOS amplifier would not have this kind of current noise, it became clear that the amplifier was the noisiest part of the output stage, and the design goal was set of finding or designing a low-noise operational amplifier which would not significantly degrade the signal to noise ratio of the signal from the CCD.

The noise of a CCD has been analyzed by Brodersen et al[3] and was found to be dominated by the surface state noise. Applying the formula developed by the authors to a bandpass filter with 32 stages and with the output stage shown in Figure 8 (with C_F=3pf, $C_{couple} >> C_{hold}$) yields an RMS voltage noise at the output of the circuit equal to 40μV.

[3]Brodersen et al, "A 500 Stage CCD Transversal Filter for Spectral Analysis," Solid State Circuits, Feb. 1976, page 78.

There is also noise associated with resetting the coupling and hold capacitors. The RMS value of this voltage noise is given by $V_n = (\frac{kT}{C})^{\frac{1}{2}}$ where C is the capacitance across the switch which has been opened. In the case of M_{DC}, this is given by $C_{couple} \| C_{hold}$ = 10pf + 1pf = 11pf and the noise level is 19μV. But M_{sample} sees 10pf ~~in~~ series with 1pf $\simeq$ 1pf with a noise level of 65μV. This is too high, but can be cut to a reasonable level by changing the output circuit slightly to that shown in Figure 12.

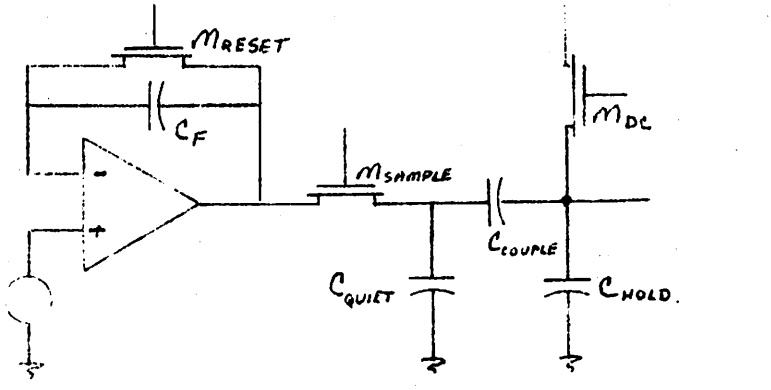


Figure 12. Output Stage with Extra Capacitor

Now M_{DC}, which sees $C_{couple} + C_{hold}$ = 5pf + 1pf = 6pf, has a somewhat higher noise level of 26μV. But the capacitance seen by M_{sample} is approximately $C_{quiet} + C_{hold}$ = 5pf + 1pf = 6pf and 26μV. (This change has the minor side effect of changing the gain through the sample and hold from 0.9 to 0.8.) The feedback capacitor also has a noise associated with its resetting, but since the DC clamp on the output is not released until the resetting is complete, that noise will not appear at the output of the circuit.

Thus the total noise level from sources other than the op-amp is $[(.8x40)^2 + (26)^2 + (26)^2]^{1/2}\mu V$ = 49μV.

III. A LOW NOISE OPERATIONAL AMPLIFIER

Only one major op-amp design for enhancement mode, n-mos transistors seems to exist. It was designed by Yannis Tsividis and published in his doctorial thesis in May, 1976. It's basic properties include an AC gain of 450, bandwidth of 5 MEGHZ, phase margin of 45° and an output voltage range equal to 60 percent of the supply range. It's major drawback is that it needs supply voltages of $\pm$ 15V, and -20V for the substrate bias. This supply range would cause transistors which were built on the lightly-doped substrate needed for a CCD to avalanche. Therefore, before it could be decided whether to use this design or make another, the transistors which would be used had to be modeled, and then Tsividis's design had to be analyzed using this transistor model, and using supplies of +15V and -5V.

Photographs of the I_D versus V_{DS} curves (with V_{GS} as a parameter) for five mos transistors were supplied by Ronald Fellman. These transistors had been fabricated on a lightly-doped substrate ($N_{sub}=10^{+15}$) using the U.C. Berkeley facilities. Their oxide thickness was thinner than could normally be expected ($t_{ox}=7x10^{-6}$cm instead of $10x10^{-6}$cm) but except for that, they could be considered equivalent to transistors which would be fabricated on a CCD chip.

The values for mosfet model parameters required by SPICE (version 2D.1) have been determined for transistors fabricated at U.C. Berkeley and many of these could be used without modification. These are included in Table II. The parameters which still needed defining were N_{SS}, U_o, and λ.

Lambda could be calculated based on the slope of the I_D, V_{DS} line in the saturated region and the equation:

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{I_D \lambda}{1 - \lambda V_{DS}}$$

For each transistor, the slope of the I_D, V_{DS} curve was measured for each value of V_{GS}, λ was calculated and an average value was taken.

Estimates of Uo and N_{SS} were also made for each transistor. These values, together with those of λ, were used as model parameters in SPICE, graphs were generated, and the values were tweaked until the graphs matched the photographs. The results are shown in Table I and Figure 13.

Transistor	L_{eff}*	λ	W^{**}_{drawn}	U_{spice}	N_{SS}
#1	.2	.05	2	750	5.9×10^{10}
#2	.3	.04	.3	1432	15×10^{10}
#3	.4	.033	1.6	968	4.0×10^{10}
#4	.4	.033	10	900	9.2×10^{10}
#5	.5	.02	2.8	930	8.8×10^{10}

*L_{eff} is the effective channel length after diffusion.
**W_{drawn} is the value of the channel width which was drawn on the mask.

TABLE I - Intermediate Model Parameters for SPICE

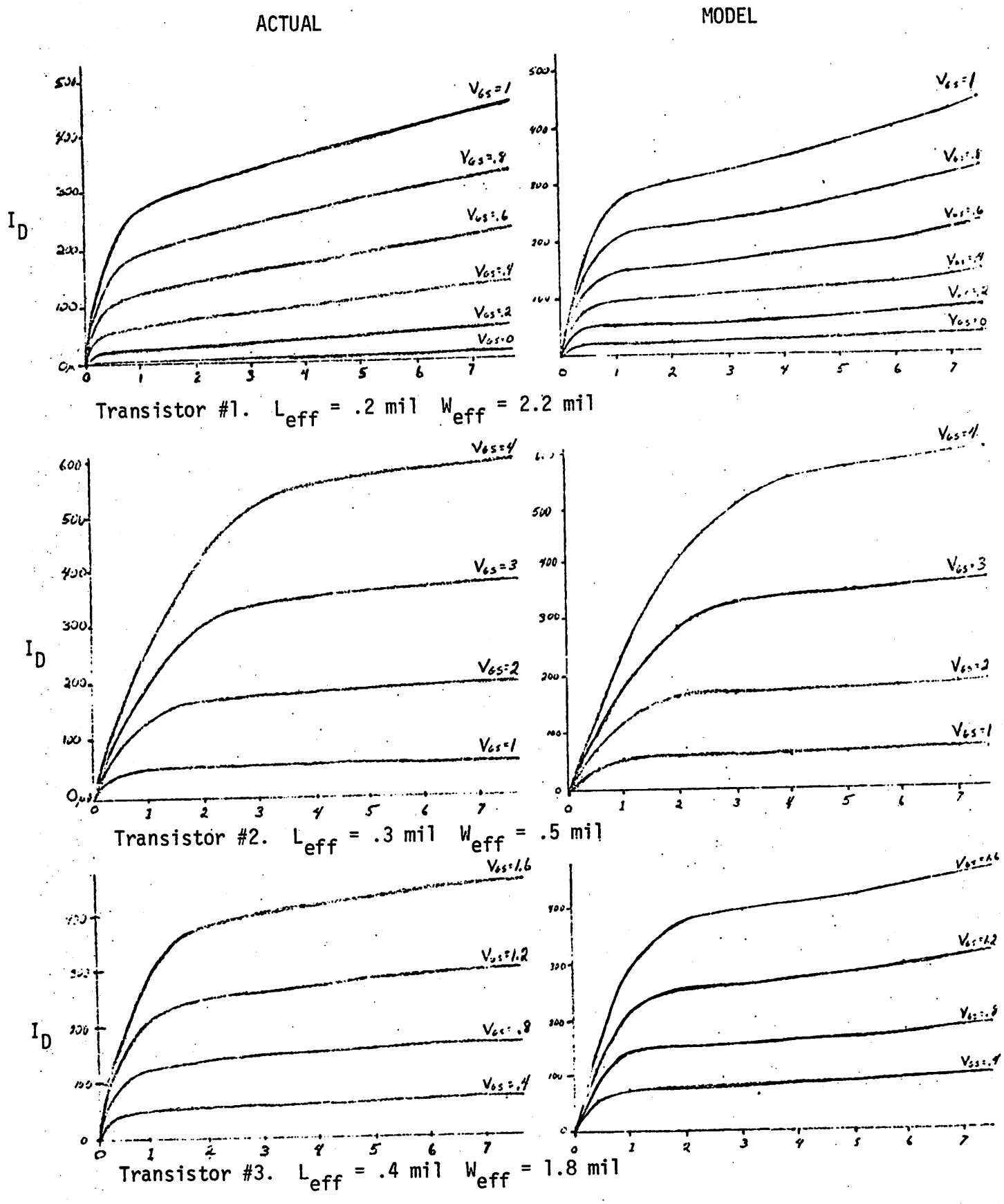
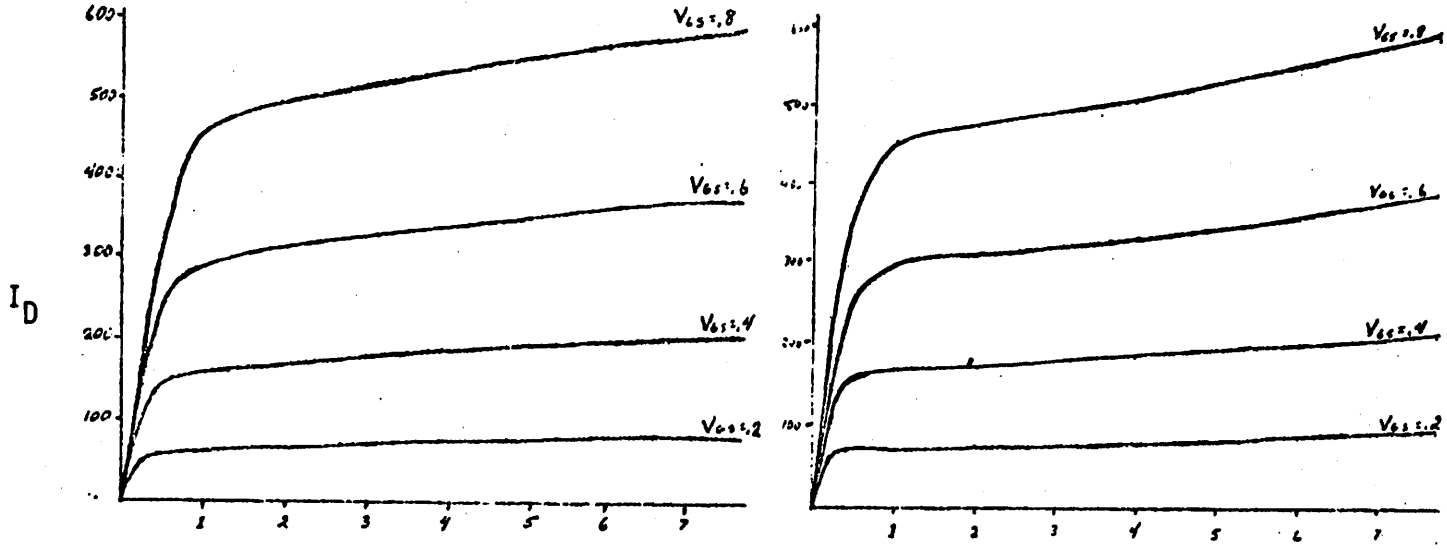
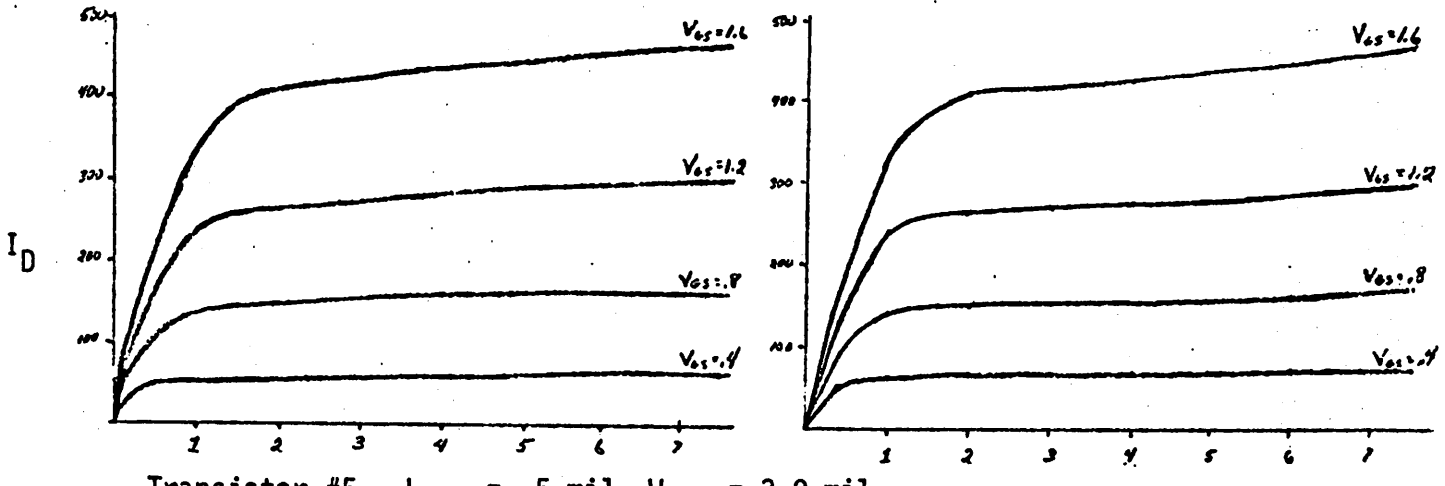


Figure 13. Transistor Model



Transistor #4. L_{eff} = .4 mil W_{eff} = 10 mil



Transistor #5. L_{eff} = .5 mil W_{eff} = 3.0 mil

Figure 13, continued

There are two interesting points brought out in this table. The first is that L and λ appear to be inversly proportional with λ = .011 (1/L) (Figure 14). This is a very useful relationship

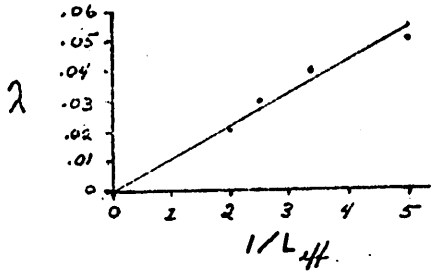


Figure 14. Relationship between L and λ

for predicting the value of λ when L is not one of the values available from the test transistors.

The other interesting fact appears in the relationship between W and Uo. With the exception of transistor #1 (where Uo has starting dropping as a result of the short channel), the larger W is, the smaller Uo appears to be. This could be explained if the effective value of W in the device was larger than the value of W which is drawn on the mask. This in turn might be caused by the fact that the electric field between the drain and source is not perfectly straight, but bows out slightly at the edges. (See Figure 15.)

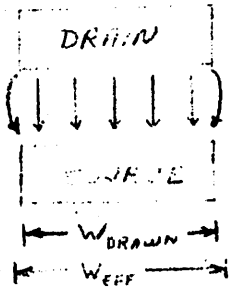


Figure 15. Possible Source of Extra Transistor Width

If this is the case, then the value of Uo given by SPICE is related to the true value of Uo by the equation:

$$U_{spice} = Uo \frac{W_{effective}}{W_{drawn}} = Uo \frac{W_{drawn} + \Delta W}{W_{drawn}}$$

or,

$$\Delta W = (U_{spice})(W_{drawn})(\frac{1}{Uo}) - W_{drawn}$$

The actual value of ΔW and Uo could be found by graphing the lines given by the above equation for each transistor, and finding their interaction. This is shown in Figure 16.

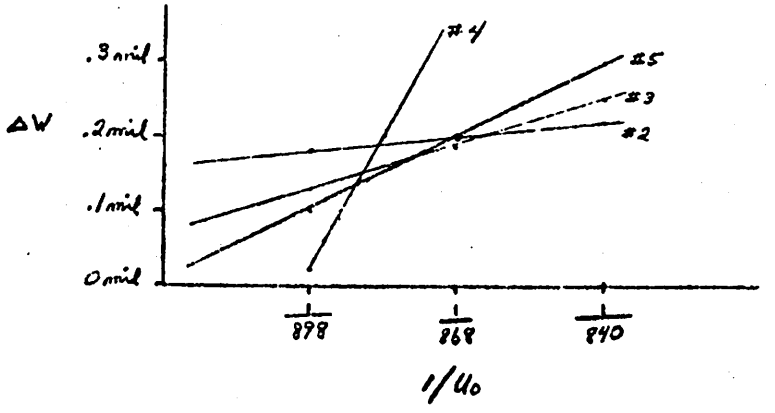


Figure 16. Relationship between W and Uo

The lines for models 2, 3, and 4 intersect nearly perfectly, and forcing #4 to fit will only change its output current by 3 percent. Therefore, the final results are that Uo = 868 and $W_{effective} = W_{drawn} + .2$ mil. The final results for the model are shown in Table II.

TABLE II

MOSFET MODEL PARAMETERS FOR SPICE

Parameter	Value	Description
N_{sub}	$1x10^{15}$	Substrate doping
t_{ox}	$1x10^{-5}$	Oxide thickness in cm
N_{SS}	$8.65x10^{10}$	Surface state density
Uo	868	Surface mobility
λ	$.011(1/L_{eff})$	Channel length modulation parameter
ΔW	.2 mil	Channel width modulation parameter
PHI	.58	Surface potential at strong inversion
XJ	$2.95x10^{-4}$	Metallurgical junction depth
LD	.83	Latural diffusion coefficient
U_{crit}	$4.9x10^{4}$	Critical field for mobility degradation
U_{exp}	.1	Critical field exponent
U_{tra}	0	Transfield factor
CGD	$2.1x10^{-11}$	Gate-drain overlap capacitance per cm channel width
CGS	$2.1x10^{-11}$	Gate source overlap capacitance per cm channel width
CGB	$1x10^{-12}$	Gate bulk overlap capacitance per cm channel length
CBD	$1.2x10^{-8}$	Zero bias B-D junction cap per cm^2 junction area
CBS	$1.2x10^{-8}$	Zero bias B-S junction cap per cm^2 junction area

TABLE II, cont.

MOSFET MODEL EQUATIONS USED IN SPICE

Linear: $$I_D = U_{eff}\, C_{ox} \frac{W_{eff}}{L_{eff}(1-\lambda V_{DS})} \left(V_{GS}-V_{bi}-\frac{V_{DS}}{2}\right)(V_{DS}) - \frac{2}{3}\gamma_d\left((V_{DS}+PHI-V_{BS})^{\frac{3}{2}}-(PHI-V_{BS})^{\frac{3}{2}}\right)$$

Saturation: $$I_D = U_{eff}\, C_{ox} \frac{W_{eff}}{L_{eff}(1-\lambda V_{DS})} \frac{1}{2}(V_{GS}-V_{bi})^2 - \frac{1}{4}\gamma_d{}^4\, f^2(V_{GS},V_{BS}) - \frac{2}{3}\gamma_d\left((V_{GS}-V_{bi}+\frac{1}{2}\gamma_d f(V_{GS},V_{BS})+PHI-V_{BS})^{\frac{3}{2}}-(PHI-V_{BS})^{\frac{3}{2}}\right)$$

where:

$$U_{eff} = U_o \left(\frac{U_{crit}\cdot t_{ox}}{V_{GS}-V_{bi}-U_{tra}\cdot V_{DS}}\right)^{U_{exp}}$$

$$C_{ox} = \frac{\varepsilon_{ox}\,\varepsilon_o}{t_{ox}}$$

$$W_{eff} = W_{drawn} + \Delta W$$

$$L_{eff} = L_{drawn} - 2\cdot XJ\cdot LD$$

$$V_{bi} = \Phi_{MS} - \frac{q\cdot N_{SS}}{C_{ox}} + PHI$$

$$\gamma_d = \frac{\sqrt{2\varepsilon_{si}\varepsilon_o q\, N_{sub}}}{C_{ox}}\left(1 + \frac{XJ}{L_{drawn}} - \frac{XJ}{L_{drawn}}\left(1 + \frac{2\sqrt{2\varepsilon_{si}\varepsilon_o/q\, N_{sub}}\ \sqrt{PHI - V_{BS}}}{XJ}\right)^{\frac{1}{2}}\right)$$

$$f(V_{GS},V_{BS}) = 1 - \left(1 + 4\left(\frac{V_{GS}-V_{bi}+PHI-V_{BS}}{\gamma_d{}^2}\right)\right)^{1/2}$$

Since a noise analysis is going to be undertaken for the op-amp chosen, it is necessary to model the noise of the mos transistors. This consists of two parts, thermal noise and $\frac{1}{f}$ noise. Both types can be modeled as a noise current between the drain and source or as a voltage noise in series with the gate as shown in Figure 17.

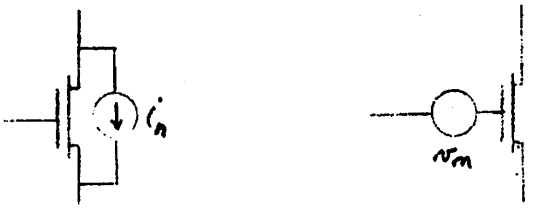


Figure 17. Transistor Equivalent Noise Sources

Thermal noise is given by the equation $i_n^2 = 4kT\ (\frac{2}{3}gm)$ and $\frac{1}{f}$ noise by the equation:

$$i_n^2 = \frac{K\ I_D}{C_G\ f^b} \quad \text{where } a \simeq 1 \text{ and } b \simeq 1.$$

Warren Ong[4] analyzed the parameters a, b, and $\frac{K}{C_G}$ for $\frac{1}{f}$ noise. Unfortunately, he did not report the value of C_G, but based on the information given, we were able to predict that it was the gate capacitance of a transistor made at Berkeley and having a W = 3.5mil and an L_{eff}= .8mil. Using the numbers he developed, the total noise in a mosfet can be modeled as $i_n^2 = 4kT\ (\frac{2}{3}\ gm) + \frac{(9.5x10^{-15})I_D^{1.2}}{(W_{eff} x L_{eff})\ f^{.88}}$

or $v_n^2 = 4kT\ (\frac{2}{3gm}) + (9.5 x 10^{-15})\ I_D^{1.2}/(W_{eff} \times L_{eff})(gm^2)(f^{.88})$

$$= [\frac{1.38}{\sqrt{W/L}\ \sqrt{I_D}} + \frac{1.34x10^8}{f^{.88}}\ (\frac{I_D \cdot 2}{W^2})]^{1/2}\ mV/\sqrt{HZ}^5$$

[4]Ong, "Noise Characterization of MOSFETS," page 27.

[5]This equation is obtained from the one before it by using the expression $gm = (2K'\ I_D\ W/L)^{1/2}$

Tsividis had measured his op-amp as having 60μV equivalent input noise between 10Hz and 10KHz. So to test the validity of the noise model, I analyzed the noise of his circuit (with the aid of Spice, by a method described in detail later) and obtained an equivalent input noise of 40μV. Clearly the agreement is not perfect, but it is probably satisfactory when working with noise.

It was now time to see if the existing op-amp design would be satisfactory in this application. The circuit is shown in Figure 18 and Table III. With the output approximately centered between the supplies (V_{out} = 8.5V) the circuit had an AC gain of 200, unity gain bandwidth of 8 MEGHz (C_{comp} = 40pf) and phase margin 45°. But as the DC transfer curve (Figure 19) shows, the circuit could not maintain that gain through much of its range. The range was also rather limited since, although the highest ouput voltage was a good 13.5 volts, the lowest output voltage was only 5 volts. And finally, the output noise through the previously designed output stage was 180μV (see Appendix A). This is significantly higher than the desired result of about 60μV, so it was decided to design a lower noise op-amp which would work well when built on lightly doped substrates.

In general, an operational amplifier can be broken up into four stages - a differential input stage, a differential to single ended converter, a gain stage (with a capacitor across it), and an output stage, as shown in Figure 20.

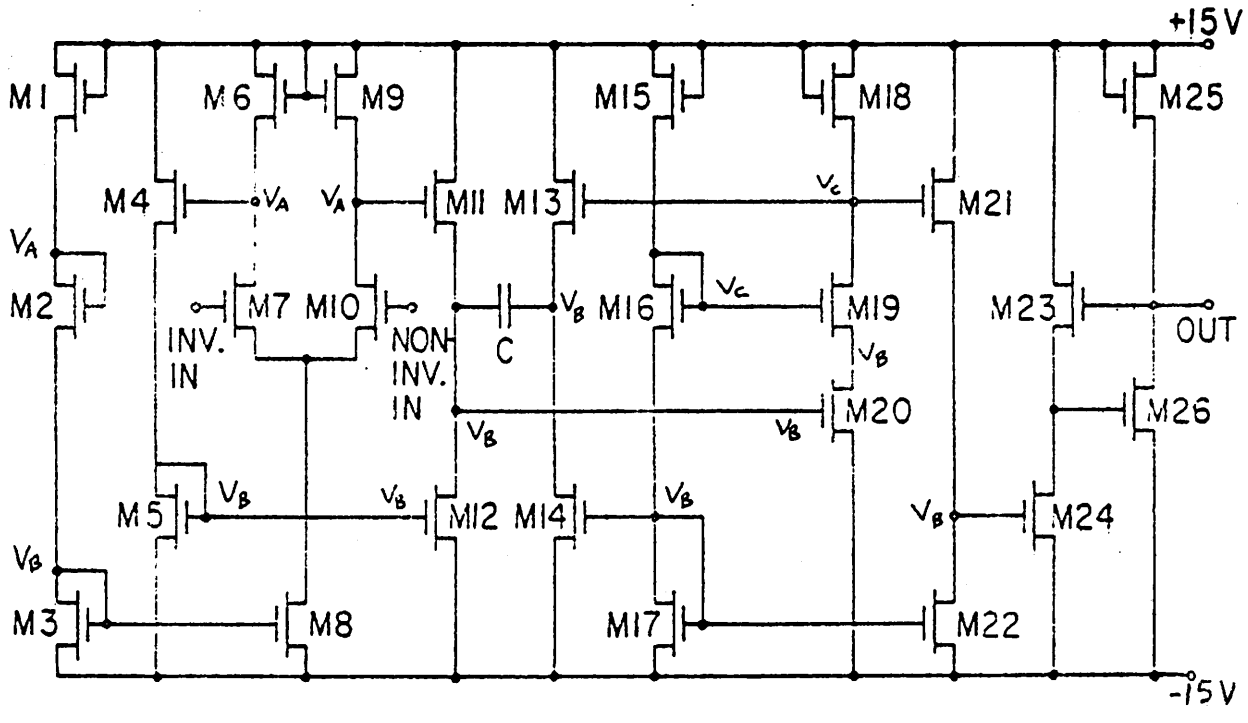


Figure 18. Tsividis's Op-Amp

TABLE III

DEVICE SIZES FOR TSIVIDIS'S OP-AMP

Device	W_{drawn} in mils	L_{drawn} in mils	W/L Expected
M1	3.500	1.000	4.38
M2	.500	10.500	.0667
M3	3.500	1.00	4.38
M4	.500	4.125	.170
M5	3.725	.500	12.46
M6	1.750	1.000	2.19
M7	18.000	.500	60.20
M8	3.500	1.000	4.38
M9	1.750	1.000	2.19
M10	18.000	.500	60.20
M11	.500	4.125	.170
M12	3.725	.500	12.46
M13	5.500	.500	19.23
M14	5.750	.500	18.39
M15	.500	8.175	.0856
M16	2.250	.500	7.525
M17	2.250	.500	7.525
M18	.500	1.775	.596
M19	8.750	.500	29.26
M20	8.750	.500	29.26

TABLE III (Cont)

Device	W_{drawn}	L_{drawn}	W/L Expected
M21	8.500	.500	28.43
M22	8.750	.500	29.26
M23	.750	1.500	.731
M24	15.250	.500	48.49
M25	1.500	1.675	1.15
M26	12.250	1.000	22.18

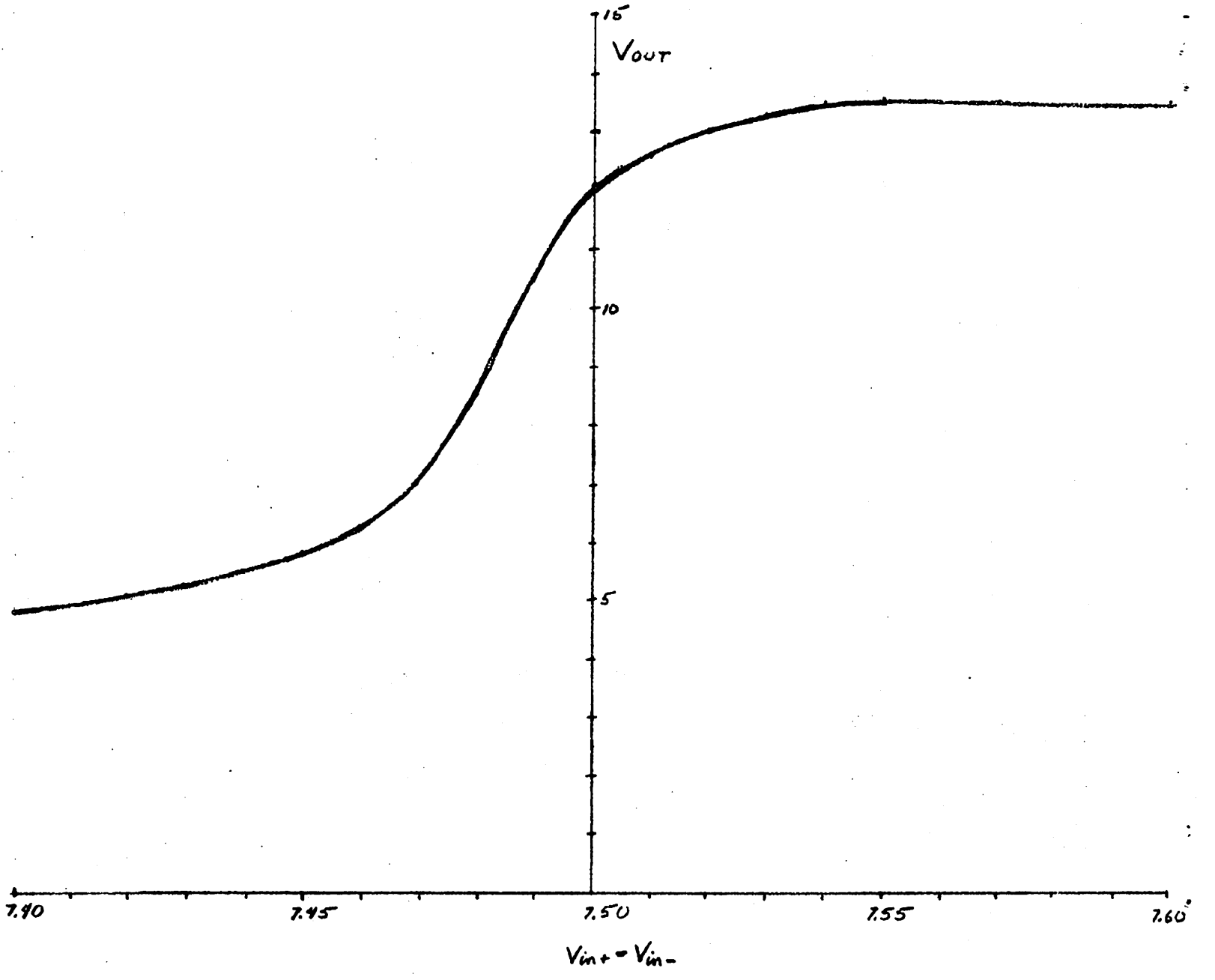


Figure 19. DC Transfer Curve for Tsividis's Op-Amp

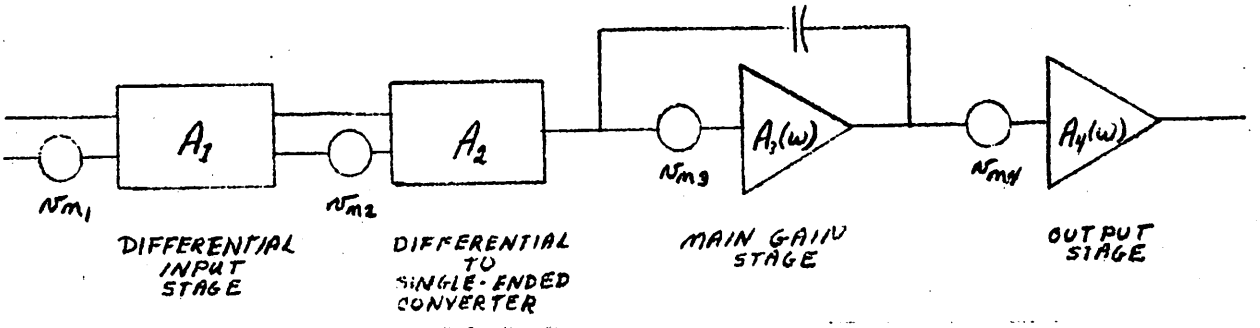


Figure 20. A Four Stage Amplifier with Noise Sources

Now imagine each stage has an input voltage noise associated with it. The total equivalent noise at the input to the amplifier can be calculated by finding the noise gain from each source to the output, then dividing by the gain from input to output. Thus:

$$v_{out}^2 = v_{n1}^2 \cdot (A_1 A_2 A_3(\omega) A_4(\omega))^2 + v_{n2}^2 (A_2 A_3(\omega) A_4(\omega))^2 +$$

$$v_{n3}^2 (A_3(\omega) A_4(\omega)) + v_{n4}^2 (A_4(\omega))^2$$

$$v_{eq}^2 = v_{n1}^2 + \frac{v_{n2}^2}{A_1^2} + \frac{v_{n3}^2}{(A_1 A_2)^2} + \frac{v_{n4}^2}{(A_2 A_2 A_3(\omega))^2}$$

Notice that each noise source appears at the input, divided by the gain that preceeded it, so if the gains at the front of the op-amp are large, the total noise will be correspondingly small. But also notice that at high frequencies where $A_3(\omega)$ is small, v_{n4} may easily become the dominate noise source. Therefore, there are at least four useful rules in designing a low noise amplifier:

1. Use low noise transistors

2. Do not use any more bandwidth than necessary

3. If a stage is inherently noisy, preceed it with as much gain as possible

4. Follow the main gain stage with the quietest possible output stage, preferably one having unity gain

Transistors can be designed to have low thermal noise by giving them a large current and a large W/L. This does, however, require large devices and high power consumption, which is a disadvantage.

By far the noisiest stage which will be used in this op-amp is a source follower which is designed to drop a large voltage. This is because the signal gain from input to output is about one, but the noise gain from the current source transistor to the output is equal to the gm ratio of the two transistors. Thus, referring to Figure 21,

$$I = \frac{K'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2 = \frac{K'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2$$

$$\sqrt{W/L}_2 \, (V_{GS2} - V_T) = \sqrt{W/L}_1 \, (V_{GS1} - V_T)$$

$$\frac{V_{GS2} - V_T}{V_{GS1} - V_T} = \frac{\sqrt{W/L_1}}{\sqrt{W/L_2}}$$

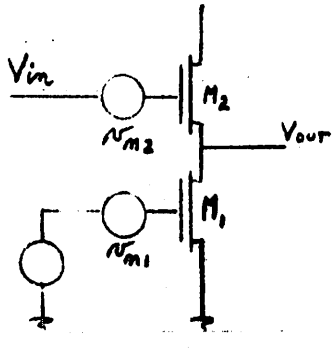


Figure 21. Noise in a Source Follower

However, the output noise is:

$$v^2_{\text{noise out}} = v_{n1}^2 \left(\frac{gm_1}{gm_2}\right)^2 + v_{n2}^2 = v_{n1}^2 \left(\frac{W/L_1}{W/L_2}\right) + v_{n2}^2$$

which can be significantly larger than just $v_{n1}^2 + v_{n2}^2$ if V_{GS2} is significantly larger than V_{GS1}.

The light substrate doping meant that the maximum difference between the most positive and most negative supply could be only 20V. Anything larger could cause avalanche breakdowns in the transistors. It also meant that the transistors' threshold voltage was not very dependent on the backgate bias voltage. Since the zero bias threshold voltage is very near zero this meant the circuit had to be designed for very small $V_{T's}$. Furthermore, on short channel devices ($L \leq .5$ mil) the effect of V_{BS} was even less than on devices with longer channels. It was determined using SPICE that in order to achieve a V_{TH} of .4V or greater with 5 volts backgate bias, the channel length had to be .7 mil or wider. Finally, transistors fabricated on light substrates have a much lower drain-source impedance when the device is in saturation than those built on heavy substrates. This effect became noticeable when $L \leq .4$ mil.

Keeping these facts about noise and threshold voltage in mind, the circuit shown in Figure 22 and Table IV was developed.

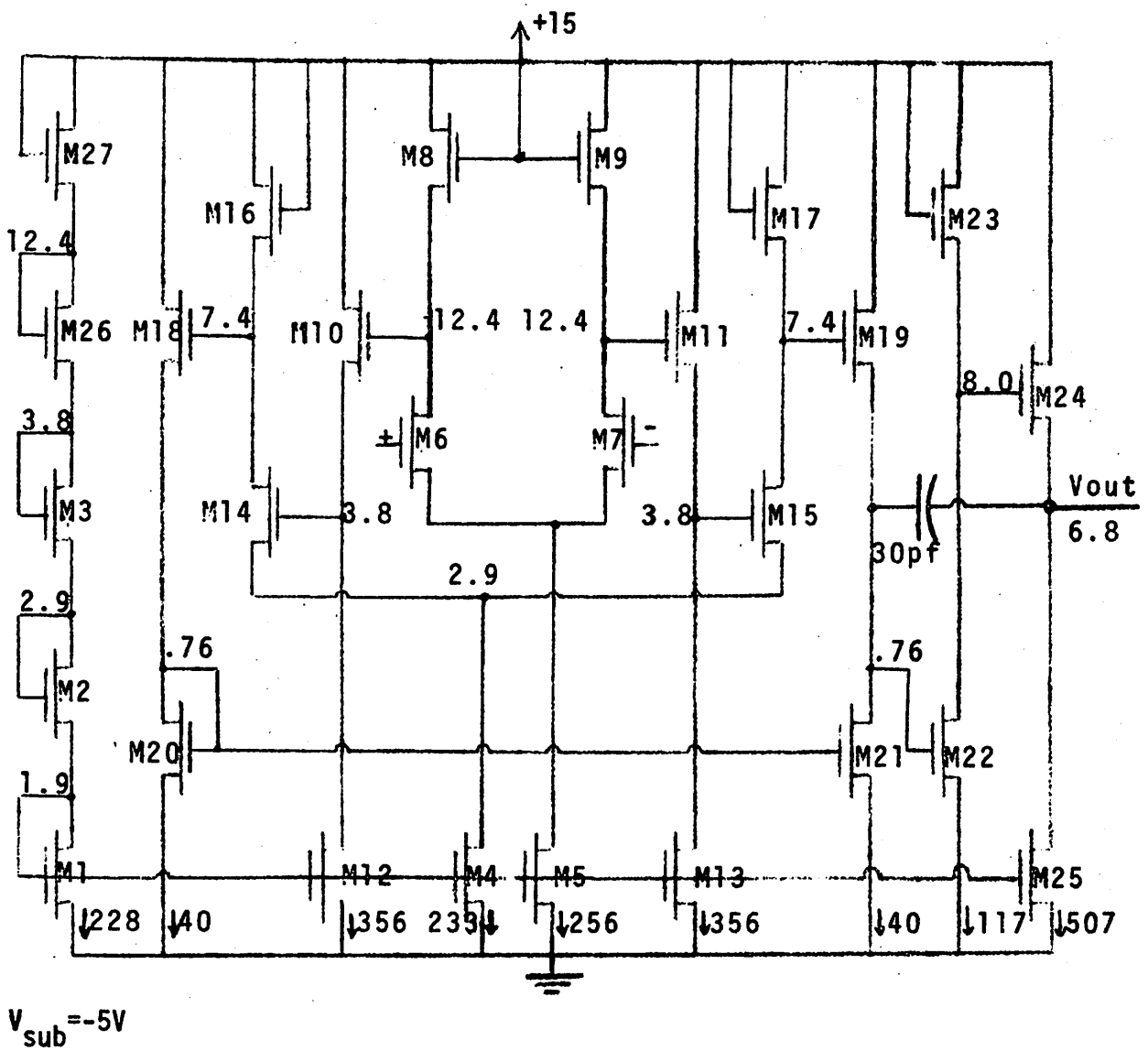


Figure 22. Low Noise Operational Amplifier

Table IV

DEVICE SIZES AND OPERATING POINT OF THE LOW-NOISE OP-AMP

	W_{drawn}	L_{drawn}	W/L_{eff}	I_D	gm	g_{DS}
M1	3.4 mil	.7 mil	7.2	231×10^{-6}	290×10^{-6}	4.81×10^{-6}
M2	6.0	.4	30.0	231	551	12.1
M3	6.0	.4	30.0	231	552	12.1
M26	.5	2.5	.30	231	56.1	12.1
M27	3.4	.7	7.2	231	296	4.87
M4	3.4	.7	7.2	236	295	4.99
M5	3.4	.7	7.2	259	325	6.05
M6	30.0	.4	150.0	130	1090	8.84
M7	30.0	.4	150.0	130	1090	8.84
M8	1.6	.7	3.6	130	156	2.74
M9	1.6	.7	3.6	130	156	2.74
M10	1.2	3.2	.467	360	87.3	1.96
M11	1.2	3.2	.467	360	87.3	1.91
M12	5.2	.7	10.4	360	451	7.77
M13	5.2	.7	10.4	360	451	7.77
M14	2.8	.4	15.0	118	311	7.66
M15	2.8	.4	15.0	118	311	7.66
M16	.5	3.2	.167	118	35.0	.239
M17	.5	3.2	.167	118	35.0	.239
M18	.5	8.0	.0625	39.6	12.6	.081
M19	.5	8.0	.0625	39.6	12.6	.081
M20	8.0	.7	16.4	39.6	187	.804
M21	8.0	.7	16.4	39.6	187	.804
M22	20.0	.7	40.0	115	543	2.73
M23	.5	3	.179	115	36.3	.598
M24	30.0	.5	100.0	515	2030	30.7
M25	7.0	.7	1.36	515	644	11.9

Transistors M5 - M9 form the input differential stage. Its differential gain (G_{diff_1}) is given by $\frac{v_{out,\,dm}}{v_{in,\,dm}} = \frac{gm_6}{gm_8}$. Its common mode gain is given by $\frac{v_{out,\,cm}}{v_{in,\,cm}} = \frac{g_{DS5}}{2(gm_8)}$. The values of gm_6 and gm_8 were mostly set by external considerations. M_6 and M_7 were given the largest W/L that device size constraints would permit (W = 30 mil), L = .4 mil). the current through M5 was set high enough (256 μA) to insure that the input transistors were not too noisy, but low enough to avoid dropping excessive voltage across M8 and M9. The W/L ratio of M8 and M9 was then set so the transistors would drop 2.5V. This yielded W=1.6mil, L=.7mil, so the differential gain of the stage was $\frac{gm_6}{gm_8} = \frac{W/L_6}{W/L_8} = 6$.

The first stage is then followed by some level shifting sources followers with a gain G_{SF} of .95, and the next stage is another differential amplifier. Its main purpose is to provide the rest of the gain, external to the main gain stage, for which the op-amp can be compensated.

The next stage consisting of M18 - M21, is the differential to single-ended converter. It was put this far from the input stage because it is very noisy. Its design was strongly related to the design of the high gain stage which follows it, so they will be discussed together.

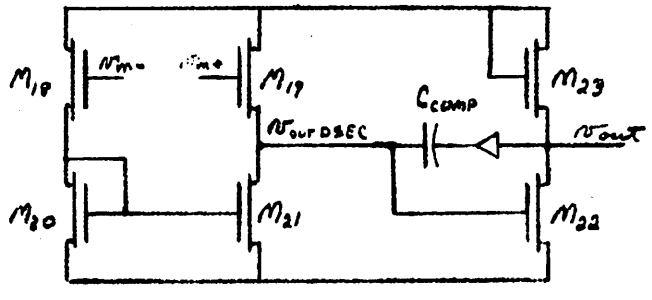


Figure 23. Differential to Single-Ended Converter and Gain Stage

Referring to Figure 23, the voltage gain through the differential to single-ended converter is given by:

$$v_{outDSEC} = v_{in}\left(\frac{gm_{18}}{gm_{20}+gm_{18}}\right)\left(\frac{gm_{21}}{gm_{19}+g_{DS21}}\right) + v_{in}\left(\frac{gm_{19}}{g_{DS\,21}+gm_{19}}\right)$$

$$= (v_{in+} - v_{in-})\left(\frac{gm_{19}}{2(g_{DS21}+gm_{19})}\right)\left(1+\frac{gm_{18}\,gm_{21}}{gm_{19}\,(gm_{20}+gm_{18})}\right)$$

$$+ \frac{v_{in+}\,v_{in-}}{2}\left(\frac{gm_{19}}{g_{DS21}+gm_{19}}\right)\left(1 - \frac{gm_{18}\,gm_{21}}{gm_{19}\,(gm_{20}+gm_{18}}\right)$$

assuming $gm_{21} = gm_{20}$, $gm_{19} = gm_{18}$ and $g_{DS21} << gm_{19}$,

$$v_{outDSEC} = (v_{in+} - v_{in-})\left(\frac{1}{2}\right)\left(1+\frac{gm_{18}}{gm_{18}+gm_{20}}\right)+(v_{in+} + v_{in-})\left(\frac{1}{2}\right)\left(1-\frac{gm_{18}}{gm_{18}+gm_{20}}\right)$$

therefore, by making $gm_{20} >> gm_{18}$, the differential gain G_{DSEC} will approach one and the common mode gain will approach zero. Now if in the next stage, gm_{22}/gm_{23} is made equal to gm_{20}/gm_{18}, $gm_{22} >> gm_{23}$ and the condition for high gain will be met for that stage.

The dominant pole of this system is to be given by $\frac{gm_{19}}{C_{comp}(1+G_G)}$, where G_G is the gain of the main gain stage. Therefore, the smaller gm_{19} is made, the smaller C_{comp} can be, or the greater the gain in the previous stages can be for a given bandwidth. For instance, in this particular case, the desired bandwidth is 2.5 MEGHz. The gain through the entire circuit is $G(\omega) = G_{diff_1}\, G_{SF}\, G_{diff_2}\, G_{DSEC}\, G_G / 1+j\omega\left(\frac{G_G C_{comp}}{gm_{19}}\right)$

$\simeq \frac{G_{Diff_1}\, G_{SF}\, G_{Diff_2} G_{DSEC}}{\omega\, C_{comp}/gm_{19}}$ at high frequencies

At $\omega = 2\Pi$ x 2.5 MEGHz we want $G(\omega) = 1$, therefore,

$$G_{Diff_2} = \frac{(2\Pi)(2.5\times10^{6})(C_{comp}/gm_{19})}{G_{Diff2}\ G_{SF}\ G_{DSEC}}$$

For this circuit C_{comp} = 30pf, $gm_{19} = 1.3\times10^{-5}$, $G_{Diff1} = 6$,

$G_{SF} = .95$, $G_{DSEC} = .92$, so G_{Diff2} may be given a value of:

$$\frac{2X3.14x2.5x10^{6}x30x10^{-12}/1.3x10^{-5}}{6x.95x.92} = 7.$$

The output stage is a simple source follower, designed with high current and high W/L so its transistors will be quiet and it will be able to supply a large current without dropping much voltage. The compensation capacitor is connected to the output of the source follower, rather than directly across M_{22} in order to avoid the zero at $\frac{gm_{22}}{C_{comp}}$ which that configuration would exhibit.[6]

The major problem with this circuit was achieving a reasonably large slew rate while keeping gm_{19} small. Look again at Figure 23. When the op-amp is slewing, V_{in-} will be at its most negative value (V_{min}) and the current in M_{21} (I_{min}) will $\frac{K'}{2}(W/L)_{18}\ (V_{min} - V_T)^2$. Similarly, the current in M_{19} (I_{max}) will be $\frac{K'}{2}(W/L)_{19}(V_{max} - V_T)^2$. So if the quiescent current I_Q is defined as $\frac{K'}{2}(W/L)\ (V_Q - V_T)^2$, then the current available to charge C_{comp} (I_{slew}) is the difference between I_{min} and I_{max} and $I_{slew} = I_Q\ [(\frac{V_{max} - V_T}{V_Q - V_T})^2 - (\frac{V_{min} - V_T}{V_Q - V_T})^2]$.

[6]For more information on this zero, and all stages used in this op-amp, see Tsividis, "Nonuniform Pulse Code Modulation Encoding Using Integrated Circuit Techniques," chapter 5.

Cearly, it is desirable to have I_Q as large as possible, but that level is basically determined by the gm needed for compensating the amplifier. The other option is to make $\frac{V_{in\ max}}{V_{in\ Q}}$ as large as possible. Obviously, if $V_{in\ max}$ can be made twice as large as $V_{in\ Q}$, a slew current of three to four times the quiescent current will be available. This is the method which was used, but is required careful biasing of the entire circuit. The voltages and currents resulting from this biasing are shown in Figure 22 and their rational is as follows.

Since it is desirable to have the voltage level into the differential to single ended converter as low as possible, it is desirable to have the voltage at the gates of M_{14} and M_{15} as low as possible. This voltage was chosen to be 4 volts, which allows V_{GS14} and V_{GS15} to be one volt and V_{DS4} to be one volt greater than V_{GS4}, thus insuring that M_4 is in saturation. Unfortunately achieving this voltage requires a large voltage drop across M_{10} and M_{11} compared with M_{12} and M_{13}, making this an inherently noisy stage. Therefore, the current was set very high (350μV) to reduce the noise. (This high current was also necessary in order to reduce the gm of M_{10} & M_{11} since they were driving the Miller multiplied gate-drain capacitance of M_{14} and M_{15}.)

Now the voltage which could be dropped across M_{16} and M_{17} had to be determined. To do this, imagine the voltage at the gate to M_6 is much lower than the voltage at M_7 (the condition which exists while slewing downward). Then all the current from M_5 will be flowing through M_9, so M_8 will be off, so the voltage across M_8 will be V_{T8}, which means

the voltage at the gate of M_{10} will be 4V + 1.5V = 5.5V. Similarly, the voltage at the gate of M_{15} will be about 3V, so all the current from M_4 will be flowing through M_{14} and M_{16}, as long as M_{14} is saturated. Therefore, the gate-source voltage of M_{16} should be 15 - 5.5 = 9.5V when all the current is flowing through it. Therefore, when half the current is flowing the voltage across M_{16} should be $(9.5V - V_{TH}) \frac{1}{\sqrt{2}} + V_{TH} = 7.2V$. Therefore, the quiescent voltage at the gates of M_{18} and M_{19} should be 15 - 7.2V = 7.8V. The desire to have $gm_{19} \cong 1x10^{-5}$ plus the knowledge that they would be dropping about 7V, yielded a W/L for M_{18} and M_{19} of $\frac{.7}{8}$ which yielded a current of 40μA. This in turn meant the slew current would equal about

$40\ [(\frac{12 - .6}{6.6-.6})^2 - \frac{4-.6}{6.6-.6})^2]$ = 130μA and the slew rate would be 130μA/30pf = 4.3V/μsec.

M_{20} and M_{21} were then given a W/L of 8/.7 because for this value, their effect on the thermal noise of the op-amp would be about the same as the effect of the input transistors. L was chosen to equal .7 volts, because that value would yield a threshold voltage of .4V, and increasing L further would not increase the threshold much. It was important to have a high threshold because it was neccessary that M_{21} stay in saturation when V_{out} was at its most positive value. The W/L of M_{22} was made three times that of M_{21} in order to keep down the noise of the device, and M_{23} was likewise scaled, giving this stage a gain of 13. Since M_{23} ought to drop about the same voltage as M_{19}, it ought to drop about 7V. Transistors M_{24}

and M_{25} form a source follower, with M_{24} dropping about one volt. Therefore, the output of the op-amp has been biased to sit at 7V, very near the center of the supply range, by use of a simple symmetry.

The most troublesome part of this design so far, is in making sure that M_4 stays biased in the saturated region when the device parameters (especially V_{TH}) are changed. To insure that this would be alright, the bias chain of M_1 - M_{27} was constructed. It works on the following principle. Notice that the V_{GD} of M_4 (the voltage which must be kept positive) is equal to $V_{DD} - V_{GS8} - V_{GS10} - V_{GS14} - V_{GS4}$. If the bias chain can be designed so that $V_{GS27} = V_{GS8}$, $V_{GS26} = V_{GS10}$, $V_{GS3} = V_{GS14}$, and $V_{GS1} = V_{GS4}$, then V_{GD4} will equal V_{GS2}, by default. This can be achieved by using the fact that $V_{GSa} = V_{GSb}$ if $I_a/(W/L)_a = I_b/(W/L)_b$, assuming $V_{THa} = V_{THb}$. Therefore, every current in the first three stages was made proportional to the current in the bias string by using V_{GS1} as the gate voltage for all the current sources. Then the W/L's in the bias chain were scaled to those whose voltage they were supposed to drop using the equation $(W/L)_b = I_b/I_a \cdot (W/L)_a$. The validity of this method was tested by doubling the substrate doping given to SPICE and checking the new operating point and the new ac characteristics. The circuit behaved as expected with the voltages along the bias string changing somewhat due to the changed threshold voltages but with the other bias points mirroring them almost perfectly, and with the other ac characteristics essentially unchanged.

The op-amps entire performance was then tested on SPICE and the results agreed well with the hand calculations. They are shown in Figures 24 - 26.

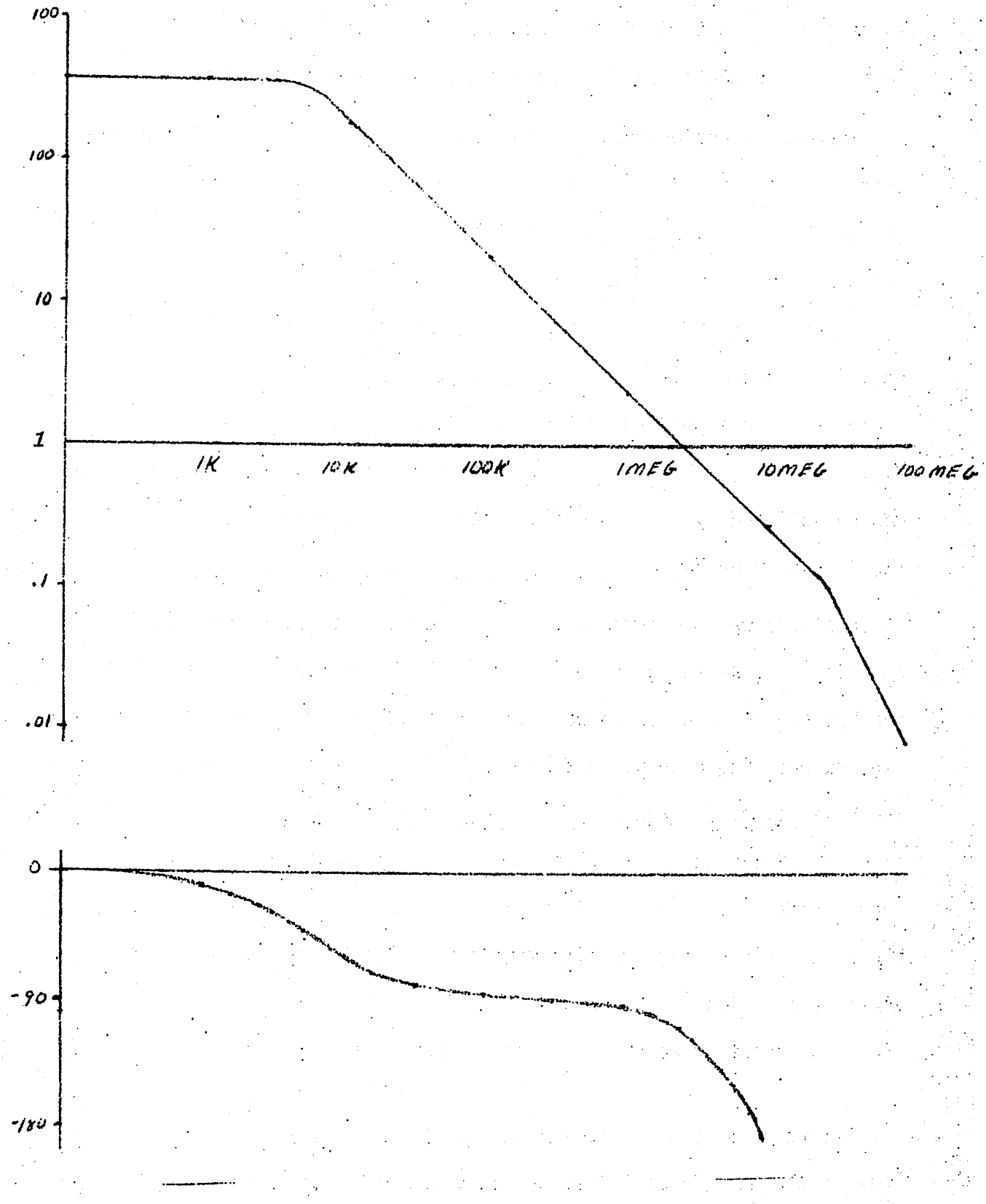


Figure 24. AC Gain and Phase for Low Noise Op-Amp

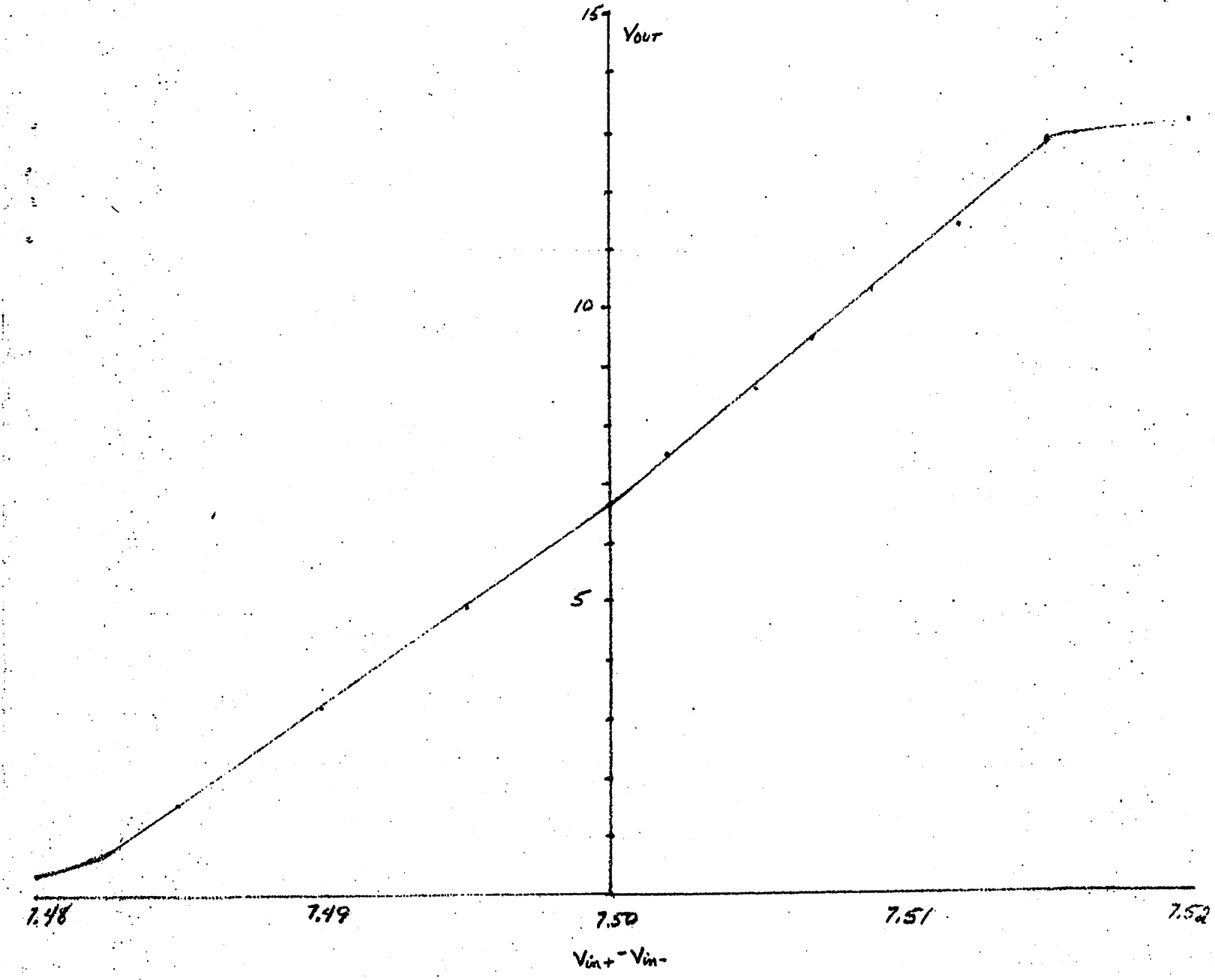


Figure 25. DC Transfer Curve for Low Noise Op-Amp

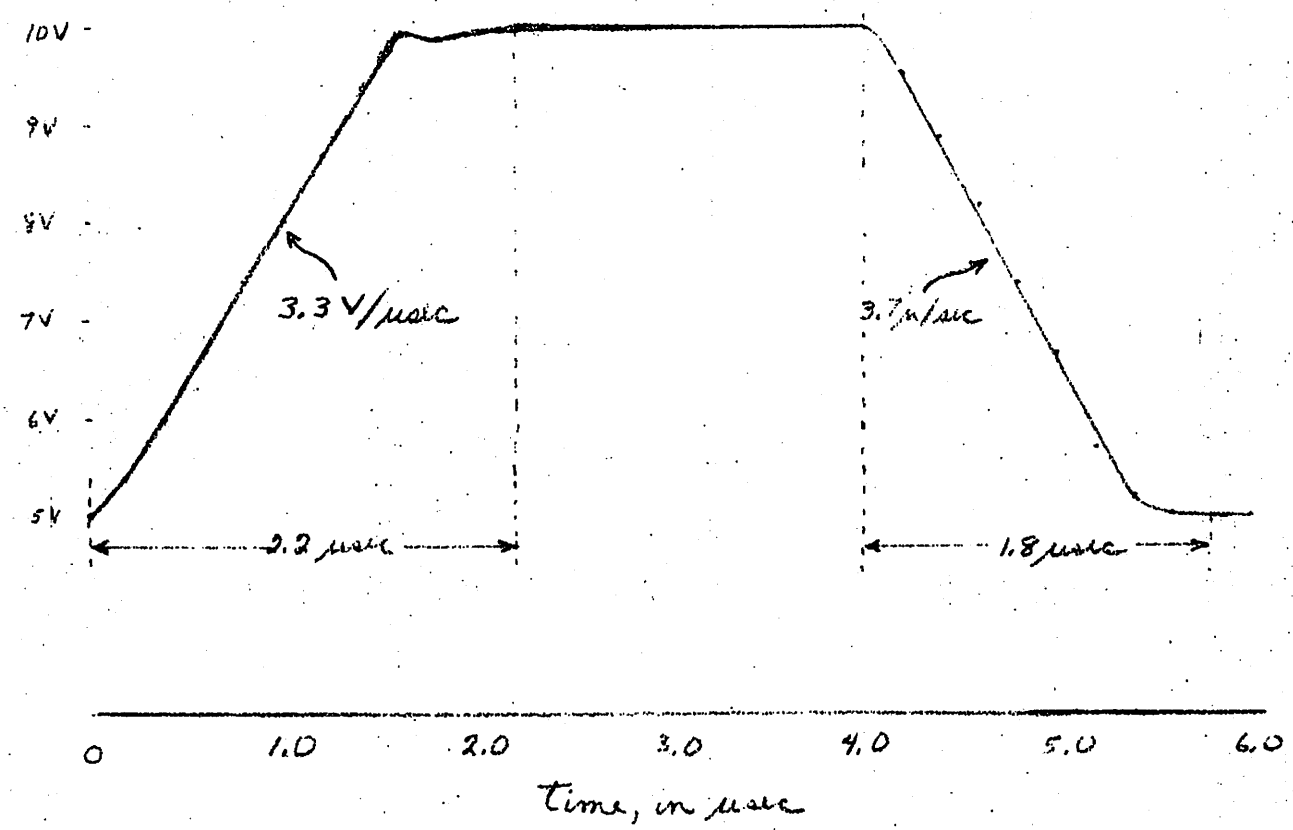


Figure 26. Five Volt Step Response of Low Noise Op-Amp

Notice in Figure 24 that the op-amp has small signal gain of 380, a phase margin of 79° and a bandwidth of 2.5 MHz. It also has a common mode gain at DC of 7.5×10^{-4}, yielding a CMRR of 114db. Its DC output range is .3V to 12.5V. It slews at 3.5v/μsec and it settles to .05% from a 5 volt step in 2.0 μsec. It draws a total current of 2.2mA and dissipates 32 mW. The total gate area is 118 mil^2.

As a final test the op-amp was hooked up as it would be used in the circuit and the waveforms out of the op-amp and out of the sample and hold were plotted. The results are shown in Figure 27. The crucial test of the op-amp in this configuration is in whether the gain from the input to the output of the op-amp has been linear. If so, then:

$$\Delta V_{out} = -\Delta V_{sig} \frac{C_{sig}}{C_F + \frac{C_{sig}+C_{FZ}+C_{stray}+C_F}{A}} - \Delta V_{FZ} \frac{C_{FZ}}{C_F + \frac{C_{sig}+C_{FZ}+C_{stray}+C_F}{A}}$$

$$= 4 \left(\frac{.3}{3 + \frac{.3+6+1.6(3.5)+3}{400}} \right) + 1 \left(\frac{6}{3 + \frac{.3+6+1.6(3.5)+3}{400}} \right)$$

$$= 2.371V$$

SPICE gave an answer of $\Delta V_{out} = 2.368 \pm .005$. The op-amp has therefore, behaved in a perfectly linear fashion and should work fine on the output stage of a CCD filter.

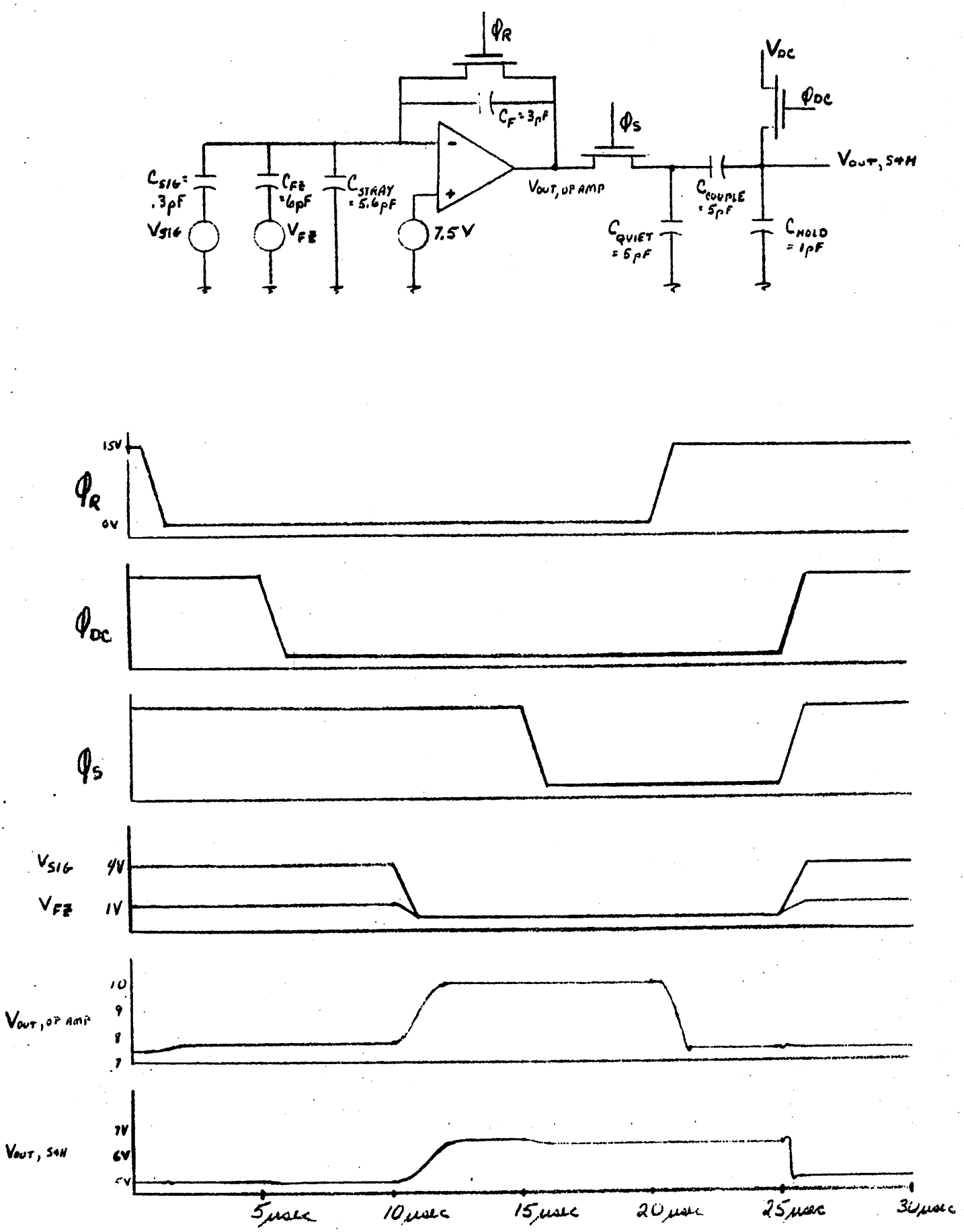


Figure 27. Circuit Transient Response

The major tradeoffs made in this design were in:

1. the choice of the current in the source followers (M_{10} - M_{13}), which had to be high enough to keep them relatively quiet, but low enough to avoid excessive power dissipation,

2. the choice of size for M_{20} - M_{22}, since making these devices larger would have increased their contribution to the noise at the input to the op-amp, but also would have increased the overall gain of the op-amp,

3. choosing the size of M_{24} and M_{25}. This involved four factors, namely, the voltage across M_{24}, the current in the output stage, the size of M_{24}, and the gm of M_{24}. The voltage across M_{24} should not be large since it subtracts directly from the maximum dc voltage which the output can achieve, and the current should be high in order to provide good drive capability to the output. The gm should be high in order to provide low output impedance, but also in order to provide as perfect a buffer as possible for the compensation capacitor. This is important because the op-amp's open loop response has a zero at $\omega = \frac{gm_{24}}{C_{comp}}$. This zero is presently out a 10 MHGHz, but if gm_{24} were reduced (i.e., I_{24} is reduced or V_{GS24} is increased) the zero would move to a lower frequency and could start causing excessive phase shift and a flattening of the gain before the gain has reached unity.

IV. NOISE ANALYSIS

In order to predict the noise at the output of the op-amp, both inputs were connected to 7.5 volts, and a low pass filter consisting of M_{sample} and a 6pf capacitor were placed on the output (since this is equivalent to the load the op-amp will see when operating). Then a 1PA sinusoidal current source was placed across the source and drain of each transistor, and the voltage this produced on the output of the low pass filter was calculated and plotted as the source's frequency was varied from 100Hz to 1GHz. This arrangement is shown in Figure 28, where the noise source for M_8 has been included as an example.

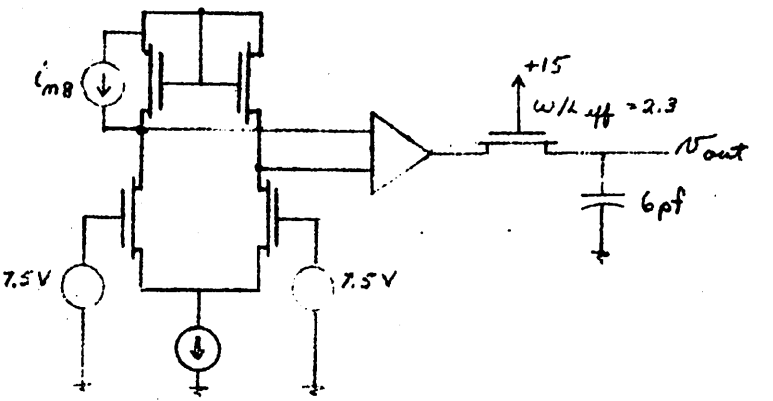


Figure 28. Arrangement for Measuring Each Transistor's Noise Transimpedance

The value of the thermal noise was calculated for each transistor using the expression $i_n^2 = 4kT\ (\frac{2}{3}\ gm)$. This value was then multiplied by the transimpedance of the circuit at several selected frequencies. The total noise at the output of the sample and hold due to thermal noise was calculated by taking the square root of the sum of the square of each term at each frequency. Similarly, for $\frac{1}{f}$ noise, the value of

each noise source was calculated for f = 1Hz, multiplied by its gain at 1Hz, and summed in quadature with the other $\frac{1}{f}$ sources to get the output value at 1Hz. Its value at all other frequencies (up to the frequency where the gain breaks) could then be found by multiplying the value at one hertz by $(\frac{1}{f}.88)^{\frac{1}{2}} = \frac{1}{f}.44$. The details of all these calculations are shown in Appendix A. The total noise found in this way was then divided by the circuit gain to get the equivalent input noise, and the remaining problem was to determine the noise gain from the op-amp input to the output when the feedback loop is closed and the correlated double sampler is operating.

Referring to Figure 29, notice that when the DC reset switch is closed, the output is essentially shorted to a DC voltage, and no signal from the op-amp will appear there. Similarly, when the sampling switch is open, no signal will appear. Therefore, let us look at the signal gain when the DC switch and feedback reset switch are open and the sampler is closed. Then V_n sees a non-inverting amplifier followed by a low pass filter and a divider.

$$v_{out} = v_n \left(\frac{C_F + C_{stray}}{C_F + \frac{C_F + C_{stray}}{A(\omega)}}\right)\left(\frac{1}{1+j\omega \frac{C_{hold}+C_{quiet}}{g_{DS,\,sample}}}\right)\left(\frac{C_{couple}}{C_{couple}+C_{hold}}\right)$$

$$= v_n \left(1 + \frac{C_F + C_{stray}}{C_F}\right)\left(\frac{C_{couple}}{C_{couple} + C_{hold}}\right) \text{ for low frequencies}$$

$$\text{or} \quad = v_n \left(A(\omega)\right)\left(\frac{1}{1+j\omega \frac{C_{hold} + C_{quiet}}{g_{DS,\,sample}}}\right)\left(\frac{C_{couple}}{C_{couple}+C_{hold}}\right) \text{ for high frequencies}$$

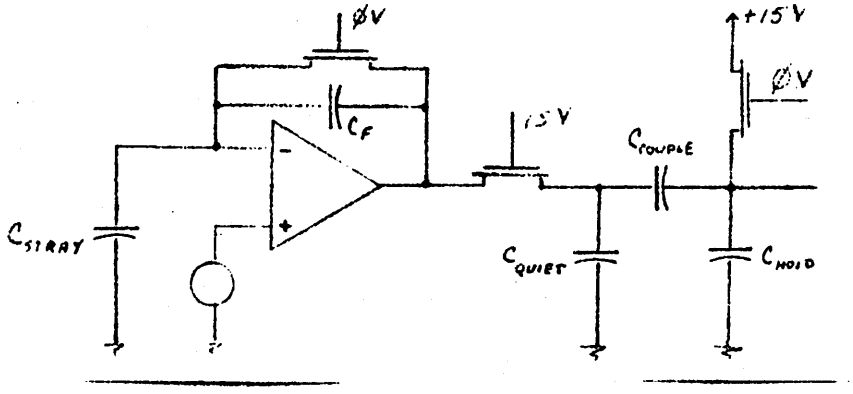


Figure 29. Circuit for Calculating Noise Gain

The break between high and low frequencies occurs where $A(\omega)$, the open loop amplifier gain equals $1 + \frac{C_F + C_{stray}}{C_F}$, the closed loop amplifier gain. The total op-amp noise at the output, through the circuit gain just derived is plotted in Figure 30. This total noise can be broken into three separate components, also plotted in Figure 30. The first component is due to $\frac{1}{f}$ noise and can be modeled as falling at a rate of $\frac{1}{f^{.44}}$ between 0Hz and 600KHz, and as dropping at a rate of $\frac{1}{f}$ from there on. The second component is the thermal noise from those transistors which reach the output of the op-amp through the dominant pole, and which therefore has the shape of white noise, limited by a single pole filter with a break frequency of 600KHz. The last component is the thermal noise generated by those transistors whose noise is not attenuated by the dominant pole of the op-amp (namely, M_{22}, M_{23}, M_{24}, M_{25}, and the transistors in the bias chain). Their summed response is flat out to 10MHz, at which point it is attenuated by the low pass filtering affect of the sample and hold circuit. These components are shown in Figure 30.

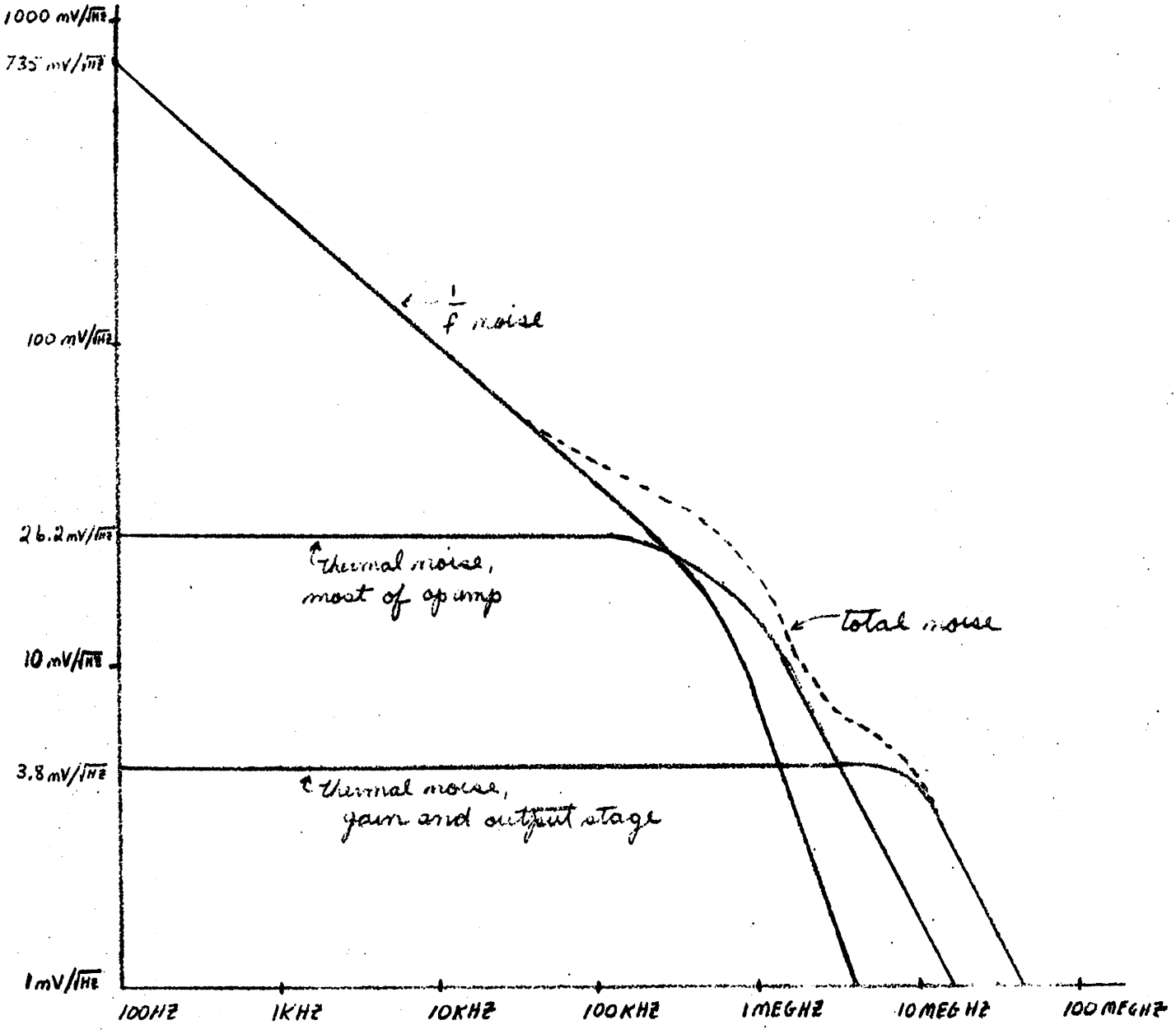


Figure 30. Op-Amp Noise as it Appears at the Output of the Sample and Hold with M_{DC} Open and M_{sample} Closed

The noise circuit can now be reduced to that shown in Figure 31.

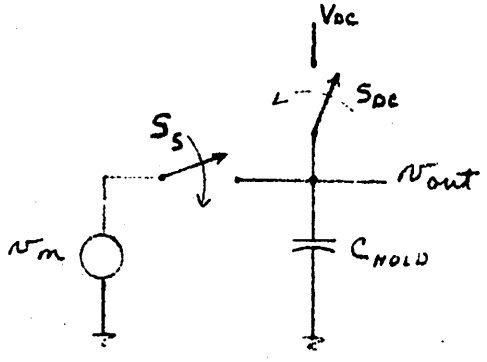


Figure 31

The noise voltage source v_n is composed of the three components discussed above. The remaining question is - what effect do the switches have on the noise into this stage? We will look at this qualitatively first, then derive the result mathematically. Imagine v_n is a white noise source, bandlimited at a very low frequency. Let S_{DC} and S_S be closed, then open S_{DC}. Once S_{DC} is open, the low frequency components of v_n will start charging C_H, but because they are low frequency, they will not have changed the output level very much before S_S is opened and their effect on the output is stopped. When S_{DC} is closed, the charge they added will be removed. But as the bandwidth of the noise gets closer and closer to $\frac{1}{\Delta t}$ (where Δt is the time between when S_{DC} is opened and S_S is opened) more and more of the total signal amplitude gets passed. At very wide bandwidths, very little of the noise will actually be attenuated by the sampler so the sampler will essentially be taking the difference between two points on a random waveform. This will yield an RMS output voltage greater than what it would be without the correlated double sampler. Thus the sampler will

strongly attenuate low frequency noise, but it will magnify high frequency noise. Brodersen and Emmons[7] analyzed the effect of correlated double sampling on bandlimited white noise, and their derivation is repeated here.

The RMS output voltage of the correlated double sampler is the RMS difference between the input voltage, v (t), at two points in time separated by the time interval Δt. This can be calculated by the formula:

$$v_{out}^2 = \lim_{T \to \infty} \frac{1}{T} \int_0^T (v(t)-v(t+\Delta t))^2 \, dt$$

$$= \lim_{T \to \infty} \frac{1}{T} \int_0^T v^2(t) - 2\, v(t)\, v(t+\Delta t) + v^2(t+\Delta t) \, dt$$

$$= \lim_{T \to \infty} \frac{2}{T} \int_0^T v^2(t) - \lim_{T \to \infty} \frac{2}{T} \int_0^T v(t)v(t+\Delta t)dt$$

Notice that the second term is the convolution in time of v (t) with itself, evaluated at time Δt, and the first term is the same thing, evaluated at time zero. Furthermore, a convolution in time can be calculated by taking the inverse Fourier transform of the time function's Fourier transform and the Fourier transform of bandlimited white noise is:

[7] Brodersen and Emmons, "The Measurement of Noise in Buried Channel Charge Coupled Devices", Appendix A.

$$\frac{v_n}{1+\frac{j\omega}{\omega_c}}$$

Thus, $\lim_{T \to \infty} \frac{1}{T} \int_0^T v(\tau)v(\tau+t)\, d\tau$

$$= \frac{1}{2\pi} \int_0^\infty e^{j\omega t} \frac{|v_n|^2}{(1+j\frac{\omega}{\omega_c})(1-j\frac{\omega}{\omega_c})}\, d\omega$$

$$= \frac{1}{2\pi} \int_0^\infty e^{j\omega t} \frac{|v_n|^2}{1+(\frac{\omega}{\omega_c})^2}\, d\omega$$

$$= |v_n|^2 \frac{1}{4RC} e^{-|t|/RC} \text{ where } RC = \frac{1}{\omega_c}$$

Therefore $v_{out}^2 = \frac{2|v_n|^2}{4RC} (e^0 - e^{-\Delta t/RC})$

$$v_{out}^2 = \frac{2|v_n|^2}{4RC} (1 - e^{-\Delta t/RC})$$

Since the effect of the correlated double sampler on bandlimited white noise can be calculated, it would be desirable to approximate $\frac{1}{f}$ noise as a series of bandlimited white noise sources, summed in quaduature. This can be done to a reaonable degree of accuracy by using the series of noise sources listed below.

1) $v(600KHz) \times .82 \times 4^{.44} \times \frac{\sqrt{2}}{1+j\frac{4f}{600KHz}} = v(600K) \frac{2.13}{1+j\frac{f}{150K}}$

2) $v(600KHz) \times .82 \times [16^{.88} - 2.13^2]^{\frac{1}{2}} \times \frac{\sqrt{2}}{1+j\frac{16f}{600K}} = v(600K) \frac{3.05}{1+j\frac{f}{37.5K}}$

3) $v(600K) \times .82 \times [64^{.88} - 3.05^2 - 2.13^2]^{\frac{1}{2}} \times \frac{\sqrt{2}}{1+j\frac{64f}{600K}} = v(600K) \frac{5.80}{1+j\frac{f}{9375}}$

4) $v(600K) \times .82 \times [256^{.88} - 5.80^2 - 3.05^2 - 2.13^2]^{\frac{1}{2}} \times \frac{\sqrt{2}}{1+j\frac{256f}{600K}} = v(600K) \frac{10.64}{1+j\frac{4}{2343}}$

5) $v(600K) \times .82 \times [1024^{.88} - 10.64^2 - 5.80^2 - 3.05^2 - 2.13^2]^{\frac{1}{2}} \times \frac{\sqrt{2}}{1+j\frac{1024f}{600K}} = v(600K) \frac{19.6}{1+j\frac{f}{586}}$

These noise sources and their summed result are shown in Figure 32.

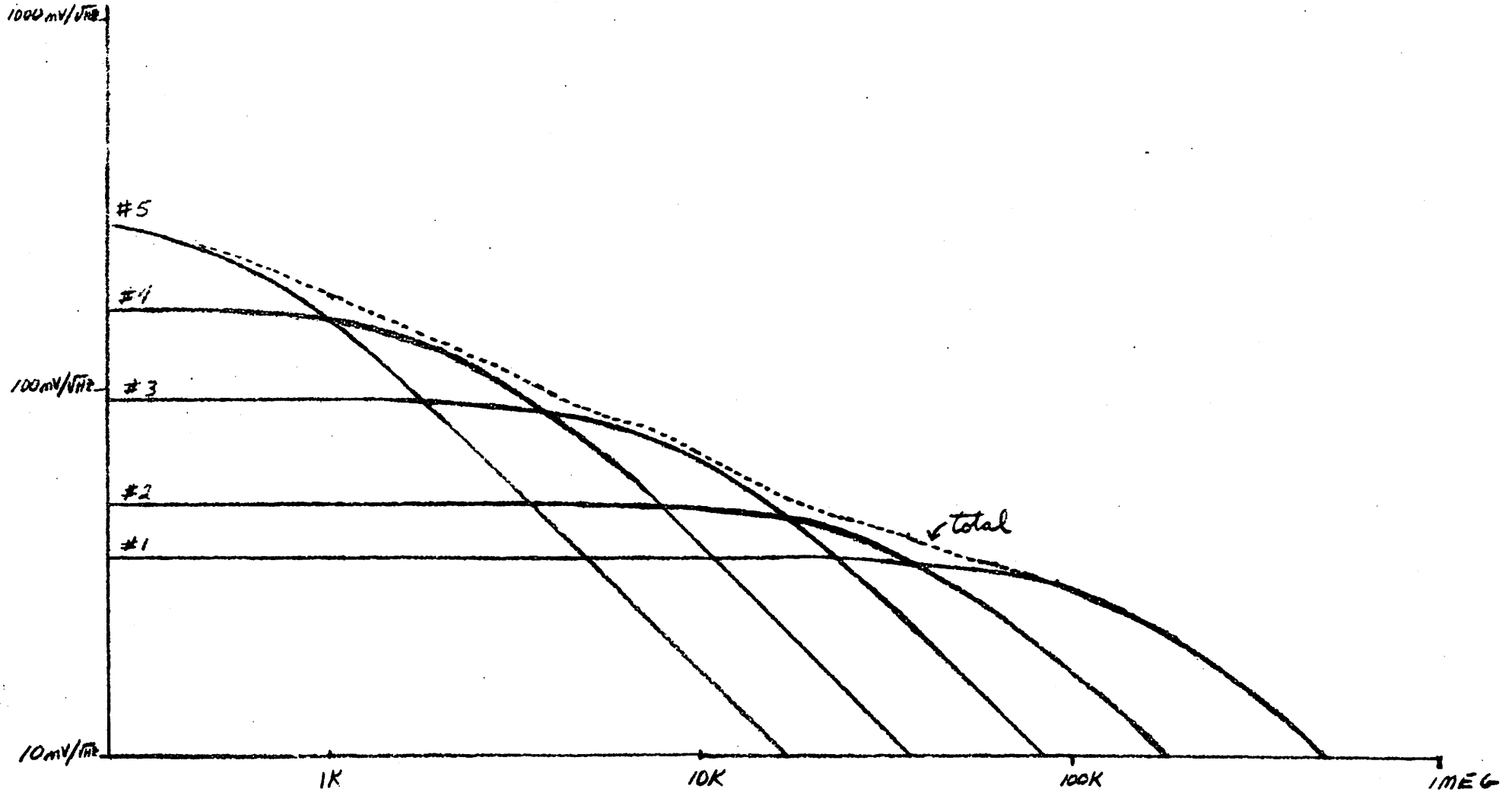


Figure 32. Approximation of $\frac{1}{f}$ Noise as a Series of Bandlimited White Noise Sources

From Figure 27, it can be seen that the output needs 1.3μsec to settle after the DC switch has been released, and 3μsec to settle after the signal has arrived, therefore, the minimum time which can be allowed between the opening of M_{DC} and the opening of M_{sample} is 5μsec. Therefore, the noise at the output due to the op-amp can be calculated:

$$v_n^2 = \frac{(16nV)^2(2.13)^2(2\pi \times 150KHz)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(150KHz)}\right)$$

$$+ \frac{(16nV)^2(3.05)^2(2\pi \times 37.5K)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(37.5K)}\right)$$

$$+ \frac{(16nV)^2(5.80)^2(2\pi \times 9375)}{2}\left(1-e^{-(5x.10^{-6})(2\pi)(9375)}\right)$$

$$+ \frac{(16nV)^2(10.64)^2(2\pi \times 2344)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(2344)}\right)$$

$$+ \frac{(16nV)^2(19.6)^2(2\pi \times 586)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(586)}\right)$$

$$+ \frac{(26.2\times10^{-9})^2(2\pi\times600KHz)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(600KHz)}\right)$$

$$+ \frac{(3.8\times10^{-9})^2(2\pi\times10MEGHz)}{2}\left(1-e^{-(5\times10^{-6})(2\pi)(10MEGHz)}\right)$$

$$= (31\mu V)^2 \text{ due to } \frac{1}{f} \text{ noise}$$

$$+ (36\mu V)^2 \text{ due to thermal noise limited at 600KHz}$$

$$+ (22\mu V)^2 \text{ due to thermal noise limited at 10MEGHz}$$

$$= (52\mu V)^2$$

This 52μV from the op-amp coupled with the 49μV from the CCD and from reseting the capacitors, yields a total RMS voltage noise at the output of the stage of 71μV. When looking at the impulse response of a CCD transversal filter with this output stage, the peak output voltage will equal $V_{in,\,max} \cdot \frac{C_{ox}}{C_F} \quad \frac{C_{couple}}{C_{couple}\,C_{hold}} = 5 \times \frac{.3}{3} \times .8 = .4V$, so the signal to noise ratio on the output of the CCD will be 75db.

V. CONCLUSION

In summary, a CCD output stage has been proposed which uses a pair of op-amps as a charge integrater, followed by coupling capacitors and correlated double samplers. This stage has the advantage of being independent of amplifier offset and of the noise caused by resetting the feedback capacitor. It doesn't cause signal distortion and it severely attenuates low frequency $\frac{1}{f}$ noise from the amplifier. Its disadvantages are that it amplifies high frequency noise by a factor of $\sqrt{2}$, and it is a somewhat complex circuit. The RMS value of the noise at its output is 71μV, and the amount of noise contributed by each component is listed in Table V. The total output signal to noise ratio is 75db.

Table V

Source	Cause	Value at Output
CCD	Surface States	32μV
M_{sample}	Thermal	26μV
M_{DC}	Thermal	26μV
Op-Amp	$\frac{1}{f}$	31μV
Op-Amp	Thermal, 600KHz	36μV
Op-Amp	Thermal, 10MEGHz	22μV
	Total	71μV

APPENDIX A - NOISE CALCULATIONS

Tables VII and VIII show the detailed noise calculations for Tsividis's op-amp, and the low noise op-amp, respectively. Column one shows the transistor which is generating the noise. Column two gives the RMS value of the thermal current noise for that transistor. Columns three through eleven give the value of each noise source, multiplied by the transimpedance from the source to the output of the low pass filter. The next columns show the $\frac{1}{f}$ noise of each transistor at 1Hz, and its value at the output of the circuit.

The row below the last transistor shows the sum of all the components at each frequency. The row titled "input referred" gives the value of the noise, divided by the gain of the op-amp. The last row gives the value of the noise at the output of the sample and hold. It assumes $C_{stray} = 6pf + C_{in}$ (the input capacitance of the op-amp), $C_F = 3pf$, and $\frac{C_{couple}}{C_{couple} + C_{hold}} = .8$.

The thermal noise out of the circuit which is caused by Tsividis's op-amp (not including the effects of the correlated double sampler) is 126μV. The $\frac{1}{f}$ noise contributes 560μV. When the sampler is added, the entire noise equals $\sqrt{2} \times 126\mu V = 180\mu V$.

The total thermal noise out of the circuit caused by the low noise amplifier is 32μV and the $\frac{1}{f}$ noise out is 230μV. When the correlated double sampler is included, the total noise out is 52μV.

Table VII. Noise in Tsividis's Op-Amp

	pA/$\sqrt{HZ}$	100	1K	10K	100K	1MEG	3MEG	10MEG	30MEG	100MEG	$\frac{1}{f}$@1Hz	μV_{out}
M1	1.26	3nV	3nV	3nV	.8nV	.09nV	.04nV	.02nV	.003nV	0nV	203	1
M2	.416	10	10	10	2.6	.27	.08	.01	.001	0	130	3
M3	1.25	35	35	32	8.7	.89	.26	.06	.005	0	203	6
M4	.685	553	553	516	138.5	14.69	5.38	1.40	.24	.001	386	312
M5	2.10	1696	1695	1582	424.6	45.02	16.49	4.29	.379	.003	600	485
M6, M9	1.30	515	515	481	129.0	13.57	4.66	.90	.058	0	203	80
M7, M10	3.14	1336	1335	1246	334.1	35.14	11.97	2.28	.165	.001	146	62
M8	1.29	37	37	35	9.4	.97	.29	.08	.015		212	6
M11	.687	624	624	582	156.1	16.55	6.06	1.59	.161	.002	386	350
M12	2.12	1925	1923	1795	481.7	51.07	18.70	4.91	.497	.007	600	545
M13	3.03	0	1	7	18.1	18.52	16.82	6.35	.683	.010	582	0
M14	2.38	0	1	5	14.2	14.55	13.21	4.99	.536	.008	582	0
M15	.498	6	6	6	1.7	.78	.70	.27	.037	.001	196	4
M16	1.64	2	2	2	.7	.43	.60	.60	.200	.009	540	2
M17	1.64	16	16	14	4.1	2.18	2.25	1.74	.616	.010	540	10
M18	.979	55	55	51	15.4	7.16	6.41	2.49	.339	.009	212	12
M19	2.68	3	3	3	1.0	.65	.90	.90	.299	.013	168	0
M20	3.21	177	176	165	49.3	22.77	7.77	7.77	.924	.017	168	9
M21	3.77	17	17	17	17.5	17.30	5.82	5.82	.661	.041	629	3
M22	2.97	14	14	14	13.8	13.63	4.59	4.59	.520	.033	629	3
M23	1.14	8	8	8	7.5	7.44	2.51	2.51	.288	.027	620	4
M24	3.40	22	22	22	22.4	22.20	7.49	7.49	.859	.081	514	4
M26	1.22	2	2	2	1.9	1.90	1.46	1.56	.493	.096	701	0
M26	2.64	4	4	4	4.0	4.11	3.38	3.38	1.068	.208	297	0
Total Out		3060	3058	2854	767.2	93.43	51.43	17.90	2.368	.252		873
Input Referred		15.48	15.48	15.48	15.51	17.84						4.416
Out thru Gain		41.1	41.1	41.1	41.2	39.4	36.8	14.2	1.89	.202		11.73

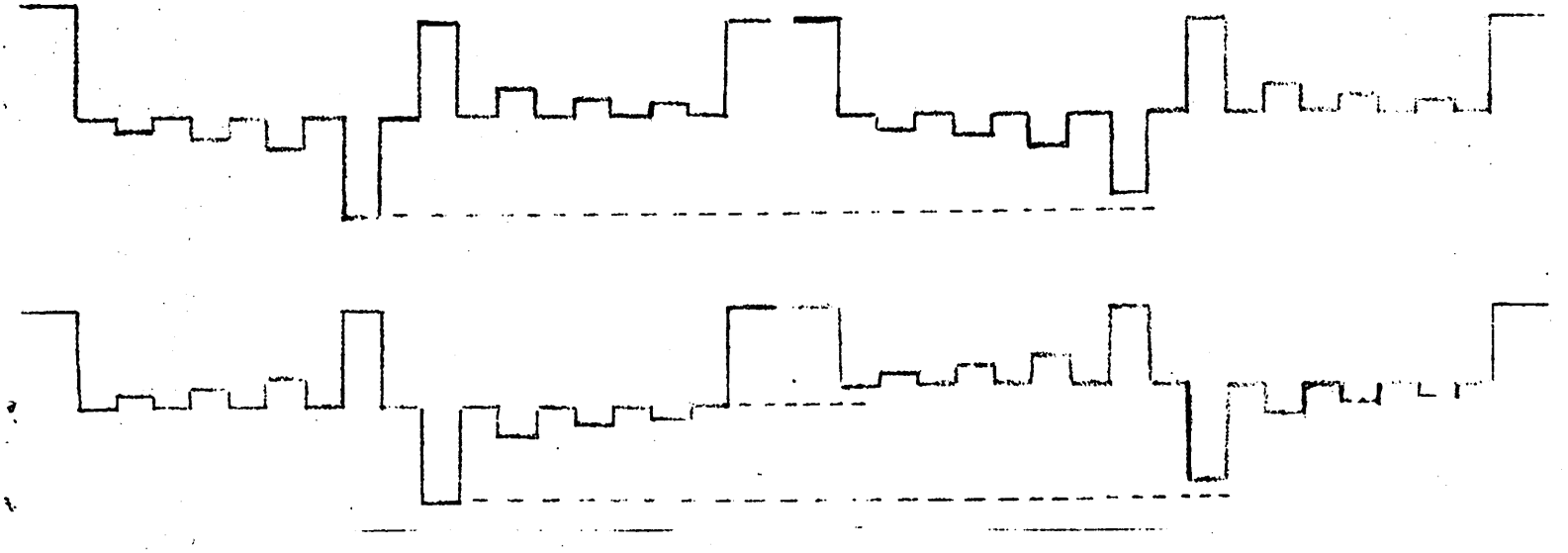
Table VIII. Noise in Low Noise Op-Amp

	$pA/\sqrt{Hz}$	100	1K	10K	100K	1MEG	3MEG	10MEG	30MEG	100MEG	$\frac{1}{f}$@1Hz	μV_{out}
M1	1.78	13nV	13nV	6nV	.7nV	.19nV	.35nV	.51nV	.194nV	.014nV	492nV	3
M2	2.47	1	1	1	.1	.02	.04	.06	.038	.007	593	0
M3	2.47	1	1	1	.1	.02	.04	.06	.029	.003	593	0
M26	.79	4	4	2	.2	.06	.11	.16	.057	.003	223	0
M27	1.81	2	2	1	.1	.03	.05	.07	.032	.003	492	0
M4	1.81	18	18	9	1.0	.20	.21	.21	.088	.011	493	5
M5	1.89	0	0	0	0	.01	.02	.05	.018	.001	527	0
M6,7	4.92	1695	1668	820	93.6	9.74	3.51	.98	.095	0	269	95
M8,9	1.85	637	627	308	35.2	3.66	1.31	.34	.021	0	697	240
M10,11	1.39	952	937	461	52.6	5.48	2.03	.64	.058	0	594	400
M12,13	3.16	2164	2130	1047	119.5	12.47	4.62	1.46	.131	.001	741	509
M14,15	2.62	595	567	289	32.9	3.43	1.29	.51	.176	.025	805	182
M16	.62	134	132	65	7.4	.78	.29	.10	.020	.002	304	66
M17	.62	147	145	71	8.1	.85	.34	.18	.072	.011	304	72
M18	.38	298	293	144	16.4	1.64	.52	.15	.025	.002	97	76
M19	.38	321	316	155	17.7	1.78	.58	.23	.078	.012	97	82
M20	1.44	1128	1110	546	62.3	6.23	1.95	.58	.094	.008	113	89
M21	1.44	1217	1197	589	67.2	6.75	2.22	.88	.296	.045	113	96
M22	2.46	56	55	27	5.6	4.67	4.56	3.63	.884	.070	137	3
M23	.636	14	14	7	1.4	1.21	1.18	.94	.229	.018	310	7
M24	4.72	2	2	1	.3	.31	.58	1.33	.952	.163	355	0
M25	2.66	1	1	1	.2	.18	.33	.75	.536	.092	571	0
Total Out		3494	3436	1691	193.0	20.51	8.57	4.67	1.500	.209		748
600KHz part		3494	3436	1691	193.0	19.93	7.13	2.33	.472	.057		748
10MEGHz part						4.84	4.76	4.05	1.424	.201		
input referred		9.28	9.28	9.28	9.27							1.99μV
total out thru gain		26.2	26.2	26.2	25.8	14.1	6.72	3.73	1.200	.167		5.61μV

APPENDIX B - STRANGE OCCURRENCES IN THE DISCRETE PROTOTYPE OF THE OUTPUT STAGE

The discrete prototype of the output stage behaved basically as expected, with three exceptions. The most obvious problem was that the signal was very noisy, and that is discussed in the main body of the text. The other two problems involved an apparent signal distortion, and an uncertainty in the signal gain.

The CCD which was used in this prototype performed the function of a Hilbert transform, which has an impulse response of $\frac{1}{t}$. Therefore the signals out of the CCD and output stage should have looked like those in Figure 33a. Instead, they looked like those in Figure 33b, except that the effect has been exaggerated to make it more obvious.



a) Expected b) Actual

Figure 33. Expected and Actual Output From Hilbert Transform CCD

Notice that the DC level out doesn't sit midway between the peaks, as it should. Also notice that in the second half of the CCD, the ratio of the highest peak to the rest of the peaks in its half is correct, but in the first half, the highest peak is too small, although all the other peaks appear to be correct. This waveform could be explained if the CCD channel was narrower than expected, and the mask had been aligned against one edge of it, as shown in Figure 34.

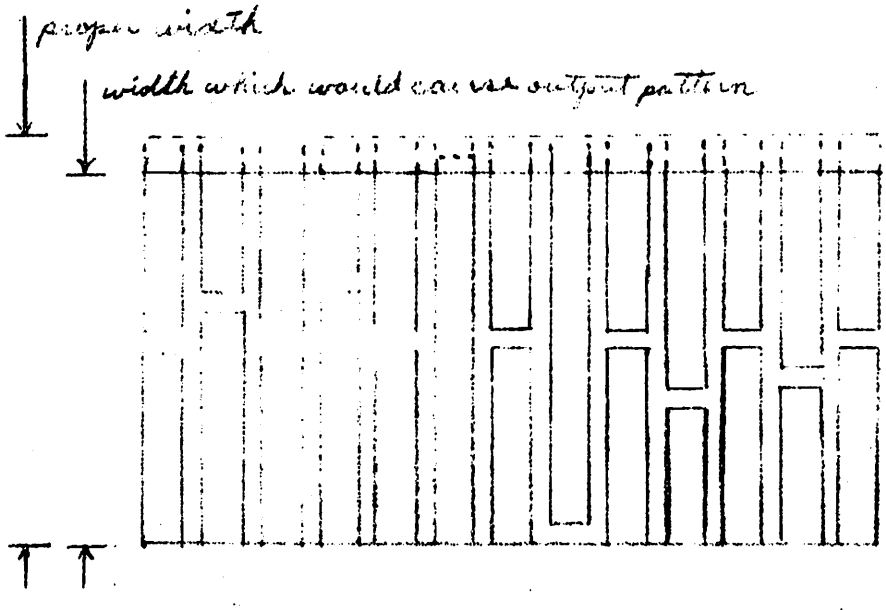


Figure 34. Mask Which Could Cause Output Waveform

Unfortunately, a microscopic examination of the CCD did not support this theory - the center of the tap weights appeared to be in the center of the channel, so we have no defendable explanation for the problem.

The other problem was even stranger. The gain of the circuit seemed to vary from day to day and was never as large as expected. To investigate this further, the peak to peak output voltage was measured as the value of the feedback capacitor was varied, the value of the input voltage was varied, and the day during which the measurements were taken was varied. The output voltage was then compared with the expected output voltage. The results are shown in Table IX. The closest thing to a conclusion that can be drawn from this data is that the long term gain variations seem much more pronounced than the short term ones. The proportion of the expected charge that is actually flowing onto C_F does not seem to depend on the input voltage, and probably does not depend on the value of C_F. In another experiment, the clock rate was slowed by a factor of 10, but the gain did not improve, so the problem does not seem to be caused by insufficient charging time. Cooling the circuit caused too many side effects to measure the effect on gain. So although we have some idea of what the cause is not, we still do not know what the cause is. We can only hope that it is a function of being a discrete prototype and will not appear on the integrated version.

Table IX - Circuit Output Voltage

C_{CCD}	V_{in}	C_f	V_{out}, Expected	V_{out} Day#1	V_{out} Day#2	V_{out} Day#3	$V_{out}/V_{expected}$ Day#1	$V_{out}/V_{expected}$ Day#2	$V_{out}/V_{expected}$ Day#3
.48	3	1	1.17		.440	.580		.38	.50
		1.5	.78	.520			.67		
		3	.39	.330	.177	.250	.85	.45	.64
		4	.29	.210	.111	.148	.72	.38	.51
		5	.23	.140	.077	.091	.61	.33	.40
		6	.19	.110	.066	.073	.58	.35	.38
		7	.17	.092	.060	.064	.54	.35	.38
		8	.15	.085	.055	.058	.57	.37	.39
		10	.12		.045	.045		.38	.38
		15	.078		.032	.030		.41	.38
.16	3	1.5	.26	.175			.67		
		3	.13	.115			.88		
		4	.10	.080			.80		
		5	.078	.050			.64		
		6	.065	.040			.62		
		7	.065	.035			.63		
		8	.049	.032			.65		
.48	1	1	.39		.190	.300		.49	.77
		3	.13		.050	.070		.26	.54
		4	.10		.030	.025		.30	.25
		6	.065		.015	.010		.23	.23
Average:							.67	.36	.44

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