NMOS PHASE LOCK LOOP

by

H. Khorramabadi

Memorandum No. UCB/ERL M77/67

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1.1 Introduction

Phase-lock loops are a class of circuits with many applications in communication systems. However, the complexity of the circuitry makes the P.L.L. Technique uneconomical and impractical until recent years.

The development of single-chip bipolar phase-locked loops made them more attractive for industrial and consumer instruments. Now-adays P.L.L.s are used for many applications such as F.M. and stereo demodulators, tone decoders, frequency-synthesizers and others.

The next step is the implementation of P.L.L. in M.O.S. technology, where the higher density and lower power consumption makes it superior to the bipolar.

2.1 The Phase Locked Loop Principle

The phase locked loop is a feedback system made up of a phase comparator, a low pass filter, an error amplifier and a voltage-controlled oscillator. Fig. 2.1 shows the block-diagram of a phase-locked loop. The VCO is an oscillator whose frequency is controlled by an external voltage. When an input signal is applied to the system the phase comparator compares the phase and frequency of the incoming signal with the VCO frequency and generates an error voltage proportional to the phase difference between the two signals. This voltage is then filtered, amplified and applied to the control input of the VCO. The control voltage forces the VCO frequency to vary in a direction that reduces the frequency difference between the two signals. The range of frequencies over which the loop

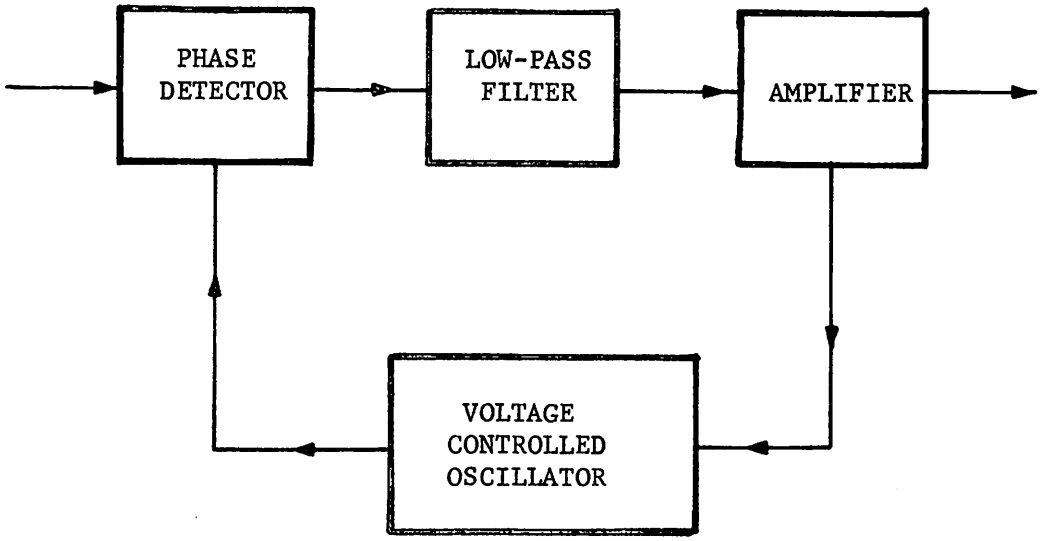

Fig 2.1 Block-diagram of a Phase-locked loop

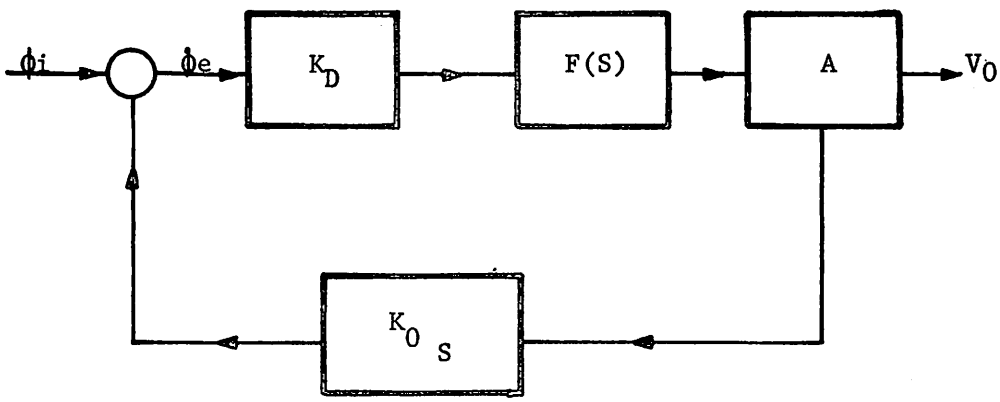

Fig 2.2 Block-diagram of PLL system

can maintain lock is called the "Lock Range". The "Capture Range" is the band of frequencies over which the loop can acquire lock from an unlocked condition.

The circuit can be treated as a linear feedback system while in lock. Figure 2.2 gives a block-diagram of the system in this mode. The closed-loop transfer function is:

$$\frac{V_o}{\phi_i} = \frac{SK_D F(s)A}{S + K_D K_o F(s)A} \tag{2.1}$$

we are interested in the response of the loop to frequency

$$\omega_i = S\phi_i$$

$$\frac{V_o}{\omega_i} = \frac{K_D F(s)A}{S + K_D K_o F(s)A} \tag{2.2}$$

$$K_v = K_o K_D A \tag{2.3}$$

$$\frac{V_o}{\omega_i} = \frac{1}{K_o} \frac{K_v F(s)}{S + K_v F(s)} \tag{2.4}$$

we will first consider the simplest case which the loop filter is removed (F(s) = 1).

$$\frac{V_o}{\omega_i} = \frac{1}{K_o} \frac{K_v}{S + K_v} \tag{2.5}$$

Fig. 2.3 shows the frequency response and the root locus of this first-order low pass transfer function. The loop bandwidth is equal to K_v. Since there is no low pass filter in the loop, undesirable sum frequency

components and out of band signals are transfered to the output. By adding a single pole low-pass filter:

$$F(s) = \frac{1}{1 + \frac{s}{\omega_1}} \tag{2.6}$$

the PLL becomes a second order system with root locus shown in Fig. 2.4. The transfer function becomes:

$$\frac{V_o}{\omega_i}(s) = \frac{1}{K_o}\left[\frac{1}{1 + \frac{s}{K_v} + \frac{s^2}{\omega_1 K_v}}\right] \tag{2.7}$$

the damping factor is

$$\xi = 1/2\sqrt{\omega_1/K_v} \tag{2.8}$$

$$\omega_{-3dB} = \sqrt{K_v \omega_1} \tag{2.9}$$

There is a peaking in the frequency response. Lowering ω_1 for narrow bandwidths increases the peaking which can cause the loop to ring. A good alternative is to place the poles on radials angled 45° from the real axis, which gives a damping factor of $1/\sqrt{2}$ and a maximally flat low-pass pole configuration:

$$\omega_1 = 2K_v \tag{2.10}$$

$$\omega_{-3dB} = \sqrt{2}\, K_v \tag{2.11}$$

In order to have narrow bandwidth without unacceptable peaking a zero must be added to the loop filter as shown in Fig. 2.5. The loop-filter pole can now be made small without causing instability.

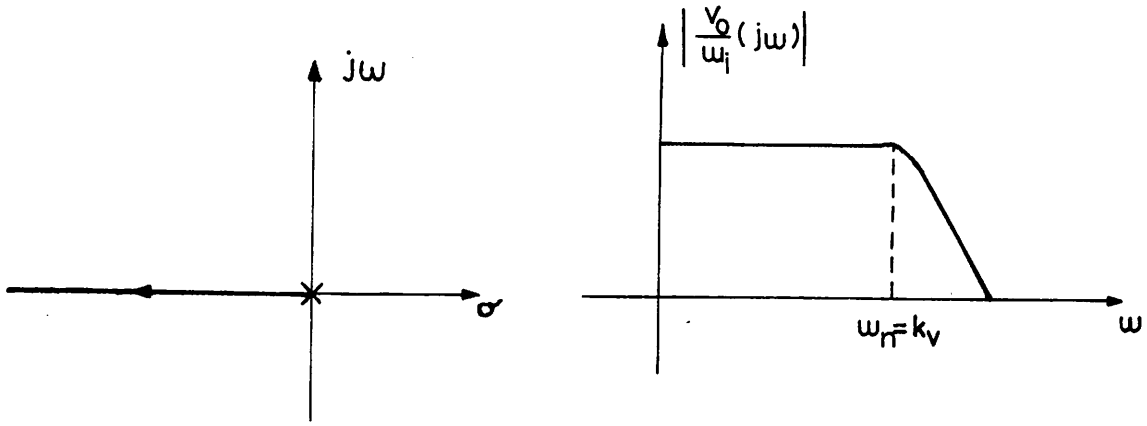

Fig 2.3 Root-locus and frequency response of first order loop

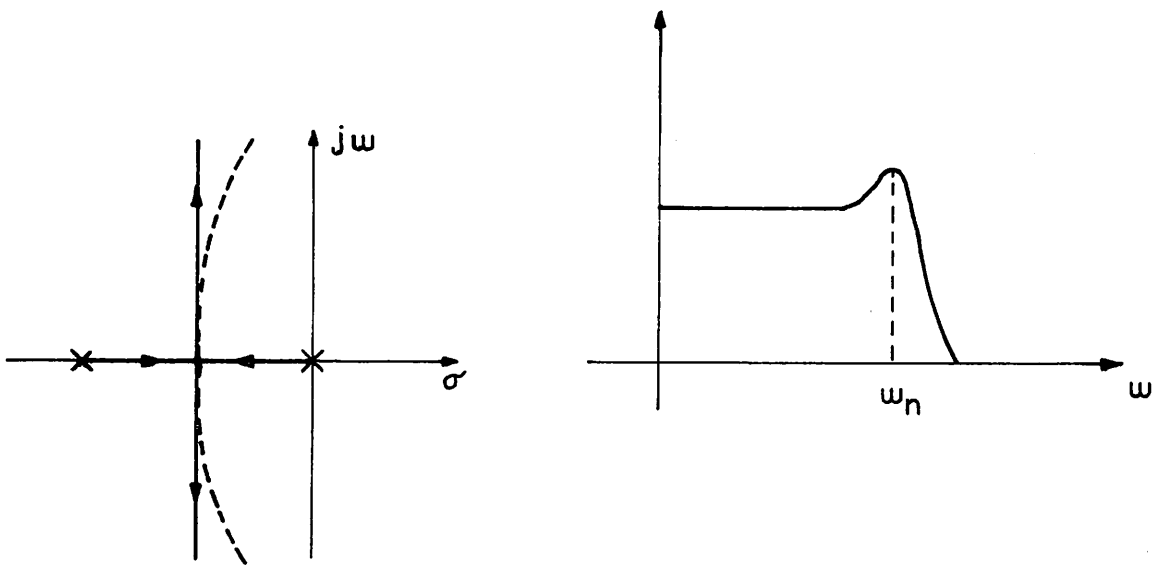

Fig 2.4 Root-locus and frequency response of second order loop

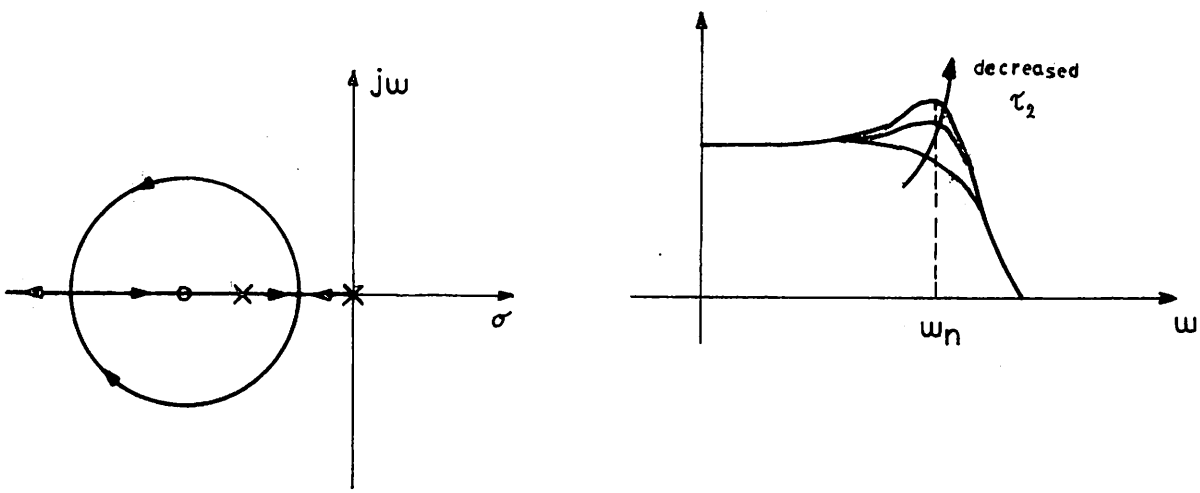

Fig 2.5 Root locus and frequency response of second order loop with a zero.

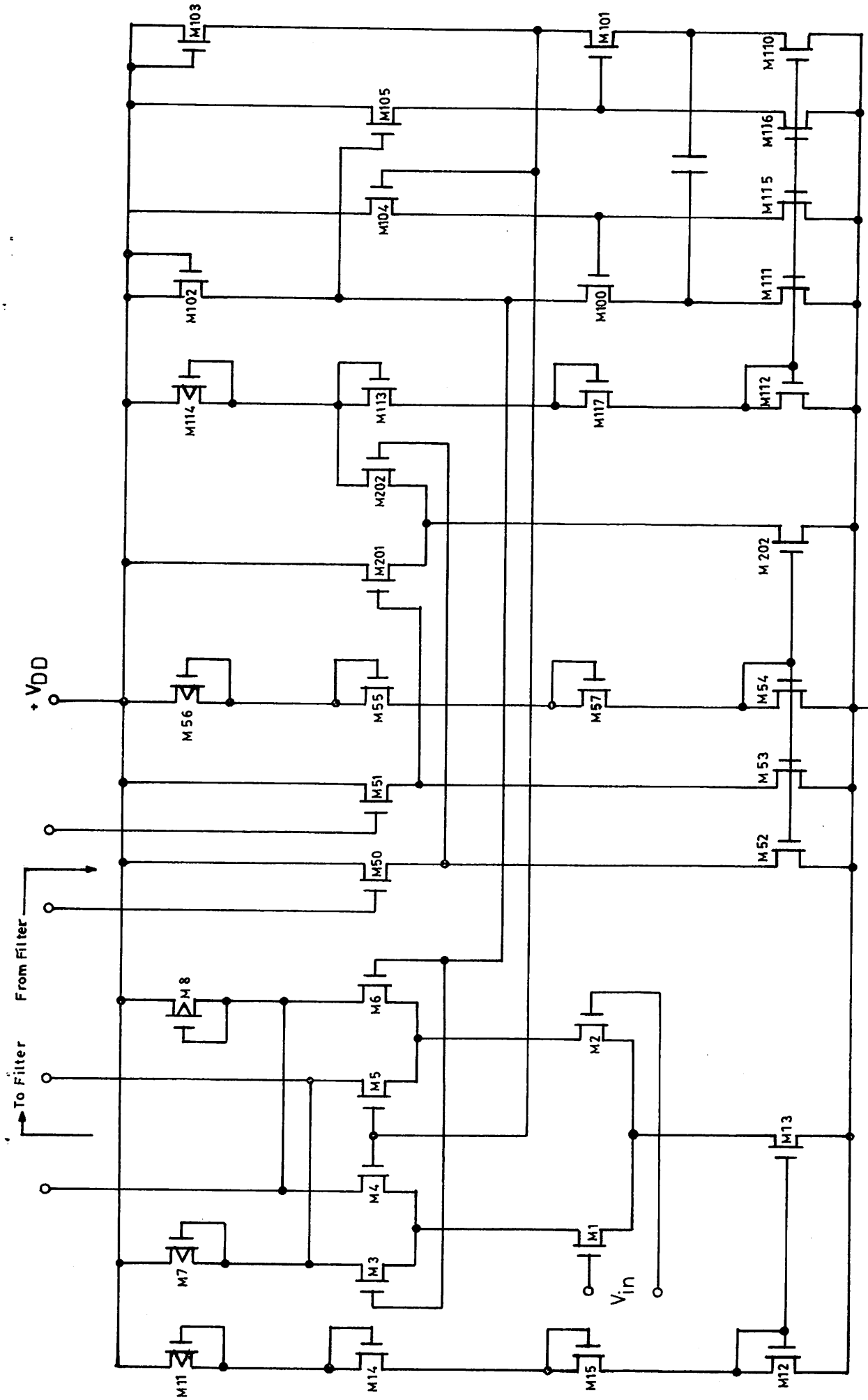

FIG 3.1 SCHEMATIC OF NMOS PHASE-LOCKED LOOP

Chart of W/L of Circuit Transistors:

	W(micron)	L(micron)
M1	200	10
M2	200	10
M3	10	10
M4	10	10
M5	10	10
M6	10	10
M7	5	30
M8	5	30
M11	5	30
M12	10	10
M13	10	10
M14	5	20
M15	5	10
M50	10	10
M51	10	10
M52	15	10
M53	15	10
M54	20	10
M55	5	10
M56	5	15
M57	10	10
M100	82	10
M101	82	10
M102	5	35

M103	5	35
M104	5	18
M105	5	18
M110	10	10
M11	10	10
M12	10	10
M113	5	20
M14	5	15
M15	20	10
M16	20	10
M17	5	10
M201	30	10
M202	30	10
M203	20	10

3. Circuit Description

Fig. 3.1 is the schematic of the proposed circuitry. The circuit is made of 38 transistors. M_1.....M_8 form the phase detector with depletion loads. M50 and M51 are the level-shifting transistors. Voltage to current conversion is done by M201, M202. The VCO is made by M100....M116. All the other transistors form the circuit current sources. Each part is described separately then the whole circuit is analysed.

3.1 Phase Detector

The phase detector is of four quadrant Gilbert multiplier type. This circuit has three types of application according to the magnitude of v_1 and v_2.

(a) v_2 and v_1 small - the circuit behaves as a multiplier.

(b) v_2 large, v_1 small - v_1 is multiplied by a square-wave and the circuit acts as a modulator

(c) v_2 large, v_1 large - the circuit works as a phase-dector.

Our case is the third one where v_2 is the VCO square-wave output and v_1 is the signal the phase lock loop has to lock to.

v_1 is a sine wave. Lets first assume that the transconductance of the input differential pair is high enough so that this stage will be switched on and off at the zero crossings of the input signal. Fig. 3.3 shows the output signal, when v_1 and v_2 are of identical frequencies and phase difference ϕ. M_3.....M_6 are switched on and off by the VCO square wave which has the effect of multipling the output of M_1 and M_2 by +1 for half of VCO signal cycle and by -1 for the other half. The output waveform consists of a dc component and a component at twice the incoming frequency.

The dc component is:

$$V_{average} = \frac{1}{2\pi}\int_o^{2\pi} V_o(t)d(\omega_o t) \tag{3.1}$$

$$= -\frac{1}{\pi}(A_1 - A_2)$$

$$V_{ave} = I_{SS} R_L^* (\frac{2\phi}{\pi} - 1) \tag{3.2}$$

Fig. (3.5) shows the dc component of the output versus ϕ. Fig. 3.4 shows the output for v_1 small. In order to calculate the output lets apply a sin-wave to v_1 and a square wave to v_2 terminals.

$$v_1 = V_1 Sin(\omega_i t + \phi_i) \tag{3.3}$$

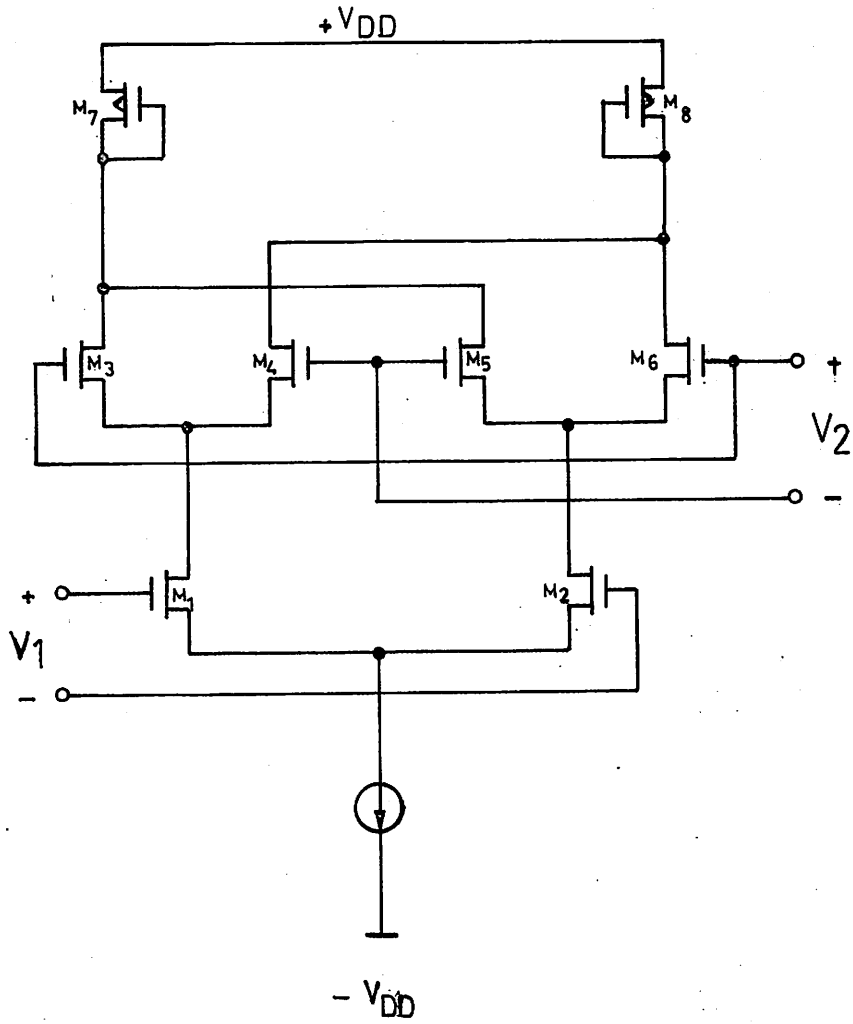

Fig 3.2 MOS Phase Detector

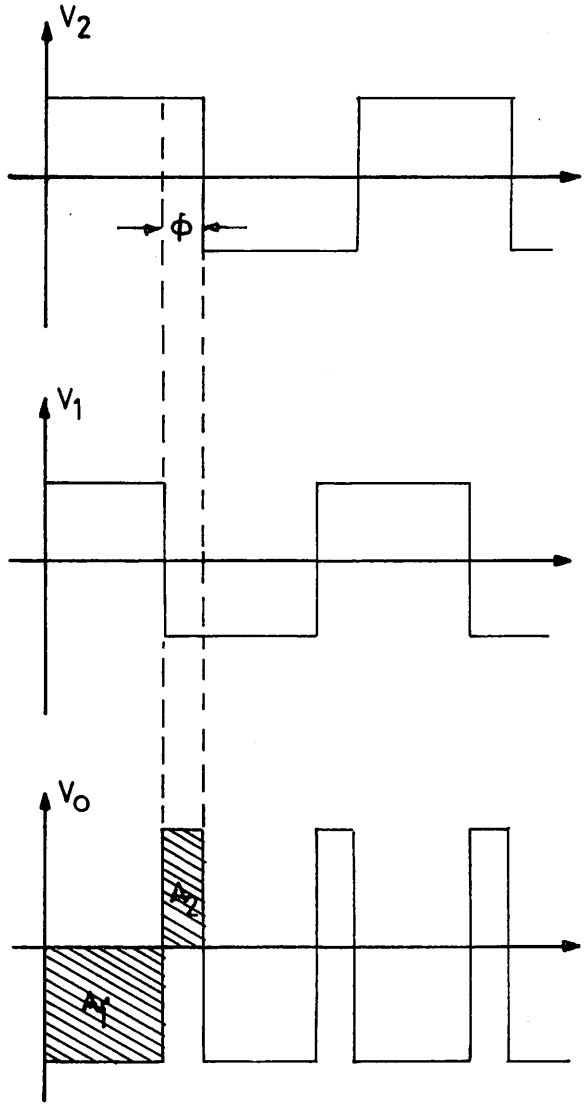

Fig 3.3

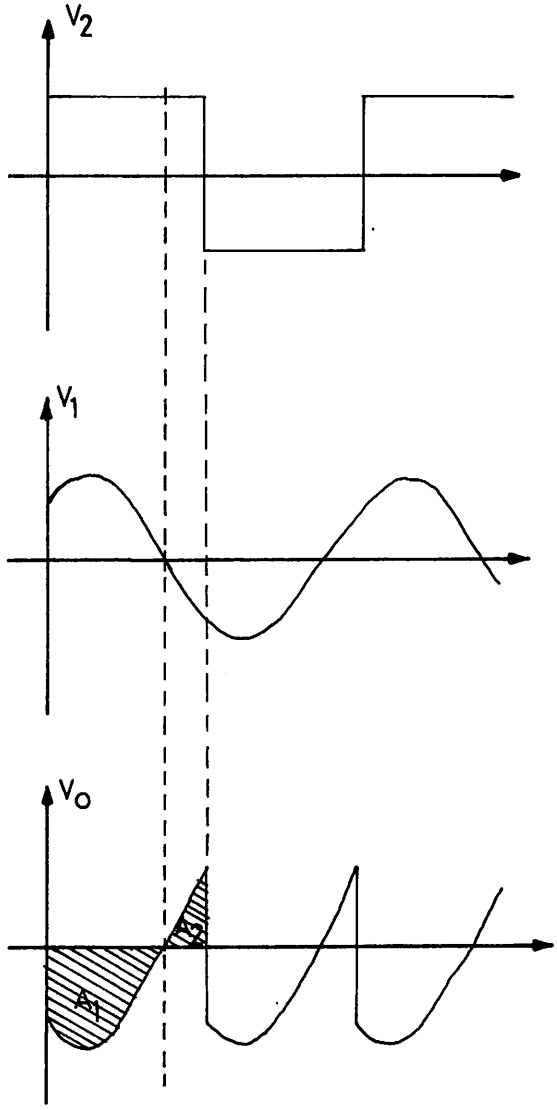

Fig 3.4

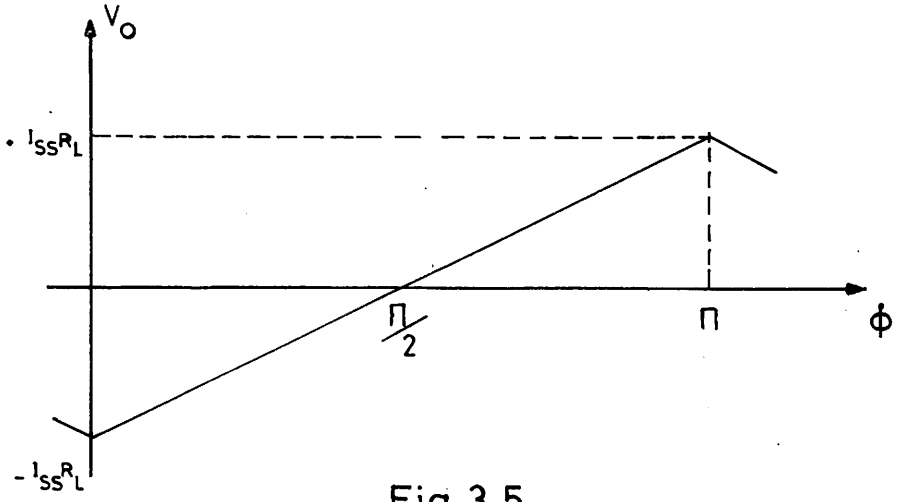

Fig 3.5

$$V_2 = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \text{Sin}[(2n+1)\omega_o t] \tag{3.9}$$

$$V_o = \frac{2Ad}{\pi} \sum_{n=0}^{\infty} \frac{V_1}{2n+1} \text{Cos}[(n+1)\omega_o t - \omega_i t - \phi_i] - \sum_{n=0}^{\infty} \frac{V_1}{2n+1} \text{Cos}[(2n+1)\omega_o t + \omega_i t + \phi_i] \tag{3.5}$$

When the phase lock loop is in lock $\omega_o = \omega_i$ and the first term (n=0) becomes:

$$\frac{2Ad}{\pi} v_1 \text{ Cos } \phi_i \tag{3.6}$$

$$Ad = g_m R_L = \sqrt{2I_{SS} K_1}\, R_L \tag{3.7}$$

$$V_o = \frac{2\sqrt{2I_{SS} K_1}}{\pi} R_L V_1 \text{ Cos } \phi_i \tag{3.8}$$

So for small v_1 the output voltage depends not only on phase difference but on the input signal amplitude too. The circuit still acts as phase detector but with a smaller K_V which reduces the lock and capture range of the PLL.

In the previous formulas the load devices were assumed to be simple resistors. The actual load devices are depletion MOSFET ($V_T < 0$) which makes the calculations more complicated. Fig. 3.6 shows the I-V curve of a depletion MOSFET whose gate is connected to its drain. The drain current is given by:

$$I_D = K[2(-V_T)V_{DS} - V_{DS}^2]\ [1 + \lambda V_{DS}] \quad \text{for } V_{DS} \leq -V_T \tag{3.9}$$

$$I_D = K[-V_T]^2\ [1 + \lambda V_{DS}] \quad \text{for } V_{DS} \geq -V_T \tag{3.10}$$

$$V_T = V_{TO} + \gamma(\sqrt{V_{BB} + V_S + \phi} - \sqrt{\phi}) \tag{3.11}$$

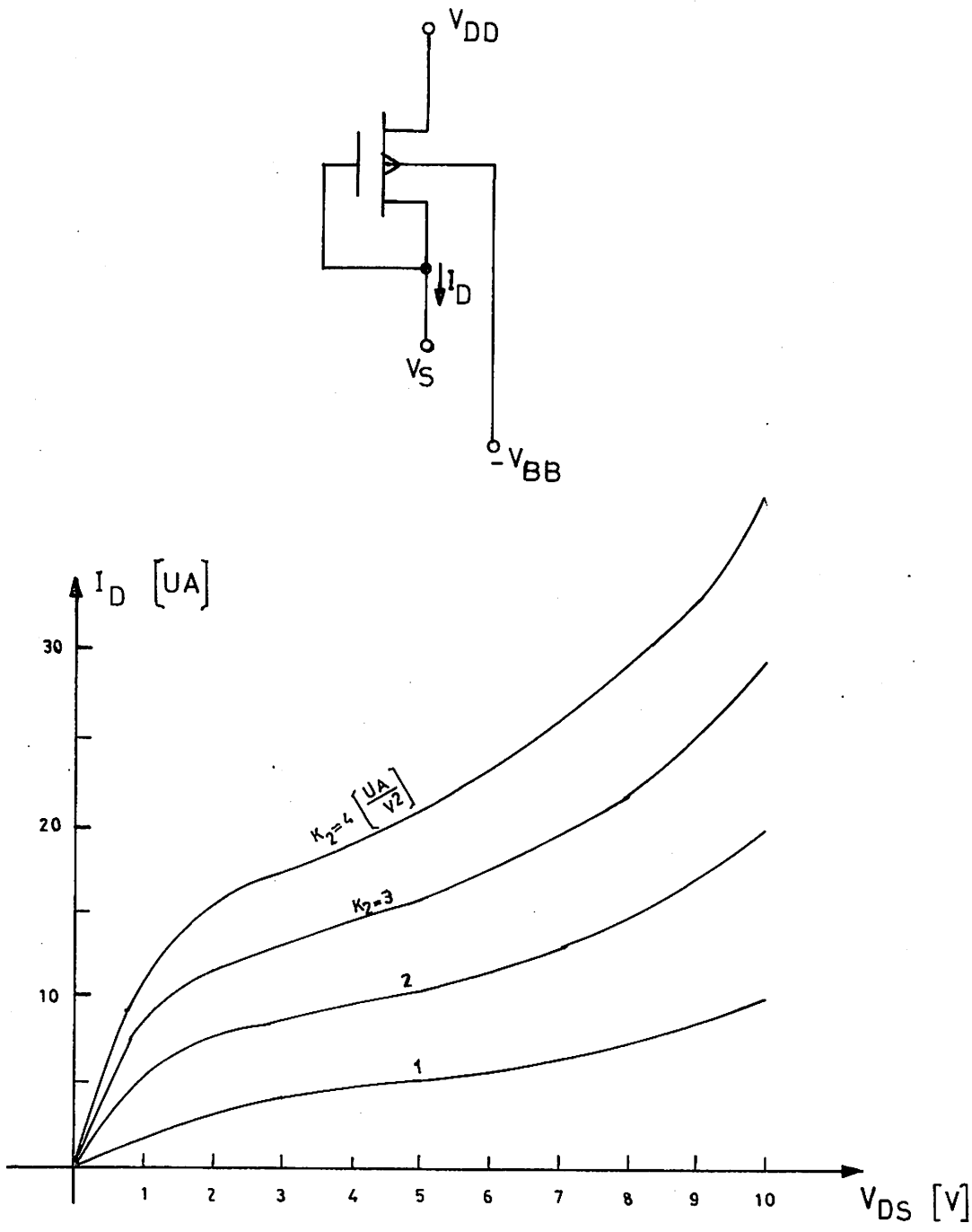
V_{DD}
I_D
V_S
$-V_{BB}$
I_D [UA]
30
20
10
$K_2=4\left[\frac{UA}{V2}\right]$
$K_2=3$
2
1
1
2
3
4
5
6
7
8
9
10
V_{DS} [V]

Fig 3.6

For v_1 small:

$$Ad = g_m R_o \tag{3.12}$$

in order to have a high gain the depletion loads should be biased at $V_{DS} \tilde{=} V_T$

$$\frac{1}{R_o} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial}{\partial V_{DS}} \left[K(-V_T)^2(1 + \lambda V_{DS})\right] \tag{3.14}$$

$$\frac{1}{R_o} = \frac{I_D \lambda}{1 + \lambda V_{DS}} + \frac{\gamma_2}{\sqrt{\phi + V_{BB} + V_S}} \sqrt{KI_D (1 + \lambda V_{DS})} \tag{3.15}$$

normally $\lambda V_{DS} << 1$ so:

$$R_o = \frac{1}{\gamma_2} \sqrt{\frac{\phi + V_{BB} + V_S}{KI_D}} \tag{3.16}$$

$$Ad = 2 \sqrt{I_{D_1} K_1} \frac{1}{\gamma_2} \sqrt{\frac{\phi_2 + V_{BB} + V_{out}}{K_2 I_{D_2}}}$$

$$= \frac{2}{\gamma_2} \sqrt{\frac{\left(\frac{w}{\ell}\right)_1}{\left(\frac{w}{\ell}\right)_2} (\phi_2 + V_{BB} + V_{out})} \tag{3.17}$$

$$K_D = \frac{4}{\pi \gamma_2} \sqrt{\frac{\left(\frac{w}{\ell}\right)_1}{\left(\frac{w}{\ell}\right)_2} (\phi_2 + V_{BB} + V_{out}) \quad V_1} \tag{3.18}$$

for V_1 large:

$$V_o = 2\left(V_{DS}\Big|_{I=I_{SS}}\right) \tag{3.19}$$

$$K_D = \frac{4}{\pi}\left(V_{DS}\Big|_{I=I_{SS}}\right) \tag{3.20}$$

V_{DS} can either be found from the curve or can be found from the curve or can be calculated from:

$$I_{SS} = K_2\,[-V_{TO} - \gamma\sqrt{V_{BB} + V_{DD} - V_{DS} + \phi} + \gamma\sqrt{\phi}\,]^2\,(1 + \lambda V_{DS}) \text{ for } V_{DS} \geq -V_T$$

or if working in linear region:

$$I_{SS} = K_2[2(-V_{TO} - \gamma\sqrt{V_{BB} + V_{DD} - V_{DS} + \phi} + \gamma\sqrt{\phi})V_{DS} - V_{DS}^2](1 + \lambda V_{DS})$$

$$\text{for } V_{DS} \leq -V_T$$

K_D is an important factor in the capture and lock range of the P.L.L. These two can be adjusted by adjusting K_D. Inspecting the I-V curve of the load, K_D can be adjusted by either changing K_2 or changing I_{SS}.

3.2 Voltage Controlled Oscillator

The VCO is a source-coupled multivibrator in which the charging current in the capacitor is varied in response to the control input. M102, M103 function as non-linear resistors. M104 and M105 level-shift the source voltage of M102, M103 in order to keep M100, M101 in saturation region. Lets first assume that there is no body-effect (each transistor body is connected to its source). With M101 turned off and M100 on, M102 carries $2I_1$ and has a voltage drop of $\frac{2I_1}{K_3} + V_T$ across it. M103 is off and its source voltage is $V_{DD}-V_T$. In Fig. 3.7

$$V106 = V_{DD} - 2V_T - \sqrt{\frac{I'}{K_2}} \tag{3.21}$$

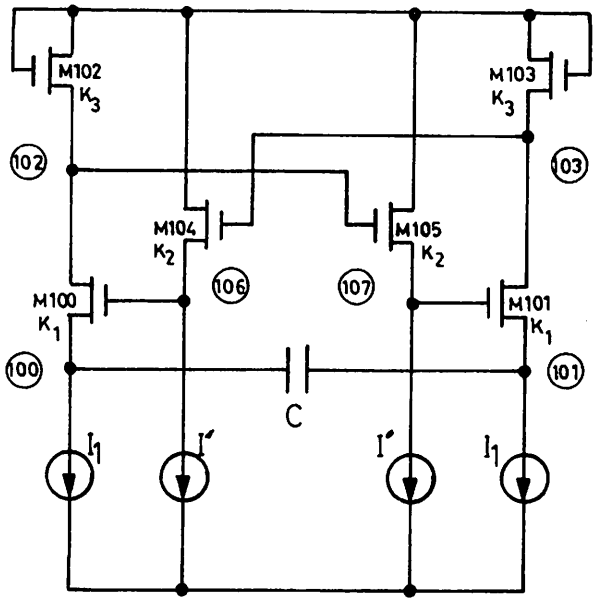

Fig 3.7 MOS Oscillator

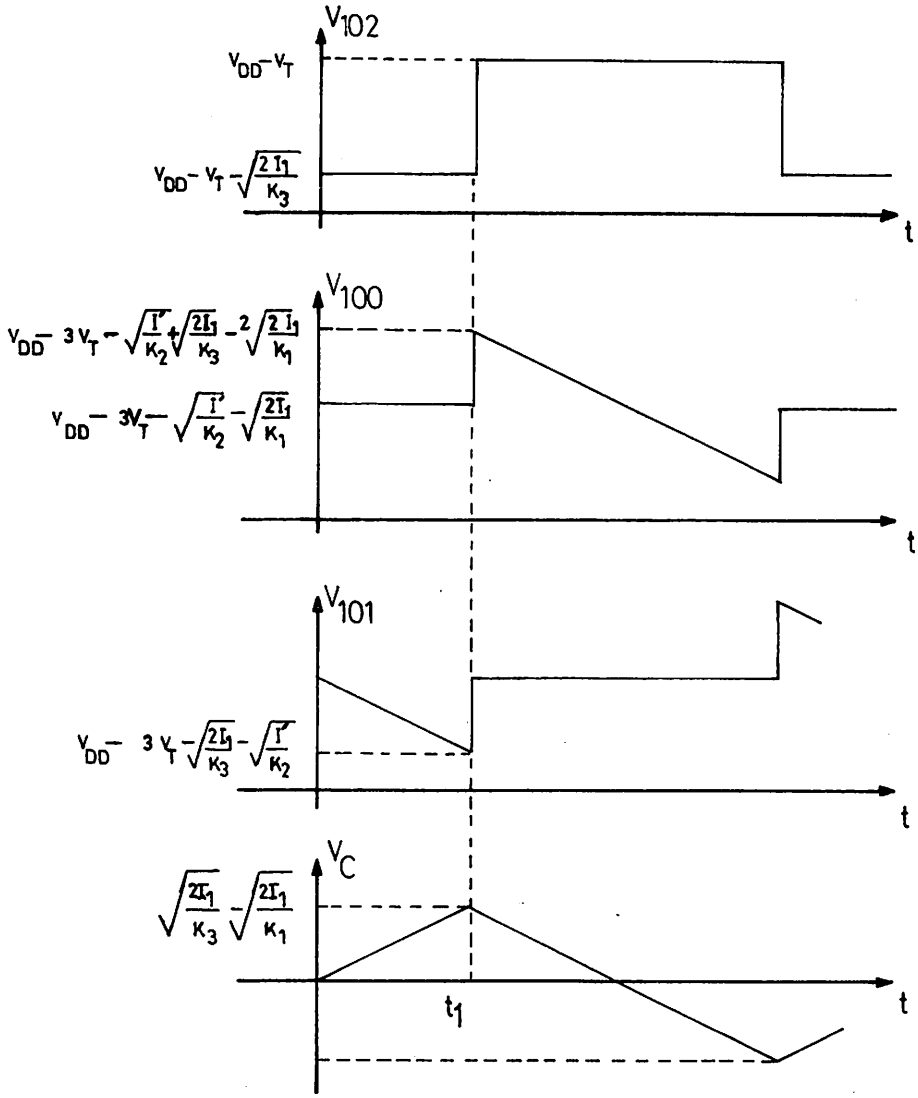

Fig 3.8

$$V100 = V_{DD} - 3V_T - \sqrt{\frac{I'}{K_2}} - \sqrt{\frac{2I_1}{K_1}} \tag{3.22}$$

The capacitor is being charged by current I_1, making the source voltage of M101 more negative. At the point when:

$$V101 = V_{DD} - 2V_T - \sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{I'}{K_2}} \tag{3.23}$$

M101 turns on. Current is drawn from M103 which make the gate of M100 more negative, turning M100 and M102 off. This change of state is due to the positive feedback behaviour of the circuit. Fig. 3.8 shows the waveforms of the circuit. Now in order to calculate the period of the oscillations:

$$\text{Max}(V_{100}-V_{101}) = \sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} \tag{3.24}$$

$$\text{voltage swing across C} = 2\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}}\right) \tag{3.25}$$

The half period is:

$$T/2 = \frac{C\Delta V}{I_1} = \frac{2C\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}}\right)}{I_1} \tag{3.26}$$

$$\boxed{T = \frac{4\sqrt{2}\,C}{\sqrt{I_1}}\left(\frac{1}{\sqrt{K_3}} - \frac{1}{\sqrt{K_1}}\right)} \tag{3.27}$$

$$f = \frac{\sqrt{I_1}}{4\sqrt{2}\,C} \times \frac{1}{\left(\frac{1}{\sqrt{K_3}} - \frac{1}{\sqrt{K_1}}\right)} \tag{3.28}$$

and in order to keep M100, M101 in saturation:

$$V102 \geq V106 - V_T \tag{3.29}$$

$$V102 = V_{DD} - V_T - \sqrt{\frac{2I_1}{K_3}} \tag{3.30}$$

$$V106 = V_{DD} - 2V_T - \sqrt{\frac{I'}{K_2}} \tag{3.31}$$

$$\therefore\ K_2 \leq \frac{I'}{\left(\sqrt{\frac{2I_1}{K_3}} - 2V_T\right)^2} \tag{3.32}$$

The above formula shows that without body-bias the frequency of the oscillator is a function of C, K_1, K_3 and I_1 and have no dependence upon V_T. Now lets consider the case where the circuit is integrated and all bodies are connected to the most negative voltage in the circuit. Node voltages for time t_1, are:

$$V100 = V_{DD} - 3V_{TO} - \gamma(\sqrt{VBS_{103} + \phi} + \sqrt{VBS_{104} + \phi} + \sqrt{VBS_{100} + \phi}) + 3\gamma\sqrt{\phi} - \sqrt{\frac{I'}{K_2}} - \sqrt{\frac{2I_1}{K_1}} \tag{3.33}$$

$$V101 = V_{DD} - 3V_{TO} - \gamma(\sqrt{VBS_{102} + \phi} + \sqrt{VBS_{103} + \phi} + \sqrt{VBS_{101} + \phi}) + 3\gamma\sqrt{\phi} - \sqrt{\frac{I'}{K_2}} - \sqrt{\frac{2I_1}{K_3}} \tag{3.34}$$

$$V102 = V_{DD} - V_{TO} - \gamma\sqrt{VBS_{102} + \phi} + \gamma\sqrt{\phi} - \sqrt{\frac{2I_1}{K_3}} \tag{3.35}$$

$$V103 = V_{DD} - V_{TO} - \gamma\sqrt{VBS_{103} + \phi} + \gamma\sqrt{\phi} \tag{3.36}$$

$$V106 = V_{DD} - 2V_{TO} - \gamma(\sqrt{VBS_{103} + \phi} + \sqrt{VBS_{104} + \phi}) + 2\gamma\sqrt{\phi} - \sqrt{\frac{I'}{K_2}} \tag{3.37}$$

$$V107 = V_{DD} - 2V_{TO} - \gamma(\sqrt{VBS_{102} + \phi} + \sqrt{VBS_{105} + \phi}) + 2\gamma\sqrt{\phi} - \sqrt{\frac{I'}{K_2}} - \sqrt{\frac{2I_1}{K_3}} \tag{3.38}$$

$$V100 - V101 = \frac{2I_1}{K_3} - \frac{2I_1}{K_1} - \gamma x \cdot$$

$$\underbrace{\left(\sqrt{VBS_{103} + \phi} - \sqrt{VBS_{102} + \phi} + \sqrt{VBS_{104} + \phi} - \sqrt{VBS_{105} + \phi} + \sqrt{VBS_{100} + \phi} - \sqrt{VBS_{101} + \phi}\right)}_{A} \tag{3.39}$$

So the last term in the above formula is added by the body effect. In the circuit the bodies are tied to $-V_{DD}$ so:

$$A = \sqrt{VDD + V_{103} + \phi} - \sqrt{V_{DD} + V_{102} + \phi} + \sqrt{V_{DD} + V_{106} + \phi} - \sqrt{V_{DD} + V_{107} + \phi} + \sqrt{V_{DD} + V_{100} + \phi} - \sqrt{V_{DD} + V_{101} + \phi} \tag{3.40}$$

The voltages $V_{100}.....V_{107}$ are dependent upon I_1 so $A = f(I_1)$

$$V_{100} - V_{101} = \sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} - \gamma A \tag{3.41}$$

$$T = \frac{4C}{I_1}\left(\sqrt{\frac{2I_1}{K_1}} - \sqrt{\frac{2I_1}{K_3}} - \gamma A\right) \tag{3.42}$$

In order to integrate the VCO capacitor on the chip it shall be kept as small as possible. For this purpose we have to work with the smallest possible I_1 and largest possible $\frac{\left(\frac{w}{L}\right)_3}{\left(\frac{w}{L}\right)_1}$. This ratio is limited by the chip size and the minimum supply voltages. Voltage swing across the capacitor shouldn't be greater than about half the supply voltage and this is what determines K_3.

Another way to analyse the circuit is to use the negative resistance approach. A current source I is applied instead of the capacitor and the voltage V is found. M_{100} and M_{102} will carry $I_1 - I$ and the current $I_1 + I$ will pass through M101 and M103.

$$V_{100} = V_{DD} - VDS_{103} - VGS_{100} - VGS_{104}$$

$$= V_{DD} - 2V_T - \sqrt{\frac{I_1 + I}{K_3}} - \sqrt{\frac{I_1 - I}{K_1}} - VGS_{104} \qquad (3.43)$$

$$V_{101} = V_{DD} - VDS_{102} - VGS_{101} - VGS_{102}$$

$$= V_{DD} - 2V_T - \sqrt{\frac{I_1 - I}{K_3}} - \sqrt{\frac{I_1 + I}{K_1}} - VGS_{102} \qquad (3.44)$$

$$V_{100} - V_{101} = \sqrt{\frac{I_1 - I}{K_3}} + \sqrt{\frac{I_1 + I}{K_1}} - \sqrt{\frac{I_1 + I}{K_3}} - \sqrt{\frac{I_1 - I}{K_1}}$$

$$= (\sqrt{I_1 - I} - \sqrt{I_1 + I}) \left(\frac{1}{\sqrt{k_3}} - \frac{1}{\sqrt{K_1}}\right) \qquad (3.45)$$

The first term is negative so in order to have a negative non-linear

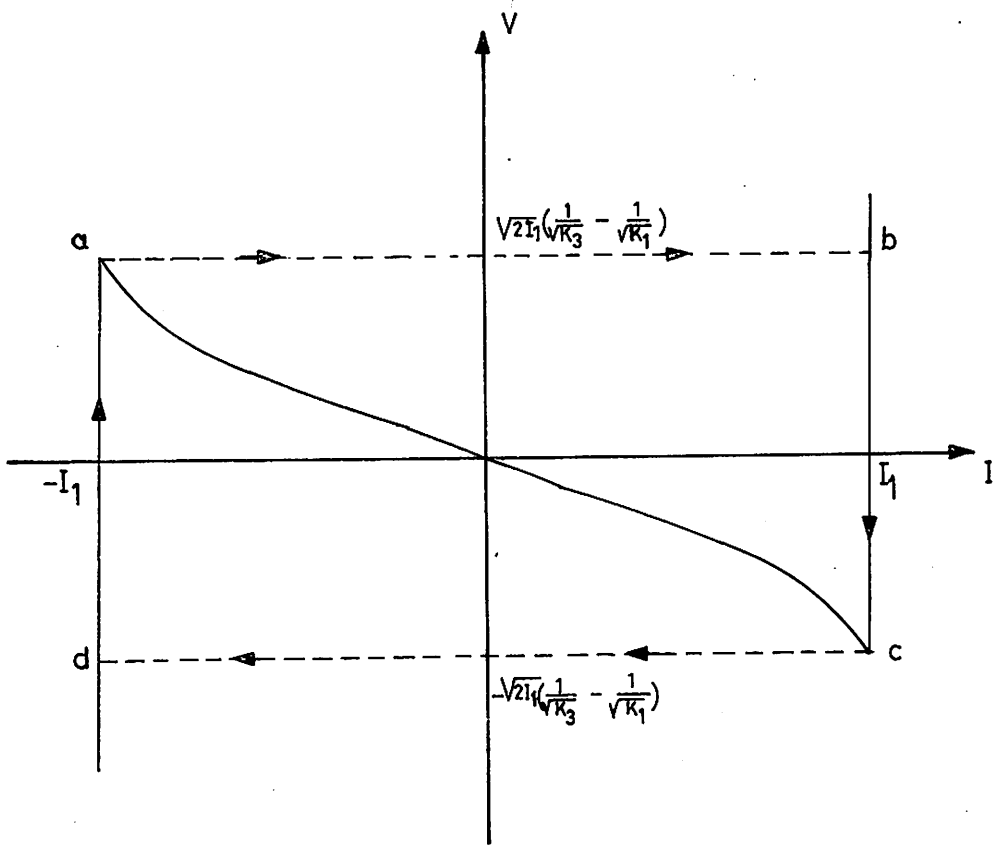

Fig 3.9 I-V Curve of the VCO

resistance the second term shall be positive:

$$\frac{1}{\sqrt{K_3}} - \frac{1}{\sqrt{K_1}} > 0 \tag{3.46}$$

$$\frac{K_1}{K_3} > 1 \tag{3.47}$$

Larger ratios of $\frac{K_1}{K_3}$ increases the positive feedback which results in more reliable oscillation.

Fig. 3.9 shows the I-V curve. If the test current source is replaced by a timing capacitor the circuit behaves as a relaxation oscillator with limit cycles as shown in Fig. 3.9 ab is a fast transition where M100 and M101 are both active. bc is a slow relaxation where M100 is off and M_{101} is on.

3.3 Voltage to Current Converter

Fig. 3.10 shows the part of the circuit which changes the low-pass filter output voltage to the control current for VCO.

Source followers M_{50}, M_{51} level shift the input voltages by $\sqrt{\frac{I_3}{K}} + V_T$ in order to keep M_{201}, M_{202} in saturation. The VCO current while free running is:

$$I_o = I' - \frac{I'}{2B} = I'(1 - \frac{1}{2B}) \tag{3.48}$$

and the frequency is:

$$f = \frac{I_1}{4C\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} - \gamma A\right)} \tag{3.49}$$

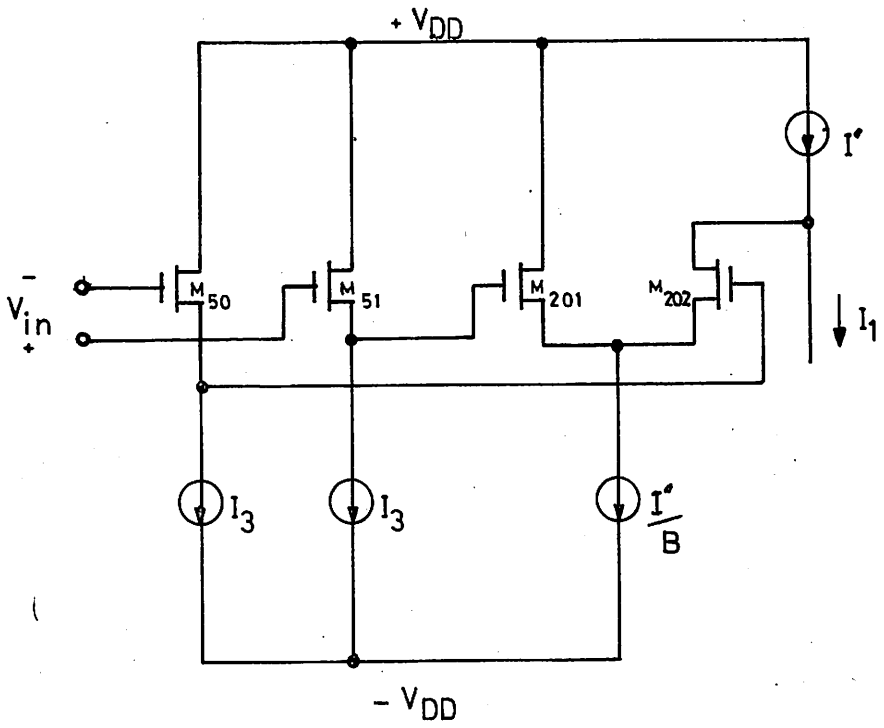

Fig 3.10 Voltage to Current Converter

neglecting the A dependence upon I_1:

$$\frac{df}{dI} = \frac{1}{4C}\left[\frac{1}{2\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} - \gamma A\right)} - \frac{\gamma A}{2\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} - \gamma A\right)^2}\right] \tag{3.50}$$

the second term is negligible so:

$$\frac{df}{dI} = \frac{1}{4C}\left(\frac{1}{2\left(\sqrt{\frac{2I_1}{K_3}} - \sqrt{\frac{2I_1}{K_1}} - \gamma A\right)}\right)$$

$$= \frac{f}{2I_1}$$

$$= \frac{1}{4\pi I_o}\omega_o \tag{3.51}$$

M_{50}, M_{51} have no gain. For the differential pair M_{201}, M_{202}:

$$\frac{dI}{dV_{in}} = 1/2\ g_m = 1/2 \times 2\sqrt{\frac{I'}{2B}K}$$

$$= \sqrt{\frac{I'}{2B}K}$$

$$= \sqrt{\frac{I_o}{2B\left(1 - \frac{1}{2B}\right)}K}$$

$$= \sqrt{\frac{I_o K}{2B - 1}} \tag{3.52}$$

$$K_o = \frac{df}{dV_{in}} = \frac{df}{dI} \times \frac{dI}{dV_{in}}$$

$$= \frac{\omega_o}{4\pi I_o} \sqrt{\frac{I_o K}{2B - 1}}$$

$$\boxed{K_o = \frac{\omega_o}{4\pi} \sqrt{\frac{K}{I_o(2B - 1)}}} \qquad (3.53)$$

3.4 Low-Pass Filter

An on chip MOS sampled data recursive filter is recommendable for this circuit.

External filters can be made of a buffer and a simple R-C filter.

For designing the filter:

$$\omega_n = \sqrt{\frac{K_V}{\tau_1 + \tau_2}} \qquad (3.54)$$

where: $\omega_1 = \frac{1}{\tau_1}$ filter pole

$$\omega_2 = \frac{1}{\tau_2} \text{ filter zero} \qquad (3.55)$$

$$\xi = 1/2\ \omega_2(\tau_2 + \frac{1}{Kv})$$

4. Result of Circuit Simulation

The circuit was checked by spice simulation. The actual circuit is consisted of thirty eight transistors. As the phase lock loop takes quite a few cycles to lock, the computer run shall be done for at least ten cycles of input frequency. This requires a very big computer time

and the limited computer memory locations for spice makes it impossible to make the run for the whole circuit. For this reason the circuit was first checked block by block and then it was simplified for simulation of the whole circuit.

The changes were:

The phase detector depletion load transistors were replaced by two resistors. The reason was that having depletion loads we had to either have a buffer and an RC filter or use a sampled data recursive filter. Both schemes were very time consuming for simulation. Using two load resistors reduced the filter to a single capacitor.

M50, M51 are replaced by two batteries. Some of the MOS current sources were replaced by ideal current sources. The simulated circuit is shown in Fig. 9.1.

Simulated Circuit Calculations

a) Phase detector gain:

In the simulated circuit ISS = 10UA, R_L = 50K so:

$$V_{out\ p-p} = 10UA \times 100K = 1V$$

$$V_{average} = -(1V)\left(1 - \frac{2\phi}{\pi}\right)$$

$$= K_D(\phi - \pi/2)$$

$$\therefore \quad \boxed{K_D = \frac{1V}{\pi/2} = .637 \ \text{volts/radion}}$$

for small signal inputs from (3.8):

$$K_D = v_1/\pi \times 2\sqrt{2\ ISS\ K_1}\ R_L$$

$$= V_1/\pi \times 2\sqrt{2\times10\times10^{-6} \times 300 \times 10^{-6}} \times 50\times10^{3}$$

$$K_D = 2.47\ v_i\ [\text{rad}]^{-1}$$

b) VCO gain:

In section 3.3 we find equation (3.53)

$$K_o = \frac{\omega_o}{4\pi}\sqrt{\frac{K}{I_o(2B-1)}}$$

in our circuit B = 1, I_o = 10 UA, K = 45 UA/V^2 f_o = 1 KHz

$$K_o = \frac{\omega_o}{4\pi}\sqrt{\frac{45}{10(2-1)}}$$

$$\boxed{K_o = .17\ \omega_o}$$

The loop gain is:

$$K_V = K_D\ K_o = .637 \times .17\ \omega_o$$

$$\boxed{K_V = .11\ \omega_o}$$

From (2.10) flat bandwidth will be achieved at:

$$\omega_1 = 2K_V$$

$$\frac{1}{RC} = 2\times.11 \times 2\pi\times10^{3}$$

$$R = 100K$$

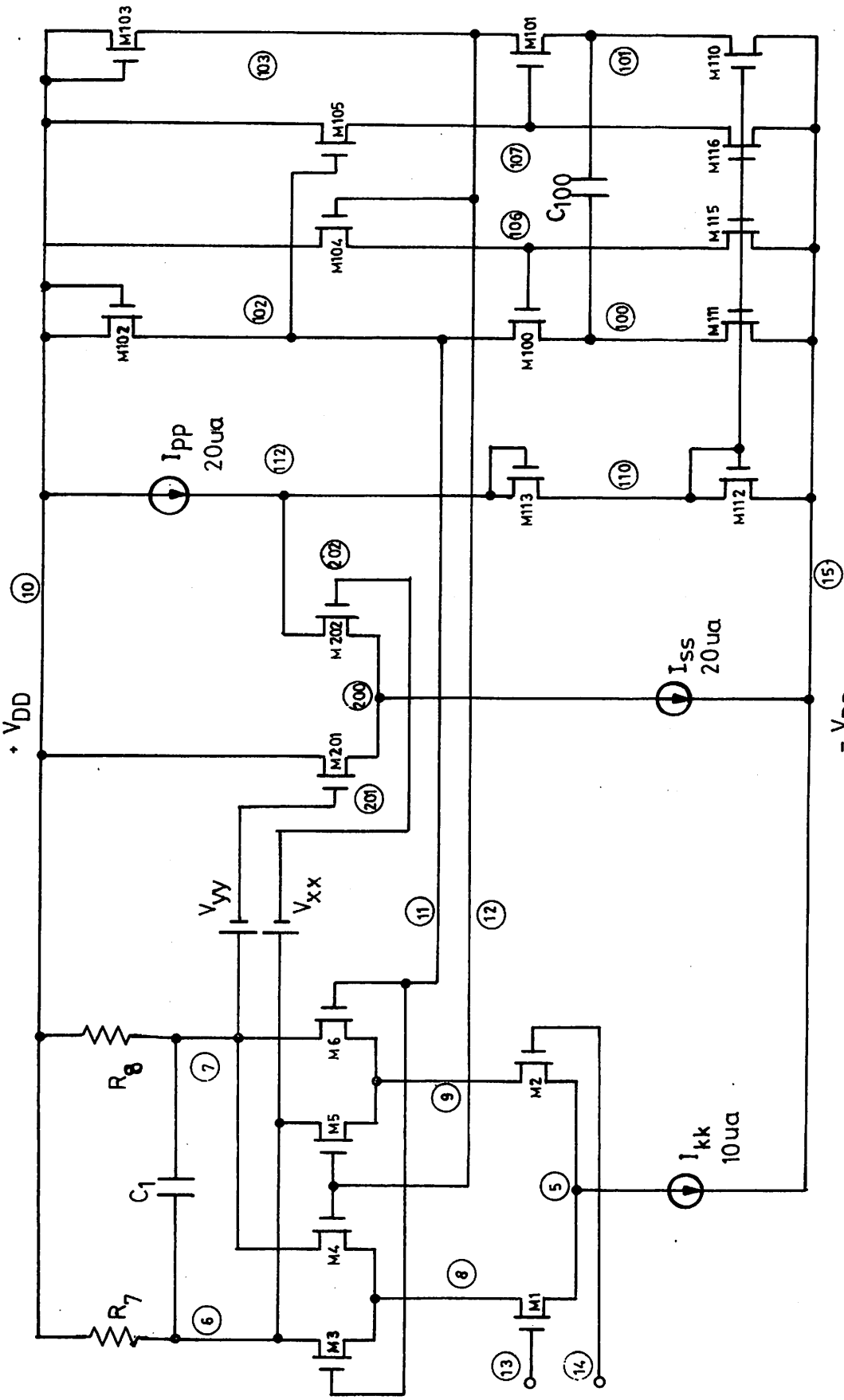

Fig 4.1 SCHEMATIC OF THE SIMULATED CIRCUIT

$\therefore$ $\boxed{C = 7.4\ NF}$

A copy of the computer simulation is attached. It shows the phase-lock loop locking to the incoming signal. The initial conditions were taken from the free-running node voltages. As can be seen the error voltage has still got second harmonic on it. In order to see the dc component the output is integrated and plotted in Fig. 4.2.

5. Conclusions

Spice simulation proved the acceptable functioning of the circuit. One of the applications of this circuit is telephone touch tone decoding. All the seven PLLs and the VCO timing capacitors and the low pass filters can be integrated on one chip. For a 1KHZ center frequency a 1 NF capacitor is needed. Dividing the VCO frequency by 32 by adding 5 flip flops to each PLL will result in 30 PF integrable timing capacitors. For this purpose were narrow bandwidth is desirable B and K should both be large in K_o, and K_D must be kept small.

The linearity of the output frequency response should be checked after the fabrication. A linear output is expected. If so this PLL can be used for all the other applications the bipolar PLLs are used for.

REFERENCES

1. R.G. Meyer, Nonlinear Analog Circuits Chapter 12, class notes.

2. F. M. Gardner, "Phase-Lock Techniques, " Wiley, New York, 1966.

3. "Application of Phase-Locked Loops," Signetics Corporation, 1974.