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PRACTICAL DESIGN CONSIDERATIONS FOR MOS SWITCHED CAPACITOR LADDER FILTERS

by

G. M. Jacobs

Memorandum No. UCB/ERL M77/69

11 November 1977

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I. INTRODUCTION

Frequency selective filtering circuits perform one of the most important functions of present day electronics systems. The theory behind filter design has been highly developed in a search for special filter functions and types of circuitry that will simplify their implementation. This effort is now extending itself to the field of integrated circuits whose small size previously prohibited any complex filtering from being practical. Today's large scale integration techniques are being used to integrate entire systems, some of which require on-chip filtering. The filters for this purpose must make efficient use of silicon area and need no trimming.

The research activity in MOS-LSI compatible switched capacitor filters began at Berkeley in 1975, with the development of a monolithic NMOS operational amplifier of reasonable performance. This led to the work of I. Young [11], in which a classical recursive filter section, customarily implemented digitally, was implemented in the analog domain using switched capacitor delay elements. While good results were obtained, this technique has the drawback that as the sample rate is increased, the sensitivity of the filter to capacitor ratio errors increases. By altering the configuration of the switched capacitors, a switched capacitor integrator can be realized, as investigated by F. Hostica [12,13]. This allows filter configurations closely related to those realizable with classical analog integrators. In Hostica's work these integrators were used to realize state variable filters with excellent performance. However, active filters made up of second order sections, such as state variable sections, tend to have increased sensitivity when multiple

pole filters are implemented. It is well known from classical filter theory [1]-[8] that for these high order filters a passive doubly-terminated RLC ladder achieves the lowest sensitivity to component variations in the passband and in fact has zero sensitivity to component variation when the power is matched between source and load. Over a decade ago, Orchard [10] showed that this low sensitivity can be maintained in active filters using a "leapfrog" or "active ladder synthesis" which was developed to simulate RLC ladder networks exactly using active filter building blocks [1]. In order to obtain minimum sensitivity high order filters, a similar approach to the "leapfrog" design was taken in this paper although the implementation and design criteria differ.

These configurations have been incorporated in the work of D. Allstott, in the design and fabrication of monolithic fully integrated high-order filters. This work has resulted in the fabrication of an experimental fully-integrated high-order NMOS filter with excellent performance characteristics. These configurations have also been utilized by K. Tan in his work on high-order fully integrated analog filters using bipolar technology.

The objective of this research was to consider analytically several practical aspects of the design of sampled-data ladder filters. In section II, the previous work in the area of sampled data integrators is reviewed. In section III, the flow graph techniques used for the design of active ladder structures is reviewed. In this section, a new configuration for the realization of the high-pass function is presented. In IV, the use of lossless integrator configurations to compensate for sampled-data integrator phase shift is explored, and in section V, a new method of incorporating zeros is explored. In chapter VI, a preliminary study of

noise in switched-capacitor ladder filters is presented. In section VII, new results are given on the effects of terminations on the noise, dynamic range, and area of ladder filters. Finally, in section VIII, experimental results are presented as taken from breadboards of the various types of filters.

II. ELEMENTS OF SWITCHED CAPACITOR FILTERS [12]

The design of switched capacitor filters requires the use of several common building blocks that are spread throughout the circuit. These are described below:

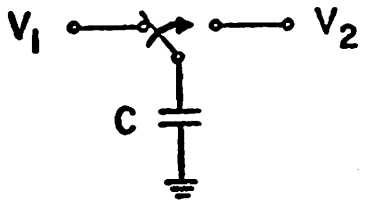
A. Switched Capacitor "Resistors"

A major reason that active filters have not previously been fully integrated in MOS technology is the necessity of accurately defining resistance-capacitance products, which requires that the absolute value of the resistors and capacitors be well controlled. In addition, integrated (diffused) resistors have poor temperature and linearity characteristics as well as requiring a large amount of silicon area.

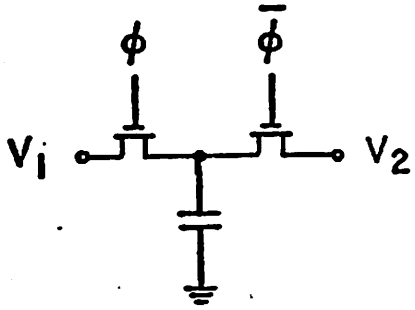
A circuit that performs the function of a resistor which does not have these disadvantages has been investigated by several workers [12]-[15] and is shown in Fig. 1a. The operation of this "resistor" is as follows: the switch is initially in the left hand position so that the capacitor C is charged to the voltage, V_1. The switch is then thrown to the right and the capacitor is discharged to V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C(V_2-V_1)$. If the switch is thrown back and forth every T_c seconds, then the current flow, i, into V_2 will be

$$i = \frac{C(V_2-V_1)}{T_c} \qquad (1)$$

Thus the size of an equivalent resistor which would perform the same function as this circuit is $R = T_c/C$. If the switching rate, $f_c = 1/T_c$,



(a)



(b)

Fig.1 a) Switched capacitor "resistor"
b) MOS implementation of (a)

is much larger than the signal frequencies of interest, then the time sampling of the signal which occurs in this circuit can be ignored and the switched capacitor can then be considered as a direct replacement for a conventional resistor. If, however, the switch rate and signal frequencies are of the same order, then sampled data techniques are required for analysis and, as for any sampled data system, the input should be band-limited below $f_c/2$ as dictated by the sampling theorem.

The MOS realization of the circuit of Fig.1a is shown in Fig.1b The two MOSFETs are operated as switches which are pulsed with a two phase non-overlapping clock (ϕ and $\bar{\phi}$) at a frequency f_c. The stability and linearity of the resistance value $R = 1/f_c C$, is much better than that obtained from diffused resistors, since the insulator in a properly fabricated MOS capacitor has essentially ideal characteristics. For example, typical temperature coefficients for these capacitors are less than 10ppm [16]. Another important advantage of the switched capacitor resistors is the high accuracy of RC time constants that can be obtained with their use. If a capacitor, C_1, which is switched at a clock rate of f_c is connected to a capacitor, C_2, the resultant time constant of this RC network, τ_{RC}, is

$$\tau_{RC} = \left(\frac{1}{f_c C_1}\right) C_2 = \frac{1}{f_c}\left(\frac{C_2}{C_1}\right) \qquad (2)$$

For a given clock rate the value τ_{RC} is therefore determined by a ratio of capacitor values which makes it insensitive to most processing variations.

The relative values of the capacitors C_1 and C_2 are determined by photolithographic definition of their area. Since the capacitance per unit area is uniform across an IC it is possible to achieve high

precision in the capacitor ratio. It has been shown that the error in such ratios can be less than 0.1% using standard MOS processing techniques [16]. In addition, the stability of this ratio is extremely high since, to first order, there is no temperature dependence in the capacitance ratio. It is thus apparent that the switched capacitor resistor of Fig. 1 makes it possible to design precise stable RC active filters which can be fully integrated using MOS technology.

B. Switched Capacitor "Resistor" Inverter and Differencer

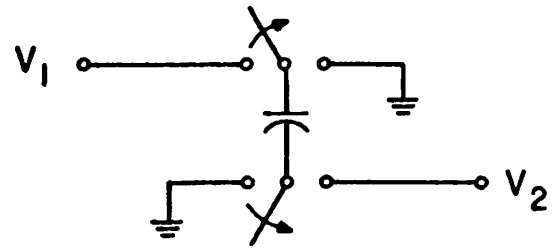
By slightly modifying the switched capacitor resistor of Fig. 1 one can realize a sign inversion and difference of several voltages. The charge transferred to V_2 in Fig. 2a is taken from the bottom plate of the capacitor and is therefore related to the negative of voltage V_1. More precisely, the "current" flow between V_1 and V_2 is given by

$$i = \frac{C[V_2-(-V_1)]}{T_c} = \frac{C(V_2+V_1)}{T_c} \tag{3}$$

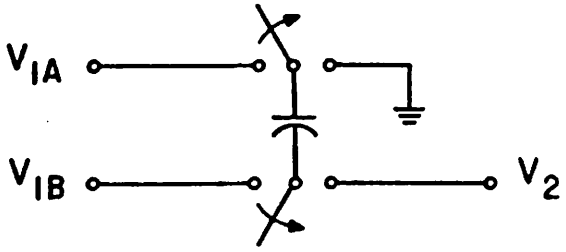
The inversion requires only 2 more MOS switches over the non-inverting case. By charging a capacitor to the difference of two voltages before switching, one can achieve a switched capacitor "resistor" that transfers charge related to this difference. The circuit for a differencer is shown in Fig. 2b. The "current" flow between nodes $V_{1A,B}$ and V_2 is given by

$$i = \frac{C[V_2-(V_{1B}-V_{1A})]}{T_c} \tag{4}$$

The voltage source V_2 could be the virtual ground input of an operational amplifier in which case the circuits described above could be used to feed several voltages into the op amp with appropriate signs.



(a)



(b)

Fig.2 Switched capacitor "resistor"
a) inverter
b) differencer

C. Sampled Data Integrators [12]

Sampled data filters are most easily designed using state space theory. This was used previously as an analog simulation technique for analog computers. The basic building block of these computers is an operational amplifier connected as an integrator as shown in Fig. 3a. The transfer function of this integrator is

$$H(\omega) = -\frac{1}{j\omega R_1 C_2} \tag{5}$$

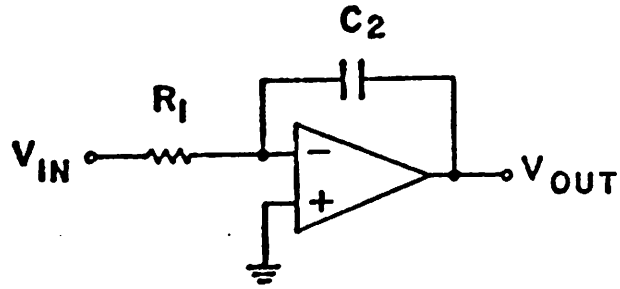
In Fig. 3b, the resistor, R_1, in the integrator has been replaced by the switched capacitor circuit of Fig. 1a with $C_1 = 1/f_c R_1$. In the n^{th} clock period, the capacitor C_1 is charged to the voltage $V_{IN}(nT_c)$ and then after the switch is thrown to the right, is discharged by the operational amplifier. The charge $C_1 V_{IN}(nT_c)$ is thus effectively transferred from C_1 to the feedback capacitor C_2. Taking into account the delay of one clock period introduced by the switching process results in the following charge conservation equation:

$$C_2 V_{OUT}[nT_c] = C_2 V_{OUT}[(n-1)T_c] - C_1 V_{IN}[(n-1)T_c] \tag{6}$$

Since this is a sampled data system, the z-transform technique should be used, which yields the transfer function

$$H(z) = \frac{-(C_1/C_2)z^{-1}}{1-z^{-1}} \tag{7}$$

A block diagram of the z-transform interpretation of this integrator is shown in Fig. 3c. It should be noted here that sampled data filters, being a cross between analog and digital methods, present unique problems for analysis and synthesis. The goal of this paper is to design using the well documented continuous time filter theory. Analysis



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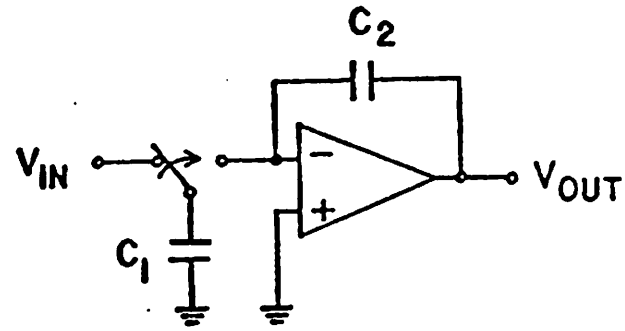

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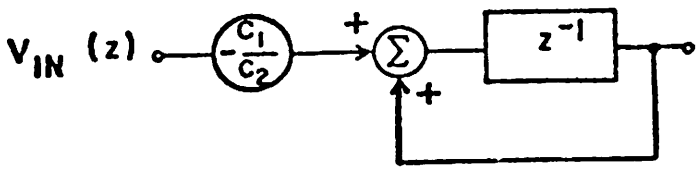


(c)

Fig.3 a) continuous time integrator b) sampled data integrator
c) z-transform block diagram of (b)

however, is often done in the sampled domain in order to provide more exact simulations of the actual circuits.

III. DESIGN OF ACTIVE LADDER NETWORKS

A. The Signal Flow-Diagram

The key to the design of an active ladder network lies in the use of a state space description [17]. This method begins by transforming the differential equations describing the network into a pictoral representation called a flow-diagram. The flow-diagram, unlike a circuit schematic, contains nodes for both voltage and current variables in the circuit. The branches which interconnect these nodes represent the transfer functions of each circuit element. There are usually several valid flow-diagram representations of a given network which must be realized in different ways. The objective here is to manipulate the signal flow-diagrams in order to obtain a representation that can be realized with switched capacitor integrators. To write down a flow-diagram for a canonical network, one simply creates a node for each voltage and current in the circuit, and then interconnects them with the proper impedance using Kirchoff's nodal and loop equations. There are also many rules for the proper reduction of redundant branches in a flow-diagram. The reader is left to examine these in the reference [17]. Examples will follow.

B. Flow-Diagram Construction for Lowpass, Bandpass and Highpass Networks

1) Lowpass Ladder

In this section, flow diagrams for RLC filter networks will be constructed. Fig. 4 shows a doubly terminated lowpass ladder with

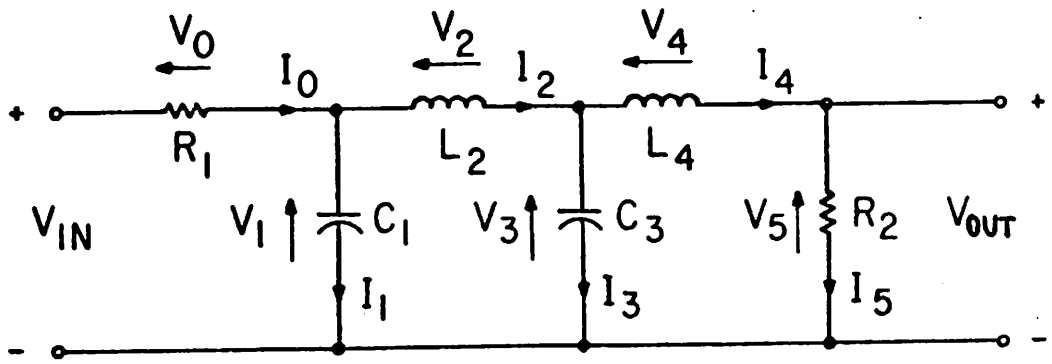


Fig.4 Doubly terminated lowpass ladder with voltages and currents defined

voltages and currents defined. As stated earlier, the first step toward constructing a flow diagram is to create a node for each voltage and current in the circuit. This is shown in Fig. 5a. Each node is now defined by the gains leading into it. Multiple inputs into a single node are to be considered summed at that node. For integrator realizations, one should attempt to define the circuit impedances using integrations only. For example, V_1 in the ladder of Fig. 4 should be defined by an arrow (gain) leading into it with value $1/sC_1$ from I_1. Similarly, I_2 should be defined from V_2 by the gain $1/sL_2$. See Fig. 5b. Resistances (and conductances) appear in the diagram as multipliers between currents and voltages. The diagram is completed by defining the remaining nodes using the following loop and node equations:

$$
\begin{aligned}
V_0 &= V_{IN}-V_1 & V_3 &= (1/sC_3)I_3 \\
I_0 &= V_0G_1 & V_4 &= V_3-V_5 \\
I_1 &= I_0-I_2 & I_4 &= (1/sL_4)V_4 \\
V_1 &= (1/sC_1)I_1 & I_5 &= I_4 \\
V_2 &= V_1-V_3 & V_5 &= I_5R_2 \\
I_2 &= (1/sL_2)V_2 & V_{out} &= V_5 \\
I_3 &= I_2-I_4
\end{aligned}
\qquad (8)
$$

The completed diagram is shown in Fig. 6 . It should be emphasized that this flow-diagram is one of many that describe the ladder (for example, differentiations could have been used) but this one was chosen because of its ease of implementation when using switched capacitor techniques.

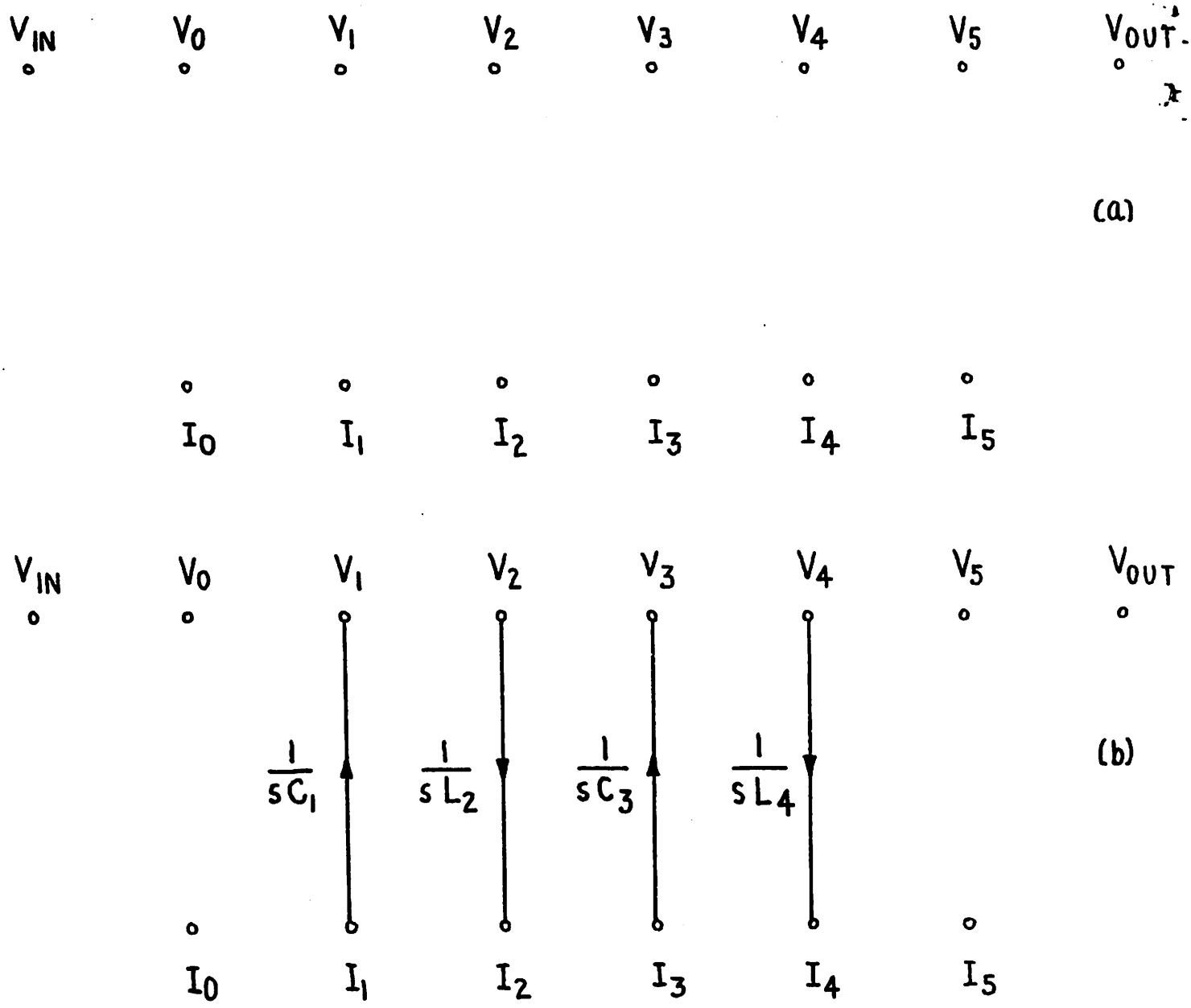


Fig.5 Flow-diagram construction of lowpass ladder in Fig.4
a) voltage and current nodes
b) addition of integrations

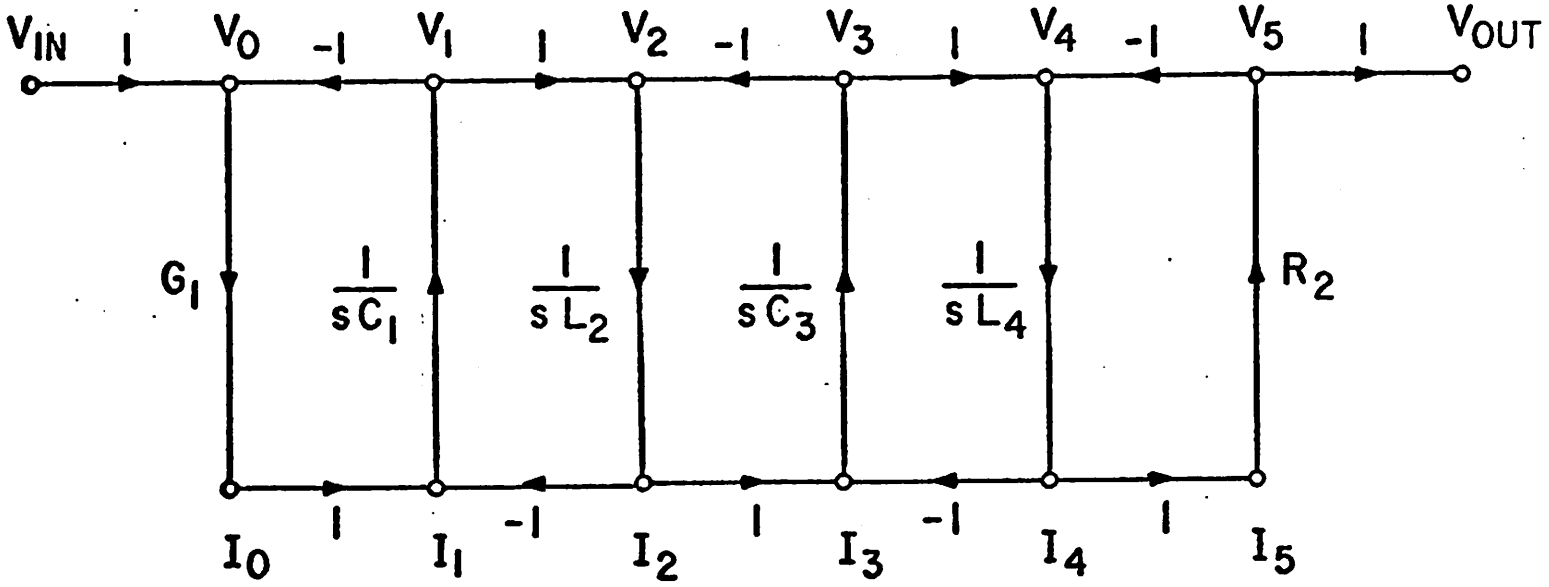


Fig.6 Completed flow-diagram for lowpass ladder in Fig.4

2) Bandpass ladder

The bandpass ladder is obtained by performing the standard bandpass transform on the lowpass ladder [2]. This is done by letting

$$\underline{S} \rightarrow \frac{\omega_o}{B.W.} \left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right) \tag{9}$$

where B.W. is the desired 3 dB bandwidth of the passband and ω_o is the center frequency. The transformation is traditionally performed on a lowpass prototype whose cutoff frequency ω_o is 1 rad/sec. Figures 7a,b show a 2 pole lowpass ladder and its equivalent bandpass structure after transformation. Fig. 8 shows how each element transforms. A signal flow-diagram can be constructed from the network of Fig. 7b that contains only integrators. It is slightly more complicated than the lowpass ladder due to the shunt and series element pairs. Several of the voltage and current nodes require triple summations as shown in the flow diagram for a fourth order bandpass network given in Fig. 7c .

3) Highpass ladder

The highpass ladder is obtained by performing the highpass transform [2]

$$S \rightarrow 1/s \tag{10}$$

on the lowpass prototype. This transform simply interchanges capacitive and inductive elements in the network. Figs. 9a,b show a highpass ladder and its corresponding all-integrator flow diagram.

C. Circuit Implementation

Once the proper flow diagram is drawn for a network, it requires only several additional steps to obtain an actual circuit representation. The diagram of Fig. 6 completely describes the lowpass ladder of Fig. 4 .

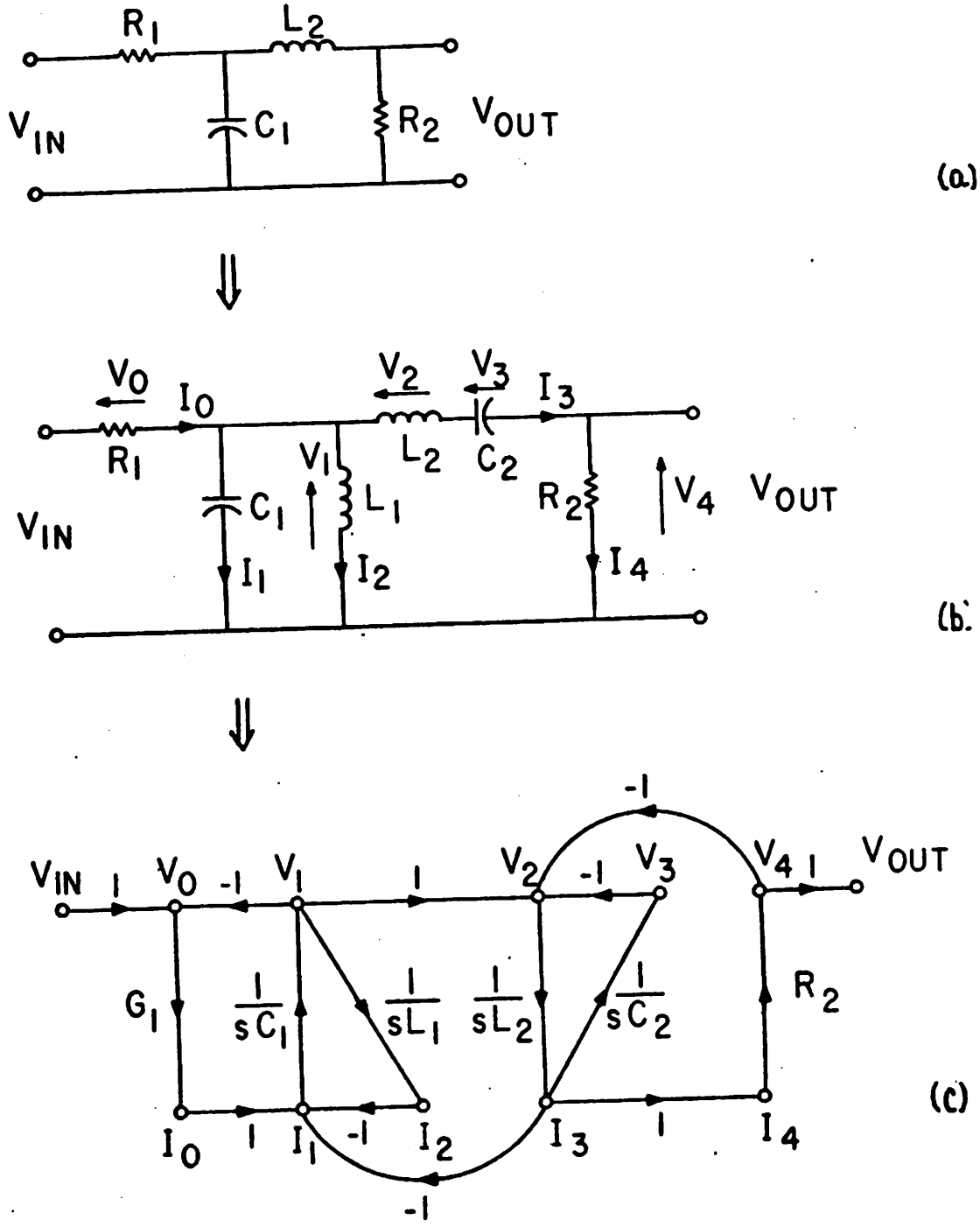


Fig.7 Bandpass Ladder
a) lowpass prototype
b) corresponding bandpass ladder
c) flow-diagram of (b)

$$S \longrightarrow \frac{w_0}{B.W.}\left(\frac{S}{w_0} + \frac{w_0}{S}\right)$$

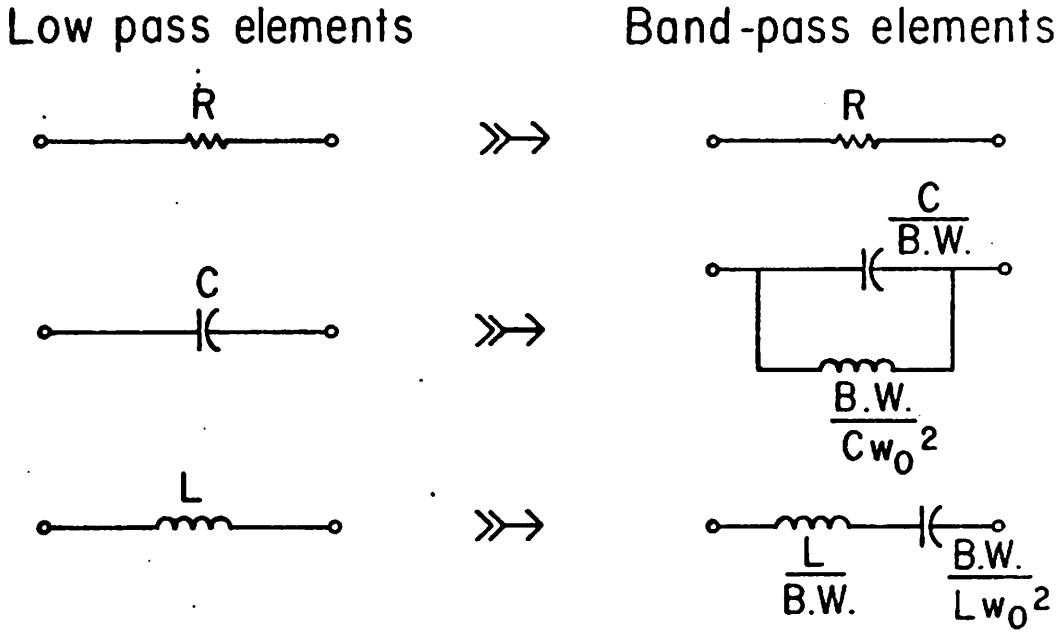
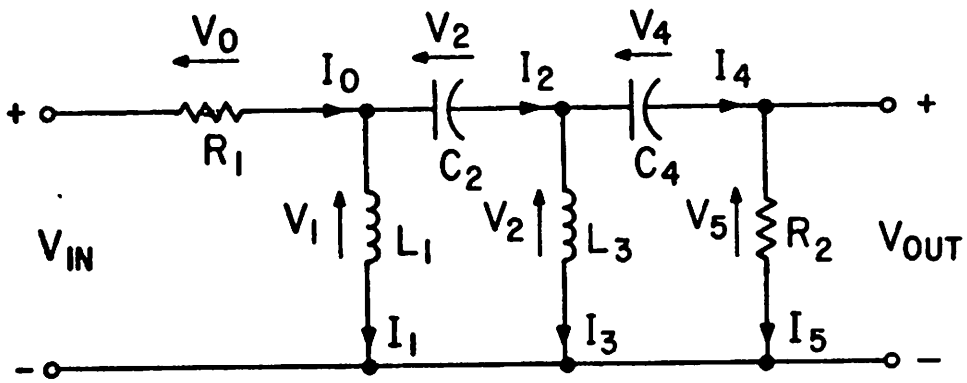
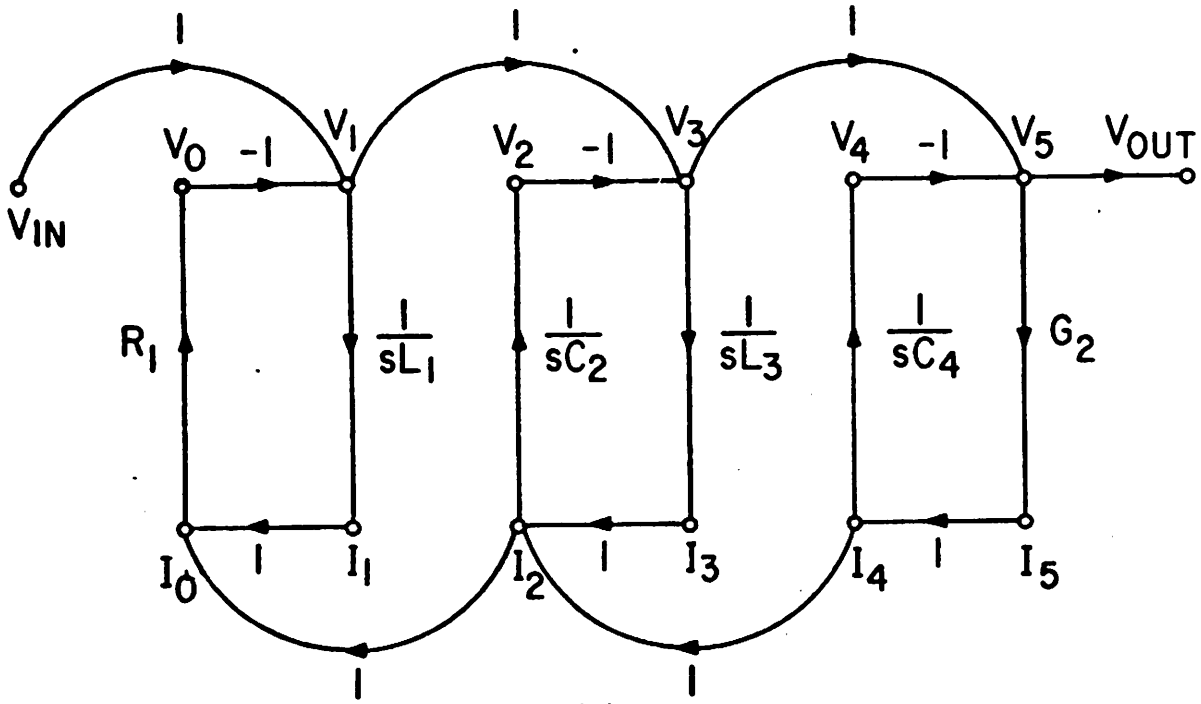


Fig.8 Lowpass to Bandpass Transform



(a)



(b)

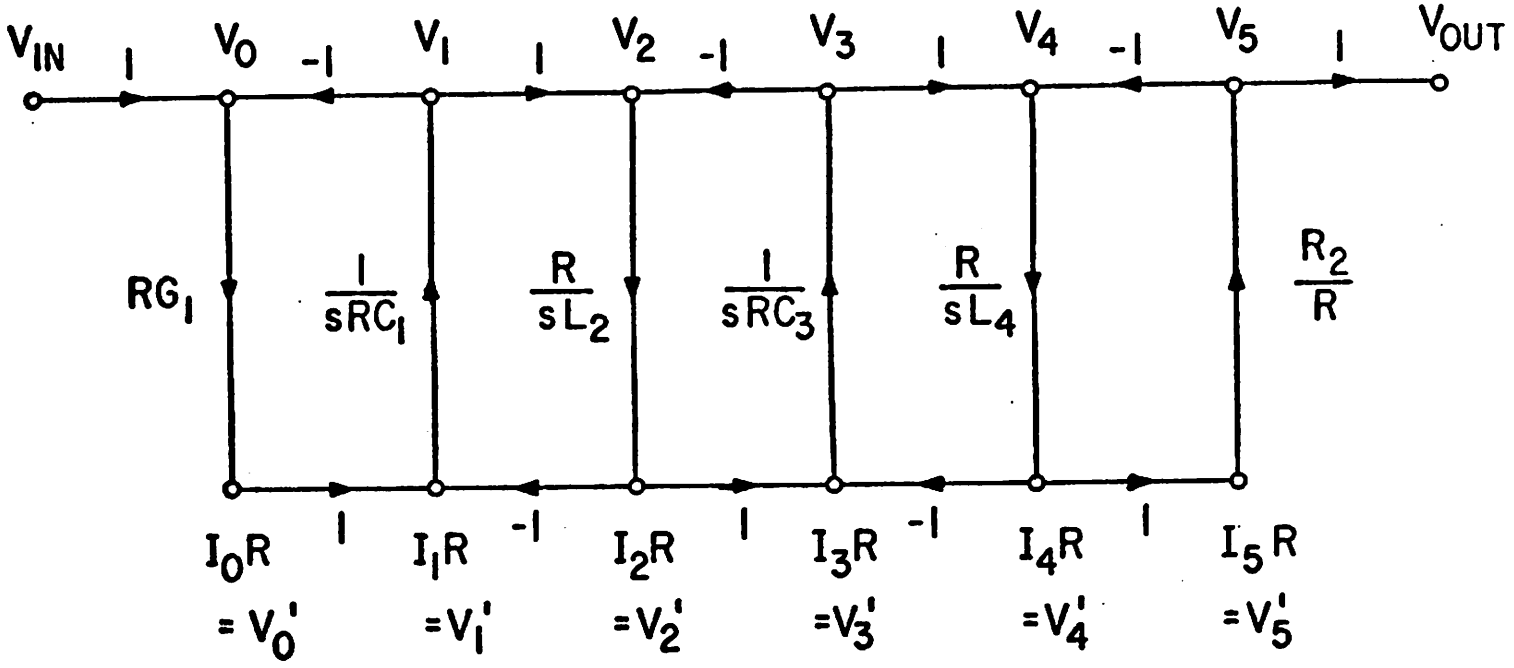
Fig.9 a) doubly terminated highpass ladder
b) flow-diagram of (a)

However, there are nodes representing currents, and integrators are bordered by both voltages and currents. Since the implementation will use voltage controlled voltage sources (operational amplifiers) as integrators, it is desirable to transform current nodes to voltages. This is performed by multiplying all currents nodes by a scaling resistance R. The currents now become voltages and to maintain the proper relationships between all nodes, the transfer functions are also scaled. The scaled diagram is shown in Fig. 10a. Scaled current nodes are shown as voltages with "primes". The integrators now have the conventional 1/RC or R/L time constants. The tradeoffs involved in choosing a value for R are discussed in Sec. VII. If R = 1, the integrator time constants are simply the original L or C values.

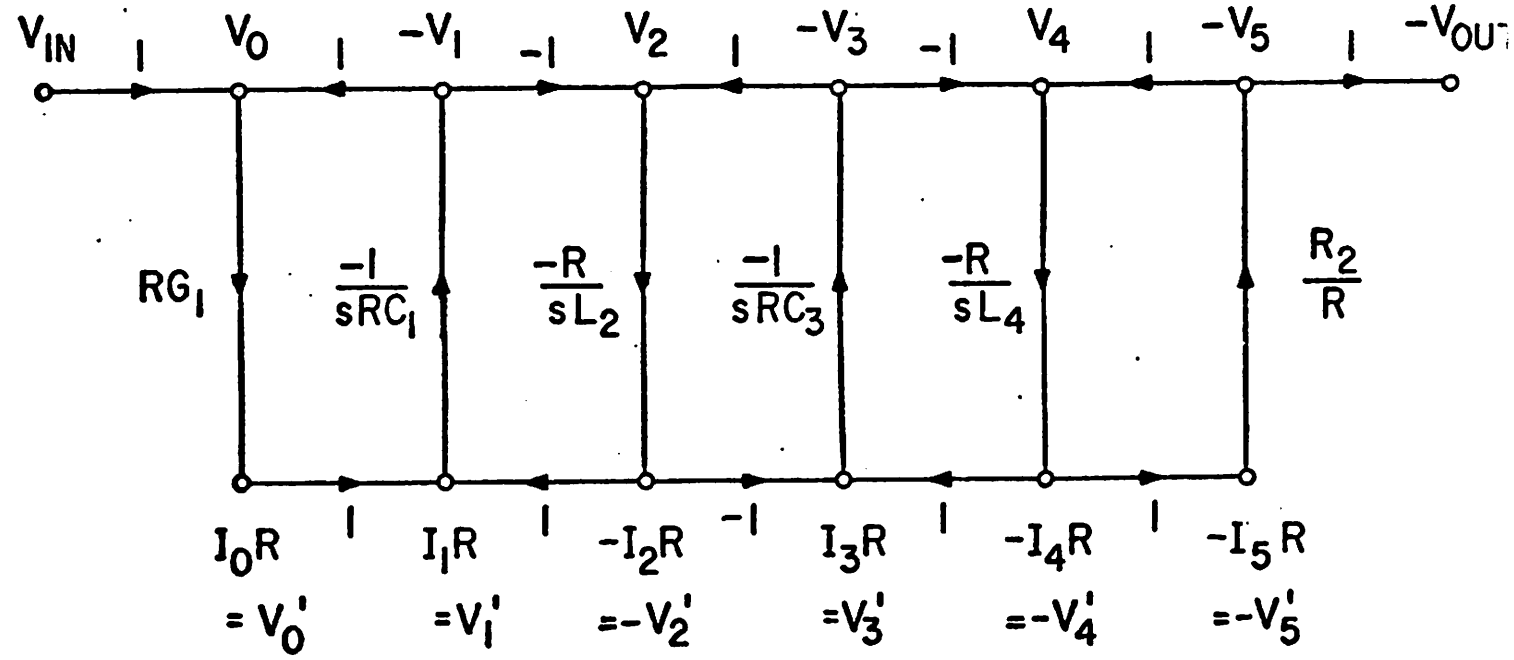
The circuit of Fig. 10a is implemented using non-inverting integrators requiring two more switches than the inverting type. However, circuit simplification may again be achieved by inverting the signs on the flow-diagram integrators and making the necessary changes on connecting nodes. This is shown in Fig. 10b. This simplified circuit is illustrated symbolically in Fig. 11. [17].

As a specific example, refer to Fig. 4 for a fourth order lowpass ladder, which requires the following values for the prototype filter to obtain a Butterworth response. (ω_o=1rad/sec): [15]

$$\begin{aligned} R_1 &= 1\Omega \\ C_1 &= 0.7654\ F \\ L_2 &= 1.848\ H \\ C_3 &= 1.848\ F \\ L_4 &= 0.7654\ H \\ R_2 &= 1\Omega \end{aligned} \qquad (11)$$



(a)



(b)

Fig.10 a) scaled all-voltage version of flow-diagram in Fig.6
b) flow-diagram in (a) adjusted for inverting integrators

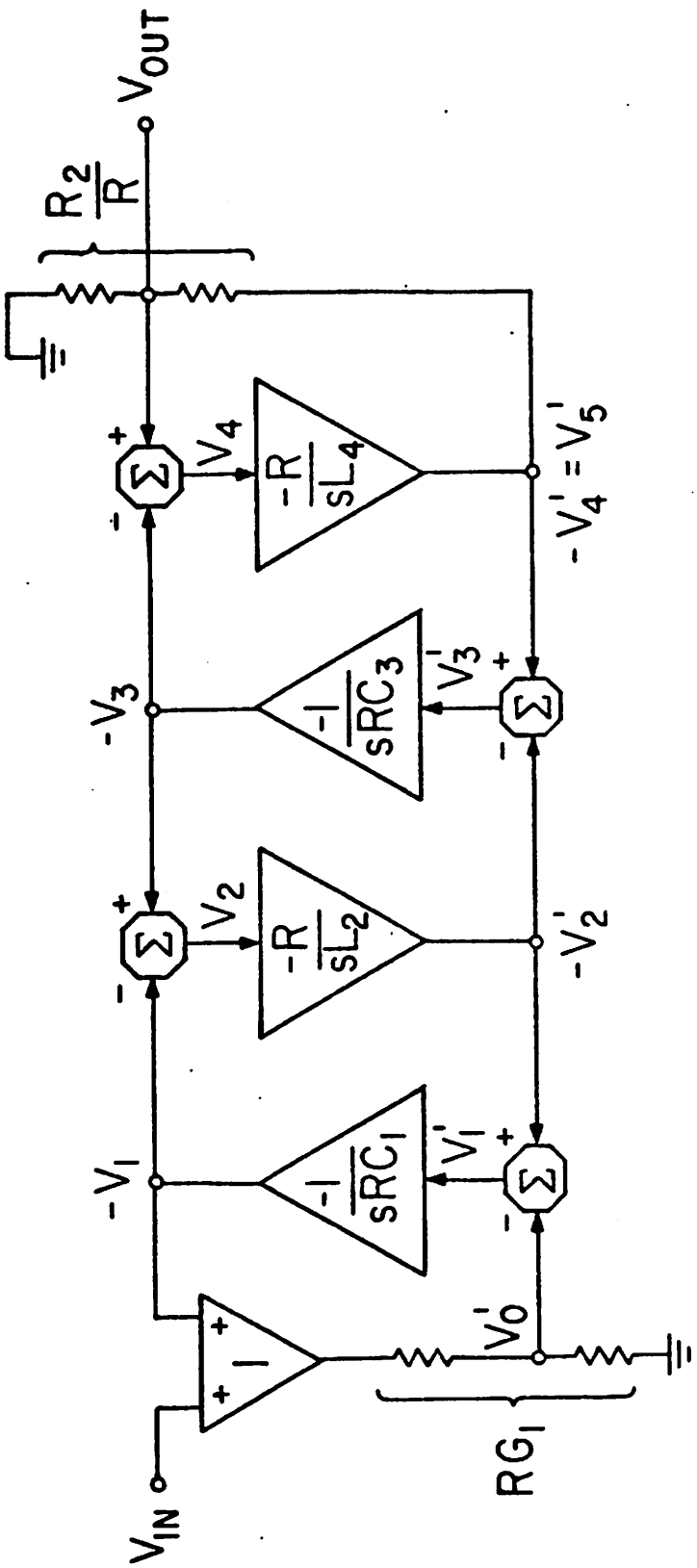


Fig.11 Symbolic representation of flow-diagram in Fig.10(b)

These values are scaled to $\omega_o = 2\pi(1000\text{Hz})$ - the desired cutoff frequency.

$$\begin{aligned} R_1 &= 1\Omega \\ C_1 &= 1.218\times10^{-4}\ \text{F} \\ L_2 &= 2.941\times10^{-4}\ \text{H} \\ C_3 &= 2.941\times10^{-4}\ \text{F} \\ L_4 &= 1.218\times10^{-4}\ \text{H} \\ R_2 &= 1\Omega \end{aligned} \tag{12}$$

If we let our current scaling resistor R = 1Ω, then the L, C values are the integrator time constants. From equation (2),

$$\tau_{RC} = \frac{1}{f_c}\left(\frac{C_2}{C_1}\right) = L,C \tag{13}$$

To get the actual ratio $\left(\frac{C_2}{C_1}\right)$ of the feedback capacitor to the input capacitor for a specific integrator, it is necessary to multiply its L or C value (time constant) by the sampling rate. Therefore, for a 40 kHz clock rate:

$$\begin{aligned} \left(\frac{C_2}{C_1}\right)_{C_1} &= (1.218\times10^{-4})(4.0\times10^{4}) = 4.872 \\ \left(\frac{C_2}{C_1}\right)_{L_2} &= (2.941\times10^{-4})(4.0\times10^{4}) = 11.76 \\ \left(\frac{C_2}{C_1}\right)_{C_3} &= (2.941\times10^{-4})(4.0\times10^{4}) = 11.76 \\ \left(\frac{C_2}{C_1}\right)_{L_4} &= (1.218\times10^{-4})(4.0\times10^{4}) = 4.872 \end{aligned} \tag{14}$$

The usual impedance scaling done on continuous time networks is not necessary. The one ohm terminations are actually the simplest in terms of circuit hardware. The clock rate is an important choice because it

determines the magnitude of the ratios necessary. Any clock rate over the Nyquist rate will do, but the designer should pick a rate that is optimum for circuit values and fabrication. The switched capacitor network for the Butterworth filter is shown in Fig. 12. The input is brought in with a negative sign (180° phase shift) to avoid the use of an extra capacitor. The circuit of Fig. 12 consists completely of the elements described earlier. The input capacitors to the op amps switch into a virtual ground thus allowing them to perform summations as well as define integrator time constants. The terminations are paths from the output to the input of the first and last integrators.

The method outlined in this section applies to any type of filter. The design is very straightforward since the values obtained from filter tables need only be scaled in frequency and by the clock rate to obtain capacitance ratios.

IV. EFFECTS OF TIME DELAYS IN SAMPLED DATA INTEGRATORS

Frequency Response Errors

The implementation of a continuous time flow diagram using sampled data integrators must be examined closely to determine the effect of the time delays through the integrators on the transfer function. The z-domain representation of a sampled data integrator was discussed in section IIc. It will be shown in this section that the frequency response characteristics of a sampled data integrator differ significantly from those of a continuous time integrator. The "errors" (pole movement) brought about by the difference do indeed show up in the filter transfer function, but can be minimized by slightly modifying the sampled data integrators.

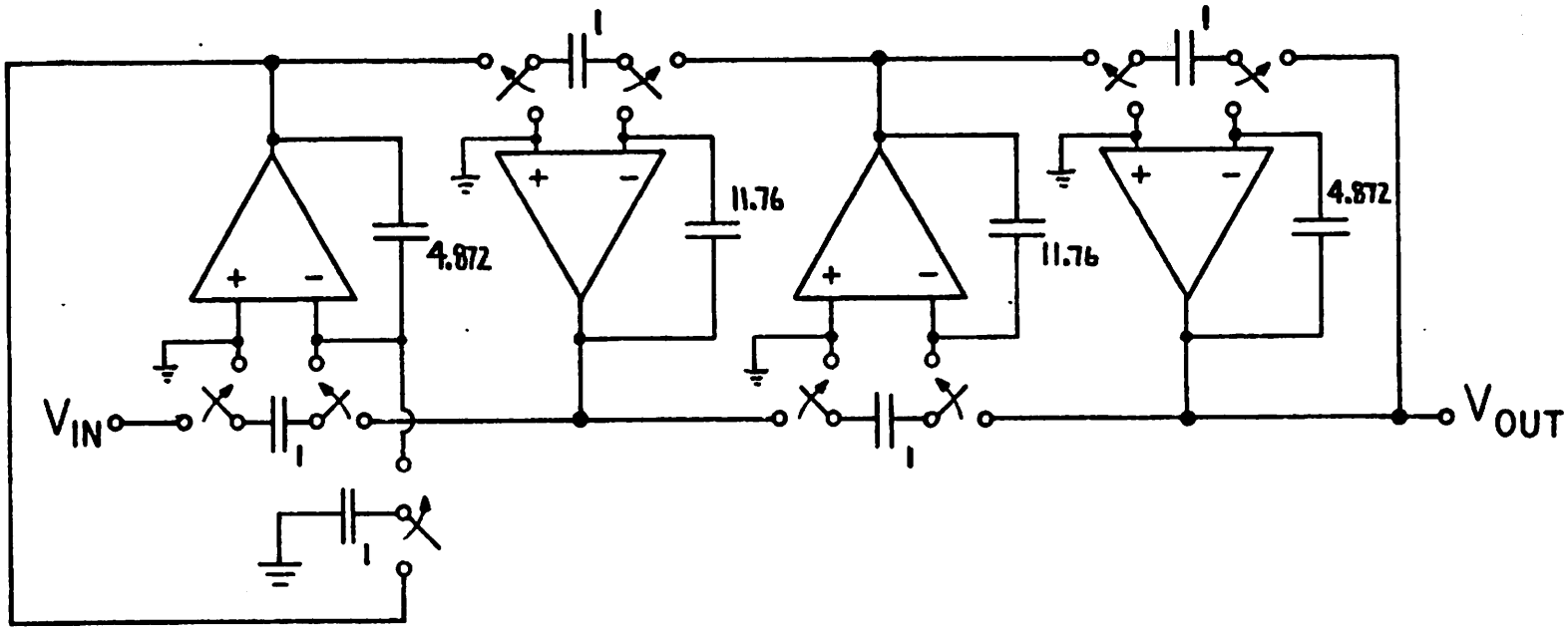


Fig.12 Switched capacitor circuit for Butterworth lowpass example of Section IIIc

Neglecting gain constants, the z-transform of the sampled data integrator, Eq. (7) can be compared to the Laplace transform of a conventional integrator, $\frac{1}{s}$.

$$\frac{1}{s} \leftrightarrow \frac{Tz^{-1}}{1-z^{-1}} \tag{15a}$$

T, the sampling period is included to facilitate comparison between the s-plane and z-plane. This relation implies the following mapping between the s-plane and z-plane:

$$s \leftrightarrow \frac{1}{T}(z-1) \tag{15b}$$

Some understanding of the effect of this transformation on the frequency response can be made by a comparison with the impulse invariant (I.I.) transformation [22]. This transform preserves the frequency response (is aliasing is unimportant) by requiring that a pole, s_k in the s-plane, transform to a pole in the z-plane at $(z_k)_{I.I.} = e^{s_k T}$. From Eq.(15b), it is seen that the use of switched capacitor (S.C.) integrators in place of continuous time integrators would yield a z-plane pole at $(z_k)_{S.C.} = Ts_k+1$. The difference between the two pole positions $(z_k)_{I.I.}$ and $(z_k)_{S.C.}$ is given by

$$(z_k)_{I.I.} - (z_k)_{S.C.} = e^{s_k T} - (Ts_k+1) = \frac{(s_k T)^2}{2} + \frac{(s_k T)^3}{6} + \ldots \tag{16}$$

This discrepancy implies that there is pole movement due to the integrators, since the transform in Eq. (15b) simply moves the continuous time pole over in the z-plane by 1 unit. It can be seen that for high Q poles, the error due to time delays will be severe since the poles will be shifted closer than required to the unit circle. There is even the possibility of an unstable condition occurring when transformed poles move outside the unit circle. Fig. 13 illustrates these conditions.

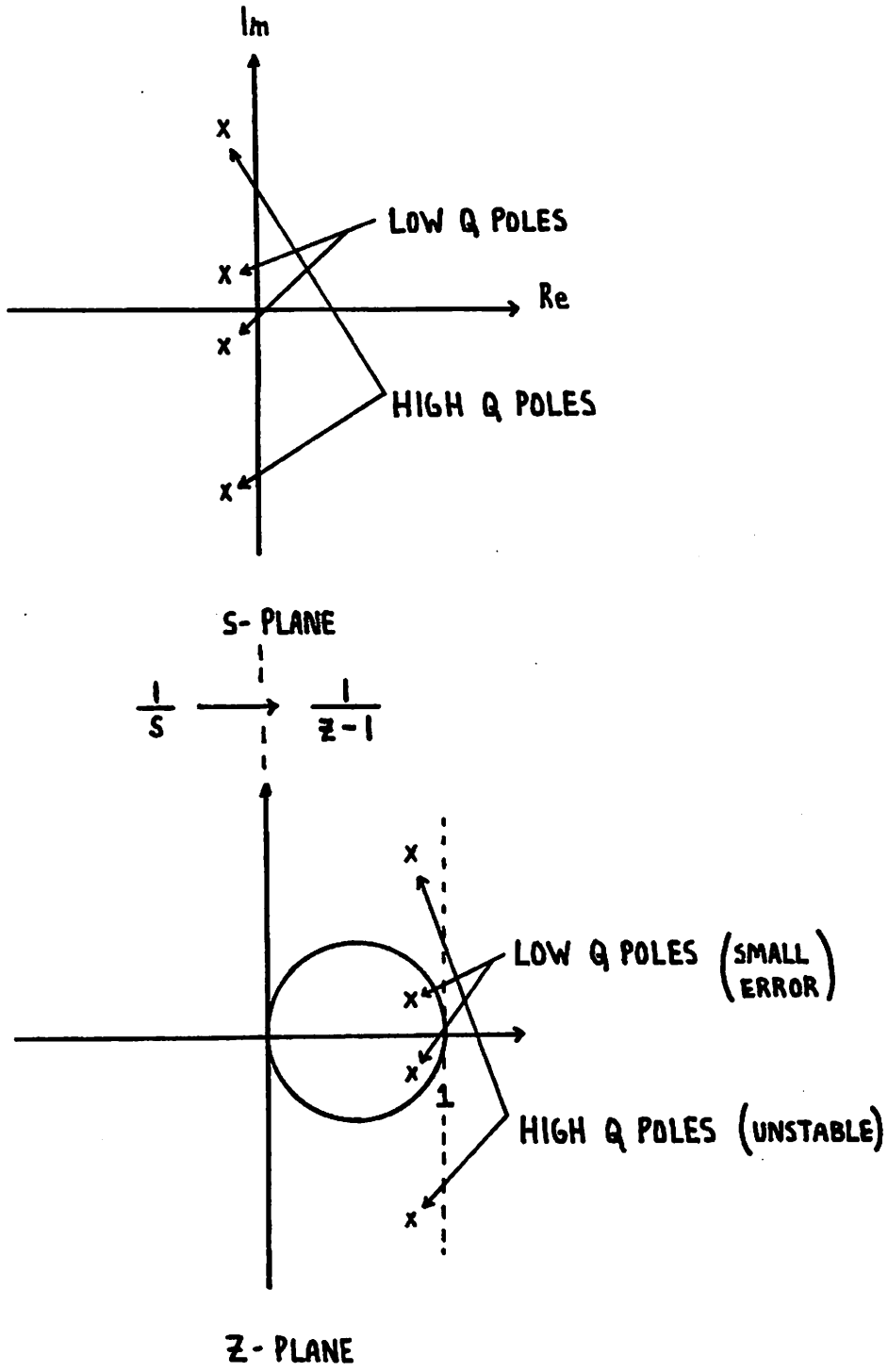


Fig.13 Transform performed on s-plane poles by sampled data integrator in Fig.3(c)

The sampling period can be adjusted to help the problem of pole movement. A smaller T (higher sampling rate) will yield less error due to the fact that higher order terms in $s_k T$ in equation (16) will decrease in importance. An alternate method for obtaining the correct filter transfer function would be to pre-distort the poles before implementation. However, the predistorted network, although yielding the desired transfer function, will not have the same sensitivity characteristics as the original doubly terminated prototype [18]. It has been observed that the predistortion technique causes the sensitivity to component variation to rise significantly [19].

1) "Direct Transform" Integrator [20]

The recent work of Bruton [20,21] on digital filters offers some very simple solutions to the problem of pole movement in what he terms as the "Discrete Transform Digital Integrator" (D.D.I.) which was discussed above. The error of the transform as described by Eqns. (15) and (16) can be related to excess phase shift in the integrators which is analagous to a loss term in the inductive or capacitive element being simulated. The pole of a lossy integrator moves off the origin out onto the negative real axis. This is equivalent to a small magnitude error and phase shift in the integrator transfer function as shown in Eq. (17):

LOSSY INTEGRATOR:

$$I(j\omega) = \frac{1}{(j\omega+a)} = \frac{1}{j\omega} \times \frac{1}{(1-j\frac{a}{\omega})} = \frac{1}{j\omega}[1+(j\frac{a}{\omega} - \frac{a^2}{\omega^2} + \ldots)] \qquad (17)$$

The expansion terms in the parenthesis in Eq. (17) may be considered the "error" terms of the integrator if lossless properties are desired.

The first order term $j(\frac{a}{\omega})$ results in an excess phase shift through the integrator while the second order term $-(\frac{a}{\omega}^2)$ corresponds to a fractional magnitude error in the integrator transfer function. While higher odd order terms contribute to phase shift and higher even order terms contribute to magnitude error, their effect is usually negligible with respect to the terms shown in the equation.

The switched capacitor integrator described by Eq. (7) may be examined for similar properties by letting $z = e^{j\omega T}$. It is found that for

$$I(z) = \frac{T}{z-1},\ I(z)\Big|_{z=e^{j\omega T}} = \frac{T}{(e^{j\omega T}-1)} = \frac{T}{j\omega T}\, e^{-j\omega T/2}\left(\frac{\omega T}{2\sin\omega T/2}\right)$$

$$\approx \frac{1}{j\omega}\left(1 - \frac{j\omega T}{2} - \frac{\omega^2 T^2}{4} + \ldots\right) \qquad (18)$$

Thus, the "direct transform" integrator shows a frequency response that is characteristic of a lossy continuous time integrator (Eq. 17) where the terms $-\frac{j\omega T}{2}$ and $-\frac{\omega^2 T^2}{4}$ in Eq. (18) relate to phase shift and magnitude error respectively.

2) "Lossless Digital Integrator" (L.D.I.) [20]

Using this information, Bruton modified his digital integrators to eliminate excess phase shift [20]. This was accomplished by a mathematical frequency scaling of the network elements by $e^{-sT/2}$ or one half delay. All integrator transfer functions are affected by the scaling such that their delays are reduced by one half clock period. The mapping from the s-plane to the z-plane as studied previously in Eq. (15) is modified by the scaling such that:

$$\frac{1}{s} \Leftrightarrow \frac{z^{-1}}{1-z^{-1}} \times z^{1/2} = \frac{z^{-1/2}}{1-z^{-1}} = \frac{z^{1/2}}{z-1} \qquad (19a)$$

$$s \leftrightarrow \frac{z-1}{z^{1/2}} = z^{1/2} - z^{-1/2} \tag{19b}$$

The effects of the scaling on the integrator frequency response are demonstrated using the same procedure as in Eq. (18)

$$I(z) = \frac{Tz^{1/2}}{z-1} = \frac{T}{z^{1/2}-z^{-1/2}}, \quad I(z)\Big|_{z=e^{j\omega T}} = \frac{T}{e^{j\omega T/2}-e^{-j\omega T/2}}$$

$$= \frac{T}{2j \sin \omega T/2} = \frac{1}{j\omega}\left[\frac{\omega T}{2 \sin \omega T/2}\right] \tag{20}$$

All terms contributing to phase shift have vanished in Eq. (20) thus reducing pole movement greatly. Notice that the term remaining does correspond to a magnitude error in the integrators but, the doubly terminated ladder was originally chosen for its zero sensitivity to these errors in the passband.

The thought of subtracting half delays from each integrator may seem awesome in terms of hardware, however, fortunately, this alteration requires nothing more than changing the ϕ and $\bar{\phi}$ phasing of the switches on adjacent integrators. Referring to Fig. 14, using two "building block" integrators to implement this ladder section results in identical switching schemes for each section. This corresponds to the input switch of op amp 2 switching with action "a", i.e., towards the amplifier at the same time as the switches of op amp 1. The delay around the two-integrator loop is equal to two clock periods. Assuming ideal op amps, the output of integrator 1 is available as soon as its switches close into the op amp, or after one-half clock period. By inverting the phasing of the switch on integrator 2, as shown by action "b" in Fig. 14 , the signal at the output of integrator 1 is picked up after one-half clock period and the effective delay is reduced.

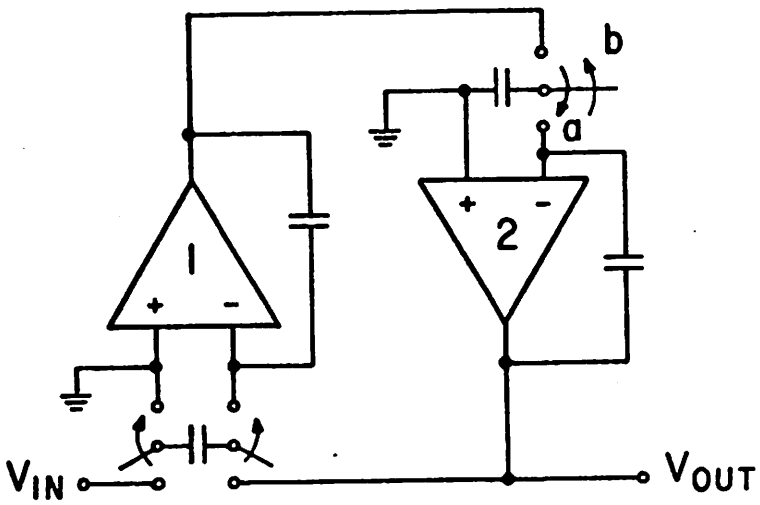


Fig.14 Switch phasing for D.D.I. integrators(a) and L.D.I. integrators(b) on simple ladder section

The loop delay is now one clock period as required by the L.D.I.. This idea may be extended to any length ladder such that when any amplifier is integrating, the stages that are fed by that integrator are switched so as to pick up the signal at its output.

The dramatic result of switching clock phases to implement L.D.I. integrators is shown in the spectrum analyzer photo of Fig. 15. Here the fourth order Butterworth example presented in section IIIB was breadboarded using the circuit of Fig. 12 and discrete analog switches, op amps, and capacitors. The top trace shows the peaked transfer function of the circuit when all switch phases are the same (D.D.I.). The bottom flat trace exhibits the desired Butterworth response and was taken after changing clock phasing on every other stage. Note that the phase shift in the (D.D.I.) is such that it corresponds to a "negative loss" in the elements yielding peaking in the transfer function.

The frequency scaling by $e^{-sT/2}$ of the network does not affect the resistive terminations. The terminations appear as lossy L.D.I. integrators at either end of the ladder. The z-representation of a lossy L.D.I. integrator is given in Fig.16a. Unfortunately, the process of adjusting switch phasing breaks down when implementation of Fig.16a is attempted. There is no way to achieve a half-delay around the termination loop using the circuit of Fig.16b. As is, the circuit simulates a termination of $Re^{-sT/2}$ ohms. The effect of terminating the network with this impedance rather than a pure resistance is usually negligible as long as the clock period is small compared to the frequencies passed by the filter. This statement will be verified with experimental results in section VIII.

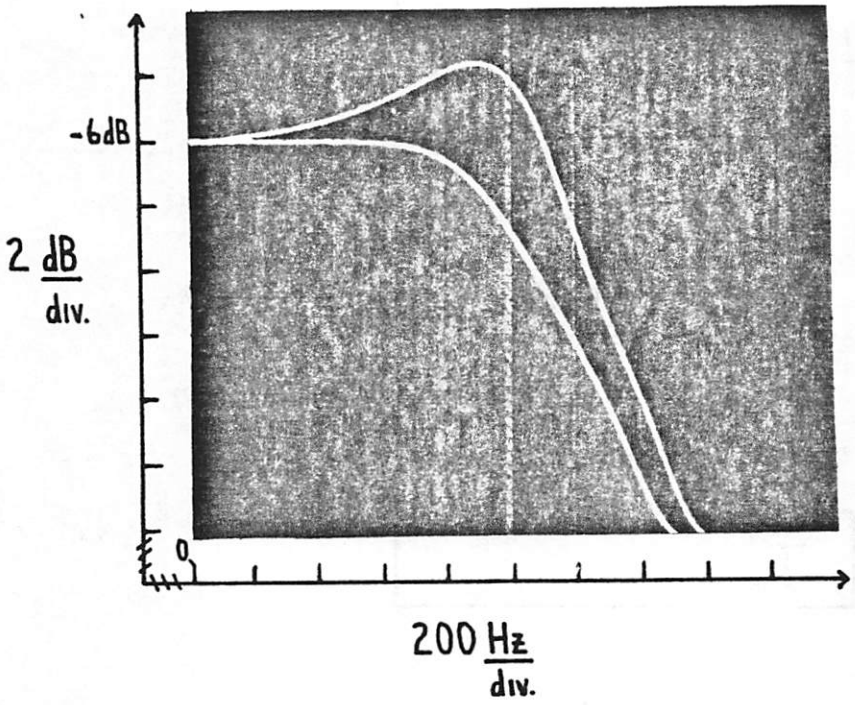
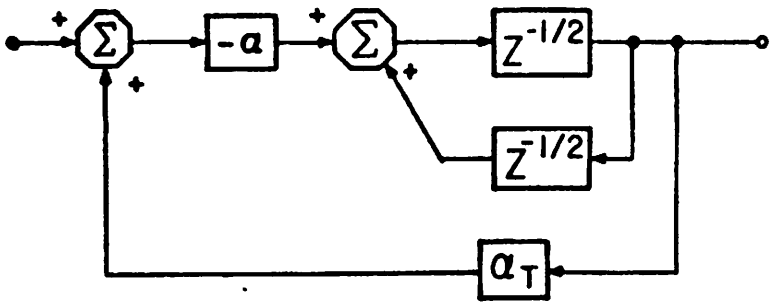
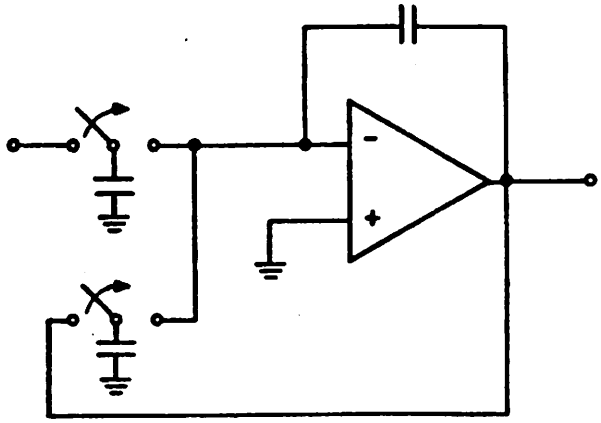


Fig.15 Passband of fourth order Butterworth switched capacitor filter
-top trace: D.D.I. integrators
-bottom trace: L.D.I. integrators



(a)



(b)

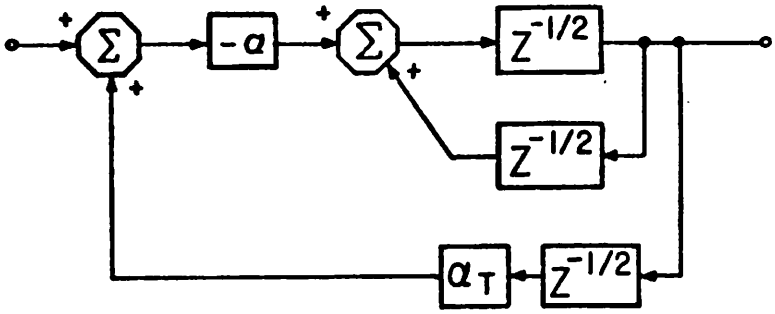


Fig.16 a) Z-transform block diagram of lossy L.D.I. integrator
b) Circuit implementation of lossy integrator and its z-transform block diagram showing extra ½ delay

By slightly altering the switched capacitor circuit and using the L.D.I. method, the simplicity of design for the switched capacitor filters is maintained. Well documented classical filter tables provide the necessary information for obtaining the capacitor ratios for a given desired frequency response.

V. THE ADDITION OF TRANSMISSION ZEROES TO FILTER RESPONSE

The addition of transmission zeroes to a ladder filter response has great importance in many filter applications. The zero addition is easily accomplished on the RLC lowpass prototype by adding feedthrough capacitors across the series arms of the ladder network as in Fig. 17 Imaginary axis zero locations are the resonant frequencies of the series L-C arms. The flow diagram for this non-canonical network is not as straightforward as the simple lowpass case. The approach to flow diagram construction of this circuit taken by the reference [17] is suitable only for continuous time active RC implementation as it contains voltage attenuators (multiplications) separate from op amp integrators. As will be shown, it is desirable to avoid multiplicative constants in a switched capacitor implementation that are not included with the integrations. In addition, op amps should also be kept to a minimum for die size considerations in the IC.

In order to design a switched capacitor elliptic network it is necessary to examine in detail the operations that are performed by the added feedthrough capacitors to the lowpass ladder structure. An understanding of their circuit function will uncover a simple technique for their incorporation into the circuit. Referring to Fig. 18a, a

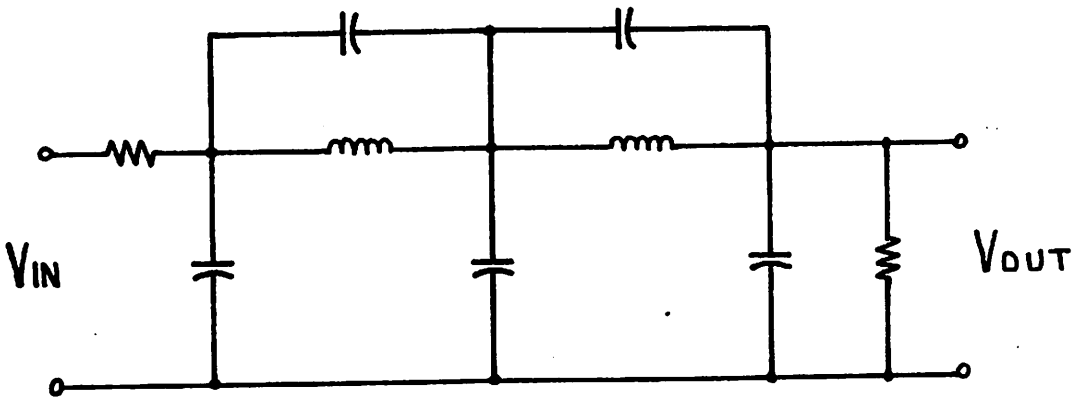


Fig.17 Doubly terminated lowpass ladder
with transmission zeroes

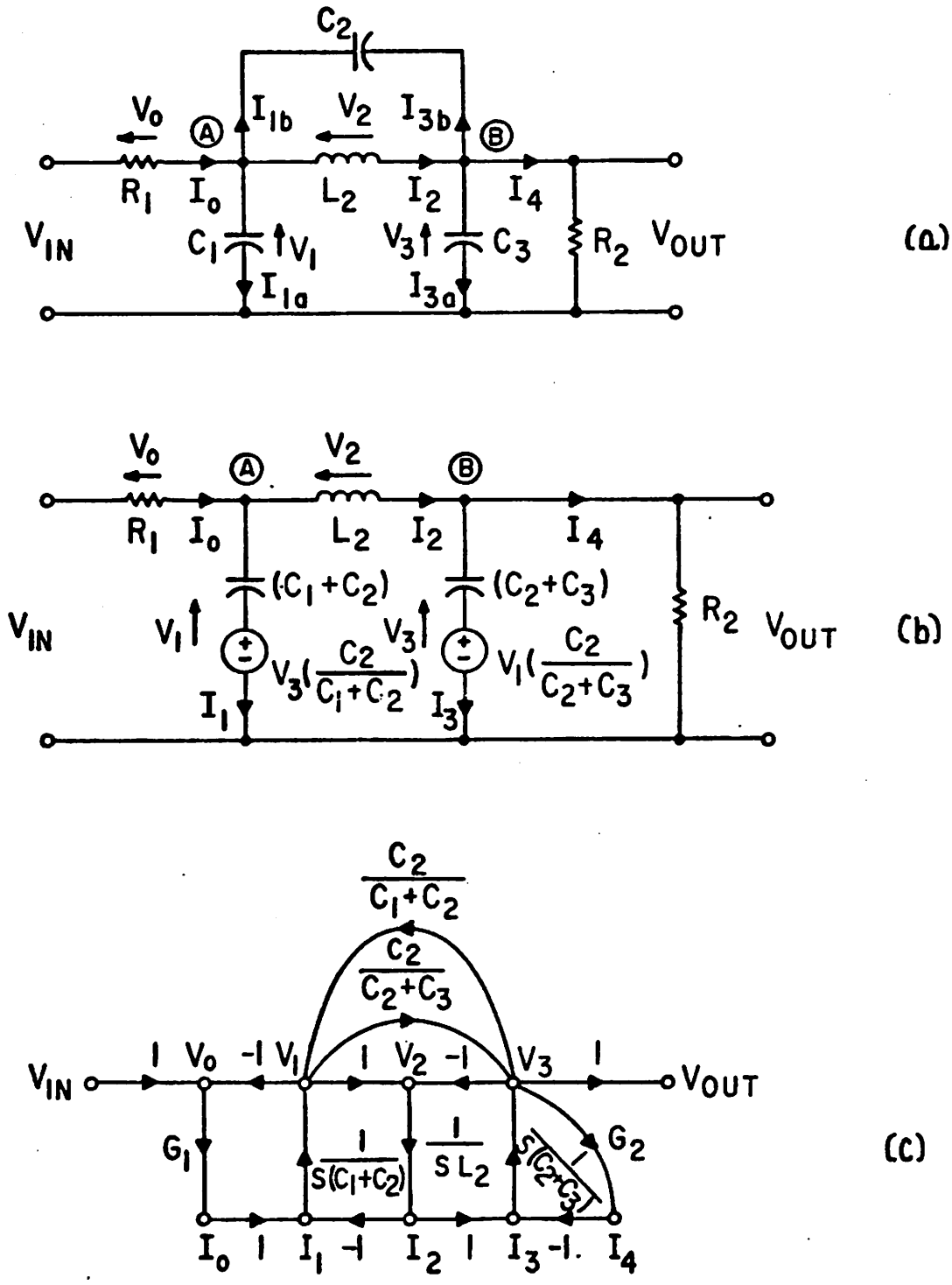


Fig.18 a) 3 pole - 2 zero lowpass ladder
b) equivalent circuit of (a)
c) flow-diagram of (b)

3 pole, 2 zero RLC filter is shown with voltages and currents defined. Using Kirchoff's current law at nodes A and B, the following equations are derived to explain the function of C_2. This is shown symbolically in Fig.18c and the equivalent circuit is given in Fig.18b.

Node A $\quad I_o - I_2 - C_1 V_1 s - C_2(V_1 - V_3)s = 0$

$$V_1 = \frac{(I_o - I_2)}{s(C_1+C_2)} + V_3\left(\frac{C_2}{C_1+C_2}\right) \qquad (21)$$

FEEDBACK

Node B $\quad I_2 - I_4 - C_3 V_3 s - C_2(V_3 - V_1)s = 0$

$$V_3 = \frac{(I_2 - I_4)}{s(C_2+C_3)} + V_1\left(\frac{C_2}{C_2+C_3}\right) \qquad (22)$$

FEEDFORWARD

Thus, C_2 has been identified as an element that feeds some of the voltage V_3 to node V_1 and vice-versa. As illustrated in Fig.18c, in order to implement a transmission zero pair, it is necessary to change the integrator time constants that represent shunt capacitors in the lowpass case to account for the feedthrough capacitor. This action along with creating the feedforward and feedback paths described completely simulates the added series capacitance.

In a switched capacitor implementation, the integrator time constants are easily changed by adjusting their capacitor ratios. However, the new paths linking V_1 and V_3 (of Fig. 18) present a problem because both voltages are op amp outputs and are not suitable for adding without using an additional amplifier. Fig. 19 shows a circuit to achieve the addition without extra op amp stages. The circuit performs a standard sampled data integration on V_{IN} but, in addition, continuously multiplies

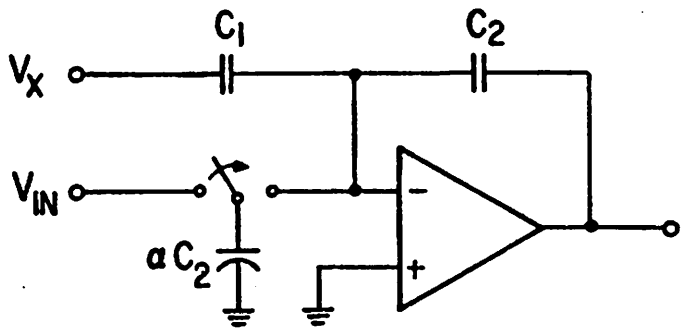


Fig.19 Switched capacitor integrator/summer

V_x by a constant and sums it to the output. Since C_1 and C_2 are held to a virtual ground on one side by the op amp, C_1 charges to $q_1 = C_1 V_x$ and the output due to V_x is given by,

$$V_{out} = -\frac{q_1}{C_2} = -(\frac{C_1}{C_2})V_x. \qquad (23)$$

Although the summation is continuous, in the filter, V_x wll be derived from another integrator whose output changes only once every clock cycle. The D.C. bias point of an op amp summer which uses capacitors to determine the gain is unstable due to thermal and surface leakage currents which result in excess charge build-up at the inverting input. However, the presence of the switched capacitor "resistor" (αC_2 in Fig. 19) which is connected to a voltage source V_{IN}, provides an exit path for the excess charge thereby stabilizing the summer. Using the integrator/summer in place of the conventional integrators for C_1 and C_3 (now (C_1+C_2) and (C_2+C_3)) in Fig. 18c, allows the necessary additions at nodes V_1 and V_3. Since the summations can only be brought in with a sign inversion, some minor modifications must be made to the flow diagram. For example, if node V_1, the output of an op amp, must contain a fraction of another node voltage V_3, the two voltages must be of opposite sign on the flow diagram. The reason for this lies in the fact that V_3 is brought into the negative input of the op amp feeding V_1 and its sign is inverted in the summation. This situation is illustrated in Fig. 20.

The method described above for obtaining transmission zeroes requires very little hardware over the all pole filter circuit. The example chosen to demonstrate the design methods of this section is a

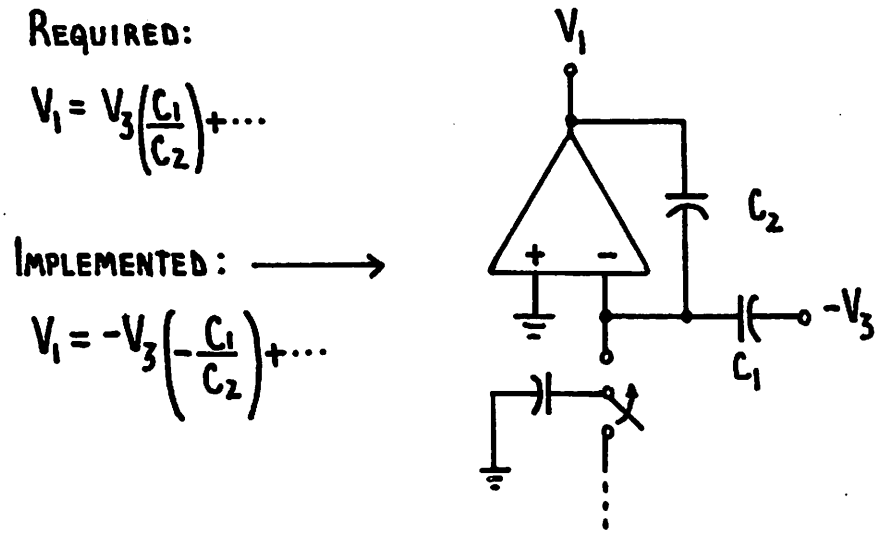


Fig.20 Method of implementing feedforward and feedback on lowpass ladder with transmission zeros

fifth order elliptic filter. The RLC network contains 7 energy storing devices. The final switched capacitor circuit requires only 5 operational amplifiers. In addition, 4 switches and 6 extra capacitors are required over the simple lowpass structure. Fig. 21 shows the network, its corresponding flow diagram, and the switched capacitor circuit.

VI. NOISE IN SWITCHED CAPACITOR FILTERS

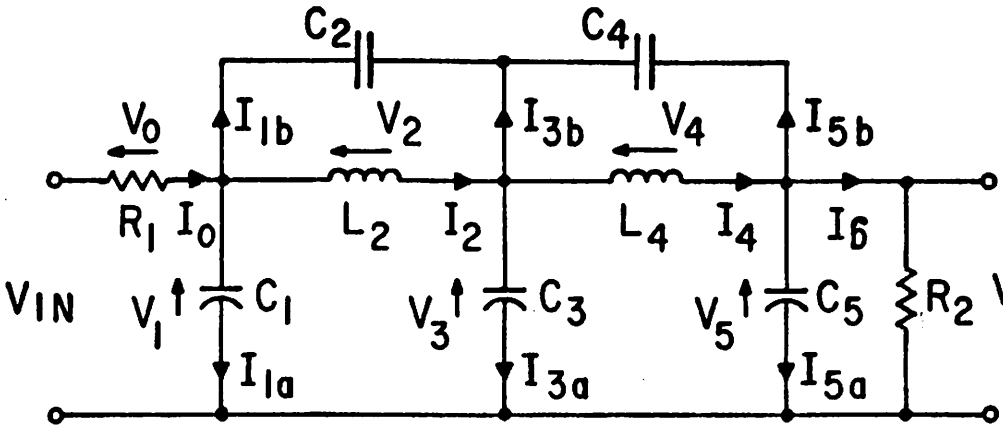
The switched capacitor simulation of a passive RLC network contains noise sources that are not found in the prototype. In order to predict the noise performance of a filter, the individual noise contributing sources must first be isolated, and then reflected to the output (or input). The noise model used in this paper treats the switched capacitor integrator as a building block cell for the filter. The noise properties of the integrator cell, as characterized in this section, may be specified for a particular filter where a complete noise analysis is then performed.

A. Noise Sources

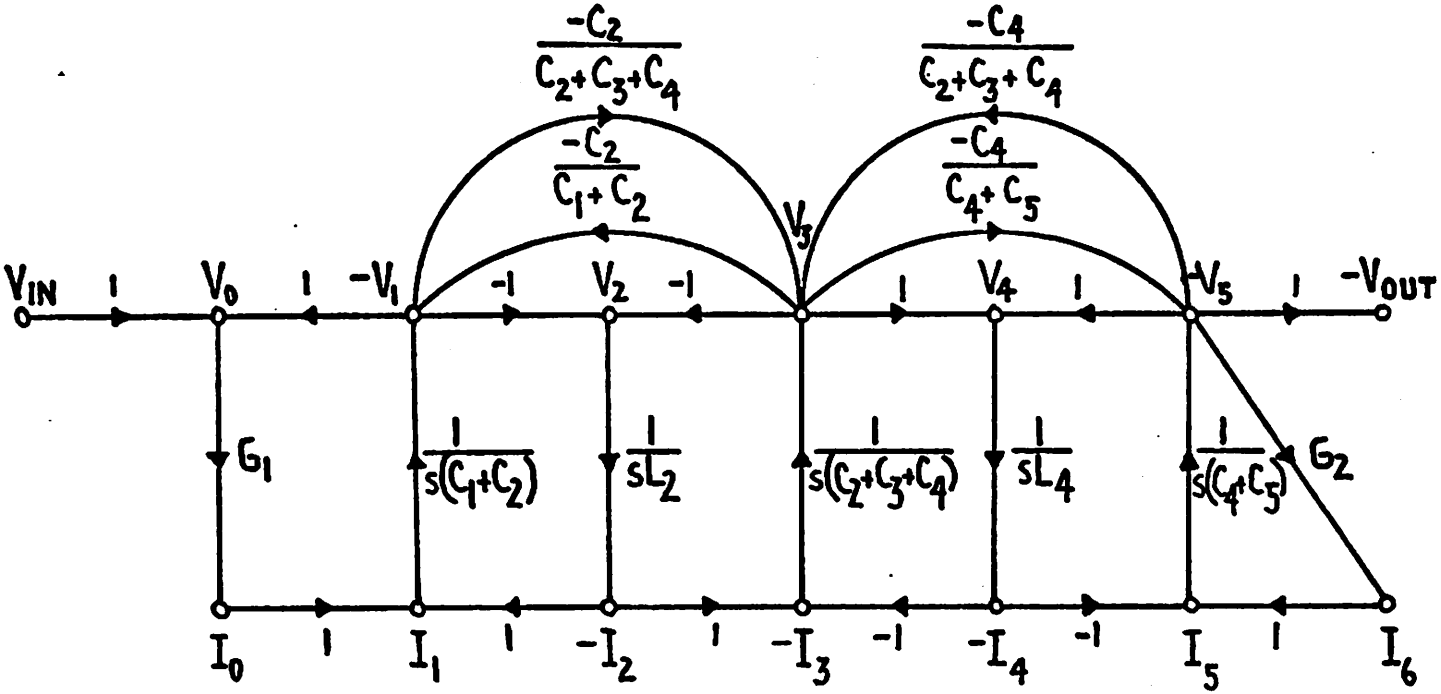
For each integrator, two main noise sources are isolated relating to 1) the "on" resistance of the MOS switches, and 2) the r.m.s. noise of the operational amplifier:

1. Switched Capacitors

Every operational amplifier integrator in the filter circuit is fed by one or several switched capacitor "resistors" at its input. The switched capacitor, as shown in Fig.1b, is constructed with two MOS transistors which alternately switch "on" and "off". The resistance of the switch channels has an associated thermal noise voltage which gets sampled on to the capacitor. The resistance however, also forms a single



(a)



(b)

Fig.21 a) Five pole - four zero lowpass ladder
b) Flow-diagram of (a)
(continued)

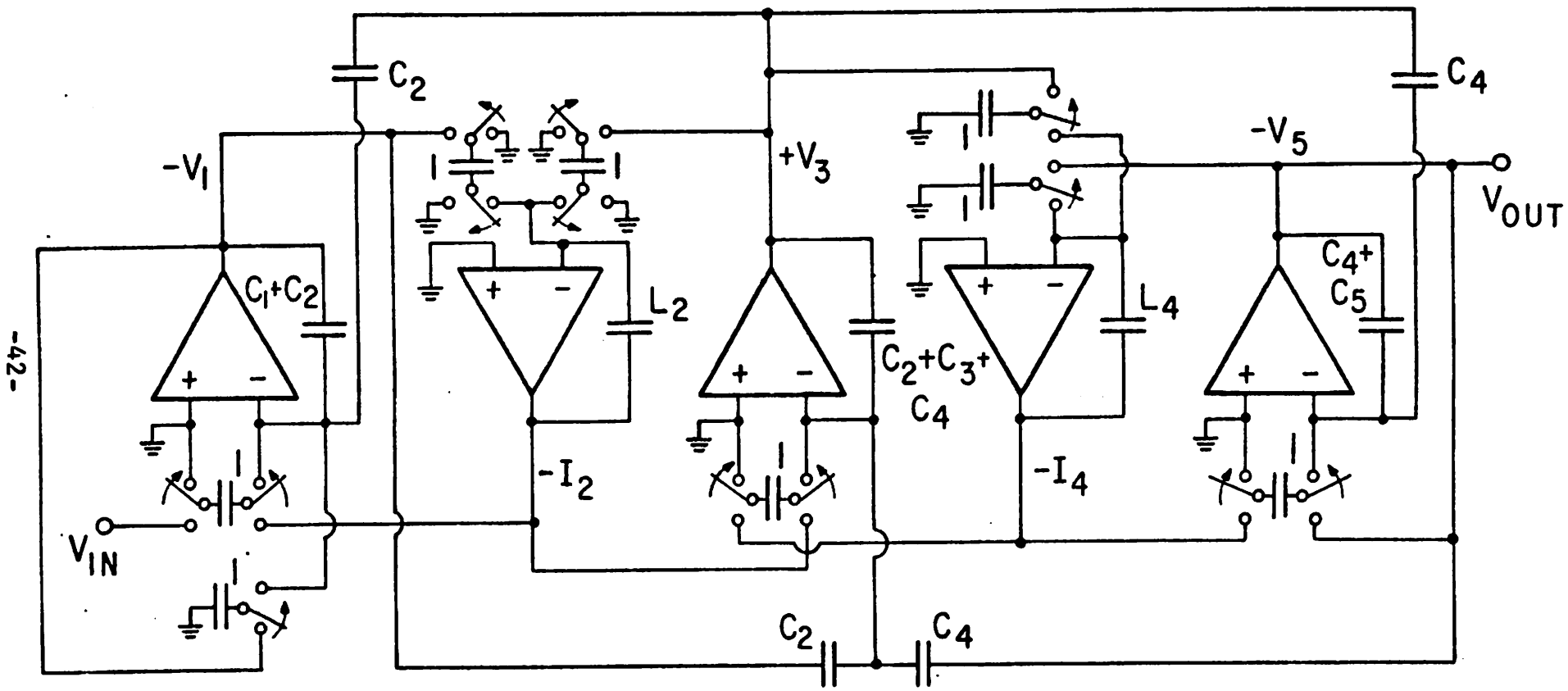


Fig.21(c) Switched capacitor circuit of Fig.21(a)

pole lowpass RC filter with the capacitor and therefore band-limits the noise. The noise power spectral density due to the "on" resistance of a switch is

$$v_n^2 = 4kTR \tag{24}$$

where R = "on" resistance of channel

k = Boltzmann's constant

T = Temperature in °K

The noise spectral density that is stored on the capacitor therefore is

$$v_{nc}^2 = 4kTR|H(f)|^2 \text{ where} \tag{25a}$$

$$|H(f)|^2 = \left[\frac{1}{1+(2\pi fRC)^2}\right] \tag{25b}$$

RC filter transfer function

Integrating Eq. (25a) over all frequencies yields the squared r.m.s. noise voltage associated with the switched capacitor [24]. This is done in Eq. (26):

$$v^2_{\substack{rms \\ capacitor}} = \int_{-\infty}^{\infty} 4kTR|H(f)|^2 df = 4kTR\left(\frac{1}{4RC}\right) = \frac{KT}{C} \tag{26}$$

Using the information of Eqs. (24)-(26), two cases must be examined for the switched capacitor integrator as shown in Fig. 22. They are the noise contributions for when each of M_1 and M_2 is switched "on" while the opposing transistor is "off".

When ϕ is high, M_1 is "on" and the noise voltage sampled onto C_1 is given in Eq. (25) with $R = RM_1$, the channel resistance of M_1. The noise contribution of M_2 should also be mentioned. If M_2 is modelled as a large resistance in the off state, then its noise voltage will also be large, but the bandwidth of the RC filter formed by M_2 and C_1

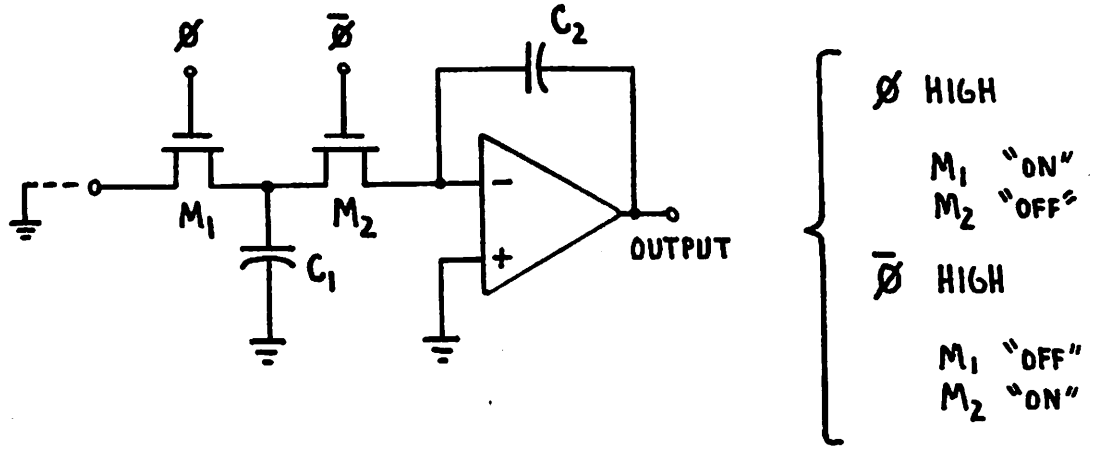


Fig.22 Circuit used to calculate noise of input switched capacitor "resistor" on sampled data integrator

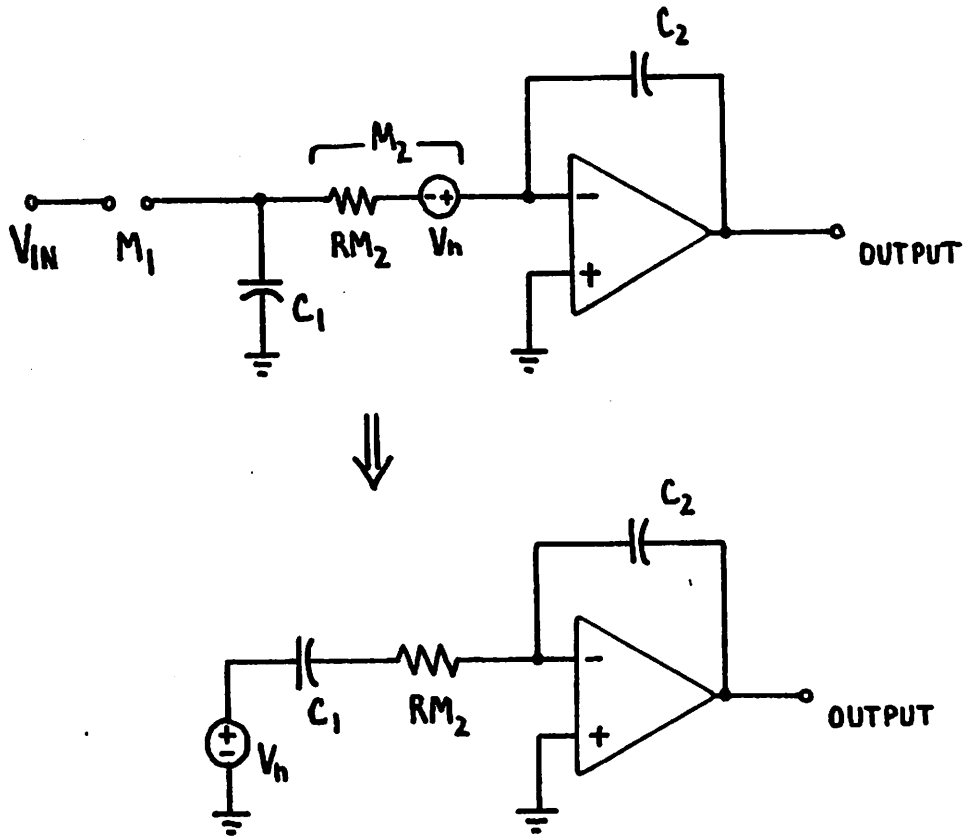


Fig.23 Equivalent circuit of Fig.22 when $\bar{\phi}$ is high

will be extremely small. The noise, when eventually passed through the integrator would appear as a slowly varying offset voltage on the output and this effect will not be considered further. The gain of the integrator with M_2 in the "off" state is very close to zero, so the noise voltages generated in either transistor are not transmitted directly to the output during this half clock cycle.

When $\bar{\phi}$ goes high, the charge on C_1 due to the noise of M_1 is integrated and appears at the output with squared r.m.s. value shown in Eq. (26) times the gain C_1/C_2 of the integrator. Neglecting the effects of M_1 in the "off" state for the reasons explained above, the remaining noise source is the "on" resistance RM_2 of the channel of switch M_2. The equivalent circuit for this state is shown in Fig. 23 The noise voltage v_n that is sampled onto C_1 is unimportant since it is lost at the next half clock cycle when V_{in} is switched back in and charges C_1 to a new value. The gain from v_n to the output when $\bar{\phi}$ is high is not zero and therefore must be considered. Exercising the virtual ground method for ideal gain calculations, the transfer function between v_n and the output as shown in Fig. 23 is found to be:

$$\frac{v_{output}}{v_n} = \frac{-(C_1/C_2)}{RM_2C_1s+1} \quad \begin{matrix}\text{ideal}\\ \text{op}\\ \text{amp}\end{matrix} \tag{27}$$

The noise due to M_2 appearing at the output of an ideal op amp would therefore be band-limited only by the RM_2C_1 filter time constant ($=RM_1C_1$ for identical M_1 and M_2 transistors). However, in reality, if the compensation of the op amp band-limits before the frequency $1/2\pi RM_2C_1$, then the noise bandwidth of v_n at the output would simply be the bandwidth

of the op amp with gain (C_1/C_2). In most cases, the ratio of the op amp bandwidth to that of the RM_2C_1 filter is small and the contribution of transistor M_2 to the total noise at the integrator output may be neglected.

Thus, the contribution of any one switched capacitor C feeding an integrator may be represented as an r.m.s. voltage source of value

$$v_{\substack{\text{rms} \\ \text{capacitor} \\ \text{noise}}} = \sqrt{\frac{KT}{C}} \qquad (28)$$

in series with its input voltage.

2. Operational Amplifiers

The operational amplifier is an active circuit with many noise sources present. For the analysis of an operational amplifier connected as a building block integrator however, it is sufficient to consider the noise of the amplifier as a whole. This requires some knowledge of the amplifier design beforehand and it is assumed here that the designer has a good idea of what the r.m.s. noise voltage of the op amp will be and, that an MOS amplifier which has negligible input noise currents is used. In order to analyze the complete integrator, the equivalent r.m.s. noise voltage of the op amp is reflected to a single input as shown in Fig. 24. The generator $v_{n\text{-rms}}$ represents the sum of the noise powers due to noise sources at both inputs.

The switching action of the input capacitors periodically changes the feedback around the op amp and therefore the gain. When the switches are out, i.e., away from the op amp, the gain that the noise generator sees is unity since the open switch terminals at the input represent a very large resistance. When the switches toggle, the gain of the

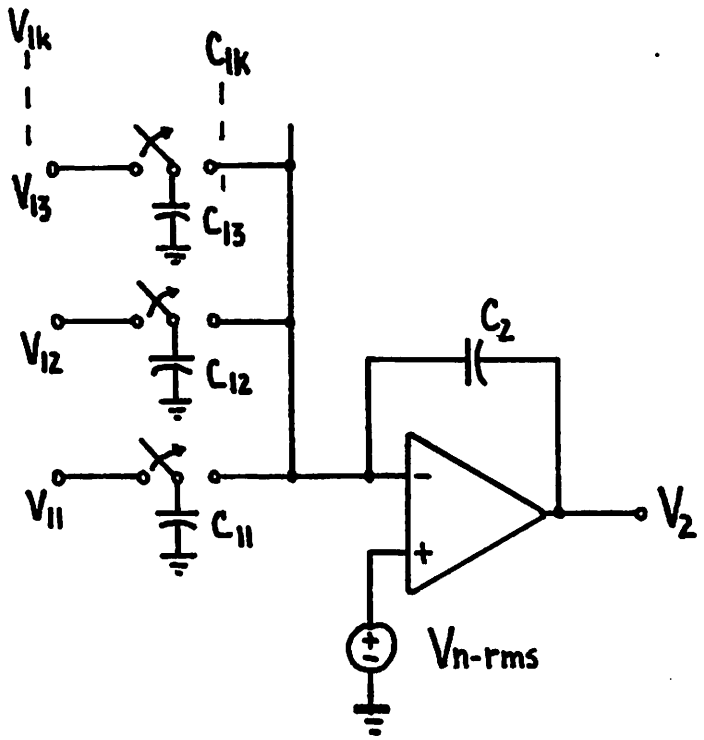


Fig.24 Circuit used to calculate noise of op amp in sampled data integrator

op amp for the noise generator changes to

$$\alpha_n = 1 + \frac{\sum_{i=1}^{k} C_{1i}}{C_2} \tag{29}$$

where k = number of input capacitors. This is the only time when the next stage will be sampling the output of the operational amplifier in an L.D.I. filter configuration. Therefore, the total r.m.s. operational amplifier noise voltage can be represented as a generator of value

$$v_{\substack{rms \\ op\ amp}} = \left[1 + \frac{\sum_{i=1}^{k} C_{1i}}{C_2} \right] v_{n\text{-}rms} \tag{30}$$

in series with the output voltage.

B. Analysis of Noise in Complete Filter

In the last section, the noise sources of a single switched capacitor integrator were identified. These sources may now be specified for the integrators of a switched capacitor filter. In order to characterize the noise of the entire filter, it is necessary to calculate the effect that each noise source located in the circuit has on the total noise at the output. For example, assume that noise source v_{rms_1} feeds node x of a circuit. The spectral density noise of v_{rms_1} is simply $v_{rms_1}/f_c^{1/2}$ for a sampled data system, where f_c is the sampling rate. Therefore, the output spectral density noise due to v_{rms_1} is

$$v_{OSD_1} = |T(j\omega)| \frac{v_{rms_1}}{f_c^{1/2}} \tag{31}$$

where $T(j\omega)$ is the transfer function between node x and the output. Using an all voltage flow-diagram or a symbolic representation of the filter circuit, one can add in the noise sources at appropriate

nodes and then find the transfer functions from each node to the output using Mason's Gain Formula [25] or an equivalent method. The feedback loops remain unaltered in the circuit implying that the denominator of the transfer functions between all internal nodes and the output will be the same as that of the original filter transfer function. An example of this analysis will be presented in Section VII.

VII. TERMINATION EFFECTS

The termination resistances of a ladder filter are simulated by negative feedback paths with appropriate gain constants in the active implementation. In contrast to the continuous time filter, the simulated resistances of the switched capacitor filter have little effect on the input and output impedances of the circuit. They are still an important choice however, because they have a direct effect on many other characteristics of the active filter performance.

A. Silicon Area

In order to implement termination reistances different from the RLC prototype (usually 1 ohm source and load resistors), a standard impedance scaling is performed. The scaling factor K_M changes <u>all</u> of the impedances in the network but preserves the original transfer function of the filter. Each element of the network is scaled as shown below [2]:

Impedance Scaling

$$R_{NEW} = K_M R_{OLD} \tag{32a}$$

$$L_{NEW} = K_M L_{OLD} \tag{32b}$$

$$C_{NEW} = \frac{1}{KM} C_{OLD} \tag{32c}$$

The scaling procedure alters all of the integrator time constants representing elements in the active circuit. Since the time constants in switched capacitor filters are derived from capacitor ratios, any change will directly affect the silicon area required to construct the capacitors. In some cases, the total area needed to implement a filter may be reduced, but the inverse relation between the scaling direction of inductors and capacitors as shown above limits the usefulness of this technique. Aside from this, as will be seen in the next sections, other incentives for changing the termination resistances exist which may outweigh the disadvantages of a possible larger silicon area requirement.

B. Noise/Dynamic Range

The active ladder circuit models the state equations of a passive network exactly thus having the property that internal node voltages of the circuit are equal to voltage and current levels in the RLC network. As explained in Section III, the use of operational amplifier integrators implies that the active filter must be an "all voltage" circuit. Since both modelled voltages and currents appear as voltages (operational amplifier outputs), problems may be encountered due to the energy storing properties of the inductors and capacitors being simulated. For example, in a simulation of a parallel RLC tank circuit, one operational amplifier output voltage, V_I, represents the current in one of the energy storing elements. At resonance, voltage V_I will be equal to the circulating current of the tank which is Q times the voltage input across the tank for unity R. In high Q situations, the dynamic range of the filter suffers because the input voltage must be kept very low to avoid V_I from clipping at the supply voltage.

A scaling procedure to change terminations can often solve these problems. Intuitively, it can be seen that larger resistances on the RLC prototype would limit the current drawn from the input voltage. In the same way, an impedance scaling of the active network can reduce or increase the currents and therefore their representative voltages in the circuit. As an example, the 5 pole, 4 zero filter shown in Fig. 21 was breadboarded with both 1 ohm and 4 ohm terminations. The ripple was designed at 0.1dB for the passband of 0-3100Hz. Spectrum analyzer photos in Fig. 25 show the outputs of each of the five op amps - each representing a particular voltage of current in the circuit as shown. In Fig.25b, the two outputs representing currents have dropped 12dB due to the fourfold increase in termination resistances.

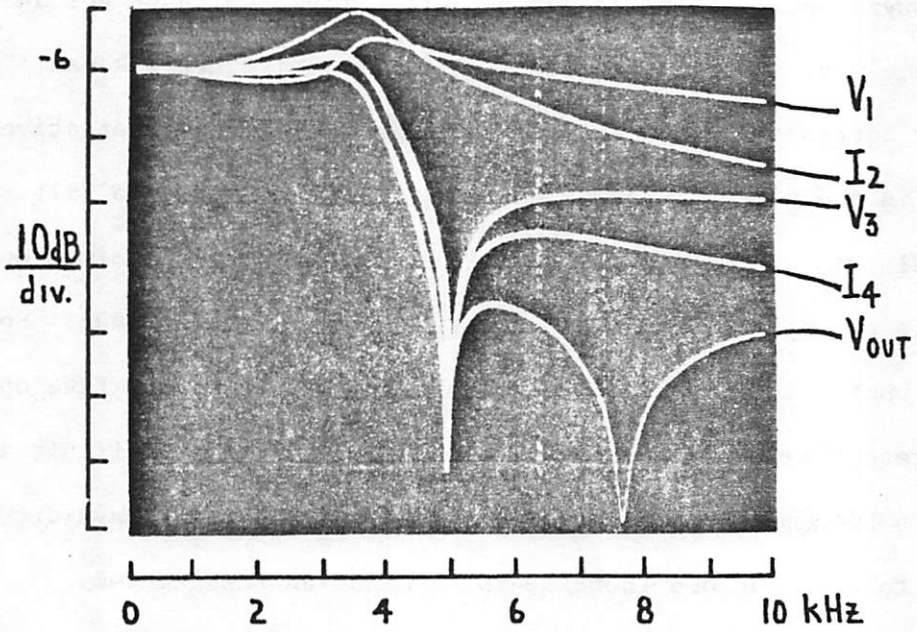
Care must be exercised when scaling impedances in a filter circuit. If the terminations are increased so as to cause the "current" node levels in the circuit to drop to the same order of magnitude as the noise level, then the advantages of the scaling may be outweighed by increased noise. In the same way, if the terminations are decreased, current node levels will eventually rise to a point where the input voltage must be kept so low to avoid saturation in the circuit that the dynamic range will again be severely decreased. For these reasons, there is often an optimum value for the terminations. An example showing the analysis of these properties follows.

C. Example: Effects of Termination Resistance on Silicon Area, Noise, and Integrator Gains of a Two Pole Bandpass Filter

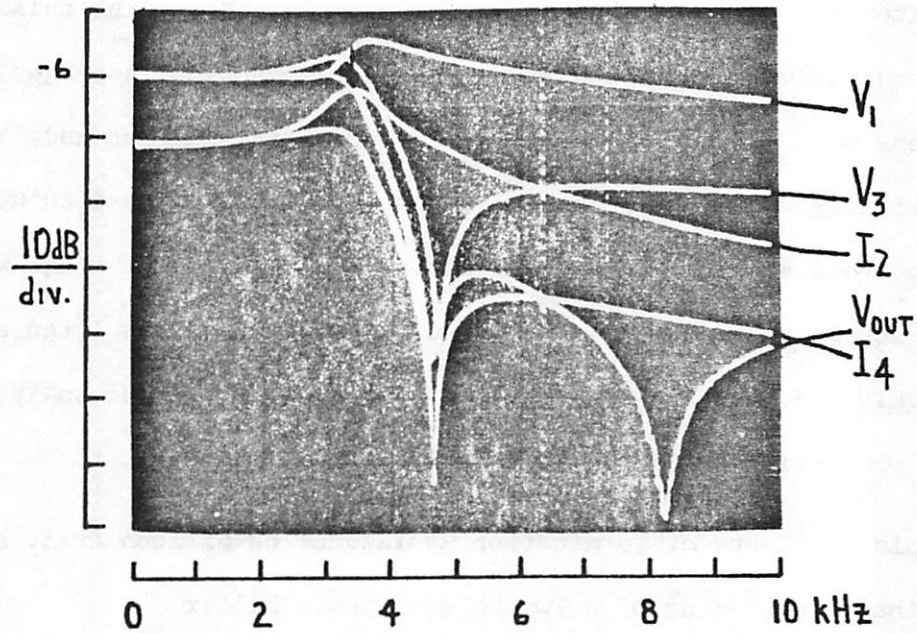
In order to demonstrate the trade-offs involved when choosing the termination resistances, a second order bandpass filter will be

CURRENT NODE SCALING

(SEE FIG. 21 FOR CIRCUIT)



$R_1 = R_2 = 1\Omega$



$R_1 = R_2 = 4\Omega$

Fig.25 Scaling of ladder termination resistances to reduce "current" node voltages in circuit

analyzed for its noise performance, silicon area of capacitors, and internal gains as a function of the terminations. Although generalizations can be made regarding the method of analysis, due to the complexity of the subject and the large amount of variables, specific results of the analysis are different for every filter.

The doubly terminated second order bandpass structure of Fig. 26 was studied.

1. Noise Sources

Using the noise models of Section VI, all sources of noise are first identified in the bandpass circuit. The switched capacitor circuit has been designed to be flexible in order to allow changes in termination. As shown in Fig.26d, the op amp integrator representing the capacitor and two resistors has an input for V_{IN}, termination feedback, and the output of the second integrator. The op amp integrator representing the inductor has a single input. For each input, there is an associated switched capacitor αC which adds an r.m.s. noise voltage $\sqrt{kT/\alpha C}$ to the voltage from which it is fed. The noise voltages of each switched capacitor are shown added at points $\alpha_i C$, $2\alpha_T C$, $\alpha_c C$, and $\alpha_L C$ of the symbolic diagram of Fig.26c. Note that the multipliers G_T and $2G_T$ are implemented within the first integrator.

Each of the two operational amplifiers of the bandpass circuit contributes an r.m.s. noise voltage as given in Eq. (30). Points 0_1 and 0_2 of Fig.26c represent those noise contributions being added to the circuit.

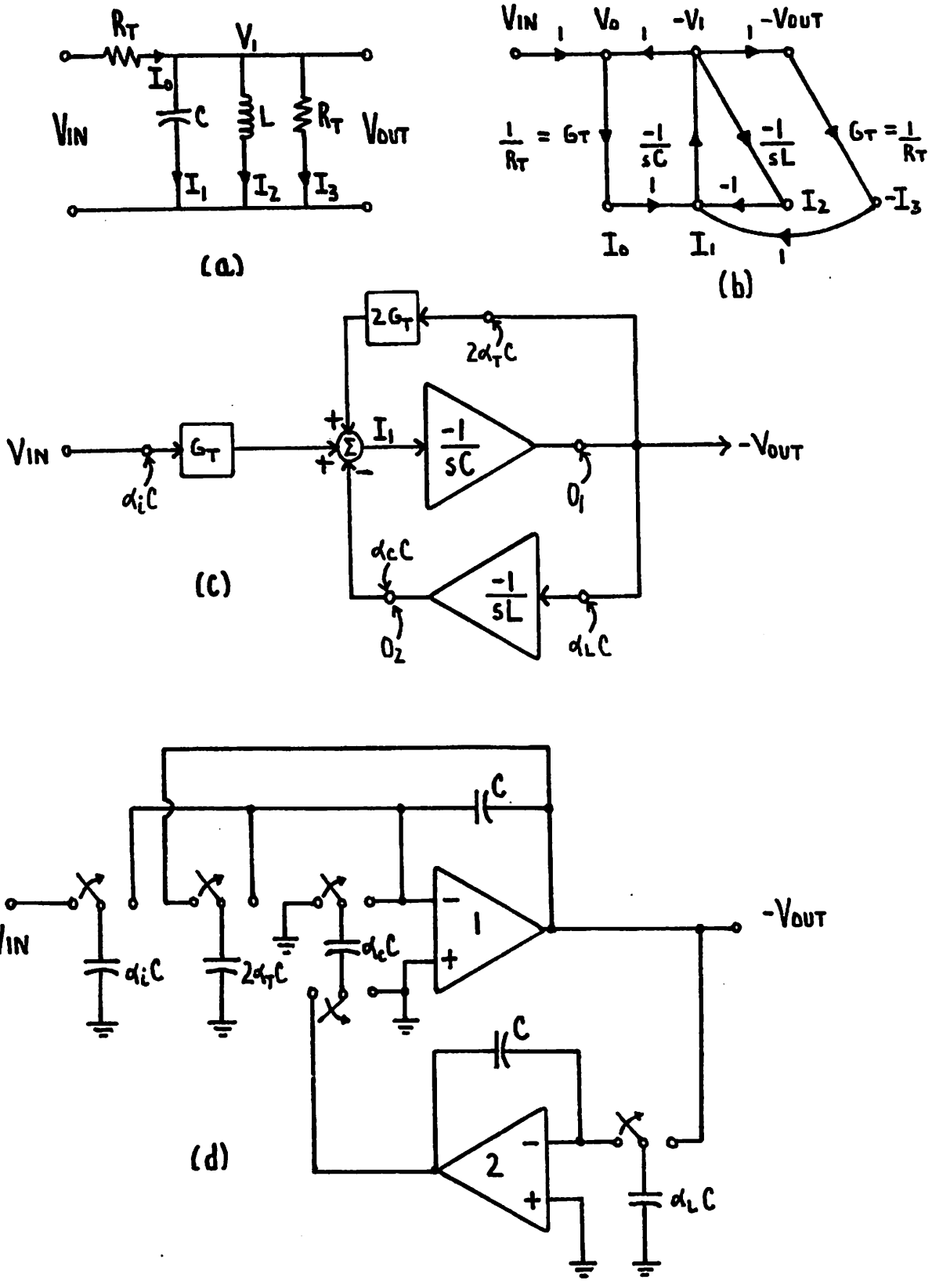


Fig.26 2-pole bandpass filter studied in example of Section VIIc a) RLC network b) flow-diagram c) symbolic representation with noise sources added d) switched capacitor circuit

2. Transfer Functions of Noise Sources to Output

Having identified the noise sources, it is necessary to calculate the transfer function from their locations in the circuit to the output. This is done using Mason's Gain Formula [25] and defining a forward path from each noise input to the filter output. Referring to Fig.26c, the loops and forward paths are found to be

Loops: $\frac{-1}{s^2CL}$

$\frac{-2G_T}{sC}$

$\Delta = 1 + \frac{1}{s^2CL} + \frac{2G_T}{sC}$

$= \frac{s^2CL+2LG_Ts+1}{s^2CL}$

Forward Paths

$FP_{\alpha_i C} = \frac{-G_T}{sC}$

$FP_{2\alpha_T C} = \frac{-2G_T}{sC}$

$FP_{\alpha_c C} = \frac{1}{sC}$

$FP_{\alpha_L C} = \frac{-1}{s^2CL}$

$FP_{0_1} = 1$

$FP_{0_2} = \frac{1}{sC}$

The denominator of the filter transfer function Δ is the same for each of the noise source transfer functions. The deletion of any of the forward paths shown breaks all feedback loops. Therefore, the transfer function of each noise source to the output is simply its corresponding forward path divided by Δ. Eqs. (33) below show the resulting transfer functions:

$$T(s)_{\alpha_i C} = \left(\frac{-G_T}{sC}\right)\left(\frac{1}{\Delta}\right) = \frac{-sLG_T}{s^2CL+2G_TLs+1} \qquad (33a)$$

$$T(s)_{2\alpha_T C} = \left(\frac{-2G_T}{sC}\right)\left(\frac{1}{\Delta}\right) = \frac{-sL2G_T}{s^2CL+2G_TLs+1} \qquad (33b)$$

$$T(s)_{\alpha_c C} = \left(\frac{1}{sC}\right)\left(\frac{1}{\Delta}\right) = \frac{sL}{s^2CL+2G_TLs+1} \tag{33c}$$

$$T(s)_{\alpha_L C} = \left(\frac{-1}{s^2CL}\right)\left(\frac{1}{\Delta}\right) = \frac{-1}{s^2CL+2G_TLs+1} \tag{33d}$$

$$T(s)_{0_1} = \left(\frac{1}{\Delta}\right) = \frac{s^2CL}{s^2CL+2G_TLs+1} \tag{33e}$$

$$T(s)_{0_2} = \left(\frac{1}{sC}\right)\left(\frac{1}{\Delta}\right) = \frac{sL}{s^2CL+2G_TLs+1} \tag{33f}$$

Most of the noise transfer functions of Eqs. (33) exhibit bandpass characteristics and it is safe to say that their cumulative effects will be at a maximum at the center frequency ω_o. This assertion will be verified experimentally later, but for the present, it allows a simplification of Eqs. (33). Evaluating each function at $\omega_o = \frac{1}{\sqrt{LC}}$ yields the following noise "gains" to the output from each source:

$$T(j\omega)_{\alpha_i C}\Big|_{\omega_o} = -\frac{1}{2} \tag{34a}$$

$$T(j\omega)_{2\alpha_T C}\Big|_{\omega_o} = -1 \tag{34b}$$

$$T(j\omega)_{\alpha_c C}\Big|_{\omega_o} = \frac{1}{2G_T} \tag{34c}$$

$$T(j\omega)_{\alpha_L C}\Big|_{\omega_o} = \frac{\sqrt{LC}}{j2G_TL} = -jQ \tag{34d}$$

$$T(j\omega)_{0_1}\Big|_{\omega_o} = \frac{jC}{2G_T\sqrt{LC}} = jQ \tag{34e}$$

$$T(j\omega)_{0_2}\Big|_{\omega_o} = \frac{1}{2G_T} \tag{34f}$$

The simple expressions above represent the gain each noise source will see at the center frequency when referenced to the output. In practice,

the sum effect of all noise sources will be found by adding the noise powers at the output. The power transfer function of each expression in Eqs. (34) is its magnitude squared which implies that the absolute value of the transfer function of Eqs. (34) may be used. Note that only (34c) and (34f) depend on the terminations.

3. Scaling Effects/Noise Expressions

As discussed earlier, the scaling of the terminations requires a change in the integrator time constants. The gain α through an integrator is the reciprocal of the time constant τ (scaled by f_c) and is equal to the ratio of the input switched capacitor to the feedback capacitor as shown in Fig. 3 Therefore, another consequence of scaling the terminations is that the gain of the integrator is changed and, this may be an important consideration depending on the open loop gain and compensation of the operational amplifiers. In most cases however, the size of the capacitors necessary to determine a ratio will be the limiting factor. For the example, the gain of integrator 1 (proportional to 1/C) will scale directly with $R_T = 1/G_T$ (see Fig.26) while the gain of integrator 2 (proportional to 1/L) will scale with an inverse relationship as given by Eq. (32). The relationship between V_{IN} and the output remains the same regardless of the termination scaling. This places interesting restrictions on the switched capacitor circuit in which gains are only introduced by integrators. Referring to Fig.27a, assume that the integrator gain must be scaled up for input V_{1A} by ten times but the gain from V_{1B} to the output must remain unchanged. The top circuit of Fig.27b achieves the scaling by reducing both the feedback capacitor and the V_{1B} input capacitor. It also has the advantage of reducing the silicon area required to construct the capacitors. However, if it

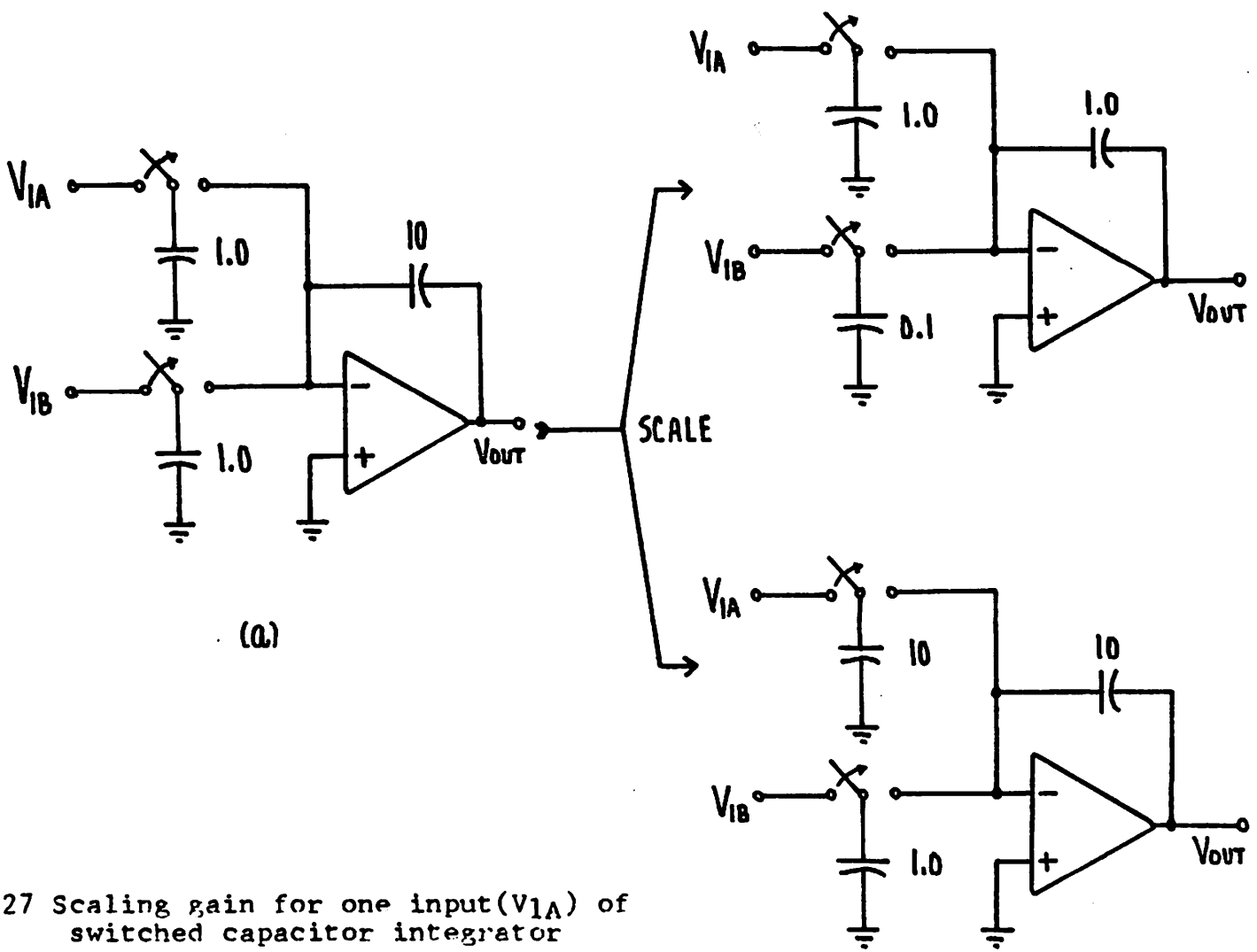


Fig.27 Scaling gain for one input(V_{1A}) of switched capacitor integrator

is assumed that the capacitor of size "1.0" as shown in Fig.27a is the minimum size that can be fabricated on I.C., then the top circuit of Fig.27b is unacceptable and the bottom circuit must be used. Silicon area required for the bottom circuit is greater than the original. This nonlinear relationship between capacitor sizes and integrator gains (as dictated by terminations) is very important in the noise analysis. A minimum capacitor size, determined from technology limits and allowable $\frac{kT}{C}$ noise, must be assumed before the scaling effects are to be calculated.

For the bandpass circuit, the gain constant for the input to integrator 1 that comes from integrator 2 must be scaled with the terminations while the gains for the other two inputs remain the same. The gain constant of integrator 2 is scaled for its single input. In addition, the rule for minimum size capacitance must be followed. The relation between silicon area and termination resistances will exhibit nonlinearities due to the enforcement of the minimum size rule because when the smaller capacitor of a ratio can no longer be reduced, the larger capacitor must be increased in size yielding a more dramatic change in area.

The noise equations for the filter may now be derived using the combined information contained in Eqs. (28)-(34). The spectral density noise voltage at the output due to noise generated by the switched capacitors is

$$V_{OUT\text{-}s.d.} = \frac{1}{f_c^{1/2}} \left[\left(\frac{1}{2}\right)^2 \left(\frac{kT}{\alpha_i C}\right) + \left(\frac{kT}{2\alpha_T C}\right) + \left(\frac{1}{2G_T}\right)^2 \left(\frac{kT}{\alpha_c C}\right) + Q^2 \left(\frac{kT}{\alpha_L C}\right) \right]^{1/2} \tag{35}$$

The integrator gain constants scale with the terminations as follows:

$$\alpha_C' = \alpha_C/G_T \tag{36a}$$

$$\alpha_L' = \alpha_L G_T \tag{36b}$$

where $\alpha_{C,L}$ = the integrator gain constants for G_T = 1 mho. Although the time constants scale linearly with terminations, the size of the input capacitors does not linearly depend on G_T due to the minimum size rule. Therefore, Eq. (35) cannot be evaluated over different values of G_T. For this problem, the analysis was performed by tabulating all capacitor sizes necessary for each value of the terminations in the circuit and then using Eq. (35) with appropriate capacitor values substituted to find the noise. The filter circuit for G_T = 1 mho using minimum size capacitors where possible was designed as the starting point of the table.

The spectral density noise voltage at the output due to the noise generated by the op amps is

$$V_{\substack{OUT\text{-}s.d.\\ Op\ Amp\\ Noise}} = \frac{V_{n\text{-}rms}}{f_c^{1/2}} \left[\left(\frac{1}{2G_T}\right)^2 (1+\alpha_L G_T)^2 + Q^2 \left(1+\alpha_C \left(\frac{1}{G_T} + 2 + 1\right)\right)^2 \right]^{1/2} \tag{37}$$

Op amps are assumed to have equal r.m.s. noise. The scaling of the gain constants is included in this expression and the noise for any value of G_T may be calculated. Since the gain of V_{IN} and the termination feedback through integrator 1 stays constant, there are terms in the expression that do <u>not</u> scale with G_T.

4. Summary of Analysis/Experimental Results

To summarize the results of these rather complicated expressions, several graphs were constructed. The table of circuit capacitor values

for each value of terminations was compiled based on the three prototype circuits shown in Fig. 28. Analysis was performed on filters with Q's of 1, 10, and 100 all having center frequencies of 1kHz and clock rates of 40kHz. The minimum size capacitance was assumed to be 1pf. From the table of capacitors, a total was calculated for each circuit and the silicon areas required to construct these totals was graphed in Fig. 29 based on an assumed value of 0.2pf per mil^2. The graph exhibits sharp corners at $R_T = 1/G_T = 1$ ohm where the minimum size capacitance is used where possible on the inputs of the integrators.

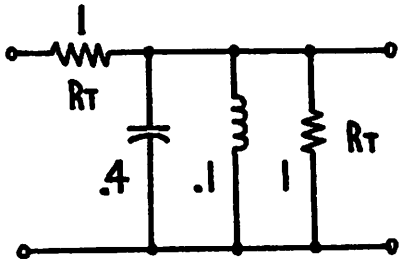
The linear relationship between integrator gain constants and termination resistances is shown in Fig.30 for the three filters. The widely separated gains of the two integrators for the high Q filter are seen to approach each other as the termination resistances are increased as expected.

Using the capacitor listing for each circuit, Eq. (35) was evaluated and the output noise normalized to $(\frac{kT}{1pf})\frac{1}{f_c^{1/2}}$ was graphed. In addition, the output noise due to the op amps normalized to $\frac{v_{n\text{-}rms}^2}{f_c^{1/2}}$ was calculated from Eq. (37) and the results were graphed along with the capacitor noise curves. This is shown in Fig. 31.

Experimental data was obtained for the filter of Fig.26 from a breadboarded circuit made with discrete op amps, capacitors, and analog switches. The filter tested was designed for a Q = 10 with center and clock frequencies of 1kHz and 40kHz respectively. Fig.32 shows a photograph taken from a spectrum analyzer that was connected to the output of the filter with the input shorted to ground. The noise exhibits the peaked response predicted earlier. The picture has a linear voltage scale

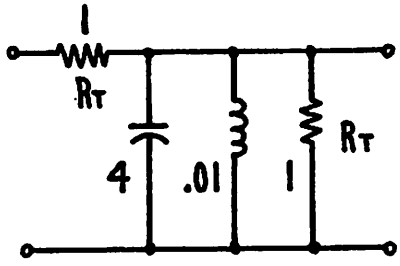
2 POLE BANDPASS FILTER

PROTOTYPES



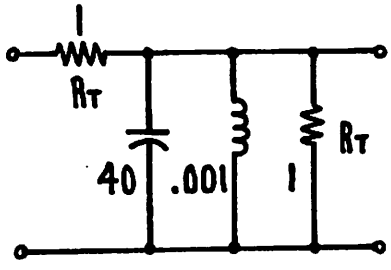
(a)

Q=1
SCALE TO 1kHz/40kHz
C=318μF L=80μH
α_C = .0785
α_L = .3141
} FOR RT=1



(b)

Q=10
SCALE TO 1kHz/40kHz
C=3.18mF L=8.0μH
α_C=.00785
α_L=3.141
} FOR RT=1



(c)

Q=100
SCALE TO 1kHz/40KHz
C=31.8mF L=.80μH
α_C=.000785
α_L=31.41
} FOR RT=1

$$\omega_o = \frac{1}{\sqrt{LC}} \qquad Q = \frac{1}{2\alpha_T}\sqrt{\frac{C}{L}}$$

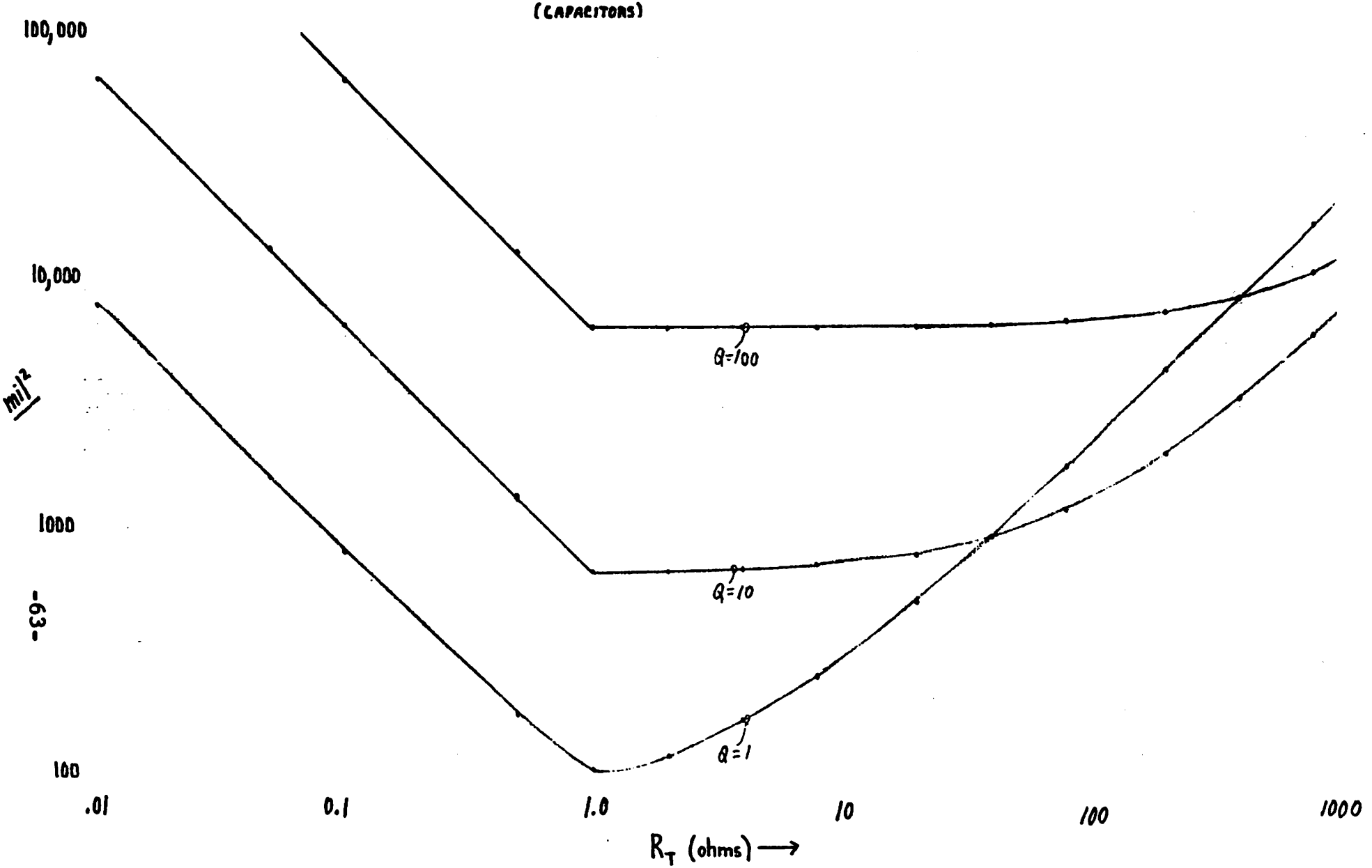
$$S_{\omega_o}^{C,L} = \frac{1}{2} \qquad S_Q^C = \frac{1}{2} \qquad S_Q^L = \frac{-1}{2}$$

Fig.28 Second order bandpass prototypes used in example of Section VIIc and Table I (Scaled element values and capacitor ratios are given at the right)

Silicon Area vs. R_T

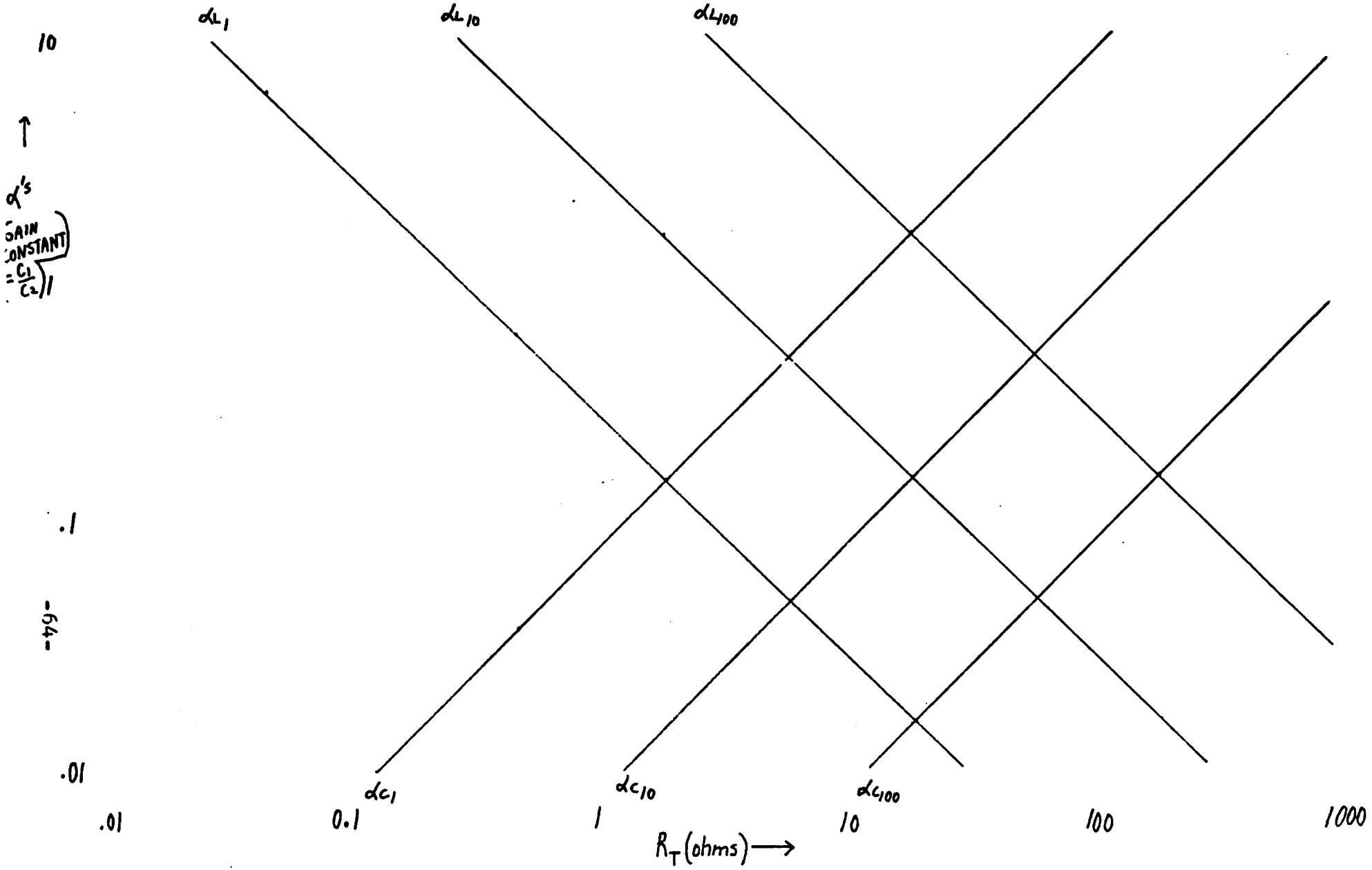
(CAPACITORS)

FIG. 29



Op Amp Integrator Gains vs. R_T

Fig. 30

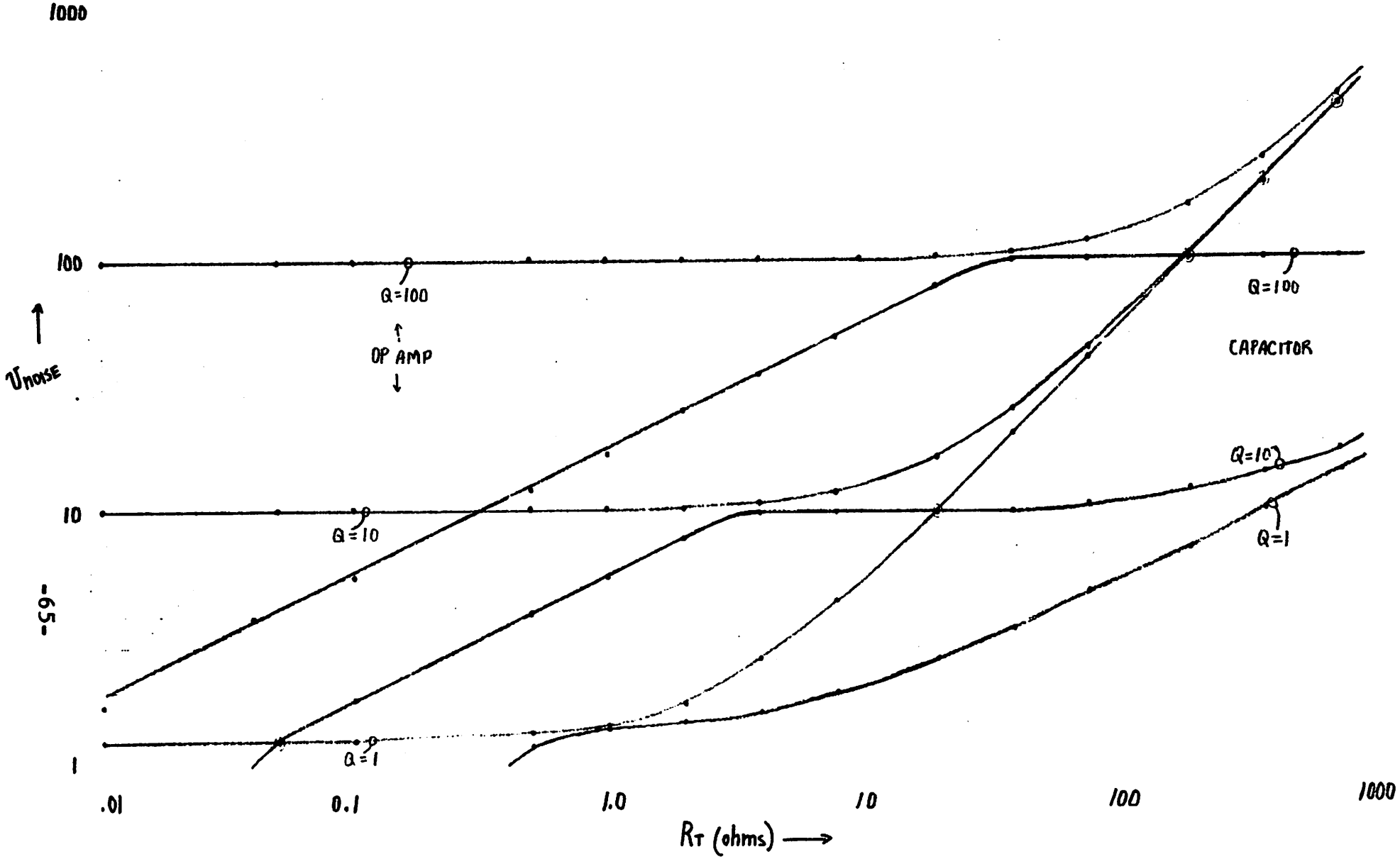


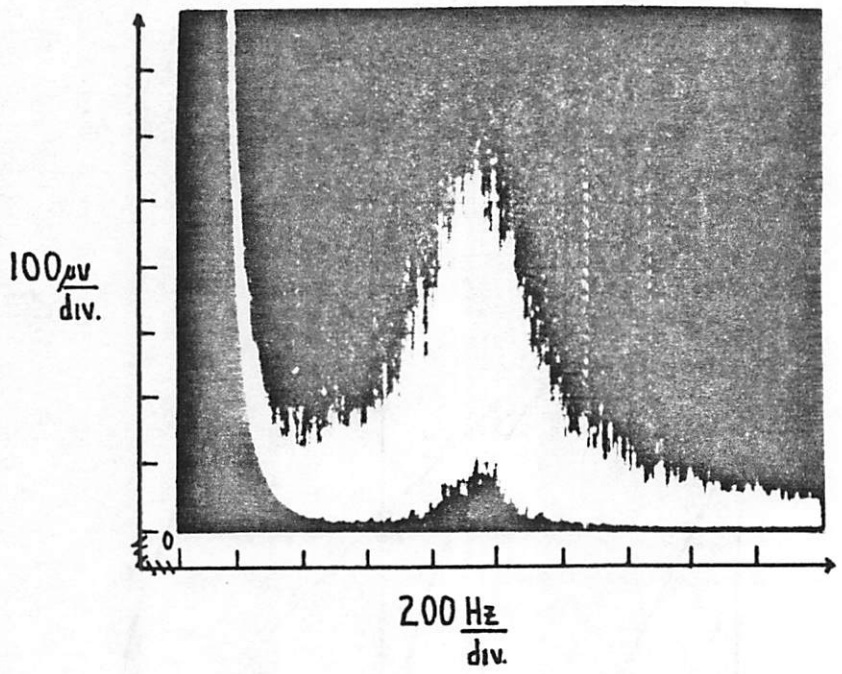
$\frac{1}{f_c^{3/2}}\left(\frac{kT}{1pf}\right)=1$

$\frac{V_{n\text{-}rms}^2}{f_c^{1/2}}=1$

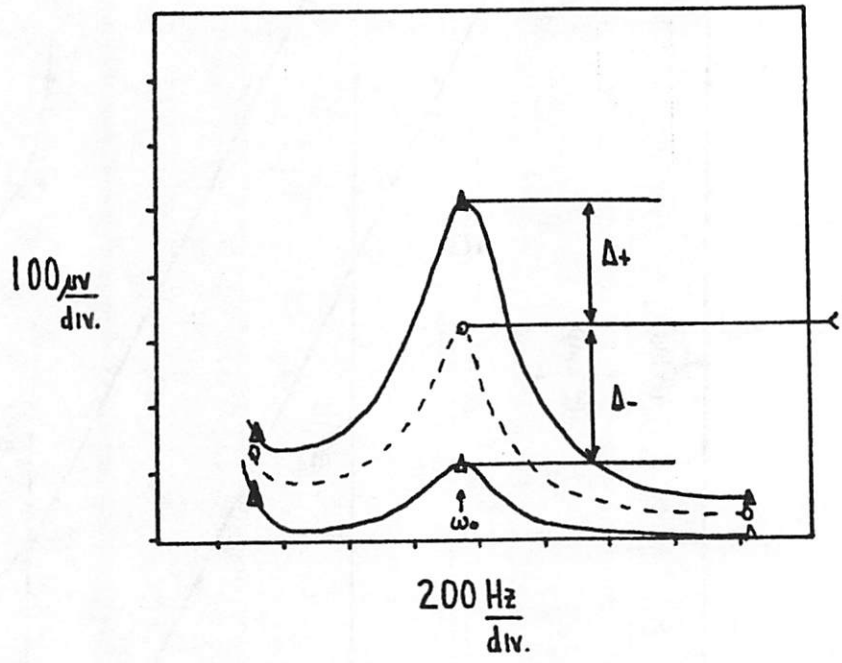
Normalized Output Noise Voltage vs. R_T

Fig. 31





(a)



(b)

Fig.32 a) Noise spectral density at output of 2-pole bandpass filter
b) Method of taking reading from photograph

(proportional to noise power) and represents the r.m.s. noise of the filter passed through a 100Hz bandwidth filter contained in the spectrum analyzer. The true r.m.s. value is the center of the noise "curve". Fig.32b shows the r.m.s. value taken off a typical photo along with the estimate of errors involved in this procedure. Dividing the values taken from the photos by $\sqrt{100Hz}$ yields the spectral density noise at the output. The experimental data is plotted in Fig. 33 normalized so that the value of op amp noise at the output of the experimental and theoretical (Fig. 31) filters for R_T = 1 ohm is the same. Only op amp noise was used for the comparison because capacitors on the breadboard were sufficiently large to make (kT/C)noise negligible with respect to the noise generated by the op amps.

The graphs of Figs.29-31 present a complete picture of the influence of the termination resistances on filter noise, silicon area, and integrator time constants. A first order examination of the data shows that at the expense of a slightly increased noise from the minimum, the optimum termination resistance is equal to the Q of the two pole filter. For this termination value, the silicon area is at a minimum and the integrator gains are close to one another placing similar demands on the operational amplifiers.

It should be emphasized here that the preceeding example was intended to show an analysis procedure. The characteristics of a specific filter will depend on many things such as frequency response, Q, and size or order.

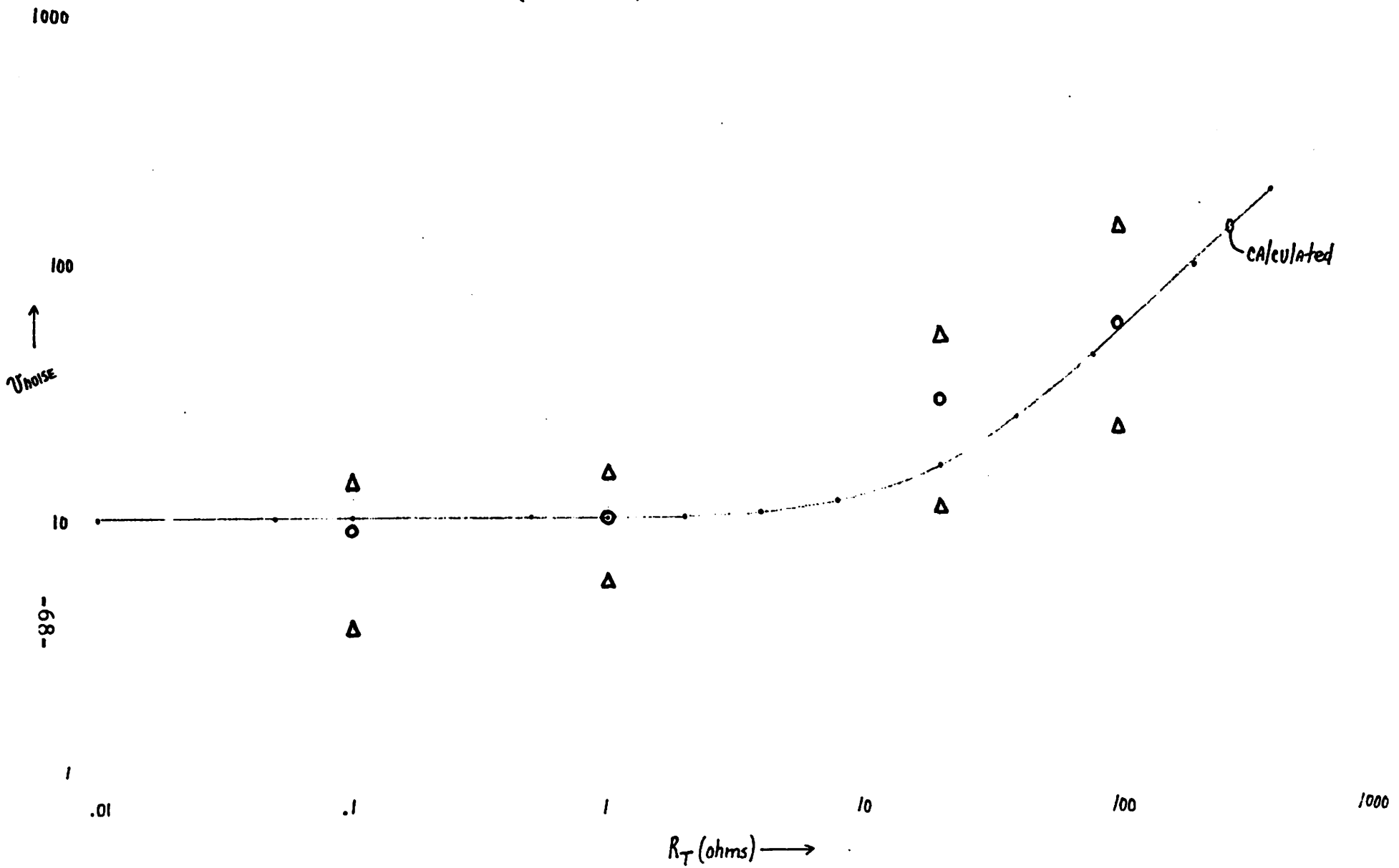
D. Improper (extra 1/2 delay) L.D.I. Terminations

As explained in Section IV, the switched capacitor implementation of a lossy integrator used for simulating terminations contains an extra half

FIG. 33

EXPERIMENTAL NOISE DATA

(NORMALIZED) (SEE FIG 32)



delay in the feedback loop. The effect of the extra half delay is to terminate in an impedance of $Z_T = R_T e^{-j\omega T/2}$ ohms rather than a pure resistance of R_T ohms. The impedance will be almost completely resistive, however, if $\omega T << 1$. In this case, the termination is approximately equal to R_T in series with an impedance of $-jR_T \sin\omega T/2 \approx -\frac{jR_T\omega T}{2}$ ohms. The exact reation for the changes in the frequency response of a filter due to the added termination impedances can be found in the references [20,23]. The experimental results from switched capacitor filters as presented in Section VIII verify that the effects of the improper L.D.I. terminations are small. In addition, Table I was prepared to show computer simulation data from the three bandpass filters whose prototypes are given in Fig. 28 The computer program accepts a digital z-domain representation of the switched capacitor filter circuit (Fig.26d) and computes the transfer function.

The errors due to improper terminations are negligible for the two higher Q filters, however the filter with Q = 1 shows appreciable errors in center frequency and bandwidth when improperly terminated. This rather surprising result warranted a closer look at the filter and the following reasons for the error were postulated:

An improperly terminated L.D.I. integrator exhibits errors in both the phase shift and magnitude (time constant) of its transfer function as compared with the properly terminated integrator. Further, the first order fractional magnitude error depends only on the gain α of the integrator and the termination feedback α_T (Fig. 16). This result is explained in detail in Appendix I. The magnitude error of the lossy integrator in the second order bandpass filter is analogous to a variation of C in the circuit which affects both ω_o and Q of the frequency response. For the Q = 1

TABLE I

COMPUTER SIMULATION RESULTS

TERMINATION STUDY

2 Pole Bandpass Filter f_o=1kHz f_c=40kHz
1 ohm Terminations (prototypes: See Fig. 28)

	A	B	C	D	% ⇒ $\frac{\text{INCORR.} - \text{CORRECT}}{\text{CORRECT}} \times 100\%$		
CONDITIONS	f_o (Hz)	INSERT. LOSS AT f_o (dB)	B.W. (Hz)	$Q = \frac{f_o}{\text{B.W.}}$	Δ_A	Δ_B	Δ_D
Q=1 Correct L.D.I. Termination (nominal)	1000	-6.02062	998	1.002			
Incorrect L.D.I. Termination	1050	-5.99177	1090	0.963	5%	.02885dB	3.9%
Q=10 Correct L.D.I. Termination (nominal)	1002	-6.02221	100	10.02			
Incorrect L.D.I. Termination	1006	-5.99518	100	10.06	0.2%	.02703dB	0.4%
Q=100 Correct L.D.I. Termination (nominal)	1001	-6.02080	10	100.10			
Incorrect L.D.I. Termination	1001.4	-5.99385	10	100.14	.04%	.02695dB	.04%

filter, the fractional error in α which is proportional to 1/C was found to be large. As shown by the prototypes of Fig. 28, $Q = \frac{1}{2}\sqrt{C/L}$ for one ohm terminations, and the higher Q filters were implemented by scaling C and L appropriately. As the value of C was increased to raise the Q, α for the integrator simulating C dropped by the same amount causing the fractional magnitude error to also drop. This result is illustrated in Table I where the difference between the Q of the improperly and properly terminated filters scaled inversely with the value of C in the circuit.

VIII. EXPERIMENTAL RESULTS

Although switched capacitor filters are ideally suited for integration, experimental verification of many theoretical predictions was more easily accomplished by means of a discrete component "breadboard". Circuits were constructed using high input impedance (JFET or MOS) op amps, analog switches, and standard mica capacitors. There were significantly large errors in the capacitor ratios due to parasitics in the switches and the required use of standard values of capacitors (with 5% tolerances!). The purpose of the breadboard however, was to verify predictions without a high degree of accuracy before integrated circuit fabrication was attempted. In a sense, the inaccuracies of the breadboard tested the low sensitivity characteristics of the doubly terminated ladder simulation and, as will be seen, in most cases, circuit performance was excellent despite the errors.

This section presents experimental results of the test circuits along with computer simulations of proposed new circuits. In addition, a sensitivity study of one filter, performed on the computer, is included. L.D.I. integrators were used in all circuits.

A. Lowpass Ladder

The fourth order lowpass ladder of Fig. 4 was constructed for a Butterworth response with the element values and clock rate given in the example of Section IIIc. Fig.12 shows the switched capacitor circuit. The frequency response was observed on a spectrum analyzer as shown in Fig. 34. The expanded passband is shown in Fig. 15 (bottom trace).

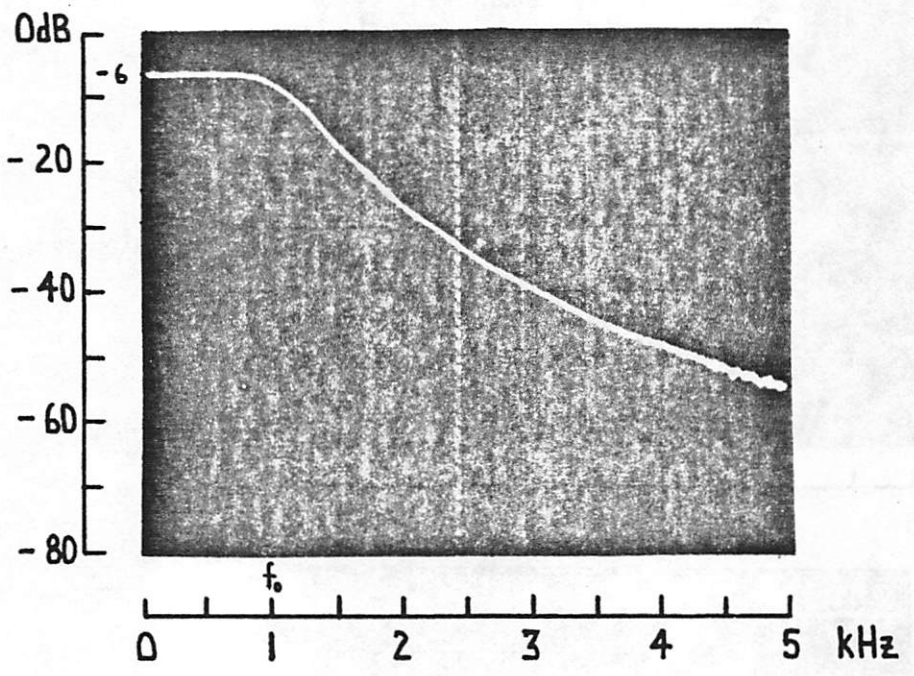
B. Lowpass Filter with Transmission Zeros

The fifth order lowpass ladder with four transmission zeros presented as an example in Section V was constructed. The network and switched capacitor circuit are shown in Fig. 21. Element values are given below:

$$
\begin{aligned}
R_1 &= 1\Omega & L_4 &= 53.70\mu H \\
C_1 &= 33.77\mu F & C_4 &= 11.00\mu F \\
L_2 &= 39.40\mu H & C_5 &= 30.70\mu F \\
C_2 &= 32.4\mu F & R_2 &= 1\Omega \\
C_3 &= 71.5\mu F
\end{aligned}
\qquad (38)
$$

The passband was designed for D.C. to 3100Hz with 0.1dB ripple. Minimum stopband rejection was 37dB. A clocking rate of 128kHz was used and Fig. 35 shows photos of the observed frequency reponse. In this case, the inaccuracies of the breadboarded circuit were visible in the frequency response. The insertion loss and ripple in the passband were greater than expected, as shown in Fig. 35a. Zero frequencies were also in error.

In order to investigate these observations further, the filter was simulated on a computer (using same program described in Section VIId).



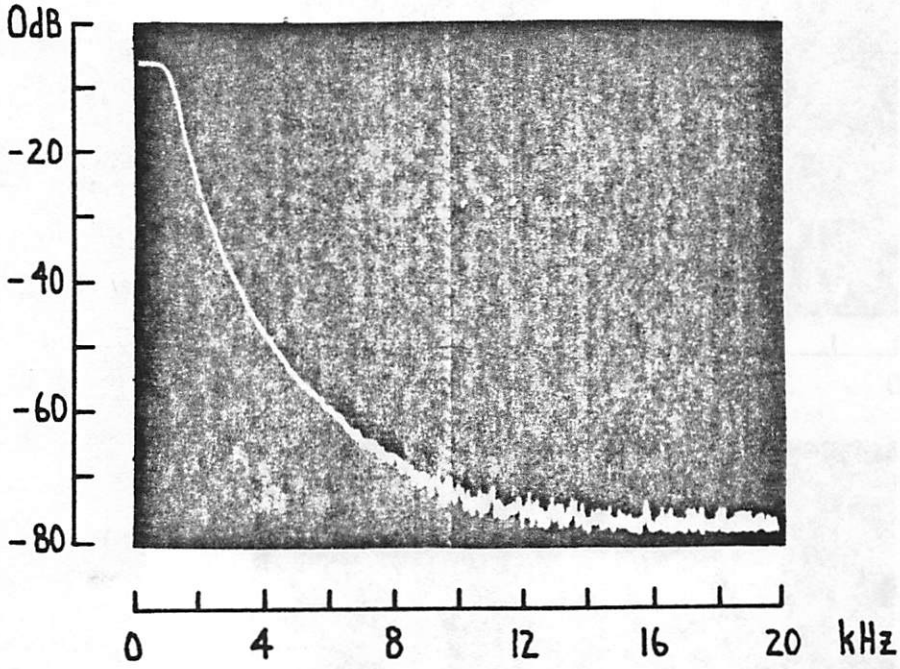


Fig.34 Frequency response of 4-pole Butterworth lowpass switched capacitor filter (f_c=40kHz)

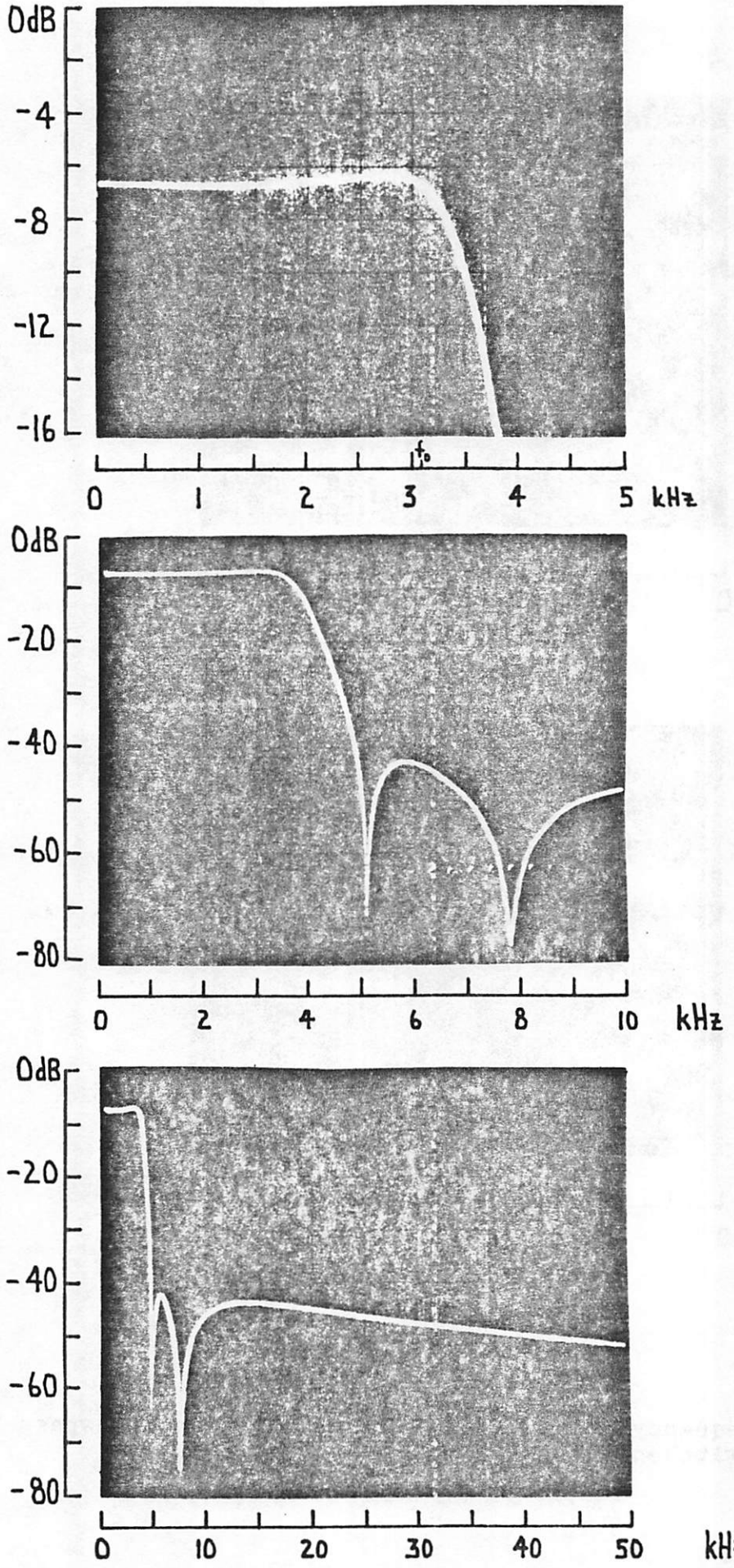


Fig.35 Frequency response of 5-pole, 4-zero lowpass switched capacitor filter (f_c=128kHz)

Along with the nominal case, nine other simulations were done, each with a 1% variation on one of the integrator gain constants. These included a variation in each integrator capacitance ratio along with and ratios used for determining the feedforward and feedback paths as described in Section V. Table II contains the results of the sensitivity study and it indicates that tolerances in the capacitance ratios of the bread-board must have been quite large as previously postulated to cause the observed errors in the frequency response.

C. Bandpass Filters

1. Two-Pole

The 2 pole bandpass circuit of Fig.26dwas constructed for a Q = 10. Values for circuit elements are given in Fig. 28b. The observed frequency response is shown in Fig. 36.

2. Four-Pole

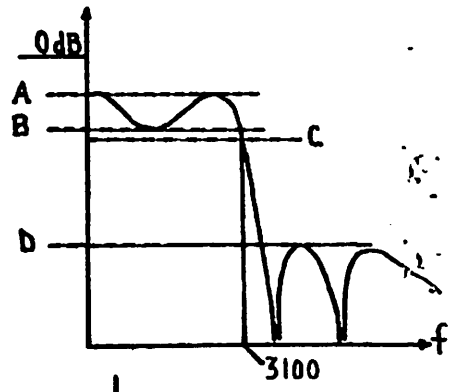
The switched capacitor version of a fourth order bandpass network (Fig. 7b) was constructed using the circuit of Fig. 37. A second order butterworth response lowpass prototype was used for the design. The bandpass network was obtained by means of the bandpass transform shown in Fig. 8. The calculated 3dB points were 500Hz and 2500Hz with the center frequency chosen as the geometric mean of these two frequencies. Element values are given below: f_c = 50kHz.

$$\begin{aligned} R_1 &= 1\Omega & C_2 &= 180\mu F \\ L_1 &= 180\mu H & R_2 &= 1\Omega \\ C_1 &= 113\mu F & \omega_o &= 1118Hz \\ L_2 &= 113\mu H & Q &= 0.6 \end{aligned} \tag{39}$$

TABLE II

COMPUTER SIMULATION RESULTS

SENSITIVITY ANALYSIS



5 Pole Lowpass Filter
4 Transmission Zeros
Passband Ripple=0.1dB
0-3100Hz
f_c=128kHz

1% VARIATION ON INTEGRATOR GAIN CONSTANTS

RATIO VARIED 1%	A MIN. INSERT. LOSS	A-B PASSBAND RIPPLE	C LOSS AT 3100 Hz	D MIN. STOPBAND REJ.
NOMINAL	-6.0012dB	.0599dB	-6.1003dB	-37.3333dB
α_1 (C_1+C_2)	-6.0206dB	.0445dB	-6.1449dB	-37.2481dB
α_2 (L_2)	-6.0026dB	.0605dB	-6.0810dB	-37.076 dB
α_3 $(C_2+C_3+C_4)$	-5.9786dB	.0775dB	-6.0466dB	-37.5818
α_4 (L_4)	-6.0007dB	.0617dB	-6.1041dB	-37.5759dB
α_5 (C_4+C_5)	-5.9918dB	.0674dB	-6.0927dB	-37.1602dB
$\frac{C_2}{C_1+C_2}$	-5.9702dB	.0853dB	-6.0629dB	-37.3292dB
$\frac{C_4}{C_4+C_5}$	-6.0115dB	.0515dB	-6.1117dB	-37.4561dB
$\frac{C_4}{C_2+C_3+C_4}$	-5.9910dB	.0678dB	-6.0866dB	-37.3347dB
$\frac{C_2}{C_2+C_3+C_4}$	-6.0206dB	.0443dB	-6.1446dB	-36.9099dB

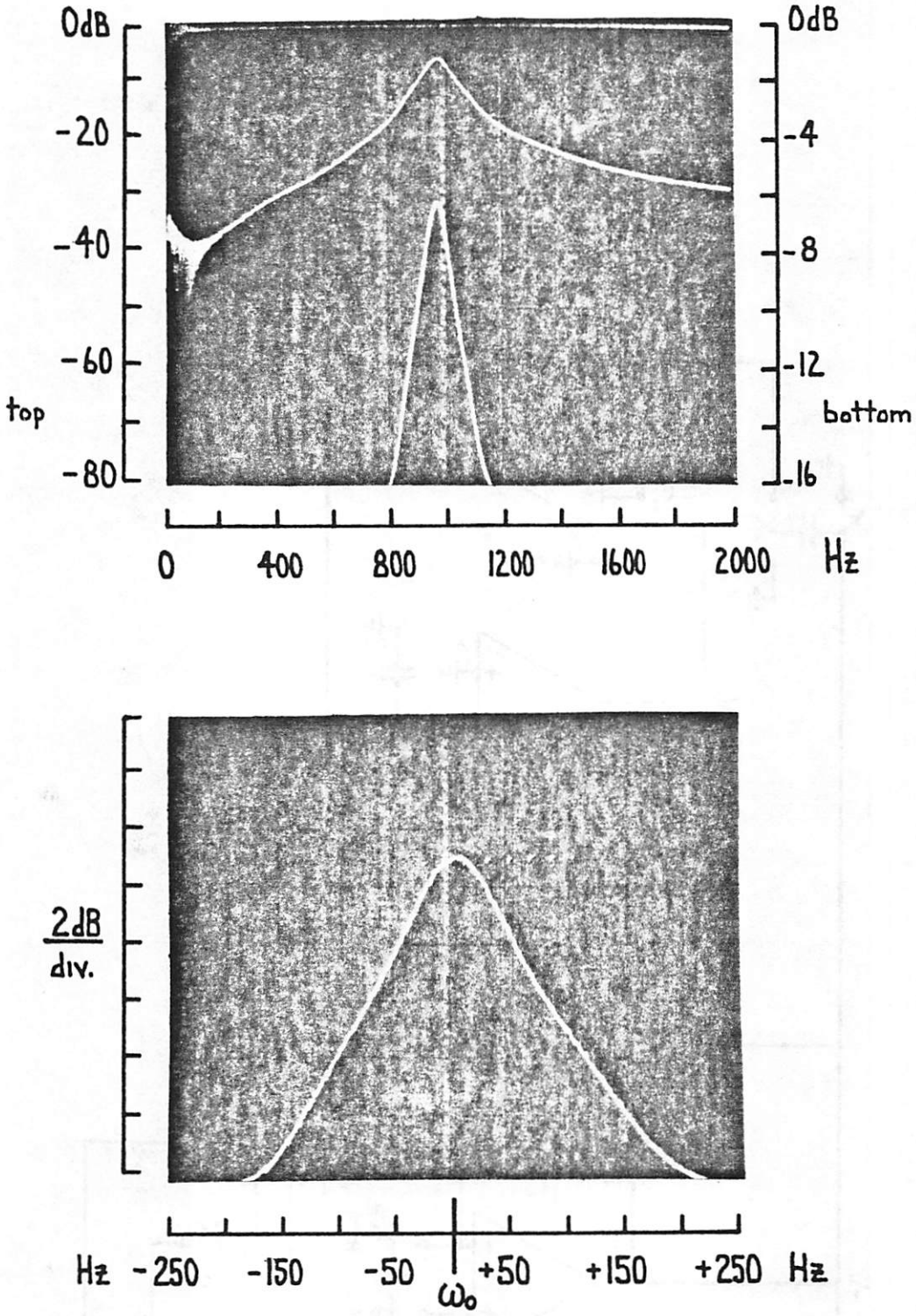


Fig.36 Frequency respone of 2-pole bandpass switched capacitor filter (f_c=40kHz)

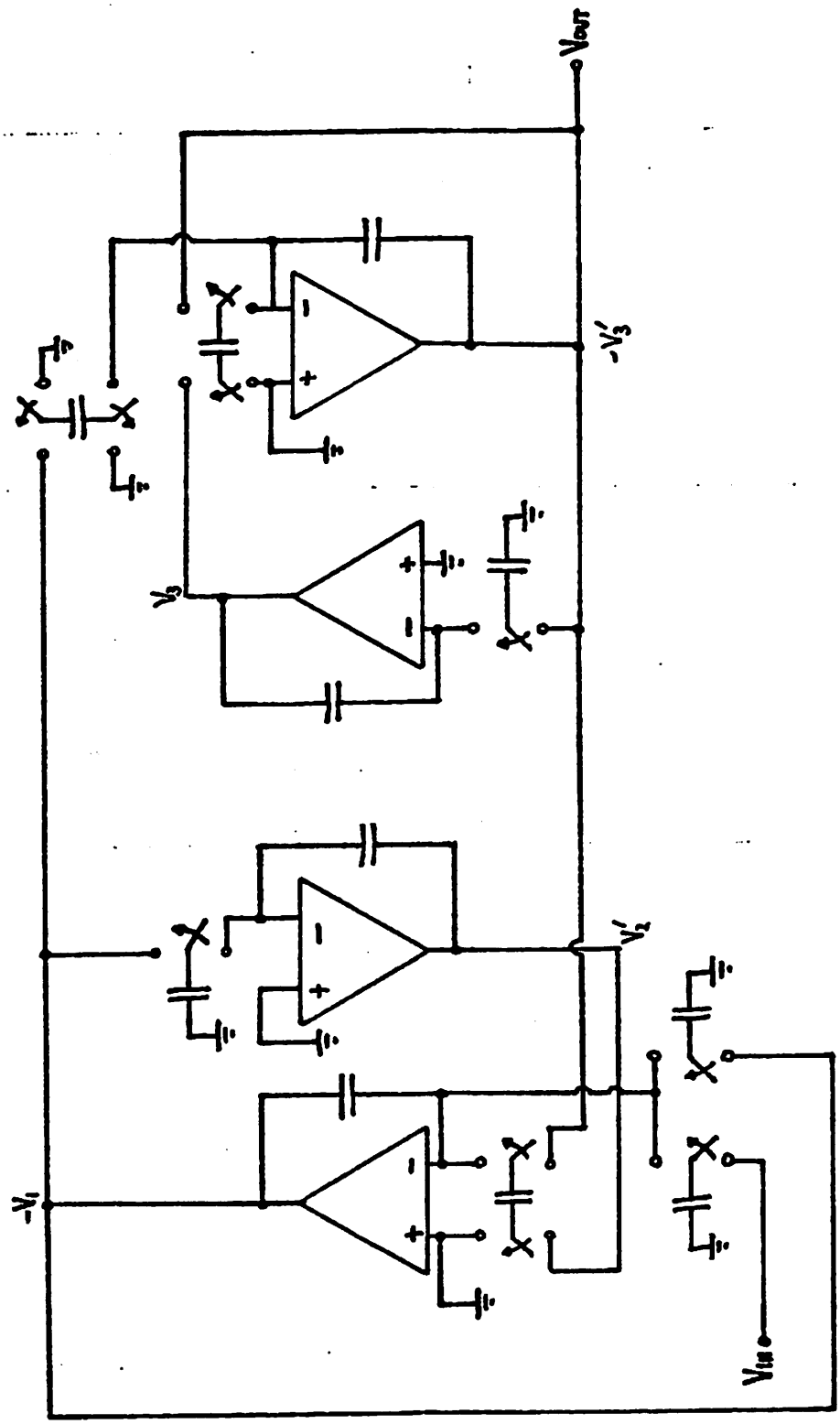


Fig.37 Switched capacitor circuit of Fourth order bandpass filter

The observed frequency response of the fourth order network is shown in Fig. 38. The trace exhibits the desired -12dB/octave slope on either side of the passband.

Several attempts were made to construct a fourth order bandpass filter with a higher Q than the example above. However, several problems were encountered. A primary problem with the high Q filters was the size of capacitor ratios necessary in the switched capacitor circuit. Unfortunately, as dictated by the bandpass transform (Fig. 8) the values of inductors and capacitors in the circuit becomes widely separated as the Q increases. In the ladder filter, the transform creates large and small size capacitors and inductors both, therefore, an impedance scaling does not help. Another problem observed on the breadboards was a mysterious "loss" in the circuit that caused Q's to drop below their calculated values. In addition, the flat response of the passband was destroyed in the high Q circuits and the frequency response showed signs of the two resonant tanks of the network being detuned. This problem is unsolved as yet but circuit parasitics are again the suspected cause since computer simulations showed none of these errors.

D. Bandpass Elliptic Filter

A proposed switched capacitor filter circuit that has not yet been breadboarded is that for an elliptic bandpass network. The network of Fig. 39 was examined. Using the method outlined in Section V, the series capacitor arms can be reflected to the shunt arms yielding the flow diagram shown in Fig. 40. A digital representation of the flow diagram was simulated and the results are shown in Fig. 41. This circuit looks promising because of its simplicity. In effect, it consists of two lossy resonant circuits separated by a lowpass ladder.

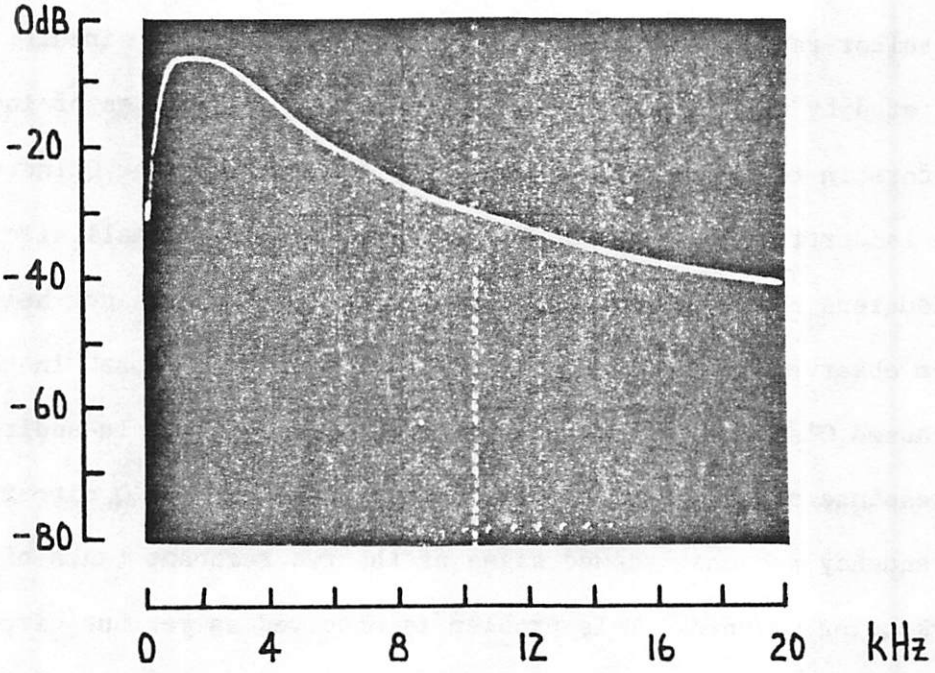
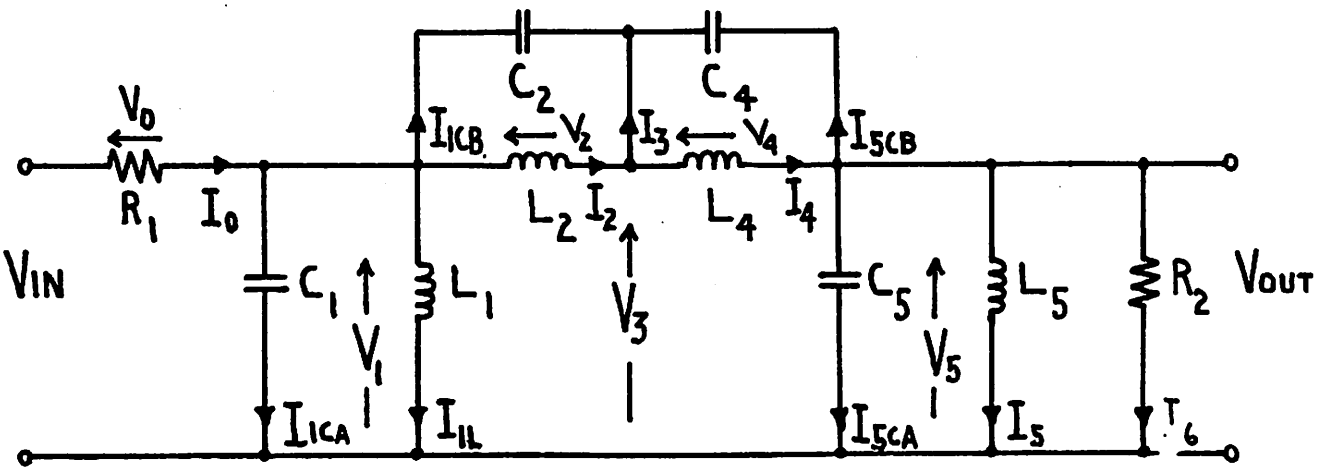


Fig.38 Frequency response of 4-pole Butterworth bandpass switched capacitor filter (f_c=50kHz)



$R_1 = 1\Omega$	$C_4 = 69.1$ F
$C_1 = 357.4$ F	$L_4 = 83.4$ H
$L_1 = 35.9$ H	$C_5 = 357.4$ F
$C_2 = 153.9$ F	$L_5 = 35.9$ H
$L_2 = 185.8$ H	$R_1 = 1$

PASSBAND 1209 - 1633 Hz .1dB RIPPLE

ZEROES 941, 2098 Hz

$\omega_o = 1405$ Hz

Fig.39 a) Elliptic bandpass filter
b) Element values for simulation

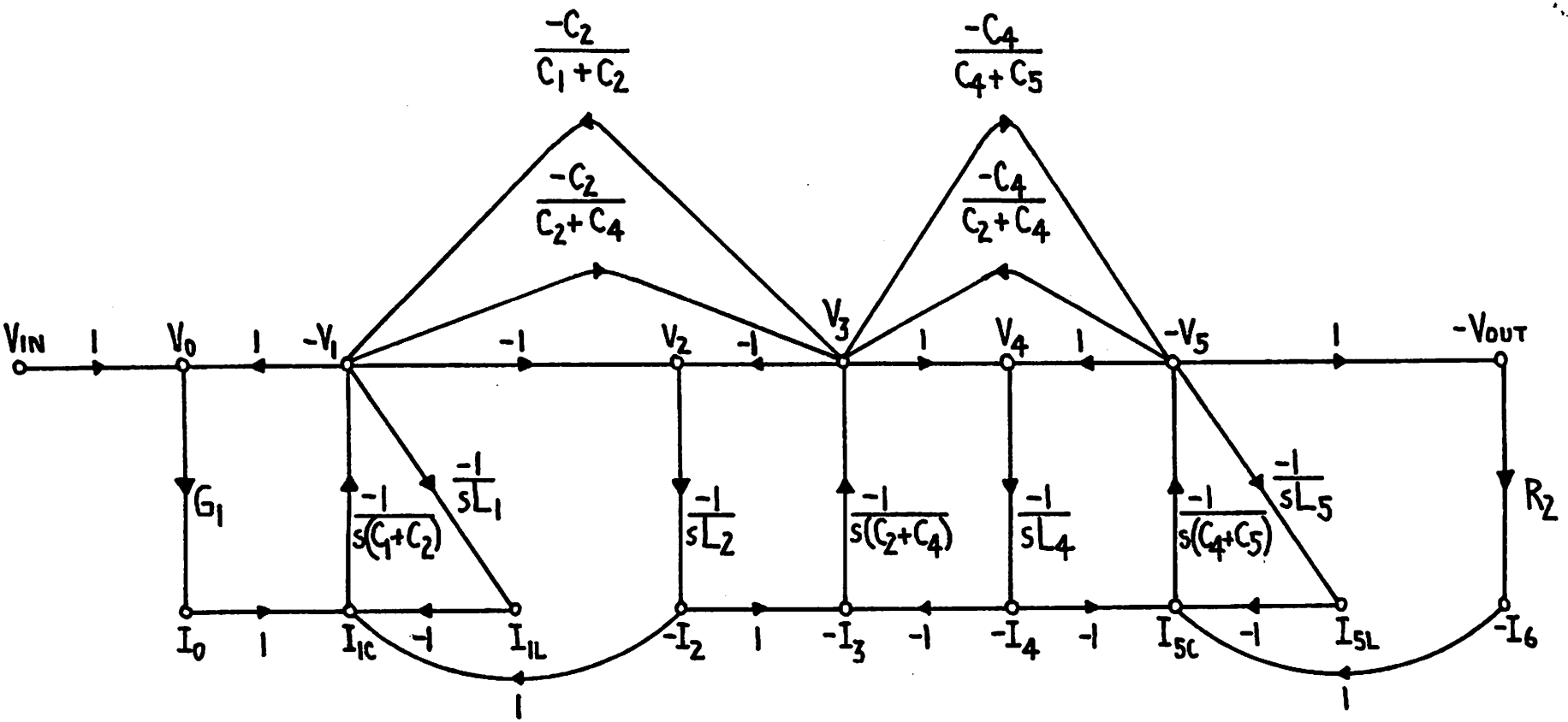


Fig.40 Flow-diagram for elliptic bandpass filter in Fig.39(a)

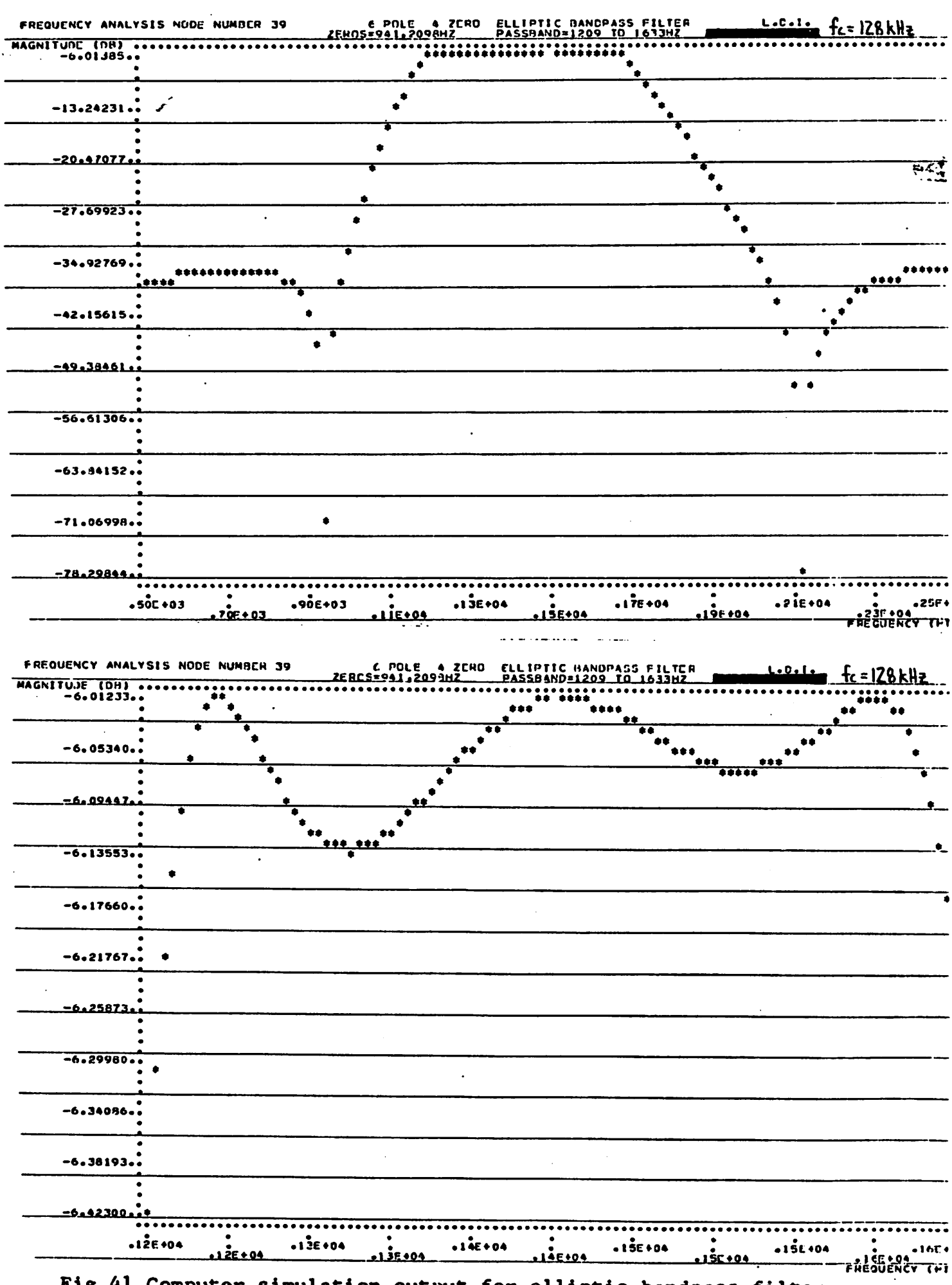


Fig.41 Computer simulation output for elliptic bandpass filter in Figures 39,40

E. Highpass Filter

The network and corresponding flow diagram of Fig. 42 were examined. A z-domain equivalent of the circuit was simulated with the element values chosen to give a Chebychev (.1dB ripple) response. The cutoff and clock frequencies were 1kHz and 128kHz respectively. See Fig. 43.

$R_1 = 1\Omega$ $\quad C_4 = 102.29\mu F$

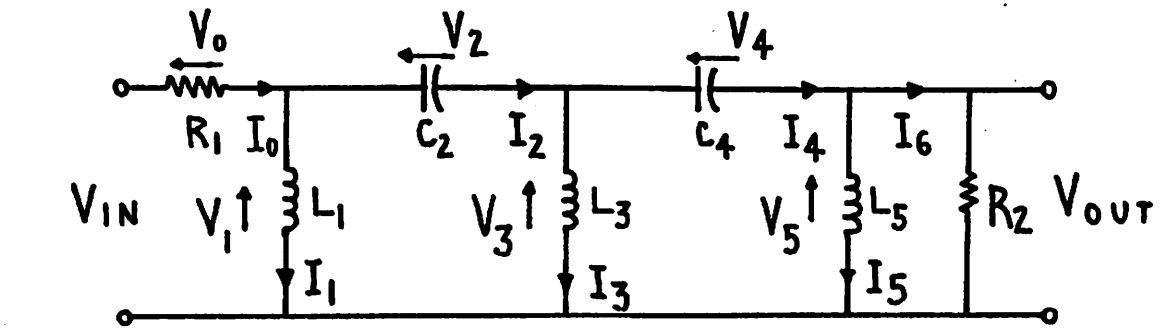
$L_1 = 122.31\mu H$ $\quad L_5 = 122.31\mu H$

$C_2 = 102.29\mu F$ $\quad R_2 = 1\Omega$

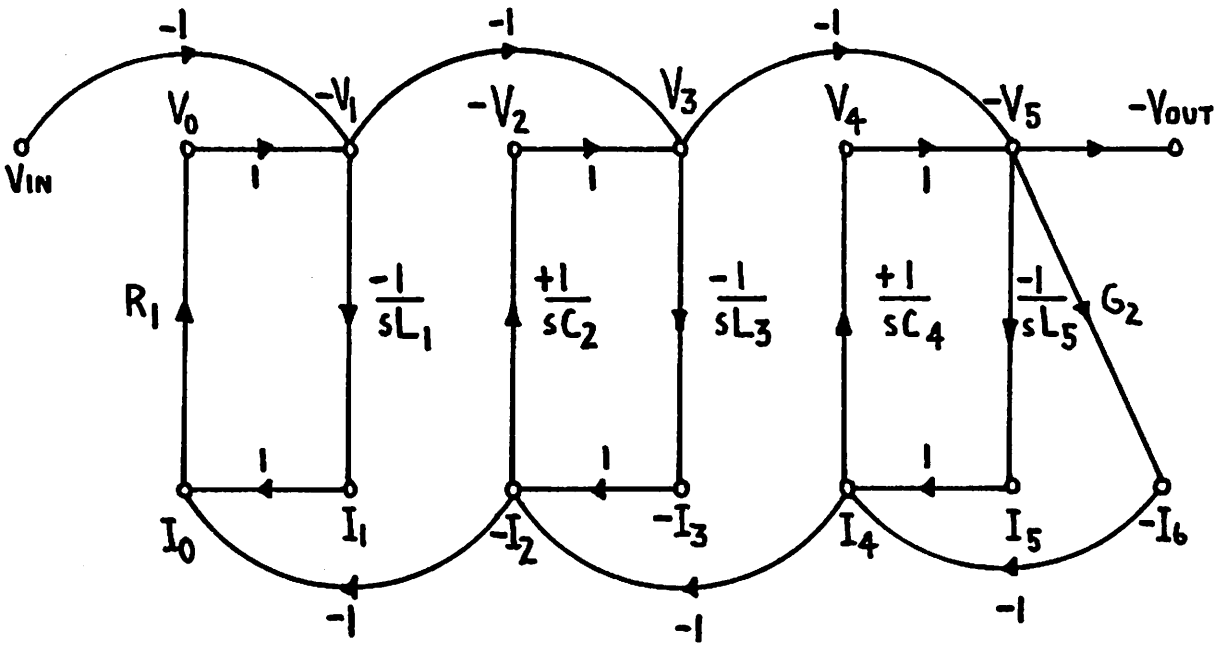
$L_3 = 71.02\mu H$

From the flow diagram for the network, it is observed that the switched capacitor implementation is complicated by the need for voltage additions occurring away from integrators. For example, $-V_1$ and $-V_2$ of Fig. 42b are summed at node V_3 and then integrated. In addition, their sum must be sent to node $-V_5$. This cannot be done using standard switched capacitor integrators because the sum is performed within the integrator by adding charges from switched capacitors. One way to implement the summation is to feed voltages $-V_1$ and $-V_2$ to both nodes V_3 and $-V_5$. However, note that the voltage sum $-V_5$ must also be sent to another node. A detailed look at this method shows that the switched capacitor circuit of an n pole highpass filter will contain integrators with the number of inputs approaching 2n!

By rearranging the circuit flow diagram, a profound simplification was discovered. Fig. 44a shows a symbolic representation of the flow diagram of Fig.42b. The representation of Fig. 44b is equivalent with the only change being that summers are now placed at integrator outputs. An integrator with a voltage summed to its output is the function performed by the circuit



(a)



(b)

Fig.42 a) Doubly terminated highpass ladder
b) Flow-diagram of (a)

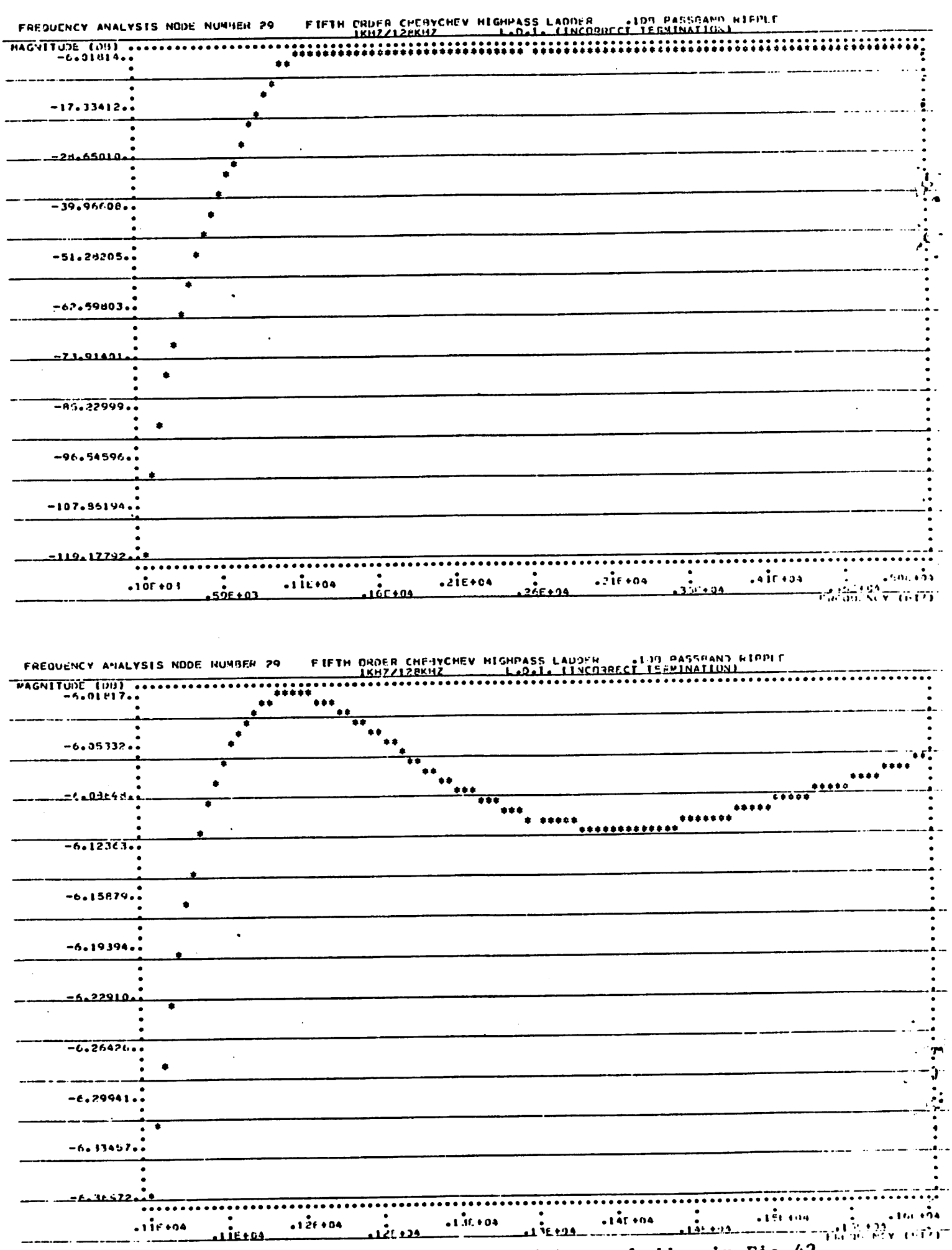


Fig.43 Computer simulation output for highpass ladder in Fig.42

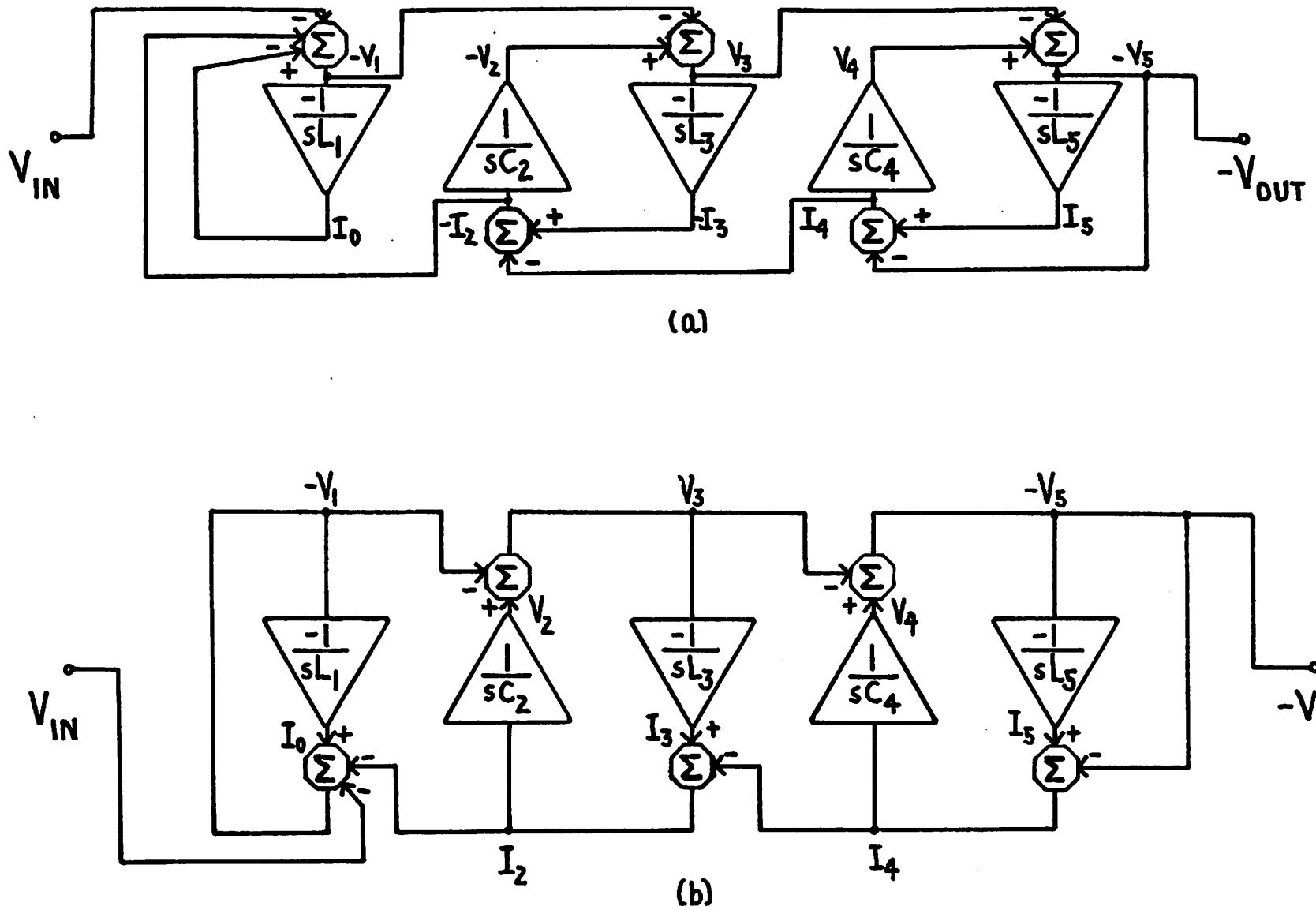


Fig.44 a) Symbolic representation of high pass flow-diagram in Fig.42(b)
b) Equivalent representation of (a)

presented in Section V and shown in Fig. 19 . Replacing conventional integrators with integrator/summers yields the circuit shown in Fig. 45 for the highpass ladder. This proposed method for implementing a highpass filter has not yet been breadboarded, but further investigation is planned for the future.

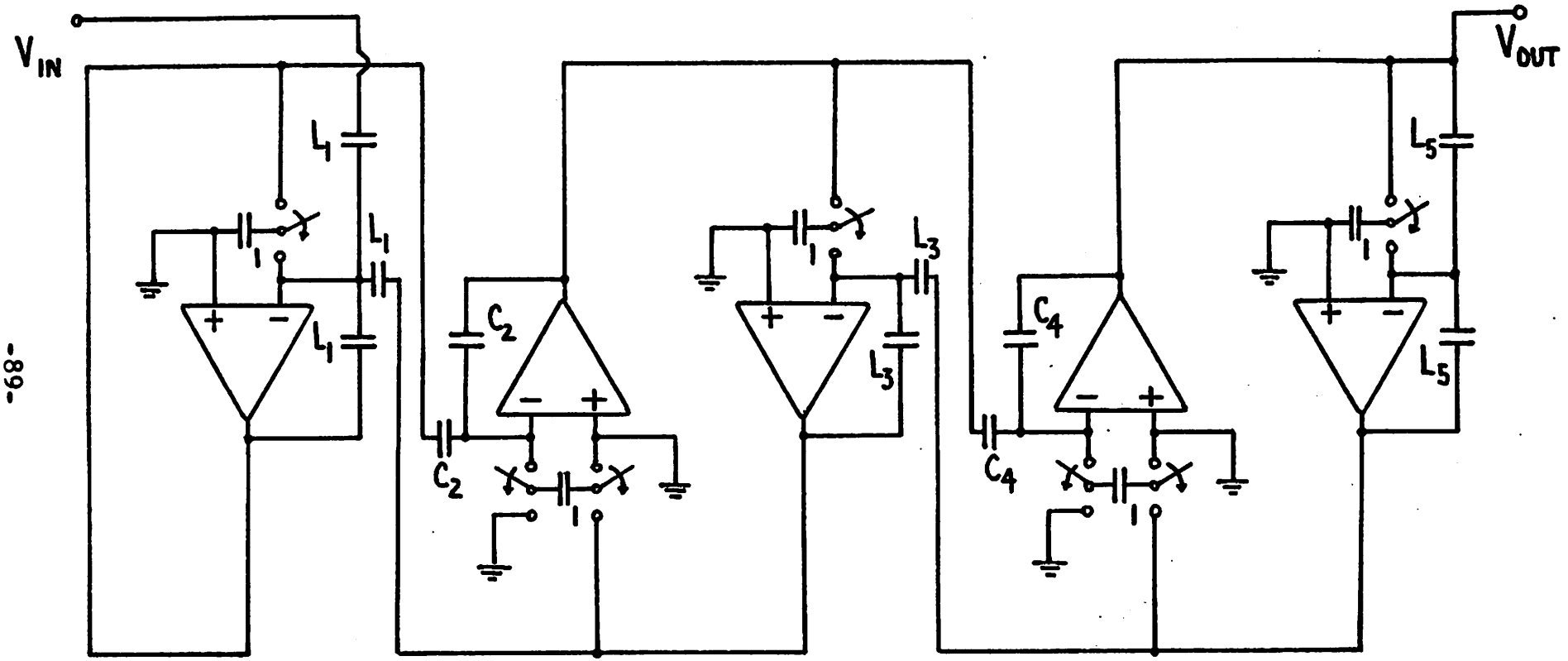


Fig.45 Highpass ladder switched capacitor circuit of Fig.44(b)

IX. CONCLUSION

Practical design methods and considerations have been presented for doubly terminated ladder filters using switched capacitors. By using "lossless" integrators [20] the designer of switched capacitor ladders can take advantage of well documented classical filter theory to provide networks suitable for his needs. Learning flow diagram construction techniques allows the implementation of many different structures in addition to the common ladder structures discussed. Of interest for the future are singly terminated networks and other active filter structures which may be constructed using switched capacitors.

As the MOS process technology advances, further developments in filter design should follow. Higher density may be achieved by shrinking line-widths and increasing the quality of MOS transistor performance, allowing simpler and subsequently smaller operational amplifier circuits.

APPENDIX I ANALYSIS OF IMPROPERLY TERMINATED L.D.I. LOSSY INTEGRATOR

Refer to Fig. 16. The transfer function of a correctly terminated L.D.I. lossy integrator is found to be

$$\frac{-\alpha}{(z^{1/2}-z^{-1/2})+\alpha_T\alpha} \tag{A.1}$$

while the transfer function of an incorrectly terminated L.D.I. lossy integrator is

$$\frac{-\alpha}{(z^{1/2}-z^{-1/2})+\alpha_T\alpha z^{-1/2}} \tag{A.2}$$

The procedure outlined in Section IV will be used again to compare these transfer functions in the familiar continuous time domain. First, the transfer function of the conventional continuous time lossy integrator shown in Fig. A1 is

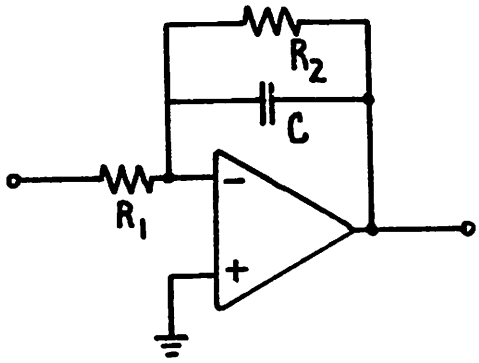
$$\frac{-k}{j\omega+\alpha_T k} \tag{A.3}$$

where $1/k = \tau$, the time constant of the integrator. Comparing (A.1) to (A.3) by letting $z = e^{j\omega T}$ yields

$$\frac{-k}{j\omega+\alpha_T k} \leftrightarrow \frac{-\alpha/T}{j\omega\left(\frac{2\sin \omega T/2}{\omega T}\right) + \frac{\alpha_T\alpha}{T}} \tag{A.4}$$

where T/α is the time constant τ of the switched capacitor integrator $= \left(\frac{C_2}{C_1 f_C}\right)$ (Fig. 3b). Eq. (A.4) shows that the termination is implemented correctly. The small magnitude error $(2\sin \omega T/2)/\omega T$ is characteristic of the L.D.I. integrator and was explained in Section IV.

Now, (A.2) is compared to (A.3) to determine the effects of the improper termination.



$$k = \frac{1}{R_1 C}$$

$$\alpha_T = \frac{R_1}{R_2}$$

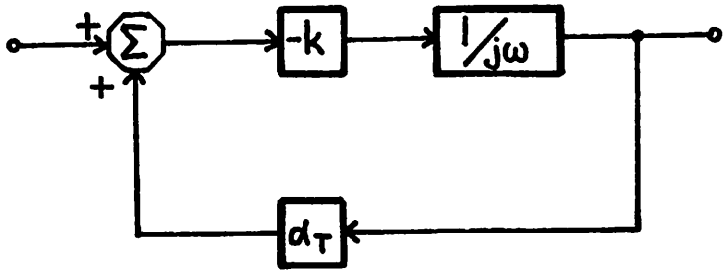


Fig. A1 Circuit and block diagram of conventional lossy integrator

$$\frac{-k}{j\omega+\alpha_T k} \leftrightarrow \frac{-\alpha/T}{j\omega\left(\frac{2\sin \omega T/2}{\omega T}\right) + \frac{\alpha_T \alpha e^{-j\omega T/2}}{T}}$$

$$= \frac{-\alpha/T}{j\omega\left(\frac{2\sin \omega T/2}{\omega T}\right) + \frac{\alpha_T \alpha}{T}\left(1 - \frac{j\omega T}{2} - \frac{(\omega T)^2}{8} + \ldots\right)}$$

$$\approx \frac{-\alpha/T}{j\omega\left(\frac{2\sin \omega T/2}{\omega T} - \frac{\alpha_T \alpha}{2}\right) + \frac{\alpha_T \alpha}{T}\left(1 - \frac{(\omega T)^2}{8}\right)} \qquad \text{(A.5)}$$

The first order magnitude error due to the incorrect termination is observed to depend only on α and α_T of the integrator! If $\omega T << 1$ this magnitude error dominates and Eq. (A.5) becomes

$$T(j\omega) = \frac{-\alpha/T}{j\omega\left(1 - \frac{\alpha_T \alpha}{2}\right) + \frac{\alpha_T \alpha}{T}} \qquad \text{(A.6)}$$

The fractional error $\frac{\alpha_T \alpha}{2}$ of the time constant τ can cause large errors when α and α_T are close of unity.

For the low Q filter discussed in Section VII, $\alpha = .0785$, $\alpha_T = 2$ and since $Q = \frac{1}{2}\sqrt{C/L}$ for one ohm terminations, the sensitivity of Q to variations in C (and therefore τ) is 1/2. From Eq. (A.6) the fractional magnitude error was $\frac{\alpha\alpha_T}{2} = 7.85\%$. Multiplying by the sensitivity 1/2 yields the 3.9% error in Q observed for the improperly terminated filter in Table I.

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