AN APPROACH TO THE ROUTING OF MULTILAYER PRINTED CIRCUIT BOARDS

by

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Abstract

In the design of large and complex electronic systems, a central problem is the interconnection of functional and/or circuit modules. With the advent of miniaturization, it is often necessary to connect hundreds or thousands of terminals by means of printed wires on a multilayer board with prescribed constraints. The specification is given in terms of a signal net list. A key question is whether a given signal net list can be routed with a specified multilayer board. Up to now, approaches to the problem have been, by and large, heuristic and cut-and-try.

In this paper we introduce a new approach. The essence is to decompose the complex problem into four phases, namely: vias assignment, linear placement of via columns, layering and single-line routing. Each sub-problem can be formulated succinctly and quasi-optimum results are obtained. An implementation program has been developed using Fortran on CDC 6400 computer.

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I. Introduction

Multilayer routing has been one of the more popular subjects of recent interest in the area of design automation. One main reason is that it is now possible to fabricate various kinds of circuits within a single semiconductor chip. Thus, more complicated and large-scale circuits or systems can be designed by using chips as basic building blocks. The multilayer printed circuit (MPC) board is a vehicle for carrying out such designs, and it is used as the medium for interconnecting modules which consist of components and building blocks of various forms. For these designs, modules can be considered as being mounted on top of the board. Terminals of the modules are connected to appropriate pins of the MPC board, which are inserted through the drilled-through holes of the board. Connections on the various layers of the board are made by way of printed wires. Printed wires are either made by etching process or by additive process. In order to connect wires between layers, plated-through holes, called vias, are provided on the MPC board.

In this paper we only deal with the routing problem of the over-all layout and we assume that placement of modules has been prescribed. There are three fundamental considerations in the design of a MPC board. The first deals with the question of feasibility of interconnection. In essence, given the placement and interconnection specification, we want to know whether interconnection can actually be made with a specified MPC board. Alternatively, we may ask what kind of requirements must be imposed on the design of the MPC board in order to meet the specifications of interconnection. The second consideration lies in the cost. Cost depends on many factors and is directly affected by such things as the size of the board, the number

of layers, the number of vias, etc. The third consideration is reliability. It is affected by the density distribution of wiring and vias as well as the number of vias needed. Therefore, given a set of feasible designs, the basic objective is to select one which is of minimum cost and maximum reliability.

There are two main difficulties in treating the routing problem analytically, namely: (1) the size of the problem is usually too large to permit global optimization, and (2) the secondary objectives and physical constraints are not clearly understood and often conflicting. For example, an optimum design with respect to minimum area may not be satisfactory in terms of reliability. Consequently, optimality is at best a fuzzy concept in the context of an over-all routing design. On the other hand, it is not difficult to introduce the concept of optimality at various stages of an over-all design if the problem can be meaningfully divided into simple subproblems, each amenable for analytical treatment. We shall introduce such an approach in this paper. The approach offers a systematic and sequential decomposition of the complex routing problem for the MPC board into four independent phases. Simpler design objectives can be stated at each phase and related as much as possible to physical parameters of the board. Local optimization in each phase can be achieved. The method also has a prognostic capability in the sense that routability can be expressed in terms of routing track requirement, and track requirement is of course directly related to cost.

It should be pointed out that although we deal with the routing of MPC boards. The method can be adapted to other technologies. For example, in MOS technology, the basic modules are in the form of regularly shaped blocks, called polycells, which have pins on two opposite sides of the

blocks. Interconnection is to be made between polycells with a maximum of two layers. The main objective is to minimize the in-between areas. Some of the algorithms developed in the present approach can be applied. However, the over-all problem is different and modifications are necessary. The present paper does not address problems other than the design of MPC boards. We always assume that modules are mounted on top of the MPC board and placement is specified in advance.

In Section 2 we shall introduce some preliminary concepts and motivations of our approach. A simple example will be given to illustrate our various objectives. The decomposition scheme will be discussed and illustrated in Section 3. The complexity of the decomposed phases will be analyzed. However, the details of each subproblem, i.e., the theory involved and the algorithms are not included in this paper. In Section 4, we shall give an overview of the implementation program. The results are illustrated with the routing of a processing unit of an ILLIAC IV board.

II. Preliminary Remarks

The present status of the routing problem leaves much room for improvement. Most commonly used methods depend mainly on heuristics and cut-and-try. The recent progress in miniaturization of electronic componenets has made it feasible to design high density circuits on a small MPC board. As circuit density increases, the complexity of the routing problem makes it more difficult to do the routing design manually. Various computer assisted approaches have been proposed [1-7]. The most widely used methods are extensions or modifications of the works of Lee [1] and Hightower [2]. In these approaches point-to-point connecting path is determined, one at a time, on the board. Large memory space and

computation time are usually required. Steven's channel routing approach [4] offers a quick way of doing routing design. However, vias are assigned on a demand basis and are random in location. This often creates a problem in reliability, as many vias may cluster in a small area. In 1974, H. So [6] developed a systematic approach to tackle the problem of routing MPC boards with regularly spaced columns of pins and vias. His method has the predictive ability for specifying requirements of the MPC board to achieve 100% routing. Our approach represents an extension and generalization of So's work. Thus we shall assume throughout that our MPC boards contain fixed locations for pins and vias.

Consider the MPC board as shown in Fig. 1. The pins marked by "x" and vias marked by "o" are arranged on regularly spaced rectangular grids. The separation distance between adjacent rows and adjacent columns dictates the track requirements, i.e., the maximum number of parallel wires that are permitted without causing serious cross talk or the possibility of short circuit. The interconnection specification may be indicated by a numbering system associated with the pins. For example, the pins with the same number as shown in Fig. 1 belong to the same signal net and should be connected together by wires. Depending on the nature of the problem, in addition to placement and interconnection specifications, there may exist various overriding considerations imposed on the board. For example, the number of layers may be fixed but the track requirement is flexible, or vice versa.

In order to have a better understanding of the routing problem in general, and the motivation of our approach in particular, let us consider a simple example as shown in Fig. 2a. We assume that the board has two layers only and there are four columns of pins and three columns of vias as shown. The five signal nets as specified by the numbers on the pins

are to be interconnected. We shall at the outset restrict our routes to be horizontal and vertical only. Furthermore, we adopt the strategy of the unidirectional-layer routing as introduced by So. Specifically, unidirectional-layer routing implies:

(E-1) Only points (pins or vias) on the same line (row or column) can be connected directly, and physical connections are confined within the two immediate channels of a given line.

(E-2) Connections for points on a row are made in one layer, and connections for points on a column are made in another layer.

With these assumptions in mind, a possible realization for the problem is found as shown in Fig. 2b. A realization is a complete specification of physical routes on the board such that all the signal nets are connected and no two nets intersect with each other. We can observe that there are three steps involved in obtaining the realization of Fig. 2b form the specification of Fig. 2a. For instance, net 3 consists of pins at coordinates (A,1), (A,2), (B,7) are connected through vias at coordinates (A,4) and (B,4) to form a connection pattern for the net: (A,1) - (A,2) - (A,4) - (B,4) - (B,7). The second step is the assignment of connection patterns of all the nets to different layers. The solid lines in Fig. 2b indicate connections in the first layer, and the dotted lines, the second layer. The third step is to route the wires in such a way so that nets do not intersect with each other. In the realization of Fig. 2b, there are altogether eleven horizontal tracks and nine vertical tracks. In Fig. 2c we show an alternative realization which has only eight horizontal tracks. The second realization is certainly superior to the first because less tracks imply less space needed or lower density.

The particular example brings out a number of points which deserve comments. First, vias are selected arbitrarily in routing a particular net. Judicious choices of vias at each step for each net are obviously an important factor in the over-all design. There exists actually the possibility of minimizing the number of vias required for interconnection. Second, after a particular set of connection patterns is obtained, we may consider permuting vias columns to reduce the number of tracks, thus obtaining more efficient designs. Third, in case of track congestions which violate the given track requirement, we may use more layers to distribute the concentration of wires. Finally, blockage is a problem which needs to be attacked, especially when we deal with the routing of large and complex nets. Layering is one way to handle the problem. There exist other possibilities after we reduce the over-all problem to the routing of a single line on a single layer. These will be elaborated in the next section. We shall divide the over-all problem into four distinctive phases. They are referred as vias assignment, linear placement of vias columns, layering and single line routing. It will be seen within each phase, some optimization will be undertaken to achieve specific aims.

III. The Approach

III.1. Via assignment

The first phase of our approach is vias assignment. The essence of this phase is to establish the fact that interconnection is feasible. This is accomplished by assigning appropriate vias in order to determine connection patterns of all the nets. A principal objective in this phase is to minimize the number of vias columns, thus reducing the size of the board or increasing the routing area. We shall illustrate this by way of an example.

Fig. 3a shows a two-layer board with four nets defined by the numbers on the pins. First, according to the constraint of the unidirectional routing some partial connections can be made without using any vias (e.g. pins of net 3 connected by horizontal connection on row B in the top layer, and pins of net 3 connected by vertical connection on column 1 in the bottom layer as shown). For convenience, we shall call a set of pins which belong to the same net and which are located on the same row and/or column a generalized pin. Thus, individual pins which belong to a generalized pin of a net can be connected without the use of vias. In this example we have three generalized pins which are shown in Fig. 3a when individually connected. In our strategy, connections for generalized pins are made first. For the remaining interconnection, vias must be used. The manner in which vias are selected is important. For example, Fig. 3b illustrates particular connection patterns which leave net 4 unconnected in spite of available vias on the board not used. On the other hand, Fig. 3c shows connection patterns in which all nets are properly connected. It should be pointed out that up to now we have not considered the actual physical routing of the nets. For example, as shown in Row A of Fig. 3c, net 1 and net 2 intersect with each other. In actual routing net 2 can be routed in the channel immediately below Row A. This aspect will be considered in the last phase of our method, the single-line routing. What we have seen in this example is that by selecting vias carefully we can obtain connection patterns for all signal nets with the vias columns provided. Furthermore, after the connection patterns are obtained, the problem is reduced to much simpler problems with routing specifications on a single line basis. In this problem there are eight single-line specifications, and each can be considered by itself. They are, as shown in Fig. 3c:

Row A: [(A,1),(A,2),(A,4)], [(A,3),(A,5)]

Row B: [(B,1),(B,2),(B,5)], [(B,3),(B,4)]

Row C: [(C,1),(C,4)], [(C,2),(C,3)]

Row D: [(D,2),(D,5)], [(D,3),(D,4)]

Column 1: [(B,1),(D,1)]

Column 2: [(A,2),(D,2)], [(B,2),(C,2)]

Column 4: [(A,4),(B,4)], [(C,4),(D,4)]

Column 5: [(C,5),(D,5)].

There are two fundamental features that we consider in this first phase of routing. In short we want to demonstrate the feasibility of interconnection with the use of a minimum number of vias. The first is to minimize the number of vias columns. The reason is obvious in view of the fact that a primary objective is to reduce the size of the board thus the cost. Our second feature is to minimize the actual number of vias used. The reason is that with less vias we enhance reliability. These two features have been analyzed and the problems have been formulated. It turns out that to obtain an optimum solution in each case amounts to solving an NP complete computational problem. The concept of NP completeness was first introduced by Cook [15] and Karp [16]. It means that the number of computational steps needed has no known polynomial bound. In another paper we demonstrate this fact and introduce heuristic algorithms which lead to locally optimum solutions [13].

III.2. Geometric placement of via columns

In our first example in Fig. 2, we gave two realizations for the same routing problem. In obtaining the superior realization in Fig. 2c, we did not start from scratch. Rather, we took advantage of the first

realization in Fig. 2b and made further improvement. It is clear that after a preliminary realization, we are at liberty to perturb the realization as long as we do not disturb the connection patterns. We know that because of fixed placement we cannot alter the location of the pins. Yet vias columns are less rigidly located. One obvious option which we have at our disposal is to permute the vias columns in order to reduce the number of horizontal tracks. In the example of Fig. 2c, this reduction was achieved by interchanging the first and the third vias columns. In Fig. 4 another example is shown where by using an optimum permutation of vias columns we again manage to reduce the horizontal tracks from that obtained by an arbitrary vias assignment shown in Fig. 3c.

The problem at hand can be stated succinctly. For a given vias assignment of a unidirectional-layer routing, what is the optimum placement of vias columns so that the maximum number of horizontal tracks is a minimum. Horizontal track is defined in terms of the number of horizontal connecting edges intersecting a vertical cut at an interval between points (pins or vias) on the board. This turns out to be a linear placement problem for minimizing density. It is again an NP complete problem. In another paper an algorithm is developed which guarantees a solution for the linear placement problem within a factor of $(1+\epsilon)$ from the optimum is presented [12,14].

III.3. Layering

After vias assignment and linear placement of vias columns have been carried out, the routing problem has been reduced to the much simpler problem of single-layer and single-line routing. At this stage we must take a look at the track requirement. The objective of layering is to allow more

layers for the purpose of evenly distributing the number of connecting edges at different layers. This was first proposed by So [6]. We are not going to dwell on this particular problem. However, in [14] we proposed a procedure implementing the idea in [6]. It should be mentioned that the reason it is possible to separate this aspect from the over-all problem is because of the constraints (E-1) and (E-2) imposed.

III.4. Single-line routing

At the completion of the layering phase, the original routing problem of a MPC board has been reduced to several single-line connection patterns on a single layer. A typical example is shown in Fig. 5a. Here, we do not distinguish between pins and vias. The specification is in terms of a net list connecting different points on the line. The problem is to find a physical realization of the net specification as represented graphically in Fig. 5a so that no two routes intersect with each other. In addition, we wish to pose the problem of minimizing the maximum number of horizontal tracks between points. However the interest here is with respect to the tracks on each side of the line called upper street and lower street. In Fig. 5b we show one realization which requires a total of seven tracks with four on the upper street and three on the lower street. In Fig. 5c we show an alternative realization with a total of five tracks, which represents the optimum. This problem has been thoroughly studied and sufficient and necessary conditions for minimum horizontal tracks have been found [10,11,14]. Theorems as well as routing algorithms are given. In particular, the most practical case with maximum track $\rho = 4$ has been treated in detail.

IV. Overview, Examples and Conclusion

In the previous sections we discribe the general problem of routing a MPC board and the approach we have developed. The details of the decomposed subproblems are given in other papers. The routing system has been implemented in Fortran on CDC 6400 computer. We shall illustrate the system by designing an ILLIAC IV processing unit with a two-layer board.

Figure 6a shows a processing unit of an ILLIAC IV processing unit with 20 modules fixed in location. The interconnection specification for the 55 nets is given by the numbers marked on the pins. With a two-layer routing, using the algorithms we developed in vias assignment, linear placement and single-line routing, we obtain a realization as shown in Fig. 6b and Fig. 6c. Altogether, 111 horizontal tracks and 47 vertical tracks are required. In the realization, vias columns are placed in the vertical space between modules. The horizontal space between modules is not used to provide vias. Considerable space has not been utilized, and obviously the realization given by Fig. 6b and Fig. 6c is not very efficient.

In order to make improvement from the above which is based on the direct approach of using vias columns only, we can modify it by dividing the board into different sections. Let us consider a particular case as shown in Fig. 7a where a board with 17 modules is to be designed. On the edge some input-output (I/O) terminals are prescribed. Figure 7b shows a direct approach with vias columns only provided between modules. Obviously, the space utilization for regions marked A and with shades is not efficient and could result in congestions of interconnection in other areas. To correct this fallacy, we divide the board into three sections as shown in Fig. 7c thus allowing both vias columns and vias rows to fill the board

evenly. In applying our algorithms, the vias assignment phase and the linear placement phase are mingled. An iteration procedure can be introduced between the two phases in the sense that vias assigned in one section are considered as pins when another section is treated. Sectioning is usually done on an ad hoc basis and it depends on the geometry of the placement.

For the example in Fig. 6a , we have also used the sectioning technique to complete the routing. With the three sections marked in Fig. 8a, the iteration procedure for the first two phases is used for Sections I and II first and then merged to the whole board. The result routing for the two layers is shown in Fig. 8b and Fig. 8c. Altogether there are 84 horizontal tracks and 56 vertical tracks. In Table 1, we summarize the pertinent results of the two realizations. It is seen that by using sectioning we can obtain a better space usage. On the other hand more vias are required for the second realization.

In conclusion, we have introduced a new approach to solve the routing problem of multilayer printed circuit board. The main advantage is that we have decomposed the complex problem into several independent phases. Therefore we can analyze each phase and obtain quasi-optimum solutions. The over-all procedure is summarized in the flow chart shown in Table 2. Further examples are given in a report [17]. The fundamental assumption here is that we have restricted ourselves to unidirectional-layer routing and this assumption is key to all phases in our approach.

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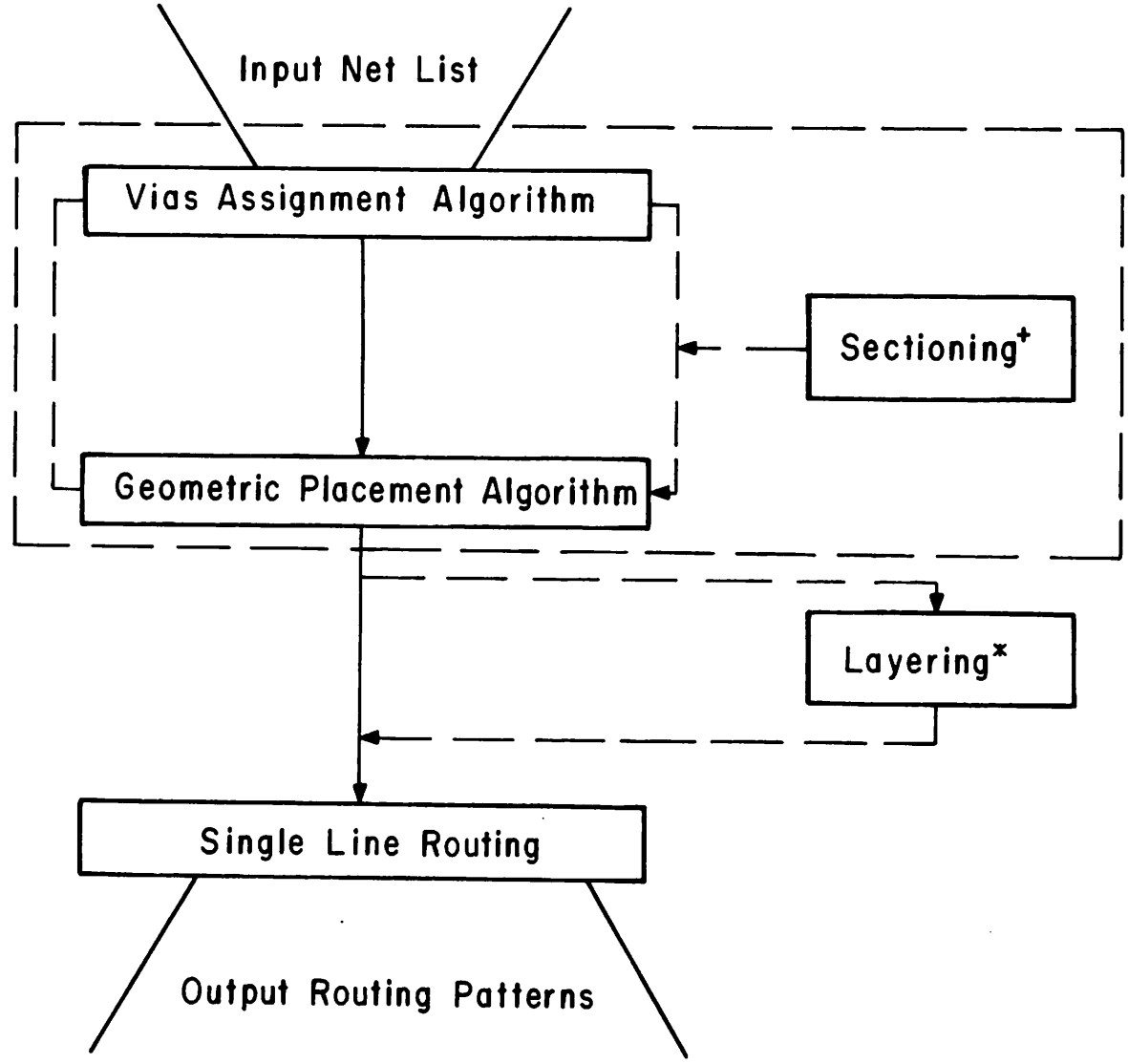
ILLIAC IV board.	no sectioning	sectioning
Number of pins on the board:	218	218
Number of generalized pins on the board (for nontrial nets):	130	130
Number of vias rows:	0	12
Number of vias columns:	7	7
Number of vias used:	130	145
Vias to pins ratio:	0.596	0.665
Number of horizontal tracks in the realization:	111	84
Number of vertical tracks in thr realization:	47	56

Table 1. Data for the realizations shown in Figs. 6 and 8.



+ manually done

* not implemented

Table 2. Flowchart of the routing system.

Figure Captions

Fig. 1. MPC board with pins and vias columns regularly spaced.

Fig. 2. (a) Five nets defined on a two layered board with regular geometry. (b) A realization with 11 horizontal tracks and 9 vertical tracks. (c) An alternative realization with 8 horizontal tracks.

Fig. 3. (a) Four nets to be connected. (b) Net 4 left unconnected. (c) All nets are properly connected.

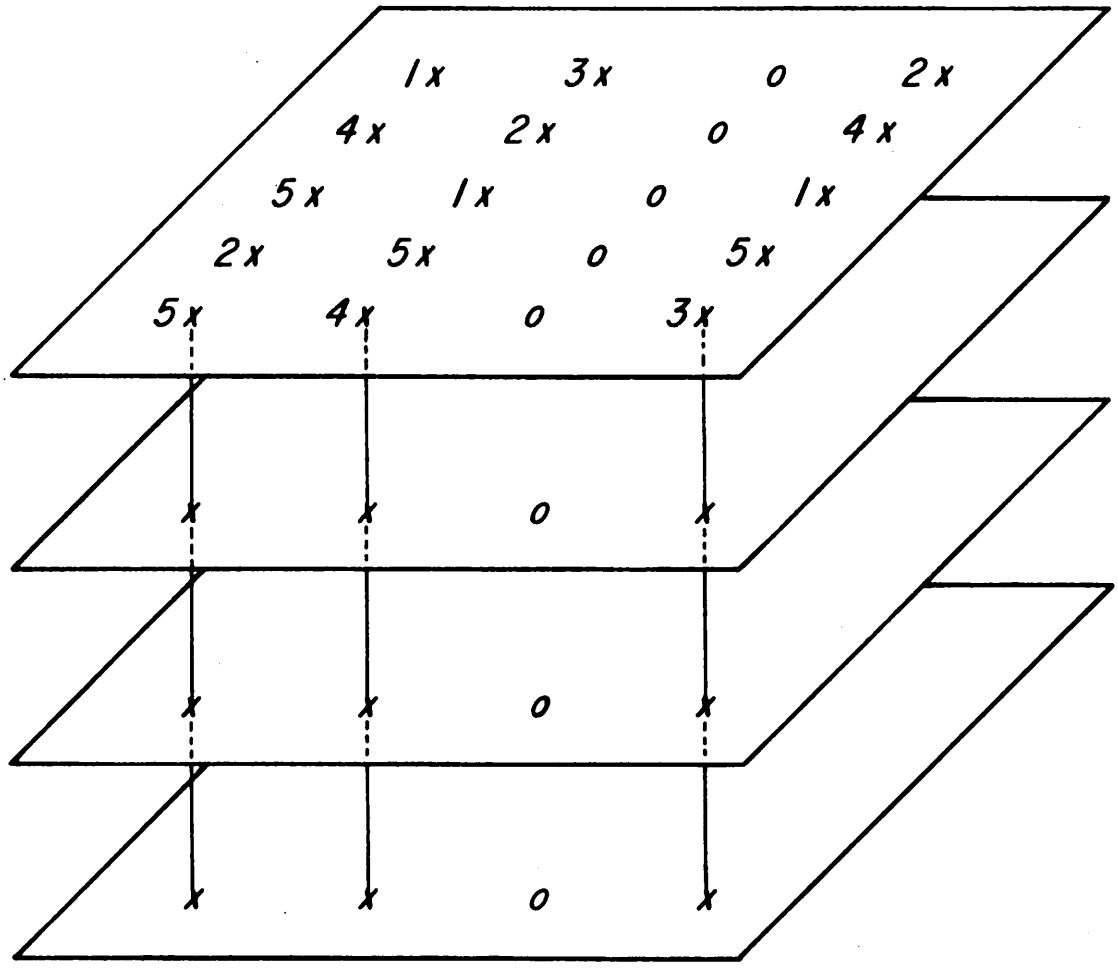
Fig. 4. (a) A realization of Fig. 3c with 8 horizontal tracks. (b) An alternative realization with 6 horizontal tracks.

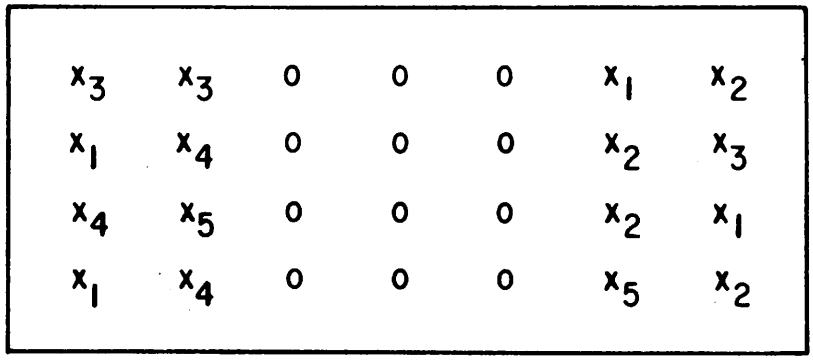
Fig. 5. (a) A graphical representation of a net list over a line. (b) A realization requires 4 tracks in the upper street and 3 tracks in the lower street. (c) An alternative realization requires 2 tracks in the upper street and 3 tracks in the lower street.

Fig. 6. (a) An ILLIAC IV processing unit. (b) Horizontal layer realization. (c) Vertical layer realization.

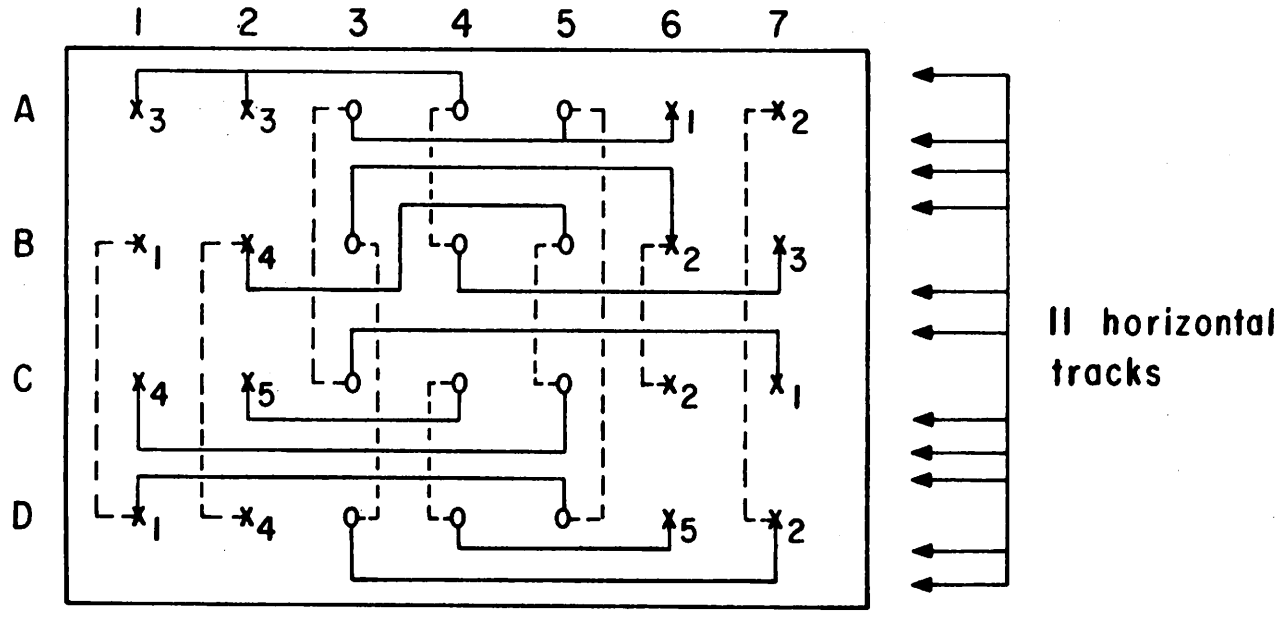
Fig. 7. (a) A board with 17 chips. (b) All vias appear columnwise. (c) Board divided into 3 sections, vias can appear rowwise.

Fig. 8. (a) An ILLIAC IV processing unit divided into 3 sections. (b) Horizontal layer realization. (c) Vertical layer realization.

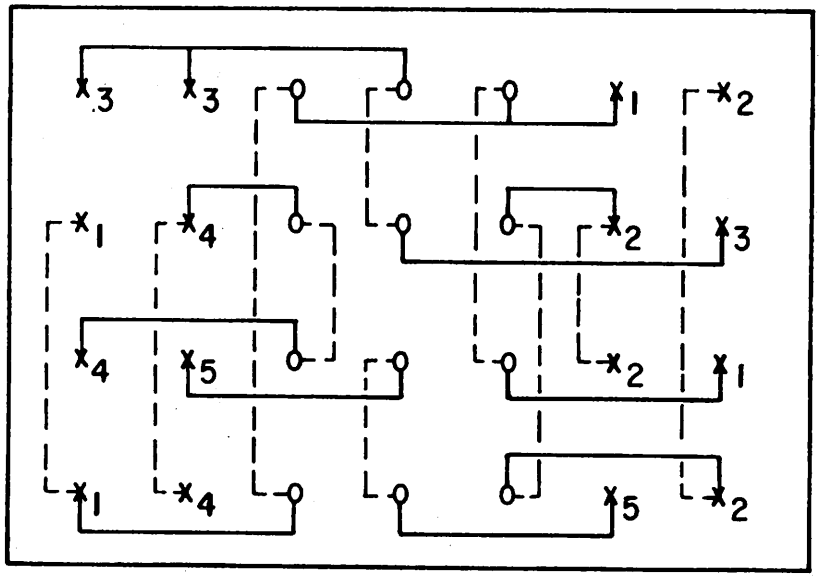

1x 3x 0 2x
4x 2x 0 4x
5x 1x 0 1x
2x 5x 0 5x
5x 4x 0 3x
x x 0 x
x x 0 x
x x 0 x


x3 x3 0 0 0 x1 x2
x1 x4 0 0 0 x2 x3
x4 x5 0 0 0 x2 x1
x1 x4 0 0 0 x5 x2

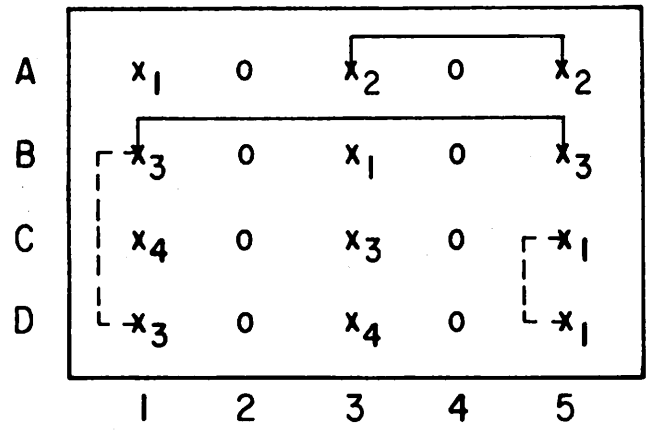
(a)


1 2 3 4 5 6 7
A
B
C
D
11 horizontal tracks

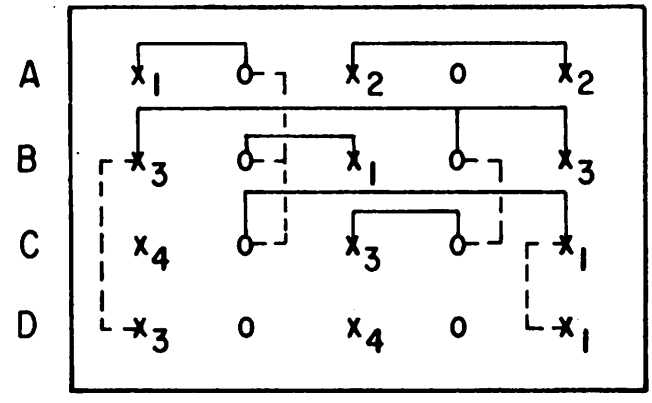
(b)



(c)



(a)



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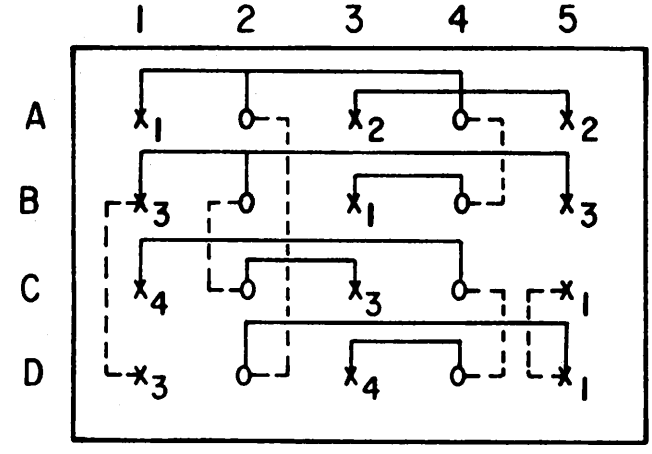
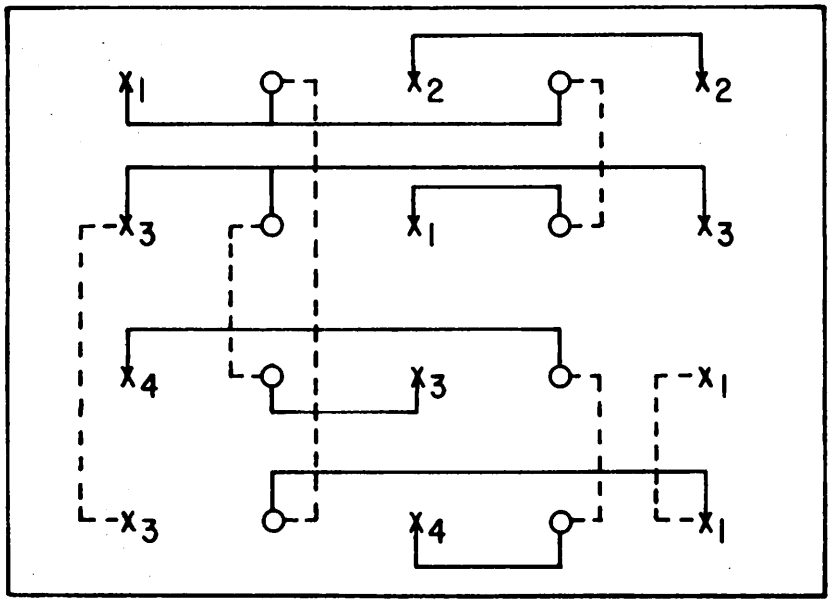
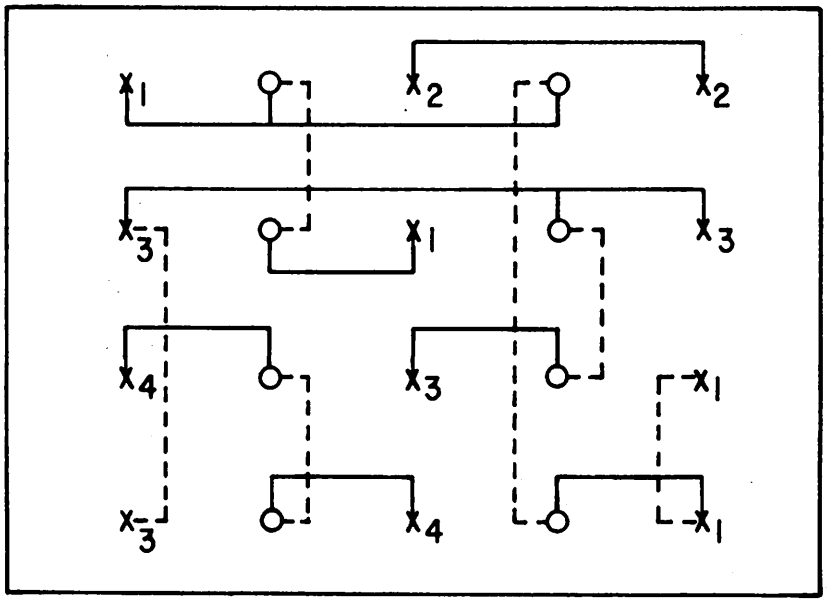


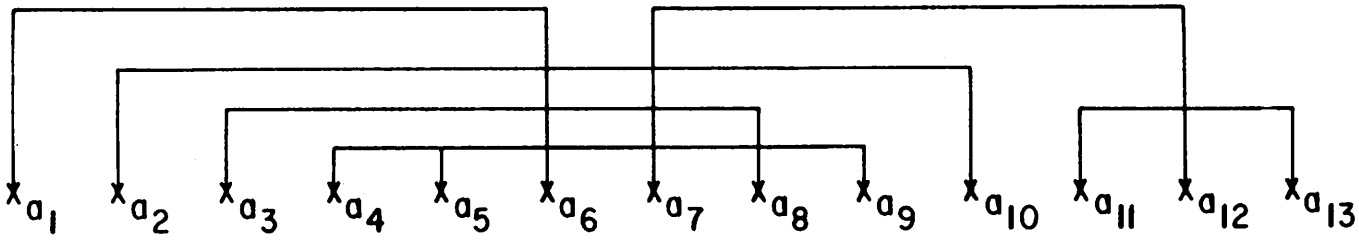
(c)



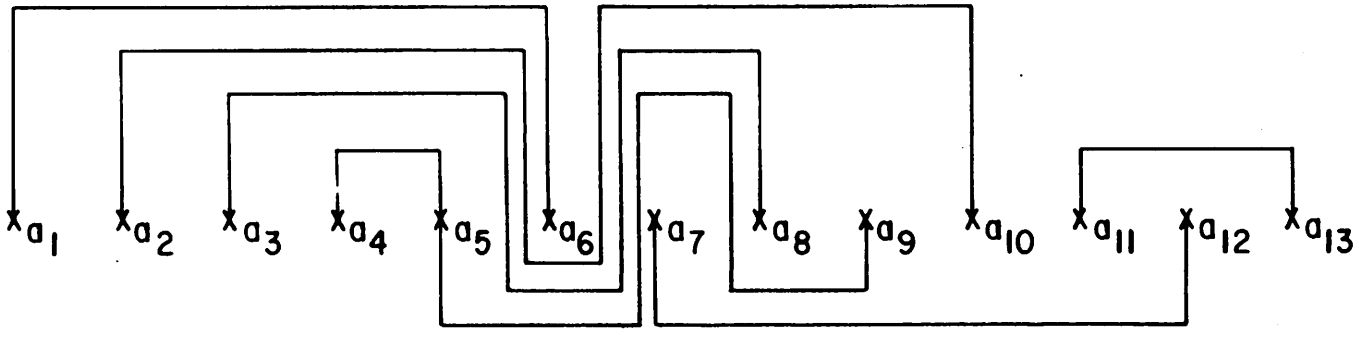
(a)



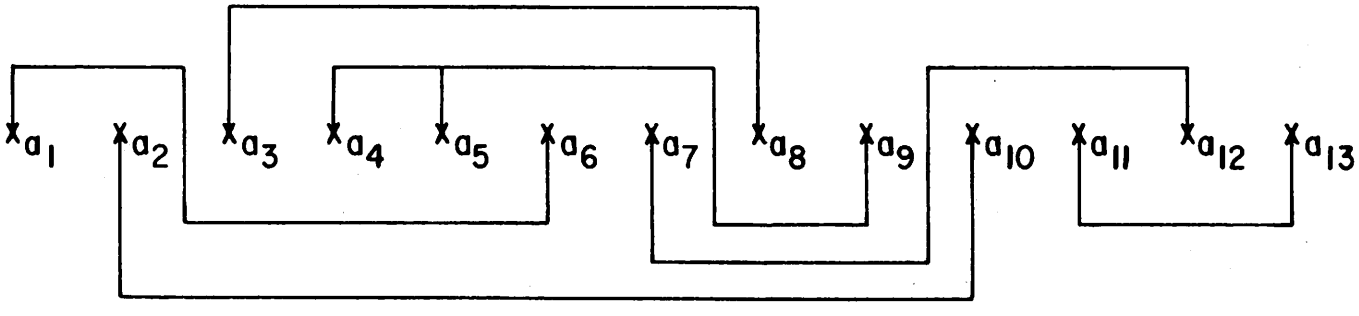
(b)


a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 a_9 a_{10} a_{11} a_{12} a_{13}

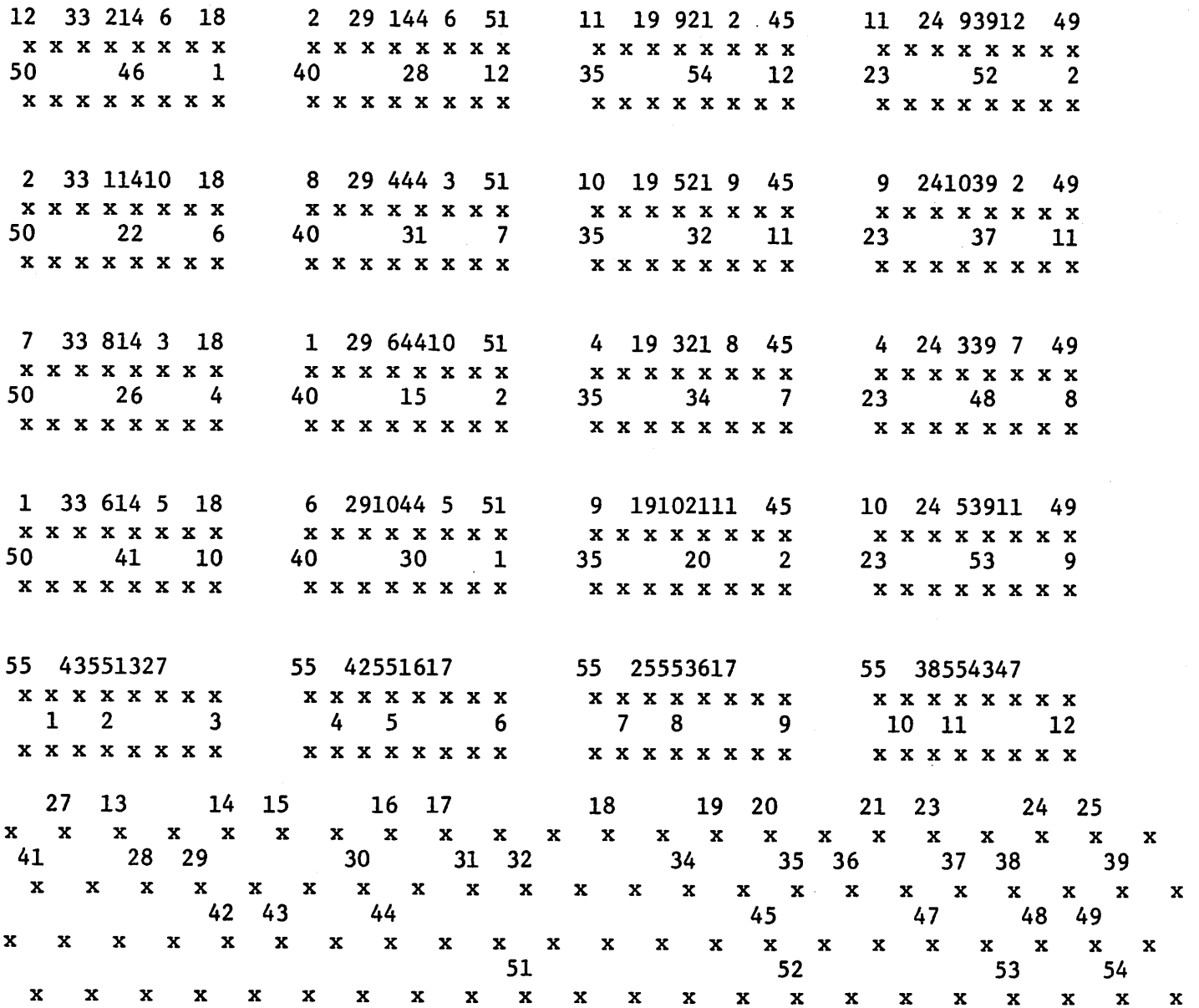
(a)

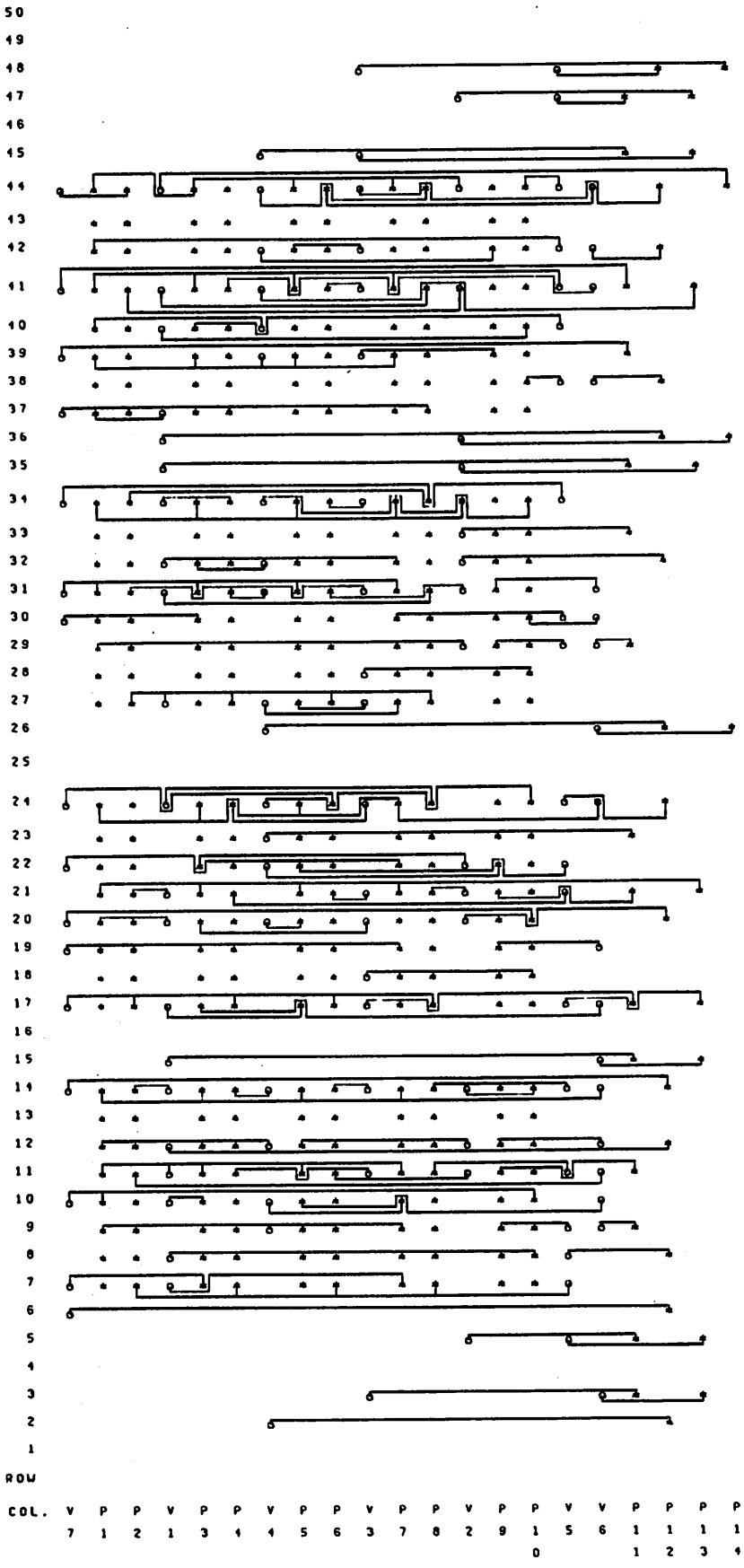

a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 a_9 a_{10} a_{11} a_{12} a_{13}

(b)

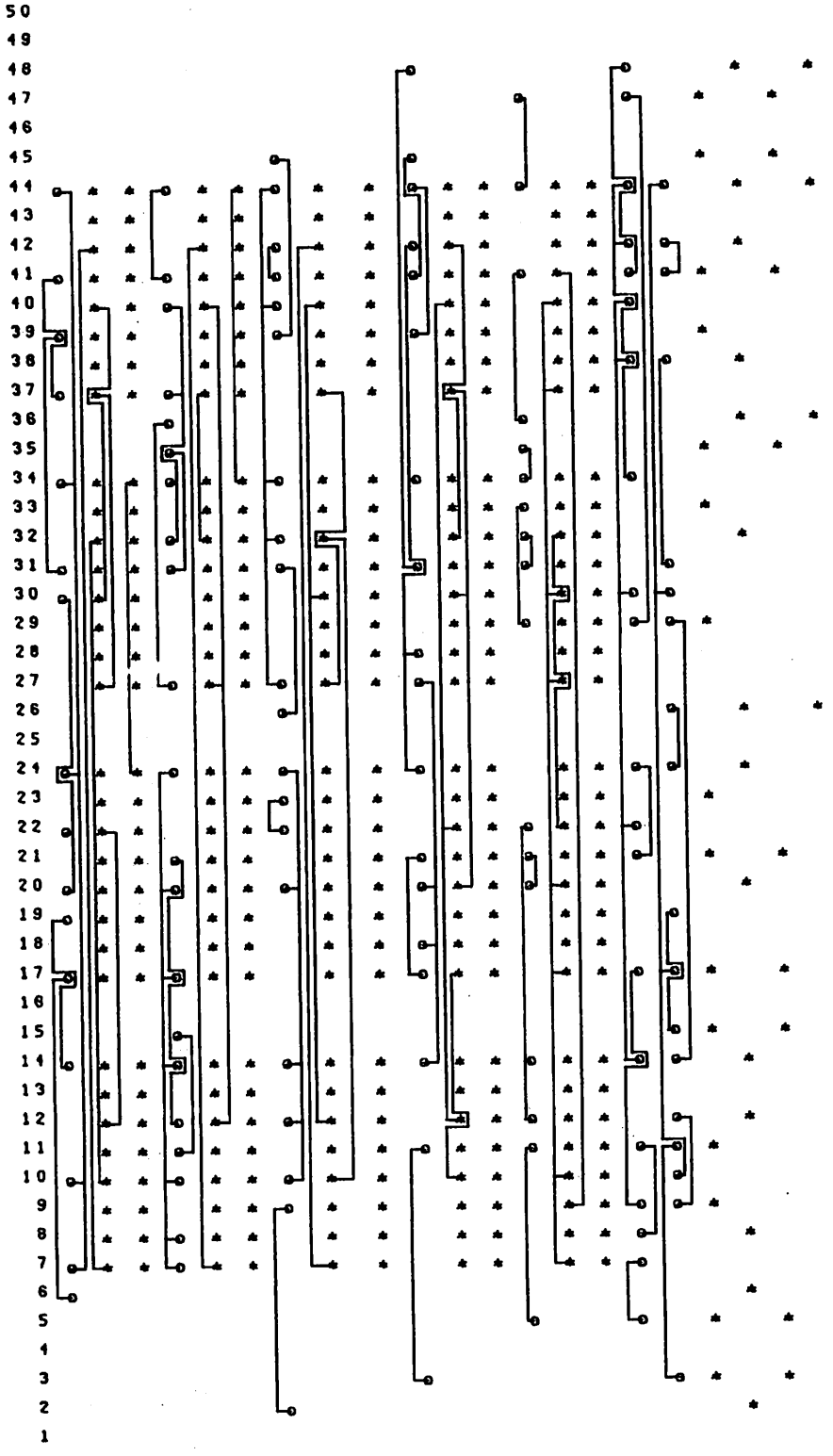

a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 a_9 a_{10} a_{11} a_{12} a_{13}

(c)

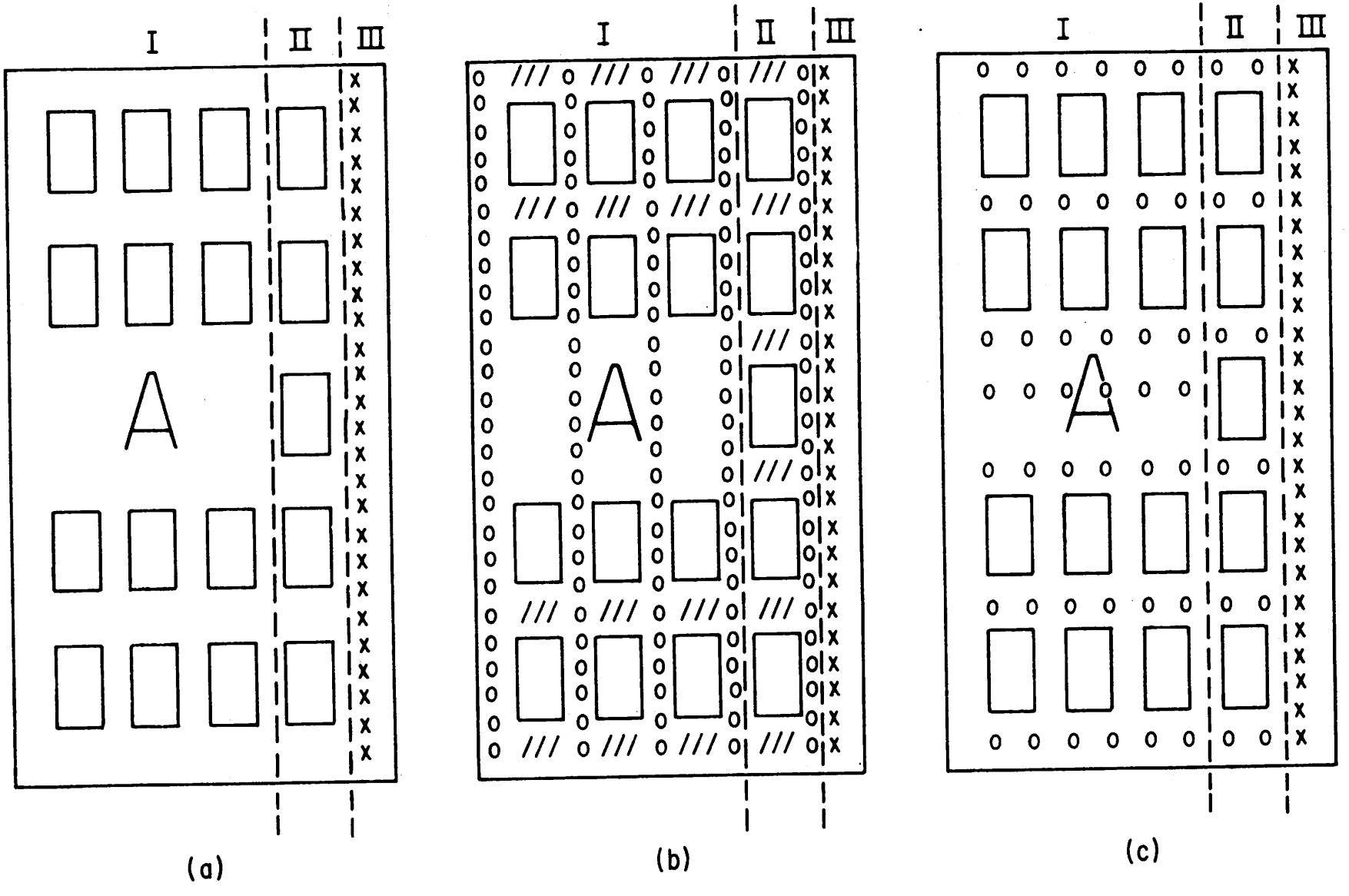

12 33 214 6 18
50 46 1
2 29 144 6 51
40 28 12
11 19 921 2 45
35 54 12
11 24 93912 49
23 52 2
2 33 11410 18
50 22 6
8 29 444 3 51
40 31 7
10 19 521 9 45
35 32 11
9 241039 2 49
23 37 11
7 33 814 3 18
50 26 4
1 29 64410 51
40 15 2
4 19 321 8 45
35 34 7
4 24 339 7 49
23 48 8
1 33 614 5 18
50 41 10
6 291044 5 51
40 30 1
9 19102111 45
35 20 2
10 24 53911 49
23 53 9
55 43551327
1 2 3
55 42551617
4 5 6
55 25553617
7 8 9
55 38554347
10 11 12
22 26 27 13 14 15 16 17 18 19 20 21 23 24 25
33 40 41 28 29 30 31 32 34 35 36 37 38 39
46 50 42 43 44 45 47 48 49
51 52 53 54



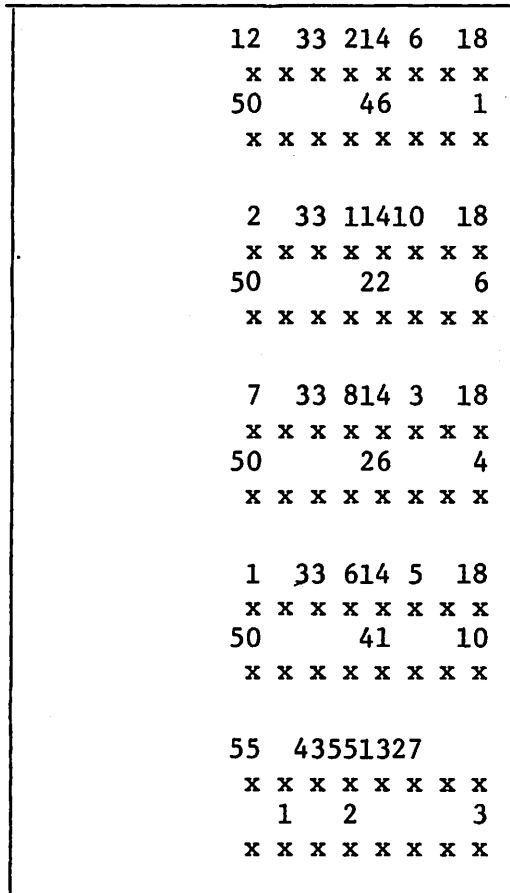
ROUTING OF A BOARD FROM ILLIAC IV CP UNIT.
HORIZONTAL LAYER, NON-SECTIONED.
NUMBER OF CHIPS= 20.
NUMBER OF SIGNAL NETS= 55.
NUMBER OF VIAS SELECTED= 130.
NUMBER OF TRACKS REQUIRED= 111.
KUH, TING, HORNG (OCTOBER 19, 1976)



ROUTING OF A BOARD FROM ILLIAC IV CP UNIT.
VERTICAL LAYER, NON-SECTIONED.
NUMBER OF CHIPS= 20.
NUMBER OF SIGNAL NETS= 55.
NUMBER OF VIAS SELECTED= 130.
NUMBER OF TRACKS REQUIRED= 47.
KUN, TING HORNG (OCTOBER 19, 1976)


I
II
III
A
(a)
(b)
(c)

I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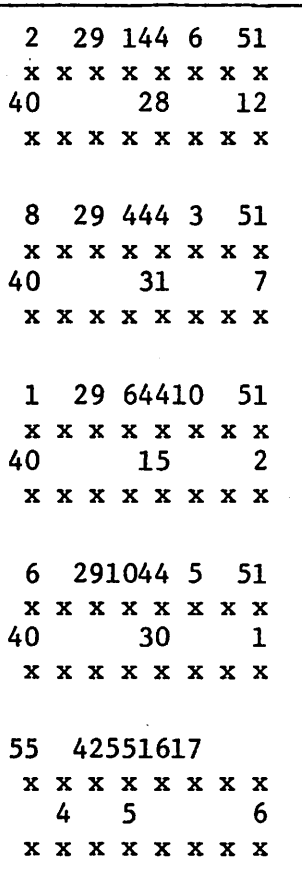
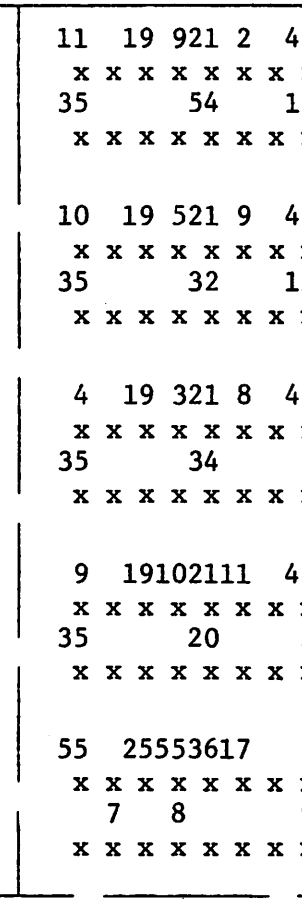
50 46 1
2 33 11410 18
50 22 6
7 33 814 3 18
50 26 4
1 33 614 5 18
50 41 10
55 43551327
1 2 3


2 29 144 6 51
40 28 12
8 29 444 3 51
40 31 7
1 29 64410 51
40 15 2
6 291044 5 51
40 30 1
55 42551617
4 5 6

II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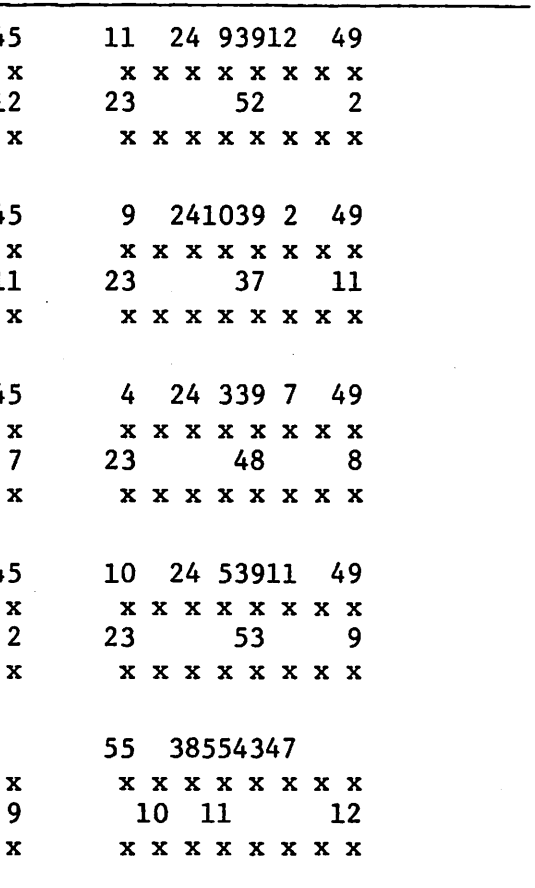
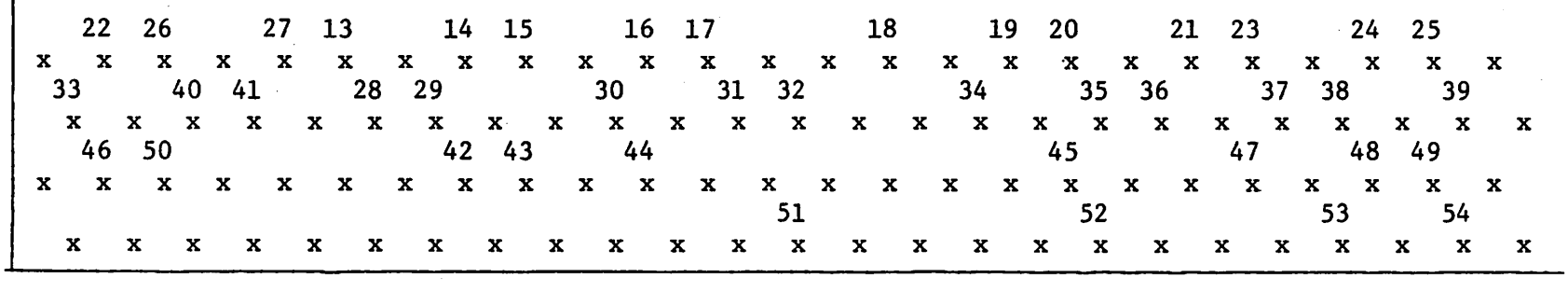
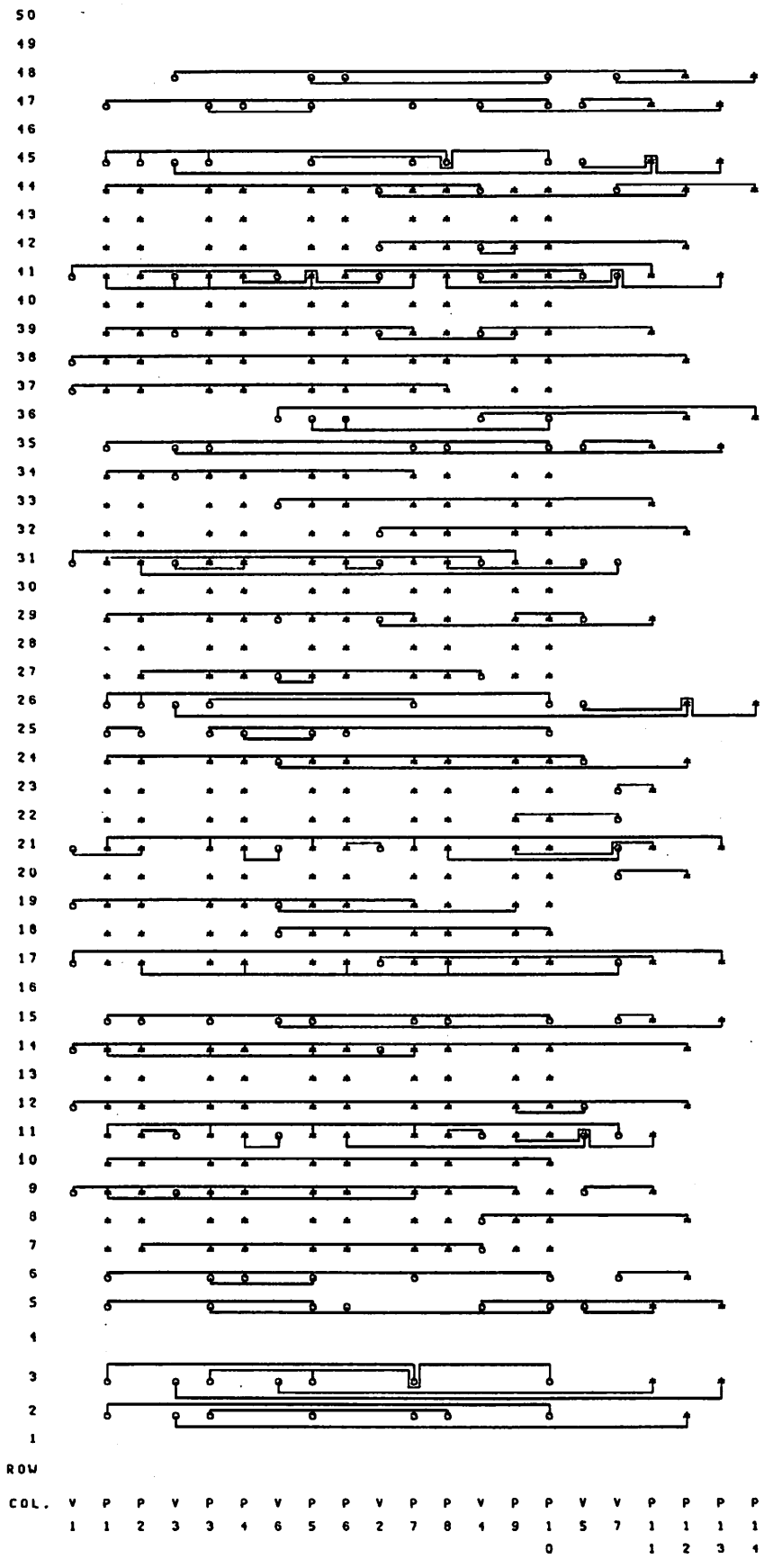
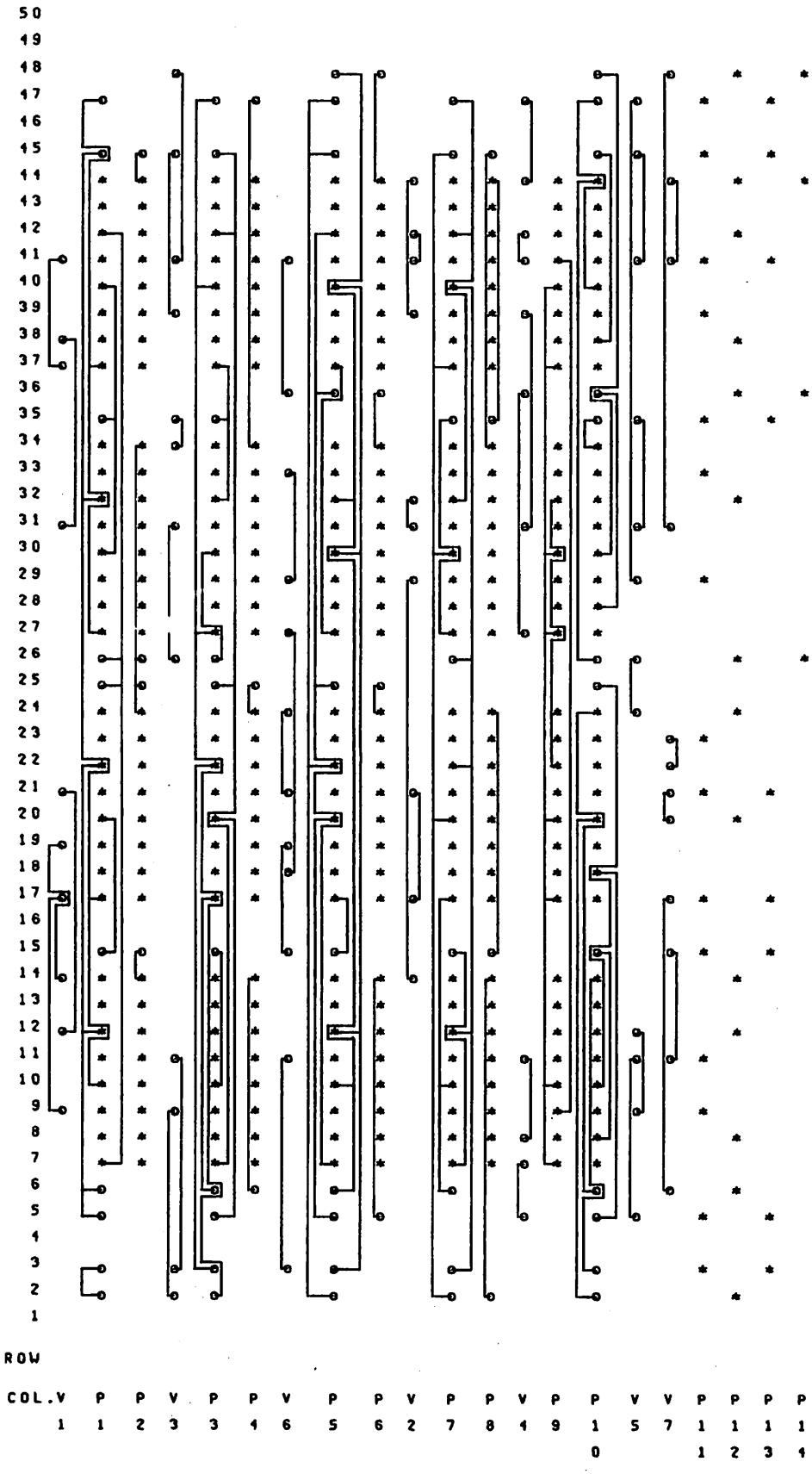
35 54 12
10 19 521 9 45
35 32 11
4 19 321 8 45
35 34 7
9 19102111 45
35 20 2
55 25553617
7 8 9


11 24 93912 49
23 52 2
9 241039 2 49
23 37 11
4 24 339 7 49
23 48 8
10 24 53911 49
23 53 9
55 38554347
10 11 12


22 26 27 13 14 15 16 17 18 19 20 21 23 24 25
33 40 41 28 29 30 31 32 34 35 36 37 38 39
46 50 42 43 44 45 47 48 49
51 52 53 54



ROUTING OF A BOARD FROM ILLIAC IV CP UNIT.
HORIZONTAL LAYER, SECTIONED.
NUMBER OF CHIPS= 20.
NUMBER OF SIGNAL NETS= 55.
NUMBER OF VIAS SELECTED= 145.
NUMBER OF TRACKS REQUIRED= 84.
KUH, TING, HORNG (OCTOBER 20, 1976)



ROUTING OF A BOARD FROM ILLIAC IV CP UNIT.
VERTICAL LAYER, SECTIONED.
NUMBER OF CHIPS= 20.
NUMBER OF SIGNAL NETS= 55.
NUMBER OF VIAS SELECTED= 145.
NUMBER OF TRACKS REQUIRED= 56.
KUH, TING, HORNG (OCTOBER 20, 1976)