HIGH-PERFORMANCE NMOS OPERATIONAL AMPLIFIER

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

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Daniel Senderowicz, D. A. Hodges and P. R. Gray
Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
University of California, Berkeley, California 94720

Abstract

A high-performance operational amplifier 300 mil^2 in area has been designed and fabricated in a standard N-channel silicon-gate enhancement-depletion MOS process. Specifications achieved include open-loop gain, 1000; power consumption, 10 mW; common mode range within 1.5 volts of either supply rail; unity-gain bandwidth, 3.0 MHz with 80° phase margin; RMS input noise (2.5 Hz-46 kHz), 25 μV; C-message weighted noise -5 dbrnc; and 0.1% settling time, 2.5 μs.

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I. Introduction

Operational amplifiers are necessary elements in LSI analog components such as charge-coupled device filters,[1] analog-to-digital converters,[2] and sampled-data recursive and state variable filters[3,4]. This paper describes a high-performance operational amplifier realized in a standard N-channel silicon-gate MOS process. This amplifier offers better performance, lower power consumption, and requires less silicon chip area than previous designs[5].

Compared to bipolar transistors, MOS transistors exhibit lower transconductance per unit supply current, poorer device matching, and higher equivalent input noise levels. On the other hand, MOS transistors are superior as low-offset analog switches and high input impedance amplifying devices. Modern MOS processes employing local oxidation, high resistivity substrates, and self-aligned device structures show extremely small parasitic capacitances and provide very high analog circuit density. Through proper use of the analog memory capability of MOS sampled-data circuits, the effects of device mismatching and flicker (1/f) noise can be greatly reduced. Overall, the performance of analog LSI based on MOS technology can match or surpass that of circuits based on bipolar technology in many applications, while providing markedly higher levels of integration.

II. Circuit Requirements

The operational amplifier described here is intended for use at audio frequencies. One to twenty or more amplifiers may be incorporated on a larger analog MOSLSI chip. An open-loop DC voltage gain greater than 1000 is typically needed to provide closed-loop gain accuracy

on the order of 0.1%. A unity-gain bandwidth greater than 2 mHz is necessary if the amplifier is to be useful throughout the audio frequency range. This requirement was to be met with internal phase compensation adequate to assure stability underall conditions. It was desired that the output be capable of driving at least 1 volt RMS into a 1000 ohm external load, and 2 volts RMS into a high-impedance load, but quiescent DC power consumption was required to be less than 20mW. Common mode rejection and power supply rejection greater than 60 dB were desired. RMS noise integrated over the audio band, referred to the input, was required to be under 100 microvolts. Finally, output settling time to 1% of final level for a 1 volt step input, unity gain operation, was to be under 2 microseconds when driving a 20 pF capacitive load. This is necessary to permit operation in sampled-data system with clock rates up to 250 kHz. Subject to all of the above requirements, device count and die area for the integrated amplifier were to be as small as possible. Also, the device must operate over a range of supply voltages from ± 5 volts to ± 10 volts.

Process Technology

N-channel MOS was chosen as the general technology for this work, in order to achieve maximum compatibility with high-density digital circuitry, charge-coupled devices, and precision-ratioed MOS capacitor arrays.

Depletion load devices are very useful in obtaining the high gain per stage required for an internally-compensated amplifier. All the desired process features were available to us in a standard silicon gate NMOS production process employed by Intel Corporation; the experimental amplifiers were fabricated on their line. The starting material was 35 ohm-cm p-type silicon and local oxidation was used in the field region.

Separately-masked implantations are used to set the threshold voltages of enhancement and depletion transistors. Two levels of polysilicon are employed, although the amplifier could have been made with a single layer of poly without penalty in performance. In this case, the non-precision capacitor could be realized between the polysilicon gate and implanted channel of a large-area depletion-mode MOS transistor.

IV. Overall Circuit Configuration

The maximum practical voltage gain obtainable with a single-stage MOS transistor amplifier with depletion-mode MOS load is on the order of 100. Thus a minimum of two stages are necessary to obtain open-loop gain of 1000. On the other hand, stability problems make an internally-compensated amplifier with more than three stages impractical. We chose a classical operational amplifier configuration employing two high gain stages followed by a near unity-gain buffer with low output impedance, as shown in Fig. 1. The first stage provides the differential to single-ended conversion with wide common-mode range. It has a high output impedance so that it functions as a transconductance amplifier. The second stage, designed as an integrator, almost entirely determines the overall gain and phase characteristics. The third stage, which employs local feedback to achieve low output impedance with broad-band voltage gain of about 1, makes it possible to drive low impedance loads without significantly affecting the overall gain and phase characteristics.

The small-signal low-frequency voltage gain is given by:

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} \qquad (1)$$

At low frequencies, these parameter are given by:

$$A_{V1} = g_{m1}/(g_{o1}+g_{i2}) \tag{2}$$

$$A_{V2} = g_{m2}/(g_{o2}+g_{i3}) \tag{3}$$

$$A_{V3} \simeq 1.0 \tag{4}$$

where g_m, g_o and g_i represent transconductance, input conductance and output conductance respectively for the stage denoted by the second subscript. Since the low frequency input conductance of MOS transistors is extremely small, the overall voltage gain is approximately

$$A_V = \frac{g_{m1}g_{m2}}{g_{o1}g_{o2}} \tag{5}$$

Obviously it is desirable to have high transconductances and low output conductances.

V. Depletion versus enhancement transistors as load devices

In light of the above discussion, it is probably clear that a gain stage employing depletion transistors as load devices (see Fig. 2b) would offer higher gain than a stage employing enhancement loads (Fig. 2a). The load line construction shown in Figure 3 illustrates this point for a case in which the desired bias point is at drain current I_{D1} and output voltage $V_{DD}/2$. A small-signal analysis of these two alternative cases (neglecting the output conductance of the active device) shows that the small-signal voltage gain for the depletion-loaded stage is given by:

$$A_{VD} = -\frac{2}{\gamma}\sqrt{\beta_R}\ \sqrt{V_0+V_{BB}+2\phi_F} \tag{6}$$

and for the enhancement-loaded stage by:

$$A_{VE} = -\sqrt{\beta_R}\left[\frac{1}{1+\frac{\gamma}{2\sqrt{V_0+V_{BB}+2\phi_F}}}\right] \qquad (7)$$

where: β_R = geometry ratio of active device to load device

V_0 = output voltage

V_{BB} = body bias

γ = body factor

ϕ_F = substrate built-in potential.

For a given value of β_R, the gain advantage for the depletion-loaded stage is given by:

$$\frac{A_{VD}}{A_{VE}} = \frac{2}{\gamma}\sqrt{V_0+V_{BB}+2\phi_F} + 1 \qquad (8)$$

For the parameters used in this circuit, i.e. V_{DD} = 10V, V_{BB} = 0, γ = 0.4, and ϕ_F = 0.3, the depletion-loaded stage gives 13 times higher gain at V_0 = 5V. The effects of active device output conductance, neglected in the above analysis, more seriously degrade the gain of the depletion-loaded stage. Nevertheless, 4 to 6 times higher gain is achieved in the depletion-loaded stage even when these effects are included. Note that the geometry ratio of an enhancement-loaded stage would have to be 4^2 to 6^2 larger than that for a depletion-loaded stage to achieve the same voltage gain. Penalties in die area and parasitic capacitance would be substantial.

VI. Circuit Description

A simplified schematic diagram for the complete operational amplifier is shown in Figure 4. A differential input stage M1, M2 is biased and

loaded with current sources. Two voltage level shifters, implemented with transistors as discussed later but shown here as batteries, drive a current mirror M17, M18 which provides differential to single-ended conversion while maintaining good common mode rejection. Output impedance of this state is relatively high.

The second stage consists of common-source amplifier M21 loaded with a current source. Capacitor C makes this stage perform as an integrator when driven from the high output impedance of the first stage.

The output buffer has high input impedance, low output impedance, and a voltage gain of approximately unity. It consists of M29, operating as a source-follower, and subcircuit B (described below) which has complementary voltage follower characteristics.

Important goals in circuit design were to minimize the sensitivity of amplifier performance to independent variations in absolute values of enhancement and depletion transistor threshold voltages, and to power supply variations.

A. Input stage

A more detailed circuit diagram for the input stage and level shifter is shown in Figure 5. The biasing current I_{D6} for the differential pair M1, M2 is derived using a current mirror of enhancement devices, M5, M6 biased with depletion device M7. The advantage over using a single self-biased depletion device in the M6 position is that arrangement shown has a lower minimum saturated drain voltage at the drain of M6, resulting in a larger input common mode range while retaining full gain.

The voltage gain of this stage may be approximated as follows. The differential to single-ended converter conveys the small-signal drain

currents from both M1 and M2 to the output, so the overall transconductance is $(g_{M1}+g_{M2})/2$. The output conductance as seen at the drain of M18 is dominated by the small-signal conductance of M4 as a load device. Provided M4 remains in saturation (i.e. for V_2 lower than $V_{DD}+V_{TD}$, where V_{TD} is necessarily negative), the overall voltage gain is given by:

$$A_{V1} \simeq \frac{2}{\gamma}\sqrt{\frac{(Z/L)_1}{(Z/L)_3}\ \frac{I1}{I3}\ (V_2+V_{BB}+2\phi_F)} \qquad (9)$$

The relationship between I4 and I6 is a compromise between gain and slew rate for the complete amplifier.

If I3 and I4 are larger than I6, the maximum charging current for the compensation capacitor is I6. But if I3 and I4 are made too large, the dynamic conductance of M3, M4 significantly reduce the voltage gain. For I4 is smaller than I6, slew rate is sacrificed but gain is improved. We chose I3=I4=I6, which provides the gain required with an acceptable slew rate.

When the noise performance of the complete amplifier was simulated using SPICE[6] and based on the referred input voltage, load devices M3, M4 and M17, M18 proved to be a major sources of 1/f noise. A first-order noise model for MOS transistors shows that total 1/f noise output at a fixed bias point is inversely proportional to gate area.[7] In order to reduce noise, we increased gate width and length of M3, M4 in proportion, increasing gate area without any first-order effect on the desired dc operating conditions.

An important parameter for general-purpose operational amplifiers is common-mode range. In this circuit, the common-mode range in the positive direction is determined by the quiescent voltages V1 and V2. For best common-mode range without sacrificing gain, the voltage across M3 and M4

should be slightly greater than the magnitude of the depletion-mode threshold voltage, V_{TD}, independent of the supply voltage. Thus the level shifter voltage V_{LS} should be a function of $V_{DD}+V_{TD}$. If this condition is met, voltage gain and common mode range for the input stage will be maximized, independent of V_{DD} and V_{TD}. The level shifter circuit designed to meet this objective while minimizing internal dynamic series impedance is shown in Fig. 6.

B. Level shifter

The level shifter is designed so that V1=V2=V9 as a dc bias condition. his voltage level is set at $V_{DD}-|V_{TD}|$, as desired for maximum gain, by design of M8 and M9.

$$V9 = V_{DD}-V_{T8}\left[1 - \sqrt{1 + \left(\frac{V_{T9}}{V_{T8}}\right)^2 \cdot \beta_R\left(\frac{9}{8}\right)}\right] \qquad (10)$$

where $\beta_R(\frac{9}{8})$ denotes the ratio $(Z/L)_9/(Z/L)_8$. By properly choosing the geometry ratio, β_R, for M9, M8 the quantity within the brackets may be made equal to -1, thus achieving $V9 = V_{DD}+V_{TD}$, which is the desired operating point for the load devices M3 and M4.

The voltage V9 is transferred to the gates of M11 and M12 as follows. M10, M11, and M12 are identical long-channel devices (small Z/L) biased at identical relatively large gate-source voltages. Since the double current mirror M15, M16, M19, M20 is composed of high transconductance devices (large Z/L) the gate-source voltage is small, allowing a large gate-source voltage for M10, a smaller device. The current in M10 is mirrored by M19, M20 and flows in M15, M16. Devices M11 and M12 act as feedback elements for M13 and M14 respectively. Therefore the voltage at the drains of M13 and M14 is determined by the current through M11 and M12.

This results in identical gate-source voltages for M10, M11, and M12, which in turn yields the desired quiescent value for V1 and V2.

The dynamic series resistance of the level shifter must be low to avoid any significant phase shift for signals passing through it. If M13-M14 have large Z/L ratios compared to M11-M12, the equivalent series resistance through the level shifter is approximately $1/g_{m13}$; or about 6000 ohms in this circuit.

C. Integrator

Figure 7 shows a schematic diagram of the integrator stage. M21 and M23 form a cascoded inverting amplifier with higher output impedance than would be obtained with M21 alone. M24 is the load device, while M22 provides a constant component of drain current for M21 which raises its transconductance without raising the current which flows in M23 and M24. This strategy increases the gain available, which is approximately given by:

$$A_V = \frac{2}{\gamma} \sqrt{\beta_R \left(\frac{21}{24}\right) \frac{I_{D21}}{I_{D24}} (V_0+V_{BB}+2\phi_F)} \qquad (11)$$

From (10) it would appear that the ratio I_{D21}/I_{D24} should be made as large as possible (for instance, by increasing the current in M22). However, this would reduce the current available from M24 to charge the integrator capacitance C. The current in M24 must always be larger than the signal current from the previous stage if the integrator is to remain effective for large signal swings. These considerations fix the minimum value of I_{D24}.

The gain transistor M21 must have a large transconductance, both to achieve a high gain and to minimize the undesirable effects of the

transmission zero on the positive real axis caused by integrator capacitor C. Transistor M31 gives a zero at a frequency corresponding to the open-loop second dominant pole, improving both frequency response and phase margin. The upper limit on the transconductance of M21 is determined mainly by permissible die area. The final value of Z/L chosen for this device is 65.

As a final design consideration, we wish to minimize the variations in amplifier input offset voltage as a function of variations in supply voltages and transistor threshold voltages. This suggests the desirability of designing so that the quiescent gate-source voltage and drain current density in M21 is the same as in M17-M18 in the previous stage.

D. Output stage

A broad-band unity-gain stage with low output impedance is desired. Gain accuracy is not critical. A complementary MOS source follower would perform very well. In an NMOS process, similar results are achieved following the idea indicated in Fig. 8, which represents the block B in Figure 4. If a transconductance amplifier of gain g_f drives a trans-resistance amplifier of gain r_r, the overall voltage gain is

$$A_{V3} = (-g_f)r_r.$$

A gain of approximately 1 is easily achieved. The actual circuit of the output stage is shown in Fig. 9. The transconductance stage is formed of M25, M27 and M28. The voltage amplifier with a gain of approximately 10 is formed by M30, M29 if the gate of M29 is driven by the input signal as shown. Transistor M26 behaves as a feedback resistor of $1/g_{M26}$ ohms, resulting in the desired transresistance characteristics. When M25 and M26 are identical in geometry, the overall stage gain is approximately unity.

of this stage is approximately

$$R_0 = \frac{1}{g_{m29}+g_{m30}} \qquad (12)$$

The actual value of R_0 in the final design is about 800 ohms.

The complete schematic for the amplifier is shown in Fig. 10. Device sizes are listed in Table I. A die photograph of the amplifier is shown in Figure 11; die area for the amplifier excluding bonding pads is about 200 mil^2.

VII. Results

Circuit analysis programs SPICE[6] and ASPEC were extensively used for design. Simulation gave correct predictions of final performance in all respects. The amplifier shows excellent stability, as well as wide input and output common mode range, comparable to amplifiers employing complementary devices. Measured characteristics for the final design are tabulated in Table II. Figures 12 and 13 show the simulated and actual voltage follower response respectively. Figure 14 is a 6 volts step response, and Fig. 15 is a DC transfer curve. Figure 16 shows a noise spectrum. The C-message weighted noise is -5 dbrnc and the broad-band noise 2.5 Hz to 46 KHz is 25 μV.

VIII. Conclusions

This work has shown that a general-purpose operational amplifier with good overall characteristics is feasible in N-channel silicon gate MOS technology. Compared to standard bipolar transistor operational amplifiers such as the 741, the amplifiers reported here is inferior in input offset, internal noise gain, and load driving capability. However, it is quite adequate

for many applications, and the small die area required points the way to feasible large-scale integration of important analog systems such as pulse code modulation voice encoders[8] and analog sampled data filters.[9]

XI. Acknowledgement

Intel Corporation provided circuit fabrication and assistance in evaluation of the amplifier. We thank Dennis Langley and Ben Warren for their efforts and encouragement.

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Transistor No.	Type Threshold	Width(μ)	Length(μ)	ID(μA)
M1	Enh	120	10	16.0
M2	Enh	120	10	16.0
M3	Depl	30	36	56.1
M4	Depl	30	36	56.1
M5	Enh	120	14	28.1
M6	Enh	120	14	32.1
M7	Depl	30	100	28.1
M8	Depl	10	70	27.7
M9	Depl	10	35	27.7
M10	Enh	8	100	23.2
M11	Enh	8	100	19.4
M12	Enh	8	100	19.4
M13	Enh	120	10	40.1
M14	Enh	120	10	40.1
M15	Enh	120	10	19.4
M16	Enh	120	10	19.4
M17	Enh	120	10	40.1
M18	Enh	120	10	40.1
M19	Enh	120	10	23.2
M20	Enh	240	10	38.8
M21	Enh	657	10	254.7
M22	Depl	30	20	158.9
M23	Depl	80	8	95.9
M24	Depl	30	27	95.9
M25	Depl	8	80	33.6
M26	Depl	8	80	34.2
M27	Enh	60	8	33.7
M28	Enh	60	8	34.3
M29A	Depl	85	8	150.0
M29B	Enh	24	12	0.0
M30	Enh	200	8	150.0
M31	Depl	8	10	0.0
C1				8 pF

Table I

Process	Si gate E/D
Circuit area	(0.18 mm^2)
Open loop gain	1000
Input offset	<15 mV
Supplies	+5, -5
Supply current (no load)	1.0 mA
Common mode range	$\pm$3.5 V
Common mode rejection	75 db
Unity-gain bandwidth	3.0 MHz
Phase margin	80°
Positive/negative slew rate	2.2/2.2 V/μs
RMS noise, referred to input	25 μV (2.5Hz-46kHz)
0.1% settling time, 1 V step	2.5 μs

Table II. Typical measured parameters on NMOS operational amplifier.

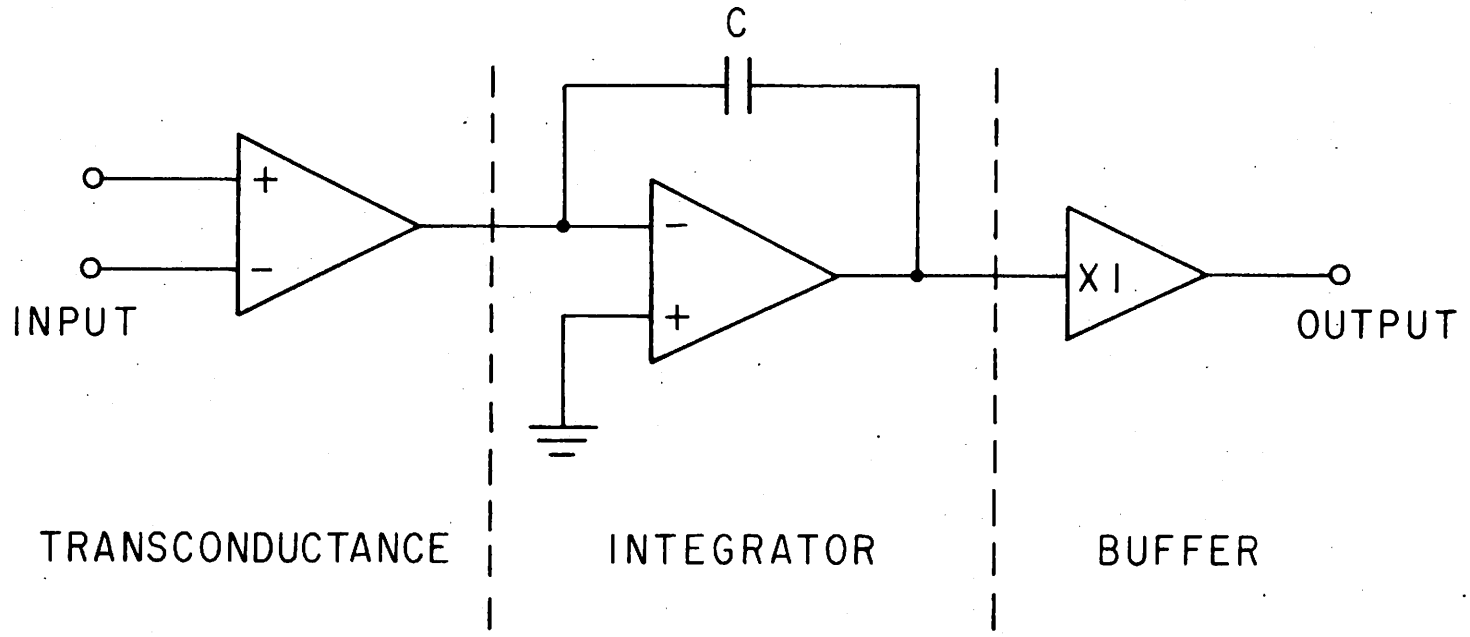


Fig. 1. Block architecture of the OP AMP.

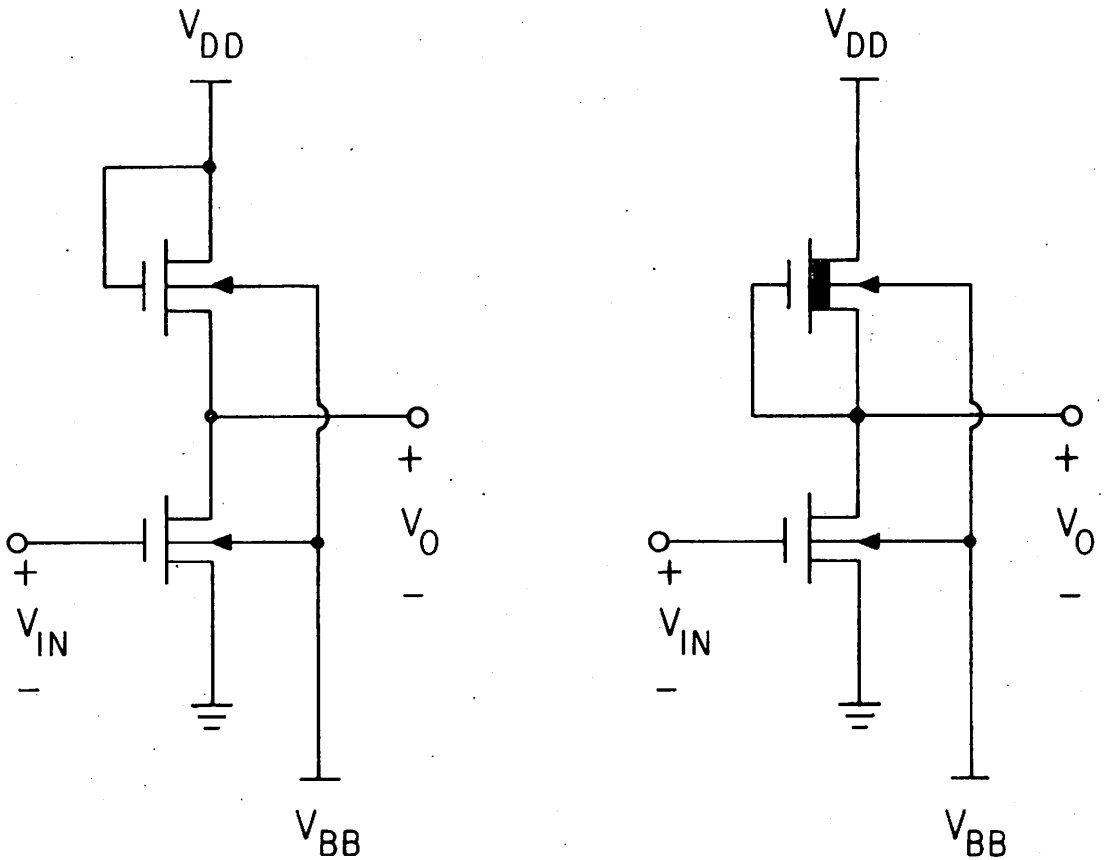


Fig. 2. Inverter stages realized with enhancement and depletion loads.

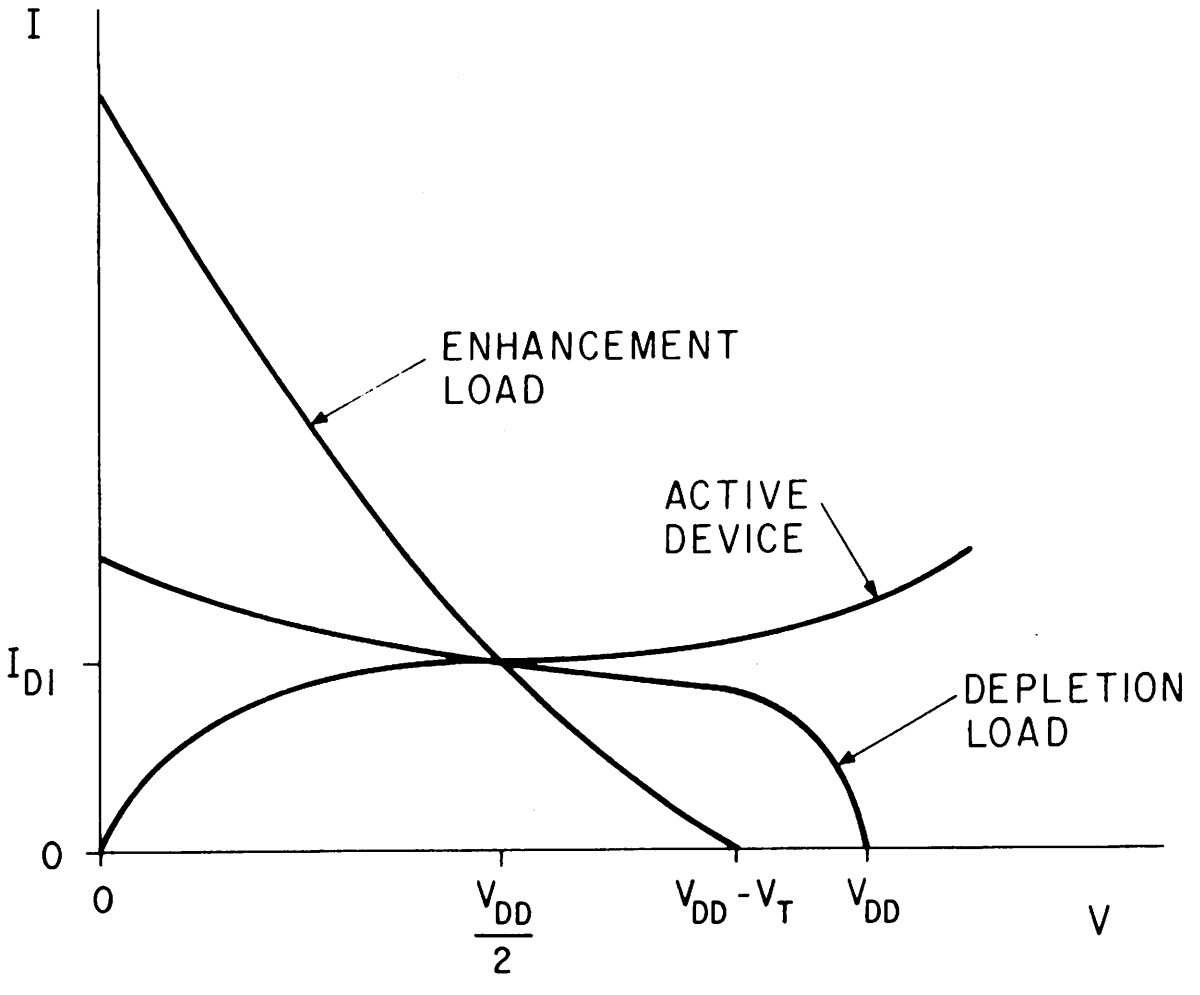


Fig. 3. Load characteristics of enhancement and depletion loads.

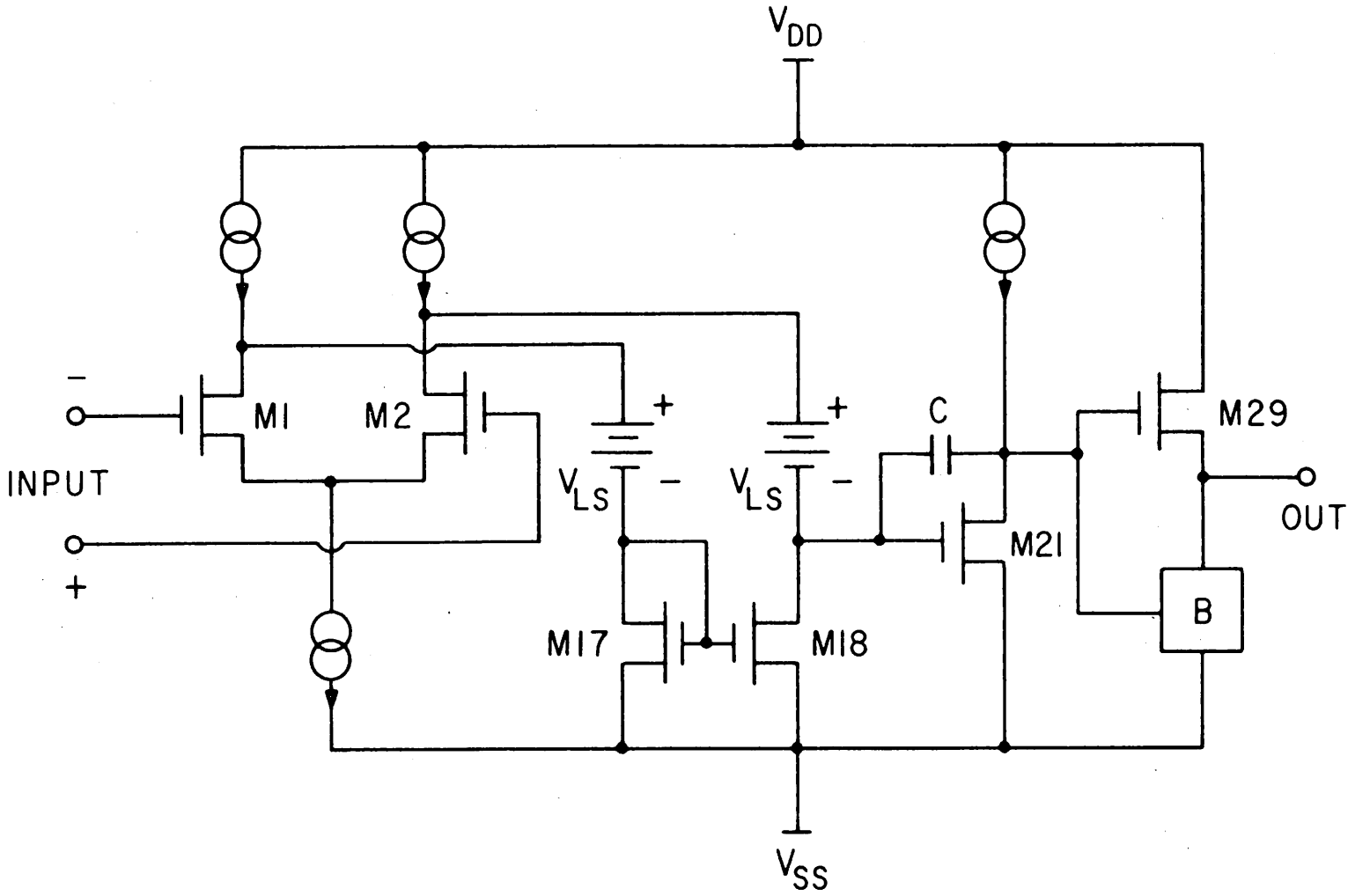


Fig. 4. Simplified circuit schematics of the OP AMP.

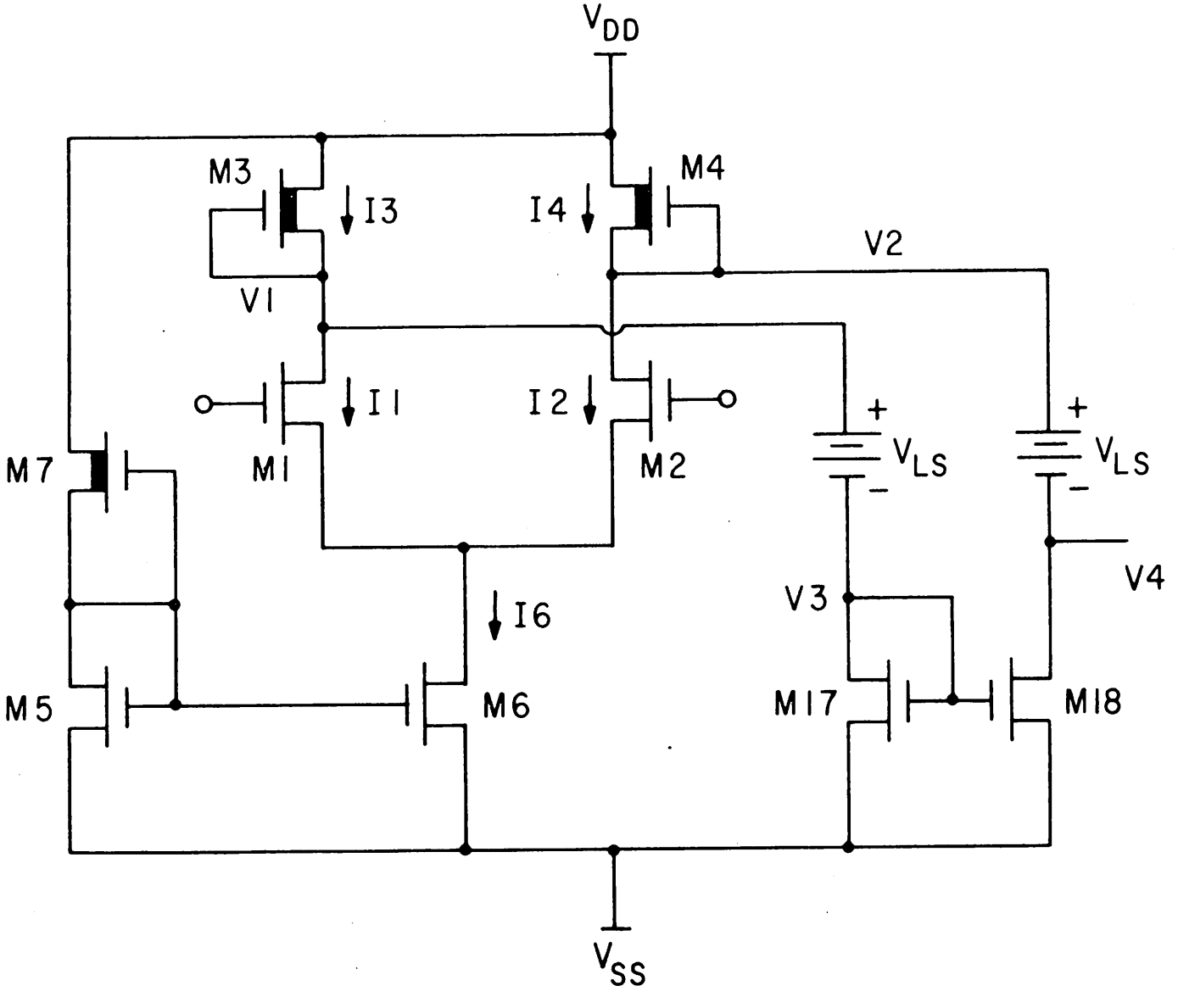
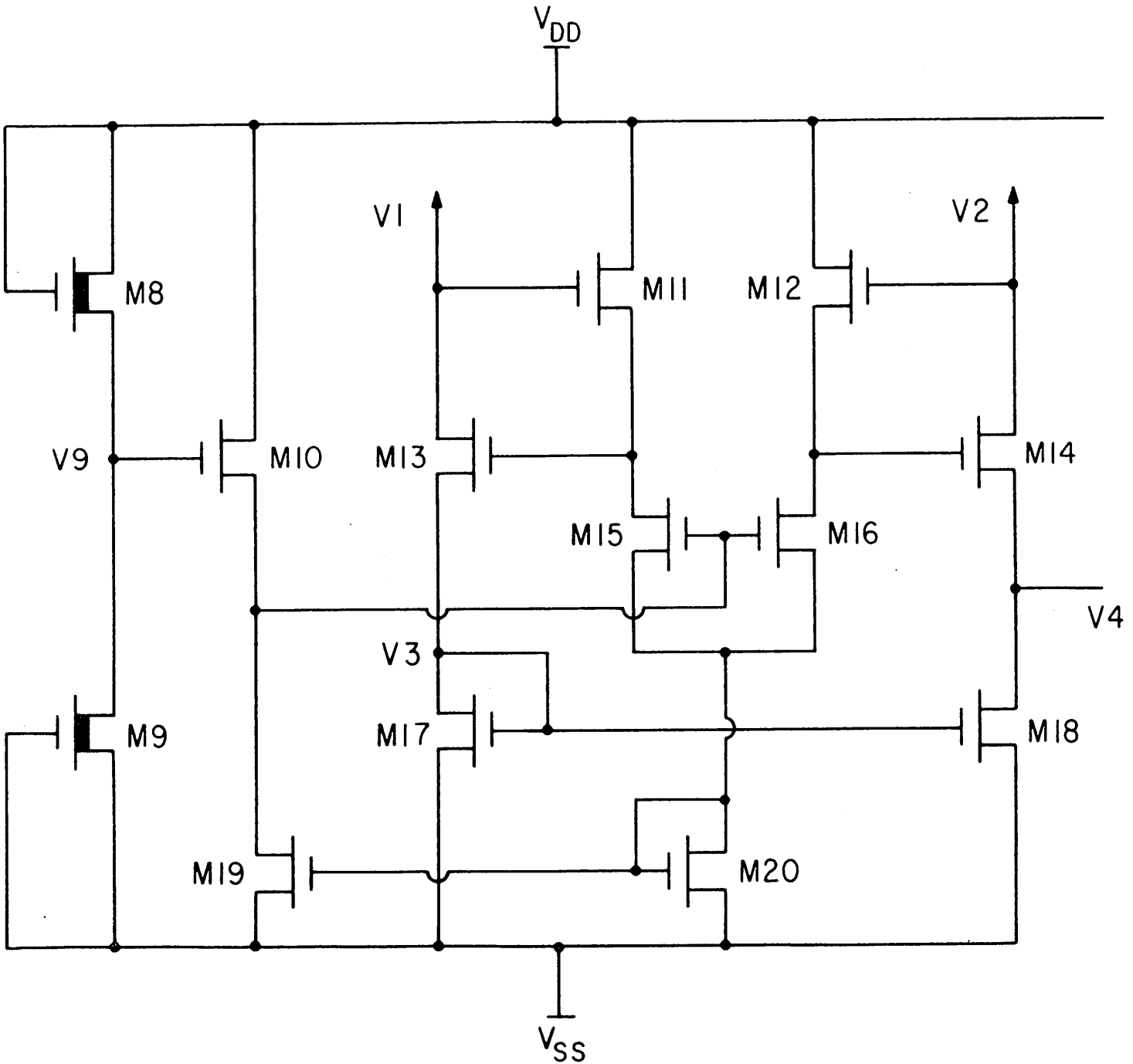


Fig. 5. Input stage and simplified level shifter.

Fig. 6. Detailed circuit schematics for level shifter and differential to single ended converter.



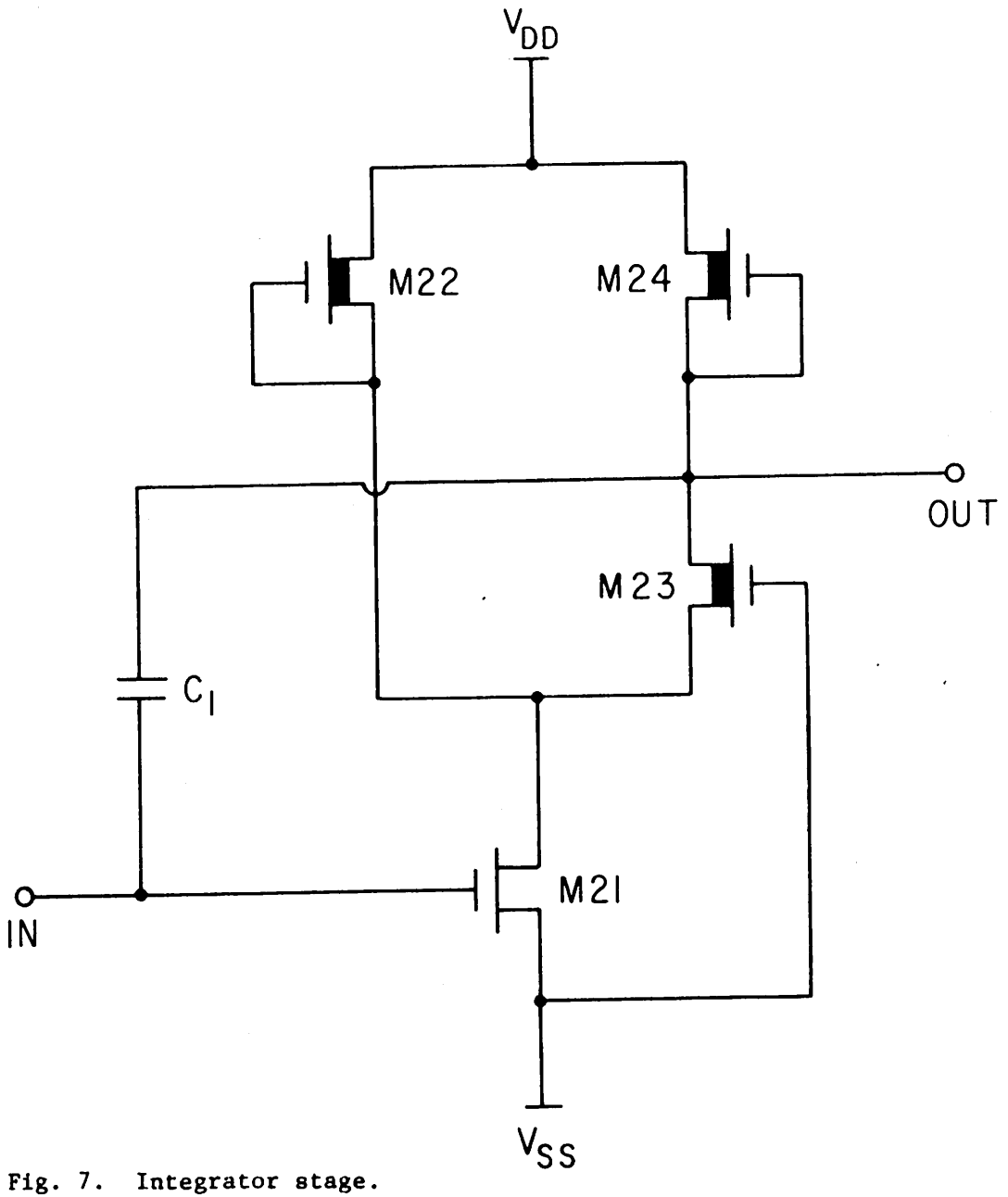


Fig. 7. Integrator stage.

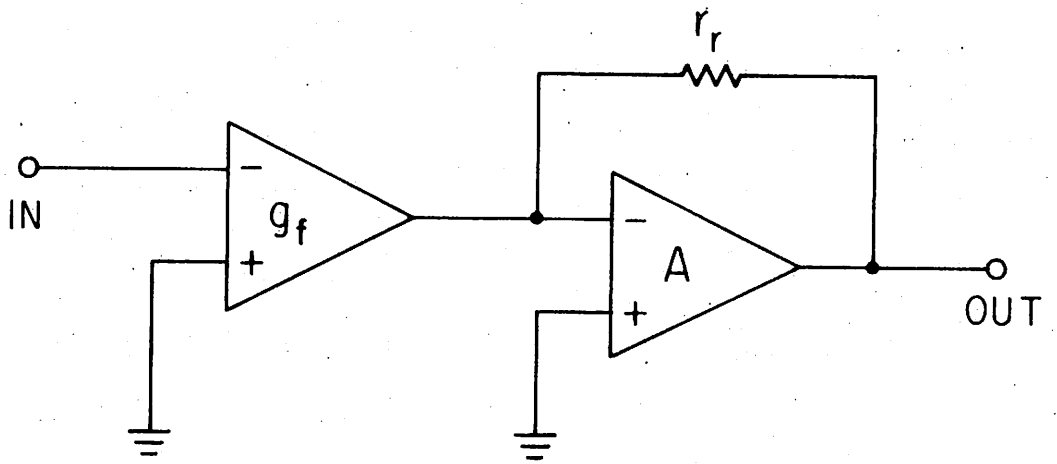


Fig. 8. Block diagram for output stage.

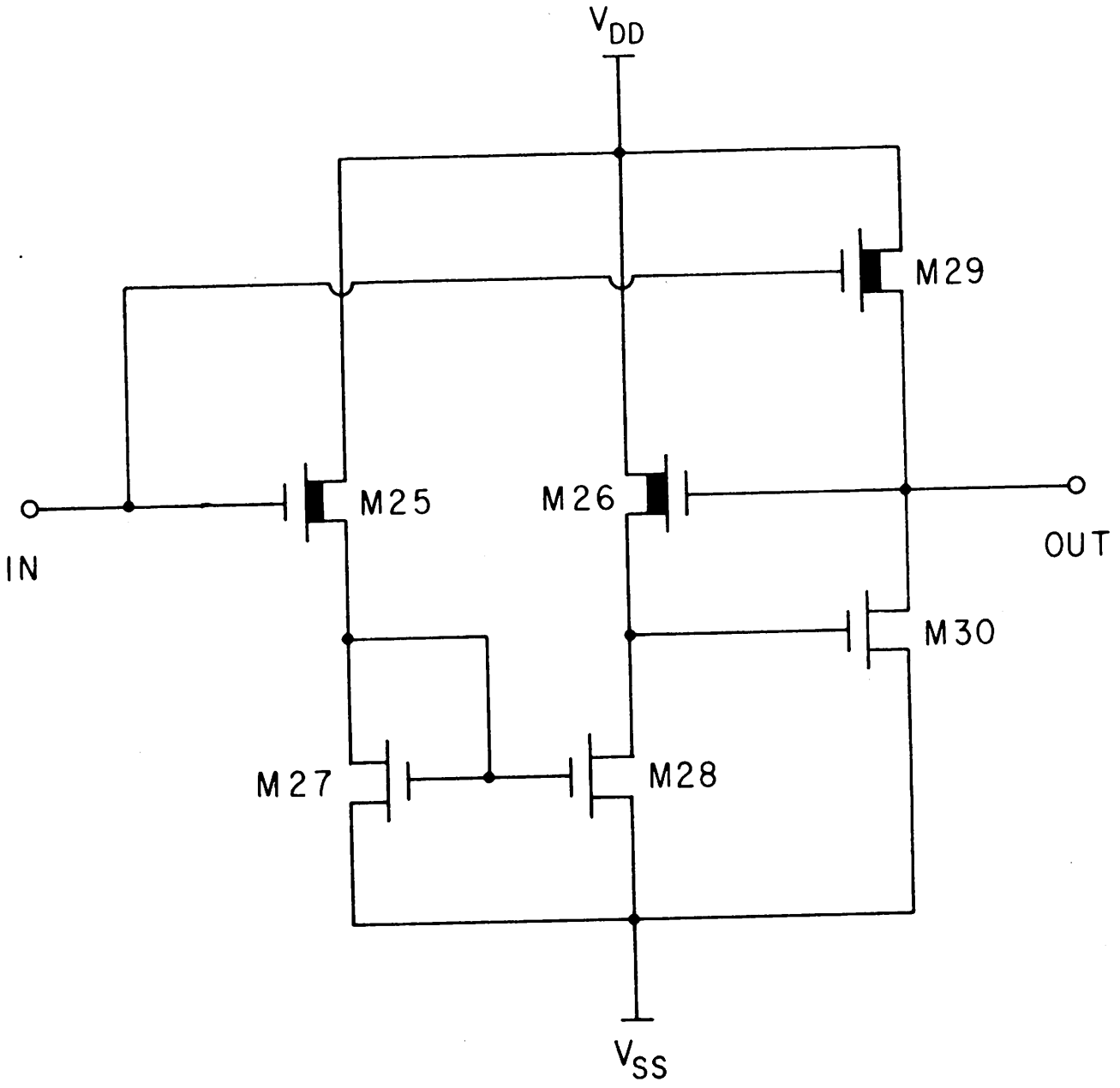
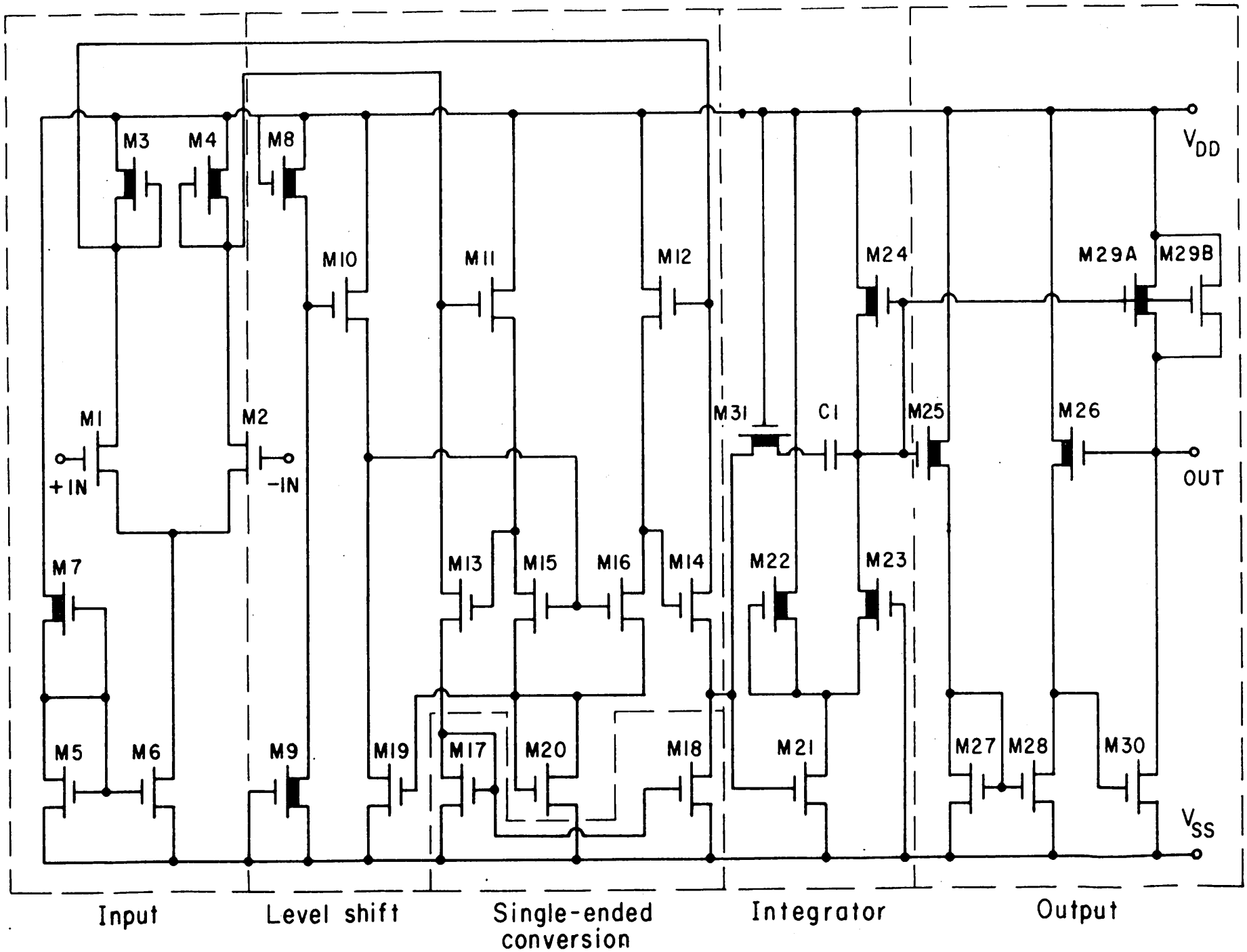


Fig. 9. Circuit schematic for output stage.


M3
M4
M8
M10
M11
M12
M24
M29A
M29B
V_{DD}
M1
M2
M31
C1
M25
M26
+IN
-IN
OUT
M7
M13
M15
M16
M14
M22
M23
M5
M6
M9
M19
M17
M20
M18
M21
M27
M28
M30
V_{SS}
Input
Level shift
Single-ended conversion
Integrator
Output

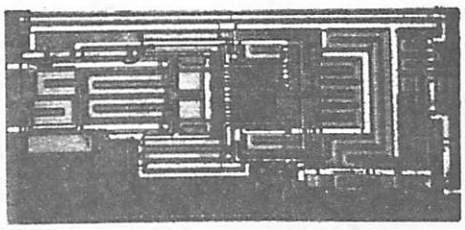


Fig. 11. Die Photo.

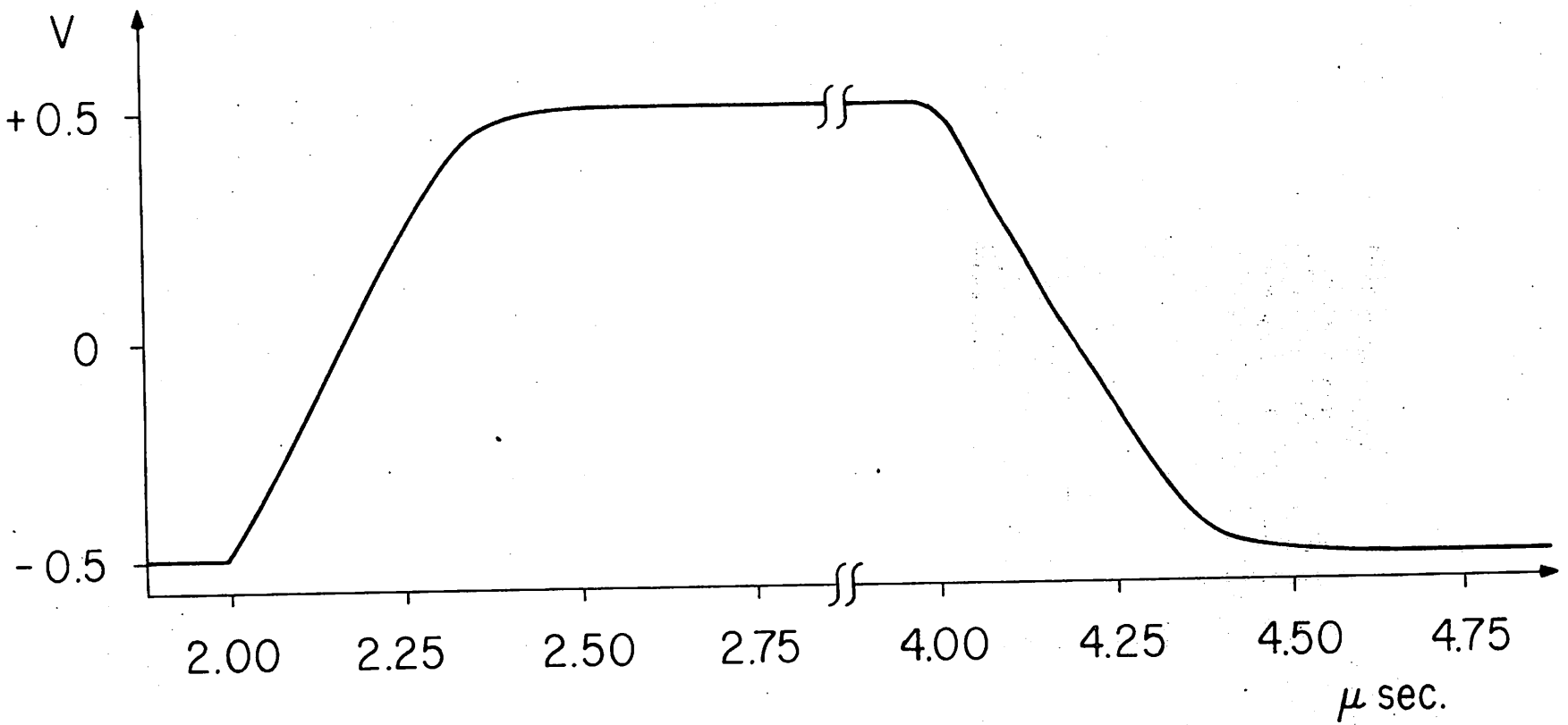


Fig. 12. Simulated voltage follower response.

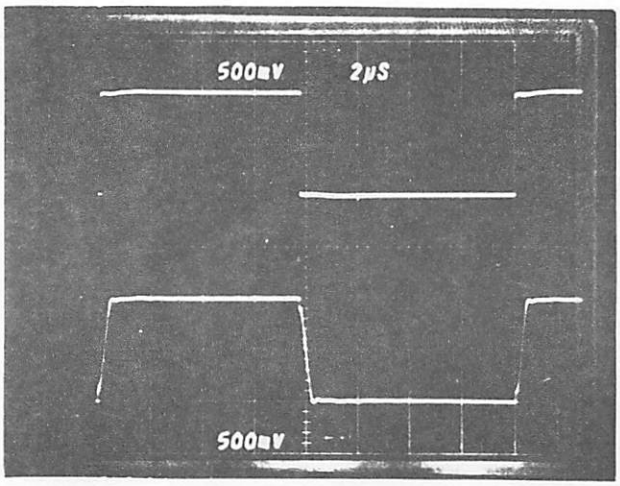


Fig. 13. Measured voltage follower response.

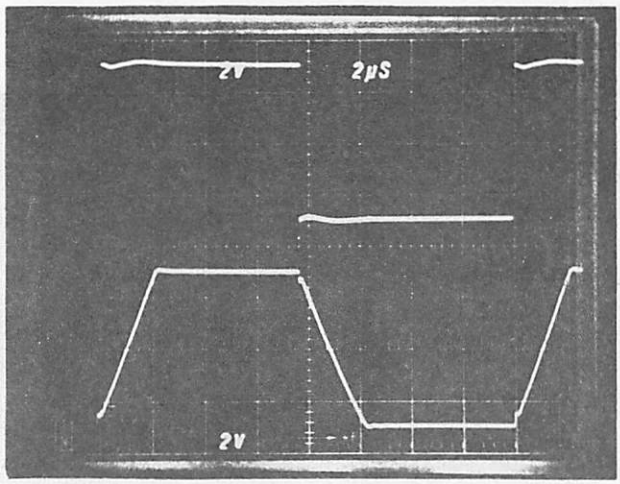


Fig. 14. Measured voltage follower response with a 6V step.

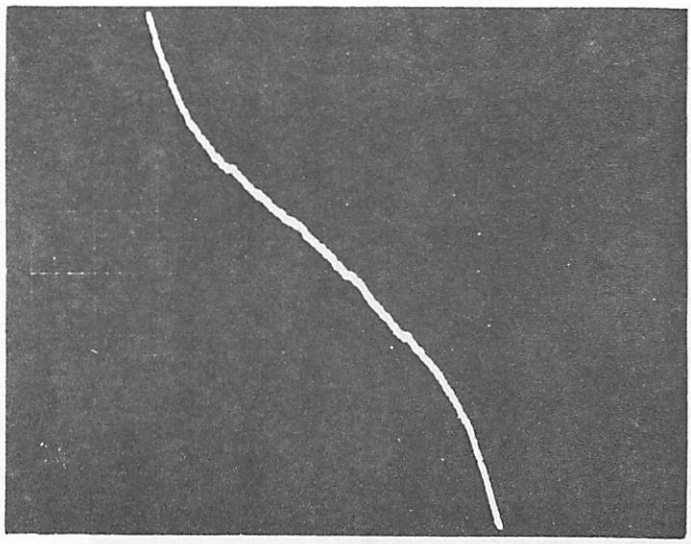


Fig. 15. DC transfer curve.

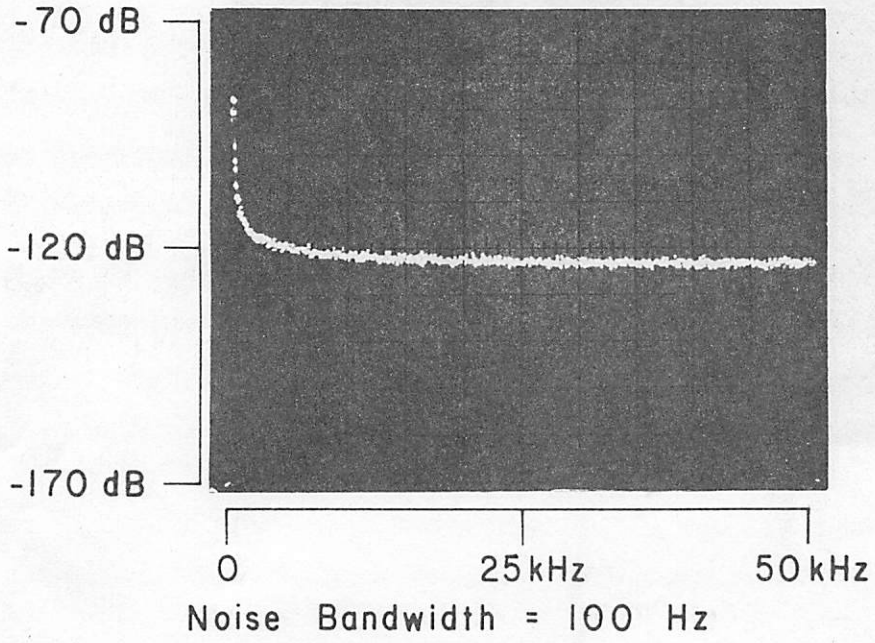


Fig. 16. Noise spectrum in the voltage follower configuration.