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FULLY INTEGRATED ANALOG FILTERS  
USING BIPOLAR/JFET TECHNOLOGY

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Memorandum No. UCB/ERL M78/53

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USING BIPOLAR/JFET TECHNOLOGY

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Abstract

A new approach for realizing high order analog filters which can be fully integrated using a compatible bipolar and ion-implanted JFET process is described. This approach is based on the recognition that what is really needed is a long time constant monolithic integrator which can be effectively realized in a small silicon area. These integrators have been designed, fabricated and used in an 'leapfrog' or active ladder configuration to realize a fifth order 8 kHz Chebyshev lowpass filter with 0.1 dB passband ripple. No external trimming operations and no anti-aliasing prefilter are required.

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## I. Introduction

Frequency selective circuits are widely used in communications and control systems. In many cases, these filters must cut off sharply and must have small passband ripple. These tight specifications can only be met with precision high order filters. Conventional RC active filters which use thin film or hybrid technologies often require external trimming [1],[2]. From the standpoint of cost effectiveness, it is desirable to realize a fully integrated filter system which requires small silicon area and no external trimming operations.

Two promising approaches to realizing high order monolithic filters are the CCD filtering technique, and the switched capacitor MOS filter approach [3],[4]. However, the main disadvantage of these approaches is that they are analog sampled data systems which require a continuous-time prefilter to minimize aliasing effects.

In this paper, a new approach for realizing precision continuous-time monolithic analog filters is described. This approach is based on the recognition that what is really needed is an integrator with a long time constant which can be effectively realized in a small silicon area. Such an integrator can be used as a building block for realizing different filtering functions. The filter technique described in this paper uses ion-implanted JFET's in a new circuit technique both to achieve the required long

integrator time constants and to control them precisely by reference to an external clock frequency.

Since this is a continuous-time analog filter, no anti-aliasing prefilter is required. This approach is demonstrated with a fifth order 8 kHz Chebyshev lowpass filter with passband ripple of 0.1 dB. Excellent agreement between the experimental and designed values has been obtained.

## II. Integrators As Basic Building Blocks

The key element in a variety of filter configurations is an integrator which can be used to realize different filtering functions. Figure 1 shows the circuit for a second order 'state variable' filter. It requires two resistors and two differential input integrators. Despite its simplicity, three different transfer functions are available. These transfer functions can be easily derived and are shown below:

$$\frac{V_{br}}{V_{in}} = \left( \frac{R_8}{R_7 + R_8} \right) \left( \frac{\omega_1 \omega_2 + s^2}{s^2 + s(\omega_1 R_7 / (R_7 + R_8)) + \omega_1 \omega_2} \right) \quad (1)$$

$$\frac{V_{bp}}{V_{in}} = \left( \frac{-R_8}{R_7 + R_8} \right) \left( \frac{s \omega_1}{s^2 + s(\omega_1 R_7 / (R_7 + R_8)) + \omega_1 \omega_2} \right) \quad (2)$$

$$\frac{V_{1p}}{V_{in}} = \left(\frac{R_8}{R_7+R_8}\right) \left(\frac{\omega_1\omega_2}{s^2 + s(\omega_1 R_7 / (R_7+R_8)) + \omega_1\omega_2}\right) \quad (3)$$

Examining these expressions carefully, we notice that equations (1), (2), (3) correspond to the second order bandreject, bandpass and lowpass transfer functions, respectively. For these transfer functions, it is interesting to note that

$$\omega_0 = \sqrt{\omega_1\omega_2} \quad (4)$$

$$Q = \left(1 + \frac{R_8}{R_7}\right) \sqrt{\frac{\omega_2}{\omega_1}} \quad (5)$$

where  $\omega_0$  corresponds to the resonance frequency, and  $Q$  corresponds to the quality factor of the second order filter.

These second order stages can be cascaded to form a higher order filter as shown in figure 2(a). In this example, three second order sections are cascaded to realize a sixth order filter. Each of the second order sections realizes a pair of complex poles in the s-plane as shown in figure 2(b). The main advantage of this cascading method is

that it is very easy to implement for any realizable transfer function. The main disadvantage is that it typically has a higher sensitivity of network parameters due to component variations as compared with the direct implementation method.

One example of the direct implementation method is the fifth order doubly-terminated lowpass passive ladder network, as shown in figure 3(a). From classical circuit theory, it is well known that under the maximum power transfer condition, this network has an extremely low sensitivity due to component variations over the passband region [5].

By standard flowgraph techniques, this passive ladder network can be transformed into the 'leapfrog' or active ladder configuration using integrators, as shown in figure 3(b) [6],[7]. The transfer functions of these passive and active ladder networks are identical. More importantly, there is a one-to-one correspondence between the reactive element values and the gain constants of the integrators. Because of this one-to-one correspondence, this active ladder network retains the low sensitivity properties of the passive prototype.

For instance, this active ladder network can be used to realize a fifth order 8 kHz Chebyshev lowpass filter with passband ripple of 0.1 dB. The required unity gain bandwidths of the integrators for this example have values



ranging from 4 kHz to 7 kHz as shown in Table I. To illustrate the sensitivity of this active ladder network, the nominal magnitude response of the fifth order lowpass filter is plotted across the frequency band of interest, as shown by the solid line of figure 4. The dotted lines indicate the bounds of the worst case deviations of any combination of  $\pm 2\%$  variations in the gain constants of the integrators. Notice that despite such a wide variation in component values, the maximum deviation is less than 0.1 dB. The extremely low sensitivity of this type of active ladder network enables the monolithic integration of high order, high precision analog filters without any external trimming.

This direct implementation method is not limited to lowpass realizations. Bandpass, highpass and bandreject transfer functions are all realizable using integrators as basic elements [8],[9].

### III. Monolithic Integrator

#### A. Integrator requirements

Integrators can be used in a variety of circuit configurations to realize different filtering functions. In this section, the requirements for realizing integrators with time constants in the audio frequency range are described.

A simple differential input integrator can be designed using two resistors, two capacitors and one operational

amplifier, as shown in figure 5. The gain constant of this integrator is equal to  $1/(RC)$ . For low frequency operation, long RC time constants are required. For instance, for a frequency of 5 kHz with a monolithic capacitor of 30 pF, a resistor of 1 megohm is required. This large value resistor is not efficiently realized in conventional monolithic approaches because it requires a large silicon area. Also, the precise value of the RC product is difficult to control due to process and temperature variations.

In order to implement integrators monolithically and efficiently, a way to realize integrators with long time constants in small silicon areas is needed. Also, a technique of stabilizing the absolute magnitude of the RC product, or equivalently, the gain constant of the integrator is required.

#### B. Monolithic integrator

As described earlier, to realize an integrator with a long time constant, a large value of resistance must be realized. The circuit of figure 6 effectively realizes a large value resistor by employing a small value of transconductance. In this circuit, the input stage is a transconductance amplifier followed by an inverting gain stage and feedback integrating capacitor. The gain constant of this integrator is precisely defined by the ratio of  $G_m$  to  $C$ , while the transconductance,  $G_m$ , is expressed by the follow-

ing expression:

$$G_m = \frac{2 \sqrt{I_d I_{dss}}}{V_p} \quad (6)$$

where  $I_{dss}$  is defined as the saturation drain current,  $I_d$  is the drain current, and  $V_p$  is the pinchoff voltage of the JFET.

Again, for a frequency of 5 kHz, using a monolithic capacitor of 30 pF, a transconductance of 1 micro-mho is required. This small value of  $G_m$  can be easily achieved by designing JFET's with small value of  $Z/L$ , as well as by operating the input stage with low current. The required chip area for realizing such a small value transconductance (and hence large value of resistance) is small.

By varying the voltage at the controlling node at  $V_c$ , the biasing current source,  $I_d$ , can be varied, and by varying  $I_d$ , the  $G_m$  of the input stage is changed. Hence, by varying  $V_c$ , the  $G_m$  of the input stage, and thus the gain constant of the integrator can be varied. This feature will be used to control the absolute magnitude of the gain constant of the integrator, as described in the next section.

C. Absolute bandwidth control

The absolute magnitude of the gain constant of the integration is difficult to control due to process and temperature variations. This problem can be solved by utilizing the fact that while the absolute values of monolithic component parameters are not well controlled, the matching of one value to another on the same die is quite good. Using this fact, the time constants of the integrators can be locked to an externally supplied precision clock frequency using a phase-locked-loop system as shown in figure 7 [10]. The three main elements of this block diagram are the phase comparator, the voltage-controlled-oscillator (VCO) and the voltage-controlled-filter (VCF).

The oscillating frequency of the VCO is precisely defined by the gain constants of the two integrators, and is equal to

$$\omega_{osc} = \sqrt{\omega_1 \omega_2} \quad (7)$$

where  $\omega_1$ ,  $\omega_2$  are the gain constants. As previously described, the gain constant of the integrator can be controlled through  $V_c$ . Hence by controlling  $V_c$ , the frequency of oscillation can be controlled. The voltage-controlled-filter is designed using the same type of integrators as those of the VCO. The bandwidth of the filter is designed

to be exactly proportional to the frequency of oscillator. By varying  $V_c$ , both the frequency of the oscillator and the bandwidth of the filter are varied, and the bandwidth of the filter tracks the frequency of the oscillator. The phase comparator compares the external precision clock frequency,  $f_s$ , to the frequency of the VCO, and generates an error voltage. After passing through a simple lowpass filter, the error voltage,  $V_c$ , is then fed back to the controlling node. In the steady state,  $V_c$  forces the gain constants of the integrators to have the desired values, such that the frequency of the oscillator is exactly equal to the external precision clock frequency. Since the bandwidth of the filter is always exactly proportional to the frequency of the oscillator, the bandwidth of the filter is always exactly proportional to the external precision clock frequency, and is independent of process and temperature variations.

The approach described above has several advantages. First, monolithic integrators with long time constants can be realized in a small area. Second, the ratio-matching of the gain constants of integrators depends only on the ratio-matching of the current sources and the ratio-matching of the capacitors. These can be accurately achieved [11],[13]. Finally, the absolute magnitude of the gain constant, and thus the bandwidth of the filter, can be precisely controlled by reference to an external precision frequency, and it is insensitive to process and temperature

variations.

## VI. Practical Design Considerations

Ideally, an integrator has the  $1/f$  frequency response as shown in figure 8(a). The phase is exactly 90 degrees and the gain at DC is infinite. Unfortunately, an actual monolithic integrator deviates from these ideal characteristics. For instance, the non-ideal integrator has a finite DC gain. However, this is not an important consideration since for most cases, a DC gain of about 1000 is sufficient to give very accurate frequency responses.

Another non-ideal effect is due to the second pole of the monolithic integrator as shown in figure 8(b). In this figure,  $f_0$  corresponds to the gain constant and  $f_1$  corresponds to the second pole of the non-ideal integrator. Because of the presence of  $f_1$ , the phase angle at  $f_0$  is not exactly 90 degrees. This excess phase will cause a slight peaking in the magnitude response, as shown in figure 8(c). In this case, a 0.1 degree phase error causes approximately a 0.1 dB peaking in the passband of the magnitude response of a fifth order Chebyshev lowpass filter. Typically, to achieve a phase error of less than 0.1 degree, the ratio of  $f_1$  to  $f_0$  has to be greater than 50.

One important practical consideration is the nonlinearity of the monolithic integrator. Figure 9(a) shows the basic monolithic integrator. A closer look at this circuit

discloses that the input transconductance stage is linear for a limited range of input voltage. A plot of output current versus input voltage is shown in figure 9(b). Notice that the output current saturates at a maximum input voltage of  $-V_p$ , where  $V_p$  is the pinchoff voltage of the JFET transistors.

To improve the linearity of the transconductance amplifier, the maximum input voltage range can be extended by using the input stage shown in figure 10(a). In this circuit, four additional transistors, Q2 through Q5, are used as source degeneration JFET resistors to increase the linearity of the transconductance amplifier. A plot of output current versus input voltage is shown in figure 10(b). Notice that by simply adding four transistors, the maximum input voltage range has been increased by a factor of three. Actually, we can add as many of the JFET resistors as necessary to improve the linearity of the transconductance amplifier. The only disadvantage is that when the number of transistors increases, the required chip area also increases. This may impose a practical limit on the maximum number of transistors used.

The final design of the monolithic integrator is shown in figure 11. The input transconductance stage consists of transistors Q1 through Q12. Transistors Q2 through Q5 are used as source degeneration resistors as mentioned earlier. Transistors Q8 through Q10 are used as active loads.

Transistors Q11 and Q12 are used as emitter degeneration resistors to improve the noise and offset of the integrator. With no emitter degeneration, the noise and offset of the bipolar devices when referred to the input will be amplified by the ratio of the bipolar to JFET transconductances. By using JFET transistors as degeneration resistors, we can lower the noise and the offset voltage of the integrator with little increase in silicon area. Transistor Q1 is the biasing JFET current source. By controlling the voltage at node  $V_c$ , the biasing current, and thus the transconductance of the input stage can be varied. This feature is used to control the bandwidth of the integrator as outlined earlier.

The following stage is the source follower which consists of transistors Q13 and Q14. This is used to minimize the loading to the input transconductance stage. Transistors Q15 and Q16 constitute the common emitter inverting gain stage. Transistors Q18 and Q17 are used as emitter follower output stage to reduce the output impedance to about 10 kilo-ohms.

The output of the integrator is clamped by transistor Q19, such that the output common mode range is always smaller than the input common mode range. This prevents the integrator from latching up.

Typically, to realize a given transfer function, integrators of different gain constants are required. These different gain constants are achieved by scaling the ratios



of the integrating capacitors while keeping all the input transconductance stages identical. In this way, excellent matching of transconductances can be achieved. Previous work has shown that it is possible to achieve ratio-matching accuracy of a few tenths of one percent for monolithic MOS capacitors [11].

## V. Experimental Results

### A. Description of the experimental IC

The photograph of the experimental IC chip is shown in figure 12. The overall chip size is 90 x 100 mils. A 10  $\mu\text{m}$  minimum feature size and 5  $\mu\text{m}$  minimum alignment tolerance were used. In this chip, there are seven ratioed MOS capacitors of values ranging from 15 to 30 pF. There are two identical monolithic integrators with each realized in a silicon area of 850 mils<sup>2</sup>. A bipolar compatible ion-implanted JFET process has been used [12],[13]. The process is similar to a standard bipolar process, with the addition of two ion-implantation steps. The first implant (boron) is used to create the channel while the second implant (phosphorus) is used to realize the top gate of the JFET transistors. The JFET pinchoff voltage is designed to be 4 volts.

### B. Performance of the integrator

The measured performance of the monolithic integrator agrees very well with the design values. With power supplies of  $\pm 12$  volts, the DC open loop gain is 10,000. Both the power supply rejection ratio (PSRR) and the common mode rejection ratio (CMRR) are 70 dB. The nominal unity gain bandwidth using a 20 pF integrating capacitor is 7 kHz. The slew rate using a 20 pF integrating capacitor is 0.5 V/ $\mu$ sec. The total power dissipation for each integrator is only 4 mW. Table II summarizes the performance of the monolithic integrator.

Realization of high order, high precision filters requires precision ratio-matched integrators. As described earlier, the ratio-matching of integrators depends on the ratio matching of  $G_m/C$ . Experimental data on the matching of  $G_m$  and C are tabulated and shown in figure 13. Based on a sample size of 43, the standard deviation of the matching of MOS capacitors is 0.24 % for this process, and the standard deviation of  $G_m$  based on 94 samples, is found to be 0.75 %. Since these two parameters are uncorrelated, the standard deviation of the ratio-matching of monolithic integrators is  $(0.75^2 + 0.24^2)^{1/2} = 0.79$  %. This will introduce a worst case deviation of less than 0.05 dB in the passband magnitude response of the fifth order lowpass filter mentioned earlier.

C. Performance of the fifth order lowpass filter using leap-frog structure

The monolithic integrators described earlier have been used in a 'leapfrog' or active ladder configuration to construct a fifth order 8 kHz Chebyshev lowpass filter with 0.1 dB passband ripple. To realize such a fifth order lowpass filter, a total of seven integrators are required. Two integrators are used in the VCO and five integrators are used in the filter section. The estimated area to integrate this complete fifth order lowpass filter using the process previously described would be 10,000 sq. mils, and the total power dissipation would be approximately 50 mW.

The measured frequency response of the fifth order lowpass filter is shown in figure 14(a). The measured passband ripple is 0.1 dB to within 0.05 dB, with a cutoff frequency of 8 kHz. By controlling the external frequency, the cutoff frequency of the filter was tunable over a range of 6 kHz to 10 kHz. The measured frequency response over a wider frequency range is shown in figure 14(b). Notice that the filter is performing well into the 200 kHz range without any aliasing problem. The stopband rolloff is approximately 100 dB/decade. These measured data were obtained without any external trimming operations, and they agree very well with the expected design values.

The filter is relatively insensitive to power supply variations. A 20 % variation in the power supply introduced less than 0.02 dB change in the passband of the magnitude response. A change of 50 degrees in ambient temperature

resulted in a passband deviation of 0.05 dB and a cutoff frequency variation of 1 %. These results were obtained on a breadboarded filter system which consists of several packages of monolithic integrators. It is believed that, for a fully monolithic filter system, the sensitivity due to temperature variation will be very much reduced.

The filter has a wide dynamic range of operation. The measured output noise in the frequency band of 100 Hz to 10 kHz is 200  $\mu$ Vrms. At a signal frequency of 1 kHz, the measured total harmonic distortion (THD) for an output voltage of 7.5 Volts peak to peak is only 0.3 %. When the output voltage is increased to 10 Volts peak to peak, the measured THD is increased to 1 %. Based on the 1 % THD output voltage and the 200  $\mu$ Vrms noise level, the dynamic range is 85 dB. Table III summarizes the performance of this fifth order lowpass filter.

## VI. Conclusions & Future Developments

The design techniques for realizing fully integrated analog filters using a compatible bipolar and ion-implanted JFET technology have been described. This approach is applicable to a wide variety of filters. Monolithic integrators with long time constants have been designed and fabricated. These integrators have been used in an 'leap-frog' or active ladder configuration to realize a fifth order, 8 kHz Chebyshev lowpass filter with 0.1 dB passband

ripple. The low sensitivity properties of the active ladder structure enables the realization of this high order filter without any external trimming operations. A dynamic range of 85 dB has been obtained. Since this is a continuous time approach, no anti-aliasing prefilter is required.

Because of this non-sampled data approach, this technique may be able to achieve a higher frequency of operation. Also, for this active ladder lowpass network, transmission zeros can be easily achieved without any additional integrators. Only two additional capacitors are needed for each pair of transmission zeros [14].

#### Acknowledgment

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## FIGURE CAPTIONS

- Figure 1. A second order filter.
- Figure 2 (a) A sixth order filter by cascading three second order sections, and (b) the pole locations of the lowpass filter in the s-plane.
- Figure 3. (a) A doubly terminated LC ladder network, and (b) the equivalent active ladder network.
- Figure 4. The worst case deviations for a fifth order Chebyshev lowpass filter with 0.1 dB nominal passband ripple.
- Figure 5. A simple RC differential input integrator.
- Figure 6. The basic monolithic differential input integrator.
- Figure 7. A block diagram of the filter system.
- Figure 8. (a) Frequency and phase response of an ideal integrator, (b) frequency and phase response of a non-ideal integrator, and (c) the effects of excess phase.
- Figure 9. (a) The basic monolithic integrator, and (b) a plot of  $I_o$  versus  $V_{in}$ .
- Figure 10. (a) The monolithic integrator with a new input stage, and (b) a plot of  $I_o$  versus  $V_{in}$ .
- Figure 11. A schematic of the monolithic integrator.
- Figure 12. A photograph of the experimental IC.
- Figure 13. Distributions of the matching of  $G_m$  and  $C$ .
- Figure 14. (a) Measured frequency response of the fifth order Chebyshev lowpass filter over a narrow frequency

range, and (b) measured frequency response of the lowpass filter over a wide frequency range.

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Table I

The required unity-gain bandwidths for realizing  
a fifth order 8 kHz Chebyshev lowpass filter  
with 0.1 dB passband ripple

<u>Integrator</u>	<u>Unity-gain bandwidth</u>
I1	6.9759 kHz
I2	5.8343 kHz
I3	4.0506 kHz
I4	5.8343 kHz
I5	6.9759 kHz

Table II

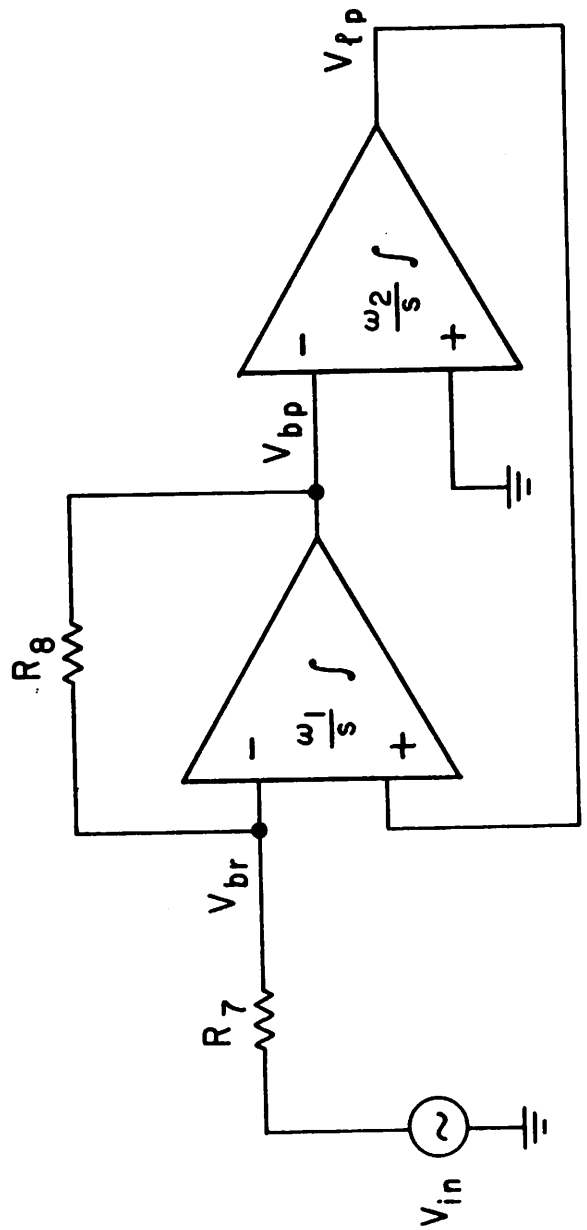
Integrator Performance Data

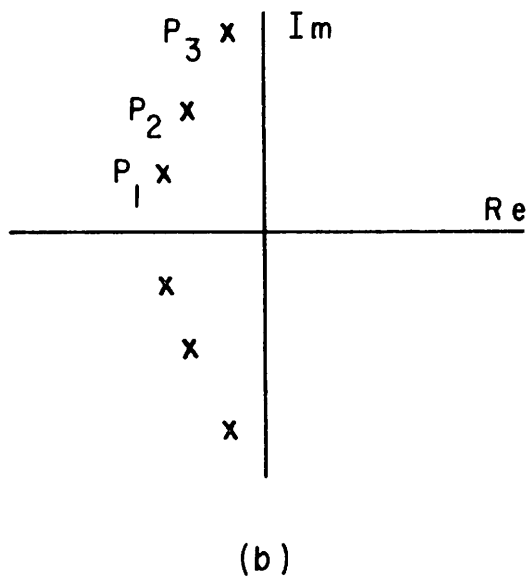
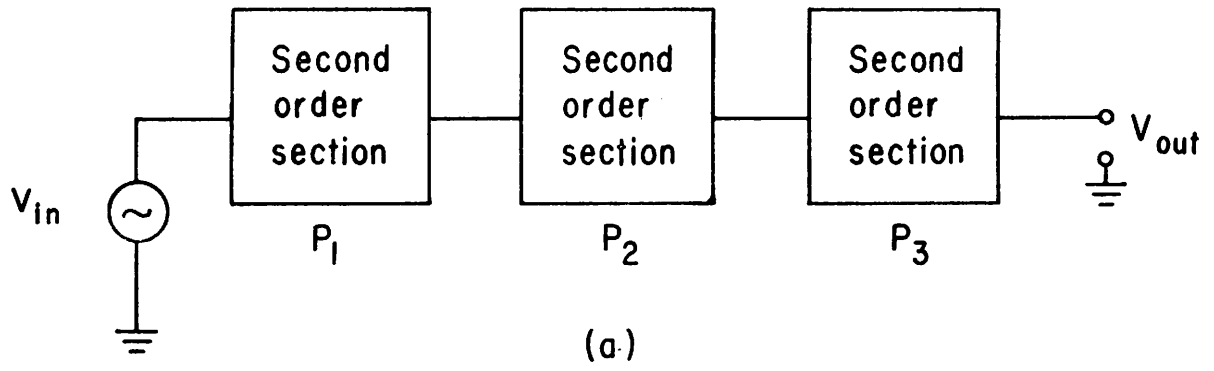
Power supplies	$\pm 12V$
DC open loop gain	10,000
CMRR, PSRR (DC)	70 dB
Nominal unity gain BW (20pF)	7 kHz
Input offset voltage (standard deviation)	16 mV
Power dissipation	4 mW
Chip area	850 mil <sup>2</sup>

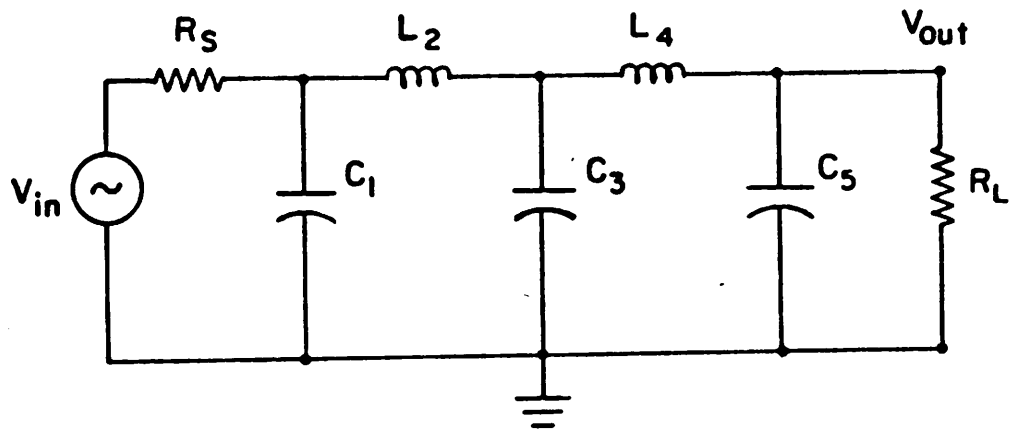
Table III

Fifth-order Filter Performance Data

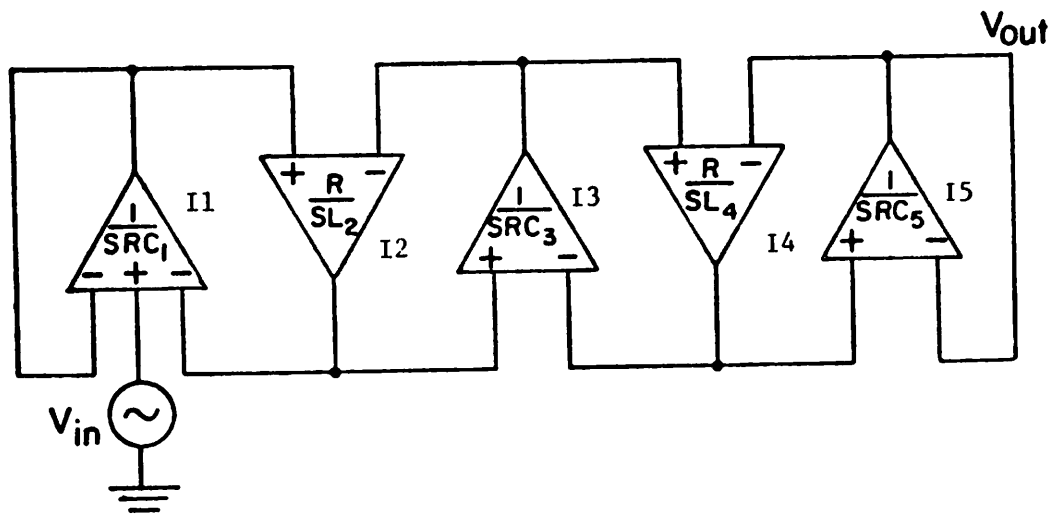
Ripple bandwidth	8 kHz
Passband ripple	0.1 dB
Output THD (1 kHz, 10 Vp-p)	1 %
Output noise (100 Hz - 10 kHz)	200 $\mu$ Vrms
Dynamic range	85 dB



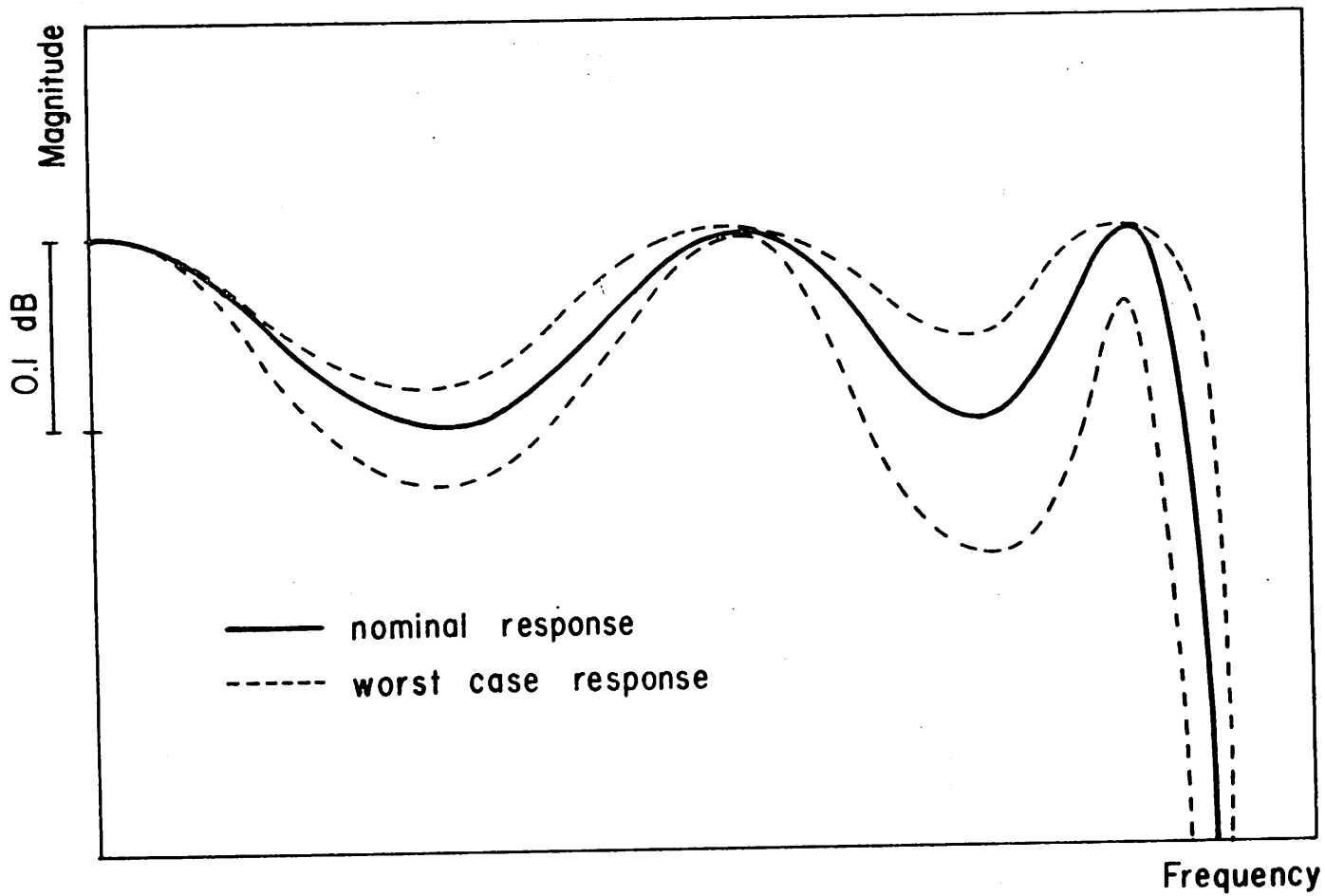




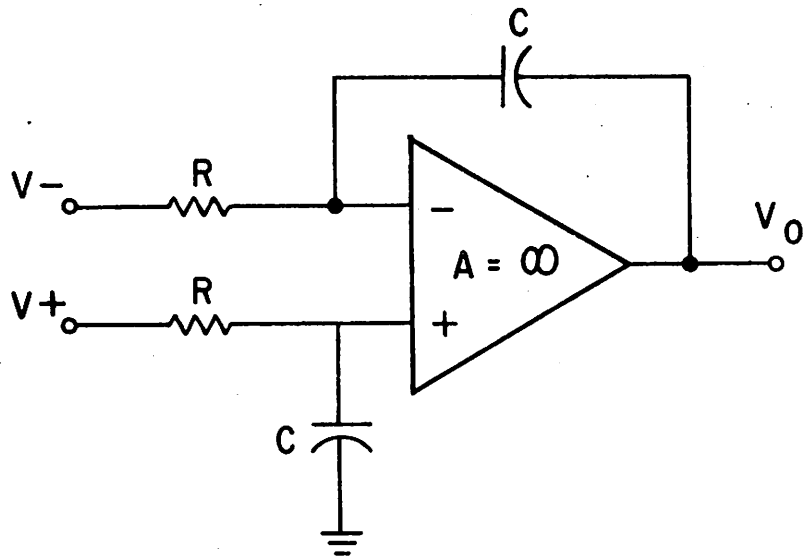
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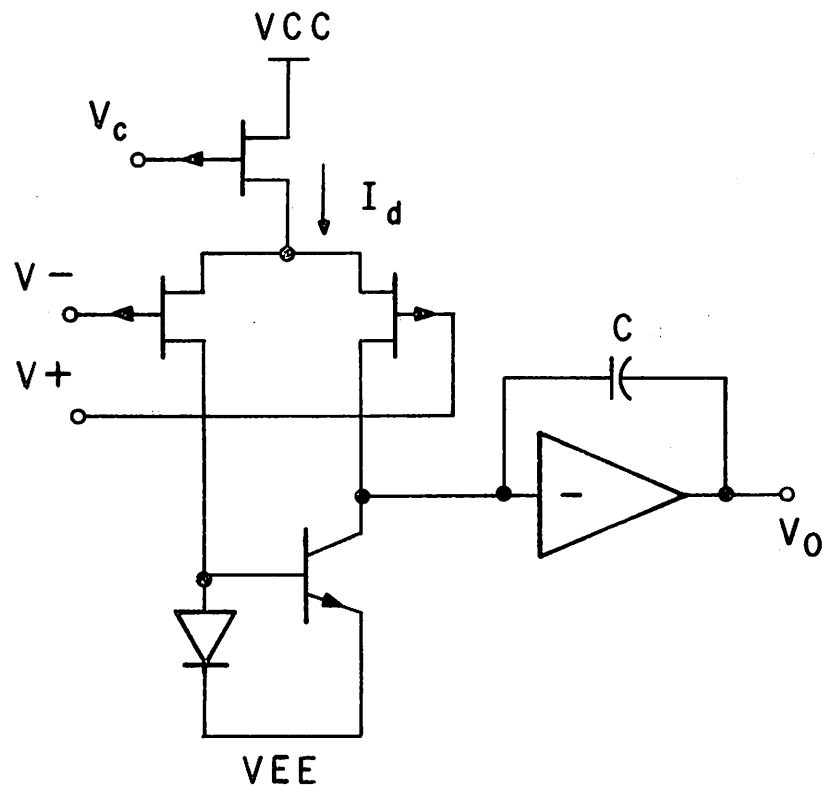


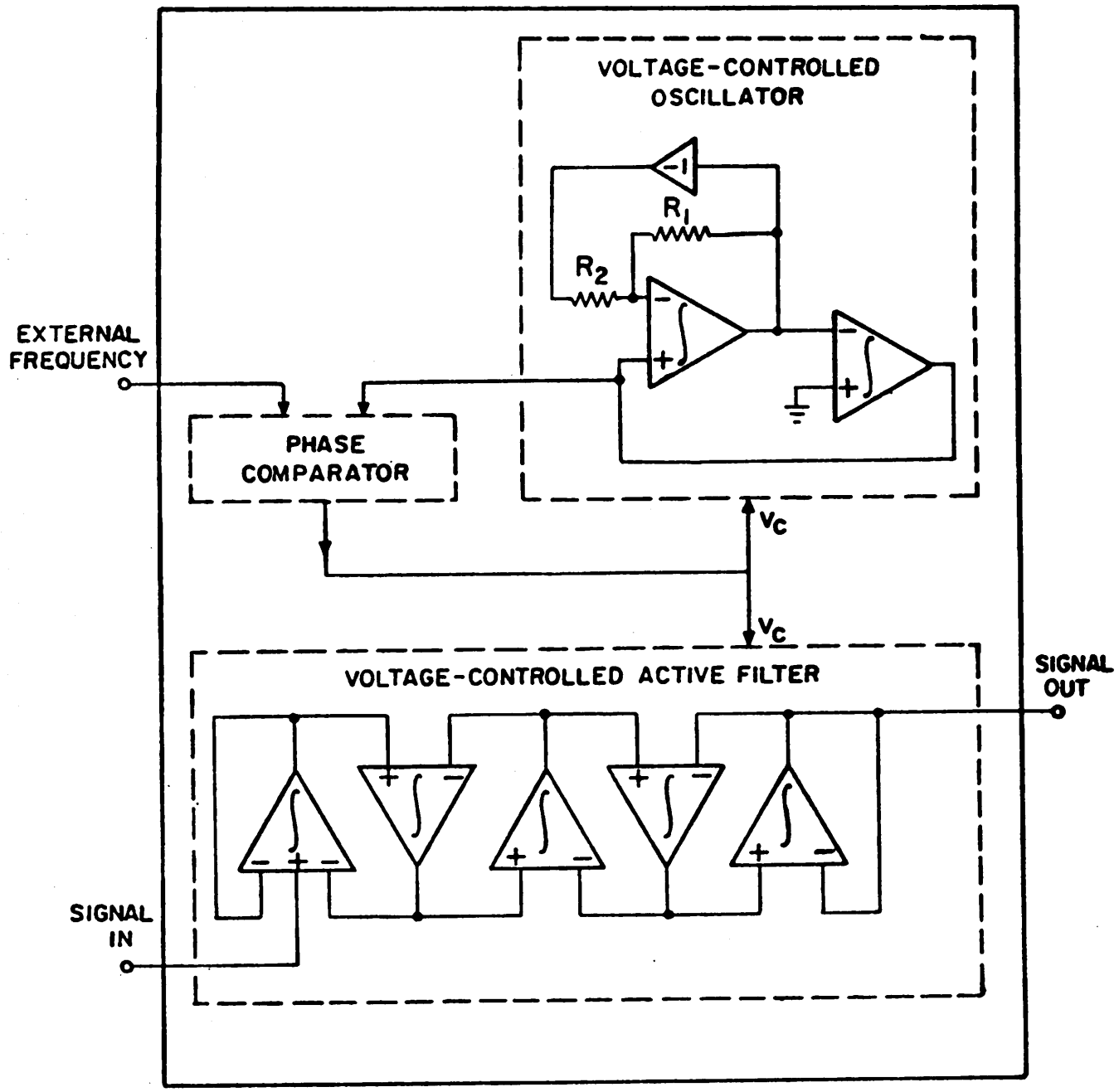
(b)

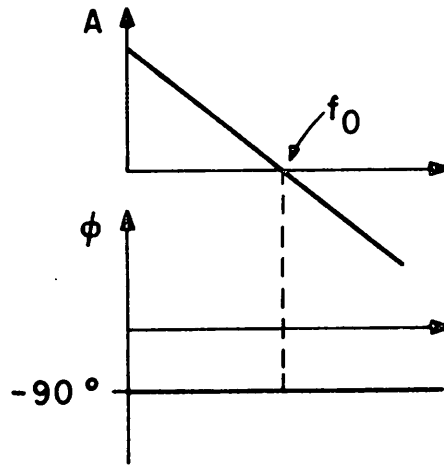




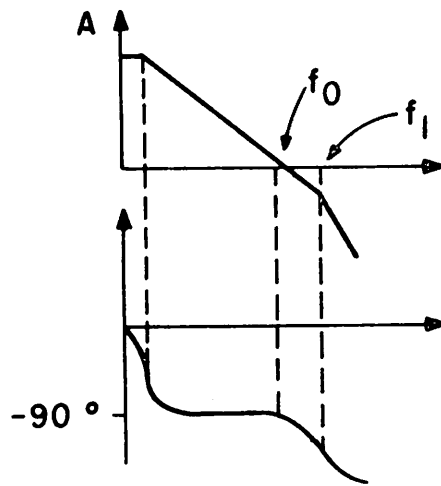




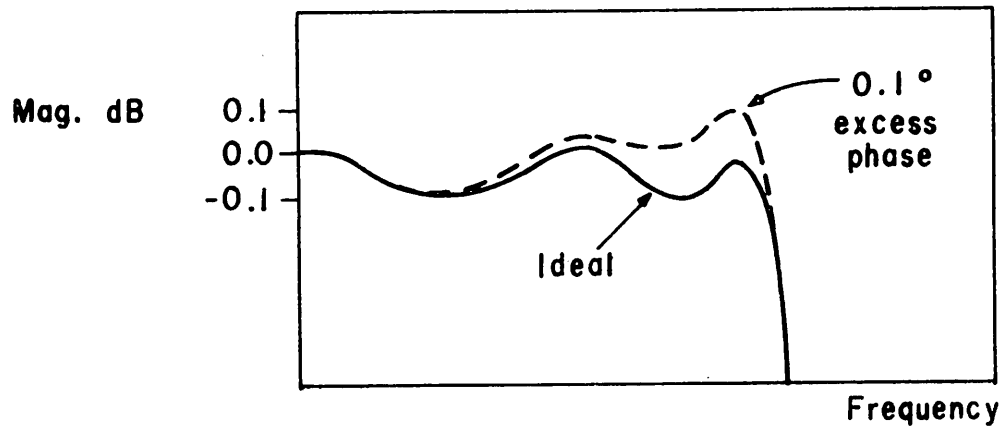




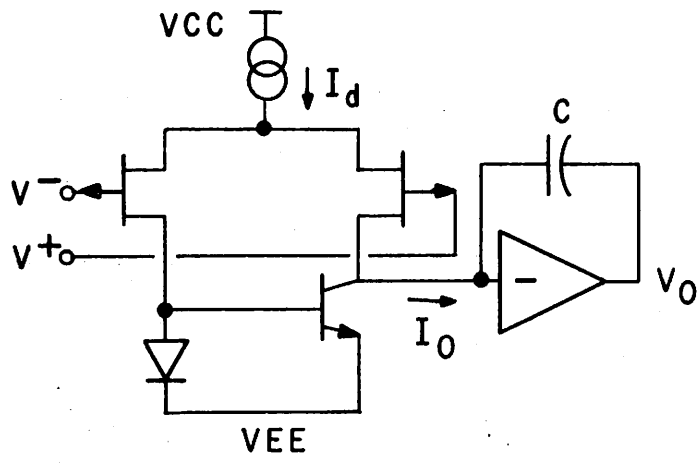
(a)



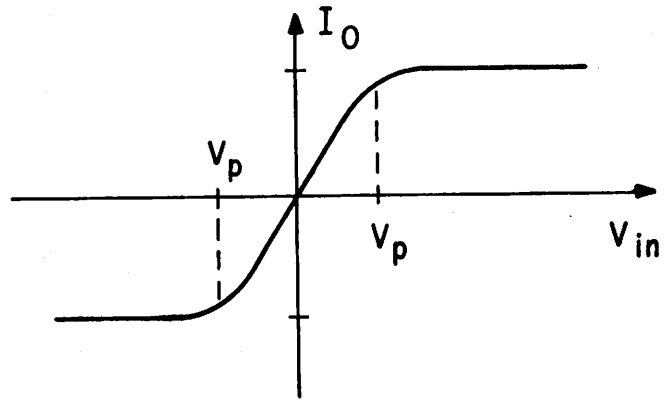
(b)



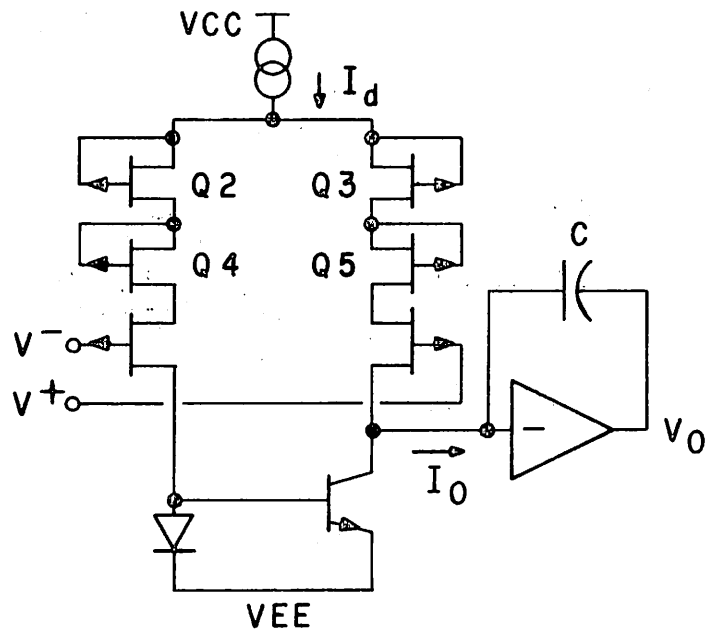
(c)



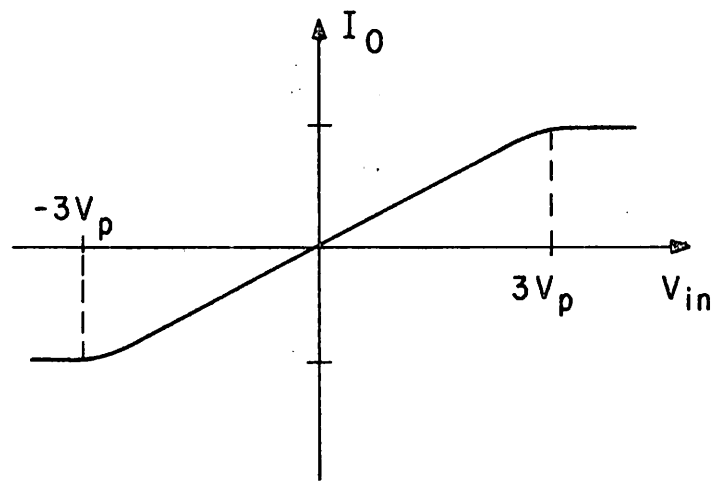
(a)



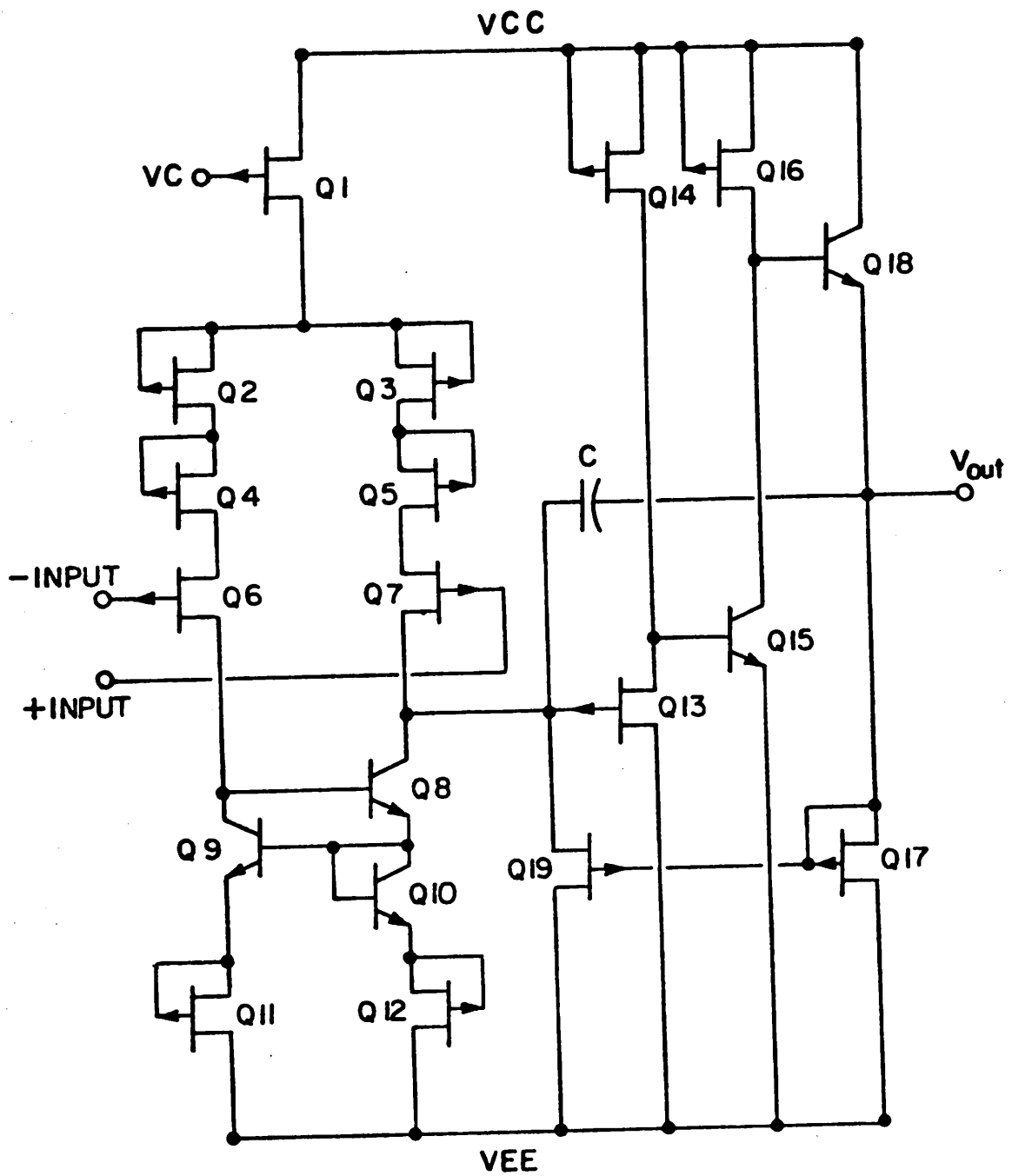
(b)

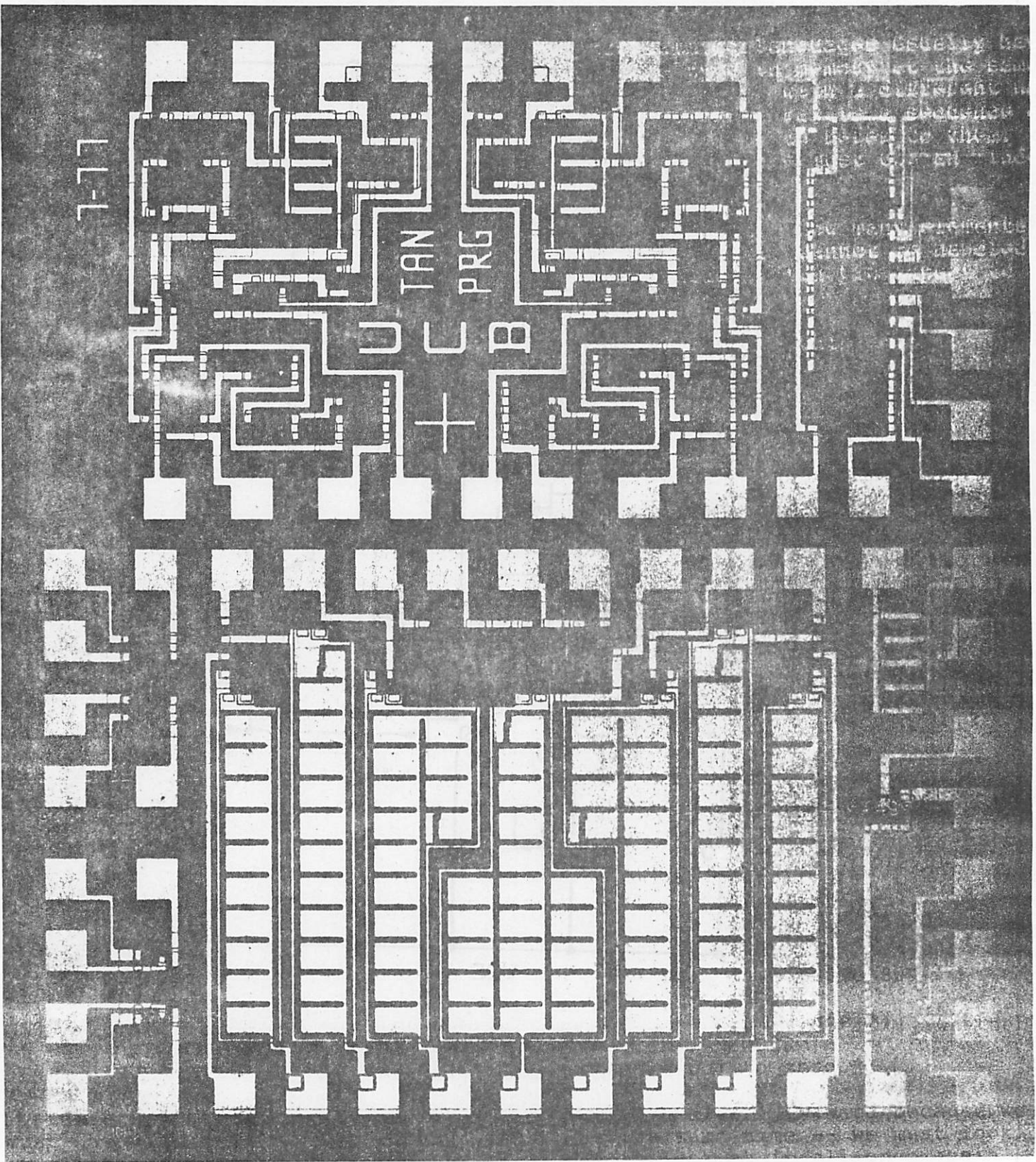


(a)

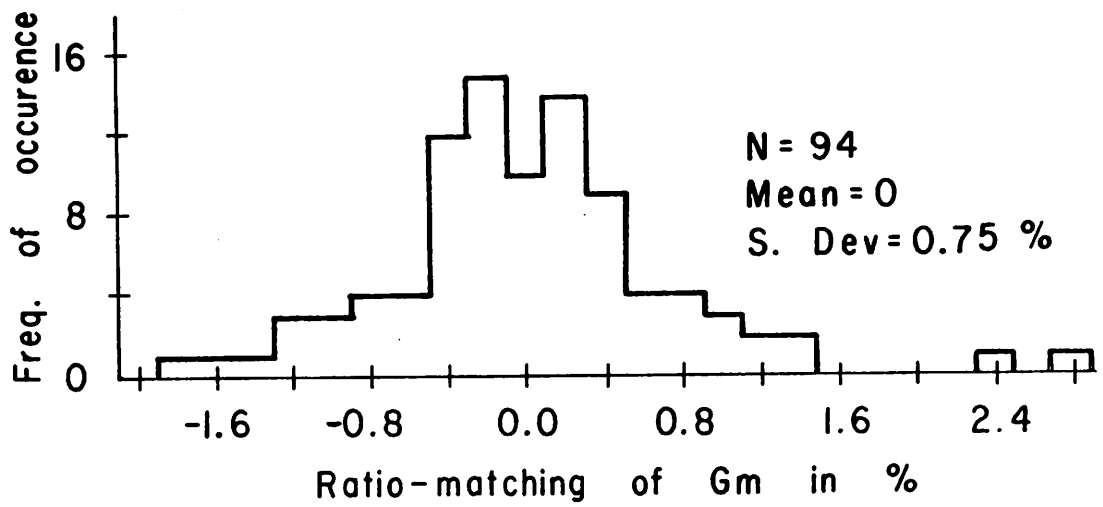
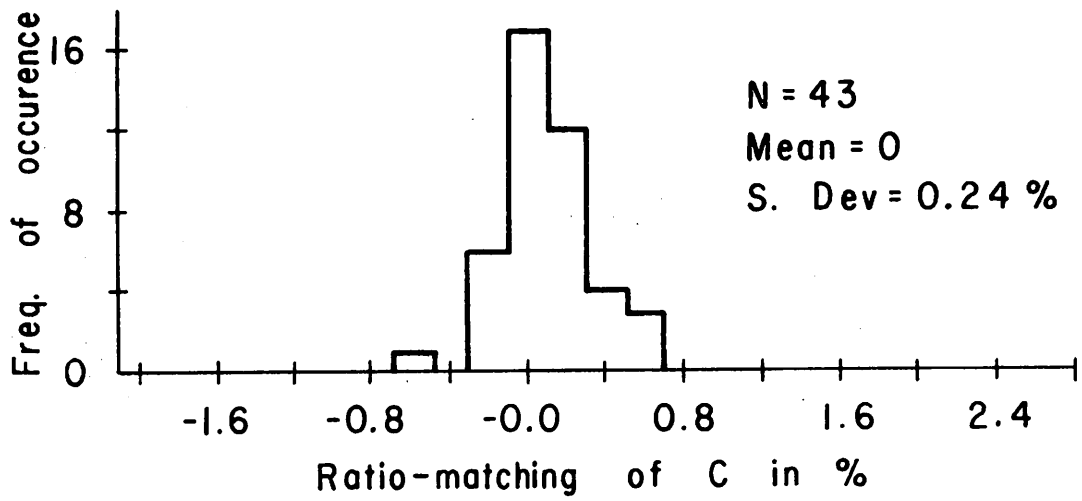


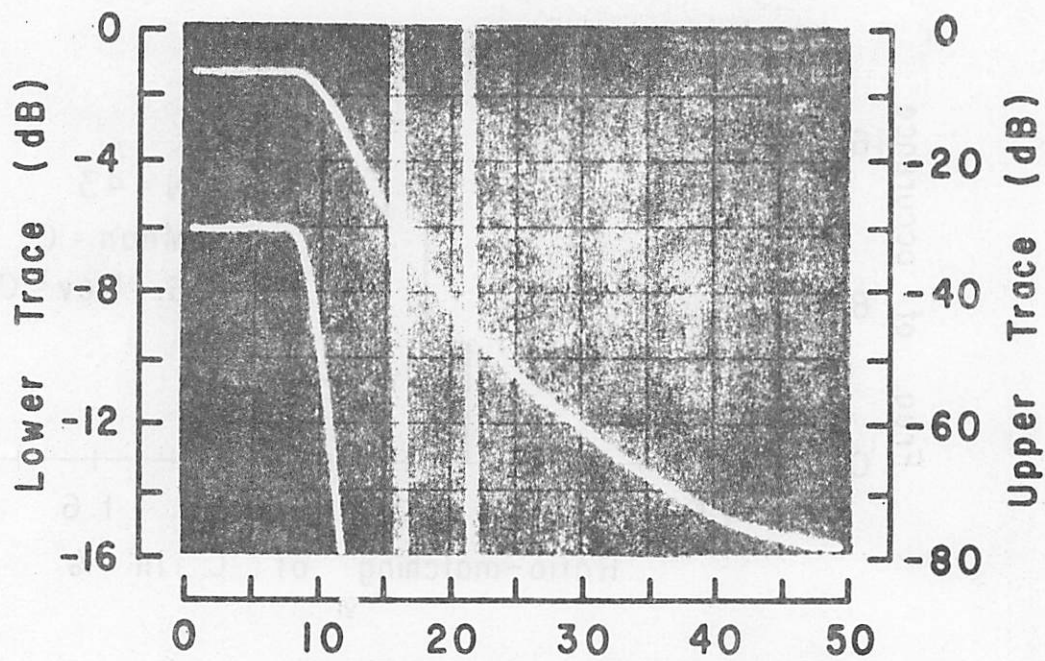
(b)



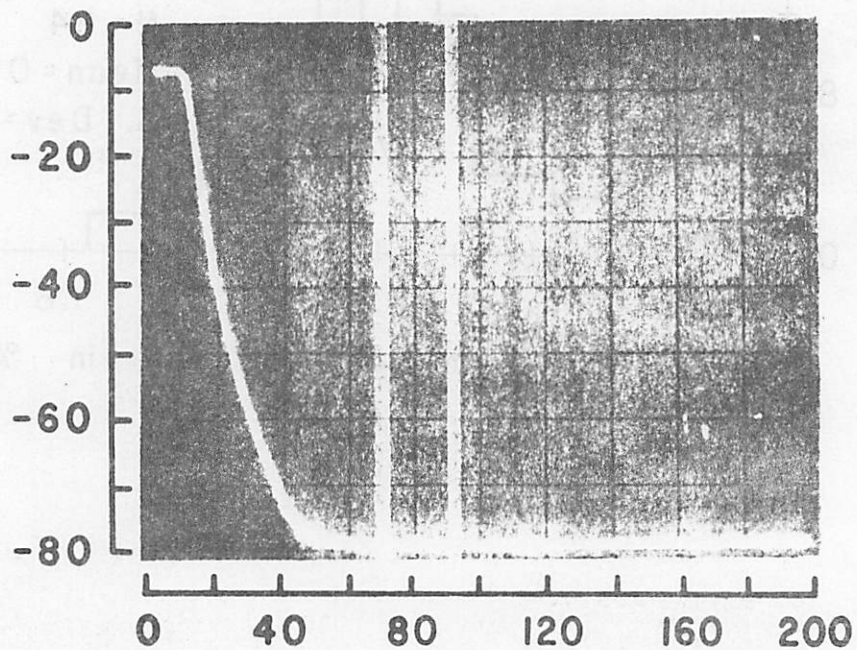








(a) Frequency (kHz)



(b) Frequency (kHz)