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Memorandum No. UCB/ERL M78/70

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INTRODUCTION

Frequency selective analog filtering has long evaded the efforts of technologists and designers to develop filter realizations which can be completely integrated on a silicon chip. The development of low-cost, high-performance monolithic operational amplifiers led to the utilization of active RC filtering techniques to replace passive RLC filters in the 1960s. Classical RC active filters have proven difficult to realize in completely monolithic form because stable, precise RC products cannot be achieved in standard monolithic processes. As a result, the preferred technological approach to voice-frequency analog filtering until very recently has been discrete component or hybrid integrated circuit realizations of various types of active filters. Recent developments in monolithic circuit techniques offer the possibility of fully integrating the voice-frequency filtering function, with resultant savings in manufacturing cost. One of these techniques, the switched-capacitor approach, is the subject of this paper.

This technique makes use of the unique properties of metal-oxide-semiconductor (MOS) integrated circuit technology. This technology has become widely used in the realization of digital LSI circuits because of its superior logic density, which arises from the fact that, in contrast to bipolar, the MOS transistor is self-isolating. While the density advantage of MOS has led to its wide utilization for digital circuits, a second key advantage, which has only recently been recognized, has led to the increasing use of MOS technology to perform analog signal processing. In contrast to bipolar technology, MOS integrated circuits offer the ability to store charge on a node over a period of many milliseconds and to sense the value of the charge continuously

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ABSTRACT

In the past several years, much progress has been made in bringing the economies of integrated circuit technology to bear on the realization of voice band frequency selective filters. This paper will review one approach to this problem, the use of switched capacitor techniques. The paper emphasizes the practical aspects of switched-capacitor filter design under the constraints imposed by MOS integrated circuit technology. The basic operation of switched capacitor filters is reviewed, followed by a discussion of the properties of the various circuit building blocks in MOS technology. Finally, a summary of several filter organizations which appear to be well suited to switched-capacitor implementation are described.

Research sponsored by the Naval Research Laboratory Contract N000173-77-C-0238.

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This technique makes use of the unique properties of metal-oxide-semiconductor (MOS) integrated circuit technology. This technology has become widely used in the realization of digital LSI circuits because of its superior logic density, which arises from the fact that, in contrast to bipolar, the MOS transistor is self-isolating. While the density advantage of MOS has led to its wide utilization for digital circuits, a second key advantage, which has only recently been recognized, has led to the increasing use of MOS technology to perform analog signal processing. In contrast to bipolar technology, MOS integrated circuits offer the ability to store charge on a node over a period of many milliseconds and to sense the value of the charge continuously

and non-destructively. The former results from the high impedance of the MOS transistor in the off state, and the latter results from the essentially infinite input impedance of the MOS transistor in the active mode of operation. This inherent analog memory capability does not exist in bipolar technology because the recombination current associated with the flow of minority carriers in a bipolar transistor rapidly discharges the small capacitance on which the voltage information is stored.

The charge storage feature of MOS technology was first utilized in dynamic random access memory design and dynamic logic. In both instances, information storage on small nodal capacitances in the circuit allows the elimination of active or pullup transistors which are otherwise required to preserve the information content of the circuit. This results in greater circuit density. While the information stored on nodal capacitance is essentially analog in that the node voltage has a continuous range of values, in digital applications the information is usually interpreted as being only one of two logic levels; these binary levels are typically refreshed (restored) every two milliseconds.

The charge storage feature of MOS technology was first used to perform analog signal processing with the advent of the bucket brigade shift register. In this device, a time-varying analog signal is converted to a series of charge packets, proportional to the value of the input signal at the sample instants. These charge packets are passed serially through a chain of MOS capacitors, the motion of the charge being brought about by the action of appropriately clocked MOS devices. In analog filtering applications of such devices, the charge at each capacitor site is sensed non-destructively by MOS transistors. These sensed voltages

can, for example, be added in a weighted summation to produce a single output, providing a realization of a sampled-data transversal filter [1].

The charge-coupled device (CCD), which was developed subsequent to the bucket brigade, provides a similar function in analog signal processing applications, but with the integration of the storage capacitance with the MOS switch structure and MOS sensing device in such a way that transversal filters and other analog signal processing devices can be fabricated in a smaller silicon area and achieve higher performance. These devices provide an extremely effective technological tool for attacking filtering problems in which transversal filter structures are required, for example as matched and adaptive filters [2].

However, the utilization of CCD and bucket brigade filters in large-quantity low-cost general filtering applications has been hindered by several factors. First, until very recently, the peripheral circuitry required to convert the input signal into charge packets, and to recover a low-impedance voltage signal at the output, had to be realized off-chip since this circuitry was not thought to be easily realizable on the same chip. Second, the transversal filter itself has certain limitations as a general-purpose analog filtering and signal processing technique. Among these is the fact that since the signal is time sampled at the input to the CCD, a continuous-time anti-aliasing filter is required to bandlimit the input signal to a frequency below the sampling rate. Since the sampling rate in CCD's must be relatively low (to minimize filter length and conserve silicon area) a relatively complex anti-aliasing filter is required. Also, since CCD filters are non-recursive, for transfer functions with a narrow passband which have long impulse responses, a very long CCD filter utilizing large silicon area is required.

In the last two years, the concept of analog charge storage and processing in MOS technology has been applied in new ways and has overcome some of the difficulties inherent in the transversal filter structures. First, in order to obtain highly selective filters with long impulse responses in a small silicon area, one is led to adopt a recursive filter structure. The classical second-order recursive filter section, shown in Fig. 1, requires two delay elements (shown as a D) and four multiplication elements which can be greater than unity. While a passive charge-coupled structure can realize the delays, an active amplifier of some type must be used to provide gain. This second-order recursive section can perhaps be most efficiently realized by simply using two capacitive delay elements together with several amplifiers as shown in Fig. 2 [3,4]. This structure has the advantage that infinitely long impulse responses can be obtained, but it suffers from the disadvantage that as one attempts to make the sampling rate higher to ease the anti-aliasing requirements, the sensitivity of the filter response to variation in the parameters α_1 and α_2 becomes larger. Since in an analog recursive filter like the one shown in Fig. 2, these coefficients are realized using ratioed passive components, a severe practical limitation is imposed on the range of sample rates and the selectivity of responses obtainable from analog realizations of these filters.

The recursive section of Fig. 2 consists of analog switches, operational amplifiers, and capacitors. These same elements can be rearranged to provide many alternate filtering configurations with sensitivity properties more closely resembling those of continuous-time filters, in the limit of high sampling rates. These filters have come to be called switched-

capacitor filters, and are distinguished by the fact that they utilize a capacitor and MOS switches to simulate the circuit behavior of a resistor, as shown in Fig. 3 [5,6,7].

The operation of this "resistor" is as follows: the switch is initially in the left-hand position so that the capacitor C is charged to the voltage V_1. The switch is then thrown to the right and the capacitor is discharged to the voltage V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C(V_2-V_1)$. If the switch is thrown back and forth at a clock rate f_c, then the average current flow i from V_1 into V_2 will be $C(V_2-V_1)f_c$. Thus the size of an equivalent resistor which would give the same average current as this circuit is

$$R = \frac{1}{Cf_c} \tag{1}$$

If the switched rate is much larger than the signal frequencies of interest then the time sampling of the signal which occurs in this circuit can be ignored in a first-order analysis and the switched capacitor can often be considered as a direct replacement for a conventional resistor. If, however, the switch rate and signal frequencies are of the same order then sampled data techniques are required for analysis and, as for any sampled data system, the input signal should be bandlimited as dictated by the sampling theorem.

Note that we have assumed that V_1 and V_2 are voltage sources, and that the values of V_1 and V_2 are not affected by the switch closures. While this is in effect true in the filters to be described in this paper, which are based on switched-capacitor integrators, it is not true in more general circuits containing capacitors and switches. In these cases simple substitution of switched capacitors for resistors can give results different from the continuous case.

The switched-capacitor resistors require very little silicon area to implement large resistance values. In fact the silicon area decreases as the required value of resistance increases. To implement audio frequency filters a resistance on the order of 10 mΩ is needed if a monolithic capacitor of a reasonable size is to be used (~10 pF). This value of resistance is easily achieved by switching a 1 pf capacitor at 100 kHz rate, requiring approximately a silicon area of .01 mm^2 (to be compared to a total chip area of 10-20 mm^2). If a 10 MΩ resistor were implemented by using a polysilicon line or diffusion the area required would be at least 100 times larger.

By using this switched-capacitor resistor in conjunction with other capacitors and op amps it is possible to realize many of the circuit configurations used in conventional RC active filters. As in the case of the recursive filter of Fig. 1 and the CTD filters, the signal in switched-capacitor filters is sampled in time so that anti-aliasing filter is required. However, in contrast to the circuit of Fig. 2, as the sampling rate is increased the sensitivities generally decrease to those of the continuous-time RC active counterpart. Also the penalty in silicon area for a high sample rate is much less in the switched-capacitor filters in comparison to the CTD transversal filters.

Viewed from a conventional RC active filter standpoint, these filters have the property, which will be demonstrated below, that all the RC time constants of the filter are determined by the clock frequency which is used to drive the switches and by capacitor ratios. Thus the problem

and by capacitor ratios. Thus the problem of controlling RC products of controlling RC products to a high degree of accuracy, which is characteristic of RC active filter realizations, is reduced for these filters to the problem of maintaining accurate capacitor ratios and supplying an accurate external clock frequency. This property makes the filters much more practical for monolithic realization.

A conventional single pole RC lowpass filter is shown in Fig. 4a and a switched capacitor implementation of this filter is shown in Fig. 4b. In spite of the simplicity of this filter it demonstrates some of the most important advantages of the use of switched capacitors. The 3 dB bandwidth of the conventional RC filter is

$$\omega_{3dB}^{RC} = \frac{1}{R_1 C_2} \tag{2}$$

The 3 dB width of the switched capacitor filter can be approximately found by substituting the effective resistance of the switched capacitor C_1 into Eq. 1 to obtain

$$\omega_{3dB}^{SC} \approx f_c\left(\frac{C_1}{C_2}\right); \quad f_c >> \omega_{3dB}^{SC} \tag{3}$$

(The constraint that $f_c >> \omega_{3dB}^{SC}$ is imposed in order that the effect of time sampling and charge sharing can be ignored.) Since the bandwidth of the switched capacitor filter is proportional to a ratio of capacitor values, it can be accurately defined with a high degree of stability

From Eq. 3 it can be seen that ω_{3dB}^{SC} is proportional to the clock frequency; thus programmability can be achieved by simply varying the clock rate (a property which is common to all discrete time filters).

If one were restricted to the use of passive components and switches as in the case of Fig. 4b, a very limited class of filter responses would be possible. It is possible, however, to design MOS operational amplifiers that can be used with switches and capacitors so as to extend greatly the capability of the filters. In the next section the limitations of the MOS technology and its relation to switched capacitor filter circuits will be described.

PROPERTIES OF MOS SWITCHES, CAPACITORS, AND OPERATIONAL AMPLIFIERS

The properties of MOS technology and the switched capacitor resistors place significant limitations on the range of realizable filter configurations. In this section these limitations are explored.

A. MOS Capacitors

The MOS transistor itself is essentially a nonlinear capacitor in which the charge induced on one plate by the applied voltage forms the conducting channel of the transistor. The dielectric of this capacitor is silicon dioxide, which is one of the most stable dielectrics known. However, the MOS transistor itself is not particularly useful as a capacitor because of its inherently nonlinear behavior. Within an MOS integrated circuit, capacitors which have a sufficiently low voltage coefficient to be useful as precision passive components are generally made in one of several ways:

1. Metal/oxide/crystalline silicon capacitors. This structure is formed by utilizing a heavily doped (low resistance) region in the silicon substrate as the capacitor back plate, and the interconnect metallization (usually aluminum) as the top plate. This particular capacitor type is best suited to metal-gate CMOS and MOS processes which do not use self-alignment procedures and can thus realize the capacitors directly without process modifications.

2. Poly-silicon/oxide/Poly-silicon capacitors. In this capacitor structure, the two plates of the capacitor are formed of two separate layers of poly-silicon (deposited polycrystalline silicon). This capacitor structure is best suited to silicon gate NMOS and CMOS processes having two poly-silicon layers, which can realize these capacitance structures without extra process steps.

3. Other capacitance structures. By including extra masking steps, any combination of silicon substrate, poly-silicon layer, and metallization layer can be used as the plates of the capacitors. However, such structures are only needed in silicon gate processes which have only one layer of poly-silicon.

These capacitance structures tend to have common characteristics. From the standpoint of switched-capacitor filters, the most important of these characteristics are:

1. Ratio accuracy. A key aspect of the performance of any frequency-selective filter is the accuracy and reproducibility of the frequency response. For switched-capacitor filters this requires a certain level of accuracy in the ratios of capacitors. Integrated MOS capacitors have a value which is determined by the dielectric constant, the thickness of the dielectric and the area of the capacitor. Assuming that the dielectric constant and thickness do not vary, the ratio of two capacitors made within the same integrated circuit will depend only on their area ratio. This is primarily determined by the geometrical shape of the capacitors defined by the photolithographic mask used to make the integrated circuit.

Errors in the geometrically defined ratio occur because the actual definition of the capacitor is done optically, which results in errors in the capacitor edge location due to the finite wavelength of the

light used and the control of the chemical or plasma etching of the metallization and in addition because the thickness of the dielectric can vary with distance across the integrated circuit. These effects can be alleviated with careful layout of the components and the errors generally get smaller as the capacitor dimensions are made larger. Generally speaking, the achievable ratio accuracies range from 1-2% for small capacitor geometries (~400 μ^2) to on the order of .1% for capacitor geometries which approach the limit of economical size (40,000 μ^2) [8]. This also implies that as the capacitance ratio gets larger, the achievable accuracy in a given area decreases since the smaller of the two capacitors must be decreasing.

2. Voltage coefficient and temperature coefficient. MOS capacitors made with heavily doped silicon plates display voltage coefficients in the range of 10 to 100 parts per million per volt. Temperature coefficients are generally in the range of from 20 to 50 parts per million per degree centigrade and are of course much lower for the value of a ratio [8]. These variations are low enough to be insignificant in almost all applications.

3. Parasitic capacitances. In both poly-silicon/poly-silicon capacitors and in metal-silicon capacitors, a sizable parasitic capacitance exists from the bottom plate of the capacitor to the substrate. In the case of poly-poly capacitors, this is the capacitance of the SiO_2 layer under the first layer of poly. In the case of metal-silicon capacitors, it is the capacitance of the P-N junction surrounding the heavily doped region. Typically, this capacitance has a value of from one-fifth to one-twentieth of the MOS capacitor itself, depending on the technology. Also, because the top plate of the MOS capacitor must be connected to other circuitry, a small capacitance will exist from the top plate to the substrate due to the interconnections. This capacitance can

range from .01 to .001 of the desired MOS capacitance, depending on the capacitor size, layout and technology. These parasitic capacitances are unavoidable, and the design of switched capacitor filters must be done in such a way that they do not degrade the performance of the filter.

B. MOS Switches

The second principal component in switched-capacitor filters is the MOS switch. This device behaves like a resistor in the on state and in the off-state like an open circuit. The important parameters of the MOS transistor from the standpoint of switched-capacitor filters are the on resistance, off leakage currents, and the parasitic capacitances. Typical NMOS silicon gate technology is capable of producing switch devices with a channel length of 5 microns and, assuming a length/width ratio of unity, an on resistance of 5k ohms (with a gate drive voltage of five volts with respect to the source). This device would display a leakage current from the source and drain to the substrate of on the order of 10^{-14} amps at 70 degrees centigrade. The parasitic capacitance from source and drain to substrate would be about .020 pF (picofarads) each, and the overlap capacitance from drain to gate and source to gate would be about .005 pF. The charge induced in the channel when the gate potential is five volts more positive than the source and drain is approximately .03 picocoulombs. The values of capacitances used as passive components in switched-capacitor filters typically range from 1 to 20 pF. Thus the effect of the various parasitic capacitances on the behavior of the filter must be carefully considered, as well as the flow of the charge stored in the channel of the transistor.

C. MOS Operational Amplifiers

Until very recently, virtually all commerically manufactured operational amplifiers were fabricated utilizing either bipolar technology or a mixture of bipolar and MOS technology. Recently, the trend toward higher levels of integration on MOS-LSI chips has led to the need for all-MOS operational amplifiers to be included on such chips. Considerable recent work has been carried out directed towards the realization of CMOS and NMOS operational amplifiers. Typically achieved levels of performance are a gain of from 60 to 80 dB, common-mode and power supply rejection ratios of 60 dB, unity-gain bandwidth of 2 MHz, and power dissipation of 5-15 mW [9]. These devices typically occupy a die area on the order of .2 mm^2, so that the inclusion of several tens of them on a single chip is feasible.

D. Sampled-data Differential Integrators and Summers

Often in filter design the need arises for a differential integrator, which integrates the difference between two analog voltages. The traditional approach to this function is shown in Fig. 5a, and requires two matched capacitors and two matched resistors. The input-output relation for this circuit is

$$V_{out} = \frac{-\left(\frac{1}{R_1 C_2}\right)}{j\omega} (V_1 - V_2) \tag{4}$$

The differential integrator function is quite amenable to realization in switched-capacitor form as shown in Fig. 5b. Here, the basic switched-capacitor concept has been used to replace a resistor (Fig. 3), but in addition, the capability of the capacitor to perform a level shift function has been utilized. The result is a particularly

efficient realization of the integrator which for frequencies much less than the clock rate, realizes the following input-output relation:

$$V_{out} = \frac{-\left(\frac{f_c C_1}{C_2}\right)}{j\omega} (V_1 - V_2) \tag{5}$$

Switched capacitor differential integrators are subject to several important deviations from ideal behavior. These result from the parasitic capacitances from each plate of the capacitor to ground, and from finite bandwidth and gain in the operational amplifier. The effect of the parasitic capacitances on the circuit are illustrated in Fig. 6. For the integrating capacitor C_2, the parasitic capacitance, C_{SUB2}, from the op amp output to ground has no effect on circuit operation, since it is driven from the op amp output voltage source. (Unless, it is too large, when it can cause stability problems in the op amp). Assuming that an amplifier of sufficiently high gain is used, the parasitic capacitance C_{p2} from the inverting input of the operational amplifier to ground does not affect circuit operation since the steady state voltage does not change at this input. Further, the parasitic capacitance, C_{SUB1}, from the bottom plate of the sampling capacitor C_1 has no effect on circuit operation because it is always connected to either an input voltage or to ground. Therefore, the only parasitic capacitance of any significance is that from the top plate of the sampling capacitor to ground, C_{p1}. The charge placed on this capacitor when the input sampling switches are on is transferred into the integrating capacitor. This results in a transfer function from input to output of

$$V_{out} = \frac{-f_c}{j\omega} \left[\frac{C_1}{C_2} (V_1 - V_2) + \frac{C_{P1}}{C_2} V_1 \right] \tag{6}$$

which can be rearranged to give:

$$V_{out} = \frac{-f_c}{j\omega}\left[\left(\frac{C_1 + \frac{C_{p1}}{2}}{C_2}\right) V_{dm} + V_{cm}\left(\frac{C_{p1}}{C_2}\right)\right] \tag{7}$$

where $V_{dm} = V_1 - V_2$ and $V_{cm} = (V_1+V_2)/2$. Thus the effect of C_p cause the integrator to have a degraded common mode rejection ratio (CMRR) and to change slighly the differential mode gain constant. By making C_1 and C_2 large compared to C_{p1} the CMRR can be increased to any desired level. Practical circuits generally have a CMRR of 40-60 dB.

If the filter circuit only requires a non-inverting integrator (i.e. $V_1 = 0$, $V_2 = V_{IN}$) then from Eq. 6 it can be seen that the integrator is unaffected by the parasitic capacitance. Therefore it is possible to use a very small value for C_1 and/or C_2 to obtain very large ratios (>200) without consuming large amounts of silicon area.

The frequency response of the switched capacitor integrator shown in Fig. 5b deviates from that of the continuous one in Fig. 5a in a very important way. The sampling process inherent in the switching introduces an excess phase shift at frequencies approaching the clock frequency in the switched capacitor version. A straightforward analysis (over a complete clock cycle) of the switched-capacitor integrator gives a frequency response:

$$H_1(\omega) = -\left[\frac{(C_1\ f_c/C_2)}{j\omega}\right] \frac{\omega T_c}{2\ \sin(\omega T_C/2)}\ e^{-j\omega T_o/2} \tag{8}$$

The first term in brackets is the response of an ideal continuous integrator, and the rest of the expression is the deviation from that response caused by the sampling process. The most important aspect of this deviation is the delay term. The resulting excess phase shift will distort the frequency response of the complete filter in a way which

is similar to the effects of excess phase shift in operational amplifiers in conventional RC active filters. Typically, this distortion takes the form of Q-enhancement, in which the response of the filter shows some undesired peaking.

The problem of excess phase due to sampled data effects can be attacked in three ways. The filter can be pre-distorted so that the response is the desired one when the excess phase is present. This approach has the disadvantage of increasing component sensitivity and also considerably complicating the design of filters requiring transmission zeros in the response. A second approach is to use a more complex integrator which inherently has less excess phase shift. Several such configurations have recently been proposed [11]. Perhaps the simplest approach is one based on earlier work by Bruton [10] on digital integrators, in which it was shown that the excess phase in the simple digital integrator could be precisely removed by decreasing the delay time through the integrator block by precisely one-half clock cycle. In ladder filters, in which one integrator always samples the output of another integrator, one can alternatively remove a full unit of delay from every other integrator. Fortunately, this can very easily be accomplished in switched-capacitor filters by simply reversing the phase of alternate clocks in the ladder filters. This clocking technique has been termed lossless digital integrator (LDI) clocking after Bruton. The correct switch phasing for the LDI clocking scheme is illustrated in Fig. 7 [11].

In addition to integrating a signal it is often necessary to sum one signal with the integrated value of other inputs. The circuit in Fig. 8 performs this function with only one op amp. The output of this circuit is

$$V_{OUT} = -\left(\frac{f_c C_\mu}{C_T}\right)\frac{V_{TN}}{j\omega} - \frac{C_S}{C_1} V_x \tag{9}$$

where it is assumed that the clock rate is high enough that the sampled-data effects are not important.

The effect of finite op amp open-loop gain is to cause the integrator to display a pole at some finite low frequency rather than at zero frequency. Typically, this pole is a factor of 1000 or more below the unity-gain frequency of the integrator (as determined by the op amp open loop gain) so that this behavior does not usually have an important effect on filter performance.

There are two primary sources of noise in switched-capacitor integrators. The first is due to the thermal noise in the MOS transistor switches. When a MOS transistor switch is in the ON state connecting a capacitor, C, to a voltage source, the thermal noise power in the resistive channel of the switch (4kTR) appears in series with the voltage source. The noise source is bandlimited by the RC circuit formed by the on resistance of the switch, R, and the sampling capacitor. This single pole low pass circuit has a noise bandwidth of $\frac{1}{4RC}$. The bandlimited noise power is therefore

$$V^2_{rms} = (4kTR)\left(\frac{1}{4RC}\right) = \frac{kT}{C} \tag{10a}$$

When the switch is turned off this noise is then sampled and held on the sampling capacitor.

In the switched-capacitor integrator, the noise contributed by each of the two switches must be considered. The analysis outlined above applies directly to the noise contributed by the switch between the input and the sampling capacitor. The analysis of the noise contributed by

the switch between the sampling capacitor and the operational amplifier input is more complex because it involves the frequency response of the operational amplifier itself and the timing of the switches sampling the amplifiers output. However, it appears that the noise contributed by this device is similar in magnitude to that contributed by the first switch.

More quantitative noise analysis can be made on the passive low pass circuit of Fig. 4, which gives insight into the noise to be expected from the use of switched-capacitors in place of resistors. Since the circuit of Fig. 4a is the same type of circuit which was analyzed in arriving at Eq. 10a (bandlimited resistor noise) the output noise of this simple RC circuit is

$$V_{rms}^2 = \frac{kT}{C_2} \tag{10b}$$

To calculate the noise of the switched-capacitor circuit of Fig. 4b it is necessary to take into account the noise of the two switches, the capacitive division of this noise and the two separate sampling operations which occur each clock cycle. This calculation yields an output noise for the switched capacitor circuit of

$$V_{rms}^2 = \left[\frac{kT}{C_2}\right] \left\{ \frac{\left(\frac{C_1}{C_2}\right)\left(2 + \frac{C_1}{C_2}\right)}{\left(1 + \frac{C_1}{C_2}\right)^2} \right\} \tag{10c}$$

Since the factor in curly brackets is always less than one, by comparison with Eq. 10b it can be seen that the switched capacitor circuit always has less noise than its RC equivalent. In fact if the ratio C_1/C_2 is small, the noise of the switched capacitor circuit is substantially lower (eg. if $C_1/C_2 = .2$, the factor is .17).

The second important noise source is that of the operational amplifiers.

Since the most attractive feature of these filters is that they can be completely integrated in NMOS technology, one must carefully consider the effects of the relatively noisy NMOS operational amplifiers (compared to bipolar amplifiers) which must be used. These amplifiers inherently display a relatively high value of 1/f noise because of the surface behavior in the channel of the MOS transistors. This low frequency noise falls in the passband of voice-frequency filters. For typical NMOS-LSI processes, this noise restricts the dynamic range of these filters to the range of 90-100dB or less.

A second important noise source related to the operational amplifier is the broadband noise of the amplifiers, which is aliased into the passband by the sampling process. This can be an important source of noise unless the operational amplifier is designed to have a low level of noise output at frequencies beyond its own unity-gain frequency.

E. Practical Considerations for MOS Implementation

The techniques have been shown for implementing all the basic building blocks of conventional RC active filters using MOS technology. There are, however, some constraints on the type of active filters which can be used that are imposed by some additional practical aspects of the MOS circuit elements, if high performance filters are required.

1. Switched capacitor resistors cannot close an op amp feedback path.

Since the switched-capacitor resistor does not provide a continuous time path, it cannot be used to provide the continuous time feedback necessary to stabilize an op amp; as required for example in negative immittance converter filter circuits. However, switched-capacitor resistors

can be used in conjunction with capacitors to shape the frequency dependence of the feedback as long as a continuous time path exists.

This constraint complicates the design of circuits which require a precise value of closed loop gain (such as often required in voltage controlled-voltage source filters), since capacitors and switched capacitors must be connected in parallel in order to insure a continuous feedback path for the op amp as well as stability against charge accumulation. Alternatively, conventional diffused or ion-implanted resistors could also be used, but they result in increased power dissipation.

2. No floating nodes

All capacitive plates are subject to charge accumulation from a variety of parasitic sources such as leakage currents, electromagnetic radiation and transient power-up conditions. In order to insure stability of the circuit there must be a path either directly or through switched-capacitor resistors from every node in the circuit to a voltage source. For example the top plate of capacitor C_2 in Fig. 4b is stabilized against parasitic charge build up because it is indirectly connected to the input voltage source, V_{IN}, through the switched-capacitor resistor C_1.

3. At least one plate of every capacitor must be connected to a voltage source or switched between voltage sources. The nonlinear parasitic capacitance between the lower plate of any capacitor and the substrate must be connected to either a voltage source or switched between voltage sources. It will then be charged and discharged, but will not affect the filter response. This therefore rules out capacitive voltage dividers which are composed of three or more series capacitors or circuits which sequentially switch both ends of a capacitor into an op amp.

4. The non-inverting op amp input should be kept at a constant voltage. If the positive input of the op amp is connected to a signal voltage then the filter response is sensitive to all the parasitic capacitances due to switches, bus lines and substrate that are connected to the inverting input. In addition, increased common-mode performance is required of the op amp.

III. Switched Capacitor Filter Organizations

In spite of the constraints imposed by the MOS technology there still remains a large variety of possible active filter organizations which can be used for monolithic implementations.

One class of filters which are particularly well suited to switched capacitor techniques are those which use op amps as integrators in the same way they would be used in an analog computer realization [16]. This class of filters is closely related to such commonly used circuits as the infinite gain-multiple feedback, state variable, and leapfrog (or active ladder) filters. An important advantage of these types of filters is that they can be organized so that there is a close correspondence between these circuits and passive LC ladder networks. By exploiting this correspondence the extensive tables available for the LC networks can be used to considerably decrease the filter design effort. Also by simulating passive LC circuits the active filter retains the low sensitivity of the frequency response to errors in the element values which is present in the passive network.[15] In particular a doubly-terminated LC ladder which has been designed for maximum power transfer in the passband has very low sensitivity of the passband response to first order changes in the values of the L and C elements. For the switched-capacitor implementation this implies an extremely low sensitivity of the filter response to the accuracy of the

capacitor ratios.

A second-order lowpass filter will be discussed in detail to demonstrate the design techniques as well as the practical considerations. The extension to higher-order lowpass, bandpass and highpass filters is then relatively straightforward and will be discussed briefly.

A. Second-Order Lowpass Filter Example

In this section a switched capacitor simulation of a two pole singly terminated LC ladder (Fig. 9a) will be derived and then related to state variable and infinite gain-multiple feedback filters. A single rather than double termination is used because for this low-order filter only a small decrease in sensitivity is obtained with the addition of a second termination which does not justify the extra circuitry (for higher-order filters the sensitivity decreases with two terminations is much more dramatic).

The values of the L and C values for the passive prototype filter can be found from standard design tables for a normalized lowpass filter; i.e. $R_T = 1\Omega$ and a cutoff of $\omega_{co} = 1$ rad/sec. An abbreviated version of these tables is given in Table I which gives the values of L and C for a few of the standard filter responses. The relationships between the table values $\mathcal{L}$ and $\mathcal{C}$ and LC values for arbitrary values of the cutoff frequency, ω_{co}, and termination resistance, R_T, are,

$$L = \frac{\mathcal{L} R_T}{\omega_{co}} \tag{11a}$$

$$C = \frac{\mathcal{C}}{R_T \omega_{co}} \tag{11b}$$

In Fig. 9a the node voltages and loop currents are defined for the passive circuit. The equations which describe this network can be written so that they only contain integrations:

$$V_1 = V_{IN} - R_T i_1 \tag{12a}$$

$$i_1 = \frac{1}{SL} (V_1 - V_2) \tag{12b}$$

$$V_2 = \frac{1}{SC} i_1 \tag{12c}$$

$$V_{OUT} = V_2 \tag{12d}$$

Since the op amps which will be used to implement this circuit are voltage controlled-voltage sources it is necessary to represent the current i_1 by a voltage, V_1'. This can be accomplished by multiplying i_1 by a scaling resistance, R_S, so tht $V_1' = i_1 R_S$. The resulting all voltage equations which maintain the proper relationships between the voltage and current nodes are:

$$V_1 = V_{IN} - \frac{R_T}{R_S} V_1' \tag{13a}$$

$$V_1 = \frac{R_S}{SL} (V_1 - V_2) \tag{13b}$$

$$V_2 = \frac{1}{S R_S C} V_1' \tag{13c}$$

$$V_{OUT} = V_2 \tag{13d}$$

Figure 9b is a schematic representation of the circuit which represents these equations in which the bandwidths of the two integrators are (R_S/L) and $(1/R_S C)$. This two integrator loop structure is more commonly known as a second-order state variable network. This network

is very versatile since in addition to the low pass response which is available at V_2, a bandpass response is simultaneously present at the V_1' node and a high pass at V_1.

The switched-capacitor implementation of the network of Fig. 9b is obtained by replacing the conventional integrators with their switched-capacitor equivalents shown in Fig. 5 which yields the network in Fig. 9c. The termination path, R_T/R_S, is implemented by the capacitor, C_T, which is switched between the input and output of the first integrator. The capacitor ratios in Fig. 9c can be determined in terms of the normalized L and C values given in Table II, $\mathcal{L}$ and $\mathcal{C}$, by combining Eqs. 1, 11 and 13,

$$\frac{C_T}{C_L} = \left(\frac{\omega_{co}}{f_c}\right) \frac{1}{\mathcal{L}} \tag{14a}$$

$$\frac{C_L}{C_u} = \mathcal{L}\left(\frac{R_T}{R_S}\right)\left(\frac{f_c}{\omega_{co}}\right) \tag{14b}$$

$$\frac{C_C}{C_u} = \mathcal{C}\left(\frac{R_S}{R_T}\right)\left(\frac{f_c}{\omega_{co}}\right) \tag{14c}$$

where C_u is a unit capacitor which other capacitors are ratioed against, f_c is the clock rate of the switches and ω_{co} is the desired cutoff frequency (in rad/sec) of the filter.

The value of the ratio R_S/R_T is a free variable which can be used to maximize the filter dynamic range as well as to adjust the capacitor ratios $\frac{C_L}{C_u}$ and $\frac{C_C}{C_u}$ in order to minimize the silicon circuit area required for implementation. From Eqn. 14 it is seen that the minimum ratios are achieved when $\frac{C_L}{C_u} = \frac{C_C}{C_u}$ which implies that

$$\frac{R_T}{R_S} = \left(\frac{\mathcal{C}}{\mathcal{L}}\right)^{1/2} \tag{15}$$

The maximum dynamic range of the filter is achieved when all the op amp

outputs have the same peak voltage. If the gain from the filter input to the output of an internal op amp is greater than the gain to the output of the filter, that internal op amp will saturate before the output amplifier saturates. On the other hand, if the gain to the interior op amp is low, then this implies that there will be gain from this node to the filter output and thus any noise generated in the internal op amp will be amplified.

For the filter in Fig. 9 the peak amplitude at V_1 and V_{OUT} occurs at a frequency $\omega_o = \frac{1}{\sqrt{LC}}$ which yields a gain to the internal op amp output, V_1' of

$$\frac{V_1'(\omega_o)}{V_{IN}(\omega_o)} = \frac{R_S}{R_T} \tag{16a}$$

and to the filter output, V_2 of

$$\frac{V_2(\omega_o)}{V_{IN}(\omega_o)} = \left(\frac{\mathcal{L}}{\mathcal{C}}\right)^{1/2} . \tag{16b}$$

From Eqs. 16a and 16b it is seen that if R_S/R_T is set by Eq. 15 then the dynamic range is maximized since all outputs have the same peak gain (as well as simultaneously resulting in the minimum size for the capacitors). The optimization of the design for dynamic range and minimum circuit area is particularly simple for this low order filter since simple analytic expressions can be obtained. For higher order filters the same general considerations for the R_S/R_T ratio hold, but the optimum values are more dependent on the particular frequency response.

Up to this point in the analysis it has been assumed that the clock rate has been sufficiently high that the magnitude errors in the integrators due to the time delay through the switched capacitors have had a negligible effect on the frequency response of the filters. In order to

check the validity of this assumption or if it is desirable to operate the clock at a low rate (a small multiple of the cutoff frequency), a more exact analysis is desirable. The exact frequency response can be found by analyzing the equivalent discrete time circuit for the filter. In Fig. 9d such an equivalent circuit is shown for the lowpass filter of Fig. 9c. The delay blocks (squares with a D) represent a half of a clock cycle delay ($\frac{T_c}{2} = \frac{1}{2f_c}$) which is obtained by the switch phasing shown in Fig. 7. The remaining elements are multipliers and summers as in conventional digital filters. The extra delay associated with the termination (the path which contains the C_T/C_L multiplier) results in a phase shift which has a relatively large effect on the frequency response of filters which have both a low Q(~1) and a low ratio of the clock rate to the filter cutoff frequency.

The z-transform transfer function of the discrete time network of Fig. 9d is given by

$$H(z) = \frac{\dfrac{C_u^2}{C_L C_c}}{z^2 - z\left(2 - \dfrac{C_T}{C_L} - \dfrac{C_u^2}{C_c C_L}\right) + \left(1 - \dfrac{C_T}{C_L}\right)} \tag{17}$$

The exact frequency response, $H(\omega)$, of the filter can be determined by evaluating $H(z)$ along the unit circle defined by $z = e^{j\omega T_c}$; i.e., $H(\omega) = H(z)\big]_{z=\exp[j\omega T_c]}$. The deviation of this discrete time switched capacitor transfer function from the response obtained with a continuous time prototype RLC filter response can be reduced by a modification of the capacitor ratios. The modified capacitor ratios $\left(\left(\frac{C_T}{C_c}\right)_M, \left(\frac{C_u}{C_c}\right)_M\right.$ and $\left.\left(\frac{C_u}{C_C}\right)_M\right)$ can be chosen by matching the Q and center frequency ω_o, of the two transfer functions where ω_o and Q are defined by the continuous time transfer function as follows:

$$H_{L.P.}(\omega) = \frac{\omega_o^2}{\omega_o^2 - \omega^2 + j\omega \frac{\omega_o}{Q}} \tag{18}$$

The values of the modified ratios in terms of the ratios calculated by using eqns. 14 and 15 $\left(\frac{C_T}{C_L}, \frac{C_u}{C_L} \text{ and } \frac{C_u}{C_c}\right)$ are

$$\left(\frac{C_T}{C_c}\right)_M = \left[1 - e^{-C_T/C_c}\right] \tag{19}$$

$$\left(\frac{C_u}{C_L}\right)_M^2 = \left(\frac{C_u}{C_u}\right)_M^2 = 1 - 2e^{-C_T/2C_c} \cos\left\{\left(\frac{C_u}{C_c}\right)^2 - \frac{1}{4}\left(\frac{C_T}{C_c}\right)^2\right\}^{1/2} + e^{-C_T/C_c} \tag{20}$$

In Fig. 10 a plot of the magnitude of the switched capacitor transfer function with modified ratios for a Butterworth (Q=.707) filter for clock rates 20 and 40 times the cutoff frequency of 1 kHz is compared to the continuous time LC filter response (or for $f_c = \infty$). Note that the responses are very close at frequencies $f \ll f_c$ but deviate as f appraoches f_c. The aliased response of the switched capacitor filter which is clocked at 20 kHz is clearly evident in the region near f = 20 kHz.

A simplification of the circuit shown in Fig. 9c can be made by recognizing that the integrator labeled L which has the negative feedback through capacitor C_T is in effect a lossy integrator which can be replaced by a switched-capacitor resistor and a capacitor to ground. The resultant circuit with resistors in place of switched-capacitors is known as an infinite gain-multiple feedback network [13]. Several filters of this form (shown in Fig. 11) were fabricated by Hostica et al. [14] using an n-channel metal gate MOS process. The filters which were fabricated included responses which had a high Q (Q=73) and low Q (Q=1). The two filters required about 2800 $(\text{mil})^2$.

In the top trace in Fig. 12a the frequency response of the high Q filter is shown. The reference level of 0 dB at DC corresponds to 0 dB insertion loss through the filter. The peak of the response is a factor of Q times larger (Q=73 yields 37 dB). Also shown in Fig. 12a is the noise spectral density (measured with a 30 Hz bandwidth) which has been amplified by 30 dB. As expected because of the 37 dB gain of the filter at the center frequency the noise also shows a peak at f_o.

In Fig. 13 the low Q filter response is shown as well as the noise of the filter (also after an amplification of 30 dB with a bandwidth of 30 Hz). Since this filter has very little gain in the passband the noise is not amplified, however the 1/f noise of the input MOSFETs of the amplifier can be seen. In Table II the measured and calculated filter performance is shown for a small sample of these filters.

B. High Order Lowpass

It is possible to implement higher order (>2) lowpass filters by cascading the second order sections which were just described. However, the frequency response will then exhibit relatively high sensitivity to component variations. A better method is to simulate a passive LC lowpass ladder which has the desired order [15]. A five pole network of this form is shown in Fig. 14a. Note that resistor terminations are used at each end of the ladder since this results in significant reductions in sensitivity for these high order filters.

Following a procedure similar to that used to obtain Fig. 9b and 9c, a switched capacitor simulation of the passive prototype five pole filter shown in Fig. 14a can be obtained and is shown in Fig. 14b.

This network is a switched capacitor implementation of what is known as the "leapfrog" or "active ladder" active filter circuit [16]. Using the switch phasing described in Fig. 7, the capacitor ratios are given by

$$\frac{C_{R_T}}{C_u} = \frac{R_S}{R_T} \tag{21a}$$

$$\frac{C_{C_i}}{C_u} = \mathcal{C}_i \left(\frac{R_S}{R_T}\right)\left(\frac{f_c}{\omega_{co}}\right) \; ; \; i = 1,3,5 \tag{21b}$$

$$\frac{C_{L_i}}{C_u} = \mathcal{L}_i \left(\frac{R_T}{R_S}\right)\left(\frac{f_c}{\omega_{co}}\right) \; ; \; i = 2,4 \tag{21c}$$

where $\mathcal{C}_i$'s and $\mathcal{L}_i$'s are the normalized values corresponding to a cutoff frequency of 1 $\frac{\text{rad}}{\text{sec}}$ and a 1Ω termination resistance, R_T, obtained from design tables. The input and output terminations, C_{R_T}, were set equal to minimize sensitivity, but if extremely low sensitivity is not required it is sometimes possible to reduce capacitor ratios by not setting them equal. The values of R_S and R_T are free variables as in the second order case and as discussed in the previous section their ratio should be chosen to minimize the capacitor ratios and maximize filter dynamic range (see the discussion leading to Eqns. 15 and 16). The modification of the capacitor ratios which was found to be necessary with low Q second order filters (Eqns. 19 and 20) due to the phase shift in the terminations has been observed not to be necessary for the higher order doubly terminated filters even for precise passband frequency characteristics as long as the clock rate is at least 10-20 times the cutoff frequency of the filter. A fifth order Chebychev filter was fabricated by Allstot et al. [17] which was designed for a .1dB

passband ripple and a cutoff frequency of 3400 Hz when clocked at a rate of 128 kHz. The die which required 6300 mil^2 is shown in Fig. 15 and the experimental frequency response is shown in Fig. 16. The measured performance is summarized in Table III.

C. The addition of Transmission Zeroes to Filter Response

The addition of finite transmission zeroes to a lowpass ladder filter response has great importance in many filter applications. The zero addition is easily accomplished on the LC lowpass prototype by adding a shunting capacitor across the series arm of the ladder network such as C_2 in Fig. 17(a). Imaginary axis zero locations are the resonant frequencies of the L-C tank circuit, i.e., $\omega_{zero} = [C_2L_2]^{-1/2}$. The active filter implementation of this non-canonical network is not as straight forward as the simple lowpass case. The usual approach to simulation of the circuit is suitable only for continuous-time active RC implementations as it contains voltage attenuators (multiplications separate from op amp integrators) [16]. This is not desirable in a switched capacitor implementation since additional op amps would be required.

In order to design a switched capacitor network with zeroes which does not require any additional operational amplifiers, it is useful to examine in detail the operations that are performed by the feed-through capacitors added to the lowpass ladder structure. Referring to Fig. 17(a), a three-pole, two-zero RLC filter is shown with voltages and currents defined. Using Kirchnoff's current law at nodes A and B, the following equations are derived to explain the function of C_2,

(this is shown symbolically in Fig. 17(b).

$$V_1 = \frac{(I_0-I_2)}{s(C_1+C_2)} + V_3\left(\frac{C_2}{C_1+C_2}\right), \tag{22}$$

and

$$V_3 = \frac{(I_2-I_4)}{s(C_2+C_3)} + V_1\left(\frac{C_2}{C_2+C_3}\right). \tag{23}$$

Thus, C_2 has been identified as an element that feeds some of the voltage V_3 to node V_1 and vice versa as well as to modify the integrator time constants. The integrator/summer circuit shown in Fig. 8 can be used to perform this function if minor modifications are made to the circuit to take into account the fact that all summations involve a sign inversion [11]. The complete switched-capacitor circuit is shown in Fig. 18. As seen in this figure the method described above for obtaining transmission zeros only requires two switches and four capacitors over the all pole circuit.

In the filter of Fig. 18 note that the input capacitor is twice the usual unit size ($2C_u$). This doubles the overall gain of the filter and avoids the 6dB insertion loss usually associated with doubly terminated filters.

A monolithic implementation of this version of an elliptic filter has been integrated [17] and is shown in Fig. 19 using standard MOS technology. The filter was designed for an elliptic lowpass response with 0.1 dB passband ripple, a cutoff frequency of 3400 Hz, and a transmission zero at 8.8 kHz when clocked at 128 kHz. Again, the measured performance shown in Fig. 20 agrees very closely with the design goals as summarized in Table IV.

D. Bandpass Filters

The technique of simulating passive RLC ladders which was used to implement the lowpass filters in the previous section is directly applicable to the design of bandpass filters. An important advantage of these filters is that because of their low sensitivity to component values it is possible to attain relatively high values of Q (up to ~100) with a high degree of precision.

The bandpass design is based on the use of the standard lowpass to bandpass transformation [12] which involves replacing each capacitor and inductor in a normalized lowpass circuit (e.g. see Table 1) with a parallel LC (tank) circuit and series LC circuit respectively. The values of the inductor and capacitor in the tank circuit which replaces a capacitor are

$$^{C}\mathcal{C} = \frac{\mathcal{C}Q}{\omega_o R_T} \tag{24a}$$

$$^{L}\mathcal{C} = \frac{R_T}{\mathcal{C}Q\omega_o} \tag{24b}$$

where ω_o is the center frequency of the desired bandpass filter, Q is the selectivity ($Q = \frac{f_0}{f_{BW}}$), f_{BW} is the 3dB bandwidth, and R_T the termination resistance.

The LC values of the series circuit which replace an inductor $\mathcal{L}$, are

$$^{L}\mathcal{L} = \frac{\mathcal{L}Q}{\omega_0 R_T} \tag{25a}$$

$$^{C}\mathcal{L} = \frac{R_T}{\mathcal{L}Q\omega_0} \tag{25b}$$

The passive prototype circuit is then transformed into a switched capacitor circuit following a method similar to that indicated in Fig. 9. An example of the complete procedure is outlined in Fig. 21 which

leads to a second order bandpass filter. In Fig. 21a a normalized lowpass filter (ω_{co} = rad/sec) is shown which is transformed using the lowpass to bandpass transformation into the circuit shown in 21b. An all-integrator representation of the circuit is given in 21c and the switched capacitor implementation follows in 21d. The values of the capacitor ratios in Fig. 21d are found from Eqs. 1, 24, and Fig. 21c.

$$\frac{C_T}{C_c} = \left(\frac{\omega_o}{f_c}\right)\left(\frac{1}{Q}\right) \tag{26a}$$

$$\frac{C_c}{C_u} = \left(\frac{R_S}{R_T}\right)\left(\frac{f_c}{\omega_o}\right) Q \tag{26b}$$

$$\frac{C_L}{C_u} = \left(\frac{R_T}{R_S}\right)\left(\frac{f_c}{\omega_o}\right)\frac{1}{Q} \ . \tag{26c}$$

since C = 1 F, it has not been included in the above expressions. It can be seen from these equations that if the Q is large then the capacitor ratios can also become very large. The size of the ratios can be minimized, however, by requiring that

$$\frac{R_T}{R_S} = Q. \tag{27}$$

This condition also matches the peak gain from the input to the internal node V_2' with the gain to the output (which is unity) and therefore maximizes the dynamic range. The effect of the sampled data time delays (especially the delay through the termination path) on the transfer function of a second order bandpass filter is the same as already discussed for a lowpass filter. Therefore the equations which describe the modification of the capacitor ratios (which retain the same Q and center frequency for the switched capacitor bandpass filter as the prototype LC filter) are the same as those given in Eq. 19 and 20. For this to be true, however, the R_T/R_S ratio must be set by the condition given Eq. 27 and the switches phased as shown in Fig. 7.

Even after minimizing the capacitor ratios, the ratios can be very large for high Q filters. It is possible, however, to decrease the size of the ratios by increasing the sensitivity of the filter. This is accomplished by using the switch phasing for the integrators which was described earlier that gives a full clock cycle of delay and thus yields an integrator which has an additional phase shift of $e^{-j\omega T_c/2}$ (see Eq. 8). This precisely defined amount of extra phase shift results in a pole movement which increases the Q of the filter (and also increases the sensitivity).

As in the case of the lowpass filter shown in Fig. 11, single op amp bandpass filters can be implemented which make use of the equivalence between a lossy integrator and an RC circuit. These single op amp structures are essentially switched capacitor versions of the infinite gain-multiple feedback bandpass circuits of active filter theory [13].

The implementation of higher order bandpass filters is a straightforward extension of the procedure outlined in Fig. 21. As in the case of the high order lowpass filters the modifications to the capacitor ratios which compensate for sampled data effects in the second order filters (Eqs. 19 and 20) are usually not necessary in the high order bandpass circuits.

E. Other Filter Organizations

The implementation of highpass and band reject filters can also be performed by use of the appropriate transformation on a lowpass LC circuit and then developing the switched capacitor realization by the use of the switched capacitor integrators.

Of course, as mentioned earlier there are many other possible switched capacitor filters that are based on active filter circuits that are consistent with the limitations of the MOS implementation.

There are also switched capacitor filter organizations which are not based on standard active filters [18,19,20]. One example is the filter which was shown in Fig. 2. Another is the N-path circuit which uses modulation techniques to translate a very narrow lowpass characteristic up to a center frequency which is controlled by the clock rate of the switches [20]. In this way extremely narrow bandpass and band elimination filters can be realized and in fact Q's in excess of 1000 are readily achievable.

CONCLUSIONS

Design considerations for MOS switched-capacitor filters have been described. The major advantage of this approach is that a broad range of monolithic MOS filters can be realized which are insensitive to component variations. MOS filters have been designed and tested, and the results confirm the theoretical predictions.

Commercial exploitation of the switched-capacitor filtering technique is proceeding at a rapid pace. The first areas for application of the technique has been in special-purpose frequency selective filters for telecommunications applications, and in telephone applications in particular. An example is the monolithic dual channel filter shown in Fig. 22. This device contains two fifth-order elliptic lowpass filters with 3.4 kHz cutoff frequencies, a 60 Hz high-pass filter, and all necessary anti-aliasing filtering on the chip itself. While the application of this

particular device is for anti-aliasing and reconstruction of the voice signal at the analog-digital interface in a PCM telephone switching or transmission system, the basic techniques are currently being applied to other telecommunication circuits.

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*Note: this has been submitted but not yet accepted. Will be removed from galleys if not accepted for conference.

TABLE I

LAND C VALUES FOR NORMALIZED LOWPASS FILTERS

$\left(R_T = 1\Omega \quad \omega_{co} = 1^{rad}/_{sec}\right)$

	Butterworth	Chebychev (.1 dB Passband Ripple)	Bessel
C	1.4142F	1.3911F	1.3617F
$\mathcal{L}$	.7071H	.8191H	.4539H

TABLE II

MEASURED PERFORMANCE PARAMETERS OF A SAMPLE OF SECOND-ORDER FILTERS

		Filter I	Filter II
Clock rate f_c		102.4 kHz	16 kHz
Calculated:	center frequency f_0	3.75 kHz	264 Hz
	selectivity Q	73.14	0.99
Measured:	center frequency mean	3.715 kHz	287 Hz
	center frequency standard derivation	13 Hz	1 Hz
	selectivity mean	71.2	0.97
	selectivity standard deviation	2.2	0.004
	output wideband noise (rms)	0.85 mV	160 μV

TABLE III

MEASURED PERFORMANCE PARAMETERS OF A FIFTH-ORDER

LOW-PASS LADDER FILTER

Ripple Bandwidth (f_c = 128 kHz)	3400 Hz
Total Passband Ripple	± 0.1 dB
Output THD (3 $volts_{p-p}$)	0.5%
Power Dissipation	30 mW
Chip area (Fifth order)	68x98 mils
Noise (300 - 3 kHz)	180 μV_{RMS}
Dynamic Range (1% THD)	80 dB

TABLE IV

MEASURED PERFORMANCE PARAMETERS OF A

THIRD-ORDER ELLIPTIC LOWPASS LADDER FILTER

Clock Frequency	128 kHz
Ripple Bandwidth	3400 Hz
Total Passband Ripple	0.1 dB
Minimum Stopband Rejection	30.4 dB
RMS Output Voltage (1% THD)	2.6 V
RMS Noise (300-3 kHz)	80 μV
Dynamic Range	90 dB
Power Dissipation	18 mW
Filter Die Area	4400 mil^2

Figure Captions

Fig. 1. A second order direct form discrete time filter.

Fig. 2. Analog sampled data realization of the filter shown in Fig. 1 using MOS switches, capacitors and operational amplifiers.

Fig. 3. a) A switched-capacitor which in many cases can simulate the function of a resistor. b) An MOS implementation of the circuit shown in part a).

Fig. 4. a) A single-pole R-C continuous low-pass filter. b) Single-pole low-pass filter utilizing a switched-capacitor resistor.

Fig. 5. a) A conventional differential R-C integrator and b) a switched-capacitor differential integrator.

Fig. 6. A switched-capacitor differential integrator showing the parasitic capacitances associated with the switches and capacitors.

Fig. 7. A two-integrator loop with proper switch phasing to minimize phase errors.

Fig. 8. A switched-capacitor integrator/summer.

Fig. 9. a) Two-pole singly terminated L-C ladder filter. b) Analog simulation of the LC ladder filter. c) Switched-capacitor realization of ladder simulator. d) Discrete time model for switched-capacitor circuit of (c).

Fig. 10. Magnitude response of example filter

Fig. 11. Switched-capacitor implementation of an infinite gain-multiple feedback lowpass filter.

Fig. 12. a) Frequency response and output noise spectrum of high-Q version of experimental filter of Fig. 11. The noise spectrum was taken with a bandwidth of 30 Hz and amplified by 30 dB.

Fig. 13. Frequency response and output noise spectrum of low-Q version of the filter of Fig. 12. The noise spectrum was taken with a bandwidth of 30 Hz and was amplified by 30 dB.

Fig. 14. a) Doubly terminated RLC fifth-order all-pole low-pass ladder filter.

Fig. 14. b) Switched-capacitor version of fifth-order all-pole low-pass filter.

Fig. 15. Die photo of experimental fifth-order all-pole low-pass switched-capacitor filter. Bottom edge of chip contains test devices.

Fig. 16. Frequency response of experimental low-pass fifth-order filter.

Fig. 17. a)An experimental RLC third-order elliptic low-pass filter, b)and its integrator simulation.

Fig. 18. Switched-capacitor version of third-order elliptic low-pass filter.

Fig. 19. Die photo of experimental elliptic third-order low-pass filter.

Fig. 20. Frequency response of third-order experimental elliptic low-pass filter.

Fig. 21. a) Normalized single-pole low-pass filter. b) Bandpass transformed low-pass filter. c) Integrator realization of bandpass filter. d) Switched-capacitor implementation of bandpass filter.

Fig. 22. A monolithic NMOS dual channel filter. This circuit utilizes NMOS depletion load technology with two layers of polysilicon. It contains a total of 20 operational amplifers and realizes a total of 17 poles. The die size is 150 by 166 mil. Photo courtesy of Intel Corporation.

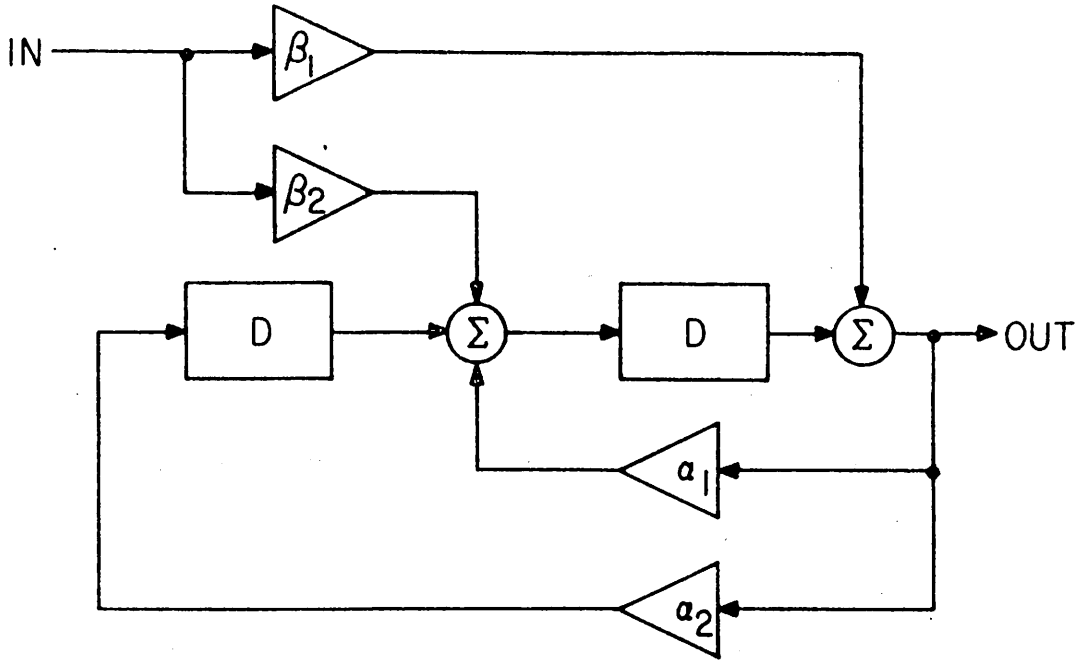


Fig. 1 Brodersen

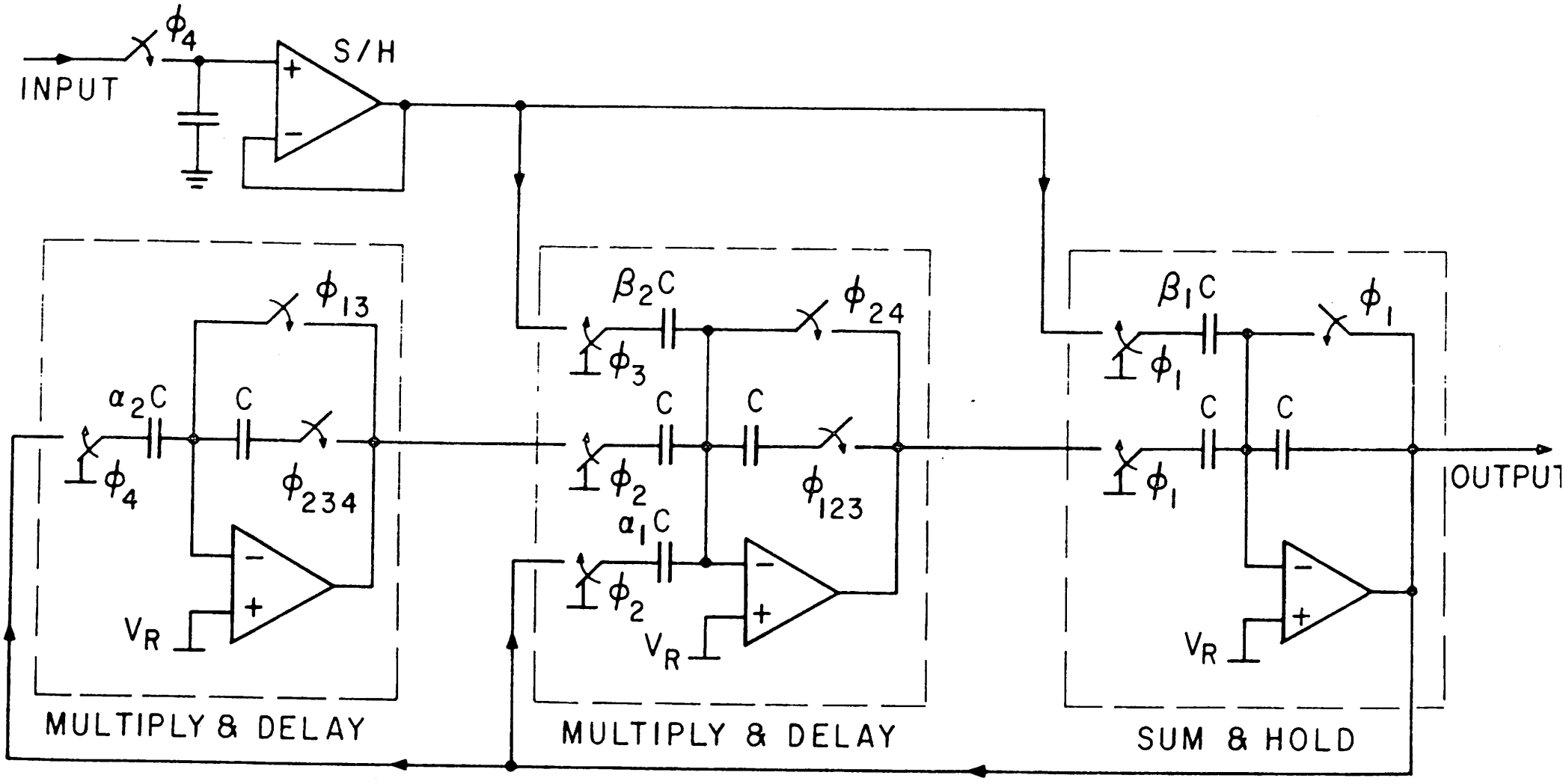


Fig. 2
Brodersen

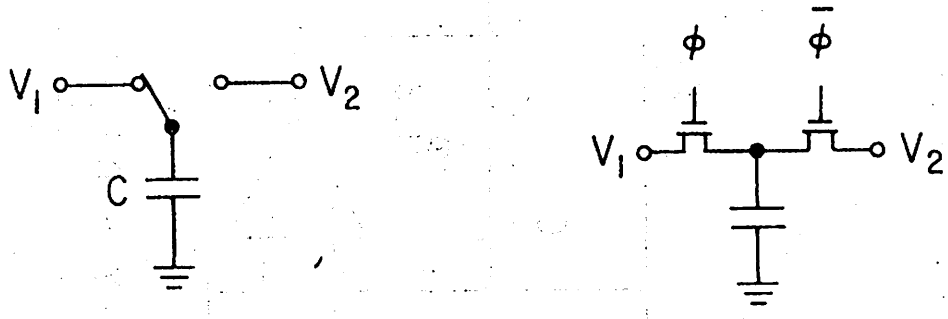
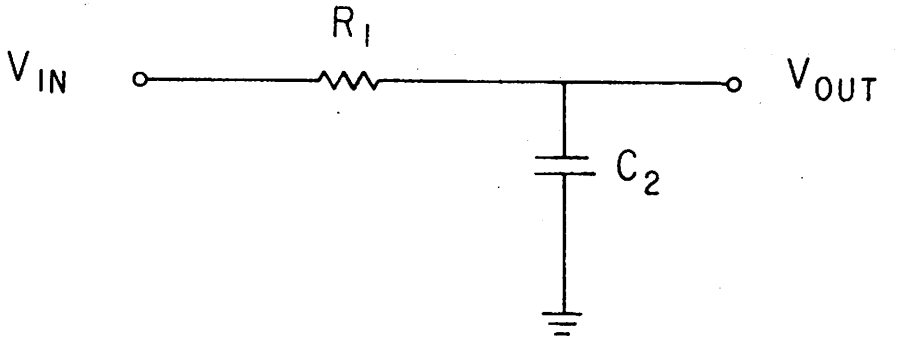
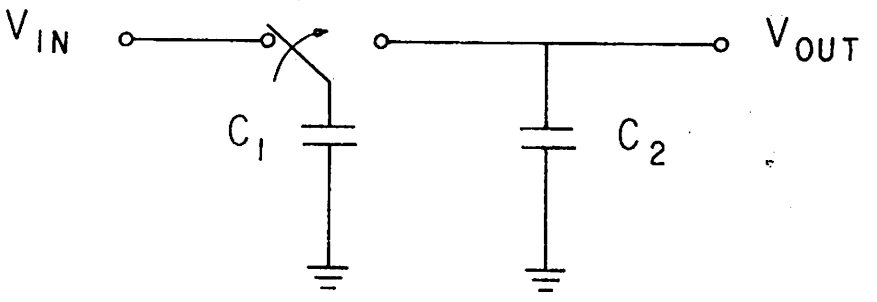


Fig. 3 Brodersen

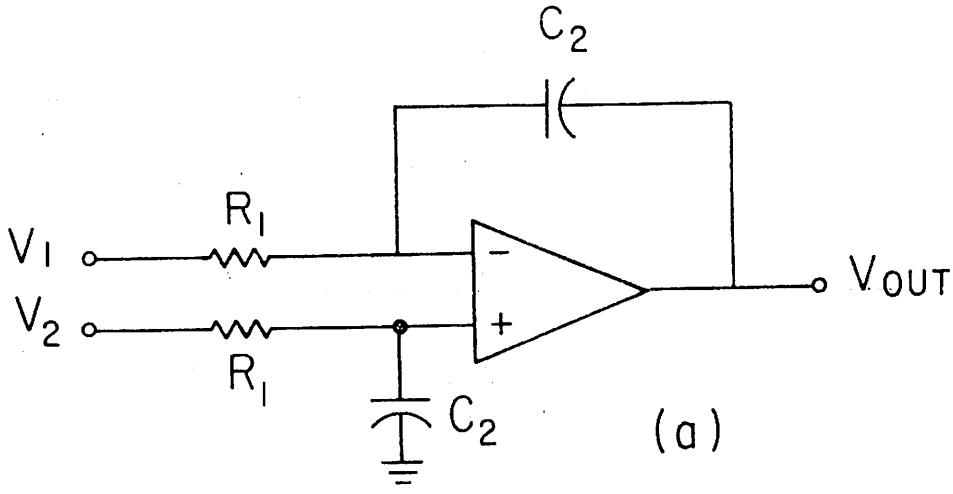


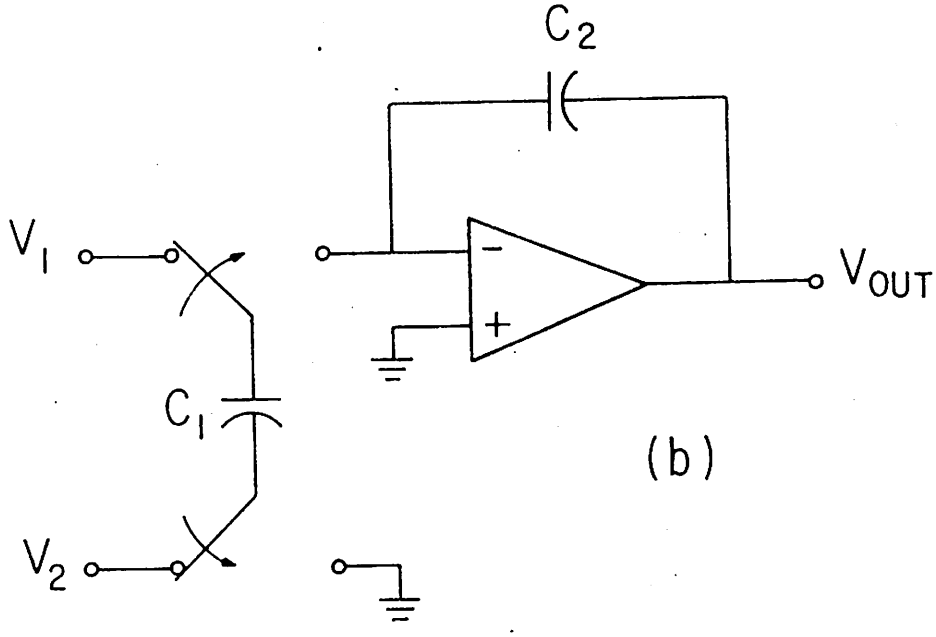
(a)

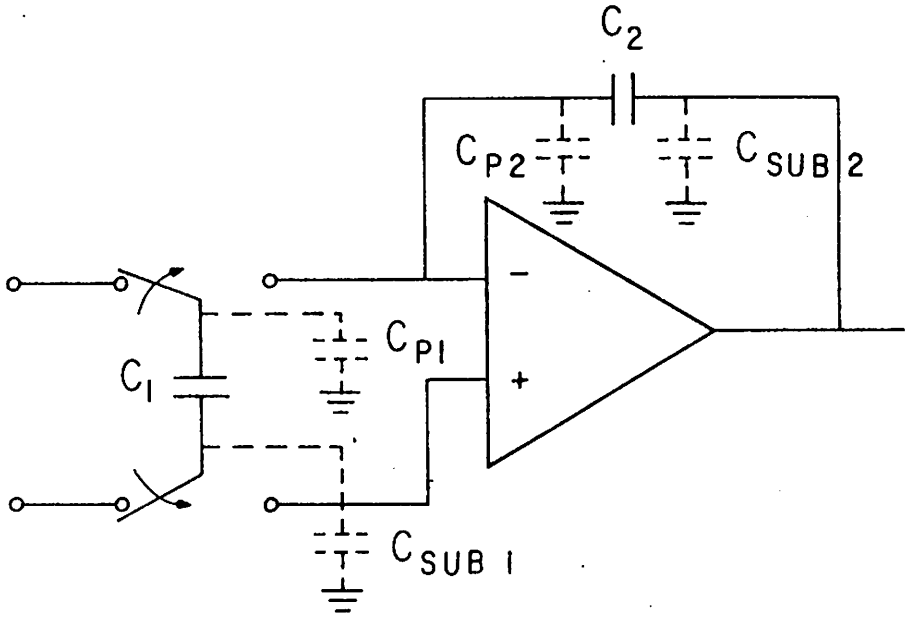


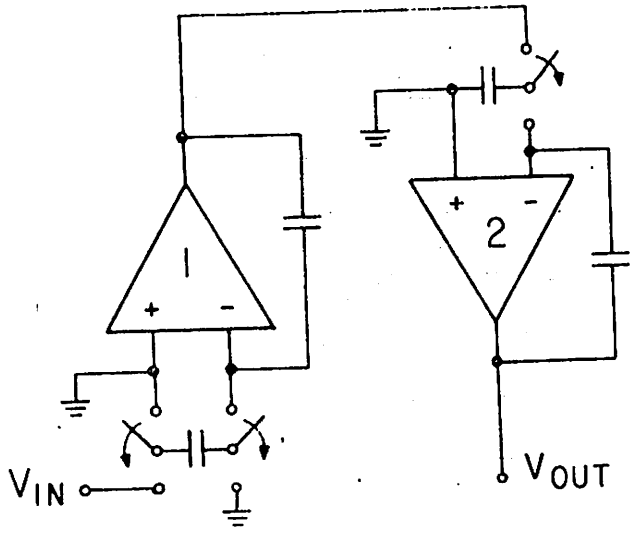
(b)

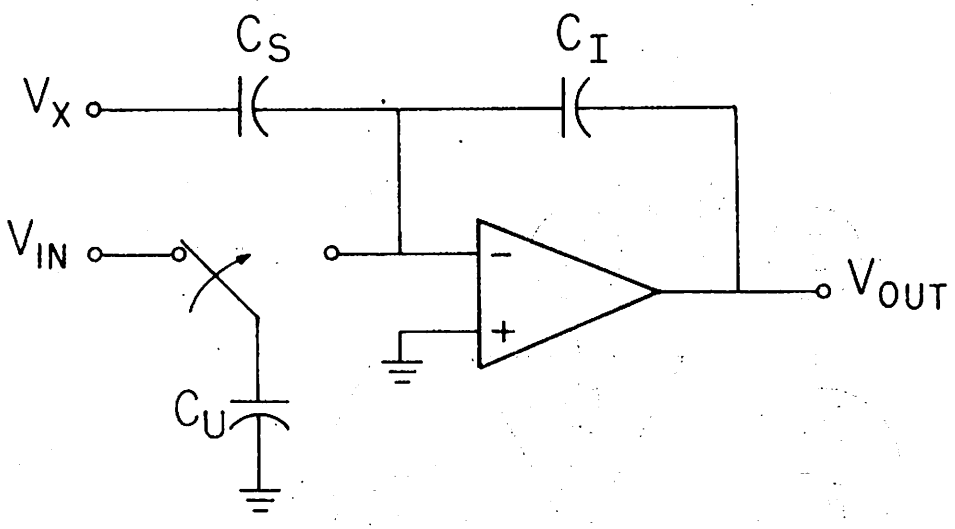
Fig. 4 - Exemplary

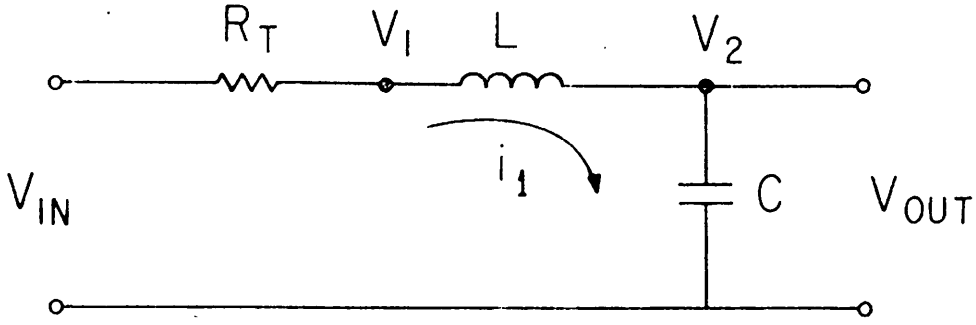

C2
R1
V1
V2
R1
C2
VOUT
(a)


C2
V1
VOUT
C1
(b)
V2

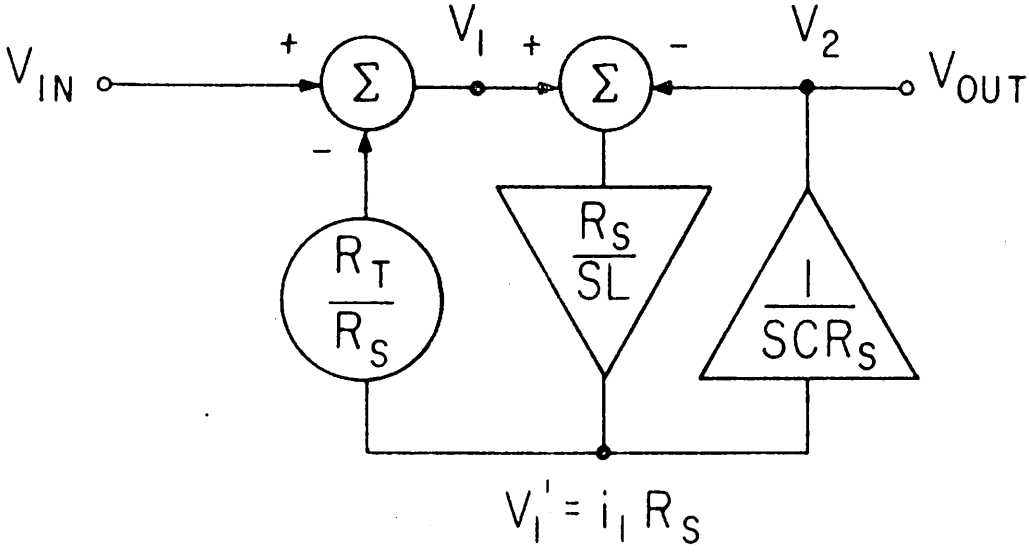

C2
CP2
CSUB 2
CP1
C1
CSUB 1
-
+


1
+
-
2
+
-
V_{IN}
V_{OUT}


C_S
C_I
V_X
V_{IN}
V_{OUT}
C_U
−
+

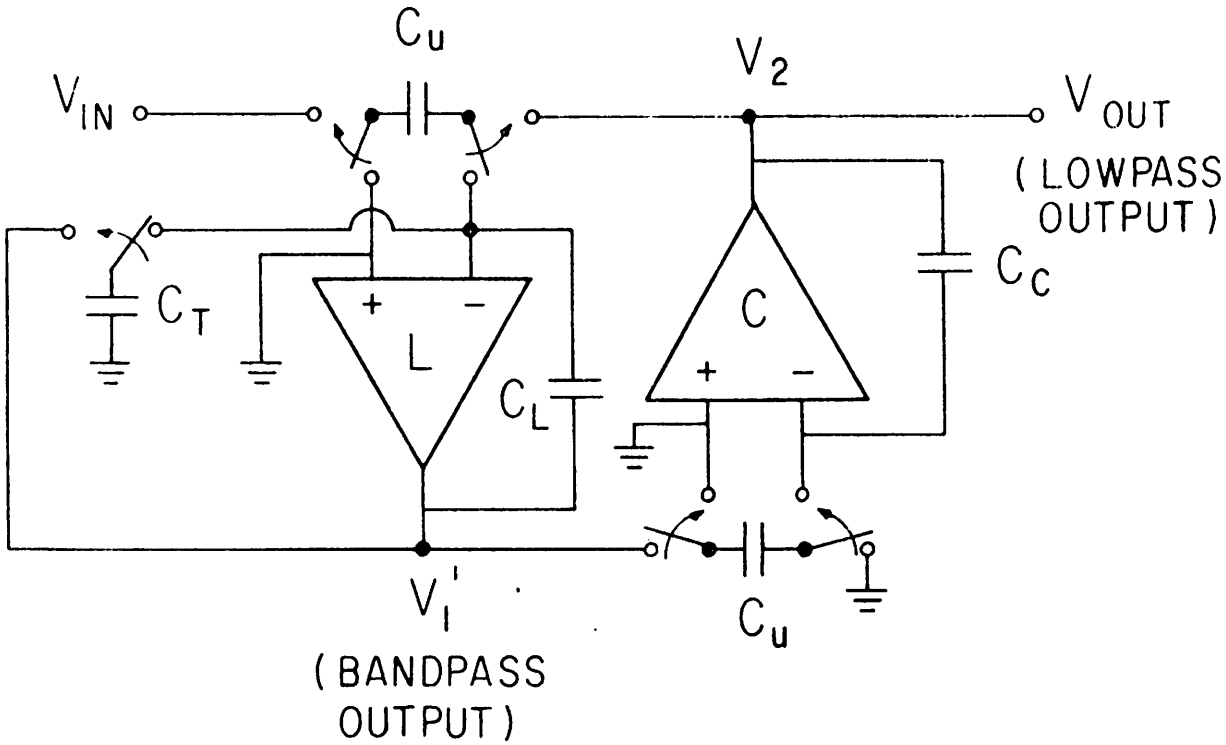


(a)

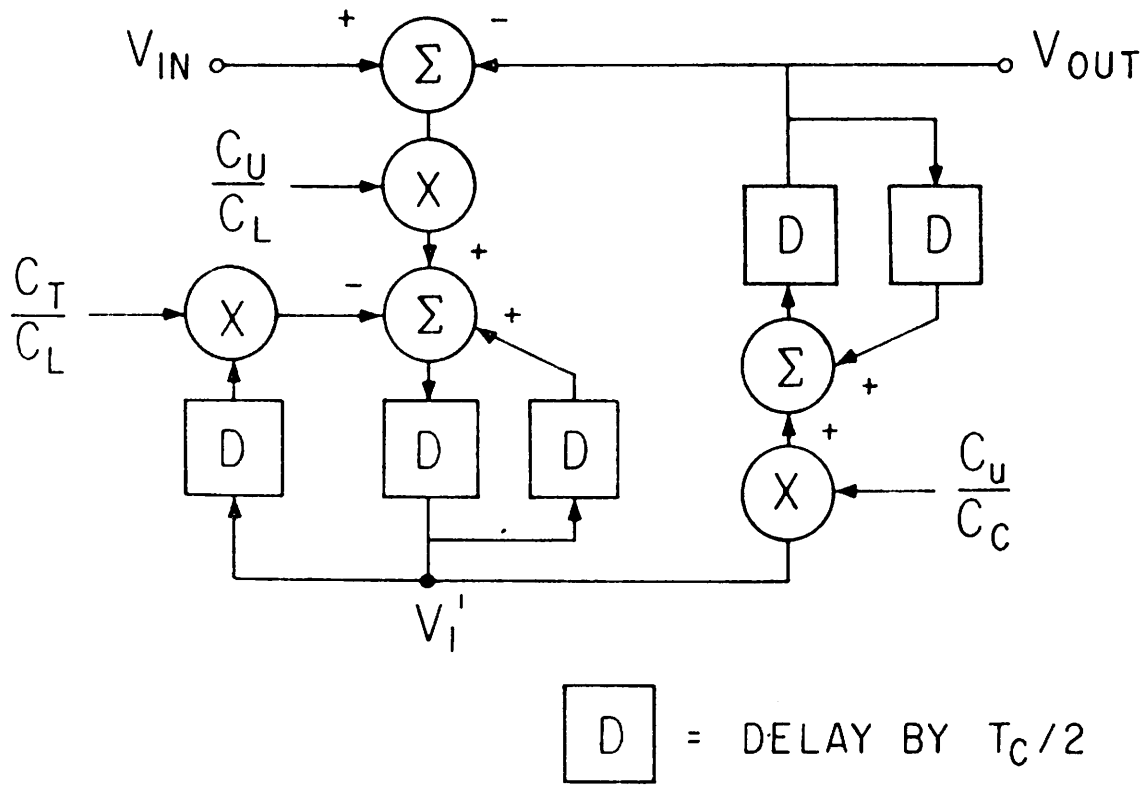


(b)

FIG. 1 - (Prior Art)


C_u
V_{IN}
V_2
V_{OUT}
(LOWPASS OUTPUT)
C_T
L
C_L
C
C_C
V_1'
C_u
(BANDPASS OUTPUT)

(c)


V_{IN}
V_{OUT}
$\frac{C_u}{C_L}$
$\frac{C_T}{C_L}$
X
Σ
D
$\frac{C_u}{C_C}$
V_1'
D = DELAY BY $T_C/2$

(d)

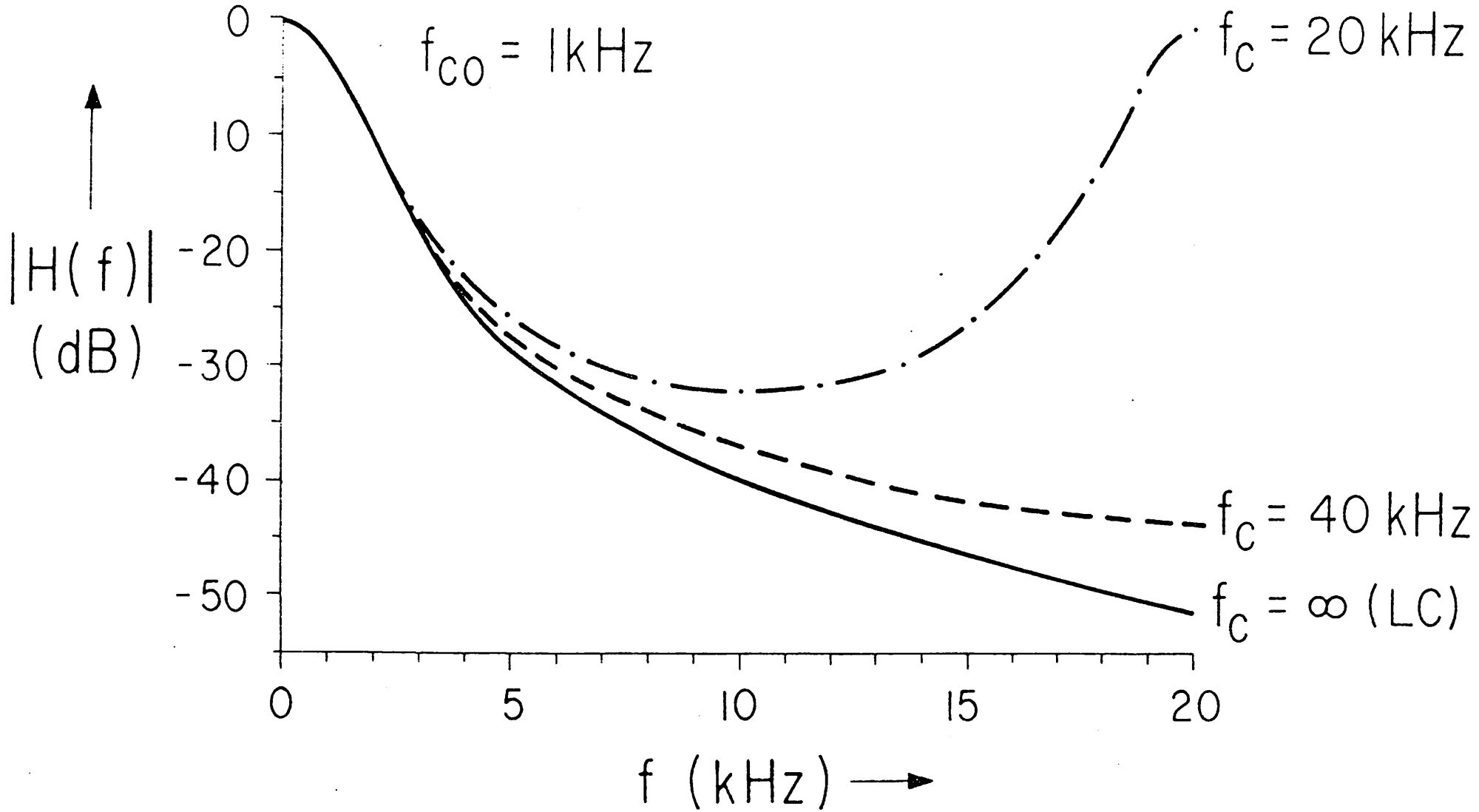

f_{co} = 1kHz
f_c = 20 kHz
f_c = 40 kHz
f_c = ∞ (LC)
|H(f)| (dB)
0
10
-20
-30
-40
-50
0
5
10
15
20
f (kHz)

Fig. 10

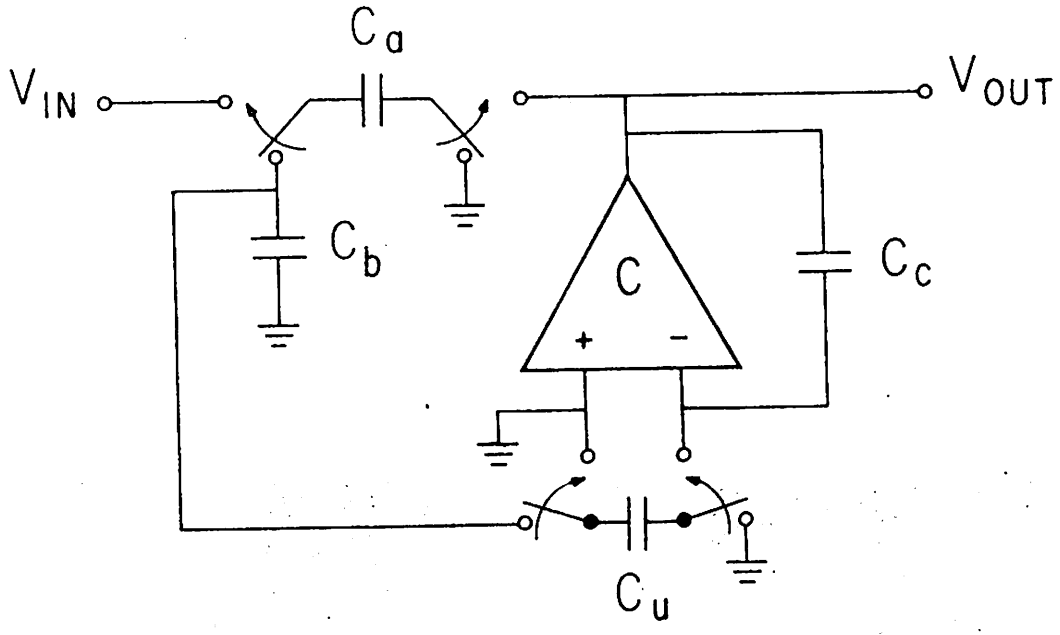


FIG. 11
BRODERSEN

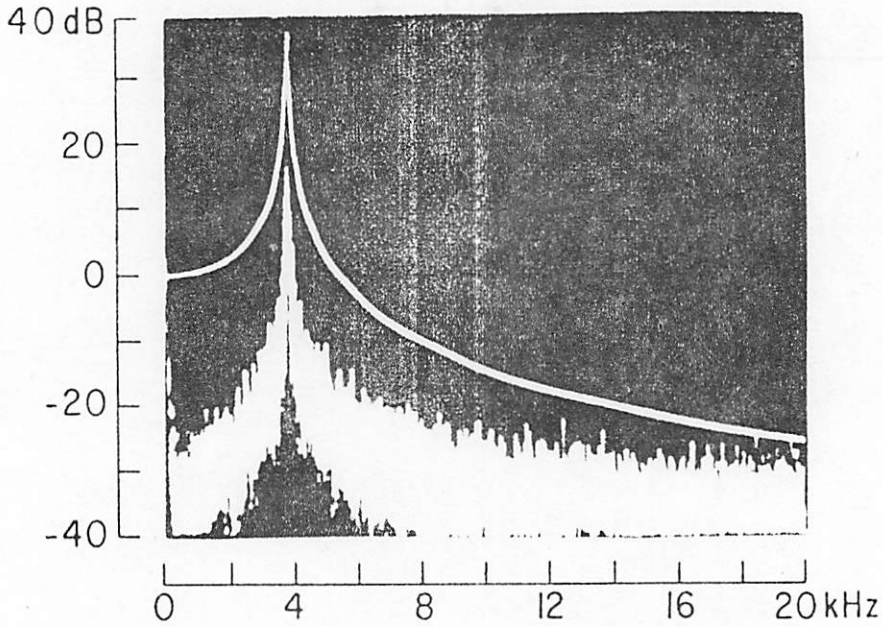


Fig. 12

Pedersen

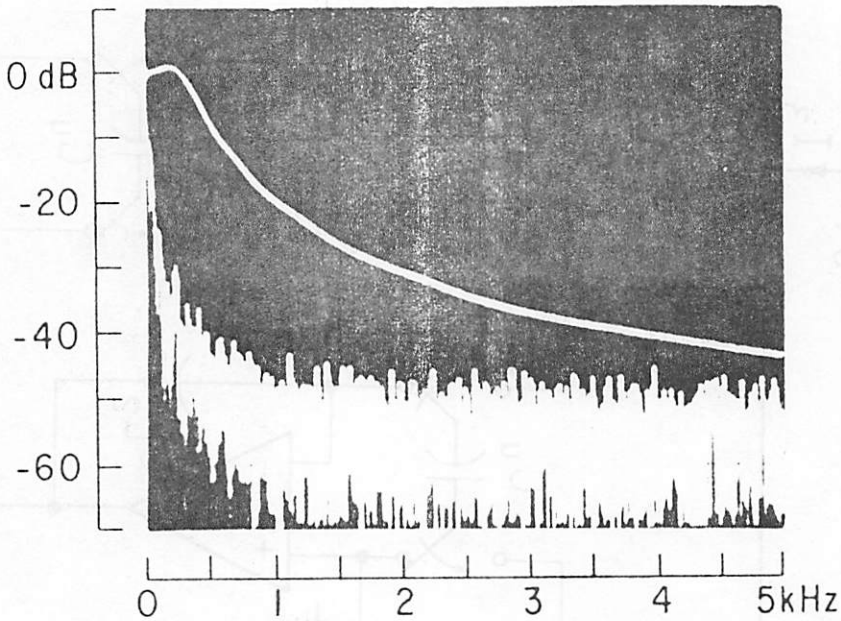
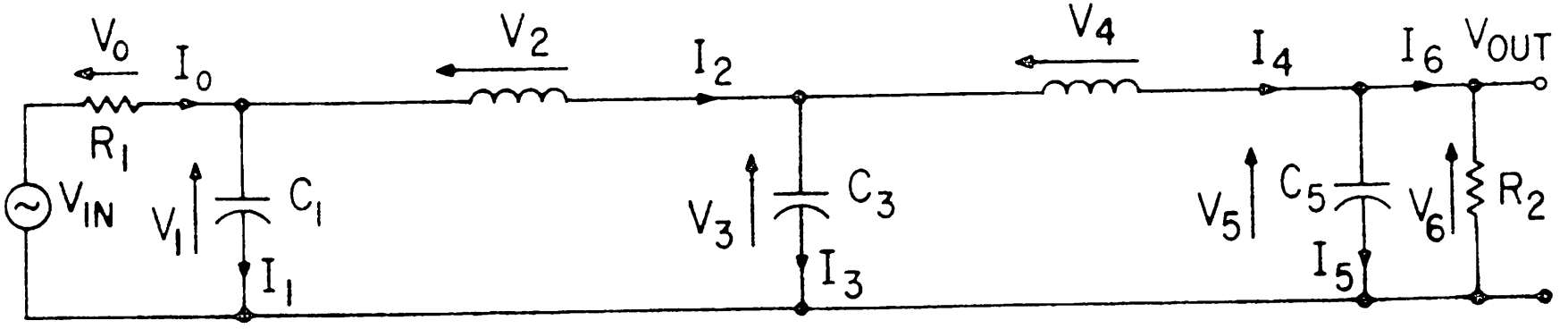
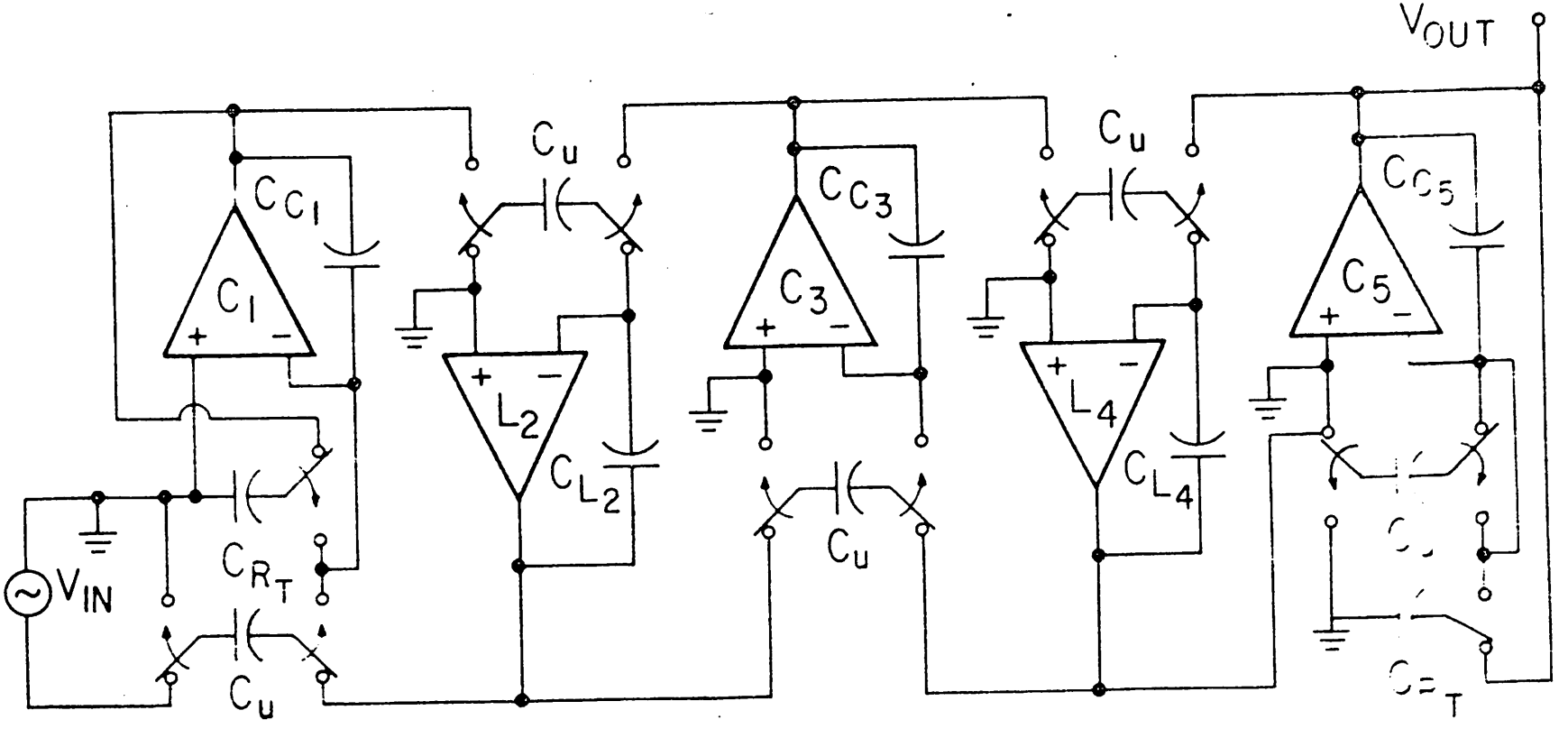
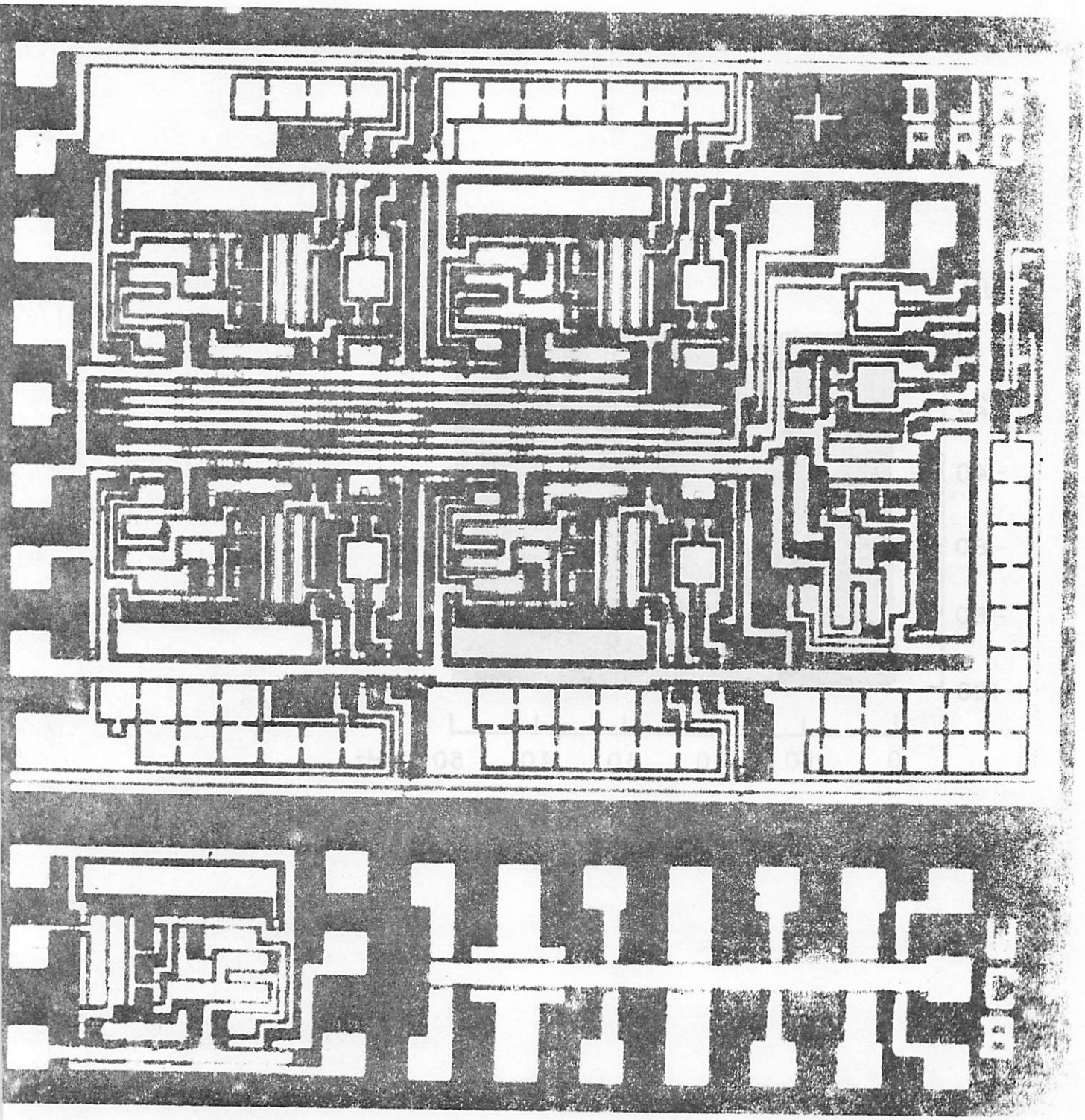
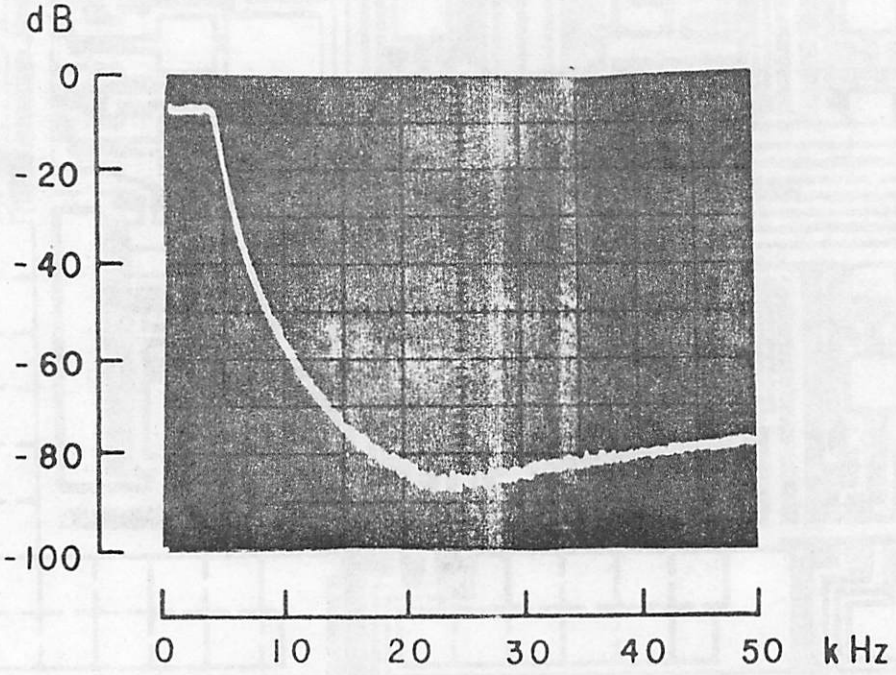


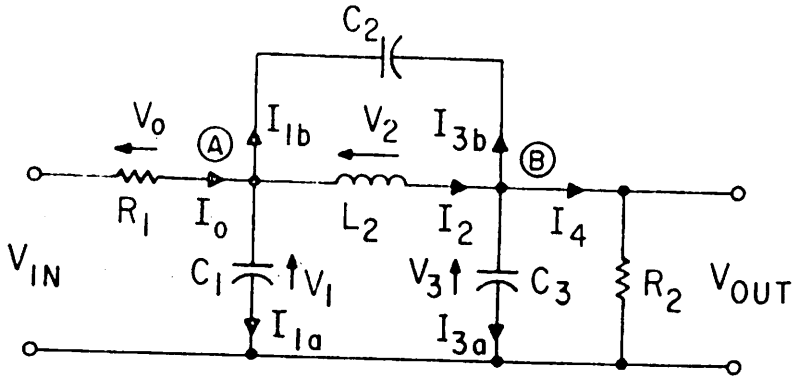
Fig 13


V0
I0
V2
I2
V4
I4
I6
VOUT
R1
VIN
V1
C1
I1
V3
C3
I3
V5
C5
I5
V6
R2

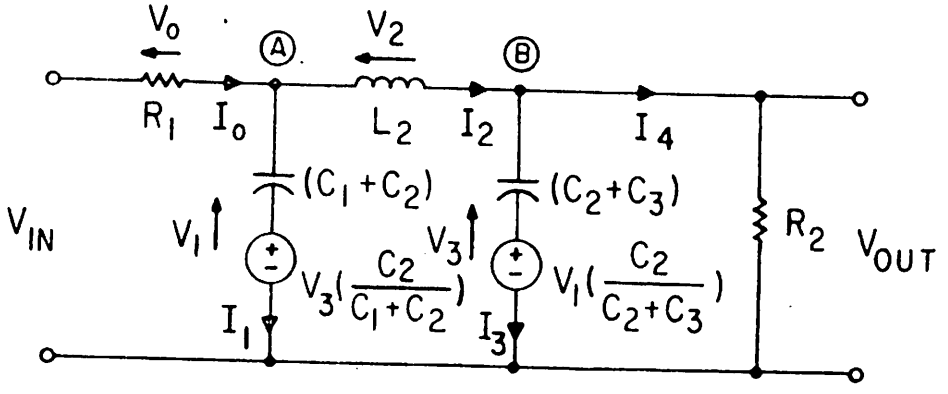

VOUT
Cu
CC1
C1
CC3
C3
CC5
C5
L2
CL2
L4
CL4
VIN
CRT
Cu
Cu
Cu
CET


+ DRB
PRO
DRB

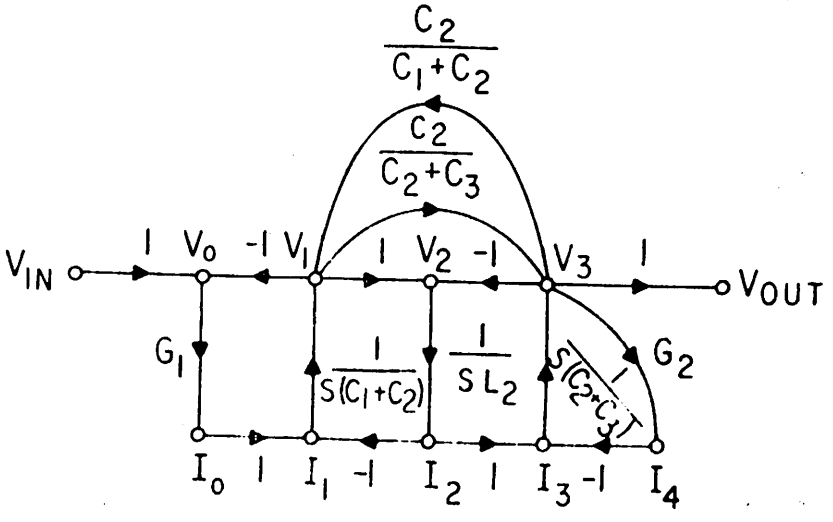

dB
0
-20
-40
-60
-80
-100
0
10
20
30
40
50
kHz


C2
V0
A
I1b
V2
I3b
B
R1
I0
L2
I2
I4
VIN
C1
V1
V3
C3
R2
VOUT
I1a
I3a

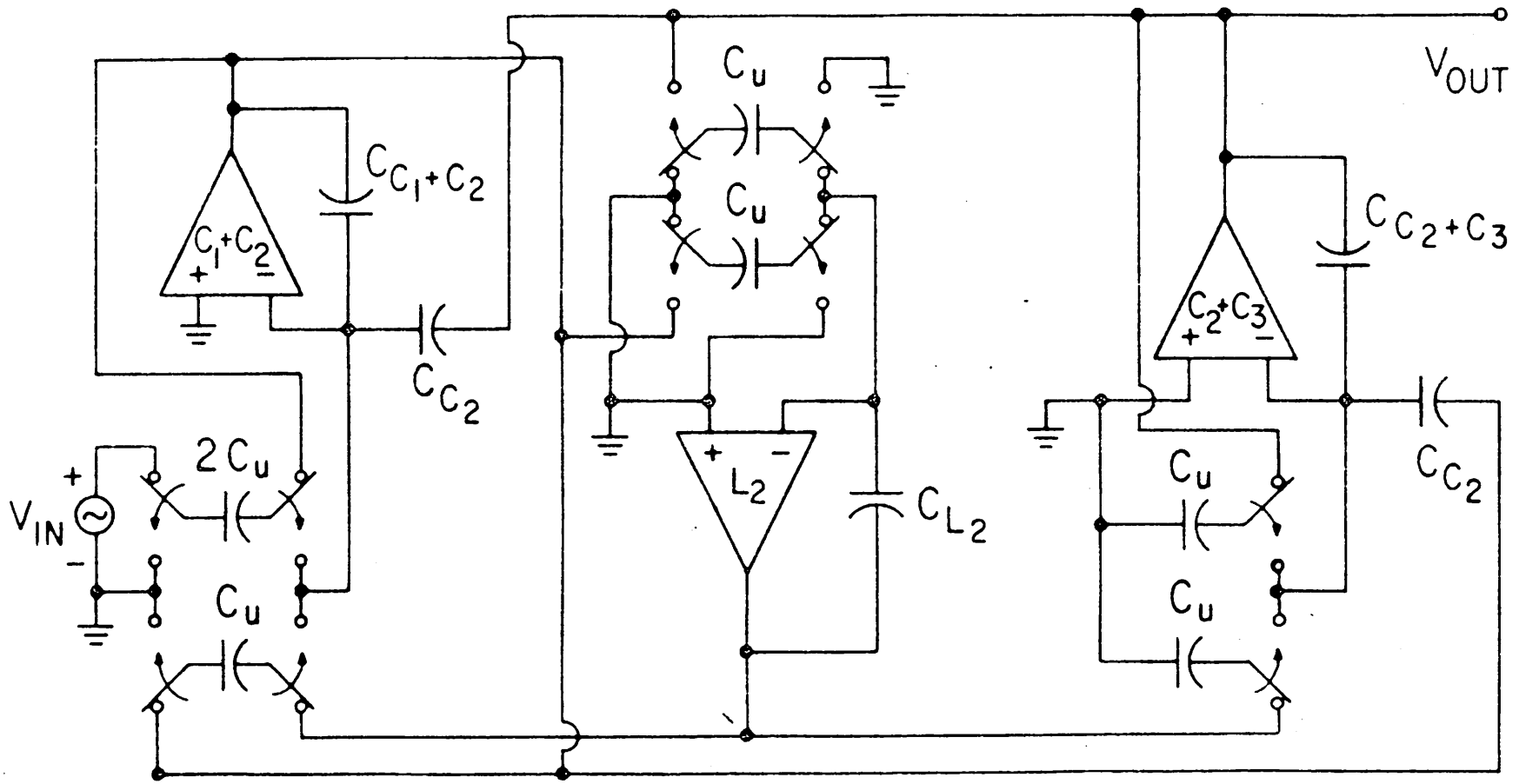
(a)


V0
A
V2
B
R1
I0
L2
I2
I4
(C1+C2)
(C2+C3)
VIN
V1
V3
R2
VOUT
V3(C2/(C1+C2))
V1(C2/(C2+C3))
I1
I3

(b)


C2/(C1+C2)
C2/(C2+C3)
VIN
1
V0
-1
V1
1
V2
-1
V3
1
VOUT
G1
1/(S(C1+C2))
1/(S L2)
1/(S(C2+C3))
G2
I0
1
I1
-1
I2
1
I3
-1
I4

(c)


V_{OUT}
C_u
C_u
$C_{C_1+C_2}$
C_1+C_2
$C_{C_2+C_3}$
C_2+C_3
C_{C_2}
C_{C_2}
$2C_u$
V_{IN}
L_2
C_{L_2}
C_u
C_u
C_u

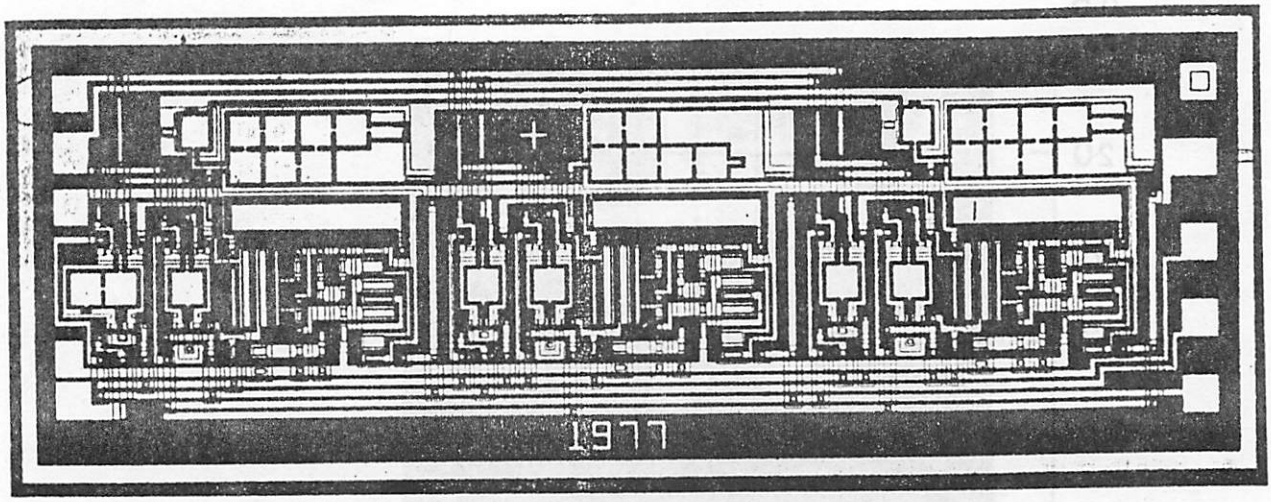


FIG. 19

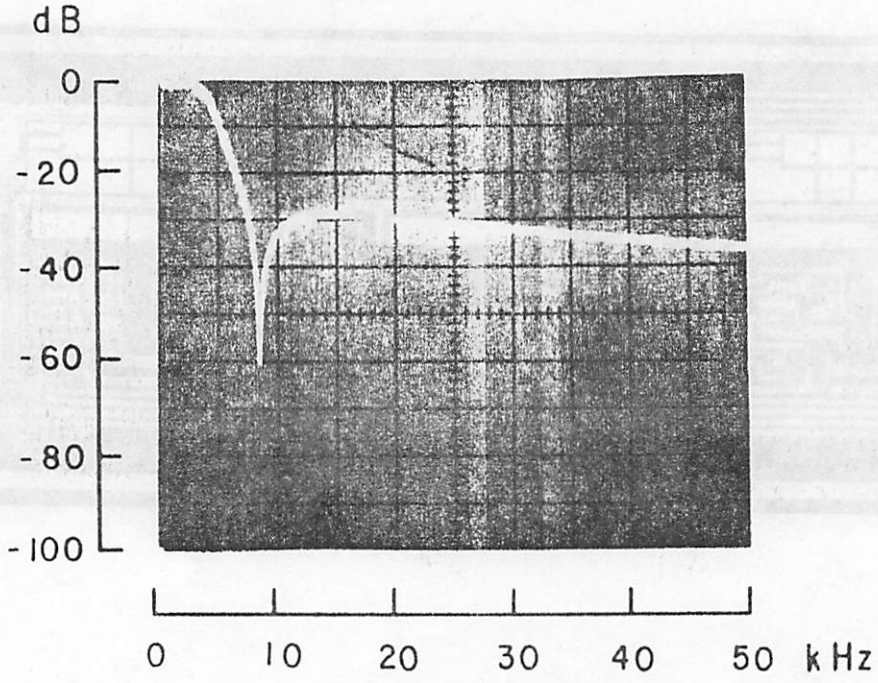
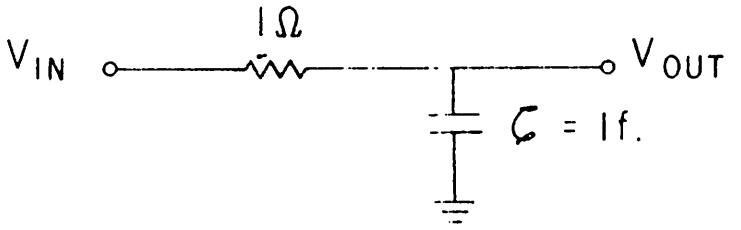
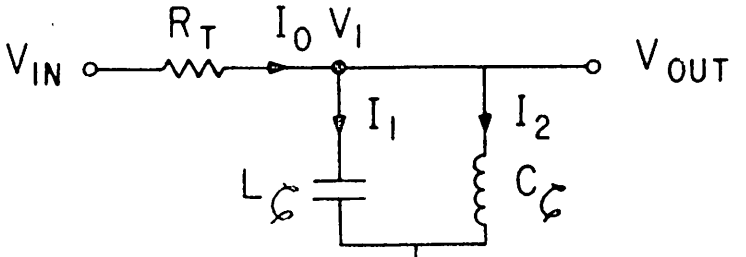


Fig. 20 Brodersen



(a)



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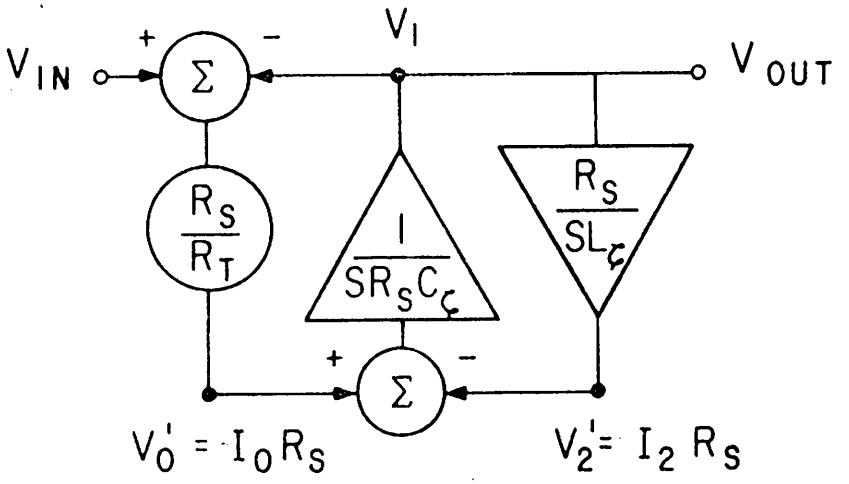
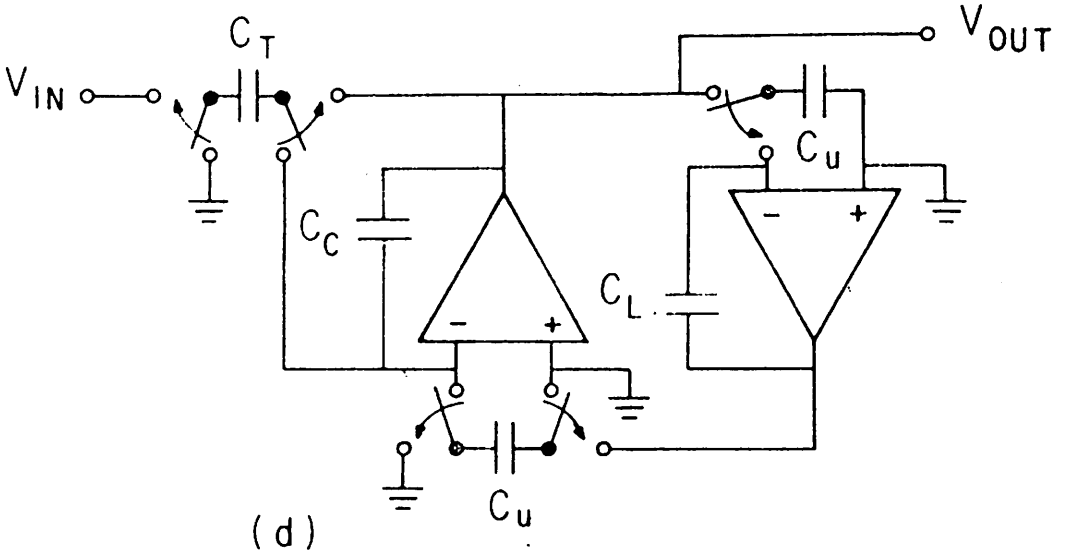


(c)



(d)

BRODERSEN - FIG. 2

Fig. 22. Not available at this time.