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MOS SWITCHED CAPACITOR LADDER FILTERS

by

David James Allstot

Memorandum No. UCB/ERL M79/30

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ABSTRACT

Switched capacitor techniques have been investigated for realizing precision high-order, frequency-selective filters using standard MOS technology. New techniques have been developed for designing recursive switched capacitor singly- and doubly-terminated active ladder filters which simulate low-sensitivity passive RLC ladder networks.

Three fully-integrated experimental NMOS prototypes have been designed and fabricated. The first circuit implemented a fifth-order Chebyshev lowpass response with 0.1 dB passband ripple and an 83 dB dynamic range. The second design was a third-order Elliptic lowpass filter which verified a new and efficient method of including complex transmission zeros. This filter achieved a 90 dB dynamic range with a power dissipation of 13 mW. The third design was an electrically-programmable second-order switched capacitor section with lowpass, bandpass, and bandreject outputs. This filter demonstrated a new technique for programming a filter response using weighted capacitor arrays.

In the switched capacitor technique, MOS capacitor ratios and sampling frequency are used as the precision elements. MOS operational amplifiers with moderate performance specifications are used to implement the switched capacitor integrators.

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DEDICATION

My wife, Vickie, meticulously drew most of the thesis figures and was a great help in assembling the final draft. Without her love, understanding and encouragement, none of this work would have been possible.

I dedicate this thesis to her for the many sacrifices she has made.

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Chapter 1
INTRODUCTION

Precision high-order filters are widely used in various types of electronic equipment such as telecommunications and other voice-band systems [1]. Monolithic implementation of these low frequency filters requires the realization of long time constants in small silicon area, and the realization of transfer functions that are insensitive to parameter variations. In addition, it is desirable to obtain a very precise response without external trimming operations. Conventional active filters implemented with thin-film or hybrid technologies do not meet these requirements, and therefore are not suitable for many applications.

Recently, these objectives have been realized in a monolithic implementation using a compatible Bipolar/JFET technology [2]. Although excellent results have been obtained, this approach requires a relatively large chip area for low frequency applications, and the required bipolar process is not directly compatible with dense digital logic which is needed for many LSI system applications.

Another promising monolithic filtering approach uses charge transfer devices (CTD's) to implement sampled-data transversal filters [3]. In the past, this approach had two main disadvantages: (1) The large insertion loss (which was typically 20 dB) limited the available dynamic range [4], and (2) the relatively low sampling rates complicated the design of the continuous-time anti-alias prefilter [5]. If higher clock frequencies were used relative to the passband frequencies in order to reduce the prefilter requirements, more CTD stages were required which further reduced the dynamic range and increased the silicon area requirements. Recently, these problems have been solved by using a double split-electrode CCD structure operating at 32 kHz with a 128 kHz sampled-data prefilter [44]. This approach appears to be very promising for future applications.

In the 1960's and early 1970's, filtering by using switches and capacitors was investigated theoretically [6]-[8]. At that time, a suitable integrated circuit technology did not exist which could efficiently realize these filters. Recent work using analog sampled-data techniques has demonstrated the viability of MOS technology for implementing second-order filters. The classical direct-form second-order digital filter section [9]-[10] has been implemented in an equivalent integrated circuit form using an MOS sampled-data approach [11]. This approach (as well as the direct-form digital prototype) has a relatively high sensitivity of the transfer function to component variation with the additional disadvantage that the sensitivity increases as the ratio of the sampling rate to passband frequencies increases. Hence, there is a tradeoff between the sensitivity properties of the direct-form sampled-data filter, and the requirements for the continuous-time anti-aliasing prefilter.

In digital filter implementations, these problems were solved by using a modified second-order structure [12]. Recently, MOS equivalents of these filters, as well as biquad second-order sections, have been realized with excellent results using switched capacitors to simulate resistors in sampled-data switched capacitor integrator configurations [13]-[15]. A major advantage of this approach is that the sensitivity of the response of these filters decreases with increasing clock frequency, in contrast to the direct-form implementations. Unfortunately, high-order filters realized by cascading these second-order sections can be too sensitive to component variations to meet high-precision filtering requirements.

It is well known from modern filter theory that for high-order filters, a passive doubly-terminated RLC ladder achieves very low sensitivity to component variations in the passband response, and in fact, has zero sensitivity when the power transfer is maximized between source and load [16]-[17]. This low sensitivity is maintained by using "leapfrog" or "active ladder synthesis" to simulate RLC ladder networks with active filter building blocks [18]-[20]. In order to obtain minimum

sensitivity high-order filters, a similar approach to the leapfrog design was taken in this thesis which makes use of new switched capacitor techniques. The precision elements in these filters are monolithic MOS capacitors whose ratios determine the frequency response. The inherent temperature stability ($< 25 \text{ ppm}/^\circ\text{C}$) and high matching accuracy (0.1%) of MOS capacitor ratios [21]-[23] make it possible to implement monolithic high-order filters with extremely precise frequency characteristics [24]-[25].

The approach to synthesis taken in this dissertation will be to configure the switched capacitor circuits to simulate the low-sensitivity continuous-time RLC ladder circuits, so that the design tables that are available for these filters can be used [26]-[27]. It will be shown that it is possible to minimize most of the discrete-time effects (particularly phase shifts due to time delays) which will allow design using classical continuous-time theory directly. However, one discrete-time characteristic which must be considered is the necessity of providing a continuous-time anti-aliasing prefilter preceding the switched capacitor filter. The low sensitivity properties of the ladder filters are actually improved with increased sampling frequency, and thus, the anti-aliasing prefilter requirements are greatly reduced (compared to the CTD and direct-form approaches) by operating the switched capacitor filters at clock frequencies which are many times greater than the passband frequencies.

In Chapter 2, the sensitivity properties of doubly-terminated RLC ladder filters are presented. The signal flowgraph synthesis procedure is reviewed, and various filter types are synthesized using switched capacitor integrators as the basic building blocks. Several new singly- and doubly-terminated highpass structures are presented.

In Chapter 3, the practical design aspects for MOS integrated circuit implementations of switched capacitor ladder filters are given along with a description of the

effects of finite sampling frequency. A new LDI integrator is presented which is insensitive to parasitic capacitance.

In Chapter 4, noise and dynamic range considerations for MOS active ladder filters are presented. Also presented are new scaling techniques which are more general than the scaling procedures which are used in the RLC prototypes.

In Chapter 5, experimental results obtained from two different integrated NMOS switched capacitor ladder filters are described. The first design is a Chebyshev fifth-order all-pole lowpass filter, and the second design implements a third-order elliptic lowpass response including a very efficient realization of transmission zeros. These filters achieve very precise responses with wide dynamic range while requiring small chip area, low power dissipation, and relatively low performance operational amplifiers. An NMOS depletion-load operational amplifier design is also summarized.

Chapter 6 presents the synthesis procedures and design considerations for an MOS switched capacitor programmable filter for applications in formant speech synthesis. New experimental results are presented for a programmable second-order switched capacitor section.

A summary of this research project is presented in Chapter 7.

In Appendix 1, the NMOS depletion-load metal-gate process which was used to fabricate the experimental test circuits is given.

Appendix 2 contains the measured NMOS device parameters which are used to estimate the performance parameters for the NMOS operational amplifier.

In Appendix 3, models are presented which are useful for simulating switched capacitor filters using a digital network analysis program called DINAP [28]. It is shown that most of the important analog effects can be modelled in the digital domain. This approach has the advantage of accurately predicting discrete-time

effects in contrast to a continuous-time simulation approach.

SWITCHED CAPACITOR LADDER FILTER SYNTHESIS

This chapter begins with a review of the sensitivity properties of doubly-terminated RLC ladder filters followed by a review of the switched capacitor resistor concept, and the development of the switched capacitor integrator. In the final sections, the signal flowgraph synthesis procedure is developed and used to design both singly- and doubly-terminated lowpass, bandpass, and highpass switched capacitor ladder filters.

2.1. Sensitivity of the Doubly-Terminated RLC Ladder Filter

For high-order filters, a passive doubly-terminated RLC ladder achieves very low sensitivity in the passband response, and in fact, has zero sensitivity when the power transfer is maximized between source and load [16]-[17]. Fig. 2.1(a) shows a doubly-terminated RLC fifth-order lowpass ladder filter. In Fig. 2.1(b), the power delivered to the output is plotted for variation of a component value. When all elements achieve their nominal values, the power delivered to the output is maximum. However, if a reactive element value is either increased or decreased, the power delivered to the output decreases. Since the slope, $\frac{\partial P_{out}}{\partial X}$, is nominally zero, small perturbations in the element values will cause very small changes in the passband response of the filter [27].

The low passband sensitivity is illustrated by considering a specific example. The fifth-order RLC lowpass ladder filter of Fig. 2.1(a) has been frequency scaled to realize a Chebyshev response with 0.1 dB nominal passband ripple and a nominal cutoff frequency of 3.4 kHz as shown in Fig. 2.2(a) [29]. The transfer function of this particular filter is most sensitive to the variation of C_3 . Fig. 2.2(b) shows the simulated results for the passband deviation from the nominal design for $\pm 1\%$

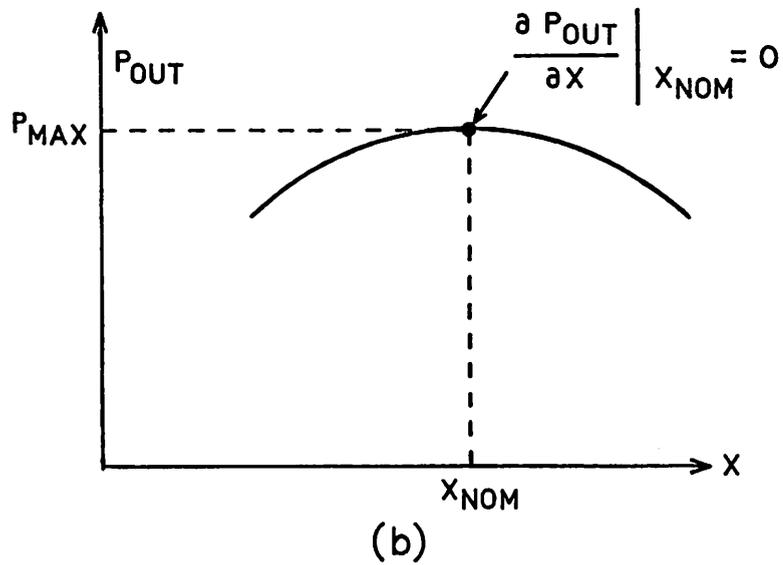
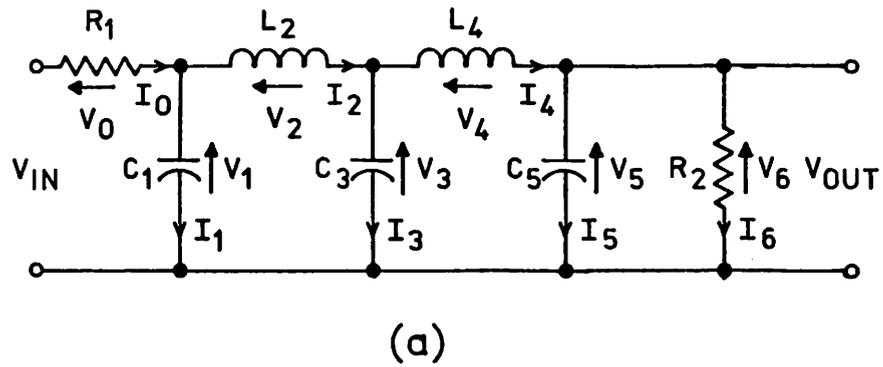


Fig. 2.1. (a) An RLC doubly-terminated fifth-order lowpass ladder filter; (b) the output power for variation of a reactive element value.

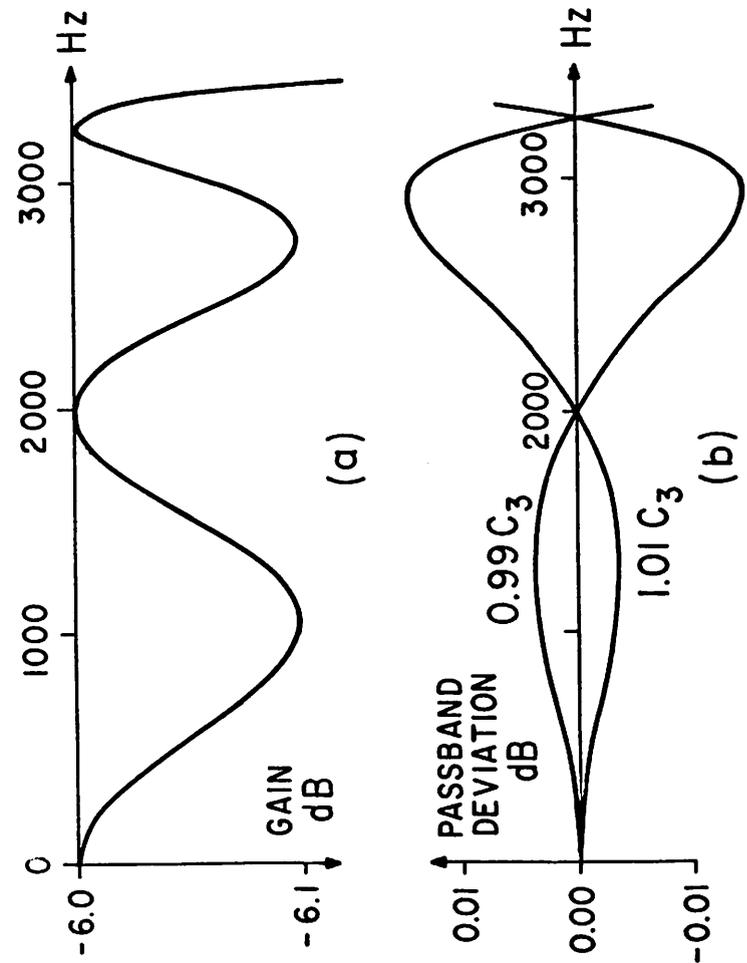


Fig. 2.2. (a) A nominal fifth-order Chebyshev lowpass response with 0.1 dB passband ripple and a 3.4 kHz cutoff frequency; (b) simulated passband deviation for $\pm 1\%$ variations in C_3 .

variations in C_3 [30]. At those frequencies where the filter response of Fig. 2.2(a) has a gain of -6 dB, indicating maximum power transfer, the passband deviation, and hence the sensitivity of Fig. 2.2(b) is zero. The sensitivity across the entire passband is very low since a variation of $\pm 1\%$ in C_3 results in a maximum passband deviation of only ± 0.015 dB. The passband sensitivity of this doubly-terminated RLC ladder is about 10 times lower than a similar singly-terminated RLC ladder [31], and about 20 times lower than a similar cascade RLC realization [32]. Hence, for implementing high-order, high precision monolithic filters, it is desirable to use an equivalent form of the doubly-terminated RLC structure in order to obtain the desired low sensitivity. Unfortunately, the network of Fig. 2.1(a) contains both inductors and resistors which are difficult to implement in MOS technology. The next sections will describe an approach for converting an RLC filter into an equivalent MOS switched capacitor ladder which is well-suited for integration, and which retains nearly ideal sensitivity properties.

2.2. The MOS Switched Capacitor Resistor Concept

Large resistance values are difficult to accurately realize in integrated circuits due to the lack of high resistivity regions. One possible solution to this problem is to use lightly doped polysilicon resistors. Unfortunately, the absolute values of these resistors vary widely with temperature and processing variations, and their voltage coefficient is rather large [33]. Ion implanted and diffused resistors have similar disadvantages as shown in Table I [34]. (These resistors are often adequate for the required continuous-time anti-aliasing prefilter).

Recently, these disadvantages have been overcome by using a capacitor which is switched between voltage sources to simulate a resistor as shown in Fig. 2.3(b) [13]-[15]. At time t , ϕ_1 turns on MOSFET M_A , and C_u is charged to

| COMPONENT TYPE | MATCHING ACCURACY | TEMPERATURE COEFFICIENT | VOLTAGE COEFFICIENT |
|------------------------|--|-------------------------|---------------------|
| MOS CAPACITOR | 0.06 % ($L=10\mu\text{m}$) | +25 ppm/°C | -20 ppm/VOLT |
| DIFFUSED RESISTOR | 2% (5 μm) 0.23% (50 μm) | +1500 ppm/°C | -200 ppm/VOLT |
| POLYSILICON RESISTOR | 2% (5 μm) | 1500 ppm/°C | — |
| ION IMPLANTED RESISTOR | 2% (5 μm) 0.15% (50 μm) | 400 ppm/°C | -800 ppm/VOLT |

Table 1. Properties of monolithic resistors and capacitors.

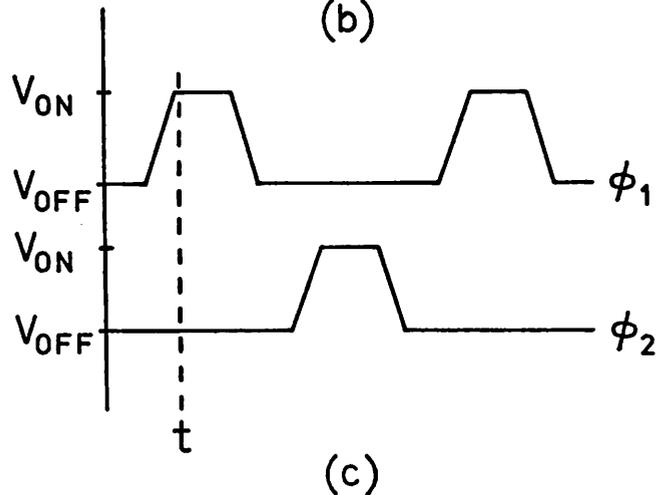
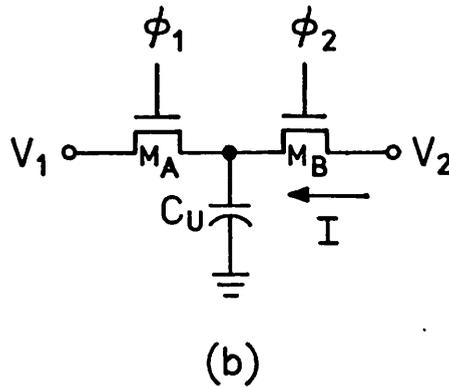
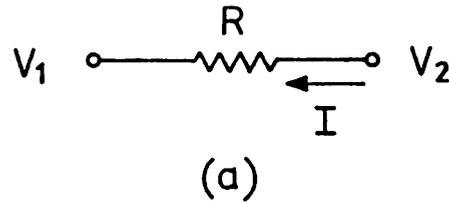


Fig. 2.3. (a) A conventional resistor, and (b) a switched capacitor "resistor"; (c) the two-phase non-overlapping clock signals used to switch the MOSFET's.

$$Q_1 = C_u V_1. \quad (2.1)$$

At time $(t + T_c)$, ϕ_2 turns on MOSFET M_B (M_A is now turned off), and C_u is charged to

$$Q_2 = C_u V_2. \quad (2.2)$$

The current which flows onto C_u is given by

$$I = \frac{\Delta Q}{\Delta t} = \frac{C_u(V_2 - V_1)}{T_c}. \quad (2.3)$$

The current flowing through the resistor of Fig. 2.3(a) during the same period of time is

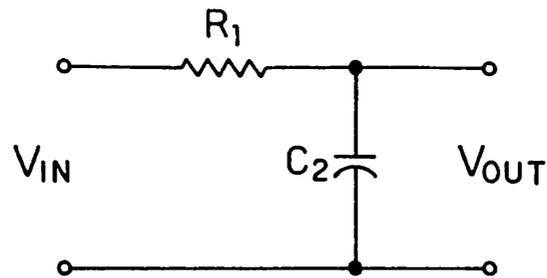
$$I = \frac{V_2 - V_1}{R}. \quad (2.4)$$

Therefore, an equivalent switched capacitor resistance, R_{EQ} , can be defined by equating Eqns. (2.3) and (2.4):

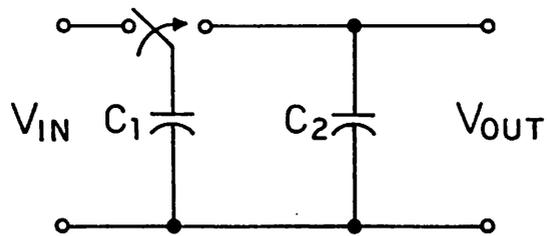
$$R_{EQ} = \frac{T_c}{C_u} = \frac{1}{f_c C_u} \quad (2.5)$$

where C_u is the switched capacitor value, and f_c is the sampling frequency. This equivalence is valid for sampling rates which are much greater than the signal frequencies of interest. If this condition is not met, more exact sampled-data analysis is required [35]-[36].

C_u may be switched between two points which are not voltage sources. For example, in Fig. 2.4, the resistor, R_1 , is replaced by the switched capacitor, C_1 , to form a sampled-data passive lowpass filter. Sampled-data techniques are required to analyze these circuits, and in certain cases, other factors such as clock duty cycles



(a)



(b)

Fig. 2.4. (a) A single-pole RC lowpass filter, and (b) a passive single-pole switched capacitor lowpass filter.

must be considered which can greatly complicate the design [37]. In this dissertation, it will be assumed that the switching occurs between voltage sources (including virtual grounds) as in the example of the switched capacitor integrator which will be described in the next section.

2.3. The MOS Switched Capacitor Integrator

Conventional filtering approaches used to implement audio and other low frequency filters would require RC integrators, as in Fig. 2.5(a), with long time constants. If the time constants were realized as RC products, large amounts of chip area would be required. Another disadvantage of this approach is that in order to insure reproducibility, the *absolute* values of both R and C must be tightly controlled, which is extremely difficult for typical temperature and processing variations as indicated previously in Table I.

These disadvantages are overcome by using the switched capacitor circuit shown in Fig. 2.5(b) which, when the ratio of the sampling frequency to the maximum passband frequency is large, closely approximates the conventional integrator of Fig. 2.5(a) [13]-[14]. The switched capacitor integrator is operated with two-phase nonoverlapping clocks as shown earlier in Fig. 2.3(c). During the sample phase, ϕ_1 , the switches are thrown to the left, and the difference between voltages V_1 and V_2 is sampled and stored on C_u . During the integration phase, ϕ_2 , the switches are thrown to the right, and the difference voltage is scaled and stored on C_l . By switching C_u at a high clock rate, f_c , relative to the passband frequencies, an equivalent resistance is obtained of value

$$R_{EQ} = \frac{1}{f_c C_u}, \quad (2.6)$$

resulting in an integrator gain constant of

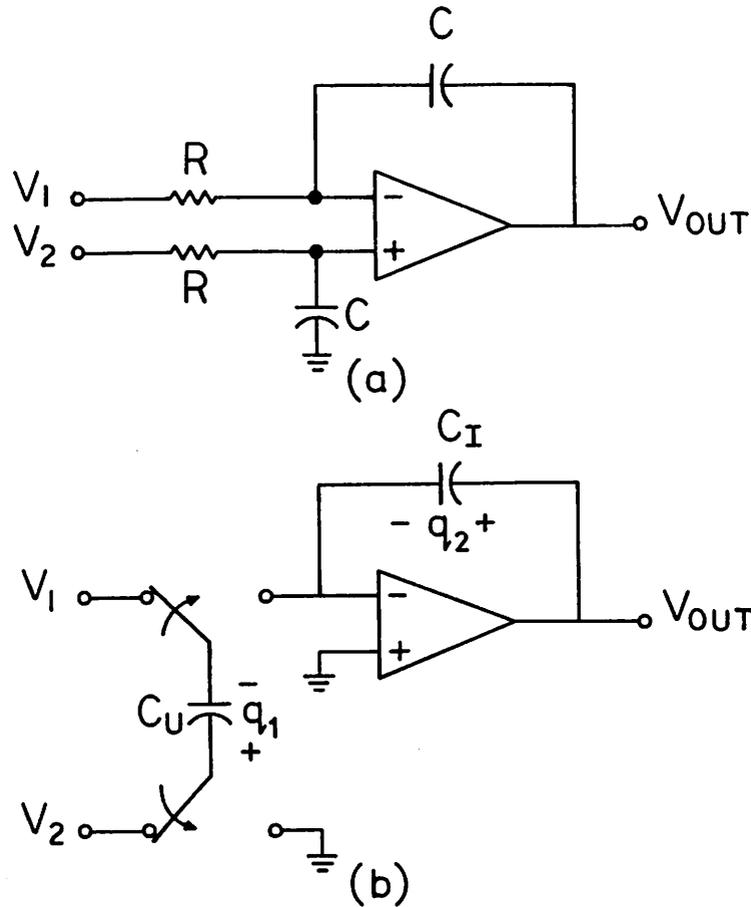


Fig. 2.5. (a) A conventional RC differential integrator, and (b) a switched capacitor integrator with differential inputs.

$$\omega_o = \frac{1}{R_{EQ}C} = f_c \left[\frac{C_u}{C_1} \right]. \quad (2.7)$$

Fig. 2.5(b) can also be analyzed directly using a z-domain analysis [35], and the conservation of charge principle. Assuming ideal components, the charge stored on the capacitors at time $(t-T_c)$ is

$$q_1(t-T_c) = C_u [V_2(t-T_c) - V_1(t-T_c)] \quad (2.8a)$$

and

$$q_2(t-T_c) = C_1 V_{out}(t-T_c). \quad (2.8b)$$

At time t when the switches are thrown to the right, the op amp discharges C_u onto C_1 , and the system charge is now

$$q_2(t) = C_1 V_{out}(t) \quad (2.9a)$$

and

$$q_1(t) = 0. \quad (2.9b)$$

Eqns. (2.8) and (2.9) can be equated to yield

$$V_{out}(t) = \left[\frac{C_u}{C_1} \right] [V_2(t-T_c) - V_1(t-T_c)] + V_{out}(t-T_c). \quad (2.10)$$

In the z-domain, this expression becomes

$$V_{out}(z) = \left[\frac{C_u}{C_1} \right] [z^{-1}V_2(z) - z^{-1}V_1(z)] + z^{-1}V_{out}(z) \quad (2.11)$$

which is solved for $V_{out}(z)$:

$$V_{out}(z) = \left[\frac{C_u}{C_l} \right] \frac{z^{-1} [V_2(z) - V_1(z)]}{1 - z^{-1}} \quad (2.12)$$

Assuming $f \ll f_c$, and replacing $z = e^{sT_c}$ in Eqn. (2.12) by its Taylor series expansion,

$$V_{out}(s) \approx \frac{f_c \left[\frac{C_u}{C_l} \right]}{s} [V_2(s) - V_1(s)], \quad (2.13)$$

with $s' = e^{sT_c}$. Hence, the term "integrator" is used to represent this building block, and the gain constant derived from Eqn. (2.13) agrees with the intuitive result of Eqn. (2.7). The differential integration property is also evident from Eqn. (2.12).

The switched capacitor realizes very large resistance values in very small chip areas. For example, from Eqn. (2.5), it is seen that by switching a 1 pF capacitor at 100 kHz, an equivalent resistance of 10 M Ω is realized in an area of only about 5 mil² for C_u plus a few additional mil² for the two minimum geometry MOSFET switch transistors. (It is also interesting to note from Eqn. (2.5) that as the resistance value increases, the area required for its switched capacitor implementation actually *decreases*). If this equivalent resistor is used in conjunction with $C_l = 10C_u$, a gain constant of 10⁴ radians/sec is obtained. Hence, by using the switched capacitor to simulate a resistance, long time constants are achieved in small silicon area, and since the integrator gain constant of Eqn. (2.7) is now determined by a *ratio* of monolithic capacitors, high matching accuracy and excellent temperature stability are obtained in monolithic MOS implementations.

The next section will review flowgraph synthesis procedures for MOS switched capacitor active ladder networks.

2.4. Flowgraph Synthesis Techniques

One technique for designing an active ladder network from a passive RLC prototype is to transform the differential equations describing the network into a pictorial representation called a flow diagram [20],[25],[38],[39]. The flow diagram contains nodes for both voltage and current variables in the circuit. The branches which interconnect these nodes represent the transfer functions of each circuit element. There are several valid flow diagram representations of a given network which require different circuit realizations. The objective is to manipulate the signal flow diagram in order to obtain a representation that can be realized with switched capacitor integrators. To construct a flow diagram, one simply creates a node for each voltage and current in the circuit, and then interconnects them with the proper impedance or admittance using Kirchhoff's nodal and loop equations. Once the proper flow diagram is constructed, the transformation into a switched capacitor circuit easily follows.

A passive doubly-terminated RLC lowpass ladder which will be used as the prototype for the switched capacitor implementation was shown in Fig. 2.1(a). In this figure, the voltages and currents of each circuit element are labelled. A complete set of loop and node equations which involves only integrations is shown below:

$$I_0 = \frac{V_0}{R_1} \quad (2.14a)$$

$$V_0 = V_{in} - V_1 \quad (2.14b)$$

$$I_1 = I_0 - I_2 \quad (2.14c)$$

$$V_1 = \frac{I_1}{sC_1} \quad (2.14d)$$

$$I_2 = \frac{V_2}{sL_2} \tag{2.14e}$$

$$V_2 = V_1 - V_3 \tag{2.14f}$$

$$I_3 = I_2 - I_4 \tag{2.14g}$$

$$V_3 = \frac{I_3}{sC_3} \tag{2.14h}$$

$$I_4 = \frac{V_4}{sL_4} \tag{2.14i}$$

$$V_4 = V_3 - V_5 \tag{2.14j}$$

$$I_5 = I_4 - I_6 \tag{2.14k}$$

$$V_5 = \frac{I_5}{sC_5} \tag{2.14l}$$

$$I_6 = \frac{V_6}{R_2} \tag{2.14m}$$

$$V_6 = V_5 \tag{2.14n}$$

$$V_{out} = V_6 \tag{2.14o}$$

The flow diagram which represents these equations is shown in Fig. 2.6(a). Each node (voltage or current) is defined by the signal paths flowing into it. The factor written next to each arrow, denoting the direction of the path, is the gain for that path. Multiple inputs into a single node are considered summed. Since the actual implementation will use voltage integrators, it is necessary to transform current nodes to voltage nodes. This is performed by multiplying all current nodes by a scaling resistance R so that the currents, I_i , are now represented as the voltages

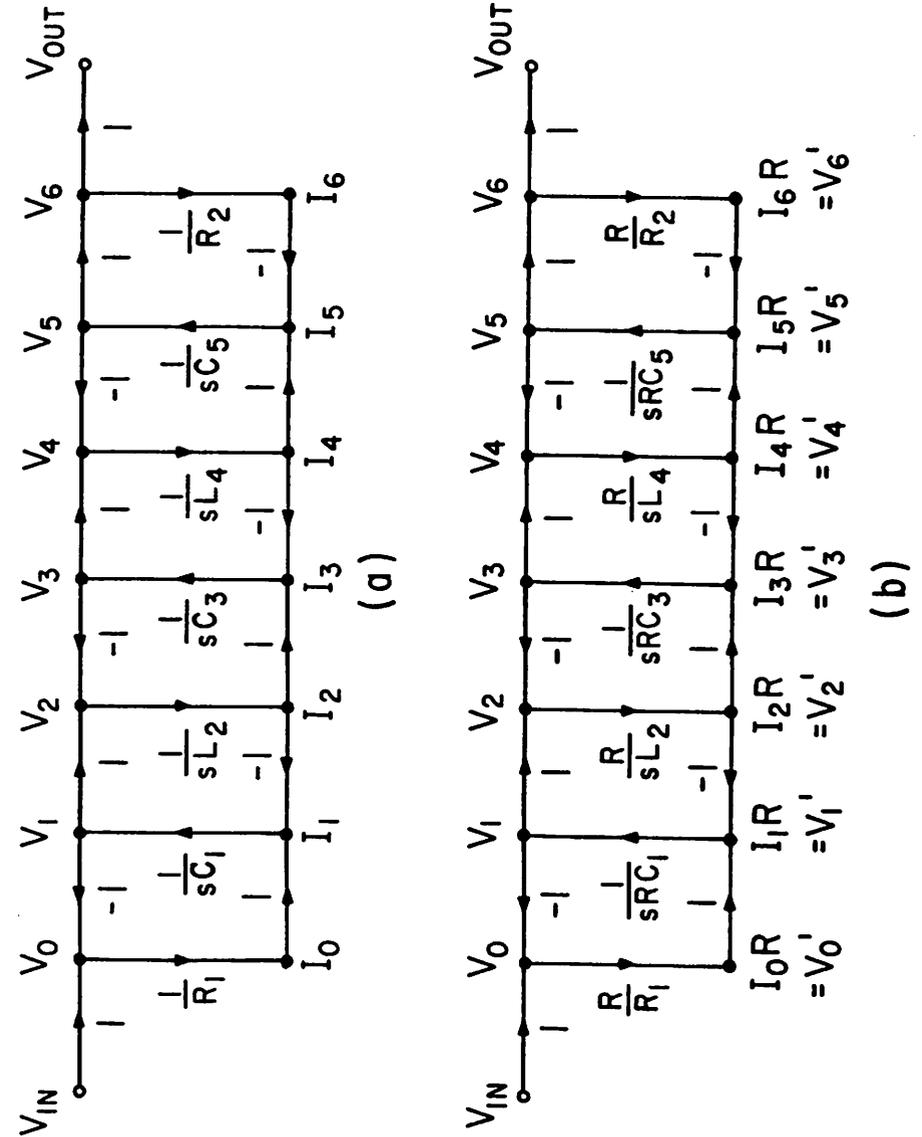


Fig. 2.6. (a) A signal flow diagram for the circuit of Fig. 2.1(a), and (b) an equivalent type-I all-voltage form.

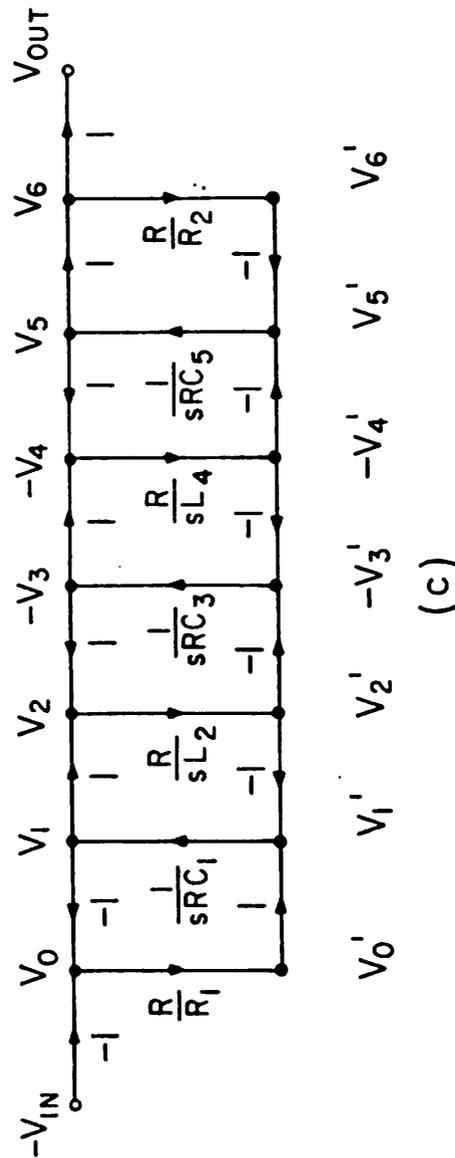


Fig. 2.6. (c) A type-II signal flow diagram for the circuit of Fig. 2.1(a).

$V_i = Ri$. In order to maintain the proper relationships between the voltage and current nodes, the branch gain factors are also scaled by R in Fig. 2.6(b).

There are tradeoffs between capacitor area and filter dynamic range which are involved in choosing a value for R which will be described in greater detail in Chapter 4 [40]-[41]. In general, a value of $R=1$ ohm is a good compromise, and for this case, the integrator time constants are the original L or C values. After scaling, the terminations, R_1 and R_2 , are realized by connecting the outputs of the terminating integrators to their inputs multiplied by the gains $\frac{R}{R_1}$ and $\frac{R}{R_2}$. The optimum choice for the values of R_1 and R_2 depends on many factors, and they will be assumed to equal 1 ohm in the designs in this chapter.

The flow diagram in Fig. 2.6(b) is one of many that describe the ladder of Fig. 2.1(a). For example, the equivalent flow diagram of Fig. 2.6(c) is useful in the development of type-II LDI switched capacitor filters which are insensitive to parasitic capacitances. This technique will be discussed in detail in Chapter 3.

2.5. MOS Switched Capacitor Filter Circuits

Using the signal flowgraph techniques, and switched capacitor integrators, many types of filters can be designed. This section will present several design examples which illustrate the signal flowgraph synthesis procedures.

2.5.1. Doubly-Terminated All-Pole Lowpass Ladder Filter

In the flow diagram of Fig. 2.6(b), it is apparent that the basic element is a differential integrator. If five switched capacitor differential integrators are interconnected as indicated in the flow diagram, the result is the complete switched capacitor circuit shown in Fig. 2.7 which closely approximates the RLC network of Fig. 2.1(a). In this figure, the phasing of the switches is alternated to obtain the

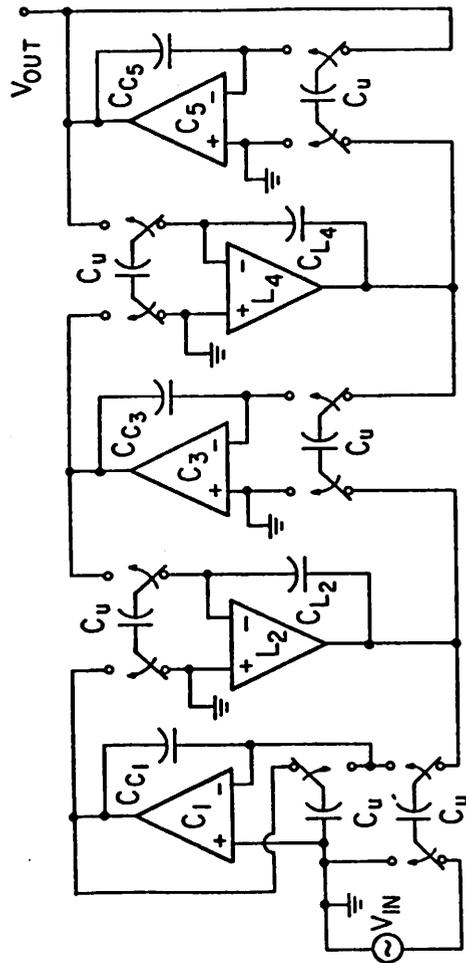


Fig. 2.7. A fifth-order switched capacitor type-I LDI doubly-terminated lowpass ladder filter.

type-I LDI configuration.

The final step in the design is to determine the capacitor ratios required in the circuit. It will be assumed that $R_1=R_2=R=1$ ohm and that the element values of the passive prototype (C_1 , L_2 , C_3 , L_4 and C_5) were obtained from standard design tables so that they correspond to a cutoff frequency of 1 rad/sec [26],[27],[29]. The ratio of the integrating capacitors (C_{C_1} , C_{L_2} , C_{C_3} , C_{L_4} and C_{C_5} in Fig. 2.7) to the switched capacitors, C_u , can be found from Eqn. (2.7) and the flow diagram:

$$\frac{C_{C_1}}{C_u} = \frac{f_c C_1}{\omega_{\infty}} \quad (2.15a)$$

$$\frac{C_{L_2}}{C_u} = \frac{f_c L_2}{\omega_{\infty}} \quad (2.15b)$$

$$\frac{C_{C_3}}{C_u} = \frac{f_c C_3}{\omega_{\infty}} \quad (2.15c)$$

$$\frac{C_{L_4}}{C_u} = \frac{f_c L_4}{\omega_{\infty}} \quad (2.15d)$$

$$\frac{C_{C_5}}{C_u} = \frac{f_c C_5}{\omega_{\infty}} \quad (2.15e)$$

where ω_{∞} is the desired cutoff frequency of the filter, and f_c is the sampling frequency.

The terminations are paths using unit sized capacitors (assuming 1 ohm termination and scaling resistors) from the output to the input of the first and last integrators. Unfortunately, there is an extra half cycle delay through the termination loops. This extra delay causes an error in the simulated termination resistance. In practice, the frequency response error due to this incorrect termination is often negligible [24],[25],[42].

2.5.2. Lowpass Ladder Filter with Finite Transmission Zeros

The addition of finite transmission zeros to a lowpass ladder filter response has great importance in many filter applications [1]. The zero addition is achieved on the RLC lowpass prototype by adding feedthrough capacitors across the series arm of the ladder network such as C_2 in Fig. 2.8(a). Imaginary axis zero locations are the resonant frequencies of the RLC resonant tank circuit, i.e. $\omega_{zero} = [L_2 C_2]^{-0.5}$. The flow diagram for this network is not as straight forward as for the simple lowpass case. The usual approach to flow diagram construction of the circuit is suitable only for continuous-time active RC implementations because it contains voltage attenuators. Usually, this is not desirable in a switched capacitor implementation since additional op amps would be required.

In order to design a switched capacitor network with zeros which does not require any additional operational amplifiers, it is useful to examine in detail the operations that are performed by the feedthrough capacitors added to the lowpass ladder structure. Referring to Fig. 2.8(a), a three-pole, two-zero RLC filter is shown with voltages and currents defined. Using Kirchhoff's current law at nodes A and B, the following equations are derived to explain the function of C_2 :

$$V_1 = \frac{(I_0 - I_2)}{s(C_1 + C_2)} + V_3 \left[\frac{C_2}{C_1 + C_2} \right] \tag{2.16}$$

and

$$V_3 = \frac{(I_2 - I_4)}{s(C_2 + C_3)} + V_1 \left[\frac{C_2}{C_2 + C_3} \right] \tag{2.17}$$

Thus, C_2 has been identified as an element that feeds some of the charge at node A to node B and vice-versa. As illustrated in Fig. 2.8(b), in order to implement a complex transmission zero pair, it is necessary to change the integrator gain

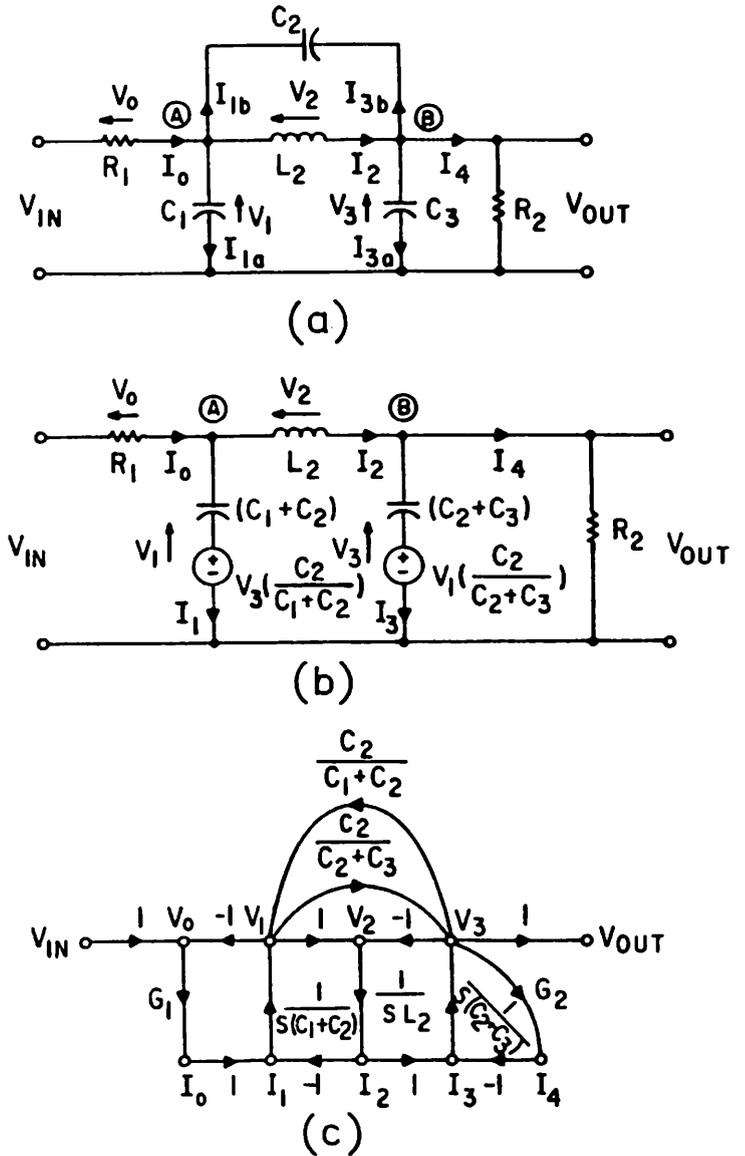


Fig. 2.8. (a) An RLC third-order elliptic lowpass ladder filter, and (b) an equivalent form, (c) the corresponding signal flowgraph.

constants that represent shunt capacitors to account for the feedthrough capacitor. This action, along with creating the feedforward and feedback paths, completely simulates the added series capacitance.

In the switched capacitor implementation, the integrator gain constants are easily changed by adjusting their capacitor ratios. The paths linking V_1 and V_3 of Fig. 2.8(c) require the addition of two op amp outputs. Fig. 2.9 shows a circuit that achieves the required integration and addition without additional op amp stages. The circuit performs a standard sampled-data integration on V_{in} , and in addition, continuously multiplies V_x by a constant and sums it to the output. Since C_1 and C_5 are held to a virtual ground on one side by the op amp, C_5 charges to $Q_5 = C_5 V_x$ and the output due to V_x is given by,

$$V_{out} = -\frac{Q_5}{C_1} = -\left[\frac{C_5}{C_1}\right]V_x \quad (2.18)$$

Although the summation is continuous, in the filter, V_x will be derived from another integrator whose output changes only once every clock cycle. Using switched capacitor integrator/summers for (C_1+C_2) and (C_2+C_3) in Fig. 2.8(c) allows the necessary additions at nodes V_1 and V_3 . Since the summations involve a sign inversion, some minor modifications must be made to the flow diagram. For example, if node V_1 , the output of an op amp, must contain a fraction of another node voltage V_3 , the two voltages must be of opposite sign on the flow diagram.

The method described above for obtaining transmission zeros requires very little additional hardware over the all-pole filter circuit. The example chosen to demonstrate the design methods of this section is a third-order elliptic filter [25]. The RLC network contains 4 energy storing devices, while the final switched capacitor circuit shown in Fig. 2.10 requires only 3 operational amplifiers. In addition, only 2 switches and 4 small capacitors are required over the simple lowpass

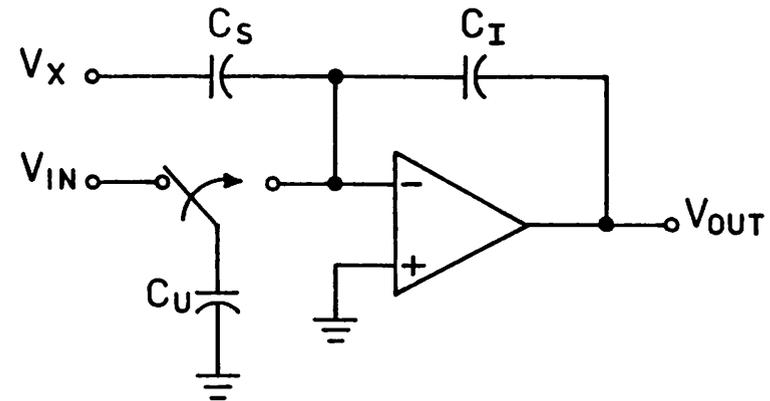


Fig. 2.9. A switched capacitor integrator/summer.

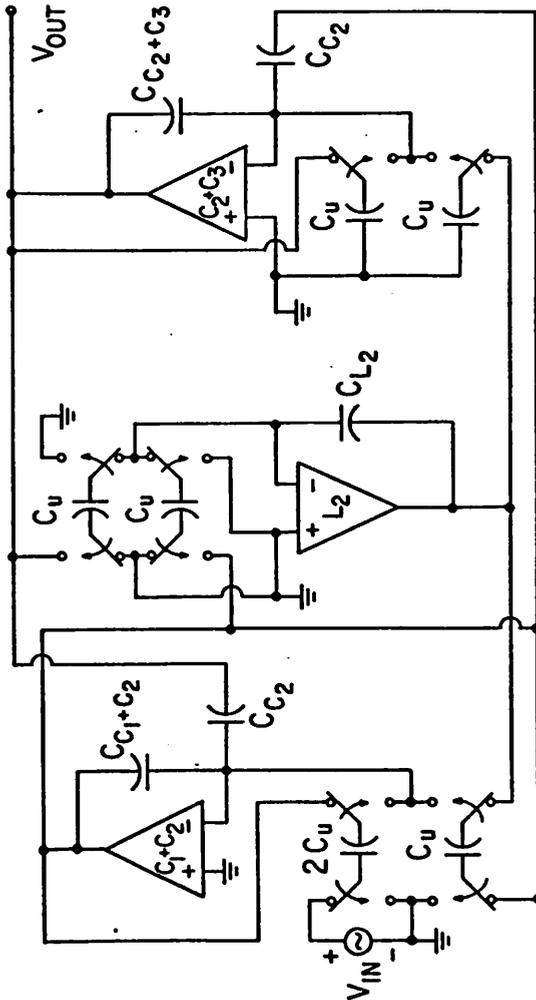


Fig. 2.10. A third-order switched capacitor type-I LDI doubly-terminated elliptic lowpass ladder filter.

structure.

2.5.3. Singly-Terminated All-Pole Lowpass Ladder Filter

A singly-terminated lowpass filter is a special case of a doubly-terminated RLC network with an infinite load resistance. Since the terminations appear as feedback paths in the switched capacitor network, the switched capacitor singly-terminated network is derived from the doubly-terminated network by simply omitting the termination feedback path on the last stage. A singly-terminated fifth-order switched capacitor lowpass filter is shown in Fig. 2.11.

2.5.4. Doubly-Terminated Bandpass Ladder Filters

The bandpass ladder is obtained by performing the standard lowpass-to-bandpass transformation on the lowpass prototype of Fig. 2.12(a). This is done by letting

$$s \rightarrow \frac{\omega_0}{B} \left[\frac{s}{\omega_0} + \frac{\omega_0}{s} \right] \quad (2.19)$$

where B is the desired bandwidth and ω_0 is the center frequency as shown in Table II [43]. Figure 2.12(b) shows a 4-pole RLC bandpass structure after transformation. An all-integrator signal flow diagram for the bandpass ladder is given in Fig. 2.12(c).

From Eqns. (2.7) and (2.19), the elements in the bandpass network of Fig. 2.12(b) are found to be

$$C_A = \frac{C_1}{B} = \frac{QC_1}{\omega_0} \quad (2.20a)$$

$$L_A = \frac{B}{C_1\omega_0^2} = \frac{1}{QC_1\omega_0} \quad (2.20b)$$

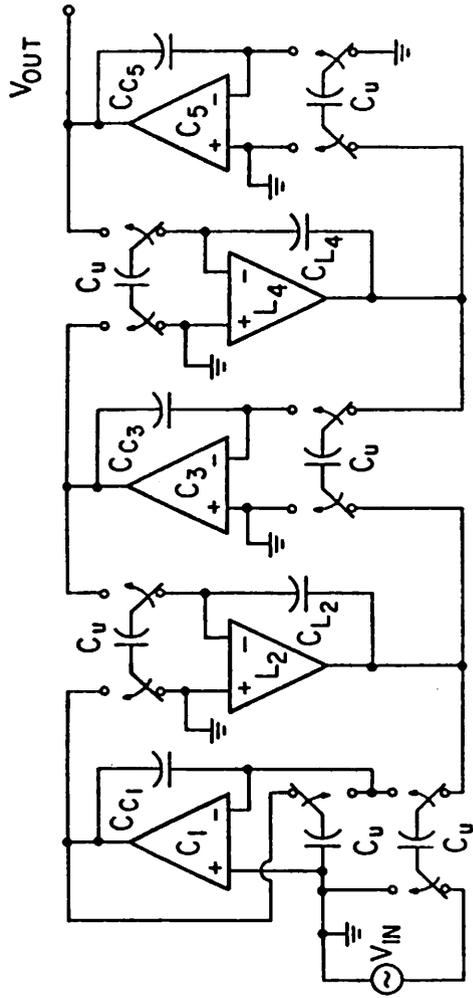


Fig. 2.11. A fifth-order switched capacitor type-I singly-terminated lowpass ladder filter.

| NORMALIZED LOW-PASS ELEMENTS | HIGH-PASS ELEMENTS | BANDPASS ELEMENTS | BAND-REJECT ELEMENTS |
|------------------------------|------------------------------------|--|--|
| L_N | $\frac{1}{\Omega_C L_N}$ | $\frac{L_N}{B}$ in series with $\frac{B}{\Omega_0^2 L_N}$ in shunt | $\frac{B L_N}{\Omega_0^2}$ in series with $1/B L_N$ in shunt |
| C_N | $\frac{1}{\Omega_C C_N}$ in series | $\frac{B}{\Omega_0^2 C_N}$ in series with $\frac{C_N}{B}$ in shunt | $\frac{1}{B C_N}$ in series with $\frac{B C_N}{\Omega_0^2}$ in shunt |

Table II. Transformations from the prototype lowpass elements to bandpass, bandreject and highpass elements.

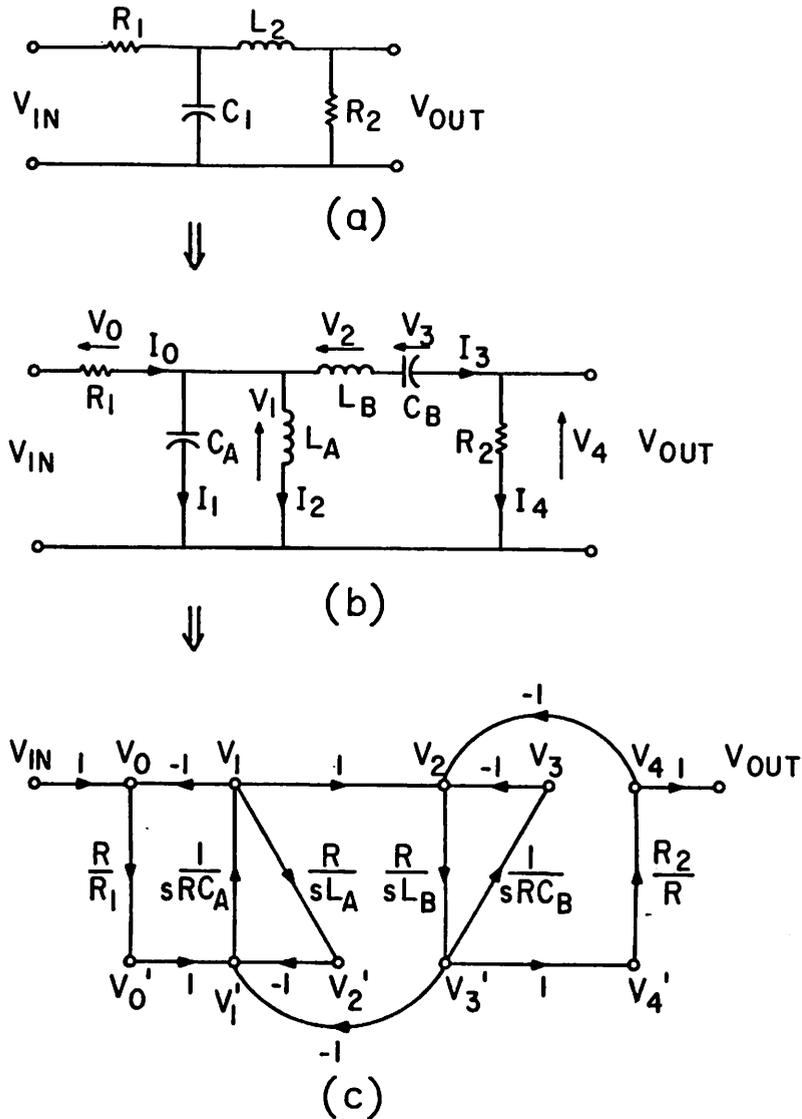


Fig. 2.12. (a) An RLC two-pole doubly-terminated lowpass ladder prototype; (b) the RLC four-pole bandpass filter, and (c) the corresponding signal flowgraph.

$$L_B = \frac{L_2}{B} = \frac{QL_2}{\omega_0} \quad (2.20c)$$

and

$$C_B = \frac{B}{L_2\omega_0^2} = \frac{1}{QL_2\omega_0} \quad (2.20d)$$

From the element values above, the capacitor ratios are calculated:

$$\frac{C_{C_A}}{C_u} = \frac{C_1 f_c}{B} = \frac{QC_1 f_c}{\omega_0} \quad (2.21a)$$

$$\frac{C_{L_A}}{C_u} = \frac{B f_c}{C_1 \omega_0^2} = \frac{f_c}{QC_1 \omega_0} \quad (2.21b)$$

$$\frac{C_{L_B}}{C_u} = \frac{L_2 f_c}{B} = \frac{QL_2 f_c}{\omega_0} \quad (2.21c)$$

$$\frac{C_{C_B}}{C_u} = \frac{B f_c}{L_2 \omega_0^2} = \frac{f_c}{QL_2 \omega_0} \quad (2.21d)$$

Note that the bandpass circuit has the same form as a lowpass ladder circuit with two-integrator loops substituted for single integrators. This corresponds to the transformations of single lowpass elements into L-C resonant circuits as dictated by Eqn. (2.19).

A signal flow diagram for the bandpass ladder is more complicated than that for the lowpass ladder due to the shunt and series element pairs. A switched capacitor version of this bandpass filter which is obtained from the flowgraph synthesis procedure of Section IV is shown in Fig. 2.13.

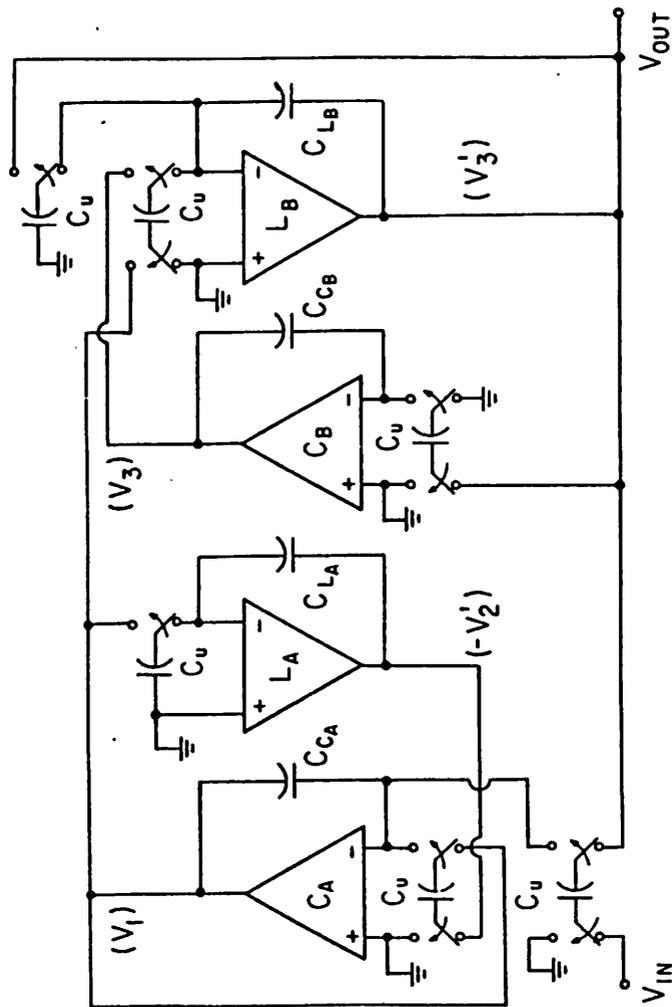


Fig. 2.13. A switched capacitor doubly-terminated four-pole bandpass ladder filter.

2.5.5. Singly-Terminated Bandpass Ladder Filter

As in the lowpass case, the singly-terminated bandpass ladder is obtained from the doubly-terminated bandpass ladder by simply eliminating a termination feedback loop. A singly-terminated RLC 4-pole bandpass derived from the singly-terminated RLC lowpass of Fig. 2.14(a) is shown in Fig. 2.14(b), with its switched capacitor equivalent circuit in Fig. 2.15.

2.5.6. Singly-Terminated Highpass Ladder Filter

A highpass filter is obtained by performing the standard lowpass-to-highpass transformation on the RLC lowpass prototype as indicated in Table II. This is done by letting

$$s \rightarrow \frac{\omega_c}{s} \quad (2.22)$$

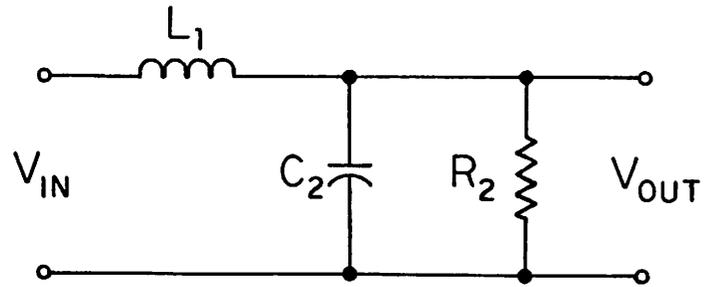
which simply replaces all inductors by capacitors and vice-versa. A singly-terminated RLC highpass ladder filter is shown in Fig. 2.16(a). Figure 2.16(b) shows the corresponding signal flowgraph which unfortunately cannot be directly implemented using switched capacitor techniques because summed signals (such as V_2) cannot be accessed and fed forward since the summing is performed into a virtual ground. The intermediate flowgraph of Fig. 2.16(c) can be constructed by defining some new variables:

$$V_2 = -(V_1 - V_{in}) = -V_1' \quad (2.23a)$$

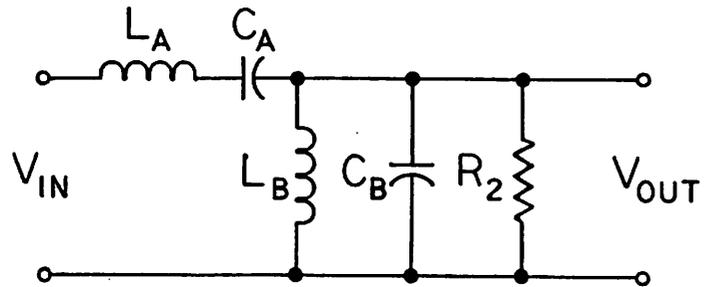
$$V_4 = -(V_3 - V_2) = -V_3' \quad (2.23b)$$

$$I_1 = I_2 + I_3 = I_2' \quad (2.23c)$$

$$I_3 = I_4 + I_5 = I_4' \quad (2.23d)$$



(a)



(b)

Fig. 2.14. (a) An RLC two-pole singly-terminated lowpass ladder prototype; (b) the corresponding RLC four-pole bandpass filter.

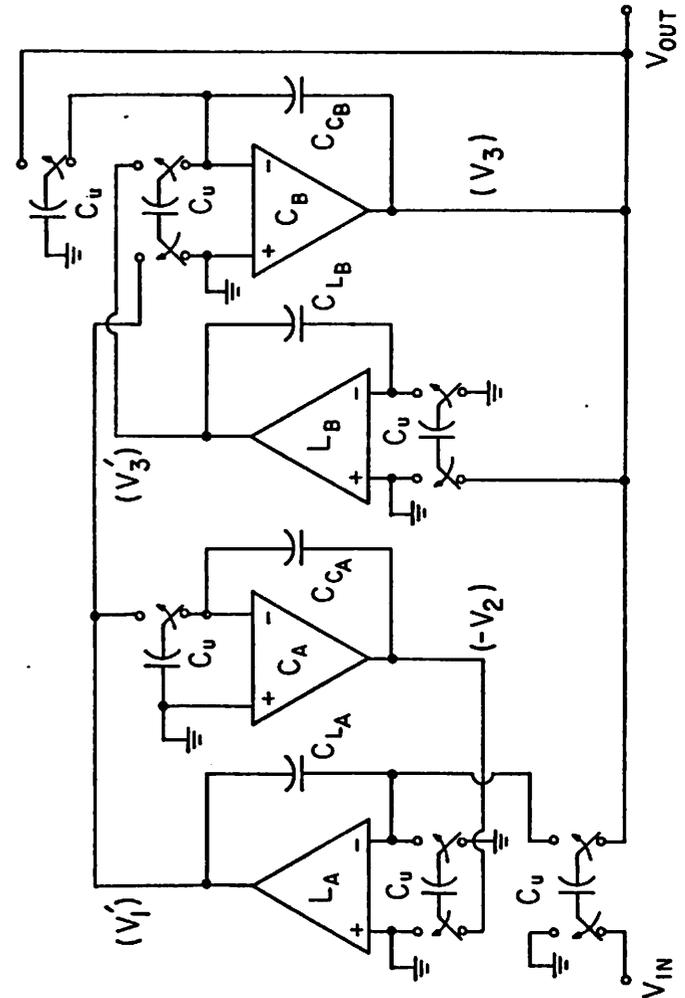


Fig. 2.15. A switched capacitor singly-terminated four-pole bandpass ladder filter.

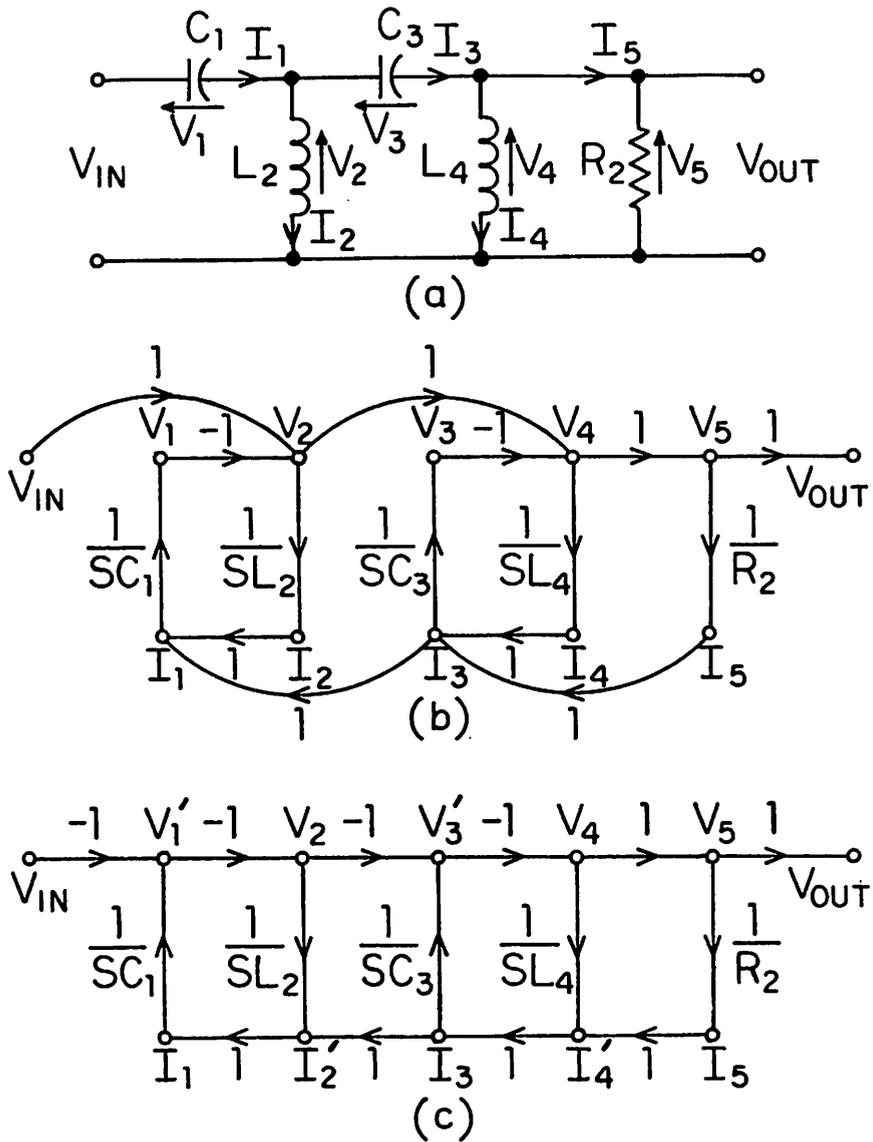


Fig. 2.16. (a) A fourth-order singly-terminated RLC ladder filter; (b) the flowgraph for Fig. 2.16(a), and (c) an equivalent intermediate flowgraph.

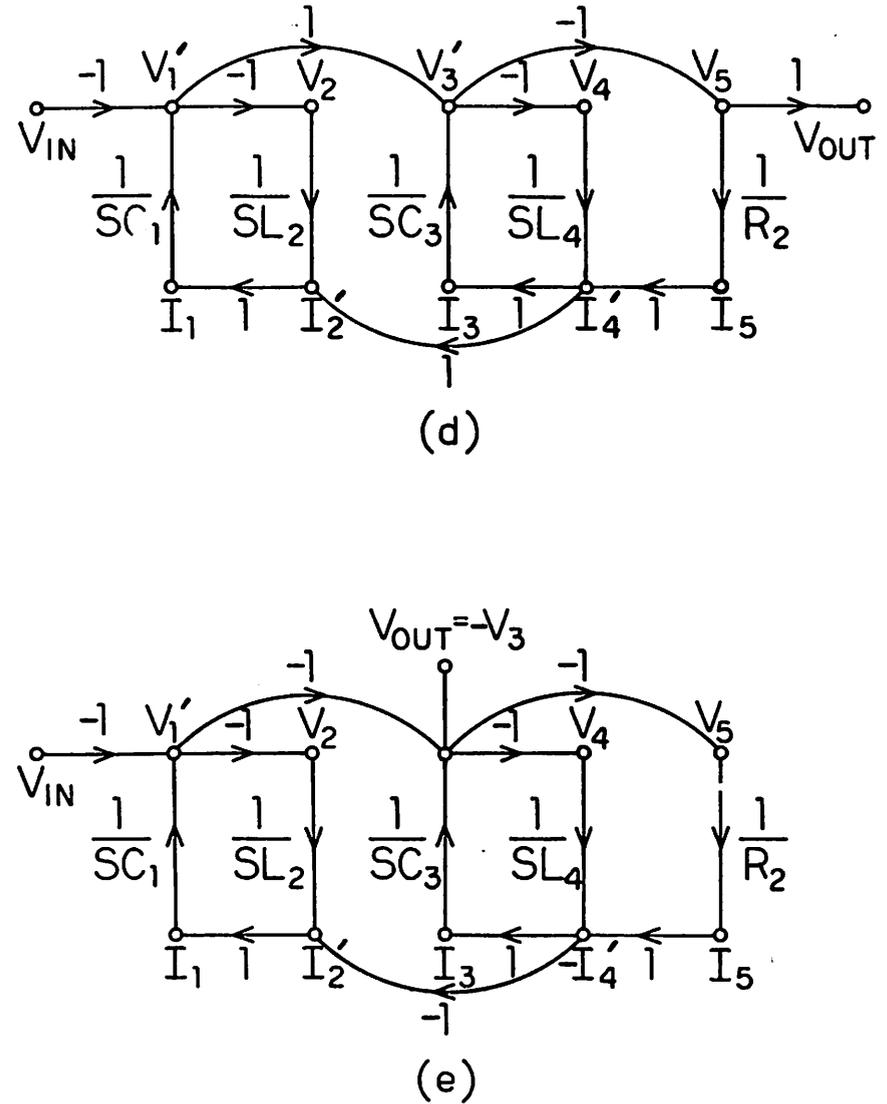


Fig. 2.16. (d) An intermediate flowgraph, and (e) the final flowgraph for the circuit of Fig. 2.16(a).

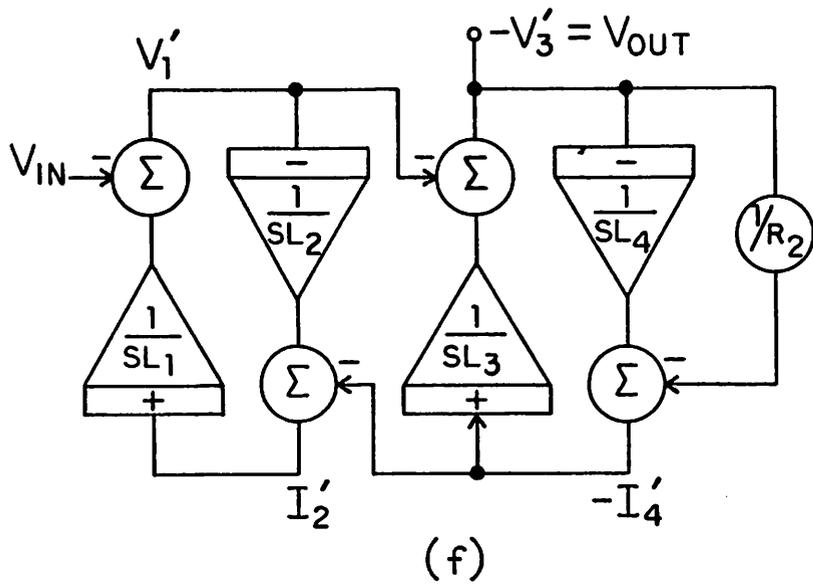


Fig. 2.16. (f) A symbolic implementation of the flowgraph in Fig. 2.16(e) using integrators and summers.

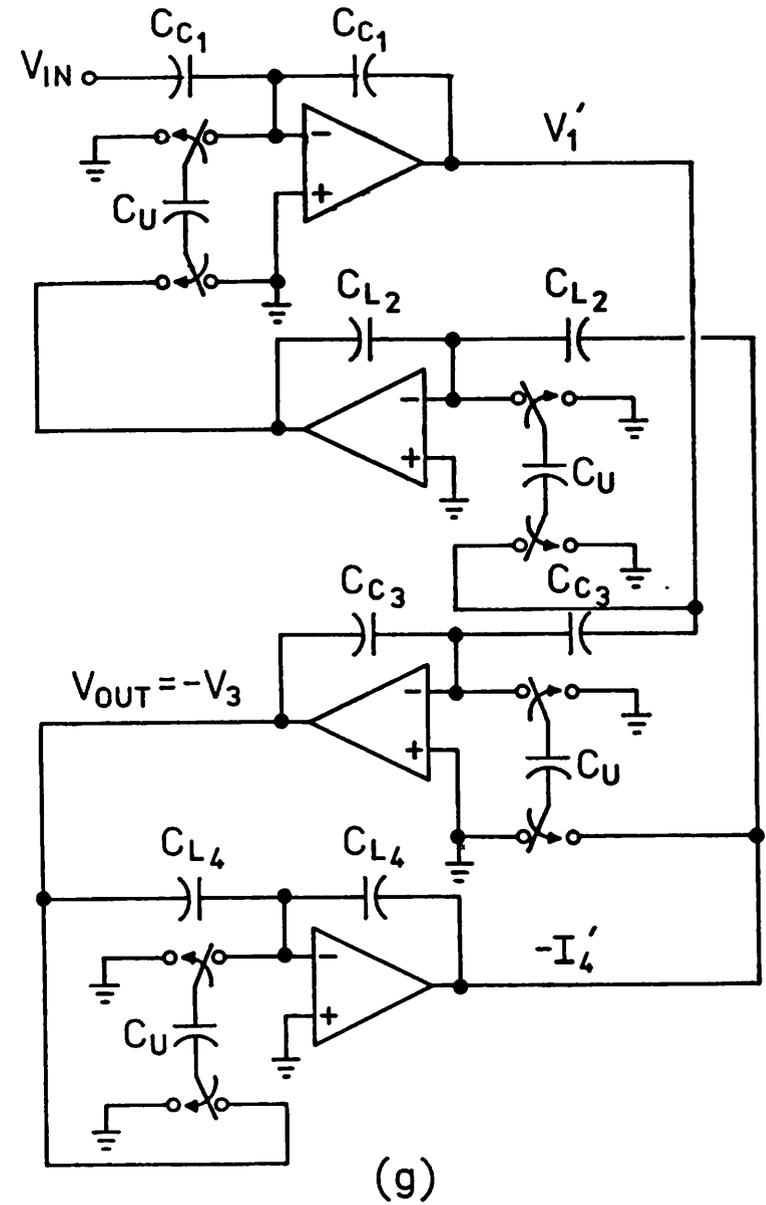


Fig. 2.16. (g) A type-II LDI switched capacitor fourth-order singly-terminated highpass ladder filter.

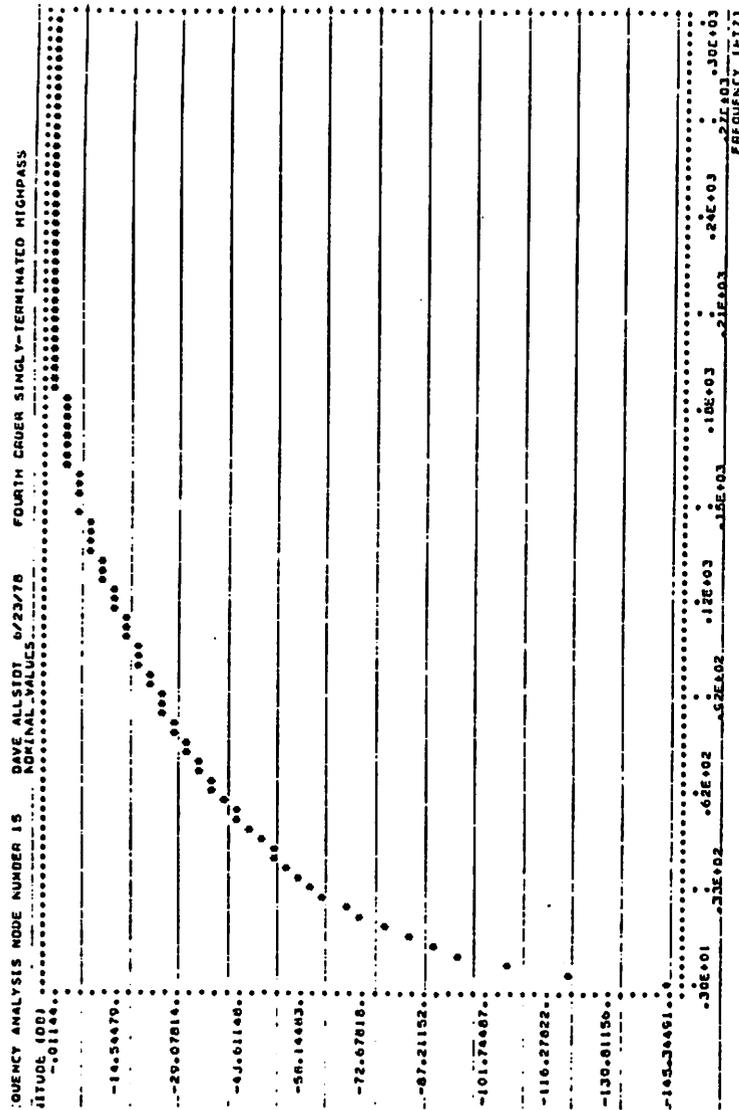


Fig. 2.16. (h) A DINAP simulation for the circuit of Fig. 2.16(g) with a 300 Hz cutoff frequency when clocked at 128 kHz.

The flowgraph of Fig. 2.16(c) is still not realizable due to the signals leaving summing nodes. However, by noting that

$$V_3' = \frac{I_3}{sC_3} - V_2 = \frac{I_3}{sC_3} + V_1' \quad (2.24a)$$

$$V_5 = V_4 = -V_3' \quad (2.24b)$$

and

$$I_2' = \frac{V_2}{sL_2} + I_3 = \frac{V_2}{sL_2} + I_4' \quad (2.24c)$$

the signal flowgraph of Fig. 2.16(d) is obtained, which when the signs are appropriately modified, results in the flowgraph of Fig. 2.16(e) which is implemented using integrator/summers in Fig. 2.16(f). Figure 2.16(g) shows the switched capacitor version, and Fig. 2.16(h) shows a DINAP simulation for a fourth-order singly-terminated highpass ladder filter with a 300 Hz cutoff frequency when clocked at 128 kHz.

2.5.7. Doubly-Terminated Highpass Ladder Filter

A signal flowgraph for the RLC doubly-terminated ladder filter of Fig. 2.17(a) is shown in Fig. 2.17(b). Unfortunately, the continuous loop formed around the summation path has a gain which is nominally one, so that this network is prone to oscillation.

One solution to this problem is to use a different form of the information contained in the signal flowgraph. From the flowgraph of Fig. 2.17(b), the output voltage is

$$V_{out} = V_1 - V_2 \quad (2.25)$$

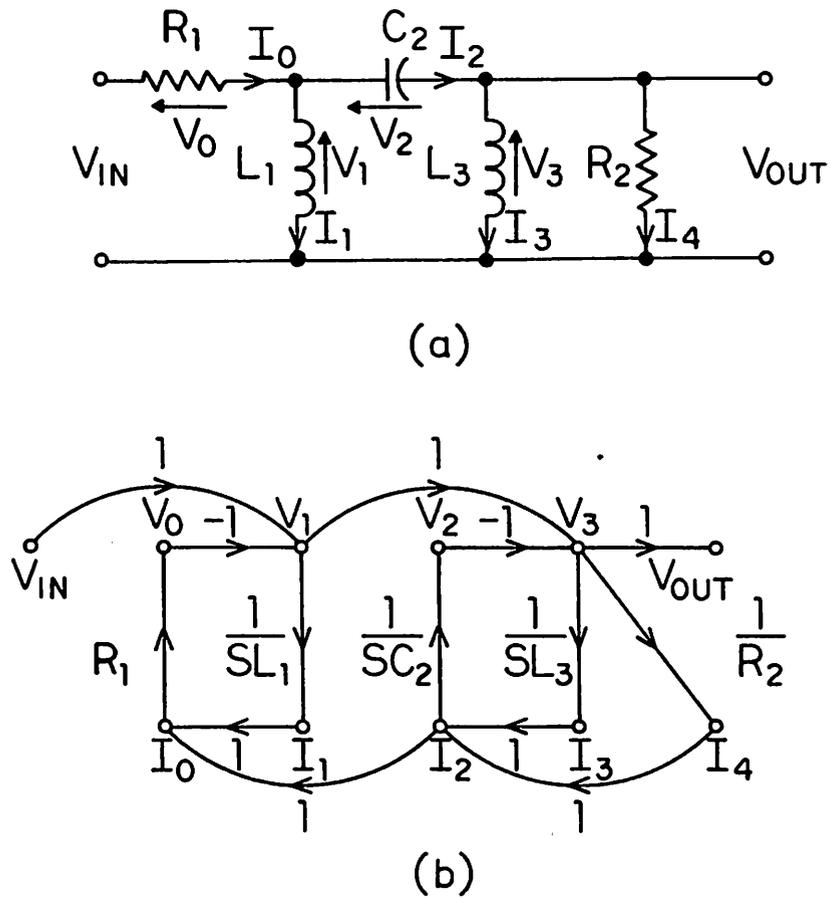


Fig. 2.17. (a) A third-order doubly-terminated highpass ladder filter and (b) a signal flow diagram.

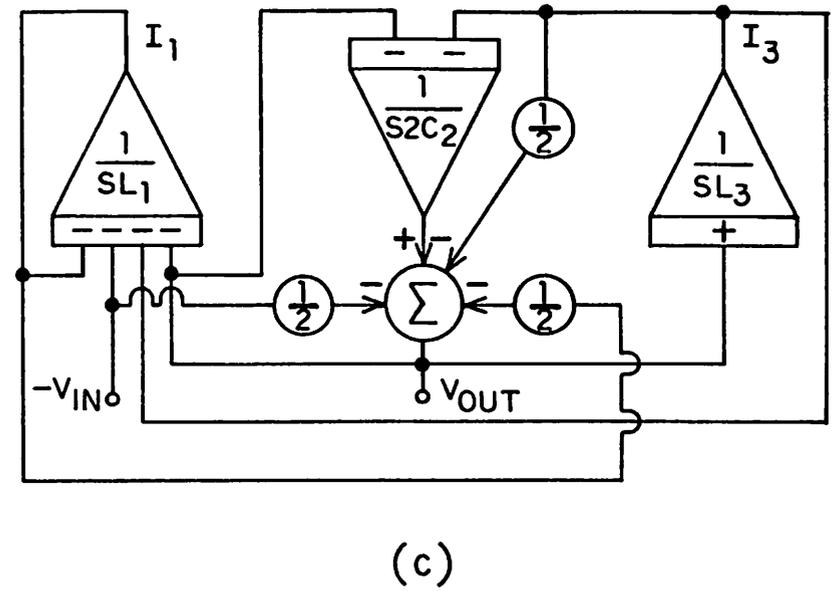


Fig. 2.17. (c) A symbolic representation of Fig. 2.17(a) using integrators and summers.

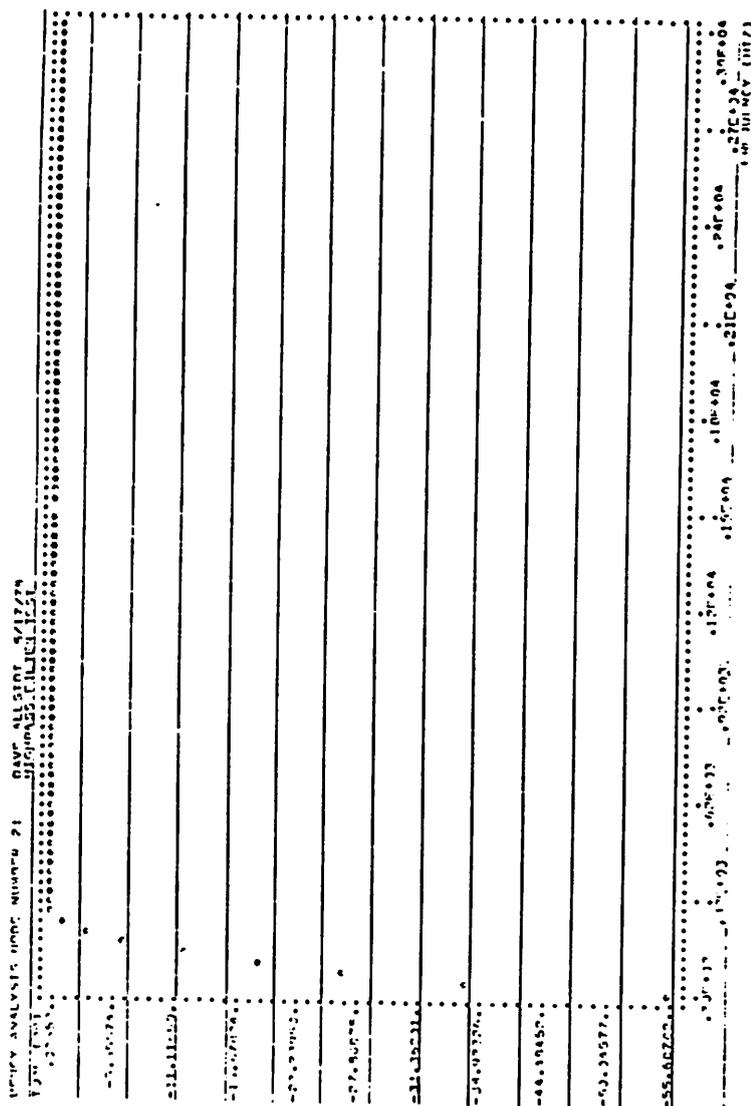


Fig. 2.17. (d) A DINAP simulation for the circuit of Fig. 2.17(c) with a 300 Hz cutoff frequency when clocked at 128 kHz.

and the other output variables in the circuit are I_1 , and I_3 . A doubly-terminated structure can be formed by solving for all of the output variables in terms of themselves and the input voltage to obtain:

$$I_1 = \frac{1}{sL_1} \left[-(-V_{in}) - I_1 - V_{out} - I_3 \right], \quad (2.26a)$$

$$V_{out} = \frac{-(-V_{in})}{2} - \frac{I_1}{2} - \frac{I_3}{2} + \frac{1}{s2C_2} (-I_3 - V_{out}) \quad (2.26b)$$

and

$$I_3 = \frac{1}{sL_3} V_3 = \frac{1}{sL_3} V_{out}. \quad (2.26c)$$

A symbolic representation of these equations is shown in Fig. 2.17(c) with a DINAP simulation in Fig. 2.17(d) for a 300 Hz cutoff frequency when clocked at 128 kHz. Since there are no continuous loops, this circuit will not be subject to oscillation.

2.5.8. Doubly-Terminated Elliptic Highpass Ladder Filter

Many applications require a highpass response with additional rejection of certain frequencies. A doubly-terminated RLC elliptic highpass filter is shown in Fig. 2.18(a). This circuit can be simplified by solving for V_1 and V_3

$$V_1 = s \left[\frac{L_1 L_2}{L_1 + L_2} \right] (I_0 - I_2) + \left[\frac{L_1}{L_1 + L_2} \right] V_3, \quad (2.27a)$$

and

$$V_3 = s \left[\frac{L_2 L_3}{L_2 + L_3} \right] (I_2 - I_4) + \left[\frac{L_3}{L_2 + L_3} \right] V_1. \quad (2.27b)$$

to obtain the equivalent circuit for the elliptic highpass shown in Fig. 2.18(b). Using an equation formulation similar to that of the previous section, the circuit of Fig. 2.18(c) is derived with a DINAP simulation shown in Fig. 2.18(d). An advantage of this formulation over a direct four amplifier implementation is that by forming the equivalent circuit of Fig. 2.18(b), the large L_2 value is reduced by paralleling it with the two smaller inductors, L_1 and L_3 , and therefore, the required silicon area is greatly reduced.

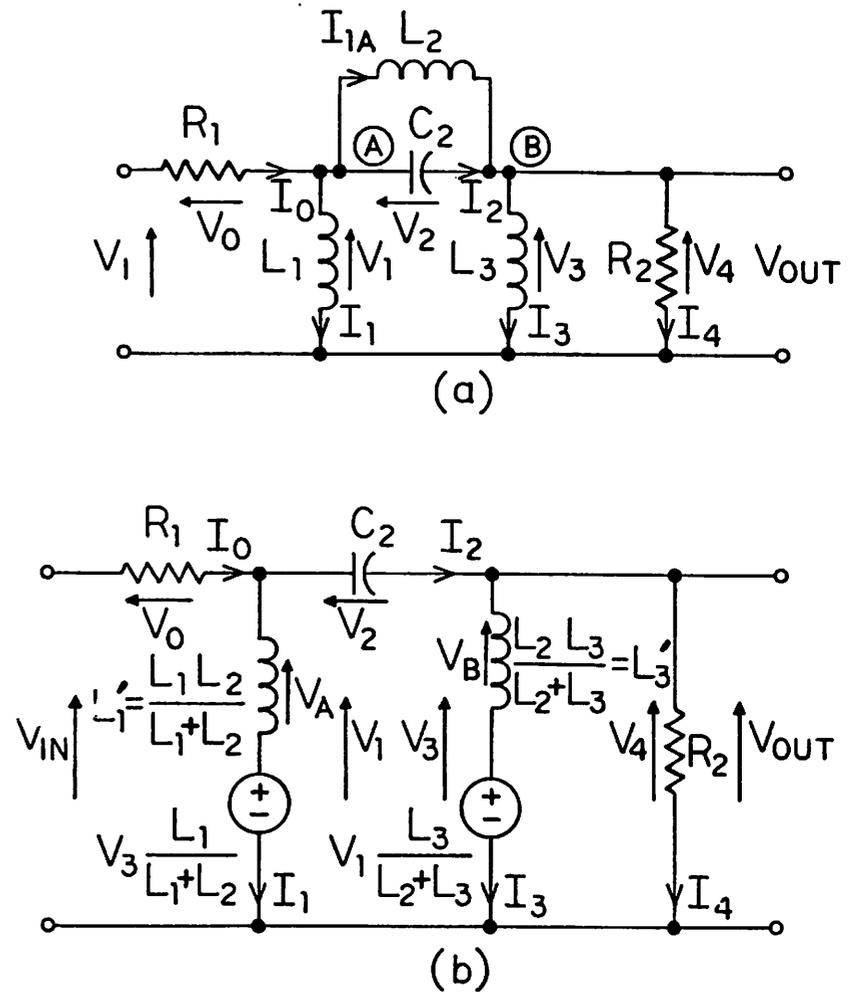


Fig. 2.18. (a) A doubly-terminated RLC third-order elliptic highpass filter, and (b) an equivalent form.

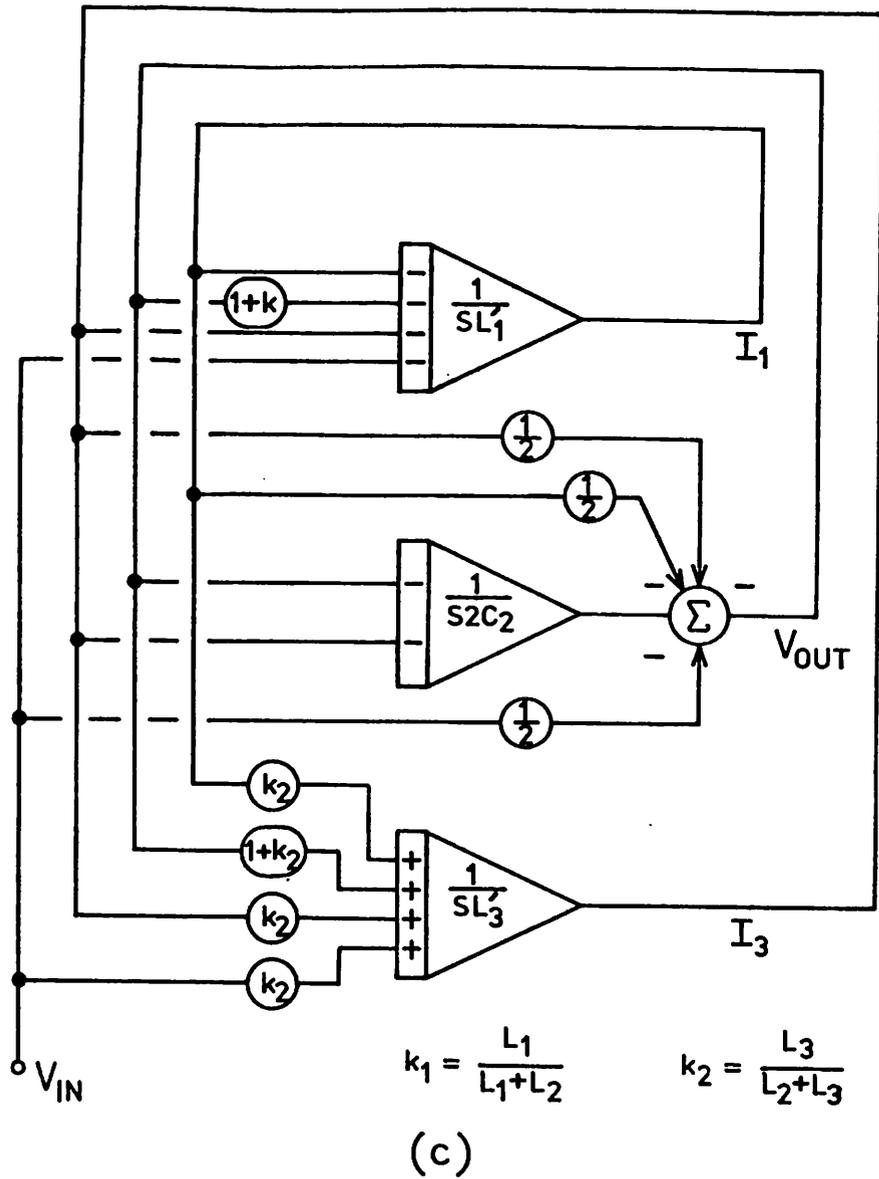


Fig. 2.18. (c) A symbolic implementation of Fig. 2.18(a) using integrators and summers.

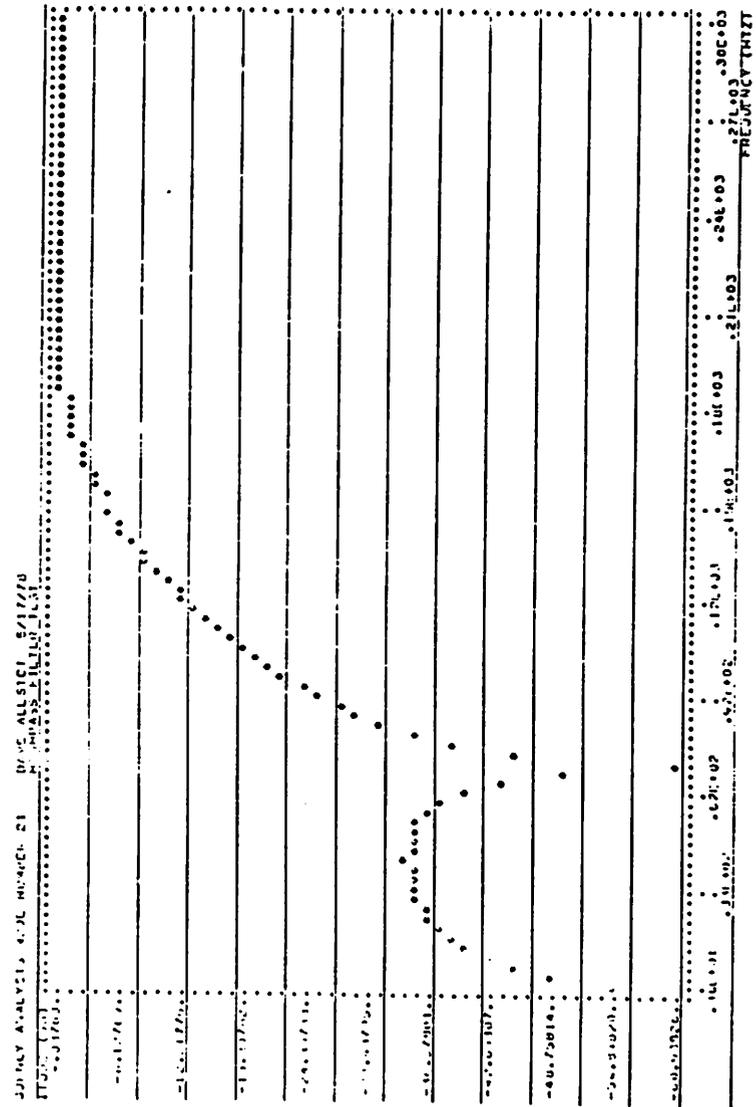


Fig. 2.18. (d) A DINAP simulation for the circuit of Fig. 2.18(a) with a 300 Hz cutoff frequency when clocked at 128 kHz.

CONSIDERATIONS FOR THE MONOLITHIC MOS IMPLEMENTATION OF SWITCHED CAPACITOR FILTERS

In the monolithic MOS implementation of switched capacitor ladder filters, there are several important effects which must be considered including: (1) The finite switching frequency of the sampled-data system; (2) nonidealities associated with the passive MOS switches and capacitors, and (3) nonidealities associated with the operational amplifiers. These practical design aspects will be considered in this chapter.

3.1. Sampled-Data Discrete-Time Effects

Switched capacitor filters are analog discrete-time systems which, in many cases, are derived from continuous-time RLC prototypes. In this section, the effects of transforming from the continuous- to the sampled-data domain are described.

3.1.1. Continuous-Time RC Integrators

The conventional inverting integrator of Fig. 3.1(a) consists of a resistor, R_1 , a capacitor, C_1 , and an operational amplifier. The transfer function for this RC integrator is given by

$$H(s) = - \frac{A_o}{(A_o+1)sR_1C_1 + 1} \quad (3.1)$$

with magnitude

$$|H(\omega)| = \frac{A_o}{[1 + (A_o+1)^2(R_1C_1)^2\omega^2]^{1/2}} \quad (3.2)$$

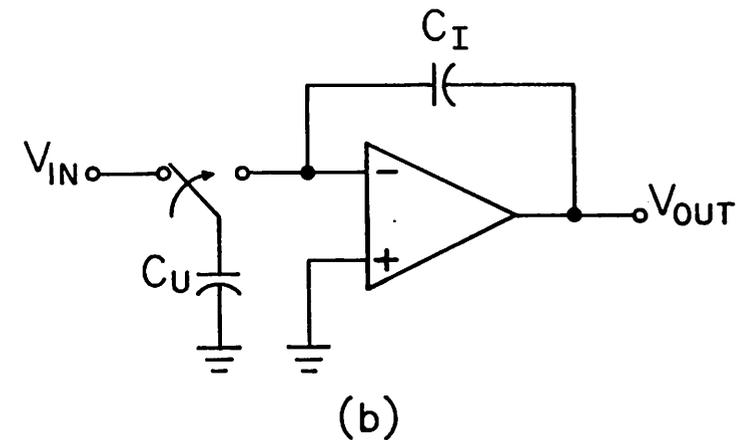
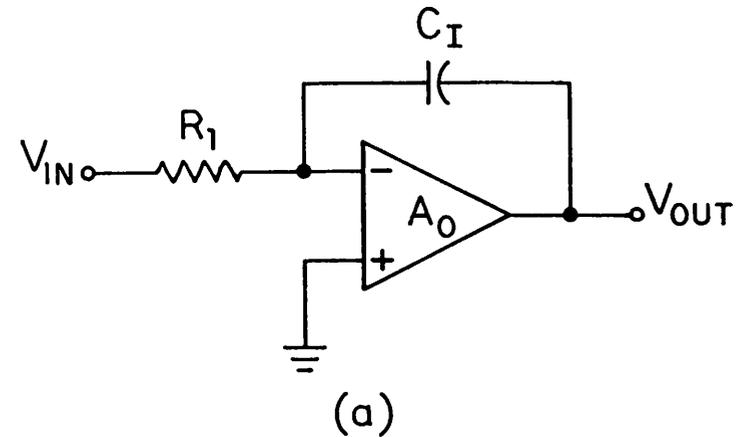


Fig. 3.1. (a) A conventional continuous-time RC integrator; (b) a sampled-data switched capacitor integrator.

and phase

$$\Phi(\omega) = -\pi - \tan^{-1}\omega R_1 C_1 (A_0 + 1) \quad (3.3)$$

where A_0 is the DC open-loop gain of an otherwise ideal op amp. The magnitude asymptotes and phase of Eqns. (3.2) and (3.3) are plotted in Figs. 3.2(a) and (b), respectively. From Fig. 3.2(a), it is evident that finite op amp gain results in a lossy integrator with an error in the integrator bandwidth. To reduce this error to less than 1%, the op amp is required to have A_0 greater than 100, and when A_0 is greater than 1000, the integrator gain constant error is less than 0.1%. If A_0 is infinite, the transfer function of Eqn. (3.1) becomes

$$H(s) = -\frac{\omega_0}{s} \quad (3.4a)$$

or equivalently,

$$H(\omega) = -\frac{\omega_0}{j\omega} \quad (3.4b)$$

with $\omega_0 = \frac{1}{R_1 C_1}$. The characteristics of analog sampled-data integrators will be presented in the next section.

3.1.2. Discrete-Time Switched Capacitor Integrators

An important difference between the conventional RC integrator of Fig. 3.1(a), and the switched capacitor integrator of Fig. 3.1(b) is that the latter usually only samples the input signal once each clock cycle. Hence, there can be a time delay through the integrator of up to one full clock period. The excess phase shift associated with this time delay can result in significant Q-enhancement if a switched capacitor integrator is used to directly replace a conventional RC integrator

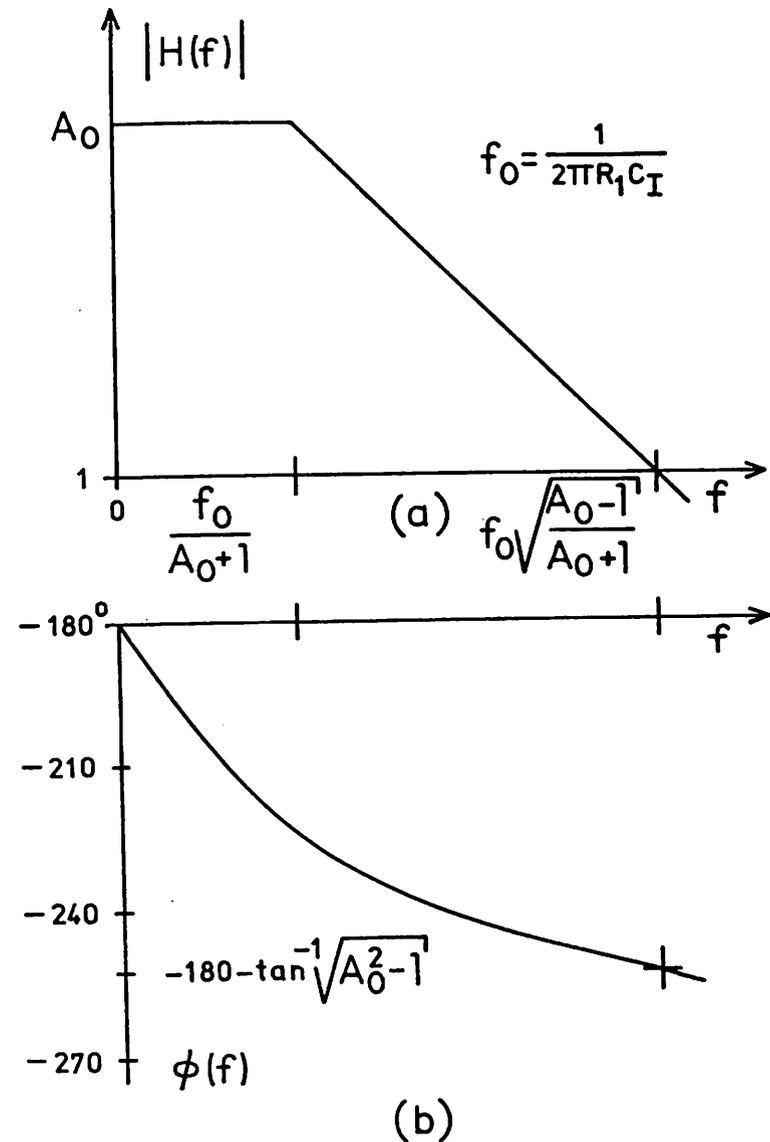


Fig. 3.2. (a) The magnitude and (b) the phase plots for an RC integrator with A_0 representing the op amp DC open-loop gain.

in an active ladder circuit. This phase shift can complicate the design, but more importantly, can break down the analogy of the design with the RLC passive ladder prototype. If this happens, the low sensitivity obtainable with a doubly-terminated ladder may be lost. Fortunately, the effect of this deleterious phase shift can be almost completely eliminated.

In order to analyze the effect of the time delay, it is useful to develop a z-transform model of the inverting integrator of Fig. 3.1(b) (assuming an ideal op amp) [38]-[39]. The switched capacitor, C_u , will be charged to the input voltage, $V_{in}(t)$, at the beginning of each clock period, and will be switched to the op amp virtual ground halfway through each cycle. Therefore, at the beginning of the n^{th} clock period (i.e. $t=nT_c$), the switch is in the left position, and C_u has a charge $Q_{C_u}=C_u V_{in}(nT_c)$. The value of the output signal at this time is stored as the charge, Q_{C_1} , on the integrating capacitor, C_1 . Its value was determined a half cycle earlier at $t=(n-1/2)T_c$ and therefore, $Q_{C_1}=C_1 V_{out}((n-1/2)T_c)$. At the next half cycle time, $t=(n+1/2)T_c$, the switch is in the right position, and the capacitor C_u is discharged by the op amp as the charge is transferred from C_u to C_1 . The charge on C_1 is now

$$C_1 V_{out}[(n+1/2)T_c] = C_1 V_{out}[(n-1/2)T_c] - C_u V_{in}(nT_c). \quad (3.5)$$

The transfer function taken at this half cycle time, $H_{1/2}(z)$, is therefore

$$H_{1/2}(z) = - \left[\frac{C_u}{C_1} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right], \quad (3.6)$$

where the subscript 1/2 indicates that there is only 1/2 clock cycle of delay in the forward path of this integrator. An integrator with this half-delay property is known as a type-I Lossless Discrete Integrator (LDI) [42].

For the next half clock period from $(n+1/2)T_c$ to $(n+1)T_c$, (i.e. during the sampling interval), the output does not change, which yields another half cycle of delay. Therefore, the transfer function of the integrator taken at the end of this interval (at $t=(n+1)T_c$) has a full cycle of delay in the forward path and is given by,

$$H_1(z) = - \left[\frac{C_u}{C_1} \right] \left[\frac{z^{-1}}{1-z^{-1}} \right]. \quad (3.7)$$

This integrator is called the Direct-Transform Discrete Integrator (DDI) [42].

The type-I Lossless Discrete Integrator of Eqn. (3.6) has exactly the same phase shift as a continuous-time integrator [42]. However, the DDI integrator represented by Eqn. (3.7) has significant excess phase. To illustrate this result, the frequency responses of $H_{1/2}(z)$ and $H_1(z)$ are evaluated by setting $z=e^{j\omega T_c}$ to obtain

$$H_{1/2}(\omega) = - \frac{\omega_o}{j\omega} \left[\frac{\omega T_c}{2\sin(\omega \frac{T_c}{2})} \right] \quad (3.8)$$

and

$$H_1(\omega) = - \frac{\omega_o}{j\omega} \left[\frac{\omega T_c \exp(-j\omega \frac{T_c}{2})}{2\sin(\omega \frac{T_c}{2})} \right], \quad (3.9)$$

with $\omega_o = f_c \left[\frac{C_u}{C_1} \right]$. These expressions are factored so that the term in brackets is the deviation from the response of the continuous-time integrator given in Eqn. (3.4b).

Table I shows that the sampling frequency must be large relative to the passband frequencies in order to minimize the error in the magnitude of the integrator bandwidth in Eqns. (3.8) and (3.9). (For the designs of this thesis, the clock frequency was typically 35 times greater than the maximum passband

| NORMALIZED FREQUENCY $\frac{f}{f_c}$ | ERROR IN GAIN CONSTANT MAGNITUDE |
|---|--|
| 0.00 | 0.00 % |
| 0.05 | 0.41 |
| 0.10 | 1.66 |
| 0.15 | 3.80 |
| 0.20 | 6.90 |
| 0.25 | 11.07 |
| 0.30 | 16.50 |
| 0.35 | 23.41 |
| 0.40 | 32.13 |
| 0.45 | 43.13 |
| 0.50 | 57.08 |

Table 1. Magnitude errors in switched capacitor integrators versus normalized frequency.

frequencies so that the gain constant error was 0.13%).

From Eqn. (3.9), it is apparent that the DDI integrator has an extra phase shift of $-\pi \left[\frac{f}{f_c} \right]$ radians in its transfer function. If only integrators with this response are used in an active-ladder configuration, this phase shift is equivalent to introducing finite Q in the inductors and capacitors which are being simulated. However, the sign of this loss is opposite to that which is obtained in circuit elements due to parasitic resistances and conductances, so that instead of a droop in the frequency response (which is usually associated with finite element Q) the response exhibits peaking. In most cases, this peaking is not desirable so that the integrators should be operated to eliminate the excess phase shift.

3.1.3. DDI Switched Capacitor Filters Without Predistortion

As mentioned in the previous section, if switched capacitor filters are implemented directly using DDI integrators, the filter response will exhibit peaking due to the Q -enhancement provided by the excess phase. For example, a fifth-order filter was designed for a Chebyshev lowpass response with a 3.4 kHz cutoff frequency, and a total passband ripple of 0.1 dB when clocked at 128 kHz. The simulated DDI response of Fig. 3.3 shows a total passband peaking of about 8 dB, and a cutoff frequency greater than 4.0 kHz.

The Q -enhancement is analyzed by comparing the transfer function of the conventional integrator of Eqn. (3.4a) to the DDI transfer function of Eqn. (3.7) with its numerator and denominator multiplied by zf_c [45]. The numerators of both equations correspond to integrator gain constants while the denominators specify a mapping from the continuous- to the sampled-data domain:

$$s \rightarrow f_c(z-1) = f_c(e^{sT_c}-1). \quad (3.10)$$

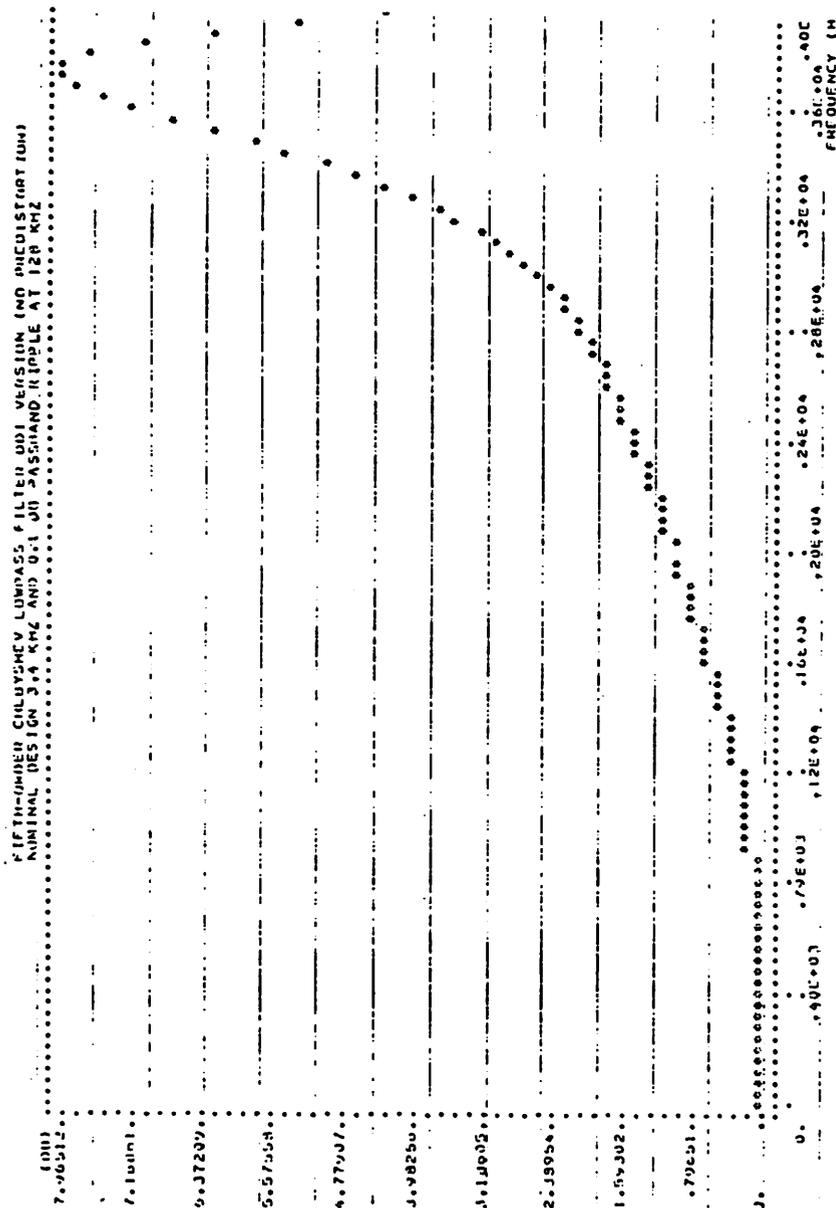


Fig. 3.3. Passband response for a fifth-order Chebyshev DDI lowpass switched capacitor filter without predistortion. Q-enhancement results in about 8 dB of peaking and increases the cutoff frequency. Sampling frequency was 128 kHz.

Consider a pole in the s-plane, $p_c = \alpha_c + j\omega_c$. Eqn. (3.10) can be used to calculate the new s-plane sampled-data pole position by solving for $p_i = \alpha_i + j\omega_i$ to obtain:

$$\alpha_i = f_c \ln \left[\left(\frac{\alpha_c + f_c}{f_c} \right)^2 + \left(\frac{\omega_c}{f_c} \right)^2 \right]^{1/2} \quad (3.11)$$

and

$$\omega_i = f_c \tan^{-1} \left[\frac{\omega_c}{\alpha_c + f_c} \right] \quad (3.12)$$

From these equations, it is apparent that finite sampling frequency causes significant pole movement as indicated by the arrows in Fig. 3.4. Table II lists the ideal pole positions for the prototype Chebyshev continuous-time lowpass filter, and the s-plane sampled-data pole positions calculated using Eqns. (3.11) and (3.12). It is interesting to compare the values of pole-Q for the two cases. For the continuous-time case,

$$Q_c = \frac{\omega_c}{2\alpha_c} \quad (3.13)$$

and after the sampled-data pole movement, the pole-Q is

$$Q_i = \frac{\omega_i}{2\alpha_i} \quad (3.14)$$

The values of pole-Q for the fifth-order Chebyshev DDI switched capacitor example at 128 kHz are also presented in Table II where the Q-enhancement due to excess phase is clearly evident.

The sensitivity of the peaked response of Fig. 3.3 was determined for $\pm 1\%$ variations in all capacitor ratios. The results of Fig. 3.5 indicate that the DDI

IDEAL POLE POSITIONS
ON CHEBYSHEV ELLIPSE

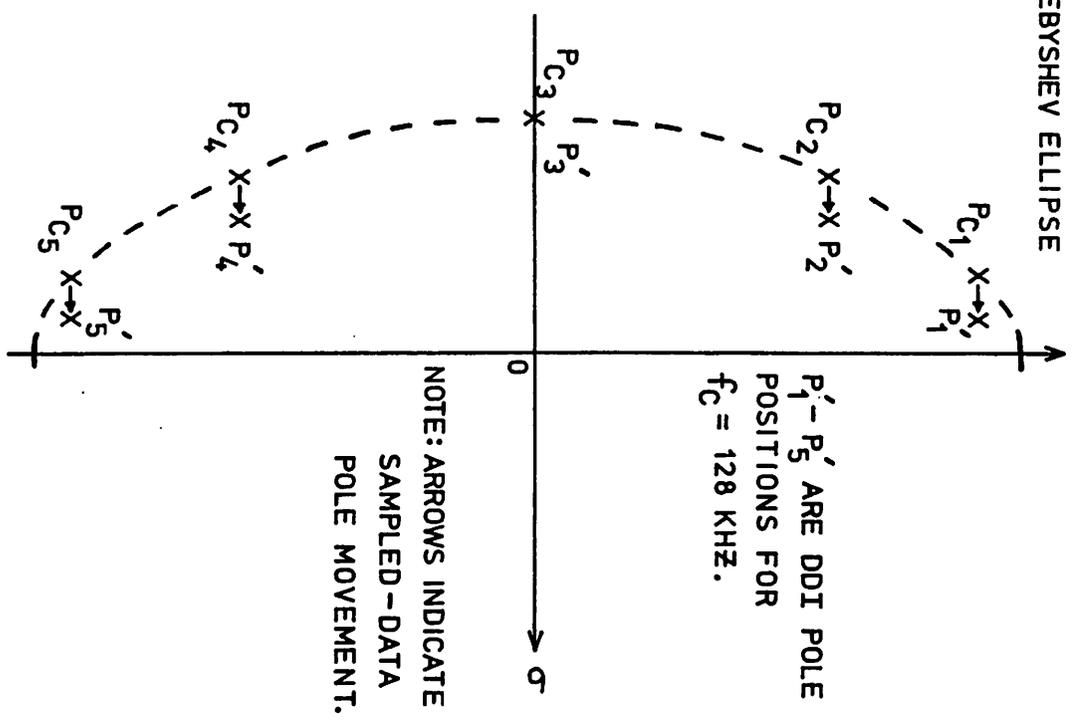


Fig. 3.4. Pole movement due to excess phase associated with the DDI switched capacitor integrators. Example is for a five-pole Chebyshev lowpass filter sampled at 128 kHz.

| CONTINUOUS CASE | | DDI SAMPLED DATA CASE (128 KHZ) | | PREDISTORTED DDI SAMPLED DATA CASE (128 KHZ) | |
|---------------------------|--------|---------------------------------|--------|--|--------|
| NORMALIZED POLE POSITIONS | POLE Q | NORMALIZED POLE POSITIONS | POLE Q | NORMALIZED POLE POSITIONS | POLE Q |
| -0.1665 -j 1.0804 | 3.24 | -0.0676 -j 1.0982 | 8.12 | -0.2585 -j 1.0446 | 2.02 |
| -0.4360 -j 0.6677 | 0.77 | -0.4095 -j 0.7163 | 0.87 | -0.4548 -j 0.6193 | 0.68 |
| -0.5389 +j 0.0000 | 0.00 | -0.5644 +j 0.0000 | 0.00 | -0.5151 +j 0.0000 | 0.00 |
| -0.4360 +j 0.6677 | 0.77 | -0.4095 +j 0.7163 | 0.87 | -0.4548 +j 0.6193 | 0.68 |
| -0.1665 +j 1.0804 | 3.24 | -0.0676 +j 1.0982 | 8.12 | -0.2585 +j 1.0446 | 2.02 |

Table II. Comparison of pole positions and pole-Q for the continuous case, and the DDI switched capacitor filters with and without predistortion. Nominal response is fifth-order Chebyshev lowpass with 0.1 dB passband ripple. Sampling rate was 128 kHz.

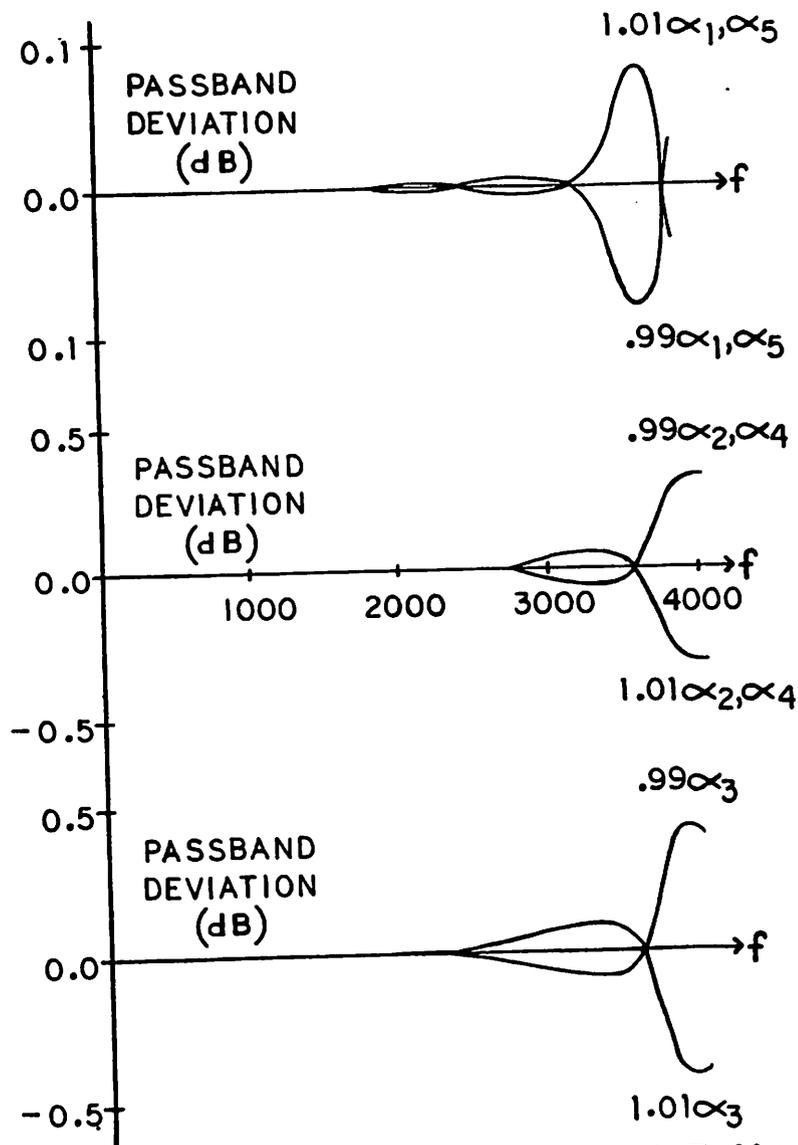


Fig. 3.5. Passband sensitivity of the DDI peaked response in Fig. 3.3 to integrator gain constants for the fifth-order switched capacitor filter without predistortion. Sample rate was 128 kHz. α_i is the reciprocal gain constant of the i^{th} integrator.

peaked response has much greater sensitivity than the nominal response of the passive RLC prototype which contradicts previously published remarks [41]-[42].

3.1.4. DDI Switched Capacitor Filters With Predistortion

The effect of finite sampling frequency is to increase the pole-Q. One way to compensate for Q-enhancement is to choose the initial continuous pole locations in such a way that the sampling effect will move them to the desired final positions as illustrated symbolically in Fig. 3.6.

Analytically, it is necessary to find the predistorted continuous pole positions, $p_d = \alpha_d + j\omega_d$, in terms of the sampled-data pole positions, p_i' , by letting $s = p_d$ in Eqn. (3.10):

$$\alpha_d = f_c \left(e^{\frac{\alpha_i'}{f_c}} \cos\left(\frac{\omega_i'}{f_c}\right) - 1 \right), \quad (3.15)$$

and

$$\omega_d = f_c e^{\frac{\alpha_i'}{f_c}} \sin\left(\frac{\omega_i'}{f_c}\right). \quad (3.16)$$

By setting $p_i' = p_c$, (i.e. the final sampled-data pole locations are equal to the desired continuous-time pole positions) the correct response is obtained. For example, Eqns. (3.15) and (3.16) have been used to calculate the element values for a predistorted fifth-order RLC ladder prototype by multiplying the poles together to form the denominator polynomial, and then using this polynomial in a Cauer-type expansion to extract the L and C values [48]. The normalized predistorted RLC network is shown in Fig. 3.7.

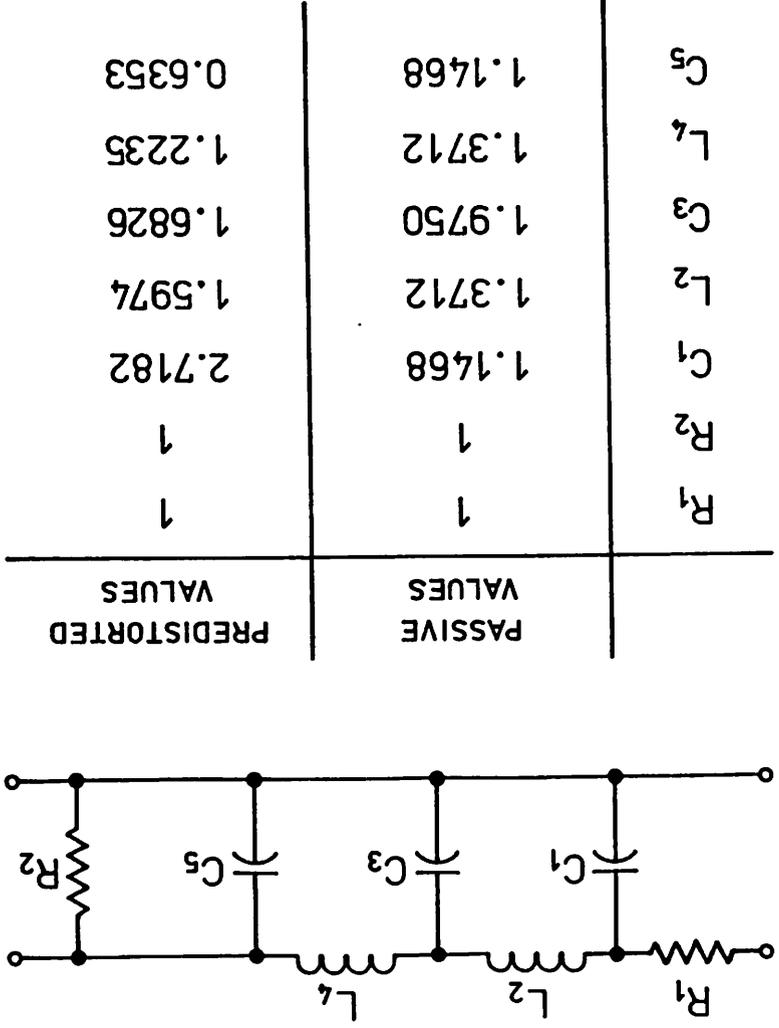


Fig. 3.7. Fifth-order doubly-terminated RLC prototype and the nominal and predistorted element values. Computations are based on a 128 kHz sampling rate.

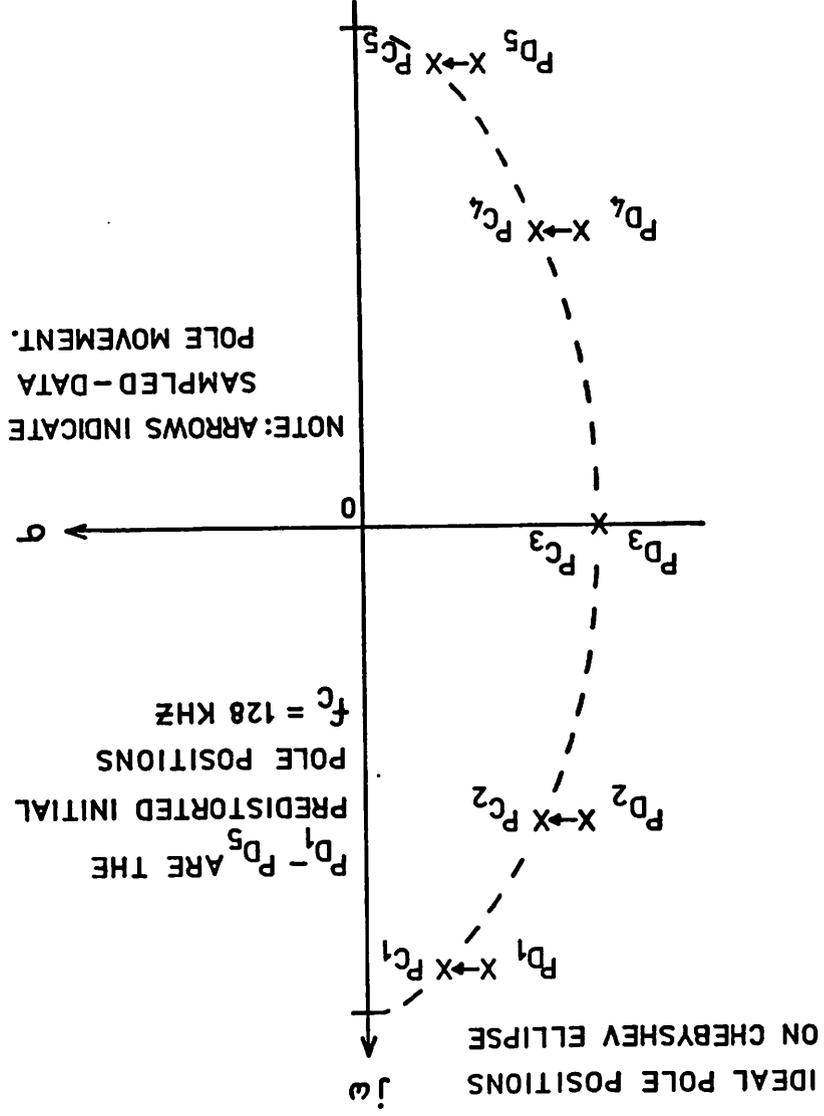


Fig. 3.6. Predistortion of the initial pole positions can be used to compensate for the Q-enhancement effect which shifts the predistorted poles to their desired positions. Sampling rate was 128 kHz.

The predistorted switched capacitor fifth-order lowpass filter has been simulated at a 128 kHz clock rate for a $\pm 1\%$ variation on all capacitor ratios with the results given in Fig. 3.8. Compared to the RLC prototype, the predistortion has increased the sensitivity by about a factor of 10. In the limit of higher clock rates, switched capacitor integrators approach continuous-time RC integrators, and the sensitivity of the switched capacitor filter approaches that of the continuous prototype. However, as the clock rate increases, the required capacitor ratios also increase resulting in an area-sensitivity tradeoff. Hence, a method of filter design which does not require predistortion is desired. By using Lossless Discrete Integrators, predistortion can be avoided in many cases, and nearly ideal sensitivity may be obtained. The LDI filter properties are described in the next two sections.

3.1.5. Type-I LDI Switched Capacitor Filters

The phasing of the switched capacitors of integrators which are connected together determines whether the frequency response of the integrator is given by $H_{1/2}(\omega)$ or $H_1(\omega)$. The two integrator loop of Fig. 3.9 demonstrates the proper switch phasing required to obtain the $H_{1/2}(\omega)$ transfer function. The signal at the output of integrator 2 is available as soon as the switched capacitor is connected to the op amp, so in order to avoid the extra half cycle of delay (and the resulting $H_1(\omega)$ response), the switches of the first integrator must be phased to immediately sample that output as shown in the figure. Therefore, the switches of adjacent integrators should be thrown in opposite directions as shown in Fig. 3.9. Integrators which are clocked to achieve this half-delay property are used in the implementation of what will be referred to as type-I LDI switched capacitor filters. A complete schematic for the type-I LDI doubly-terminated fifth-order all-pole lowpass switched capacitor ladder filter is shown in Fig. 3.10.

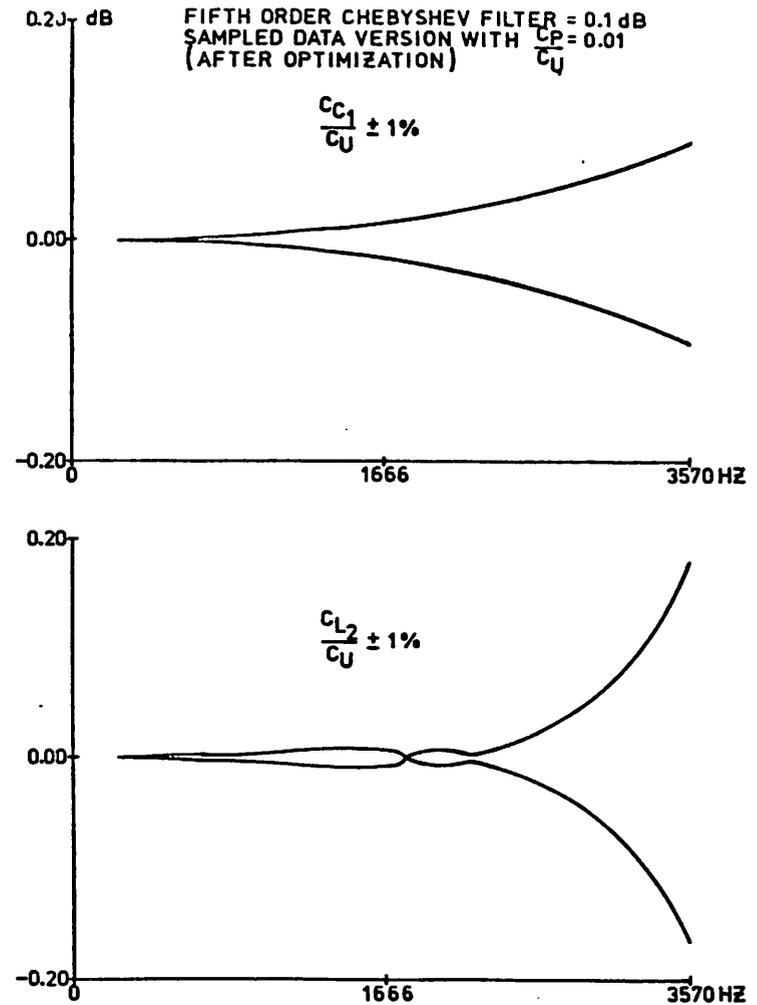


Fig. 3.8. Passband sensitivity to integrator gain constants for the fifth-order DDI switched capacitor filter with predistortion. Sampling rate was 128 kHz. Integrators 1 and 2.

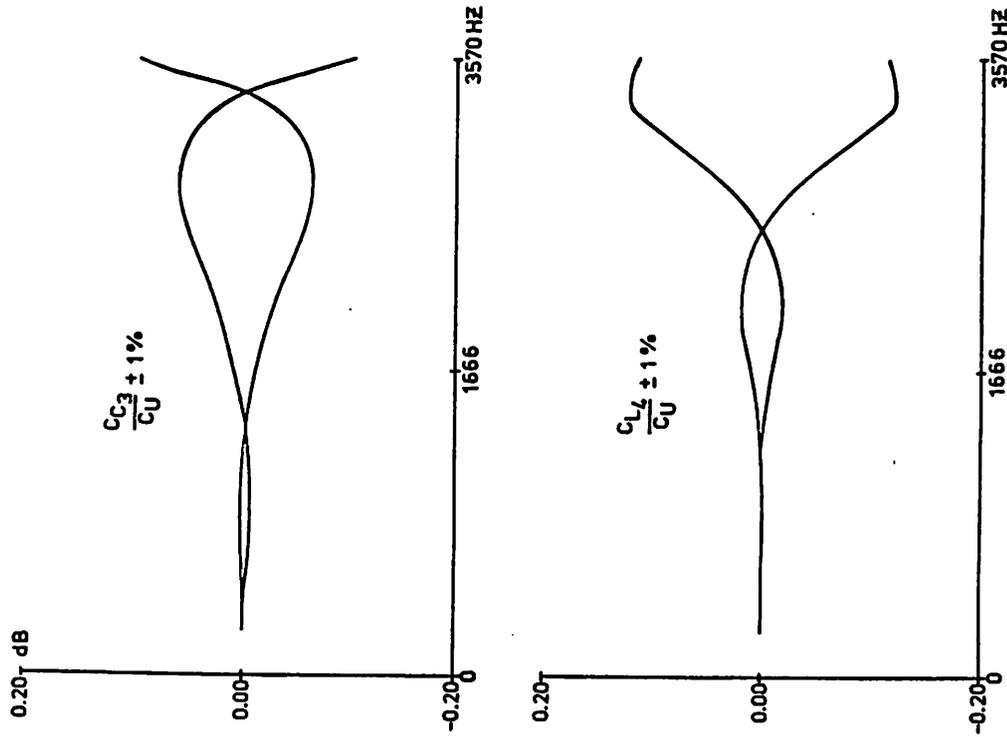


Fig. 3.8. Passband sensitivity to integrator gain constants for the fifth-order DDI switched capacitor filter with predistortion. Sampling rate was 128 kHz. Integrators 3 and 4.

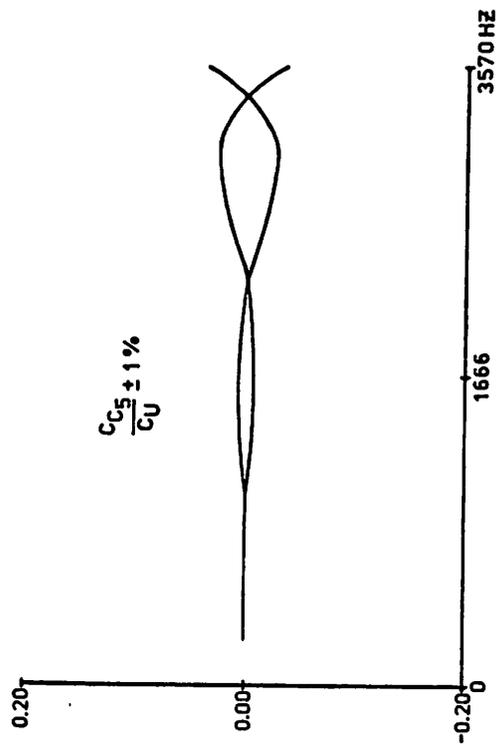


Fig. 3.8. Passband sensitivity to integrator gain constants for the fifth-order DDI switched capacitor filter with predistortion. Sampling rate was 128 kHz. Integrator 5.

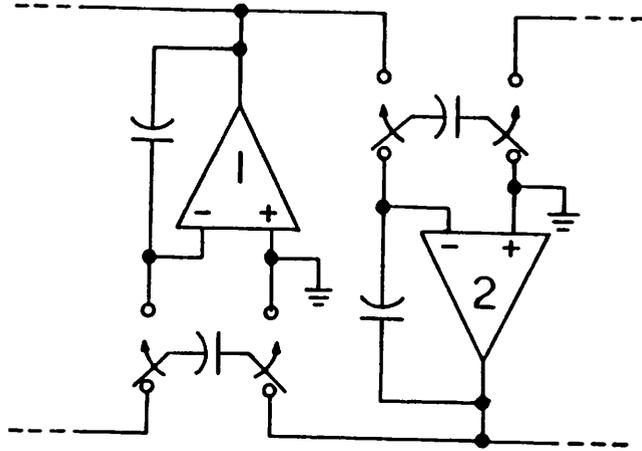


Fig. 3.9. A two-integrator loop which demonstrates the proper switch phasing required to obtain the type-I LDI integrators. Clock phases are alternated between stages.

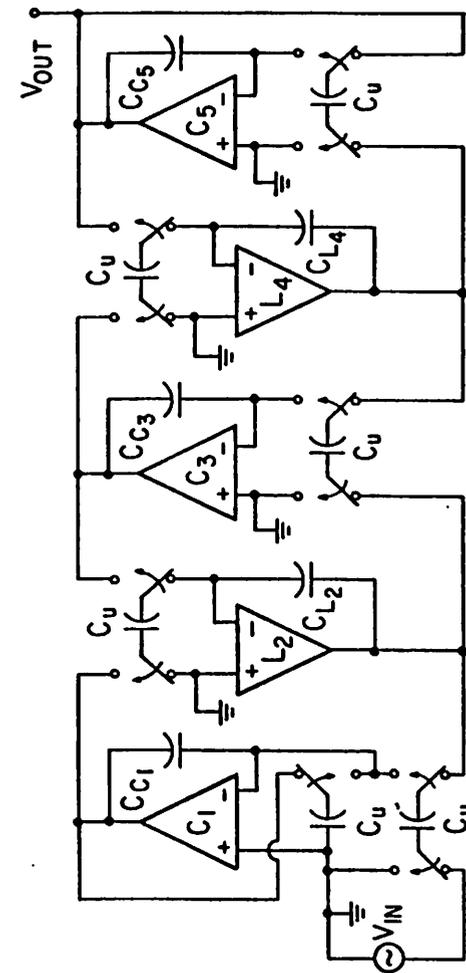


Fig. 3.10. A fifth-order lowpass type-I switched capacitor doubly-terminated ladder filter.

The passband sensitivity of the filter of Fig. 3.10 has been determined for $\pm 1\%$ variations on all capacitor ratios. As shown in Fig. 3.11, the worst-case sensitivity of the LDI network is about 5 times lower than that of an equivalent predistorted DDI network for a 128 kHz sampling frequency.

Unfortunately, the half-delay LDI realization uses the top plates of the switched capacitors as inverting integrating inputs, and therefore, the resulting frequency response is slightly in error due to the top-plate parasitic. The LDI approach described in the next section eliminates this source of error, and in addition, simplifies the clock phasing requirements.

3.1.6. Type-II LDI Switched Capacitor Filters

By using only the bottom plates of switched capacitors as integrating inputs, the errors due to top-plate parasitics are eliminated since ideally, there is no voltage change on the top plate during switching, and the bottom plate is switched between voltage sources. The noninverting integrator of Fig. 3.12(a) has a z-plane transfer function of

$$H_1(z) = \left[\frac{C_u}{C_l} \right] \left[\frac{z^{-1}}{1-z^{-1}} \right] \quad (3.17a)$$

which can be written in the frequency domain as

$$H_1(\omega) = \frac{\omega_0}{j\omega} \left[\frac{\omega T \exp(-j\omega \frac{T}{2})}{2 \sin(\omega \frac{T}{2})} \right] \quad (3.17b)$$

The circuit of Fig. 3.12(b) performs the inverting integration function with the z-plane transfer function of

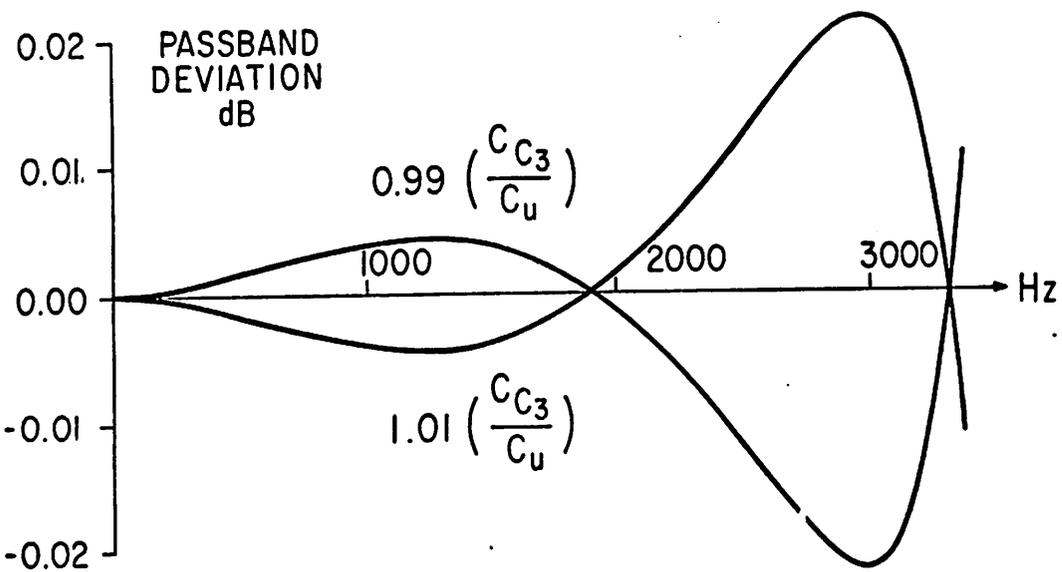


Fig. 3.11. Passband sensitivity for $\pm 1\%$ variations in $\frac{C_3}{C_u}$ which is the worst-case for the filter of Fig. 3.10. Sampling rate was 128 kHz.

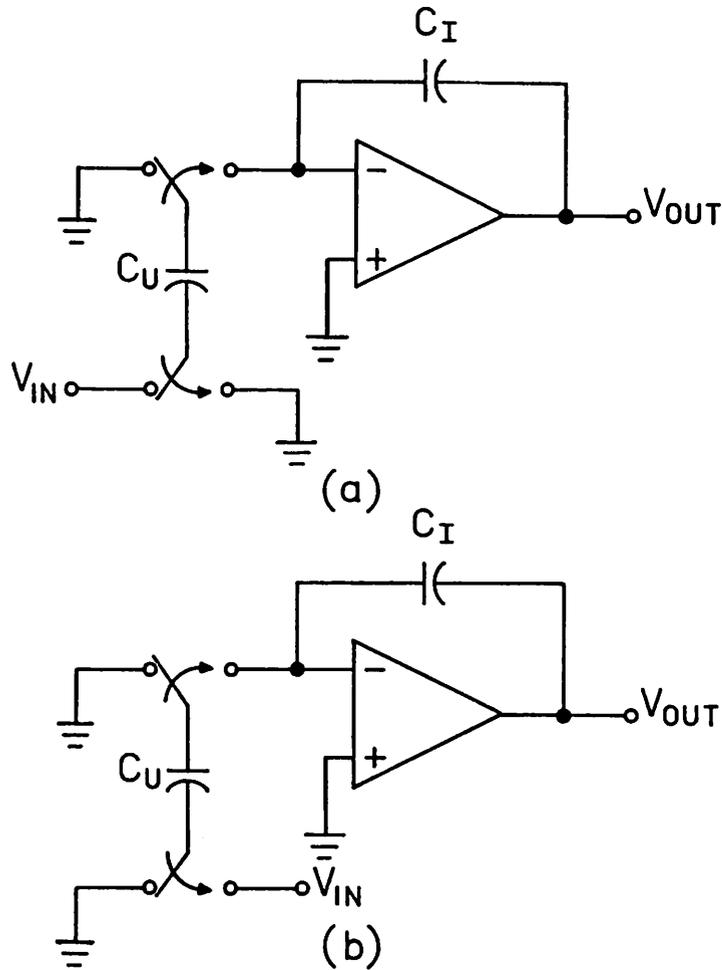


Fig. 3.12. (a) Type-II noninverting and (b) inverting switched capacitor integrators. Bottom plates are used as inputs to eliminate errors due to the top-plate parasitic.

$$H_0(z) = - \left[\frac{C_U}{C_I} \right] \left[\frac{1}{1-z^{-1}} \right] \quad (3.18a)$$

which can also be expressed as

$$H_0(\omega) = - \frac{\omega_0}{j\omega} \left[\frac{\omega T_c \exp(+j\omega \frac{T_c}{2})}{2 \sin(\omega \frac{T_c}{2})} \right] \quad (3.18b)$$

It can be seen from Eqn. (3.17b) that the noninverting integrator has excess phase-lag while the inverting integrator of Eqn. (3.18b) has a phase-lead response. These integrators will be used in the implementation of type-II LDI switched capacitor filters.

A two-integrator loop using type-II LDI integrators is shown in Fig. 3.13. By using the *same* clock phasing on both stages, the leading and lagging phase components cancel around the loop, and the correct frequency response is obtained.

The considerations for synthesis of type-II LDI filters are slightly different than for the type-I case. For the type-II designs, it is desirable to synthesize the circuits so that the signs of the integrating inputs alternate between stages, i.e., all even stages positive and all odd stages negative or vice-versa. This sign alternation allows for the same clocking on all stages, is consistent with existing ladder synthesis approaches [49]-[50], and provides a direct relationship to the DINAP simulation methods to be discussed in Appendix 3. A type-II LDI fifth-order all-pole lowpass filter is shown in Fig. 3.14. (Refer to the corresponding type-II LDI flow diagram of Fig. 2.6(c)).

Several workers are independently investigating the use of type-II LDI integrators for telecommunications applications; early indications are that excellent results will be obtained with this approach [51]-[52].

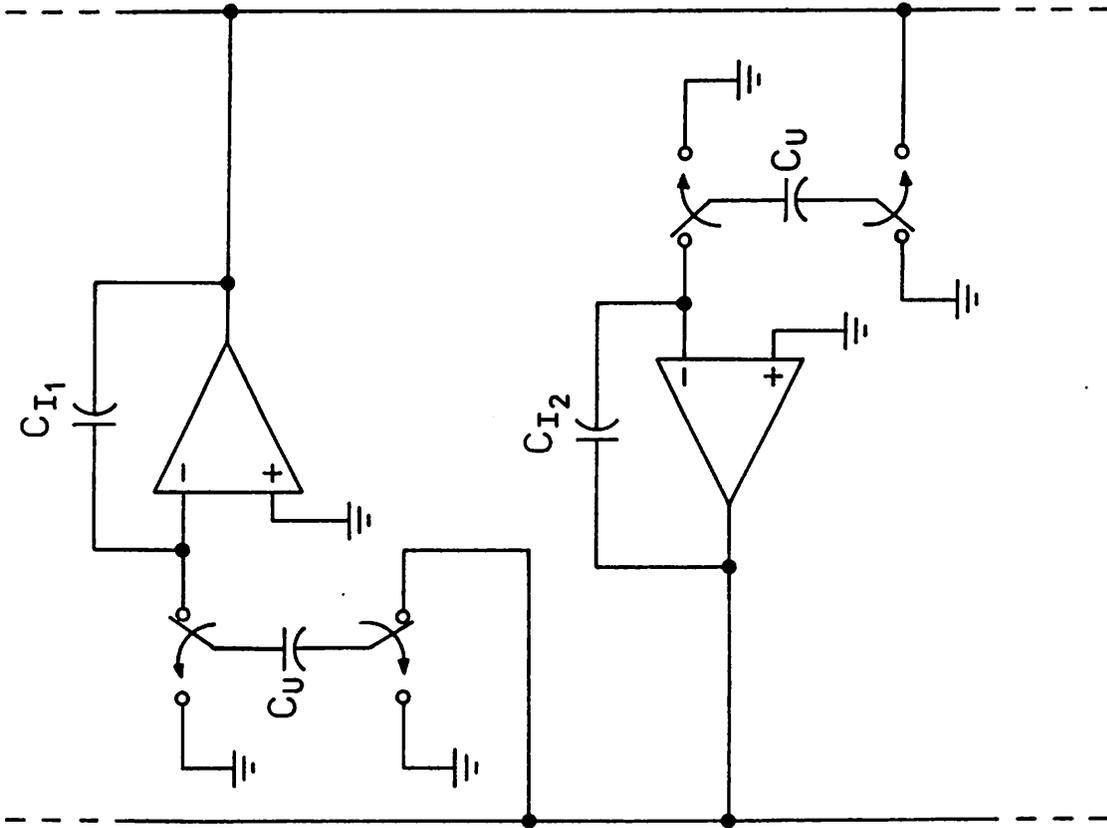


Fig. 3.13. A two-integrator loop which demonstrates the proper phasing required to obtain type-II LDI integrators. Clock phases are identical for all stages.

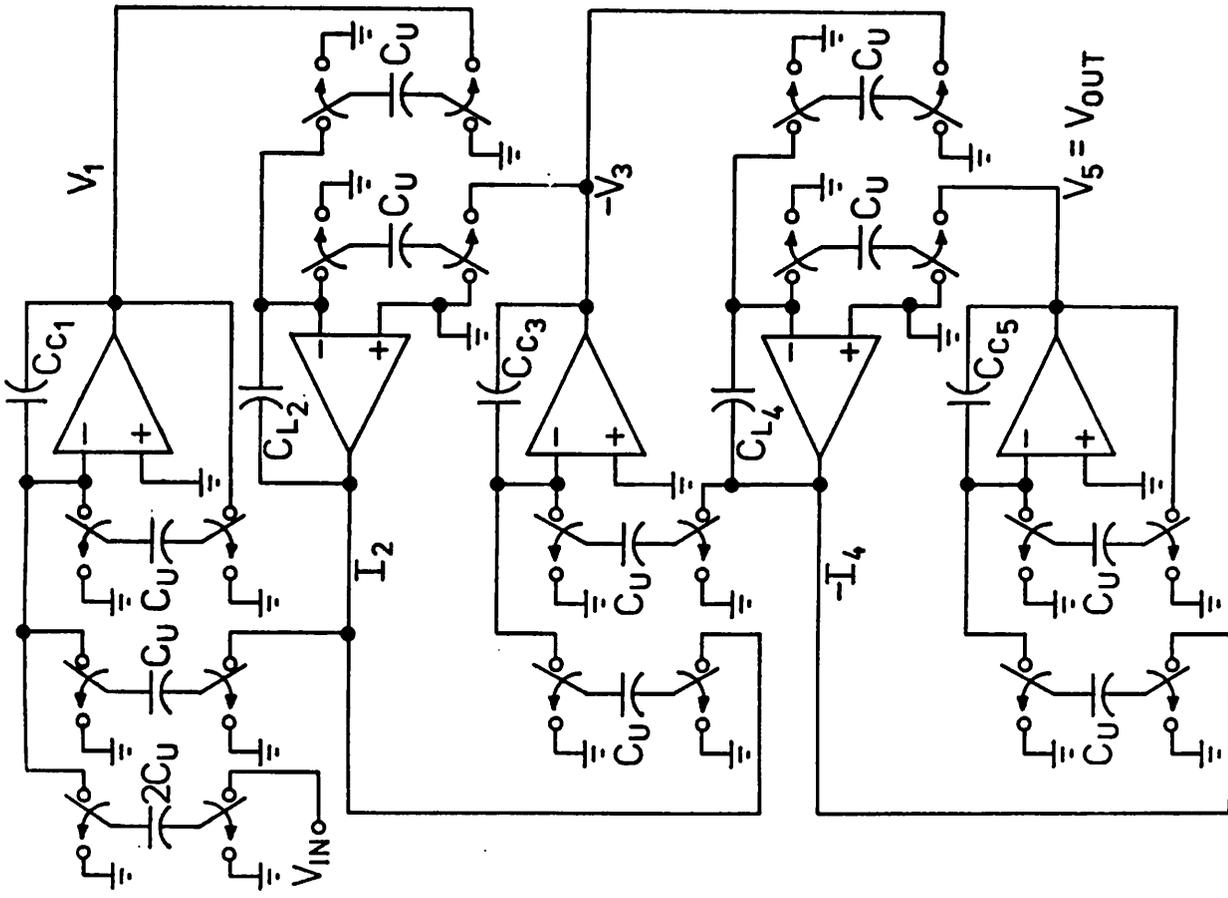


Fig. 3.14. A fifth-order lowpass type-II LDI switched capacitor doubly-terminated ladder filter.

3.1.7. LDI Switched Capacitor Filters With Predistortion

As mentioned earlier, both the DDI and LDI integrators experience a frequency dependent magnitude error. Table I shows that when the signal frequency approaches the Nyquist rate, $\frac{f_c}{2}$, the error in the integrator gain constant approaches 57%! Hence, it is obvious that for high frequency (relative to the sampling frequency) switched capacitor filters, the magnitude error must be compensated by using predistortion. The type-I LDI transfer function of Eqn. (3.6) maps a continuous s-plane pole into a sampled-data s-plane pole by the transformation

$$s \rightarrow f_c \left[z^{1/2} - z^{-1/2} \right] = 2f_c \sinh \left[\frac{s'}{2f_c} \right]. \quad (3.19)$$

With $s = -\alpha_d + j\omega_d$, and $s' = -\alpha_i' + j\omega_i'$, Eqn. (3.19) is solved to obtain:

$$\alpha_d = 2f_c \cos \left[\frac{\omega_i'}{2f_c} \right] \sinh \left[\frac{\alpha_i'}{2f_c} \right], \quad (3.20)$$

and

$$\omega_d = 2f_c \sin \left[\frac{\omega_i'}{2f_c} \right] \cosh \left[\frac{\alpha_i'}{2f_c} \right]. \quad (3.21)$$

By letting $p_i' = -p_c$, Eqns. (3.20) and (3.21) can be used to calculate the predistorted LDI pole positions. This predistortion technique can also be used to compensate for other types of nonidealities such as finite op amp gain.

3.1.8. Switched Capacitor Filters with Multiple Sampling Rates

In sampled-data systems such as switched capacitor filters, one of the most difficult practical problems is the requirement for a continuous-time antialiasing prefilter. The prefilter specifications are reduced by sampling at many times the passband frequencies, but unfortunately, this higher sampling rate results in larger capacitor ratios. An optimum solution to this problem is to operate the first stage(s) of the filter at a very high sampling rate to ease the prefilter requirements, and to operate the other stages(s) at a lower clock rate in order to simultaneously reduce the silicon area requirements.

This approach has been verified by DINAP simulation for a third-order Chebyshev lowpass filter with a 3.4 kHz cutoff and 0.1 dB passband ripple. In Fig. 3.15, the first stage is switched at 1.024 MHz, and the second and third stages are switched at 128 kHz. The switches are operated to obtain zero excess phase shift around all interior two-integrator loops, which requires that the second stage in this example has its two switched capacitors operating at two different sampling rates as shown in the figure. The DINAP simulations shown in Fig. 3.16 agree closely with the expected values.

This technique can also be used to provide a high sampling frequency stage(s) at the output of the switched capacitor filter so that continuous-time postfiltering, if necessary, becomes easier.

3.2. Passive Component Nonideal Effects

In this section, the effects of nonidealities associated with the passive filter elements will be considered [25],[46].

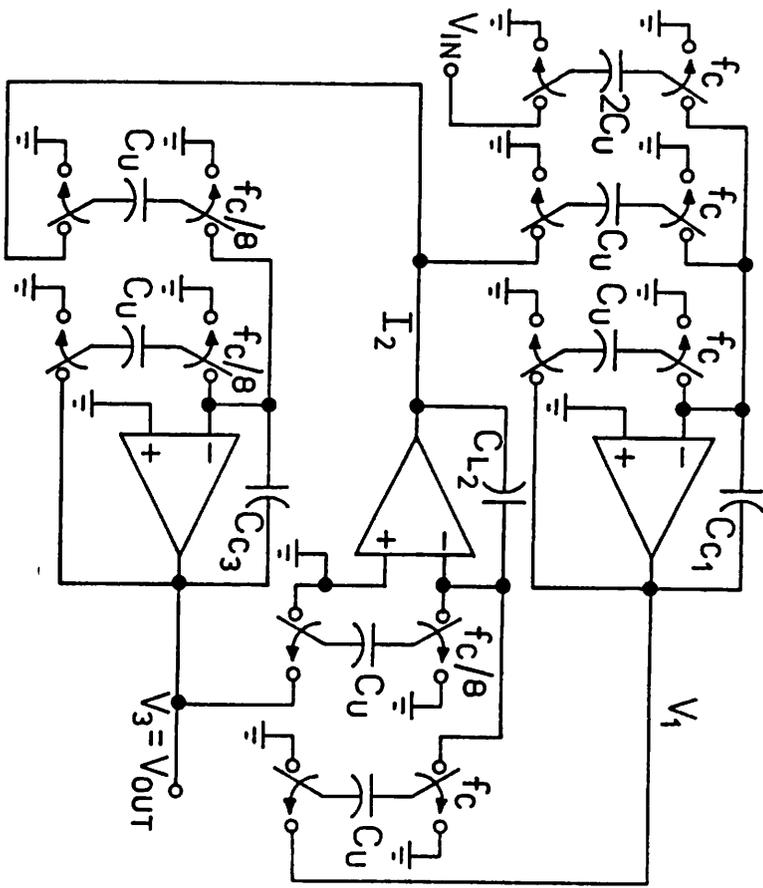


Fig. 3.15. A third-order lowpass type-II LDI switched capacitor filter with two different sampling frequencies.

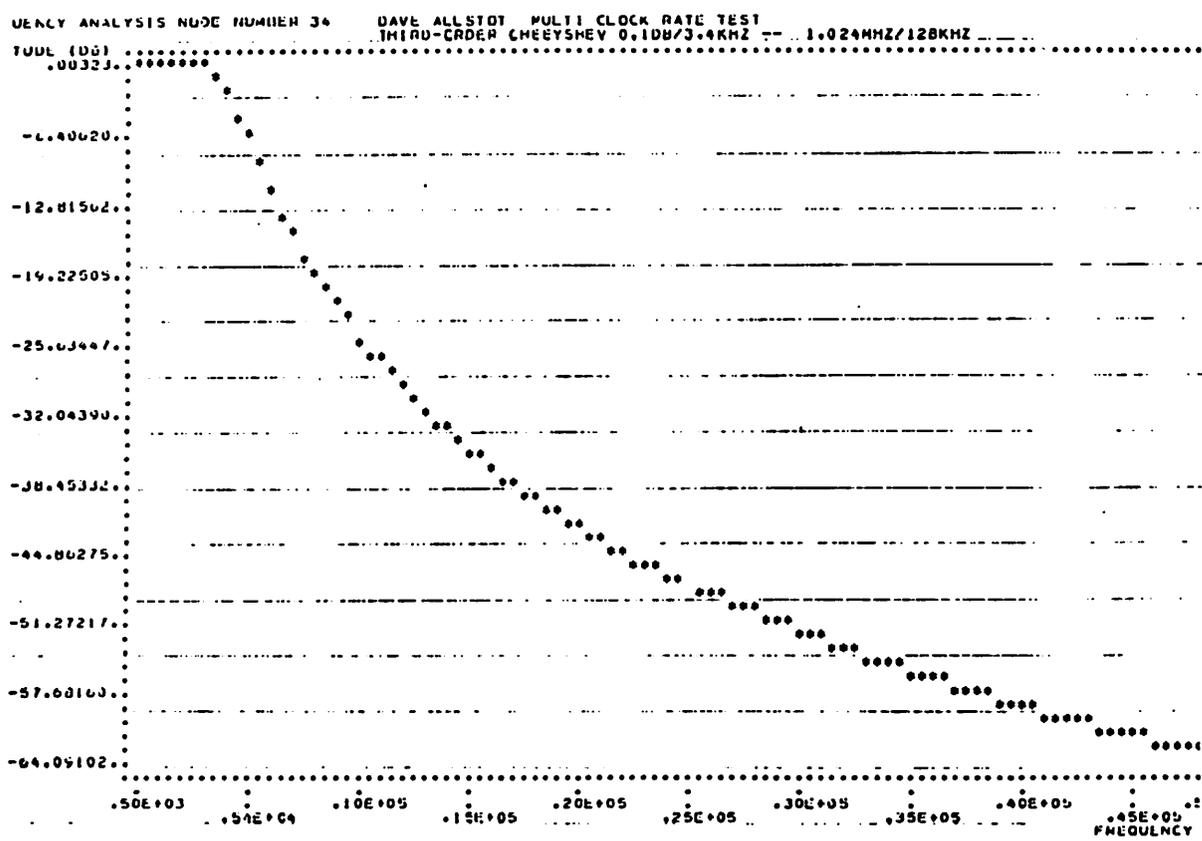


Fig. 3.16. (a) The DINAP response for the circuit of Fig. 3.15 with 128 kHz and 1.024 MHz sampling rates.

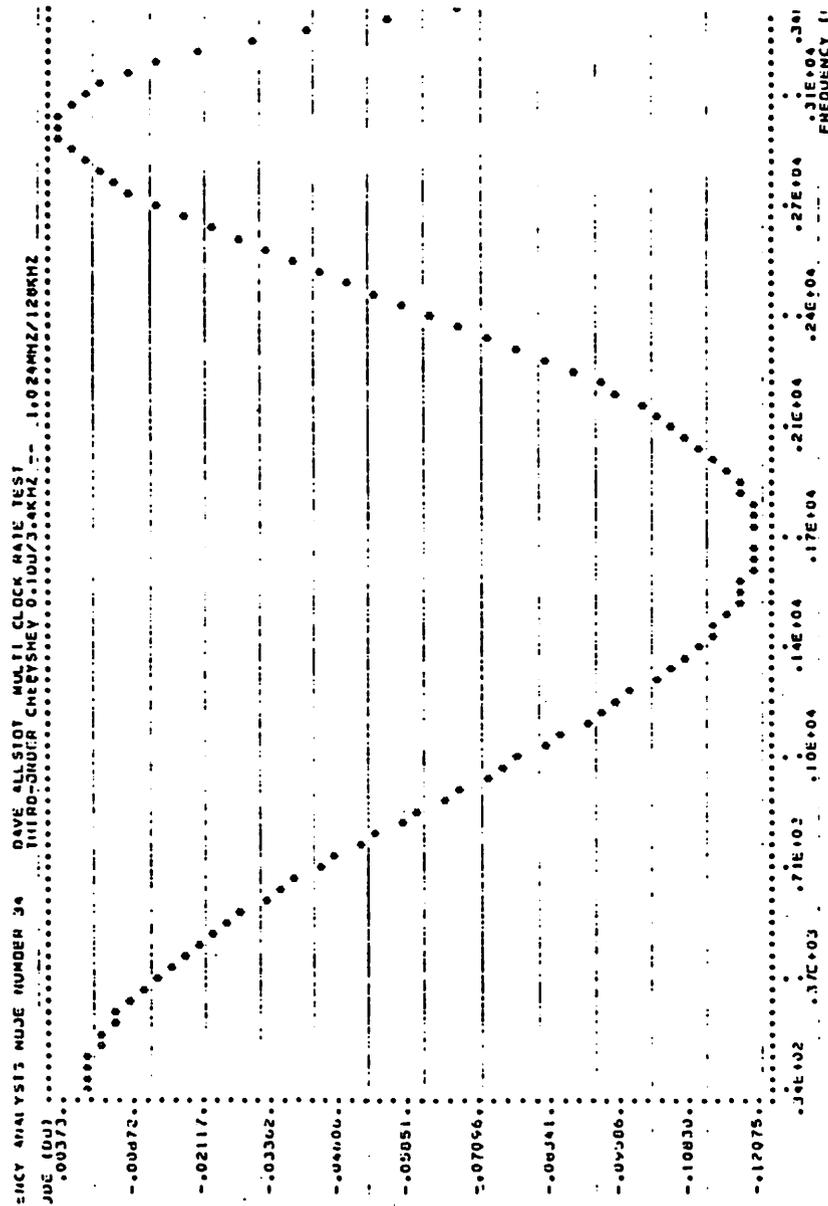


Fig. 3.16. (b) The DINAP passband response for the circuit of Fig. 3.15.

3.2.1. MOSFET Channel (Switch) Resistance

Finite MOSFET switch resistance limits the rate at which charge is transferred through a switched capacitor circuit. In order to isolate this effect from op amp settling effects (which will be shown to be dominant), it will be assumed that the op amp in the switched capacitor integrator of Fig. 3.17(a) is ideal. During the sampling interval, ϕ_1 , the charging network can be represented as the series $R_{ave}C_u$ combination shown in Fig. 3.17(b) where R_{ave} is the average switch resistance. For an input voltage of ΔV_{in} , the voltage on C_u at the end of the sampling interval is

$$V_u(T_1) = \Delta V_{in} (1 - e^{-\frac{T_1}{R_{ave}C_u}}) \quad (3.22)$$

where T_1 is the "on" time of ϕ_1 . The charge on C_u after ϕ_1 is

$$Q_u(T_1) = C_u V_u(T_1) = C_u \Delta V_{in} (1 - e^{-\frac{T_1}{R_{ave}C_u}}). \quad (3.23)$$

During the integration phase, ϕ_2 , the op amp attempts to transfer the charge from C_u to C_1 as indicated in Fig. 3.17(c). The voltage on C_u after the integration interval, T_2 , is

$$V_u(T_2) = V_u(T_1) e^{-\frac{T_2}{R_{ave}C_u}} \quad (3.24a)$$

with a charge of

$$Q_u(T_2) = C_u V_u(T_2) = C_u V_u(T_1) e^{-\frac{T_2}{R_{ave}C_u}}. \quad (3.24b)$$

The total change in charge on C_u during one complete clock cycle, $\Delta Q_u = Q_u(T_1) - Q_u(T_2)$, is given by

$$\Delta Q_u = C_u \Delta V_{in} (1 - e^{-\frac{T_1}{R_{ave}C_u}}) (1 - e^{-\frac{T_2}{R_{ave}C_u}}). \quad (3.25)$$

Since $\Delta V_{out} = -\frac{\Delta Q_u}{C_I}$, the integrator gain is

$$\frac{\Delta V_{out}}{\Delta V_{in}} = - \left[\frac{C_u}{C_I} \right] (1 - e^{-\frac{T_1}{R_{ave} C_u}}) (1 - e^{-\frac{T_2}{R_{ave} C_u}}). \quad (3.26)$$

Hence, incomplete charge transfer due to non-zero switch resistance is equivalent to a capacitor ratio error. If the values of T_i and $R_{ave} C_u$ are chosen so that the error is less than 1%, Eqn. (3.26) suggests that T_i should be greater than 5.3 $R_{ave} C_u$ time constants, while for a 0.1% error, 7.6 time constants are required. For the designs of this dissertation, the T_i intervals were typically 75 time constants making this effect negligible in comparison to settling errors which will be described later.

3.2.2. MOSFET Nonlinearity and Threshold Voltage Effects

Since the MOS transistors are being used as charge switches, nonlinearity in the channel resistance is unimportant provided that the charging and discharging intervals are sufficiently long. However, the threshold voltage of the switches must be carefully considered. As an illustration of this point, suppose in Fig. 3.17(a) that C_u is initially at 0 volts when ϕ_1 and V_{in} are connected to V_{DD} . When V_u has risen to within a threshold voltage of V_{DD} , the switch transistor turns off. Hence, the input signal may be clipped, resulting in a decrease in the dynamic range of the filter. In single channel MOS technology, bootstrapped clock drivers can be used to overcome this problem, and in CMOS technology, transmission gates can be used to obtain full voltage swings.

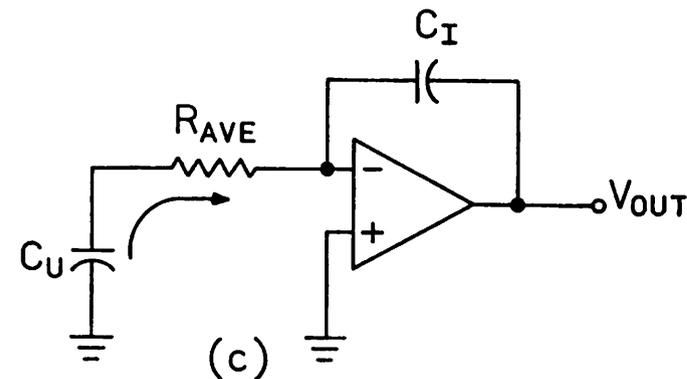
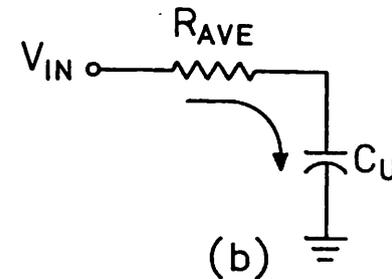
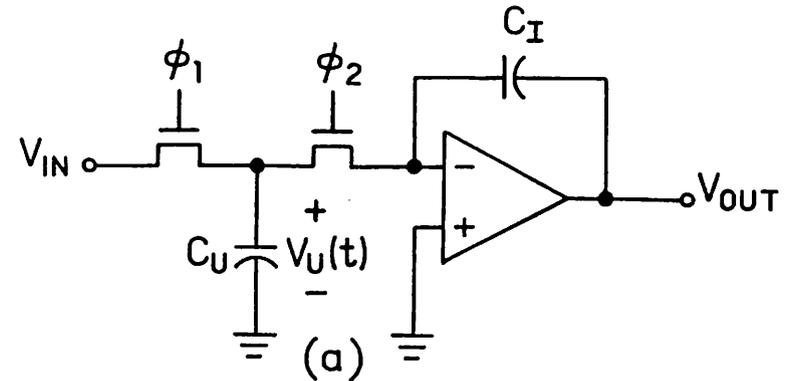


Fig. 3.17. (a) A switched capacitor integrator, and the RC circuit models for (b) the sampling phase, and (c) the integration phase.

3.2.3. MOSFET Channel-Resistance Thermal Noise

Noise will be considered in Chapter 4.

3.2.4. Capacitively-Coupled Clock Feedthrough

A switched capacitor integrator is shown in Fig. 3.18(a) including the gate-source and gate-drain capacitances for the MOSFET switches. The ϕ_1 clock signal is effectively isolated from the op amp by M_2 so that it does not affect the output. However, as shown in Fig. 3.18(b), C_{GD2} couples a portion of ϕ_2 onto the output which appears as a DC voltage with its magnitude dependent on when the output is sampled by the next stage [53]-[54]. For example, if the output is sampled on ϕ_2 (as in type-I LDI filters), the output voltage is somewhere between 0 volts and $\frac{C_{ox2}V_{DD}}{2C_1}$. If the output is sampled after ϕ_1 , the rising and falling feedthrough components approximately cancel, and the output DC offset voltage is very small. For the metal-gate NMOS process used in the prototype circuits of Chapters 5 and 6, the clock feedthrough step size was about 75 mV. Other workers have observed less than 10 mV of clock feedthrough for silicon-gate NMOS realizations of switched capacitor filters [57].

3.2.5. Junction and Surface Leakage Currents

Since the leakage currents are integrated by the switched capacitor integrators, the circuit can eventually saturate. To prevent this from happening, it is necessary to provide a discharge path for I_L as in Fig. 3.19(a) where a switched capacitor resistor is connected in a negative feedback loop between the input and the output. This feedback path places a negative charge on C_u during ϕ_1 which resets the integrator during ϕ_2 as shown in Fig. 3.19(b). The effect of this leakage current is to cause a DC offset voltage at the integrator output with its magnitude dependent

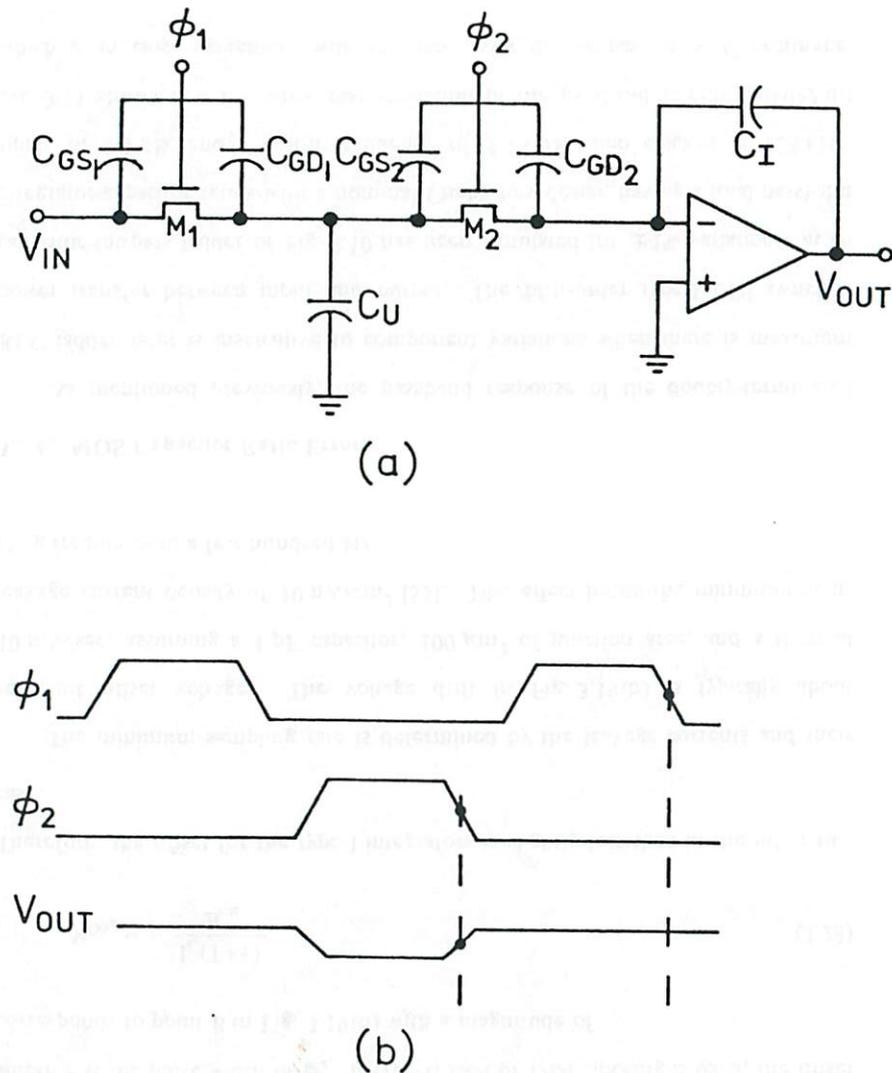


Fig. 3.18. (a) A switched capacitor integrator with parasitic switch capacitances; (b) signal waveforms showing clock feedthrough.

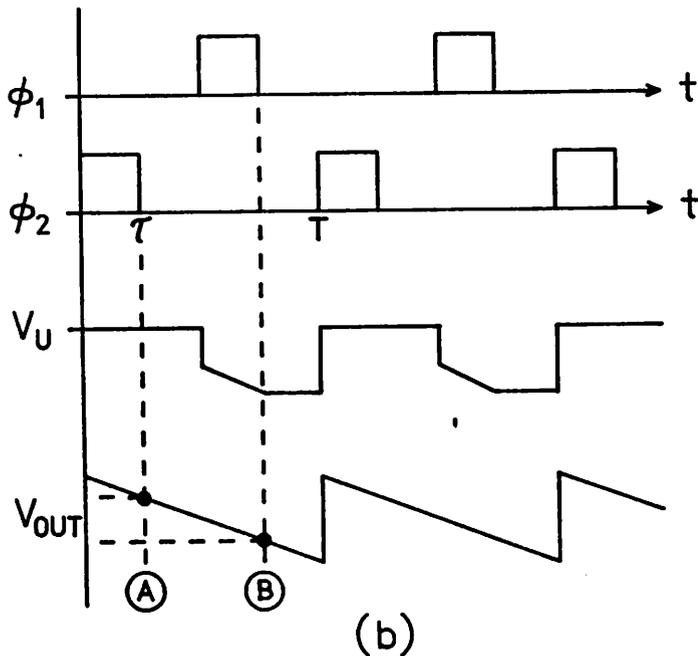
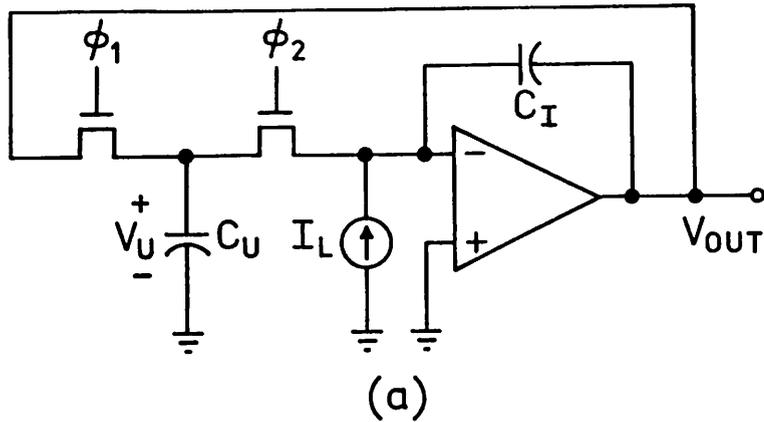


Fig. 3.19. (a) A switched capacitor integrator with negative feedback to stabilize against the leakage current, and (b) the corresponding voltage waveforms. Effective offset depends on sampling instant at the output.

on when the output is sampled. If the output is sampled at the end of ϕ_2 as in the type-I LDI integrators, the offset corresponding to time A in Fig. 3.19(b) is

$$V_{OS_A} = -\frac{I_L \tau}{C_U}, \quad (3.27)$$

where τ is the pulse width of ϕ_2 . If type-II LDI or DDI clocking is used, the offset corresponds to point B in Fig. 3.19(b) with a magnitude of

$$V_{OS_B} = -\frac{I_L(T+\tau)}{2C_U}. \quad (3.28)$$

Therefore, the offset for the type-I integrators is slightly less than in the other two cases.

The minimum sampling rate is determined by the leakage currents and their resultant offset voltages. The voltage drift in Fig. 3.19(b) is typically about 10 mV/sec, assuming a 1 pF capacitor, $100 \mu\text{m}^2$ of junction area, and a thermal leakage current density of 10 nA/cm^2 [55]. This effect limits the minimum sampling frequency to a few hundred Hz.

3.2.6. MOS Capacitor Ratio Errors

As mentioned previously, the passband response of the doubly-terminated RLC ladder filter is insensitive to component variations when there is maximum power transfer between input and output. The fifth-order type-I LDI switched capacitor lowpass ladder of Fig. 3.10 has been simulated for $\pm 1\%$ variations on all integrator capacitor ratios with a nominal Chebyshev design having a total passband ripple of 0.1 dB, and a cutoff frequency of 3.4 kHz when clocked at 128 kHz. Fig. 3.11 shows that the worst-case deviation in the passband is only $\pm 0.022 \text{ dB}$ which is in close agreement with the sensitivity of the passive RLC prototype.

Previous work has shown that monolithic capacitors can easily be matched to within a few tenths of a percent ratio accuracy [21], and hence, the passband variations due to capacitor ratio errors will be extremely small for monolithic MOS realizations.

3.2.7. MOS Capacitor Temperature Coefficient

The temperature-dependent MOS capacitance value can be linearly approximated about a nominal temperature, T_0 , by

$$C(T) = C(T_0)(1 + \alpha(T - T_0)) \quad (3.29)$$

where the temperature coefficient, α , is typically 25 ppm/°C [21]. The temperature-dependent capacitance ratio is therefore

$$\frac{C_u(T)}{C_l(T)} = \frac{C_u(T_0)(1 + \alpha(T - T_0))}{C_l(T_0)(1 + \alpha(T - T_0))} = \frac{C_u}{C_l} \quad (3.30)$$

showing that first-order temperature variations cancel, leaving the monolithic MOS capacitance ratio independent of temperature.

3.2.8. MOS Capacitor Voltage Coefficient

The voltage-dependent monolithic MOS capacitance expressed about a nominal operating voltage, V_0 , is

$$C(V) = C(V_0)(1 + \beta(V - V_0)) \quad (3.31)$$

where the voltage coefficient, β , is typically -10 ppm/volt (metal over n^+), and the voltage-dependent capacitance ratio is

$$\frac{C_u(V_{in})}{C_l(V_{out})} = \frac{C_u(V_0)(1 + \beta(V_{in} - V_0))}{C_l(V_0)(1 + \beta(V_{out} - V_0))} \quad (3.32)$$

For typical operating voltages, this error is negligible. For example, if $V_0 = 0$ volts, $V_{in} = -5$ volts, and $V_{out} = 5$ volts, the resulting ratio error is only 0.01%.

3.2.9. Parasitic Capacitances

If DDI or type-I LDI configurations are used, it is important to consider the parasitic capacitances associated with the inverting (upper as drawn) and noninverting (lower as drawn) plates of the switched capacitor, C_u , labelled C_A and C_B , respectively as shown symbolically in Fig. 3.20(b). First, consider the bottom-plate parasitic, C_B , which will be charged to V_2 when the switches are thrown to the left. When the switches are subsequently thrown to the right, C_B is discharged to ground, and thus has no effect on the charge stored on C_l . On the other hand, when the switches are to the left, the top-plate parasitic, C_A , is charged to V_1 , and when the switches are thrown to the right, C_A is discharged onto the integrating capacitor, C_l . Hence, C_A contributes an error charge whose effect must be minimized in the DDI or type-I LDI filter design.

Figure 3.20(c) shows the simulated effect that the top-plate parasitic capacitance has on the frequency response of the fifth-order Chebyshev type-I LDI lowpass filter. When $C_A = 0$, the ideal response is obtained as in the upper trace. (All other parameters are assumed ideal.) The lower trace of Fig. 3.20(c) is for the case when $C_A = 0.01C_u$. In this case, there is a DC gain error of 0.25 dB, and a slight peaking in the response of 0.05 dB. The amount of this peaking error which can be tolerated for a given application usually determines the minimum size of C_u relative to the top-plate parasitic. For typical monolithic MOS lowpass realizations, C_u ranges from about 0.5 to about 2.5 pF. (For highpass structures with large capacitor ratios, C_u may be as small as 0.02-0.10 pF [51],[56]).

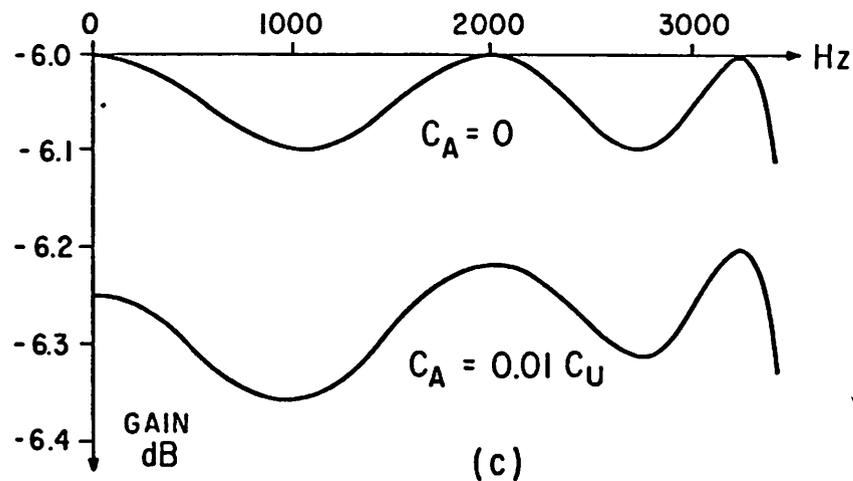
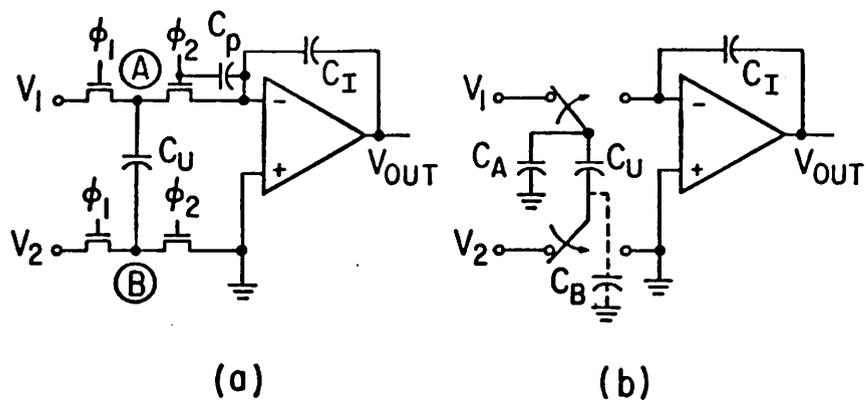


Fig. 3.20. (a) A type-I switched capacitor differential integrator, and (b) a symbolic representation showing parasitics; (c) effects of top-plate parasitic on response of fifth-order Chebyshev lowpass filter. Sampling rate was 128 kHz.

The top-plate parasitic also results in a multiplication of the amplifier offset voltage. In Fig. 3.20(b), suppose that $V_1=0$, $V_2=V_{out}$, and that the amplifier has an offset voltage of V_{OS} . For this situation, the DC offset voltage at the integrator output is $V_{OS}(1+\frac{C_A}{C_U})$. If C_U becomes very small relative to C_A , this multiplication can significantly increase the effective output offset voltage, although this effect is not usually important if V_{OS} is small.

3.3. Nonidealities Associated with the Active Components

This section will cover some of the more important effects associated with the operational amplifiers.

3.3.1. Operational Amplifier DC Open-Loop Gain

A switched capacitor integrator is implemented using a differential amplifier, which in the case of Fig. 3.21, has an open-loop DC gain of A_o . Ideally, A_o is infinite, and the integrator has a pole at the origin in the s-plane as shown in Fig. 3.21(b). However, if A_o is finite, the effect is to produce a lossy integrator by moving the pole away from the imaginary axis as indicated by the arrow. Fig. 3.21(c) shows the simulated (DINAP) effect that op amp DC gain variations have on the frequency response of a fifth-order Chebyshev lowpass filter which has the nominal response of Fig. 3.20(c). In the lower trace, all five op amps have an open-loop gain of 100. In this case, the filter has a DC gain error of 0.22 dB with a passband droop of 0.09 dB due to the poles being pushed away from the imaginary axis. In the upper trace of Fig. 3.21(c), all five op amps have an open loop gain of 1000, and the filter response shows a DC gain error of only 0.02 dB. Hence, it can be concluded that op amps with gains of 1000 can be used to realize switched capacitor lowpass ladder filters with very accurate responses when the pole Q's are

small (<10). For high-Q realizations, the op amp DC gain is required to be proportionately higher. This will be treated in greater detail in Chapter 6.

If operational amplifiers with a DC gain of less than 1000 are used, predistortion techniques similar to those presented in Section 3.1.4 can be used to compensate the response for the expected gain errors. However, the amplifier gain should not be made arbitrarily small since the sensitivity of the pole positions to gain is approximately $-\frac{1}{A_o}$, and therefore, for small A_o , typical processing variations would make it difficult to obtain a reproducible response.

3.3.2. Operational Amplifier DC Offset Voltage

Fig. 3.14 shows that each switched capacitor integrator in the active ladder configuration is embedded in a negative feedback loop, which defines a stable bias point even in the presence of op amp DC offset voltages. In terms of the overall filter, the individual integrator offsets contribute to a DC offset voltage at the output of the filter which is given by

$$V_{os} = \frac{\sum_{i=1}^n V_{os_i}}{2} \quad (3.33)$$

where n is the total number of integrating stages, and V_{os_i} is the DC offset voltage of the i^{th} stage. The offset for each integrator depends on a number of factors including leakage currents, clock feedthrough, clock phasing, top-plate parasitics, and the individual amplifier offsets as described earlier.

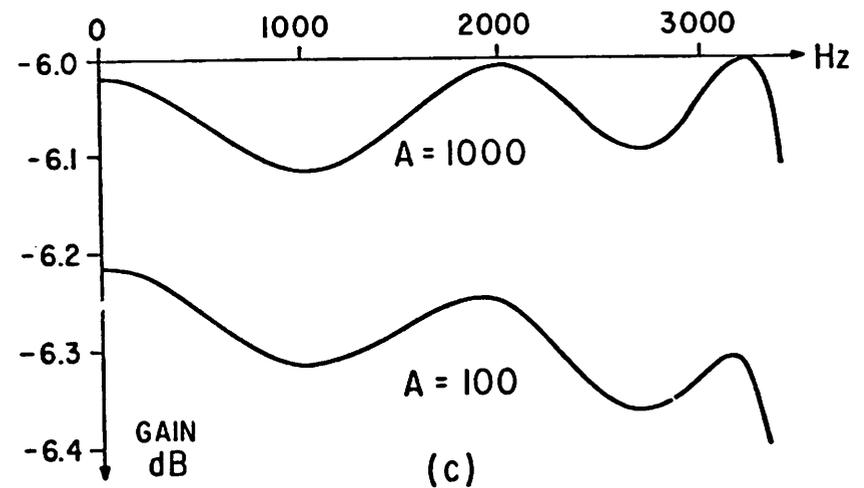
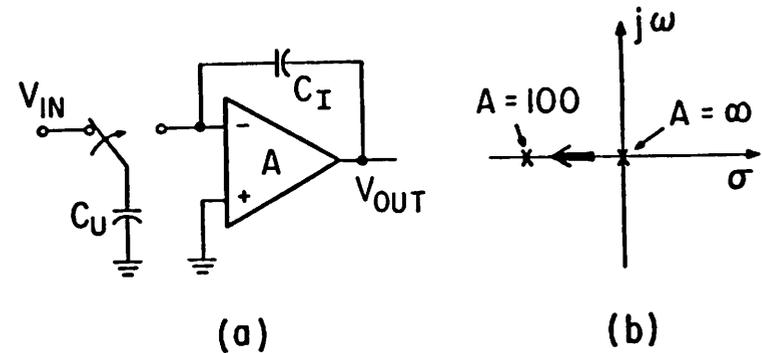


Fig. 3.21. (a) Switched capacitor integrator with finite op amp gain; (b) integrator pole position versus A_o ; (c) effect of open-loop DC gain on response of fifth-order Chebyshev lowpass filter. Sampling rate was 128 kHz.

3.3.3. Common-Mode Range and CMRR

In switched capacitor integrators, the positive input terminal of the differential amplifier is always connected to a DC bias voltage. Hence, there is no steady-state common-mode input signal, and therefore the input common-mode range and CMRR are not important parameters.

3.3.4. Amplifier Slew-Rate

The required op amp slew-rate performance is determined by several different factors: (1) The maximum rate of change of the integrator output signal; (2) the sampling frequency; (3) the duty cycle of the clocks, and (4) the clock phasing which determines when the output is sampled. The switched capacitor integrator of Fig. 3.22 samples the input during ϕ_1 and integrates during ϕ_2 as shown in the timing diagram. It will be assumed that V_{out} is sampled at the end of ϕ_2 (which represents the worst-case) so that the total time available for slewing and settling is τ , where $\tau = k_d T$ depends on the duty cycle. Neglecting sampling for the moment, the output signal can be represented as

$$V_{out}(t) = V_p \sin(\omega t) \quad (3.34)$$

which has a maximum rate of change at ω_o of

$$\left| \frac{dV_{out}(t)}{dt} \right|_{max} = \omega_o V_p \quad (3.35)$$

Therefore, the maximum change in the output during one clock period is dependent on the sampling frequency and is given by

$$\left| \Delta V_{out} \right|_{max} = \omega_o V_p T = \frac{\omega_o V_p}{f_c} \quad (3.36)$$

As shown in Fig. 3.22(b), the total available response time, τ , consists of a slewing time, t_{slew} , and a settling time, t_{set} . Since the settling time is approximately constant, the allowable slewing time is

$$t_{slew} = \tau - t_{set} = \frac{k_d}{f_c} \left[1 - \frac{t_{set}}{\tau} \right] \quad (3.37)$$

Hence, the required op amp slew-rate is

$$SR = \frac{\left| \Delta V_{out} \right|_{max}}{t_{slew}} = \frac{\omega_o V_p}{k_d \left[1 - \frac{t_{set}}{\tau} \right]} \quad (3.38)$$

where it is assumed that $\tau > t_{set}$. For example, for a 3.4 kHz signal with a 3 volt peak, $\omega_o V_p = 0.064$ volts/ μ sec. If $k_d = 0.25$ (25% duty cycle), and half of the integration time is allowed for settling, $\frac{t_{set}}{\tau} = 0.5$, then the required slew-rate is 0.51 volts/ μ sec. The prototype filters to be described in Chapters 5 and 6 used an NMOS operational amplifier with a measured slew-rate of 1 volt/ μ sec.

3.3.5. Amplifier Settling Response

Consider a switched capacitor integrator which uses a two-pole amplifier with a low frequency gain of A_o and a dominant pole at p_1 :

$$A(s) = \frac{A_o}{\left[1 + \frac{s}{p_1} \right] \left[1 + \frac{s}{p_2} \right]} \quad (3.39)$$

During the sampling interval, the capacitor C_1 stores the output voltage, and the op amp is an open-loop condition. During the integration phase, the circuit can be modelled as a charge multiplier responding to a step input. The transfer function

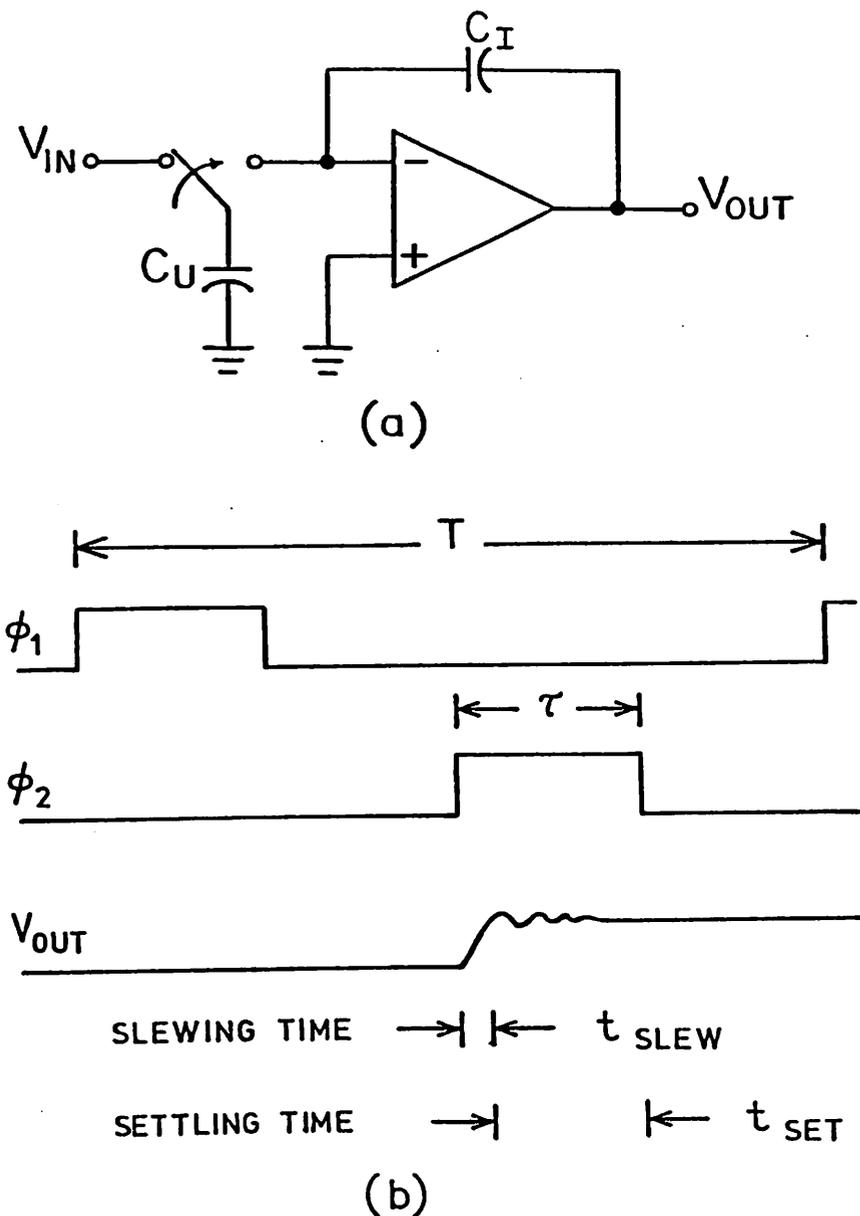


Fig. 3.22. (a) A switched capacitor integrator, and (b) the voltage waveforms defining the slewing and settling times.

for the circuit of Fig. 3.23(a) is

$$H(s) = \frac{-\left[\frac{C_U}{C_I}\right]}{1 + \frac{1}{T(s)}}, \quad (3.40)$$

where $T(s)$ is the loop-gain of the charge multiplier,

$$T(s) = \frac{\left[\frac{C_I A_o}{C_U + C_I}\right]}{\left[1 + \frac{s}{p_1}\right] \left[1 + \frac{s}{p_2}\right]}. \quad (3.41)$$

The step response of the circuit depends on the location of the closed-loop poles in Eqn. (3.40) which are derived as

$$s_{1,2} = -\left[\frac{p_1 + p_2}{2}\right] \pm \frac{j}{2} \left[4p_1 p_2 (1 + T_o) - (p_1 + p_2)^2\right]^{1/2}, \quad (3.42)$$

where T_o is the low frequency loop-gain,

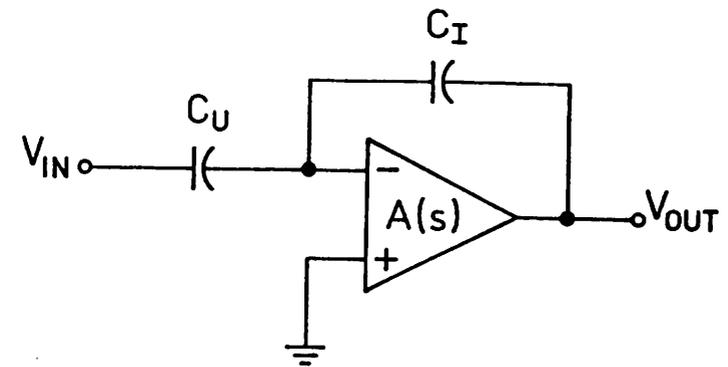
$$T_o = \frac{C_I A_o}{C_U + C_I}. \quad (3.43)$$

A root-locus plot is shown in Fig. 3.23(b). The poles become complex when

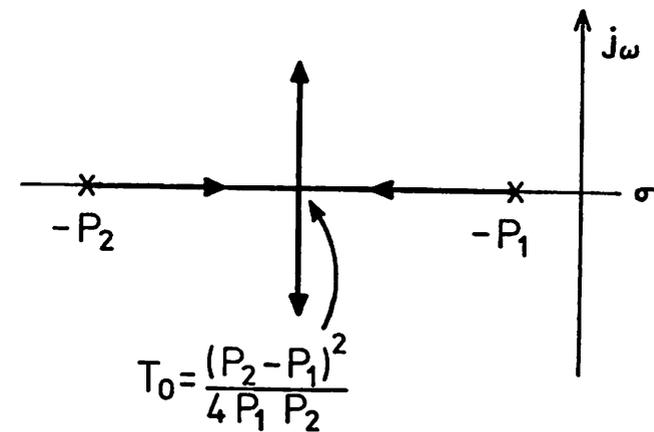
$$T_o = \frac{(p_2 - p_1)^2}{4p_1 p_2} \approx \frac{p_2}{4p_1}, \quad (3.44)$$

which is typically about 500 for NMOS designs. Since the actual low-frequency loop-gain is usually about 1000 (A_o), the transient response will be complex. The pole position, p_2 , is often dependent on loading, and therefore, the details of the step response should be considered for the worst-case stage within the filter. In general, settling time is the dominant consideration in determining the maximum

sampling frequency for a switched capacitor filter.



(a)



(b)

Fig. 3.23. (a) A model of the switched capacitor integrator during the integration time; (b) root locus plot of the pole positions during the integration time.

DYNAMIC RANGE CONSIDERATIONS FOR SWITCHED CAPACITOR FILTERS

The dynamic range of a switched capacitor filter is defined as the ratio of the RMS output voltage at a given total harmonic distortion (THD) level to the total RMS noise voltage within a specified bandwidth. For example, in telephony applications, the maximum signal level is 3 dB below the 1% THD signal level, and the RMS noise voltage is measured in the c-message band which extends from 300 Hz to 3.4 kHz.

The harmonic distortion generated by a switched capacitor integrator is determined by the linearity of the operational amplifier, and by the peak signal level at the output node of the integrator. The nonlinearity of the MOS capacitors also contributes to distortion, but since the capacitor voltage coefficient is typically very small (10 ppm/volt for metal over n^+), THD is usually dominated by the operational amplifiers.

There are two sources of noise in an MOS switched capacitor integrator: (1) The noise of the MOS operational amplifier, and (2) the thermal noise generated by the switches which form the switched capacitor resistors. The noise at the output of a switched capacitor filter is determined by the RMS sum of the noise contributions from each of the integrators. In this chapter, techniques are presented for maximizing dynamic range while minimizing the silicon area requirements.

4.1. Harmonic Distortion in a Switched Capacitor Integrator

The gain transfer curve of a typical NMOS operational amplifier is somewhat nonlinear as shown in the enhancement-depletion example of Fig. 4.1(a). The op amp nonlinearities give rise to harmonic distortion in a switched capacitor integrator which depends on the peak output signal level. In this section, a method of analyzing low-level harmonic distortion in a switched capacitor integrator is presented.

The type-I inverting switched capacitor integrator of Fig. 4.1(b) is implemented with an MOS operational amplifier which has a DC open-loop gain of A which is a function of the DC output voltage as shown in Fig. 4.1(a) and in Table I. The z-plane transfer function of this inverting integrator including gain effects is given by

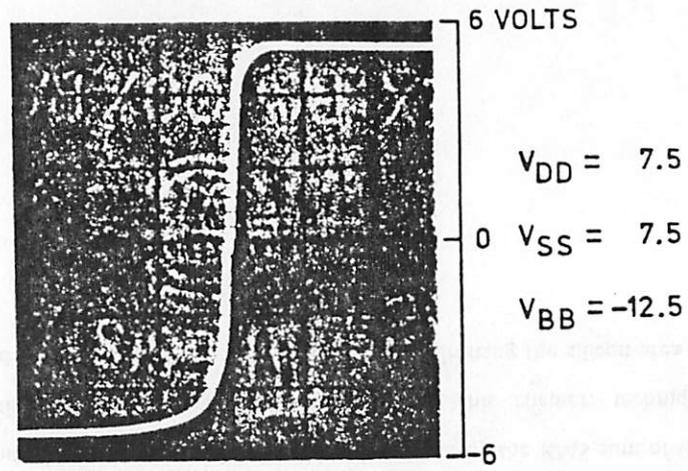
$$H(z) = - \frac{A \left[\frac{C_u}{C_l} \right]}{z \left[A+1 + \frac{C_u}{C_l} \right] - [A+1]} \quad (4.1)$$

and by setting $z = e^{j\omega T}$, the magnitude of the integrator transfer function is obtained:

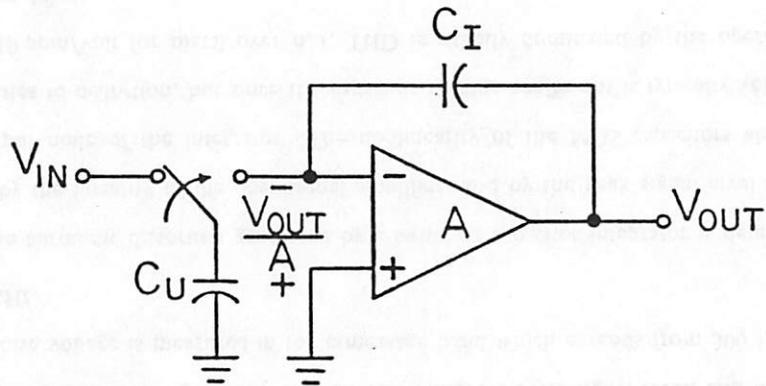
$$|H(\omega)| = \frac{A \left[\frac{C_u}{C_l} \right]}{\left[\left[A+1 + \frac{C_u}{C_l} \right]^2 + [A+1]^2 - 2[A+1] \left[A+1 + \frac{C_u}{C_l} \right] \cos(\omega T) \right]^{1/2}} \quad (4.2)$$

An analytical evaluation of harmonic distortion based on Eqn. (4.2) is quite complicated. Fortunately, THD can be estimated by using the concept of differential gain error which involves calculation of the relative gain change at a given output voltage with respect to the gain at a quiescent output voltage [65]. The positive differential gain error is defined as

$$E^+ = \frac{G^+ - G_Q}{G_Q} \quad (4.3)$$



(a)



(b)

Fig. 4.1. (a) Open-loop gain transfer characteristic for the enhancement-depletion NMOS op amp of Chapter 5; (b) A type-I inverting switched capacitor integrator where the op amp has the gain characteristic given in (a).

| V_{OUT} (VOLTS) | SMALL SIGNAL GAIN | INTEGRATOR GAIN AT f_0 |
|----------------------|----------------------|-----------------------------|
| 5.0 | 122 | 0.99282 |
| 4.5 | 172 | 0.99537 |
| 4.0 | 273 | 0.99768 |
| 3.5 | 628 | 0.99910 |
| 3.0 | 983 | 1.00053 |
| 2.5 | 971 | 1.00052 |
| 2.0 | 958 | 1.00051 |
| 1.5 | 946 | 1.00049 |
| 1.0 | 932 | 1.00047 |
| 0.5 | 919 | 1.00046 |
| 0.0 | 906 | 1.00044 |
| - 0.5 | 864 | 1.00038 |
| - 1.0 | 822 | 1.00032 |
| - 1.5 | 786 | 1.00026 |
| - 2.0 | 753 | 1.00020 |
| - 2.5 | 505 | 0.99950 |
| - 3.0 | 252 | 0.99736 |
| - 3.5 | 165 | 0.99511 |
| - 4.0 | 123 | 0.99289 |
| - 4.5 | 80 | 0.98823 |
| - 5.0 | 46 | 0.97847 |

Table I. The op amp open-loop gain, and the integrator gain as a function of the output voltage level.

and similarly, the negative differential is

$$E^- = \frac{G^- - G_Q}{G_Q} \quad (4.4)$$

where for this example, G_Q is the integrator gain at zero volts output, and G^+ and G^- are the integrator gains at the maximum positive and negative excursions of the output signal, respectively. The second and third harmonic distortion terms are calculated by using the following equations:

$$HD_2 = \frac{1}{8}(E^+ - E^-) \quad (4.5)$$

and

$$HD_3 = \frac{1}{24}(E^+ + E^-). \quad (4.6)$$

These equations are valid at small distortion levels where HD_2 is proportional to the output signal, and HD_3 is proportional to the square of the output signal.

The distortion performance of the switched capacitor integrator of Fig. 4.1(b) at $f_o = 3.2$ kHz with a 128 kHz sampling rate has been calculated using the method described above. The integrator gain at f_o (which is ideally one) was calculated using Eqn. (4.2) with the results shown in Table I, and then using Eqns. (4.3) thru (4.6), the second and third harmonic distortion terms were calculated as shown in Fig. 4.2. When the peak output approaches 4.0 volts, the harmonic distortion increases significantly so that the differential analysis described above can no longer be used. Fig. 4.2 is in good agreement with the experimental results presented in Chapter 5 which show a dramatic increase in distortion for a similar peak voltage.

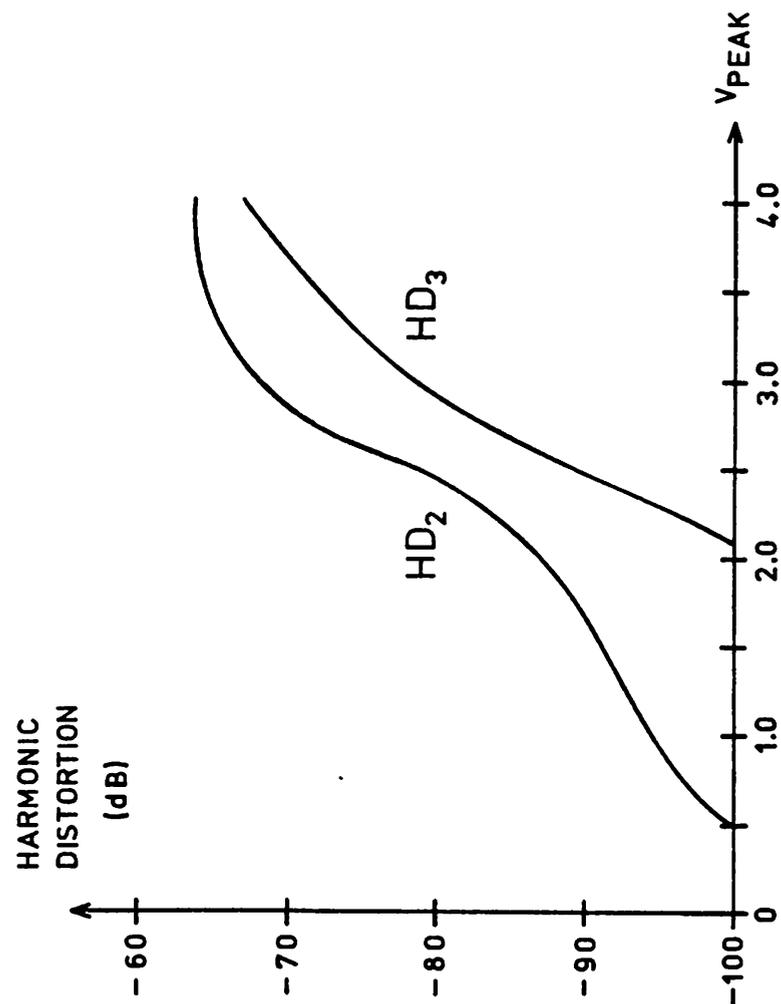


Fig. 4.2. Second and third harmonic distortion for the switched capacitor integrator using the op amp characteristic of Fig. 4.1.

4.2. Scaling Techniques for Switched Capacitor Filters

The dynamic range of a switched capacitor filter with more than one integration stage is maximized by scaling the circuit so that the peak output voltage levels are the same for each of the integrators [66]. Several different scaling techniques are presented in this section along with a brief discussion of the basic noise-distortion-silicon area tradeoffs.

4.2.1. Impedance Scaling

An RLC prototype circuit is impedance scaled by a factor of k using the following relationships [43]:

$$R_i \rightarrow kR_i \quad (4.7a)$$

$$L_j \rightarrow kL_j \quad (4.7b)$$

and

$$C_m \rightarrow \frac{C_m}{k} \quad (4.7c)$$

The effect of impedance scaling is illustrated by considering the second-order RLC prototype shown in Fig. 4.3(a). The current flowing in this circuit before scaling is

$$I(s) = \frac{sC}{s^2LC + sRC + 1} V_{in}(s) \quad (4.8a)$$

and the output voltage is given by

$$V_{out}(s) = \frac{1}{s^2LC + sRC + 1} V_{in}(s). \quad (4.8b)$$

The scaled version of this circuit obtained using Eqn. (4.7) is shown in Fig. 4.3(b).

The value of the current flowing in this circuit is found by substituting the scaled

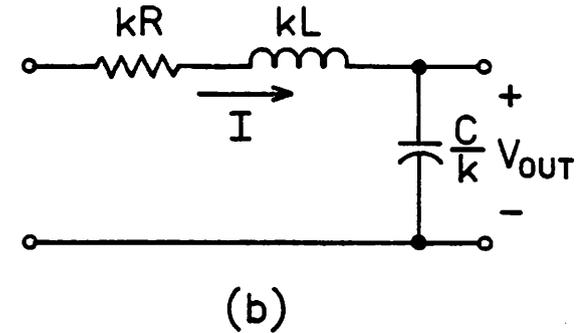
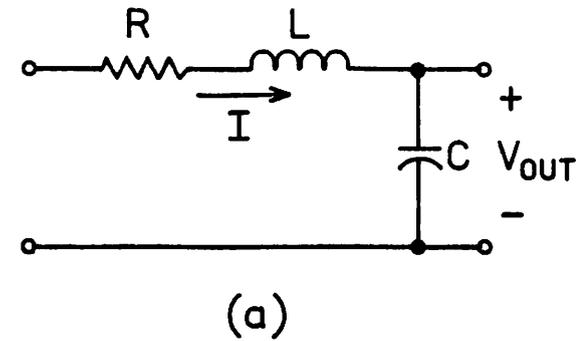


Fig. 4.3. A singly-terminated second-order RLC filter (a) before and (b) after impedance scaling.

element values into Eqn. (4.8a) to obtain

$$I(s) = \frac{s \left[\frac{C}{k} \right]}{s^2 \left[kL \right] \left[\frac{C}{k} \right] + s \left[kR \right] \left[\frac{C}{k} \right] + 1} V_{in}(s) = \frac{1}{k} \frac{sC}{s^2 LC + sRC + 1} V_{in}(s) \quad (4.9a)$$

and similarly, the output voltage is obtained from Eqn. (4.8b) as

$$V_{out}(s) = \frac{V_{in}(s)}{s^2 \left[kL \right] \left[\frac{C}{k} \right] + s \left[kR \right] \left[\frac{C}{k} \right] + 1} = \frac{V_{in}(s)}{s^2 LC + sRC + 1}. \quad (4.9b)$$

It is apparent from Eqns. (4.8) and (4.9) that impedance scaling reduces the current by a factor of k while the voltage level is unchanged. In a similar manner, all inductor currents in a high-order filter are reduced by a factor of k due to impedance scaling while all capacitor voltages remain unchanged.

The dynamic range is maximized by scaling the filter so that all internal integrator outputs have the same peak amplitude [17],[66]. A switched capacitor implementation of the scaled circuit of Fig. 4.3(b) has one output voltage which is directly proportional to the inductor current, I (bandpass output), and another output which is equal to the capacitor voltage, V_{out} (lowpass output). For $Q \gg 1$, the maximum lowpass output voltage for the circuit of Fig. 4.3(b) occurs at the frequency $\omega_o = [LC]^{-1/2}$ and is

$$\frac{V_{out}}{V_{in}}(\max) = \frac{1}{R \left[\frac{C}{L} \right]^{1/2}} = Q \quad (4.10a)$$

and the maximum bandpass voltage, V'_{out} , corresponding to I is

$$\frac{V'_{out}}{V_{in}}(\max) = \frac{1}{kR}. \quad (4.10b)$$

In order for the magnitudes of Eqns. (4.10a) and (4.10b) to be equal, the circuit must be impedance scaled by a factor of $k = \left[\frac{C}{L} \right]^{1/2}$.

A estimate of the silicon area required to implement a switched capacitor version of the scaled RLC prototype of Fig. 4.3(b) can be made by assuming that the area is dominated by the integrating capacitors for the L and C stages. The total area required is proportional to the capacitance ratio

$$\text{Area} \propto \frac{C_i}{C_u} = \left[\frac{f_c}{\omega_{co}} \right] \left[kL + \frac{C}{k} \right] \quad (4.11)$$

where L and C are the normalized element values for a cutoff frequency of 1 rad/sec and ω_{co} is the desired cutoff frequency. The area of Eqn. (4.11) is minimized for a scaling factor of

$$k = \left[\frac{C}{L} \right]^{1/2}. \quad (4.12)$$

Notice that for this example, the scaling factor which optimizes dynamic range also minimizes the silicon area required. For high-order filters, it is generally true that those conditions which maximize dynamic range also minimize the required die area.

The impedance scaling technique described above simultaneously reduces all inductor currents by k . Unfortunately, for high-order filters, the peak inductor currents are generally not equal before scaling, and therefore after scaling, the peak amplitudes will still be different since all currents are equally affected. Thus, although impedance scaling works well for second-order filters, it is not generally applicable for optimizing dynamic range in high-order filters. A switched capacitor scaling technique which can be used to independently scale all internal nodes

representing *either* voltages or currents is presented in the next section.

4.2.2. Switched Capacitor Node-Voltage Scaling

A section of an unscaled type-I LDI switched capacitor ladder filter is shown in Fig. 4.4(a). In the z -domain, the three unscaled output voltages are as follows:

$$V_{n-1}(z) = \left[\frac{f_c C_u}{C_{n-1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] [V_{n-2}(z) - V_n(z)] \quad (4.13a)$$

$$V_n(z) = \left[\frac{f_c C_u}{C_n} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] [V_{n-1}(z) - V_{n+1}(z)] \quad (4.13b)$$

and

$$V_{n+1}(z) = \left[\frac{f_c C_u}{C_{n+1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] [V_n(z) - V_{n+2}(z)]. \quad (4.13c)$$

As an example, assume that it is desired to scale the voltage V_n by a factor of k without affecting the other output nodes, so that after scaling,

$$\frac{V_n(z)}{k} = \left[\frac{f_c C_u}{k C_n} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] [V_{n-1}(z) - V_{n+1}(z)]. \quad (4.14)$$

From this equation, it is apparent that the voltage at any node can be scaled by simply changing the gain constant for that integrator, i.e., $C_n \rightarrow k C_n$. In addition, if a node is scaled by k , the inputs driven from that node must be scaled by $\frac{1}{k}$ in order to insure that the other integrator outputs are unchanged. For the previous example, this requires that

$$V_{n-1}(z) = \left[\frac{f_c C_u}{C_{n-1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] V_{n-2}(z) - \left[\frac{k f_c C_u}{C_{n-1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] \frac{V_n(z)}{k} \quad (4.15a)$$

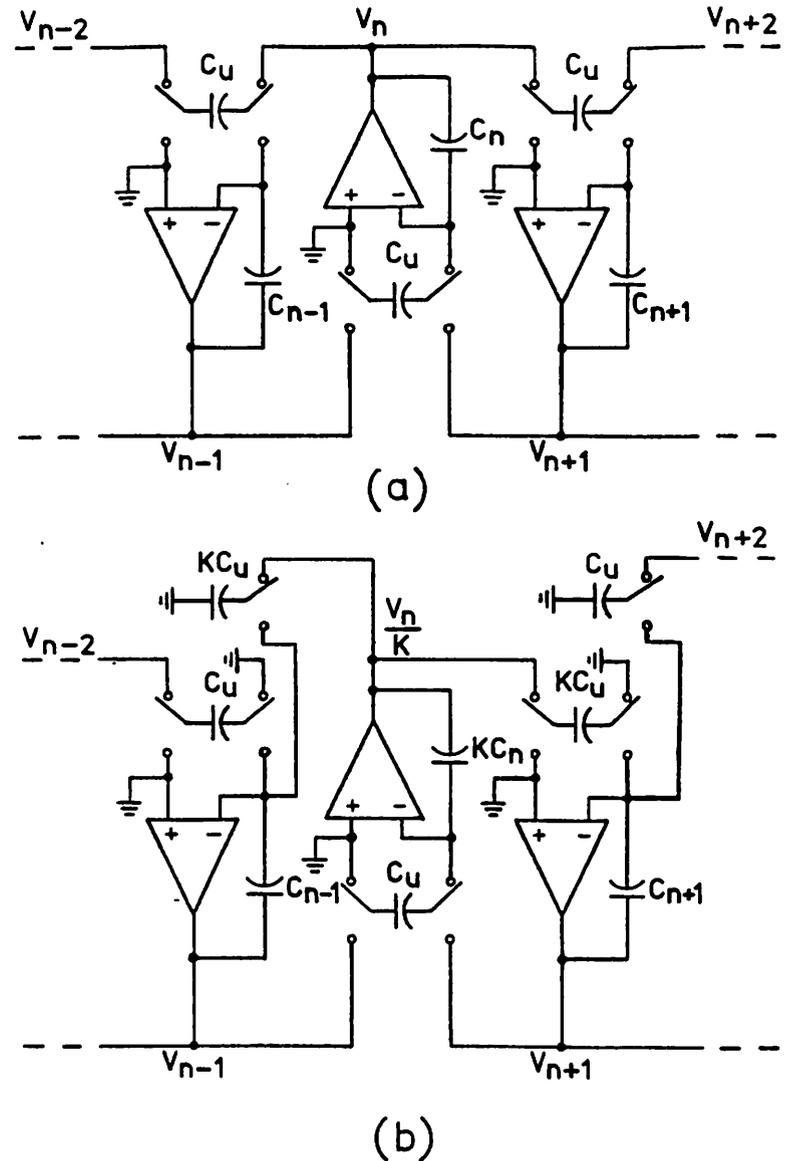


Fig. 4.4. A section of a switched capacitor ladder filter (a) before and (b) after node-voltage scaling.

and

$$V_{n+1}(z) = \left[\frac{k f_c C_u}{C_{n+1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] \frac{V_n(z)}{k} - \left[\frac{f_c C_u}{C_{n+1}} \right] \left[\frac{z^{-1/2}}{1-z^{-1}} \right] V_{n+2}(z). \quad (4.15b)$$

Eqn. (4.15) shows that all of the switched capacitors driven from a scaled node, $\frac{V_n(z)}{k}$, are changed to a value of kC_u . For example, if a node voltage is halved ($k=2$), then all switched capacitors connected to that node are doubled. The switched capacitor section after node-voltage scaling is shown in Fig. 4.4(b). In general, two additional switched capacitors are added for each scaled node, and if k is not an integer, the capacitor matching accuracy between the different sized switched capacitors is slightly reduced.

For both node-voltage scaling and impedance scaling, there is a tradeoff between noise and signal level (distortion). This tradeoff is illustrated by assuming that the gain from the input to the output of the filter is constant. For an arbitrary internal node, V_x , the following relationships apply for the unscaled and scaled versions, respectively:

$$\frac{V_{out}}{V_{in}} = \left[\frac{V_{out}}{V_x} \right] \left[\frac{V_x}{V_{in}} \right] \quad (4.16a)$$

and

$$\frac{V_{out}}{V_{in}} = \left[\frac{V_{out}}{V_x} \right] \frac{\left[\frac{V_x}{k} \right]}{V_{in}} = \left[\frac{kV_{out}}{V_x} \right] \left[\frac{V_x}{kV_{in}} \right]. \quad (4.16b)$$

The first term in both equations is a measure of the noise gain from V_x to the output of the filter, and the second term represents the magnitude of the peak signal at

node V_x relative to the input. Hence, the first term determines the noise performance, and the second term determines the distortion performance. Notice from Eqn. (4.16b), that as the noise gain is increased by k , the peak amplitude at V_x is reduced by k and vice-versa. Thus, there is a direct tradeoff between noise and distortion, and it is for this reason that the peak amplitudes are set equal for all stages in order to maximize dynamic range.

4.2.3. Switched Capacitor Loop Scaling

For bandpass and bandreject RLC filters, the relative spread in the LC element values rapidly increases as the selectivity increases. For example, consider the RL lowpass prototype shown in Fig. 4.5(a). Applying the lowpass-to-bandpass transformation of Chapter 2 results in the circuit of Fig. 4.5(b) where the bandpass reactive values are given as

$$L_B = \frac{QL_n}{\omega_o} \quad (4.17a)$$

and

$$C_B = \frac{1}{QL_n\omega_o}. \quad (4.17b)$$

From these equations, it is apparent that the ratio of $\frac{L_B}{C_B}$ increases in proportion to Q^2 which is very undesirable because in a switched capacitor implementation, it results in a similar spread in the required capacitor ratios. In addition, if this network is not scaled, the peak current remains constant for a fixed termination resistance while the peak capacitor voltage increases in proportion to Q . Thus, the dynamic range is significantly degraded for high- Q applications.

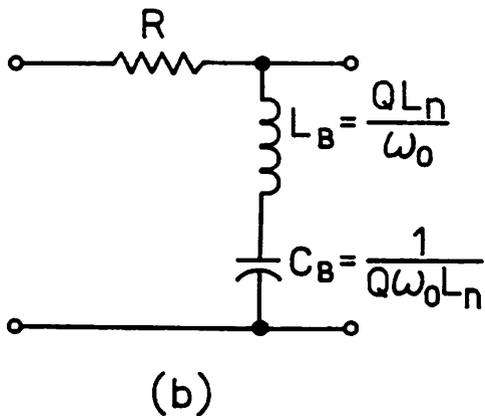
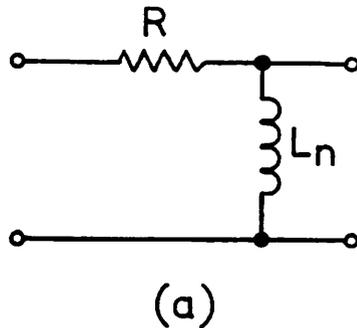


Fig. 4.5. (a) A single-pole RL filter, and (b) a bandpass circuit obtained using the lowpass-to-bandpass transformation.

A signal flowgraph for the RLC bandpass prototype of Fig. 4.5(b) is shown in Fig. 4.6(a). The current, I_1 , is given by

$$I_1 = \frac{\omega_0}{sQL_n} [V_{in} - V_0 - V_2] \quad (4.18a)$$

which can also be written as

$$I_1 = \frac{\omega_0}{s} \left[\frac{V_{in}}{QL_n} - \frac{V_0}{QL_n} - \frac{V_2}{QL_n} \right] \quad (4.18b)$$

Thus, all inputs to the I_1 integrator have been divided by QL_n and the integrator gain constant has been changed to ω_0 . Similarly, the lowpass output voltage, V_2 , is written as

$$V_2 = \frac{Q\omega_0 L_n}{s} I_1 \quad (4.19a)$$

or equivalently,

$$V_2 = \frac{\omega_0}{s} [QL_n I_1] \quad (4.19b)$$

Thus, the input of the second integrator has been multiplied by QL_n , and the gain constant has become ω_0 . Using Eqns. (4.18) and (4.19), an equivalent signal flowgraph is drawn in Fig. 4.6(b). At this point, the circuit has been rearranged so that the integrator gain constants are equal. However, for maximum dynamic range, the peak amplitudes must still be scaled to be equal. From Eqn. (4.10a), the maximum lowpass output voltage is found to be

$$V_2(\max) = \frac{1}{R} \left[\frac{L_B}{C_B} \right]^{1/2} = \frac{QL_n}{R} \quad (4.20a)$$

and the maximum bandpass current is

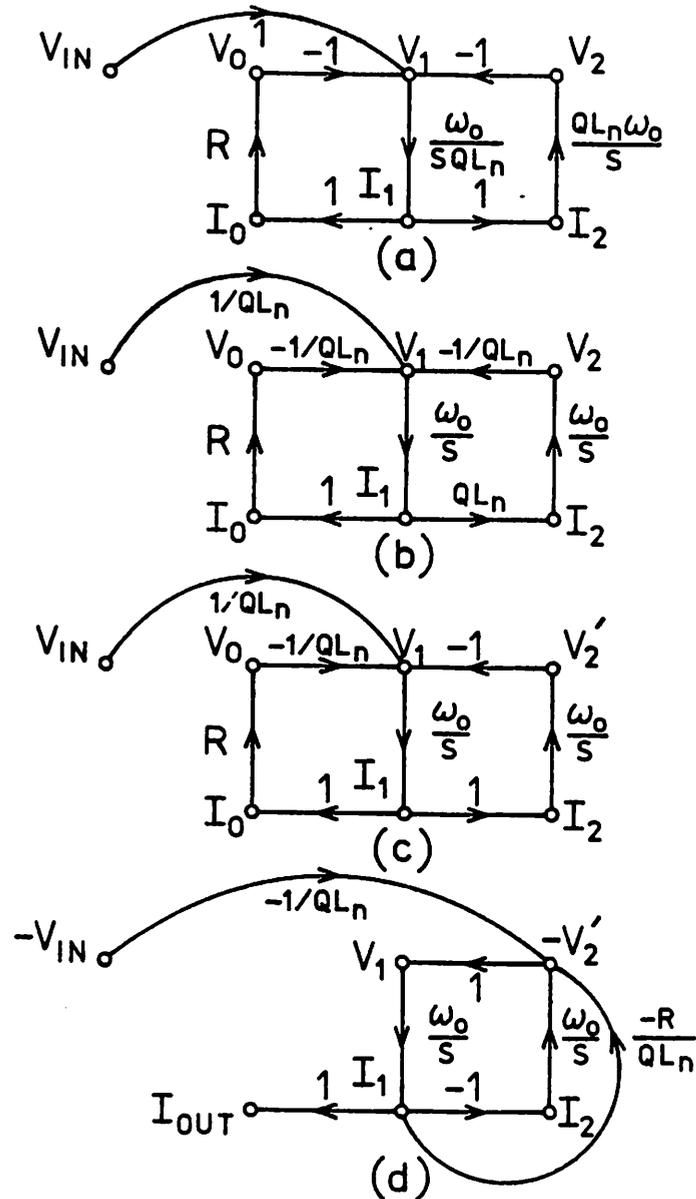


Fig. 4.6. A series of signal flowgraphs which illustrate the switched capacitor loop-scaling technique.

$$I_1(\max) = \frac{1}{R}. \quad (4.20b)$$

In order for these peak amplitudes to be equal, the lowpass output must be reduced by a factor of QL_n as follows:

$$V_2' = \frac{V_2}{QL_n} = \frac{\omega_0}{s} \left[\frac{QL_n I_1}{QL_n} \right] = \frac{\omega_0}{s} I_1 \quad (4.21)$$

where V_2' is the scaled lowpass output voltage. The input to the bandpass stage, V_1 , must also be modified to account for the scaling as shown below and in the scaled flowgraph of Fig. 4.6(c):

$$V_1 = \frac{V_{in}}{QL_n} - \frac{V_1}{QL_n} - \frac{V_2}{QL_n} = \frac{V_{in}}{QL_n} - \frac{V_1}{QL_n} - V_2'. \quad (4.22)$$

For this network, the switched capacitor inputs to the bandpass stage at V_1 from V_{in} and I_1 (through R) become very small as QL_n becomes large since the switched capacitor size is $\frac{C_u}{QL_n}$ where C_u is the unit switched capacitor which is usually about 1 pF. Because of the small size, it is difficult to accurately define and match these capacitors in a monolithic implementation. This problem is solved by rerouting these two signals through charge multiplication paths associated with the adjacent lowpass integrator as shown in Fig. 4.6(d). In this case, the feedforward capacitors are $\frac{1}{QL_n}$ times the integration capacitor in contrast to the network of Fig. 4.6(c) where they were $\frac{1}{QL_n}$ times the switched capacitor value. Since the integration capacitor is usually much larger than the switched capacitor, the capacitor values associated with the two feedforward paths are more accurately realized in monolithic form. The final network of Fig. 4.6(d) provides a scaled bandpass output, but the lowpass output is lost due to the addition of summation paths to the lowpass

stage. This technique has been verified by other workers for monolithic versions of second-order [52] and high-order [67] bandpass and bandreject filters. The area-noise-distortion considerations are identical to those of the impedance and node-voltage scaled networks.

4.3. Noise in a Switched Capacitor Integrator

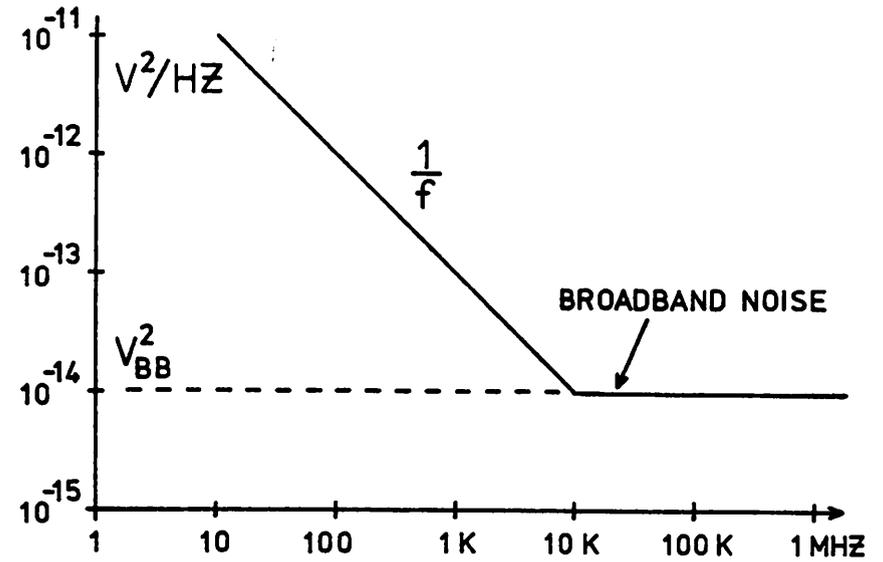
In this section, the sources of electrical noise in a switched capacitor integrator will be described.

The equivalent input noise spectral density of an MOS operational amplifier is frequency dependent as illustrated in Fig. 4.7(a). The power spectral density at low frequencies (<10 kHz) is dominated by the flicker component which decreases as $\frac{1}{f}$, and the spectral density at higher frequencies is relatively constant (typically $100 \text{ nV}/[\text{Hz}]^{1/2}$) and is determined by the thermal noise associated with the channel resistance of the MOS transistors. Depending on the passband frequencies of the filter, one or both of these components may be important in determining the dynamic range at the output of the filter.

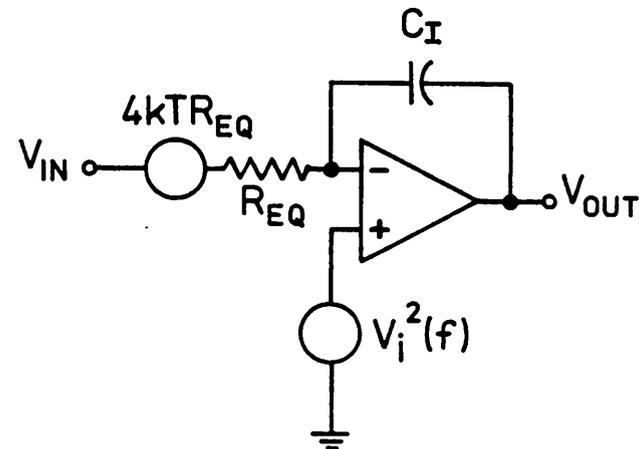
The noise performance of the Miller integrator of Fig. 4.7(b) will first be analyzed considering both the thermal noise of the resistor and the equivalent input noise of the operational amplifier. It will be assumed that the op amp has a low frequency gain of A_o with a one-pole rolloff to the unity-gain frequency, f_u . The gain constant of the integrator is $f_o = \frac{1}{2\pi R_{EQ} C_I}$ as shown in Fig. 4.8(a).

First, consider the spectral noise contribution from the resistor. As shown in Fig. 4.8(a), this white noise source is lowpass filtered by the integrator which has a transfer function of

$$H_R(f) = \frac{A_o}{1 + \frac{jfA_o}{f_o}} \tag{4.23}$$



(a)



(b)

Fig. 4.7. (a) A typical plot of the equivalent input noise power spectral density for an NMOS depletion-load op amp; (b) A Miller integrator with op amp and resistor noise sources.

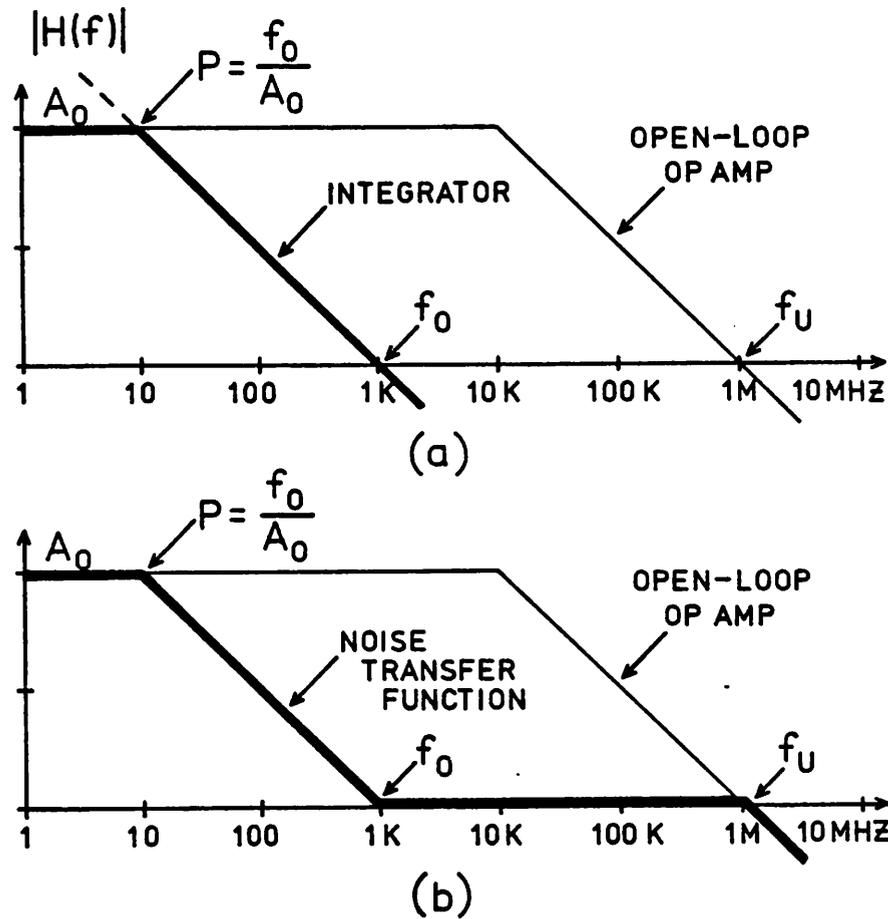


Fig. 4.8. (a) Transfer function from the resistor noise source to the output; (b) the transfer function from the op amp equivalent noise source to the output.

The power spectral density at the integrator output is therefore equal to

$$V_{\text{OUT RESISTOR}}^2(f) = \left[4kTR_{\text{EQ}} \right] \left[\frac{A_0^2}{1 + \left(\frac{fA_0}{f_0} \right)^2} \right] \quad (4.24)$$

Now, consider the noise contributed at the integrator output by the operational amplifier. The transfer function from $V_i^2(f)$ to the integrator output of Fig. 4.7(b) is given by

$$H_A(s) = \frac{1 + sC_1R_{\text{EQ}}}{sC_1R_{\text{EQ}}} \quad (4.25)$$

and is shown as the darkest line in Fig. 4.8(b). Notice that this curve is made up of four separate sections, and therefore, the output power spectral density can be determined separately for each of the four cases as follows:

$$V_{\text{out}}^2(f) = V_i^2(f) A_0^2 \quad \text{for } 0 \leq f < \frac{f_0}{A_0} \quad (4.26a)$$

$$V_{\text{out}}^2(f) = V_i^2(f) \left[\frac{f_0}{f} \right]^2 \quad \text{for } \frac{f_0}{A_0} \leq f < f_0 \quad (4.26b)$$

$$V_{\text{out}}^2(f) = V_i^2(f) \quad \text{for } f_0 \leq f < f_u \quad (4.26c)$$

and

$$V_{\text{out}}^2(f) = V_i^2(f) \left[\frac{f_u}{f} \right]^2 \quad \text{for } f_u \leq f \quad (4.26d)$$

where $V_i^2(f)$ is the equivalent input noise power spectral density of the operational amplifier. Given an op amp power spectral density, Eqn. (4.26) can be evaluated to determine the total RMS noise at the integrator output in any specified bandwidth.

Next, consider the spectral density at the output of the switched capacitor integrator of Fig. 4.9(a) due to the equivalent input op amp noise. For baseband frequencies, the switched capacitor is equivalent to a resistor, R_{EQ} , and therefore, for these low frequencies, the switched capacitor integrator is identical to the Miller integrator of Fig. 4.7(b). Thus, a similar analysis applies with a slight change in the frequency limits as follows:

$$V_{out}^2(f) = V_i^2(f) A_o^2 \quad \text{for } 0 \leq f < \frac{f_o}{A_o} \quad (4.27a)$$

$$V_{out}^2(f) = V_i^2(f) \left[\frac{f_o}{f} \right]^2 \quad \text{for } \frac{f_o}{A_o} \leq f < f_o \quad (4.27b)$$

and

$$V_{out}^2(f) = V_i^2(f) \quad \text{for } f_o \leq f < \frac{f_c}{2} \quad (4.27c)$$

assuming $\frac{f_c}{2} < f_u$ where f_c is the switched capacitor sampling frequency. The op amp noise above $\frac{f_c}{2}$ in frequency must be treated using sampled-data techniques.

It will be assumed that f_c is greater than the $\frac{1}{f}$ noise corner of the op amp so that flicker noise is not aliased and thus, only the broadband op amp noise need be considered. The output noise for this case depends on when the output is sampled. For example, if the output is sampled during ϕ_1 as in Fig. 4.9(b), the op amp is in unity gain as shown in Fig. 4.10(a), and the squared RMS noise at the output is

$$V_{OUT_{samp}}^2 = \int_0^{\infty} V_{BB}^2 \left[1 + \left(\frac{f}{f_o} \right)^2 \right]^{-1} df = \frac{\pi f_u V_{BB}^2}{2}, \quad (4.28)$$

where V_{BB}^2 is the broadband power spectral density. The sampled output power

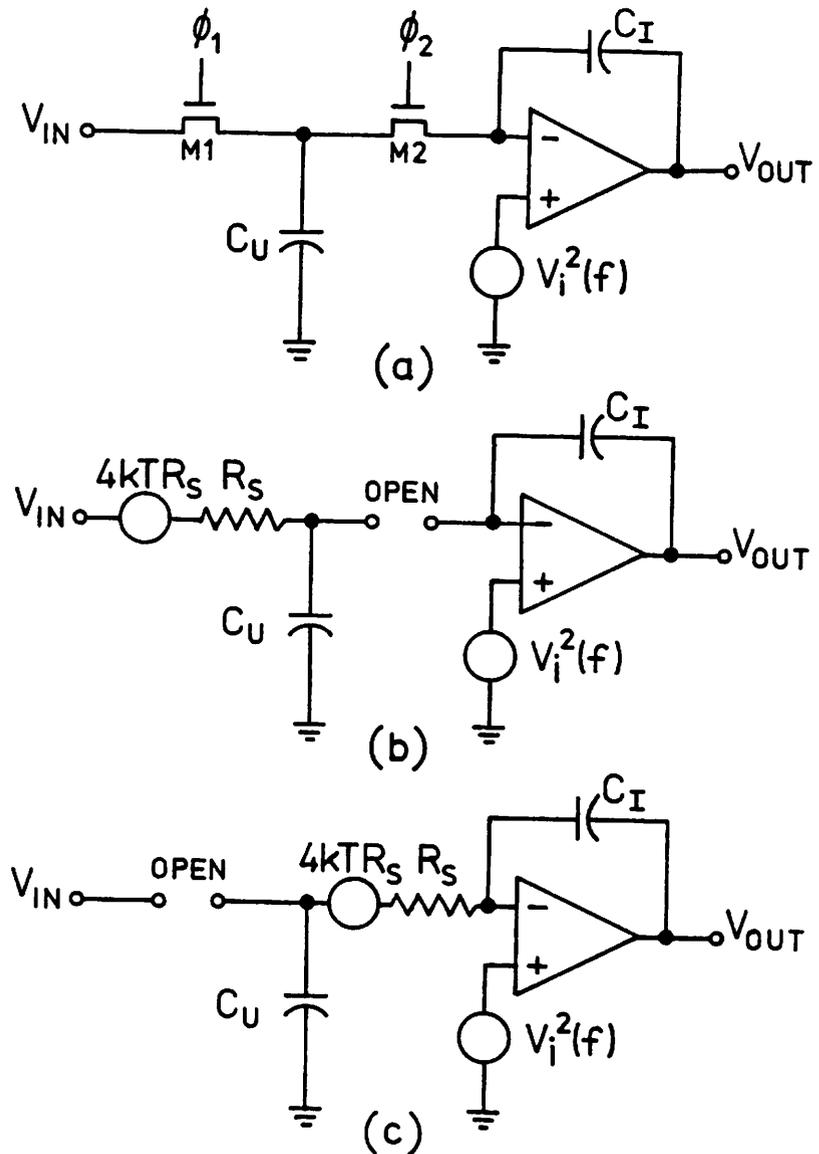


Fig. 4.9. (a) A switched capacitor integrator; (b) the noise model during ϕ_1 , and (c) the noise model during ϕ_2 .

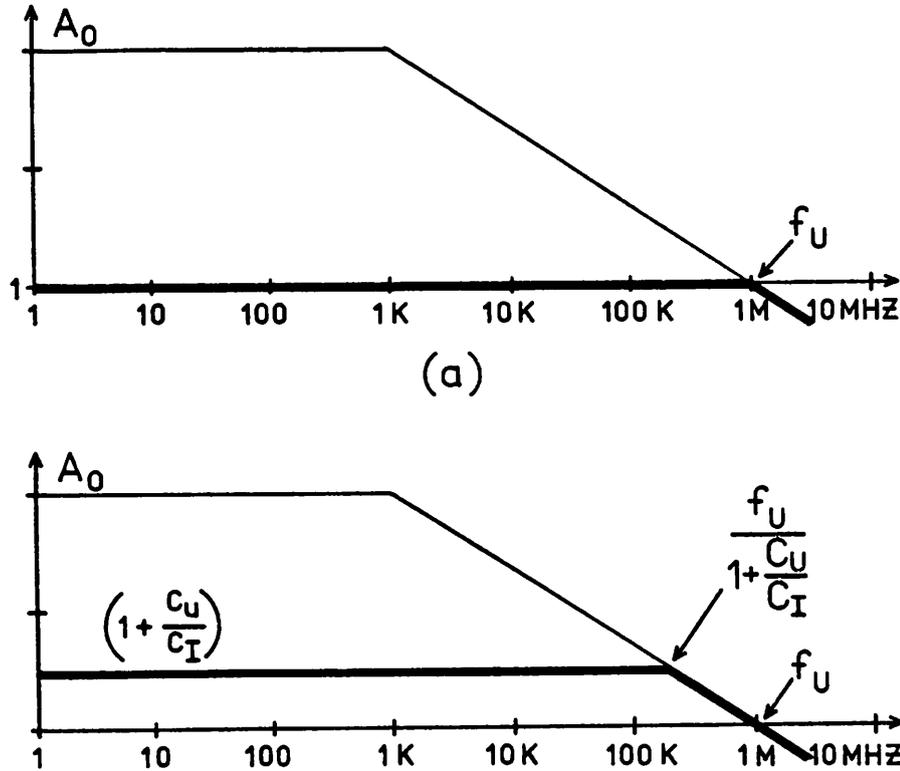


Fig. 4.10. Frequency response from the op amp input noise source to the integrator output for (a) the circuit of Fig. 4.9(b) and (b) for the circuit of Fig. 4.9(c).

spectral density is therefore

$$V_{PSD}^2 = \frac{\pi f_u V_{BB}^2}{2f_c} \tag{4.29}$$

On the other hand, if the output is sampled during ϕ_2 as in Fig. 4.9(c), the closed loop op amp gain is $(1 + \frac{C_u}{C_I})$ as shown in Fig. 4.10(b). The squared RMS noise at the output for this case is

$$V_{out}^2 = \int_0^\infty \frac{V_{BB}^2 (1 + \frac{C_u}{C_I})^2}{\left[1 + (\frac{f}{f_u})^2 (1 + \frac{C_u}{C_I})^2\right]} df = \frac{\pi f_u (1 + \frac{C_u}{C_I}) V_{BB}^2}{2} \tag{4.30}$$

and the corresponding power spectral density is

$$V_{PSD}^2 = \frac{\pi f_u (1 + \frac{C_u}{C_I}) V_{BB}^2}{2f_c} \tag{4.31}$$

Equations (4.28) through (4.31) assume that f_u is less than $\frac{1}{2\pi R_s C_u}$. If this assumption is not valid, the same analysis can be used with f_u replaced by $\frac{1}{2\pi R_s C_u}$.

The noise contributions from the MOSFET switch transistors also need to be considered. Again, the baseband and high frequency terms will be considered separately. The transistor M_1 connected to ϕ_1 has an on resistance of R_s as shown in Fig. 4.9(b). For low frequencies, the switched capacitor can be replaced by a resistor, R_{EQ} , and the Miller integrator of Fig. 4.7(b) along with the transfer function of Fig. 4.8(a) are used to obtain the spectral densities at the integrator output:

$$V_{out}^2 = 4kTR_s A_o^2 \text{ for } 0 \leq f < \frac{f_o}{A_o} \tag{4.32a}$$

and

$$V_{\text{out}}^2 = 4kTR_s \left[\frac{f_o}{f} \right]^2 \quad \text{for } \frac{f_o}{A_o} < f. \quad (4.32b)$$

The total squared RMS noise contribution at the integrator output from this noise source is

$$V_{\text{RMS}}^2 = 2kT\pi R_s A_o f_o. \quad (4.33)$$

At low frequencies, transistor M_2 connected to ϕ_2 also has its noise filtered by the integrator so that Eqns. (4.32) and (4.33) also apply for the noise source of that transistor.

Finally, the sampling effects for these two noise sources must be considered. When M_1 is on, as in Fig. 4.9(b), its noise is lowpass filtered by the $R_s C_u$ combination giving a total squared RMS noise on C_u of

$$V_{\text{RMS}}^2 = \frac{kT}{C_u}. \quad (4.34)$$

When M_1 is opened, this noise is sampled onto C_u giving a power spectral density at C_u of

$$V_{\text{PSD}}^2 = \frac{kT}{f_c C_u} = kTR_{\text{EQ}}. \quad (4.35)$$

The transfer function from C_u to the integrator output is derived from the circuit of Fig. 4.9(c) to be

$$H(s) = \frac{\frac{C_u}{C_1}}{1+sR_s C_u} \quad (4.36)$$

and the output spectral density is therefore

$$V_{\text{out}}^2(f) = \frac{kTR_{\text{EQ}} \left[\frac{C_u}{C_1} \right]^2}{\left[1 + (2\pi f R_s C_u)^2 \right]}. \quad (4.37)$$

When M_2 is on, its noise is filtered onto C_u in a similar manner, and when M_2 is subsequently opened, this noise is sampled onto C_u . However, ϕ_1 then turns on M_1 , and this noise voltage is returned to the input source so that M_2 does not contribute any sampled noise at the integrator output.

The spectral density calculations for the switched capacitor integrator can be used to estimate the noise performance of any switched capacitor filter by multiplying the power spectral density by $|T(f)|^2$ where $T(f)$ is the transfer function from the integrator output to the filter output, and then integrating over the desired bandwidth.

EXPERIMENTAL RESULTS FOR NMOS LOWPASS PROTOTYPES

In this chapter, experimental results from two NMOS integrated switched capacitor ladder filters are presented. The first design realized a fifth-order Chebyshev lowpass response, and the second, a third-order Cauer lowpass response [24]-[25]. Monolithic MOS capacitor ratios and clock frequency were used as the precision components. The performance of the NMOS depletion-load operational amplifier used to implement the filters is also given.

5.1. NMOS Depletion-Load Operational Amplifier

The NMOS operational amplifier used in both filter designs (shown schematically in Fig. 5.1), is a simplified version of a recently reported design [14]. It was integrated using the NMOS metal-gate depletion-load process given in Appendix 1. The measured results presented in Table I are in good agreement with the theoretical calculations of Appendix 2.

5.1.1. DC Open-Loop Gain

The DC open-loop gain of NMOS depletion-load operational amplifiers depends on both power supply and body-bias voltages [14],[47]. Figure 5.2 shows that the measured open-loop gain for ± 7.5 volt supplies with 0, 2.5, and 5.0 volts of body bias varied from 400 to 1000 as measured about zero volts at the output. Figure 5.3 shows the low frequency open-loop gain characteristics for ± 5.0 volt supplies with 0, 2.5 and 5.0 volts body bias, and in this case, the gain ranged from 33 to 60. As discussed in Chapters 3 and 4, for lowpass filters, it is desirable to have a small-signal voltage gain of several hundred over the entire output voltage range in order to minimize frequency response errors and harmonic distortion.

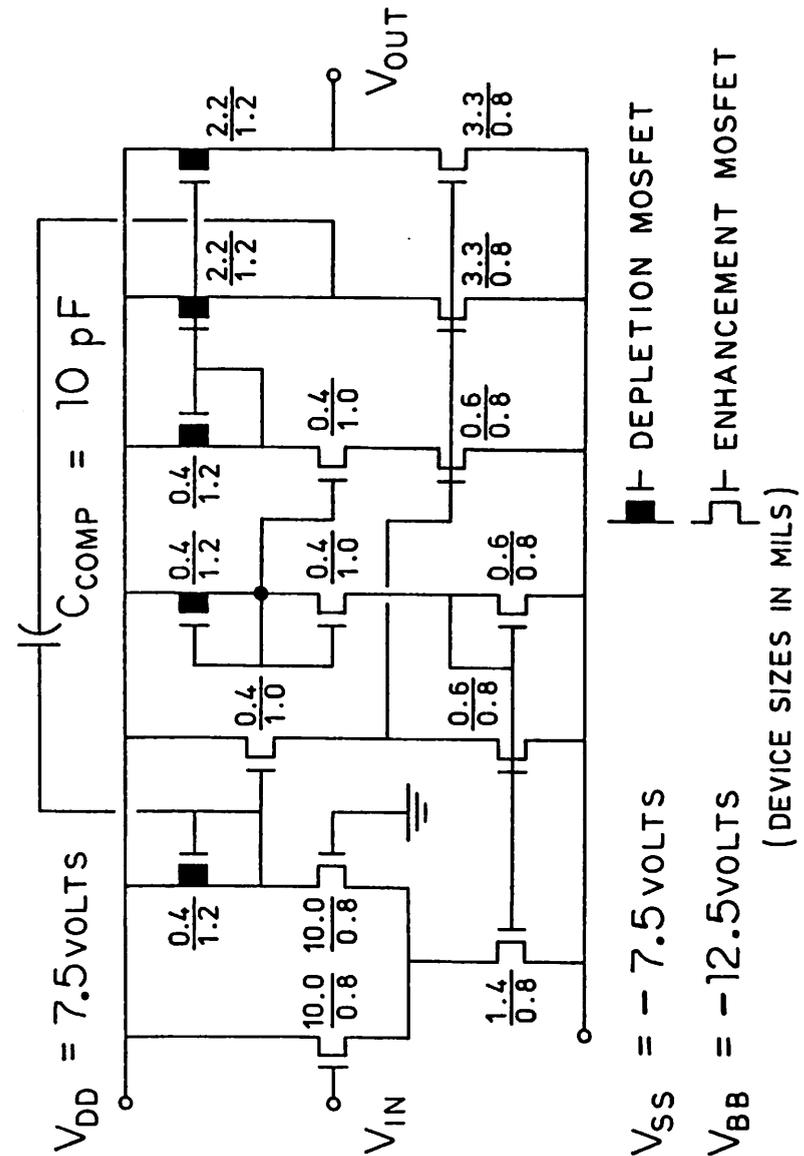


Fig. 5.1. Depletion-load NMOS operational amplifier.

| | |
|-------------------------|----------------------|
| POWER SUPPLIES | $V_{DD} = 7.5$ VOLTS |
| | $V_{SS} = -7.5$ |
| | $V_{BB} = -12.5$ |
| DC OPEN-LOOP GAIN | 1000 |
| EQUIVALENT INPUT OFFSET | 120 mV |
| CMRR | 54 dB |
| PSRR | 46 dB |
| UNITY GAIN BANDWIDTH | 1 MHz |
| SLEW RATE | 1 VOLT/ μ SEC |
| POWER DISSIPATION | 6 mW |
| DIE AREA | 400 mil ² |

Table I. Measured NMOS enhancement-depletion operational amplifier performance parameters.

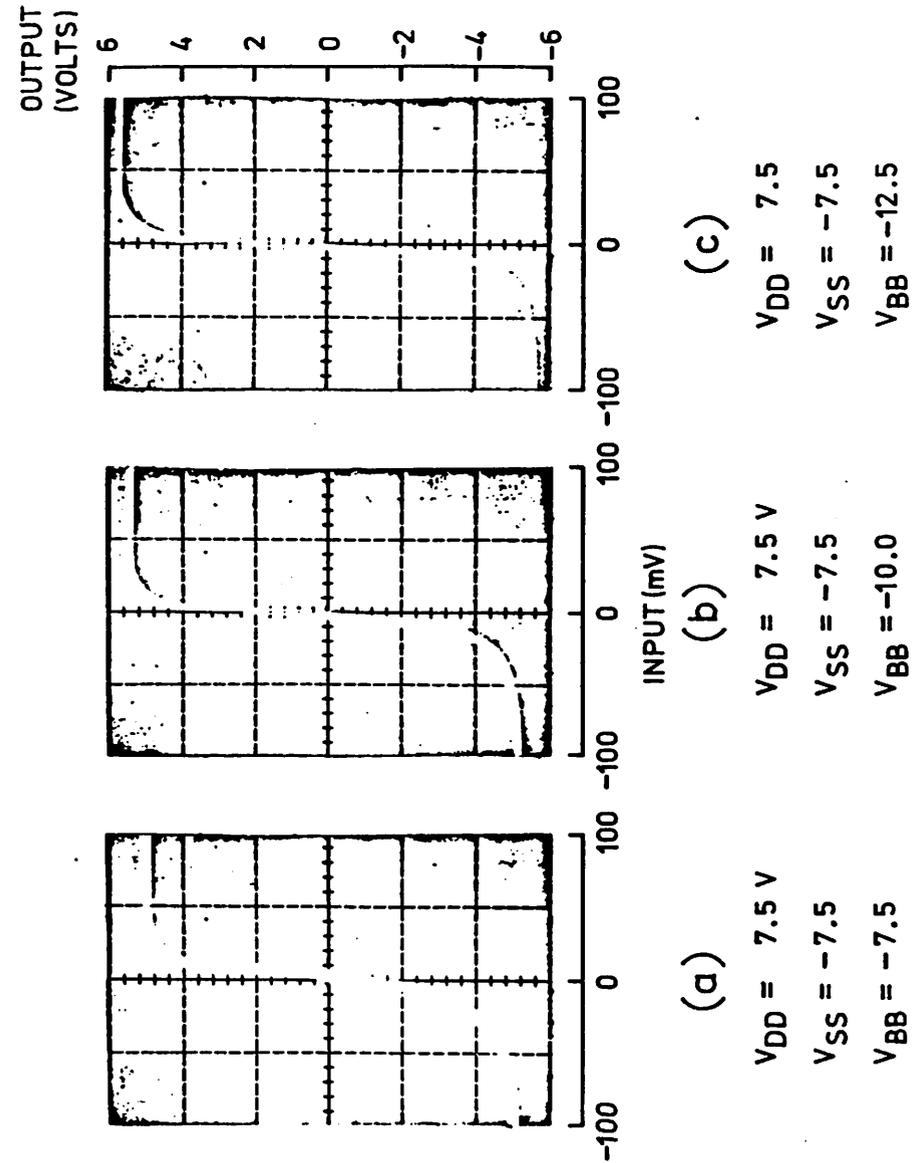


Fig. 5.2. Open-loop op amp gain versus body-bias variations for ± 7.5 volt power supplies.

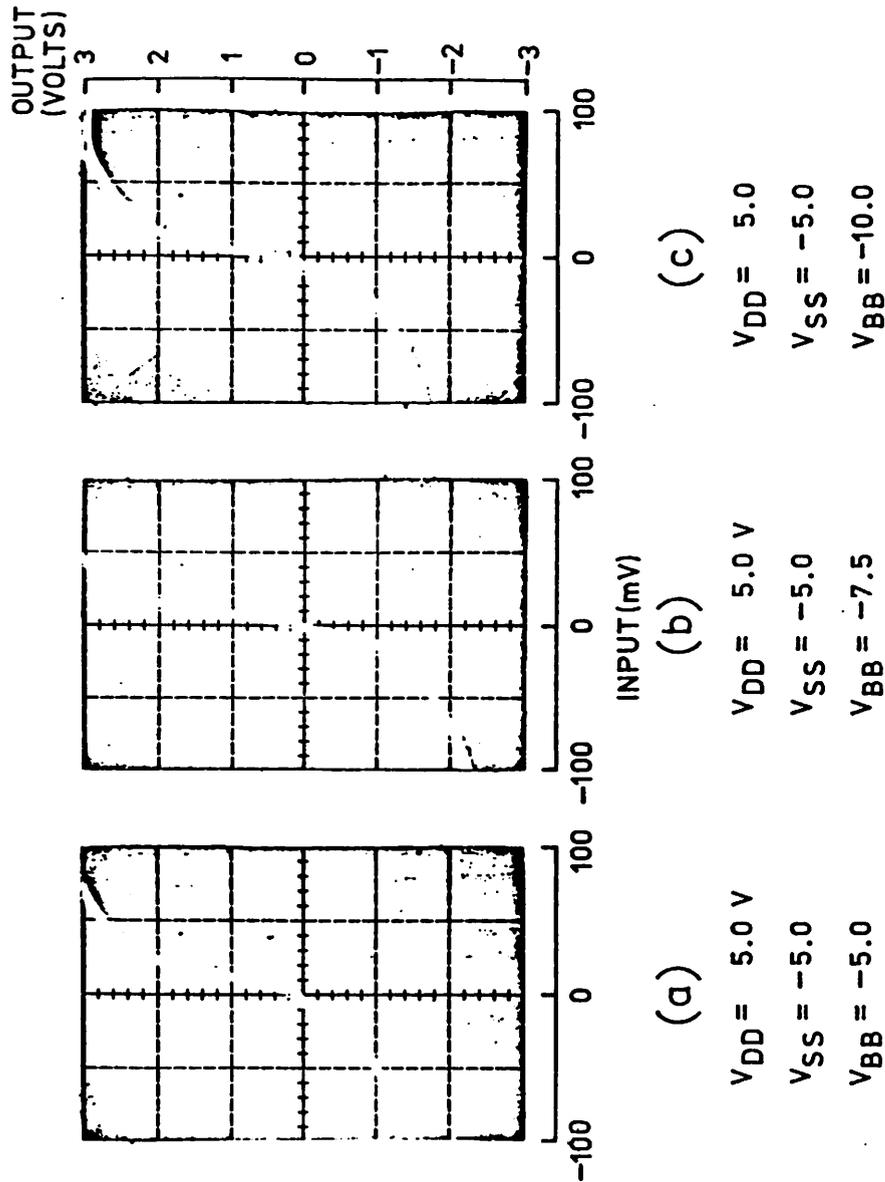


Fig. 5.3. Open-loop op amp gain versus body-bias variations for ± 5.0 volt power supplies.

Hence, for best filter performance, this particular amplifier should be operated with ± 7.5 supplies with 5.0 volts body bias. Note from Fig. 5.2 that when the output voltage is below -3.2 volts, the gain decreases to about 100. This point on the gain curve corresponds to the voltage where a sharp increase in harmonic distortion is observed in the filter.

5.1.2. Equivalent Input Offset Voltage

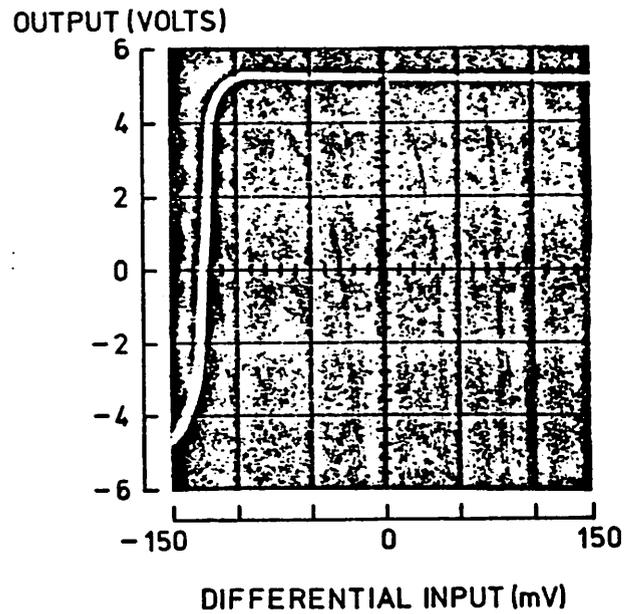
The measured offset voltage of 122 mV in Fig. 5.4 is typical of this amplifier, and is primarily due to the paraphase input stage. As described in Chapter 3, the amplifier offset voltages contribute to a DC offset voltage at the filter output which should be minimized in order to maximize dynamic range. The offset voltage of this particular amplifier can be decreased by unbalancing the input pair of transistors in order to counteract the effect of unequal loads.

5.1.3. Common-Mode Range and CMRR

The measured common-mode range and CMRR are displayed in Fig. 5.5. This parameter is not important for switched capacitor integrators if the op amps are used with the noninverting input connected to a DC bias voltage since there are no steady-state common-mode signals for this case.

5.1.4. Equivalent Input Noise

The measured unity-gain noise spectral density is shown in Fig. 5.6. The measured $\frac{1}{f}$ noise corner is at about 10 kHz, and the broadband noise spectral density at 2 kHz is about $1\ \mu\text{V}/[\text{Hz}]^{1/2}$.



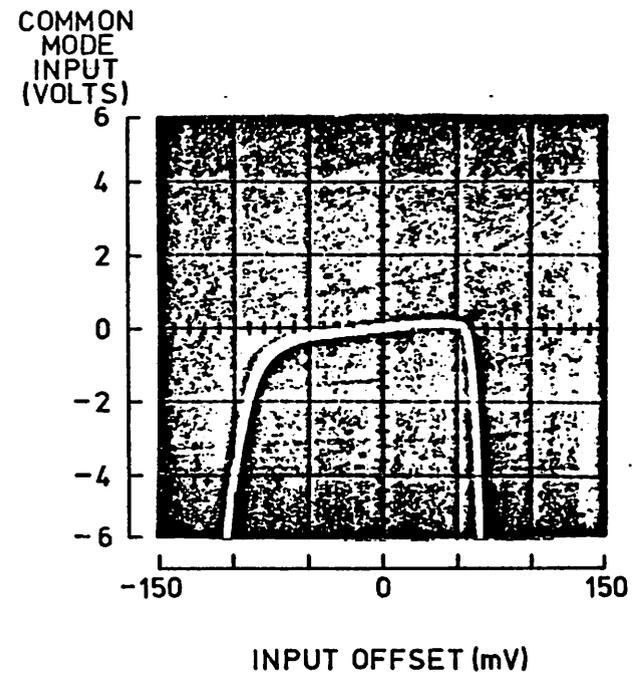
$$V_{DD} = 7.5 \text{ V}$$

$$V_{SS} = -7.5$$

$$V_{BB} = -12.5$$

$$V_{OS} = 122 \text{ mV}$$

Fig. 5.4. Op amp input offset voltage.



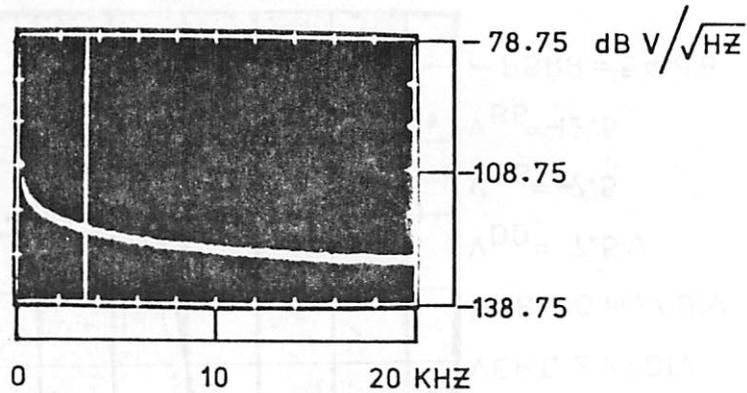
$$V_{DD} = 7.5 \text{ V}$$

$$V_{SS} = -7.5$$

$$V_{BB} = -12.5$$

$$\text{CMRR} = 54 \text{ dB}$$

Fig. 5.5. Measured op amp common-mode range and CMRR.



$$V_{DD} = 7.5 \text{ V}$$

$$V_{SS} = -7.5$$

$$V_{BB} = -12.5$$

(-122.9 dB V/√HZ at 3400 HZ MARKER)

Fig. 5.6. Measured op amp unity-gain noise spectral density.

5.1.5. Power Supply Rejection

The measured power supply rejection for both the V_{DD} and V_{SS} supplies is presented in Fig. 5.7 for a low frequency signal. The PSRR is typically greater than 45 dB.

5.1.6. Power Supply Current versus Supply Voltage

The data for supply current versus supply voltage given in Fig. 5.8 shows that ± 3.0 volts is required to bias up the amplifier, and the "on" current is about $400 \mu\text{A}$. The total power dissipation is 6 mW for ± 7.5 volt supplies.

5.1.7. Slew-Rate Performance

Slew-rate and settling time can affect the accuracy and distortion performance of switched capacitor filters. The measured unity-gain transient performance for ± 1 volt steps is shown in Fig. 5.9. For a load capacitance of 13 pF, and a 10 pF compensation capacitance, the measured slew-rate is about 1 volt/ μsec .

5.1.8. Unity-Gain Bandwidth

Figure 5.10 shows the simulated op amp magnitude and phase response for ± 7.5 volt supplies with 5.0 volts body bias when connected in unity gain with a 10 pF load. The predicted unity-gain bandwidth is 2.5 MHz with a phase margin of 70 degrees. The measured unity-gain bandwidth was about 1.5 MHz.

5.2. DDI Switched Capacitor Fifth-Order Chebyshev Lowpass Filter

In this section, the performance of the DDI (with predistortion) switched capacitor fifth-order all-pole Chebyshev lowpass filter shown schematically in Fig. 5.11 is described. It was integrated using the NMOS depletion-load metal-gate

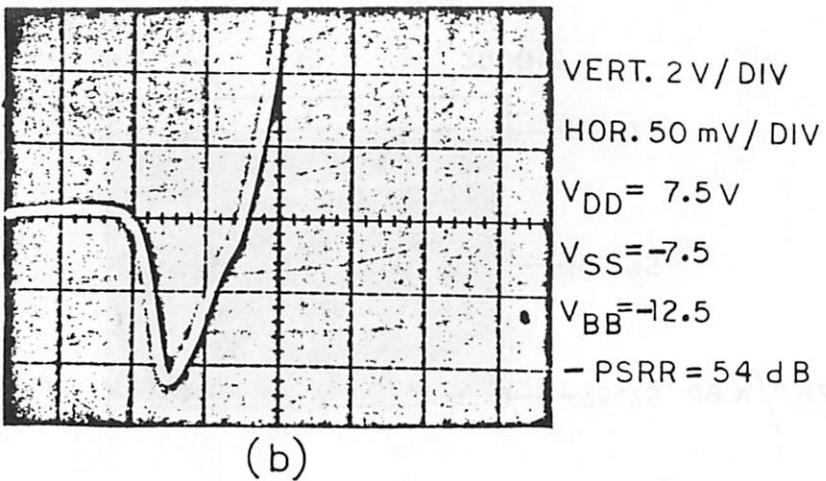
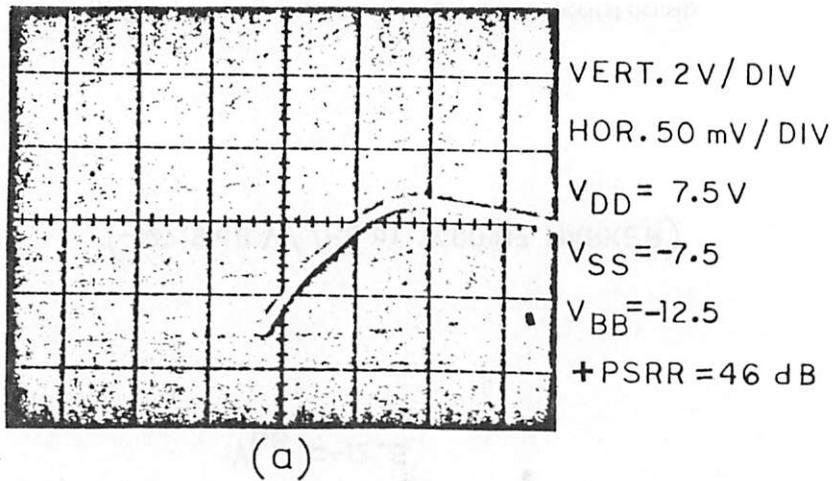


Fig. 5.7. Measured op amp PSRR.

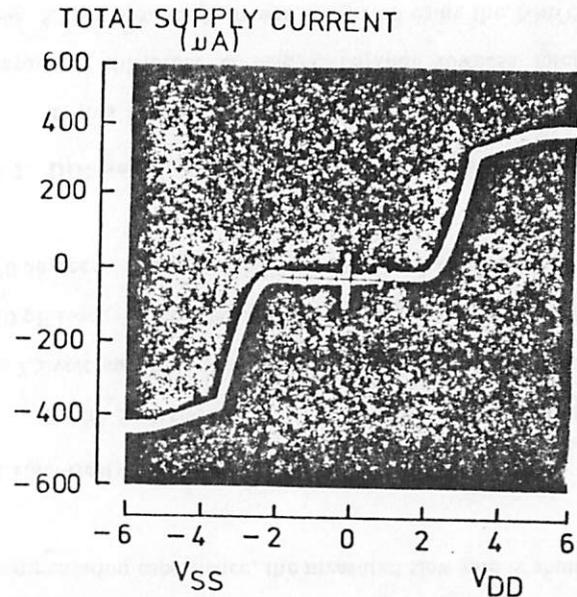


Fig. 5.8. Op amp supply current versus power supply voltage.

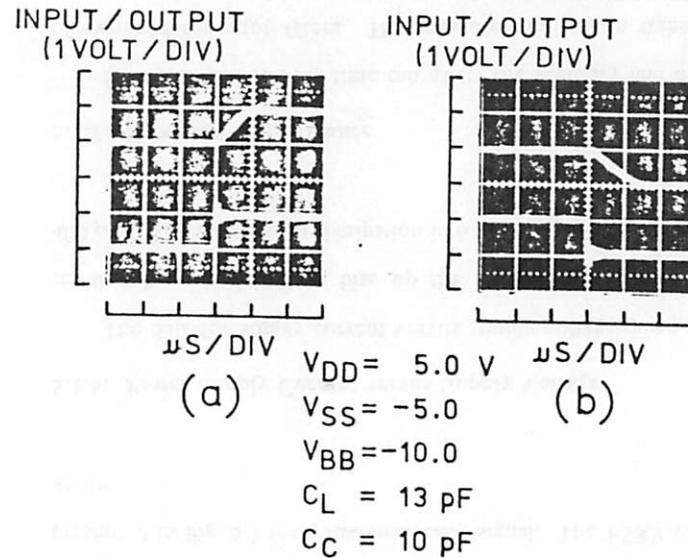


Fig. 5.9. Measured op amp slew-rate performance.

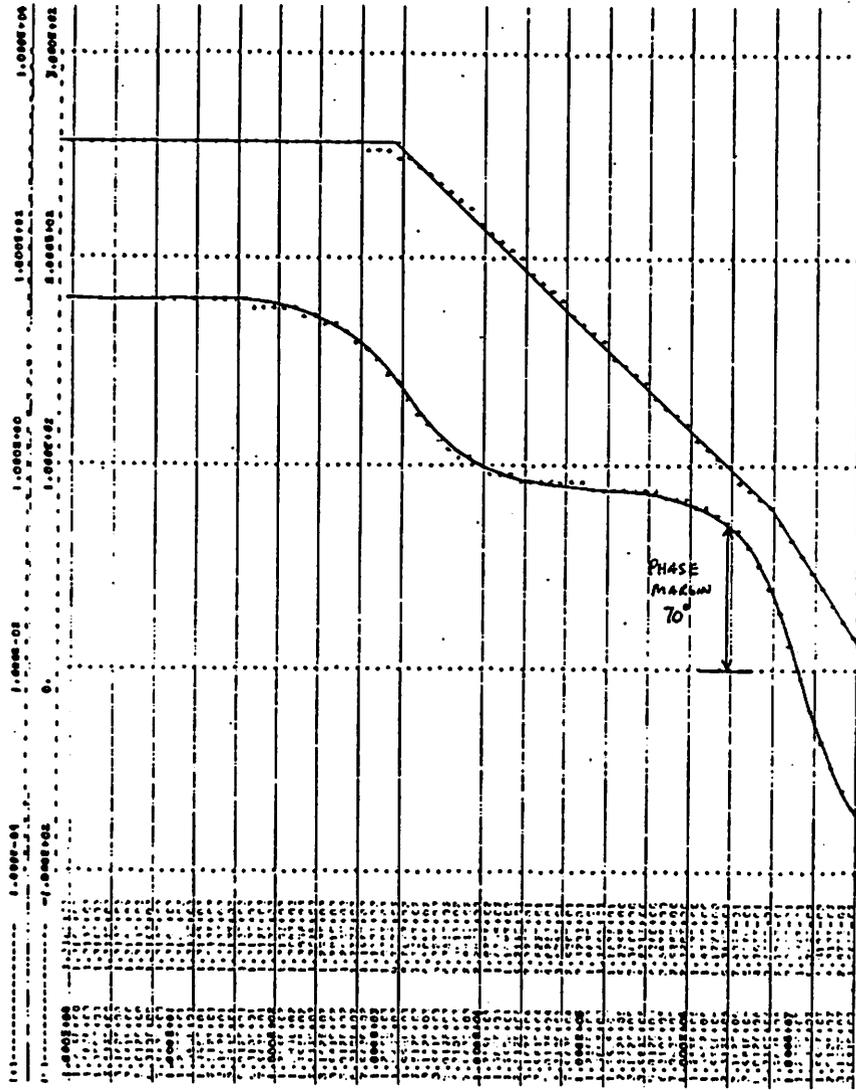


Fig. 5.10. Simulated op amp gain/phase responses.

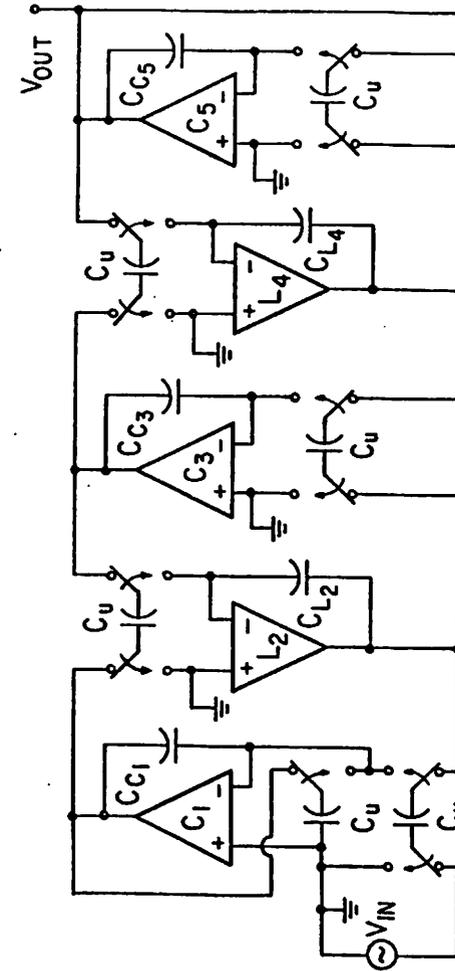


Fig. 5.11. A switched capacitor DDI fifth-order all-pole lowpass ladder filter.

process of Appendix 1. The die photograph is shown in Fig. 5.12. The lower right corner contains an operational amplifier which required a die area of about 400 mil². The test transistors are on the upper right, and the fifth-order lowpass filter is shown in the left portion of the die photo. The operational amplifiers, and switched capacitors are embedded in the center, surrounded by the five integrating capacitors which range in size from about 10 pF to about 40 pF. The switched capacitors are each about 2.3 pF. The overall die size is 98 mils by 105 mils, and the filter is approximately 70 mils by 90 mils.

5.2.1. Frequency Response

The measured frequency response for a sampling rate of 128 kHz is given in Fig. 5.13. Figure 5.13(a) shows the response over a large frequency range. The typical stop-band rejection is about 80 dB. The details of the passband are presented in Fig. 5.13(b). The measured ripple bandwidth and total passband ripple are in excellent agreement with the design goals of 3400 Hz and 0.1 dB, respectively.

Figure 5.14(a) shows the frequency response over a very wide frequency range. The first alias term at 128 kHz is apparent.

5.2.2. Frequency Response versus Sampling Rate

The gain constant of a switched capacitor integrator is directly proportional to the sampling frequency. Hence, the cutoff frequency of switched capacitor filters scales linearly with f_c . This is illustrated in Fig. 5.15 which shows the response for several different sampling rates. Note that the passband ripple remains constant. This feature provides one possible degree of freedom for designing programmable filters which will be described in greater detail in Chapter 6.

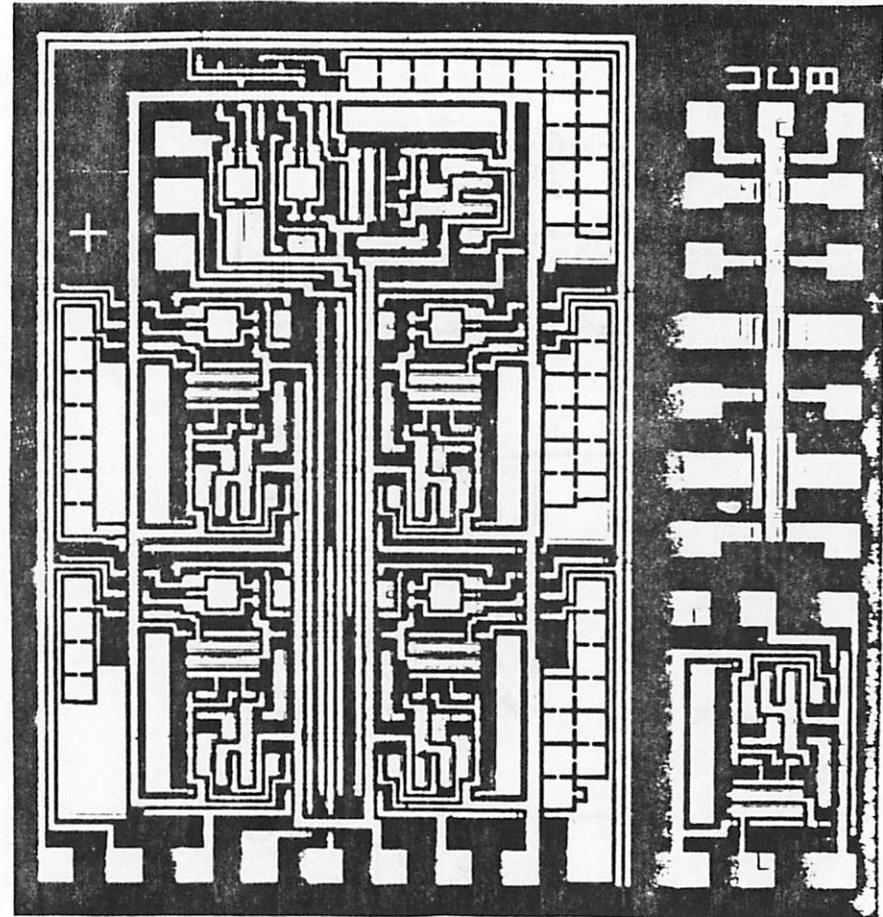
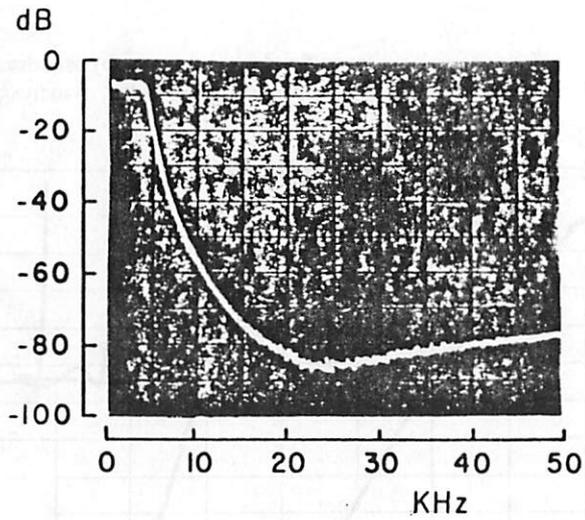
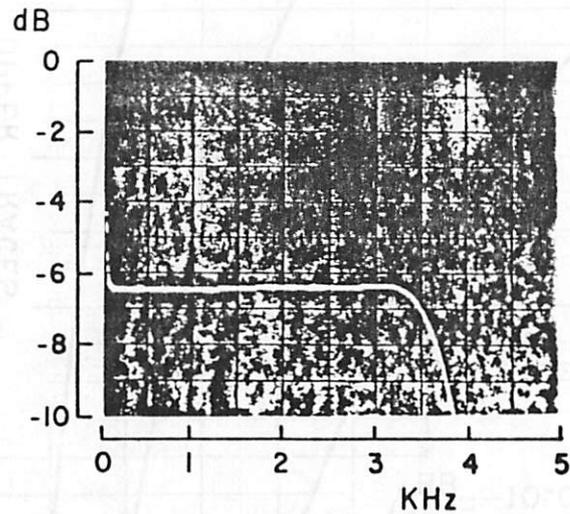


Fig. 5.12. Die photo of the fifth-order switched capacitor lowpass ladder filter, test operational amplifier, and test transistor array. Die size is 98 mils by 105 mils.

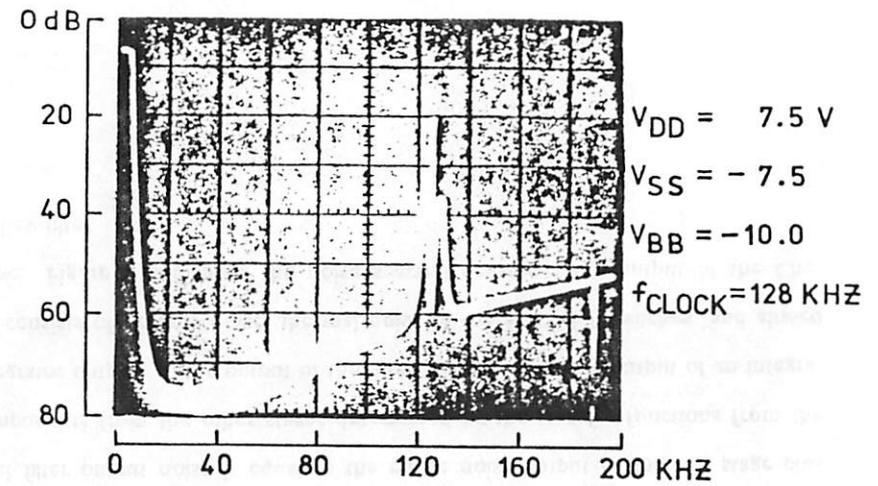


(a)

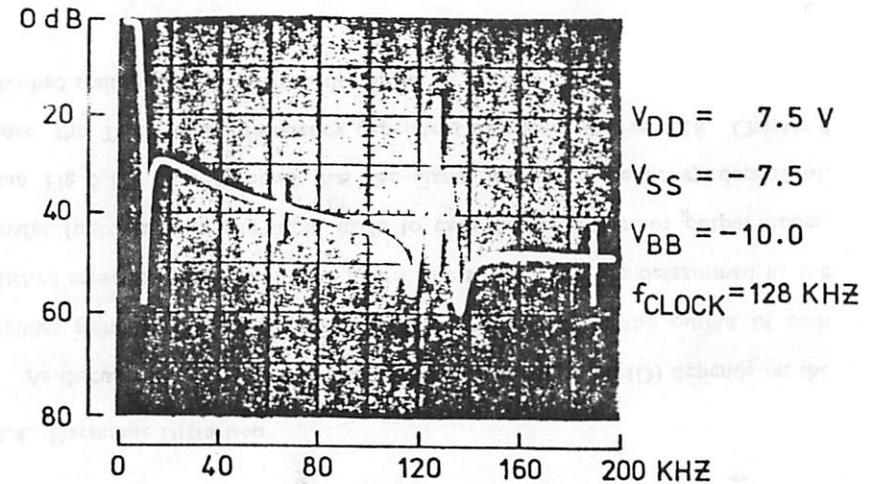


(b)

Fig. 5.13. (a) Measured frequency response for the fifth-order Chebyshev lowpass DDI switched capacitor filter with predistortion at 128 kHz sampling rate, and (b) the passband details.



(a)



(b)

Fig. 5.14. Measured switched capacitor lowpass frequency responses showing 128 kHz alias term. (a) Fifth-order Chebyshev lowpass filter; (b) Third-order elliptic lowpass filter.

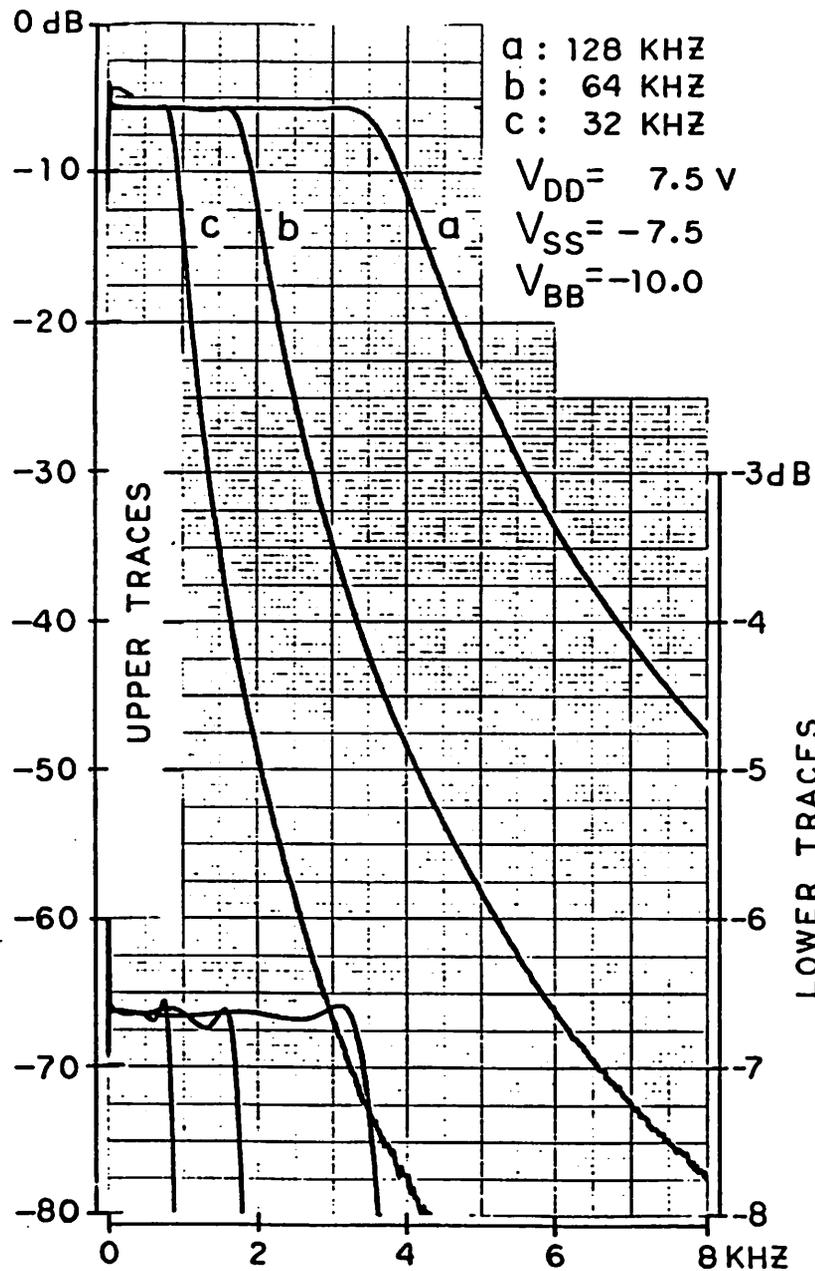


Fig. 5.15. Switched capacitor fifth-order Chebyshev lowpass frequency response for different sampling rates.

5.2.3. Frequency Response versus Power Supply Variations

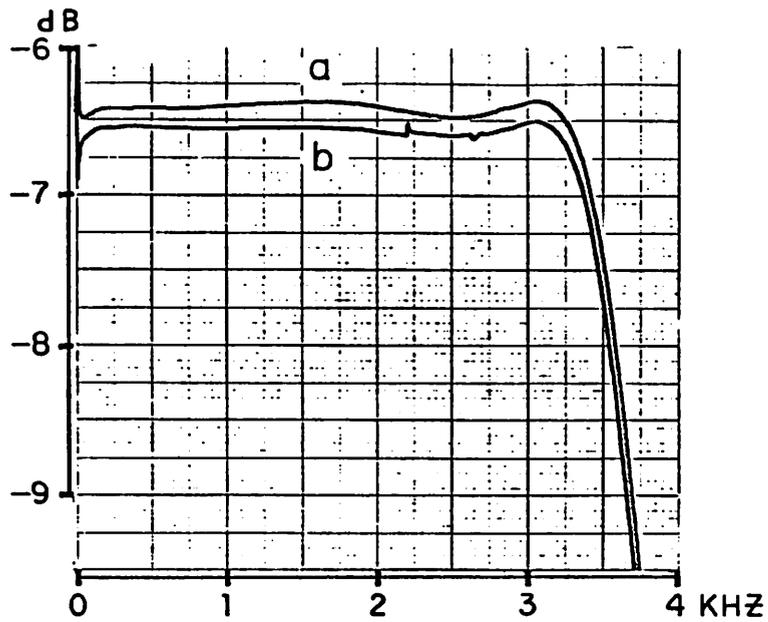
When the power supplies were changed from ± 7.5 volts to ± 5.0 volts, the responses of Fig. 5.16 were obtained. The small changes in the response illustrates the low sensitivity of the doubly-terminated switched capacitor ladder structure. The supply voltage coefficient of absolute gain at 1 kHz is 0.03 dB/volt.

5.2.4. Harmonic Distortion

As discussed in Chapter 4, Total Harmonic Distortion (THD) depends on the amplifier gain characteristics as well as the signal levels at the output of each switched capacitor integrator in the filter. The signal levels are determined by the transfer function from the input node to each of the integrator output nodes. From Fig. 5.17, it is apparent that the signal levels are frequency dependent. Hence, the THD is also frequency dependent as shown in Fig. 5.18. Chapter 4 described scaling techniques to reduce THD.

5.2.5. Noise Performance

Noise considerations were presented in Chapter 4 where it was shown that the total filter output noise is equal to the entire noise output of the last stage plus components from the other stages determined by the transfer functions from the integrator outputs to the output of the filter. The noise at the output of an integrator consists of op amp noise, thermal noise of the MOSFET switches, and aliased noise. Figure 5.19 displays the noise spectral density at the output of the Chebyshev filter.



TRACE a:

$$V_{DD} = 7.5 \text{ V}$$

$$V_{SS} = -7.5$$

$$V_{BB} = -10.0$$

TRACE b:

$$V_{DD} = 5.0 \text{ V}$$

$$V_{SS} = -5.0$$

$$V_{BB} = -7.5$$

Fig. 5.16. Switched capacitor Chebyshev lowpass fifth-order passband frequency responses at different power supply voltages.

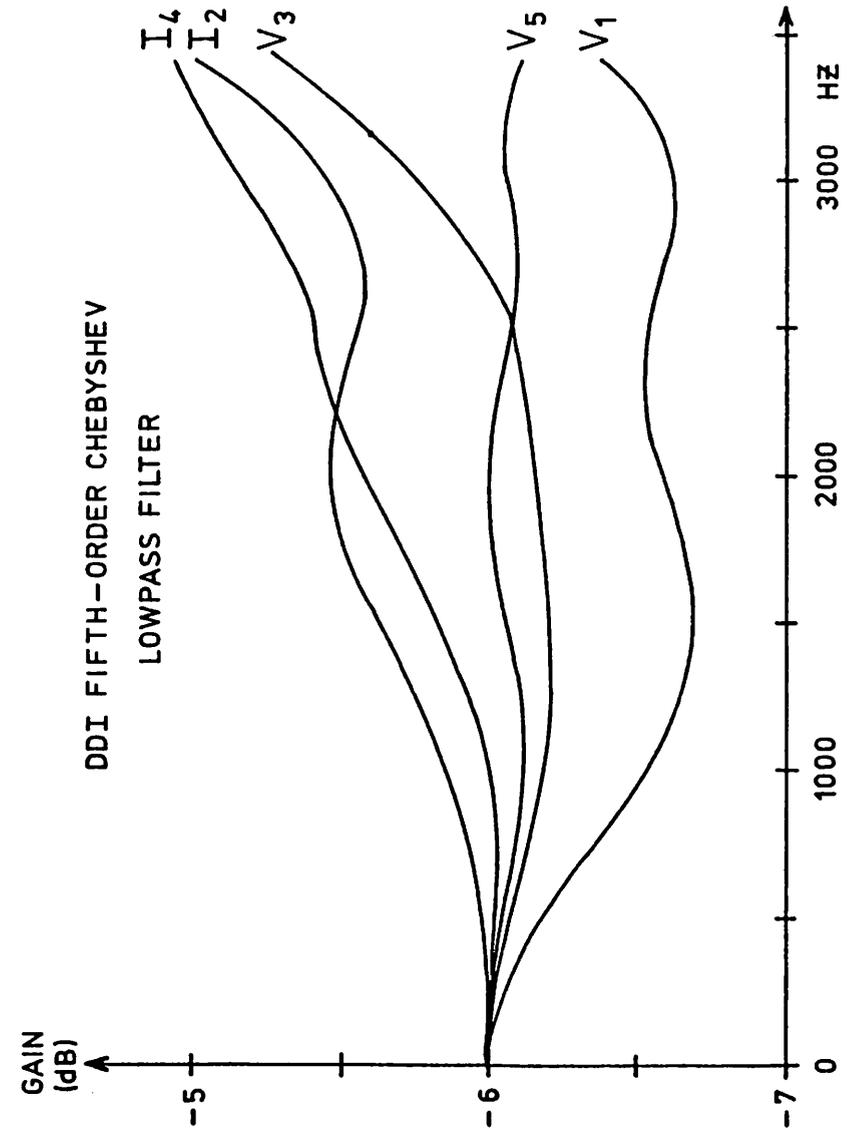


Fig. 5.17. Switched capacitor fifth-order Chebyshev internal-node transfer functions relative to the input voltage.

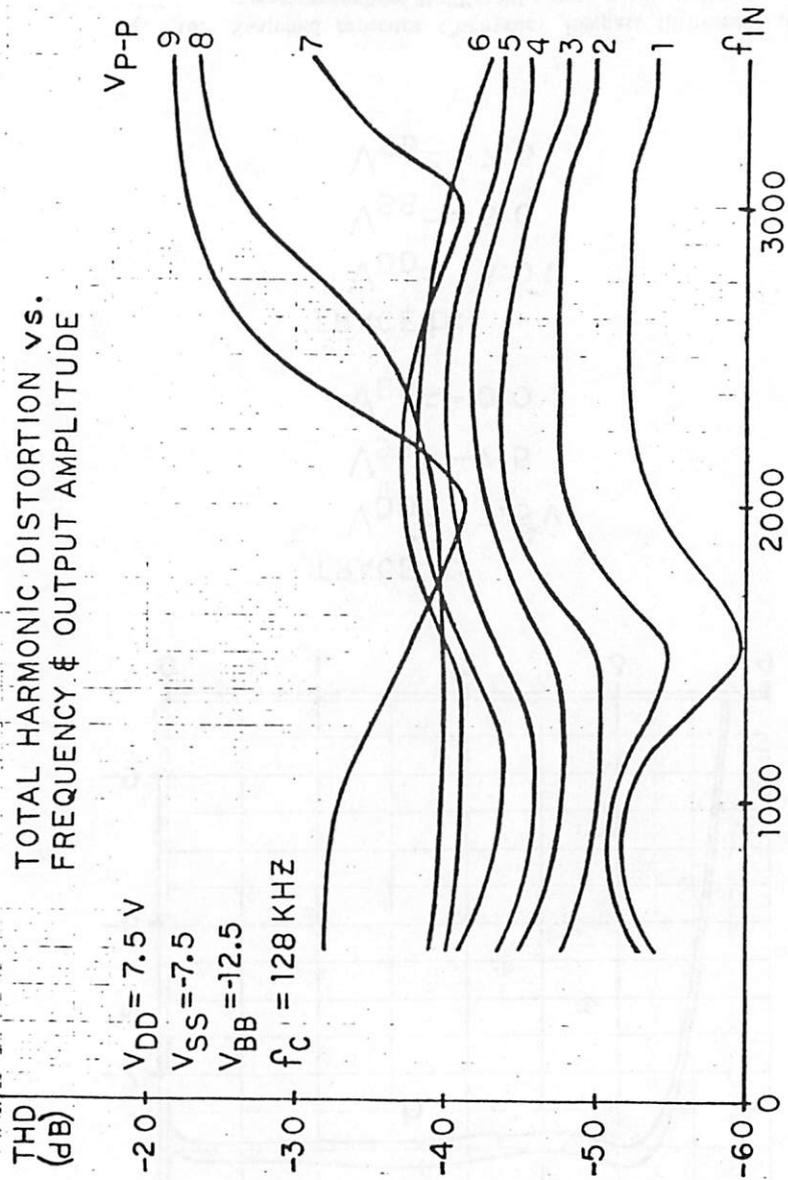
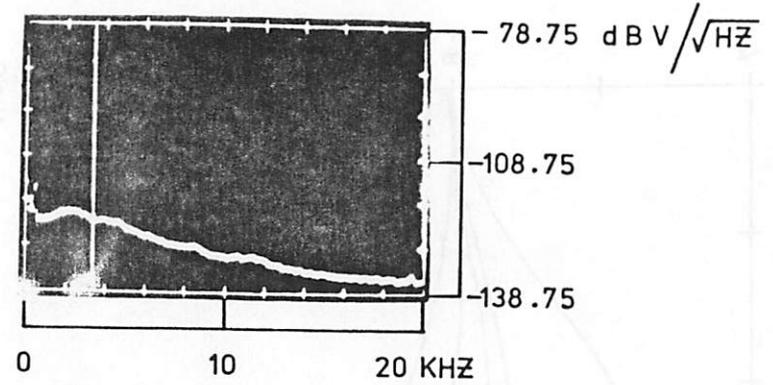


Fig. 5.18. THD performance of the fifth-order switched capacitor Chebyshev lowpass ladder filter.



$V_{DD} = 7.5 \text{ V}$
 $V_{SS} = -7.5$
 $V_{BB} = -12.5$
 $f_{\text{CLOCK}} = 128 \text{ KHZ}$

(-122.9 $\text{dBV}/\sqrt{\text{Hz}}$ at 3400 HZ MARKER)

Fig. 5.19. Noise spectral density of the Chebyshev fifth-order switched capacitor lowpass ladder filter.

5.3. LDI Switched Capacitor Third-Order Elliptic Lowpass Filter

In this section, the performance of the type-I LDI switched capacitor three-pole, two-zero elliptic lowpass filter of Fig. 5.20 is described. The die photograph is shown in Fig. 5.21. The three operational amplifiers with their associated switched capacitors are shown in the right portion, while the integrating and zero-forming capacitors are along the left portion of the photo. The zero-forming capacitors are about 2 pF each, and are directly below the first and third integrating capacitors. The integrating capacitors vary in size between 15 and 20 pF. The die size is 40 mils by 110 mils.

5.3.1. Frequency Response

The measured frequency response for a sampling rate of 128 kHz is given in Fig. 5.22. Figure 5.22(a) shows the response over a wide range of frequencies. The minimum stop-band rejection is about 30 dB with a transmission zero at about 9 kHz. The details of the passband are shown in Fig. 5.22(b). The measured ripple bandwidth and total passband ripple are in excellent agreement with the design goals of 3400 Hz, and 0.13 dB, respectively. A statistical distribution of insertion loss, clipping level, and passband ripple are displayed in the histogram of Fig. 5.23 based on a sample size of 9 from a single processing run. Excellent process tracking appears feasible with this approach.

Fig. 5.14(b) shows the alias term at 128 kHz.

Note that the insertion loss for this filter is 0 dB while the insertion loss of the RLC doubly-terminated ladder prototype is 6 dB. In switched capacitor filters, the insertion loss can be scaled by simply changing the size of the input switched capacitor relative to the other switched capacitors. For example, the input capacitor, shown at the bottom of Fig. 5.21, was doubled in the elliptic filter to increase the

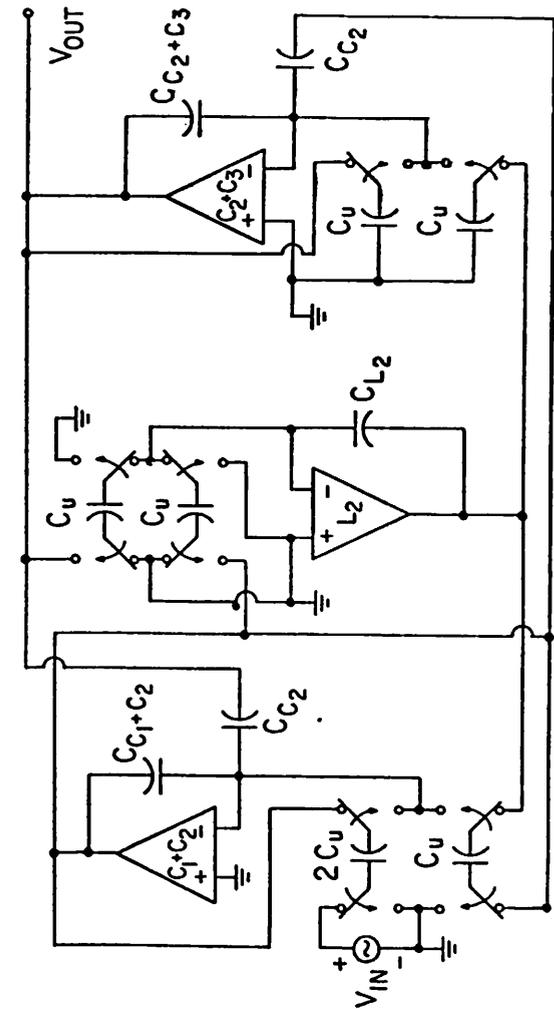


Fig. 5.20. Third-order elliptic lowpass type-I LDI switched capacitor ladder filter.

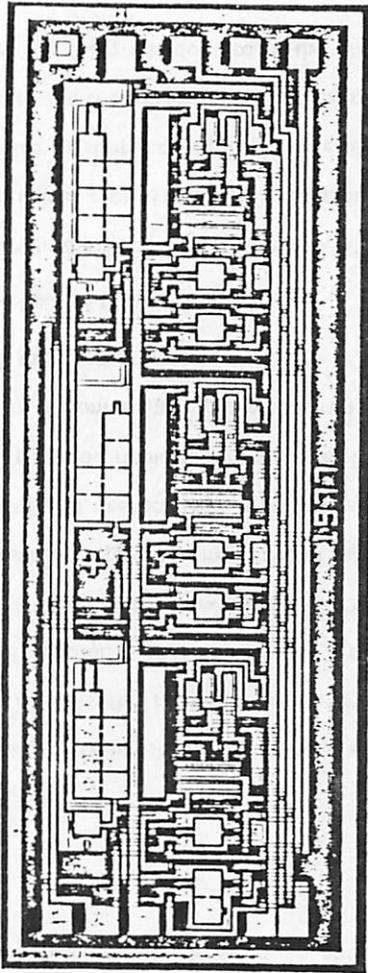
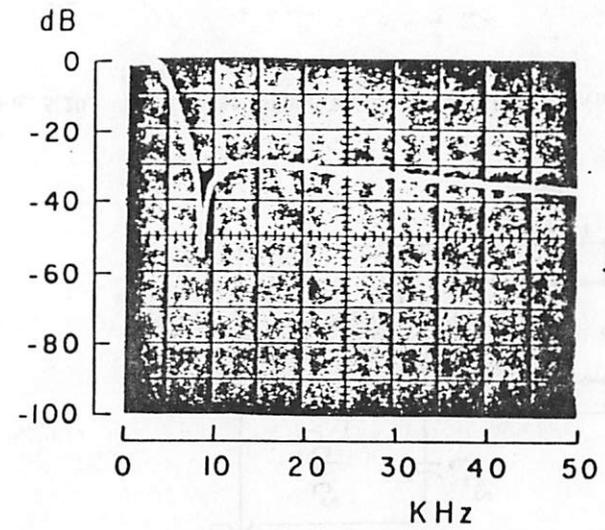
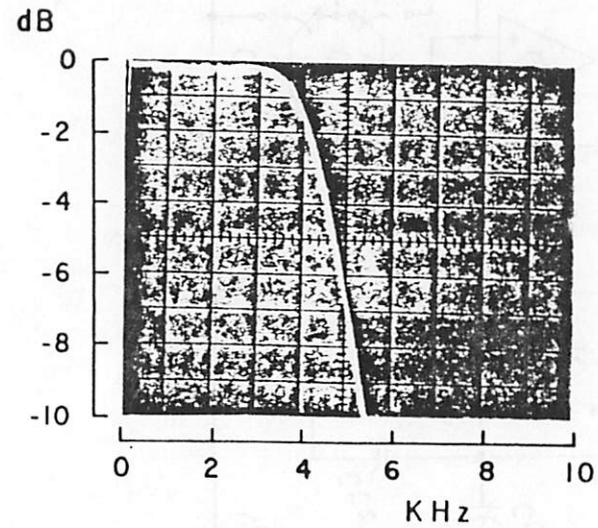


Fig. 5.21. Die photo of the third-order elliptic lowpass switched capacitor ladder filter.



(a)



(b)

Fig. 5.22. (a) Measured frequency response for the third-order elliptic switched capacitor lowpass ladder filter clocked at 128 kHz, and (b) the passband details.

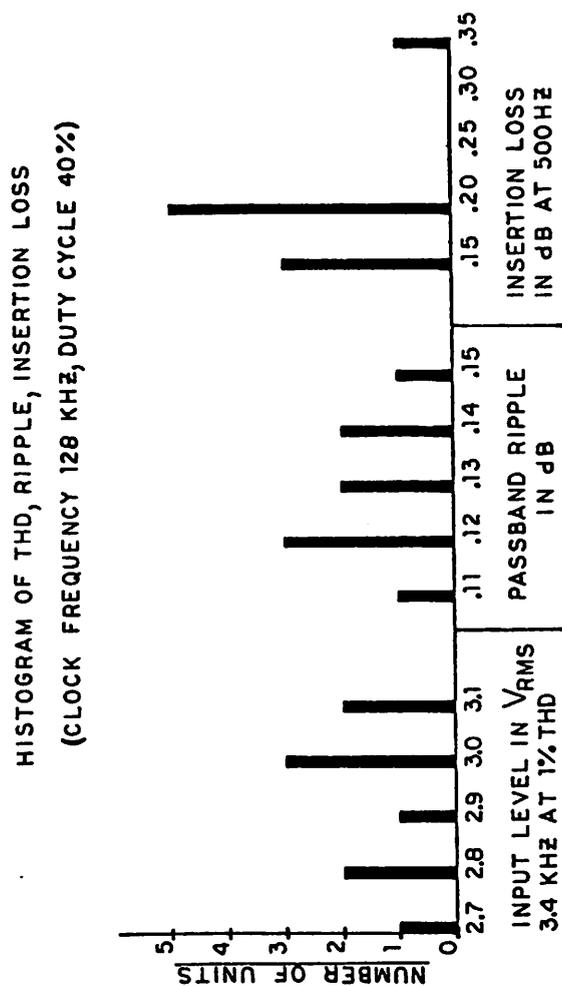


Fig. 5.23. Histogram of passband ripple, insertion loss and THD for a sample of 9 (third-order elliptic switched capacitor lowpass ladder filters.

gain by 6 dB, thus reducing the insertion loss to 0 dB.

5.3.2. Frequency Response versus Sampling Rate

Figure 5.24 shows the filter response for several values of clock frequency. In Fig. 5.24(a), the response scales with low sampling rates until the leakage current is significant during the long integration periods. For this particular example, the minimum sampling rate is about 1 kHz. Fig. 5.24(b) shows the scaled responses for several intermediate sampling frequencies, and Fig. 5.24(c) shows the response at high sampling rates. At sampling frequencies above 300 kHz, the slewing and settling errors in the amplifiers distort the frequency response. However, other workers with higher performance amplifiers have observed that sampling frequencies approaching 1 MHz can be used before significant distortion occurs [45],[51]. Figure 5.25 illustrates the clipping level, noise, and passband ripple as a function of clock frequency.

5.3.3. Frequency Response versus Power Supply Voltages

The measured frequency response for different power supplies is presented in Fig. 5.26. The supply voltage coefficient of absolute gain at 1 kHz is 0.03 dB/volt.

5.3.4. Harmonic Distortion

The transfer functions from the filter input to each internal integrator output are shown as functions of frequency in Fig. 5.27. The measured THD versus frequency is presented in Fig. 5.28, and THD versus signal level for a 1 kHz input is shown in Fig. 5.29. For signal levels of about 0.3 volts RMS, THD is less than 0.1%. The increase in distortion at lower signal levels is due to the slight amount of crossover distortion in the op amp transfer characteristics of Fig. 5.2.

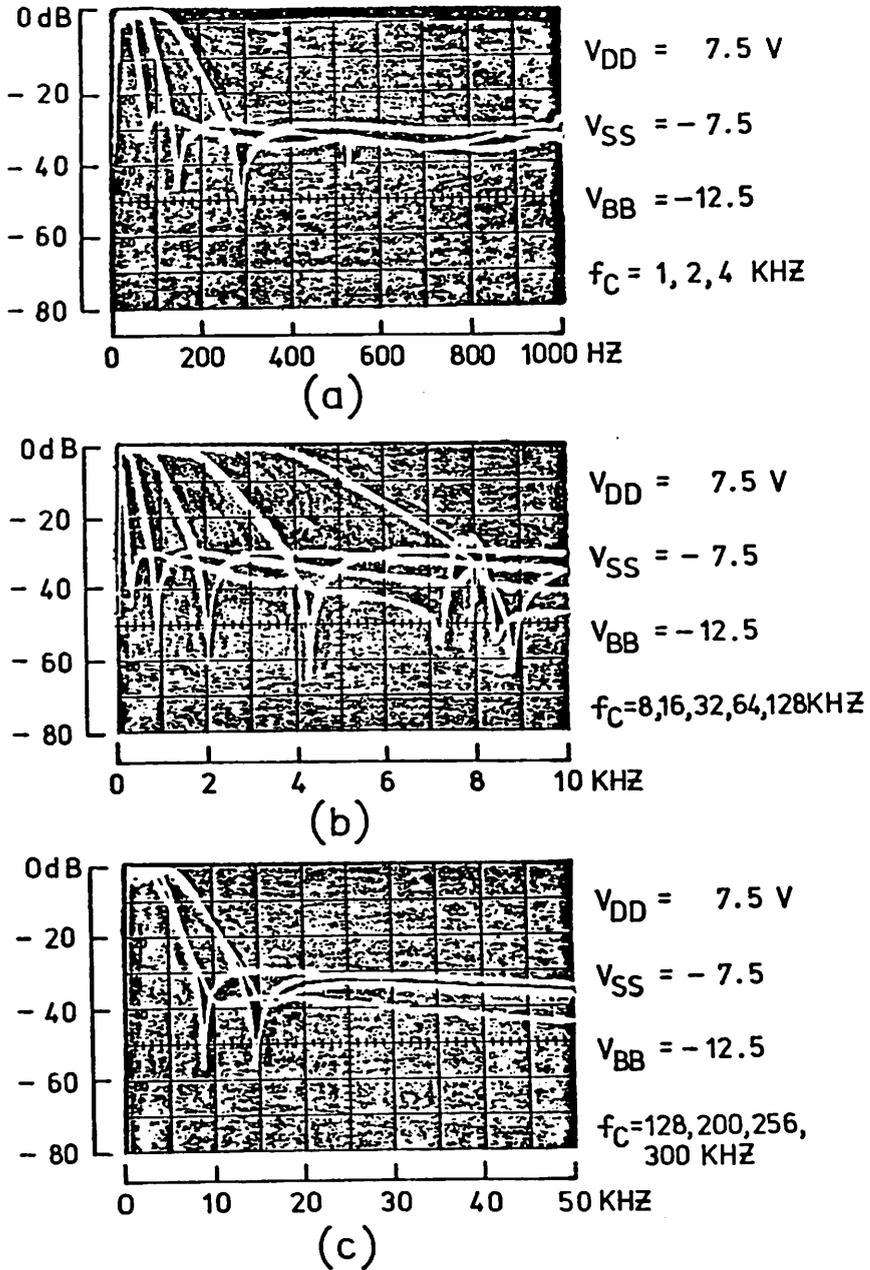


Fig. 5.24. Switched capacitor third-order elliptic lowpass frequency response versus sampling rate.

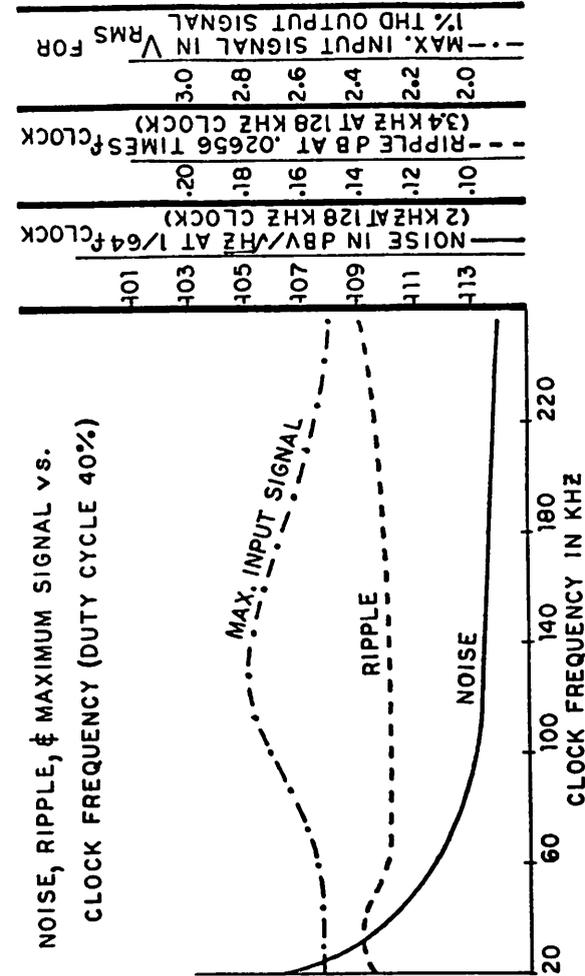


Fig. 5.25. Measured noise spectral density, passband ripple and clipping level versus clock rate for the elliptic third-order switched capacitor lowpass ladder filter.

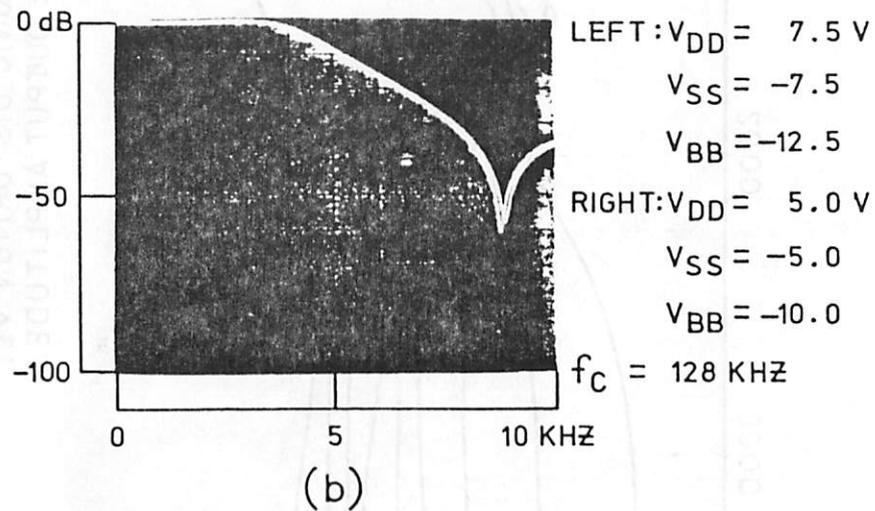
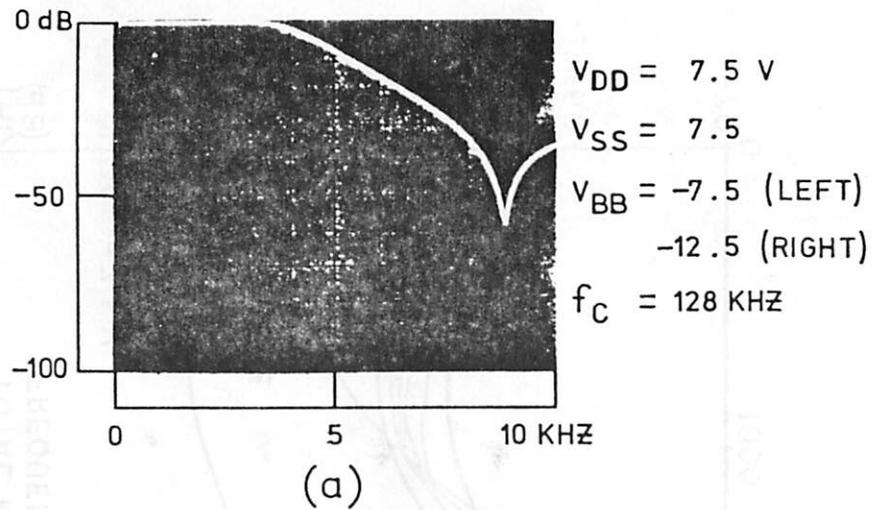


Fig. 5.26. Switched capacitor third-order elliptic lowpass frequency response for different power supply voltages.

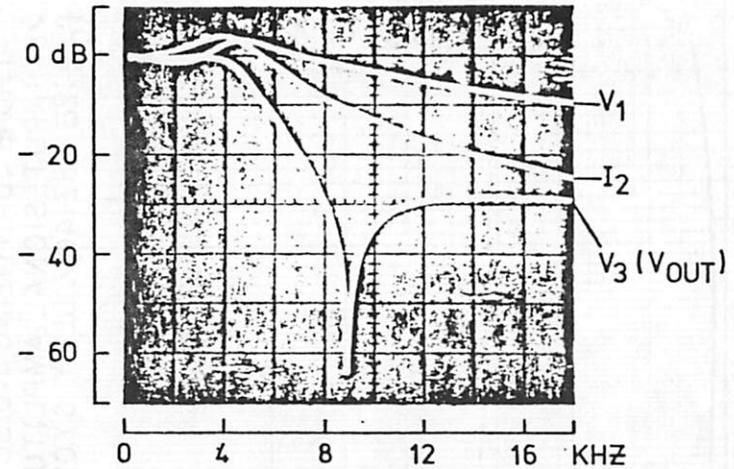


Fig. 5.27. Switched capacitor third-order elliptic lowpass internal-node transfer functions relative to the input.

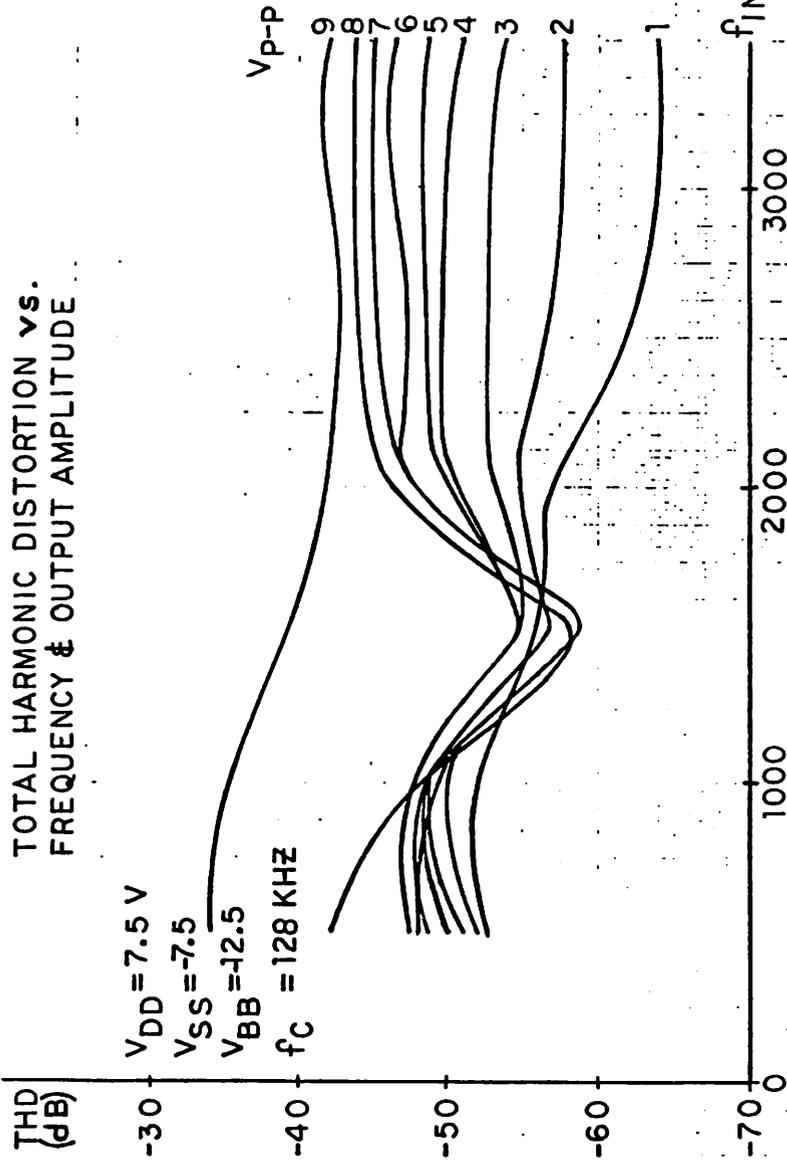


Fig. 5.28. Measured THD performance of the third-order elliptic switched capacitor lowpass ladder filter.

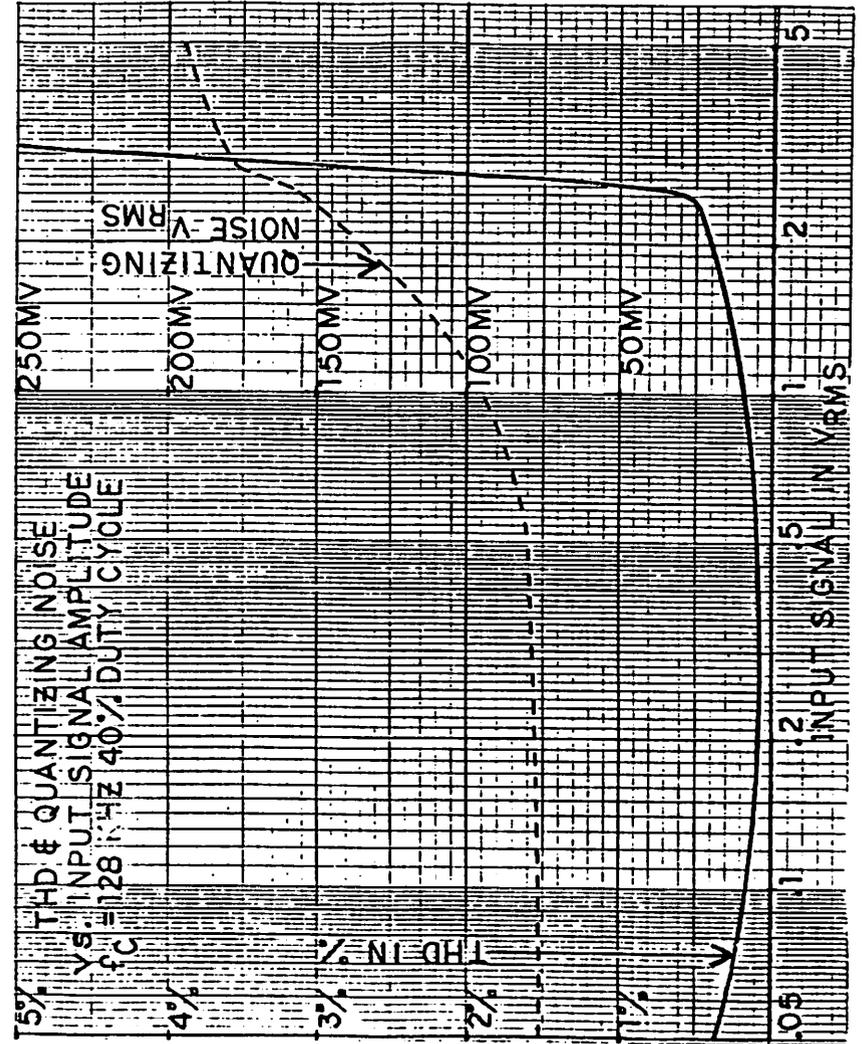


Fig. 5.29. THD and quantizing noise versus input amplitude for the switched capacitor third-order elliptic lowpass ladder filter. Quantizing noise is the noise measured at the sampling frequency in a 1 Hz bandwidth.

5.3.5. Noise Performance

The output noise spectral density versus frequency is pictured in Fig. 5.30 for a spectrum analyzer bandwidth of 100 Hz. The sampling rate was 128 kHz.

5.3.6. Power Supply Rejection

The measured supply rejection is presented in Fig. 5.31 for all power supplies and clocks. The rejection can be increased by more careful layout which includes shielding wherever required. Higher performance amplifiers would also improve this specification.

5.3.7. Phase Sensitivity

The phase at the 3400 Hz cutoff frequency was measured for different samples with variations in clock frequency, clock duty cycle, and temperature. The results given in Table II show that the switched capacitor doubly-terminated ladder filters have very low phase sensitivity in addition to low magnitude sensitivity.

5.3.8. Temperature Performance

Three samples were tested at 0, 25, and 65 degrees C. Noise remained constant over temperature; the insertion loss at 1000 Hz changed less than 0.1 dB, and the passband ripple changed less than 0.05 dB for a 2.8 V_{RMS} input signal. The temperature coefficient of absolute gain at 1 kHz was about 0.0006 dB/°C.

5.3.9. Intermodulation Distortion

The measured intermodulation distortion versus applied signal level is displayed in Fig. 5.32.

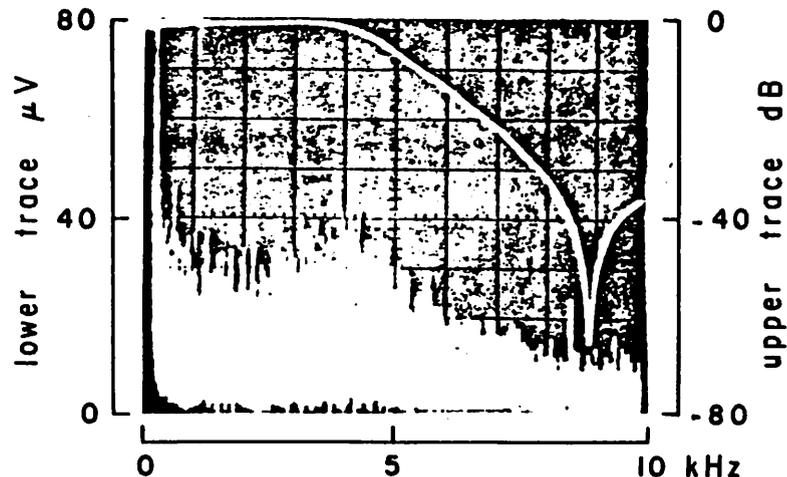


Fig. 5.30. Output noise for the third-order elliptic lowpass switched capacitor ladder filter. Analyzer bandwidth is 100 Hz.

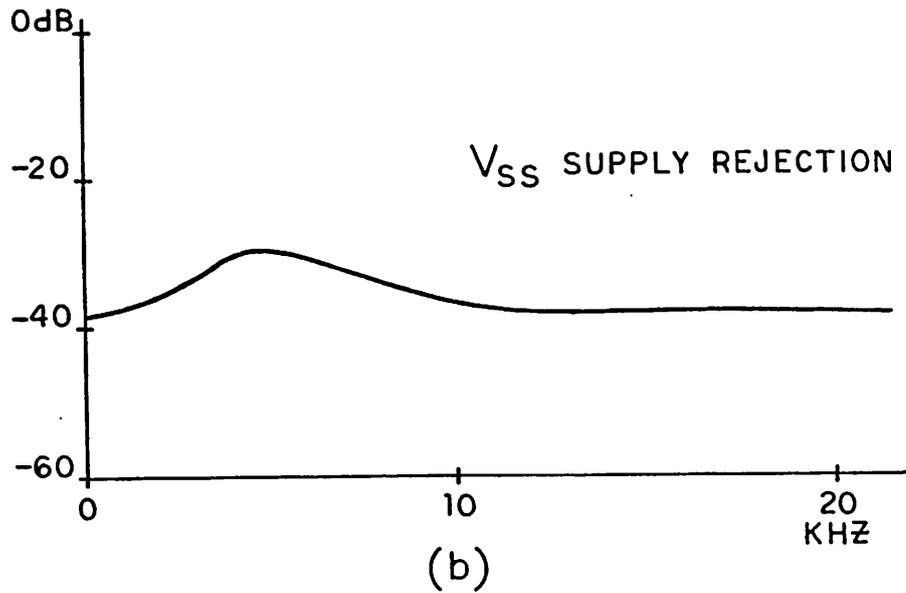
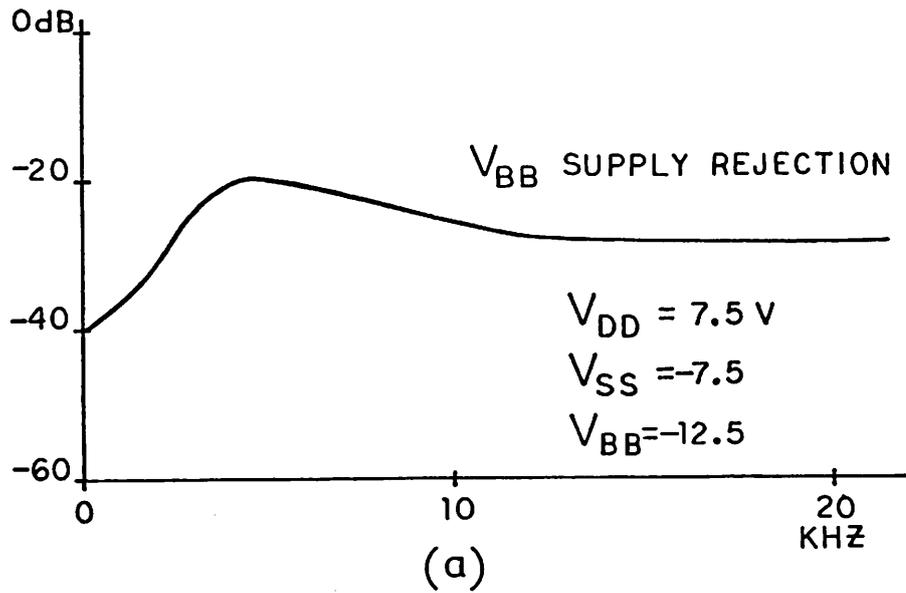


Fig. 5.31. Measured power supply rejection for the third-order elliptic lowpass switched capacitor ladder filter. (a) V_{BB} supply; (b) V_{SS} supply.

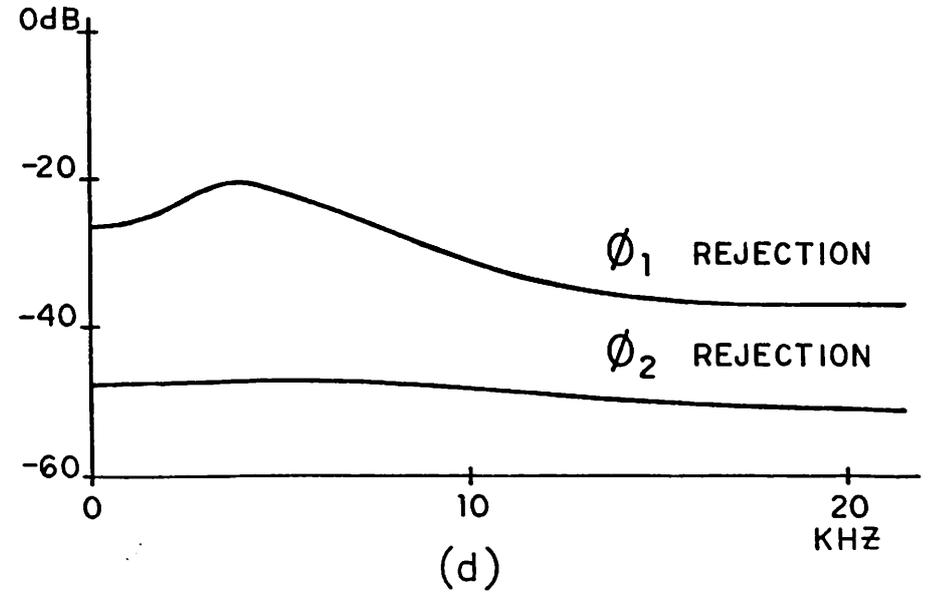
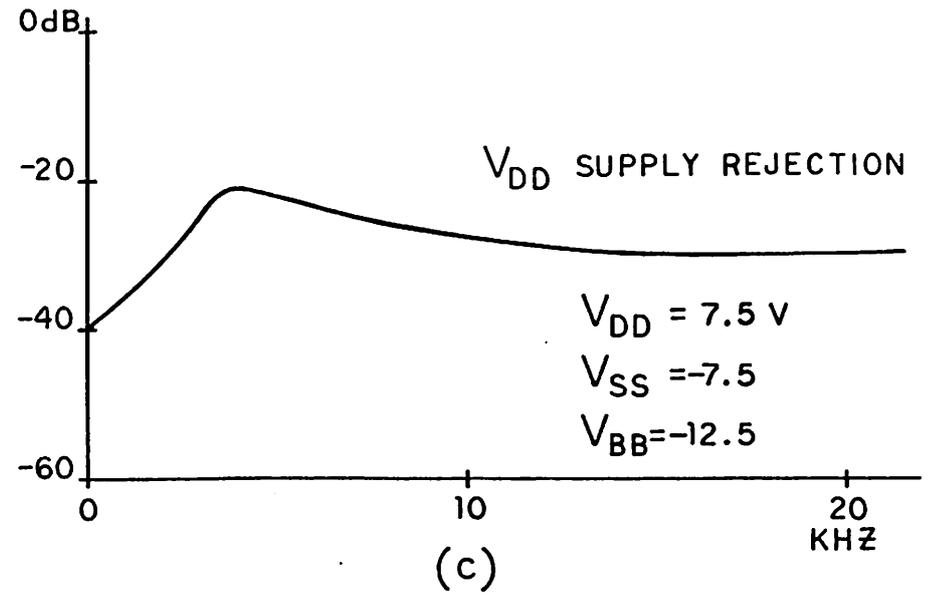


Fig. 5.31. Measured power supply rejection for the third-order elliptic lowpass switched capacitor ladder filter. (c) V_{DD} supply; (d) clocks.

| SAMPLE NO. | 1 | 2 | 3 | |
|------------|--------|-------|--|-------|
| I | 16 KHZ | 81.8° | 82.0° | 83.0° |
| | 32 | 81.8 | 82.2 | 83.1 |
| | 64 | 81.9 | 82.2 | 83.1 |
| | 128 | 81.6 | 81.8 | 82.6 |
| | 256 | 80.8 | 81.2 | 82.3 |
| II | 0 °C | 80.5° | 80.9° | 81.8° |
| | 25 | 81.2 | 81.5 | 82.3 |
| | 65 | 80.0 | 80.7 | 81.3 |
| III | 40% | 81.4° | NOTE: DATA IN I AND II ASSUMES 40% DUTY CYCLE | |
| | 30 | 80.2 | | |
| | 20 | 79.6 | | |
| | 10 | 81.1 | | |
| | 5 | 74.6 | | |

Table II. Measured phase sensitivity for the third-order type-I LDI switched capacitor ladder filter.

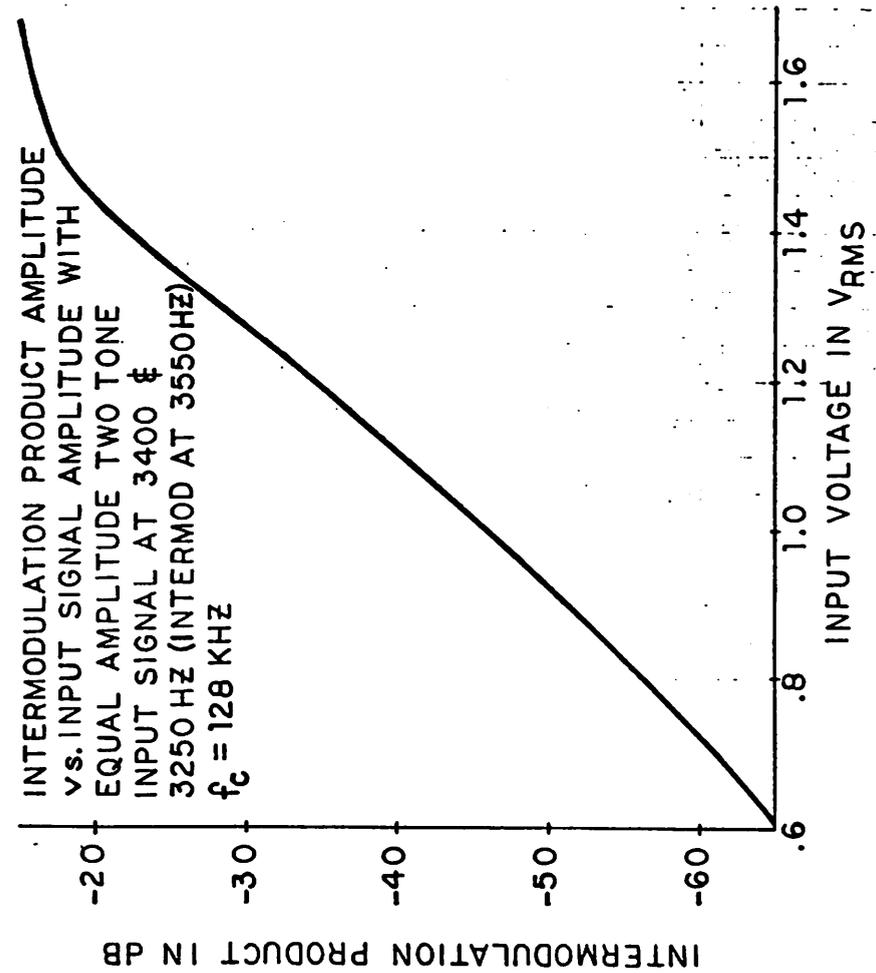
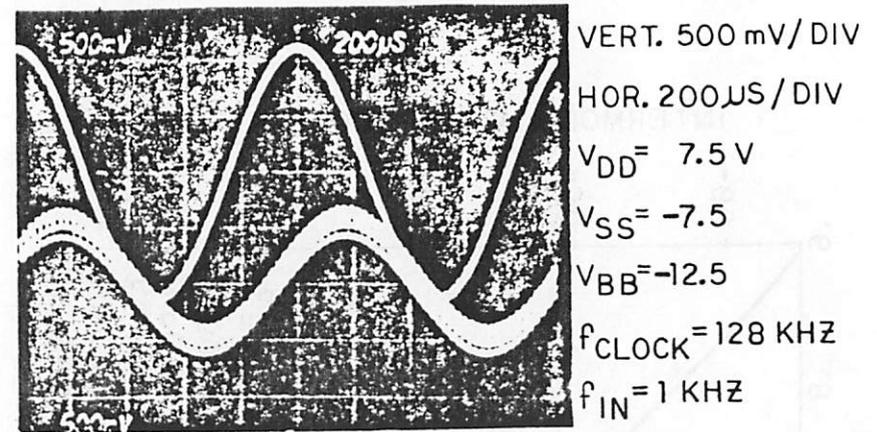


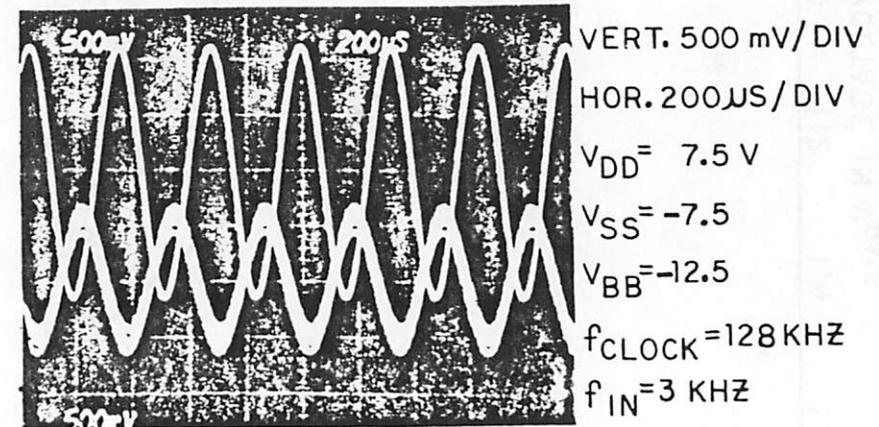
Fig. 5.32. Measured intermodulation distortion (IM) for the third-order elliptic lowpass switched capacitor ladder filter.

5.3.10. Quantizing Noise

The output of switched capacitor filters changes in small steps at each integration time as shown in Fig. 5.33. Hence, there are components at the clock frequency due both to clock feedthrough and to signal transitions. In this context, quantizing noise is defined as the total magnitude of the signal at the sampling frequency in a 1 Hz bandwidth, and is displayed in Fig. 5.29. When the input signal is very small, the quantizing noise is due almost entirely to clock feedthrough which for the metal-gate process used in these experiments is about 75 mV.



(a)



(b)

Fig. 5.33. Output waveforms for the third-order elliptic lowpass switched capacitor ladder filter clocked at 128 kHz.

AN ELECTRICALLY-PROGRAMMABLE SWITCHED CAPACITOR FILTER

Switched capacitor techniques have been used to integrate frequency selective filters using standard MOS technology [11],[13]-[15],[24]-[25]. In determining the usefulness of this approach for a given application, the obvious advantages of integration such as small size and low manufacturing cost must be weighed against the disadvantages of the cost and time required to mask program a desired filter response. This restricts the usefulness of these filters to those applications with sufficient manufacturing volume to justify the expense of mask programming, and it completely eliminates their use in applications that require a time-varying response such as adaptive filters and speech and music synthesizers. A monolithic filter which can be programmed by the application of digital control signals would therefore find widespread use, and is the subject of this chapter [59].

6.1. Synthesis of the Programmable Second-Order Section

In this section, the synthesis approach will be described using s-plane notation. The singly-terminated RLC second-order lowpass filter shown in Fig. 6.1(a) was chosen as the prototype for this design because it can be configured in an active form in which the peak gain (G), selectivity (Q), and center frequency (ω_0) are independently programmable. To illustrate this very important point, compare the general form of the transfer function for a second-order lowpass filter which is given by

$$H(s) = \frac{k}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{6.1}$$

where k is a constant, to the transfer function for the RLC circuit of Fig. 6.1(a)

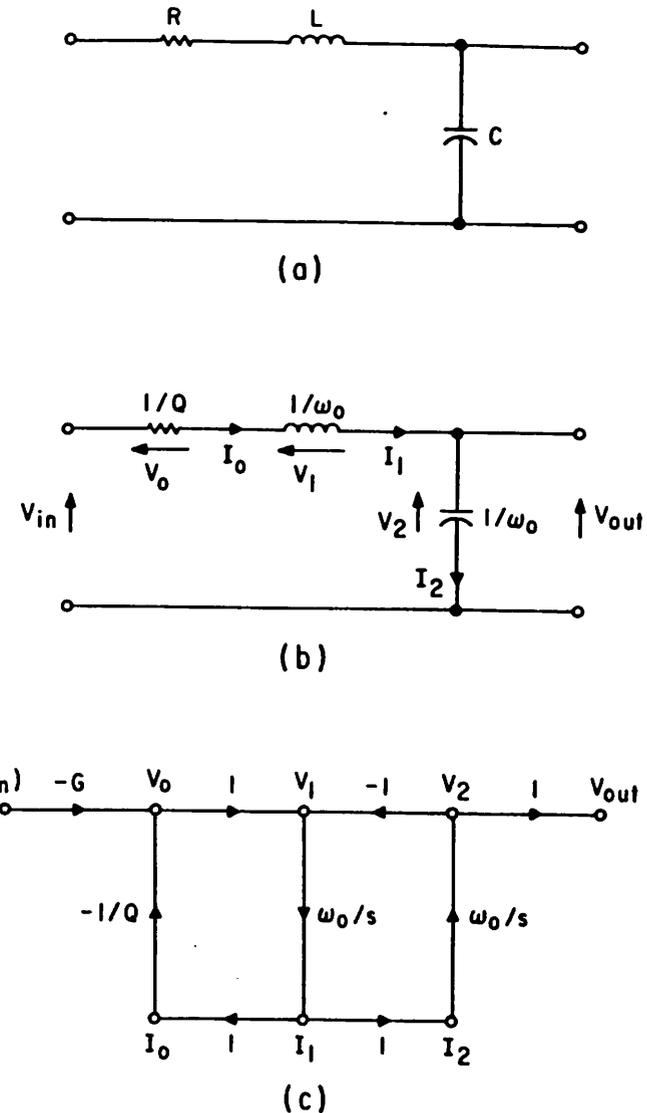


Fig. 6.1. (a) The singly-terminated RLC second-order lowpass prototype and (b) an equivalent form after impedance scaling; (c) the corresponding signal flowgraph.

which is given by

$$H(s) = \frac{\frac{1}{LC}}{s^2 + s\frac{R}{L} + \frac{1}{LC}} \quad (6.2)$$

In order to obtain programmability, Eqns. (6.1) and (6.2) are equated to solve for L and C in terms of ω_0 and Q to obtain:

$$L = \frac{RQ}{\omega_0} \quad (6.3a)$$

and

$$C = \frac{1}{RQ\omega_0} \quad (6.3b)$$

For given values of R and ω_0 , it is apparent that the values for L and C become widely separated (proportional to Q^2) as Q becomes large which is undesirable since it would result in a similar spread in the required capacitor ratios in a switched capacitor implementation. Fortunately, a significant improvement is obtained if the impedances are scaled so that the termination resistance, R, is equal to $\frac{1}{Q}$ since the

L and C values then become

$$L = \frac{\left[\frac{1}{Q}\right]Q}{\omega_0} = \frac{1}{\omega_0} \quad (6.4a)$$

and

$$C = \frac{1}{\left[\frac{1}{Q}\right]Q\omega_0} = \frac{1}{\omega_0} \quad (6.4b)$$

After scaling, the reactive element values are *equal* and are determined by the center frequency independently of Q and peak gain. The scaled RLC prototype is shown in Fig. 6.1(b), and a corresponding signal flowgraph is shown in Fig. 6.1(c).

The switched capacitor circuit which implements the flowgraph of Fig. 6.1(c) would usually be realized with only the two operational amplifiers required to implement the two integrators. In this case, however, the termination path presents a practical problem because for high Q, the switched capacitor which implements the $\frac{1}{Q}$ termination becomes very small (0.01pF). Therefore, it was decided to use a third operational amplifier to realize the $\frac{1}{Q}$ termination around the bandpass stage, and to set the peak gain through the filter. The third operational amplifier is used in a charge multiplier configuration as shown in Fig. 6.2 with a minimum capacitor size of $C_s=0.42$ pF. In order to insure DC stability against leakage currents and power-up transients, a switched capacitor resistor was connected across C_Q . It is interesting to note that the filter of Fig. 6.2 has the same form as a second-order state-variable filter [60]. It thus retains many of the advantageous state-variable properties including low sensitivity to component variations, and the availability of lowpass, bandpass, and bandreject outputs.

6.2. Design of the Programmable Switched Capacitor Arrays

There are several considerations in determining what type of capacitor arrays to use for programming the switched capacitor filter response. The silicon area required for the arrays should of course be minimized while maintaining a large enough unit capacitor size to provide good matching accuracy. More importantly, the arrays must be designed so that capacitor switching during dynamic programming will not distort the response or create large displacement currents. With these considerations in mind, two different types of capacitor arrays were designed for

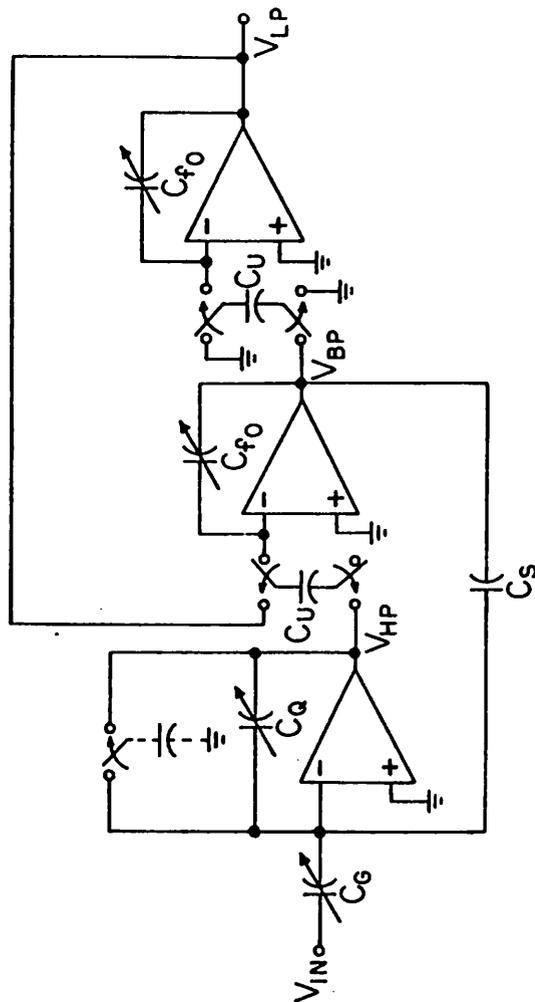


Fig. 6.2. The switched capacitor second-order electrically programmable filter.

use in the second-order programmable filter.

For the circuit Fig. 6.2, the first-order relationships between the programmable capacitor ratios, $\frac{C_Q}{C_s}$ and $\frac{C_G}{C_s}$, and the selectivity (Q) and peak gain (G) are given by

$$\frac{C_Q}{C_s} = Q \quad (6.5a)$$

and

$$\frac{C_G}{C_s} = G. \quad (6.5b)$$

Because of the linear relationships in Eqn. (6.5), six-bit binary-weighted MOS capacitor arrays similar to those first used by McCreary [58] were chosen to implement these functions as shown in Fig. 6.3(a). Neglecting the offset voltage of the operational amplifier, the top plates of the capacitors in this array are either switched to ground or to a virtual ground. Since there is no voltage change across the capacitors during switching, there is no harmful flow of displacement currents, and hence, this filter can be used in dynamic programming applications. Because the charge multiplier configuration is not sensitive to parasitic capacitances, a small unit capacitor size ($C_s = 0.42$ pF) was chosen to implement the binary Q and G capacitor arrays for this stage.

The first-order relationship between the programmable capacitor ratio, $\frac{C_{f_0}}{C_u}$, and the center frequency, f_0 , is

$$\frac{C_{f_0}}{C_u} = \frac{f_c}{2\pi f_0}. \quad (6.6)$$

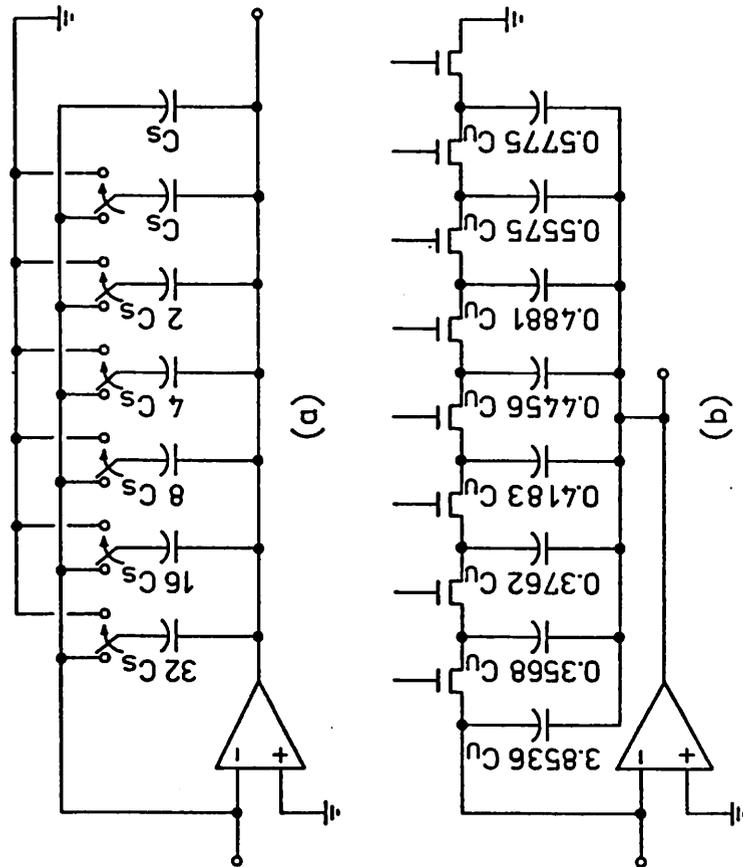


Fig. 6.3. (a) The six-bit binary-weighted capacitor array used to program the gain and the selectivity, and (b) the non-binary capacitor array used to program the center frequency.

It was desired to have the center frequencies logarithmically span an octave of frequency such that when the sampling rate was changed by a factor of two, a new set of center frequencies would be obtained which would smoothly continue the logarithmic progression. Since the relationship in Eqn. (6.6) is an inverse (and because of the logarithmic progression), binary-weighted capacitor arrays were not suitable for center frequency programming. Therefore, a more flexible type of MOS capacitor array was developed as shown in Fig. 6.3(b). The amount of capacitance selected in this array is determined by turning on all the MOS switches except one. The switch which is off electrically separates the array into two parts. The value of capacitance determining f_o is the sum of all capacitors between the off switch and the op amp. As in the binary arrays, the remaining capacitors to the right of the off switch are connected to ground so that the displacement current generated during program switching is minimized.

In Fig. 6.4, the capacitance ratios required to program eight different center frequencies with 1.089 logarithmic spacings are given for a clock rate of 10 kHz. The values of the capacitors which are programmed in the non-binary array are determined by the difference between adjacent capacitor ratios as shown in the graph. This type of array is extremely efficient in its use of capacitor area. For example, in order to obtain the lowest center frequency of 225 Hz, a capacitor ratio of 7.07 is required, and since the total capacitance in the array is 7.07 unit squares, no silicon area is wasted. Type-I LDI integrators were used to implement the filter, and C_u was chosen to be about 2.6 pF. In this particular design, there is no significant performance advantage in using type-II LDI integrators since C_u must be several picofarads in order to accurately realize the fractional unit capacitors required in the C_i arrays. It will be shown later that the error introduced by the top-plate parasitic capacitance is very small.

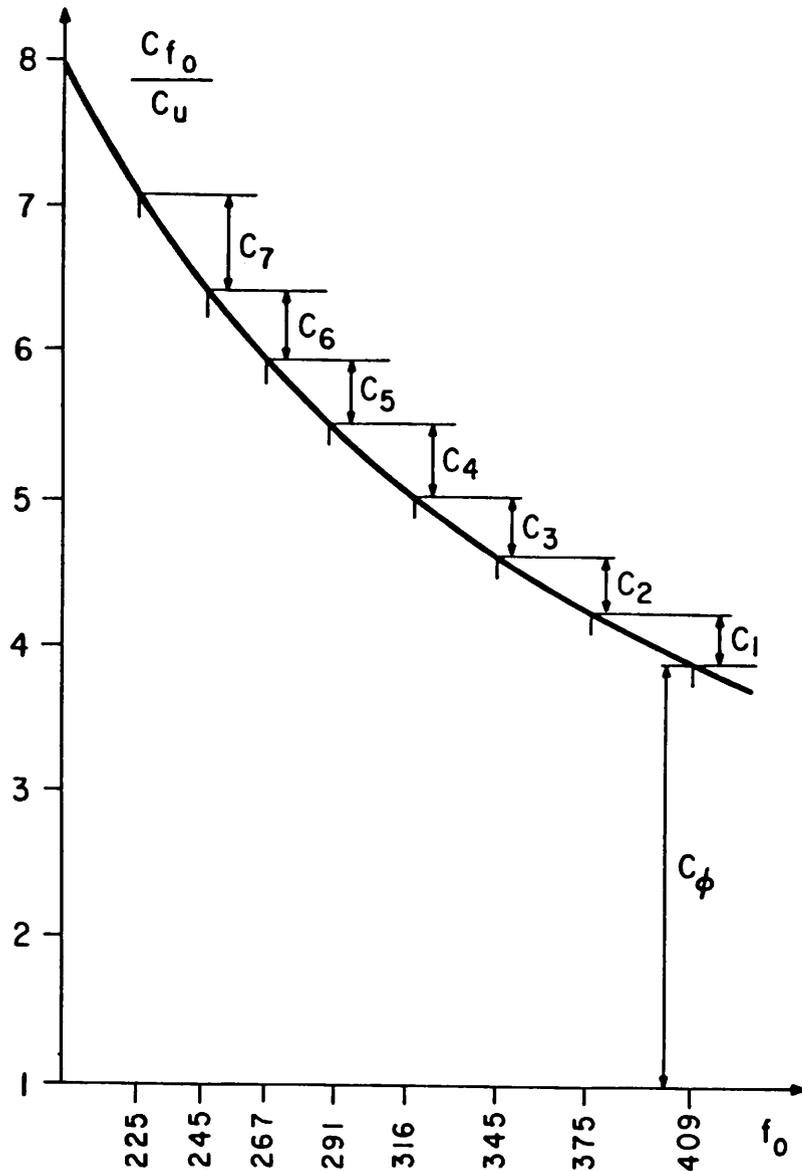


Fig. 6.4. Capacitor ratio versus center frequency. The non-binary capacitor values are determined by the difference between successive capacitor ratios.

Eqn. (6.6) also shows a direct one-to-one relationship between f_0 and f_c . Therefore, for a given capacitor ratio, the sampling frequency can be used to program the center frequencies of the filter. This programming technique was also used in the formant speech synthesis filter to be described later in this chapter. In the next section, the practical design considerations for the switched capacitor programmable second-order section will be presented.

6.3. Practical Design Considerations

The practical limitations of the MOS operational amplifiers, parasitic capacitances, and other nonidealities can affect the performance of switched capacitor filters. In some cases where the filter specifications are relatively relaxed as in a formant speech synthesizer, frequency response deviations can be tolerated if they are predictable. In cases where the specifications are tighter, it may be necessary to compensate or predistort to eliminate these errors. Therefore, it is important for both cases to develop a set of design equations which relate the actual filter performance to the parameters of the individual components. In this section, the practical design considerations for the programmable second-order filter will be presented.

6.3.1. Sampled-Data Transfer Functions

The switched capacitor implementation has a frequency response which is slightly different from the response of the RLC prototype due to the termination errors introduced by the finite switching frequency. The sampled-data transfer functions are given below:

$$H_{BR}(z) = \frac{-\left[\frac{C_G}{C_Q}\right] \left[z(z^2 + a_1 z + 1)\right]}{b_3 z^3 + b_2 z^2 + b_1 z + b_0} \quad (6.7a)$$

$$H_{BP}(z) = \frac{\alpha z(z-1)}{z^2 + a_1 z + 1} H_{BR}(z) \quad (6.7b)$$

$$H_{LP}(z) = \frac{\alpha}{(z-1)} H_{BP}(z) \quad (6.7c)$$

where

$$\alpha = \frac{C_u}{C_{f_0}} \quad (6.7d)$$

$$a_1 = \left[\frac{C_u}{C_{f_0}} \right]^2 - 2 \quad (6.7e)$$

$$b_3 = \left[\frac{C_u}{C_{f_0}} \right] \left[\frac{C_s}{C_Q} \right] + 1 \quad (6.7f)$$

$$b_2 = \left[\frac{C_u}{C_{f_0}} \right]^2 + \left[\frac{C_p}{C_Q} \right] - 2 \left[\frac{C_u}{C_{f_0}} \right] \left[\frac{C_s}{C_Q} \right] - 3 \quad (6.7g)$$

$$b_1 = \left[\frac{C_u}{C_{f_0}} \right] \left[\frac{C_p}{C_Q} + \frac{C_s}{C_Q} - 1 \right] - 2 \left[\frac{C_p}{C_Q} \right] + 3 \quad (6.7h)$$

and

$$b_0 = - \left[1 - \frac{C_p}{C_Q} \right]. \quad (6.7i)$$

The frequency responses are obtained from these equations by setting $z = e^{j\omega T}$. The resulting expressions can then be solved to obtain the actual sampled-data Q and center frequency values. In general the approximation to the RLC prototype becomes better as the clock frequency increases relative to the center frequency. A better fit between the continuous and sampled-data responses can be obtained by slightly modifying the capacitor ratios [64].

6.3.2. Exact Design Equations

The lowpass transfer function of Eqn. (6.1) is given in terms of the parameters ω_0 and Q which are defined in Fig. 6.5. From the figure, it can be seen that the actual peak frequency and selectivity can deviate from these assumed values by an amount which becomes significant for small values of Q. The actual peak frequency, ω_{peak} , is given by

$$\omega_{peak} = \omega_0 \left[1 - \frac{1}{2Q^2} \right]^{1/2}, \quad (6.8)$$

and the actual Q value is

$$Q_A = Q \left[\frac{1}{1 - \frac{1}{4Q^2}} \right]^{1/2}. \quad (6.9)$$

From these equations, it is apparent that the discrepancy in the approximate expressions increases as Q decreases. For example, if the desired Q is one, Eqn. (6.8) predicts a peak frequency of $\omega_{peak} = 0.707\omega_0$, and Eqn. (6.9) predicts a Q_A value of $Q_A = 1.1547$.

6.3.3. Op Amp DC Gain Effects for Integrator Stages

The finite DC gain of the NMOS operational amplifiers used to implement the switched capacitor integrators causes errors in the filter frequency response, especially for high Q values. (It is assumed here that the bandreject stage is ideal). The actual Q_A is given in terms of the desired Q by

$$Q_A = \left[\frac{1}{2Q+A} \right] \left[1 + A^2 + \frac{A}{Q} \right]^{1/2} \approx 1 - \frac{2Q}{A} \quad (6.10)$$

where the approximation is valid for large Q values. This relationship is plotted in

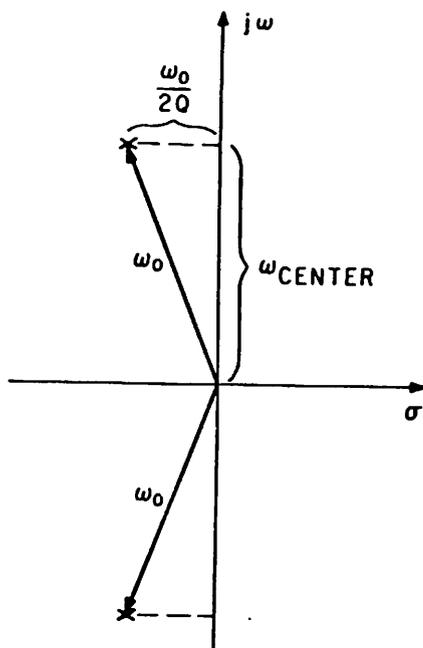


Fig. 6.5. An s-plane pole plot which defines the parameters ω_0 , Q , and the center frequency.

Fig. 6.6 for two cases where the op amp has infinite gain, and for a gain of 1000. For $Q=50$, and $A=1000$, the error is 10% which gives a Q_A of 45. This deviation can be reduced by using higher gain op amps, or by using a compensated non-binary array to correct for the gain errors.

The center frequency also depends on the op amp gain as shown in the following formula:

$$\omega_A = \omega_0 \left[\frac{1}{A+1} \right] \left[A^2 + \frac{A}{Q} + 1 \right]^{1/2} \approx \omega_0 \left[\frac{A}{A+1} \right]. \quad (6.11)$$

For $A=1000$, the difference between ω_0 and ω_A is less than 0.1%, and can therefore be neglected for most cases. It should be emphasized that it is the DC op amp gain which is most important, and not the gain at the center frequency because the switched capacitor integrator responds to a step response where the final value after slewing and settling depends only on the low frequency gain. The frequency response of the op amp determines the settling response.

6.3.4. Op Amp Gain Effects for the Bandreject Stage

A schematic of the gain-setting bandreject stage, neglecting the switched capacitor feedback resistor, is shown in Fig. 6.7. The output of this stage is given by

$$V_o = - \left[\frac{C_G}{C_Q} \right] \left[\frac{A}{A+1 + \frac{C_G}{C_Q}} \right] V_{in} - \left[\frac{C_s}{C_Q} \right] \left[\frac{A}{A+1 + \frac{C_s}{C_Q}} \right] V_{BP}. \quad (6.12)$$

Thus, the finite DC op amp gain of the bandreject stage introduces both a filter gain error and a filter Q error as given by the first and second bracketed terms, respectively. The filter peak gain error is maximum when Q is minimum and G is maximum. For example, if $Q=1$, $G=64$, and $A=1000$, then the error in the peak

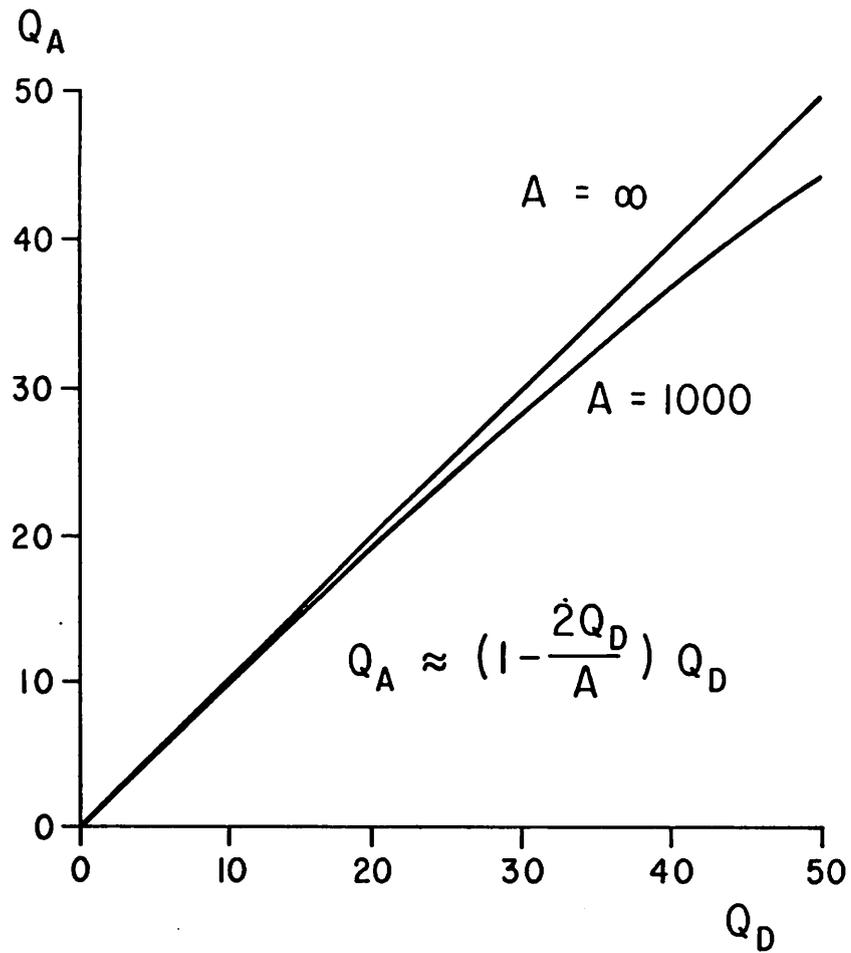


Fig. 6.6. A graph of Q versus desired Q for two different values of DC op amp gain for the two amplifiers used to implement the switched capacitor integrators.

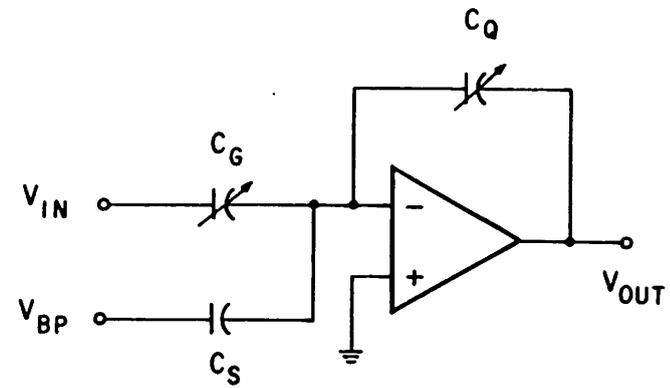


Fig. 6.7. A simplified schematic of the gain-setting bandreject stage.

gain is about 6%. The Q error is worst-case for minimum Q and G. If $G=1$, $Q=1$, and $A=1000$, the Q error is only about 0.2%.

6.3.5. Top-Plate Parasitic Capacitance

Since type-I LDI integrators were used in this design, it is important to consider the effect of the parasitic capacitance connected to the top-plate of the switched capacitors. For a switched capacitor value of C_u , and a top-plate parasitic capacitance of C_p , the center frequency (assuming everything else is ideal) is

$$\omega_A = \omega_o \left[1 + \frac{C_p}{C_u} \right]^{1/2}, \quad (6.13)$$

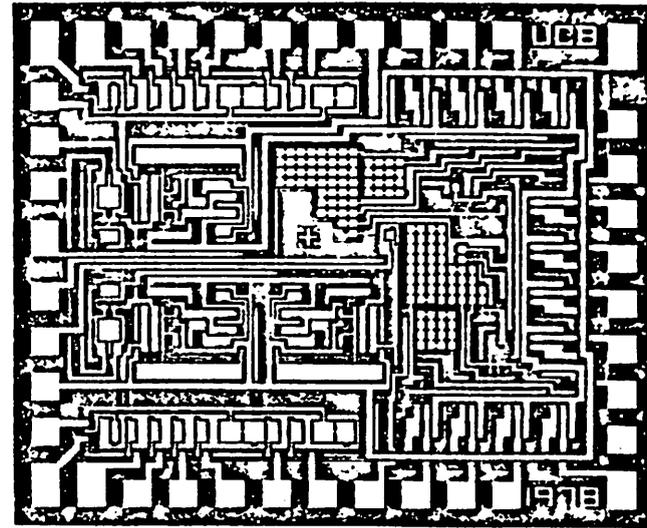
and the actual Q value is given by

$$Q_A = Q \left[1 + \frac{C_p}{C_u} \right]^{1/2}. \quad (6.14)$$

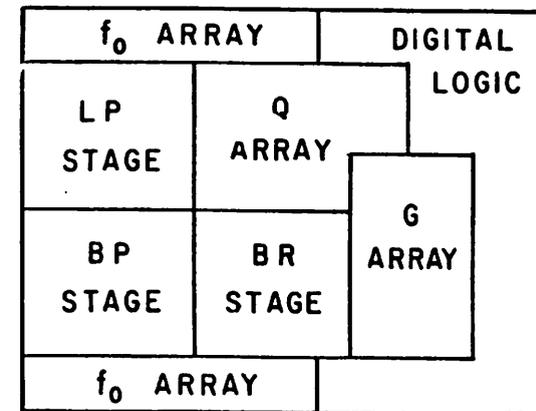
In this design, the switched capacitor size was about 2.3 pF, and the top-plate parasitic was about 0.025 pF. Thus, the error due to top-plate parasitic is only about 0.5% which is negligible for the formant speech synthesizer application. If necessary, type-II integrators could be used to obtain greater accuracy.

6.4. NMOS Prototype Experimental Results

An experimental prototype of the electrically programmable second-order switched capacitor filter shown schematically in Fig. 6.2 has been integrated using the NMOS metal-gate enhancement-depletion process described in Appendix 1. A photograph of the 88 mils by 105 mils (including bonding pads) die is shown in Fig. 6.8. The NMOS operational amplifier used in this circuit is identical to the one described in Chapter 5. The programmable filter can produce 32,768 (2^{15}) different



(a)



(b)

Fig. 6.8. (a) A die photograph of the 88 mils by 105 mils NMOS experimental chip, and (b) a layout block diagram of (a).

frequency responses at each of the lowpass, bandpass, and bandreject outputs for each clock frequency. Representative experimental results are presented in the following sections.

6.4.1. Center Frequency Programming

By applying a 3-bit digital word to the two non-binary arrays, any one of eight different center frequencies can be programmed. As mentioned earlier, the center frequencies were designed with logarithmic spacings where $f_o(n) = 1.089f_o(n-1)$. The eight experimentally observed center frequencies shown in Fig. 6.9 for a 20 kHz clock rate are in good agreement with the expected design values.

6.4.2. Clock Frequency Programming

The gain constant of a switched capacitor integrator, $\omega_o = f_c \left[\frac{C_u}{C_l} \right]$, is directly proportional to the sampling frequency. This one-to-one relationship can also be used as a degree of freedom in programming a switched capacitor filter. Since frequency division by a factor of two is easily achieved using standard flip-flops, this filter was designed in such a way that when the clock rate was changed by a factor of two, a new set of center frequencies was generated which smoothly continued the logarithmic progression as illustrated in Fig. 6.10. Thus, with a 1 kHz minimum clock frequency and a 256 kHz maximum clock rate, the center frequencies range over eight octaves from 22.5 Hz to 10573 Hz in 1.089 logarithmic steps.

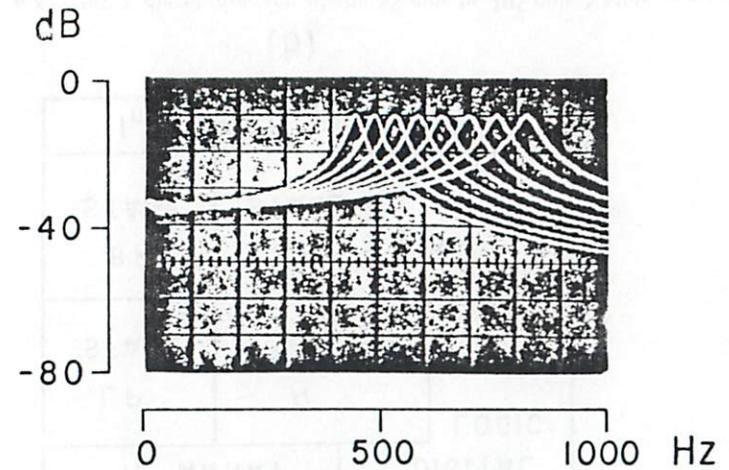


Fig. 6.9. The eight experimentally observed programmable center frequencies for a 20 kHz clock rate.

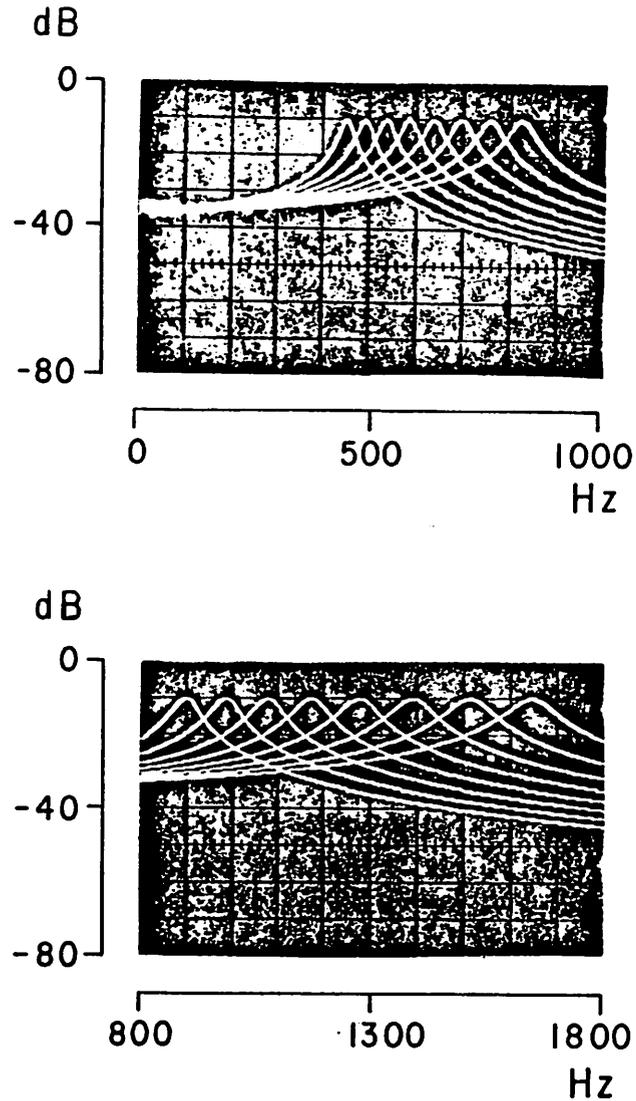


Fig. 6.10. The eight experimentally observed center frequencies for 20 kHz and 40 kHz clocks. The filter is designed so that the logarithmic progression of center frequencies is smoothly continued as the sampling rate is changed by a factor of two.

6.4.3. Selectivity Programming

A six-bit digital word is used to program a binary-weighted capacitor array to any one of 64 different Q values from $Q=1$ to $Q=64$. Figure 6.11 shows five of the possible 64 values ranging from four to 64 by factors of two. Notice that the highest experimental Q is about 56. The deviation from the desired value of 64 is due to finite DC op amp gain of 1000 as described earlier.

6.4.4. Gain Programming

A six-bit binary word is also used to program the peak gain through the filter. Figure 6.12 shows seven of the possible 64 G values ranging from one to 64 by factors of two. Good agreement is observed between theory and experiment.

6.4.5. Low-Q Passband Details

For low-Q applications, there is a significant difference between the actual values for the center frequency and gain and the parameters ω_0 and Q due to the theoretical approximations used in Section 6.3. The experimental passband details of Figure 6.13 show that as Q is decreased, and these approximations become invalid, the peak frequency is reduced such that when Q is one, $\omega_{\text{peak}}=0.707\omega_0$, and the gain is increased by about 1.25 dB. For $Q \geq 5$, these discrepancies are less than 1%.

6.4.6. Dynamic Range

The output dynamic range was measured for maximum and minimum values of Q and peak gain. The noise contributed at the output of the filter by the internal op amps and their associated switched capacitor resistors is amplified by an amount equal to Q, and hence, the dynamic range decreases for higher Q's. The distortion

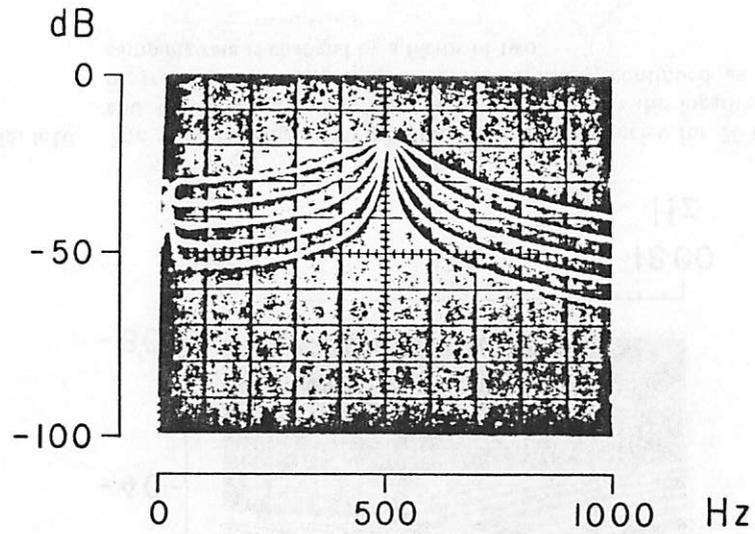


Fig. 6.11. Experimental results for five of the possible 64 programmable Q values.

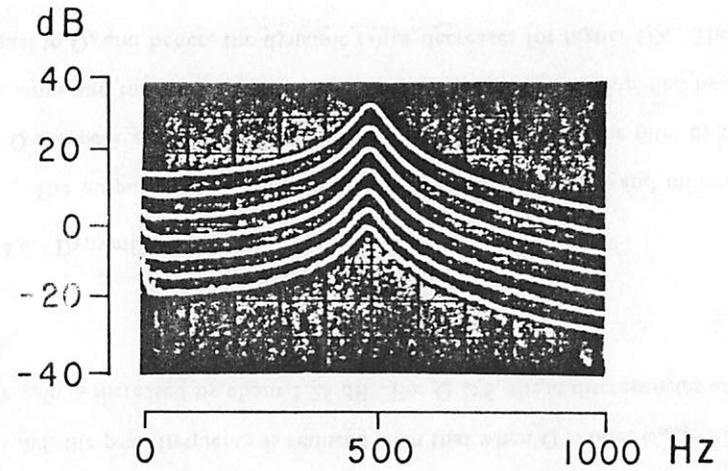


Fig. 6.12. Experimental results for seven of the possible 64 programmable peak gain values.

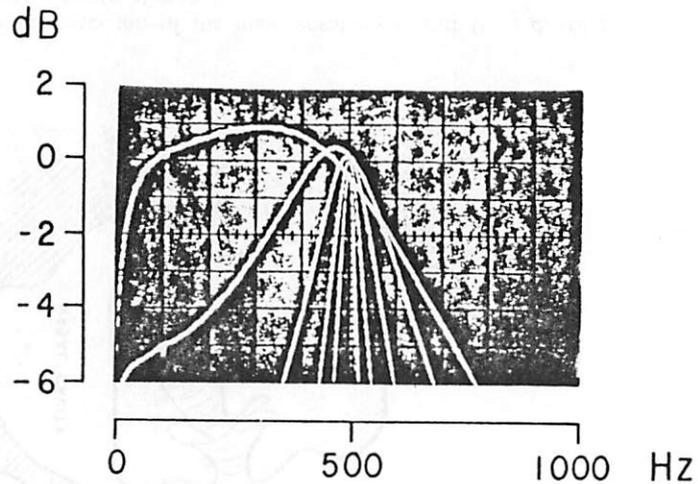


Fig. 6.13. Low Q passband details for a 20 kHz clock rate.

at the output remains relatively constant. Preliminary results indicate a dynamic range of from 65-90 dB as Q is varied from one to 64 for $f_0=450$ Hz at a 20 kHz clock rate. Complete dynamic range data will be published at a later date [61].

6.5. A Formant Speech Synthesis System

There are many applications which require electrically programmable filters including adaptive equalizers, and music and speech synthesizers. This section will describe an application wherein several switched capacitor second-order sections are dynamically programmed to implement a formant speech synthesis system. The major advantage of the formant algorithm is that good quality speech can be synthesized with a low data rate of about 300 bits/second [62].

6.5.1. The Vocal Tract Model

Figure 6.14(a) shows a cross-section of the male vocal tract which is a lossy acoustic tube about 17 cm in length. Theoretically, this tube has an infinite number of natural frequencies or *formants*. In order to produce different sounds, the frequency response characteristics of the vocal tract are altered by changing the cross-sectional area of the tube at the tongue, lips or teeth.

There are several methods by which the vocal tract responses can be electrically simulated [62]. One method of electrically modelling the vocal tract is shown in Fig. 6.14(b). In this model, a distributed LC ladder is used in which each LC pair contributes to a resonant frequency. The main disadvantage of this approach is that it is very difficult to independently program the formants. Therefore, it was decided to use a cascade of electrically-programmable switched capacitor second-order sections which allows the gain, Q , and formant frequencies to be independently controlled.

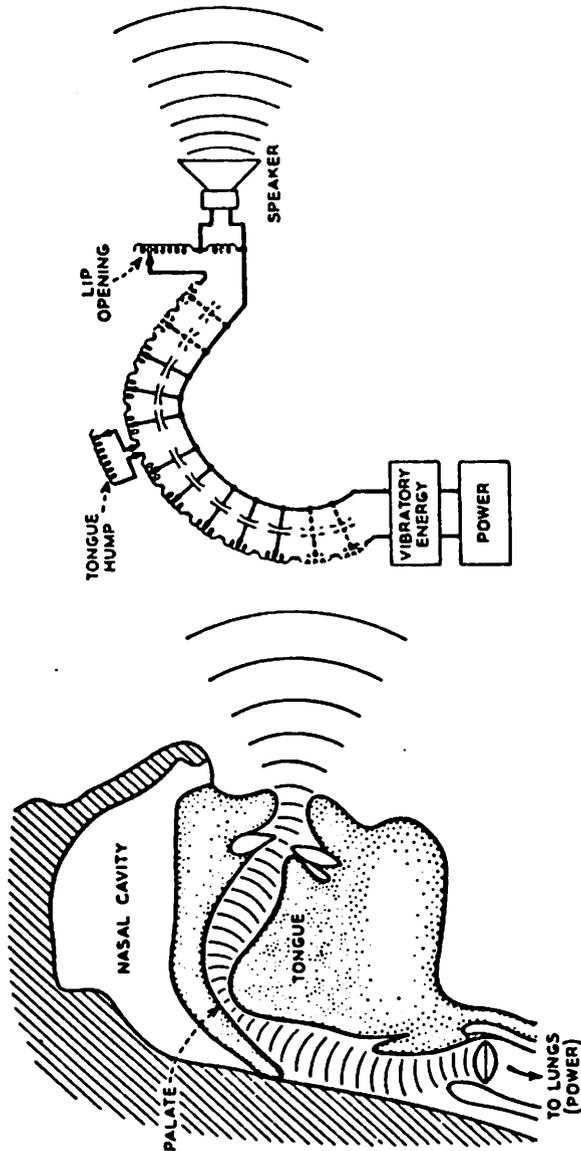


Fig. 6.14. (a) A cross-section of the male vocal tract, and (b) a distributed LC ladder electrical model.

6.5.2. A Switched Capacitor Formant Synthesizer

A block diagram of the formant synthesis system is shown in Figure 6.15. It has been shown experimentally that good quality speech can be obtained by simulating only the three low frequency formants [62]. These three formants are implemented with second-order switched capacitor filters which have their gain, center frequency and selectivity programmed by a digital controller. In addition, it has been shown that all of the higher frequency formants can be empirically modelled using high-order pole correction with a fixed response. In this case, two poles with center frequencies above the third formant are used as correction. The response of this filter is dynamically programmed every 1-10 msec to produce the synthesized speech.

As mentioned earlier, the clock frequency can be changed to program these filters, and this feature has been exploited in the formant synthesizer. The first formant stage is clocked at 10/20 kHz, the second at 30/60 kHz, and third at 60/120 kHz. Since there are 32768 responses/output/clock frequency, and since there are five different clock frequencies, there are 3.78×10^{22} possible different responses for this system!

At the present time, the English vowels have been synthesized with excellent results. Figure 6.16 shows two different vocal tract responses for the vowels /a/ as in "father", and /e/ as in "bet", and their corresponding time waveforms. This system is currently being characterized and the complete results will be published at a later date [63].

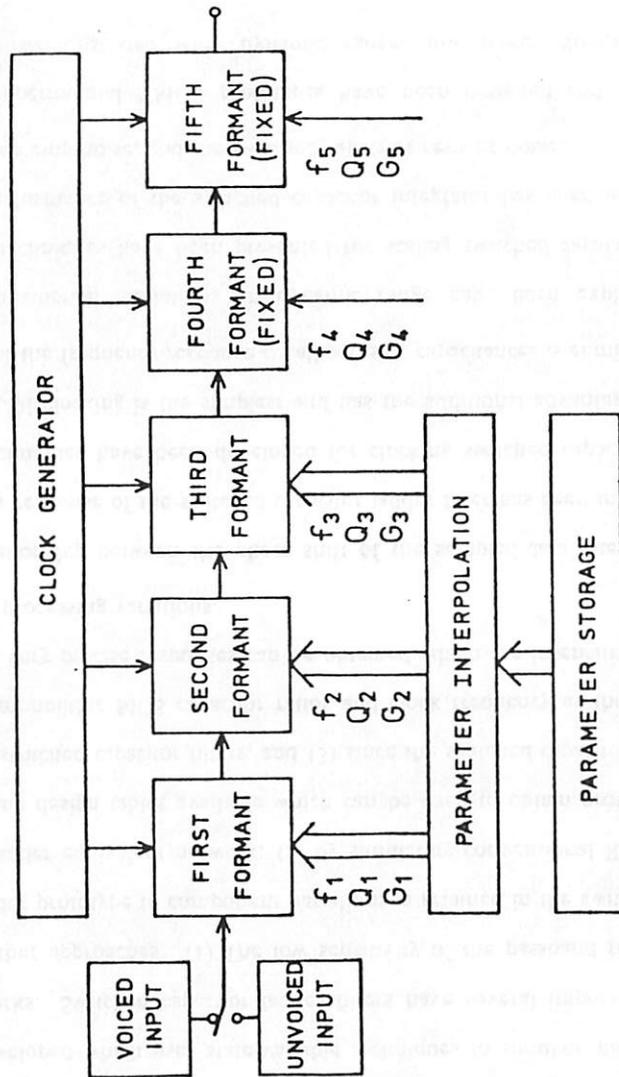
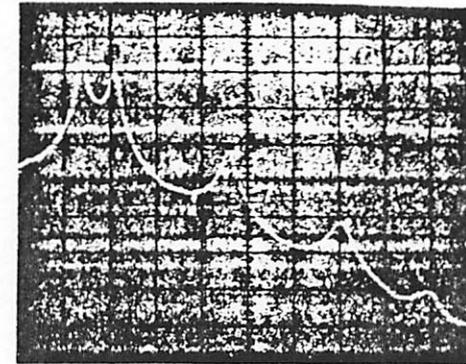
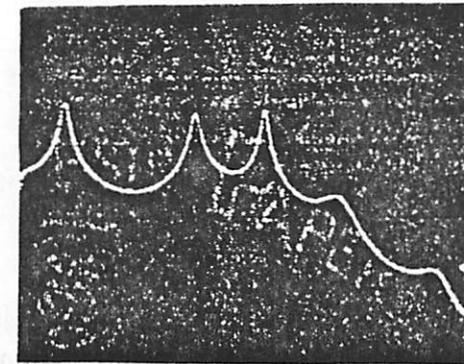


Fig. 6.15. A block diagram of a formant speech synthesis system which uses five second-order filter sections, three which are dynamically programmed, and two which have fixed responses.



/a/



/e/

Fig. 6.16. Frequency and time responses for two different English vowels obtained from the formant speech synthesis system.

Chapter 7

CONCLUSIONS

A new approach for designing precision high-order switched capacitor filters has been developed which uses state-variable techniques to simulate passive RLC ladder networks. Switched capacitor ladder filters have several important advantages over other approaches: (1) The low sensitivity of the passband response of the RLC ladder prototype to component variations is retained in the switched capacitor active ladder equivalent network; (2) by simulating conventional RLC filters, there are many design tables available which can be used to obtain prototypes for synthesizing switched capacitor filters, and (3) since the switched capacitor response depends on monolithic MOS capacitor ratios and clock frequency as the precision components, very precise responses can be obtained which are insensitive to temperature and processing variations.

The relationship between the phase shift of the sampled-data integrator and the frequency response of the switched capacitor ladder filter has been investigated, and three techniques have been developed for clocking switched capacitor filters. The type-II LDI clocking is the simplest and has the additional advantage that the dependence of the frequency response on all parasitic capacitances is eliminated.

The fundamental limitations on dynamic range have been explored, and several new techniques have been presented for scaling switched capacitor filters. The noise performance of the switched capacitor integrator has been analyzed in terms of the op amp noise, and the switched capacitor resistor noise.

Three experimental NMOS prototypes have been designed and fabricated. These filters demonstrated wide dynamic range, low power dissipation and

insensitivity to component variations. One circuit verified a new technique for designing switched capacitor filters using switched weighted capacitor arrays to achieve digitally-programmable frequency responses.

There are several areas where future work may be directed: (1) Reducing the required number of operational amplifiers; (2) high frequency switched capacitor filters; (3) maximum dynamic range filters; (4) N-path filters; (5) minimum area realizations, and (6) the development of bilinear switched capacitor integrators which are insensitive to parasitic capacitances.

Appendix 1

NMOS METAL-GATE ENHANCEMENT-DEPLETION PROCESS

This appendix details the NMOS process used to fabricate the switched capacitor filters described in this dissertation. The process evolved to its present form through previous efforts [53],[58]. Boron diffusions are used as isolation regions, and the substrate is boron-doped p-type <100> orientation with 25-50 ohm-cm resistivity.

Fabrication Sequence

1. Initial wafer cleaning:

- (a). Deionized water DI:HF (9:1), room temperature dip for 2 mins.
- (b). TCE, 60 ° C for 10 mins.
- (c). Acetone, room temperature for 2 mins.
- (d). DI rinse.
- (e). Clean for 15 mins. in $H_2SO_4:H_2O_2$ (4:1) at 90 ° C (piranha cleaning step).
- (f). DI rinse.
- (g). N_2 blow dry.

2. Initial oxidation: N-type drive-in furnace, 0.92 μm of oxide.

- (a). Wet O_2 at 0.5 liters/min, 1150 ° C, 90 mins.
- (b). Dry N_2 at 0.65 liters/min, 850 ° C, 10 mins.

3. Negative photoresist step: (p^+ isolation diffusion mask)

- (a). Apply Kodak 747 Micronegative Photoresist; spin at 5000 rpm for 30 secs.

- (b). Air dry for 15 mins.
- (c). Prebake at 90 ° C for 30 mins.
- (d). Expose mask, 3.5 secs.
- (e). Spray develop, 30 secs.
- (f). Spray rinse, 20 secs.
- (g). Alcohol dip, 7 secs. Isopropyl:methanol (1:1).
- (h). Light DI rinse.
- (i). Light N_2 blow dry.
- (j). Postbake at 125 ° C for 30 min.
- (k). Oxide etch, $NH_4F:HF$ (5:1), room temperature, 9.5 mins. (0.1 microns/min.)
- (l). Photoresist strip, $H_2SO_4:H_2O_2$ (4:1), 90 ° C, 5 mins.

4. Piranha Clean.

5. Boron predeposition: P-type predeposition furnace at 950 ° C. Simultaneous flow for 15 mins. of the following gases:

- (a). B_2H_6 , 0.26 liters/min.
- (b). O_2 , 0.013 liters/min.
- (c). N_2 , 1.3 liters/min.

6. Etch boron glass: HF:DI (1:3), 1.5 min. dip.

7. Piranha clean.

8. Field oxide growth: N-type drive-in furnace, 1150 ° C, 0.4 μm of oxide over p^+ .

- (a). Wet O₂, 0.5 liters/min., 16 mins.
 - (b). Dry O₂, 1.0 liters/min., 10 mins.
9. Negative photoresist step: (N⁺ diffusion mask)
Same as step 3 except etch for 10 mins.
10. Piranha clean.
11. Phosphorous predeposition: N-type predeposition furnace, 1100 ° C.
- (a). O₂ at 0.1 liters/min. and N₂ at 1.25 liters/min. for 5 mins.
 - (b). O₂ at 0.1 liters/min., N₂ at 1.25 liters/min., and POCl₃ at 0.096 liters/min. for 20 mins.
 - (c). N₂ at 1.25 liters/min. for 10 mins.
12. Etch phosphorous glass: HF:DI (1:3), 1.5 min. dip.
13. Piranha clean.
14. Field oxide growth: N-type drive-in furnace, 0.5 μm of oxide over n⁺.
- (a). Wet O₂ at 0.5 liters/min., 1100 ° C for 34 mins.
 - (b). Dry N₂ at 1.0 liters/min., 900 ° C for 10 mins.
15. Negative photoresist step: (Gate oxide mask)
Same as step 3 except etch for 6.5 mins.
16. Piranha clean.
17. Gate oxide growth: N-type drive-in furnace, 0.1 μm of dry oxide.
- (a). Dry O₂ at 1.5 liters/min., 1000 ° C for 110 mins.
 - (b). Dry N₂ at 1.0 liters/min., 900 ° C for 10 mins.
18. Negative photoresist step: (Depletion-implant mask)

Same as steps 3(a)-3(j). (No oxide etch)!

19. Phosphorous depletion implant: $2.1 \times 10^{12}/\text{cm}^2$ at 150 keV.
20. Piranha clean.
21. Boron enhancement implant: $7.8 \times 10^{11}/\text{cm}^2$ at 50 keV.
22. Oxide etch: Using Q-tip, etch back of wafer *only*.
23. Piranha clean.
24. Phosphorous gettering step: N-type predeposition furnace.
- (a). O₂ at 0.1 liters/min. and N₂ at 1.25 liters/min. for 5 mins. at 1000 ° C.
 - (b). O₂ at 0.1 liters/min., N₂ at 1.25 liters/min., and POCl₃ at 0.096 liters/min. for 2 mins. at 1000 ° C.
 - (c). N₂ at 1.25 liters/min. for 10 mins.
25. Etch phosphorous glass: Dip in H₂SO₄:H₂O₂ for 5 mins.
26. Negative photoresist step: (Contact mask)
Same as step 3 except expose for 1.8 secs. and then shift one row and expose for 1.7 secs. to eliminate pinholes. Oxide etch time is 1 min.
27. Piranha clean.
28. HMDS dry.
29. Evaporate 0.4 to 0.6 microns of aluminum.
30. Positive photoresist step: (Metallization mask)
- (a). HMDS dry.
 - (b). Apply AZ1350J positive photoresist and spin at 8000 rpm for 30 secs.

- (c). Prebake at 90 ° C for 45 mins.
 - (d). Expose mask for 15 secs.
 - (e). Develop with AZ1350J developer: DI (1:1) for 45 secs.
 - (f). Light DI rinse.
 - (g). Postbake at 90 ° C for 30 mins.
 - (h). Aluminum etch with type-A etchant at 60 ° C with light agitation.
 - (i). DI rinse.
 - (j). Acetone PR strip for 5 mins.
 - (k). DI rinse.
 - (l). N₂ blow dry.
31. Sintering treatment: Sintering oven at 450 ° C for 5 mins. with N₂:H₂ (forming gas) (9:1) at 1 liters/min.

Appendix 2

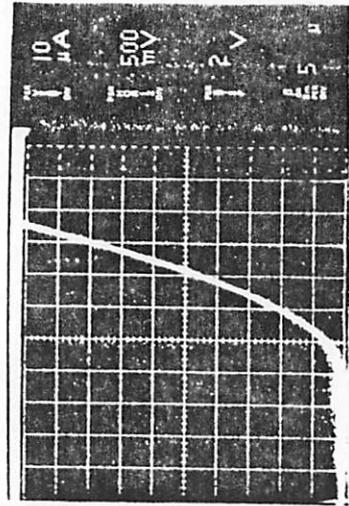
NMOS ENHANCEMENT-DEPLETION DEVICE CHARACTERISTICS

The NMOS enhancement-depletion metal-gate process was described in Appendix 1, and the characteristics of the transistors fabricated with that process are briefly described in this appendix.

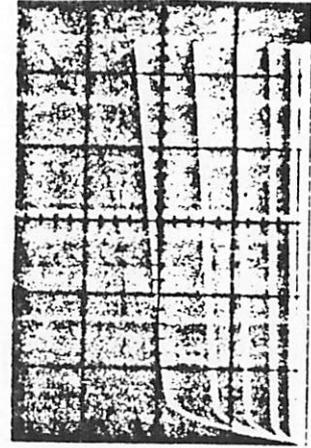
Figure A2.1 shows a series of enhancement device characteristics for a device with a 0.4 mil channel width, and a 1.0 mil channel length for 0 and 5 volts of body bias. From these curves, the zero-bias threshold voltage is found to be about 0.5 volts; λ is about 0.01 volts⁻¹, and γ is about 0.6 volts^{1/2}.

A typical set of I-V curves for a depletion device with a W of 0.4 mils, and an L of 1.0 mils is shown in Fig. A2.2. From this data, the zero-bias depletion threshold is found to be about -3.5 volts, and the other parameters are similar to those for the enhancement device above.

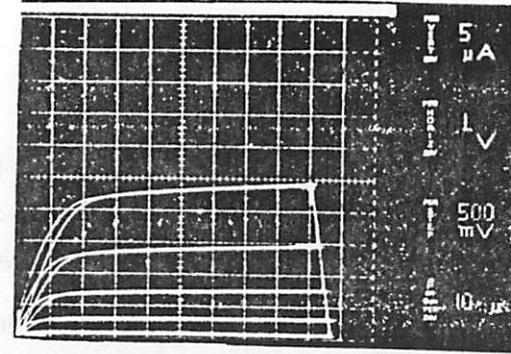
The performance parameters of the operational amplifier were estimated using the device data above, and good agreement was obtained between the predicted values and the experimental values using first-order modelling equations.



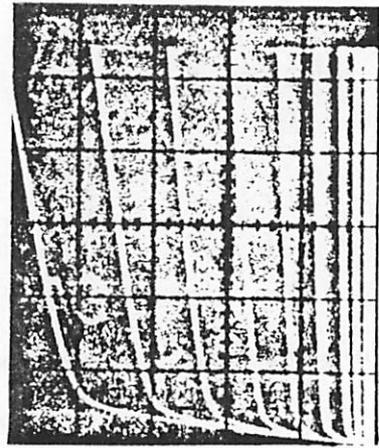
(c)



(d)



(a)



(b)

Fig. A2.1. Experimental I-V curves for the enhancement NMOS device with $W=0.4$ mils, and $L=1.0$ mils with 0 and 5 volts body bias.

Fig. A2.2. Experimental I-V curves for the depletion NMOS device with $W=0.4$ mils, and $L=1.0$ mils with no body bias.

SIMULATION TECHNIQUES FOR SWITCHED CAPACITOR FILTERS

It is difficult to simulate MOS switched capacitor filters because of the analog input and output voltages which are valid only at discrete time intervals, and because it is usually desirable to obtain the AC steady-state frequency response of a circuit which is operating in a switched or transient mode. At the present time, no computer program exists for directly simulating the frequency response of switched capacitor filters at the MOS device level. Hence, it is necessary to model the filters at a higher level for simulation on the currently available CAD packages.

One approach is to use a continuous-time, continuous-amplitude simulation program such as SPICE2 [30]. Since SPICE2 cannot simulate discrete time delays in an AC analysis mode, significant errors due to the omission of sampling effects (such as DDI Q-enhancement) may occur.

Another simulation technique involves using a discrete-time, discrete-amplitude digital filter simulation program such as DINAP (Digital Network Analysis Program) [28] wherein the various analog effects are modelled using digital filter elements. DINAP can determine the AC frequency response of digital filters where the sampling rate, and number of bits of truncation and roundoff are specified. Since the switched capacitor filter has continuous amplitude, the maximum allowable number of bits, 21, is specified for both truncation and roundoff accuracy.

A1.1. The DINAP Program [28]

The three elements available for simulating digital filters using the DINAP program are shown in Fig. A3.1: (1) Ideal one-unit delay elements; (2) coefficient multipliers, and (3) two-input summers. Many of the important switched capacitor filter parameters can be simulated with DINAP by modelling switched capacitor integrators using these three basic elements.

To illustrate the procedure for transforming from switched capacitor to digital filter form, consider the type-II noninverting integrator of Fig. A3.2(a). With the switches to the left at time, $(t-T)$, and to the right at time, t , the output voltage is obtained by using the conservation of charge principle ($T = \frac{1}{f_{\text{clock}}}$):

$$V_{\text{out}}(t) = \left[\frac{C_u}{C_l} \right] V_{\text{in}}(t-T) + V_{\text{out}}(t-T) \quad (\text{A3.1})$$

which, when the z-transform is taken results in

$$V_{\text{out}}(z) = \left[\frac{C_u}{C_l} \right] z^{-1} V_{\text{in}}(z) + z^{-1} V_{\text{out}}(z). \quad (\text{A3.2})$$

This equation shows that $V_{\text{out}}(z)$ is a delayed sum of $V_{\text{in}}(z)$ scaled by $\left[\frac{C_u}{C_l} \right]$ and $V_{\text{out}}(z)$. The digital network which implements Eqn. (A3.2) is shown in Fig. A3.2(b). Similarly, the inverting integrator of Fig. A3.2(c) has its output voltage given by

$$V_{\text{out}}(t) = - \left[\frac{C_u}{C_l} \right] V_{\text{in}}(t) + V_{\text{out}}(t-T) \quad (\text{A3.3})$$

with a z-transform of

$$V_{\text{out}}(z) = - \left[\frac{C_u}{C_l} \right] V_{\text{in}}(z) + z^{-1} V_{\text{out}}(z). \quad (\text{A3.4})$$

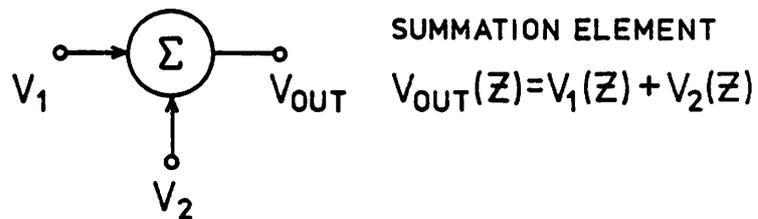
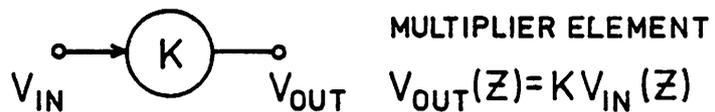
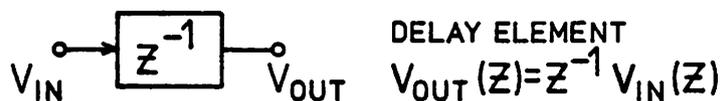


Fig. A3.1. The three digital filter elements which are used in the DINAP program to simulate switched capacitor filters.

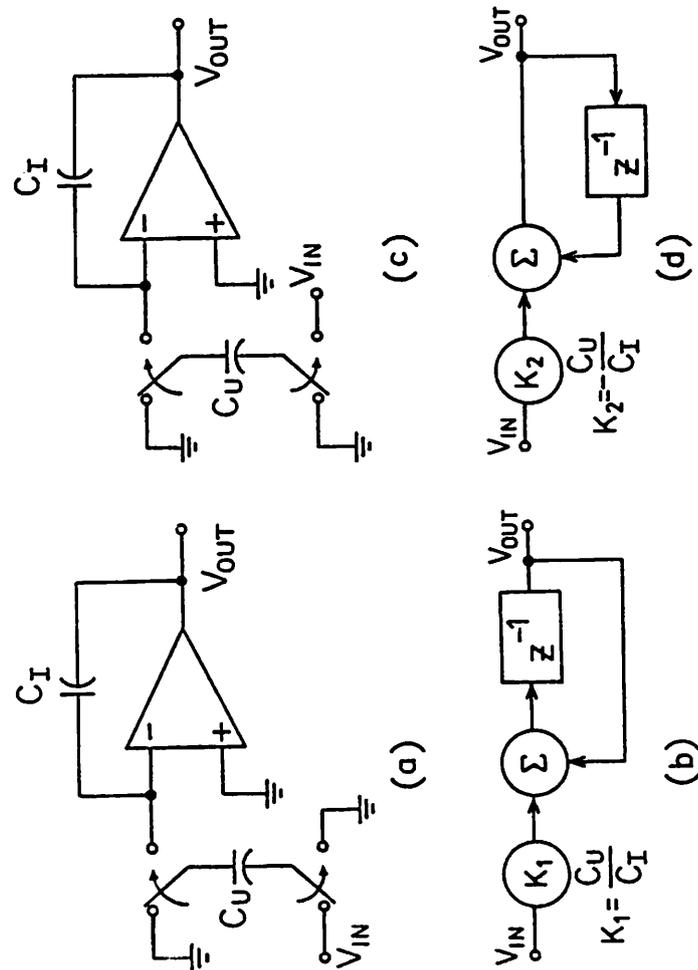


Fig. A3.2. (a) A switched capacitor type-II noninverting integrator, and (b) the corresponding digital filter model; (c) a type-II inverting integrator and (d) the digital filter equivalent.

Implementation of Eqn. (A3.4) also requires a summation of the delayed output with a scaled and undelayed version of the input as illustrated in Fig. A3.2(d).

A3.2. Modelling Analog Effects in DINAP

All analog effects which can be expressed analytically in the z-domain can be simulated on DINAP. In this section, models for several of the more important analog second-order limitations will be considered.

A3.2.1. Top-Plate Parasitic Capacitance

A type-I differential switched capacitor integrator is shown in Fig. A3.3(a) where C_p represents the parasitic capacitance connected to the top plate of the switched capacitor. The output voltage for this circuit is given in the z-domain as

$$V_{out}(z) = - \left[\frac{C_u + C_p}{C_I} \right] \frac{z^{-1}}{1-z^{-1}} V_1(z) + \left[\frac{C_u}{C_I} \right] \frac{z^{-1}}{1-z^{-1}} V_2(z). \quad (A3.5)$$

Obviously, C_p alters the gain constant associated with the top-plate input. Eqn. (A3.5) is modelled using DINAP elements in Fig. A3.3(b).

A3.2.2. Op Amp DC Gain Effects

An inverting type-I integrator is shown in Fig. A3.4(a) where it is assumed that the op amp has infinite bandwidth with an open-loop DC gain of A_o . The output voltage for this switched capacitor circuit (neglecting the top-plate parasitic capacitance) is given by

$$V_{out}(z) = \frac{- \left[\frac{C_u}{C_I} \right] A_o z^{-1}}{1 + A_o + \left[\frac{C_u}{C_I} \right]} V_{in}(z) + \frac{\left[A_o + 1 \right] z^{-1}}{1 + A_o + \left[\frac{C_u}{C_I} \right]} V_{out}(z) \quad (A3.6)$$

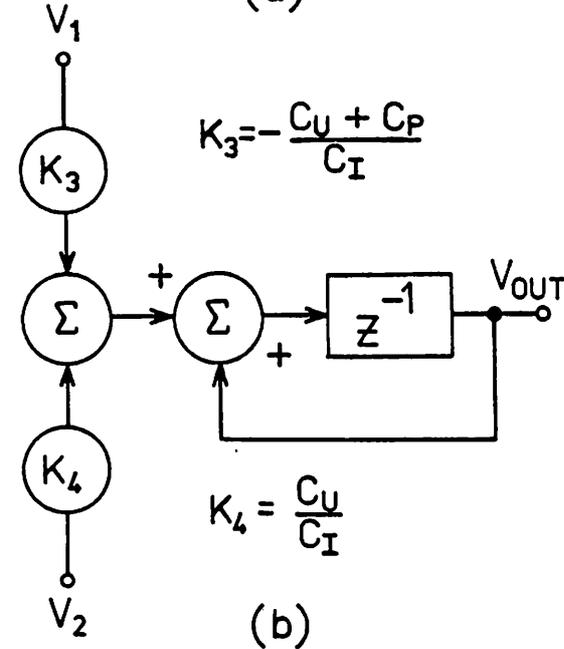
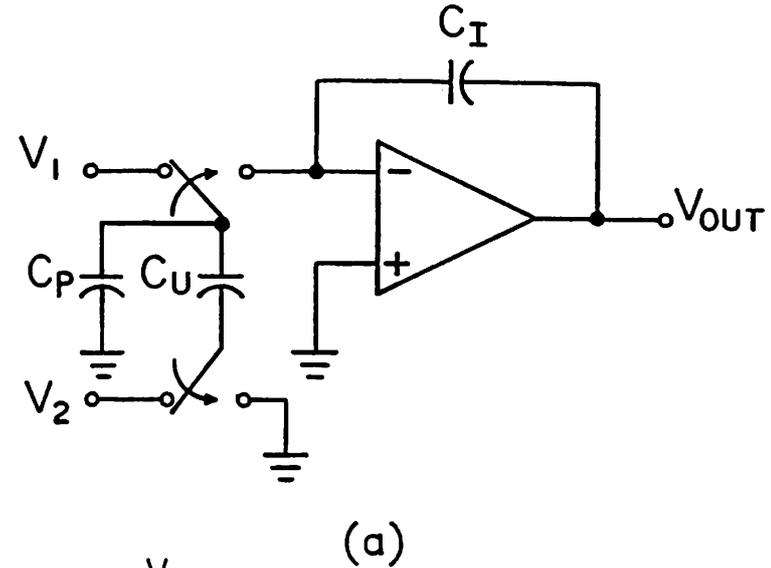
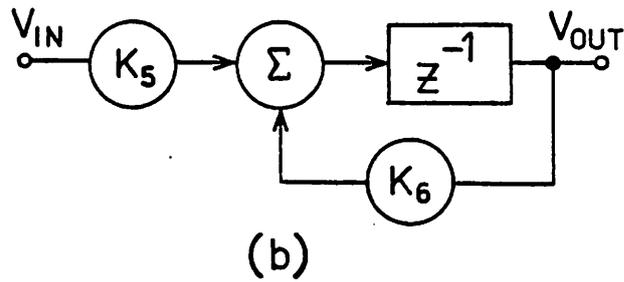
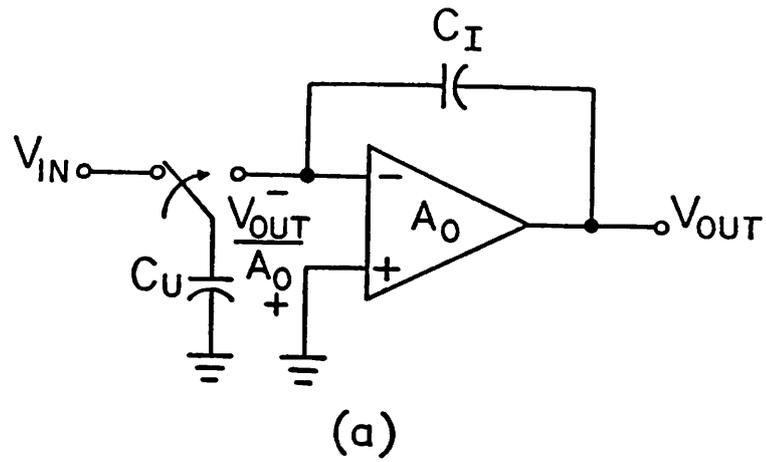


Fig. A3.3. (a) A type-I differential switched capacitor integrator with top-plate parasitic capacitance, C_p , and (b) the digital filter equivalent circuit.



$$K_5 = \frac{-\frac{C_U}{C_I} A_0}{1 + A_0 + \frac{C_U}{C_I}}$$

$$K_6 = \frac{1 + A_0}{1 + A_0 + \frac{C_U}{C_I}}$$

Fig. A3.4. (a) A type-I inverting switched capacitor integrator with finite op amp DC open-loop gain, and (b) a digital filter equivalent circuit.

with the DINAP model shown in Fig. A.3.4(b).

Other analog effects can be modelled for simulation with DINAP using similar techniques.

REFERENCES

- [1] R.A. Friedenson, R.W. Daniels, R.J. Dow, and P.H. McDonald, "RC active filters for the D3 channel bank," *Bell System Technical Journal*, vol. 54, no. 3, pp. 507-529, March 1975.
- [2] K.S. Tan and P.R. Gray, "Fully integrated analog filters using Bipolar/JFET technology," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 814-821, December 1978.
- [3] D.D. Buss, D.R. Collins, W.H. Bailey, and C.R. Reeves, "Transversal filtering using charge transfer devices," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 138-146, April 1973.
- [4] R.D. Baertsch, W.E. Engeler, H.S. Goldberg, C.M. Puckette, and J.J. Tiemann, "The design of practical charge-transfer transversal filters," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 133-142, February 1976.
- [5] C.H. Séquin, "Antialiasing inputs for charge-coupled devices," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 609-616, December 1977.
- [6] D.L. Fried, "Analog sampled data filters," *IEEE J. Solid-State Circuits*, vol. SC-7, pp. 302-304, August 1972.
- [7] A. Fettweis, "Theory of resonant transfer circuits," *Adv. Study Institute on Network and Switching Theory*, Italy, September 1966.
- [8] K. Hirano and S. Nishimura, "Active RC filters containing periodically operated switches," *IEEE Trans. on Circuit Theory*, May 1972.
- [9] L.R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*, Prentice-Hall, Inc., Chap. 2, 1975.
- [10] A.V. Oppenheim and R.W. Schaffer, *Digital Signal Processing*, Prentice-Hall, Inc., Chap. 4, 1975.
- [11] I.A. Young, P.R. Gray and D.A. Hodges, "Analog NMOS sampled data recursive filters," *Digest Int. Solid-State Circuits Conf. (Philadelphia)*, pp. 156-157, February 1977.
- [12] R.C. Agarwal and C.S. Burrus, "New recursive digital filter structures having very low sensitivity and roundoff noise," *IEEE Trans. on Circuits and Systems*, vol. CAS-22, no. 12, pp. 921-927, December 1975.
- [13] B.J. Hosticka, R.W. Brodersen and P.R. Gray, "MOS sampled data recursive filters using state variable techniques," *Proc. Int. Symp. on Circuits and Systems (Phoenix)*, pp. 525-529, April 1977.
- [14] B.J. Hosticka, R.W. Brodersen and P.R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600-608, December 1977.
- [15] J.T. Caves, M.A. Copeland, C.F. Rahim, and S.D. Rosenbaum, "Sampled analog filtering using switched capacitors as resistor equivalents," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 592-599, December 1977.
- [16] H.J. Orchard, "Inductorless filters," *Electronic Letters*, vol. 2, pp. 224-225, June 1966.
- [17] K.R. Laker, M.S. Ghauri and J.J. Kelly, "Minimum sensitivity active (leapfrog) and passive ladder bandpass filters," *IEEE Trans. on Circuits and Systems*, vol. CAS-22, pp. 670-677, August 1975.
- [18] F.E.J. Girling, and E.F. Good, "Applications of active ladder synthesis," *Wireless World*, pp. 445-450, September 1970.

- [19] G. Szentirmai, "Synthesis of multi-feedback active filters," *Bell System Technical Journal*, pp. 527-555, April 1973.
- [20] W.E. Heinlein and W.H. Holmes, *Active Filters for Integrated Circuits*, Prentice-Hall International, Inc., Chap. 8, 1974.
- [21] J.L. McCreary and P.R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques--part I," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 371-379, December 1975.
- [22] R.E. Suarez, P.R. Gray and D.A. Hodges, "All-MOS charge redistribution analog-to-digital conversion techniques--part II," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 379-385, December 1975.
- [23] G. Smarandoiu, "Nonlinear converters for pulse-code-modulation systems," Ph.D. Thesis, ERL Memo No. UCB/ERL M78/27, Electronics Research Laboratory, University of California, Berkeley, CA, May 1978.
- [24] D.J. Allstot, R.W. Brodersen and P.R. Gray, "Fully-integrated high order NMOS sampled data ladder filters," *Digest Int. Solid-State Circuits Conf. (San Francisco)*, pp. 82-83, February 1978.
- [25] D.J. Allstot, R.W. Brodersen and P.R. Gray, "MOS switched capacitor ladder filters," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 806-814, December 1978.
- [26] A.I. Zverev, *Handbook of Filter Synthesis*, John Wiley and Sons, Inc., New York, 1967.
- [27] G.C. Temes and J.W. LaPatra, *Introduction to Circuit Synthesis and Design*, McGraw-Hill Book Co., New York, 1977.
- [28] DINAP--A Digital Network Analysis Program, Dept. of Electrical Engineering and Computer Sciences, Purdue University, Lafayette, Indiana.

- [29] Harry H-F Lam, *Analog and Digital Filters: Design and Realization*, unpublished manuscript, July 1976.
- [30] E. Cohen, "Program Reference for SPICE2," ERL Memo No. ERL-M592, Electronics Research Laboratory, University of California, Berkeley, CA, June 1976.
- [31] R. Easton, private communication.
- [32] K.S. Tan, private communication.
- [33] P.R. Gray, private communication.
- [34] G. Kelson, H.H. Stellrecht, and D.S. Perloff, "A monolithic subsystem for high-accuracy A/D conversion," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 396-403, December 1973.
- [35] E.I. Jury, *Theory and Application of the Z-Transform Method*, John Wiley and Sons, Inc., New York, 1964.
- [36] C.F. Kurth and G.S. Moschytz, "Two-port analysis of cascaded switched capacitor networks," *IEEE Trans on Circuits and Systems*. (To be published).
- [37] Y.P. Tsividis, "Experimental and analytical evaluation of a switched capacitor filter and remarks on the resistor/switched capacitor correspondence," *IEEE Trans. on Circuits and Systems*. (To be published).
- [38] G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design considerations for MOS switched capacitor ladder filters," *Proc. Int. Symp. on Circuits and Systems (New York)*, pp. 324-329, May 1978.
- [39] G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched capacitor ladder filters," *IEEE Trans. on Circuits and Systems*, vol. CAS-25, pp. 1014-1021, December 1978.

- [40] L.T. Bruton, F.N. Trofimenkoff and D.H. Treleaven, "Noise performance of low-sensitivity active filters," IEEE J. Solid-State Circuits, vol. SC-8, pp. 85-91, February 1973.
- [41] G.M. Jacobs, "Practical design considerations for MOS switched capacitor ladder filters," ERL Memo No. UCB/ERL M77/69, Electronics Research Laboratory, University of California, Berkeley, CA, November 1977.
- [42] L.T. Bruton, "Low Sensitivity digital ladder filters," IEEE Trans. on Circuits and Systems, vol. CAS-22, no. 3, pp. 168-176, March 1975.
- [43] D.E. Johnson, *Introduction to Filter Theory*, Prentice-Hall International, London, 1976.
- [44] A.A. Ibrahim, G.J. Hupe and T.G. Foxall, "Double-split-Electrode transversal filter for telecommunications applications," IEEE J. Solid-State Circuits, February 1979. (To be published).
- [45] P.R. Gray, private communication.
- [46] D.J. Allstot, R.W. Brodersen and P.R. Gray, "Considerations for MOS implementations of switched capacitor filters," Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA., November 1978.
- [47] D. Senderowicz, P.R. Gray and D.A. Hodges, "High performance depletion-load NMOS operational amplifier," IEEE J. Solid-State Circuits, vol. SC-13, pp. 760-766, December 1978.
- [48] K.S. Tan, private communication.
- [49] D.A. Vaughn-Pope and L.T. Bruton, "Transfer function synthesis using generalized doubly-terminated two-pair networks," IEEE Trans. on Circuits and Systems, vol. CAS-24, pp. 79-88, February 1977.

- [50] S.K. Mitra and R.J. Sherwood, "Digital ladder networks," IEEE Trans. on Audio and Electroacoustics, vol. AU-21, pp. 30-36, February 1973.
- [51] W.C. Black, Jr., D.J. Allstot and R.P. Thiels, "Low-power CMOS monolithic switched capacitor PCM filters," (To be published).
- [52] B.J. White, G.M. Jacobs and G.F. Landsburg, "Fully-integrated DTMF receiver," Digest of the Int. Solid-State Circuits Conf. (Philadelphia, Pa.), pp. 36-37, February 1979.
- [53] B.J. Hosticka, "MOS sampled data recursive filters using state variable techniques," ERL Memorandum No. ERL-M77/65, Electronics Research Laboratory, University of California, Berkeley, CA, August 1977.
- [54] I.A. Young, "MOS switched-capacitor analog sampled-data recursive filters," Ph.D. Thesis, Memorandum No. UCB/ERL M78/61, Electronics Research Laboratory, University of California, Berkeley, CA, November 1978.
- [55] R.W. Brodersen, private communication.
- [56] P.R. Gray, D. Senderowicz, H. O'Hara, and B.W. Warren, "A single-chip NMOS dual channel filter for PCM telephony applications," ISSCC Digest of Technical Papers (Philadelphia), pp. 26-27, February 1979.
- [57] C.R. Hewes, private communication.
- [58] J. L. McCreary, "Successive Approximation Analog-to-Digital Conversion Techniques in MOS Integrated Circuits," Ph.D. Thesis, University of California, Berkeley, 1975.
- [59] D. J. Allstot, R. W. Brodersen, and P. R. Gray, "An electrically programmable analog NMOS second-order filter," Digest of the Int. Solid-State Circuits Conf. (Philadelphia), pp. 76-77, February 1979.

- [60] W. J. Kerwin, L. P. Huelsman and R. W. Newcomb, "State-variable synthesis for insensitive circuit transfer functions," *IEEE J. Solid-State Circuits*, vol. SC-2, pp. 87-92, September 1967.
- [61] D. J. Allstot, R. W. Brodersen and P. R. Gray, "A digitally programmable analog NMOS switched capacitor filter," *IEEE J. Solid-State Circuits*, December 1979. (To be published).
- [62] L. R. Rabiner and R. W. Schafer, *Digital Processing of Speech Signals*, Prentice-Hall, Inc., New York, 1978.
- [63] T. Tsuda, G. Evancoe, et al, "A formant speech synthesizer using MOS/LSI technology," (To be published).
- [64] R. W. Brodersen, P. R. Gray and D. A. Hodges, "MOS switched capacitor filters," *Proceedings of the IEEE*, January 1979.
- [65] R. G. Meyer, "Nonlinear analog integrated circuits," EECS 240 class notes, University of California, Berkeley, 1976.
- [66] K. Martin and A. Sedra, "Designing leapfrog and SFG filters with optimum dynamic range," *Proceeding of the IEEE (letter)*, vol. 65, pp. 1210, August 1977.
- [67] R. W. Brodersen, private communication.