A UNIFORM CHANNEL IGFET

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ABSTRACT

It is shown that there are bias conditions for an IGFET with a resistive gate that will cause both channel charge and field along the channel to be constant. Under these conditions, velocity along the channel is proportional to the current. The experimental constraints that are necessary to take account of variable bulk charge and of misoriented gate contacts are derived.

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INTRODUCTION

An insulated-gate field-effect transistor (IGFET) having useful properties can be constructed if the gate is made of resistive material and provided with two contacts. Depending on the location of the gate contacts, a voltage can be applied either parallel to [1] or transverse to [2] to the current flowing in the channel between the source and the drain. This paper will consider only resistive-gate structures in which the potential drop is parallel to the channel current.

A schematic diagram of an n-channel resistive-gate IGFET fabricated on a p-type silicon substrate is shown in Fig. 1. There are two contacts to the gate, one above the source (called the source gate), and the other above the drain (called the drain gate). Except for the modifications to the gate, the device is identical to a conventional IGFET. If the potential of the neutral bulk is taken as zero, the potential of the source gate is $\left[V_{GS}(0) + V_{SB} - \phi_{MS}\right]$ where $V_{GS}(0)$ is the bias between the source gate and the source electrode, V_{SB} is the bias between the source and the substrate, and ϕ_{MS} is the work function difference between the metal gate and the silicon substrate. The potential of the drain gate is $\left[V_{GS}(0) + \Delta V + V_{SB} - \phi_{MS}\right]$ where ΔV is the bias between the two gate contacts. The potential of the drain is $\left[V_{DS} + V_{SB} + 2\,\phi_F\right]$ where V_{DS} is the bias between the drain and the source and ϕ_F is the Fermi potential of the substrate.

The coordinate system used in the analysis of the device is as shown in Fig. 1. The y-axis is directed along the length of the channel and the z-axis along its width. The x-axis is directed toward the

substrate. The channel has a length L and a width Z. It is assumed that Z>>L.

We describe the channel of an IGFET as uniform when neither the channel charge per unit area $Q_n(y)$ nor the channel field $\mathcal{E}_y(y)$ vary from the source to the drain. In a conventional IGFET, if the gate and substrate bias are held constant while the drain bias is increased, the channel charge is reduced near the drain, but unaffected at the source. Therefore, a uniform channel is only approached in the conventional IGFET when the gate bias is much larger than the drain bias.

With a resistive-gate IGFET the reduction of the channel charge that is caused by increasing the drain bias can be counteracted by the increase in channel charge when the gate bias is increased toward the drain. It is thus possible to achieve a uniform channel by balancing these competing effects and, as a result, to obtain the capability of varying the gate and channel fields independently of each other.

A uniform channel is useful to investigate the transport properties of surface free-carriers because it imposes a proportional relationship between the current-voltage characteristic of the IGFET and the velocity-field characteristic of the surface carriers. In this paper we derive the bias conditions under which the channel in a resistive-gate IGFET is uniform. In a companion paper [3] we present the velocity-field curves for surface carriers obtained from measurements on resistive-gate IGFET's.

THEORY

In a resistive-gate device the gate bias is a function of y. For a uniform resistor, the gate bias is given by

$$V_{GS}(y) = V_{GS}(0) + \Delta V \frac{y}{L} \tag{1}$$

The formulas used to analyze the conventional IGFET can be applied to the resistive-gate device provided that they are modified to account for the potential drop across the gate. Using Eq. (1) we find that the equation for the channel charge in strong inversion [4] becomes

$$Q_n(y) = -C_i \left\{ V_{GS}(0) + \Delta V \frac{y}{L} - V_{FB} - 2\phi_F - \left(V - V_{SB}\right) - \frac{1}{C_i}\sqrt{2q\,\varepsilon_s N_A \left(2\phi_F + V\right)} \right\} \tag{2}$$

where C_i is the capacitance per unit area of the insulator and V(y) is the bias between the surface and the bulk. The other symbols have their usual meaning. We restrict our discussion to values of V_{SB} and V_{DS} satisfying the inequality

$$V_{SB} \geq V_{DS} \tag{3}$$

Therefore, we can expand the square root term in Eq. (2) to obtain

$$Q_n(y) = Q_n(0) - C_i\left[\Delta V \frac{y}{L} - \gamma\left(V - V_{SB}\right)\right] \tag{4}$$

where $Q_n(0)$ is the channel charge at the source and

$$\gamma = 1 + \frac{1}{2C_i}\sqrt{\frac{2q\,\varepsilon_s N_A}{2\phi_F + V_{SB}}} \tag{5}$$

If we assume that a uniform channel has been achieved, then $Q_n(y)$ and $\mathcal{E}_y(y)$ will be independent of y. The channel field and the bias between the surface and the bulk are related by

$$\mathcal{E}_y(y) = -\frac{dV}{dy} \tag{6}$$

Since $\mathcal{E}_y(y)$ is constant

$$V(y) = V_{SB} + V_{DS}\frac{y}{L} \tag{7}$$

With V(y) given by Eq. (7) we see from Eq. (4) that the channel charge is constant if

$$\Delta V = \gamma V_{DS} \tag{8}$$

Eq. (4) gives the channel charge under the condition $V_{SB} \geq V_{DS}$. If Eq. (7) is substituted into Eq. (2) which is the more general equation for the channel charge, we find that there is no value of ΔV that will yield a constant channel charge and hence a uniform channel unless the square-root term in Eq. (2) can be converted into a linear function of V(y). The square-root term represents the contribution of the charge in the depletion layer to the total charge in the semiconductor. In the derivation of Eq. (4) we converted the depletion-layer charge into a linear function of V(y) by expanding the square-root and retaining only the first two terms of the expansion.

We have shown that the bias condition stated in Eq. (8) is necessary for the existence of a uniform channel. The bias condition is sufficient if it ensures that Eq. (7) is the solution of the IGFET differential equation. The IGFET differential equation can be written [5]

$$\frac{dV}{dy} = -\frac{I_D}{Z\bar{\mu}_n(y)Q_n(y)} \tag{9}$$

where I_D is the drain current and $\bar{\mu}_n(y)$ is the average electron mobility. With ΔV given by Eq. (8) the substitution of Eq. (7) into the differential equation yields

$$\frac{V_{DS}}{L} = - \frac{I_D}{Z\bar{\mu}_n(y)Q_n(0)} \tag{10}$$

Clearly Eq. (7) satisfies the differential equation (i.e., both sides of the equation are constant) if the mobility $\bar{\mu}_n$ is independent of y. In general, the mobility is a function of the gate field $\mathcal{E}_x(y)$ and the channel field $\mathcal{E}_y(y)$ so that the y-dependence of the mobility arises because of the y-dependence of these fields. Since the channel field is constant when V(y) is given by Eq. (7), the mobility has no y-dependence owing to a dependence on $\mathcal{E}_y(y)$. In general then, Eq. (7) satisfies the differential equation only if the gate field $\mathcal{E}_x(y)$ is constant. The gate field is given by

$$\mathcal{E}_x(y) = \frac{C_i}{\epsilon_s}\left\{V_{GS}(0) + \Delta V \frac{y}{L} - V_{FB} - 2\phi_F - \left(V-V_{SB}\right)\right\} \tag{11}$$

With V(y) given by Eq. (7) and ΔV given by Eq. (8) we find that

$$\mathcal{E}_x(y) = \mathcal{E}_x(0) + \frac{C_i V_{DS}}{\epsilon_s L}\left(\gamma-1\right)y \tag{12}$$

where $\mathcal{E}_x(0)$ is the gate field at the source. Eq. (12) shows that the gate field is constant only if $\gamma = 1$.

From the preceding discussion we conclude that the bias condition stated in Eq. (8) is sufficient for the existence of a uniform channel if the mobility is either constant or a function only of the channel field. If the mobility also depends on the gate field, we have the additional requirement that $\gamma = 1$. From Eq. (5) we see that $\gamma \to 1$ as the substrate bias is increased. It is not possible for γ to be precisely one, but when the mobility depends on the gate field, we expect the channel to be approximately uniform when $\gamma \lesssim 1$. In order to check this conclusion, Eq. (9) was solved numerically.

In the general one-dimensional theory of the IGFET developed by Sah and Pao [5], the channel charge is given by

$$Q_n\left(\phi_s, V\right) = -\frac{C_D}{2}\int_o^{\phi_s} \frac{\exp\left[q\left(\Phi-V-2\Phi_F\right)/k_BT\right]d\Phi}{F\left(\Phi,V\right)} \tag{13}$$

where ϕ is the electrostatic potential, ϕ_s is the surface potential,

$$C_D = \left[\frac{2\varepsilon_s q^2 N_A}{k_B T}\right]^{1/2} \tag{14}$$

and

$$F(\phi,V) \cong \left[e^{q\left(\phi-V-2\phi_F\right)/k_BT+q\phi/k_BT-1}\right]^{1/2} \tag{15}$$

It has been shown that the dependence of the mobility on the gate and channel fields is well described by an empirical relationship of the form [6]

$$\bar{\mu}_n = \frac{\mu_o}{\left[1+\left|\frac{\mathcal{E}_x(y)}{\mathcal{E}_{cx}}\right|\right]\left[1+\left|\frac{\mathcal{E}_y(y)}{\mathcal{E}_{cy}}\right|\right]} \tag{16}$$

where μ_o is the low-field mobility and the constants $\mathcal{E}_{cx}$ and $\mathcal{E}_{cy}$ are the critical fields for the gate and channel, respectively. Using Eqs. (13) and (16) the solution of Eq. (9) is obtained by solving for the values of ϕ_s, V, Q_n, $\mathcal{E}_x$, and $\mathcal{E}_y$ at n equally spaced points along the channel. The values at the point $\left(y_{n+1}, V_{n+1}\right)$ are obtained from the point $\left(y_n, V_n\right)$ by the fourth-order Runge-Kutta method [7].

In Fig. 2a-c and Fig. 3a-c we show plots of $Q_n/Q_n(0)$, $\mathcal{E}_x/\mathcal{E}_x(0)$,

and $\mathcal{E}_y/(V_{DS}/L)$ obtained from the numerical solution of Eq. (9). The constants $Q_n(0)$ and $\mathcal{E}_x(0)$ are the channel charge and gate field at the source, respectively. In making these plots we have taken

$$C_i = 3.45 \times 10^{-8} \text{ F cm}^{-2}, \quad N_A = 10^{15} \text{ cm}^{-3}, \text{ and } L = 10 \text{ } \mu\text{m}.$$

We have assumed that $\mathcal{E}_{cx} = 2 \times 10^5 \text{Vcm}^{-1}$ and $\mathcal{E}_{cy} = 3 \times 10^3 \text{Vcm}^{-1}$. These values for $\mathcal{E}_{cx}$ and $\mathcal{E}_{cy}$ were chosen in order to observe the effect of a field-dependent mobility on the solutions without the need of a large bias because the computer time needed to solve Eq. (9) becomes excessive if the gate and drain bias are too large. Typical values for $\mathcal{E}_{cx}$ and $\mathcal{E}_{cy}$ are somewhat larger than the ones we have used [6]. We have also assumed a constant density of fast surface states $N_{fs} = 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$.

The plots shown in Fig. 2a-c were obtained for the bias condition $V_{DS} = V_{SB} = 2.58$ V and $V_{GS}(0) = 5.16$ V. For this bias condition $\mathcal{E}_x(0) \simeq \mathcal{E}_{cx}$ and $V_{DS}/L \simeq \mathcal{E}_{cy}$. The solution of Eq. (9) was obtained at 54 points along the channel. Two sets of points are plotted: one set for $\Delta V = 0$ (Δ) and the other set for $\Delta V = 2.96$ V ($\square$) which is the bias required by Eq. (8) for a uniform channel. The result for a uniform channel is shown by the solid line. From Fig. 2b we see that with $\Delta V = 2.96$ V, the gate field increases from the source to the drain as is expected from Eq. (12). However, the corresponding solutions for the channel charge and channel field, as shown in Fig. 2a and Fig. 2c, respectively, are very close to the solution for a uniform channel.

The plots shown in Fig. 3a-c were obtained for the bias condition $V_{DS} = V_{SB} = 5.16$ V and $V_{GS}(0) = 5.16$ V. For this bias condition $\mathcal{E}_x(0) \simeq \mathcal{E}_{cx}$ and $V_{DS}/L \simeq 2\mathcal{E}_{cy}$. The solution of Eq. (9) was obtained

at 107 points along the channel, but only every other point has been plotted. Only the solution for the bias $\Delta V = 5.72$ V is shown which is the bias required for a uniform channel. Because of the increase in bias, the increase in gate field that is shown in Fig. 3b is greater than that shown in Fig. 2b. However, the corresponding solutions for the channel charge and channel field, as shown in Figs. 3a and 3c, respectively, are still close to the solution for a uniform channel.

If the channel is approximately uniform, the variation of the gate field is given by Eq. (12). Let $\Delta\mathcal{E}_x/\mathcal{E}_x(0)$ be the percentage increase of the gate field between the source and drain. Shown in Fig. 4 is a plot of $\Delta\mathcal{E}_x/\mathcal{E}_x(0)$ versus V_{DS} for several values of $V_{GS}(0)$ calculated using Eq. (12). The plot was made for the bias condition $V_{SB} = V_{DS}$. It can be seen that $\Delta\mathcal{E}_x/\mathcal{E}_x(0)$ increases with increasing drain bias and increases with decreasing gate bias.

In order to be consistent with a uniform channel, the decrease in mobility as a result of the increase in gate field must be small. The dependence of the mobility on the gate field can be described by an empirical relationship of the form [6]

$$\mu = \frac{\mu_o}{1 + \left|\mathcal{E}_x(y)/\mathcal{E}_{cx}\right|} \tag{17}$$

Using this relationship the percentage decrease of the mobility between the source and drain $\Delta\mu/\mu(0)$ corresponding to the increase in the gate field shown in Fig. 4 can be found. Shown in Fig. 5 is a plot of $\Delta\mu/\mu(0)$ versus drain bias for the device of Fig. 4. In making this plot we have taken $\mathcal{E}_{cx} = 7.1 \times 10^5$ Vcm^{-1} which is a typical value for

our devices [3]. We see from the figure that the decrease in mobility is less than 4.1% for the entire range of bias considered in contrast to the increase in gate field shown in Fig. 4 which exceeds 40% for the smallest value of gate bias. The decrease in mobility is much less than the increase in gate field because the increase in gate field is large when the dependence of the mobility on the gate field is small, and the increase in gate field is small when the dependence of the mobility on the gate field is large. In summary, we conclude that, for the devices studied, the variation in mobility due to the variable gate field is sufficiently small for the channel to be a close approximation to a uniform channel when the bias conditions stated in Eqs. (3) and (8) are satisfied.

Effects of Misalignment of the Gate Contacts

The theory presented thus far has assumed that the source and drain gates are perfectly aligned to the edges of the source and drain diffusions. This alignment cannot be achieved in practice. In order to obtain a uniform channel, it is necessary to apply a voltage across the section of the gate that lies over the channel. Therefore, the source and drain gates must lie entirely over the diffusions as shown in Fig. 6. The gate resistance is divided into three parts: R_s which lies over the source diffusion, R_g which lies over the channel, and R_d which lies over the drain diffusion. The total gate resistance R_g' is, therefore, given by

$$R_g' = R_s + R_d + R_g \tag{18}$$

Because of the dimensional offset, the voltage across the section of the gate that lies over the channel is

$$\Delta V = \frac{Rg}{R'_g} \Delta V' \tag{19}$$

and the gate voltage at the edge of the source diffusion is

$$V_{GS}(0) = V'_{GS} + \frac{Rs}{R'_g} \Delta V' \tag{20}$$

where $\Delta V'$ is the bias between the two gate contacts and V'_{GS} is the bias between the source gate and the source electrode. The offset resistances affect the bias that must be applied in order to obtain a uniform channel. We have previously shown that a uniform channel required $\Delta V = \gamma V_{DS}$. When an offset is present, the bias that must be applied to achieve a uniform channel is

$$\Delta V' = \frac{R'_g}{Rg} \gamma V_{DS} \tag{21}$$

In order to apply the proper bias to obtain a uniform channel, we must know the values of R_s and R_d. A method of determining these resistances is as follows. First, we consider the channel conductance as a function of gate bias when $V_{DS} \simeq 0$. The channel conductance is defined

$$g_{ch} = \frac{\partial I_D}{\partial V_{DS}} \Big| V_{GS}, V_{SB} \tag{22}$$

In order to obtain an analytic expression for the channel conductance, we assume that the mobility is independent of the fields. Eq. (9) can then be integrated to give

$$I_D = \frac{Z\mu_o V_{DS}}{\int_o^L \frac{dy}{|Q_n|}} \tag{23}$$

It should be noted that the channel charge does not depend on V since we have assumed that $V_{DS} \simeq 0$, but it does depend on y because of the voltage drop ΔV across the gate. Using Eqs. (22) and (23) we find that

$$g_{ch} = \frac{Z\mu_o}{\int_o^L \frac{dy}{|Q_n|}} \tag{24}$$

Now we consider the threshold voltage V_T which is the value of the gate bias at which the channel becomes strongly inverted. Assume first that there is no misalignment ($R_s = R_d = 0$) and that $\Delta V > 0$. As $V_{GS}(0)$ is increased, the drain-gate bias reaches V_T first, but the entire channel does not become strongly inverted until $V_{GS}(0) = V_T$. When $V_{GS}(0) < V_T$ and $V_{GS}(0) + \Delta V > V_T$, the channel near the source is weakly inverted and the channel near the drain is strongly inverted.* Since the weakly and strongly inverted regions of the channel are in series, the weakly inverted region dominates in determining the channel conductance. Eq. (24) then reduces to

$$g_{ch} = \frac{Z\mu_o}{\int_o^{L_w} \frac{dy}{|Q_n|}} \tag{25}$$

where L_w is the length of the weak inversion region ($L_w \leq L$).
It has been shown [8] that in an MOS system under conditions of weak inversion

$$|Q_n| \simeq Ke^{qV_{GS}/nk_BT} \tag{26}$$

* The channel conductance is most sensitive to the gate voltage and hence to the offset resistances in weak inversion. If the entire channel is weakly inverted, the conductance is so small that accurate measurements are difficult. Therefore, in order to determine R_s and R_d, we only consider bias conditions such that part of the channel is weakly inverted and part of the channel is strongly inverted.

where K and n are constants. Substituting Eq. (1) into Eq. (26), we find that for the resistive-gate device

$$|Q_n| = Ke^{q\left[V_{GS}(0) + \Delta V\frac{y}{L}\right]/nk_BT} \tag{27}$$

Using this result Eq. (25) can be integrated to give

$$g_{ch} = \frac{Z\mu_o\, q\Delta V\, Ke^{qV_{GS}(0)/nk_BT}}{L\, n\, k_BT\left[1-\exp(-q\Delta VL_w/nk_BTL)\right]} \tag{28}$$

To interpret this equation, we note that when $\Delta V > 0$, the length of the weak-inversion region is related to the threshold voltage by

$$V_{GS}(0) + \Delta V\,\frac{L_w}{L} = V_T \tag{29}$$

Solving this expression for L_w and substituting the result into Eq. (28) gives

$$g_{ch} = \frac{Z\mu_o q\Delta V\, Ke^{qV_{GS}(0)/nk_BT}}{Lnk_BT} \tag{30}$$

provided that $\left[V_T - V_{GS}(0)\right]/n$ is greater than several k_BT/q. The separation of the measured curves of channel conductance versus V'_{GS} for two values of $\Delta V'$ ($\Delta V'_a$ and $\Delta V'_b$) can be found by solving Eq. (30) for the gate-bias difference at which two curves have the same value of conductance. Using Eqs. (19), (20), and (30) we find that, if $\Delta V'_b - \Delta V'_a$ is held constant and $\Delta V'_a$ is increased, the separation of successive curves approaches

$$V'_{GS_a} - V'_{GS_b} = \frac{R_s}{R'_g}\left(\Delta V'_b - \Delta V'_a\right) \tag{31}$$

Thus we see that the separation of curves for g_{ch} versus V'_{GS} for $\Delta V' > 0$ and $V_{GS}(0) < V_T$ can be used to determine R_s/R'_g. (In determining R_s/R'_g it is convenient to let $\Delta V'_b - \Delta V'_a = 1V$.)

The value of R_d/R'_g can be determined by interchanging the role of the source and drain and repeating the measurements for $\Delta V' > 0$. Alternatively, R_d/R'_g can be determined without interchanging the source and drain by measuring conductance versus voltage for $\Delta V' < 0$ and $V_{GS}(0) - |\Delta V| < V_T$. Following an analysis similar to that given above, we find that if $\Delta V'_b - \Delta V'_a$ is held constant and $\Delta V'_a$ is increased, the separation of successive conductive-voltage curves approaches

$$V'_{GS_a} - V'_{GS_b} = \left(1 - \frac{R_d}{R'_g}\right)\left[|\Delta V'_a| - |\Delta V'_b|\right] \tag{32}$$

Thus we see that the separation of curves of g_{ch} versus V'_{GS} for $\Delta V' < 0$ and $V_{GS}(0) - |\Delta V| < V_T$ can be used to determine R_d/R'_g.

In order to verify these results, Eq. (24) was integrated numerically using Simpson's rule. The integration used the analytic expression [9]

$$Q_n\left(\phi_s, V\right) = -C_D \frac{k_B T}{q}\left\{\left[e^{q(\phi_s - V - 2\phi_F)/k_B T} + \frac{q\phi_s}{k_B T} - 1\right]^{1/2} - \left[\frac{q\phi_s}{k_B T} - 1\right]^{1/2}\right\} \tag{33}$$

for the channel charge rather than the integral form given in Eq. (13) in order to avoid the excessive computer time needed to perform a double numerical integration. In Figs. 7 and 8 we show plots of normalized conductance g ($g = qg_{ch}L/Z\mu_o C_i k_B T$) versus V'_{GS} for various values of $\Delta V'$ obtained from the numerical integration of Eq. (24). In making these plots we have taken $C_i = 3.45 \times 10^{-8}$ Fcm^{-2}, $N_A = 10^{15}$ cm^{-3},

$L = 10\ \mu m$, and $N_{fs} = 5 \times 10^{10}\ eV^{-1}\ cm^{-2}$. Fig. 7 is for $R_s = R_d = 0$, and Fig. 8 is for $R_s/R'_g = 0.375$ and $R_d/R'_g = 0.125$.

In these plots the value of $\Delta V'$ changes by 1 volt between successive conductance-voltage curves. In Fig. 7 ($R_s = 0$) we see that in the region where $\Delta V' > 0$ and $V_{GS}(0) < V_T$ (the value of V_T can be obtained by extrapolating the linear portion of the conductance-voltage curve for $\Delta V' = 0$ to the voltage axis), the separation of successive curves goes to zero in accordance with Eq. (31). In Fig. 8 the separation approaches the value of R_s/R'_g also in agreement with Eq. (31). A similar agreement with Eq. (32) can be seen for the conductance-voltage curves in the region where $\Delta V' < 0$ and $V_{GS}(0) - |\Delta V| < V_T$.

A typical measurement of channel conductance versus the bias of the source gate is shown in Fig. 9. The measurement is for an n-channel IGFET fabricated on a (100) substrate. Conductance is measured for $\Delta V'$ between +5 and -5 volts with a 1 volt separation between each curve. For the device shown the total gate resistance R'_g is 290 Ω. From the plot we find that $R_s/R'_g = 0.18$ and $R_d/R'_g = 0.13$ so that $R_s = 52\ \Omega$ and $R_d = 38\ \Omega$. The values of R_s and R_d found in this manner are used in Eq. (21) to determine the bias required to establish a uniform channel.

As a further check on the theory discussed above, the channel conductance g_{ch} is measured as a function of V'_{GS} when various values of an external resistance R_e are placed between the source gate and the gate-source power supply. In the presence of the external resistor the source offset resistance becomes

$$R_s = R_{so} + R_e \tag{34}$$

where R_{so} is the value of R_s when $R_e = 0$, i.e., R_{so} is the built-in

offset resistance. Equation (34) is plotted in Fig. 10 along with values of R_s obtained from the conductance versus V'_{GS} technique. The measurements shown in Fig. 10 were made on a p-channel IGFET fabricated on a (100) substrate. There is good agreement between the measured values of R_s and the values predicted by Eq. (34).

The presence of the offset resistances has been attributed to the offset of the source gate and drain gate from the edges of the source and drain diffusions. Although this effect must be present, it is also found that part of the observed resistance is due to contact resistance between the aluminum lines which form the source gate and the drain gate and the nichrome film which forms the gate resistor. This is determined by varying the spacing between the aluminum lines and observing that the gate resistance approaches a limit that is independent of the spacing. This result is further verified by the fact that the values of R_s and R_d can be reduced by passing current through the gate resistor. The current apparently enhances the contact between the aluminum and the nichrome. The theory developed in this section is independent of the origin of the offset resistances. Only the values of R_s and R_d need to be determined in order to apply the bias necessary to achieve a uniform channel.

CONCLUSIONS

We have shown that the channel in a resistive-gate IGFET is approximately uniform when the bias conditions stated in Eqs. (3) and (21) are satisfied. Furthermore, in contrast to the conventional IGFET, the gate and channel fields can be varied independently of each other over a wide range of values. This is desirable since it permits

a simple interpretation of experimental data in terms of physical parameters. The resistive-gate IGFET has been used to measure the velocity-field characteristics of surface carriers. These results are presented in a companion paper [3].

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FIGURE CAPTIONS

1. Structure of an n-channel, resistive-gate IGFET.

2. Computed variation in the normalized channel parameters with position for an n-channel device having: $C_i = 3.45 \times 10^{-8}$ F cm^{-2}, $N_A = 10^{15}$ cm^{-3}, L = 10μm, $N_{fs} = 10^{10}$ eV^{-1} cm^{-2}: (a) channel charge, (b) gate field, (c) field along the channel.

3. Computed variation in the normalized channel parameters with position for the device of Fig. 2 under the bias conditions: $V_{DS} = V_{SB} = 5.16$V, $V_{GS}(0) = 5.16$V and $\Delta V = 5.71$V: (a) channel charge, (b) gate field, (c) field along the channel.

4. Calculated values of the percentage increase in the gate field between the source and drain versus drain bias for several values of V_{GS}. The channel is assumed uniform and the device parameters are the same as those given in the caption of Fig. 2.

5. Calculated values of the percentage decrease in mobility versus drain bias for several values of V_{GS}. The channel is assumed uniform and the device parameters are the same as those given in the caption of Fig. 2.

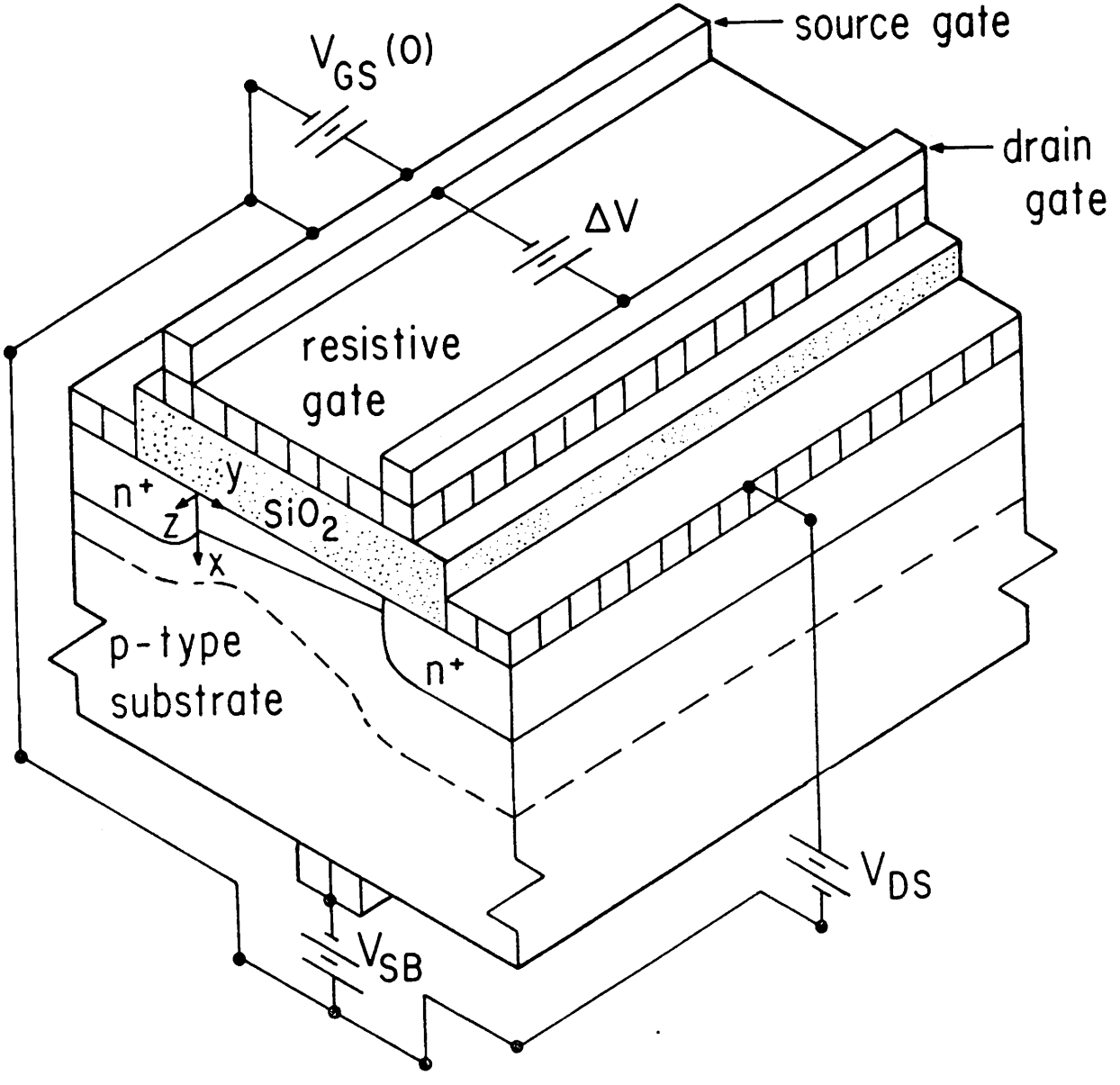
6. Cross section of a resistive-gate IGFET showing the origins of the source and drain contact resistances.

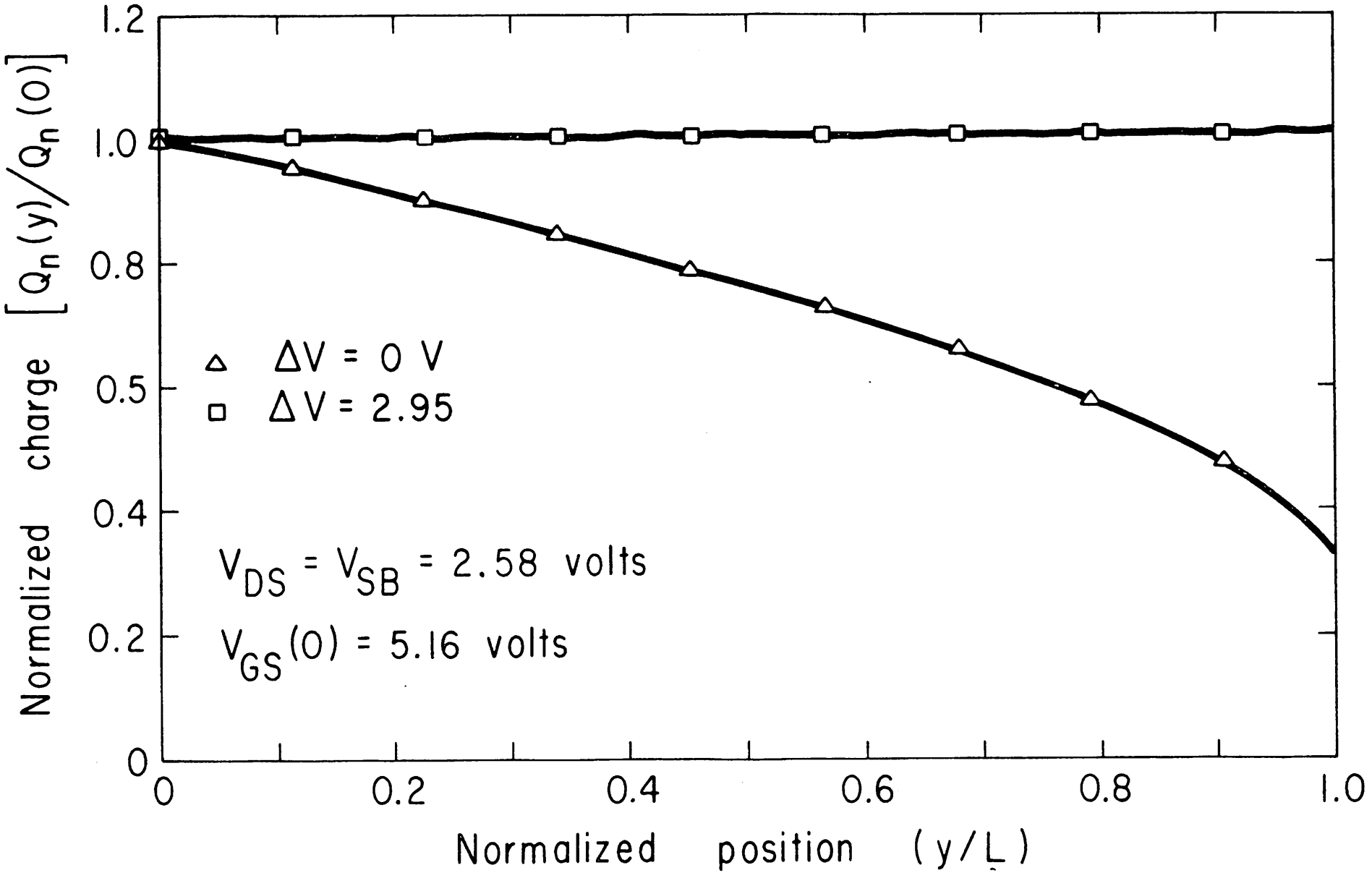
7. Normalized channel conductance g versus V'_{GS} for several values of $\Delta V'$ for $R_s = R_d = 0$ $\left(g = qg_{ch}L \Big/ \mu_o Z C_i k_B T \right)$. Device parameters are the same as those given in the caption of Fig. 2 except $N_{fs} = 5 \times 10^{10} eV^{-1} cm^{-2}$.

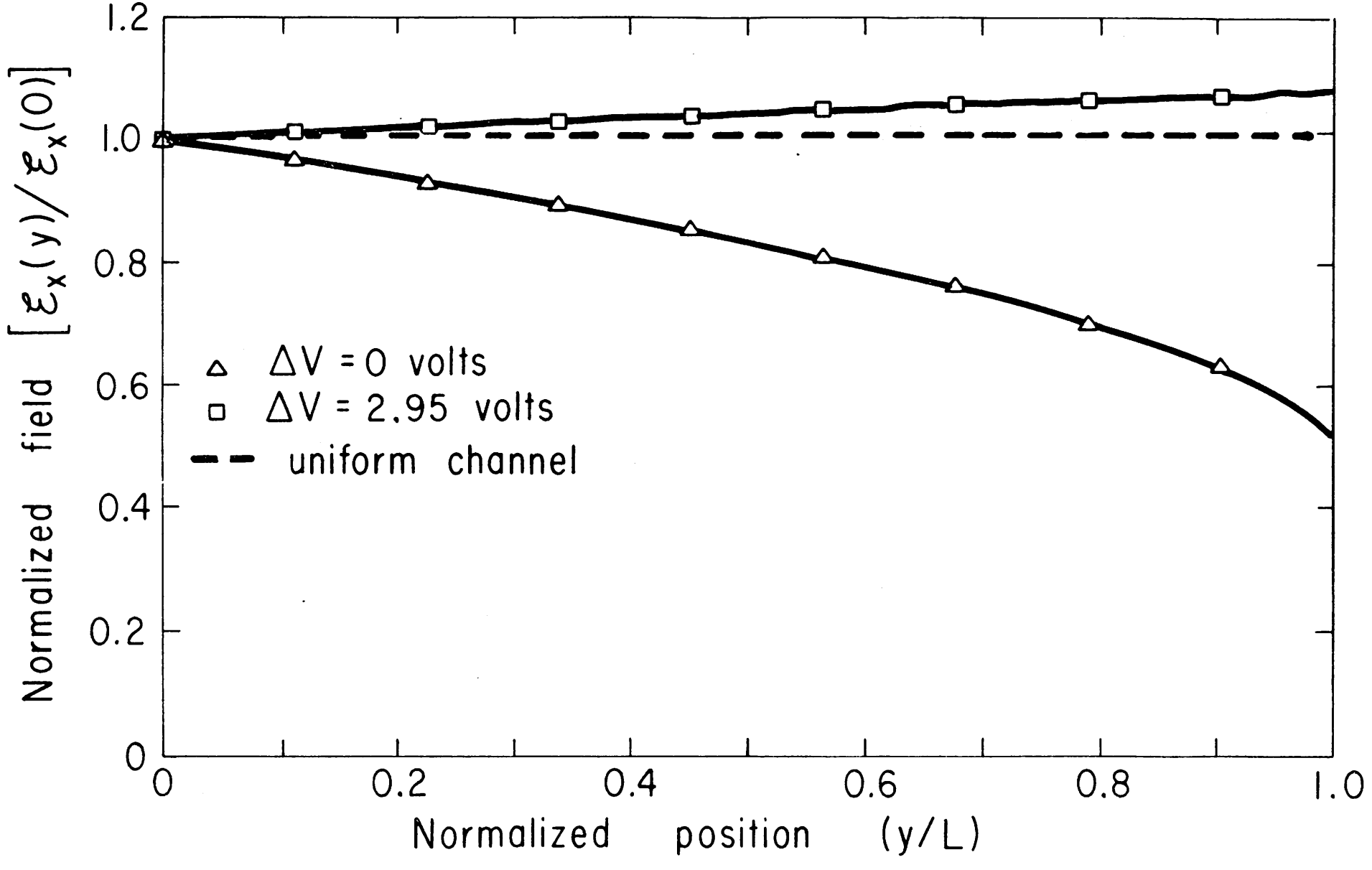
8. Normalized channel conductance versus V'_{GS} for several values of $\Delta V'$ for non-zero R_s and R_d for the device of Fig. 7.

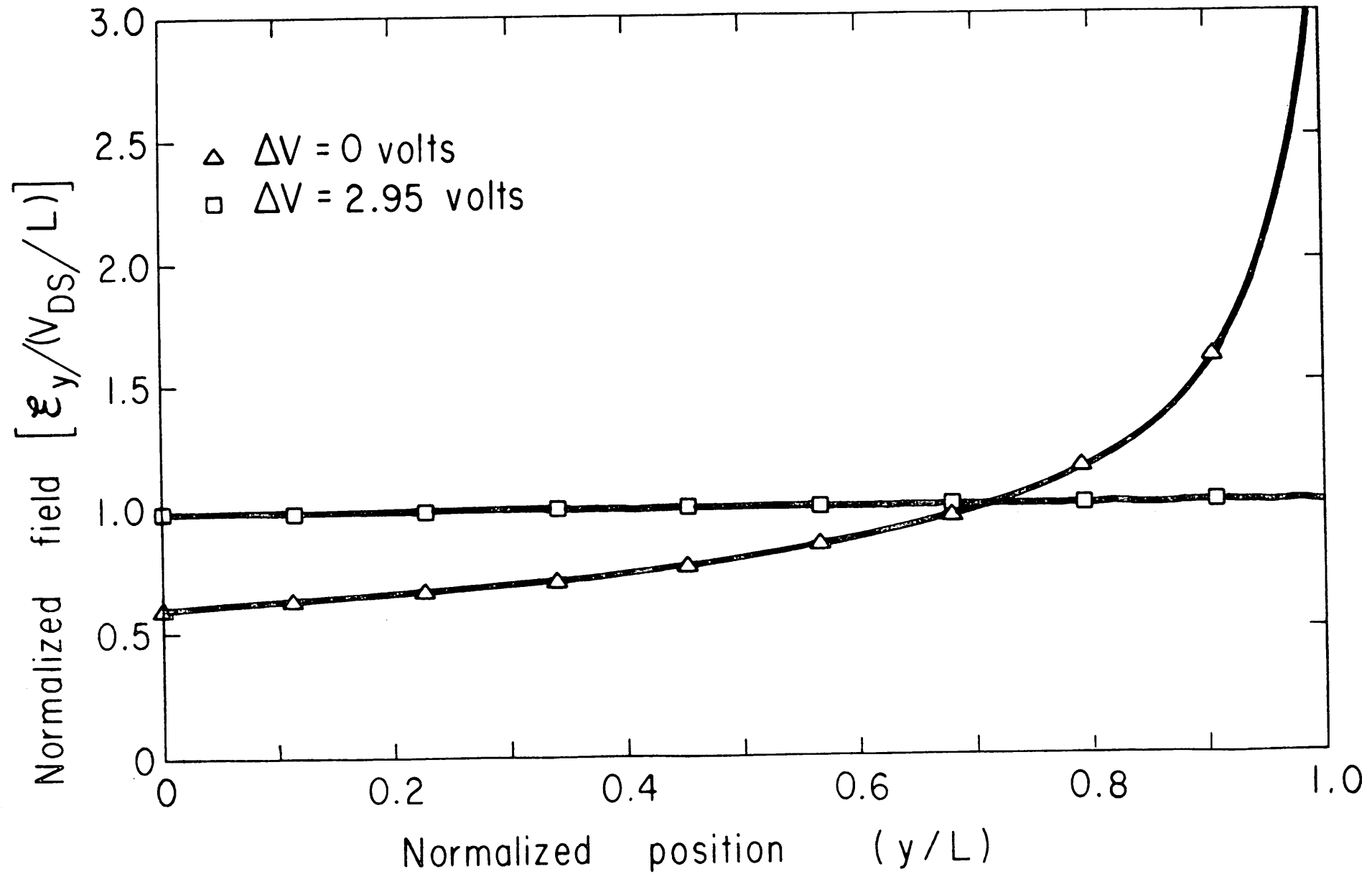
9. Channel conductance versus V'_{GS} for several values of $\Delta V'$ for a typical resistive-gate device.

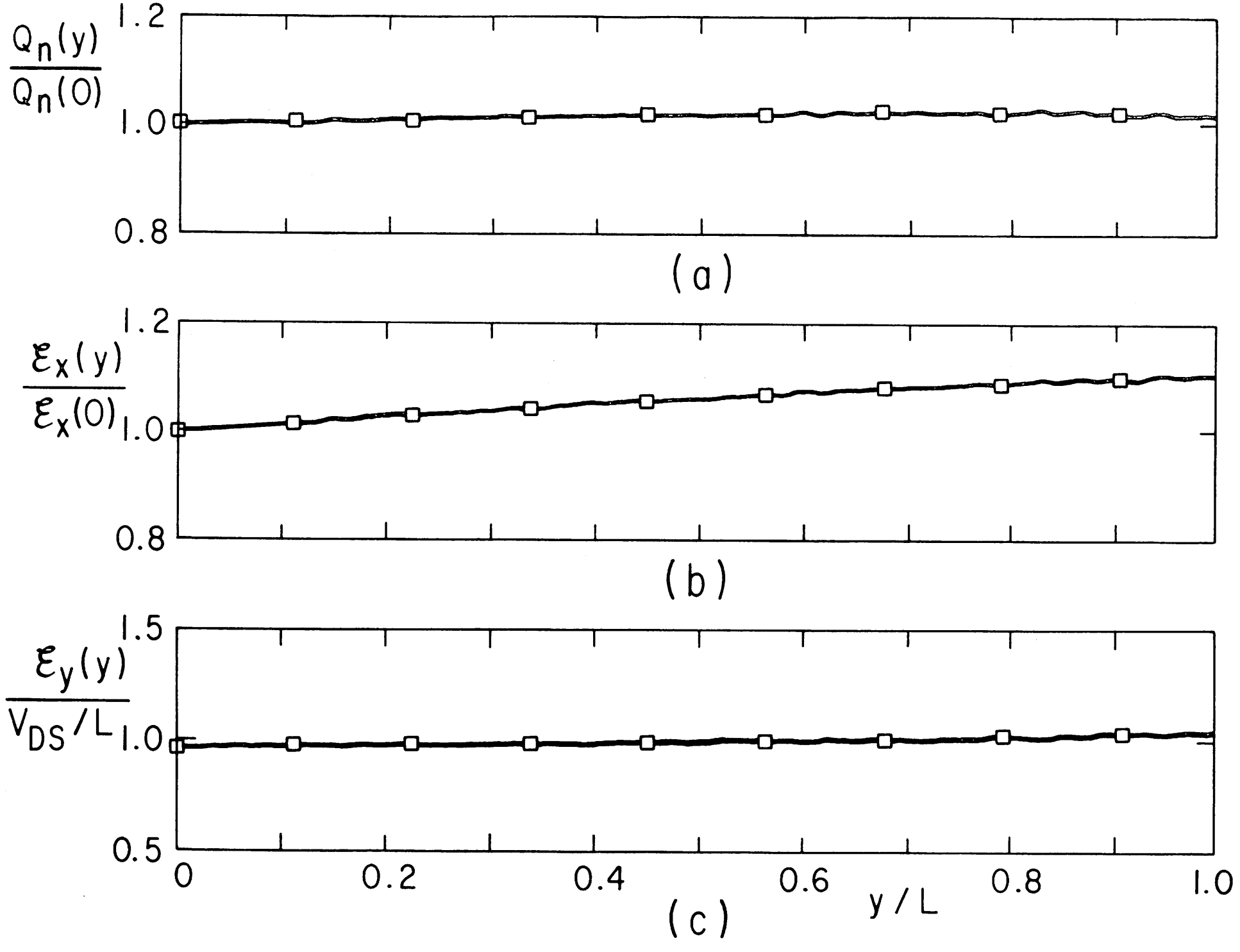
10. Source offset resistance versus external resistance.

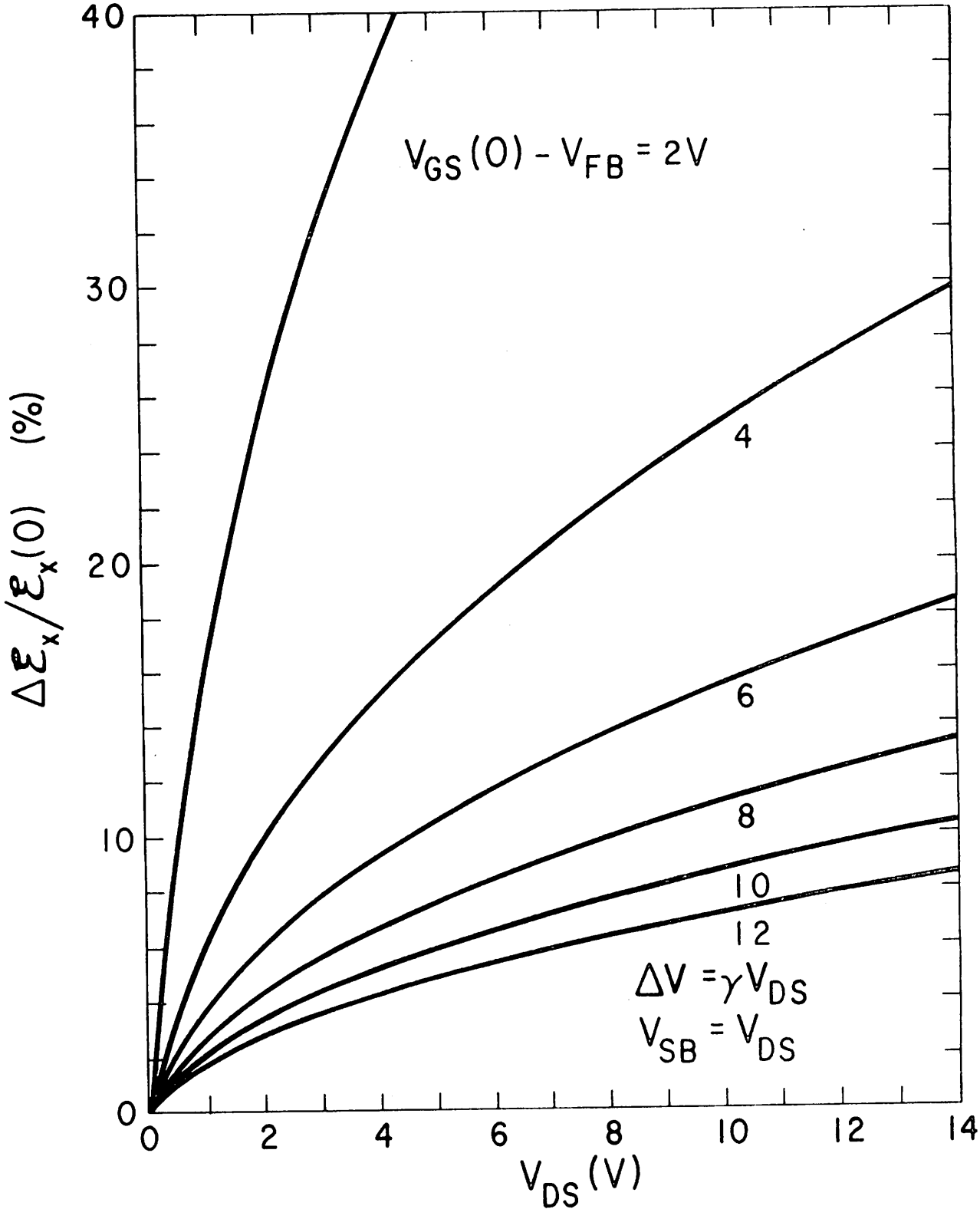

source gate
$V_{GS}(0)$
drain gate
ΔV
resistive gate
y
n^+
z
SiO_2
x
p-type substrate
n^+
V_{DS}
V_{SB}

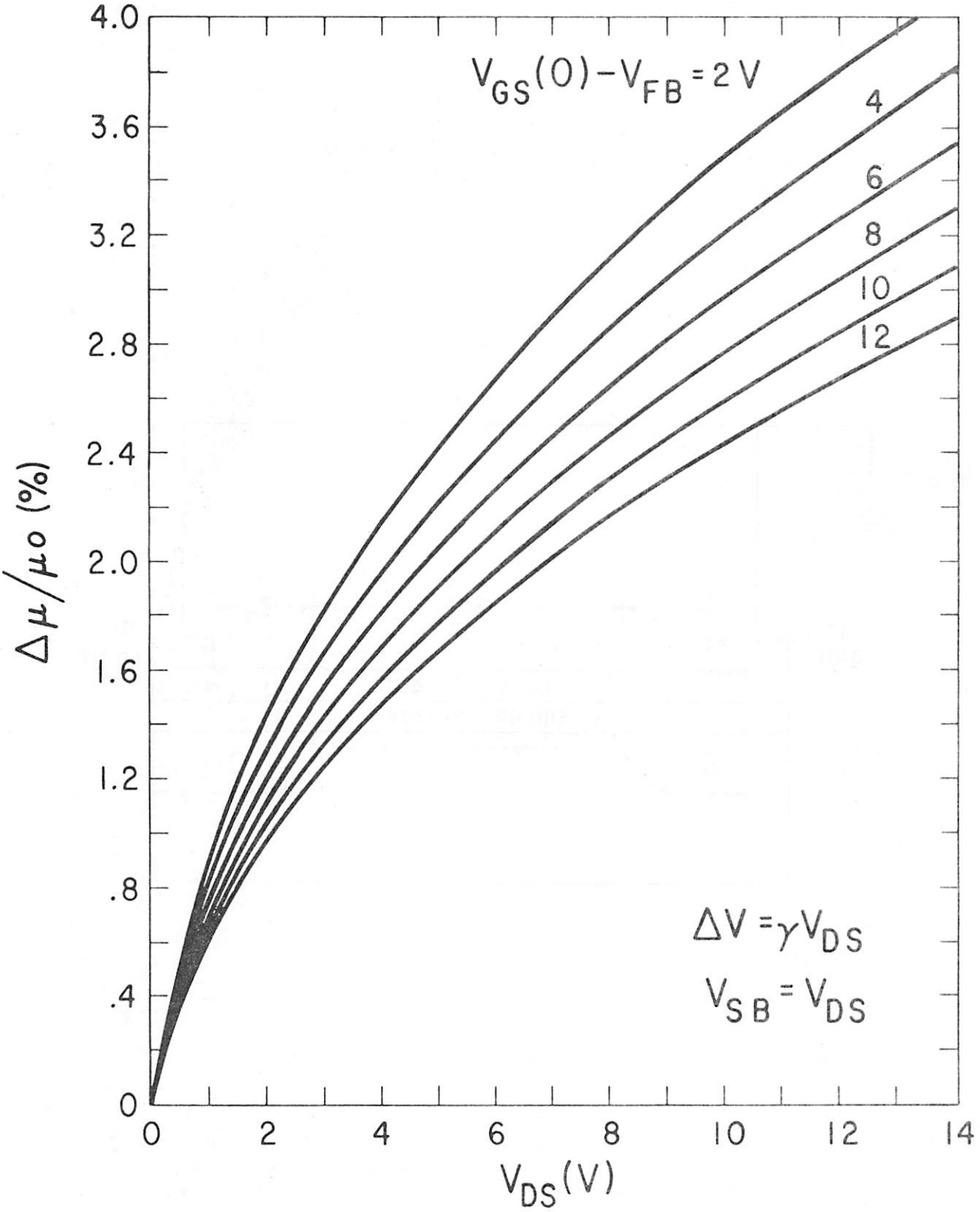

1.2
1.0
0.8
0.5
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1.0
Normalized charge [Qn(y)/Qn(0)]
Normalized position (y/L)
ΔV = 0 V
ΔV = 2.95
VDS = VSB = 2.58 volts
VGS(0) = 5.16 volts

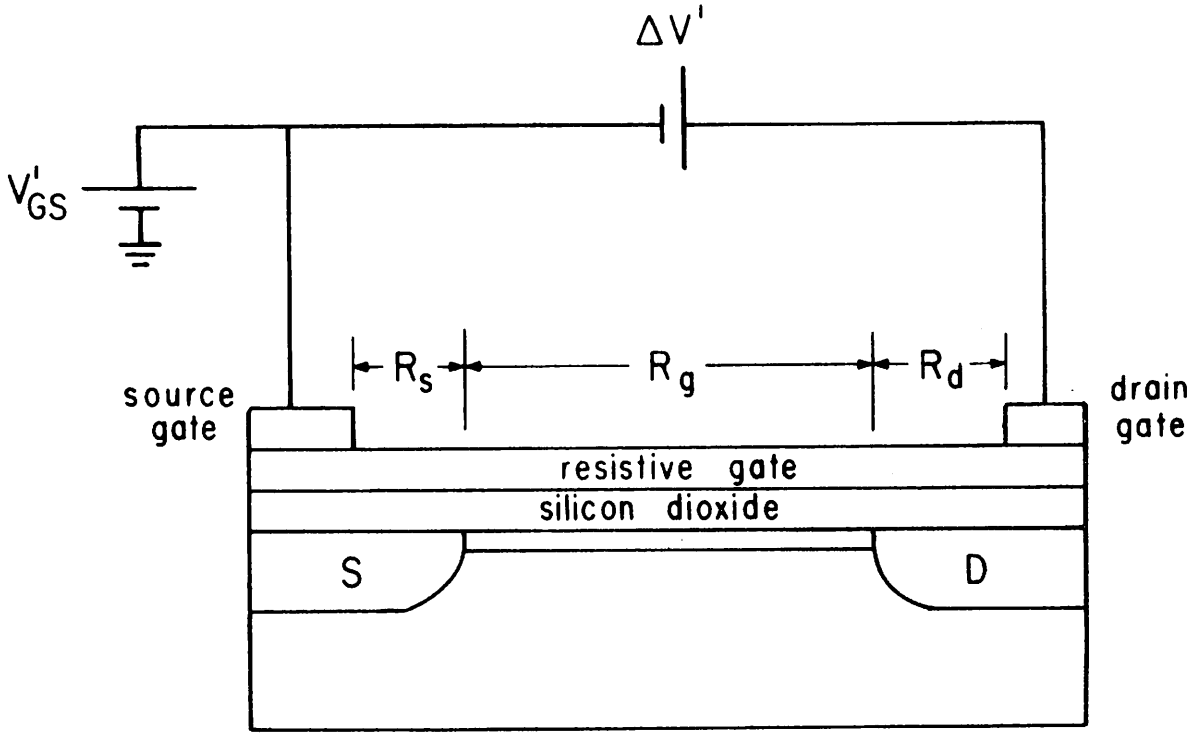

1.2
1.0
0.8
0.6
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1.0
Normalized field $[\mathcal{E}_x(y)/\mathcal{E}_x(0)]$
Normalized position (y/L)
ΔV = 0 volts
ΔV = 2.95 volts
uniform channel

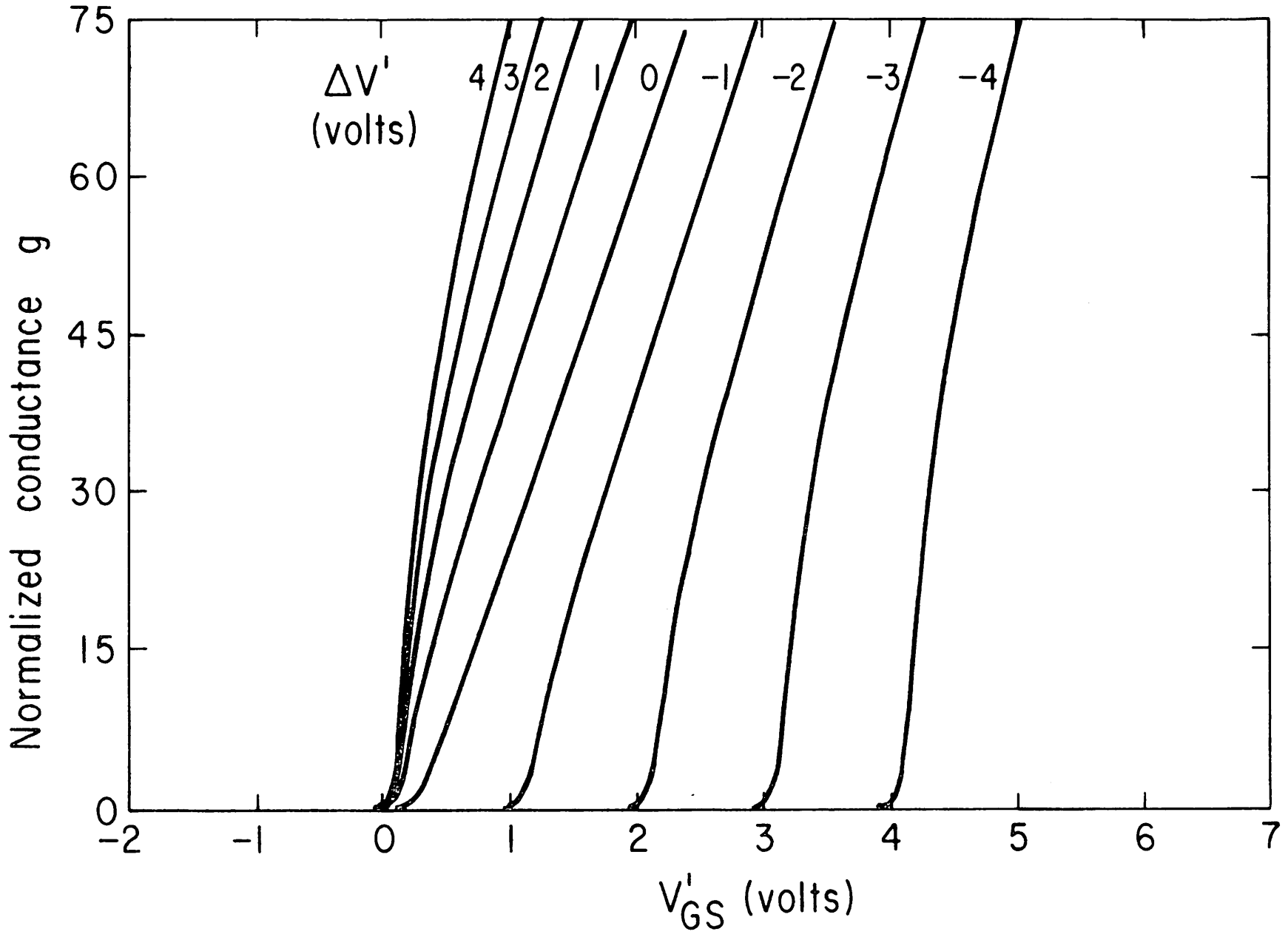

3.0
2.5
2.0
1.5
1.0
0.5
0
0
0.2
0.4
0.6
0.8
1.0
Δ ΔV = 0 volts
□ ΔV = 2.95 volts
Normalized field [ε_y/(V_DS/L)]
Normalized position (y/L)

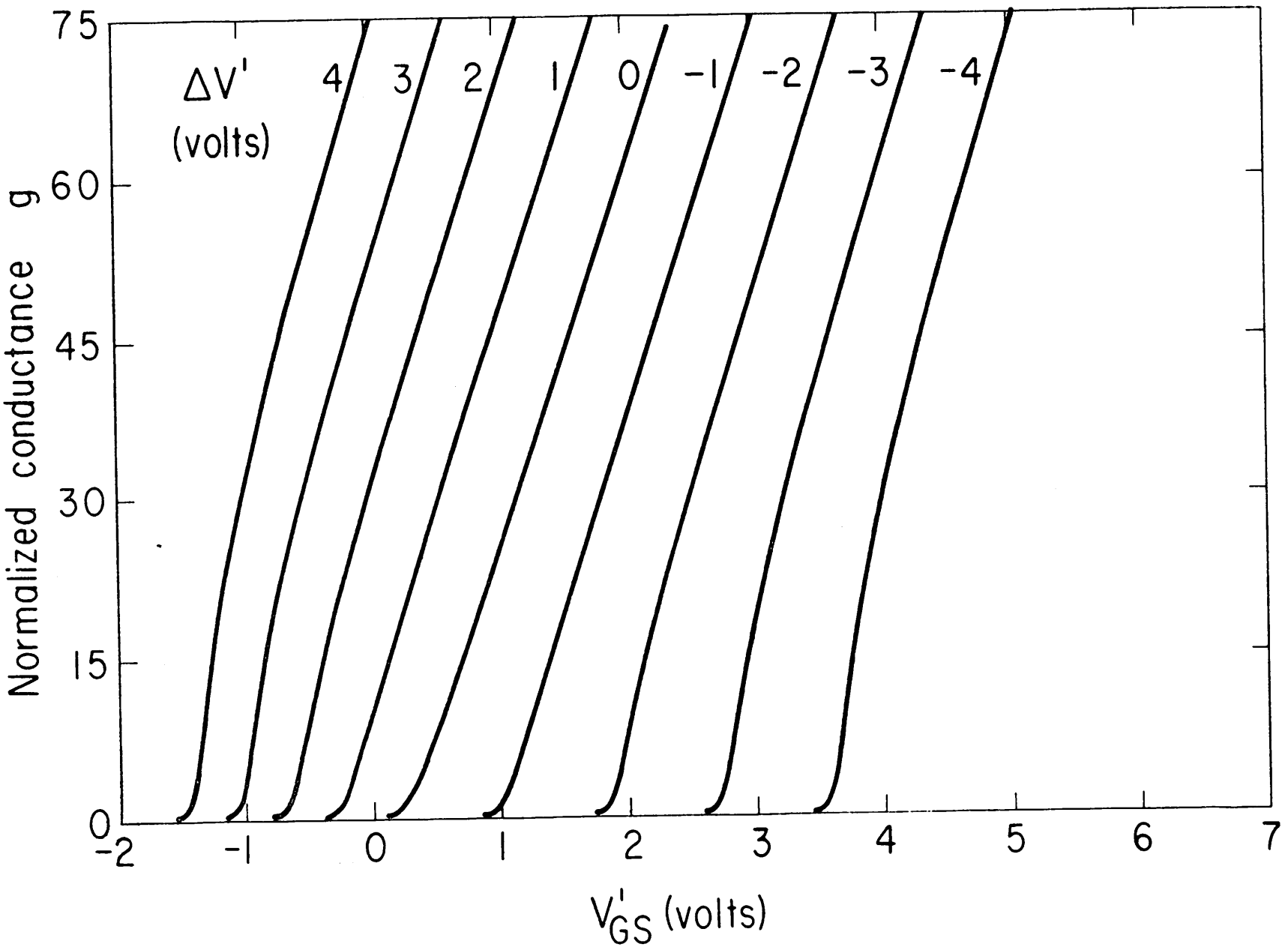

$\frac{Q_n(y)}{Q_n(0)}$
1.2
1.0
0.8
(a)
$\frac{\mathcal{E}_x(y)}{\mathcal{E}_x(0)}$
1.2
1.0
0.8
(b)
$\frac{\mathcal{E}_y(y)}{V_{DS}/L}$
1.5
1.0
0.5
0
0.2
0.4
0.6
0.8
1.0
y/L
(c)

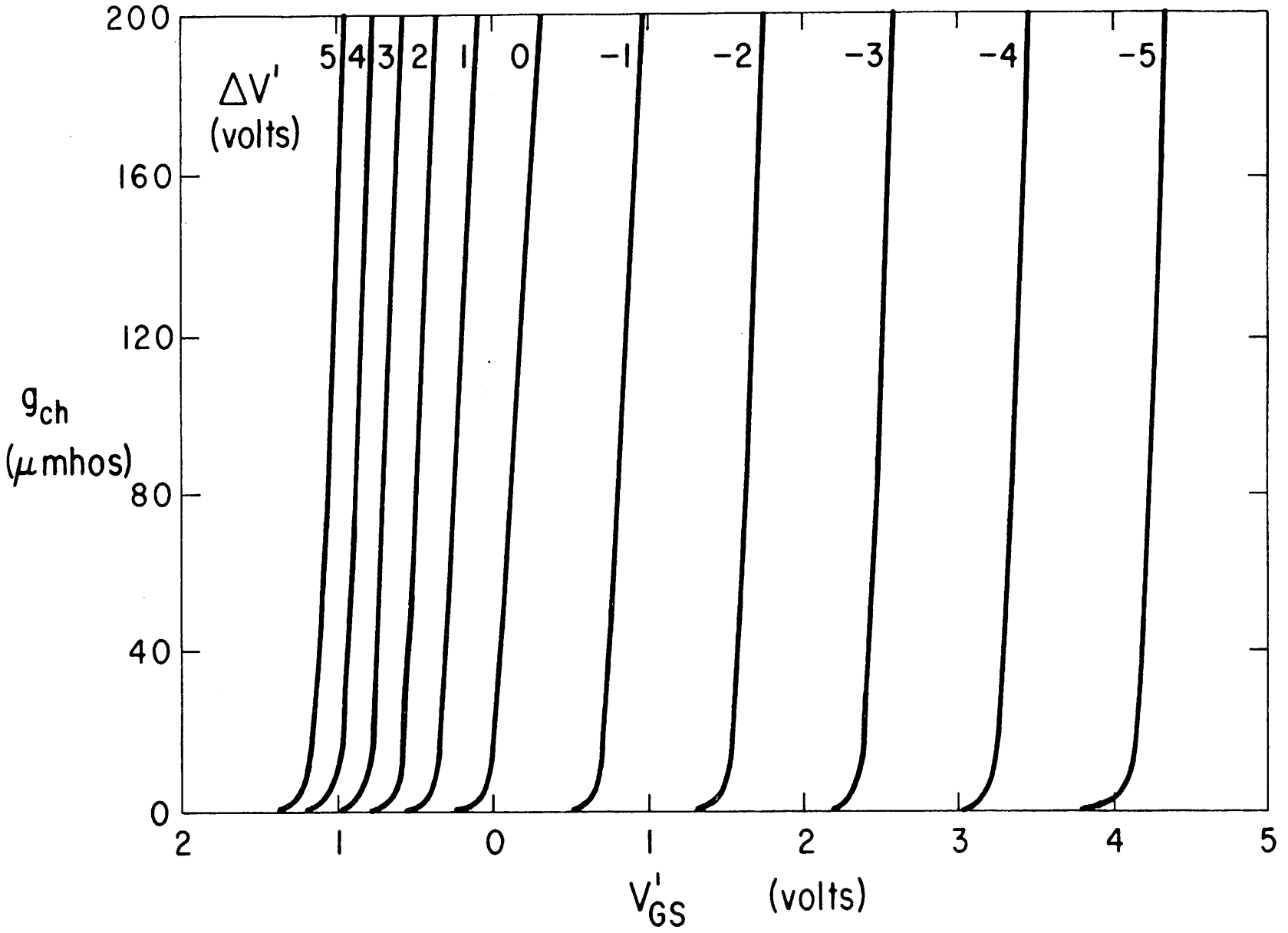

40
30
20
10
0
0
2
4
6
8
10
12
14
$V_{GS}(0) - V_{FB} = 2V$
4
6
8
10
12
$\Delta V = \gamma V_{DS}$
$V_{SB} = V_{DS}$
$\Delta \mathcal{E}_x / \mathcal{E}_x(0)$ (%)
V_{DS} (V)

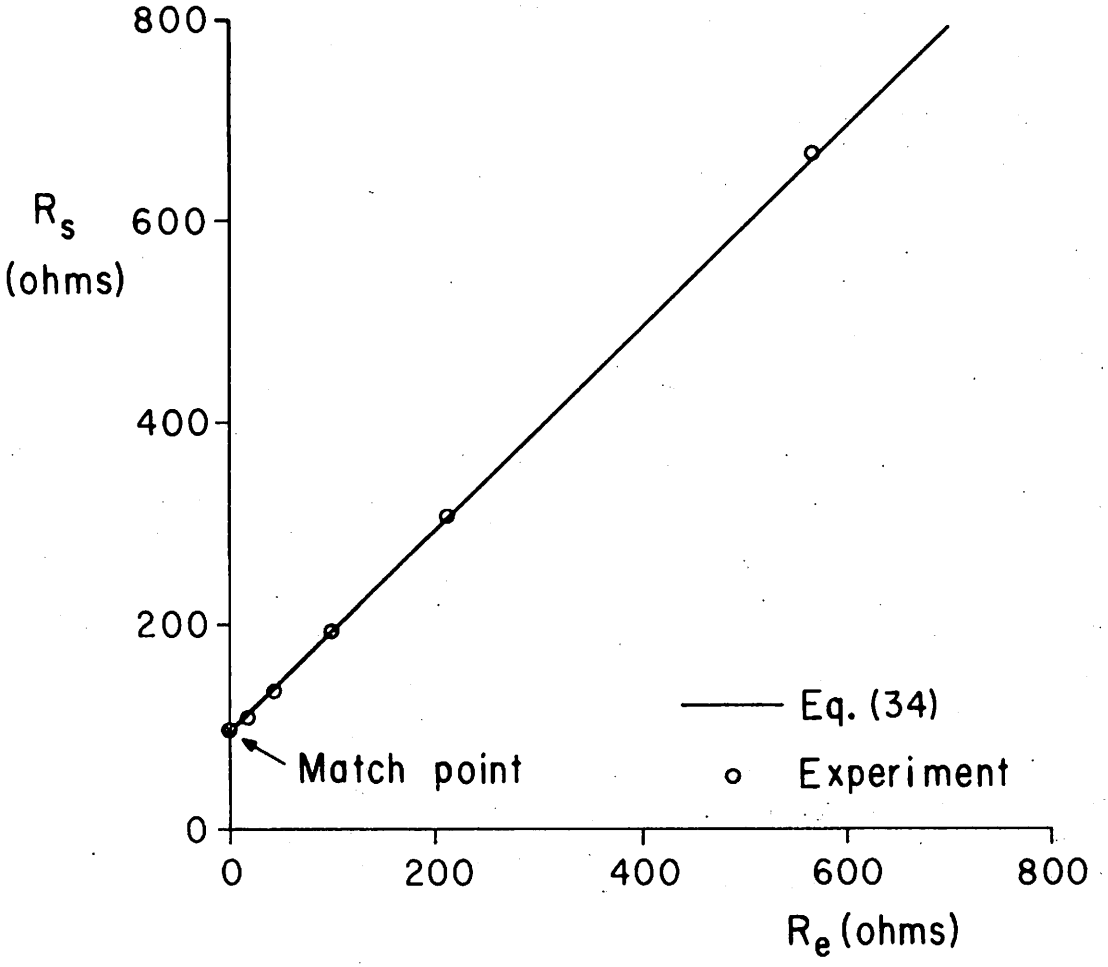

$V_{GS}(0)-V_{FB}=2V$
4
6
8
10
12
$\Delta V=\gamma V_{DS}$
$V_{SB}=V_{DS}$
$\Delta\mu/\mu o$ (%)
V_{DS}(V)
0
.4
.8
1.2
1.6
2.0
2.4
2.8
3.2
3.6
4.0
0
2
4
6
8
10
12
14


ΔV'
V'GS
Rs
Rg
Rd
source gate
drain gate
resistive gate
silicon dioxide
S
D


75
60
45
30
15
0
Normalized conductance g
ΔV'
(volts)
4
3
2
1
0
-1
-2
-3
-4
-2
-1
0
1
2
3
4
5
6
7
V'GS (volts)


75
60
45
30
15
0
Normalized conductance g
ΔV'
(volts)
4
3
2
1
0
-1
-2
-3
-4
-2
-1
0
1
2
3
4
5
6
7
V'GS (volts)


200
160
120
80
40
0
g_{ch}
(μmhos)
$\Delta V'$
(volts)
5
4
3
2
1
0
-1
-2
-3
-4
-5
2
1
0
1
2
3
4
5
V'_{GS} (volts)


800
600
400
200
0
R_s (ohms)
0
200
400
600
800
R_e (ohms)
Eq. (34)
Experiment
Match point