CHARACTERIZATION AND MEASUREMENT OF 1/f NOISE IN MOS-LSI NMOS DEVICES

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And lastly, I wish to thank my wife, Li-ming, who put up with more than anyone could reasonably expect.

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Contents

Abstract

Equivalent gate-noise voltages of LSI-MOS transistors have been measured at a frequency of 1KHZ, bandwidth 10HZ and drain-source bias 3.10V. Experimental results of the bias dependence of noise have been presented and carefully examined in cognizance with various noise theories and BDM noise model.

Symbols

$\overline{i_{dF}^2}$	mean-squared drain current due to 1/f noise
Δf	bandwidth
i_o	the height of the current pulse due to a single current carrier
W	channel width between the drain and source
L	channel length between the drain and source
f	sinusoidal frequency
q	electronic charge
I_{DS}	drain bias current
Q_{CH}	total inversion-layer channel charge
μ_{ss}	mobility in the surface-state band
μ_s	effective surface-carrier mobility
V_{GS}	gate-source bias voltage
V_G	effective gate bias voltage
N_{ss}	surface-state density (cm^{-2}/ev)
$\bar{N}_{ss}$	effective surface density (cm^{-2})
C_{ox}	oxide layer capacitance per unit area
$\overline{v_{gF}^2}$	mean-squared equivalent gate 1/f noise
$\overline{\delta i_{dF}^2}$	mean-squared drain current fluctuation
$\overline{\delta_N^2}$	mean-squared carrier density fluctuation
d_t	oxide thickness containing a uniform density of traps
α	a factor which determines the probability of tunneling
$\bar{\alpha}$	surface-state efficiency
K	Boltzmann's constant
T	absolute temperature

A. Introduction

The wide range of the process time constants of the trapping of current carriers involving the surface states at oxide-silicon interfaces makes the noise spectrum inverse proportional to frequency. Although analyses of 1/f noises have been carried out by many investigators, they are all based on the concept of the trapping of free carriers in silicon semiconductor [9].

The MOS drain-noise current arises from fluctuations of the drain current [9], either due to a change in the number of free carriers or due to a change in the number of trapped carriers. Based on the former process, some investigators [7], [8] indicate that the quivalent noise voltage is dependent both on gate-bias and surface-state density. An interpretation, assuming a direct gate-bias dependence of the equivalent noise voltage besides its proportional dependence on the surface-state density, has been made by Klaassen [8]. Based on the latter cause, most investigators [2]-[6] indicate that the equivalent gate-input noise voltage is dependent on the surface-state density, but not on the gate bias. Because of the interdependence among gate bias, quasi-Fermi level and surface-state density, it is difficult to draw a conclusion of the actual energetic distribution of the surface-state density from experimental results by a direct comparison with the two theoretical results.

The BDM current noise equation utilized in SPICE2 circuit analysis is a simple function of drain bias current with chosen noise constants and predefined process parameters. BDM current noise equation poorly represents the true nature of surface-state density within bandgap, and hence that of noise.

B. Theoretical Background

Based on the concept of random trapping of free carriers in surface states, theoretical calculations of drain noise current led to different results due to difference in nature of assumptions. Among these, five different results are identified and compared [1].

Theory 1: This theory is due to the work of Leventhal [2]. He proposed that the channel inversion layer free carriers are in motion in surface-state-band with a reduced mobility and that there is a wide range of time constant involved in the capture and generation of carriers obeying Shockley-Reed-Hall (SRH) statistics. Using Fourier transform theory and considering random current pulses arising due to carrier motion in the assumed surface band, Leventhal performed noise spectrum calculation and obtained the following mean-squared drain-noise current for the triode region of the I_{DS}-V characteristics.

$$\frac{\overline{i^2}_{dF}}{\Delta f} = \frac{i_o^2 \ \bar{N}_{ss} \ W \ L}{f} \qquad (1)$$

where i_o is the height of the current pulse due to a single current carrier. i_o is related to the total inversion-layer channel charge, Q_{CH}, and drain bias current, I_{DS}, by the following equation:

$$i_o = \frac{qI_{DS}}{Q_{CH}} \ \frac{\mu_{ss}}{\mu_s} \qquad (2)$$

By inserting appropriate expressions for I_{DS} and Q_{CH}, it can be shown assuming negligible substrate doping effects, that

$$\frac{\overline{i_{dF}^2}}{\Delta f} = \left(\frac{\mu_{ss}}{\mu_s}\right)^2 \left(\frac{I_{Ds}}{V_G}\right)^2 \frac{q^2\bar{N}_{ss}}{C_{ox}^2\, fWL} \left(\frac{3}{2} \frac{\theta}{1-(1-\theta)3/2}\right)^2 \quad (3)$$

where $\theta = \dfrac{2I_{DS}}{BV_G^2}$ and $B = \dfrac{W}{L} \cdot C_{ox}\mu_s$

The equivalent mean-squared gate noise voltage, $\overline{v_{gF/\Delta f}^2}$, in the drain bias current saturation region is given by dividing equation (3) by $g_m^2 = 2I_{DS}/V_G$ i.e.,

$$\left.\frac{\overline{v_{gf}^2}}{\Delta f}\right|_{sat} = \frac{9}{16} \left(\frac{\mu_{ss}}{\mu_s}\right)^2 \frac{q^2\bar{N}_{ss}}{C_{ox}^2\, fWL} \left(\frac{1+\lambda V_{DS}}{1+\frac{3}{2}\lambda V_{DS}}\right)^2 \quad (3)'$$

where λ is the channel length modulation parameter. In current saturation, $\overline{v_{gF}^2}/\Delta f$ becomes independent of gate bias provided N_{ss} is uniformly distributed across the semiconductor band gap. When N_{ss} is nonuniformly distributed, the variation of $\overline{v_{gf}^2}/\Delta f$ with V_{DS} will depend on the details of nonuniformity. When an increase in the gate bias voltage and the movement of quasi-Fermi level does not involve any change in the magnitude of N_{ss}, the value of $\overline{v_{gf}^2}/\Delta f$ is constant in current saturation region. $\overline{v_{gf}^2}/\Delta f$ can either increase or decrease with V_G, depending upon whether N_{ss} distribution has a peak near the edge of the bandgap or near the center of the gap as column (B), (C) in fig. 1 [1].

Theory 2: This theory is due to the work of Christenson et al. [3], who calculated the low frequency noise voltage spectrum for a MOS transistor under the assumption that the time constant dispersion, giving a 1/f spectrum, is caused by tunneling of carriers at the silicon-silicon oxide interface to traps located inside the oxide. The frequency spectrum of the mean squared fluctuations in the number of trapped carriers is determined by charge time constant which is related to a discrete trap level within semiconductor band gap. Based on SRH statistics, the calculations relate the mean squared drain current fluctuation, $\overline{(\delta i_{dF})^2}$, to the mean squared free-carrier density fluctuation, $\overline{(\delta N)^2}$, by the following equation:

$$\overline{(\delta i_{dF})^2} = \frac{qI_{DS}}{WLQ(x)} \cdot \overline{(\delta N)^2} \qquad (4)$$

where Q(x) is the channel mobile charge per unit area at point x. The equivalent overall gate-noise voltage spectrum is obtained by integration, in order to include the trap energy distribution and trap density distribution within the oxide layer. Consider the simplest case that the effectively uniform trap energy levels are within $\pm$ 2KT range of the free carrier quasi-Fermi level, which contributes most effectively in the generation of noise. This simple case leads to the following expression:

$$\frac{\overline{i_{dF}^2}}{\Delta f} = \frac{\bar{N}_{ss}}{(d_t \alpha)} \frac{WL}{f} \left(\frac{qI_{DS}}{Q_{CH}} \right)^2 \qquad (5)$$

where $\bar{N}_{ss} = 4KTN_{ss}$ is defined as an effective surface-state density, and d_t is the oxide thickness containing a uniform density of traps, and α is a factor which determines the probability of tunneling. Equation (1) is identical to (5) provided

$$\left(\frac{\mu_{ss}}{\mu_s}\right)^2 = \frac{1}{d_t\alpha} \qquad (6)$$

Leventhal cited $\frac{\mu_{ss}}{\mu_s} = \frac{1}{7}$ and Christensson et al. cited $d_t\alpha = 40$. Jntroduced the effects of oxide field on the probability of tunneling [4], the form of drain-noise current spectrum remains essentially the same as that of equation (5) and the bias dependence of the noise voltage spectrum is also similar to that of theory 1.

Theory 3: This theory is due to the work of Hsu [5], who assumed that the random occupancy of surface states modulates the surface potential, causing fluctuation of channel charge and, hence, the fluctuation of drain current. This leads to the following equation:

$$\frac{\overline{i_{df}^2}}{\Delta f} = \frac{q^2 g_m^2}{C_{ox}^2 WL} \cdot \frac{\bar{N}_{ss}}{f(d_t\alpha)} \qquad (7)$$

for both triode and saturation drain current. In triode region, the result of (7) becomes identical to that of (5). In saturation region, there is some difference between the results. The bias dependence of the equivalent gate noise

voltage, according to (7), is primarily due to the variation of N_{ss} within the band gap, as in fig. 1 [1].

Theory 4: This theory is due to the work of Fu and Sah [6], who suggested that the charge fluctuation in oxide traps arises from carrier tunneling between the fast interface surface states and the oxide trap states. They also suggested a second fluctuation, at higher frequency, arises from the random thermal emission and capture of electrons and holes at the fast interface state through the thermal or SRH process. This provides a separate time constant for tunneling, in addition to the time constant in SRH thermal process. The tunneling process in theories 2 and 3 is absorbed into the SRH thermal capture coefficient.

The calculation of drain-noise current spectrum based on the concept of induced charge fluctuation in conducting channel due to the mechanism of carrier tunneling via the intermediate states is given for triode drain current. The results agrees with that of equation (7).

Theory 5: This is due to the work by F. Berz [7] and F.M. Klaassen [8]. As the low frequency noise spectrum and its bias dependence are concerned, theory 1, 2, 3 and 4 give more or less the same results.

Based on the assumptions originally introduced by McWhorter [9], Berz and Klaassen worked out a different theory. They regard the basic cause of noise to be the fluctuation in the

occupancy of traps, which modulates the channel conductivity and hence drain current. The tunneling model for carrier trapping and a wide range of time constant values are also valid in theory 5.

Klaassen obtained the following equation for triode bias current:

$$\frac{\overline{i_{dF}^2}}{\Delta f} = \frac{q\mu_s \bar{\alpha}}{L^2} \quad \frac{I_{DS}V_{DS}}{f} \tag{8}$$

where $\bar{\alpha}$ is the surface state efficiency. The major difference of the results obtained by both Berz and Klaassen is that the magnitude of mean-square drain-noise current in triode region is proportional to the power dissipation in the channel, namely, $I_{DS}V_{DS}$. Diving (8) by g_m^2, it gives an equation for mean-square gate noise voltage in triode region:

$$\frac{\overline{v_{gF}^2}}{\Delta f} = \frac{q\bar{\alpha}}{WLC_{ox}} \quad \frac{1}{f} \quad (V_G - \tfrac{1}{2}V_{DS}) \tag{9}$$

In saturation region, V_{DS} is replaced by V_G, and the mean squared gate-noise voltage becomes linearly dependent on V_G. This result is quite different from previous theories 1, 2, 3, and 4. Devices tested by Klaassen had low surface-state density and a uniform distribution of the same within the band gap of silicon. This is contradictory to the conclusion in theory 3 by Hsu in his interpretation of the variation of gate-noise voltage with the effective gate bias. In the light

of results of other theories, it is possible to draw the conclusion that N_{ss} in the devices tested by Klaassen is also nonuniform within the band gap.

C. BDM Model

The 1/f noise model used in conjunction with ac analysis portion of SPICE2 is described in SPICE2 MOS Modeling Handbook by D.R. Alexander et al. of BDM Corporation [10]. The mean-squared current noise, $\overline{i_{dF}^2}/\Delta f$, cited by them is as follows:

$$\frac{\overline{i_{dF}^2}}{\Delta f} = \frac{KF \cdot I_{DS}^{Af}}{fC_{ox}WL_o} = \frac{KF \cdot I_{DS}^{AF}}{fC_{ox}W(L_M - 2L_D X_J)} \qquad (10)$$

where

L_o = Effective channel length

L_M = Mask defined channel length

L_D = Lateral diffusion constant

X_J = Metallurgical junction depth

AF = Flicker noise exponent, typical value = 1.2

KF = Flicker noise coefficient, typical value = 10^{-26}

In the drain current saturation region, as most of the test devices performed, the mean-squared noise voltage referred to the gate is given by:

$$\frac{\overline{v_{gF}^2}}{\Delta f} = \frac{KF\left[\frac{B}{2}(1+\lambda V_{DS})\right]^{AF}}{fC_{ox}WL_o} V_G^{2AF} \qquad (11)$$

where $B = \mu C_{ox}(\frac{W}{L_o})$

Noise voltage of BDM equation (11) is a direct and some power dependence of gate bias, V_G, which is the only device

characteristic variable in BDM noise equation for a given device at some drain-source bias. Surface-state density, N_{ss}, of theory 1 and surface-state efficiency, $\bar{\alpha}$, of theory 5 are also a direct and power dependence of gate bias if mean-squared noise voltages of theory 1 and theory 5 are described separately by BDM noise equation in drain bias saturation. These physical mechanisms seem to be unlikely. The BDM noise equation is only useful mathematically for fitting curves to experimentally measured noise data; by itself, BDM noise equation cannot be used to predict noise behaviors of MOS devices properly.

D. Experimental Results

The NMOS devices used in this project are Intel I0-167 chips. There are three ENMOS devices and one DNMOS device in a single IO-167 chip. Channel wideth, W, and channel length, L, together with layers of poly-silicon are shown in Table 2.

Noise measurement of three I0-167 chips were performed at bandwidth, Δf, 10HZ, frequency, f, 1KHZ, and drain-source bias V_{DS} , 3.10V. Curves of mean-squared noise voltage per unit bandwidth versus drain bias currents of chip 11, 13 and 21 are shown in fig. 8a, 8b, 9 and 10. Curves of mean-squared noise voltage per unit bandwidth versus effective gate bias voltage of chip 11 are shown in fig. 8b.

Fig. 8a, 8b, 9 and 10 show the variation of $\overline{v_{gF}^2}/\Delta f$ with drain bais currents for twelve devices of four types. These curves also show the possibility of either increasing or decreasing N_{ss} with the movement of electron quasi-Fermi level toward the conduction band edge for a given type device. A moderate variation in N_{ss} with I_{DS} is obvious in the cases of devices ENMOS's at poly layer one and poly layer 2 both with W/L=100/7. A larger variation of N_{ss} with drain bias currents is seen to occur in the DNMOS's at poly layer 2 with W/L=100/8. The maximum and minimum values of $\overline{v_{gF}^2}/\Delta f$, for different types of devices in the same chip, and for corresponding types of devices in different chips, occur at different values of I_D.

E. Comparison of Experiment with Theories and with BDM Model

a. Comparison of Experiment with Theories

The moderate variation of $\overline{v_{gF}^2}/\Delta f$ of ENMOS's with W/L=100/7 both at poly layer 1 and at poly layer 2 in fig. 8-10 indicates the dependence of $\overline{v_{gF}^2}/\Delta f$ on the drain bias current, and consequently on the gate-bias voltage, is not strong in these two types of devices. This behavior does not necessarily imply that the surface-state density, N_{ss}, is nearly uniformly distributed across the silicon bandgap, nor does it conclusively prove that the product, $V_G N_{ss}$, in ENMOS with W/L=100/7 remains nearly constant with the variation of the gate-bias voltage V_G. Based on theories 1-4, $\overline{v_{gF}^2}/\Delta f$ of ENMOS with W/L=100/7 at both poly layer 1 and 2 in fig. 8-10 indicates that N_{ss}, within the bandgap, varies moderately. If based on theory 5, however, $\overline{v_{gF}^2}/\Delta f$ tends to indicate $V_G N_{ss}$ maintains almost a constant value.

On the other hand, the variation of $\overline{v_{gF}^2}/\Delta f$ of DNMOS with W/L=100/8 at poly layer 2 is not moderate. Its increasing or decreasing with drain bias current indicates that $\overline{v_{gF}^2}/\Delta f$ cannot be a direct function of drain saturation current, and hence, gate bias voltage. Based on theories 1-4, N_{ss} of DNMOS with W/L=100/8 at poly layer 2 appears to increase or decrease proportionately to gate bias. Based on theory 5, however, N_{ss} would appear to be nearly constant.

The conclusions to the experimental data depend very much on the theory that one uses to interpret them. Measurements

by Fu and Sah support the theory that the equivalent gate-noise voltage is directly proportional to N_{ss}[6]. They also verified their result by the noise data with the low frequency capacitance-voltage plots on the same devices. The drain-noise current, $\overline{i_{dF}^2}/\Delta f$, is generally proportional to power dissipation in channel, i.e., $I_{DS}V_{DS}$, when operated in triode drain bias current region [11], [12]. This agrees with the analytical work of Berz [7] and Klaassen [8] towards theory 5. Das and Moore indicate that equation (3) of the conclusion of theories 1-4, can also be manipulated such that the drain-noise current, $\overline{i_{dF}^2}/\Delta f$, is proportional to power dissipation in the channel, i.e., $I_{DS}V_{DS}$ at the triode drain bias current region. In other words, equation (3) of theories 1-4 can be a unified noise-current expression, whereas equation (9) of theory 5 cannot.

In the light of the above discussion, based on the present and previously published experimental findings, it is only logical to accept the validity of analytical results of equation (3) of theories 1-4, rather than to accept equation (9) of theory 5 for NMOS 1/f noise bias dependence.

The curves of N_{ss} versus I_{DS} in fig. 11 calculated from equation (3) show nearly the same forms as those of $\overline{v_{gF}^2}/\Delta f$. Peak values of $\overline{v_{gF}^2}/\Delta f$, and hence those of N_{ss}, are not consistent of the same type device in different chips at some corresponding drain current. This is due to the irregular contribution to N_{ss} during the manufacturing process. Curves

of $\overline{v_{gF}^2}/\Delta f$ in fig. 8-10 also show that the larger value of C_{ox}, as layer poly 1, and the larger value of WL product, as ENMOS W/L=100/100 result in lower noise. These are also consistent with equation (3) of the conclusion of theories 1-4.

b. Comparison of Experiment with BDM Noise Model

Based on experimental data and BDM noise equation with typical values of AF and KF, curves of mean-squared noise voltage, $\overline{v_{gF}^2}/\Delta f$, versus bias current and versus effective gate bias voltage of chip 11 are shown in fig. 12 and fig. 8b. The order of magnitude and trend of variation based on BDM voltage noise equation (11), and hence variation of N_{ss}, are quite different from those of experimental results. From BDM model description in section C and comparison with experimental results, BDM noise equation cannot be a noise modeling equation due to its incapability to describe the true nature of noise behavior. It can only be a noise fitting equation for already known values of mean-squared noise voltage or current.

F. Conclusion

The unified expression (3) of the conclusion of theories 1-4 based on trapped-carrier density fluctuation can satisfactorily explain noise behaviors of practical devices operated in both current saturation region and triode region. For devices tested, the increasing or decreasing of mean-squared noise voltage with gate bias voltage can be attributed directly to the variation of surface-state density within semiconductor bandgap, if interpreted by the unified noise current equation (3). Present and published experimental findings lead to question the validity of theory 5 based on the concept of free carrier density fluctuation. A careful examination and comparison of the experimental data have led us to disapprove the validity of BDM noise equations (10) and (11).

H. Circuits and Tables

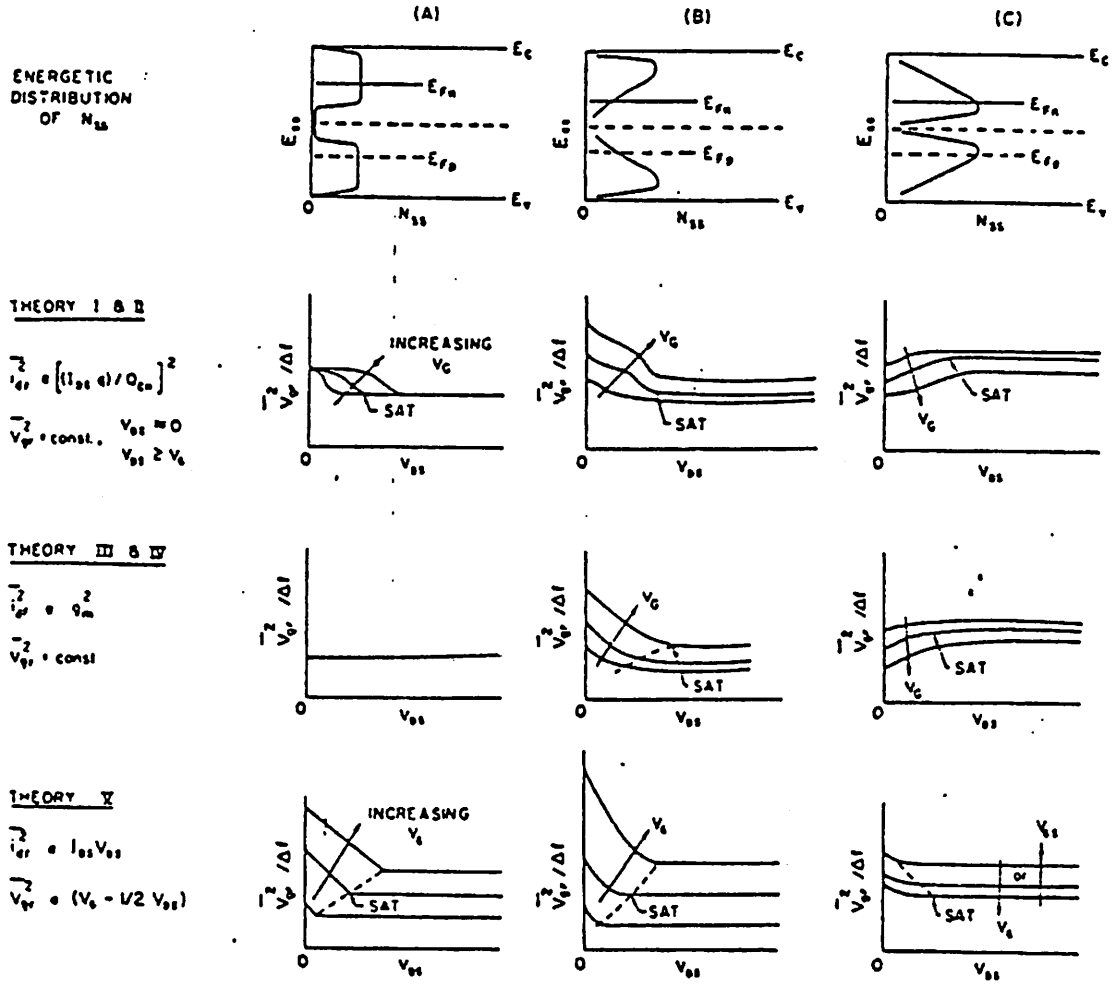

Fig.1 Qualitative representation of the variations of MOS equivalent gate-noise voltage per unit bandwidth, under three different distribution of N_{ss}, with drain voltage, assuming a constant effective gate-bias voltage [1].

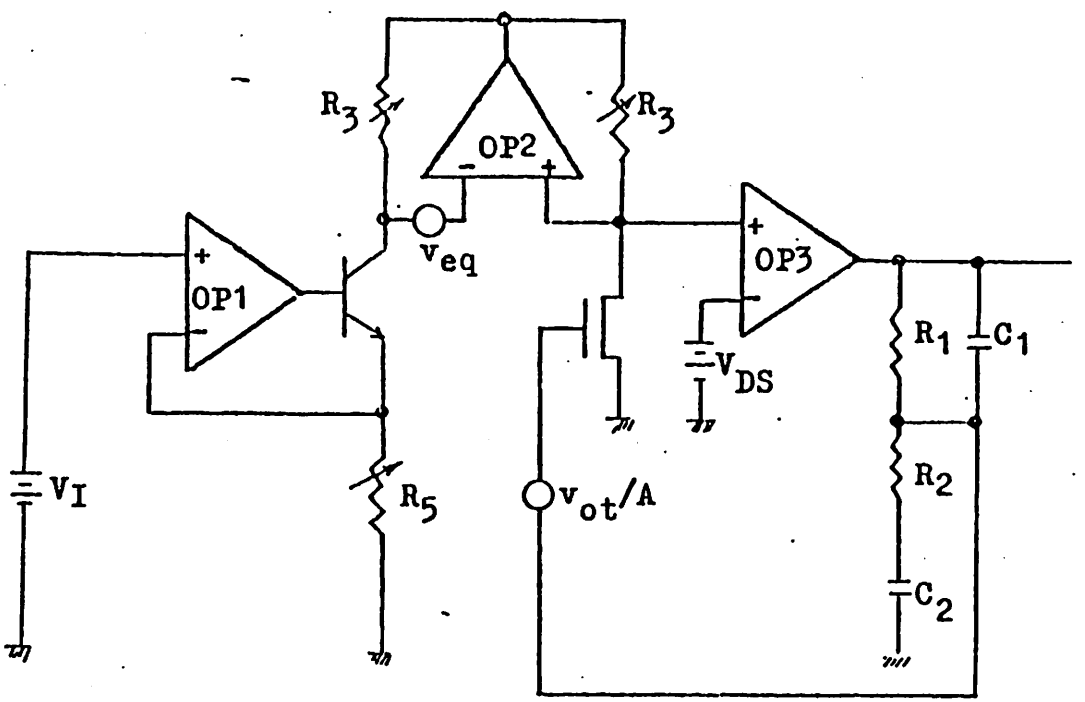

Fig.2 Noise measurement circuit with equivalent gate total noise voltage source, v_{ot}/A , and equivalent DC current-source noise voltage source, v_{eq}

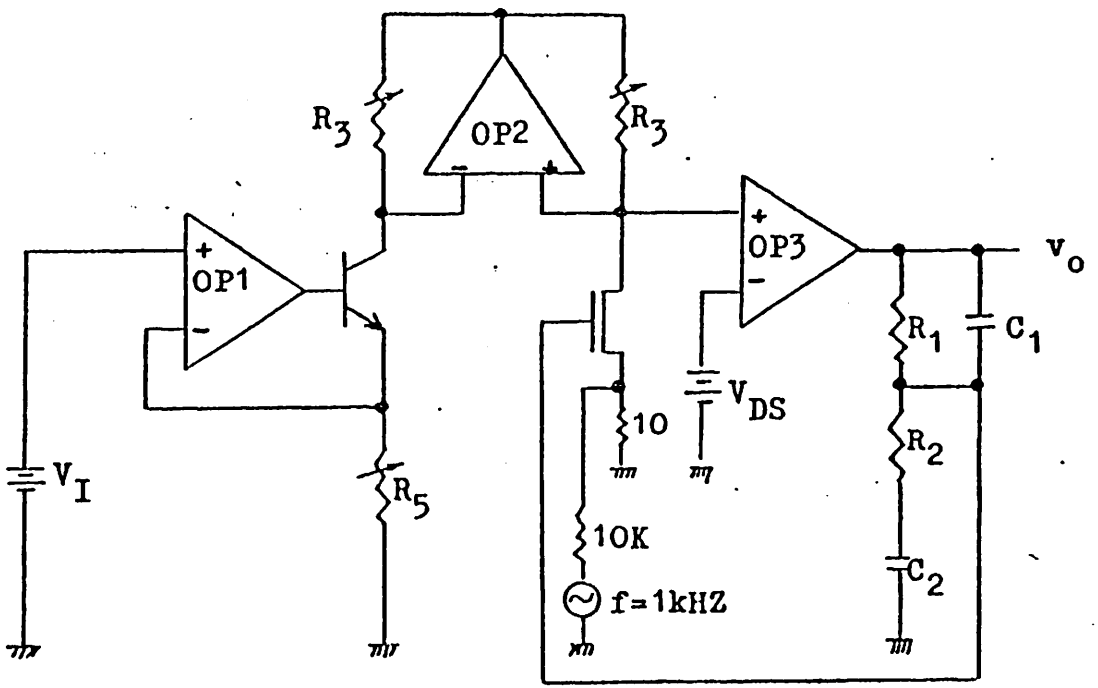

Fig.3a Circuit to measure overall small signal gain $A=v_o/v_g$

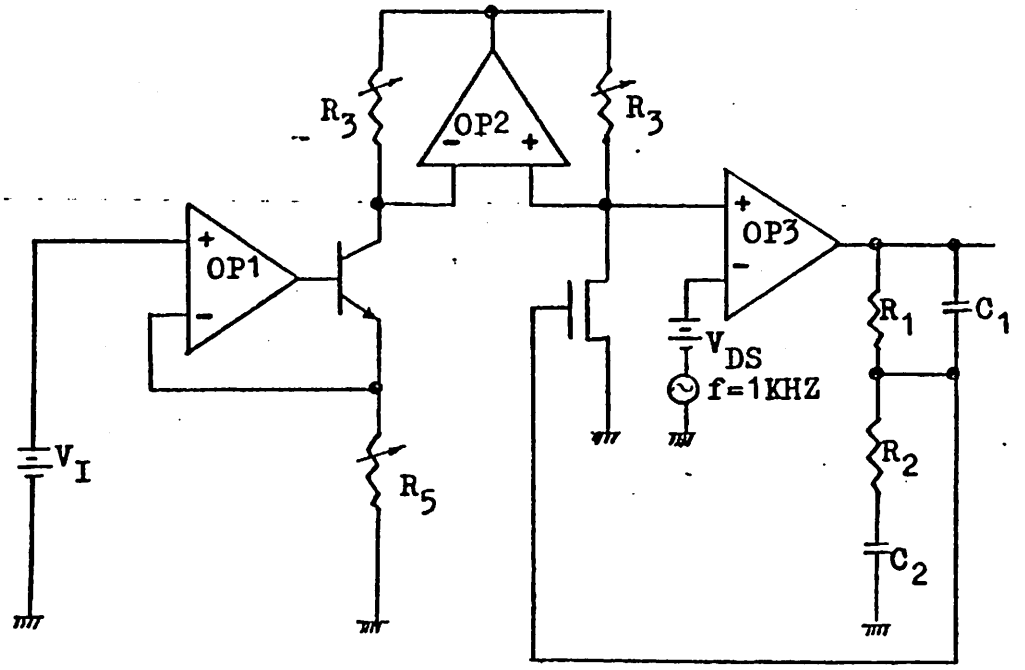

Fig. 3b Circuit to measure overall small signal gain $A=v_o/v_g$

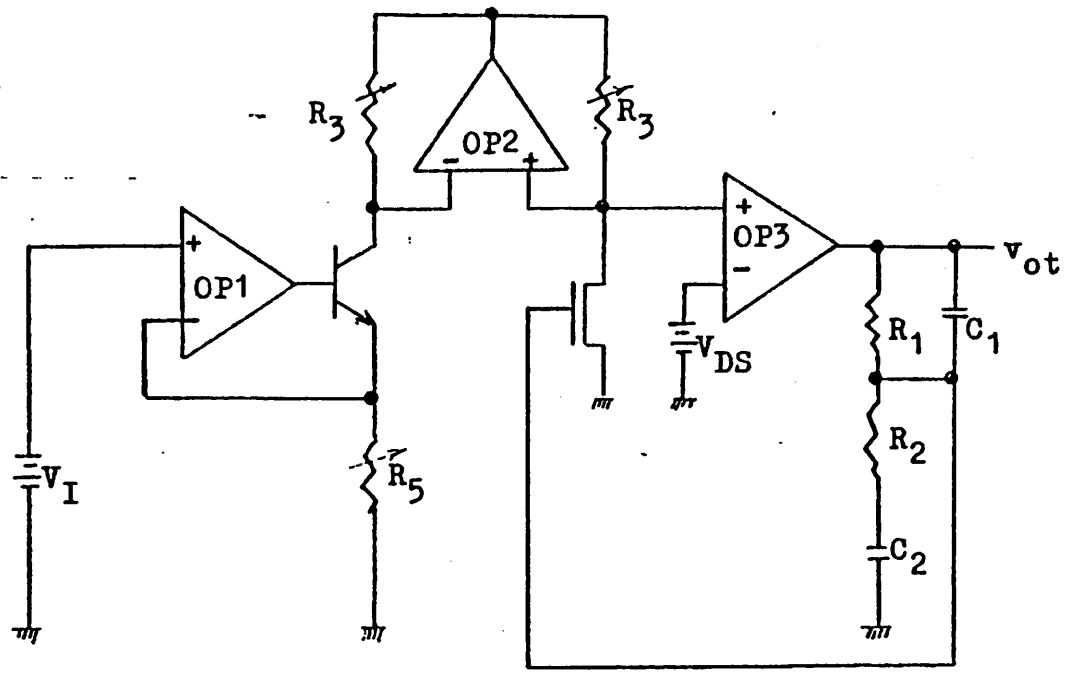

Fig.4 Circuit to measure total noise voltage at output of operational amplifier OP3

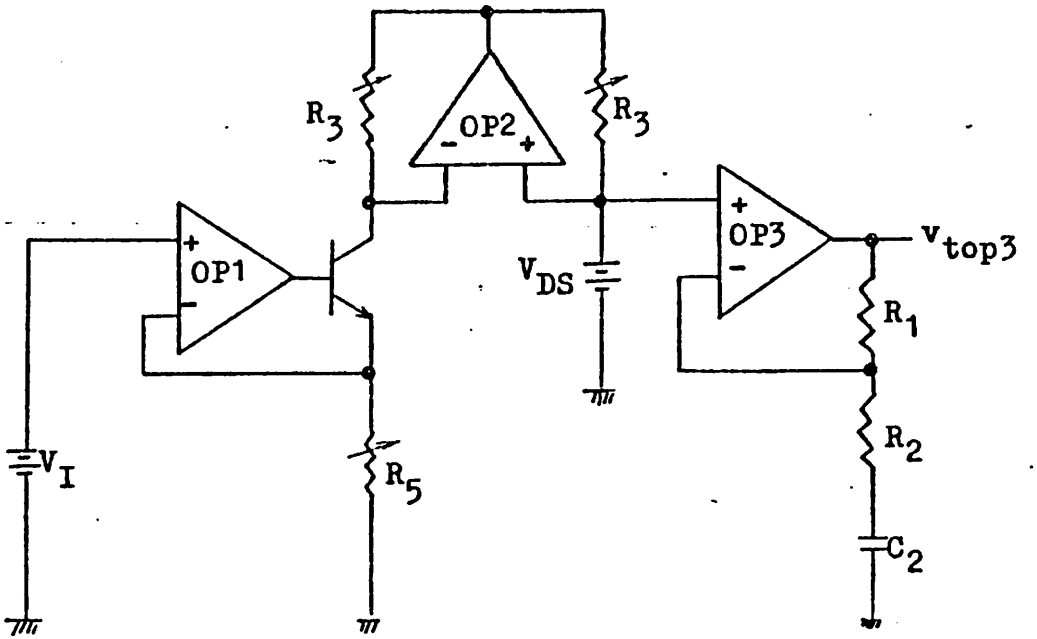

Fig.5 Circuit to measure noise voltage due to operational amplifier OP3

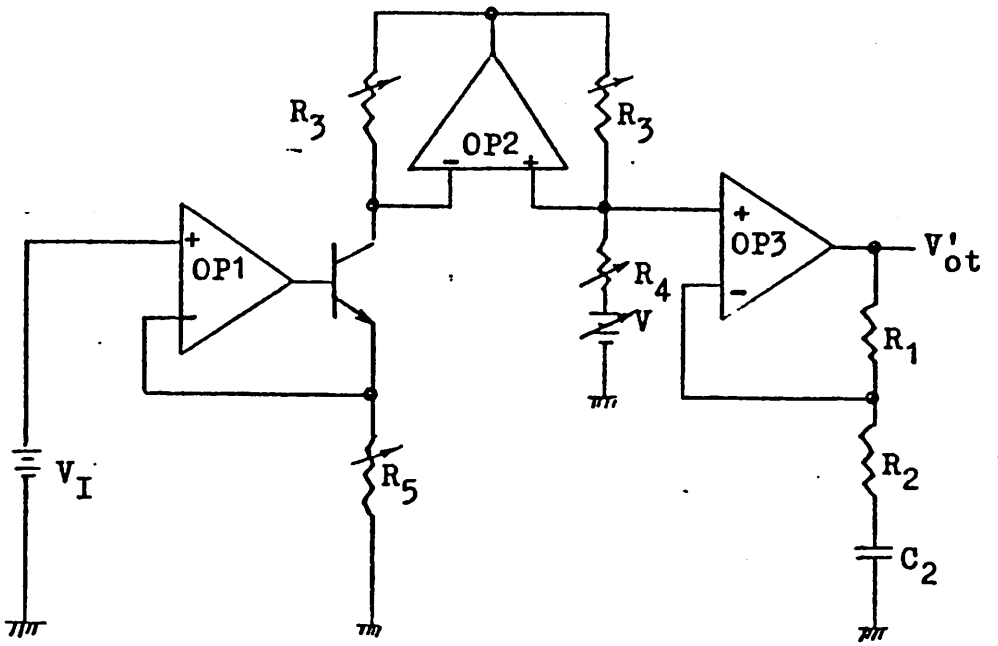

Fig.6 Circuit to measure noise voltage due to DC current-source with NMOS device removed

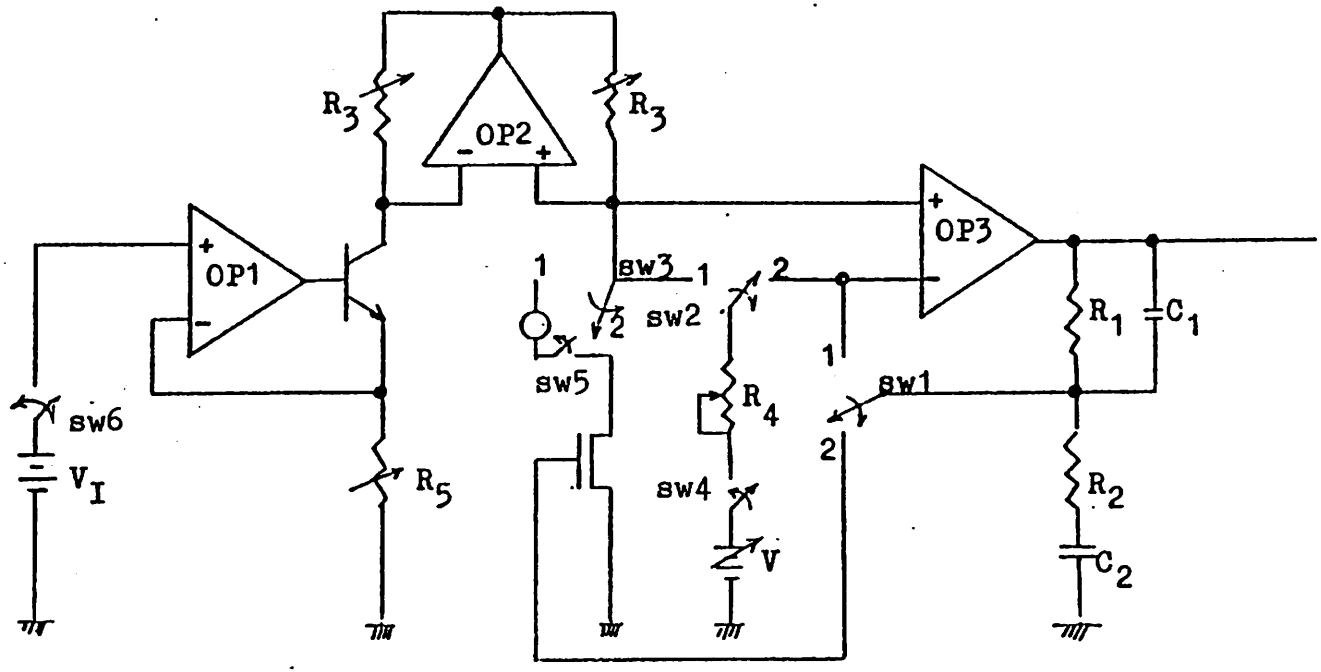

Fig.7 Actual circuit set up for bias measurement and noise measurement. Switching system is in table 1.

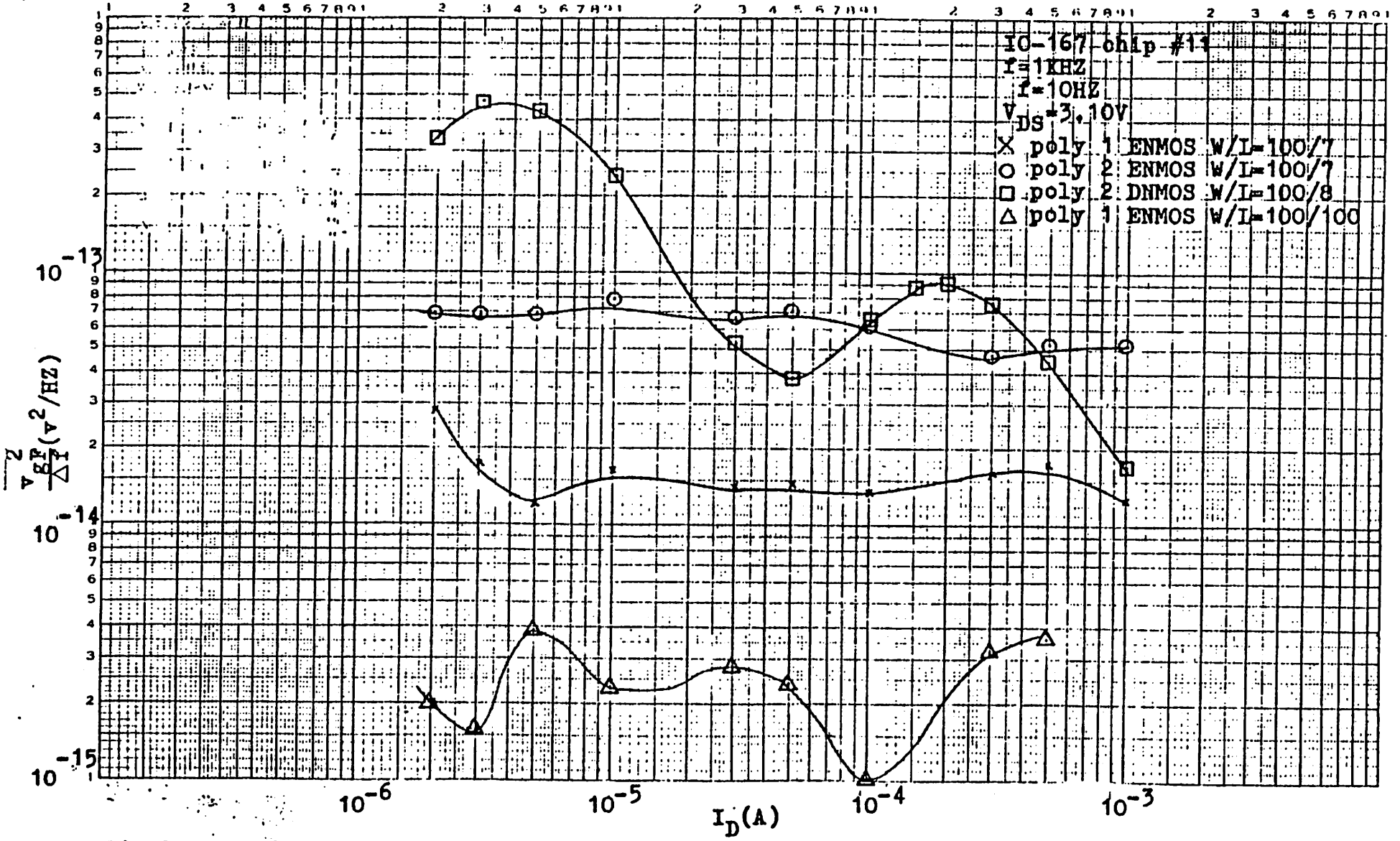

Fig.8a Experimental results on four NMOS's on the same chip showing the variation of the equivalent gate input noise voltage per unit bandwidth with drain current at 1KHZ

Fig.8b The equivalent noise voltage based on experiment and BDM noise equation as function of the applied effective gate voltage

ID-167 chip #11
f=1 KHZ
f=10HZ
V_{DS}=3.10V
x poly 1 ENMOS W/L=100/7
○ poly 2 ENMOS W/L=100/7
□ poly 2 DNMOS W/L=100/8
△ poly 1 ENMOS W/L=100/100

V_{nEP}^2 (V²/HZ)

$V_{GS}-V_T$

EMI-LOGARITHMIC 5 CYCLES X 10 TO THE INCH
5TH LINES ACCENTED

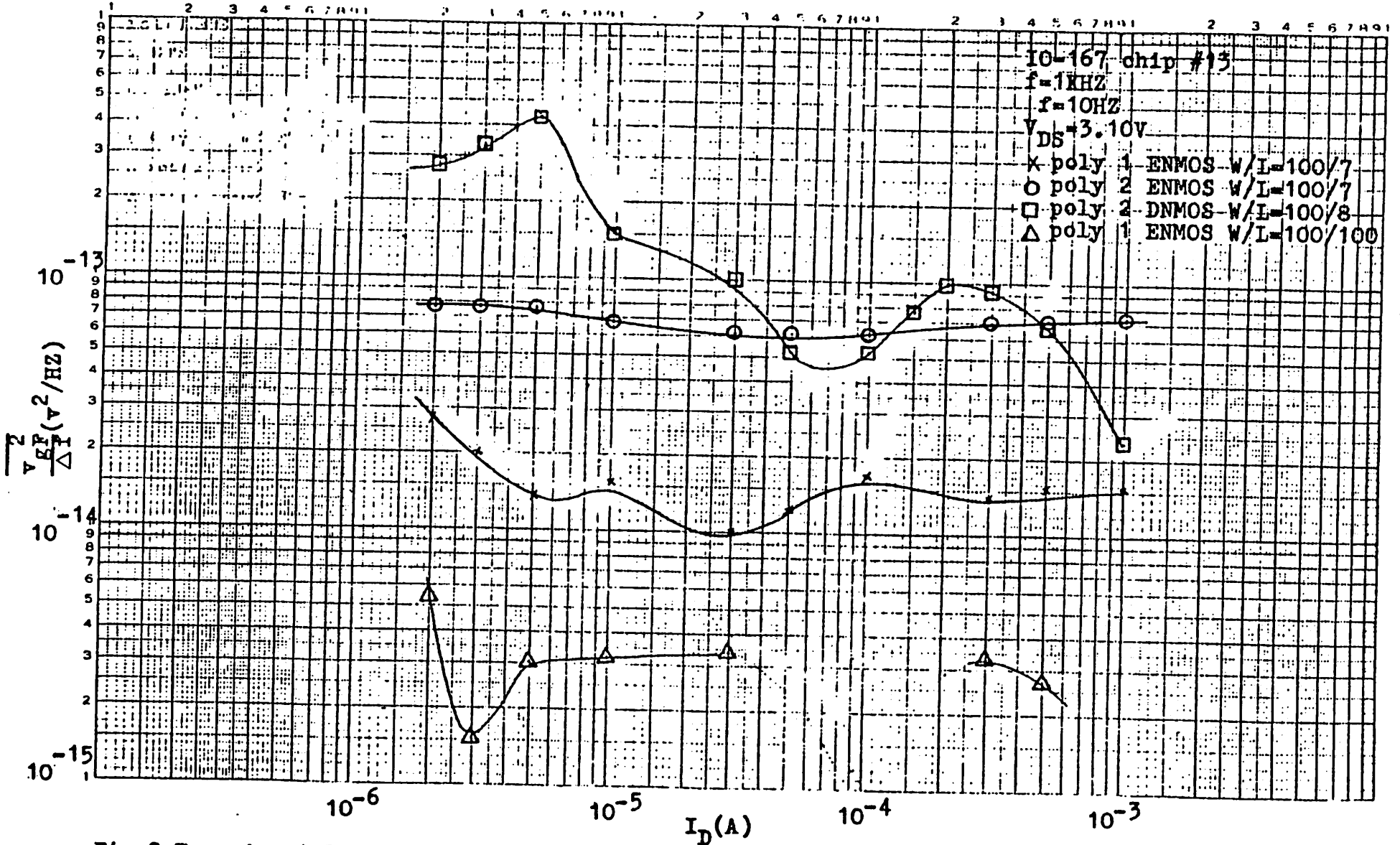

Fig.9 Experimental results on four NMOS's on the same chip showing the variation of the equivalent gate input noise voltage per unit bandwidth with drain current at 1KHZ

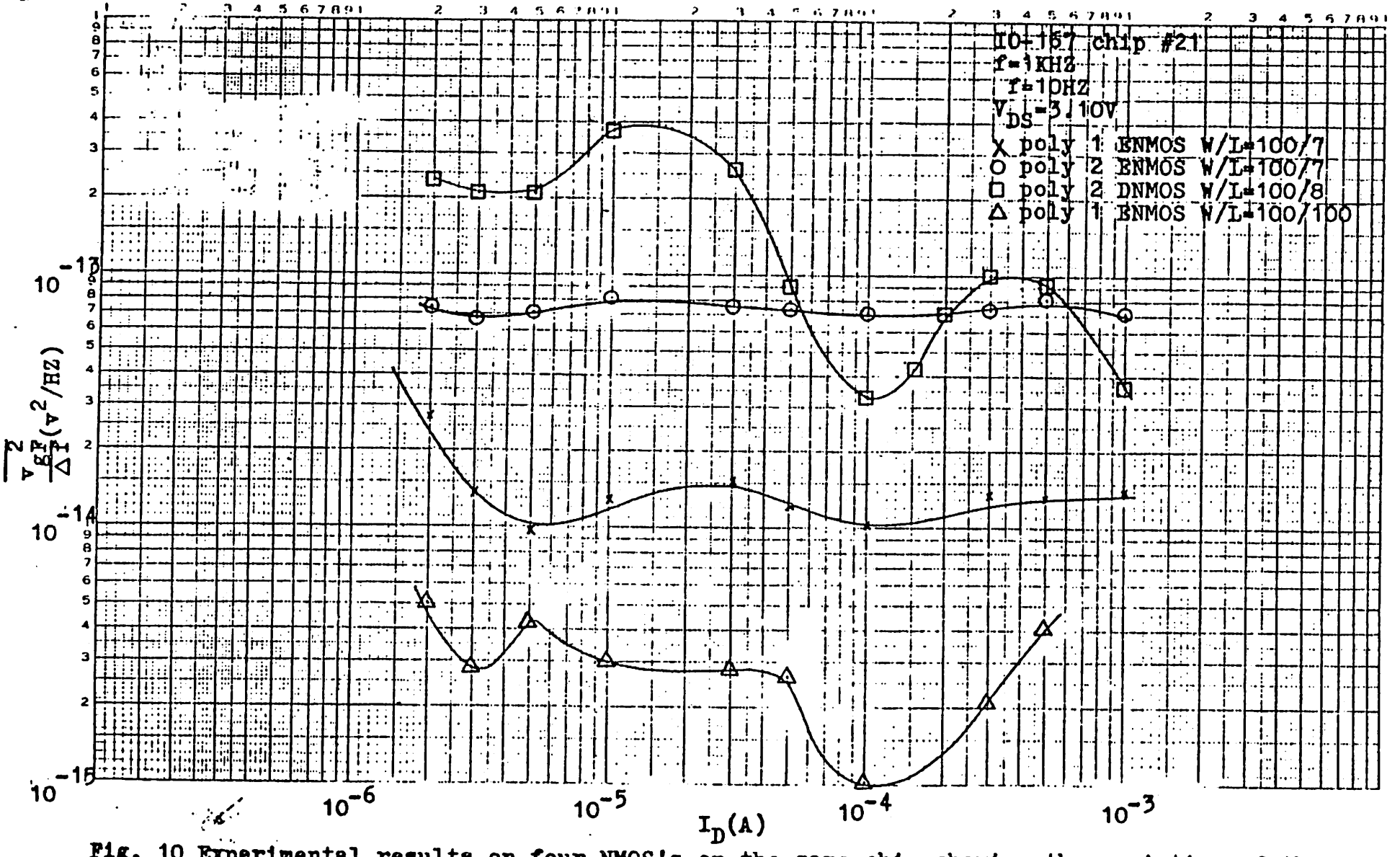

Fig. 10 Experimental results on four NMOS's on the same chip showing the variation of the equivalent gate input noise voltage per unit bandwidth with drain current at 1 KHZ

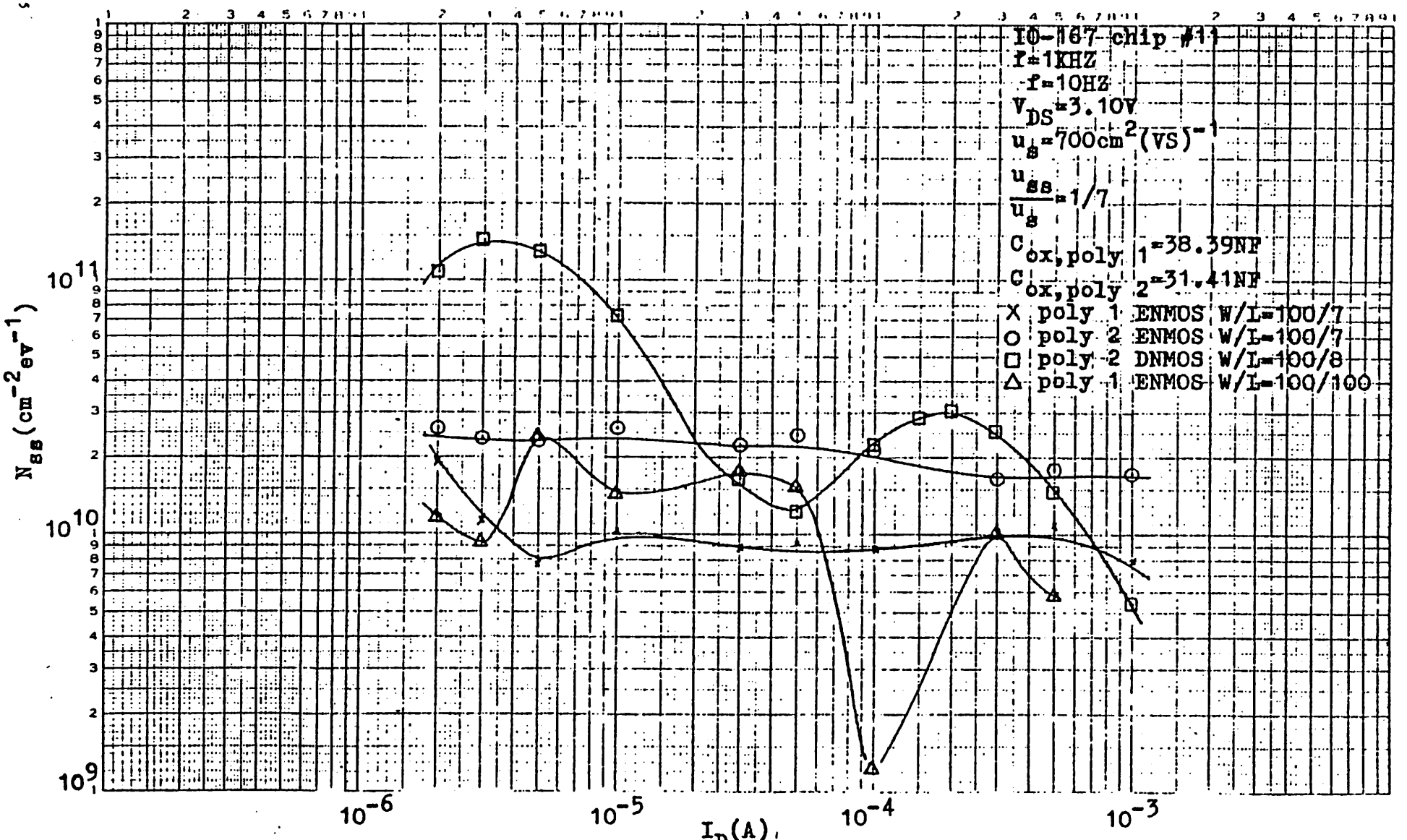

Fig.11 Theoretical results of surface state density versus drain-bias current based on the unified noise equation (3).

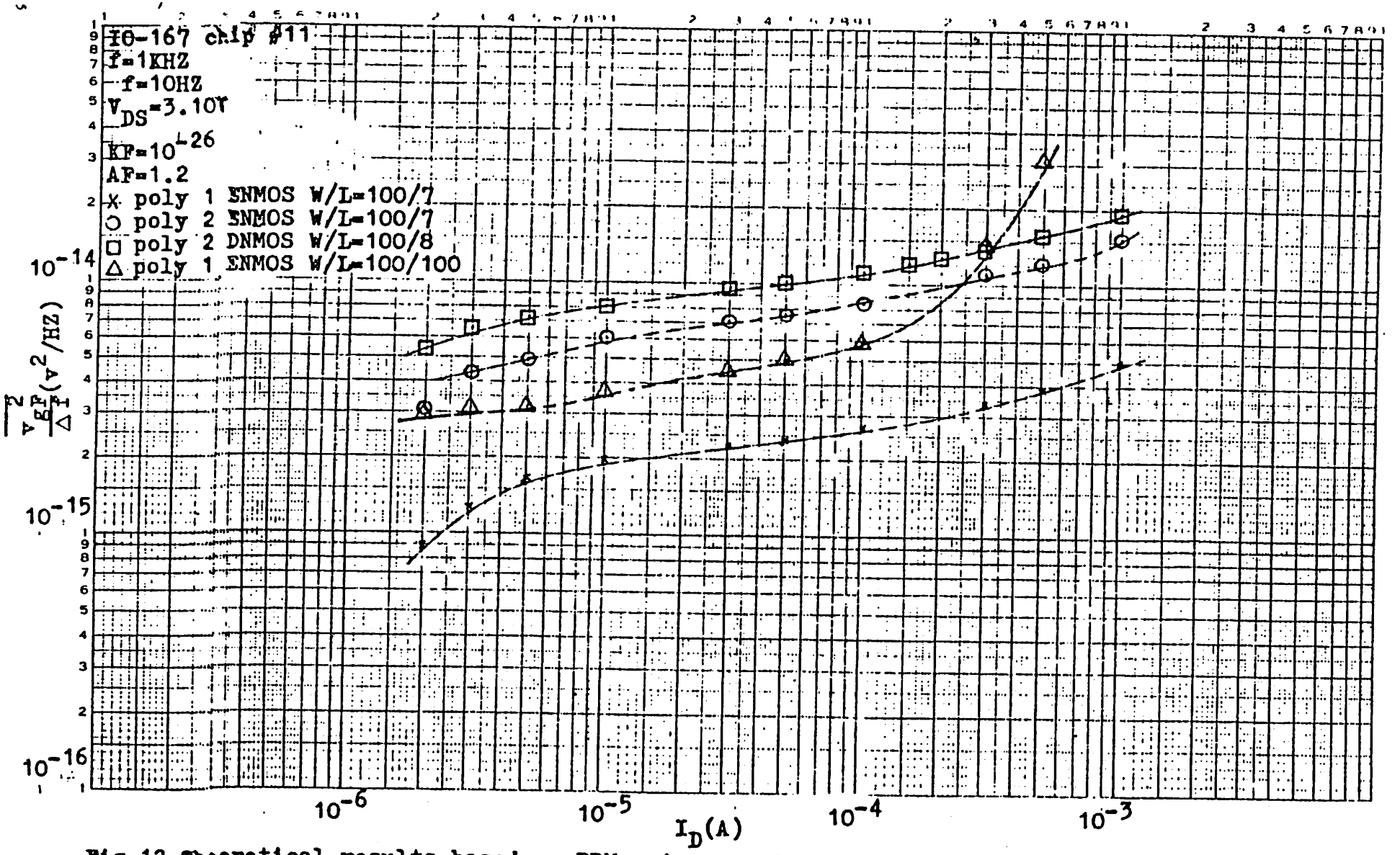

Fig.12 Theoretical results based on BDM noise equation on four NMOS's on the same chip showing the variation of the equivalent gate input noise voltage per unit bandwidth with drain current at 1KHZ

Table 1: Switching System of Bias and Noise Measurements in the Curcuit of fig. 7

Switch / Measurement	SW1	SW2	SW3	SW4	SW5	SW6	Equivalent Circuit	Note
I_D	2	2	1	on	on	on		R_4=0, adjust R_5
V_{GS}	2	2	2	on	off	on		R_4=0
v_{ot}	2	2	2	on	off	on	fig. 3	R_4=0, current meter removed
v_{top3}	1	1	1	on	off	on	fig. 4	R_4=0, $V=V_{DS}$ current meter removed
v'_{ot}	1	1	1	on	off	on	fig. 5	adjust R_4 such that $V_3^+=V_{DS}$

Table 2: NMOS devices in I0-167 chip

pin #	Type	Poly Layer	W/L
5	ENMOS	1	100/7
6	ENMOS	2	100/7
1	DNMOS	2	100/8
24	ENMOS	1	100/100

H. Appendix

a. Description of Measurement System and Circuits

The heart of the system consists of a negative feedback loop circuit involving the test device and an operational amplifier. With chosen drain bias current and drain-source bias voltage, gate-source bias is forced to a characteristic value by the negative feedback loop. The circuit uses a range of resistors R_5's to achieve different drain-current bias values. Voltage values of batteries at the inverting input of output operational amplifier OP3 are drain-source bias values.

In the course of this investigation, this circuit uses metal film resistors in order to eliminate the unwanted effects contributed by the resistors to the magnitude of the 1/f noise voltage referred to the input gate terminal. The bandwidth, Δf, 10HZ and time constant 100 sec of the selective amplifier circuit of the wave analyzer Quantec 304 are chosen. All noise voltages at the output of operational amplifier OP3 are measured with unwanted meters and signal generators removed. The voltage gain of the system was determined by direct measurement (fig. 3) or calculation (eq. 17). Most of the measurements were performed in drain-current saturation region.

With appropriate switching system in Table 1, the circuit in fig. 7 can measure overall noise voltage with test device (fig. 4), noise voltage due to output operational amplifier OP3 with test device removed (fig. 5) and noise voltage due to DC current-source and OP3 with test device removed (fig. 6).

b. Preparation for Measurement

1. Gate-source bias voltage V_{GS}

Gate-source bias voltages, V_{GS} are measured at different drain bias currents by varying R_5 in circuit of fig. 2.

2. V_T calculation

Linear regression is used to find

$$\sqrt{I_{Dsat}} = a_1 V_{GS} + a_0 \tag{12}$$

and

$$V_T = -a_0 / a_1 \tag{13}$$

3. g_m calculation

g_m is calculated by the following equation:

$$g_m = \frac{2I_D}{V_{GS}-V_T} \qquad V_{GS}-V_T \leq V_{DS} \tag{14}$$

or

$$g_m = \frac{I_D}{V_{GS}-V_T-V_{DS}/2} \qquad V_{GS}-V_T \geq V_{DS} \tag{15}$$

4. Zero compensation capacitance C_1.

Waveforms at output of operational amplifier OP3 corresponding to each drain bias current are observed. If there are oscillations, a zero compensation capacitance $C_1 = \frac{1}{2\pi f_{osc} R_1}$ is chosen, where f_{osc} is the minimum oscillaton frequency among the oscillations occurred.

5. g_m compensation resistance R_3

Voltage across R_3 should be at least ten times greater than the offset voltage of OP-07. Besides, R_3 should be large enough to minimize noise effect from DC current-source on equivalent gate noise voltage, i.e.

$$\left(\frac{v_{eq}}{g_m R_3}\right)^2 << \left(\frac{v_{ot}}{A}\right)^2 \qquad (16)$$

6. Overall small signall gain A at f=1KHZ

Overall small signal gain A is determined directly by circuit either in fig. 3a or fig. 3b. Overall small signal gain A can also be calculated by

$$A = \left|\frac{v_o}{v_g}\right| = \left|\frac{R_2+R_1}{R_2} \quad \frac{1}{(R_1C_1S+1)}\right| \qquad (17)$$

c. Procedures of Noise Measurement

1. Equivalent gate total noise voltage $v_{ot/A}$

Output noise voltage v_{ot}, is measured by circuit in fig. 4 and is referred to gate.

2. Equivalent gate operational amplifier OP3 noise voltage $v_{gop3} = v_{top3}/A$

Noise voltage v_{top3} due to output operational amplifier OP3 alone is measured by circuit in fig. 5 and is referred to gate.

3. Equivalent gate DC current source noise voltage $v_{eq}/(R_3 g_m)$ Output noise voltage v'_{ot} is measured by circuit in fig. 6 and the equivalent DC current-source noise voltage is calculated by the following equation:

$$v_{eq} = \left(\frac{(v'_{ot}/A)^2 - (v_{gop3})^2}{R_4^2} \right)^{1/2} R_3 \qquad (18)$$

R_4 in fig. 6 is adjusted such that DC bias at non-inverting input of output operation amplifier OP3 equals V_{DS}.

4. Equivalent gate NMOS noise per unit bandwidth $\overline{v_{gF}^2}/\Delta f$ is calculated by the following equation:

$$\frac{\overline{v_{gF}^2}}{\Delta f} = \frac{1}{\Delta f} \left[\left(\frac{v_{ot}}{A}\right)^2 - \left(\frac{v_{eq}}{g_m R_3}\right)^2 - v_{gop3} \right] \qquad (19)$$

d. Part List

1. Operation Amplifiers: OP-07
2. Bipolar Transistor: 2N3706
3. Restors: metal film restors
4. Capacitance: electrolytic
5. Batteries
6. Bread board

e. Apparatus

1. Wave analyzer: Quantec 304M
2. Oscilloscope: Tektronix 7704A
3. Wave generator: WaveTek, model 132
4. Digital multimeter: Fluke 8020A
5. DC power supply: Hewlett Packard 6325A

f. Notes on Measurement

1. Measurement should be carried out in a screen room.
2. Make sure that operational amplifiers are not in saturation before each noise measurement.
3. All unused cables, meters are removed before noise measurement.
4. The whole CKT should be in a metal shielding box during noise measurement

I. References

1. Makunda B. Das and James M. Moore, "Measurements and interpretation of low-frequency noise in FET's," IEEE Trans. Electron Devices., vol. ED-21, pp. 247-257, April 1974.
2. E.A. Leventhal, "Derivation of 1/f noise in silicon inverstion layers from carrier motion in a surface band." Solid-State Electron., vol. 11, pp. 621-627, 1968.
3. S. Christensson, I. Lundstrom, and C. Svensson, "Low-frequency noise in MOS transistor-: Theory," Solid-State Electron., vol. 11, pp. 796-812, 1968.
4. I. R. M. Mansour, R. J. Hawkins, and G. G. Bloodworth, "Physical model for the current noise spectrum of MOST's," Brit. J. Appl. Phys., vol. 2, pp. 1067-1082, 1969.
5. S. T. Hsu, "Surface State related 1/f noise in MOS transistor," Solid-State Electron., vol 13, pp. 1451-1459. Nov. 1970.
6. H. S. Fu and C. T. Sah, "Theory and experiment on surface 1/f noise," IEEE Tran. Electron Devices, vol. ED-19, pp. 273-285, Feb. 1972.
7. F. Berz, "Theory of low-frequency noise in MOST's," Solid-State Electron., vol. 13, pp. 631-647, 1970.

8. F. M. Klaassen, "Characterization of low 1/f noise in MOS transistor.," IEEE Trans. Electron Devices, vol. ED18, pp. 887-891, October 1971.

9. A. L. McWhorter, Semiconductor Surface Physics. R. H. Ding. Ed. Philadelphia, Pa.: University of Pennsylvania Press, 1956, p. 207.

10. D. R. Alexander, R. J. Antinone and G. W. Brown, SPICE2 MOS Modeling Handbook, BDM Corporation, Albuquerque, 1977.

11. I. Flinn, G. Bew, and F. Berz, "Low-frequency noise in MOS transistors-II: Experiments," Solid-State Electron., vol. 2, pp. 813-820, 1968.

12. C. G. Rogers, "Low-frequency noise in MOST's at coyogenic temperature," Solid-State Electron., vol. 11, pp. 1099-1104, 1968.