A MOS SWITCHED-CAPACITOR INSTRUMENTATION AMPLIFIER

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ABSTRACT

This paper describes a precision switched-capacitor sampled-data instrumentation amplifier using NMOS poly-silicon gate technology. It is intended for use as a sample-and-hold amplifier for low level signals in data-acquisition systems. The use of double correlated sampling technique achieves high power supply rejection, low dc offset and low 1/f noise voltage. Matched circuit components in a differential configuration minimize errors from switch channel charge injection. Very high common mode rejection (120 dB) is obtained by a new sampling technique which prevents the common mode signal from entering the amplifier. This amplifier achieves 1 mV input offset voltage, greater than 95 dB PSRR, 0.15% gain accuracy, 0.01% gain linearity, and a rms input referred noise voltage of 30 uV per input sample.

Introduction

Analog data acquisition systems often need to perform analog to digital conversion on signals of very small amplitude or signals superimposed on large common-mode components. This problem is traditionally solved by using fixed gain differential amplifier implemented as a stand-alone component in bipolar technology [1],[2]. However, MOS technology is increasingly being utilized to implement monolithic data acquisition systems, either as a stand-alone component or as part of a control oriented microcomputer or signal processor [3].

A typical data acquisition system generally consists of an input amplifier, sample and hold stage, and an A to D converter. The amplifier serves to increase the signal level prior to analog to digital conversion. Input offset voltage is a key aspect of amplifier performance since it can limit dc system accuracy. In some systems, it is possible to measure and substract the dc offset, but the equivalent input noise voltage represents a fundamental limit on the resolution of the system. Also, gain accuracy and gain linearity are critical parameters for instrumentation applications. In some cases, a low-amplitude signal input is superimposed on large common mode components due to electrostatic or electromagnetic induction. This adds a requirement for high common mode rejection. The data acquisition circuit may reside on the same chip as the digital LSI processor; therefore, the ability to reject power supply noise is also very important.

Compared with bipolar devices, MOS transistors display smaller transconductance at a given drain current level. This makes it difficult to achieve large values of voltage gain in a single MOS amplifier stage, and also results in high DC offsets in source coupled pairs. Also, the MOS devices inherently displays much larger 1/f noise than bipolar devices.

This paper describes a switched-capacitor circuit technique which employs double correlated sampling [4] to reduce the circuit dc offset and low frequency noise; it also uses balanced circuit configuration to achieve first order cancellation of switch channel charge injection. A charge redistribution scheme is described in this paper which allows the circuit CMRR to be independent of the op-amp CMRR, thus resulting in a very high overall common mode rejection ratio.

In section 2, a circuit approach to implement sample and hold instrumentation amplifier is described. The prototype implementation of this circuit using NMOS technology is depicted in section 3. The switch channel charge injection problems are addressed in section 4, and the fundamental noise limitation of KT/C noise is also discussed. Finally, in section 7 the experimental results of this circuit fabricated using local oxidation NMOS poly-silicon gate technology are presented.

Section 2 - Circuit Description

The MOS implementation of the differential double correlated sampling amplifier is shown in Fig.1. This circuit consists of a pair of sampling capacitors, C1, C2; gain setting capacitors, C3, C4; offset cancellation capacitors, C5, C6; and two differential amplifiers A1 and A2, where amplifier A1 is a broadband, low gain differential preamplifier, and A2 is a high gain differential operational amplifier. The input signal is sampled on to the sampling capacitors C1, C2, and subsequently transferred to the gain setting capacitors C3, C4 through a sequence of switching operations. The output voltage will be a replica of the input differential signal with a voltage gain defined by the capacitor ratio (C1+C2)/(C3+C4). The circuit is fully differential so that all the switch charge injection and power supply variations are cancelled to first order.

Operation of the circuit takes place in two phases as illustrated in Fig. 2. In the sample mode, the switches are closed as shown in Fig. 2a. In this mode, the differential and common mode input voltages appear across both C1 and C2. The difference between the offset voltage A1 and A2 is impressed across C5 and C6. The instantaneous value of the 1/f noise of both amplifiers is also stored. A requirement on this amplifier, A1, is that its gain be low enough so that its output does not saturate on its own offset when the inputs are shorted.

The input signal is sampled and a transition to the hold mode is made when clock one goes negative, turning off the input sampling switches and feedback switches. Subsequently, the switches are closed as shown in Fig. 2b, and the voltage difference between the two inputs is forced to zero. This causes a charge redistribution in capacitors C1, C2, C3, and C4, which results in an output voltage which is only proportional to the input difference voltage. Any common mode input voltage will not cause charge redistribution error even if the capacitors do not match each other exactly. Another requirement of the amplifier, A1, is that it must have a high enough bandwidth such that the loop stability is assured in this mode. Differential amplifiers A1 and A2 together must provide enough loop gain to achieve the desired closed loop gain accuracy.

This circuit has many advantages compared to other techniques. Because the amplifier dose not experience any common mode shift, the overall common mode rejection of the circuit is independent of the common mode rejection of the operational amplifier. Because of the balanced nature of this circuit, switch charge injection and clock feedthrough are cancelled to the first order. Because of the equal and opposite voltage excurrsion on the capacitors, the capacitor nonlinearity is also cancelled to the first order. The sampling bandwidth of this circuit is determined by the RC time constant of the input switch and capacitor, which is usually much faster than the settling time of an operational amplifier. The gain is set by capacitor ratios, which has

good initial accuracy [5]. very good temperature stability and is trimmable. Both the 1/f noise and the dc offsets are reduced by the use of double correlated sampling; and as a result of this usage and the balanced nature of the circuit, the power supply rejection is also very high.

The overall performance of this circuit is limited by the mismatch of charge injection from the input switches. In this switched capacitor instrumentation amplifier circuit, cancellation of switch channel charge injection is guaranteed by the symmetry of the circuit, and the offset becomes limited primarily by the mismatches of the switch charge injection. The mismatch in the switch channel charge is determined by mismatches in device parameters such as threshold voltage, channel geometry, and so forth. Experimental results to be presented later indicate that the channel charge mismatch in an 8 micron MOS device is typically on the order of one percent.

Section 3 - Experimental Implementation of Switched Capacitor Instrumentation Amplifier

Precision preamplifiers may be required to provide voltage gains from less than ten to over one thousand. The use of a single stage to obtain very large values of voltage gain requires operational amplifiers with very large open loop gain. and also very large capacitor ratios. In NMOS

technology, the voltage gain achievable in operational amplifiers is often limited, and as a result, it is more desirable to use a relatively small value of fixed gain. High values of gain can be achieved by either cascading multiple stages, as shown in Fig.3, or by using a single stage in a recirculating mode [6]. In the example described here, a fixed gain of ten is used. Another problem is the fact that many A to D converters require a single ended input voltage. Thus, a single ended output referenced to ground must be produced. This can be achieved as shown in this example where the first stage of amplification is realized in a fully differential mode, and the last stage uses a single ended output operational amplifier to generate a single ended output voltage.

Operational Amplifier Design

The broadband, low gain, differential preamplifier used in this system is just a simple differential pair with enhancement load devices. The single ended output operational amplifier shown in Fig.4 is a conventional NMOS operational amplifier design [7]. Transistors M1-M5, M20-M23, and M24-M29 are the input, gain, and output stages respectively. C1 and C2 are feedthrough capacitors, and C3 is the Miller compensation capacitor. Transistor MC is a depletion mode resistor for right half plan zero compensation. The DC bias points of this op-amp are set by the replica bias circuit composed of transistors M6-M17 [8]. Half of the voltage gain of the input stage is traded for higher frequency operation.

The output stage has a capability to drive a large capacitive load without losing a significant phase margin. This op-amp realizes a voltage gain of about 1500 with output voltage swing of about 6.5 volts.

Fig.5 shows the schematic of the fully differential operational amplifier. It uses two differential stages to achieve a voltage gain of 1500. Common mode feedback are used in these two stages to stabilize the dc bias condition. The output stages are simple source followers. The capacitors and depletion devices are for frequency compensation. Since this op-amp is to be used only at the front end stage where the signal swing is small, the output range of this amplifier is designed to be about 1 volt.

Section 4 - MOS Switch Induced Errors

MOS switches are indispensable in switched capacitor type circuits such as filters, A/D, D/A, and sense amplifiers. However, MOS switches often introduces a significant amounts of error due to clock voltage feedthrough through the gate-source, gate-drain overlap capacitance and the channel charge stored in the MOSFET switch.

As shown in Fig.6, the MOS switch is connected with a sampling capacitor which is charged to the input voltage level. When the MOS switch is turned off, the amount of

channel charge injected into the sampling capacitor represents an error source as a result of the sudden release of the charge under the MOS gate. The amount of channel charge that flows into the sampling capacitor as opposed to the amount that flows back to the input terminal is a complex function of the gate voltage fall time, input impedance level, and the size of the sampling capacitor [9]. For a typical switch size of 10X10 micron and a sampling capacitor of 5 pF for example, a 5 volt gate overdrive will introduce an error of 20 mV if half of the channel charge flows into the sampling capacitor.

One approach to the reduction of this type of error is the use of a dummy switch and dummy capacitor [10] as shown in Fig.7b. This configuration assures by symmetry that exactly one half of the channel charge will flow into the sampling capacitor. Thus, the dummy switch with one half the size of the input switch can guarantee the exact cancellation of both the channel charge injection and the clock feedthrough problems. This technique works well when the source impedance, clock frequency and fall time are all well controlled. However, when the signal is driven from an external source whose impedance level is low, this dummy capacitor will have very little effect on the the channel charge cancellation.

The differential sampling configuration shown in Fig.7c uses two carefully matched switches and capacitors to sample the differential signal. The channel charge injection will introduce the same error voltage on these two sampling

capacitors, thus giving no differential error on the sample voltages. Although the differential input voltage introduces a difference of channel charge in the two matched switches, this error term is proportional to the input differential voltage, and can be considered as a gain error.

One drawback in the configuration shown in Fig.7c is that the channel charge cancellation relies on the matching of the two differential input impedances. For circuits integrated inside a chip, the driving sources' impedance level can be well matched. However, if the sampling switches and capacitors are to be interfaced with external signal sources whose impedance level will vary, then a slight modification of the balanced configuration shown in Fig.8 will guarantee the cancellation of channel charge error under all the conditions [9]. The dummy capacitors shown in Fig.8 only serve the purpose of lowering and matching the driving source impedance level, thus their size does not have to match that of the sampling capacitors.

Another error source due to the sampling switch and capacitor is the KT/C noise [11]. This noise is generated from the broad-band thermal noise associated with the on resistance of the switch. Since the switch on-resistor and the sampling capacitor form a low pass network which band-limits the broad-band thermal noise, the total noise energy sampled onto the capacitor will be just KT/C. This KT/C noise represents a fundamental limit to the resolution of the system. For a typical sampling capacitor value of 10 pF,

the standard deviation of this noise uncertainty is about 25 uV. For a system sampling at 200K Hz, this corresponds to an in-band noise density of 50 nV per root Hz, or an equivalent noise resistance of 1.5 mega ohm. In the amplifier described in this paper, KT/C noise is the dominant noise source, since the 1/f noise is reduced by double correlated sampling.

Section 5 - Experimental Results

Two experimental circuits for the fully differential stage and single ended output stage were designed and fabricated using a local oxidation poly-silicon gate NMOS process with depletion load. The minimum geometry used in these circuits was 7 micron. The input sampling capacitors are 10 pF each, feedback capacitors are 1 pF, and the DCS capacitors are 3 pF.

A die photo of the switched capacitor amplifier with differential output stage is shown in Fig.9. The top part of the die photo contains the matched capacitor arrays, the bottom part contains the differential amplifier. The symmetrical layout of the circuit is crucial to the matching of circuit components. The die area of this circuit is about 2500 square mils.

Fig.10a shows the output waveform of this circuit with a 1 KHz sinusoidal input signal. The staircase-shaped waveform is the result of the sample and hold operations. Shown in Fig.10b is the output waveform with a square wave input signal. The output is reset to its own offset value during the sample mode when clock 1 is high, and generates an amplified input sample during the hold mode when clock 2 goes high.

Fig.11 shows the experimentally observed input offset voltage and common mode rejection ratio for five typical samples of the circuit as a function of source resistance. For small values of source resistance, the average value of the input offset voltage is 1 mV; this actually results from a layout induced systematic offset in the amplifier offset cancellation circuit and not from charge injection in the input switches. The spread of this offset is about 500 uV, which increases at high values of source resistance because the percentage of the channel charge injected into the sampling capacitors increases [9]. The CMRR at low values of source resistance is about 120 dB. This is also degraded at high values of source resistance for the same reason as the offset voltage.

Fig.12 illustrates the typical gain nonlinearity observed for the device. This nonlinearity results primarily from the nonlinear open loop characteristic of the operational amplifier. The peak deviation from linear behavior is about 0.012% of full scale at plus and minus three volts output

swing.

Table 1 shows the summary of the data measured at room temperature for power supply voltages of plus and minus 7.5 V. The voltage gain is ten with a gain accuracy of 0.15%, which is caused primarily by the finite loop gain of the operational amplifiers. The offset voltage is 1 mV.

Section 6 - Conclusion

A differential double correlated sampling instrumentation amplifier has been described. By sampling and cancelling the low frequency noise contributed by the MOS operational amplifier, the 1/f noise of the operational amplifier is virtually removed. This technique allows periodic offset cancellation of the circuit, thus, results in very low offset, very low drift, and large PSRR. A CMOS version of this circuit would have higher operating speed and gain accuracy because CMOS operational amplifiers can achieve larger voltage gain and higher operating speed than that of the NMOS operational amplifiers.

The techniques presented in this paper allow the implementation of precision circuit functions in MOS technology without resorting to process modification. The fundamental limit to the signal resolution is imposed by the KT/C noise, although this noise can be reduced either by using

a larger sampling capacitor, or by taking more sample averages [9]. These techniques enhance the performance MOS circuits for high precision instrumentation. It is hoped that the integration of a completely monolithic MOS data acquisition system will be possible in the near future.

Acknowledgements

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Figure Captions

Figure 1 - Circuit schematic of differential double correlated sampling instrumentation amplifier

Figure 2 - Illustration of the switching sequence of the instrumentation amplifier

Figure 3 - Experimental implementation of a programmable single ended output instrumentation amplifier

Figure 4 - Circuit schematic of single ended NMOS operational amplifier

Figure 5 - Circuit schematic of differential NMOS operational amplifier

Figure 6 - Clock feedthrough & channel charge injection of a MOS switch

Figure 7 - Illustration of several switch channel charge cancellation techniques

Figure 8 - Differential switch charge cancellation with dummy capacitors

Figure 9 - Die photo of a fully differential instrumentation amplifier gain block

Figure 10- Measured circuit output waveform

Figure 11- Experimentally measured Vos and CMRR as a function of source resistance value

Figure 12- Experimentally measured gain nonlinearity

Table 1 - Summary of experimental results

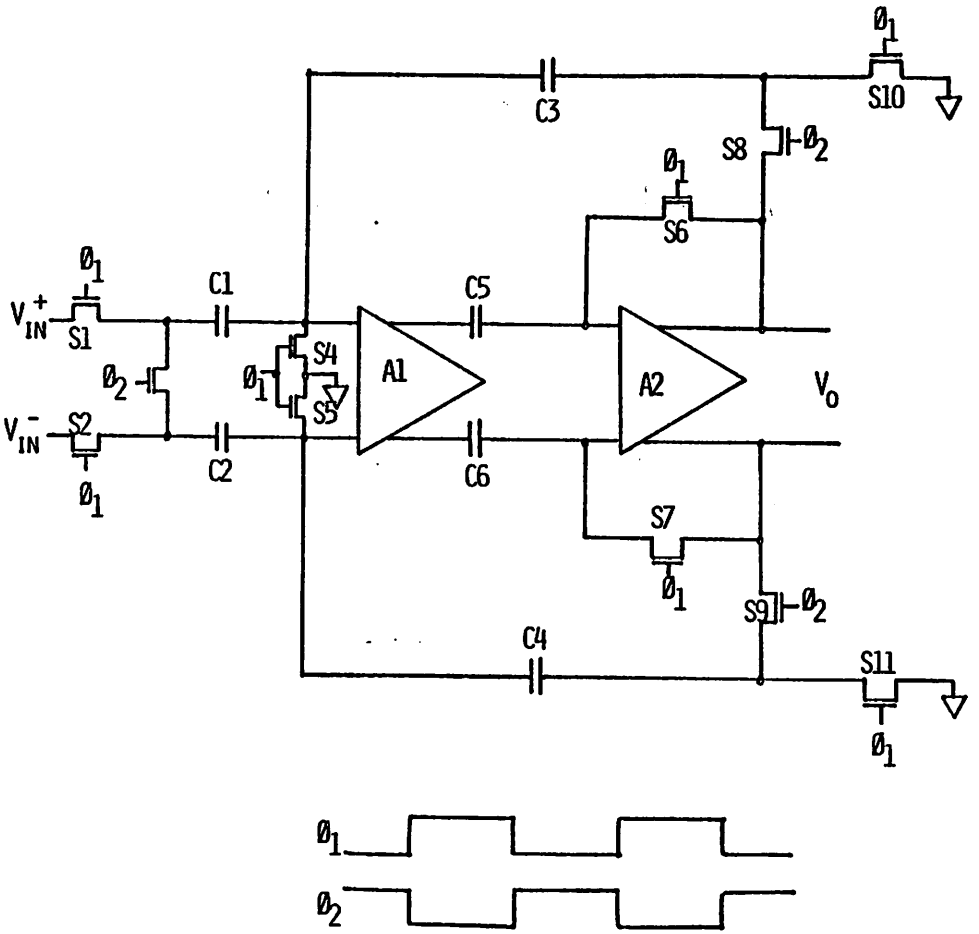


Fig.1 Circuit diagram of differential double correlated sampling amplifier

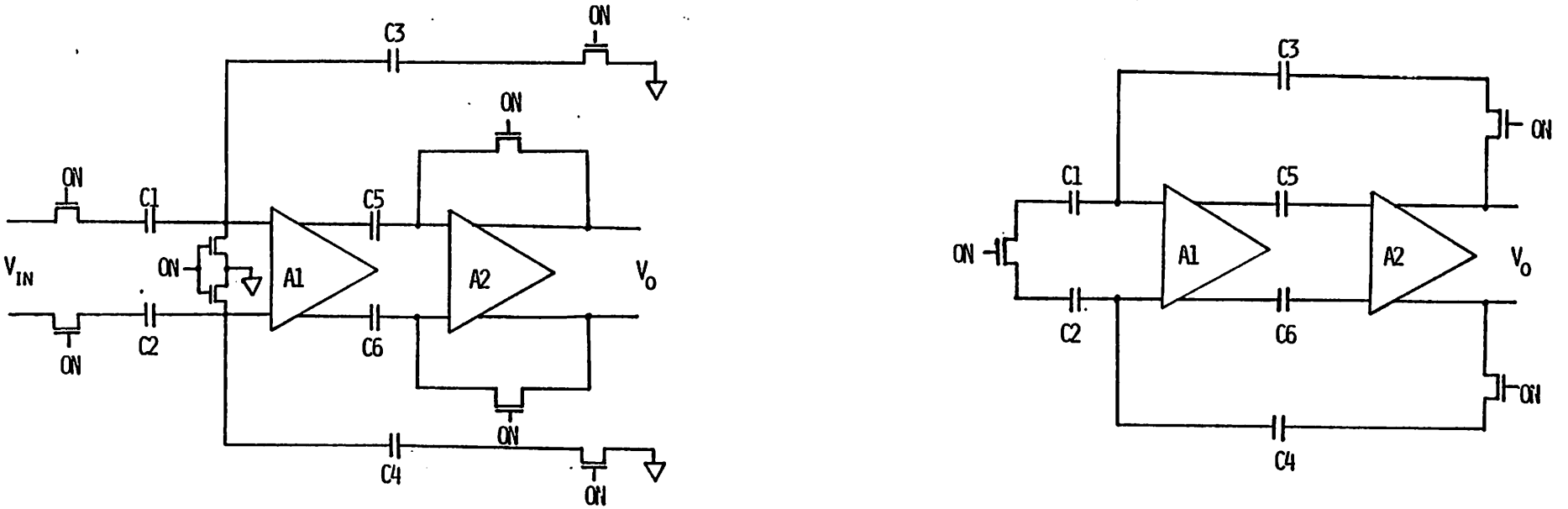


Fig. 2 Operation of the instrumentation amplifier

(a) sample mode, (b) hold mode

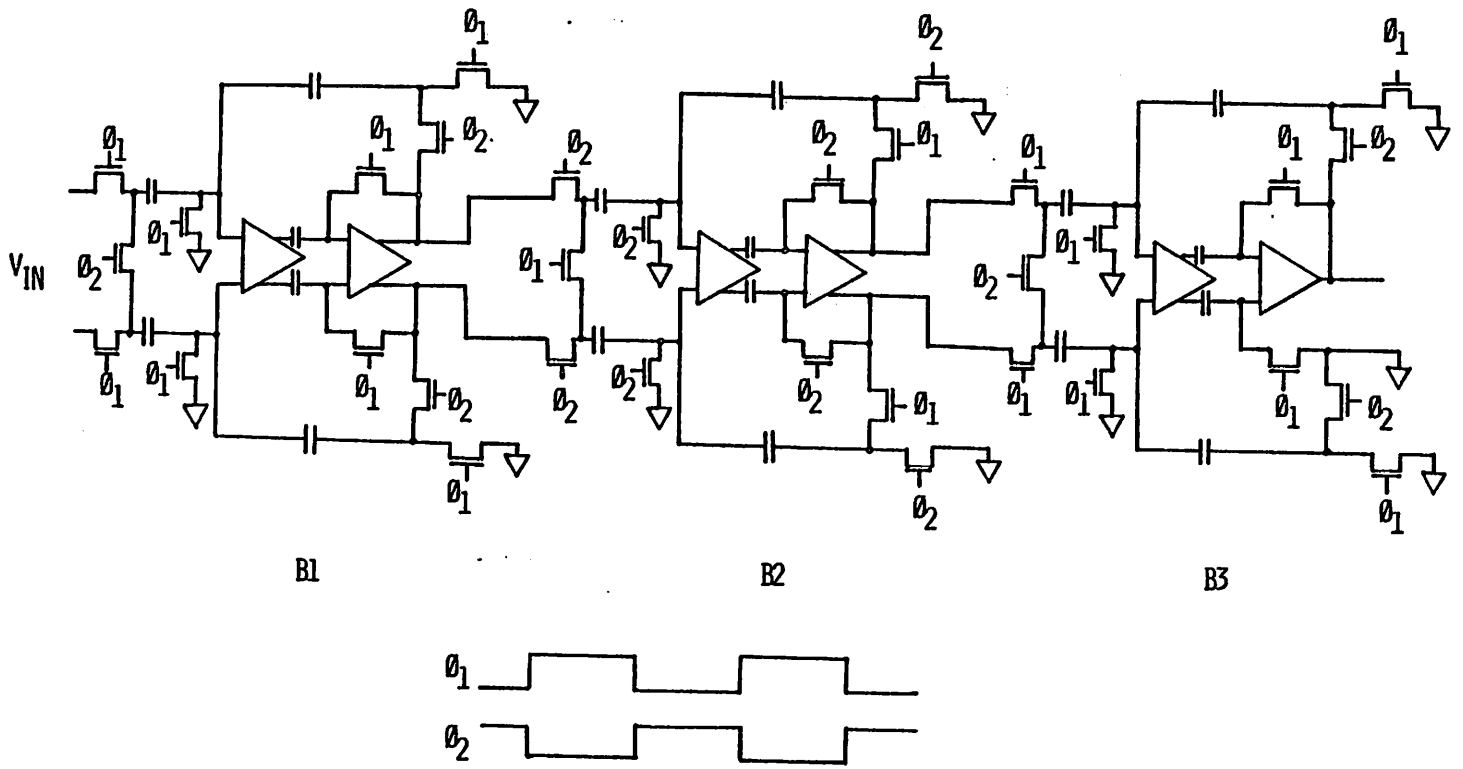


Fig. 3 A programmable single ended output instrumentation amplifier

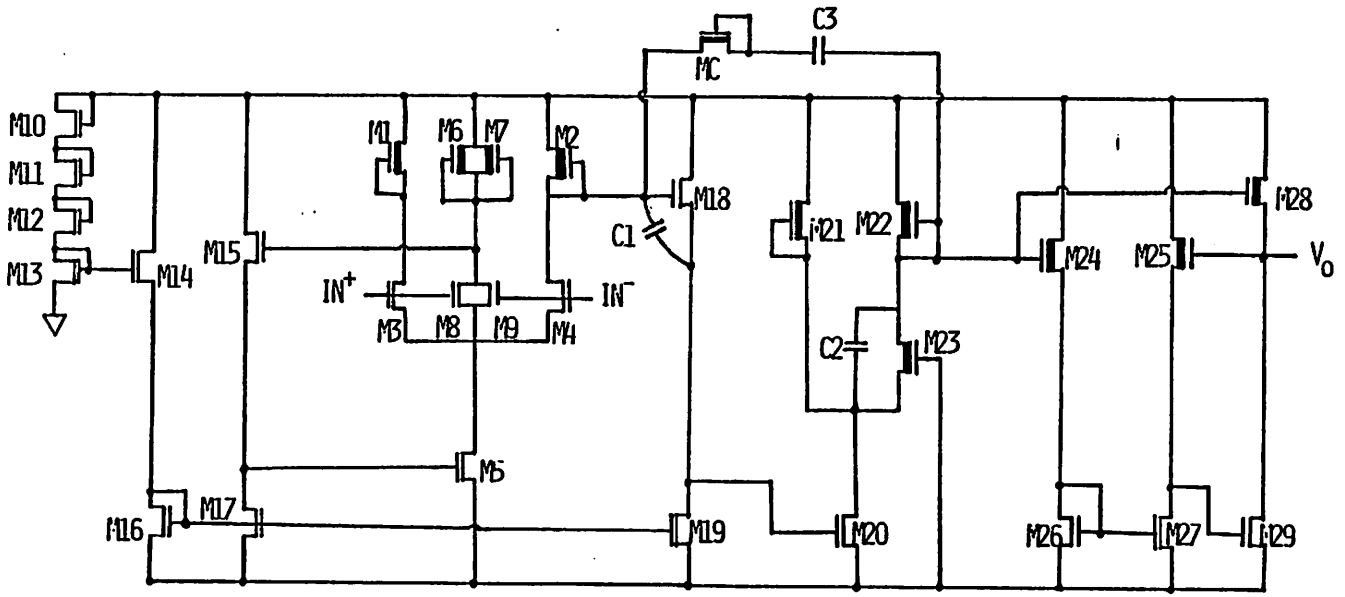


Fig. 4 Circuit schematic of single ended NMOS operational amplifier

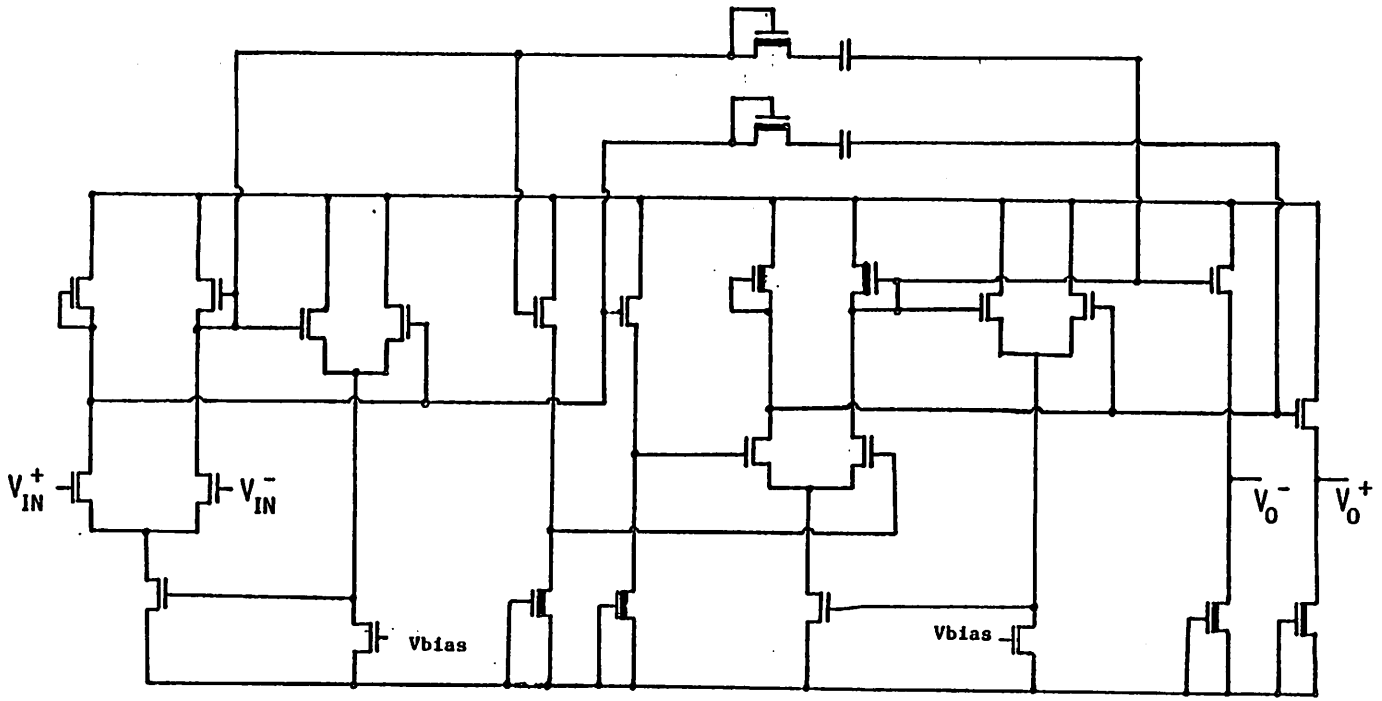


Fig. 5 Circuit schematic of differential NMOS operational amplifier

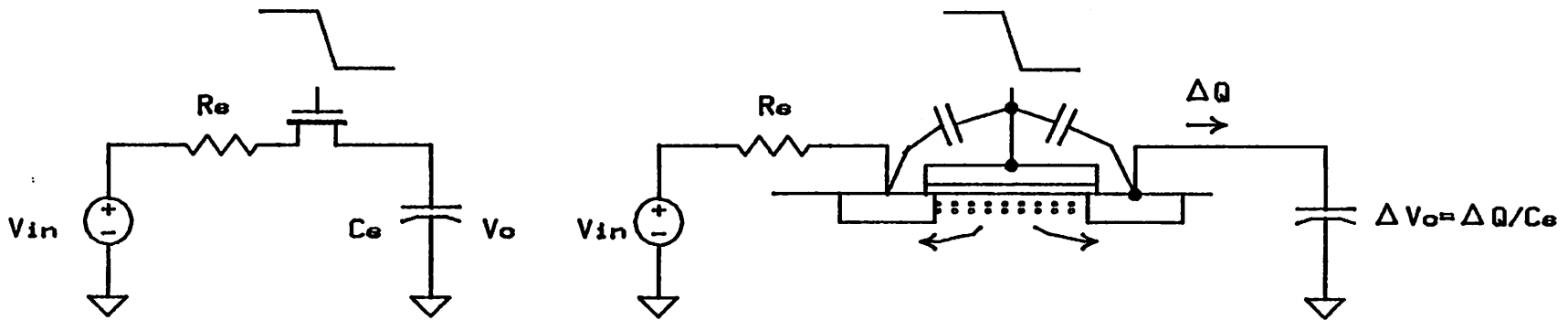
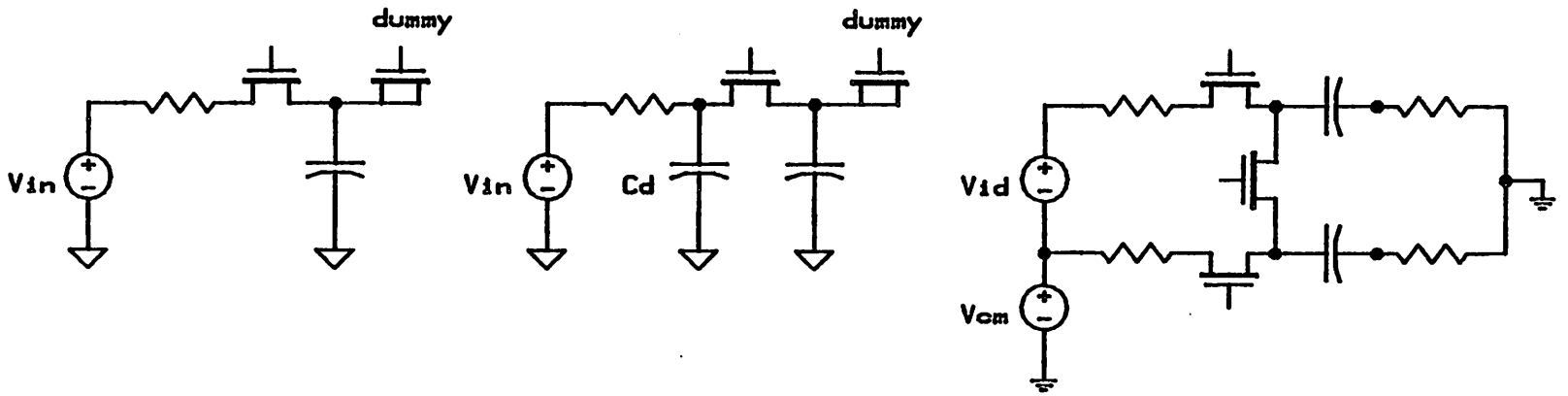


Fig. 6 Clock feedthrough and channel charge injection of a MOS switch

dummy switch dummy capacitor differential scheme



(a) (b) (c)

Fig. 7 Several switch channel charge cancellation techniques

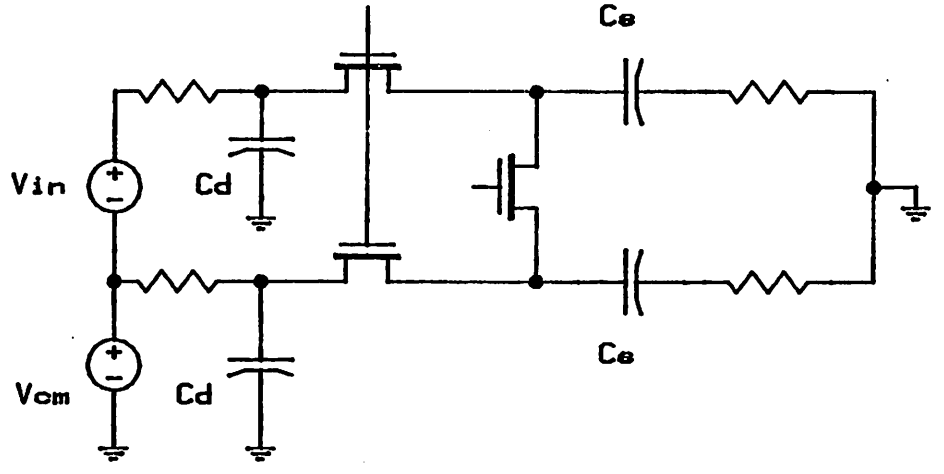


Fig. 8 Differential switch charge cancellation with dummy capacitors

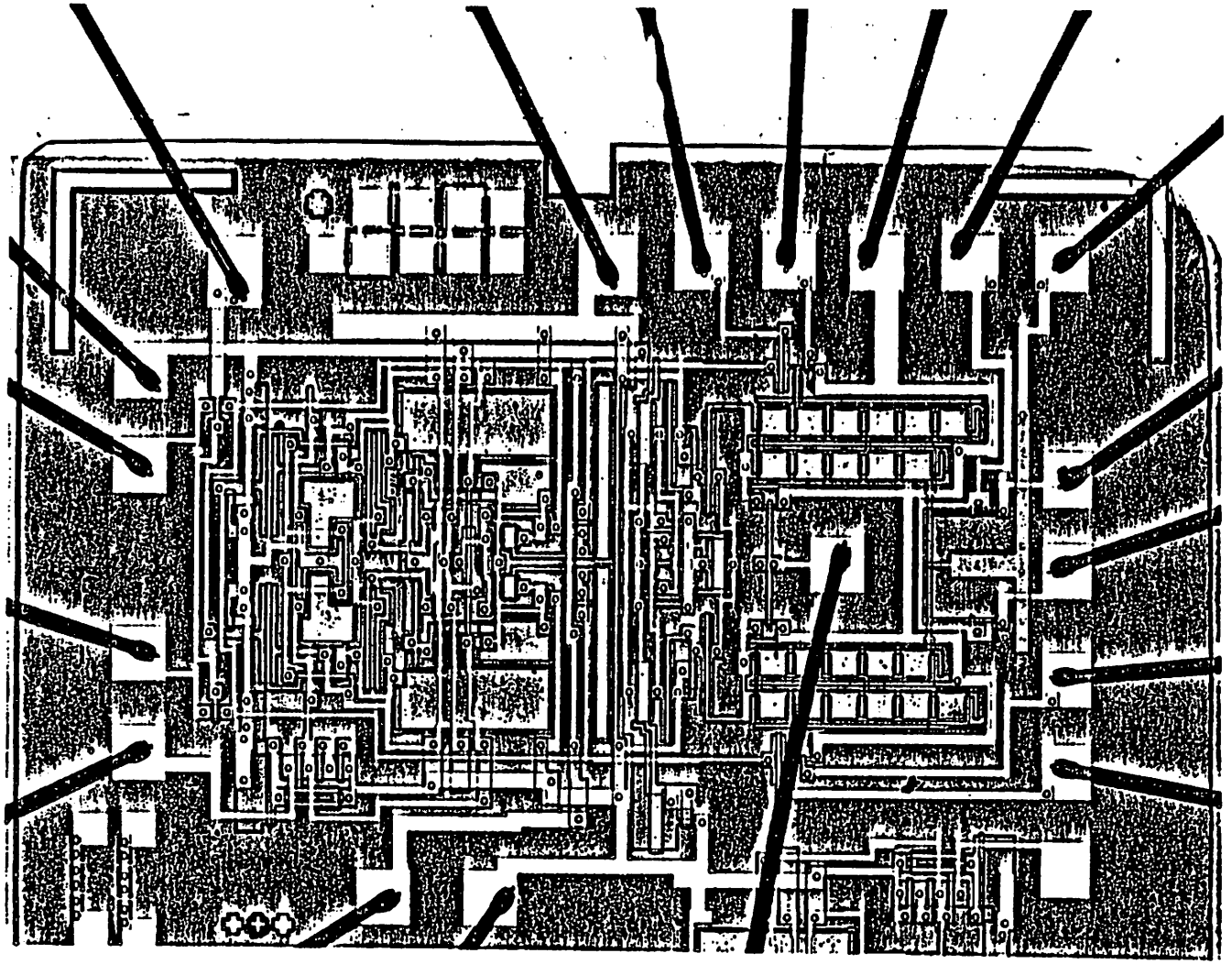
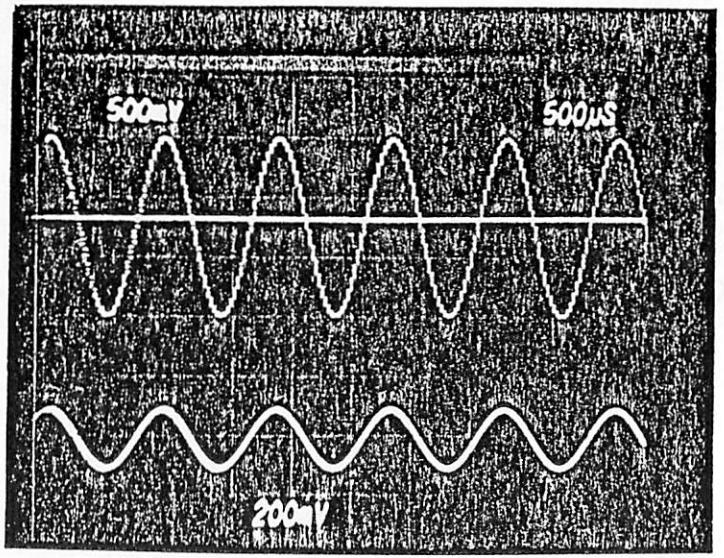
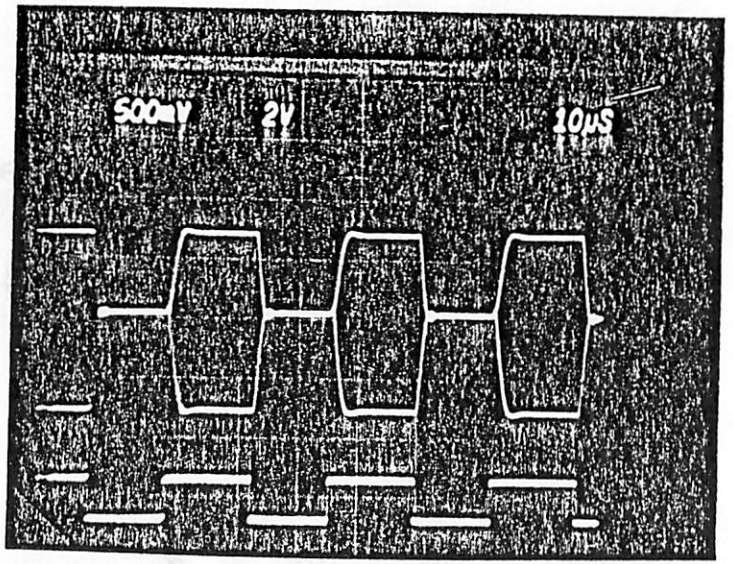


Fig. 9 Die photo of a differential instrumentation amplifier gain block

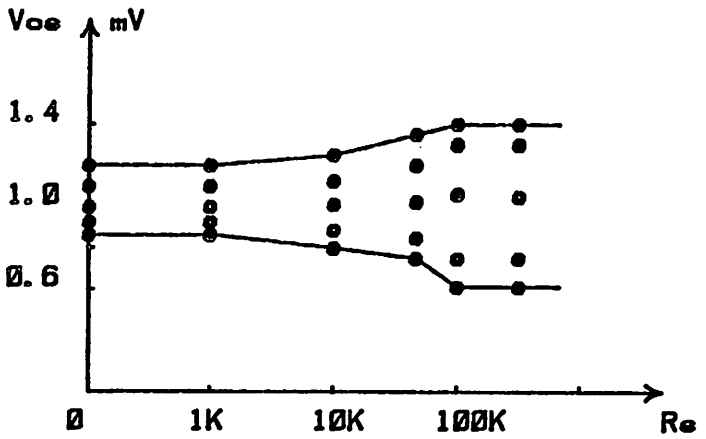


(a)

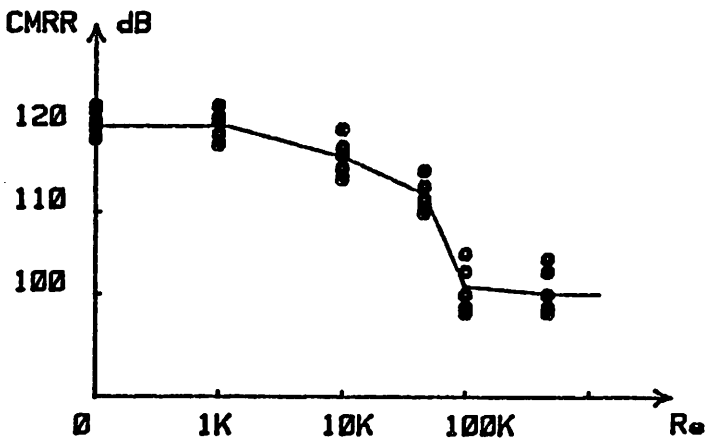


(b)

Fig. 10 Measured output waveform, (a) sinusoidal input, (b) square wave input



(a)



(b)

Fig. 11 Measured input offset voltage (a) and CMRR (b) as source resistance varies

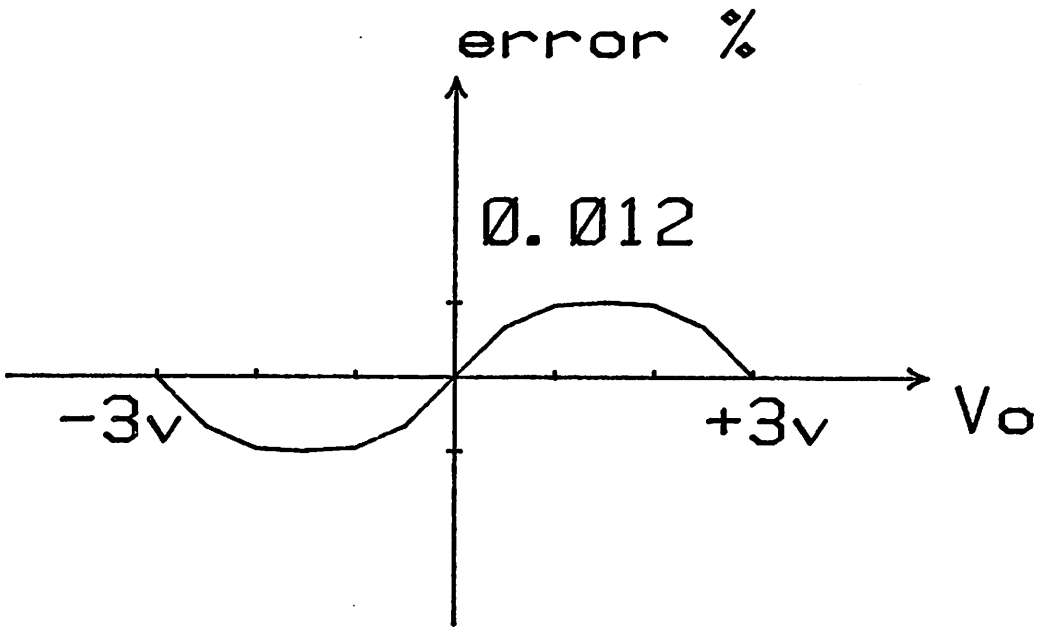


Fig. 12 Measured gain nonlinearity as a function of source resistance

Table 1

Experimental Results, 25 degrees C., +7.5 & -7.5 volts
(15 samples)

Gain accuracy (G=10)		
average value		0.15%
standard deviation		0.03%
Input offset voltage		
average value		1 mV
standard deviation		0.5 mV
Gain linearity		0.01%
Common mode rejection		
DC		120 dB
10kHz		95 dB
Power supply rejection		
pre-amp stage	DC	>95 dB
	1kHz	>95 dB
output stage	DC	95 dB
	1kHz	95 dB
Input range		+4 V, -6 V
Output range		
pre-amp stage		+0.5 V, -0.5 V
output stage		+3 V , -3 V
Acquisition time		8 uS
Equivalent input noise (500kHz BW)		30 uV

Table 1 Summary of experimental results