NOISE LIMITATIONS IN SWITCHED-CAPACITOR FILTERS

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ABSTRACT

Internal noise sources are the fundamental limitation on the achievable dynamic range in switched-capacitor filters. For low frequency applications the flicker noise of the operational amplifier is the dominant noise source, and its contribution increases as device sizes are reduced. The objectives of this research project are the understanding of the noise mechanisms and their contributions in switched-capacitor filters, and the elimination of the flicker noise from the filter by using a chopper stabilization technique. This allows both reduction in the physical size of the filter as well as an improvement in the dynamic range.

A new fully-differential chopper-stabilized filter configuration has been developed which improves both dynamic range and power supply rejection in voiceband filters. An experimental NMOS metal-gate fifth-order Chebyshev lowpass filter has been designed and fabricated. This filter, with a cutoff frequency of 3.4KHz, achieved a dynamic range of 102dB, which is significantly larger than has been previously reported.

ACKNOWLEDGEMENTS

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DEDICATION

My wife, Keh-Nan constantly gave me her love and understanding throughout the duration of my graduate study. Without the many sacrifices she made for me and my two sons, Suo-Hong and Suo-Hwan, this Ph.D work would not have been possible. Keh-Nan should be honored by a PhT, the Push husband Through, degree.

My parents have kept and passed on to me all the good character of the traditional Chinese, and thereby have given me the energy and support necessary to finish my Ph.D work.

I dedicate this dissertation to my wife and my parents.

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Chapter 3 discusses the effect of the operational amplifier output impedance on the wideband noise contribution to the switched-capacitor filter. A comparison between a single-stage amplifier with and without an output voltage buffer are used to examine this effect.

Chapter 4 describes the fundamental limits on dynamic range versus the scaling effect of technological feature size. Two low-frequency noise reduction techniques are discussed. Then the implementation of a modified chopper-stabilized operational amplifier is presented.

In chapter 5, the advantages of using fully-differential circuits in switched-capacitor filters are described. The mismatch problem in a fully-differential switched-capacitor integrator is also described. The circuits of a modified differential chopper-stabilized operational amplifier and a fifth-order lowpass switched-capacitor filter realized by MOS technology are presented.

In chapter 6, some considerations about chip design and measurement are discussed, and the experimental results of the prototype lowpass filter are presented. The noise contribution and the distortion in the filter are also discussed. Two circuits are proposed to convert between single-ended and differential systems.

Chapter 7 summarizes this research work.

In Appendix I, a theoretical noise calculation for the sampled transient thermal noise ($\frac{kT}{C}$ noise) is shown.

Appendix II analyzes the effect of the $\frac{kT}{C}$ noise and its equivalent input referred noise in a switched-capacitor integrator.

Appendix III discusses the square-wave modulation effect for both $\frac{1}{f}$ noise and thermal noise.

Appendix IV describes the process flow of the NMOS metal-gate enhancement-depletion process which was used to fabricate the experimental circuit.

In Appendix V, the layout rules used in chip design are described.

C H A P T E R 2

NOISE IN SWITCHED-CAPACITOR FILTERS

2.1. Noise Sources in Switched-Capacitor Integrator

The most important sources of noise in switched-capacitor filters are the noise of the operational amplifiers in the filters and the thermal noise from the channel resistance of the MOS switches. These noise sources and their effects on switched-capacitor filters will be analyzed from the circuit point of view with a simple bottom-plate switched-capacitor integrator. (The detailed analysis is contained in Appendices I and II.) Before going into the detailed noise analysis, the circuit properties of bottom-plate switched-capacitor integrators will be explained.

A typical differential bottom-plate switched-capacitor integrator with the output sampled on different clock phases is shown in Fig.2.1(a). Here, ϕ_1 and ϕ_2 are two non-overlapping clocks, and transistors M_1 to M_4 and M_5 to M_8 are the MOS switches. C_I is the integrating capacitor, C_{S1},

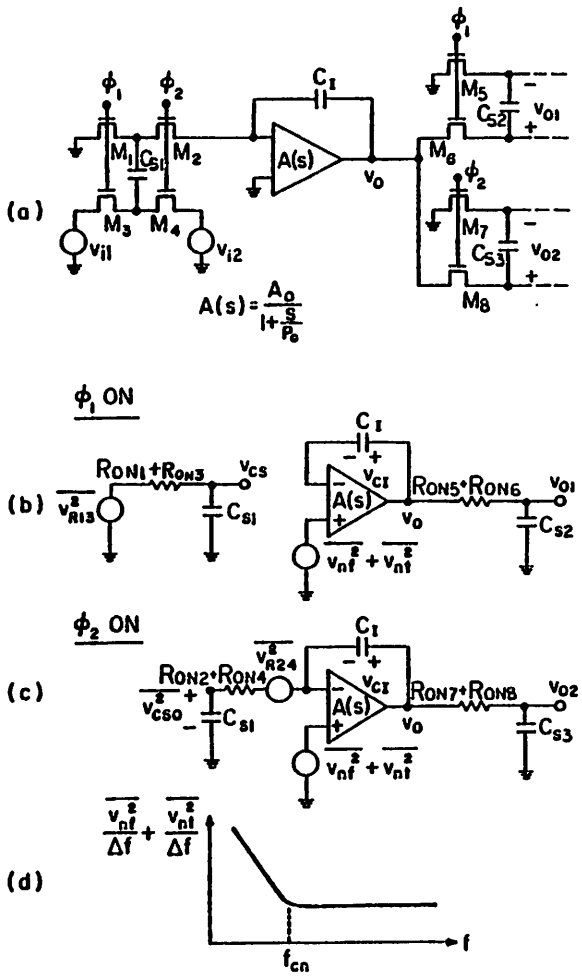


Fig.2.1 Noise in switched-capacitor integrator,
(a) bottom-plate switched-capacitor integrator with output sampled at different clock phase,
(b) ϕ_1 is on, (c) ϕ_2 is on, (d) equivalent input noise of operational amplifier.

C_{S2} and C_{S3} are the sampling capacitors at the input, the output on phase ϕ_1 and the output on phase ϕ_2, respectively. If the charge is transferred completely from C_{S1} to C_I, and to C_{S2} or C_{S3}, the z-transform transfer functions from two inputs to the outputs are

$$v_{o1}(z) = \frac{\frac{C_{S1}}{C_I} z^{-1}}{1-z^{-1}} v_{i1}(z) + \frac{-\frac{C_{S1}}{C_I} z^{-\frac{1}{2}}}{1-z^{-1}} v_{i2}(z) \qquad (2.1a)$$

$$v_{o2}(z) = \frac{\frac{C_{S1}}{C_I} z^{-\frac{1}{2}}}{1-z^{-1}} v_{i1}(z) + \frac{-\frac{C_{S1}}{C_I}}{1-z^{-1}} v_{i2}(z) \qquad (2.1b)$$

where v_{i1} and v_{i2} are the input signals and v_{o1} and v_{o2} are the output signals. The difference in the transfer function between $v_{i1}(z)$ (or $v_{i2}(z)$) and $v_{o1}(z)$ (or $v_{o2}(z)$) is the phase response, i.e. $v_{o1}(z)$ is delayed one half clock cycle relative to $v_{o2}(z)$. This difference has no effect on the noise calculation. Because the power transfer function is the important factor in noise calculation, the equivalent input referred noise at either v_{i1} or v_{i2} from the noise at the output of the integrator is independent of the phase response. Depending on the clock states, the integrator will be in different configurations; namely, the state when clock ϕ_1 is on and that when clock ϕ_2 is on. Therefore, two different circuits and noise analyses for calculating the noise in the integrator are required.

The steps used for noise analysis of switched-capacitor filter in this research work are: (1) calculate the transfer function in a simple switched-capacitor integrator from the noise source to the voltage node(s) of interest; (2) calculate the expected noise value across the capacitors in which the sampled noise charges will be transferred and/or stored in the subsequent clock sequence; (3) calculate the total effective noise at the output of the integrator through the integration function of the circuit; (4) refer the calculated noise back to the input (or if it is convenient, to the output) of the integrator (this is the referred equivalent noise in a switched-capacitor integrator in question.); (5) calculate the transfer functions from each interior node of the filter, where the referred equivalent noise is located, to the output of the filter; and (6) add all the noise powers at the output of the filter by weighting each referred equivalent noise with its own associated power transfer function. A step-by-step analysis of this method will be shown in this chapter.

Notice that in this chapter the thermal noise density used in calculating noise variance and the calculated equivalent wideband noise density are the noise power densities over the range of both positive and negative frequencies. If only the positive frequency range is of interest, such as in noise measurement, all of the wideband noise densities calculated above should have double those values in the positive frequency range and zero elsewhere. As an

example, a resistor of value R will have a noise density of 4kTR if only positive frequency range is considered, while it will have a noise density of 2kTR over the entire frequency spectrum.

Also notice that the noise variance to be calculated is obtained from the integration over the entire frequency range; thus, all of the probabilities of a random variable are considered, and therefore, the aliasing effect of the thermal noise in the sample and hold circuit is included.

In a continuous-time RC integrator, if the operational amplifier is carefully designed so that its noise contribution is negligible, then the dominant fundamental noise in the integrator is the thermal noise from the resistor. Similarly, a fundamental wideband noise can be found in a switched-capacitor integrator. This type of noise (called $\frac{kT}{C}$ noise) will be analyzed first in this chapter.

2.1.1. Sampled Wideband Noise in Switched-Capacitor Circuits ($\frac{kT}{C}$ Noise)

The finite channel resistance of the MOS switches produces a thermal noise which will be sampled by the sampling capacitor through a band-limiting RC network. This type of noise is often referred to as "transient thermal noise". The details are shown in Appendix I [5]. This process can be

described as follows.

When clock ϕ_1 is on, the circuit is shown in Fig. 2.1(b). The total channel resistance of M_1 and M_3 has a thermal noise power density, $\overline{v_{R13}^2}$, which is equal to $2kT(R_{ON1} + R_{ON3})$ through the frequency range from $-\infty$ to $+\infty$. Here k is Boltzmann's constant and T is the absolute temperature. The voltage transfer function from noise source $\overline{v_{R13}^2}$ to the voltage across the sampling capacitor (v_{CS}) is

$$H_1(s) = \frac{v_{CS}(s)}{v_{R13}(s)}\bigg|_{\phi_1 ON}$$

$$= \frac{1}{1 + sR_{ON13}C_{S1}} \qquad (2.2)$$

where $R_{ON13}=R_{ON1} + R_{ON3}$. The expected noise variance across the sampling capacitor C_{S1} is

$$E\left\{v_{CS}^2(t,\omega)\right\} = \int_{-\infty}^{+\infty} 2kTR_{ON13}\left|H_1(j\omega)\right|^2 d\omega$$

$$= \frac{kT}{C_{S1}}. \qquad (2.3)$$

This process is repeated every clock cycle and results in a noise variance of $\frac{kT}{C_{S1}}$ in each sample appearing across the sampling capacitor C_{S1}. This sampled noise is dependent only on the temperature and the size of capacitor, and

therefore, is usually referred to as $\frac{kT}{C}$ noise.

When clock ϕ_2 is on, the circuit is shown in Fig.2.1(c). Charge conservation dictates that the noise sample stored in C_{S1} be transferred and stored in the integrating capacitor C_I. If the DC voltage gain of the operational amplifier is large enough and if the time constant $(R_{ON2} + R_{ON4})C_{S1}$ is smaller than the "on" period of clock ϕ_2, then the stored noise sample has a variance of $(\frac{C_{S1}}{C_I})^2 \frac{kT}{C_{S1}}$. (The details are shown in Appendix II.) Thus, on each ϕ_2 the output of the integrator experiences a change in value whose amplitude has a variance given by $(\frac{C_{S1}}{C_I})^2 \frac{kT}{C_{S1}}$. At the same time, the thermal noise from the channel resistance of M_2 and M_4, $\overline{v_{R24}^2}$ (which has a noise density of $2kT(R_{ON2} + R_{ON4})$), is sampled by C_I through a network consisting of the operational amplifier, the sampling and integrating capacitors, and the switches. The effect of this noise can be simply analyzed as follows: for frequencies below the unity-gain frequency of the amplifier, this noise results in a displacement current which appears across C_I attenuated by a factor of $\frac{C_{S1}}{C_I}$. For frequencies well beyond the operational amplifier unity-gain frequency the output stage of the operational amplifier behaves like an ideal voltage source. This causes the displacement generated by the thermal noise of M_2 and M_4 to flow through C_{S1} and C_I. The detailed effect of this noise can be analyzed as

follows. The voltage transfer function from the noise source $\overline{v_{R24}^2}$ to v_{CI} is

$$H_2(s) = \frac{v_{CI}(s)}{v_{R24}(s)}\bigg|_{\phi_2 ON}$$

$$= \frac{-c\,[s+(1+A_o)P_o]}{c(s+P_o)+(1+sR_{ON24}C_{S1})[s+(1+A_o)P_o]} \qquad (2.4)$$

where $c = \frac{C_{S1}}{C_I}$ is the capacitor ratio which is an intrinsic parameter of a switched-capacitor integrator, and $R_{ON24} = R_{ON2} + R_{ON4}$. The operational amplifier for this analysis is modeled as a single-pole circuit with finite open-loop DC voltage gain A_o and pole frequency at P_o.

Eq.(2.4) contains two poles and one zero. The expected noise variance of $\overline{v_{CI}^2}$ resulting from $\overline{v_{R24}^2}$ is

$$E\left\{v_{CI}^2(t,\omega)\right\} = \int_{-\infty}^{+\infty} 2kTR_{ON24}\left|H_2(j\omega)\right|^2 d\omega$$

$$= c^2 \frac{kT}{C_{S1}}\left[\frac{1 + \frac{(1+A_o)^2 P_o R_{ON24} C_{S1}}{(1+c+A_o)}}{1 + c + (1+A_o)P_o R_{ON24} C_{S1}}\right]. \qquad (2.5)$$

If $A_o >> 1$ and $c << A_o$, then Eq.(2.5) can then be reduced to

$$E\left\{v_{CI}^2(t,\omega)\right\} = c^2 \frac{kT}{C_{S1}}\left[\frac{1 + A_o P_o R_{ON24} C_{S1}}{1 + c + A_o P_o R_{ON24} C_{S1}}\right]. \qquad (2.6)$$

For different value of c, there exists two conditions. Condition (1), $c \ll 1$, which is usually the case of interest in low-frequency filters or in high-Q filters; Condition (2), c is not much less than unity, which is the case when the integrator unity-gain frequency is not much below than the filter clock rate. These two conditions will be discussed separately.

If $c \ll 1$, then Eq.(2.6) results in a simple $\frac{kT}{C}$ noise variance of $c^2 \frac{kT}{C_{S1}}$. This condition can be applied directly to Eq.(2.4) and results in a simplified transfer function $H_3(s)$ of

$$H_3(s) = \frac{-c}{1 + sR_{ON24}C_{S1}} \tag{2.7}$$

which is an one-pole equation as in Eq.(2.2). Therefore, a similar expected noise variance as in Eq.(2.3) is obtained, which is $c^2 \frac{kT}{C_{S1}}$. This noise variance is sampled and stored in C_I when clock ϕ_2 turns off, and gives a similar contribution as the $\frac{kT}{C}$ noise from switches M_1 and M_3. This result disagrees with that of a previously published analysis [6].

If c is not much less than unity, then the sampled noise shown in Eq.(2.6) is less than $c^2 \frac{kT}{C_{S1}}$ which is the channel thermal noise of M_1 and M_3 sampled during ϕ_1 by C_{S1} and transferred to C_I. In this condition the sampled noise shown in Eq.(2.6) is also dependent on the two circuit-

design parameters: the operational amplifier unity-gain frequency and the time constant $R_{ON24}C_{S1}$. For different values of $A_oP_oR_{ON24}C_{S1}$, the noise of Eq.(2.6) can range from $\frac{1}{1+c}$ to 1 of $c^2 \frac{kT}{C_{S1}}$.

Another contribution results from the fact that during the time when M_2 and M_4 are turned on, if M_7 and M_8 turn off before M_2 and M_4, then the instantaneous noise in their channels is translated to the integrator output and is sampled by the sampling capacitor C_{S3}. The noise contribution due to this mechanism can be calculated in the following manner: The voltage transfer function from the noise source v_{R24}^2 to the voltage across the capacitor C_{S3} (v_{o2}) is

$$H_4(s) = \left.\frac{v_{o2}(s)}{v_{R24}(s)}\right|_{\phi_2 ON}$$

$$= \frac{\frac{-c}{1 + sR_{ON78}C_{S3}}}{(1 + sR_{ON24}C_{S1})(1 + \frac{s}{A_oP_o}) + s\frac{c}{A_oP_o}} \tag{2.8}$$

where $R_{ON78} = R_{ON7} + R_{ON8}$. The associated expected noise variance sampled by C_{S3}, if M_7 and M_8 turn off before M_2 and M_4, is

$$E\left\{v_{o2}^2(t,w)\right\} = \int_{-\infty}^{+\infty} 2kTR_{ON24}\left|H_4(jw)\right|^2 dw$$

$$= c^2 \frac{kT}{C_{S1}} K_A \tag{2.9}$$

where

$$K_A^{-1} = 1 + \frac{1 + c}{A_o P_o R_{ON24} C_{S1}} + \frac{R_{ON78} C_{S3}}{R_{ON24} C_{S1}} \left[1 + \frac{\frac{R_{ON24} C_{S1}}{R_{ON78} C_{S3}}}{1 + c + A_o P_o R_{ON24} C_{S1}} \right]^{-1} . \quad (2.10)$$

The magnitude of the coefficient K_A is dependent on the circuit parameters $A_o P_o$, $R_{ON24} C_{S1}$ and $R_{ON78} C_{S3}$, and is always less than 1. This noise is important only when the output of the integrator is sampled by a sample and hold circuit. The noise in Eq.(2.9) has a similar form as the $\frac{kT}{C}$ noise sampled in C_{S3} from the channel resistance of M_7 and M_8 (which is $\frac{kT}{C_{S3}}$). If C_{S3} is considered as an input sampling capacitor of the next stage, then the noise in Eq.(2.9) can be seen as a part of the equivalent input noise of the next stage. Therefore, if $c^2 K_A \frac{C_{S3}}{C_{S1}} << 1$, then the noise contribution due to this mechanism can be neglected; otherwise, it should be included in the noise calculation of the next stage.

For the case of $c << 1$, the integrator output consists of a series of samples whose variance is $\frac{2kT}{C_{S1}} \left(\frac{C_{S1}}{C_I}\right)^2$. In Appendix II, the spectrum of this waveform is calculated, and it is shown that the equivalent input $\frac{kT}{C}$ noise power spectral density of the switched-capacitor integrator far

below the clock rate is $\frac{2kT}{C_{S1} f_C}$ or $2kTR_{SCR}$ over the range of both positive and negative frequencies. Here $R_{SCR} (= \frac{1}{C_{S1} f_C})$ is the equivalent "switched-capacitor resistance", and f_C is the clock frequency. Compared with the thermal noise density of a resistor used in a continuous-time RC integrator ($2kTR$), the $\frac{kT}{C}$ noise power density at low frequencies is equal to that of the resistor case. Direct experimental verification has recently been published [7].

The equivalent input $\frac{kT}{C}$ noise power density for frequencies not far below the clock rate (f_C) has a $\frac{\sin^2 x}{x^2}$ shape as shown in Eq.(A.17). From the properties of an ergodic process [9], there is an interesting result from Eq.(A.17). The total average $\frac{kT}{C}$ noise power (P) at the input of the integrator due to M_1 and M_3 channel thermal noise is equal to the power in the time-varying AC component (the noise variance). This can be proven by integrating Eq.(A.17) over the entire frequency range.

$$P = \int_{-\infty}^{+\infty} S_i(\omega) d\omega$$

$$= \frac{kT}{C_{S1} f_C} \int_{-\infty}^{+\infty} \frac{\sin^2 \frac{\omega T_C}{2}}{\left(\frac{\omega T_C}{2}\right)^2} d\omega$$

$$= \frac{kT}{C_{S1}} . \quad (2.11)$$

This result also supports the assumption in Eq.(A.8) that the mean of the thermal noise v_{R13} is zero (so that the DC noise power component is zero). Therefore, the noise variance (or the total noise power) of $\frac{2kT}{C_{S1}}$ at the input of the switched-capacitor integrator shown in Fig.2.1 is a fundamental noise power which is only a function of the temperature and the size of the sampling capacitor.

2.1.2. Operational Amplifier Flicker Noise (or $\frac{1}{f}$ Noise) ($\overline{v_{nf}^2}$)

Fig.2.1(d) shows a typical equivalent input noise spectrum of an MOS operational amplifier. The corner frequency (f_{cn}) is on the order of 10 kHz to 1 MHz, and is process dependent. This low frequency noise (flicker noise or $\frac{1}{f}$ noise) results primarily from the surface states in the input stage transistors of the operational amplifier. Because the power spectrum of the $\frac{1}{f}$ noise is highly correlated at low frequencies, if the clock frequency is higher than twice the corner frequency ($2f_{cn}$), then the $\frac{1}{f}$ noise can be treated as a narrow-band noise. The same method used in the signal analysis can be applied. The reason for choosing $2f_{cn}$ as a Nyquist frequency of the $\frac{1}{f}$ noise is that for frequencies beyond the corner frequency the $\frac{1}{f}$ noise density is much less than the wideband noise density in the operational amplifier; therefore, when compared with the wideband noise

power, most of the $\frac{1}{f}$ noise power is concentrated at frequencies below f_{cn}. The following analysis is based on this assumption. From Fig.2.1, the recurrence relationships between v_{o1}, v_{o2} and v_{nf} are

$$v_{o1}[(n+1)T_C] - v_{o1}[nT_C]$$

$$= v_{nf}[(n+1)T_C] - v_{nf}[nT_C] + cv_{nf}[(n+\tfrac{1}{2})T_C] \quad (2.12a)$$

$$v_{o2}[(n+1)T_C] - v_{o2}[nT_C]$$

$$= v_{nf}[(n+1)T_C] - v_{nf}[nT_C] + cv_{nf}[(n+1)]T_C] \quad (2.12b)$$

where T_C is the period of the clock f_C. Eqs.(2.12a) and (2.12b) correspond to z-transform functions of

$$v_{o1}(z) = v_{nf}(z) + \frac{cz^{-\frac{1}{2}}}{1-z^{-1}} v_{nf}(z) \quad (2.13a)$$

$$v_{o2}(z) = v_{nf}(z) + \frac{c}{1-z^{-1}} v_{nf}(z) \quad (2.13b)$$

which correspond to the power transfer functions of

$$\frac{S_{of1}(\omega)}{S_{nf}(\omega)} = \left| \frac{v_{o1}(e^{j\omega T_C})}{v_{nf}(e^{j\omega T_C})} \right|^2$$

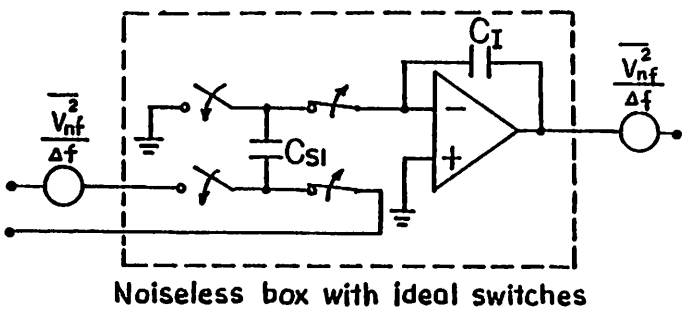
$$= 1 + \frac{c^2}{4\sin^2 \frac{uf_C}{2}} \qquad (2.14a)$$

$$\frac{S_{of2}(u)}{S_{nf}(u)} = \left| \frac{v_{o2}(e^{juf_C})}{v_{nf}(e^{juf_C})} \right|^2$$

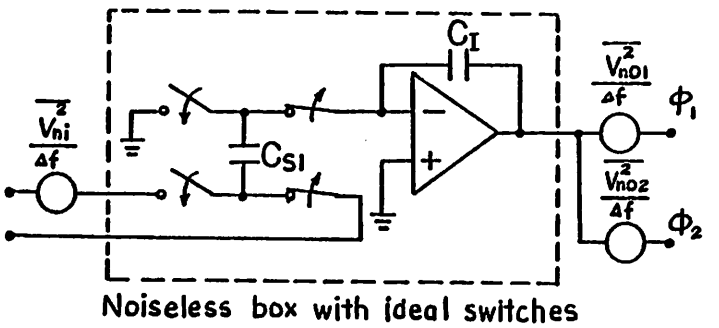
$$= 1 + \frac{c^2}{4\sin^2 \frac{uf_C}{2}} + c. \qquad (2.14b)$$

The integrator output contains two separate components which are related to the $\frac{1}{f}$ noise of the operational amplifier. The first component (the "unity-gain" component), corresponding to the first terms of Eqs.(2.14), is simply a translated replica of the $\frac{1}{f}$ noise. The second (the "integration" component), corresponding to the second terms of Eqs.(2.14), is the $\frac{1}{f}$ noise multiplied by the integrator transfer function. The third term "c" of Eq.(2.14b) is due to the correlation between the "unity-gain" and the "integration" components. This term is negligible when $c \ll 1$.

The $\frac{1}{f}$ noise of the operational amplifier can be modeled as a noise source of value $\overline{v_{nf}^2}$ at the input of the integrator (input referred from the "integrated" component) and a second noise source of value $\overline{v_{nf}^2}$ or $(1+c)\overline{v_{nf}^2}$ at the output (the "translated" component). These noise components are shown in Fig.2.2(a).



(a)



(b)

Fig.2.2 Equivalent noise components for (a) $\frac{1}{f}$ noise, (b) total noise of a switched-capacitor integrator.

2.1.3. Operational Amplifier Wideband Noise ($\overline{v_{nt}^2}$)

The wideband thermal noise of the operational amplifier can not be analyzed by the method described in the $\frac{1}{f}$ noise analysis. This thermal noise (v_{nt}) in the switched-capacitor integrator is a non-stationary random process since the circuit with clock ϕ_1 on is not in the same state as with clock ϕ_2 on. A similar analysis for calculating the thermal noise resulting from switches M_2 and M_4 can be used.

From Fig.2.1 the noise sampled by C_I from $\overline{v_{nt}^2}$ in the sampling sequence has a similar integration function as the integrated $\frac{kT}{C}$ noise described in Appendix II. The detailed analysis is as follows. If the operational amplifier has an infinite input impedance or if the parasitic capacitance across two input nodes of the operational amplifier is much smaller than the integrator capacitance C_I, then the noise sampled by C_1 during clock ϕ_1 on can be neglected as compared with the noise sampled with clock ϕ_2 on. When clock ϕ_2 is on, the circuit state is changed and the voltage transfer function from v_{nt} to v_{CI} becomes

$$\left.\frac{v_{CI}(s)}{v_{nt}(s)}\right|_{\phi_2 ON} = c\left\{(1+\tfrac{1+c}{A_o}) + s\left[(1+\tfrac{1}{A_o})R_{ON24}C_{S1} + \tfrac{1+c}{A_oP_o}\right] + s^2\,\tfrac{R_{ON24}C_{S1}}{A_oP_o}\right\}^{-1} \qquad (2.15)$$

In the usual case, $A_o >> 1$ and $\frac{c}{A_o} << 1$, Eq.(2.15) becomes

$$\left.\frac{v_{CI}(s)}{v_{nt}(s)}\right|_{\phi_2 ON} = H_5(s) = \frac{c}{(1+sR_{ON24}C_{S1})(1+\frac{s}{A_oP_o}) + s\,\frac{c}{A_oP_o}} \qquad (2.16)$$

and the expected noise variance sampled by C_I from $\overline{v_{nt}^2}$ is

$$E\left\{v_{CI}^2(t,u)\right\} = \int_{-\infty}^{+\infty} 2kTR_{teq}\left|H_5(ju)\right|^2 du = kTR_{teq}\,\frac{c^2}{R_{ON24}C_{S1} + \frac{1+c}{A_oP_o}} \qquad (2.17)$$

where $2kTR_{teq}$ is the equivalent input thermal noise density of the operational amplifier with equivalent thermal resistance R_{teq}. The band-limiting factor in Eq.(2.17) is determined by the smaller bandwidth of $\frac{1}{R_{ON24}C_{S1}}$ and $\frac{A_oP_o}{1+c}$. If $\frac{1}{R_{ON24}C_{S1}}$ is dominant, then the expected noise variance is

$$E\left\{v_{CI}^2(t,u)\right\} = c^2\,\frac{kT}{C_{S1}}\,\frac{R_{teq}}{R_{ON24}} \qquad (2.18)$$

which, in fact, is one type of $\frac{kT}{C}$ noise. This noise variance will be sampled and stored by C_I in every clock cycle after clock ϕ_2 turns off. Thus, the noise analysis shown in

Appendix II can be applied and results in a noise power density at the input of this switched-capacitor integrator of $\frac{kT}{C_{S1}f_C}\frac{R_{teq}}{R_{ON24}}$, over both positive and negative frequencies. In some applications the operational amplifier has a narrow-band design (i.e. $A_oP_o << \frac{1}{R_{ON24}C_{S1}}$). In such a case the noise sampled by C_I from v_{nt}^2 is

$$E\left\{v_{CI}^2(t,\omega)\right\} = c^2\, kTR_{teq}A_oP_o \qquad (2.19)$$

and the equivalent input noise density due to this "integrated" $\overline{v_{nt}^2}$ noise is equal to $kTR_{teq}\frac{A_oP_o}{f_C}$ over both positive and negative frequencies. This is the wideband noise density of the operational amplifier ($2kTR_{teq}$) multiplied by the effective number of aliasing ($\frac{A_oP_o}{2f_C}$).

The above analysis considered only the "integrated" noise from v_{nt} to v_{CI}. Moreover, when clock ϕ_1 is on, the thermal noise v_{nt}^2 will be sampled through the operational amplifier by the sampling capacitor C_{S2} of the next stage, and when clock ϕ_2 is on, $\overline{v_{nt}^2}$ will be sampled by C_{S3} as well. These noise samples are due to the "translation" characteristic of the circuit. That is, if the operational amplifier is connected by the feedback network as a non-inverting amplifier, the transfer function from the non-inverting input to the output of the operational amplifier is one plus the impedance ratio of the external feedback

circuits.

When clock ϕ_1 is on, the voltage transfer function from v_{nt} to the voltage across the capacitor C_{S2} (v_{o1}) is

$$\left.\frac{v_{o1}(s)}{v_{nt}(s)}\right|_{\phi_1 ON} = \frac{1}{[(1+\frac{1}{A_o}) + \frac{s}{A_oP_o}](1 + sR_{ON56}C_{S2})} \qquad (2.20)$$

where $R_{ON56} = R_{ON5} + R_{ON6}$. The noise variance sampled by C_{S2} is

$$E\left\{v_{o1}^2(t,\omega)\right\} = kTR_{teq}\frac{1}{R_{ON56}C_{S2} + \frac{1}{A_oP_o}}. \qquad (2.21)$$

This result shows that the voltage transfer functions of Eq.(2.16) and Eq.(2.20) have similar band-limiting effect on the wideband noise of the operational amplifier.

The same discussion as in Eq.(2.17) gives the result that the equivalent noise, over both positive and negative frequencies at the input of the next stage is equal to

$$\frac{kT}{C_{S2}}\frac{R_{teq}}{R_{ON56}} \quad \text{if} \quad \frac{1}{R_{ON56}C_{S2}} << A_oP_o, \qquad (2.22)$$

and

$$kTR_{teq}A_oP_o \quad \text{if} \quad A_oP_o << \frac{1}{R_{ON56}C_{S2}}. \qquad (2.23)$$

When clock ϕ_2 is on, and if $A_o >> 1$ and $\frac{c}{A_o} << 1$, the noise (v_{nt}) translated to the capacitor C_{S3} has the following transfer function

$$\left.\frac{v_{o2}(s)}{v_{nt}(s)}\right|_{\phi_1 ON} = \frac{H_5(s)}{c}\,\frac{(1+c) + sR_{ON24}C_{S1}}{1 + sR_{ON78}C_{S3}} \qquad (2.24)$$

where $R_{ON78} = R_{ON7} + R_{ON8}$. The noise variance sampled by C_{S3} is

$$E\left\{v_{o2}^2(t,w)\right\} = kTR_{teq}\,\frac{(1+c)^2}{R_{ON78}C_{S3} + \frac{1+c}{A_oP_o}}\,K_B \qquad (2.25)$$

where

$$K_B^{-1} = 1 + \frac{c\left[1 + \frac{1}{1+c}\,\frac{t_1}{t_3}\left(1 + \frac{c+2}{c+1}\,A_oP_o t_3\right)\right]}{(A_oP_o + \frac{1+c}{t_3})\left[t_3 + \frac{t_1}{(1+c)^2} + \frac{1+(1+c)\frac{t_3}{t_1}}{A_oP_o}\right]}, \qquad (2.26)$$

$t_1 = R_{ON24}C_{S1}$, and $t_3 = R_{ON78}C_{S3}$. The magnitude of the coefficient K_B is dependent on the parameters A_oP_o, $R_{ON24}C_{S1}$ and $R_{ON78}C_{S3}$, and is always less than 1. If $c << 1$, the noise variance becomes

$$E\left\{v_{o2}^2(t,w)\right\} = kTR_{teq}\,\frac{1}{R_{ON78}C_{S3} + \frac{1}{A_oP_o}}. \qquad (2.27)$$

Again, this result is similar to the result in Eq.(2.17) or Eq.(2.21). They are all band-limited by the resistance and capacitance of the switches and the unity-gain frequency of the operational amplifier. From the analysis shown in Appendix II, the translated wideband noise of the operational amplifier contributes an equivalent noise density of $\frac{kTR_{teq}}{f_C}\,\frac{1}{R_{ON78}C_{S3} + \frac{1}{A_oP_o}}$ (over both positive and negative frequencies) into the input of the next stage when clock ϕ_2 is on.

2.1.4. Summary

If the frequencies of interest are much lower than the clock frequency f_C, the DC voltage gain of the operational amplifier is large, the $(R_{ON2}+R_{ON4})C_{S1}$ time constant is much smaller than the turned-on period of switches M_2 and M_4, the leakage in the integrating capacitor can be neglected and $\frac{C_{S1}}{C_I}(=c) << 1$, then the noise can be represented by two sources, one at the input and another at the output. The input noise density is

$$\frac{\overline{v_{ni}^2}}{\Delta f} = \frac{2kT}{C_{S1}f_C} + \frac{kTR_{teq}}{\left[R_{ON24}C_{S1} + \frac{1}{A_oP_o}\right]f_C} + \frac{\overline{v_{nf}^2}}{\Delta f} \qquad (2.28)$$

and the noise density "translated" to the output node of the integrator and sampled by C_{S2} and C_{S3} are

$$\frac{\overline{v_{no1}^2}}{\Delta f} = \frac{kTR_{teq}}{\left[R_{ON56}C_{S2} + \frac{1}{A_oP_o}\right]f_C} + \frac{\overline{v_{nf}^2}}{\Delta f} \qquad (2.29)$$

and

$$\frac{\overline{v_{no2}^2}}{\Delta f} = \frac{kTR_{teq}}{\left[R_{ON78}C_{S3} + \frac{1}{A_oP_o}\right]f_C} + \frac{\overline{v_{nf}^2}}{\Delta f}, \qquad (2.30)$$

respectively, where R_{teq} is the equivalent resistance of the input referred thermal noise of the operational amplifier. These equivalent noises are illustrated in Fig.2.2(b).

In a ladder filter structure as shown in Fig.2.3 the integrator A has a differential input sampling capacitor with two inputs being sampled from two other integrators' outputs. The sampling capacitor C_{SA} will sample the two "translated" operational amplifier wideband noise components (the first terms in Eqs.(2.29) and (2.30)) and the two "translated" $\frac{1}{f}$ noise components (the second terms in Eqs.(2.29) and (2.30)) from integrators I and II and will integrate these noise components into the integrating capacitor C_{IA}. If $\frac{1}{A_oP_o}$ is much smaller than the time constants of the switched-capacitors in Fig.2.3 (i.e. $R_{ON24}C_{S1}$, $R_{ON56}C_{S2}$ and $R_{ON78}C_{S3}$ are much larger than $\frac{1}{A_oP_o}$

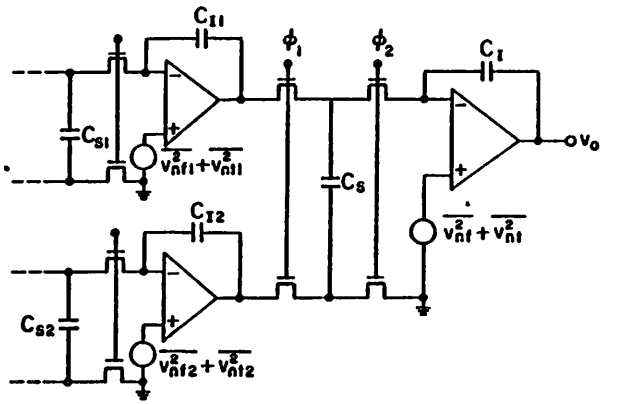


Fig.2.3 Noise in a differential switched-capacitor integrator.

in Eqs.(2.28), (2.29) and (2.30)) and the operational amplifiers have the same thermal noise density ($2kTR_{teq}'$), then the total equivalent This integration results in an effective $\frac{1}{f}$ noise power of $3\ \overline{v_{nf}^2}$ (in Eq.(2.14a) case) or $[\ 3 + (\frac{C_{S1}}{C_{I1}}) + (\frac{C_{S2}}{C_{I2}})]\overline{v_{nf}^2}$ (in Eq.(2.14b) case) at the input of this integrator, assuming these three operational amplifiers have the same $\frac{1}{f}$ noise density.

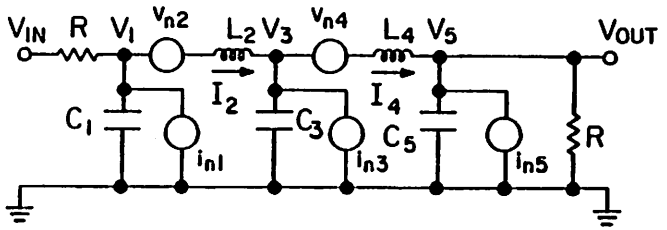
2.2. Noise Calculation in Switched-Capacitor Filters

The steps used for calculating the noise in switched-capacitor filters are described in the previous section. The steps which have been used up to the point of calculating the equivalent input referred and translated output noise components in a switched-capacitor integrator are shown in Sections 2.1.1. to 2.1.3.. The rest of steps will be shown in this section.

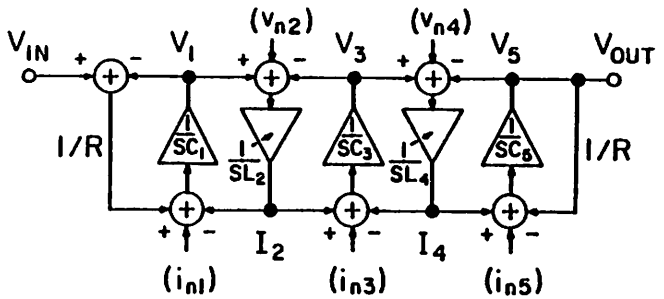
2.2.1. Equivalent Noise Sources in Switched-Capacitor Filters

In order to calculate the total noise at the output of a switched-capacitor filter, the noise sources or the equivalent noise components inside the filter must be weighed by their own transfer functions. In a RLC passive filter the transfer functions from a voltage source in series with an inductance element or a current source in parallel with a capacitance element to the output of the filter can be easily found by a circuit simulation program such as SPICE. To design an active filter one can translate the passive filter structure into a signal flow graph with the energy storage elements replaced by the integrators. By doing this the voltage sources in series with the inductors and the current sources in parallel with the capacitors become the inputs to these integrators. This translation is explained by an example of a fifth order ladder lowpass filter shown in Fig.2.4(a). In this figure the v_n's and i_n's are the equivalent noise sources of the associated energy storage elements simulated by the active circuits, not the noise sources in these passive elements.

From Fig.2.4, the reason for analyzing the noise components in a switched-capacitor integrator and referring them into the input and the output of the integrator is clear. For example, the total equivalent noise power at the input node of the integrator $\frac{1}{sC_3}$ is the sum of its input referred noise (Eq.(2.28)) and two translated noise components (Eq.(2.29) or Eq.(2.30)) from two adjacent stages $\frac{1}{sL_2}$ and $\frac{1}{sL_4}$. This condition also occurs in the



(a)



(b)

Fig.2.4 Noise calculation in the filter,
(a) a fifth-order Chebyshev lowpass filter,
(b) signal flow graph of (a).

two terminated stages ($\frac{1}{sC_1}$ and $\frac{1}{sC_5}$). The total equivalent input noise power at the input of the integrator $\frac{1}{sC_1}$ (or $\frac{1}{sC_5}$) is equal to the input referred noise of the terminated stage itself plus the translated output noise components from the integrator $\frac{1}{sC_1}$ (or $\frac{1}{sC_5}$) and the inner integrator ($\frac{1}{sL_2}$ or $\frac{1}{sL_4}$). This evidence also explains the fact of three noise power discussed in Section 2.1.4..

2.2.2. Filter Noise Calculation -- An Example

A 5-th order Chebyshev lowpass filter shown in Fig.2.4(a) and 2.4(b) will be used as an example for noise calculation. In Fig.2.4(b) the voltage transfer functions from each noise source at the input of the integrator to the output of the filter are shown in Fig.2.5. The basic relationship between the input and the output noise spectrum in a network with a transfer function of $H_n(j\omega)$ is

$$S_{no}(\omega) = S_{ni}(\omega)|H_n(j\omega)|^2 \qquad (2.31)$$

where $|H_n(j\omega)|^2$ is the power transfer function from the noise source to the output of the network. The total output noise power spectrum of the filter shown in Fig.2.4 is

$$S_{noT}(\omega) = \sum_{m=1}^{5} S_{nim}(\omega)|H_{nm}(j\omega)|^2 + S_{no5}(\omega) \qquad (2.32)$$

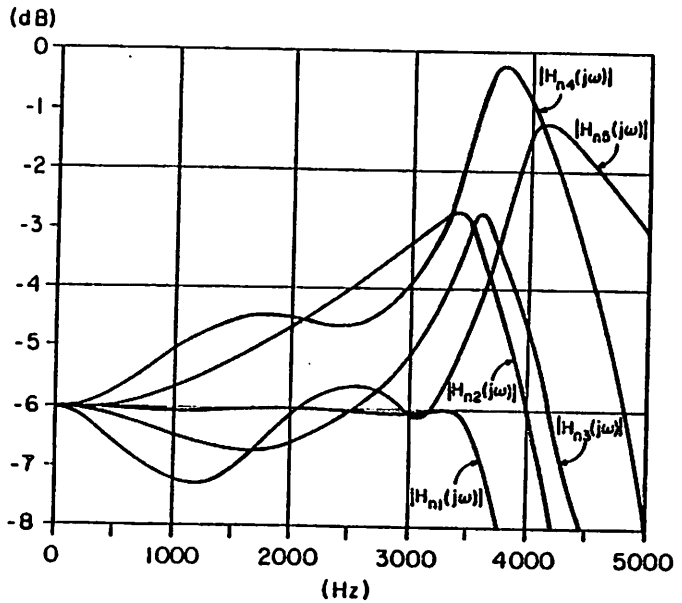


Fig.2.5 Noise transfer functions in the filter of Fig.2.4.

where $S_{nim}(\omega)$ is the total equivalent noise power density at the input node of the m-th integrator which includes the input referred noise components of the present stage (Eq.(2.28)), and the "translated" noise components from the outputs of the adjacent integrators (as in Eq.(2.29) and Eq.(2.30)); $H_{nm}(j\omega)$ is the voltage transfer function from the input of the m-th integrator to the output of the filter; and $S_{no5}(\omega)$ is the "translated" noise from the noise sources of the 5-th integrator appearing at the output of that stage (also the output of the filter).

It is assumed that the noise sources in the filter are uncorrelated so that a simple noise power summation as Eq.(2.32) can be performed.

CHAPTER 3

EFFECT OF OPERATIONAL AMPLIFIER OUTPUT IMPEDANCE IN NOISE ANALYSIS

The noise analysis shown in Chapter 2 is based on the assumption that the operational amplifier is modeled as a single-pole network with a finite open-loop voltage gain A_o. This type of network is an ideal voltage-to-voltage converter which depends only on the relationship of $\frac{A_o}{1 + \frac{s}{P_o}}$ between the input and the output nodes of the network. In other words, the output node of the network sees zero impedance; thus, the amplifier contributes no band-limiting effect in the calculation of the noise variance sampled by the sampling capacitor of the next stage. In Chapter 2 when calculating the translated noise from the operational amplifier to the sampling capacitor of the next stage (C_{S2} or C_{S3}), the band-limiting factors for the wideband noise were the unity-gain frequency of the operational amplifier and the pole formed by the channel resistance and the sampling capacitance of the next sampling switched-capacitor. However, in calculating the noise contribution to C_{S2} (or C_{S3}) from the thermal noise of the channel resistance of

the next stage (R_{ON56} or R_{ON78}), the band-limiting mechanism is only in the channel resistance and sampling capacitance of that switched-capacitor. This results in a simple noise sample of $\frac{kT}{C_S}$ to that stage. This may not be true when the amplifier is designed without output stage, as in a transconductance amplifier. This chapter will only analyze the effect of the operational amplifier output impedance in noise calculation with clock ϕ_1 on. The noise contribution in different amplifier configurations such as a single-stage amplifier with and without the output stage will be discussed.

3.1. A Single-Stage Amplifier

In order to understand the effect of the operational amplifier output impedance in the noise calculation of the sampling switched-capacitor connected to the output of the amplifier, a single-stage amplifier shown in Fig.3.1(a) is used. In Fig.3.1, C_I is the integrating capacitor, C_p is the parasitic capacitance at the input node of the amplifier, M_L and C_{SL} are the sampling switch and capacitor of the load stage respectively, G_m is the effective transconductance of the amplifier, R_o and C_o are the resistance and capacitance at the output node, and $\overline{v_{eq1}^2}$ ($=2kTR_{teq1}\Delta f$) is the equivalent input wideband noise of the amplifier.

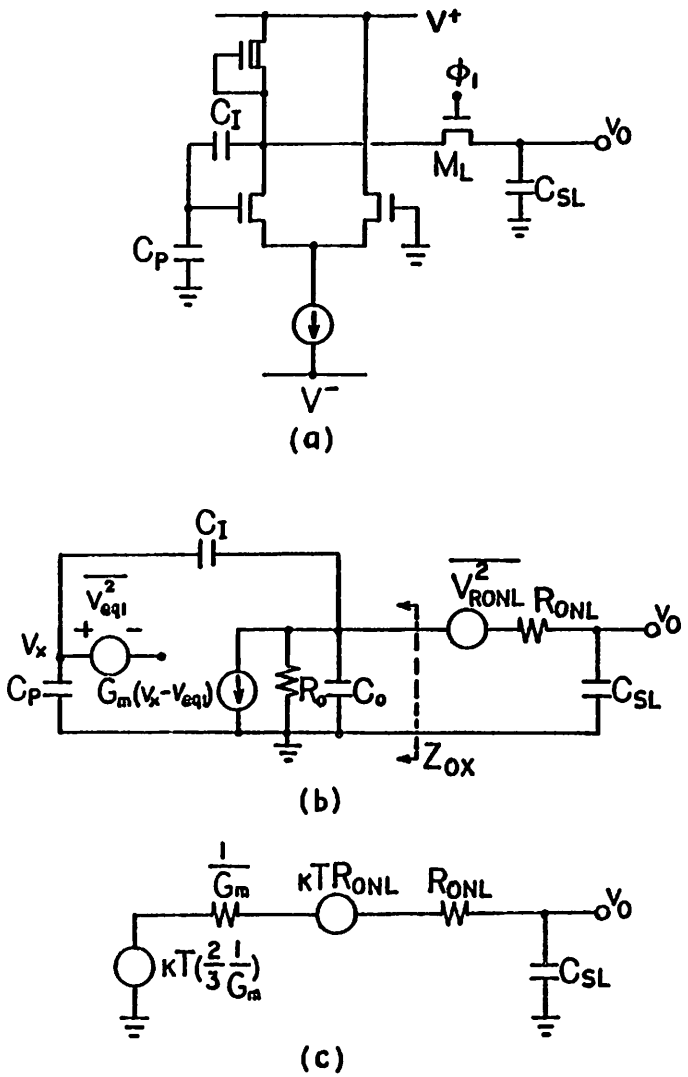


Fig.3.1 (a) A single-stage amplifier with output sampling switched-capacitor, (b) small-signal model of (a), (c) equivalent circuit for b=1 and $C_{ot} \ll C_{SL}$.

The voltage transfer function from the equivalent input wideband noise of the amplifier to the voltage across C_{SL} is

$$\frac{v_o(s)}{V_{eq1}(s)} = \frac{\frac{1}{b}}{1 + s(t_L + \frac{C_{ot} + C_{SL}}{bG_m}) + s^2 \frac{t_L C_{ot}}{G_m}} \tag{3.1}$$

where $b = \frac{C_I}{C_I + C_p}$, $C_{ot} = bC_p + C_o$, and $t_L = R_{ONL}C_{SL}$. The noise variance sampled by C_{SL} from $\overline{v_{eq1}^2}$ is

$$E\left\{v_o^2(t,u)\right\}_1 = kTR_{teq1} \frac{(\frac{1}{b})^2}{R_{ONL}C_{SL} + \frac{C_{ot} + C_{SL}}{bG_m}}. \tag{3.2}$$

The output impedance of the amplifier when it is connected as an integrator is

$$Z_{ox} = \frac{1}{(\frac{1}{R_o} + bG_m) + sC_{ot}}. \tag{3.3}$$

In the usual case $bG_mR_o \gg 1$, the voltage transfer function from V_{RONL} to v_o is

$$\frac{v_o(s)}{v_{RONL}(s)} = \frac{1 + s\frac{C_{ot}}{bG_m}}{1 + s(t_L + \frac{C_{ot} + C_{SL}}{bG_m}) + s^2 \frac{t_L C_{ot}}{bG_m}} \tag{3.4}$$

and the associated noise variance sampled by C_{SL} from the

noise source $\overline{v_{RONL}^2}$ is

$$E\left\{v_o^2(t,\omega)\right\}_2 = kTR_{ONL}\frac{1+\frac{C_{ot}}{bG_m t_L}}{R_{ONL}C_{SL}+\frac{C_{ot}+C_{SL}}{bG_m}}. \qquad (3.5)$$

The total noise variance sampled by C_{SL} from $\overline{v_{eq1}^2}$ and $\overline{v_{RONL}^2}$ is then equal to

$$\overline{v_o^2}\Big|_{tot} = kT\frac{\left[\frac{R_{teq1}}{b^2}+R_{ONL}\left(1+\frac{C_{ot}}{bG_m R_{ONL}C_{SL}}\right)\right]}{R_{ONL}C_{SL}+\frac{C_{ot}+C_{SL}}{bG_m}}. \qquad (3.6)$$

If $C_p \ll C_I$, "b" approaches unity, and $\overline{v_o^2}\Big|_{tot}$ is equal to

$$\frac{kTR_{teq1}}{R_{ONL}C_{SL}+\frac{C_{ot}+C_{SL}}{bG_m}}+\frac{kT}{C_{SL}}\left[\frac{1}{1+\frac{1}{G_m R_{ONL}+\frac{C_{ot}}{C_{SL}}}}\right] \qquad (3.7)$$

Comparing the first term with Eq.(2.21), it can be seen that the difference is the band-limiting factor in the unity-gain frequency of the amplifier. From Fig.3.1(b) the open-loop voltage gain and the pole of the amplifier are $A_o = G_m R_o$ and $P_o = \frac{1}{R_o C_o}$ respectively, which result in an unity-gain frequency of $\frac{G_m}{C_o}$. This is the same case as that

of considering the amplifier having an ideal voltage buffer at its output such that the capacitance load (C_{SL} and bC_p) will not affect the intrinsic unity-gain frequency of the amplifier. The non-ideal output impedance reduces the "effective" unity-gain frequency ($\frac{G_m}{C_{ot}+C_{SL}}$) and the amount of the noise to be sampled by C_{SL} from $\overline{v_{eq1}^2}$. The second term of Eq.(3.7) shows that the finite output impedance (due to finite G_m and C_{ot}) of the amplifier also has the effect of reducing the amount of the $\frac{kT}{C}$ noise to be sampled by C_{SL} from the channel resistance of the switch M_L. The net effect can be seen as follows.

Because the equivalent noise resistance of the amplifier R_{teq1} is approximately equal to $\frac{2}{3}\frac{1}{G_m}$, an interesting result occurs when $b\left(=\frac{C_I}{C_I+C_p}\right) = \frac{2}{3}$. Substituting this value into Eq.(3.6), $\overline{v_o^2}\Big|_{tot}$ becomes $\frac{kT}{C_{SL}}$. The capacitance ratio "b" is the feedback factor in the circuit configuration of Fig.3.1. For different values of b, $\overline{v_o^2}\Big|_{tot}$ becomes

$$\overline{v_o^2}\Big|_{tot} > \frac{kT}{C_{SL}} \qquad \text{if } b < \frac{2}{3} \qquad (3.8a)$$

$$\overline{v_o^2}\Big|_{tot} < \frac{kT}{C_{SL}} \qquad \text{if } \frac{2}{3} < b < 1. \qquad (3.8b)$$

Eq.(3.8b) is normally valid in switched-capacitor filters. It is fortunate that the amplifier with finite output impedance as shown in Fig.3.1(a) will not only reduce the

amount of the amplifier wideband noise sampled by C_{SL}, but will also make the total noise to be sampled by C_{SL} even less than the fundamental $\frac{kT}{C}$ noise in a simple switched-capacitor ($\frac{kT}{C_{SL}}$), assuming the condition $\frac{2}{3} < b < 1$ is satisfied. The minimum total noise variance ($\overline{v_o^2}|_{tot}$) that can be achieved is with b=1, $C_{ot} << C_{SL}$ and $R_{ONL} << \frac{1}{G_m}$. These conditions will result in a value of $\frac{2}{3}\frac{kT}{C_{SL}}$. The equivalent noise circuit for b=1 and $C_{ot} << C_{SL}$ is shown in Fig.3.1(c), from which one can see the factor of $\frac{2}{3}$ is from the difference between the equivalent noise resistance ($\frac{2}{3}\frac{1}{G_m}$) and the transconductance (G_m) of the MOS device. In the circuit configuration of Fig.3.1(a), if $bG_mR_o >> 1$ and $bG_m >> |sC_{ot}|$ in the frequency range of interest, the output impedance from Eq.(3.3) is equal to one over the transconductance of the circuit ($Z_{ox} \simeq \frac{1}{G_m}$). This $\frac{1}{G_m}$ is also the output impedance of an MOS transistor when it is connected as a "diode".

3.2. A Single-Stage Amplifier with Output Source Follower

A single-stage amplifier with a source follower output stage is shown in Fig.3.2(a). The small signal model for the noise calculation is shown in Fig.3.2(b), where R_{o1} and C_{o1} are the total resistance and capacitance at node V_1, R_{o2} is the resistance associated with the output current source,

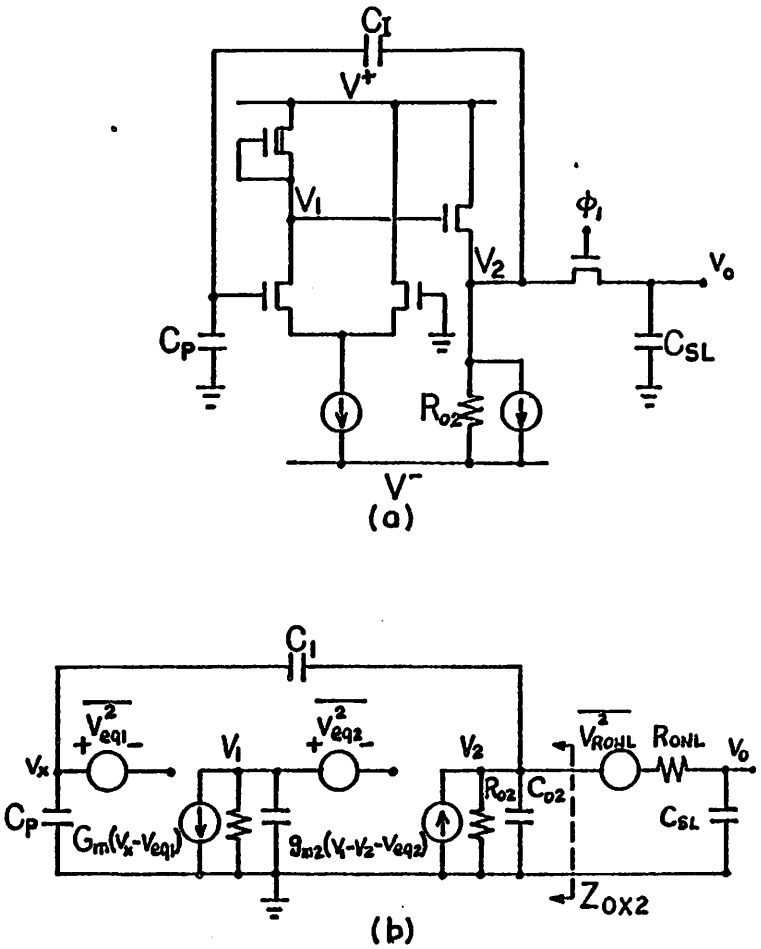


Fig. 3.2 (a) A single-stage amplifier with an output source follower, (b) small-signal model for noise calculation of circuit (a).

C_{o2} is the total capacitance at node V_2, $\overline{v_{eq1}^2}$ and $\overline{v_{eq2}^2}$ are the equivalent input noise of the gain stage and the source follower respectively, and G_m and g_{m2} are the effective transconductance of the gain stage and the source follower respectively. The voltage transfer functions from the noise sources v_{eq1} and v_{eq2} to the output v_o are

$$\frac{v_o(s)}{v_{eq1}(s)} = \frac{1}{b}\,\frac{1}{1+a_1 s+a_2 s^2+a_3 s^3} \tag{3.9}$$

$$\frac{v_o(s)}{v_{eq2}(s)} = \left(\frac{1}{bA_{o1}}\right)\frac{1+st_{o1}}{1+a_1 s+a_2 s^2+a_3 s^3} \tag{3.10}$$

where

$$a_1 = t_L + \frac{t_{o1}}{bA_{o1}} + \frac{1}{bA_{o1}g_{m2}}(C_{ot2} + C_{SL}) \tag{3.11a}$$

$$a_2 = \frac{(t_{o1} + t_L)C_{ot2} + t_{o1}(C_{SL} + g_{m2}t_L)}{bA_{o1}g_{m2}} \tag{3.11b}$$

$$a_3 = \frac{t_{o1}t_L C_{ot2}}{bA_{o1}g_{m2}} \tag{3.11c}$$

and

$$b = \frac{C_I}{C_I + C_p}, \quad A_{o1} = G_m R_{o1} >> 1,$$

$$t_{o1} = R_{o1}C_{o1}, \quad t_L = R_{ONL}C_{SL},$$

$$C_{ot2} = bC_p + C_{o2}, \quad g_{m2}R_{o2} >> 1.$$

The impedance looking into the output node V_2 is

$$Z_{ox2} = \frac{1 + st_{o1}}{bA_{o1}g_{m2} + s(C_{ot2} + g_{m2}t_{o1}) + s^2 C_{ot2}t_{o1}}, \tag{3.12}$$

the voltage transfer function from the noise source v_{RONL} to v_o is

$$\frac{v_o(s)}{v_{RONL}(s)} = \frac{1 + \dfrac{s(C_{ot2} + g_{m2}t_{o1})}{bA_{o1}g_{m2}} + \dfrac{s^2 C_{ot2}t_{o1}}{bA_{o1}g_{m2}}}{1+a_1 s+a_2 s^2+a_3 s^3}$$

$$= \frac{(1+\frac{s}{z_1})(1+\frac{s}{z_2})}{1+a_1 s+a_2 s^2+a_3 s^3} \tag{3.13}$$

where

$$\frac{1}{z_1} + \frac{1}{z_2} = \frac{C_{ot2} + g_{m2}t_{o1}}{bA_{o1}g_{m2}} \tag{3.14a}$$

$$\frac{1}{z_1 z_2} = \frac{C_{ot2}t_{o1}}{bA_{o1}g_{m2}}, \tag{3.14b}$$

and a_1, a_2, a_3 are the same as in Eqs.(3.11). The total noise variance sampled by C_{SL} from the noise sources $\overline{v_{eq1}^2}$, $\overline{v_{eq2}^2}$ and $\overline{v_{RONL}^2}$ is

$$\overline{v_o^2}\Big|_{tot} = \frac{kT}{a_2a_1-a_3}\left[\frac{R_{teq1}a_2}{b^2} + \frac{R_{teq2}(a_2 + t_{o1}^2)}{b^2A_{o1}^2}\right.$$

$$\left. + R_{ONL}(a_2 + \frac{a_1}{a_3}\frac{1}{z_1^2z_2^2} + \frac{1}{z_1^2} + \frac{1}{z_2^2})\right] \qquad (3.15)$$

The contribution from $\overline{v_{eq2}^2}$ (the second term in Eq.(3.15)) is important as long as its magnitude is on the same order as that of the first term. This contribution is mainly from the zero ($w_z = \frac{1}{t_{o1}}$) in Eq.(3.10) which is located at a lower frequency range as compared with the poles ($P_1+P_2+P_3 = \frac{1}{t_{o1}} + \frac{1}{t_L}[1 + \frac{C_{SL}}{C_{ot2}}(1 + g_{m2}R_{ONL})]$) in Eq.(3.10). Therefore, the voltage transfer function $\frac{v_o(s)}{v_{eq2}(s)}$ shows a significant gain increase when the frequency passes through the zero ($w_z = \frac{1}{t_{o1}}$). The bandwidth of this "gain-peaking" in the transfer function of Eq.(3.10) can be narrowed by making $C_{ot2}+C_{SL}(1 + g_{m2}R_{ONL})$ larger than c_{o1}.

The third term of Eq.(3.15) is the noise contribution from the noise source $\overline{v_{RONL}^2}$ which can be simplified as

$$\overline{v_o^2}\Big|_{R_{ONL}} = \frac{kT}{C_{SL}}K_C \qquad (3.16)$$

where

$$K_C^{-1} = 1 + \frac{C_{SL}}{C_{ot2} + g_{m2}t_L\left[\frac{1+bA_{o1}(\frac{1}{b_1} + \frac{t_L}{t_{o1}})}{1 + \frac{1}{b_1} + \frac{t_L}{t_{o1}}}\right]} \qquad (3.17)$$

and $b_1 = \frac{g_{m2}t_{o1} + C_{ot2}}{C_{SL}}$. The magnitude of the coefficient K_C is less than 1.

If the source follower is an ideal buffer, g_{m2} tends to be very large, and $K_C \rightarrow 1$, $R_{teq2} \rightarrow 0$, $a_3 \rightarrow 0$, $a_1 \rightarrow (R_{ONL}C_{SL} + \frac{C_{o1}}{bG_m})$. Then this case is the same as in Eq.(2.25) discussed in Section 2.1.3.. The total noise variance sampled by C_{SL} ($\overline{v_o^2}\Big|_{tot}$) is equal to

$$\frac{kTR_{teq1}}{R_{ONL}C_{SL} + \frac{C_{o1}}{bG_m}} + \frac{kT}{C_{SL}}. \qquad (3.18)$$

Notice that for $bG_mR_{ONL}C_{SL} >> C_{o1}$ this noise variance is ($\frac{R_{teq1}}{R_{ONL}}$) times larger than a single $\frac{kT}{C_{SL}}$ noise.

3.3. Summary

The above noise analysis for considering the operational amplifier output impedance shows that the output voltage buffer does have less band-limiting effect on the noise

than an operational amplifier without output stage. Also a minimum $\frac{kT}{C}$ noise can be achieved in a switched-capacitor filter by using amplifiers without any output voltage buffer. The analysis also shows that there is a factor of $\frac{2}{3}$ difference between the equivalent noise resistance and the output impedance of an MOS transistor connected as a diode. This difference does help the total noise performance in active sample and hold circuits like the switched-capacitor filters.

If the operational amplifiers in a switched-capacitor circuit are only used to drive a moderate amount of capacitive load, improved $\frac{kT}{C}$ noise performance can be obtained by designing a transconductance amplifier instead of a low output impedance amplifier. But if a large capacitive load or a resistive load exists in the circuit and is driven by a switched-capacitor integrator, a low impedance output stage is necessary in the amplifier. In this case an amplifier design with low R_{teq1} and high g_{m2} is recommended in order to minimize the net wideband noise contribution.

CHAPTER 4

NOISE REDUCTION TECHNIQUES

From the discussion of Chapter 2, the important noise sources in switched-capacitor filters are the thermal noise in the channel of the MOS switches ($\frac{kT}{C}$ noise), the $\frac{1}{f}$ noise and the wideband thermal noise contributed from the operational amplifiers within the filters. The $\frac{kT}{C}$ noise is the fundamental wideband noise in switched-capacitor integrators. Its noise density is inversely proportional to the size of capacitor used. The $\frac{1}{f}$ noise component is dependent on the process used, the operational amplifier design and the gate capacitance of the input transistors in the operational amplifier. Its noise density is also inversely proportional to the capacitor size (the gate area). The wideband thermal noise in the operational amplifier is generated by the MOS channel resistance whose equivalent input referred voltage noise density is inversely proportional to the transconductance of the amplifier. The contribution from this noise source can be made insignificant by using an amplifier without an output stage. If an output stage is required in the circuit, this noise contribution can be made small compared with the $\frac{kT}{C}$ noise by using a large

transconductance input transistors in the amplifier. Fortunately, this wideband noise source is independent of the physical device size. Therefore, with reductions in technological feature size, the requirement for both low $\frac{kT}{C}$ noise and low operational amplifier $\frac{1}{f}$ noise limits the ability to scale down the physical dimensions of the filter.

This chapter will first discuss the fundamental limits on noise and dynamic range in switched-capacitor filters versus the scaling in technological feature size. Since the $\frac{1}{f}$ noise is colored, noise translation techniques can be used to shift the noise energy to a higher frequency from the frequency range of interest in the passband. Therefore, in the second part of this chapter two methods for reducing the $\frac{1}{f}$ noise in the low frequency range will be described.

4.1. Fundamental Limits on Dynamic Range versus Scaling Effect

The effects of scaling the device geometry in digital MOS circuits have already been discussed [10]. Fig.4.1(a) shows the relative changes in the circuit performance. Here, K is the scaling factor related to the nominal value, t_{OX} is the gate oxide thickness, and W and L are the channel width and length, respectively. For a scaling factor of K

Dimension (t_{ox}, W, L)	K
Doping Concentration (N)	1/K
Voltage (V)	K
Current (I)	K
Capacitance (C)	K
Delay ($\frac{C V}{I}$)	K
Power (IV)	K^2
Power-Delay (CV^2)	K^3

(a)

Noise Source	Scaled by	Signal Voltage Swing	Dynamic Range
$\frac{k T}{C}$ Noise	1/K	K	$K^{3/2}$
$\frac{1}{f}$ Noise	1/K	K	$K^{3/2}$
Op-Amp Wideband Noise	1	K	K

(b)

Fig.4.1(a) Circuit performance for the scaling factor of K.
(b) Dynamic range versus scaling factor of K in three noise sources.

smaller than 1, the gate capacitance per unit area (C_{OX}) increases by a factor of 1/K. With the same $\frac{W}{L}$ ratio in the transistor, the total gate area reduces by a factor of K^2, and the total gate capacitance reduces by a factor of K. Therefore, for a desired capacitance value in the circuit, the capacitor area can be scaled down only by a factor of K. In order to avoid the oxide breakdown and the punch-through, the operating voltage has to be reduced by a factor of K. In an NMOS transistor the relationships between the drain current (I_D), the transconductance (g_m), the $\frac{W}{L}$ ratio and the gate to source voltage (V_{GS}), when the transistor is biased in saturation region, are:

$$I_D = \frac{u_o C_{OX}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \qquad (4.1)$$

$$g_m = u_o C_{OX} \frac{W}{L} (V_{GS} - V_T) \qquad (4.2)$$

where u_o is the electron mobility. With the same $\frac{W}{L}$ ratio the operating current (I_D) is reduced by a factor of K, while the transconductance remains constant, assuming (V_{GS}-V_T) is scaled by the same factor K.

In discussing the noise performance of switched-capacitor filters with device scaling, the $\frac{W}{L}$ ratio, an important parameter in MOS device geometry (in both transistor and capacitor), is kept constant. For a scaling factor of K, the noise performance and the dynamic range change as shown in Fig.4.1(b). The $\frac{kT}{C}$ noise and the $\frac{1}{f}$ noise power

densities increase by a factor of $\frac{1}{K}$, while the operational amplifier wideband noise power density is unchanged. Since the power supplies and the operating voltage are scaled, the available signal swing is also scaled. To simplify the analysis, the distortion due to scaling effect is ignored. If either the $\frac{kT}{C}$ noise or the $\frac{1}{f}$ noise is dominant, then the dynamic range (both signal and noise are in units of voltage) is reduced by a factor of $K^{3/2}$; and if the operational amplifier wideband noise is dominant, then this factor is K.

In summary, the $\frac{kT}{C}$ noise is the fundamental wideband noise in the sample/hold circuits. This noise can be reduced either by using the larger capacitor size or by operating the circuit at lower temperature. The operational amplifier wideband noise can be reduced in switched-capacitor filters by designing the amplifier without an output voltage buffer. The $\frac{1}{f}$ noise can be reduced either by using large input devices to obtain large gate capacitances or by using buried channel devices to avoid surface states in the device channels. However, these two approaches will increase the chip size and process complexity. Another approach is to use circuit design techniques for reducing the low-frequency noise through the frequency translation methods such as the correlated double sampling technique and the chopper stabilization technique. Both techniques require discrete-time systems to operate. Therefore, it is convenient to implement them in switched-capacitor circuits.

4.2. Correlated Double Sampling Technique

The correlated double sampling method has been used in implementing low noise readout circuits for charge-coupled-device signal processing [8],[11],[28]. This technique is based on the clock operation in sampling two different data in the circuit: one sample is the significant noise component of the circuit and another sample is the input signal plus the noise component with some delay. The circuit for this technique should also be allowed to do a subtraction function between those two samples and an amplification of the difference. Having this operation, the noise energy in the circuit will be shifted to the clock frequency and its harmonics and will be reduced in the frequencies in between. This result offers the applicability of a system which has its baseband in the low-noise frequency regions and obtains an effective higher dynamic range inside that baseband. The details of this technique is shown in the following section.

4.2.1. Principle of Correlated Double Sampling

Fig.4.2 shows a conceptual correlated double sampling (CDS) system. The sample and hold (S/H) and the subtractor are incorporated in the amplifier with an equivalent input noise of $\overline{v_n^2}$ whose spectrum is shown in Fig.4.2(a).

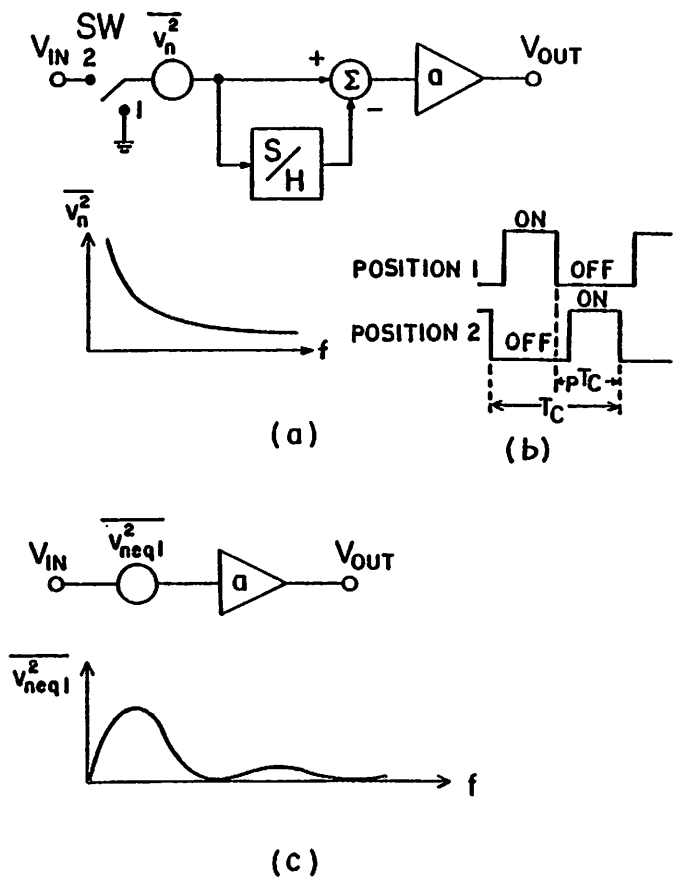


Fig.4.2 (a) Principle of correlated double sampling technique; (b) control clocks of the switches; (c) equivalent input noise of the circuit (a).

The sample/hold and the subtractor are required to perform a "one minus one's delay" function. The switch is controlled by two non-overlapping clocks with period of T_C as shown in Fig.4.2(b), where pT_C is the delay between two fall edges of the clocks. In the z-domain, the noise, v_{nOUT}, appearing at the output is equal to

$$v_{nOUT}(z) = a\, v_n(z)(\, 1 - z^{-p}\,) \tag{4.3}$$

where $z = e^{j\omega T_C}$. The associated noise power z-transform transfer function is

$$|H_{CDSz}(z)|^2 = a^2\,(\, 2 - z^{-p} - z^{p}\,) \tag{4.4}$$

in the z-domain and is

$$|H_{CDS\omega}(j\omega)|^2 = 2\,a^2\,(\, 1 - \cos \omega p T_C\,) \tag{4.5}$$

in the frequency domain. Therefore, the equivalent input noise of this correlated double sampling amplifier is

$$\overline{v_{neq1}{}^2}(\omega) = 2\,(\, 1 - \cos \omega p T_C\,)\,\overline{v_n{}^2}. \tag{4.6}$$

If $\overline{v_n{}^2}$ is a colored noise like the $\frac{1}{f}$ noise shown in Fig.4.2(a) (on a linear-linéar scale), then the equivalent input noise spectrum will look like in Fig.4.2(c). The "zeroes of the noise density function" appear at the

integral multiples of $\frac{1}{pT_C}$.

4.2.2. Circuit Implementation of Correlated Double Sampling Technique

The best way to implement a subtractor in a sample/hold circuit is to use a decoupling capacitor between the circuit which is dealing with the input sample (the signal and the noise) and the output amplifier. A circuit realization of the correlated double sampling technique is shown in Fig.4.3. Here, A_1 and A_2 are the preamplifier and the output amplifier, respectively, v_{n1} and v_{n2} are the equivalent input noise sources associated with stages A_1 and A_2, respectively, R_1 and R_2 are the feedback resistors in the preamplifier, C_D is the decoupling capacitor, C_{i2} is the input capacitance of the output amplifier, and SW1 and SW2 are two switches controlled by two non-overlapping clocks in switching between positions 1 and 2. Conceptually, during ϕ_1 the noise at the output of the stage A_1 (with R_1 and R_2 feedback network) and the equivalent input referred noise of the stage A_2 are sampled across C_D, and during ϕ_2 these sampled noises are still kept by C_D while the input signal passes through C_D. Effectively, the sampled noise is subtracted out by C_D. The clock waveforms and the corresponding switch positions are shown in Fig.4.2(b).

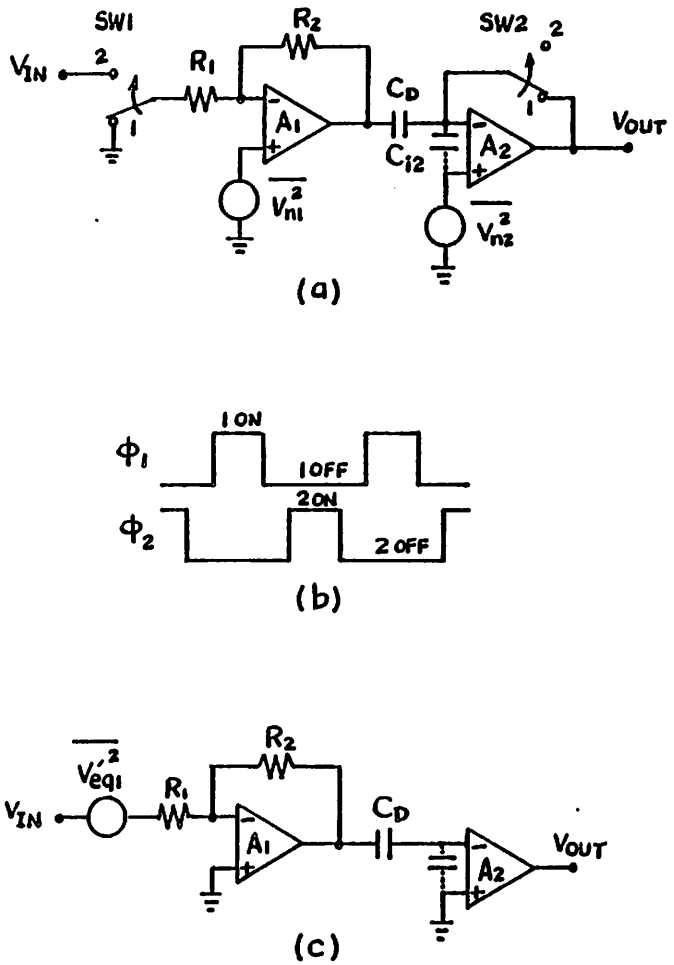


Fig.4.3 (a) Circuit realization of correlated double sampling (CDS) system, (b) control clocks of the switches; (c) equivalent circuit and noise of the circuit (a).

In the z-domain, if $C_D >> C_{i2}$, the total noise, v_{nOUT}, appearing at the output is equal to

$$v_{nOUT}(z) = (1+\frac{R_2}{R_1})\, a_2(1-z^{-p})v_{n1} + a_2(1-z^{-p})v_{n2} \qquad (4.7)$$

where a_2 is the voltage gain of the output amplifier A_2. The system voltage gain from v_{IN} to v_{OUT} when the circuit is in the "active" mode (switches in position 2) is $\frac{R_2}{R_1} a_2$. Therefore, the equivalent input noise of the circuit is

$$v'_{eq1}(z) = (1+\frac{R_1}{R_2})(1-z^{-p})v_{n1} + \frac{R_1}{R_2}(1-z^{-p})v_{n2}. \qquad (4.8)$$

If v_{n1} and v_{n2} are on the same order and if the voltage gain of the preamplifier (determined by the resistor ratio $\frac{R_2}{R_1}$) is much larger than 1, then the equivalent input noise density in the frequency domain becomes

$$\overline{v'_{eq1}{}^2}(\omega) = 2\,(\,1 - \cos \omega p T_C\,)\,\overline{v_{n1}{}^2} \qquad (4.9)$$

which is identical to Eq.(4.6). The equivalent circuit with equivalent input noise v_{eq1}' is shown in Fig.4.3(c).

The drawback of this circuit is that the output node of the amplifier (v_{OUT}) must slew back and forth between the signal level and the initialized level (the level when both switches are in position 1) during the clock sequence. This

operation puts severe constraints on the amplifier's settling time that will limit the performance of a switched-capacitor filter working at a higher clock rate.

4.3. Chopper Stabilization Technique

Another noise reduction technique is to apply chopper stabilization in the amplifiers of the filter. This technique has been used in the past in the design of precision DC amplifiers [12]. The basic concept of chopper stabilization is to force the AC and the DC components of the incoming signal to travel in two different paths within the amplifier. The DC path contains a DC chopper amplifier which provides the DC bias to the AC amplifier. Fig.4.4 shows this concept. HP and LP represent high-pass and low-pass circuits, respectively, V_{OS1} and V_{OS2} are the equivalent input offset voltages of the DC (A_1) and the AC (A_2) amplifiers, respectively, and A_1 and A_2 are the voltage gains of the amplifiers. After the DC chopper amplifier, V_{OS1} is chopped and shifted out of the low frequency range. After the second low-pass circuit (LP2), V_{OS1} is filtered out. This will result in a net offset voltage of A_2V_{OS2} at the output v_{OUT}. If A_1 is much larger than 1, the total equivalent input offset voltage at the input of the amplifier v_{IN} is equal to $\frac{V_{OS2}}{A_1} \simeq 0$. This stabilization will

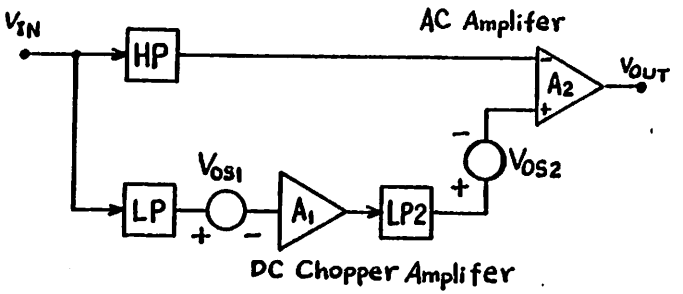


Fig.4.4 Concept of chopper stabilization technique.

reduce the equivalent input low-frequency noise as well, provided that the low-frequency noise is colored.

A modified chopper stabilization scheme is used in this research work. This scheme simplifies the circuit complexity by modulating/demodulating the signal and only modulating the noise without separating the amplifier into two paths. This section will explain this modified chopper stabilization technique.

4.3.1. Principle of Chopper Stabilization

The schematic of the chopper stabilized amplifier is shown in Fig.4.5. The amplifier consists of two stages, the first stage has voltage gain a_1, and the second stage has voltage gain a_2. Inserted at the input and the output of the first stage are two multipliers which are controlled by a synchronized chopping square wave of amplitude +1 and -1. The input referred noise spectrum of the stage a_1 ($\overline{v_{n1}^2}$) and a voiceband input signal spectrum (S_{IN}) are also shown in Fig.4.5(a).

After the first multiplier (at node A) the signal is modulated and translated to the odd harmonic frequencies of the chopping square wave, but the noise $\overline{v_{n1}^2}$ is unaffected. After the second multiplier (at node B) the signal is demodulated back to baseband, while the noise is modulated.

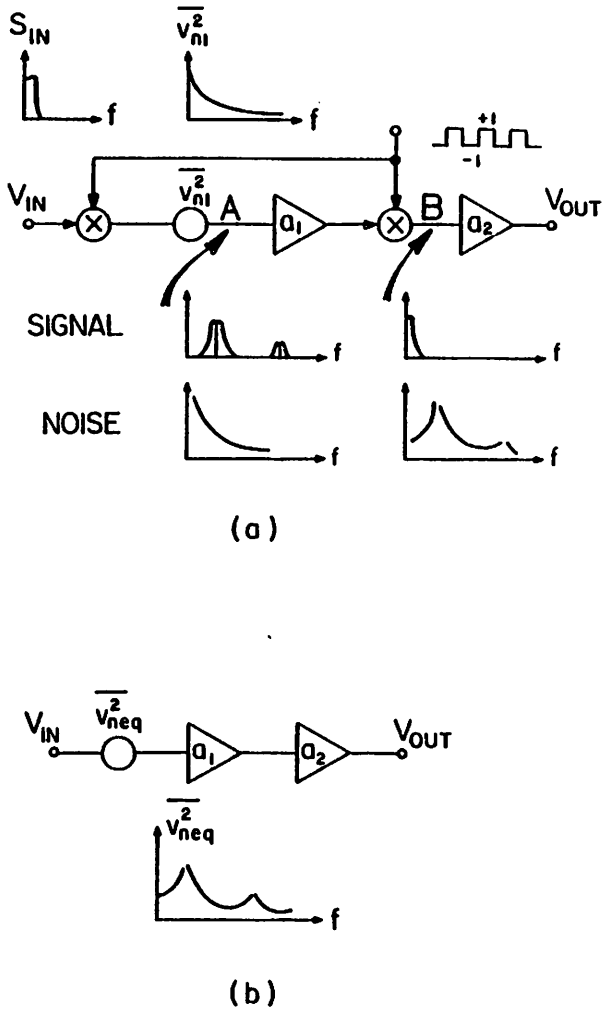


Fig.4.5 (a) A modified chopper-stabilized amplifier and the associated noise and signal spectra,
(b) equivalent circuit and noise of the circuit (a).

The spectra for the translations of the signal and the noise at node A and node B are shown in Fig.4.5(a). This chopping operation results in an equivalent input noise spectrum as shown in Fig.4.5(b), where the low-frequency noise component of $\overline{v_{n1}^2}$ (typically the $\frac{1}{f}$ noise component in this example) has been shifted to the odd harmonic frequencies of the chopping square wave. The noise density at low frequencies is now equal to the "fold-back" noise from those harmonic $\frac{1}{f}$ noise components. Therefore, if the chopper frequency is much higher than the signal bandwidth, then the $\frac{1}{f}$ noise inside the signal band is greatly reduced by the use of this technique.

Unlike the "zero noise densities" at the integral multiples of $\frac{1}{pT_C}$ in the correlated double sampling technique, the noise density at the even harmonic frequencies of the chopping square wave remains unchanged. The reason for this is that the noise at these frequencies is not modulated either by the first or by the second multiplier. Because the phase change of the noise with these frequencies is exactly equal to the phase changes of the multipliers, both multipliers do not "catch" the phase change of the noise between the clock sequence and have no modulation effect on the noise at even harmonic frequencies of the chopping square wave. This fact can be also verified by using Eq.(A.23). From this equation, the equivalent input noise density at frequency $2lf_p$ (l is the non-zero integers) is equal to

$$S_{NEQ}(2lf_p) = \frac{K_1/2}{f_p} \sum_{m=1}^{\infty} \left[\frac{2}{(2m-1)\pi}\right]^2 \left[\frac{1}{|2l-2m+1|} + \frac{1}{|2l+2m-1|}\right]$$

$$= \frac{K_1/2}{2lf_p} \qquad (4.10)$$

which is equal to the original $\frac{1}{f}$ noise density at frequency $2lf_p$ ($S_{N1}(2lf_p)$). This result explains that the net effect for modulating the noise (or the incoming signal) with frequencies equal to the even harmonic frequencies of the chopping clock is zero. The summation of all aliasing components will bring the net result equal to the original value.

4.3.2. MOS Implementation of Chopper Stabilization Technique

An MOS implementation of the chopper stabilization technique is shown in Fig.4.6, where a_1 and v_{n1} (a_2 and v_{n2}) are the voltage gain and the input noise of the first (second) stage, respectively. The multipliers described before are realized by two cross-coupled switches which are controlled by two non-overlapping clocks ϕ_{p1} and ϕ_{p2}. When ϕ_{p1} is on and ϕ_{p2} is off, the equivalent input noise is equal to v_{n1} plus v_{n2} divided by a_1. When ϕ_{p1} is off and ϕ_{p2} is on, the equivalent input noise is equal to $-v_{n1}$ plus v_{n2}/a_1. If the voltage gain of the first stage (a_1) is sufficiently high, the noise contribution from the second

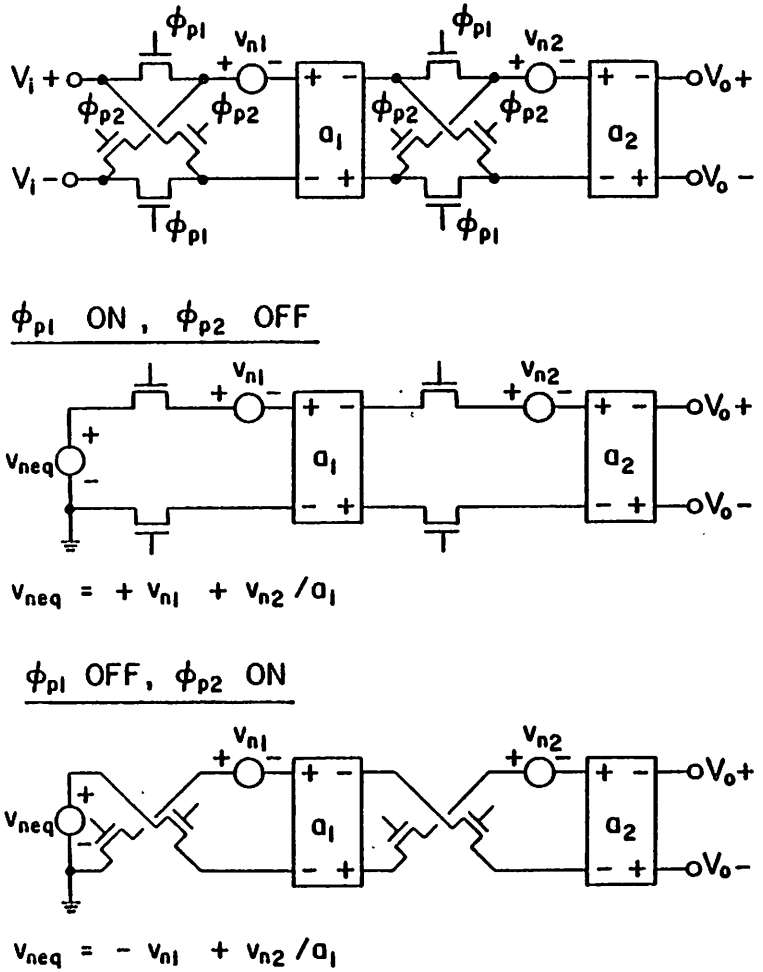


Fig.4.6 MOS implementation of a differential chopper-stabilized amplifier.

stage can be neglected and the sign of this equivalent input noise changes periodically. Effectively, a noise modulation function in the amplifier shown in Fig.4.5 is achieved.

This noise reduction technique is particularly simple to implement by the MOS technology in switched-capacitor filters. A low-noise switched-capacitor filter circuit design realized by this chopper-stabilized technique has been made to study the noise limitations discussed in chapters 2 and 3.

C H A P T E R 5

DIFFERENTIAL FILTER IMPLEMENTATION

The dynamic range of a circuit is defined as the ratio of the root-mean-square (RMS) value of the maximum signal swing with an acceptable distortion due to the circuit to the minimum detectable signal. For a circuit with finite bandwidth, the minimum detectable signal is the RMS value of the total inband noise. Thus, relatively speaking, improvements in signal swing with an acceptable distortion will result in improvement of the dynamic range. By using a fully differential circuit, the effective output signal swing is doubled relative to an ordinary single signal path circuit, provided that both circuits have the same power supplies. It will be discussed later that if the dominant noise source comes from the amplifiers used in the circuit, then the dynamic range is improved. This fact will be explained in Section 5.1.1.

The conventional circuits used to realize switched-capacitor filters are of single-ended configuration. This circuit configuration has poor power supply rejection

characteristics which limit the application of switched-capacitor filtering techniques to digital switching systems where low channel crosstalk is required [13]. Also it limits the application to high frequency switched-capacitor filter where the analog signal settling needs to be fast. The contamination from either power supplies or clocks will produce the feedthrough problem such as the "ringing" in the analog signal path of the circuit. In a switched-capacitor filter, the non-settled operational amplifier response or the incomplete charge transfer is a lossy process which limits the ability of realizing the high-Q filters [14]. Some efforts have been made to improve the power supply rejection [3],[15], and the clock feedthrough problems [16].

Since the power supply variations and the clock charge injections from the channel of the switches are common-mode perturbations to a differential circuit, by using a circuit in which the signal path is fully balanced the poor power supply rejection and the high clock feedthrough can be improved. The advantages of using a fully differential circuit in switched-capacitor filters, then, are quite obvious. This chapter will discuss the fully differential technique and the realization of a differential switched-capacitor filter incorporated with the differential chopper-stabilized operational amplifiers.

5.1. Fully Differential Technique in Switched-Capacitor Filter

The original concept of using differential-in single-ended output operational amplifier in a single signal path circuit is that the input and the output DC levels of the operational amplifier can be easily set by biasing the non-inverting input node to a desired DC level. In order to achieve the maximum possible voltage swing with fixed power supplies without distorting the signal, the output DC level of the amplifier is biased such that both positive and negative swings are equally spaced from the supplies. Therefore, the effective AC signal swing at the output of the amplifier is limited by the power supplies V^+ and V^- as shown in Fig.5.1(a), where Z_1 and Z_2 are two feedback circuits, V_{BI} and V_{BO} are the DC biases to the input and output of the amplifier, respectively. The peak-to-peak output voltage swing (V_{OUT1}) is equal to V^+-V^- in this case.

Another concept to design a circuit is to use a fully differential scheme to have more effective signal swing for the same power supplies. Fig.5.1(b) illustrates this. The input common-mode DC in Fig.5.1(b) is supplied by V_{BI}. The output common-mode DC is obtained from the common-mode bias circuitry inside the amplifier. Both circuits in Fig.5.1 have the same power supplies and the same transfer functions ($\frac{V_{OUT1}}{V_{IN}} = \frac{V_{OUT2}}{V_{IN}}$). Since the signals at v_0^+ and v_0^- are

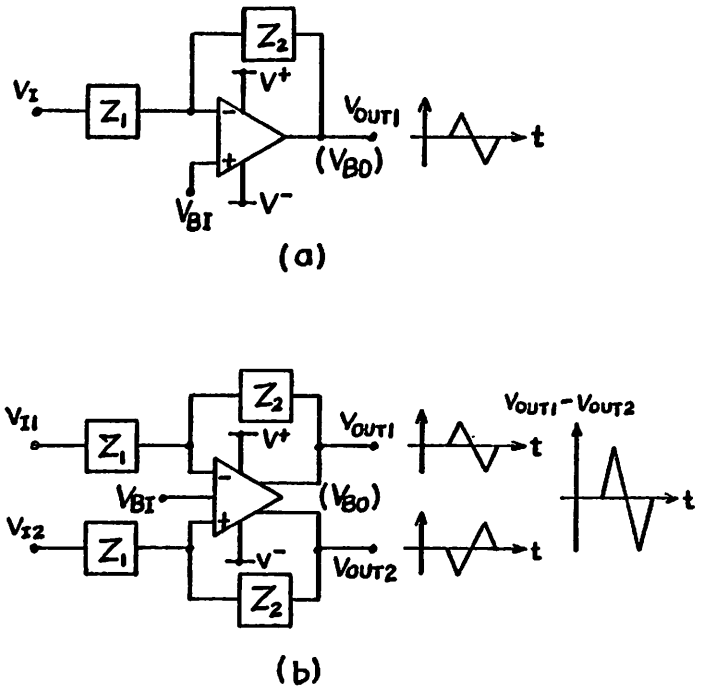


Fig.5.1 Comparison of signal swing in (a) single-ended case, and (b) differential case.

180^{o} out of phase by the nature of a fully differential network, the differential output ($v_{OUT2} = v_0^+ - v_0^-$) has an effective peak-to-peak signal swing of $2(V^+ - V^-)$ which is twice of that in Fig.5.1(a) case. This explains the improvement in signal swing in the differential output case. The following sections will discuss fully differential circuits in more detail.

5.1.1. Advantages of Fully Differential Circuits

The advantages of fully differential configuration over single-ended configuration are: (1) dynamic range improvement, (2) power supply rejection improvement, and (3) clock feedthrough cancellation. They will be discussed in detail in this section.

Balanced circuitry and differential signal paths are two characteristics of a fully differential circuit. The balanced circuitry can decrease the common-mode effects such as power supply variations and clock feedthrough. The availability of both positive and negative polarity signals in fully differential configuration simplifies the filter design, especially in an elliptic filter configuration (shown as an example in Fig.5.2). It also furnishes higher dynamic range with larger effective signal swing. Since a differential network needs more external bias and feedback circuits to the amplifier, the dynamic range may be

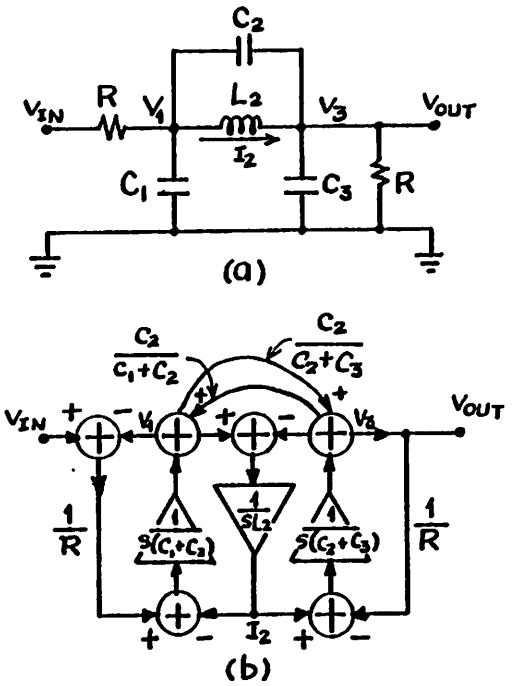


Fig.5.2 (a) A third-order elliptic lowpass filter, (b) signal flow graph of (a).

reduced due to the noise contribution from those circuits. However, if the dominant noise source is in the amplifier, the total equivalent circuit noise will remain constant in both single-ended and differential cases.This will be shown as follows.

Fig.5.3 shows the comparison of the noise between single-ended and differential RC integrators. The semiconductor chip area of capacitors in switched-capacitor filter is usually the dominant factor in the chip design. During the comparison, the total amount of integrating capacitance in each case is kept the same. Since the major noise contribution in the operational amplifier comes from the differential input stage in both cases. It is reasonable to assume the equivalent amplifier noise densities to be identical. The transfer functions for the signal from the input to the output of the integrator are identical. For the operational amplifier noise, the transfer functions from the noise source to the output of the integrator are also identical. The total noise densities at the outputs of the amplifiers are

$$\frac{\overline{v_{no1}^2}}{\Delta f} = \frac{4kTR}{u^2R^2C^2} + \left(1 + \frac{1}{u^2R^2C^2}\right)\frac{\overline{v_{nop}^2}}{\Delta f} \qquad (5.1)$$

and

$$\frac{\overline{v_{no2}^2}}{\Delta f} = \frac{16kTR}{u^2R^2C^2} + \left(1 + \frac{1}{u^2R^2C^2}\right)\frac{\overline{v_{nop}^2}}{\Delta f} \qquad (5.2)$$

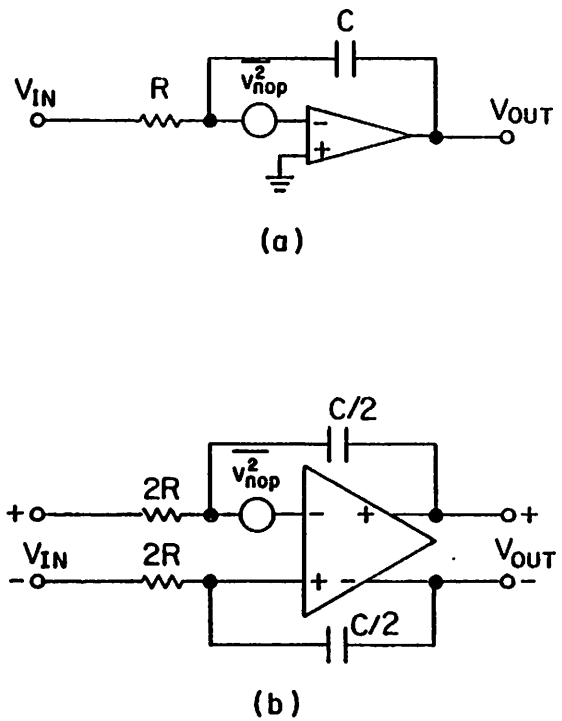


Fig.5.3 Comparison of the noise in (a) single-ended, and (b) differential RC integrator.

in the single-ended and differential cases, respectively. If the operational amplifier noise is dominant, Eq.(5.1) and Eq.(5.2) have the same magnitude. But if the thermal noise in the resistors is dominant, the noise power of differential integrator is four times larger. Fortunately, the dynamic range of commercially available voiceband switched-capacitor filters are presently limited primarily by the operational amplifier noise. Hence, the fully differential configuration provides an effective method to improve the dynamic range.

The second advantage is in improving power supply rejection. Whether the amplifier is differential-out or single-ended, the input stage is usually a differential pair. As long as the voltage gain of this stage is sufficiently high, the contributions of power supply variation, noise and offset from the gain and the output stages can be neglected. Fig.5.4 shows a simple differential pair stage with positive (V_{DD}) and negative (V_{SS}) power supplies and their variations v_{dd} and v_{ss}, respectively, and the MOS transistors M_1 and M_2 with small-signal transconductance g_{m1} and g_{m2} and output impedance r_{o1} and r_{o2}, respectively. I_C is the bias current with a shunt resistance of value R_C. R_{L1} and R_{L2} are the loads of M_1 and M_2, respectively. The response appearing at the outputs v_{01} and v_{02} resulting from the power supply variations v_{dd} and v_{ss} are

$$\left.\frac{v_{o1}}{v_{dd}}\right|_{v_{ss}=0} = a_{dH} g_{m1} r_{o1} \qquad (5.3)$$

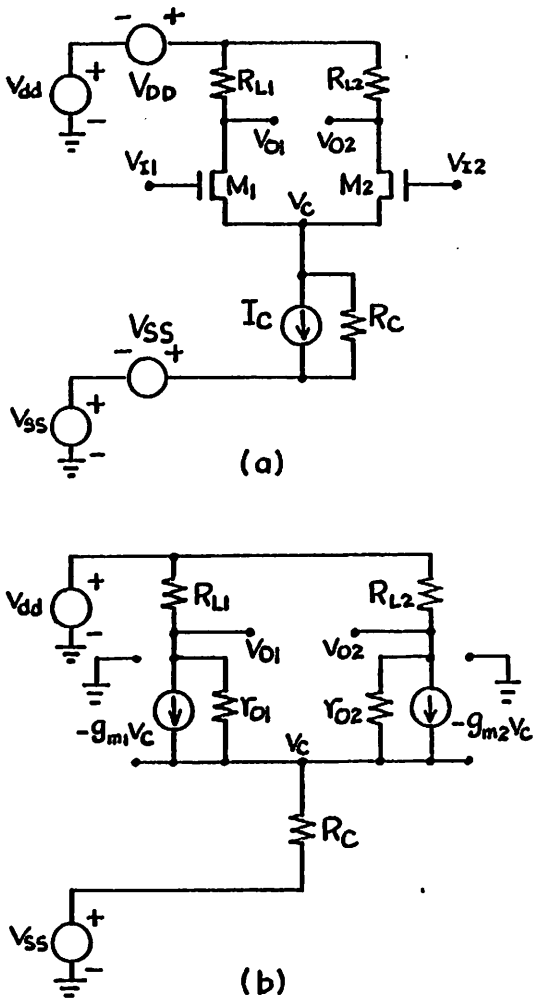


Fig.5.4 (a) Power supply variation in a differential-pair stage; (b) small-signal model of (a).

$$\left.\frac{v_{o2}}{v_{dd}}\right|_{v_{ss}=0} = a_{dR} g_{m2} r_{o2} \tag{5.4}$$

$$\left.\frac{v_{o1}}{v_{ss}}\right|_{v_{dd}=0} = a_{sR} g_{m1} r_{o1} \tag{5.5}$$

$$\left.\frac{v_{o2}}{v_{ss}}\right|_{v_{dd}=0} = a_{sR} g_{m2} r_{o2} \ , \tag{5.6}$$

where

$$a_{dR} = \frac{R_{L1} + R_{L2}}{g_{m1} r_{o1} R_{L2} + g_{m2} r_{o2} R_{L1} + \dfrac{R_{L1} R_{L2}}{R_C}} \tag{5.7}$$

and

$$a_{sR} = \frac{\dfrac{R_{L1} R_{L2}}{R_C}}{g_{m1} r_{o1} R_{L2} + g_{m2} r_{o2} R_{L1} + \dfrac{R_{L1} R_{L2}}{R_C}} \ . \tag{5.8}$$

If the differential pair and the loads are matched, then g_m's, r_o's and R_L's are identical, and

$$\left.\frac{v_{o1}}{v_{dd}}\right|_{v_{ss}=0} = \left.\frac{v_{o2}}{v_{dd}}\right|_{v_{ss}=0} = \frac{1}{1 + \dfrac{R_L}{2 g_m r_o R_C}} \ , \tag{5.9}$$

$$\left.\frac{v_{o1}}{v_{ss}}\right|_{v_{dd}=0} = \left.\frac{v_{o2}}{v_{ss}}\right|_{v_{dd}=0} = \frac{1}{\dfrac{1}{g_m r_o} + \dfrac{2R_C}{R_L}} \ . \tag{5.10}$$

Eq.(5.9) and Eq.(5.10) represent the effect of the V_{DD} and V_{SS} supply variations to the outputs of this stage. They are single-output responses. The differential output ($\Delta v_o = v_{o1} - v_{o2}$) is zero provided that the circuit is perfectly matched. In real case, mismatches occur and the differential output has responses of

$$\left.\frac{\Delta v_o}{v_{dd}}\right|_{v_{ss}=0} = a_{dR}(g_{m1} r_{o1} - g_{m2} r_{o2}) \tag{5.11}$$

$$\left.\frac{\Delta v_o}{v_{ss}}\right|_{v_{dd}=0} = a_{sR}(g_{m1} r_{o1} - g_{m2} r_{o2}) \ . \tag{5.12}$$

The mismatches of g_m, r_o and R_L are defined as

$$\begin{aligned} g_{m1} &= g_m + \frac{\Delta g_m}{2} \ , \quad g_{m2} = g_m - \frac{\Delta g_m}{2} \\ r_{o1} &= r_o + \frac{\Delta r_o}{2} \ , \quad r_{o2} = r_o - \frac{\Delta r_o}{2} \\ R_{L1} &= R_L + \frac{\Delta R_L}{2} \ , \quad R_{L2} = R_L - \frac{\Delta R_L}{2} \end{aligned} \tag{5.13}$$

where g_m , r_o and R_L are the average values. Eq.(5.11) and

Eq.(5.12) can be simplified to

$$\left.\frac{\Delta v_o}{v_{dd}}\right|_{v_{ss}=0} = \frac{\frac{\Delta g_m}{g_m} + \frac{\Delta r_o}{r_o}}{1 + \frac{R_L}{2g_m r_o R_L}} \qquad (5.14)$$

and

$$\left.\frac{\Delta v_o}{v_{ss}}\right|_{v_{dd}=0} = \frac{\frac{\Delta g_m}{g_m} + \frac{\Delta r_o}{r_o}}{\frac{1}{g_m r_o} + \frac{2R_C}{R_L}}, \qquad (5.15)$$

respectively. In usual case $2g_m r_o R_C >> R_L$, therefore Eq.(5.14) and Eq.(5.15) are approximately equal to

$$\left.\frac{\Delta v_o}{v_{dd}}\right|_{v_{ss}=0} \simeq \frac{\Delta g_m}{g_m} + \frac{\Delta r_o}{r_o} \qquad (5.16)$$

and

$$\left.\frac{\Delta v_o}{v_{ss}}\right|_{v_{dd}=0} \simeq \left(\frac{\Delta g_m}{g_m} + \frac{\Delta r_o}{r_o}\right) \frac{R_L}{2R_C}, \qquad (5.17)$$

respectively. The improvement in power supply rejection is clear when comparing Eq.(5.14) and Eq.(5.15) with Eq.(5.9) and Eq.(5.10). The rejection improves by a factor of

$$\frac{1}{\frac{\Delta g_m}{g_m} + \frac{\Delta r_o}{r_o}} \qquad (5.18)$$

in both cases, which is strongly dependent on the mismatch of the two input transistors. If the g_m and r_o mismatches are 5% each, then the improvement from single output to differential output is ten times (20dB). This calculation is based upon the variations appearing at the outputs. If the supply variations shown at the outputs are referred back to the input of the amplifier, the single-ended case (Eq.(5.9) or Eq.(5.10)) should be divided by the voltage gain of $\frac{1}{2}g_m(R_L||r_o)$ while the differential case (Eq.(5.14) or Eq.(5.15)) is divided by $g_m(R_L||r_o)$. This is another 6dB improvement.

Another supply variation mechanism occurs from the coupling of power supply through the substrate to the bottom-plate of the capacitors in the filter. This coupling can be modeled as an equivalent supply variation at the input of the switched-capacitor integrator as shown in Fig.5.5, where a_{cpd} and a_{cps} are the capacitive coupling coefficients from v_{dd} and v_{ss} to node v_p, respectively; C_{pSUB} is the substrate parasitic capacitance at the inverting node of the operational amplifier. The direct path from v_p through C_{pSUB} and C_I to output v_0 contributes the supply variations of $\frac{C_{pSUB}}{C_I} a_{cpd} v_{dd}$ and $\frac{C_{pSUB}}{C_I} a_{cps} v_{ss}$, provided that the operational amplifier has sufficient voltage gain. This kind of supply variation coupling is decreased in the differential case which is shown in Fig.5.6. This is a fully differential bottom-plate switched-capacitor integrator with two sampling

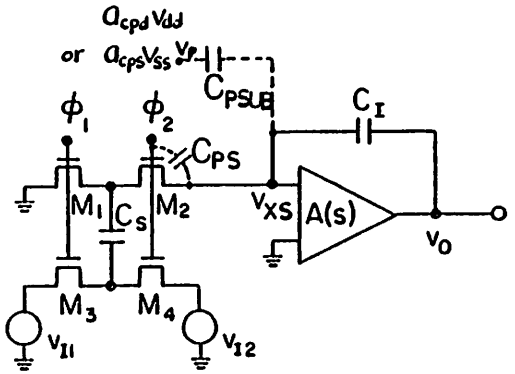


Fig.5.5. Capacitive coupling of power supply variations in a single-ended switched-capacitor integrator.

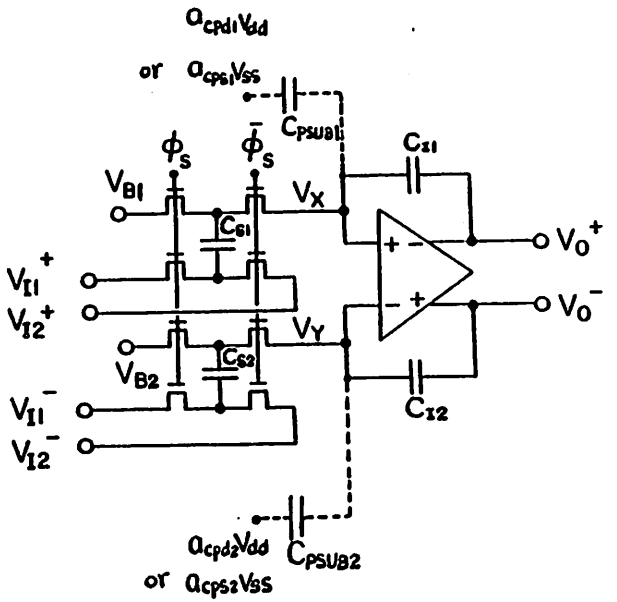


Fig.5.6 Capacitive coupling of power supply variations in a differential switched-capacitor integrator.

capacitors (C_{S1} and C_{S2}) and two integrating capacitors (C_{I1} and C_{I2}). v_{I1}^{+} and v_{I1}^{-} are one differential input. v_{I2}^{+} and v_{I2}^{-} are another differential input. The differential output supply variation (Δv_{oSUB}) exists only when there are mismatches in a_{cpd}'s, a_{cps}'s and C_I's. If the mismatches are defined as follows

$$a_{cpd1} = a_{cpd} + \frac{\Delta a_{cpd}}{2}, \quad a_{cpd2} = a_{cpd} - \frac{\Delta a_{cpd}}{2},$$

$$a_{cps1} = a_{cps} + \frac{\Delta a_{cps}}{2}, \quad a_{cps2} = a_{cps} - \frac{\Delta a_{cps}}{2},$$

$$C_{pSUB1} = C_{pSUB} + \frac{\Delta C_{pSUB}}{2}, \quad C_{pSUB2} = C_{pSUB} - \frac{\Delta C_{pSUB}}{2},$$

$$C_{I1} = C_I + \frac{\Delta C_I}{2}, \quad C_{I2} = C_I - \frac{\Delta C_I}{2}, \qquad (5.19)$$

then the differential output supply variation is

$$\Delta v_{oSUB} = \frac{C_{pSUB}}{C_I} a_{cpd} v_{dd} \left[\frac{\Delta a_{cpd}}{a_{cpd}} + \frac{\Delta C_{pSUB}}{C_{pSUB}} - \frac{\Delta C_I}{C_I} \right]$$

$$+ \frac{C_{pSUB}}{C_I} a_{cps} v_{ss} \left[\frac{\Delta a_{cps}}{a_{cps}} + \frac{\Delta C_{pSUB}}{C_{pSUB}} - \frac{\Delta C_I}{C_I} \right]. \qquad (5.20)$$

If the mismatches in a_{cpd}'s, a_{cps}'s, C_{pSUB}'s and C_I's are 5% each, then the worst-case improvement in differential output case is 6.7 times (16dB). Since this mechanism results from the coupling outside the operational amplifier, and the

transfer functions for both single-ended and fully-differential integrators from the input to the output are identical, therefore the improvement of the supply rejection in the fully-differential case due to this mechanism is the quantities inside the brackets.

The improvement in canceling the clock feedthrough of differential switched-capacitor integrators over single-ended switched-capacitor integrators can be seen from Fig.5.5 and Fig.5.6, where C_{ps}'s are the parasitic capacitances from the gates to the drains of the switches. If mismatches of C_{ps1} and C_{ps2} are defined as $C_{ps1} = C_{ps} + \frac{\Delta C_{ps}}{2}$ and $C_{ps2} = C_{ps} - \frac{\Delta C_{ps}}{2}$, then the improvement of clock feedthrough resulted from clock $\overline{\phi_S}$ through C_{ps}'s is $\left[\frac{1}{\frac{\Delta C_{ps}}{C_{ps}} - \frac{\Delta C_I}{C_I}} \right]$. This is the third advantage of using differential circuits in a switched-capacitor filter.

5.1.2. Considerations in Differential MOS Circuits

The advantage of fully differential circuitry is the balanced differential signal path. However, due to the process variations and the mismatches, some common-mode signals will appear in differential signal path and produce some undesired effects in the circuit. This section will discuss

some of these effects.

The common-mode DC output of the fully differential operational amplifier is set by an internal common-mode feedback circuit. (This will be discussed in the next section.) The common-mode DC input to the amplifier in the circuit of Fig.5.6 ($\frac{V_X + V_Y}{2}$) is set by the bias voltage V_B and the common-mode DC levels of the differential signals v_{I1}^+, v_{I1}^- and v_{I2}^+, v_{I2}^- (i.e. V_{I1}^+, V_{I1}^- and V_{I2}^+, V_{I2}^-). If the differential voltage gain of the operational amplifier is large enough, the differential charge sampled by C_{S1} and C_{S2} will be transferred to the integrating capacitors. The remaining charge held by the input capacitors of the operational amplifier forms the common-mode DC input to the amplifier. This DC voltage is

$$\frac{V_X + V_Y}{2} = V_B + \frac{C_{S1}V_{I2}^+ + C_{S2}V_{I2}^-}{C_{S1} + C_{S2}} - \frac{C_{S1}V_{I1}^+ + C_{S2}V_{I1}^-}{C_{S1} + C_{S2}} \qquad (5.21)$$

where V_B is a constant bias voltage. Notice that this common-mode DC input can be set at a negative value by the bias voltage V_B through the sampling capacitors that work like a DC level shifter. By choosing suitable V_B, the level shift function in the single-channel MOS operational amplifier can be eliminated and the frequency response of the

amplifier is improved.

If v_{I1}^+ and v_{I1}^-, and v_{I2}^+ and v_{I2}^- are not exactly 180° out of phase (i.e. v_{I1}'s or v_{I2}'s have their common-mode components), and if C_S's have mismatch (defined as $C_{S1} = C_S + \frac{\Delta C_S}{2}$ and $C_{S2} = C_S - \frac{\Delta C_S}{2}$), then the common-mode of v_X and v_Y has an AC component which in z-domain is equal to

$$\frac{v_X(z)+v_Y(z)}{2} = \left\{\frac{v_{i2}^+ + v_{i2}^-}{2} - \left[\frac{v_{i1}^+ + v_{i1}^-}{2}\right] z^{-1}\right\} + \frac{\Delta C_S}{4C_S}\left[(v_{i2}^+ - v_{i2}^-) - (v_{i1}^+ - v_{i1}^-)z^{-1}\right]. \qquad (5.22)$$

The quantity inside the first pair of brackets is the difference of two differential signals' common-mode components. This quantity will not affect the differential signal path. The quantity inside the second pair of brackets is the difference of two differential signals' differential-mode components. This is exactly the differential signal that the differential integrator is operating on. Therefore, the common-mode bias path in a fully differential switched-capacitor filter is contaminated by the injection of a differential signal due to the mismatch in the sampling capacitors. This contamination is linearly proportional to the difference of two differential signals, that will cause the overall gain and phase errors in the integrator's transfer function. These errors are similar to the errors due to the

finite operational amplifier open-loop DC voltage gain (a_o) in a single-ended switched-capacitor integrator as shown in Fig.5.5, where v_{sx} is a function of v_o ($v_{sx} = \frac{-v_o}{a_o}$), and so is a function of the difference of v_{i1} and v_{i2}. The exact z-transform transfer function in this integrator is

$$v_o(z) = \frac{\frac{C_S}{C_I}(v_{i1}(z)z^{-1} - v_{i2}(z))}{[1 + \frac{1}{a_o}(1 + \frac{C_S}{C_I})] - (1 + \frac{1}{a_o})z^{-1}} . \qquad (5.23)$$

The z-transform transfer function for an ideal bottom-plate switched-capacitor integrator is

$$v_{oideal}(z) = \frac{\frac{C_S}{C_I}(v_{i1}(z)z^{-1} - v_{i2}(z))}{1 - z^{-1}} . \qquad (5.24)$$

The difference between Eq.(5.23) and Eq.(5.24) is the deviations of the coefficients in the denominator. By transferring to the frequency domain ($z = e^{juf_C}$, T_C is the clock period), these deviations will appear as gain and phase errors [17],[18]. For a low open-loop voltage gain operational amplifier implemented in the switched-capacitor filter, the Q-value decreases from the nominal designed value and so limits the applications in high-Q and Q-sensitive filters.

A similar result occurs in the differential case. For the open-loop DC voltage gain of a_o in the operational amplifier, the z-transform transfer function is

$$v_{o1}(z) - v_{o2}(z) = \frac{(1+a_m)\frac{C_S}{C_I}[(v_{I1}^{+} - v_{I1}^{-})z^{-1} - (v_{I2}^{+} - v_{I2}^{-})]}{[1 + \frac{1}{a_o}(1 + \frac{C_S}{C_I})] - (1 + \frac{1}{a_o})z^{-1}} \qquad (5.25)$$

where a_m is a mismatch coefficient of value

$$a_m = \frac{\Delta C_S}{4C_S}\left[\frac{\Delta C_I}{C_I} - \frac{\Delta C_S}{C_S}\right] . \qquad (5.26)$$

This is a second-order effect which comes from the contamination of common-mode path by the mismatch of C_S's and C_I's. For a capacitor mismatch of 5% a_m is 0.125% of unity, and for 1% mismatch a_m is 0.005% of unity. By careful layout the gain error due to a_m can be ignored, and the net transfer function is the same as the Eq.(5.23) in single-ended case.

Since the improvements of power supply rejections and clock feedthrough cancellations in the differential case is mainly dependent on the chip layout, the symmetry and the interconnection problems might result in a larger chip area. Another problem for a fully differential circuit is that the "real world" is not fully differential and neither are most

of the circuits in other systems fully differential. Therefore a conversion for single-in to differential and differential-out to singled-ended is necessary. This conversion should not degrade the performance of the fully differential circuit.

The considerations discussed above should be made in differential MOS circuit design in order to achieve the best performance.

5.2. Realization of Differential Chopper-Stabilized Operational Amplifier in MOS Technology

A modified chopper-stabilized amplifier scheme is shown in chapter 4 (Fig.4.6). A key design problem in the implementation of differential MOS operational amplifier of this type is the realization of fully differential signal path with a well-defined common-mode voltage. In principle chopper stabilization could be implemented without simultaneously using a differential configuration. But incorporating these two techniques together a high performance switched-capacitor filtering technique is obtained; the balanced cross-coupled analog switches as phase reverser, the doubled signal swing, and all the advantages discussed on the last section are clearly shown.

The schematic diagram of a differential chopper-stabilized operational amplifier is shown in Fig.5.7. The gate dimensions of the transistors are given in Fig.5.7.1. Transistors M_{C1} to M_{C4} and M_{C5} to M_{C8} form two cross-coupled choppers which are controlled by two non-overlapping clocks ϕ_p and $\overline{\phi_p}$. Transistors M_1 to M_5, M_6 to M_{10} and M_{11} to M_{15} are the input, gain and output stages, respectively. The operating points of the input stage are biased by the common-mode feedback loop through the gain stage (M_5 to M_8). In order to get the maximum signal swing in both voltage directions, the common-mode output DC of the operational amplifier should be biased at the midpoint between two power supplies. In Fig.5.7, V_{DD} and V_{SS} have the same magnitude, therefore the common-mode output DC should be biased at the ground level. This DC level and the operating points of the gain stage are set from the common-mode feedback circuit consisting of transistors M_{16} to M_{24}, which is biased by a grounded half-circuit replica reference string of transistors M_{25} to M_{29}. In order to ensure a well-defined common-mode output DC voltage for large differential output swings, the common-mode level shifter (M_{17} to M_{24}) uses the depletion transistors. By using these depletion devices, the summing node (the sources of M_{23} and M_{24}) voltage in the common-mode level shift circuit will not change when the gates of M_{17} and M_{18} have a large differential voltage applied. The common-mode DC voltage at the input of the operational amplifier is obtained by the bias voltage

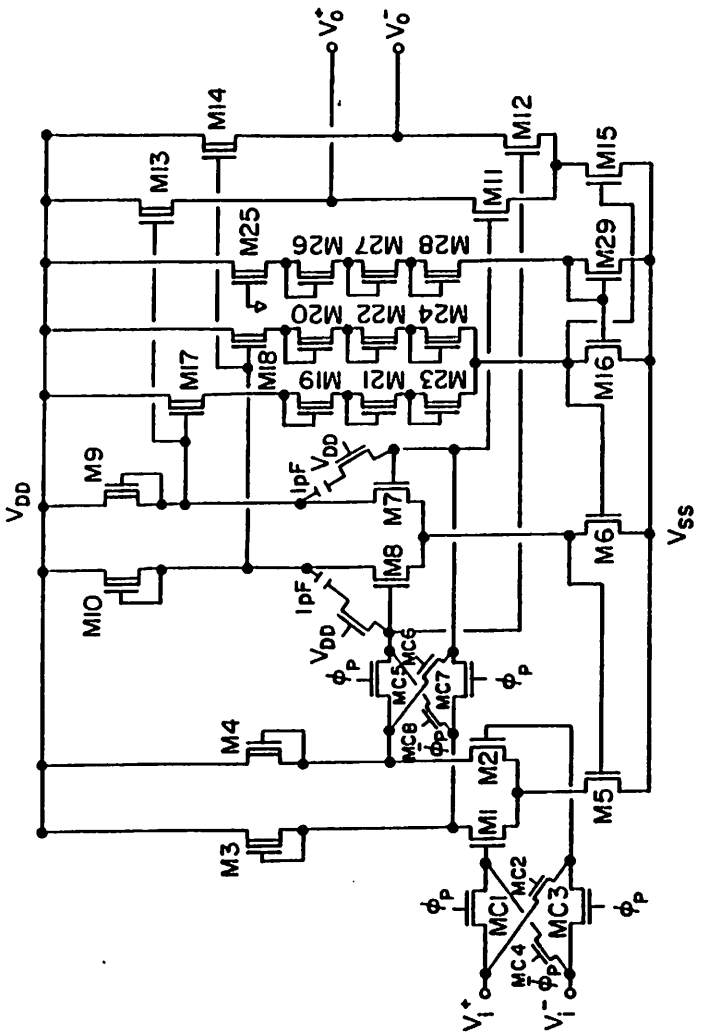


Fig.5.7 Differential chopper-stabilized operational amplifier.

	W(um)	L(um)
MC1 to MC8	10	35
M1, M2	100	20
M3, M4	15	60
M5	90	20
M6	40	20
M7, M8	40	20
M9, M10	10	40
M11, M12	80	20
M13, M14	15	20
M15	200	20
M16	120	20
M17 to M28	10	35
M29	60	20
M_{comp}	10	35

Fig.5.7.1 Mask width(W) and length(L) in the operational amplifier.

V_B shown in Fig.5.6.

Pole splitting compensation in the gain stage and a feedforward path to the output stage (M_{11} and M_{12}) are used to improve the stability of the operational amplifier for driving a large capacitive load. The triode-region transistor in series with a 1pF capacitor in the compensation feedback circuit performs like an RC network which generates a "feedback zero" to move the right-half-plane zero resulting from the low transconductance in the MOS drivers (M_7 and M_8) to the left-half-plane [19]. The function of a feedforward path is illustrated in Fig.5.8, where $-A_1(\omega)$ is the regular capacitance compensated inverter, $-A_2(\omega)$ is the feedforward path. The transfer functions are

$$\frac{V_{1o}}{V_1}(s) = -A_1(s)$$

$$= \frac{-A_{1o}}{1 + \frac{s}{p_1}} \qquad (5.27)$$

and

$$\frac{V_{2o}}{V_1}(s) = -A_2(s)$$

$$= \frac{-A_{2o}}{1 + \frac{s}{p_2}} , \qquad (5.28)$$

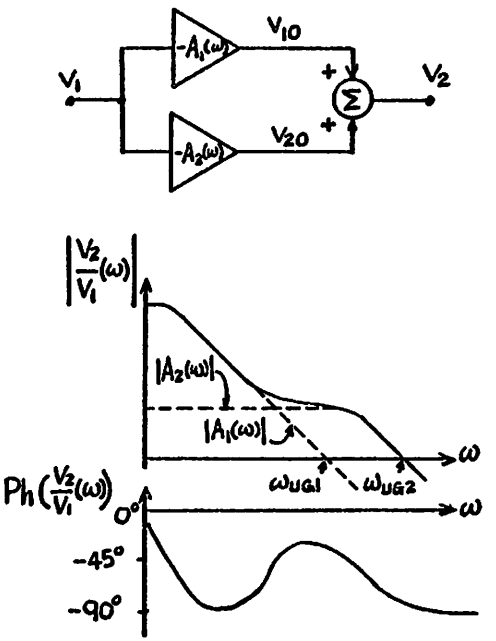


Fig.5.8 Principle of a feedforward circuit.

where p_1 and p_2 are the poles of $A_1(s)$ and $A_2(s)$, respectively. The net transfer function is

$$\frac{v_2}{v_1}(s) = -(A_1(s) + A_2(s))$$

$$= -\frac{(A_{1o} + A_{2o}) + (\frac{A_{1o}}{p_2} + \frac{A_{2o}}{p_1})s}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})} . \qquad (5.29)$$

The feedforward path extends the unity-gain bandwidth of the inverter from a low capacitive compensated one (ω_{UG1}) to a much higher ω_{UG2}. The effective bandwidth increases without reducing the phase margin.

5.3. Differential Chopper-Stabilized Switched-Capacitor Filter

The schematic diagram of a bottom-plate fifth-order differential low-pass ladder filter is shown in Fig.5.9. This filter configuration is used to implement a differential Chebyshev low-pass filter with cutoff frequency at 3400 Hz. The original passive filter network and the signal flow diagram are shown in Fig.2.4. The circuit shown in Fig.5.9 is fully differential-in and differential-out. Five chopper-stabilized operational amplifiers as shown in Fig.5.7 with chopper clock (ϕ_p and $\overline{\phi_p}$) of frequency

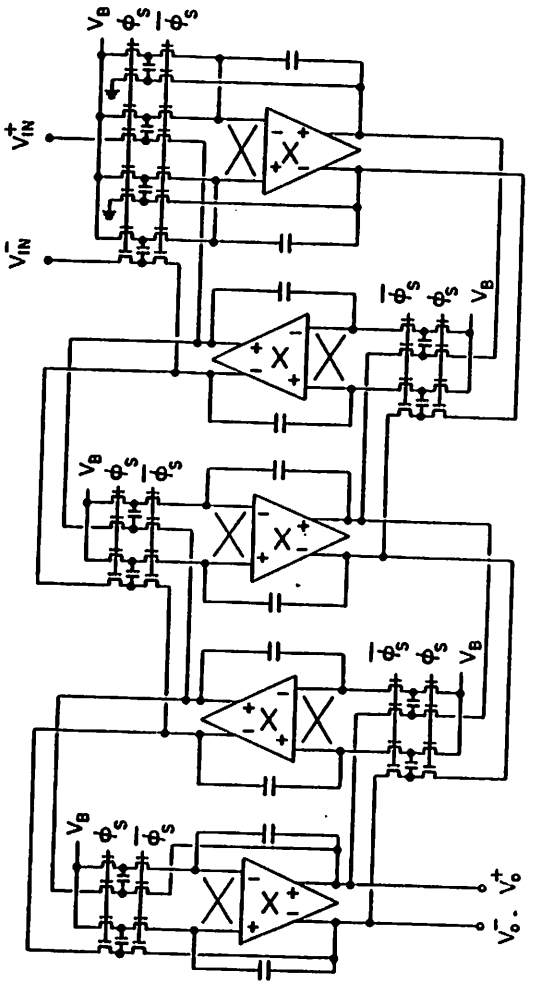


Fig.5.9 A bottom-plate fifth-order differential chopper-stabilized lowpass filter.

128KHz, and filter clock (ϕ_s and $\overline{\phi_s}$, two non-overlapping clocks) of frequency 256 KHz. From the discussion in chapter 4, the $\frac{1}{f}$ noise is translated by the chopper to the odd harmonic frequencies of the chopper clock. All the $\frac{1}{f}$ noise components will appear, in the frequency domain, equally spaced between two adjacent integer multiples of the filter clock frequency. This is exactly the Nyquist rate of the filter clock. As a result, no aliasing effect of the translated $\frac{1}{f}$ noise back into the baseband occurs and no interference between the odd harmonic frequencies of the chopper clock and the harmonic frequencies of the filter clock occurs. The chopping and the switching of the filter do not contaminate each other. This choice of chopping frequency is optimum in terms of a maximum reduction in baseband $\frac{1}{f}$ noise.

CHAPTER 6

EXPERIMENTAL RESULTS OF A PROTOTYPE LOWPASS FILTER

An experimental prototype chopper-stabilized fully differential fifth-order Chebyshev switched-capacitor lowpass filter was designed and fabricated. The purpose of this experiment is to investigate the effectiveness of the chopper stabilization scheme in reducing the low-frequency noise, and the use of differential filter configuration in improving the power supply and the clock feedthrough rejection. In this chapter the important factors in the chip design and some considerations in measurements will be discused, and then the experimental results for the on-chip test operational amplifier and the filter will be presented.

6.1. Chip Design and Measurement Considerations

An n-channel metal-gate MOS process with depletion load was used for chip fabrication. The process flow and the

layout rules are given in Appendices IV and V, respectively. The minimum transistor gate length was 20um in the operational amplifiers and 15um in the switches. One of the objectives of this experimental filter was to explore the maximum achievable dynamic range. In order to minimize the $\frac{kT}{C}$ noise, which is the fundamental noise source, a relatively large integrating capacitance was used for maximum driving capability of the operational amplifier. This integrating capacitance is about 100pF per stage (there are two integrating capacitors in one fully differential integrator stage). By using this capacitor size, the sampling capacitor was scaled down to about 4pF in the stages with low integrating to sampling capacitor ratio $(\frac{C_I}{C_S})$ and about 2pF in the stage with high capacitor ratio. Fig.6.1 shows the capacitor ratios and the sampling capacitor value for each integrator. Notice that the capacitor ratio in stage $\frac{1}{sC_1}$ and $\frac{1}{sC_5}$ is 13.74268, but in the chip layout $\frac{C_I}{C_S}$ was chosen as 12.74268. The reason is explained as follows. Two terminated bottom-plate switched-capacitor integrators in the filter configuration of Fig.5.9 are redrawn in Fig.6.2, where I_2 and I_4 represent the two internal voltage nodes in the filter structure as shown in Fig.2.4. The z-transform transfer function for Fig.6.2(a) is

$$V_1(z) = \frac{C_{S1}}{C_{S1} + C_{I1}}\left[\frac{V_{IN}(z)z^{-1} - I_2(z)}{1 - z^{-1}} + \frac{-V_1(z)z^{-1}}{1 - z^{-1}}\right], \quad (6.1)$$

Filter Clock Frequency : 256KHz

Chopper Frequency : 128KHz

Stage (Ref. to Fig.2.4(b))	Capacitor Ratio $(\frac{C_I}{C_S})$	Sampling Capacitor Size (C_S)
$\frac{1}{sC_1}$	13.74268	3.9pF
$\frac{1}{sL_2}$	16.43169	3.0pF
$\frac{1}{sC_3}$	23.66752	2.1pF
$\frac{1}{sL_4}$	16.43169	3.0pF
$\frac{1}{sC_5}$	13.74268	3.9pF

Fig.6.1 Capacitor ratio and value of the filter.

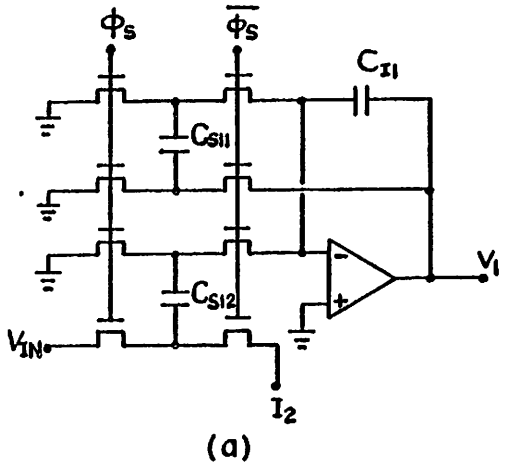


Fig.6.2 (a) Input and (b) output terminated stages in the filter of Fig.5.9.

where $C_{S11} = C_{S12} = C_{S1}$. The first term inside the brackets is the regular bottom-plate switched-capacitor integrator expression in z-domain. The second term is the one-clock cycle delay negative feedback from the output through C_{S11} to the output itself. When $\overline{\phi_s}$ is high, C_{S11} serves as a part of the integrating capacitor; therefore, the net integrating capacitance is $C_{S11} + C_{I1}$ instead of just C_{I1}. This mechanism gives an effective capacitor ratio of $\frac{C_{S1} + C_{I1}}{C_{S1}}$, even though the physical capacitance ratio remains $\frac{C_{I1}}{C_{S1}}$. In the output stage the z-transform transfer function is

$$V_{OUT}(z) = \frac{C_{S5}}{C_{S5} + C_{I5}}\left[\frac{I_4(z)z^{-1}}{1 - z^{-1}} + \frac{-V_{OUT}(z)z^{-1}}{1 - z^{-1}}\right]. \qquad (6.2)$$

The same effect results in an effective ratio of $\frac{C_{S5} + C_{I5}}{C_{S5}}$. If Eqs.(6.1) and (6.2) are rewritten as

$$V_1(z) = \frac{C_{S1}}{C_{I1}}\left[\frac{V_{IN}(z)z^{-1} - I_2(z)}{1 - z^{-1}} + \frac{-V_1(z)}{1 - z^{-1}}\right] \qquad (6.3)$$

and

$$V_{OUT}(z) = \frac{C_{S5}}{C_{I5}}\left[\frac{I_4(z)z^{-1}}{1 - z^{-1}} + \frac{-V_{OUT}(z)}{1 - z^{-1}}\right], \qquad (6.4)$$

the capacitor ratio is $\frac{C_{I1}}{C_{S1}}$ and $\frac{C_{I5}}{C_{S5}}$. The equivalent

termination in Eq.(6.1) (or Eq.(6.2)) is implemented with one clock cycle delay from the output of the integrator, while there is no delay in Eq.(6.3) (or Eq.(6.4)). For the complex-conjugate termination [20], the second term inside the brackets of Eq.(6.1) and (6.4) (or Eqs.(6.2) and (6.3)) form a complex-conjugate pair. Thus the physical $\frac{C_I}{C_S}$ ratios in the input stage and the output stage should be 12.74268 and 13.74268, or vice versa. Since the ratio of the filter clock frequency to the filter cutoff frequency is more than 75, the complex-conjugate termination is not necessary. Hence in this experimental prototype $\frac{C_{I1}}{C_{S1}}$ and $\frac{C_{I5}}{C_{S5}}$ ratio of 12.74268 is chosen in order to obtain a larger sampling capacitor C_{S1} and C_{S5} to minimize the $\frac{kT}{C}$ noise..

The die photomicrograph of this experimental chip is shown in Fig.6.3. This chip contains a fifth-order differential Chebyshev lowpass filter, a test operational amplifier and six test transistors. An HP3580A spectrum analyzer was used to measure both the frequency response of the on-chip operational amplifier and the filter as well as all the noise responses. The single-in to differential-in and the differential-out to single-ended conversion circuits as shown in Fig.6.4 were implemented by using LF356 (a low-noise JFET input operational amplifier) and metal-film resistors (having only pure thermal noise at low frequencies). By using these two kinds of external circuit parts, the noise introduced outside the test chip can be predicted

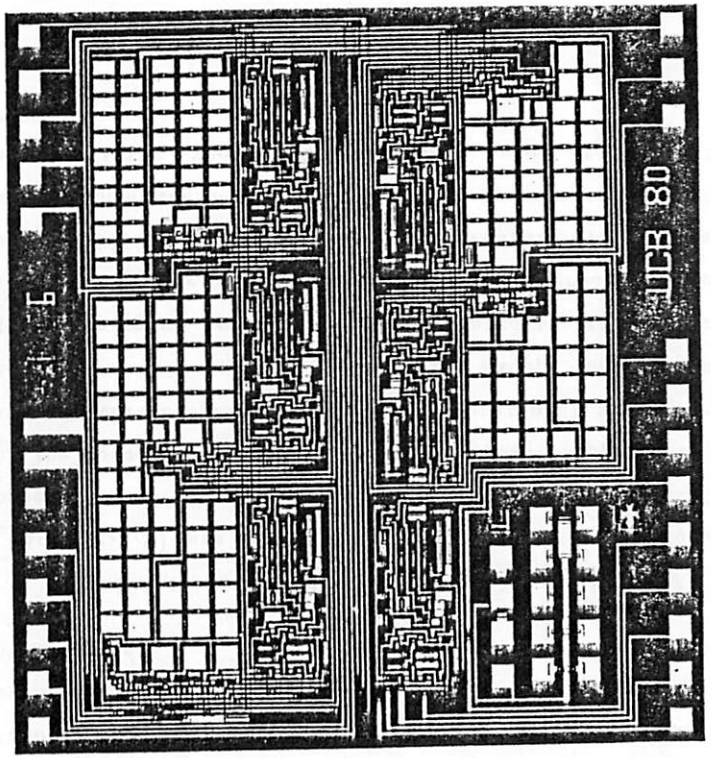


Fig.6.3 Die photomicrograph of an experimental fifth-order filter.

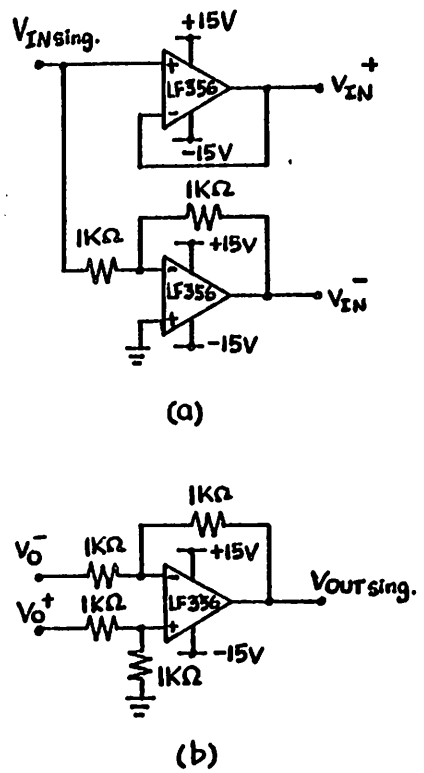


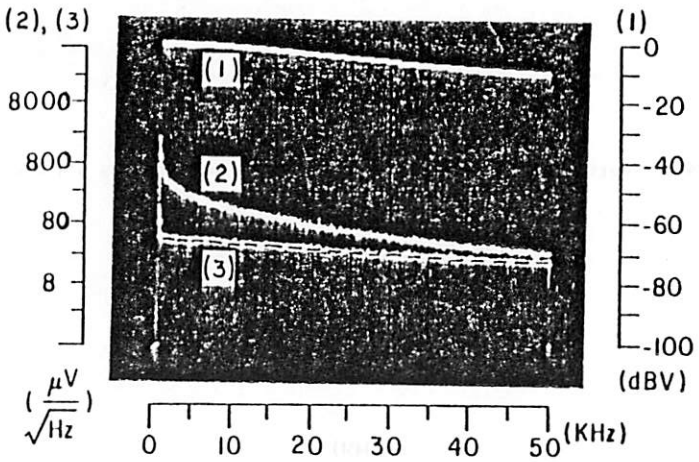
Fig.6.4 The test circuits for (a) a single-in to differential-in converter, and (b) a differential-out to single-ended converter.

and then be subtracted afterwards. The nominal power supplies (V_{DD} and V_{SS}) to the on-chip operational amplifier and the filter are + and - 7.5V. In order to obtain a low-distortion external test circuit with large on-chip differential signal swing, the LF356's were biased with + and - 15V supplies.

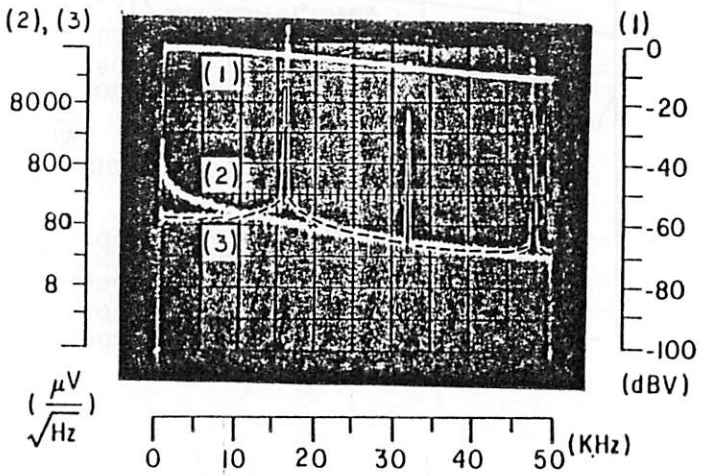
In order to ensure that the two filter clocks (ϕ_s and $\overline{\phi_s}$ in Fig.5.9) are non-overlapping, the filter clocks were chosen to have 30% duty cycle in all the measurements. During the noise measurements, all the DC power supplies to the external test circuit and the test operational amplifier or the filter were replaced by batteries except the power supply to the pulse generator which generated the filter master clock. The noise contribution from the external test circuits (LF356's and 1K metal-film resistors) were much smaller than the noise from the test operational amplifier and the filter. The measurements were taken at temperature of 25°.

6.2. NMOS Differential Chopper-Stabilized Operational Amplifier

The experimental results for the on-chip test operational amplifier are shown in Fig.6.5. The voltage transfer function measurement was taken by feeding an AC coupled



a) FOR CHOPPER FREQ (f_p) 128KHz



b) FOR CHOPPER FREQ (f_p) 16KHz

Fig.6.5 Operational amplifier output noise responses with and without chopper stabilization for chopper frequency at (a) 128KHz, and (b) 16KHz.

differential sinusoidal signal (which was internally generated by the HP3580A) and passing it through the circuit shown in Fig.6.5.(1). The differential input signal level was -60dBV. The test operational amplifier differential output frequency responses are shown in the curves labeled (1) of both Figs.6.5(a) and 6.5(b). The low-frequency open-loop voltage gain is about 57dB. The gain-bandwidth product is about 15MHz and the power dissipation is about 4mW.

Curve (3) of Fig.6.5(a) is the operational amplifier output noise response with the chopper frequency at its nominal value of 128KHz. Curve (2) of Fig.6.5(a) is the output noise response without chopper (i.e. the chopper is kept in one of the two possible states, either ϕ_p is kept on and $\overline{\phi_p}$ is kept off, or vice versa). In order to demonstrate further the translation of the $\frac{1}{f}$ noise the operational amplifier output noise was measured with the chopper frequency at one eighth of its nominal value, or 16KHz, with the results shown in the curve (3) of Fig.6.5(b). This was done because the frequency response of the HP3580A extends only to 50KHz. Curve (2) of Fig.6.5(b) has the same response as curve (2) of Fig.6.5(a) except with a 32KHz filter clock feedthrough.

The input referred noise, which is obtained by dividing the operational amplifier output noise by the voltage gain transfer function, is plotted in Fig.6.6. The dashed curve of Fig.6.6 is the input referred noise response without chopper stabilization. The bottom solid curve is the input

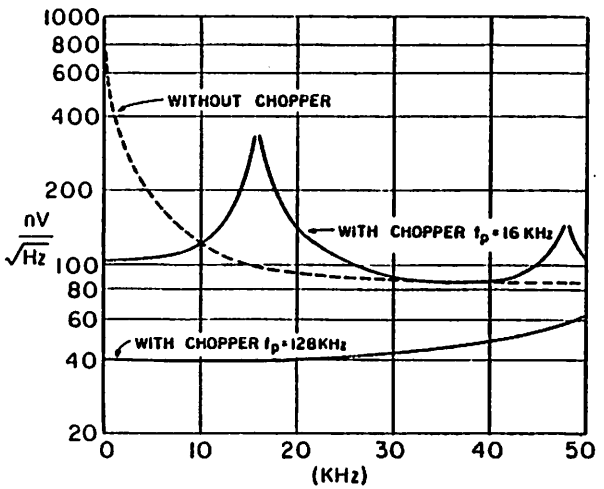


Fig.6.6 Experimental input referred noise of the operational amplifier.

referred noise response with the chopper frequency at 128KHz. In this case the noise at 1KHz is primarily due to the first fold-back 128KHz harmonic $\frac{1}{f}$ noise and the thermal noise of the operational amplifier. The total is about 40dB (100 times in noise power) less than that without chopper stabilization. The upper solid curve is the input referred noise response with the chopper frequency at 16KHz. The noise at 1KHz is about 12dB (16 times in noise power) less than that without chopper stabilization. The $\frac{1}{f}$ noise peak has been shifted to the odd harmonic frequencies of the chopper clock which are 16KHz and 48KHz in Fig.6.6. The noise at even harmonic frequencies, which is 32KHz in Fig.6.6, remains the same. This measurement confirms the analyses shown in Appendix III and section 4.3. (Eqs.(A.23) and (4.10)).

6.3. Fifth-order Chebyshev Lowpass Filter

The experimental results for the prototype fifth-order fully differential switched-capacitor Chebyshev lowpass filter were taken with the same single-in to differential-in and differential-out to single-ended conversion circuits which were used in measuring the performance of the on-chip test operational amplifier, except the differential input was DC coupled to the filter (i.e. the common-mode DC to the input of the filter was at ground level). The filter output

frequency response and the filter output noise response with and without chopper-stabilization were measured at filter clock frequencies of 64KHz, 128KHz, 256KHz, 512KHz and 1.06MHz. They will be shown and discussed in sections 6.3.1. and 6.3.2.. The dynamic range of the filter will be calculated in section 6.3.2.. The power supply rejection ratios (PSRR's) for V_{DD}, V_{SS} and V_{BB} of this differential filter will be presented in section 6.3.3..

6.3.1. Frequency Response

The observed filter differential output frequency response for the nominal filter clock frequency (256KHz) is shown in Fig.6.7 [27], where curve (a) is the overall response for frequency from DC to 50KHz, and curve (b) is the detailed passband response for frequency from DC to 5KHz. Curve (b) shows the passband response in a fine vertical scale of 1dB per division. The inband ripple is about ± 0.1dB. The cutoff frequency which is defined as the frequency at which the response leaves the ± 0.1dB window, is about 3400Hz.

The filter frequency response for different clock frequencies are shown in Figs.6.8(a) to.(f). The curves labeled (1) in these figures are the measurements with 10dB per vertical division. The curves labeled (4) and (5) are

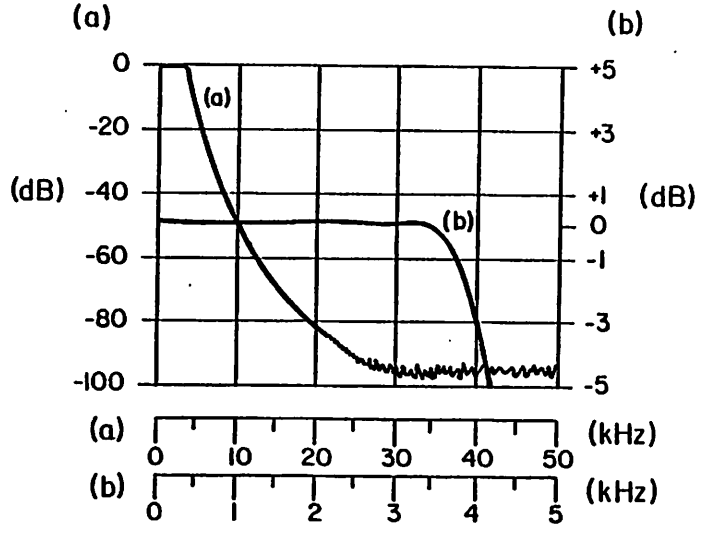
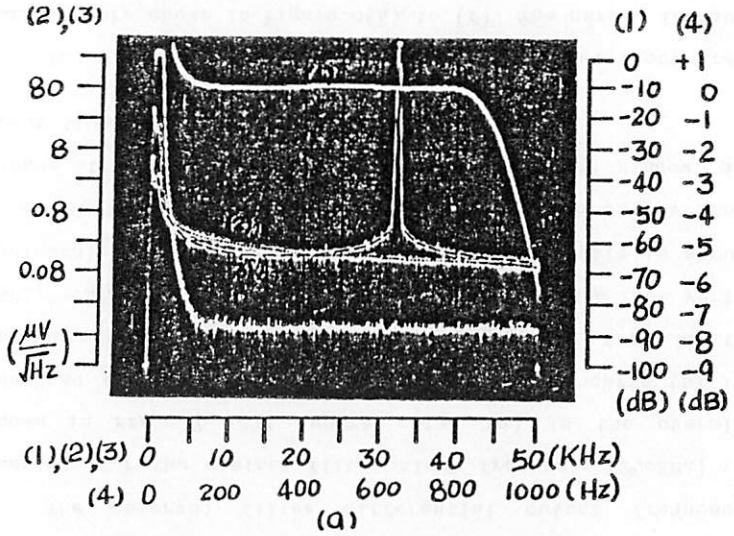


Fig.6.7 Experimental filter frequency response with filter clock frequency (f_c) of 256KHz: (a) overall response, and (b) detailed passband response.



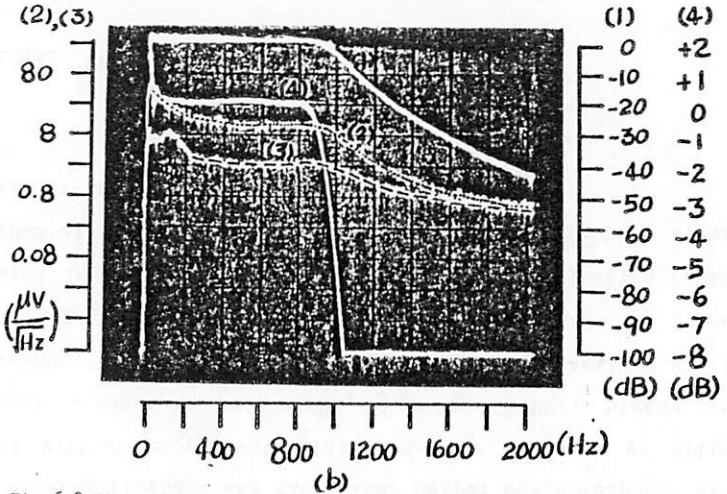


Fig.6.8 Filter frequency and noise responses: with 64KHz filter clock, (a) overall response, and (b) detailed passband response;

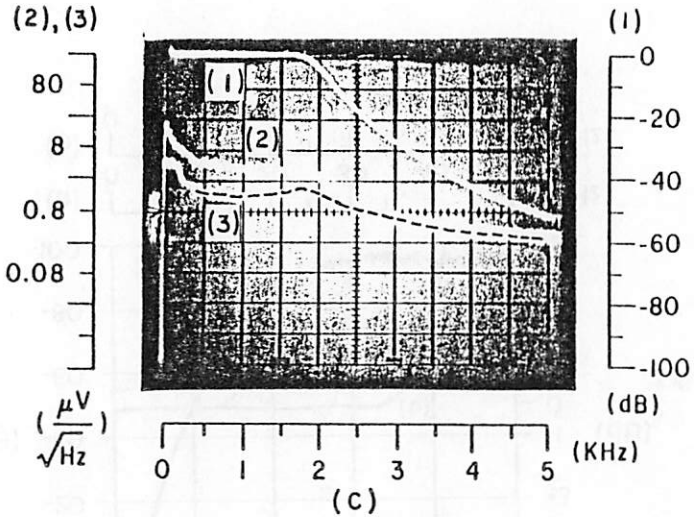


Fig.6.8 (c) with f_C=128KHz;

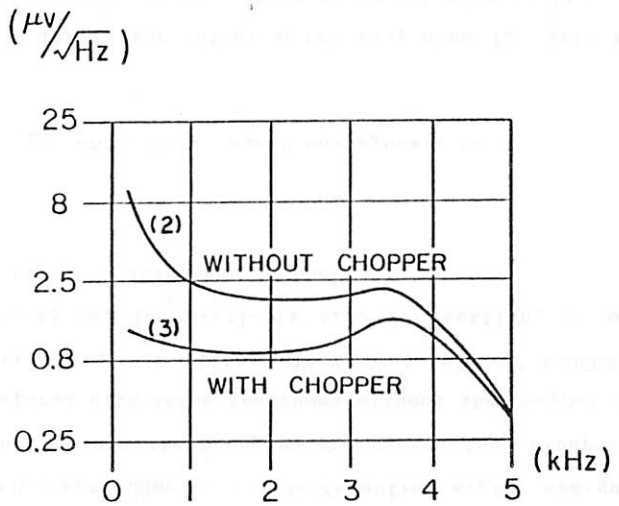
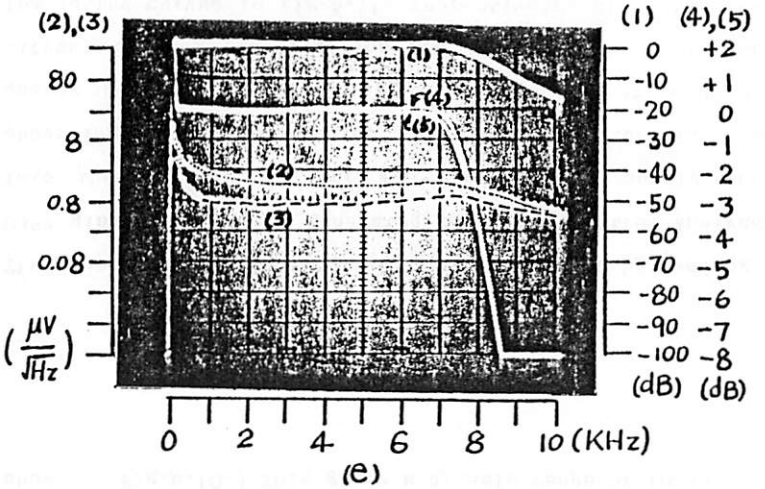


Fig.6.8 (d) with f_C=256KHz;



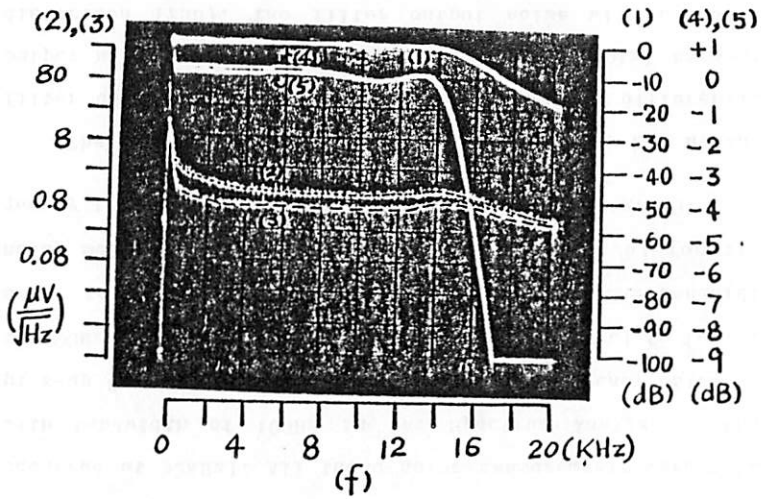


Fig.6.8 (e) with f_C=512KHz; and (f) with f_C=1.06MHz.

the detailed inband responses without and with chopper stabilization, respectively. The curves labeled (5) in Fig.6.8(a) and (b) are actually the same as the curves (4) in these two figures. As the filter clock frequency increased, the filter suffers from settling time limitations and shows a band-edge shift and larger inband ripple. The curves labeled (5) of Fig.6.8(e) and (f) are the responses with chopper in operating. At higher chopper frequency the chopper becomes mixed between two chopper states, therefore, the differential signal paths are no longer isolated from each other. Some of the differential signal charge has been lost through the choppers and causes the droop in gain as compared with those responses without the chopper operating. Notice that at filter clock frequency of 1.06MHz and 30% duty-cycle, the available time for settling in one charge transfer is less than 300nsec.

6.3.2. Noise Performance and Dynamic Range

The filter output noise responses for different clock frequencies are also shown in Figs.6.8(a) to (f). The curves labeled (2) (or the dotted curves) and the curves labeled (3) (or the dashed curves) are the noise responses without and with chopper stabilization, respectively. Curves (2) and (3) in Fig.6.8(a) are the overall responses of curves (2) and (3) of Fig.6.8(b), respectively. The noise energy at low

frequencies has been shifted to the odd harmonic frequencies of the chopper clock (shown in Fig.6.8(a) is the peak occurred at 32KHz). All these noise measurements were taken with bandwidth of 100Hz in the Spectrum Analyzer. 60Hz pick-up was shown as the "humps" at the frequency below 300 to 400Hz in the curves labeled (3) of Figs.6.8(b) to (e). In order to see the 60Hz pick-up in detail, a 10Hz bandwidth noise measurement of curve (3) of Fig.6.8(d) [26] for frequency from DC to 1KHz was taken and shown in Fig.6.9.

The experimental filter when operating at its nominal filter clock frequency of 256KHz had a maximum differential output signal swing of 5Vrms at 1KHz and 1% total harmonic distortion (THD). The filter output noise with C-message weighted was 40uVrms. (The C-message weighting function is shown in Fig.6.10.) This gives a dynamic range of 102dB.

6.3.3. Power Supply Rejections

The power supply rejection ratios were measured by feeding a 0dBV sinusoidal signal generated from the Spectrum Analyzer into the V_{DD} (or V_{SS}, or V_{BB} (body bias)) supply, and observing the response at the output of the filter. The frequency response appearing at the filter output with and without chopper stabilization are shown as the dashed and the dotted curves in Fig.6.11, respectively. Since the perturbation to the power supplies is 1Vrms, which is a

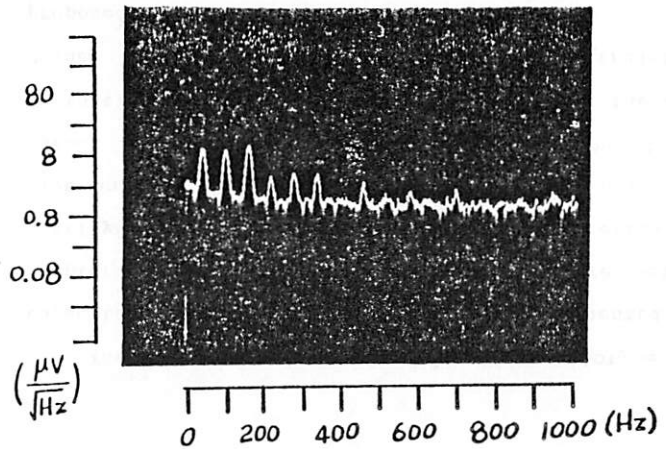


Fig.6.9 Detailed filter noise response with chopper frequency 128KHz and with 10Hz bandwidth measurement.

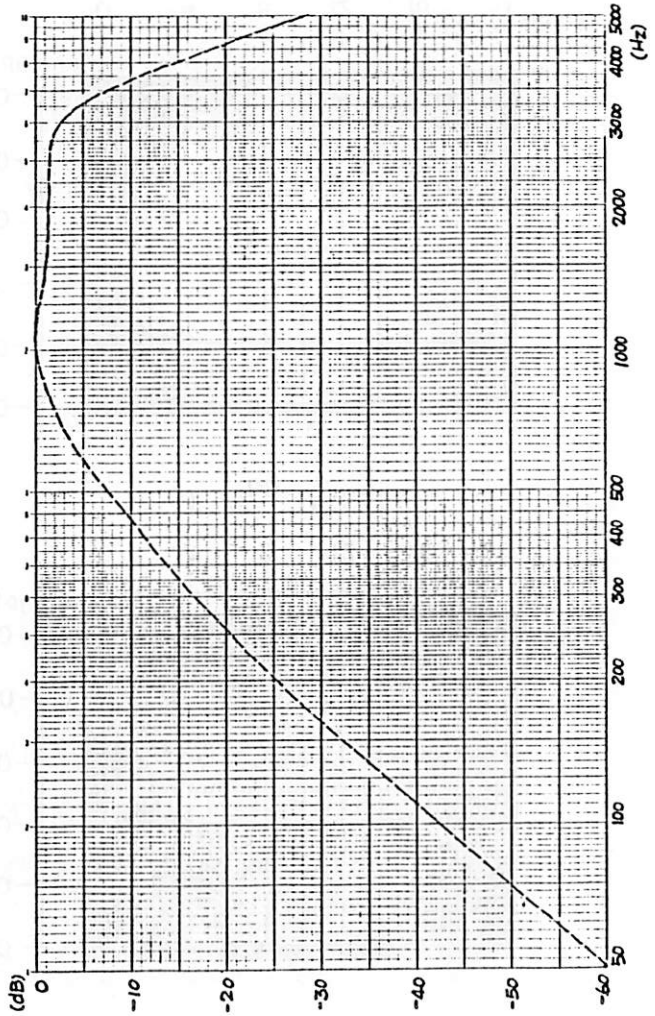


Fig.6.10 C-message weighting function.

large signal level, the responses shown in Figs.6.11(a) to (c) are the large signal power supply rejection ratios. The peaks (the frequency in which the minimum supply rejection occurs) of the dotted curves appear at the band-edge of the filter frequency response. This phenomenon will be explained in section 6.4.3.. For frequency range up to 20KHz, the minimum power supply rejection ratio is 50dB for both V_{DD} and V_{SS} supplies when the chopper is in operating.

6.4. Discussions

The experimental results for the prototype switched-capacitor lowpass filter have been presented in this chapter. At this point some discussions are necessary to clarify the correspondence between the theoretical calculation and the measured data for the filter noise and frequency responses, the mismatch problem in the chip and the distortion due to the filter structure. From the experience gained in this filter design, some better circuits will be proposed.

6.4.1. Contributions of Noise sources in the Filter

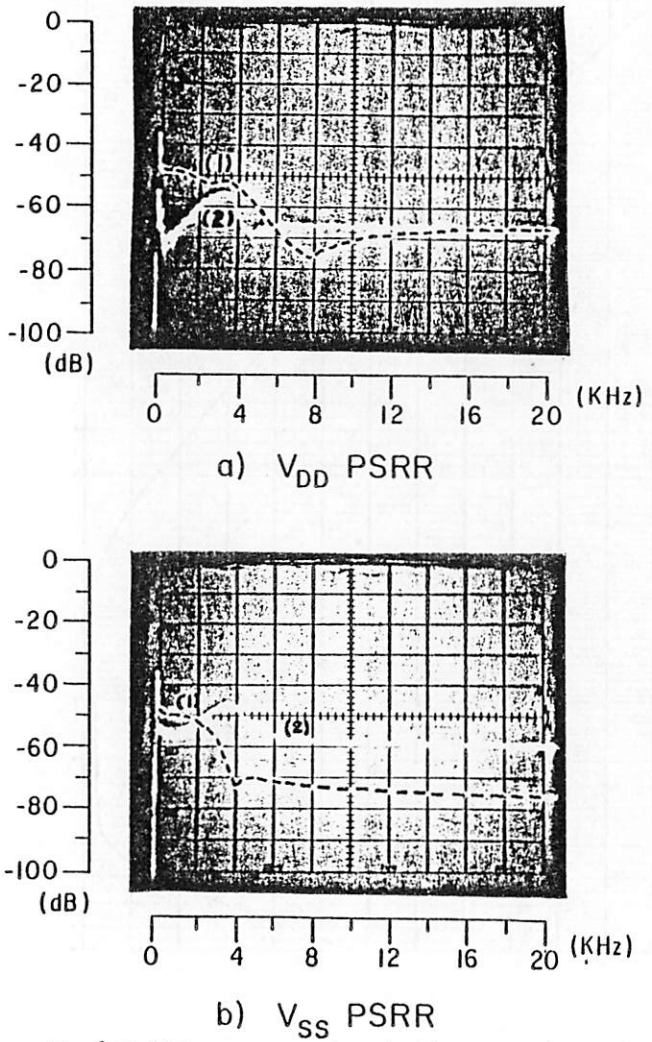


Fig.6.11 Filter power supply rejection ratios (PSRR's) with (dashed curves) and without (curver (2)) chopper stabilization for (a) V_{DD}, and (b) V_{SS}.

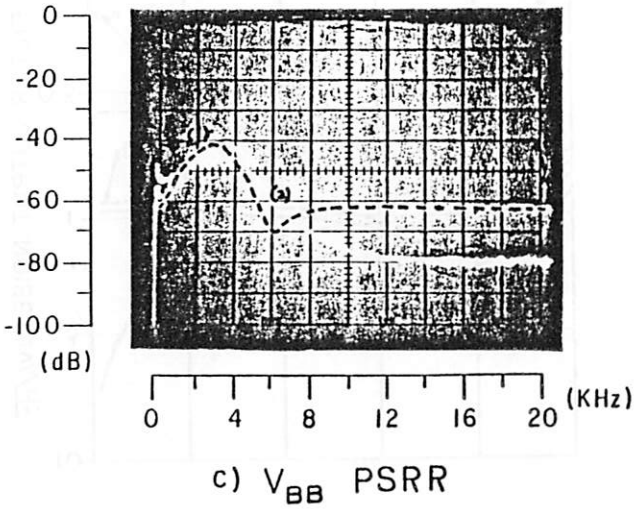


Fig.6.11(c) PSRR of V_{BB}.

This section will only discuss the performance with nominal chopper frequency (128KHz) whenever the chopper stabilization is mentioned.

By using the filter noise calculation method discussed in section 2.2.2. and the measured on-chip test operational amplifier noise responses, with and without chopper stabilization, a theoretical noise performance of the filter configuration shown in Fig.5.9 is calculated and plotted in Fig.6.12. The contribution of three noise sources, the $\frac{1}{f}$ noise and the thermal noise of the operational amplifier and the $\frac{kT}{C}$ noise, are individually calculated under the following assumptions. The equivalent input $\frac{1}{f}$ noise of the operational amplifier is the dashed curve in Fig.6.6 which is about 400nV/ $\sqrt{Hz}$ at 1KHz. The theoretical $\frac{1}{f}$ noise calculation with chopper stabilization is based on this measurement and Eq.(A.23). The first fold-back $\frac{1}{f}$ noise at 1KHz for chopper frequency Of 128KHz is about 23nV/ $\sqrt{Hz}$. Therefore the noise density of 40nV/ $\sqrt{Hz}$ at 1KHz in the bottom curve of Fig.6.6 can be used as the equivalent input thermal noise of the operational amplifier.

Fig.6.12 shows each of the three noise components with and without chopper stabilization. Since the operational amplifier thermal noise and the $\frac{kT}{C}$ noise are the wideband noise, they are not affected by modulation schemes like chopper stabilization. Eq.(A.25) explains this fact. With chopper stabilization in operation, for frequency range from

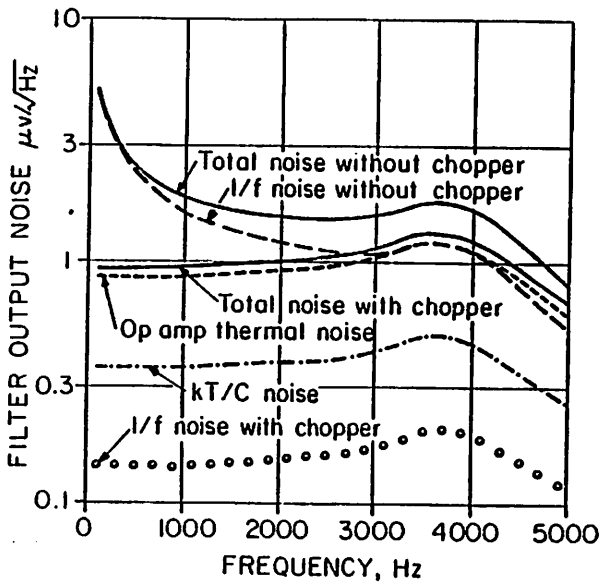


Fig.6.12 Theoretical noise calculation of the experimental filter with and without chopper stabilization.

DC to 5000Hz, the total $\frac{kT}{C}$ noise density is about 10dB higher than the total chopped $\frac{1}{f}$ noise density, and the total operational amplifier thermal noise density is another 10dB higher. Without chopper stabilization, the " $\frac{1}{f}$ noise corner frequency" of this filter is about 3000Hz which falls near the band-edge; therefore, the total noise without chopper stabilization is mainly dominated by the unchopped $\frac{1}{f}$ noise . The total noise with chopper stabilization primarily follows the total operational amplifier thermal noise curve. With chopper stabilization in operation, at 1KHz the operational amplifier noise is reduced by 40dB, while the filter output noise decreases only by 10dB. The reason is that a 40dB noise reduction in the operational amplifier is the reduction in the "noise density" of a single operational amplifier. For a sample and hold process like the switched-capacitor filter, the aliasing effect of the wideband noise (the operational amplifier thermal noise and the $\frac{kT}{C}$ noise) must be considered. In this prototype filter the aliased operational amplifier thermal noise becomes the dominant noise mechanism when the chopper is operating. The result is 10dB improvement.

Fig.6.13 shows the theoretical and measured filter output noise response for with and without chopper stabilization. Comparing these results, a very good matching occurs in the case with the chopper operating. There is about 2dB difference in the case without chopper stabilization. The $\frac{1}{f}$ noise density in the calculations is obtained from the

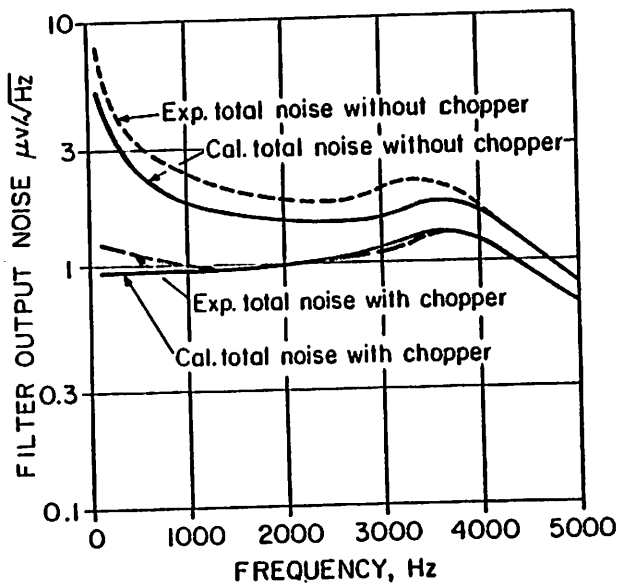


Fig.6.13 Comparison for theoretically calculated and experimentally observed total filter output noise response with and without chopper stabilization.

measurement of the on-chip test operational amplifier and is assumed constant through the five operational amplifiers in the filter, although this may not be true in a fabricating process having large variations. A 2dB (or 25%) variation among the operational amplifiers is reasonable.

6.4.2. Mismatch Effect in Filter Frequency Response

An inband ripple of 0.1dB and an operational amplifier differential open-loop voltage gain of 2000 were assumed in the design of this Chebyshev lowpass filter. The process variation brought down the operational amplifier voltage gain and the unity-gain frequency, and increased the inband ripple as well [21]. The operational amplifier chip layout was not mirrored to insure balanced matching. However, this is a good opportunity to study the mismatch problem in the fully differential circuit. One effect of this problem is the different filter frequency responses at the two differential outputs. Figs.6.14(a) and (b) show the frequency responses at the outputs V_0^+ and V_0^-, respectively. The curves labeled (2) are the detailed passband response of the curves labeled (1). A transmission-zero-like drop occurs at a frequency of 20KHz at one side (Fig.6.14(a)) but not at the other side (Fig.6.14(b)). This drop was merged in the filter differential output frequency response (Fig.6.7).

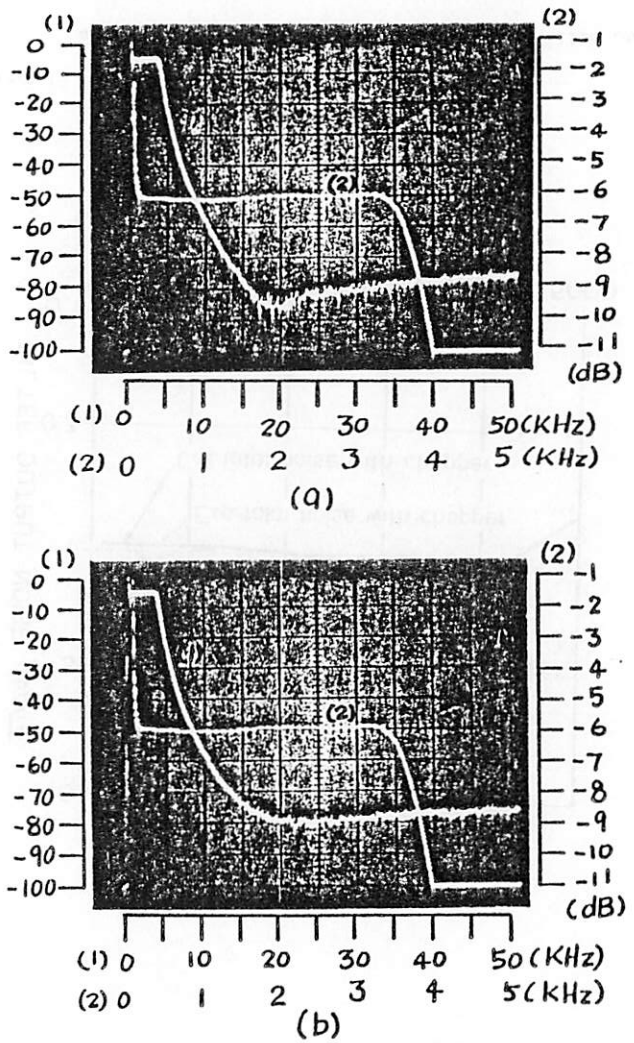


Fig.6.14 Overall and detailed filter passband frequency response at (a) + output, and (b) - output.

6.4.3. Distortion in the Filter

The filter is a symmetrical ladder structure (a Chebyshev lowpass filter). Its passive filter configuration shown in Fig.2.4(a) has C_1 equal to C_5 and L_2 equal to L_4. Therefore the transfer functions between voltage nodes and currents obey some identities, for example $\frac{I_4(s)}{V_{IN}(s)} = \frac{V_{OUT}(s)}{I_2(s)}$ and $\frac{V_3(s)}{V_{IN}(s)} = \frac{V_{OUT}(s)}{V_3(s)}$. The transfer functions (shown in Fig.2.5) for the noise from the internal nodes to the output can be used as the transfer functions for the signal from the input to the "mirrored" internal nodes such as $H_{n1} = \frac{V_{OUT}}{V_{IN}}$, $H_{n2} = \frac{I_4}{V_{IN}}$, $H_{n3} = \frac{V_3}{V_{IN}}$, $H_{n4} = \frac{I_2}{V_{IN}}$ and $H_{n5} = \frac{V_1}{V_{IN}}$. H_{n2} to H_{n5} show the peakings around the band-edge. H_{n4} has almost a 6dB peak (twice in amplitude) at the band-edge. These internal node peakings cause larger signal swings than that appearing at the output. With fixed power supplies in the active filter shown in Fig.2.4(b), the peaking signal is clamped and the distortion increases. Furthermore, the phase responses of the internal nodes show phase diversification as the frequency increases to band-edge. Fig.6.15 shows the examples for frequencies of 1000Hz and 3400Hz. The reference is V_{IN} (0dB, 0^o) in phasor representation. If V_{IN} is (1V, 0^o), the $\frac{1}{sC_3}$ stage at 3400Hz will sample two signals of (1.68V, -54^o) and (1.5V, $+177^o$). The net input to the $\frac{1}{sC_3}$ stage is then equal to (2.87V, -27^o) at 3400Hz, which is

	@ 1000Hz	@ 3400Hz
V_{IN}	0dB, 0°	0dB, 0°
V_1	-1.2dB, -6°	+1.0dB, +3°
I_2	+1.1dB, -11°	+4.5dB, -54°
V_3	-0.6dB, -34°	+3.3dB, -123°
I_4	+0.5dB, -40°	+3.6dB, +177°
V_{out}	-0.1dB, -59°	-0.1dB, +126°

Fig.6.15 Gain peaking and phase diversification in the internal nodes of the filter.

total of a 9dB gain increase. (The net input is (0.56V, +55°) at 1000Hz.) The gain peaking and the phase diversification in the internal nodes of an active filter are the important considerations in designing a low distortion switched-capacitor filter. They can be suppressed by using the loop-scaling technique [22]. The loop-scaling technique requires more sampling capacitors and therefore may introduce higher $\frac{kT}{C}$ noise at the output of the filter. This effect should be considered in filter design.

6.4.4. Proposed New Circuits

In light of the discussions of the previous sections, some considerations for designing a high performance low-noise chopper-stabilized differential switched-capacitor filter can be achieved. These suggestions are:

(1) use a mirrored layout in the operational amplifier to insure full balancing of the signal paths and matching;

(2) design a low thermal noise input stage for the operational amplifier;

(3) design a low wideband noise output stage for the operational amplifier, or design an operational amplifier without an output voltage buffer; and

(4) scale node voltages (loop-scaling technique) in the filter so that optimum dynamic range is obtained.

In order to interface with the single-ended input and output systems, a single-in to differential-in and a differential-out to single-ended conversions are necessary. These conversions can not degrade the good power supply rejections in the differential circuit. Two circuits shown in Figs.6.16 and 6.17 are proposed to meet this requirement. They are bottom-plate parasitic free and chopper-stabilized. The input signal to one side of the integrator shown in Fig.6.16 is delayed by one-half clock cycle from the other side. Therefore, the effective differential input is $V_{IN}(1 + z^{-\frac{1}{2}})$ in the z-domain. At a filter clock frequency to filter cutoff frequency ratio of more than 75 ($\frac{256KHz}{3.4KHz}$), the maximum phase error is less than 2.4^{o} and the maximum gain error is less than 0.022% through the frequency range from DC to 3.4KHz, that will not degrade the filter response.

Fig.6.17 shows a chopper-stabilized differential to single-ended converter. This converter is essentially a terminated differential switched-capacitor integrator (a one-pole lowpass filter). The chopper-stabilized operational amplifier used in herd here is a fully differential type with only one output connected to the negative feedback network. The switched-capacitors C_{RS2} and C_{RI2} and capacitor C_{IO2} attached to the non-inverting node of the amplifier are the replica circuits of those in the signal path (which contains C_{RS1}, C_{RI1} and C_{IO1}). Here, $C_{RS1} = C_{RS2}$, $C_{RI1} = C_{RI2}$

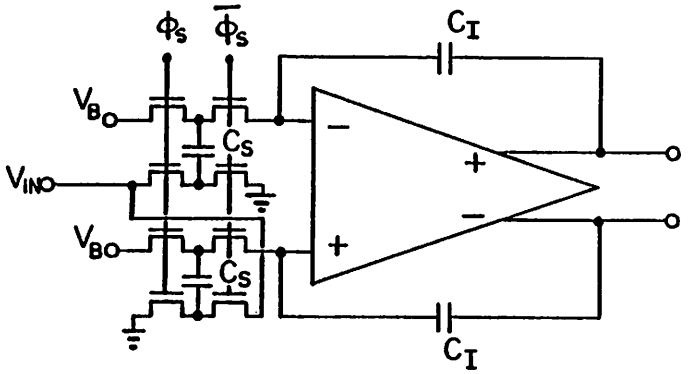


Fig.6.16 A single-in to differential-in converter.

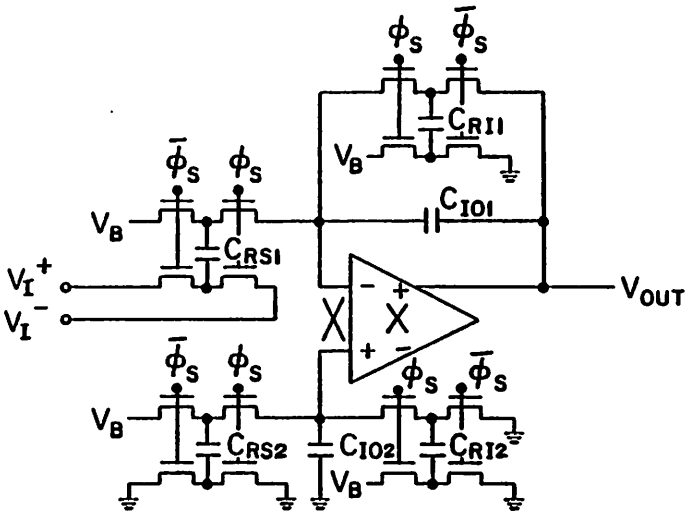


Fig.6.17 A differential-out to single-ended converter.

and $C_{IO1} = C_{IO2}$. The z-transform transfer function for the converter is

$$v_{OUT}(z) = \frac{C_{RS1}}{C_{RI1}} \frac{-v_I^-(z) + v_I^+(z)z^{-\frac{1}{2}}}{\frac{C_{IO1}}{C_{RI1}} - \left[\frac{C_{IO1}}{C_{RI1}} - 1\right]z^{-1}}. \tag{6.5}$$

If $C_{RI1} = C_{IO1}$, then

$$v_{OUT}(z) = \frac{C_{RS1}}{C_{RI1}} \left[-v_I^-(z) + v_I^+(z)z^{-\frac{1}{2}}\right] \tag{6.6}$$

which is a function of the difference between v_I^- and v_I^- delayed by half of a clock cycle. When ϕ_s is turned on the instantaneous charge Q_{inst}, in z-domain, transferred into the integrating capacitor is

$$\begin{aligned} Q_{inst} &= C_{RI1}v_{OUTinst} + C_{RS1}(v_{Iinst}^- - v_{Iinst}^+) \\ &= C_{RS1}\left[v_{Iinst}^+(z) - v_{Iinst}^-(z)\right](1 - z^{-1}) \end{aligned} \tag{6.7}$$

which is the charge difference between sampled differential input signal $v_I^+ - v_I^-$ and that with one clock cycle delay. Compared with reversing the clocks ϕ_s and $\bar{\phi}_s$ in the switched-capacitor C_{RS1}, the clock scheme as described minimizes the output voltage change per cycle. Notice that ϕ_s and $\bar{\phi}_s$ to the switched-capacitor C_{RS1} are chosen such

that when the differential outputs of the filter (v_0^+ and v_0^- of Fig.5.9) are connected to v_I^+ and v_I^-, there is no delay between v_0^+ and v_0^-. This is due to the fact that when ϕ_s is high v_0^- is held by the integrating capacitor of the $\frac{1}{sC_5}$ stage at the same value as it was one half clock cycle before (when $\overline{\phi_s}$ is turned on).

These two circuits, which perform differential to single-ended and single-ended to differential conversions in sample-data domain without losing all the advantages of using fully-differential circuitry, solve the input/output problems which are inherent to a fully-differential switched-capacitor filters.

CHAPTER 7

CONCLUSIONS

A new low-noise chopper-stabilized differential switched-capacitor filtering technique has been developed. This technique enables the filter to be scaled down in size, in accordance to the decrease in the technological feature size, without increasing the use of any additional capacitors in the filter. The noise analyses in a sample and hold circuit, such as switched-capacitor filter, and in an operational amplifier with and without the output voltage buffer were made. The results from these analyses have led to the design technique of a low-noise switched-capacitor filter circuits.

An MOS differential chopper-stabilized operational amplifier without internal level shifter and an experimental prototype fifth-order lowpass filter have been designed and fabricated. The operational amplifier meets the requirement of driving a total of 100pF integrating capacitance in one stage of a switched-capacitor integrator. The prototype filter demonstrated a power supply rejection ratio of 50dB and a dynamic range of 102dB.

APPENDIX I. TRANSIENT THERMAL NOISE [5]

A basic switched-capacitor circuit contains an MOS switch and a sampling capacitor. Since the switch is turned on and off by a clock, the process of this system is nonstationary. This Appendix will show the transient analysis of the thermal noise from the channel of the MOS switch. Fig.A.1 shows the model for the transient thermal noise analysis which includes a noise source $v_R(t)$, a noiseless resistor R and an ideal switch turned on at t=0. In this linear system, the autocorrelation function of the stationary thermal noise source $v_R(t)$ is

$$R_{RR}(t_1, t_2) = \begin{cases} 2kTR\delta(t_1, t_2) & t_1 \geq 0,\ t_2 \geq 0 \\ 0 & \text{otherwise} \end{cases} \qquad (A.1)$$

where $\delta(t)$ is Dirac delta function, and t_1 and t_2 are two time variables. The system impulse function is

$$h_{A1}(t) = \frac{1}{RC} e^{-t/RC} u(t) \qquad (A.2)$$

where u(t) is the unit step function.

The output autocorrelation function for $v_C(t)$ is

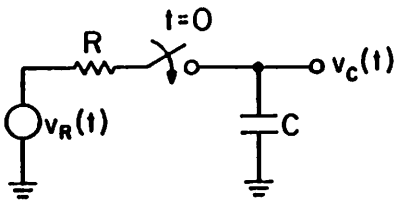


Fig.A.1 Model for transient thermal noise analysis.

$$R_{CC}(t_1,t_2) = R_{RR}(t_1,t_2) * h_{A1}(t_1) * h_{A1}(t_2)$$

$$= \begin{cases} \frac{kT}{C}\left[1 - e^{-2t_2/RC}\right]e^{-(t_1-t_2)/RC} & \text{for } t_1 \geq t_2 \\ \frac{kT}{C}\left[1 - e^{-2t_1/RC}\right]e^{-(t_2-t_1)/RC} & \text{for } t_1 \leq t_2 \end{cases}$$

(A.3)

where "*" is the convolution operator. For a long observation time, $e^{-2t_2/RC} \ll 1$ (or $e^{-2t_1/RC} \ll 1$), Eq.(A.3) becomes

$$R_{CC}(t+\tau,t) \rightarrow \frac{kT}{C} e^{-|\tau|/RC} \qquad (A.4)$$

which corresponds to the expected noise variance of

$$E\left\{v_C^2(t,u)\right\} = R_{CC}(t,t)$$

$$= \frac{kT}{C}. \qquad (A.5)$$

This result matches the result in Eq.(2.3) under the condition that the time constant RC is much smaller than the observation time (t_1 or t_2 in Eq.(A.3)). This is always true, because for a complete charging or discharging of a sampling capacitor in the switched-capacitor filter, the RC time constant must be much smaller than the switch turn on

time (the observation time).

APPENDIX II. SAMPLED WIDEBAND NOISE ($\frac{kT}{C}$ NOISE) IN SWITCHED-CAPACITOR INTEGRATOR

This appendix will analyze the effect of the $\frac{kT}{C}$ noise sampled by C_{S1} from $\overline{v_{R13}^2}$ in a switched-capacitor integrator configuration, and its equivalent noise in the integrator. The same model as shown in Fig.2.1(b) and 2.1(c) will be used in the analysis of this Appendix. The voltage waveform across the integrating capacitor C_I due to the noise source $\overline{v_{R13}^2}$ is shown in Fig. A.2. The noise sampled by C_{S1} from $\overline{v_{R13}^2}$ will transfer to C_I with a time constant $R_{ON24}C_{S1}$ defined as 1/B. Assuming the clock has a 50% duty cycle and the leakage through C_I has a time constant $1/\gamma$, the impulse response of the system is

$$h_{A2}(t) = \begin{cases} 0 & t < 0 \\ e^{-\gamma t}\,(1- e^{-Bt}) & 0 \le t \le T_C/2. \\ e^{-\gamma t}\,(1- e^{-BT_C/2}) & t > T_C/2 \end{cases} \qquad (A.6)$$

The voltage waveform across C_I is

$$v_{CI}(t) = \sum_{m=-\infty}^{\infty} v_{R13m} h_{A2}(t-mT_C+\theta) \qquad (A.7)$$

where v_{R13m} is the m-th sample from v_{R13}, which has the following properties:

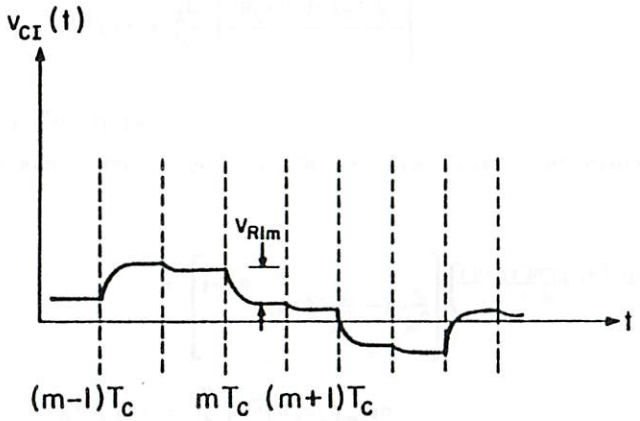


Fig.A.2 $v_{CI}(t)$ waveform due to v_{R13} in Fig.2.1.

$$E[v_{R13m}(t)] = 0 \tag{A.8}$$

$$E[v_{R13m}(t)\ v_{R13n}(t)] = \begin{cases} c^2 \frac{kT}{C_{S1}} = \sigma^2 & m=n \\ 0 & m \neq n \end{cases} \tag{A.9}$$

assuming that the $R_{OH24}C_{S1}$ time constant is much smaller than the ϕ_2 clock turn on time and the DC voltage gain of the operational amplifier is high enough. The variable θ is uniformly distributed on $[0,T]$ to insure a stationary random process. θ and v_{R13m} are independent.

The autocorrelation function of $v_{CI}(t)$ is

$$R_{II}(t) = E[v_{CI}(t)\ v_{CI}(t+\tau)]$$

$$= \sigma^2 \sum_m \frac{1}{T_C} \int_0^{T_C} h_{A2}(t-mT+\theta)\ h_{A2}(t+\tau-mT+\theta)d\theta$$

$$= \frac{\sigma^2}{T_C} \int_{-\infty}^{+\infty} h_{A2}(u)\ h_{A2}(u+\tau)du \tag{A.10}$$

where $u = t-mT_C+\theta$. The power spectrum $S_{CI}(\omega)$ corresponding to $v_{CI}(t)$ is the Fourier transform of $R_{II}(\tau)$, that is

$$S_{CI}(\omega) = \frac{\sigma^2}{T_C} \int_{-\infty}^{+\infty} e^{-j\omega\tau} \left[\int_{-\infty}^{+\infty} h_{A2}(u)\ h_{A2}(u+\tau)du \right] d\tau$$

$$= \frac{\sigma^2}{T_C} \int_{-\infty}^{+\infty} h_{A2}(u)e^{-j\omega u}du \int_{-\infty}^{+\infty} h_{A2}(v)e^{j\omega v}dv$$

$$= \frac{\sigma^2}{T_C} \left| H_{A2}(j\omega) \right|^2 \tag{A.11}$$

where $v = u-\tau$, and $H_{A2}(j\omega)$ is

$$H_{A2}(j\omega) = \int_{-\infty}^{+\infty} h_{A2}(u)e^{-j\omega u}du$$

$$= \left[1 - e^{-(B+\gamma)\frac{T_C}{2} - j\omega\frac{T_C}{2}} \right] \left[\frac{B}{(B+\gamma+j\omega)(\gamma+j\omega)} \right]. \tag{A.12}$$

In most cases, the leakage is very small, therefore $B >> \gamma$, and $S_{CI}(\omega)$ becomes

$$S_{CI}(\omega) = \frac{\sigma^2}{T_C} \left[\frac{B^2}{(B^2+\omega^2)(\gamma^2+\omega^2)} \right] \cdot \left[1 + e^{-BT_C} - 2e^{-B\frac{T_C}{2}} \cos \omega\frac{T_C}{2} \right]. \tag{A.13}$$

For the typical values of $1/B$ and T_C on the order of 10^{-8} sec and 10^{-5} sec, respectively, $S_{CI}(\omega)$ becomes

$$S_{CI}(\omega) = \frac{\sigma^2}{f_C} \frac{B^2}{(B^2+\omega^2)(\gamma^2+\omega^2)} \qquad (A.14)$$

which can be simplified further as

$$S_{CI}(\omega) = \frac{\sigma^2}{f_C} \frac{1}{\omega^2}$$

$$= c^2 \frac{kT}{C_{S1}} \frac{f_C}{\omega^2} \qquad (A.15)$$

under the conditions that the frequencies of interest are much smaller than B and the leakage is negligible ($\gamma \simeq 0$).

From Eq.(2.1), the power transfer function of a switched-capacitor integrator is

$$\left|H_{SC}(j\omega)\right|^2 = \frac{c^2}{4 \sin^2 \frac{\omega f_C}{2}} \qquad (A.16)$$

thus, the input power spectrum from Eq.(A.15) is

$$S_i(\omega) = \frac{kT}{C_{S1} f_C} \frac{\sin^2 \frac{\omega f_C}{2}}{\left(\frac{\omega f_C}{2}\right)^2}. \qquad (A.17)$$

For $x \ll 1$, $\sin^2 x \simeq x^2$, Eq.(A.17) then becomes

$$S_i(\omega) \simeq \frac{kT}{C_{S1} f_C} \qquad (A.18)$$

which is the equivalent input $\frac{kT}{C}$ noise power density due to the thermal noise in the channels of switches M_1 and M_3.

APPENDIX III. MODULATION OF THE $\frac{1}{f}$ NOISE

The modulation effect of the $\frac{1}{f}$ noise by the use of the chopper-stabilized technique will be examined in this Appendix. Let x(t) be the sign function shown in Fig.A.3(a). The Fourier transform functions of x(t), $v_{n1}(t)$ and $v_{neq}(t)$ (= $v_{n1}(t)x(t)$) of Fig.4.4 are

$$X(f) = F[x(t)]$$

$$= \sum_{m=1}^{\infty} \frac{2}{(2m-1)\pi} \{\delta[f-(2m-1)f_p] - \delta[f+(2m-1)f_p]\} \quad (A.19)$$

$$V_{N1}(f) = F[v_{n1}(t)] \quad (A.20)$$

$$V_{NEQ}(f) = F[v_{n1}(t)x(t)]$$

$$= \sum_{m=1}^{\infty} \frac{2}{(2m-1)\pi} \{V_{N1}[f-(2m-1)f_p] - V_{N1}[f+(2m-1)f_p]\}, \quad (A.21)$$

where $f_p = \frac{1}{T_p}$ is the chopping frequency. If v_{n1} is the $\frac{1}{f}$ noise, its power spectrum can be defined as $S_{N1}(f)$, and the power spectra corresponding to $V_{N1}(f)$ and $V_{NEQ}(f)$ are

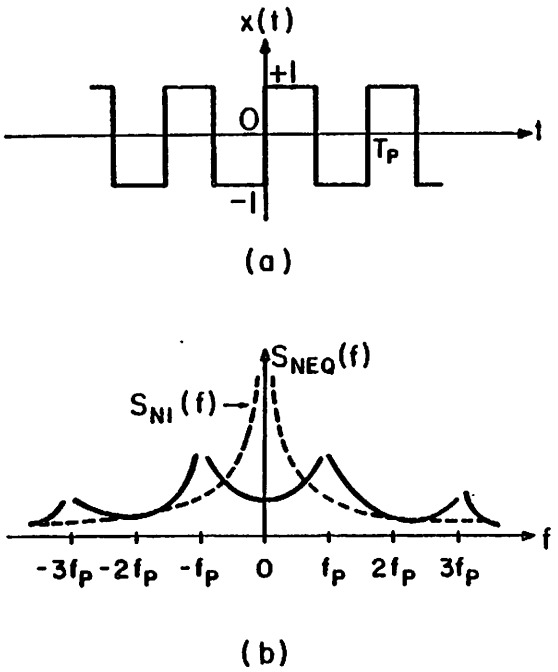


Fig.A.3 (a) Sign function x(t) with frequency $f_p = \frac{1}{T_p}$, (b) modulated $\frac{1}{f}$ noise.

$$S_{N1}(f) = \frac{K_1/2}{|f|} \qquad (A.22)$$

$$S_{NEQ}(f) = \sum_{m=1}^{\infty} \left[\frac{2}{(2m-1)\pi}\right]^2 \left[\frac{K_1/2}{|f-(2m-1)f_p|} + \frac{K_1/2}{|f+(2m-1)f_p|}\right] \qquad (A.23)$$

where K_1 is a constant of the $\frac{1}{f}$ noise. Fig.A.3(b) shows these "harmonic $\frac{1}{f}$ noise" components, they are shifted to the odd harmonic frequencies of f_p.

But, if v_{n1} is white noise with power density of

$$S_{N1}(f) = 2kTR_{N1} \qquad -\infty < f < +\infty, \qquad (A.24)$$

then

$$S_{NEQ}(f) = \sum_{m=1}^{\infty} \left[\frac{2}{(2m-1)\pi}\right]^2 4kTR_{N1}$$

$$= 2kTR_{N1} \qquad -\infty < f < +\infty. \qquad (A.25)$$

This result indicates the white noise has no modulation effect due to the sign function x(t).

APPENDIX IV. NMOS METAL-GATE DEPLETION-ENHANCEMENT PROCESS

The process used to fabricate the experimental prototype circuits in this research work is described in this appendix. The process evolved to its present form through previous efforts [23],[24],[4]. Boron implantation is used in channel-stop (p^+ isolation). Positive photoresistor is used in all photolithographic steps in the process. The substrate is boron-doped p-type <100> orientation with 25 to 50 ohm-cm resistivity. This process is intended to fabricate the threshold voltages (without body-bias) of 0.7V and -3.0V for enhancement and depletion devices.

Fabrication Sequence:

1. Initial Wafer Cleaning:
   1) TCE, 60°C, 10mins.
   2) Acetone, room temperature (R.T.), 2mins.
   3) Deionized water (DI) rinse, 1 to 2 mins.; N_2 blow dry.
   4) Piranha clean, H_2SO_4:H_2O_2 (5:1), self-heat to about 90°C, 15mins.

5) DI rinse, 1 to 2 mins.; N_2 blow dry.

6) Dip in HF:H_2O (1:5), 30secs.

7) DI rinse, 1 to 2 mins.; N_2 blow dry.

2. Initial Oxidation: N-type drive-in furnace, 0.92um wet oxide.

1) Push @ N_2 0.65 liters/min, 1150°C, 3mins.

2) Dry O_2 @ 1.0 liter/min, 1150°C, 5mins.

3) Wet O_2 @ 0.5 liters/min, through 96.8°C H_2O, 1150°C, 90mins.

4) Anneal @ N_2 0.65 liters/min, 900°C, 15mins.

5) Pull @ N_2 0.65 liters/mim, 900°C, 3mins.

3. Photoresistor Step:(p^+ field isolation implant, MASK 1)

1) HMDS vapor, with N_2 flow, 5mins.

2) N_2 flush, 5mins.

3) Apply positive photoresistor (AZ1350J); spin @ 5000rpm, 30secs.

4) Prebake, @ 90°C, 15mins., with N_2 flow.

5) Expose mask, 15secs.

6) Develop with AZ developer:H_2O (1:1), 60secs.

7) Light DI rinse, 60secs.

8) Light N_2 blow dry.

9) Postbake, @ 110°C, 15mins.

10) Oxide etch, @ buffered HF (HF:NH_4F(1:5), aged at lease 4hrs.), R.T., 9.5mins.

11) Light DI rinse, 1 to 2 mins.

12) Light N_2 blow dry.

13) Inspect under microscope for complete oxide etch.

4. Field Ion Implantation:(p^+ field implant)

Bake wafer under IR lamp for 10mins.

1) Boron:$8x10^{13}/cm^2$, @ 150KeV.

2) Strip photoresistor in Piranha, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

5. Field Oxide Growth: N-type drive-in furnace, 0.4um wet oxide over p^+

1) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

2) Dip in HP:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Push @ N_2 0.65 liters/min, 1150°C, 3mins.

4) Dry O_2 @ 1.0 liter/min, 1150°C, 5mins.

5) Wet O_2 @ 0.5 liters/min, through 96.8°C H_2O, 1150°C, 16mins.

6) Anneal @ N_2 0.65 liters/min, 900°C, 15mins.

7) Pull @ N_2 0.65 liters/mim, 900°C, 3mins.

6. Photoresistor Step:(n^+ diffusion, MASK 2)

1) Same as step 3. except oxide etch for 10mins.

2) Strip photoresistor in acetone, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

7. Phosphorus Predeposition: N-type predeposition furnace, (cool phosphorus source, $POCl_3$, 30 to 40 mins. before use.)

1) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

2) Dip in HP:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Push @ N_2 0.65 liters/min, 1100°C, 3mins.

4) Dry O_2 @ 0.1 liters/min, and N_2 @ 1.25 liters/min, 1100°C, 5mins.

5) Dry O_2 @ 0.1 liters/min, N_2 @ 1.25 liters/min, and $POCl_3$ @ 0.096 liters/min, 1100°C, 20mins.

6) Dry O_2 @ 0.1 liters/min, and N_2 @ 1.25 liters/min, 1100°C, 2mins.

7) Anneal @ N_2, 0.65 liters/min, 900°C, 10mins.

8) Pull @ N_2 0.65 liters/min, 900°C, 3mins.

8. Etch Phosphorus Glass

1) Dip in HF:H_2O(1:3), 1.5mins.

2) DI rinse, 2mins.; N_2 blow dry.

9. S/D Oxide Growth: N-type drive-in furnace, 0.5um oxide over n^+ S/D

1) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

2) Dip in HF:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Push @ N_2 0.65 liters/min, 1100°C, 3mins.

4) Dry O_2 @ 1.0 liter/min, 1100°C, 5mins.

5) Wet O_2 @ 0.5 liters/min, through 96.8°C H_2O, 1100°C, 34mins.

6) Anneal @ N_2 0.65 liters/min, 900°C, 15mins.

7) Pull @ N_2 0.65 liters/mim, 900°C, 3mins.

10. Photoresistor Step:(Gate oxide, MASK 3)

1) Same as step 3. except oxide etch for 6.5mins.

2) Strip photoresistor in acetone, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

11. Gate Oxide Growth: N-type drive-in furnace, 0.1um gate oxide

1) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

2) Dip in HF:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Push @ N_2 0.65 liters/min, 1000°C, 3mins.

4) Dry O_2 @ 0.5 liters/min, 1000°C, 110mins.

5) Anneal @ N_2 0.65 liters/min, 1000°C, 15mins.

6) Pull @ N_2 0.65 liters/mim, 900°C, 3mins.

12. Photoresistor Step:(Depletion implant, MASK 4)

Same as 1) to 9) in step 3. (No oxide etch!)

13. Phosphorus Depletion Implant:

1) Phosphorus: $2.10 \times 10^{12}/cm^2$, @ 150KeV.

2) Strip photoresistor in Piranha, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

14. Boron Enhancement Implant:

1) Boron: $7.80 \times 10^{11}/cm^2$, @ 50KeV.

2) Strip photoresistor in Piranha, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

15. Back-side Oxide Etch:

Use Q-tip with small amount of HF, etch back-side of wafer only; DI rinse, 1 to 2 mins.; N_2 blow dry.

16. Phosphorus Gettering: N-type predeposition furnace

1) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

2) Dip in HF:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Push @ N_2 0.65 liters/min, 1000°C, 3mins.

4) Dry O_2 @ 0.1 liters/min, and N_2 @ 1.25 liters/min, 1000°C, 5mins.

5) Dry O_2 @ 0.1 liters/min, N_2 @ 1.25 liters/min, and $POCl_3$ @ 0.096 liters/min, 1000°C, 2mins.

6) Anneal @ N_2, 0.65 liters/min, 1000°C, 10mins.

7) Pull @ N_2 0.65 liters/min, 900°C, 3mins.

17. Photoresistor Step:(Contact, MASK 5)

1) Same as step 3. except oxide etch for 1.5mins.

2) Strip photoresistor in acetone, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

3) Piranha clean, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

4) Dip in HF:H_2O(1:10), 10secs.; DI rinse, 1 to 2 mins.; N_2 blow dry.

5) Bake under IR lamp, 15mins.

18. Evaporate 0.4 to 0.6um of Aluminum:

19. Photoresistor Step:(metalization, MASK 6)

1) Same as 1) to 9) in step 3. except spin AZ1350J @ 7000rpm, expose mask for 12secs. and develop for 45secs.

2) Aluminum etch @ type-A etchant, 50°C (etching rate 0.01um/sec), 50 to 70 secs.

3) DI rinse, 1 to 2 mins.; N_2 blow dry.

4) Strip photoresistor in acetone, 5mins.; DI rinse, 1 to 2 mins.; N_2 blow dry.

20. Sintering Treatment: Sintering furnace

1) Push @ N_2 1.0 liter/min, 450°C, 1min.

2) Sinter @ forming gas (N_2:H_2(9:1)) 1.0 liter/min, 450°C, 15mins.

3) Pull @ forming gas 1.0 liter/min, 450°C, 1min.

APPENDIX V. NMOS METAL-GATE LAYOUT RULES[X]

The layout rules given in this appendix are very conservative, which is designed for fabricating the prototype circuits with a relative high-temperature process as described in appendix IV. The spacing shown as follows is the minimum value in the layout.

MASK 1: p^+ Isolation

width 10um

spacing 7.5um to 15um

(for those low reverse-bias voltage across p^+, substrate and n^+ use 7.5um, otherwise use 15um.)

MASK 2: n^+ Source/Drain (S/D) Diffusion

width 10um

S/D spacing 15um (for switches)

20um (for op-amps)

MASK 3: Gate Oxide

width 10um

S/D overlap 2.5um

(also contains all the contact windows in MASK 5.)

MASK 4: Depletion Implant

larger than gate oxide 10um

MASK 5: Contact

minimum size 10umx10um

or 7.5umx12.5um

to edge of S/D 5um

MASK 6: Metal

width 10um

spacing 10um

larger than gate oxide

and contact window 2.5um

REFERENCES

[1] W. Jr. Black, D. Allstot, S. Patel, and J. Wieser, "CMOS PCM Channel Filter," Digest of Technical Papers, International Solid-State Circuits Conference, p. 184-185; Feb., 1980.

[2] I. Young, D. Hildebrand, and C. Johnson, "A Low-Power NMOS Transmit/Receive IC Filter for PCM Telephony," Digest of Technical Papers, International Solid-State Circuits Conference, p. 84-85; Feb., 1980.

[3] H. Ohara, P. Gray, W. Baxter, C. Rahim, and J. McCreary, "A Precision Low-Power PCM Channel Filter with On-Chip Power Supply Regulation," IEEE Journal of Solid-State Circuits; Dec., 1980.

[4] D.J. Allstot, "MOS Switched Capacitor Ladder Filters," PhD Dissertation, University of California, Berkeley; May, 1979.

[5] A. Papoulis, "Probability, Random Variables, and Stochastic Processes," McGraw-Hill, New York; 1965.

[6] C. Gabet, and A. Knob, "Noise Analysis of Switched Capacitor Networks," International Symposium on Circuits and Systems, p.856-859, Apr., 1981.

[7] C. Gabet, and A. Knob, "Noise Generated in Switched Capacitor Network," Electronics Letters, Vol. 16, No. 19; 1980.

[8] R.W. Brodersen, and S.P. Emmons, "Noise in Buried Channel Charge-Coupled Devices," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 1; Feb., 1976.

[9] R.E. Ziemer, and W.H. Tranter, "Principles of Communications Systems, Modulation, and Noise," Houghton Mifflin, Boston; 1976.

[10] R.H Dennard, F.H. Gaensslen, H-N Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," IEEE Journal of Solid-State Circuits, vol.SC-9, No.5, Oct., 1974.

[11] J.D. Plummer, and J.D. Meindl, "MOS Electronics for a Portable Reading Aid for the Blind," IEEE Journal of Solid-State Circuits, vol.SC-7, No.2, Apr., 1972.

[12] "Burr-Brown 1979 General Catalog," Burr-Brown Research Co., 1978.

[13] P.R. Gray, R.W. Brodersen, D.A. Hodges, T.C. Choi, R. Kaneshiro, and K.C. Hsieh, "Some Practical Aspects of Switched Capacitor Filter Design," International Symposium on Circuits and Systems, Feb., 1981.

[14] K. Martin, and A.S. Sedra, "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched Capacitor Filters," International Symposium on Circuits and Systems, Apr., 1980.

[15] B.K. Ahuja, M.R. Dwarakanth, T.E. Seidel, and D.G. Marsh, "Single-Chip PCM Codec with Filters," Digest of Technical Papers, 1981 International Solid-State Circuits Conference, New York, NY, Feb., 1981.

[16] L.A. Bienstman, and H. DeMan, "An 8-Channel 8b uP Compatible NMOS Converter with Programmable Ranges," Digest of Technical Papers, 1980 International Solid-State Circuits Conference, San Francisco, CA., 1980.

[17] G.M. Jacobs, "Practical Design Considerations for MOS Switched Capacitor Ladder Filters," M.S. thesis, University of California, Berkeley,CA., Nov., 1977.

[18] R.L. Geiger, and E. Sanchez-Sinencio, "Operational Amplifier Gain-Bandwidth Product Effects on the Performance of Switched-Capacitor Networks," International Symposium on Circuits and Systems, Feb., 1981.

[19] P.R. Gray, EECS241 Class Note, University of California, Berkeley,CA., 1980.

[20] T.C. Choi, private communication.

[21] R. Kaneshiro, private communication.

[22] M. Yunus, "Design and Fabrication of High Order Switched Capacitor Band Pass Filters," M.S. thesis, University of California, Berkeley,CA., Feb., 1980.

[23] B.J. Hosticka, "MOS Sampled Data Recursive Filters Using State Variable Techniques," Ph.D. Dissertation, University of California, Berkeley,CA., Aug., 1977.

[24] I.A. Young, "MOS Switched-Capacitor Analog Sample-Data Recursive Filters," Ph.D. Dissertation, University of California, Berkeley,CA., Nov., 1978.

[25] D.J. Allstot, private communication.

[26] K.C. Hsieh, and P.R. Gray, "A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique," Figure 6, p.266, Digest of Technical Papers, International Solid-State Circuits Conference, New York, NY., Feb., 1981.

[27] Ibid, Figure 5, p.129.

[28] M.H. White, D.R. Lampe, F.C. Blaha, and I.A. Mack, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," IEEE Journal of Solid-State Circuits, vol.SC-9, No.1; Feb., 1974.