NEGATIVE RESISTANCE DEVICES

by

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ABSTRACT

Two-terminal devices which exhibit a type-S (current-controlled) or type-N (voltage-controlled) negative differential resistance can be built using only two bipolar transistors and linear positive resistors without any internal biasing power supply. Two general algorithms are presented in this paper for systematically generating all such devices. Hundreds of negative resistance devices have been derived to date using these algorithms and a selection of these circuits is presented in this paper along with their computer-simulated v-i curves. Laboratory measurements of a few sample circuits agree remarkably well with the computer-simulated results.

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I. INTRODUCTION

The invention of the dynatron in 1918 [1] proves that it is possible for a 2-terminal device with no internal power supplies to possess a differential negative resistance. This discovery was initially greeted with fascination by some and skeptism by others because it seems to violate the conservation of energy. This paradox was of course quickly resolved upon recognizing that so long as the v-i curve lies in the first and the third quadrants, the device will remain passive. Consequently, any point on the v-i curve having a negative slope must necessarily lie in the first or the third quadrant. Many vacuum tube devices exhibiting a negative differential resistance have since been invented and utilized in numerous applications [2-18].

The invention of the transistor in 1948 has naturally triggered a search for solid state negative resistance devices. Unlike vacuum tubes, however, the physics of solid state devices is much more complex. It was not until 1958 before the first negative resistance solid state device, called the tunnel diode, was invented by Esaki [19]. In fact, so exotic was the physical mechanism responsible for the negative resistance that a Nobel prize in physics was awarded to Esaki in 1973. It took another 8 years before another promising 2-terminal solid state negative resistance device, called the Gunn diode, was invented [20]. Even more exotic is the physical mechanism responsible for this differential negative resistance that it took another researcher to explain the Gunn effect [21].

Another approach for inventing new solid state negative resistance devices is to combine two or more bipolar transistors with resistors [22-26]. Because these devices were discovered mostly through intuition and ad hoc techniques, the number of such circuits reported to-date is negligible compared to those invented during the vacuum tube era.

Our objective in this paper is to present a selected catalog of new 2-transistor negative resistance devices. Using a remarkable theorem due to Nielsen and Willson [27], these circuits are generated systematically. This unified approach can be used to generate all 2-terminal negative resistance devices without internal power supply, and includes the existing circuits reported in [22-24] as special cases. If internal batteries are allowed, this approach would yield an even larger collection of negative resistance circuits, including those reported in [25-26]. Since such circuits are not passive, they

are potentially unstable and inconvenient, if not impractical, in view of the power supply requirement. Consequently, we will restrict our catalog to those negative resistance circuits which do not require a power supply.

Since the negative resistance devices presented in this paper are made of standard bipolar transistors and linear resistors only, they can be easily fabricated and mass produced as integrated circuits. Moreover, unlike the tunnel diode and the Gunn diode where the value of the negative resistance and its dynamic range can be adjusted only slightly, our catalog contains circuits with a very large range of easily adjustable parameters. In fact, by judicious choice of the values of the linear resistors, one could shape the v-i curves for different applications without invoking any sophisticated device physics. The only disadvantage of our negative resistance devices is that its switching speed is limited by the bipolar transistors and is therefore significantly slower than that of the tunnel and Gunn diodes.

The v-i curve of the negative resistance devices to be presented in this paper is characterized by a maximum point, called the "peak", and a minimum point, called the "valley", and can be either current-controlled or voltage-controlled, as shown in Figs. 1(a) and (b), respectively. These two points partition the v-i curves in Fig. 1 into regions I, II, III, respectively. Because of its shape, a current-controlled device (Fig. 1(a)) is usually called a Type-S device and a voltage-controlled device (Fig. 1(b)) is usually called a Type-N device. Throughout this paper, the coordinates of the "peak" and "valley" points of either curves will be denoted by (v_p,i_p) and (v_v,i_v) respectively.

A sample of type-S and type-N devices will be presented in Section II and Section III, respectively. A more extensive catalog is given in Appendix B. They are classified according to the number of linear resistors required in addition to the two transistors.

Circuits containing two npn transistors, or two pnp transistors, are called "npn circuits" or "pnp circuits", respectively. Circuits containing an npn and a pnp transistor are called "complementary circuits". Since pnp circuits are "duals" of npn circuits, only npn circuits are listed in this paper. Even then, to avoid overwhelming the reader with too many circuits, only a few typical circuits under each category are presented in Sections II and III. Additional circuits which are likely to be of practical importance are given in Appendix B. However, because of the exceedingly large number of

negative resistance circuits that can be generated using the systematic method to be described in Section IV, Appendix B contains only a selected subset of the numerous negative resistance circuits we have so far generated.

All circuits are presented with a family of v-i curves parametrized by different resistor values. These v-i curves are simulated by the computer program SPICE [28], which is known to give rather realistic answers for bipolar transistor circuits. Unless otherwise stated, default parameter values are assigned to the transistor models used in the simulation.

II. TYPE-S (CURRENT-CONTROLLED) NEGATIVE RESISTANCE DEVICES

A. Type-S Devices Parametrized by One Resistor

A typical complementary circuit with one resistor R is shown in Fig. 2(a). The v-i curves corresponding to 3 different values of R are shown in Fig. 2(b). The negative resistance in this case exists only over a rather narrow range of input voltage v.

B. Type-S Device Parametrized by Two Resistors

A typical complementary circuit with two resistors R_1 and R_2 is shown in Fig. 3(a). The v-i curves in Fig. 3(b) are parametrized by R_1 with R_2 held fixed at 10 kΩ. Those in Fig. 3(c) are parametrized by R_2 with R_1 held fixed at 400Ω.

In Fig. 3(b), i_v,i_p and v_p are monotone decreasing functions of R_1. On the other hand, the differential resistance in each region and the value of v_v remain more or less unchanged as R_1 is varied.

In Fig. 3(c), the values of i_v and i_p remain more or less unchanged as R_2 is varied.

C. Type-S Devices Parametrized by Three Resistors

A typical complementary circuit with three resistors R_1,R_2, and R_3 is shown in Fig. 4(a). The v-i curves in Fig. 4(b) are parametrized by R_1 with R_2 and R_3 held fixed. Likewise, the v-i curve in Figs. 4(c) and (d) are parametrized by R_2 and R_3, respectively, while the other two resistors are held fixed.

Note that the circuit in Fig. 3(a) can be obtained by setting $R_3 = 0$ in Fig. 4(a). In both circuits, the value of v_v remain more or less constant at approximately 0.8v regardless of the resistor values. To obtain a v-i curve with an adjustable v_v, another circuit topology must be chosen. One such

circuit is shown in Fig. 5(a) with the corresponding families of v-i curves shown in Figs. 5(b), (c), and (d). Note that the value of v_v in this circuit is quite sensitive to R_1 and R_2. However, like Fig. 2(b), the range of the negative resistance in this circuit is relatively narrow.

In all circuits considered so far, the differential conductance in region III is nearly infinite. For applications which requires an adjustable and finite conductance in this region, we can insert a resistor R_3 by "plier entry" with the emitter lead of transistor T_2 in Fig. 3(a) to obtain the complementary circuit shown in Fig. 6(a). The corresponding families of parametrized v-i curves are shown in Figs. 6(b), (c), and (d).

D. Type-S Devices Parametrized by Four Resistors

A typical complementary circuit with four resistors R_1,R_2,R_3, and R_4 is shown in Fig. 7(a). Four families of v-i curves are shown in Figs. 7(b), (c), (d), and (e), each parametrized by one resistance while holding the values of the other resistors fixed. Note that this circuit is obtained by inserting a resistor R_4 by "plier entry" with the emitter lead of transistor T_2 in Fig. 4(a). The following table summarized the quantities affected by each resistor, with the other held fixed. In Table 1, G_I, G_{II}, and G_{III} denote the differential conductance in regions I, II, and III, respectively.

Resistance Being Varied	v-i Curve Parameters Affected
R_1	i_p, v_p, i_v
R_2	v_p, G_I, G_{II}
R_3	i_v, v_v, G_{II}
R_4	i_v, v_v, G_{III}

Table 1

Another four-resistor type-S device having a v-i curve similar to that of an SCR is shown in Fig. 8(a). It is obvious from Figs. 8(b)-(e) that by varying R_2 we can change the values of G_{II} and v_p while keeping the values of i_v, v_v and i_p unchanged. Furthermore, varying R_3 changes v_p, v_v and i_v while keeping the other parameters unchanged; varying R_4 changes G_{II}, i_v and v_v while keeping i_p, v_p and the other parameters unchanged. Finally, note that the value of G_{III} may be changed by varying merely R_1.

E. Type-S Devices Parametrized by Five Resistors

A typical complementary circuit with five resistors R_1,R_2,R_3,R_4 and R_5 is shown in Fig. 9(a). Five families of v-i curve are shown in Figs. 9(b), (c), (d), (e), and (f), each parametrized by one resistance while holding the values of the other resistors fixed.

Some additional selected type-S devices are shown in Appendix B, along with some typical parametrized v-i curves.

Note that we have deliberately chosen the same basic topology for the circuits in Figs. 2, 3, 4, 6, and 7 in order to demonstrate how the v-i curve can be "tuned" by one or more resistors to suit different applications. There exist many more -- in fact too many that only a small subset is listed in Appendix B -- negative-resistance circuits having fundamentally distinct topologies.

III. TYPE-N (VOLTAGE-CONTROLLED) NEGATIVE RESISTANCE DEVICES

A. Type-N Devices Parametrized by One Resistor

Unrealizable (see section IV).

B. Type-N Devices Parametrized by Two Resistors

Unrealizable (see section IV).

C. Type-N Devices Parametrized by Three Resistors

The only realizable type-N device with three resistors is shown in Fig. 10(a). The v-i curves in Fig. 10(b) are parametrized by R_1 with R_2 and R_3 held fixed. Likewise, the v-i curves in Figs. 10(c) and (d) are parametrized by R_2 and R_3, respectively, while the other two resistors are held fixed.

Note that by varying either R_1 or R_2, we can change the values of v_p, i_p and v_v. On the other hand, by varying R_3 we can change the values of G_I, G_{II} and i_p simultaneously.

D. Type-N Devices Parametrized by Four Resistors

Connecting one resistor R_4 by "soldering-iron" entry across the collector and base terminals of transistor T_1 in the above circuit, we obtain a four-resistor type-N device as shown in Fig. 11(a). The presence of collector-base feedback for T_1 smooths the negative resistor region (region II) on the v-i curves (shown in Fig. 10(b)-(d)), as can be seen from Fig. 11(b), where the v-i curves are parametrized by R_4 with other resistors held fixed.

If we connect an emitter current feedback resistor R_4 for T_1 in the circuit of Fig. 10(a) by "plier entry" with its emitter lead, we would obtain the circuit shown in Fig. 12(a). Varying the value of R_4 in this case while keeping the other parameters fixed, we can merely change G_{II} and v_v as can be seen from Fig. 12(b), where the v-i curves are parametrized.

Adding one emitter current feedback resistor R_4 to both transistors shown in the circuit of Fig. 10(a), we obtain the negative resistance device shown in Fig. 13(a). The associated v-i curves are shown in Fig. 13(b)-(e). Note that the differential negative resistance in this circuit is relatively insensitive to variations in R_1,R_2,R_3, and R_4.

A four-resistor type-N device whose differential resistance is much more sensitive to variations in R_1,R_2,R_3, and R_4 is shown in Fig. 14(a). Table 2 shows how the v-i curves in Figs. 14(b)-(e) are affected by the values of the four resistors.

E. Type-N Devices Parametrized by Five Resistors

Adding a collector-to-base feedback resistor R_5 to the circuit shown in Fig. 13(a), we obtain the five-resistor type-N device shown in Fig. 15(a). Its v-i curves parametrized by each resistor, with values of the other resistors held fixed, are shown in Figs. 15(b)-(f), respectively. Comparing these v-i curves with those from Fig. 13 (without R_5), we find a much smoother negative resistance region in Fig. 15.

Connecting two more resistors R_4 and R_5 by "plier" and "soldering-iron" entries, respectively, to the circuit shown in Fig. 10(a), we obtain the interesting type-N device shown in Fig. 16(a). Its v-i curves parametrized by R_4 and R_5 while holding the values of the other resistors fixed are shown in Figs. 16(b) and (c), respectively. Note that we can tailor the v-i curve

Resistance Being Varied	v-i Curve Parameters Affected
R_1	v_p, i_p, v_v, G_{II}
R_2	$v_p, i_p, v_v, i_v, G_I, G_{II}, G_{III}$
R_3	v_p, i_p, G_I, G_{II}
R_4	$v_p, i_p, G_{II}, v_v, i_v$

Table 2

from the "bell" shape to a "trapezoidal" shape by adjusting the values of R_4 and R_5.

If we move R_5 from Fig. 16(a) to that shown in Fig. 17(a), we will obtain the sawtooth-like v-i curves shown in Fig. 17(b).

Another configuration shown in Fig. 18(a) offers a tailorable "bell-shape" v-i curve as shown in Figs. 18(b) and (c). Note that by choosing an appropriate value for R_5, we can even obtain a "symmetrical" bell-shape v-i curve over a limited voltage range.

More type-N devices with four to five resistors can be found in Appendix B, along with some typical parametrized v-i curves.

IV. SYSTEMATIC METHOD FOR GENERATING NEGATIVE RESISTANCE DEVICES

A. The Unified Approach

Our method for generating the negative resistance circuits in the preceding sections, as well as in Appendix B, consists of synthesizing Resistor-Transistor circuits having the following special topological structure:

Definition: Feedback Structure

Let the one-port N in Figs. 19(a) and (b) contain exactly 2 transistors (npn,pnp, or their combination) and linear positive resistors. Let N_S be a simplified one-port obtained by replacing each resistor in N by either a short circuit, or an open circuit. The voltage-source driven one-port in Fig. 19(a) or the current-source driven one-port in Fig. 19(b) is said to possess a feedback structure iff the short-circuited one-port N_S in Fig. 19(c) or the open-circuited one-port N_S in Fig. 19(d) can be redrawn into the form shown in Fig. 20.

Let each transistor in Fig. 19(a) or (b) be modeled by the Ebers-Moll equation

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} -1 & \alpha_r \\ \alpha_f & 1 \end{bmatrix} \begin{bmatrix} f_1(v_1) \\ f_2(v_2) \end{bmatrix}$$

where $f_1(v_1)$ and $f_2(v_2)$ denote the usual "junction law" of pn junction diodes, and α_r and α_f denote the "reverse" and "forward" current gain, where $0 < \alpha_r < 1$ and $0 < \alpha_f < 1$.

Let the dc equation of the 2-transistor circuit in Figs. 19(a) and 19(b) be written in the general form $AF(x) + Bx = C$ [27].

Theorem 1 (Nielsen and Willson)

The 2-transistor circuit in Fig. 19(a) or Fig. 19(b) has a unique solution for all values of the resistors ($R_j > 0$), all values of the transistor parameters, ($0 < \alpha_r < 1$, $0 < \alpha_f < 1$) and all values of input voltage V_s and input current I_s, if, and only if, the circuit does not possess a feedback structure.

Proof This follows as a direct application of Theorem 1 in [27].

Corollary 1

In order for a 2-transistor one-port N to exhibit a type-S negative resistance v-i curve (Fig. 1(a)), it is necessary that the voltage-driven one-port in Fig. 19(a) possesses a feedback structure.

Corollary 2

In order for a 2-transistor one-port N to exhibit a type-N negative resistance v-i curve (Fig. 1(b)), it is necessary that the current-driven one-port in Fig. 19(b) possesses a feedback structure.

Observations

1. The simplified circuit in Figs. 19(c) and (d) contains only two transistors and connecting wires.

2. The circuit in Fig. 19(a) or (b) can not contain a feedback structure if its simplified circuit in Fig. 19(c) or (d) satisfies one of the following properties:

(a) The "base" of T_1 is connected to the "base" of T_2.

(b) A pair of terminals of T_1 (or T_2) is short circuited.

(c) A terminal of either T_1 or T_2 is open circuited.

Remark 1

Although Theorem 1 provides both a necessary and sufficient condition for a 2-transistor one-port to be a negative resistance device, it does not guarantee that the circuit is realizable using real bipolar transistors. The reason is that Theorem 1 allows not only the resistors and dc sources to assume any value, but it also allows both α_r and α_f to assume any value between zero and one. In an actual bipolar transistor, $\alpha_r \simeq 0$ and $\alpha_f \simeq 1$. Hence, whenever the minimum "reverse" current gain α_r necessary to give a negative differential resistance is not negligible, the corresponding physical circuit will not yield a negative resistance.

Corollary 3

If N in Fig. 19(a) or (b) contains only one transistor, it can not be a negative resistance device.

Proof It is impossible to obtain a feedback structure in this case.

Corollary 4

Let N be a physical negative resistance one-port made of two bipolar transistors and linear positive resistors. Then using appropriate circuit models, both transistors must be operating in the forward active region [29] over the entire range of the negative resistance.

Proof Suppose at least one transistor never operates in the active region. Then this transistor is either in saturation, cut off, or reversed active mode. In each of these 3 cases, the transistor can be realistically modeled by a combination of linear positive resistors, open circuit and short circuits [29]. Since the resulting circuit contains only one transistor, it follows from Corollary 3 that N can not be a negative resistance device.

Observations:

1. It follows from Corollary 4 that even if N contains a feedback structure, it can not be a negative resistance device if the circuit topology and transistor types are such that it is impossible to bias both transistors in the forward active region by the external voltage source V_s or current source I_s.

For example, the one-port N shown in Fig. 21(a) possesses a feedback structure, as is obvious from Fig. 21(b). However, since $i_{B2} = -i_{C1}$ and since $i_{C1} > 0$ if T_1 is active, and $i_{B2} > 0$ if T_2 is active, it follows that the two transistors can never operate in the active region simultaneously. Hence, N can not be a negative resistance device.

2. Even if both transistors in N can operate in the forward active region, N may still fail to yield a negative resistance v-i curve.

For example, consider the "2-transistor analog" in Fig. 22(a) which is usually used to explain a four-layer pnpn-diode or silicon-controlled rectifier (SCR) [30]. Although this circuit clearly possesses a feedback structure (Fig. 22(b)), its v-i curve simulated by SPICE (using the Ebers-Moll model with $\beta > 1$) as shown in Fig. 22(c) does not have a negative resistance region. Note that unlike the circuit in Fig. 21(a), we can not, by inspection, rule out the circuit in Fig. 22(b) as a potential candidate for a negative resistance

device because both transistors could conceivably be operating in the forward active region. In such cases, it is necessary to simulate the circuit using different parameters and search for a negative resistance v-i curve.

For the circuit in Fig. 22(b), no such characteristic is found for all positive value of $\beta \triangleq \alpha/1 - \alpha$ that we have tried. Indeed, it can be proved rigorously that, using the Ebers-Moll circuit model, the 2-transistor circuit in Fig. 22(b) can not give a negative resistance v-i curve. Consequently, this circuit is useful only as a crude "analog" in explaining the physical mechanism inside a pnpn device. In order to obtain the negative resistance v-i curve actually observed in practice, a more realistic circuit model must be used [31].

3. If the one-port N shown in Fig. 23(a) (resp., Fig. 24(a)) gives a type-S (resp., type-N) v-i curve, then so does the internal one-port N'. On the other hand, if N' exhibits a negative differential resistance, adding a series resistor (resp., shunt resistor) $R > 0$ may "destroy" the negative resistance, by giving rise to either a monotone-increasing v-i curve (for R sufficiently large in Fig. 23(b) and sufficiently small in Fig. 24(c)), or a multivalued v-i curve as in Fig. 23(c) or 24(b).

It follows from this observation that in developing the following algorithm for generating negative resistance devices, we need not connect a resistor either in series or in parallel with the driving-point voltage source V_s, or driving-point current source I_s. Doing so would only diminish the possibility for obtaining a negative differential resistance.

Using the preceding Corollaries and Observations, we can now formulate the following algorithms for generating all 2-transistor negative resistance devices:

B. Algorithm for Generating Type-S Devices:

1. Insert a voltage source V_s by "plier-entry" into the "feedback structure" shown in Fig. 20. There are only 3 possibilities, as shown in Figs. 25(a), (b), and (c).

2. Connect one resistor by "plier-entry" with any wire (except in series with the voltage source) or by "soldering-iron" entry across any terminals (except across the voltage source) in each of the 3 configurations shown in Fig. 25.

For example, for the circuit configuration (c), there are only 7 distinct possibilities as shown in Fig. 26. The circuits in Figs. 26(a)-(b) are obtained by pliers-entries. Those in Figs. 26(c)-(g) are obtained by soldering-iron entries.

3. Assume both transistors in Fig. 26 are npn transistors. For each circuit in Fig. 26, generate 4 distinct circuits by assigning different collector and emitter combinations. For example, the 4 circuits derived from Fig. 26(g) are shown in Fig. 27.

4. a) Inspect each circuit generated in step 3 and eliminate any circuit whose transistors can not simultaneously operate in the forward active region.

b) Further elimination is often possible by deriving the driving-point small signal resistance with both transistors modeled by a small-signal model in the active region [29]. If this resistance can not be made negative for any $R > 0$ and $\alpha_f = 0.99$, eliminate the circuit.

c) Simulate each of the remaining distinct candidates for different element parameter values. Eliminate any candidate which did not yield a negative resistance v-i curve.

5. Repeat step 3 and 4 using one npn transistor and one pnp transistor (complementary case). In carrying out steps 4 and 5, the inherent symmetry of circuits should be exploited to avoid simulating redundant candidates. For example, the circuit pairs given in Figs. 26(a) and (d), Figs. 26(b) and (e), Figs. (c) and (f) are symmetrical.

6. Repeat steps 2-4 using "n" resistors at a time, where n = 2,3,4,5,...

C. Algorithm for Generating Type-N Devices:

1. Insert a current source I_s by "soldering-iron" entry into the feedback structure shown in Fig. 20. There are only 3 possibilities, as shown in Figs. 28(a), (b) and (c).

2. Connect one resistor by "pliers entry" with any wire (except in series with the current source), or by "soldering-iron" entry across any terminals (except across the current source) in each of the 3 configurations shown in Fig. 28.

For example, for the circuit configuration (a), there are only 7 distinct possibilities, as shown in Fig. 29. The circuits in Figs. 29(c)-(g) are obtained by pliers entries. Those in Figs. 29(a)-(b) are obtained by soldering-iron entries.

3.
4.
5.
6.

Same as Algorithm for type-S device.

We have screened hundreds of candidates for type-N devices containing one or two resistors created by the above algorithm. The overwhelming majority of such circuits can be categorized into one of two basic configurations as illustrated by two typical examples shown in Fig. 30(a) and 31 respectively.

For the first configuration in Fig. 30(a), the base and emitter of T_1 are directly connected across the port. Since the base-emitter v-i characteristic is relatively insensitive to the collector-emitter voltage, we can model T_1 by a pn junction diode characterized by an "exponential" v-i" curve. The remaining one-port consisting of T_2 and R must also necessarily have a monotone-increasing v-i curve in view of Corollary 3. Consequently, the v-i curve of the resulting parallel combinations must also be monotone increasing. Because of the exponential character of the pn junction law, the v-i curve for circuits belonging to this category will resemble that shown in Fig. 30(b), and can not give rise to a negative differential resistance.

For the second configuration in Fig. 31, there is no current path for the current of T_2 no matter what polarity of the external source we apply. Therefore, T_2, and consequently, T_1 can not be active. Thus we can conclude that the one-port in Fig. 31 can not exhibit a negative differential resistance.

After eliminating all one- and two-resistor circuits which can not exhibit a negative differential resistance, we are left with the 3 candidates shown in Fig. 32, where both transistors can operate in the forward active region simultaneously.

For the circuit candidate in Fig. 32(a), an increase in the driving-point voltage v causes an increase in both $i_{B1} \approx \frac{v-0.6}{R_1}$ and $i_{B2} \approx \frac{v-0.6}{R_2}$. This will lead to a corresponding increase in $i_{C1} = i_{C2}$. Since $i = i_{B1} + i_{B2} + i_{C1}$, the port current i is a monotone-increasing function of the port voltage v. Hence, this circuit must also be discarded even though both transistors are active over a reasonable range of input voltages.

For the circuit candidate in Fig. 32(b), note that the current flowing down R_2 is approximately fixed by the sum of the base-to-emitter drops of transistors T_1 and T_2 ($i_{R2} < 2(0.6)/R_2$). Consequently, any increase in the

port voltage v must be absorbed by R_1 with a corresponding increase in both collector currents. Since the port current ($i = i_{R1} + i_{C1} + i_{C2}$) must also increase with v, this circuit must also be discarded.

For the circuit candidate in Fig. 32(c), it is not obvious by inspection that the port current must also increase with the port voltage v. On the contrary, since the emitter-to-base voltage of both transistors are less than 0.8V in the active region, an increase in v will be absorbed mostly by R_1 and R_2 in order to account for the increase in i_{B1} and i_{C1}. But the increased voltage drop across R_2 tends to decrease the base-to-emitter voltage across T_2 and hence a <u>decrease</u> in i_{C2}. Is it possible for i_{C2} to decrease faster than the increase in i_{R1} and i_{R2}?

To resolve the above question, we carry out a dc analysis in <u>Appendix A assuming</u> both transistors are operating in the forward active region. The differential input conductance is found to be

$$\frac{dI}{dV} = \frac{(1+\beta_1)}{R_1} + (1+\beta_2)\left[\frac{1}{R_2} - \frac{\beta_1}{R_1}\right] \tag{1}$$

It follows from (1) that in order to obtain a <u>negative</u> differential resistance, it is necessary that

$$(1+\beta_1)R_2 + (1+\beta_2)(R_1-\beta_1 R_2) < 0 \tag{2}$$

Since $\beta_1 >> 1$ and $\beta_2 >> 1$ in the forward active region for practical transistors, (2) can be further simplified as follows:

$$n \triangleq \frac{\beta_1 R_2}{R_1} > 1 \tag{3}$$

Now, in terms of n, the collector current of T_2 derived in <u>Appendix A</u> can be recast as follows:

$$I_{C2} = \frac{\beta_2}{R_2}\left[(n-1)(V_{B1}-V)+(V_{B1}-V_{B2})\right] \tag{4}$$

Since both transistors are assumed to be operating in the active region, $V_{B1} \approx V_{B2}$, $V > V_{B1}$, $I_{C2} > 0$. It follows from (4) that $n < 1$, which contradicts (3). Hence $di/dv > 0$ whenever both transistors are operating in the forward active region.

Reluctantly, the circuit in Fig. 32(c) must also be eliminated. Since we have exhausted all possibilities, we conclude that <u>it is impossible to realize a type-N "two-transistor" negative-resistance device using less than three resistors</u>.

Interestingly enough, if we add one more resistor across the base and emitter terminals of T_1 in Fig. 32(c), we would obtain the type-N negative resistor device considered earlier in Fig. 10(a). This confirms our earlier observation that it is impossible to ascertain by inspection whether the circuit in Fig. 32(c) is capable of exhibiting a negative differential resistance.

V. CONCLUDING REMARKS

We have developed two general algorithms for systematically generating all two-transistor negative resistance devices of both type-S and type-N. These algorithms are derived from the "necessary condition" of a fundamental theorem due to Nielsen and Willson.

Using SPICE as our tool, we have simulated hundreds of potential circuit candidates and a selection of these circuits are cataloged in Appendix B. We have also verified some of these circuits in the laboratory and the experimental measurements are remarkably close to the simulated results.

There are hundreds of two-transistor circuits which possess a "feedback structure" but which nevertheless do not exhibit a negative differential resistance, regardless of the choice of resistance values, port voltage, and port current. This observation, however, does not invalidate the "sufficient condition" of Nielsen and Willson because the value of the reverse current gain α_r of real bipolar transistors is typically very small, whereas Nielsen-Willson's theorem actually allows α_r to assume values between 0 and 1. For the same reason, we have found that contrary to the original Nielsen-Willson's Theorem, the emitter and collector terminals can not be arbitrarily interchanged. In fact, our numerical simulations tend to support the following conjectures:

Conjecture 1. For a real two-bipolar-transistor one-port to exhibit a negative differential resistance, it is necessary that in the associated "feedback structure" of Fig. 20, the two emitters be connected to each other.

Conjecture 2. In order to obtain a two-transistor type-S negative resistance device, the two transistors must be complementary, i.e., one is pnp, the other is npn.

Conjecture 3. In order to obtain a two-transistor type-N negative resistance device, the two transistors must be of the same type; i.e., both pnp or both npn.

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APPENDIX

A. dc Analysis of Fig. 32(c)

The circuit in Fig. 32(c) clearly possesses a feedback structure, as shown in Fig. A.1(a). To determine whether it is possible for this circuit to exhibit a negative differential resistance, assume the two transistors are operating in the forward region and replace each transistor by the ideal dc model shown in Fig. A.1(b). Applying KCL and KVL to this circuit, we obtain

$$I = (1+\beta_1)I_{B1} + (1+\beta_2)I_{B2} \tag{A.1}$$

$$I_{B1} = \frac{V-V_{B1}}{R_1} \tag{A.2}$$

$$I_{B2} = \frac{V-V_{B2}}{R_2} - \beta_1\left(\frac{V-V\beta_1}{R_1}\right) \tag{A.3}$$

Substituting (A.2) and (A.3) into (A.1), we obtain

$$I = (1+\beta_1)\left[\frac{V-V_{B1}}{R_1}\right] + (1+\beta_2)\left[\frac{V-V_{B2}}{R_2} - \beta_1\left(\frac{V-V_{B1}}{R_1}\right)\right] \tag{A.4}$$

Differentiating (A.4) with respect to V, we obtain the following expression for the differential input conductance:

$$\frac{dI}{dV} = \frac{(1+\beta_1)}{R_1} + (1+\beta_2)\left[\frac{1}{R_2} - \frac{\beta_1}{R_1}\right] \tag{A.5}$$

This equation is used in Section IV to derive the condition for $\frac{dI}{dV} < 0$ to be possible. This analysis will also require the following expression for the collector current I_{C2} for transistor T_2:

$$I_{C2} = \beta_2 I_{B2} = \beta_2\left[\frac{V-V_{B2}}{R_2} - \beta_1\left(\frac{V-V_{B1}}{R_1}\right)\right] \tag{A.6}$$

FIGURE CAPTIONS

Fig. 1. (a) A type-S device characterized by a non-monotonic current-controlled v-i curve with one maxima and one minima.
(b) A type-N device characterized by a non-monotonic voltage-controlled v-i curve with one maxima and one minima.

Fig. 2. (a) A type-S complementary circuit with one resistor.
(b) v-i curve for R = 1,2, and 5KΩ.

Fig. 3. (a) A type-S complementary circuit with two resistors.
(b) v-i curve for R_1 = 300, 400, 500Ω, and R_2 = 10KΩ.
(c) v-i curve for R_2 = 5, 10, 20KΩ, and R_1 = 400Ω.

Fig. 4. (a) A type-S complementary circuit with three resistors.
(b) v-i curve for R_1 = 100, 200, 400Ω, R_2 = 10KΩ, and R_3 = 10KΩ.
(c) v-i curve for R_2 = 5, 10, 20KΩ, R_1 = 200Ω, and R_3 = 10KΩ.
(d) v-i curve for R_3 = 2, 10, 20KΩ, R_1 = 200Ω, and R_2 = 10KΩ.

Fig. 5. (a) A type-S complementary circuit with three resistors.
(b) v-i curve for R_1 = 5, 10, 20KΩ, R_2 = 4KΩ, and R_3 = 500Ω.
(c) v-i curve for R_1 = 20KΩ, R_2 = 2, 4, 20KΩ, and R_3 = 500Ω.
(d) v-i curve for R_1 = 20KΩ, R_2 = 4KΩ, and R_3 = 300Ω, 500Ω, 1KΩ.

Fig. 6. (a) A type-S complementary circuit with three resistors.
(b) v-i curve for R_1 = 100, 200, 400Ω, R_2 = 10KΩ, and R_3 = 300Ω.
(c) v-i curve for R_1 = 200Ω, R_2 = 5, 10, 20KΩ, and R_3 = 300Ω.
(d) v-i curve for R_1 = 200Ω, R_2 = 10KΩ, and R_3 = 300Ω, 1KΩ, 5KΩ.

Fig. 7 (a) A type-S complementary circuit with four resistors.
(b) v-i curve for R_1 = 100, 200, 400Ω, R_2 = 10KΩ, R_3 = 2KΩ, and R_4 = 300Ω.
(c) v-i curve for R_1 = 200Ω, R_2 = 5, 10, 20KΩ, R_3 = 10KΩ, and R_4 = 300Ω.
(d) v-i curve for R_1 = 200Ω, R_2 = 10KΩ, R_3 = 5, 10, 15KΩ, and R_4 = 300Ω.
(e) v-i curve for R_1 = 200Ω, R_2 = 10KΩ, R_3 = 5KΩ, and R_4 = 300Ω, 1KΩ, 5KΩ.

Fig. 8. (a) A type-S complementary circuit with four resistors.
(b) v-i curve for R_1 = 500Ω, 700Ω, 1KΩ, R_2 = 100KΩ, R_3 = 10KΩ, and R_4 = 5KΩ.
(c) v-i curve for R_1 = 700Ω, R_2 = 20, 100, 200KΩ, R_3 = 10KΩ, and R_4 = 5KΩ.
(d) v-i curve for R_1 = 700Ω, R_2 = 100KΩ, R_3 = 5, 10, 30KΩ, and R_4 = 5KΩ.
(e) v-i curve for R_1 = 700Ω, R_2 = 100KΩ, R_3 = 10KΩ, and R_4 = 5, 10, 15KΩ.

Fig. 9. (a) A type-S complementary circuit with five resistors.
(b) v-i curve for R_1 = 12, 15, 30KΩ, R_2 = 100KΩ, R_3 = 2KΩ, R_4 = 20KΩ, and R_5 = 1KΩ.
(c) v-i curve for R_1 = 15KΩ, R_2 = 40, 100, 120KΩ, R_3 = 2KΩ, R_4 = 20KΩ, and R_5 = 1KΩ.
(d) v-i curve for R_1 = 15KΩ, R_2 = 100KΩ, R_3 = 1, 2, 2.5KΩ, R_4 = 20KΩ, and R_5 = 1KΩ.
(e) v-i curve for R_1 = 15KΩ, R_2 = 100KΩ, R_3 = 2KΩ, R_4 = 15, 20, 50KΩ, and R_5 = 1KΩ.
(f) v-i curve for R_1 = 15KΩ, R_2 = 100KΩ, R_3 = 2KΩ, R_4 = 20KΩ, and R_5 = 300Ω, 1KΩ, 1.5KΩ.

Fig. 10. (a) A type-N npn circuit with three resistors.
(b) v-i curve for R_1 = 30, 60, 100KΩ, R_2 = 3KΩ, and R_3 = 200KΩ.
(c) v-i curve for R_1 = 60KΩ, R_2 = 2, 3, 10KΩ, and R_3 = 200KΩ.
(d) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, and R_2 = 100, 200, 500KΩ.

Fig. 11. (a) A type-N npn circuit with four resistors.
(b) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 75KΩ, and R_4 = 1, 2, 4KΩ.

Fig. 12. (a) A type-N npn circuit with four resistors.
(b) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 100KΩ, and R_4 = 500Ω, 1KΩ, 2KΩ.

Fig. 13. (a) A type-N npn circuit with four resistors.
(b) v-i curve for R_1 = 300, 400, 500KΩ, R_2 = 50kΩ, R_3 = 100KΩ, and R_4 = 10Ω.
(c) v-i curve for R_1 = 400KΩ, R_2 = 40, 50, 60KΩ, R_3 = 100KΩ, and R_4 = 10Ω.
(d) v-i curve for R_1 = 400KΩ, R_2 = 50KΩ, R_3 = 60, 80, 100KΩ, and R_4 = 10Ω.
(e) v-i curve for R_1 = 400KΩ, R_2 = 50KΩ, R_3 = 100KΩ, and R_4 = 5, 10, 20Ω.

Fig. 14. (a) A type-N npn circuit with four resistors.
(b) v-i curve for R_1 = 200, 500KΩ, 5MΩ, R_2 = 200KΩ, R_3 = 100Ω, and R_4 = 10KΩ.
(c) v-i curve for R_1 = 200KΩ, R_2 = 5, 20, 100KΩ, R_3 = 100Ω, and R_4 = 10KΩ.
(d) v-i curve for R_1 = 200KΩ, R_2 = 200KΩ, R_3 = 100Ω, 1KΩ, 5KΩ, and R_4 = 10KΩ.
(e) v-i curve for R_1 = 200KΩ, R_2 = 200KΩ, R_3 = 100Ω, and R_4 = 200Ω, 3KΩ, 10KΩ.

Fig. 15. (a) A type-N npn circuit with five resistors.
(b) v-i curve for R_1 = 600, 650, 700KΩ, R_2 = 50KΩ, R_3 = 20KΩ, R_4 = 100Ω, and R_5 = 4KΩ.
(c) v-i curve for R_1 = 700KΩ, R_2 = 50, 52, 55KΩ, R_3 = 20KΩ, R_4 = 100Ω, and R_5 = 4KΩ.
(d) v-i curve for R_1 = 700KΩ, R_2 = 50KΩ, R_3 = 20, 25, 30KΩ, R_4 = 100Ω, and R_5 = 4KΩ.
(e) v-i curve for R_1 = 700KΩ, R_2 = 50KΩ, R_3 = 20KΩ, R_4 = 60, 80, 100Ω, and R_5 = 4KΩ.
(f) v-i curve for R_1 = 700KΩ, R_2 = 50KΩ, R_3 = 20KΩ, R_4 = 100Ω, and R_5 = 3, 3.5, 4KΩ.

Fig. 16. (a) A type-N npn circuit with five resistors.
(b) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 100KΩ, R_4 = 1, 2, 5,KΩ, and R_5 = 5KΩ.
(c) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ; R_3 = 100KΩ, R_4 = 5KΩ, and R_5 = 2, 5, 50KΩ.

Fig. 17. (a) A type-N npn circuit with five resistors.
(b) v-i curve with R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 100KΩ, R_4 = 5KΩ, and R_5 = 5, 20, 50KΩ.

Fig. 18. (a) A type-N npn circuit with five resistors.
(b) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 100KΩ, R_4 = 100Ω, 1KΩ, 10KΩ, and R_5 = 2KΩ.
(c) v-i curve for R_1 = 60KΩ, R_2 = 3KΩ, R_3 = 100KΩ, R_4 = 1KΩ, and R_5 = 2, 5, 20KΩ.

Fig. 19. (a) A voltage-driven two-transistor one-port N.
(b) A current-driven two-transistor one-port N.
(c) Simplified circuit obtained by short-circuiting V_s and by replacing each resistor in N by either an open circuit or a short circuit.
(d) Simplified circuit obtained by open-circuiting I_s and by replacing each resistor in N by either an open circuit or a short circuit.

Fig. 20. Two-transistor feedback structure.

Fig. 21. (a) A two-transistor current-driven one-port.
(b) Associated feedback structure.

Fig. 22. (a) Two-transistor analog of a pnpn diode or SCR.
(b) Associated feedback structure.
(c) Spice-simulated v-i curve is monotone increasing.

Fig. 23. (a) One-port N' in series with positive resistor.
(b) The v-i curve of the composite one-port N is current-controlled for small values of R, and becomes monotone increasing for large values of R.
(c) The v-i curve of the composite one-port N is multivalued for large values of R.

Fig. 24. (a) One-port N' in parallel with positive resistor.
(b) The v-i curve of the composite one-port N is multivalued for small values of R.
(c) The v-i curve of the composite one-port N is voltage-controlled for large values of R, and becomes monotone-increasing for small values of R.

Fig. 25. Three exhaustive ways for inserting a voltage source by plier-entry to the two-transistor feedback structure.

Fig. 26. Seven exhaustive ways for connecting a resistor to the circuit of Fig. 25(c).

Fig. 27. Four exhaustive collector-emitter combinations of two npn transistors for the circuit of Fig. 26.

Fig. 28. Three exhaustive ways for connecting a current source by soldering-iron entry to the two-transistor feedback structure.

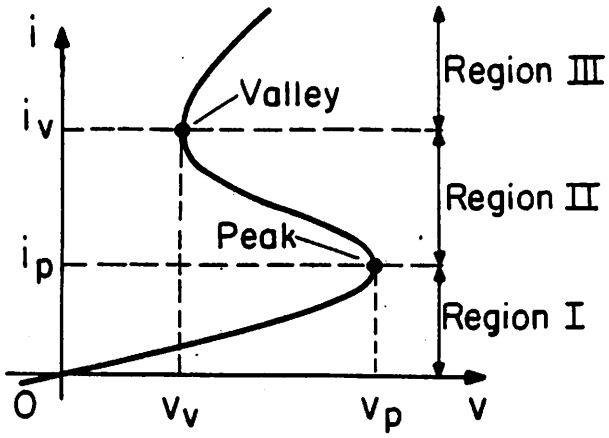
Fig. 29. Seven exhaustive ways for connecting a resistor to the circuit of Fig. 27(a).

Fig. 30. (a) one-resistor configuration 1 containing a feedback structure.
(b) Typical v-i curve ($0.5V < V_B < 0.8V$).

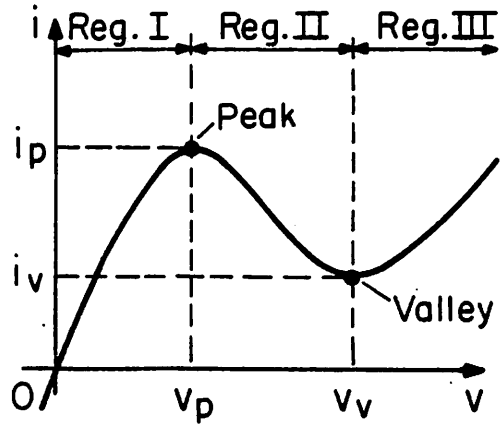
Fig. 31. Two-resistor configuration 2 containing a feedback structure.

Fig. 32. Three circuit candidates containing a feedback structure where both transistors can operate in the active region simultaneously.

Fig. A-1. (a) Feedback structure for the circuit in Fig. 32(c).
(b) Circuit model for dc analysis.

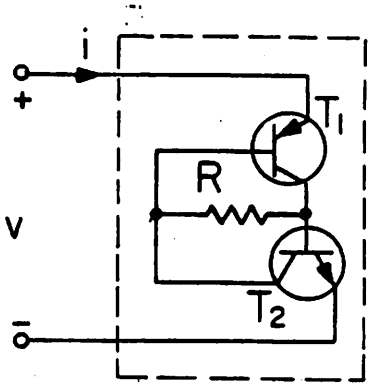


(a)

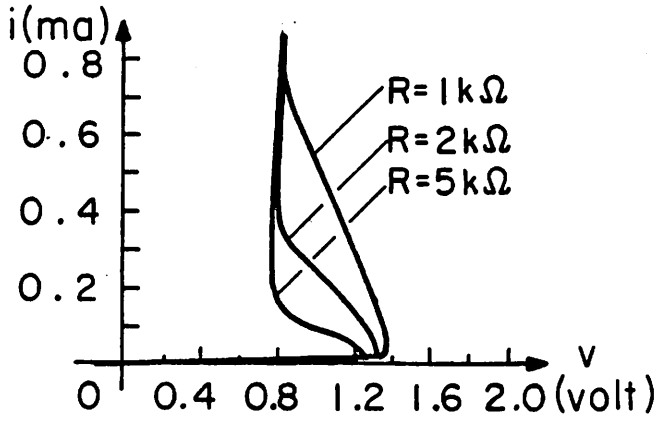


(b)

Fig. 1

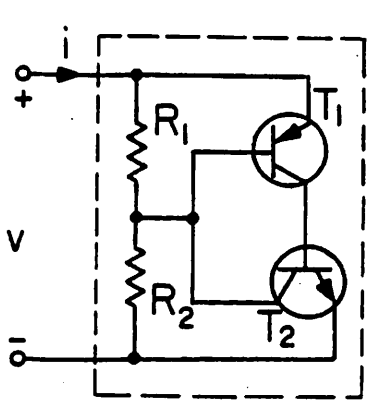


(a)

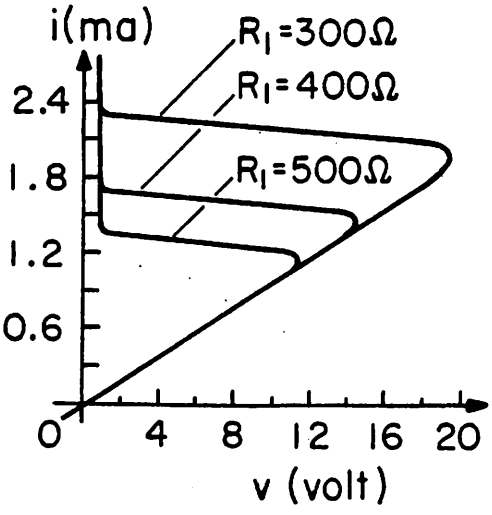


(b)

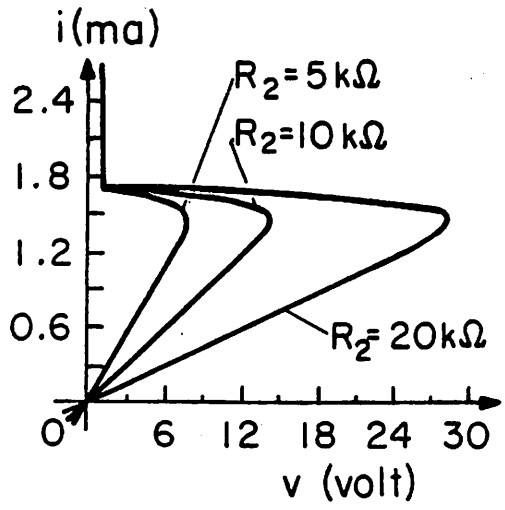
Fig. 2



(a)

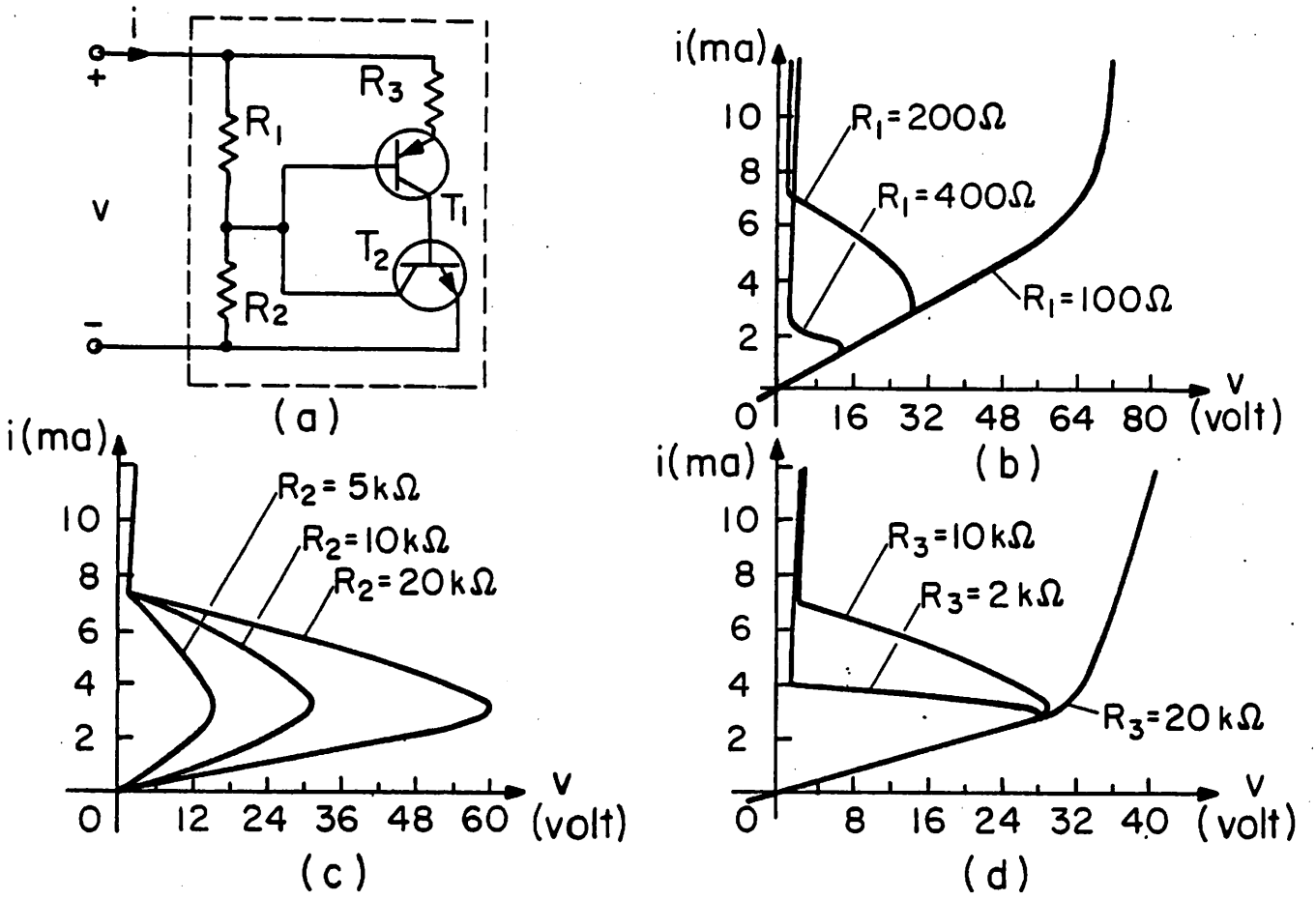


(b)



(c)

Fig. 3


i
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R1
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T1
T2
R2
v
−
(a)
i(ma)
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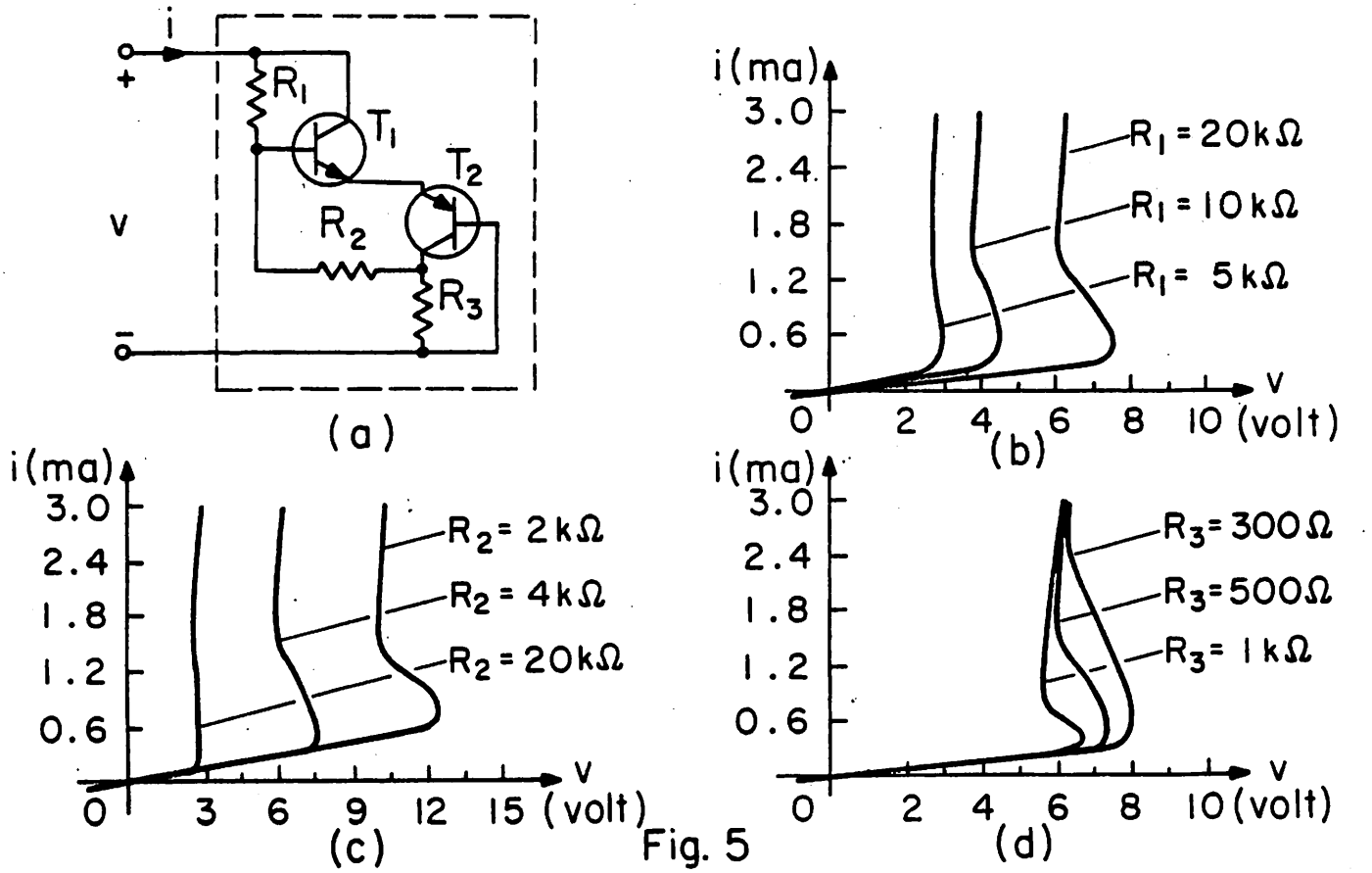
6
4
2
0
R1=200Ω
R1=400Ω
R1=100Ω
16 32 48 64 80 (volt)
v
(b)
R2=5kΩ
R2=10kΩ
R2=20kΩ
12 24 36 48 60 (volt)
(c)
R3=10kΩ
R3=2kΩ
R3=20kΩ
8 16 24 32 40 (volt)
(d)

Fig. 4


i
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3.0
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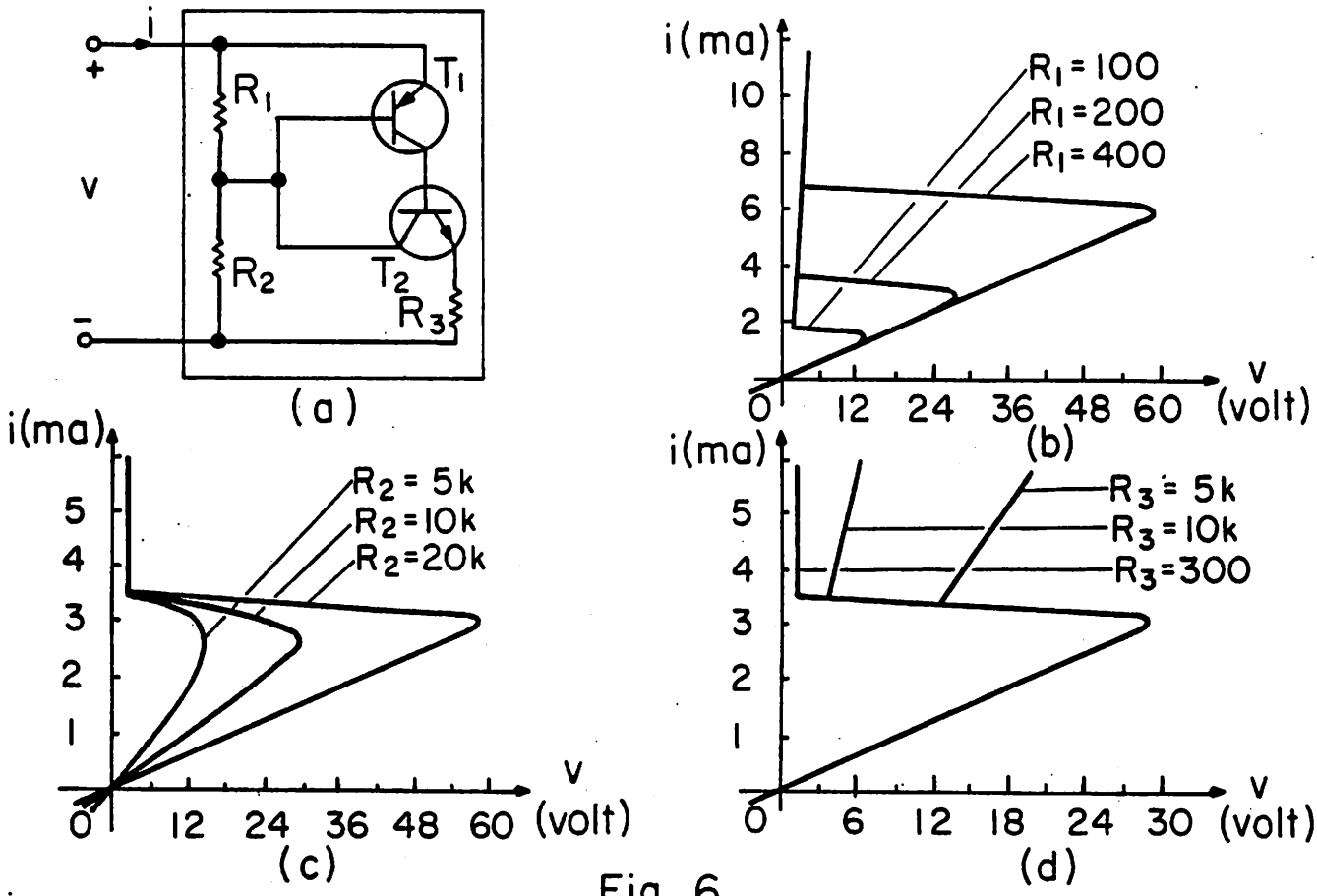
1.8
1.2
0.6
0
R1=20kΩ
R1=10kΩ
R1=5kΩ
2 4 6 8 10 (volt)
v
(b)
R2=2kΩ
R2=4kΩ
R2=20kΩ
3 6 9 12 15 (volt)
(c)
R3=300Ω
R3=500Ω
R3=1kΩ
2 4 6 8 10 (volt)
(d)

Fig. 5


i
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R1 = 400
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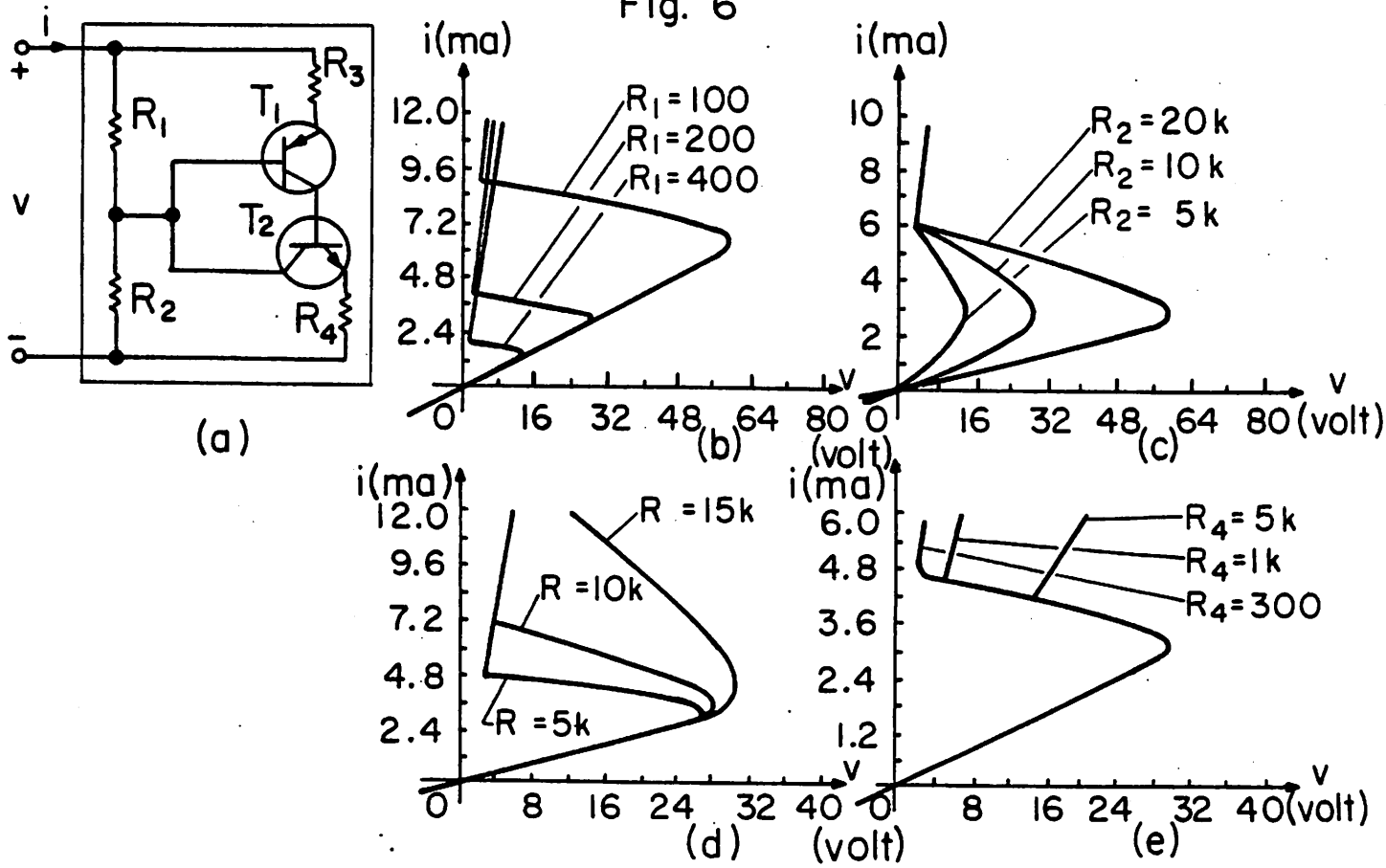
(volt)
(b)
R2 = 5k
R2 = 10k
R2 = 20k
(c)
R3 = 5k
R3 = 10k
R3 = 300
(d)

Fig. 6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R1 = 100
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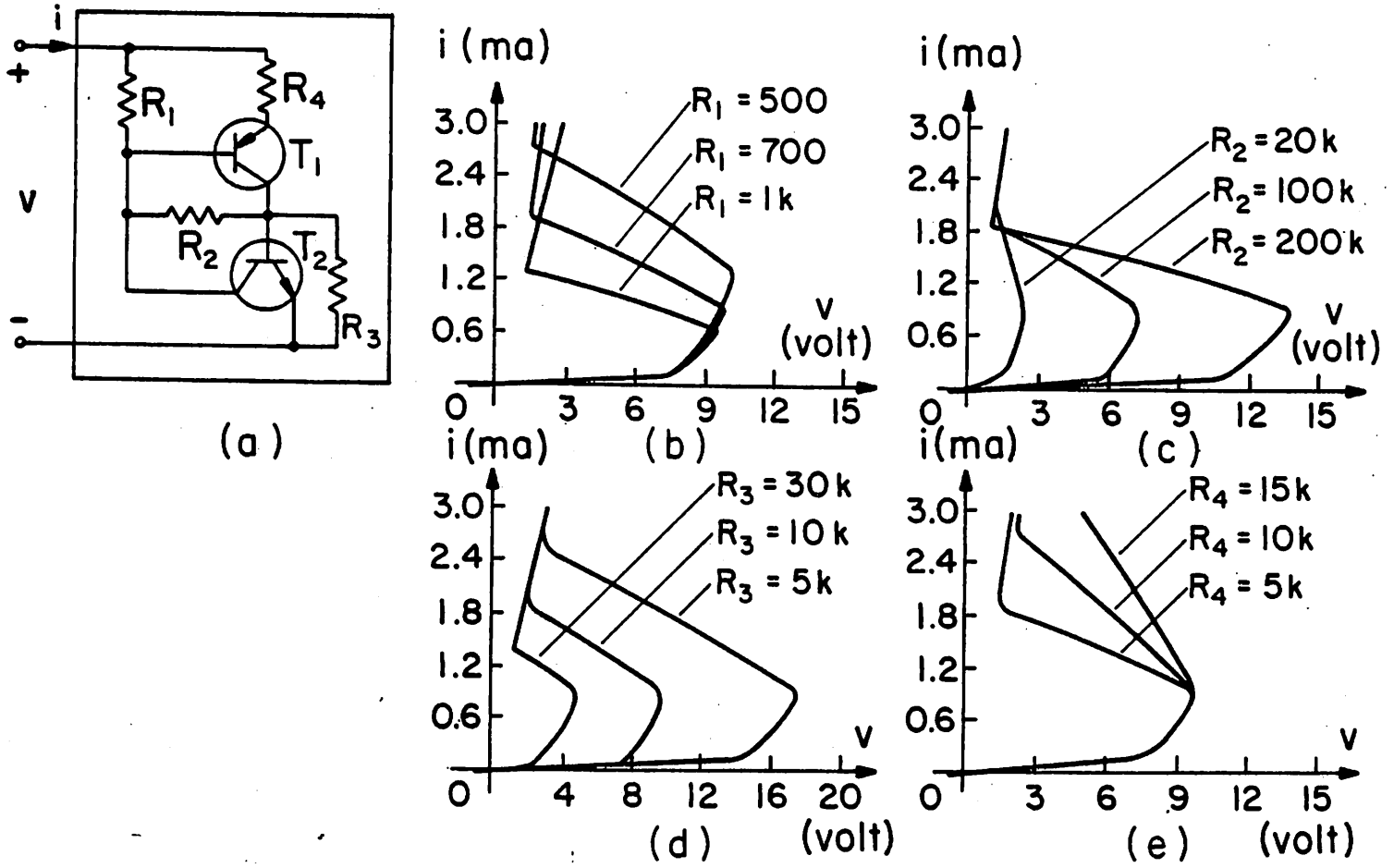
V
(volt)
(b)
R2 = 20k
R2 = 10k
R2 = 5k
(c)
R = 15k
R = 10k
R = 5k
(d)
R4 = 5k
R4 = 1k
R4 = 300
(e)

Fig. 7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R1 = 500
R1 = 700
R1 = 1k
V
(volt)
0
3
6
9
12
15
(b)
i(ma)
R2 = 20k
R2 = 100k
R2 = 200k
(c)
R3 = 30k
R3 = 10k
R3 = 5k
4
8
16
20
(d)
R4 = 15k
R4 = 10k
R4 = 5k
(e)

fig 8

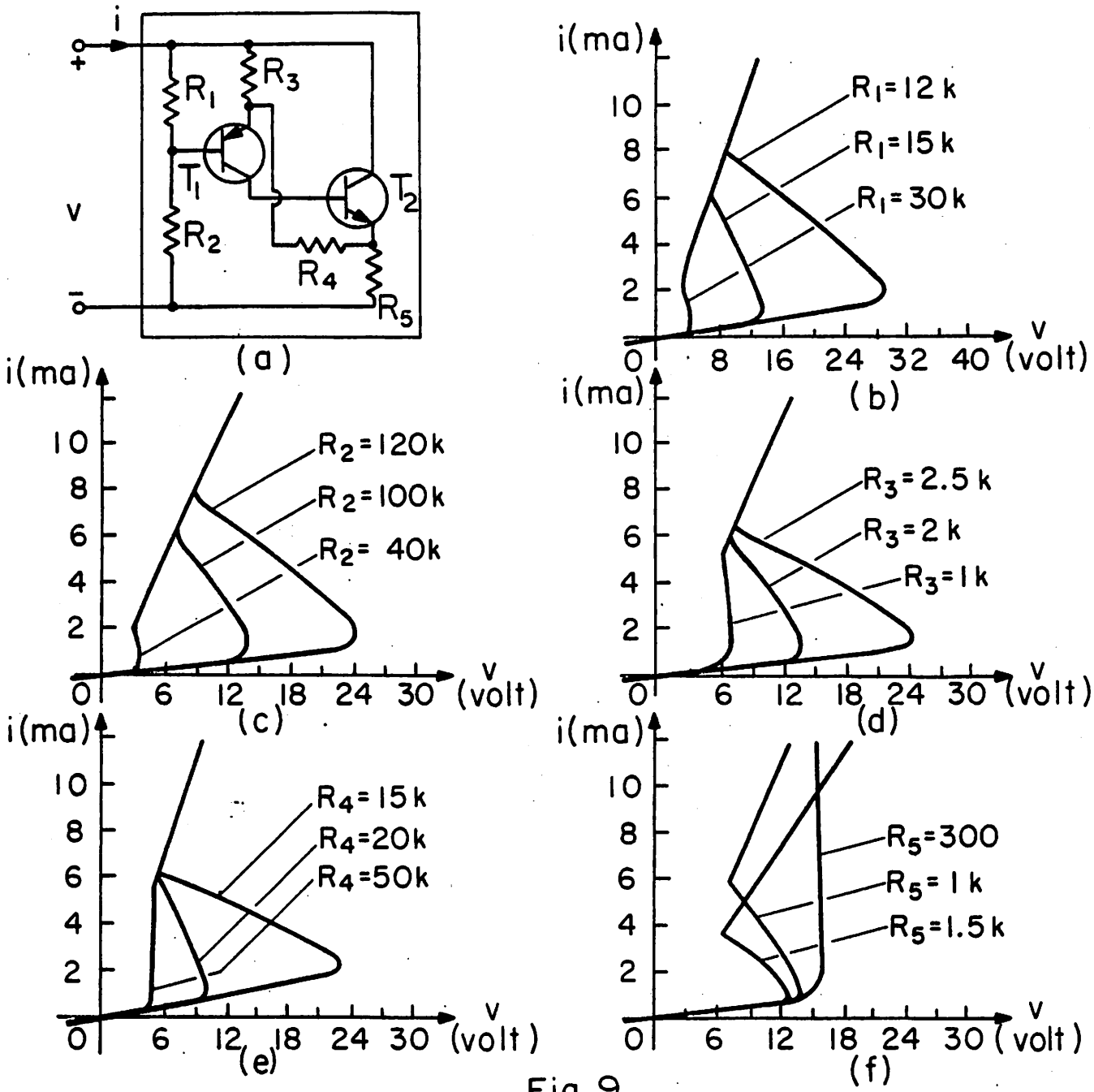

i
+
v
−
R1
R3
T1
T2
R2
R4
R5
(a)
i(ma)
10
8
6
4
2
0
8
16
24
32
40
V
(volt)
R1=12 k
R1=15 k
R1=30 k
(b)
i(ma)
10
8
6
4
2
0
6
12
18
24
30
V
(volt)
R2=120k
R2=100k
R2= 40k
(c)
i(ma)
10
8
6
4
2
0
6
12
18
24
30
V
(volt)
R3=2.5 k
R3=2 k
R3=1 k
(d)
i(ma)
10
8
6
4
2
0
6
12
18
24
30
V
(volt)
R4=15k
R4=20k
R4=50k
(e)
i(ma)
10
8
6
4
2
0
6
12
18
24
30
V
(volt)
R5=300
R5= 1 k
R5=1.5 k
(f)

Fig. 9

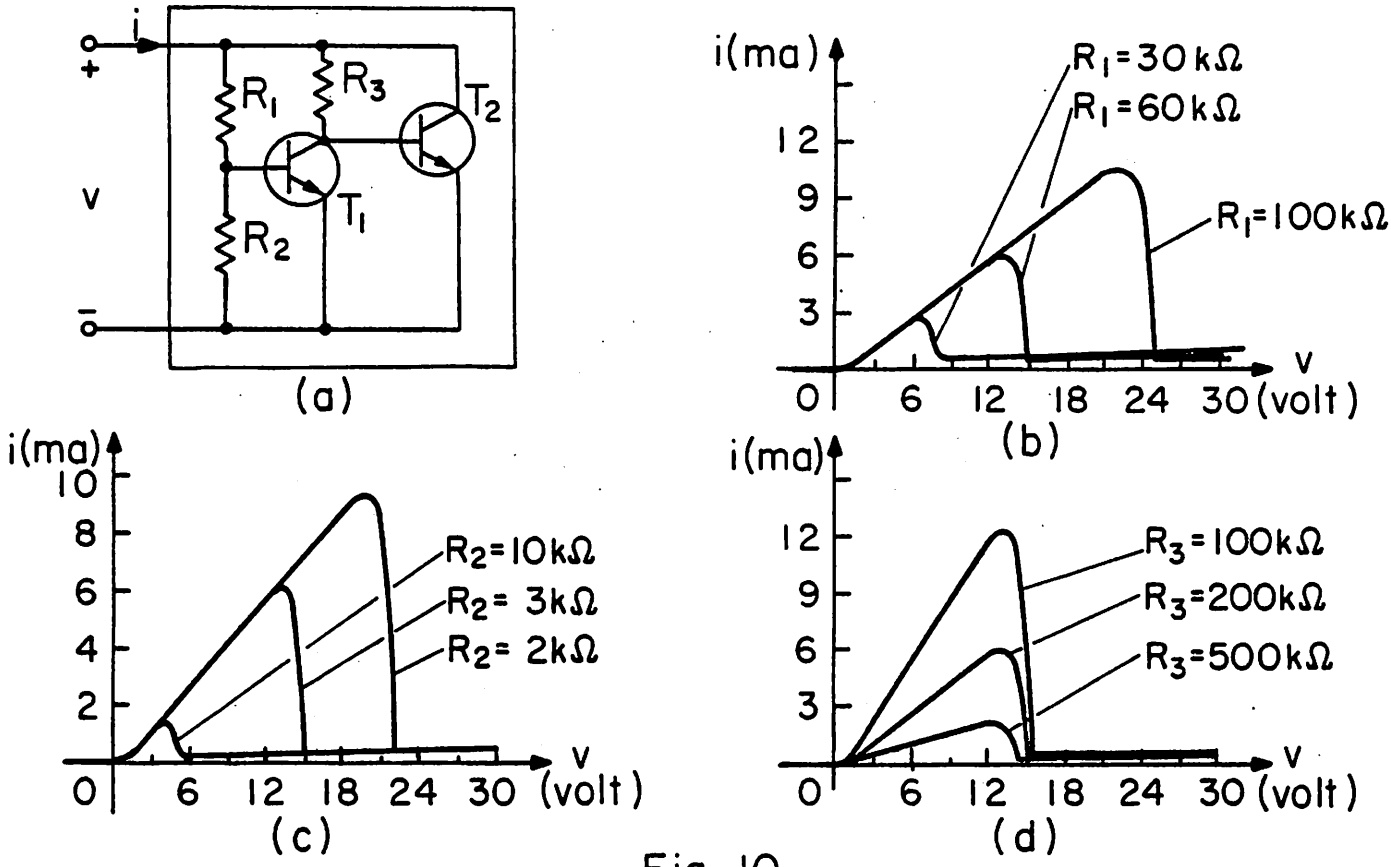

i
+
v
−
R1
R2
R3
T1
T2
(a)
i(ma)
R1=30kΩ
R1=60kΩ
R1=100kΩ
12
9
6
3
0
6
12
18
24
30
v
(volt)
(b)
i(ma)
10
8
6
4
2
R2=10kΩ
R2= 3kΩ
R2= 2kΩ
(c)
i(ma)
12
9
6
3
R3=100kΩ
R3=200kΩ
R3=500kΩ
(d)

Fig. 10

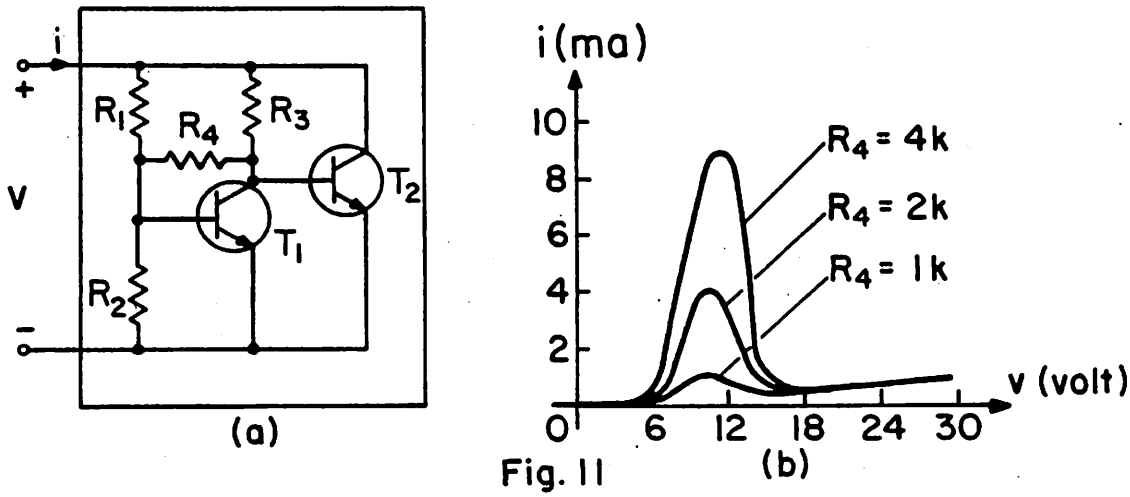

i
+
v
−
R1
R4
R3
T1
T2
R2
(a)
i(ma)
10
8
6
4
2
R4 = 4k
R4 = 2k
R4 = 1k
0
6
12
18
24
30
v (volt)
(b)

Fig. 11

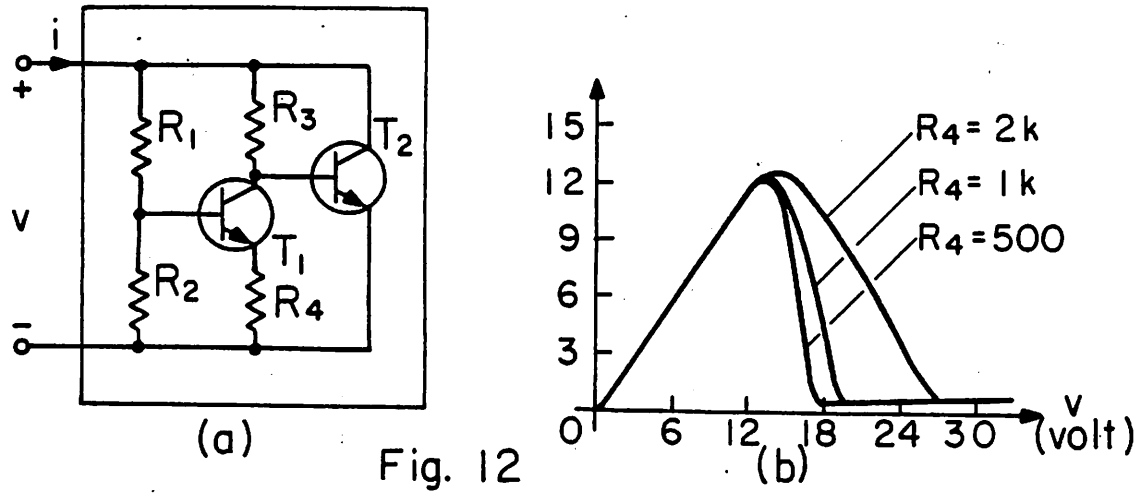

i
+
v
−
R1
R2
R3
R4
T1
T2
(a)
15
12
9
6
3
0
6
12
18
24
30
v
(volt)
R4 = 2k
R4 = 1k
R4 = 500
(b)

Fig. 12

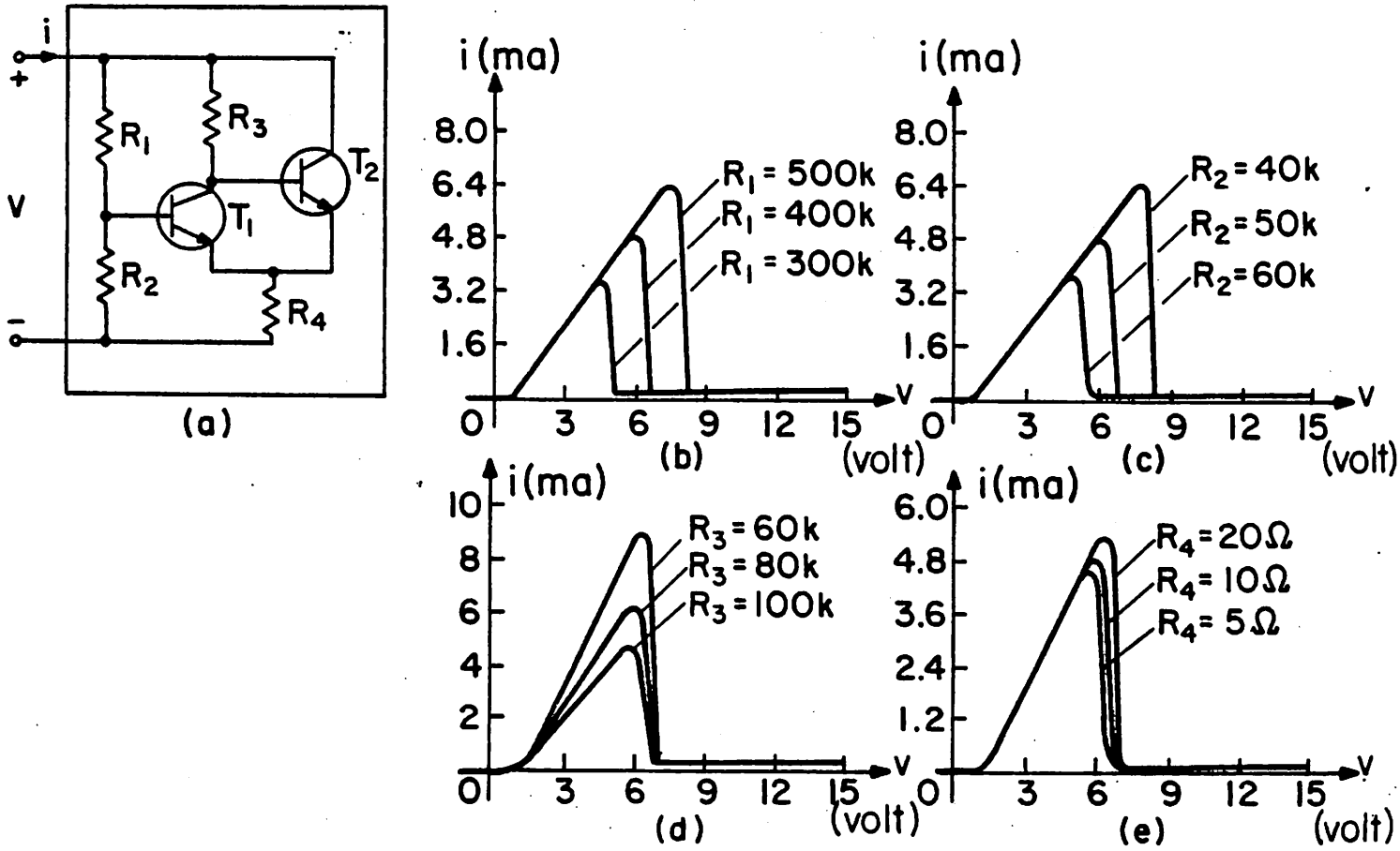

i
+
v
−
R1
R2
R3
R4
T1
T2
(a)
i(ma)
8.0
6.4
4.8
3.2
1.6
0
3
6
9
12
15
v
(volt)
R1 = 500k
R1 = 400k
R1 = 300k
(b)
R2 = 40k
R2 = 50k
R2 = 60k
(c)
10
8
6
4
2
R3 = 60k
R3 = 80k
R3 = 100k
(d)
6.0
4.8
3.6
2.4
1.2
R4 = 20Ω
R4 = 10Ω
R4 = 5Ω
(e)

Fig. 13

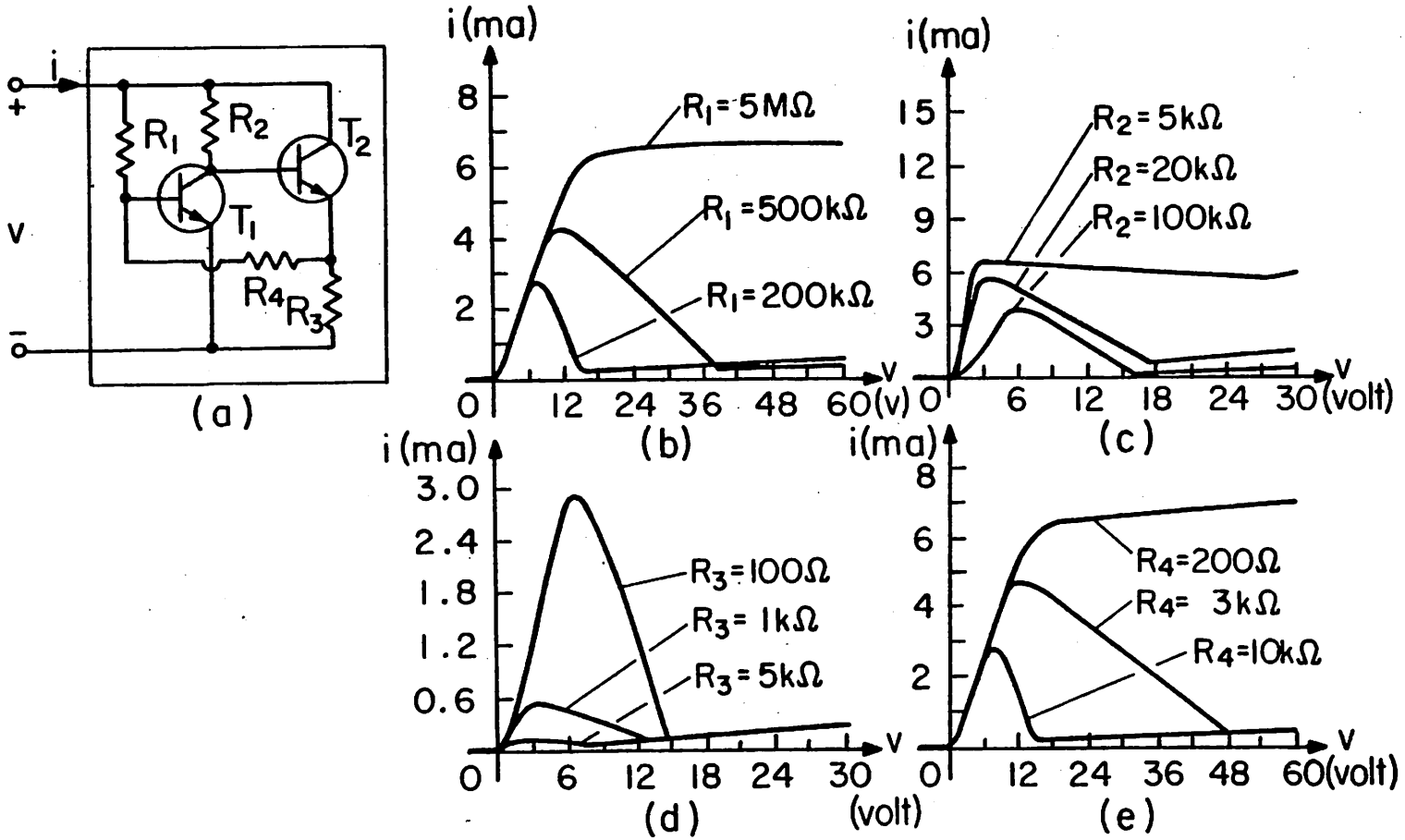

i
+
v
−
R1
R2
T2
T1
R4
R3
(a)
i(ma)
8
6
4
2
R1=5MΩ
R1=500kΩ
R1=200kΩ
0
12
24
36
48
60(v)
v
(b)
i(ma)
15
12
9
6
3
R2=5kΩ
R2=20kΩ
R2=100kΩ
0
6
12
18
24
30(volt)
v
(c)
i(ma)
3.0
2.4
1.8
1.2
0.6
R3=100Ω
R3=1kΩ
R3=5kΩ
0
6
12
18
24
30
(volt)
v
(d)
i(ma)
8
6
4
2
R4=200Ω
R4=3kΩ
R4=10kΩ
0
12
24
36
48
60(volt)
v
(e)

Fig. 14

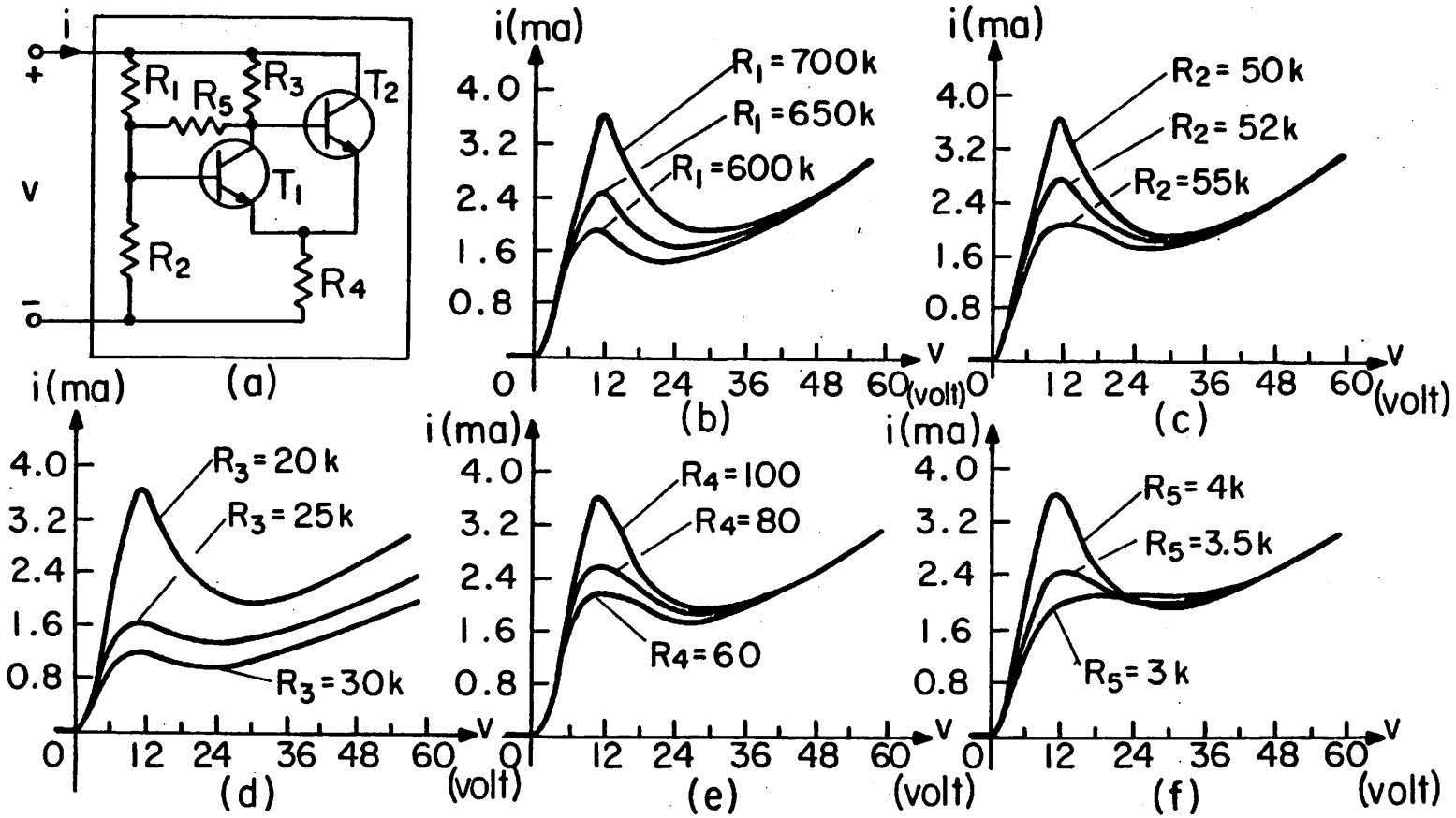

i
+
v
−
R1
R5
R3
T2
T1
R2
R4
(a)
i(ma)
4.0
3.2
2.4
1.6
0.8
0
12 24 36 48 60
v
(volt)
R1 = 700k
R1 = 650k
R1 = 600k
(b)
R2 = 50k
R2 = 52k
R2 = 55k
(c)
R3 = 20k
R3 = 25k
R3 = 30k
(d)
R4 = 100
R4 = 80
R4 = 60
(e)
R5 = 4k
R5 = 3.5k
R5 = 3k
(f)

Fig. 15

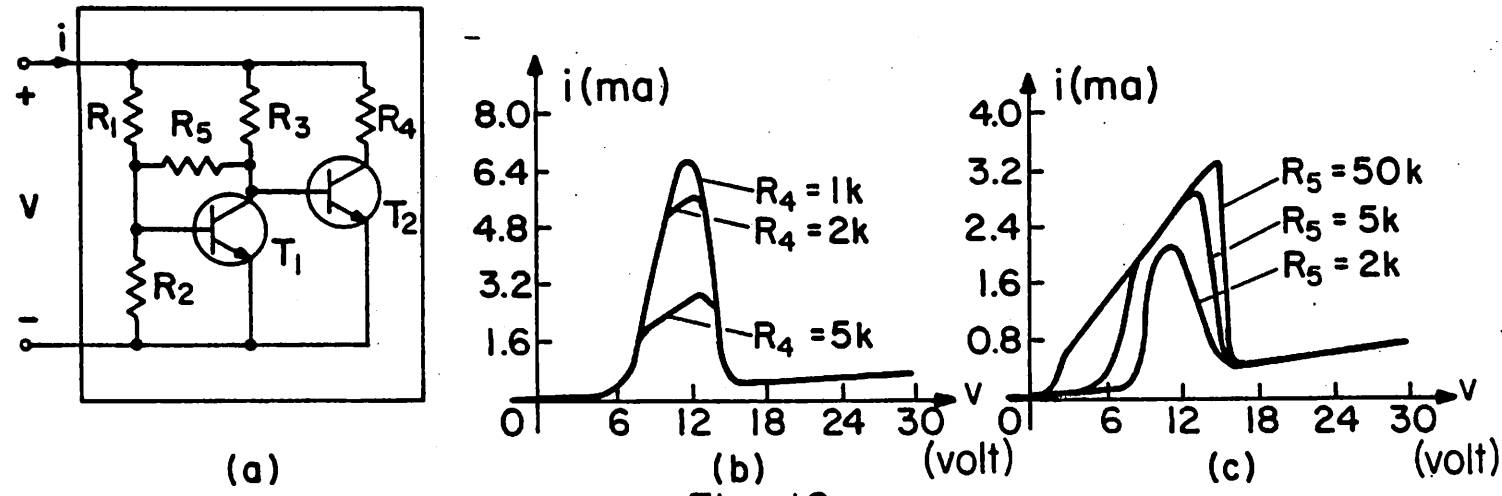


Fig. 16

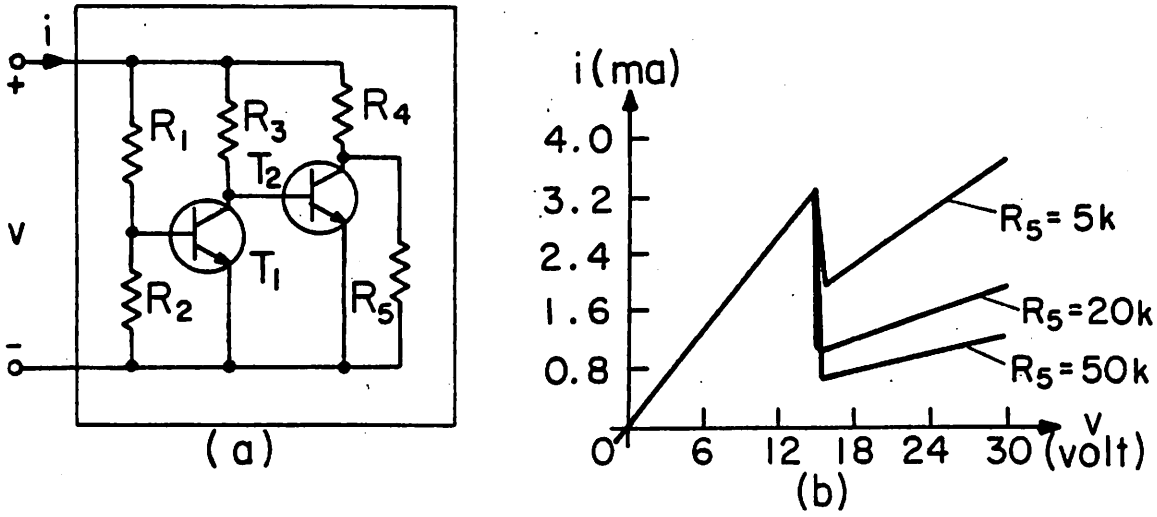


Fig. 17

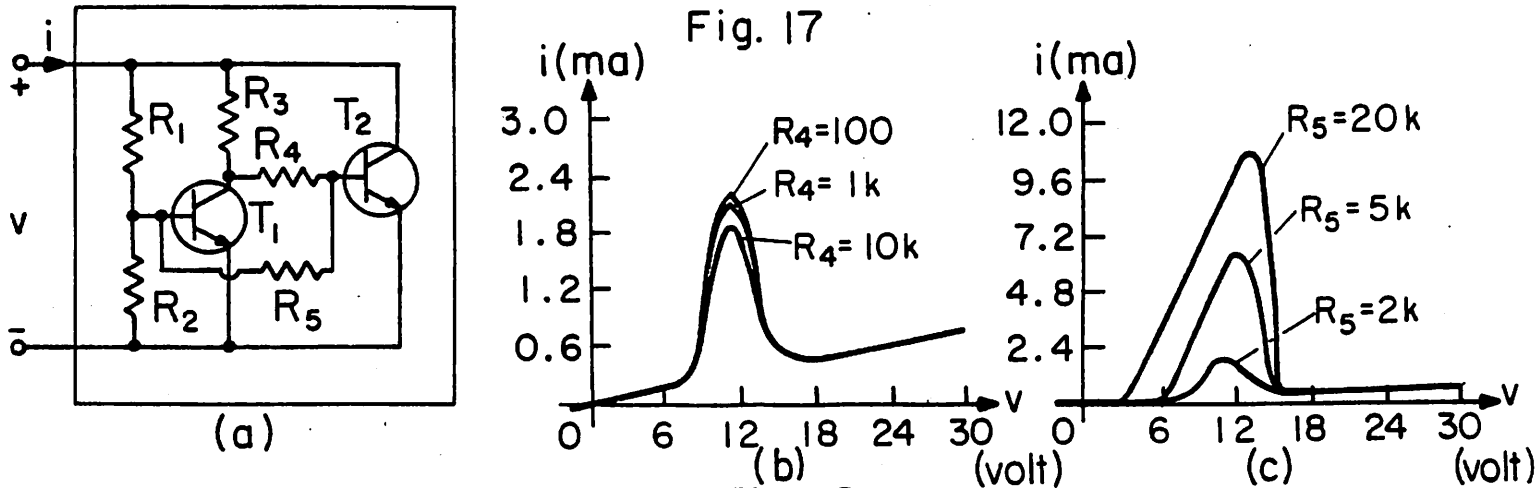


Fig. 18

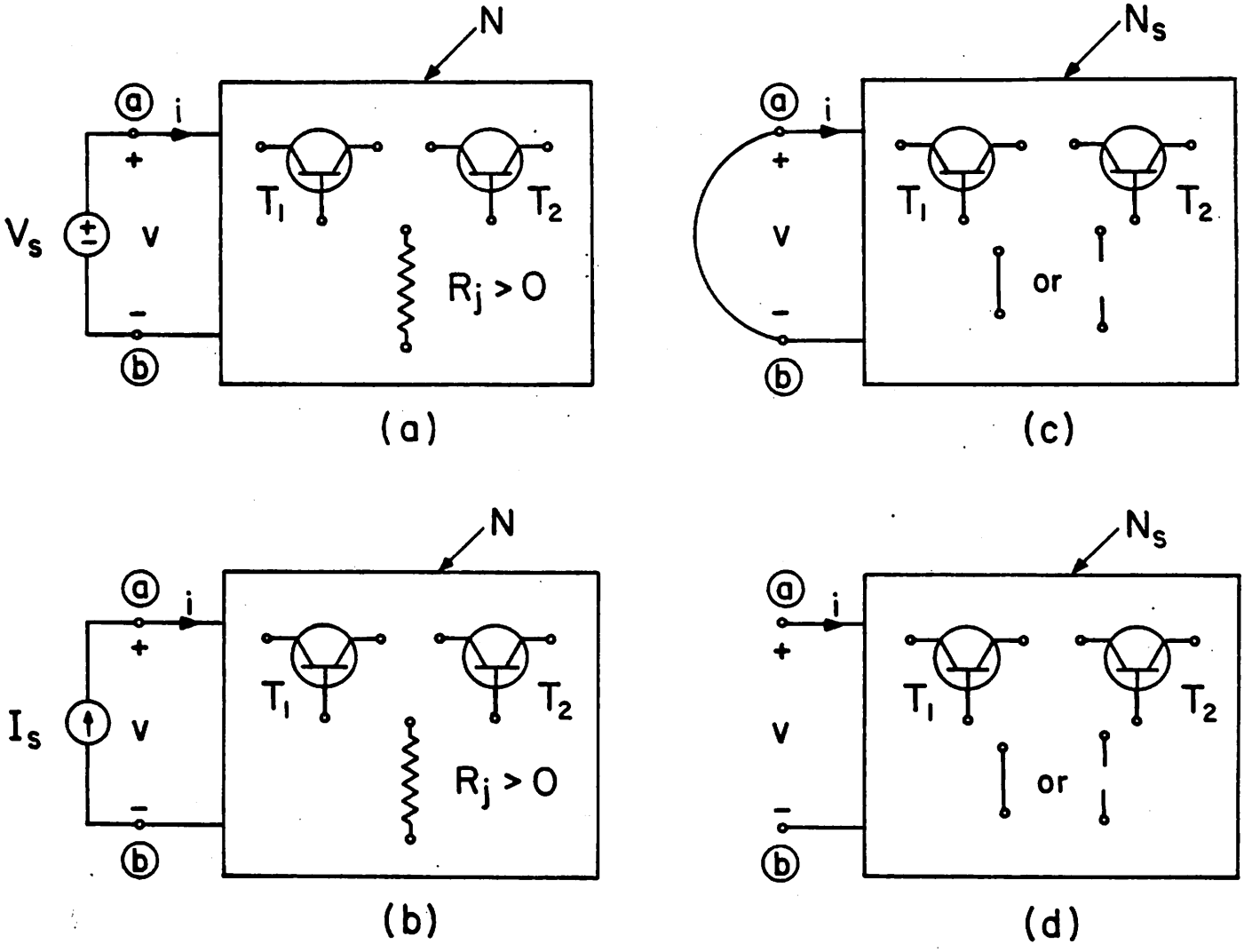


Fig. 19

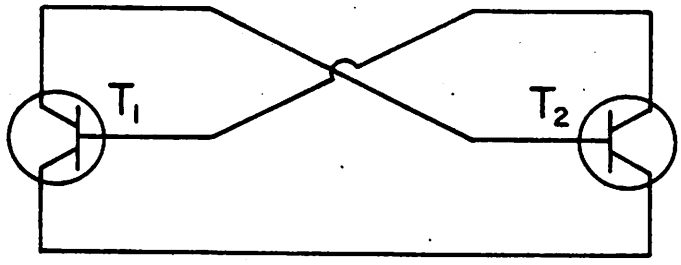


Fig. 20

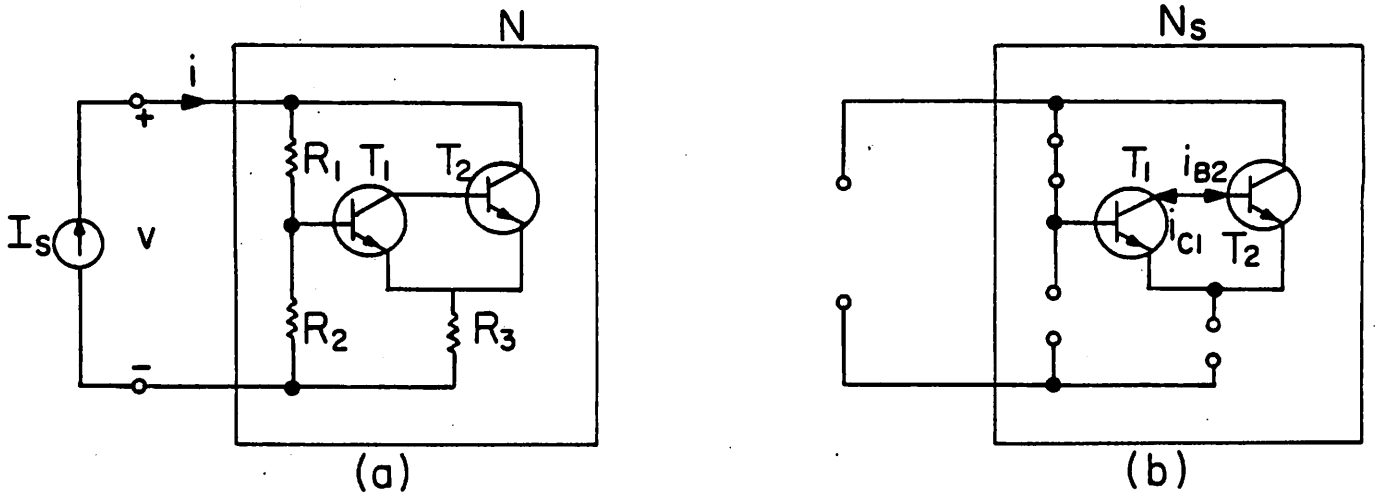


Fig. 21

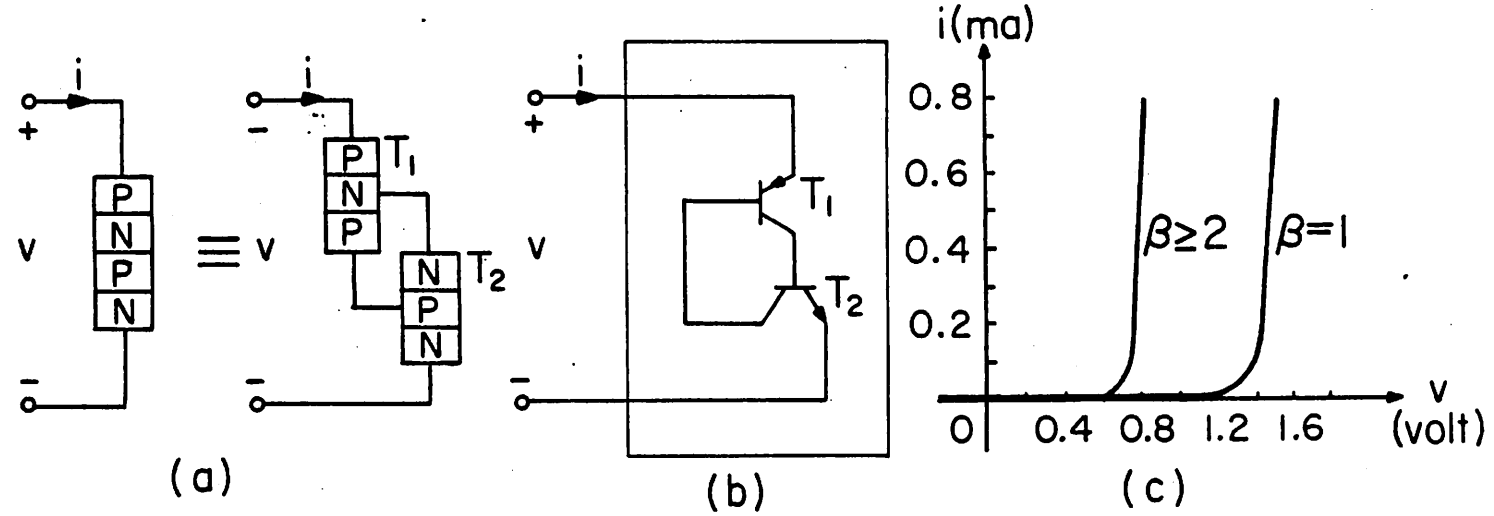


Fig. 22

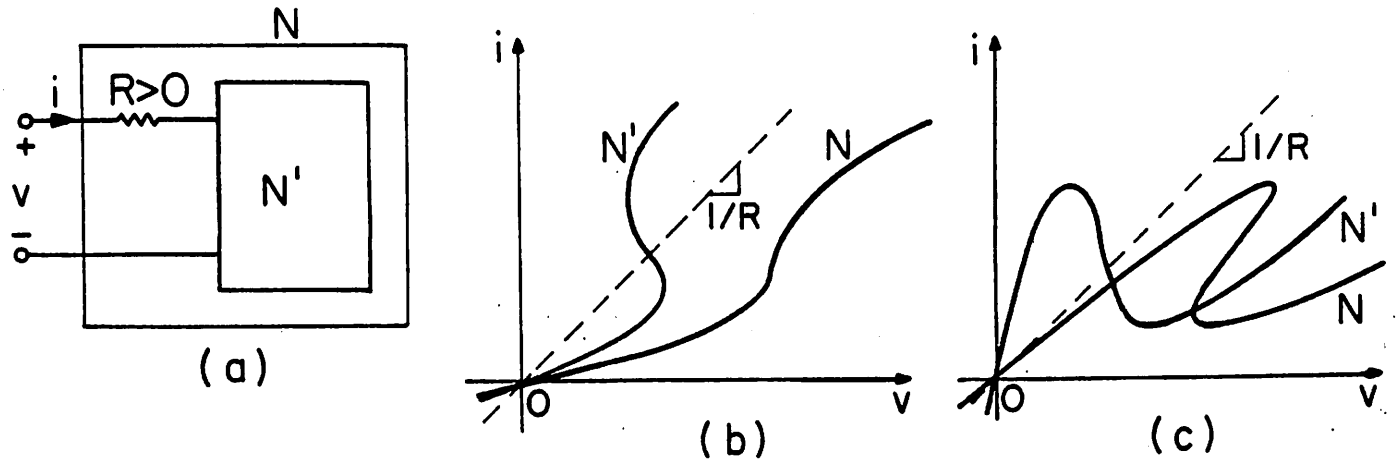


Fig. 23

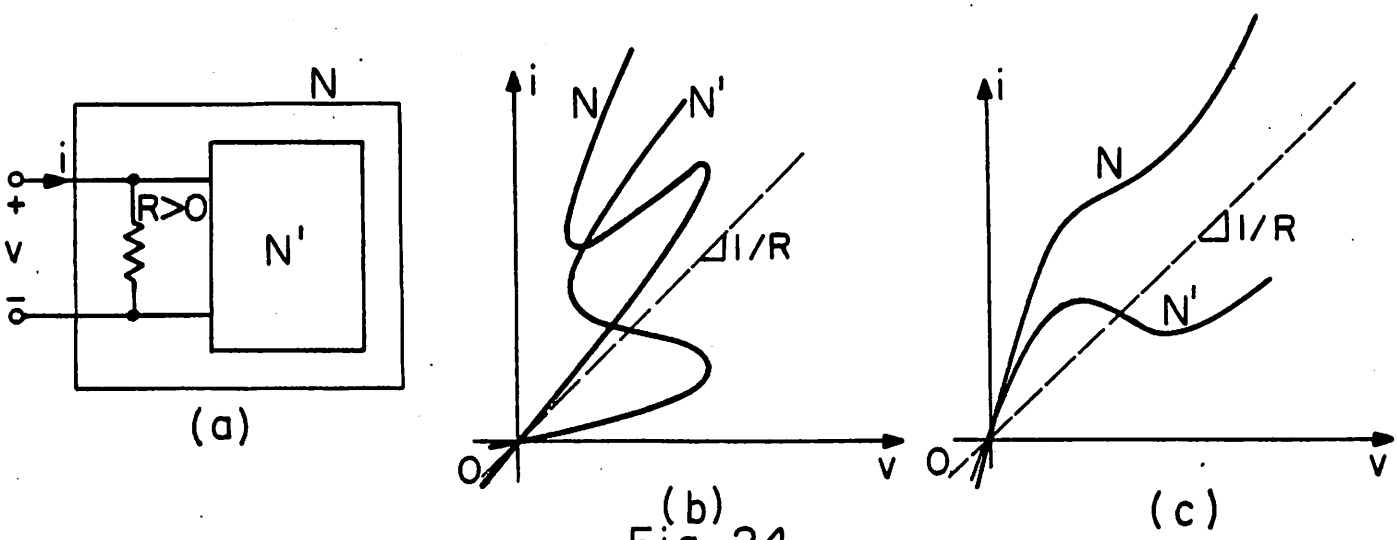


Fig. 24

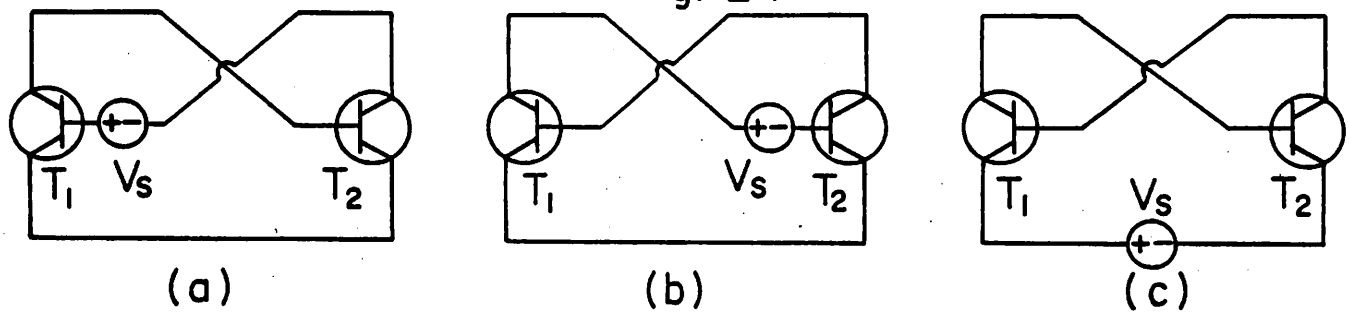


Fig. 25

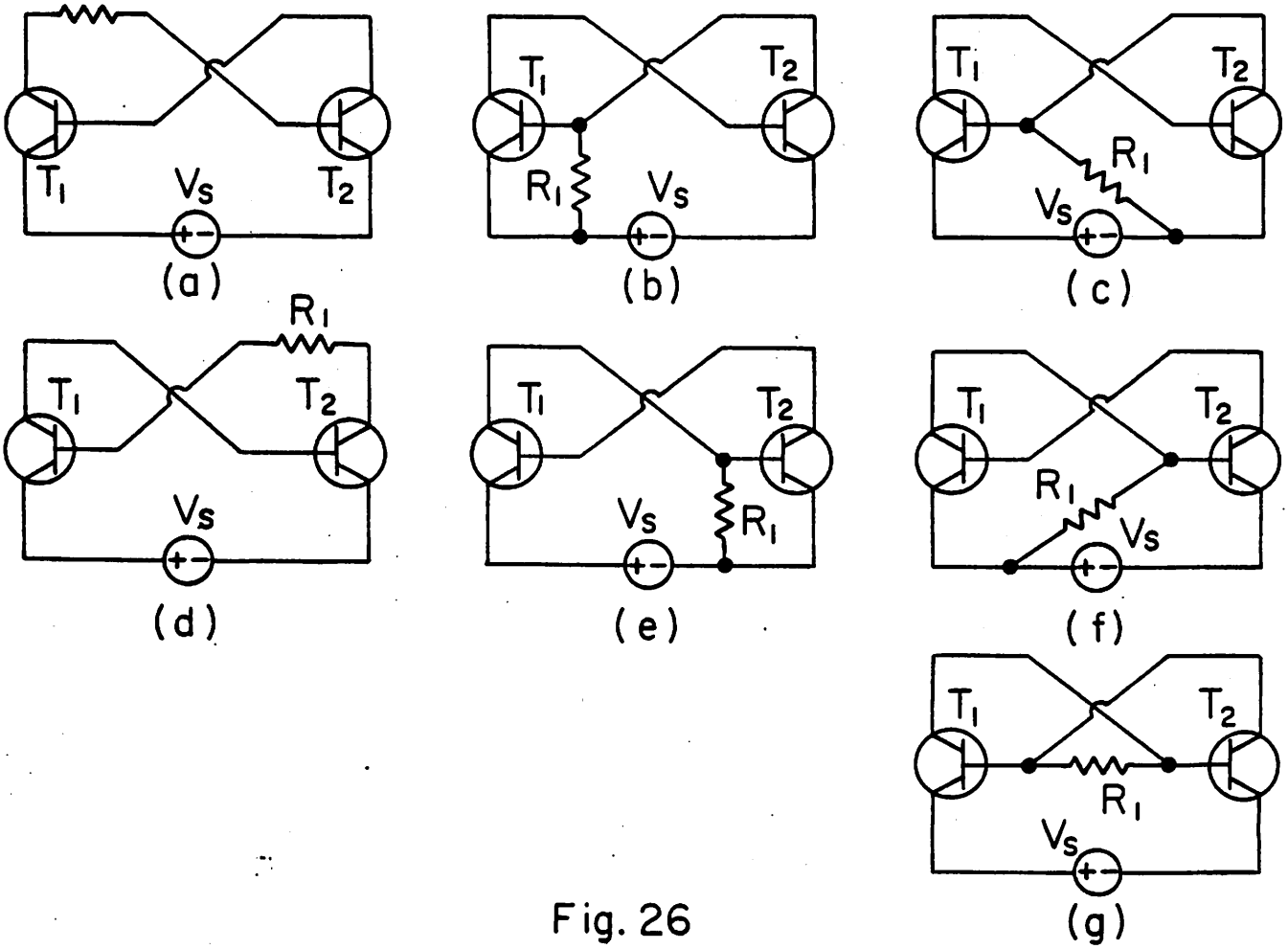


Fig. 26

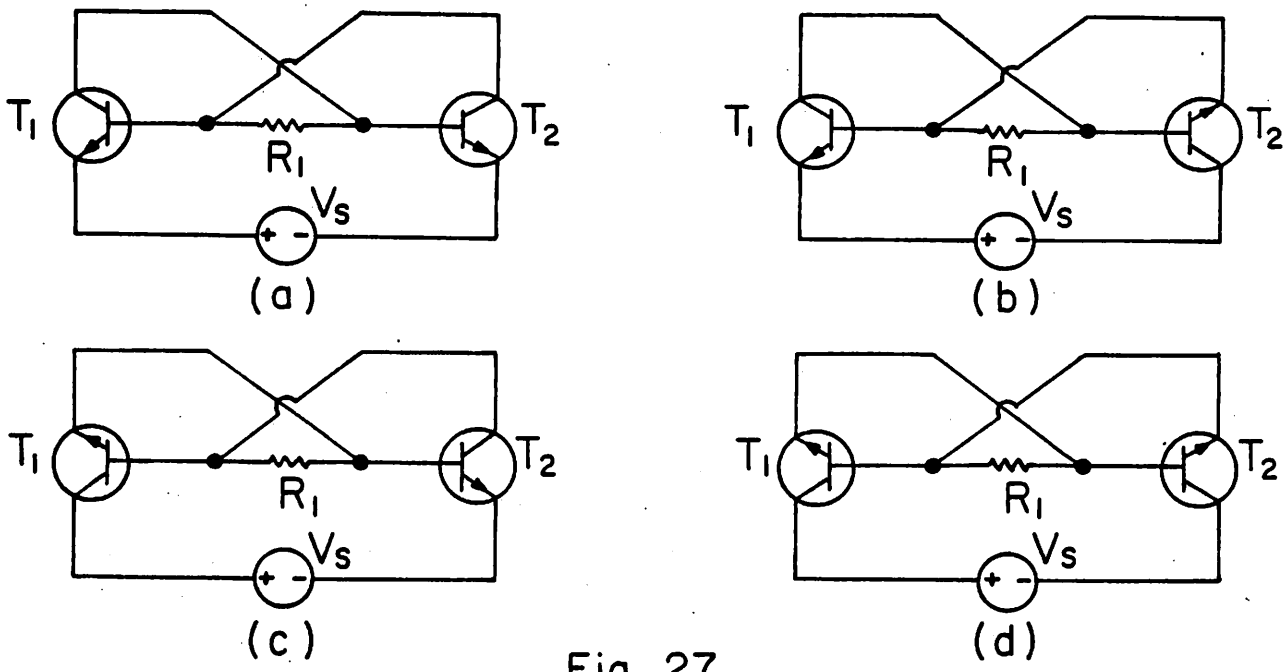


Fig. 27

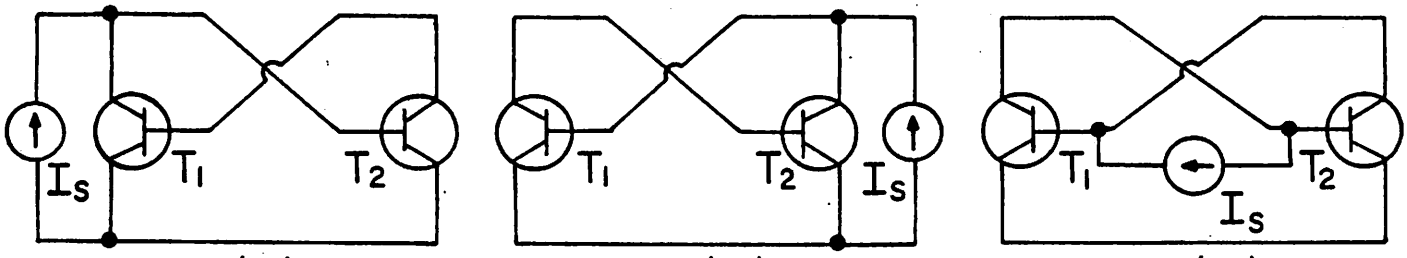


Fig. 28

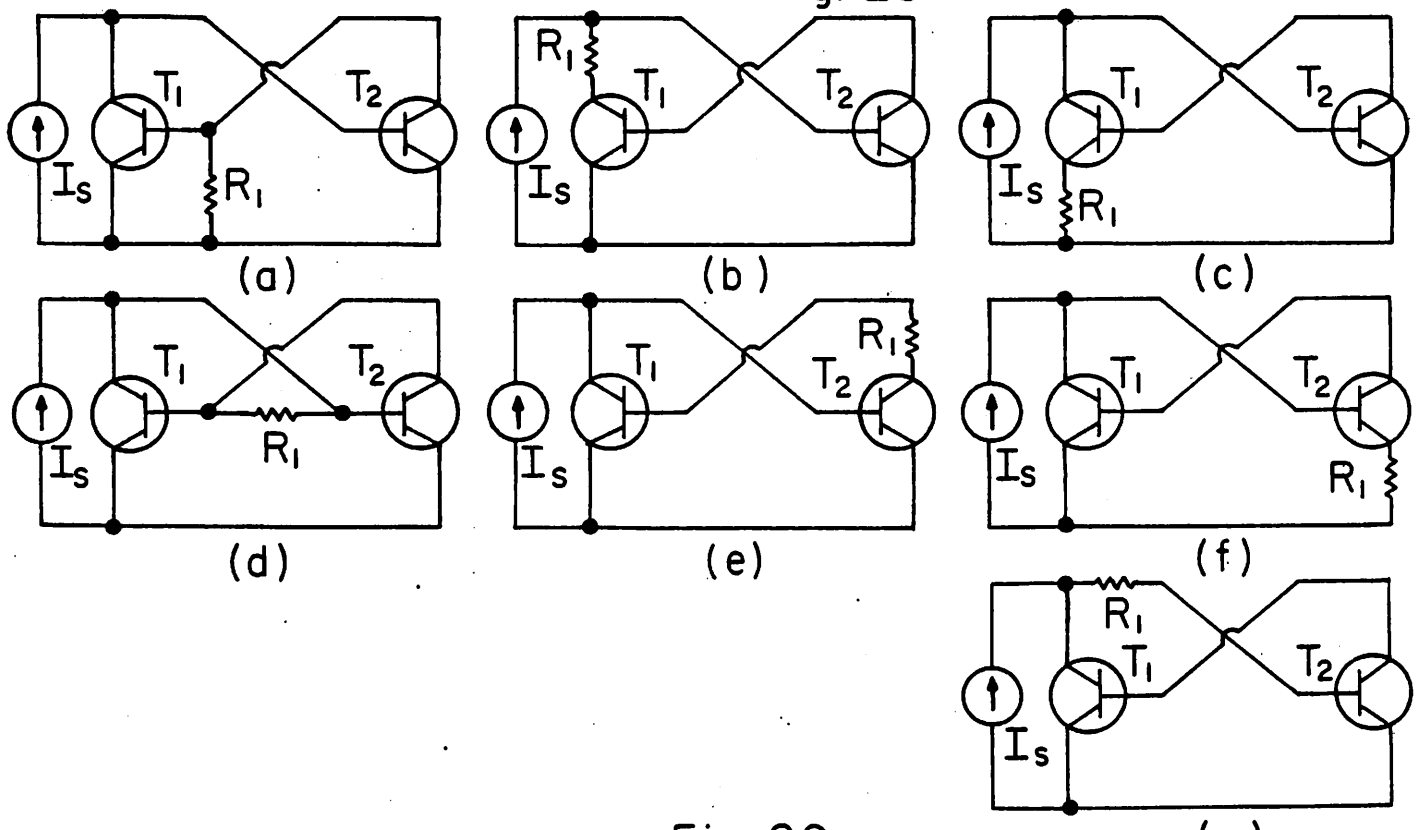


Fig. 29

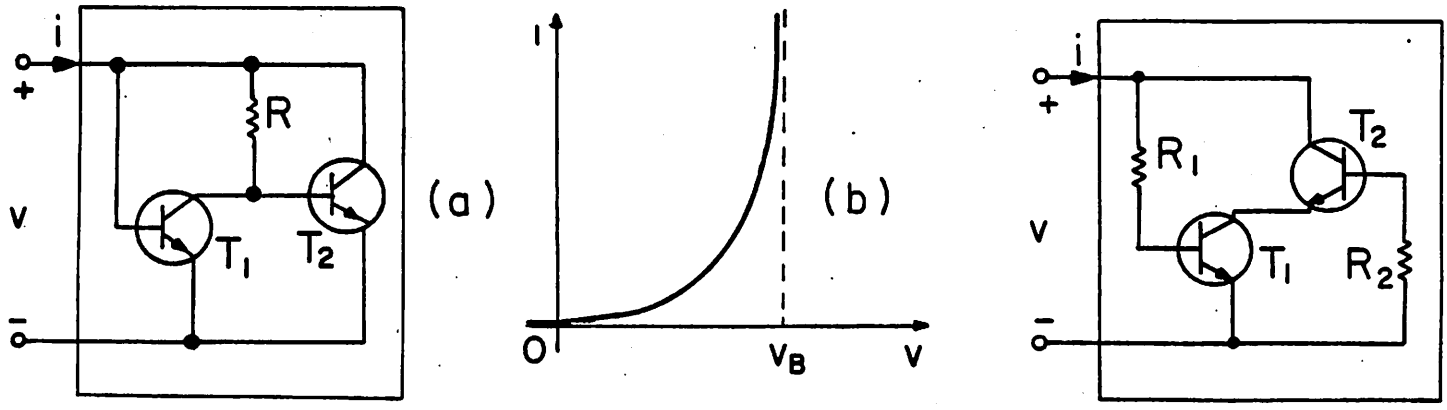


Fig. 30

Fig. 31

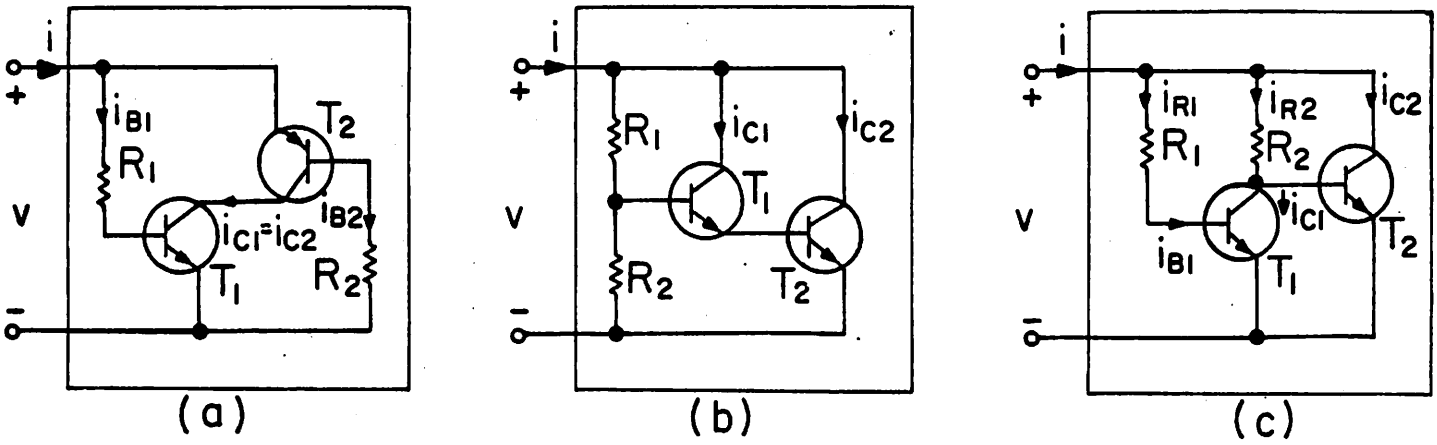


Fig. 32

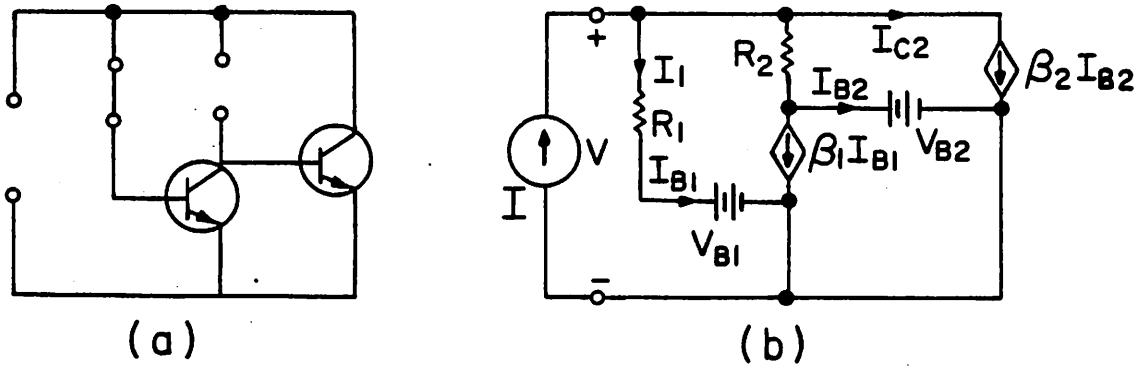
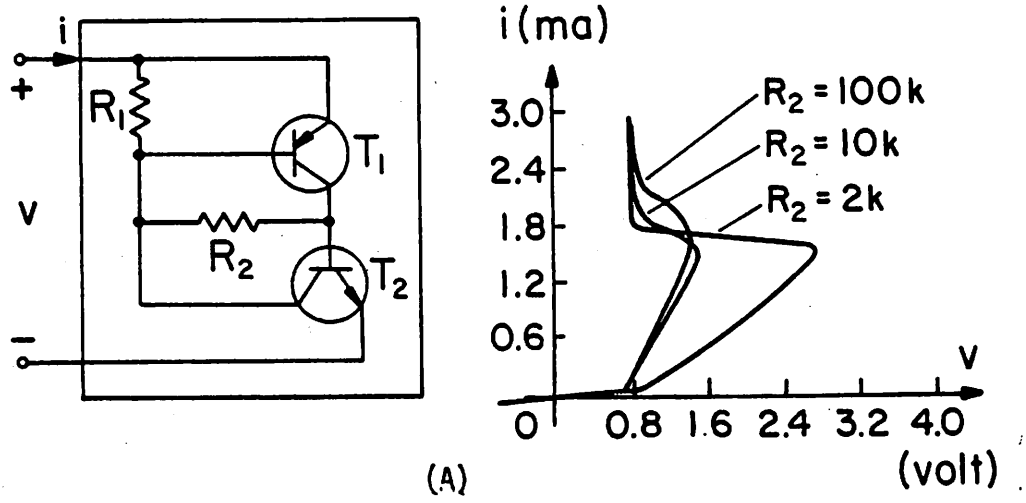


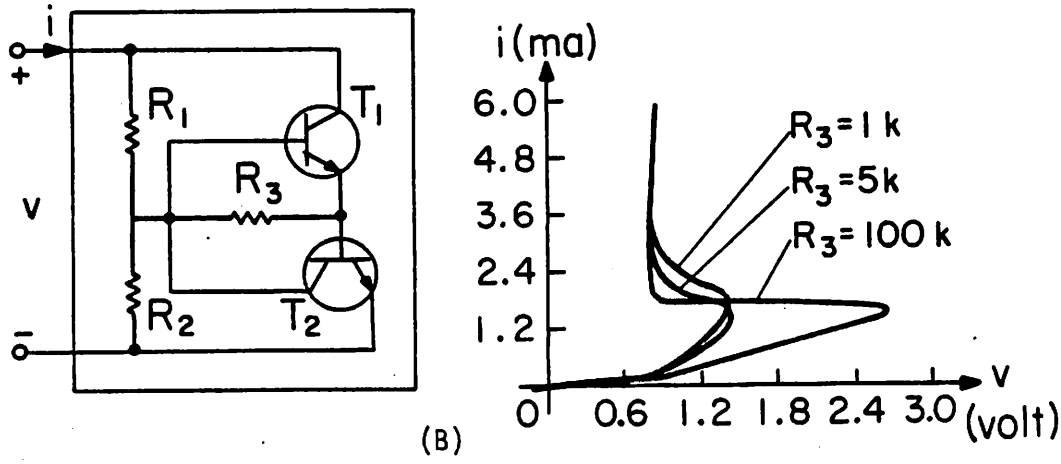
Fig. A.1

APPENDIX B: SAMPLE NEGATIVE RESISTANCE DEVICES

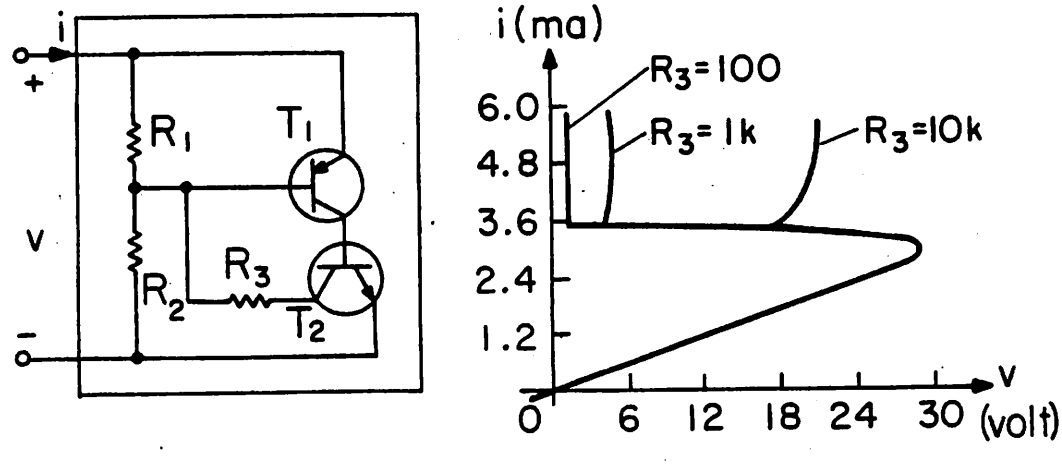
B.1: Type-S Devices



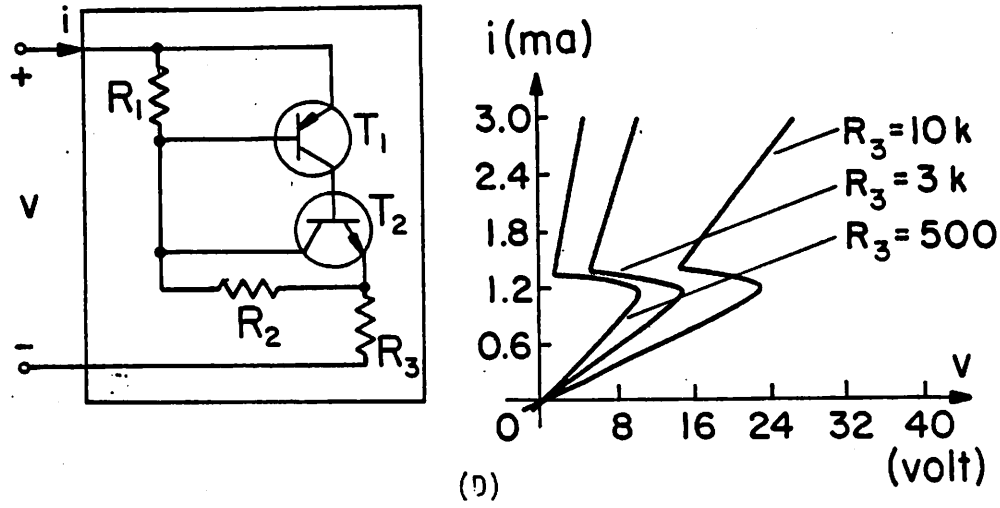
(A)



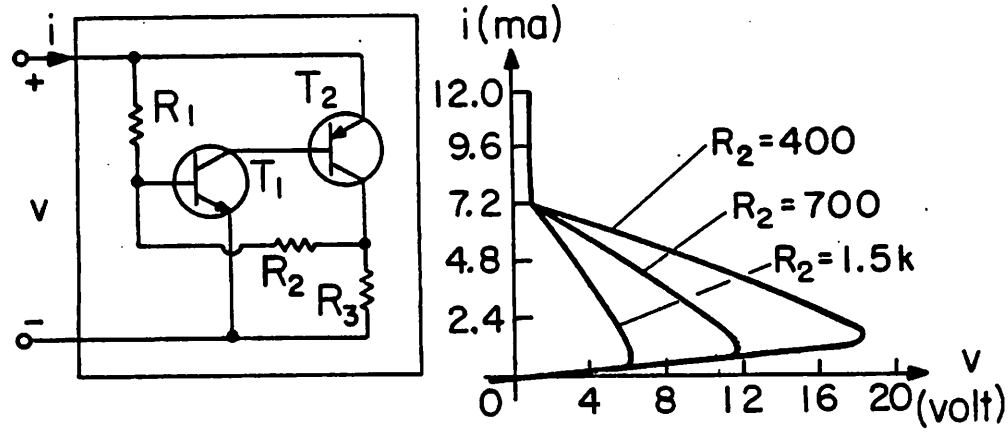
(B)



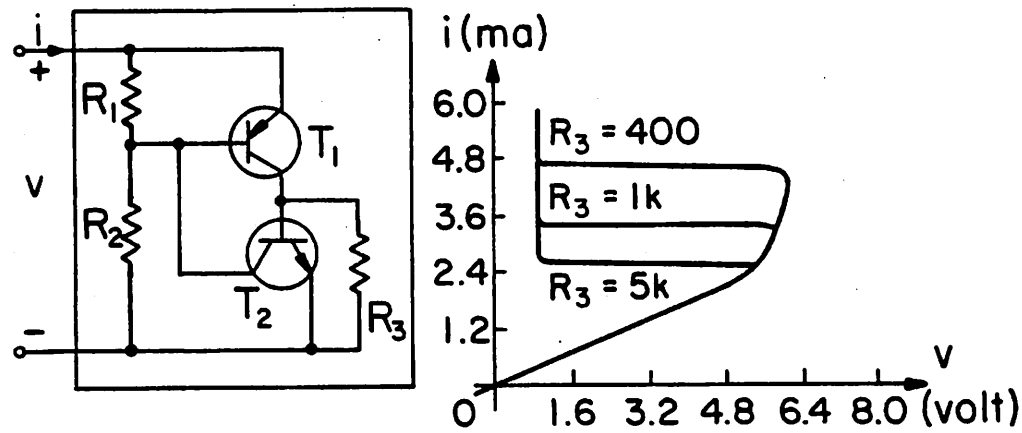
(C)


i
+
V
−
R1
T1
T2
R2
R3
i(ma)
3.0
2.4
1.8
1.2
0.6
0
8
16
24
32
40
V
(volt)
R3=10 k
R3=3 k
R3=500

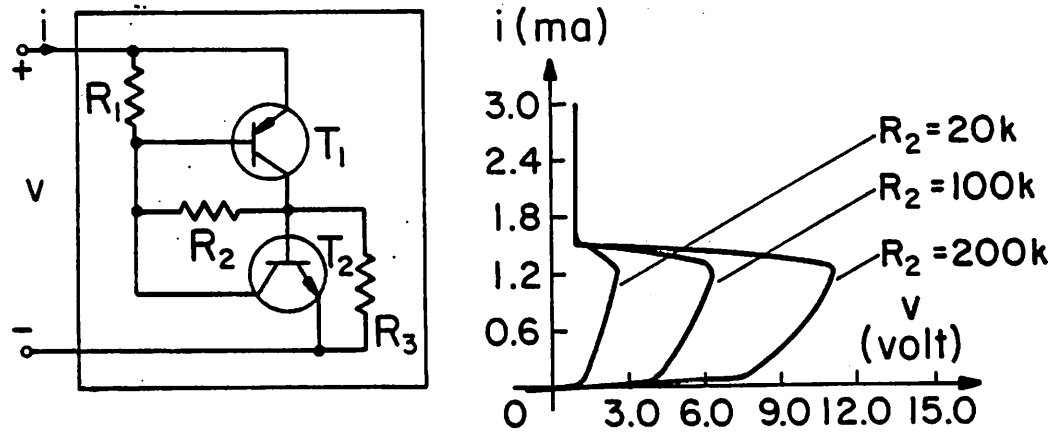
(D)


i
+
V
−
R1
T2
T1
R2
R3
i(ma)
12.0
9.6
7.2
4.8
2.4
0
4
8
12
16
20
V
(volt)
R2=400
R2=700
R2=1.5k

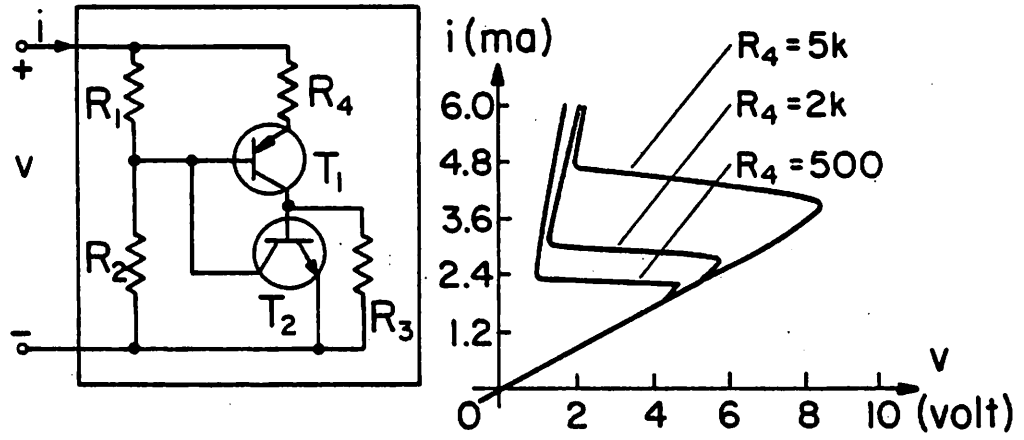
(E)


i
+
V
−
R1
R2
T1
T2
R3
i(ma)
6.0
4.8
3.6
2.4
1.2
0
1.6
3.2
4.8
6.4
8.0
V
(volt)
R3 = 400
R3 = 1k
R3 = 5k

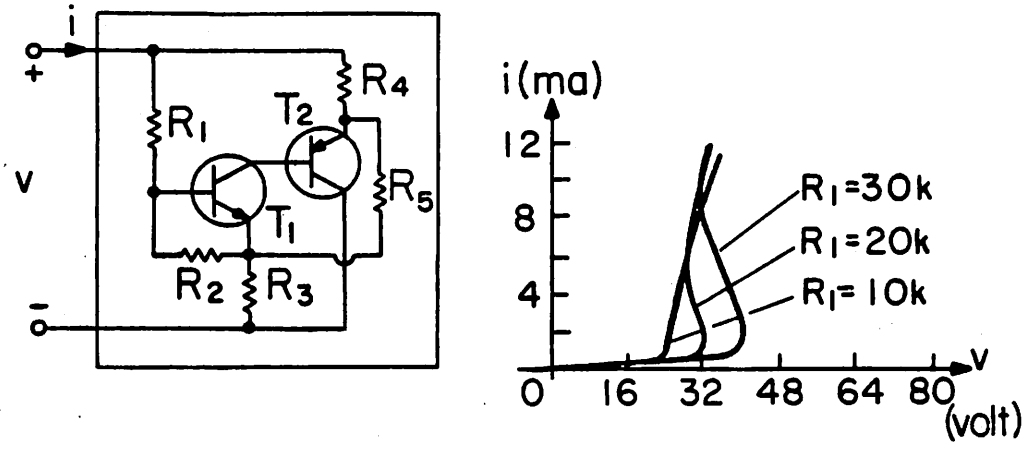
(F)


i
+
V
−
R1
T1
R2
T2
R3
i (ma)
3.0
2.4
1.8
1.2
0.6
0
3.0 6.0 9.0 12.0 15.0
V
(volt)
R2 = 20k
R2 = 100k
R2 = 200k

(G)

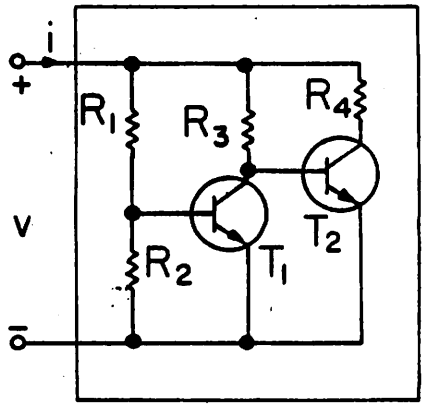

i
+
V
−
R1
R4
T1
R2
T2
R3
i (ma)
6.0
4.8
3.6
2.4
1.2
0
2 4 6 8 10 (volt)
V
R4 = 5k
R4 = 2k
R4 = 500

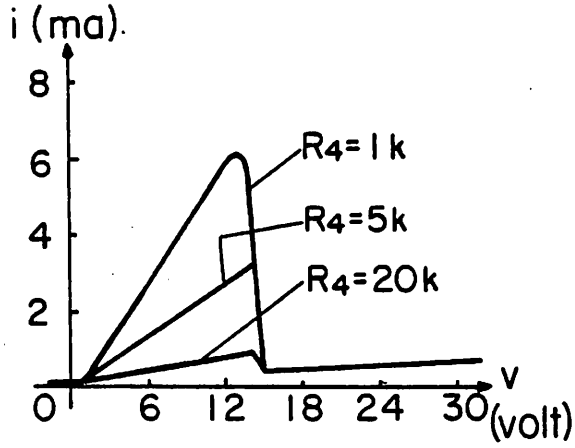
(H)


i
+
V
−
R1
T2
R4
T1
R5
R2
R3
i (ma)
12
8
4
0
16 32 48 64 80
(volt)
V
R1 = 30k
R1 = 20k
R1 = 10k

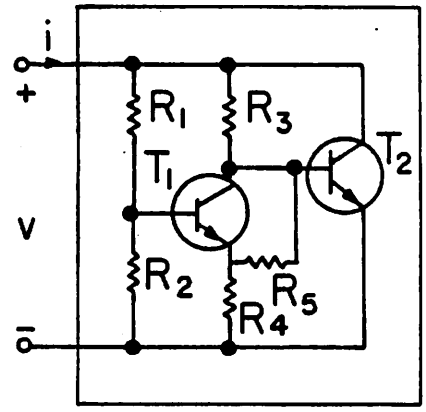
(I)

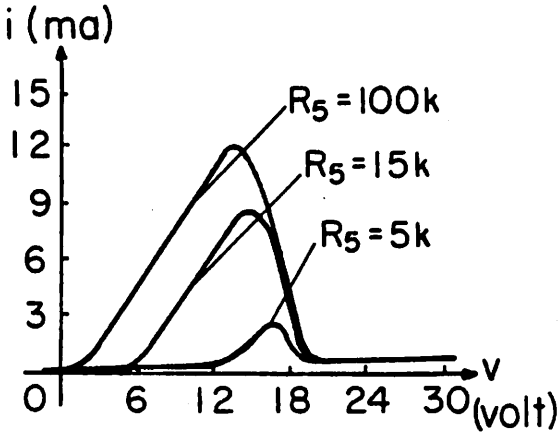
B.2: Type-N Devices



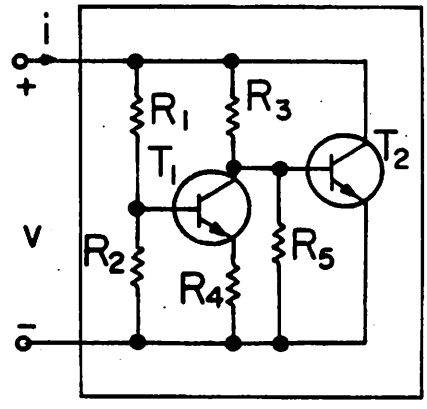


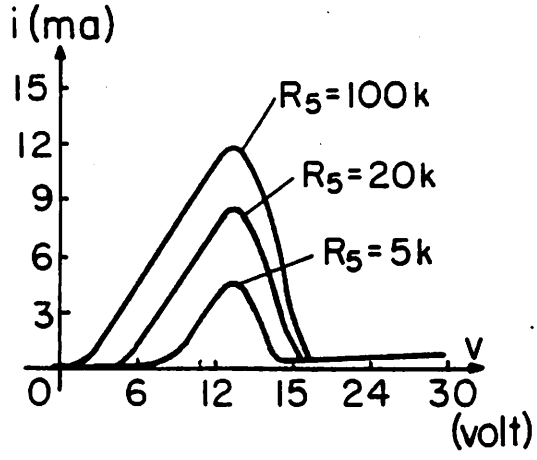
(A)



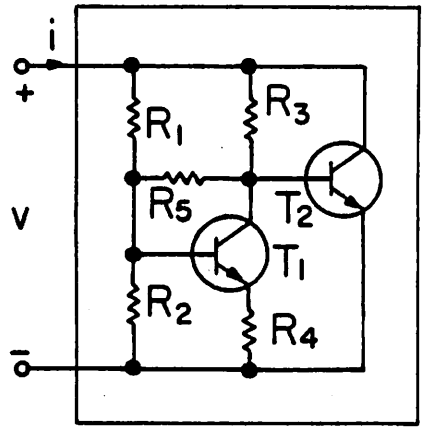


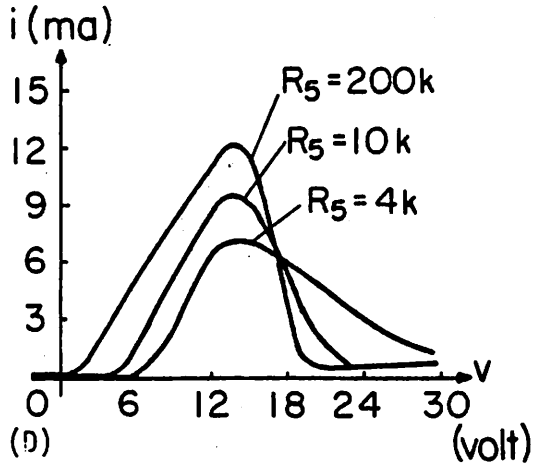
(B)



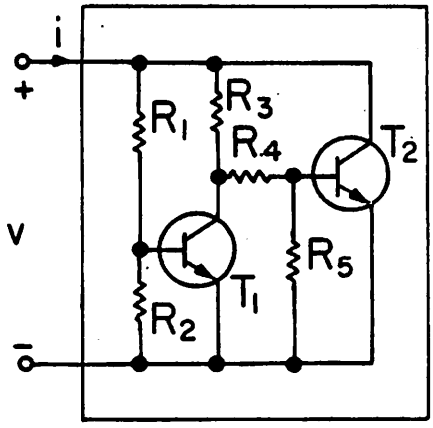


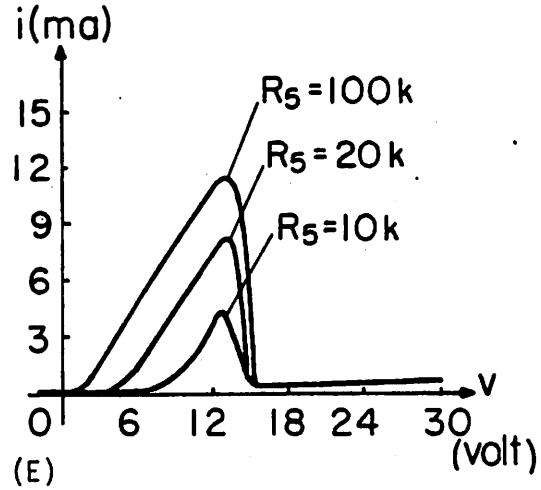
(C)


i
+
v
−
R1
R3
R5
T2
T1
R2
R4

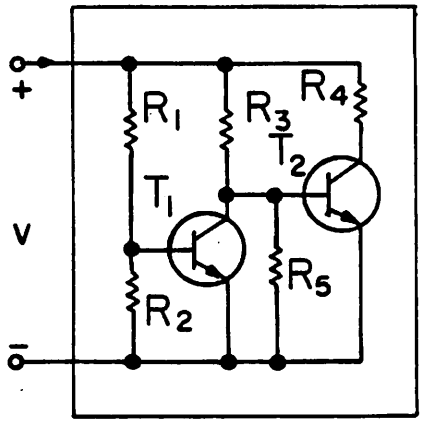

i (ma)
15
12
9
6
3
0
6
12
18
24
30
v
(volt)
R5 = 200k
R5 = 10k
R5 = 4k

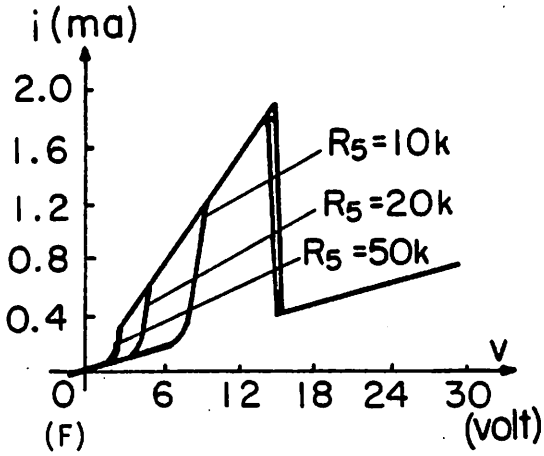
(D)


i
+
v
−
R1
R3
R4
T2
T1
R5
R2

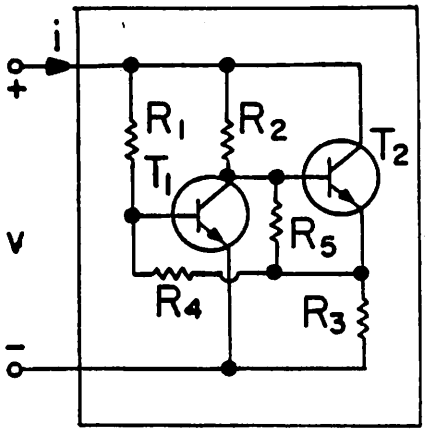

i(ma)
15
12
9
6
3
0
6
12
18
24
30
v
(volt)
R5 = 100k
R5 = 20k
R5 = 10k

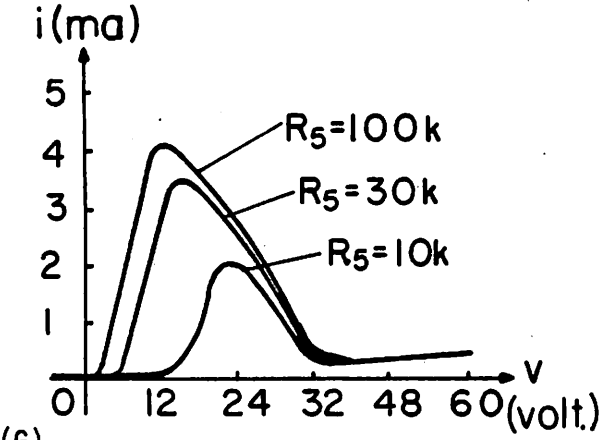
(E)


+
v
−
R1
R3
R4
T2
T1
R5
R2

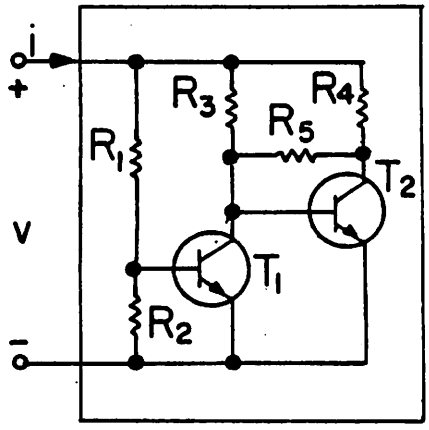

i (ma)
2.0
1.6
1.2
0.8
0.4
0
6
12
18
24
30
v
(volt)
R5 = 10k
R5 = 20k
R5 = 50k

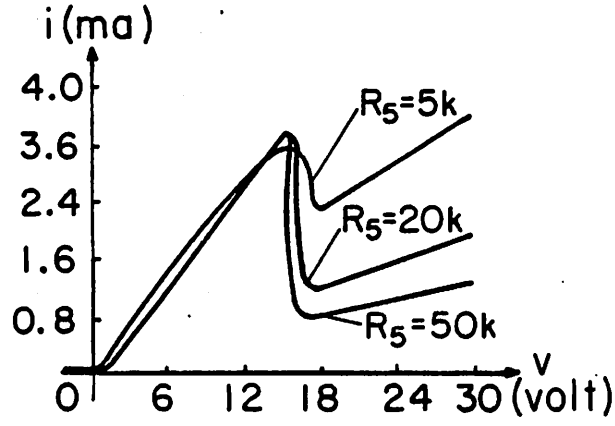
(F)


i
+
R1
R2
T2
T1
V
R5
R4
R3
−

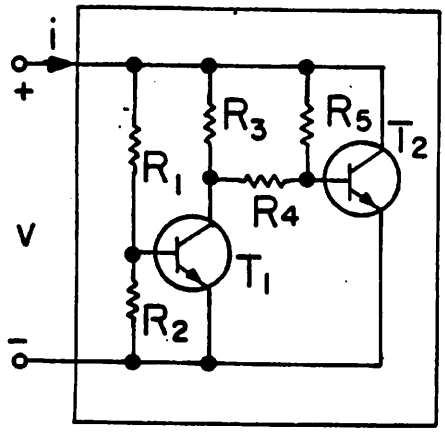

i(ma)
5
4
3
2
1
R5=100k
R5=30k
R5=10k
V
0
12
24
32
48
60
(volt.)

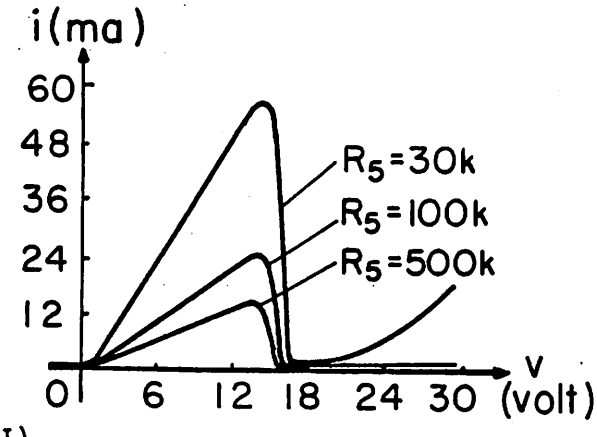
(G)


i
+
R3
R4
R5
R1
T2
V
T1
R2
−


i(ma)
4.0
3.6
2.4
1.6
0.8
R5=5k
R5=20k
R5=50k
V
0
6
12
18
24
30
(volt)

(H)


i
+
R3
R5
T2
R1
R4
V
T1
R2
−


i(ma)
60
48
36
24
12
R5=30k
R5=100k
R5=500k
V
0
6
12
18
24
30
(volt)

(I)