EVALUATION OF A FULLY-INTEGRATED HIGH-FREQUENCY SWITCHED-CAPACITOR BANDPASS FILTER

by

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Title

RESEARCH PROJECT

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Approval for the Report and Comprehensive Examination:

Committee: Professor Paul R. Gray, Research Advisor

Paul Gray 9/17/82 Date

Professor David A. Hodges

David A. Hodges 9/20/82 Date

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ABSTRACT

A fully-integrated high-frequency switched-capacitor bandpass filter is evaluated. The experimental circuit from which measurements are taken is a CMOS sixth-order 260 KHz elliptic bandpass filter with a Q of 40 and operating at a clock frequency of 4 MHz.

ACKNOWLEDGEMENT

I would like to thank Professor Paul Gray for giving me this opportunity to work with him, and for being so kind and supportive.

I also would like to express my appreciation to Ron Kaneshiro for all the help throughout the whole project.

Thanks also go to Tat Choi and the graduate students in the Integrated Circuits Group at the University of California, Berkeley, for their assistance and helpful advices.

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1. Introduction

The objective of this project is to evaluate a fully integrated switched-capacitor bandpass filter intended for AM IF filtering application which was designed and fabricated in cooperation with National Semiconductors.

A complete characterization of the test circuit, which consits of determining its frequency response versus variations in power supplies and operating clock frequency, and taking detailed measurements of noise, distortion, and power supply rejection, will be carried out.

An analysis of the data will be attempted whenever possible in order to account for the results obtained, either try to get agreement with theoretical estimations or explain any discrepancy.

A description of the filter along with some highlights in the design philosophy are first given.

2. Filter description

2.1. Design objectives

The designed filter is a sixth-order elliptic bandpass filter which will be used for AM intermediate frequency filtering in radio receivers for automobiles. The specifications dictate a center frequency of 260 KHz (within 1%), a minimum -3 dB bandwidth of 5 KHz, and a minimum stop-band rejection of 50 dB.

2.2. Design techniques

As a step toward fully integrated communication receivers, the filter has been implemented in CMOS. A detailed discussion of the design will be presented in the paper by RON KANESHIRO *et al.* Some of its most interesting features are summarized below which bear the explanation for most of the measurement results observed later.

The high sampling rate (4 MHz clock frequency) requires operational amplifiers with fast settling time and sufficient DC gain. They are of fully differential folded-cascode configuration [1]. The differential technique should also improve the filter's dynamic range (by effectively doubling the output voltage swing), and the rejection of common-mode signals such as power supply variations and clock feedthrough [2].

Identical resonators are used to alleviate the sensitivity problem common to high-Q bandpass filters, and at the same time to simplify the circuit layout. All L and C loops in the passive filter are replaced by their Thevenin equivalents before the implementation of the active filter in order to insure DC stability. Finally, large capacitor ratios are reduced by using capacitive T-networks, after some approximation has been made to convert coupling paths realized via sampling capacitors to feedforward capacitors feeding directly into the outputs of the integrators [1].

A schematic of the circuit is given in fig. 1, and component values are listed in Table I.

3. Experimental Setup

3.1. Biasing circuit

A pinout diagram of the 20-pin filter integrated circuit is shown in fig. 2 along with the biasing circuit.

Since the chip, which is intended for use in automobiles, operates from a single positive supply, a means must be provided to properly bias the internal circuitry to the mid-point voltage level when no input is present. This is done by tying pins 14 and 15 (Gm Out) and pins 16 and 17 (Gm In) together and connect them to pin 1 (V_{CM}).

V_A (pin 5: positive supply for the operational amplifiers) and V_D (pin 6: power supply for the digital clock generator) must track each other for proper operation of the chip and thus are connected to the same external source.

V_B (pin 4: the operational amplifiers' bias) runs off an independent source to allow flexibility in determining the optimal operating point as will become clear later.

The clock signal (a 4 MHz square wave from $\frac{-V_D}{2}$ to $\frac{+V_D}{2}$ is capacitively coupled to pin 7, and its DC bias is provided by the 10K-10K voltage divider so that the incoming clock signal is effectively from 0 to V_D. Two non-overlapping clock signals are generated internally.

The bandwidth select pin (pin 20) must be grounded for the selection of nominal bandwidth, but can be pulled high to change the internal capacitor ratios if the bandwith is to be doubled.

Differential inputs provided by the peripheral circuit are applied to pins 2 and 3, and the differential outputs (pins 18 and 19) are converted

to a single-ended output also by the peripheral circuit.

3.2. Peripheral circuits

A simple phase-splitter circuit shown in fig. 3a is used to provide two exactly out-of-phase signals from the single input signal, thus effectively multiplying the incoming signal by 2 before feeding it to the filter.

Two voltage followers and a summer are needed to look at the effective differential output, as shown in fig. 3b.

These peripheral circuits are realized using LF356 operational amplifiers (low-noise JFET input) and metal-film resistors in order to minimize their total noise contributions which turn out to be negligible compared to the filter's noise.

4. Experiments: procedures, results and analysis of data

The main piece of equipment used in determining the characteristics of the filter is the HP8556A/HP8552B spectrum analyzer which feeds a varying-frequency sinusoidal signal to the test circuit and receives and displays the corresponding varying-frequency output signal from the filter. An X-Y recorder (model HP7044A) is connected to the spectrum analyzer to provide hard copies of the screen display. Slightly better accuracy can be obtained with the automatic synthesizer (HP3330B) / network analyzer (HP3570A) combination.

In taking measurements, the signal loss and noise contributions due to the peripheral circuits must be taken into consideration. The signal loss is measured to be 1.4 dB which is subtracted from the total loss as shown on the plots for an accurate value of the filter's gain. The noise, as mentioned before, is negligible.

And finally, for the purpose of noise measurement, all external power supplies are replaced with batteries for cleaner power rails.

4.1. Frequency response versus power supplies

The chip is rated to operate at V_A (positive supply for the operational amplifiers) between 7V and 10V and V_B (amplifier bias) between 4V and 5V. The first set of experiments will help determine the optimal point of operation in terms of filter frequency response.

V_A and V_B are varied independently of each other. Since V_B directly controls the bias current of the amplifier which in turn determines the DC gain and the unity-gain bandwidth [1], it is varied in small steps from 3.8V to 5V; whereas V_A which has a more subtle influence on the bias current is varied in 1V steps from 8V to 10V.

The filter's frequency response is recorded for each set of values of V_A and V_B (figs. 4a through 4c), and the resulting variations of passband ripple, gain, bandwidth, center frequency, and corresponding Q are presented graphically in figs. 5a through 5e.

A decrease in V_B results in a larger passband ripple, a larger gain at the center frequency, a small change in the bandwidth and a downward shift of the center frequency. A similar trend is observed when V_A is decreased. Below a certain limit (V_A=8V and V_B=3.8V), the filter becomes unstable and oscillates. These results will now be explained.

For the folded-cascode amplifier configuration used in this design, it is shown that the amplifier DC gain is inversely proportional to the square-root of its bias current, while its unity-gain bandwidth is directly proportional to that quantity [1]. Thus decreasing V_B results in decreasing the bias current which in turn yields a larger amplifier gain and a smaller

unity-gain bandwidth. Decreasing V_A (the amplifier positive supply) will have essentially the same effect, only much milder.

A larger amplifier gain improves the accuracy of the overall response, but a smaller unity-gain bandwidth induces Q-enhancement of the filter's poles which implies a lower center frequency and increasing unstability due to excess phase in the switched-capacitor integrator (larger ripple, larger gain at the center frequency). As the bandwidth gets smaller while the sampling clock is maintained at the operating frequency of 4 MHz, the circuit eventually oscillates.

An increase in V_B (or V_A) shows the expected opposite effects, mainly a reduced passband ripple and a reduced filter gain. The first effect is due to the improved amplifier bandwidth which provides faster settling time and therefore better stability. The second one is caused by the smaller amplifier DC gain which makes the integrators appear lossy, thus introducing a droop in the frequency response [3].

Somewhere between the two extremes lies an optimal operating point where the ripple is small enough and the filter gain close to the designed value of 0.5. This optimal operating point is found at V_A=9V and V_B=4.25V. A complete characterization of the filter is carried out at that point for both cases of nominal and wide bandwidths (i.e. with pin 20 grounded and pulled high, respectively). The resulting plot of the frequency response is given in fig. 6a, and a detail of the passband in fig. 6b. The results are summarized in Table II.

A small unbalance can be noticed in the frequency response (uneven ripple and zeros). This can be accounted for by the approximation scheme in coupling signals from different resonators as mentioned earlier.

4.2. Frequency response versus clock frequency at optimal power supplies

The next experiment studies the variations in the frequency response as a function of the clock frequency. The power supplies are kept at their optimal values, namely V_A=9V and V_B=4.25V.

Going down in clock frequency would simply improve the stability of the filter as the integrators have more time to settle. This is manifested by a smaller ripple as can clearly be seen in fig. 7 and fig. 8a. Since the effective resistance of a switched capacitor C is given by $\frac{1}{Cf_c}$ where f_c is the clock frequency [4], cutting down the clock frequency will increase this effective resistance in the same ratio. This reduces the bandwidth of each integrator which results in a proportionally reduced bandwidth and center frequency of the filter. This effect can be observed in fig. 7 and is graphically represented in figs. 8c and 8d where a direct linear relationship between the filter's bandwidth (and center frequency) and the operating clock frequency is detected. The Q of the filter remains practically constant, around 40 as shown in fig. 8e.

Also noticed at lower clock frequencies is a decreasing filter gain which seems to stabilize itself after f_c has gone below 3 MHz (fig. 8b). At the same time the zeros tend to rise and disappear (fig. 7). These frequency-dependent effects may be accounted for by the fact that the summing amplifier in the filter circuit (fig. 1) which couples outputs from different resonators to generate the filter output is a high-pass circuit, due to its resistive feedback needed for DC stability.

The upper limit for the clock frequency is determined by the unity-gain bandwidth of the operational amplifiers. In our case, the filter still

functions above 4 MHz clock frequency though displaying growing ripple and a larger gain due to peaking, before entering oscillation at f_c of approximately 4.5 MHz.

4.3. Noise measurement

As mentioned earlier, external power supplies are replaced by batteries for cleaner power lines to the test circuit. As it turns out, not much improvement can be observed. Noise coming from the front-end (phase splitter) and back-end (differential-to-single-ended output) circuits is so small it can not even be measured. Thus any noise recorded would come totally from the filter chip.

Fig. 9a shows the noise level at the nominal operating point (V_A=9V and V_B=4.25V). The in-band noise density is computed by:

$$In\text{-}band\ noise\ density = \frac{Average\ of\ recorded\ in\text{-}band\ noise\ level}{\sqrt{Measurement\ bandwidth}}$$

From fig. 9a, the in-band noise density is measured to be 6.9 $\mu V_{rms}/\sqrt{Hz}$. For a ripple bandwidth of 5.8 KHz, this corresponds to a total in-band noise of 517 μV_{rms}.

Fig. 9b presents the noise level at the most stable operating point (V_A=10V and V_B=5V). The corresponding in-band noise density is 5.5 $\mu V_{rms}/\sqrt{Hz}$. This is in line with previous results, as the reduction in the in-band noise density is probably due to the reduction in the filter gain at this operating point.

Figs. 10a and 10b show the noise level at lower clock frequencies. These recorded variations in the noise level are plotted in fig. 11 and indicate a steady increase in the in-band noise density with decreasing clock

frequency. In the case where V_A=10V and V_B=5V, the noise density increases by a factor of about $\sqrt{2}$ for a reduction by half of the clock frequency. We will now try to find a theoretical explanation for this.

At high frequencies, the dominant noise sources in a switched-capacitor filter consist of the wideband noise contributed by the MOS operational amplifiers and the thermal noise from the channel resistance of the MOS switches (also referred to as the $\frac{kT}{C}$ noise). It has been shown that for a switched-capacitor integrator with sampling capacitor C_S and integrating capacitor C_I where $\frac{C_S}{C_I}$ is much smaller than 1, the equivalent input $\frac{kT}{C}$ noise power spectral density is $\frac{2kT}{C_S f_c}$ over the range of both positive and negative frequencies far below the clock rate [2]. Here k is the Boltzmann's constant, T is the absolute temperature and f_c is the clock frequency. Since the equivalent resistance R_{eq} of the switched capacitor is $\frac{1}{C_S f_c}$, the equivalent input $\frac{kT}{C}$ noise power spectral density can also be written as $2kTR_{eq}$ which turns out to be the thermal noise power spectral density of a resistor used in a continuous-time RC integrator. For a ratio $\frac{C_S}{C_I}$ not negligible compared to 1, the result will be less than $2kTR_{eq}$ [2].

As R_{eq} is inversely proportional to the clock frequency f_c, decreasing f_c would increase R_{eq} - and thus the noise power spectral density - by the same ratio. The corresponding noise voltage spectral density would be increased by the square-root of this ratio. Since for the case where V_A=10V and V_B=5V the results seem to bear out this theoretical estimation, we are led to believe that the operational amplifier wideband noise is negligible compared to the $\frac{kT}{C}$ noise in this case.

As a final check, we replace all the switched capacitors in the circuit in fig. 1 by their equivalent resistances and run a noise analysis using SPICE. The computer printout is included in the appendix. In our case, the operating frequencies are around 260 KHz - approximately $\frac{1}{15}$ of the clock frequency (4 MHz) - and the ratio $\frac{C_S}{C_I}$ is equal to $\frac{0.56}{1.38}$ or 0.4. Since this ratio is not a whole lot smaller than unity, we expect the actual value for noise to be smaller than the simulated result as discussed above.

The in-band noise density is simulated to be 6.6 $\mu V_{rms}/\sqrt{Hz}$. The simulation is carried out using a single-input path rather than a fully differential path, which means the simulated result for the actual fully differential circuit is $\sqrt{2}$ times the listed result since the total number of components is doubled and so is the noise power spectral density.

The computer-simulated value for the output in-band noise voltage density is therefore 9.3 $\mu V_{rms}/\sqrt{Hz}$, and is indeed larger than the actual measured value (6.9 $\mu V_{rms}/\sqrt{Hz}$) as expected.

4.4. Distortion and dynamic range

Fig. 12 shows the relationship betwwen the input and the output of the filter. At low input level, this relationship is a linear function with a gain of 0.5 (or -6 dB). As the input grows larger, the gain becomes smaller after the input has reached a certain level, indicating distortion in the output. This input level is in the neighborhood of 2.7 V_{pp} (peak to peak).

In order to measure distortion more accurately, we resort to the intermodulation technique. Two equal-amplitude signals whose different frequencies fall within the passband are applied simultaneously to the input of the filter, and the frequency spectrum of the output is recorded

and analyzed. Fig. 13a shows a plot of that spectrum at optimal operating point. The total IM harmonic distortion in the output is given by:

$$THD = \frac{\sqrt{\sum V^2_{Harmonics}}}{\sqrt{\sum V^2_{Fundamentals}}}$$

The input level corresponding to a fixed maximum THD - 1% as in most cases - is to be found by trial-and-error, and determines the upper limit of the dynamic range of the filter. Fig. 13a shows that for an input level of 3 V_{pp} (or 1.06 V_{rms}) the harmonics are at -43.8 dB (representing a factor of 0.00604) and -40 dB (factor of 0.01) relative to the fundamentals. The corresponding THD is:

$$\frac{\sqrt{(0.00604)^2 + (0.01)^2}}{\sqrt{2}} = 0.83\%$$

The total in-band noise voltage in this case has been computed to be 517 μV_{rms}. The dynamic range at optimal operating point for a THD of 0.83% is therefore:

$$Dynamic\ range = \frac{Maximum\ input}{Minimum\ input} = \frac{1.06}{517 \times 10^{-6}} = 2050\ or\ 66.2\ dB$$

The clock frequency is then cut down to half its nominal value, i.e. 2 MHz. This should improve the dynamic range of the filter as the operational amplifiers have more time to settle and become more stable.

Fig. 13b shows the corresponding frequency spectrum of the output for an input level of 4 V_{pp} (or 1.414 V_{rms}). The THD is computed to be 0.72%. At V_A=9V, V_B=4.25V and f_c=2 MHz, the in-band noise density is 7.27 $\mu V_{rms}/\sqrt{Hz}$ (fig. 11), the bandwidth is 3.2 KHz (fig. 8c), thus yielding a total in-band noise of 411 μV_{rms}.

In this case, the dynamic range for a THD of 0.72% is equal to:

$$\frac{1.414}{411x10^{-6}} = 3441 \text{ or } 70.7 \text{ dB}$$

There is indeed an improvement of 4.5 dB in the dynamic range of the filter as the clock frequency is reduced to half its nominal value.

4.5. Power supply rejection

With no AC signals present in the circuit and zero differential input, a DC differential output of 25 mV is recorded. This indicates possible mismatch problems in the circuit which could affect the next set of measurements.

A P-well CMOS technology was used to implement the filter. The N-type body is tied to the most positive voltage potential, namely V_A, so that any noise detected in V_A will be coupled through parasitic capacitances to the input paths of the integrators. Since a fully differential configuration is used, these parasitic signals will be canceled out if the input paths are perfectly balanced. If they are not, a residual differential output will result.

In order to measure how balanced the circuit actually is, an AC common-mode signal is directly applied to the input pins of the filter, bypassing the front-end circuit. In the ideal case, we expect a null differential output. In reality, a non-zero differential output is recorded, and fig. 14 shows a differential-to-common-mode gain of -20 dB (or 0.1). From this result we can suspect a pretty low power supply rejection.

A frequency-varying source is then capacitively coupled to V_A with zero differential voltage at the input, and the differential output

measured. The plot in fig. 15a indicates a power supply rejection of only 9dB.

In an attempt to correct for the unbalance in the circuit, the same signal is also capacitively coupled to V_B to induce variations in the common-mode levels, hoping to counteract and minimize the effect of the parasitic signals. This does in fact improve the power supply rejection to about 17 dB as shown in fig. 15b.

Finally, the same signal is injected to the input paths so that the power supply rejection thus measured is actually the power supply rejection of V_{SS}, the bottom-rail power supply which happens to be the ground line in this case. In fig. 15c it is measured to be approximately 9 dB.

The same experiments are repeated with the clock frequency at $\frac{1}{10}$ of its nominal value, i.e. 400 KHz. The results are plotted in figs. 16a and 16b. The power supply rejection is around 6 dB and - in contrast to the nominal case at f_c=4 MHz - remains more or less constant, indicating a frequency dependence of the parasitic coupling mechanism.

4.6. Sensitivity to process variations

It is shown that the frequency response of a high-Q bandpass filter is mainly sensitive to the center frequencies of the individual resonators in the circuit [1]. Therefore, the primary concern is to insure matching resonator center frequencies. This design uses identical resonators operating at the same center frequency, inter-connected by passive elements which determine the shape of the response about the center frequency. Since the resonator center frequencies are then determined by a same capacitor ratio, good accuracy of the filter center frequency can be easily achieved.

Figs. 17a and 17b show the frequency responses of five different units at the nominal clock frequency. They exhibit small variations in gain and ripple, but the center frequencies are all very close to 259 KHz (worst-case variation of 0.2%).

In the experiment which yields the data displayed in figs. 18a and 18b, the clock frequency is decreased by half to improve the stability of the circuits. The resulting frequency responses are even better, showing almost perfectly matched center frequencies.

5. Conclusion

In this project we have carried out a complete characterization of a high-frequency filter, and the results are summarized in Table III. The frequency response is well within the specifications. The noise level is somewhat high, but comes fairly close to the computer estimation, suggesting a possible reduction of the noise level by the use of larger capacitances which would also bring about an improvement in the time constant associated with the charge redistribution, but at the same time a larger clock feedthrough and therefore a degradation in the power supply rejection.

The chip also presents some aspects associated with high-frequency filters such as unstability at very high clock frequencies and sensitivity in the response of the circuit to non-ideal operating conditions (power supplies, non-ideal operational amplifiers etc.). The latter could be one explanation for the relatively low power supply rejection which has not until now been recorded for a high-frequency filter.

Finally, the collected data indicates - as expected - that the sensitivity of the frequency response to process variations is improved by using identical resonators in the circuit.

References

[1] Tat Choi, Ron T. Kaneshiro, Robert W. Brodersen, Paul R. Gray, "High Frequency CMOS Switched Capacitor Filters for Communications Applications", to be presented at the **ISSCC**, 1983

[2] Kuo-Chiang Hsieh "Noise Limitations in Switched-capacitor Filters" PhD Dissertation, University of California, Berkeley, May 1982

[3] David James Allstot "MOS Switched Capacitor Ladder Filters" PhD Dissertation, University of California, Berkeley, May 1979

[4] Robert W. Brodersen, Paul R. Gray, David A. Hodges, "MOS Switched-Capacitor Filters", **Proc. IEEE**, vol.67, pp.61-75, Jan. 1979

Figure Captions

1. 6th-order elliptic bandpass filter

2. Biasing circuit for the filter

3a. Front-end circuit: phase splitter

3b. Conversion from differential to single-ended output

4a. 4b. 4c. Frequency response vs. power supplies

5a. Ripple vs. power supplies

5b. Filter gain vs. power supplies

5c. Bandwidth vs. power supplies

5d. Center frequency vs. power supplies

5e. Filter's Q vs. power supplies

6a. Frequency response at optimal operating point

6b. Passband at optimal operating point

7. Frequency response vs. clock frequency

8a. Ripple vs. clock frequency

8b. Filter gain vs. clock frequency

8c. Bandwidth vs. clock frequency

8d. Center frequency vs. clock frequency

8e. Filter's Q vs. clock frequency

9a. Noise level at nominal operating point

9b. Noise level at another operating point

10a Noise level at nominal supplies and half clock frequency

10b Noise level vs. clock frequency

11. In-band noise density vs. clok frequency

12. Output level vs. input level

13a IM distortion at nominal operating point

13b IM distortion at half clock frequency

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15a Power supply rejection of V_A

15b Power supply rejection of V_A and V_B

15c Power supply rejection of V_{SS}

16a Power supply rejection of V_A at f_c=400 KHz

16b Power supply rejection of V_A and V_B at f_c=400 KHz

17a Frequency responses of 5 different units at nominal clock frequency

17b Passbands of 5 different units at nominal clock frequency

18a Frequency responses of 5 different units at half clock frequency

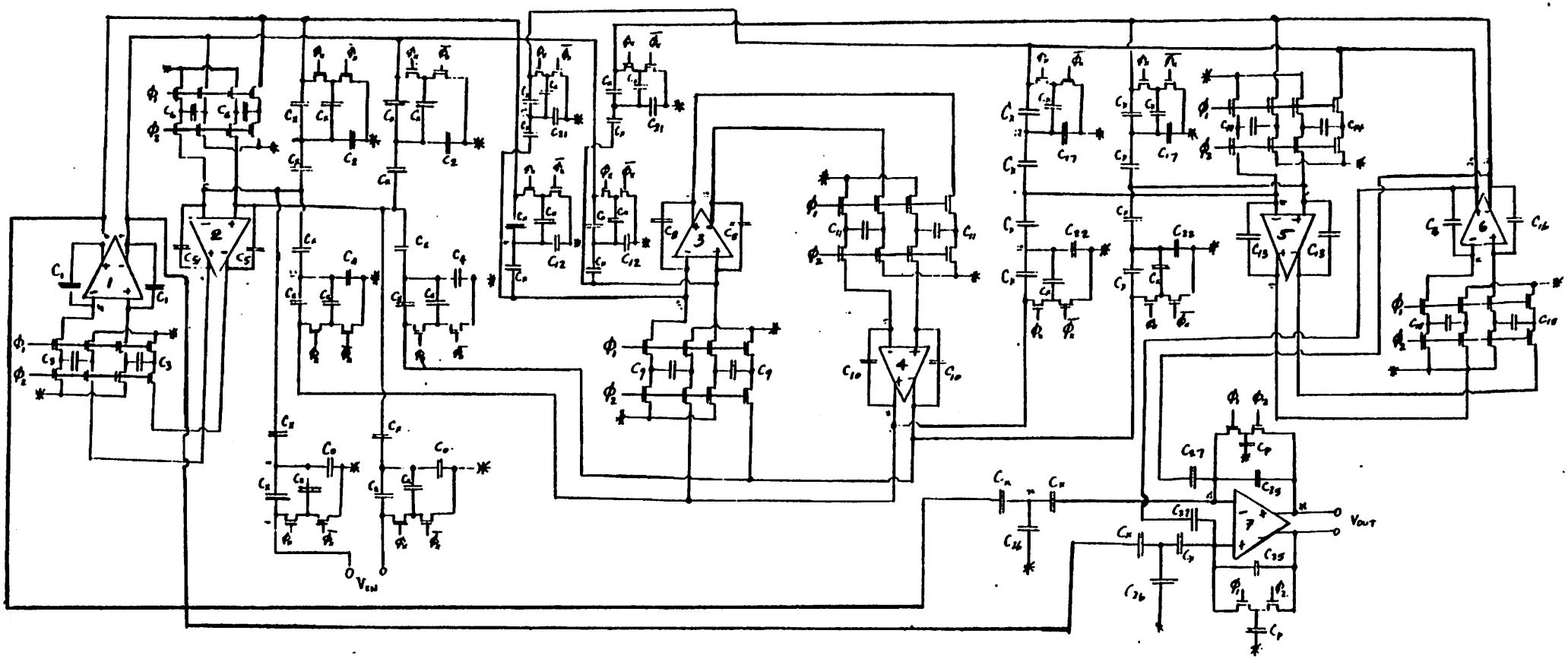
18b Passbands of 5 different units at half clock frequency

Table Captions

I. Component values

II. Characteristics of filter at nominal power supplies

III. Performance parameters of filter at nominal operating point



BANDWIDTH DOUBLED WITH ϕ_X ON

Fig. 1 6TH - ORDER ELLIPTIC BANDPASS FILTER

TABLE I

Component Values

CAPACITOR	VALUE (pF)
C_x	0.2
C_1, C_5, C_8, C_{10}, C_{13}, C_{16} C_2, C_4, C_{22}, C_{17}	1.38202737
C_3, C_6, C_9, C_{11}, C_{14}, C_{18}	0.56006799
C_{12}, C_{21}	0.75372972
C_{25}, C_{26}, C_{27}	1.54197825
C_0	1.45049940
C_p	Parasitic Capacitance

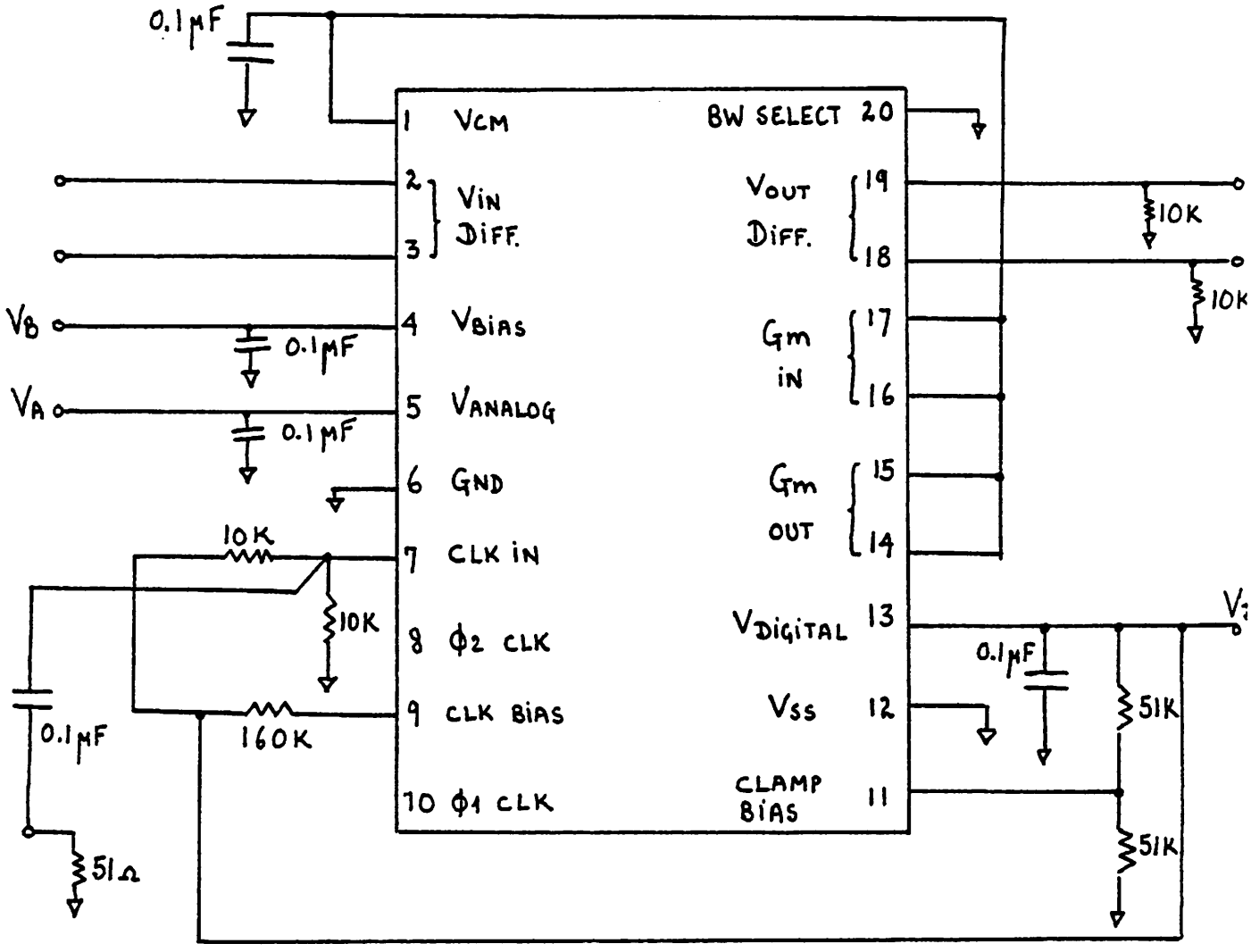


Fig. 2 BIASING CIRCUIT FOR THE FILTER

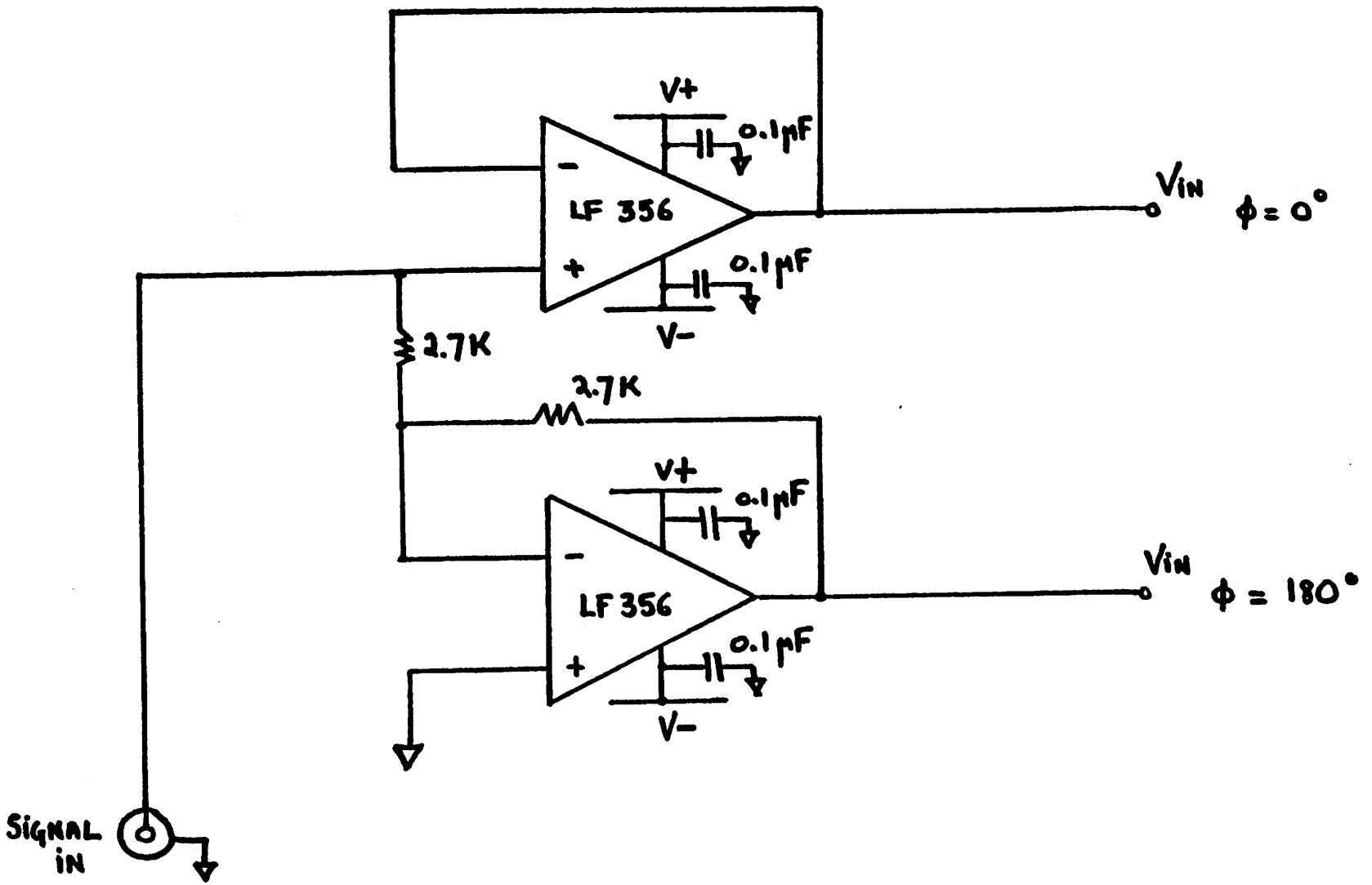


Fig. 3a FRONT-END CIRCUIT : PHASE SPLITTER

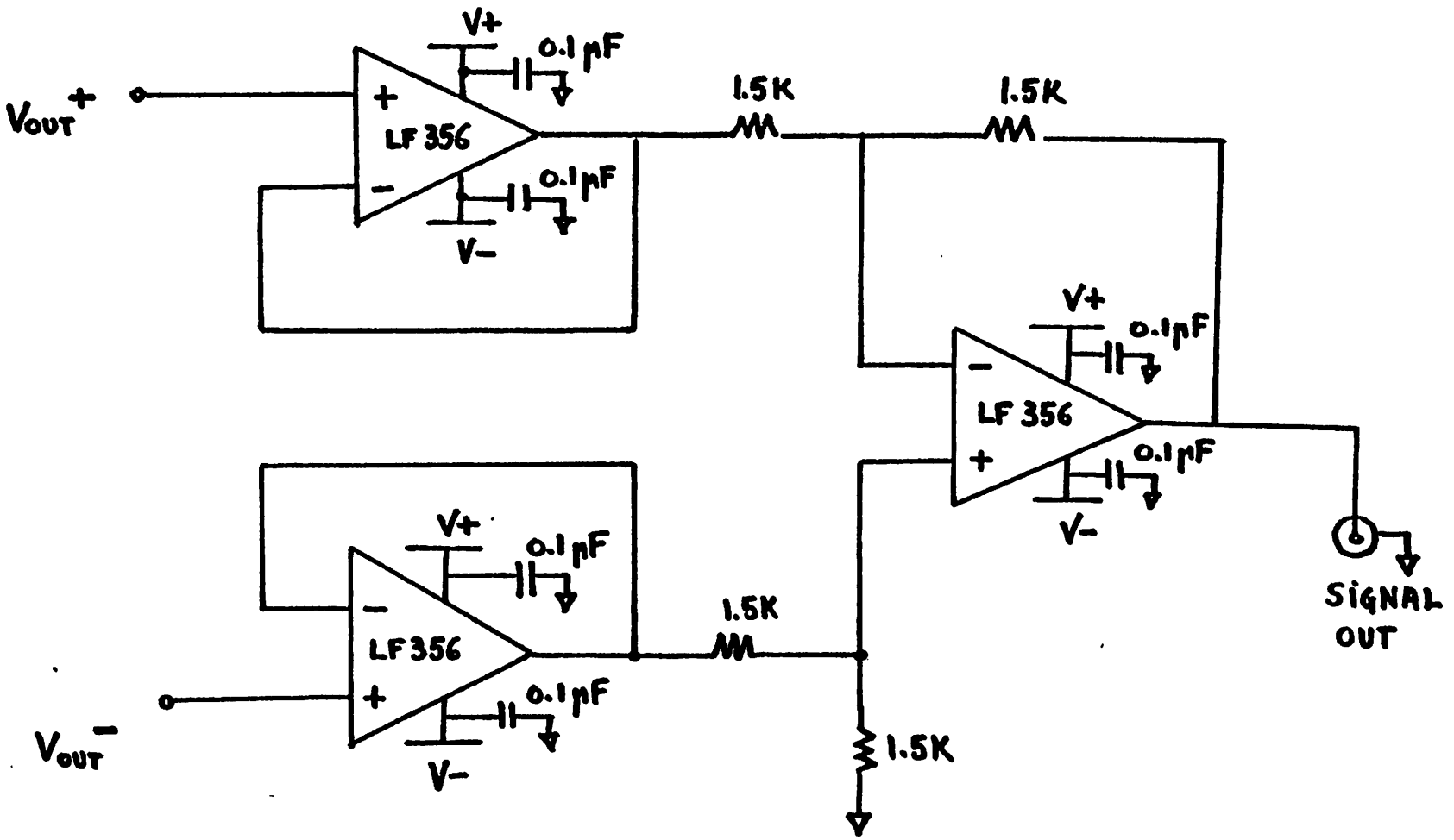


Fig. 3b CONVERSION FROM DIFFERENTIAL TO SINGLE-ENDED OUTPUT

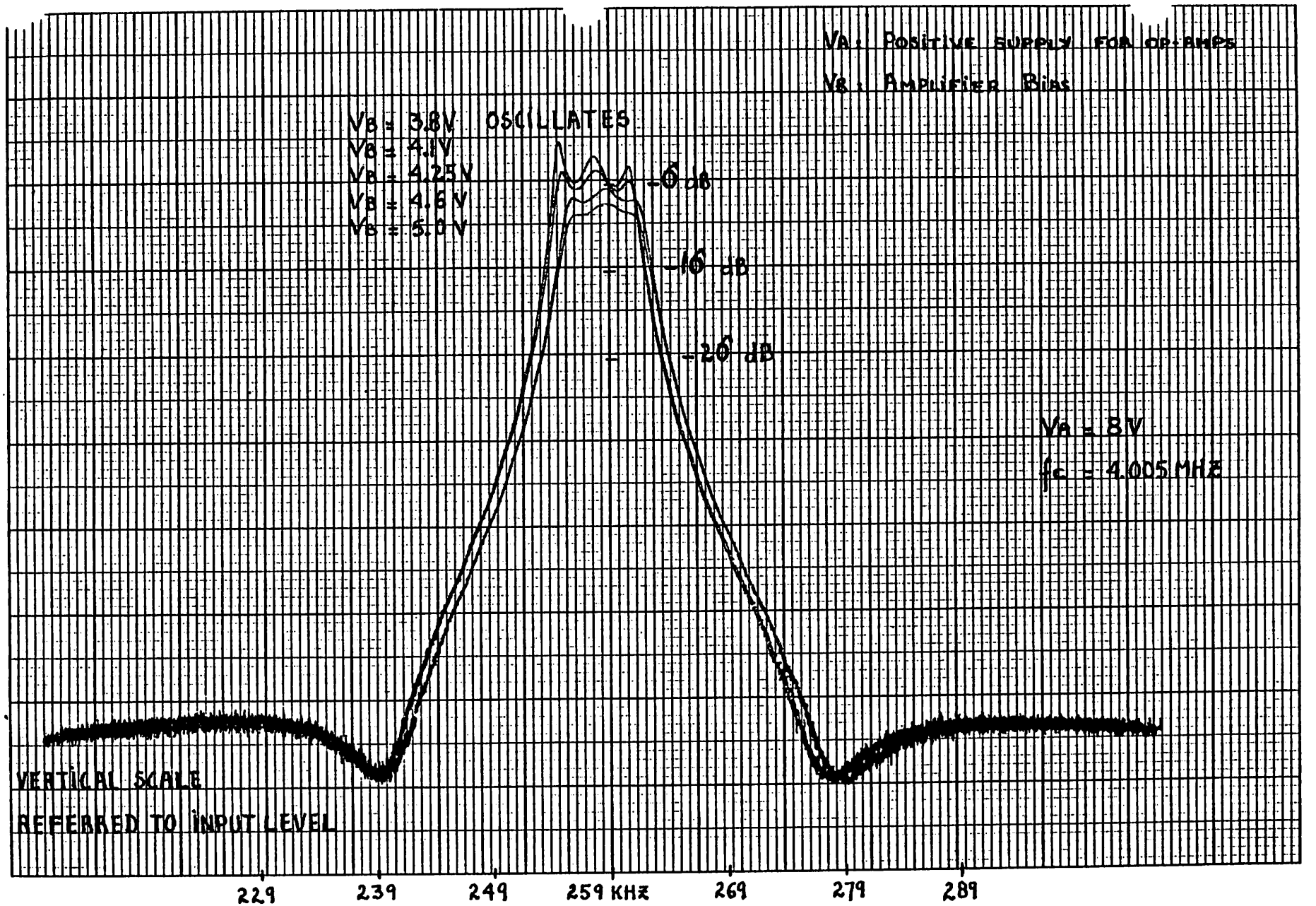


Fig. 4a FREQUENCY RESPONSE VS. SUPPLIES

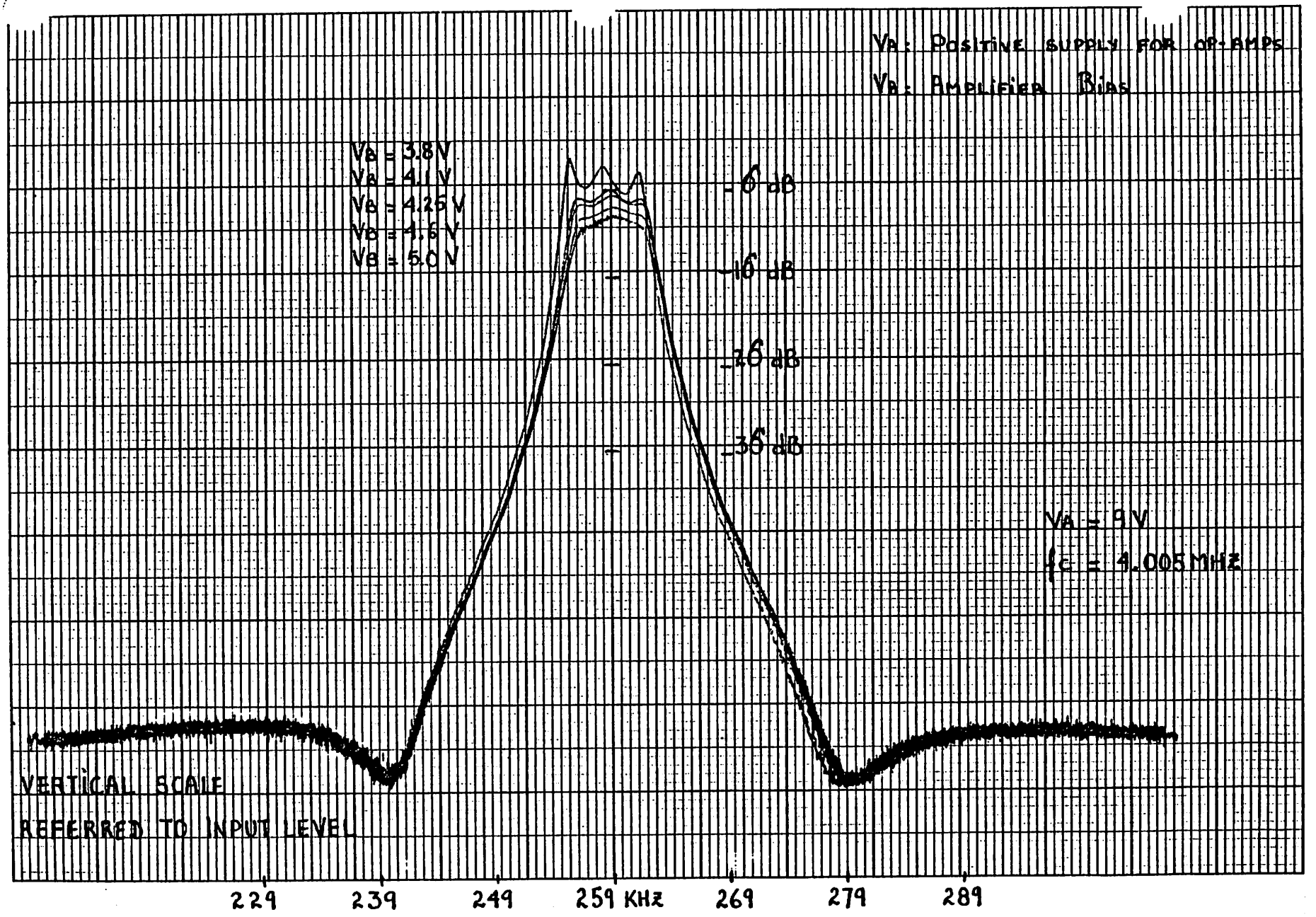


Fig. 4b FREQUENCY RESPONSE VS. SUPPLIES

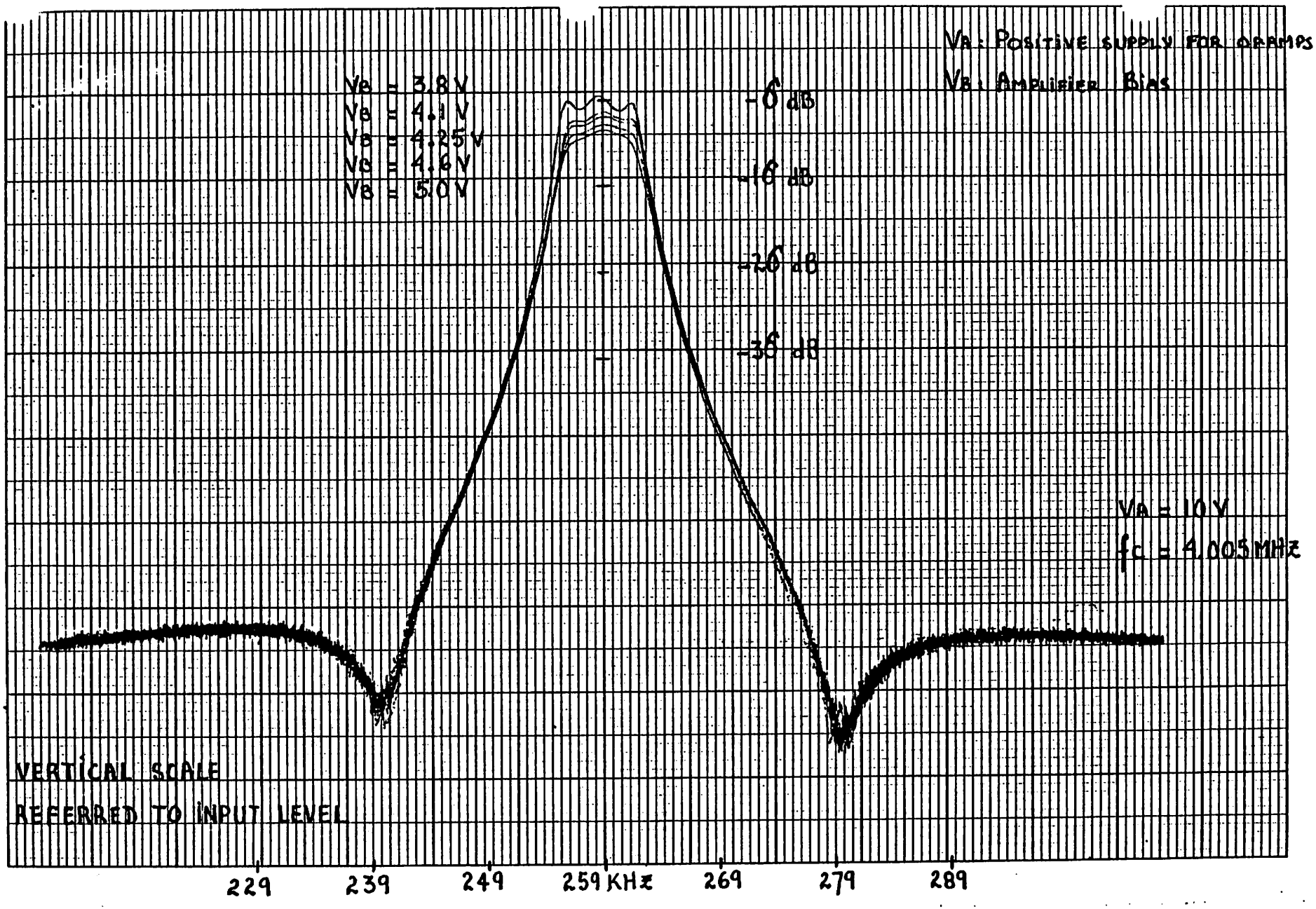


Fig. 4c FREQUENCY RESPONSE VS. SUPPLIES

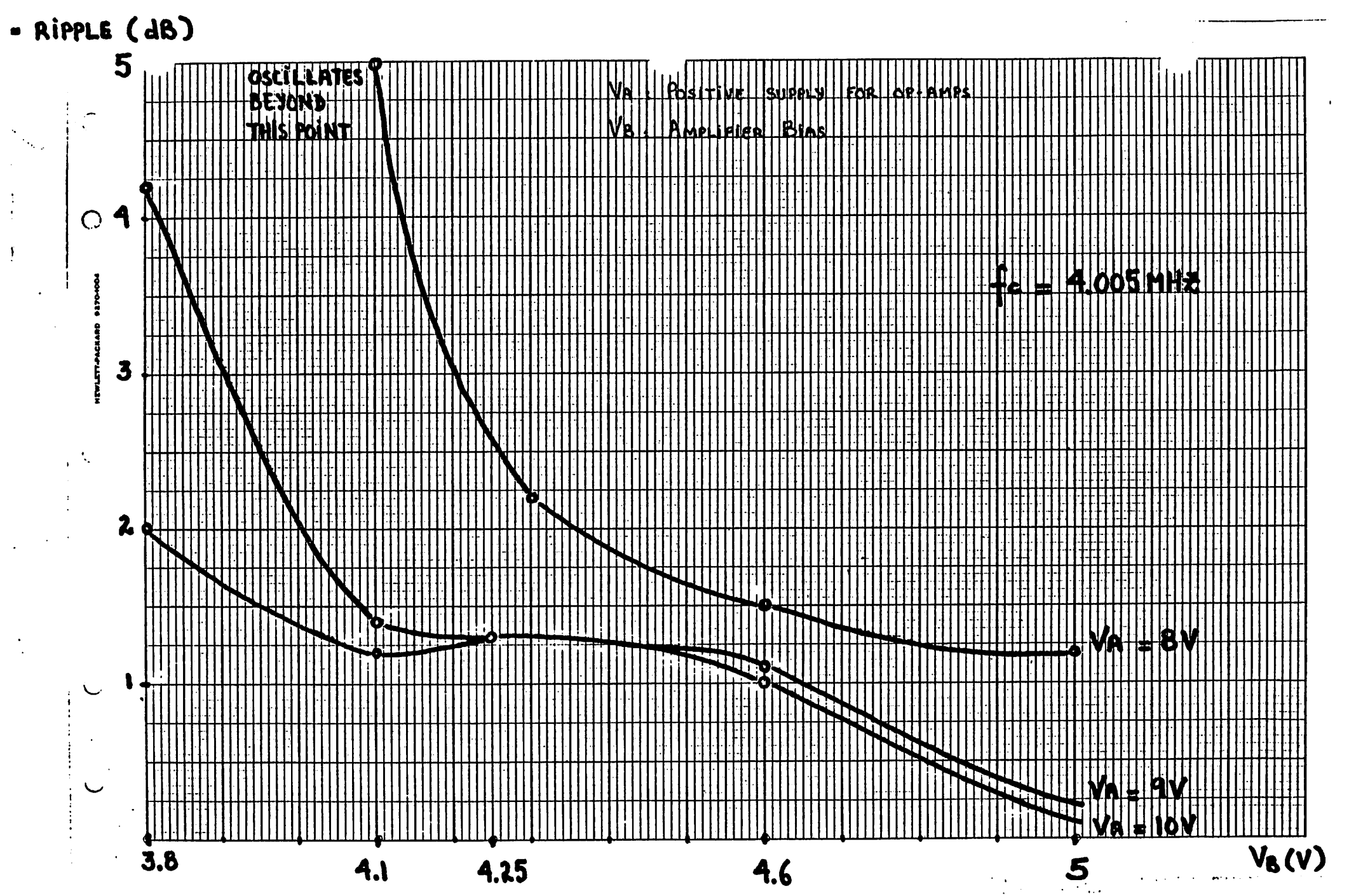


Fig. 5a RIPPLE VS. POWER SUPPLIES

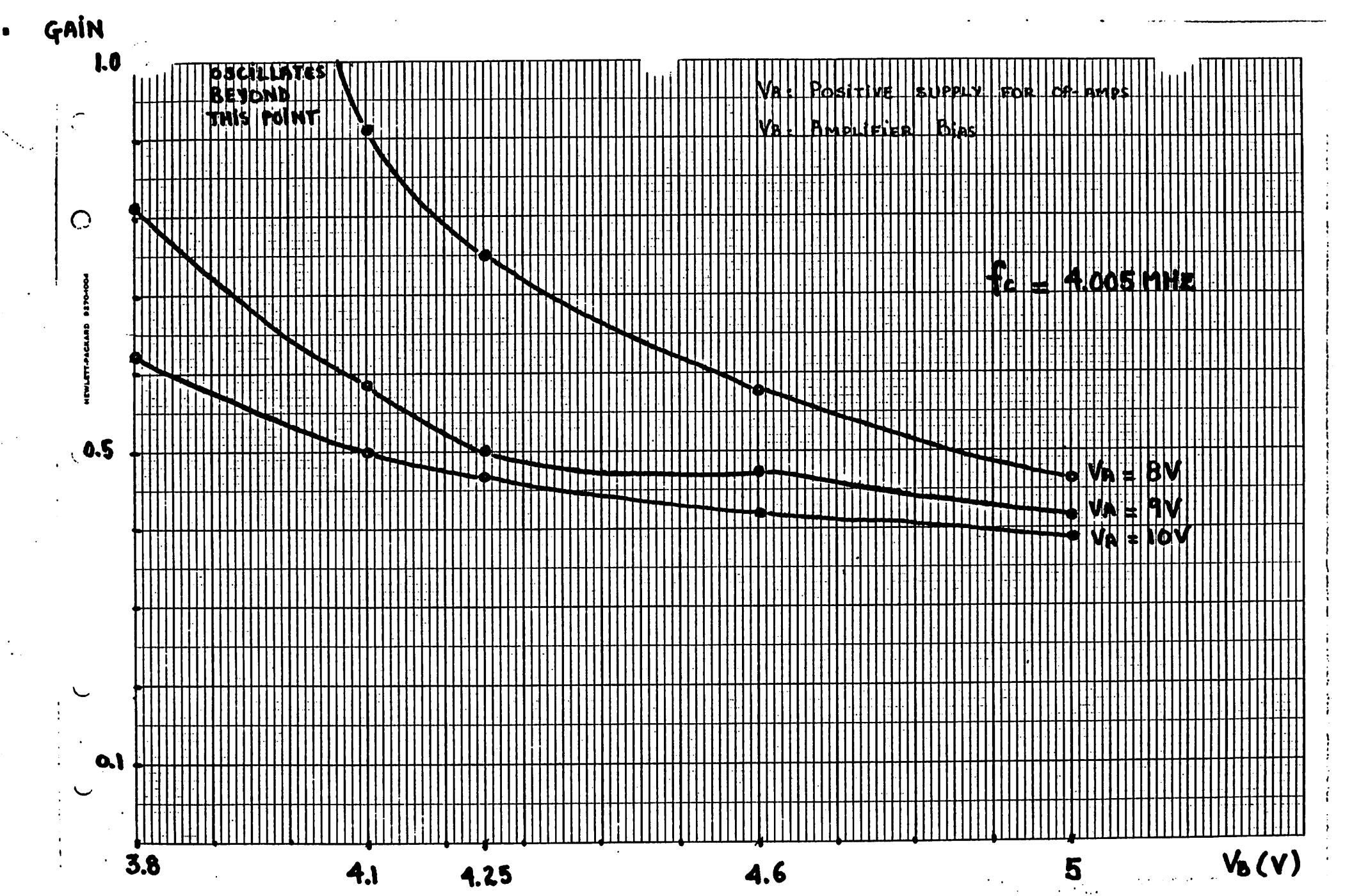


Fig. 5b FILTER GAIN VS. POWER SUPPLIES

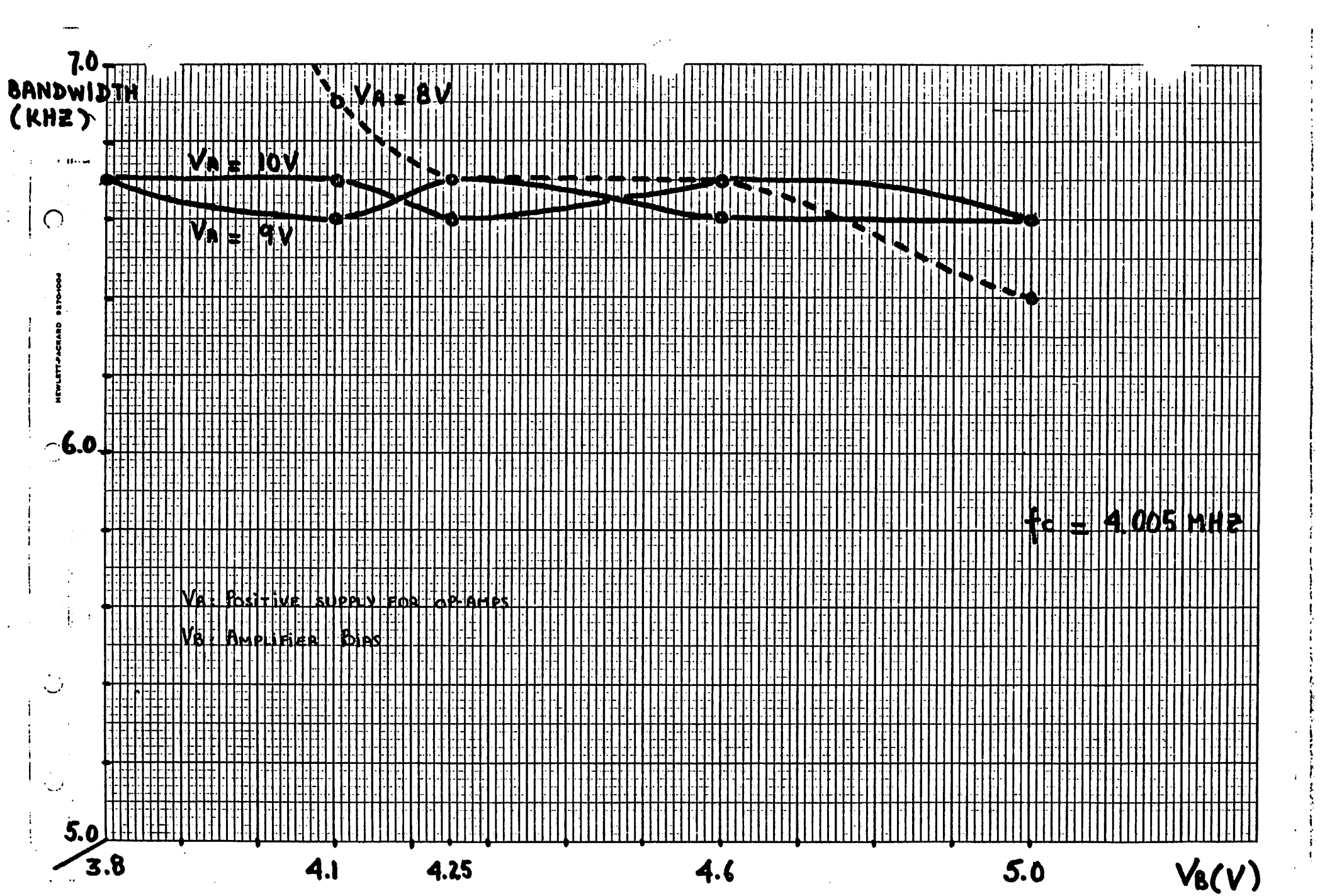


Fig. 5c BANDWIDTH VS. POWER SUPPLIES

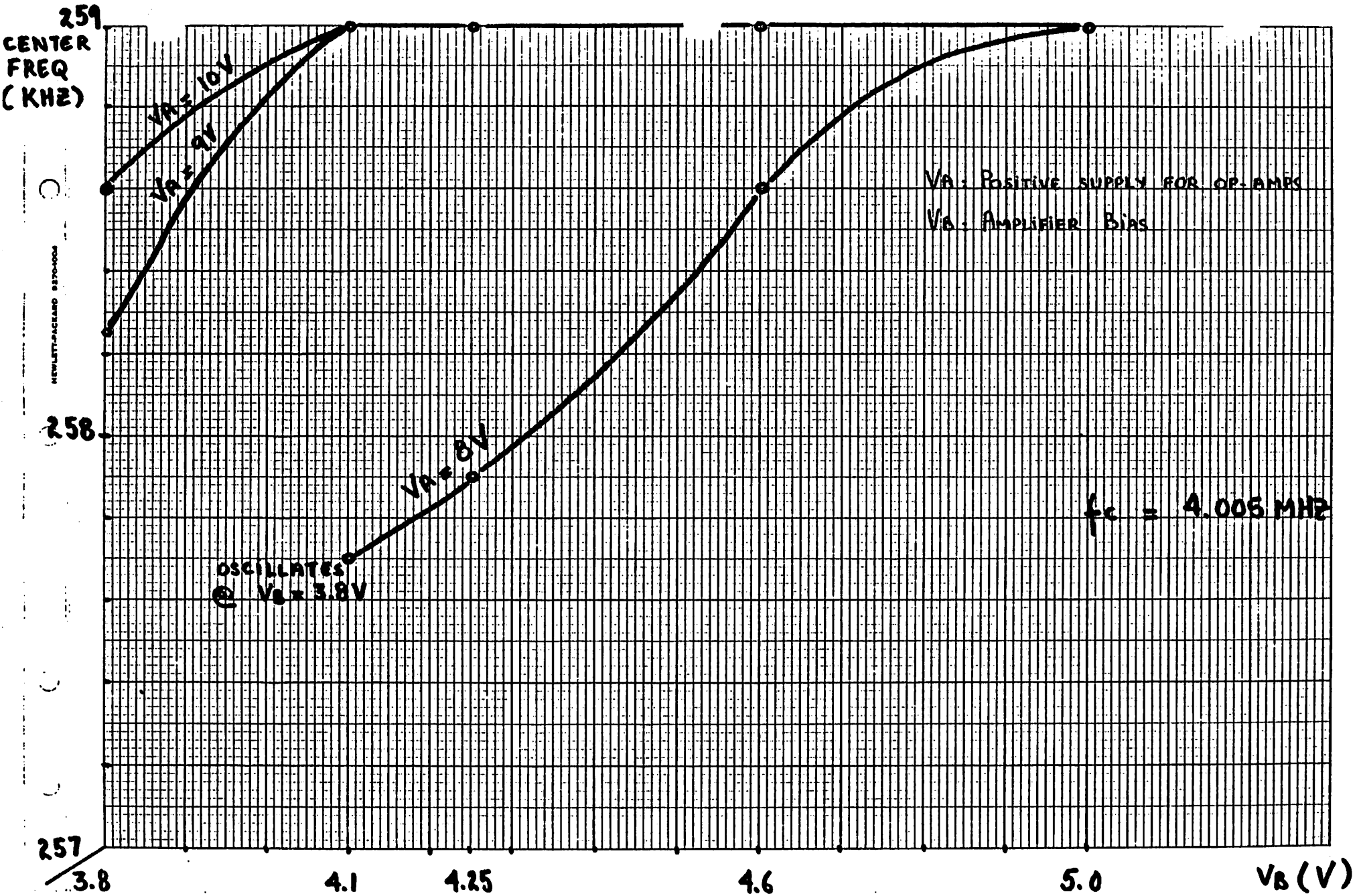


Fig. 5d CENTER FREQUENCY VS. POWER SUPPLIES

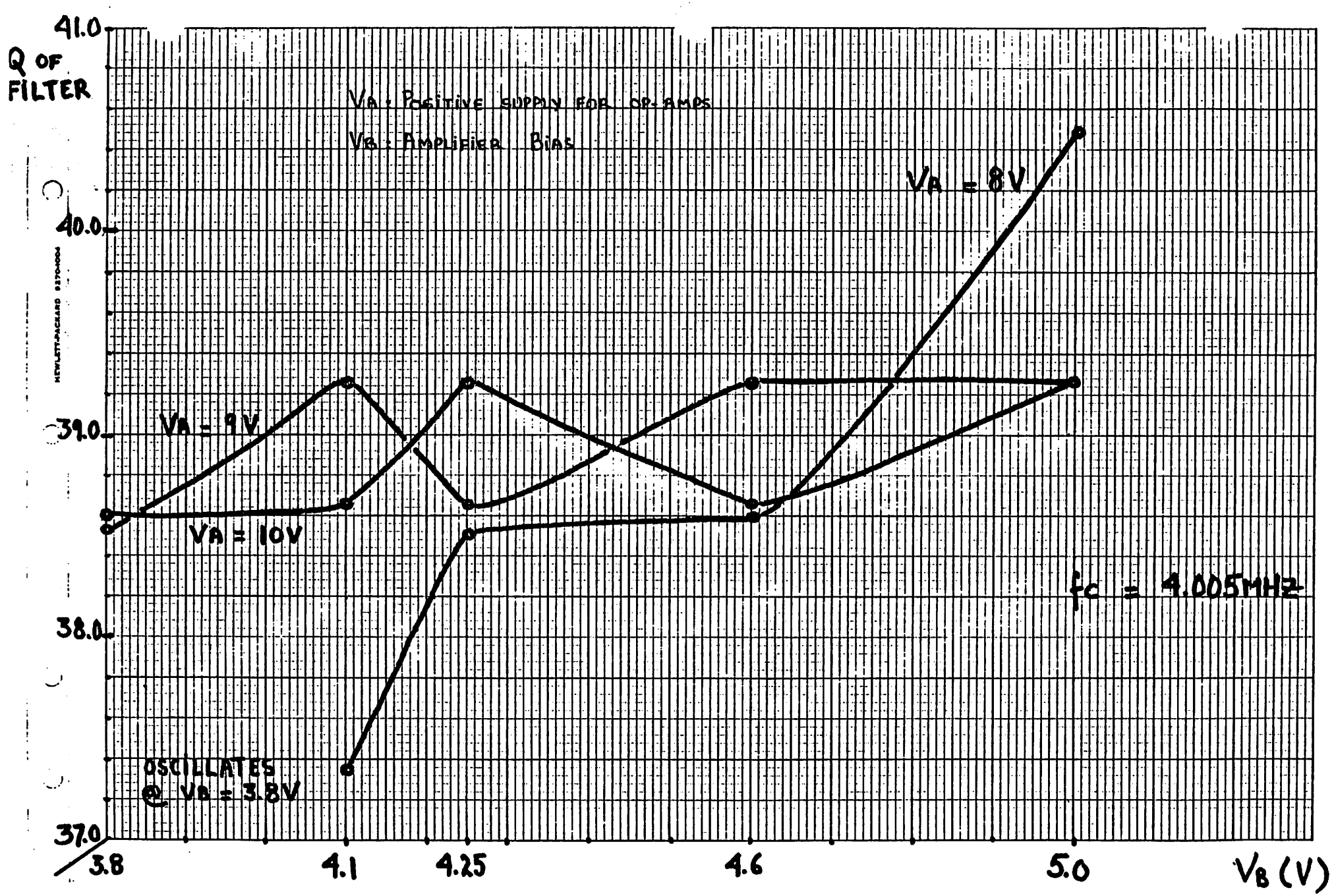


Fig. 5e FILTER's Q vs. POWER SUPPLIES

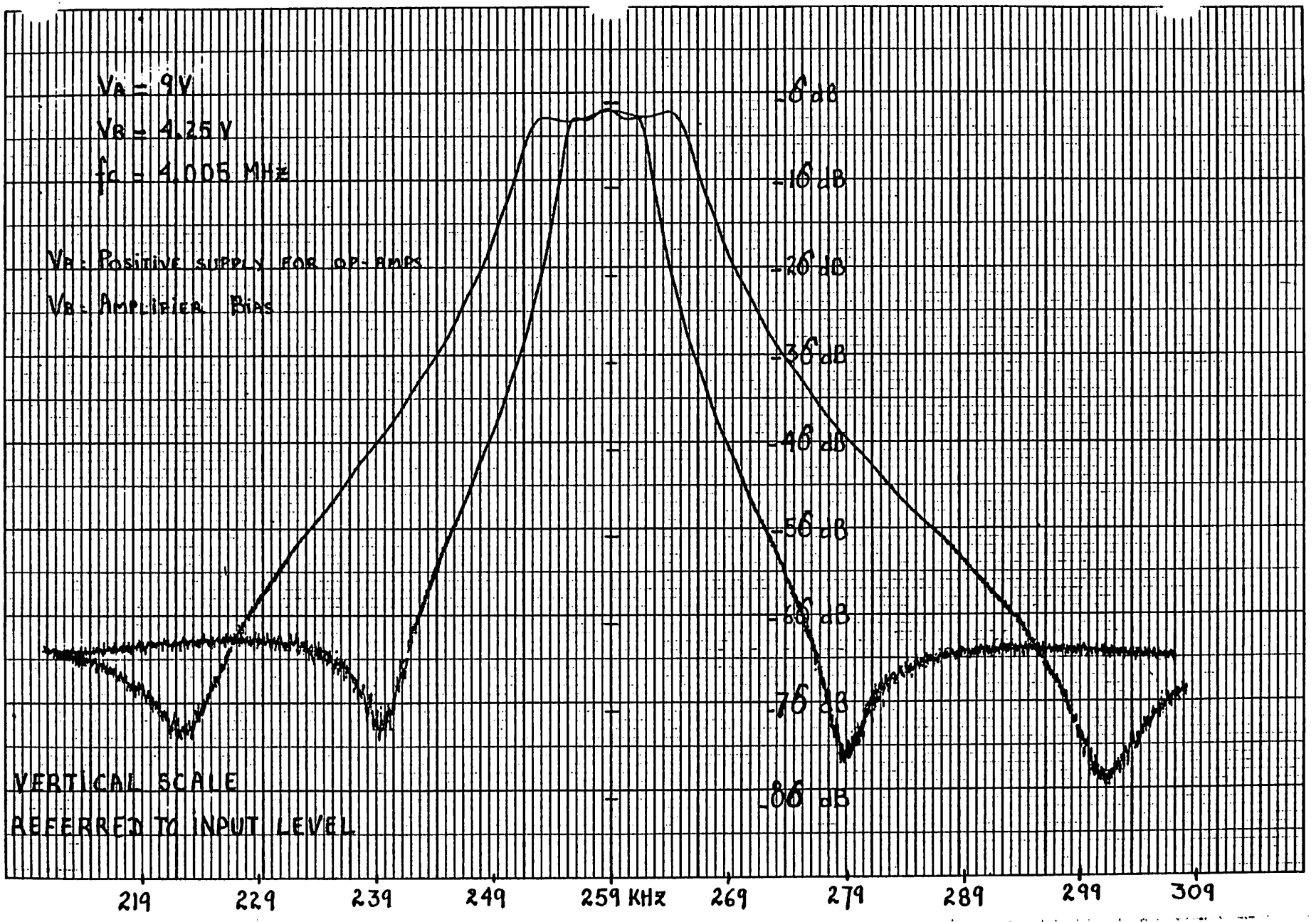


Fig. 6a FREQUENCY RESPONSE AT OPTIMAL OPERATING POINT (FOR BOTH CASES: LARGE AND SMALL BANDWIDTH)

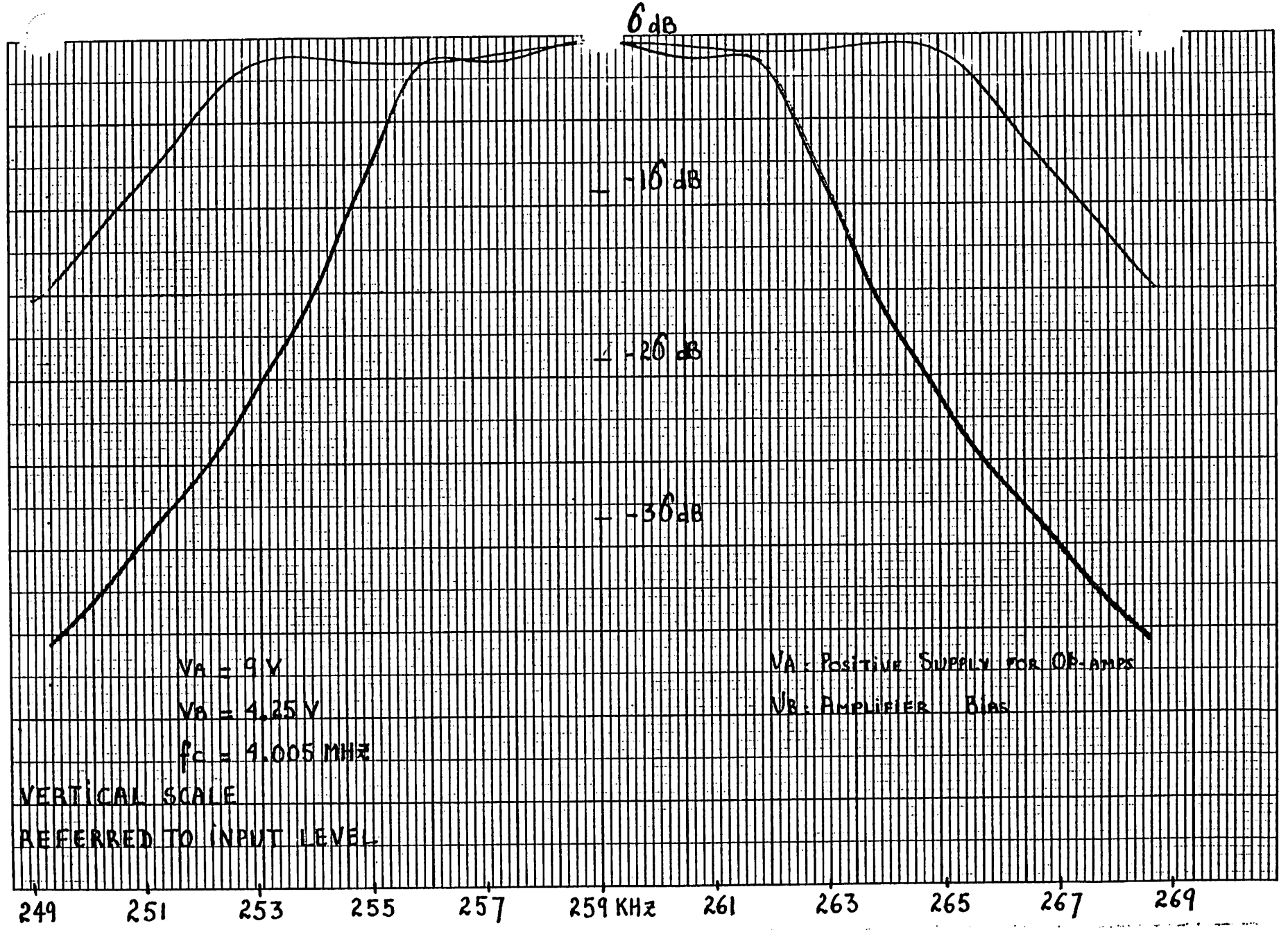


Fig. 6b PASSBAND AT OPTIMAL OPERATING POINT (FOR BOTH CASES: LARGE AND SMALL BANDWIDTH)

TABLE II

Characteristics of Filter at Nominal Power Supplies

	Nominal Bandwidth	Wide Bandwidth
Ripple	1.3 dB	1.1 dB
Ripple Bandwidth	5.8 KHz	12.2 KHz
-3 dB Bandwidth	6.5 KHz	13.3 KHz
+/-10 KHz Rejection	-38 dB	-38 dB
Zeros	+/-20 KHz -72 dB/-76 dB	+/-40 KHz -73 dB/-78 dB
Stopband Rejection	-61 dB	-61 dB

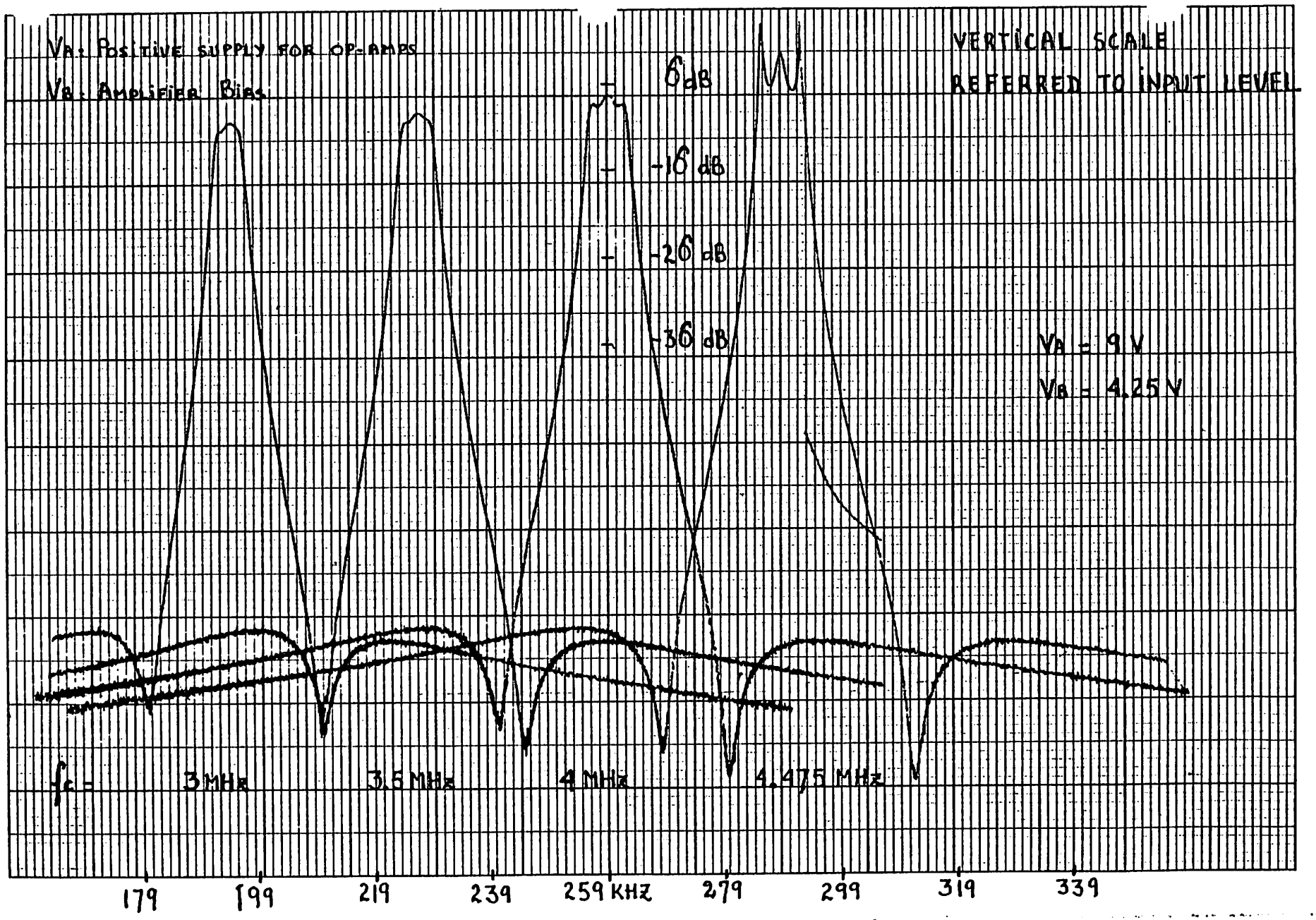


Fig. 7 FREQUENCY RESPONSE VS. CLOCK FREQUENCY

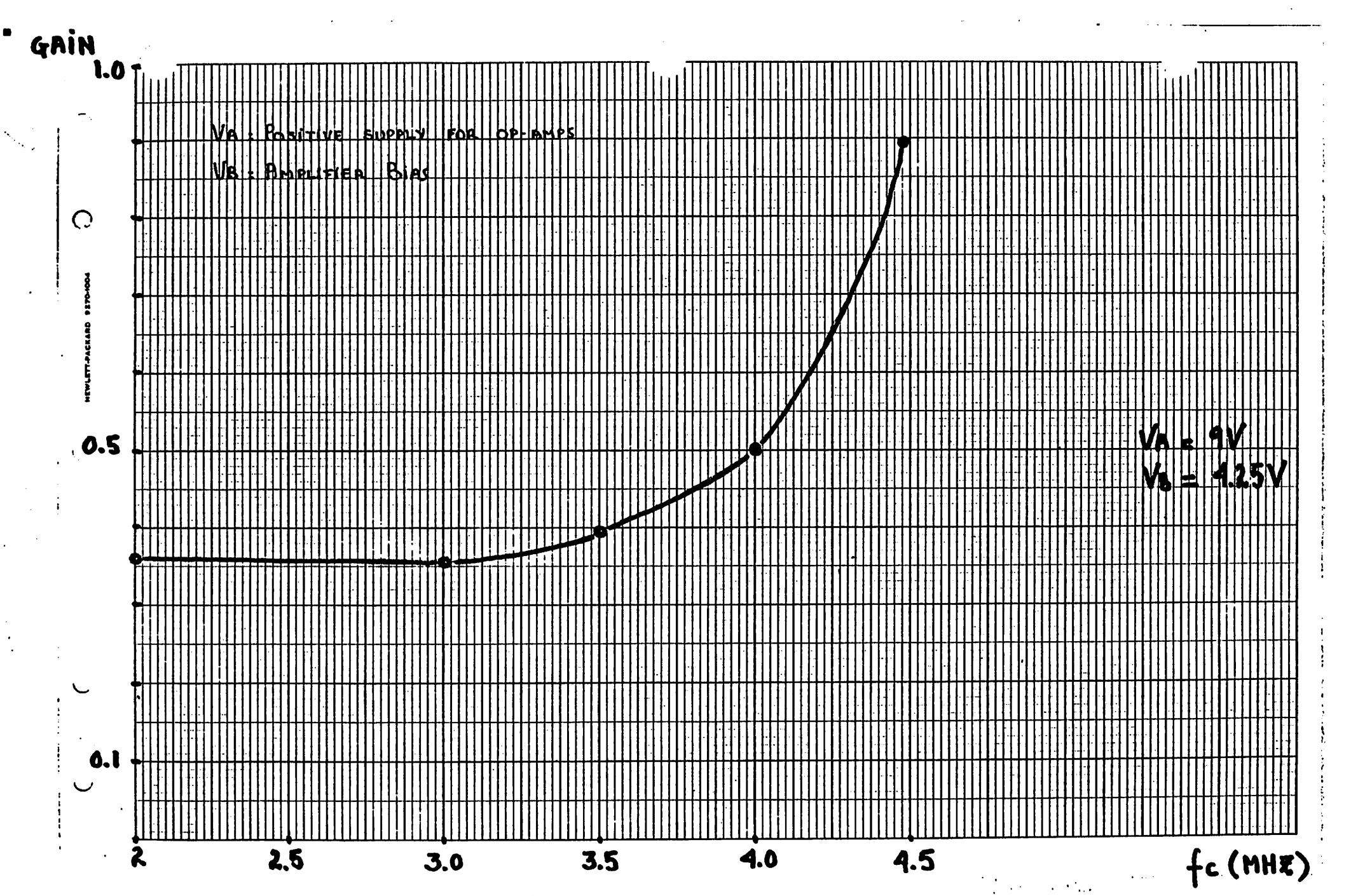


Fig. 8b FILTER GAIN VS. CLOCK FREQUENCY

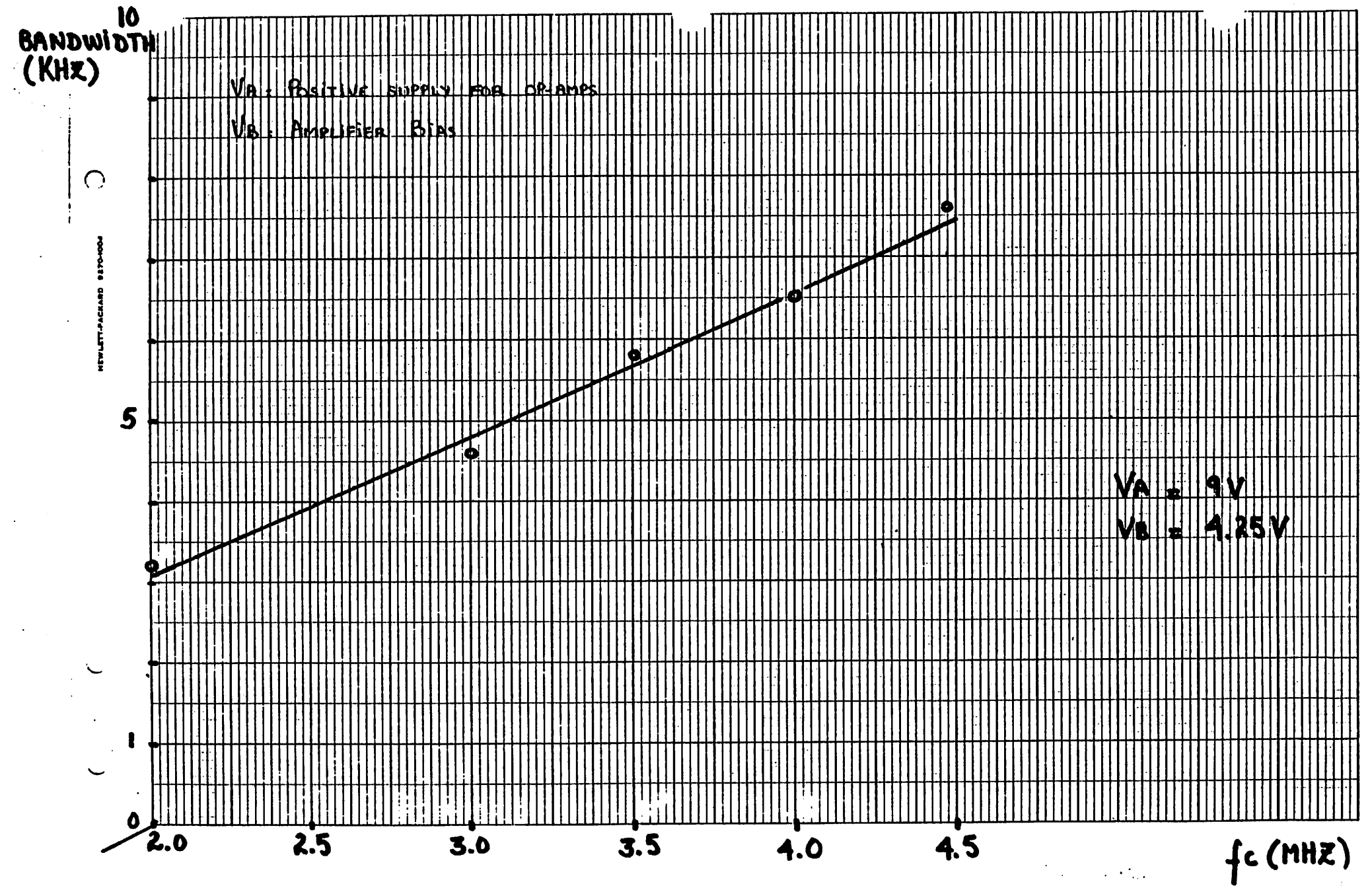


Fig. 8c BANDWIDTH VS. CLOCK FREQUENCY

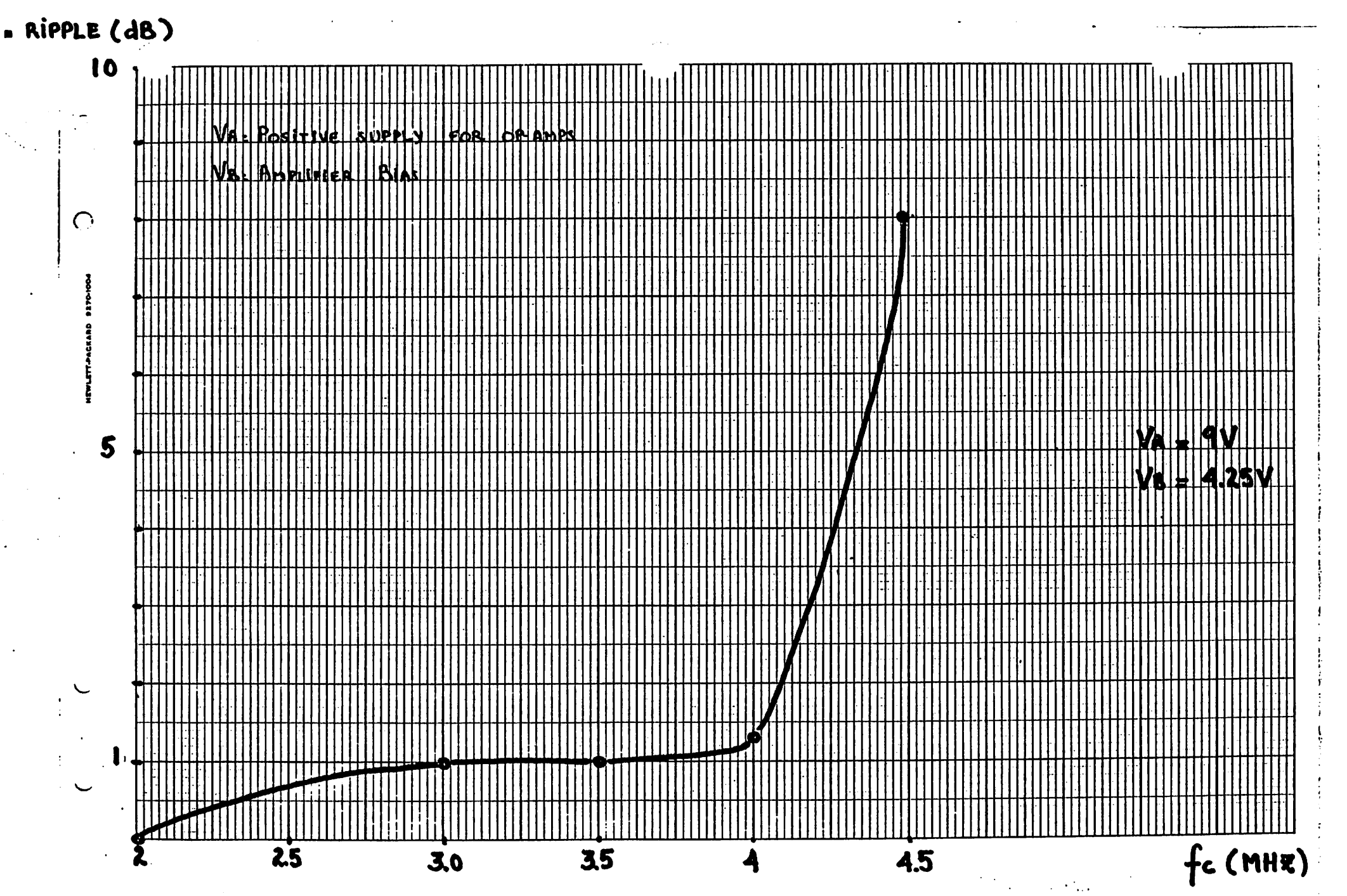


Fig. 8a RIPPLE VS. CLOCK FREQUENCY

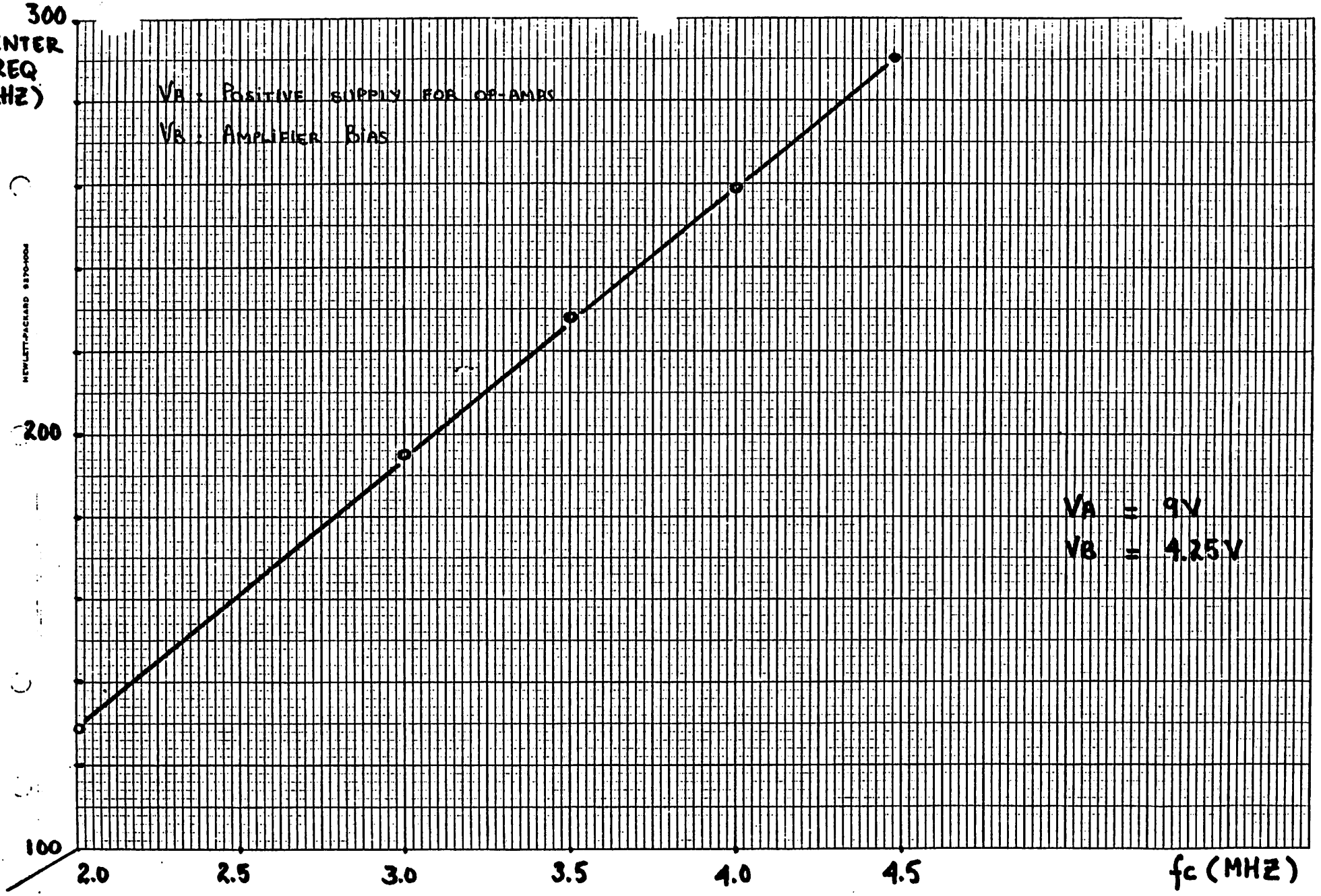


Fig. 8d CENTER FREQUENCY VS. CLOCK FREQUENCY

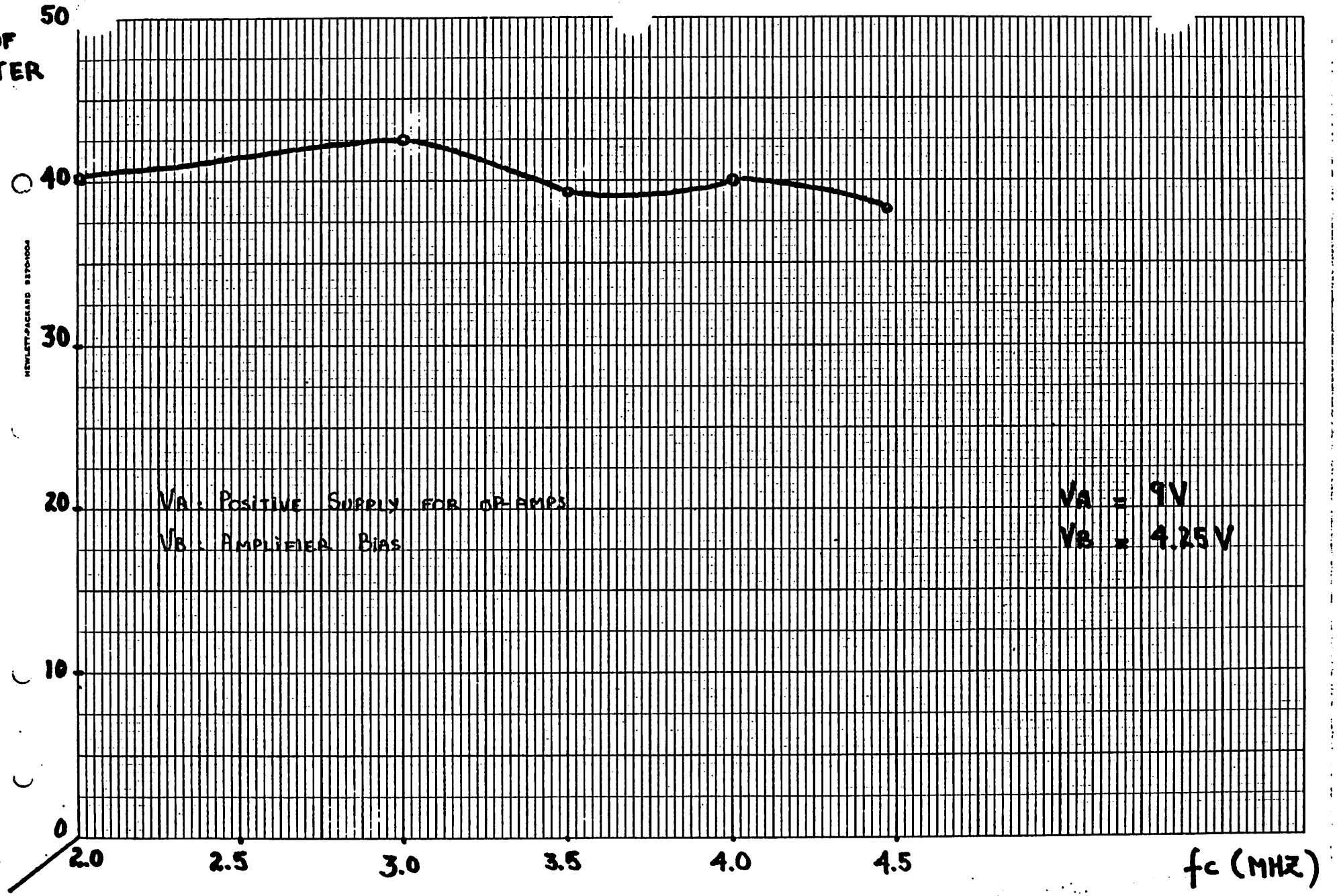


Fig. 8e FILTER'S Q VS. CLOCK FREQUENCY

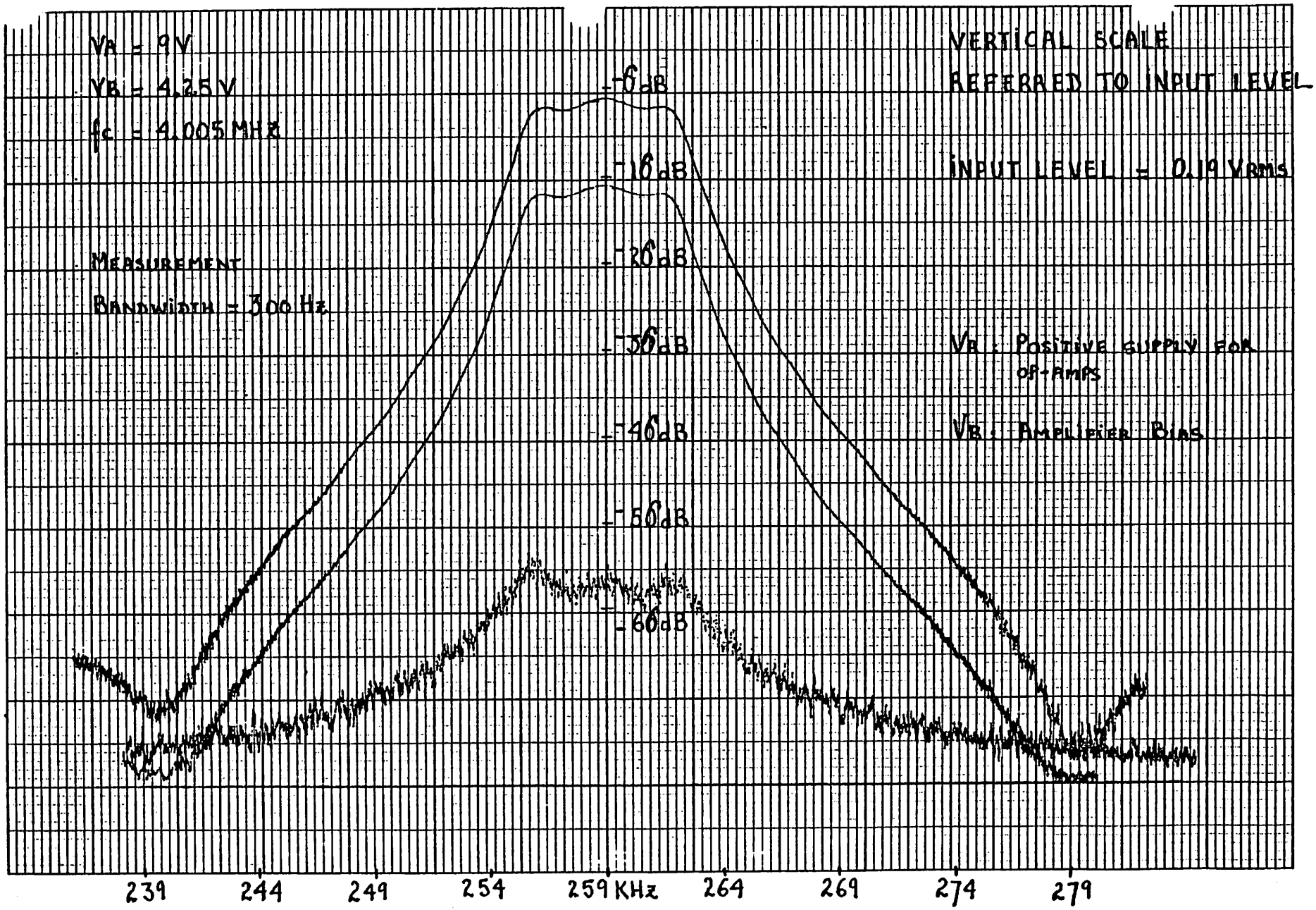


Fig. 9a NOISE LEVEL AT NOMINAL OPERATING POINT

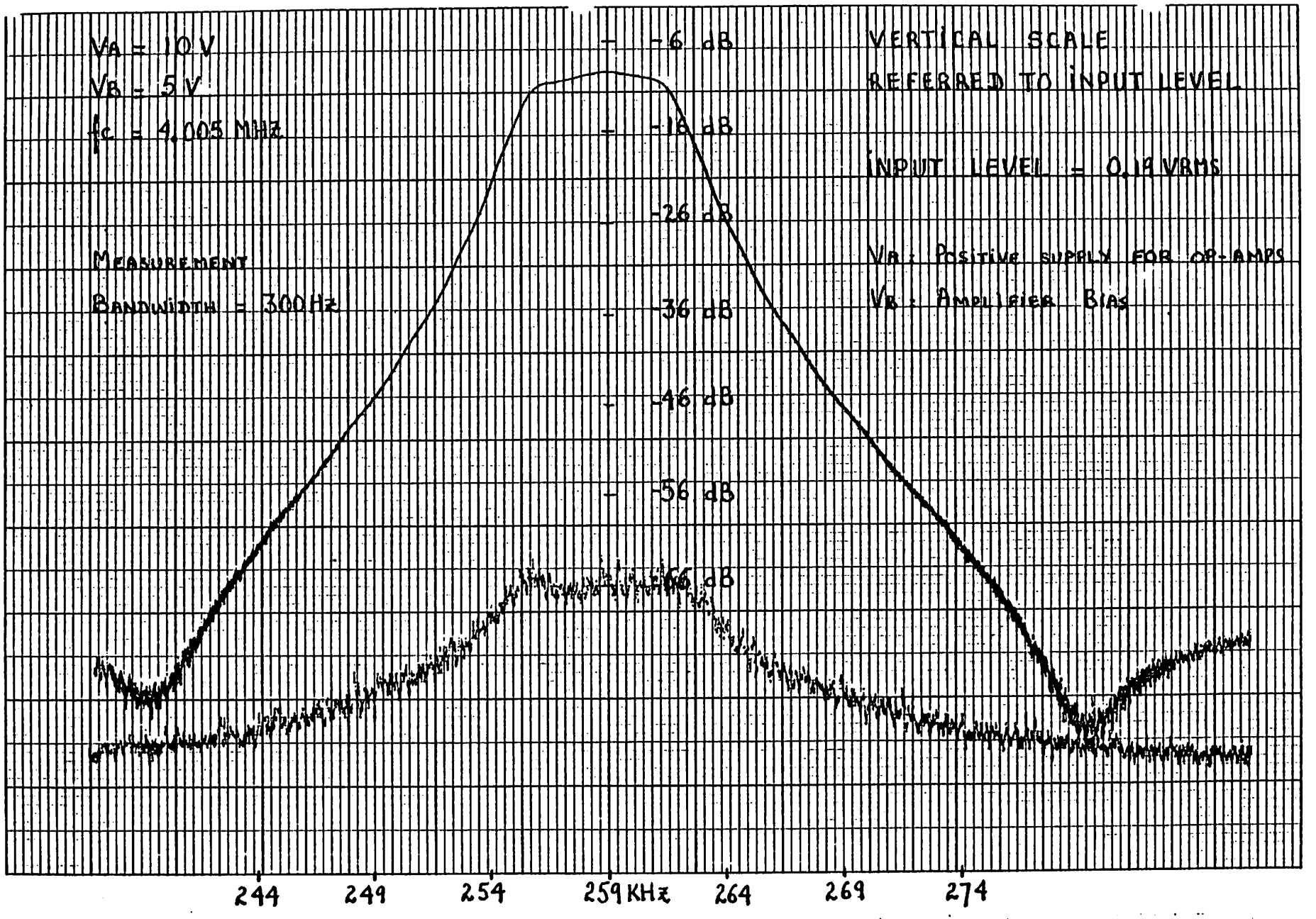


Fig. 9b NOISE LEVEL AT ANOTHER OPERATING POINT

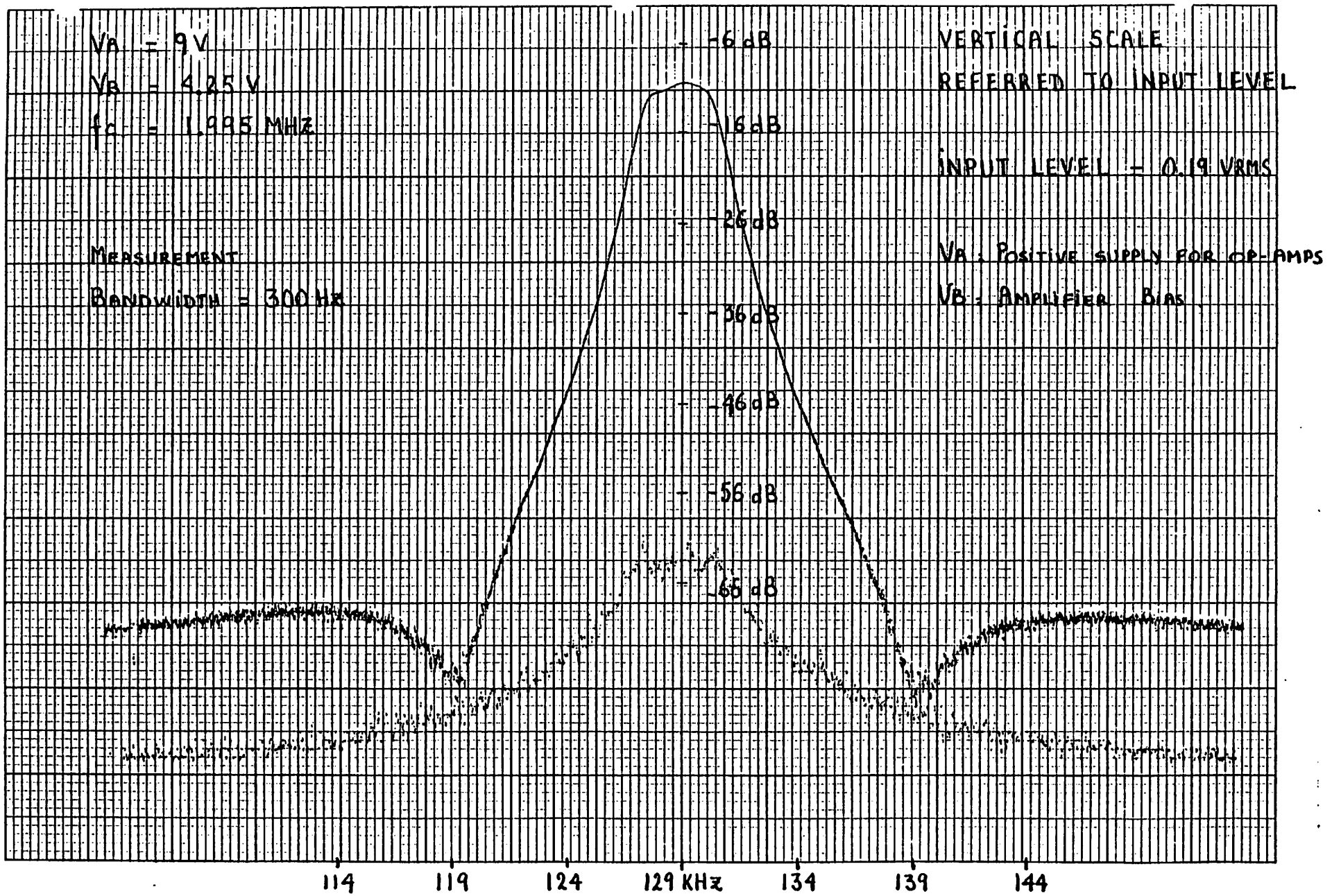


Fig. 10a NOISE LEVEL AT NOMINAL POWER SUPPLIES AND HALF CLOCK FREQUENCY

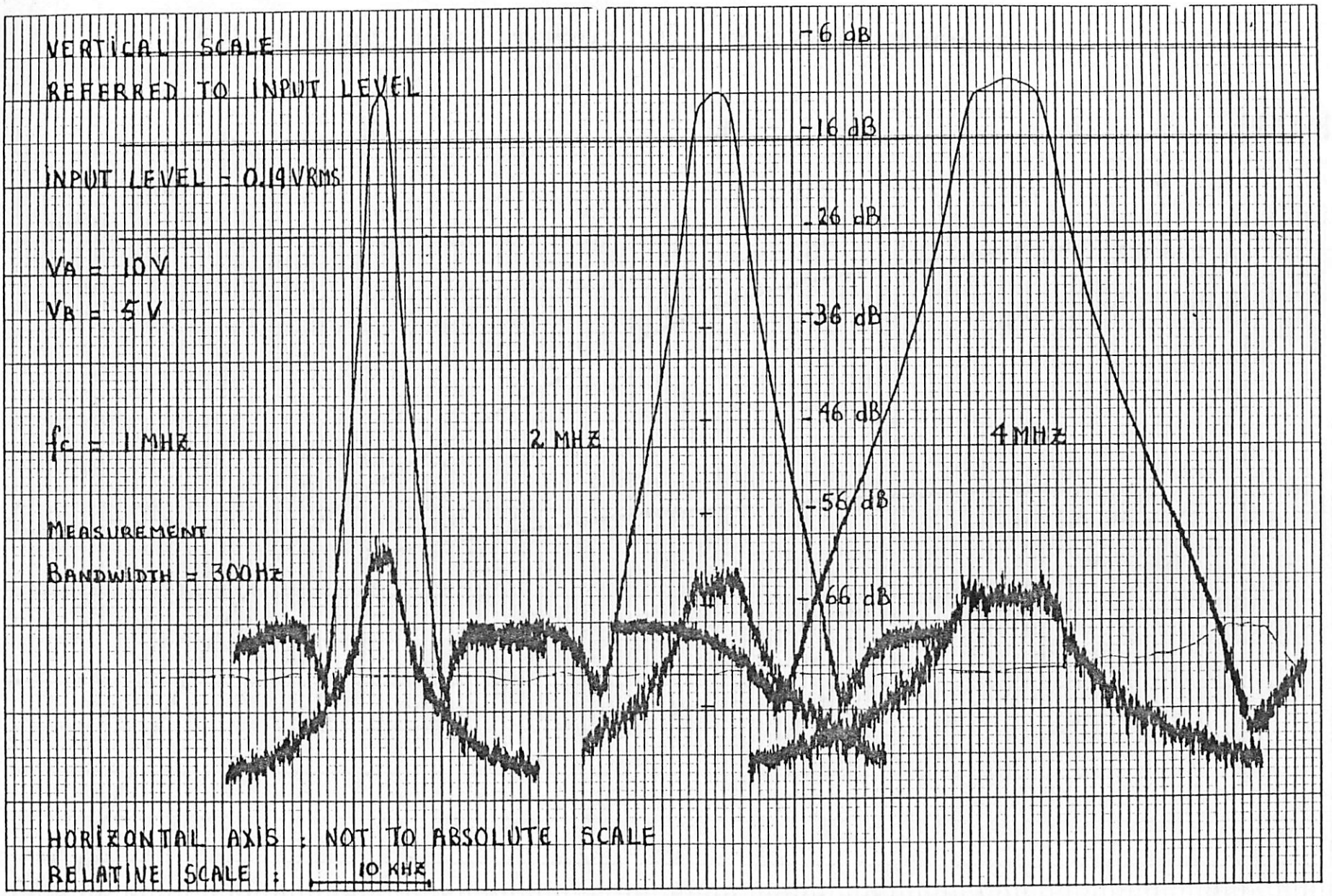


Fig. 10b NOISE LEVEL VS. CLOCK FREQUENCY

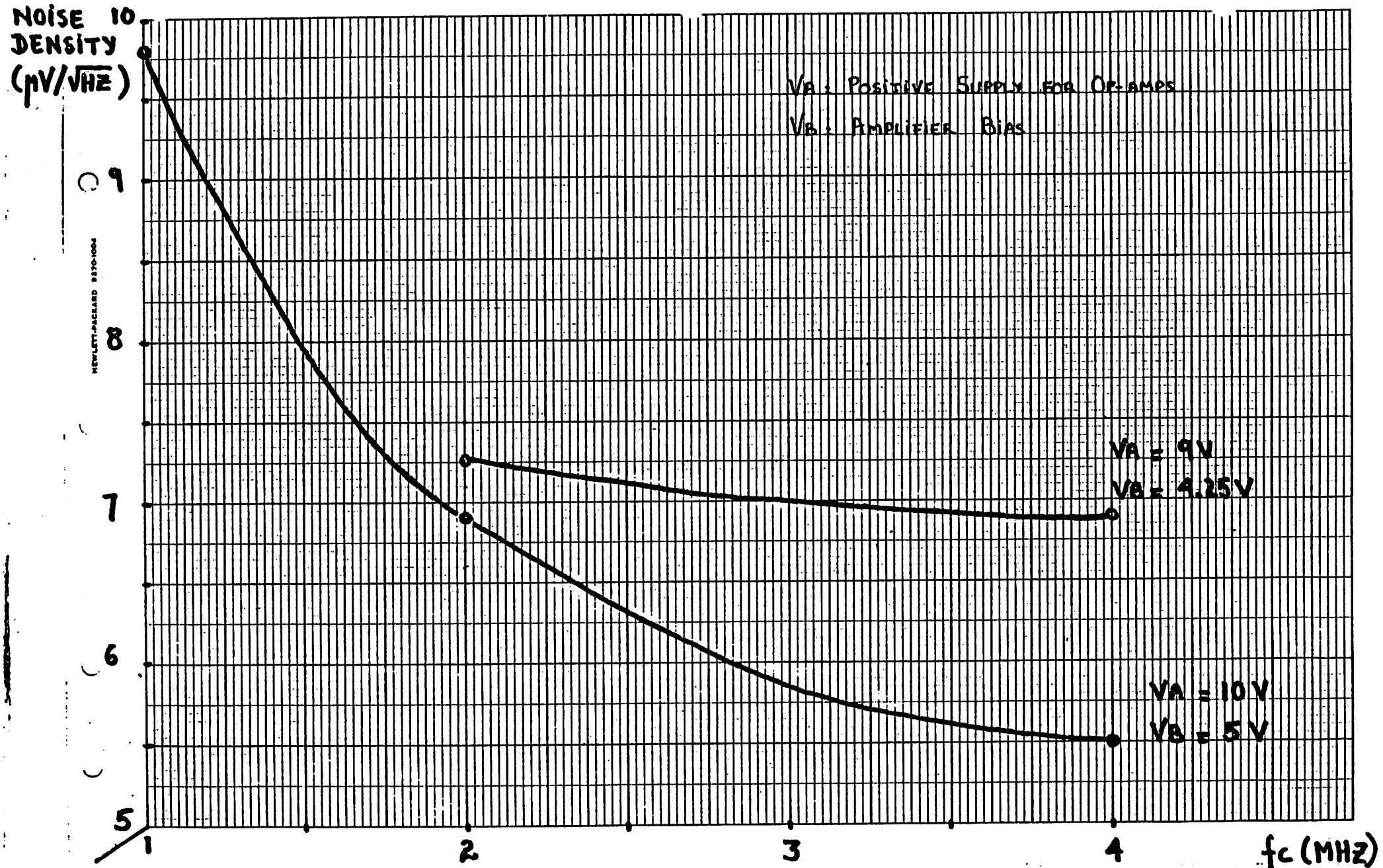


Fig. 11 IN-BAND NOISE DENSITY VS. CLOCK FREQUENCY

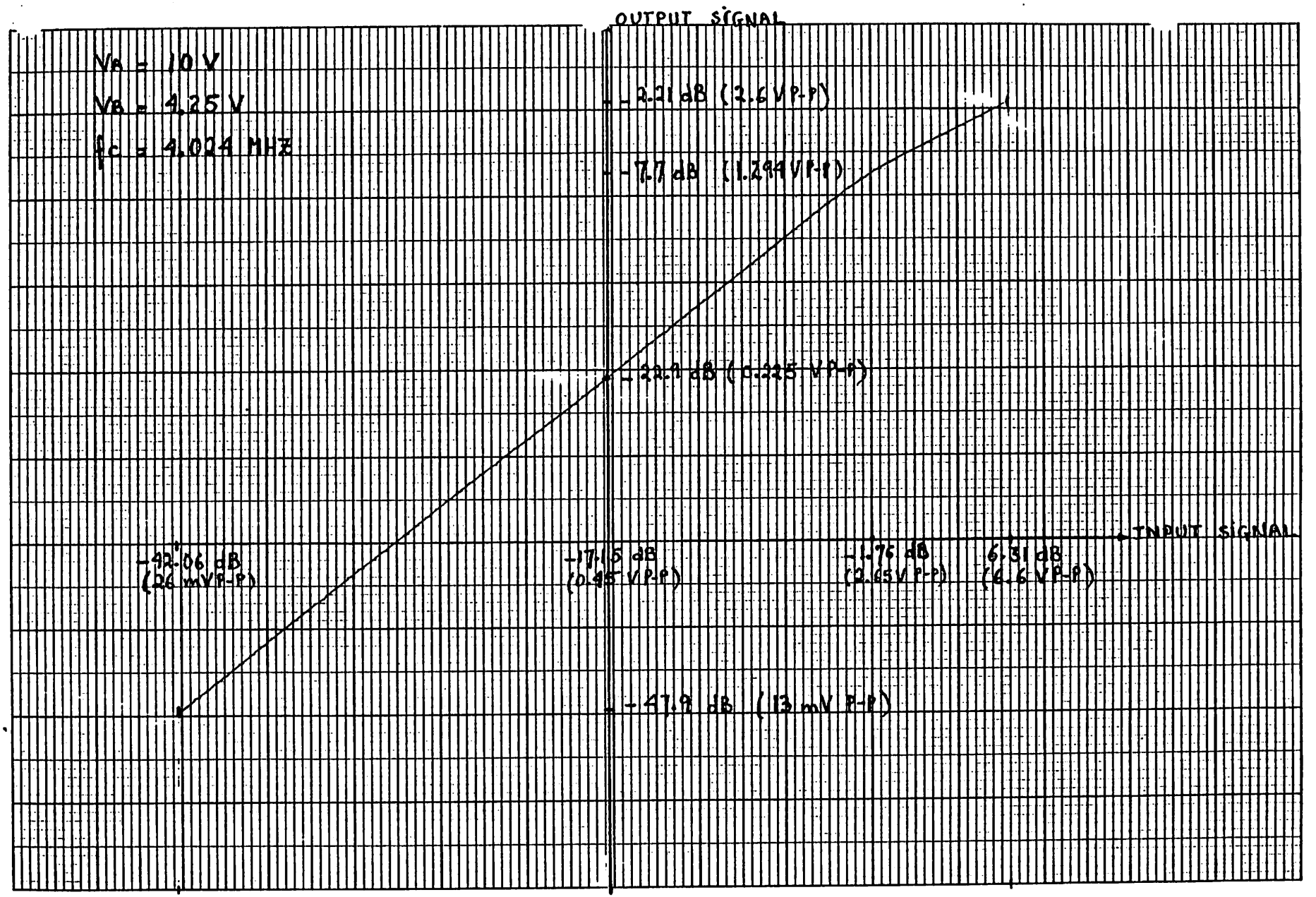


Fig. 12 OUTPUT LEVEL VS. INPUT LEVEL

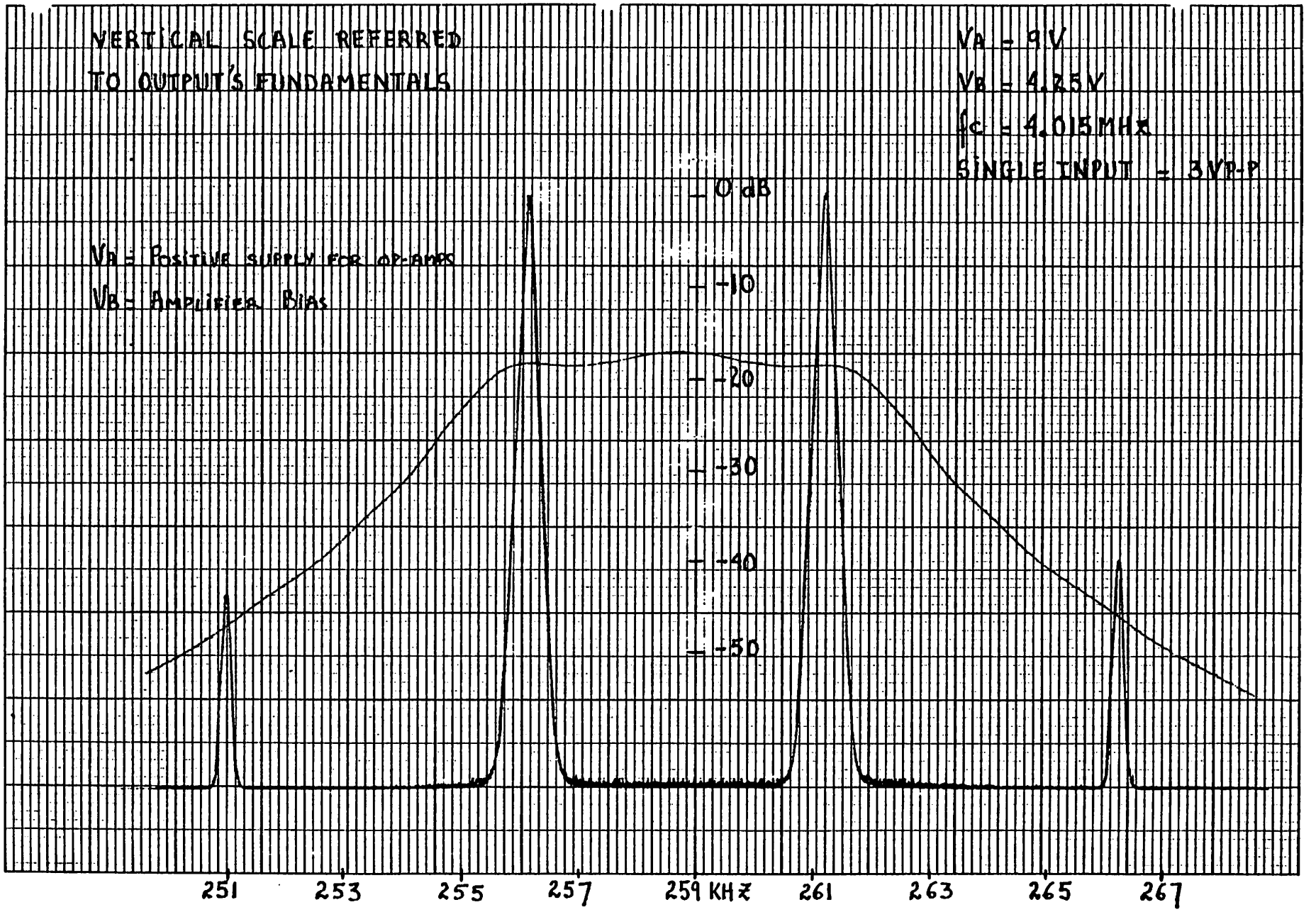


Fig. 13a IM DISTORTION (FUNDAMENTALS & HARMONICS) AT NOMINAL OPERATING POINT

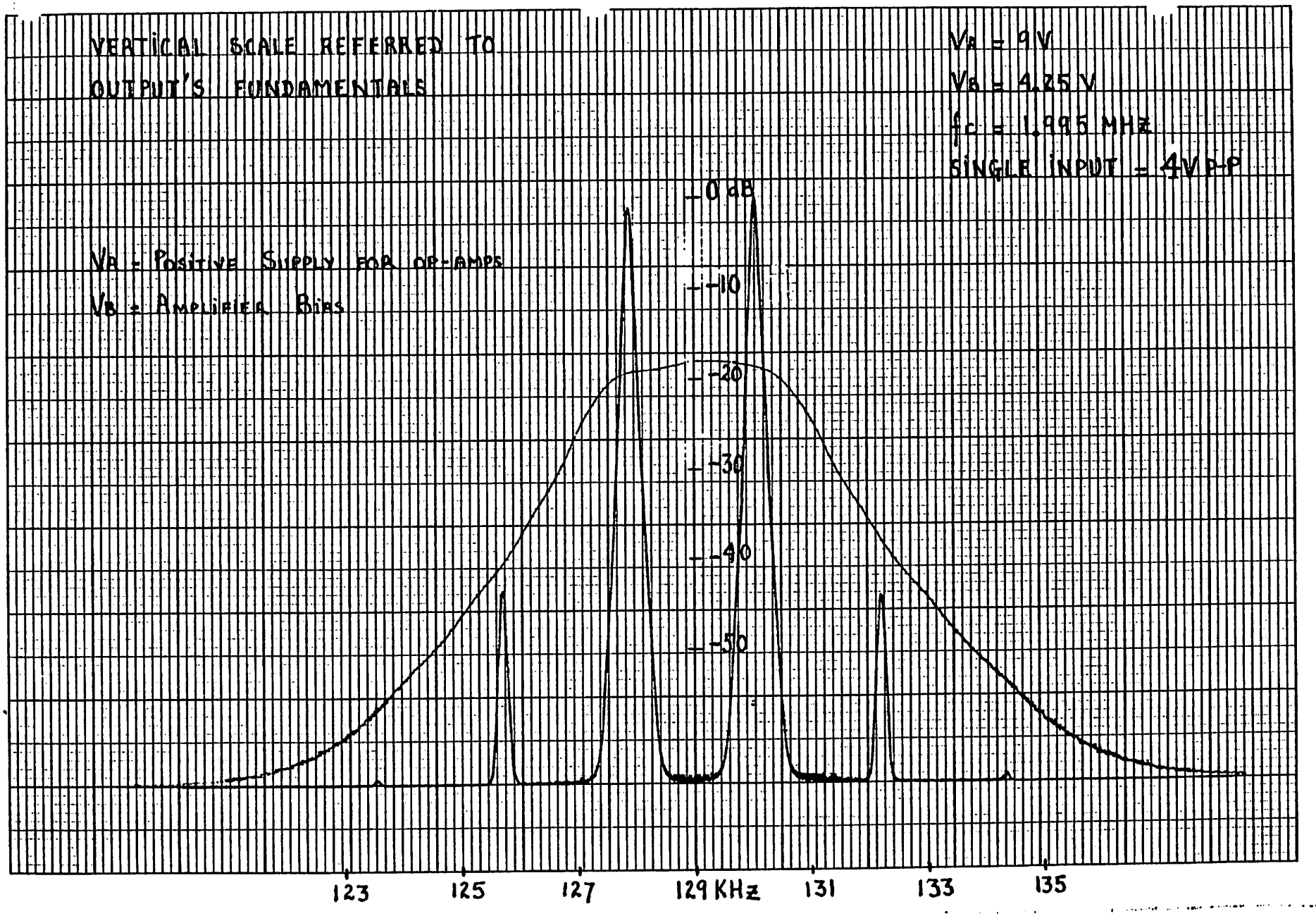


Fig. 13b IM DISTORTION (FUNDAMENTALS & HARMONICS) AT HALF CLOCK FREQUENCY

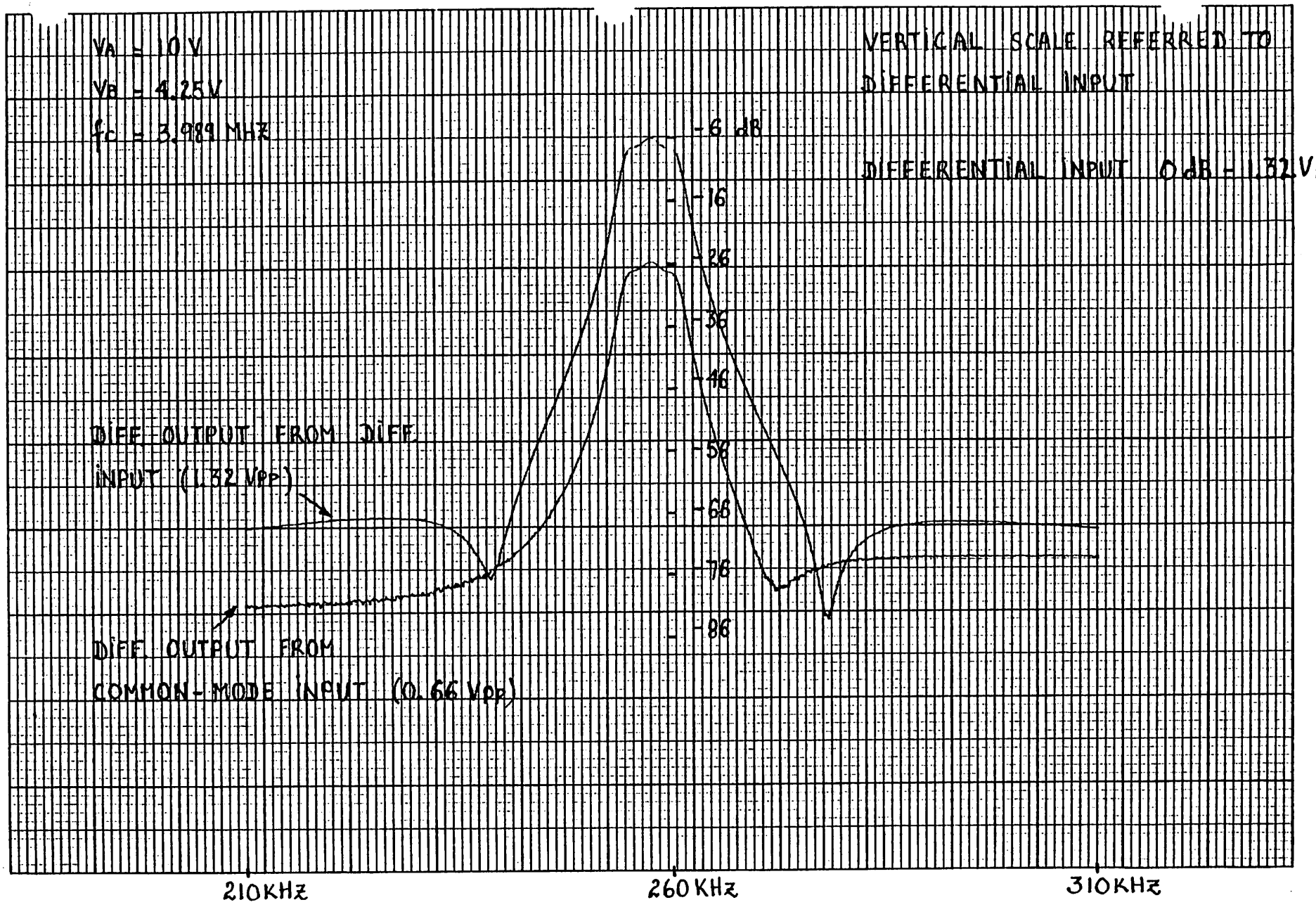


Fig. 14 DIFFERENTIAL-TO-COMMON-MODE GAIN

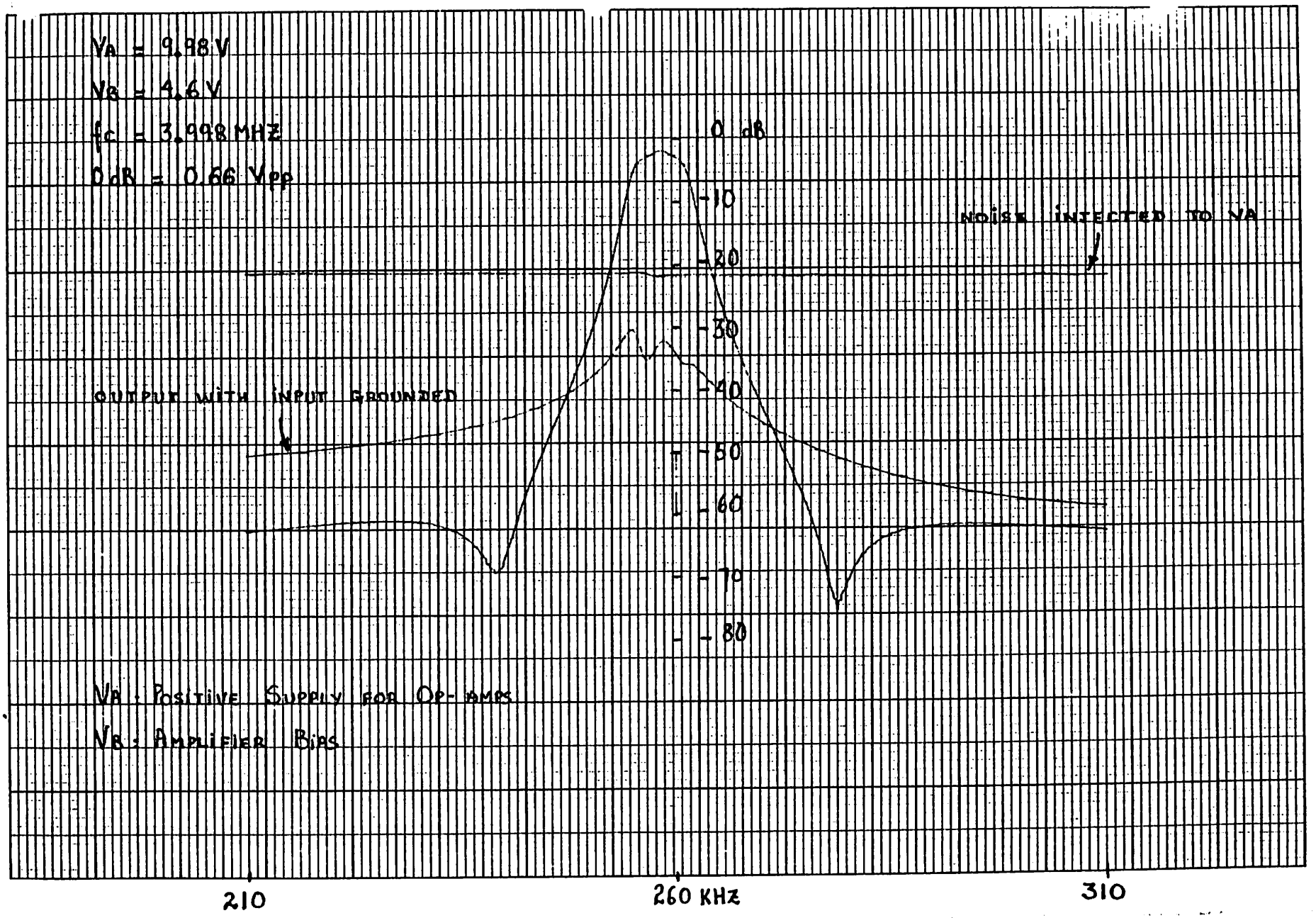


Fig. 15a POWER SUPPLY REJECTION OF VA

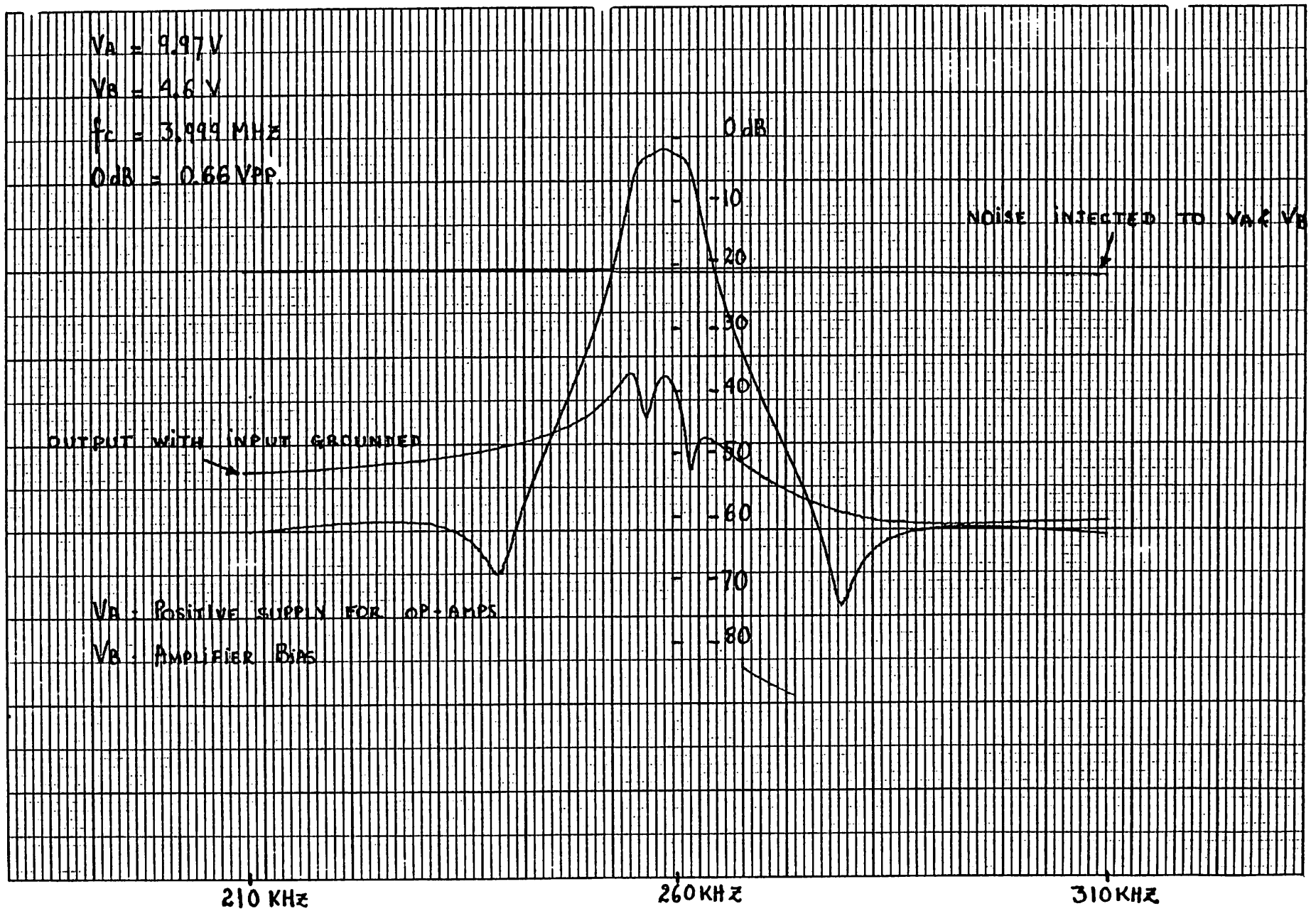


Fig. 15b POWER SUPPLY REJECTION OF V_A AND V_B

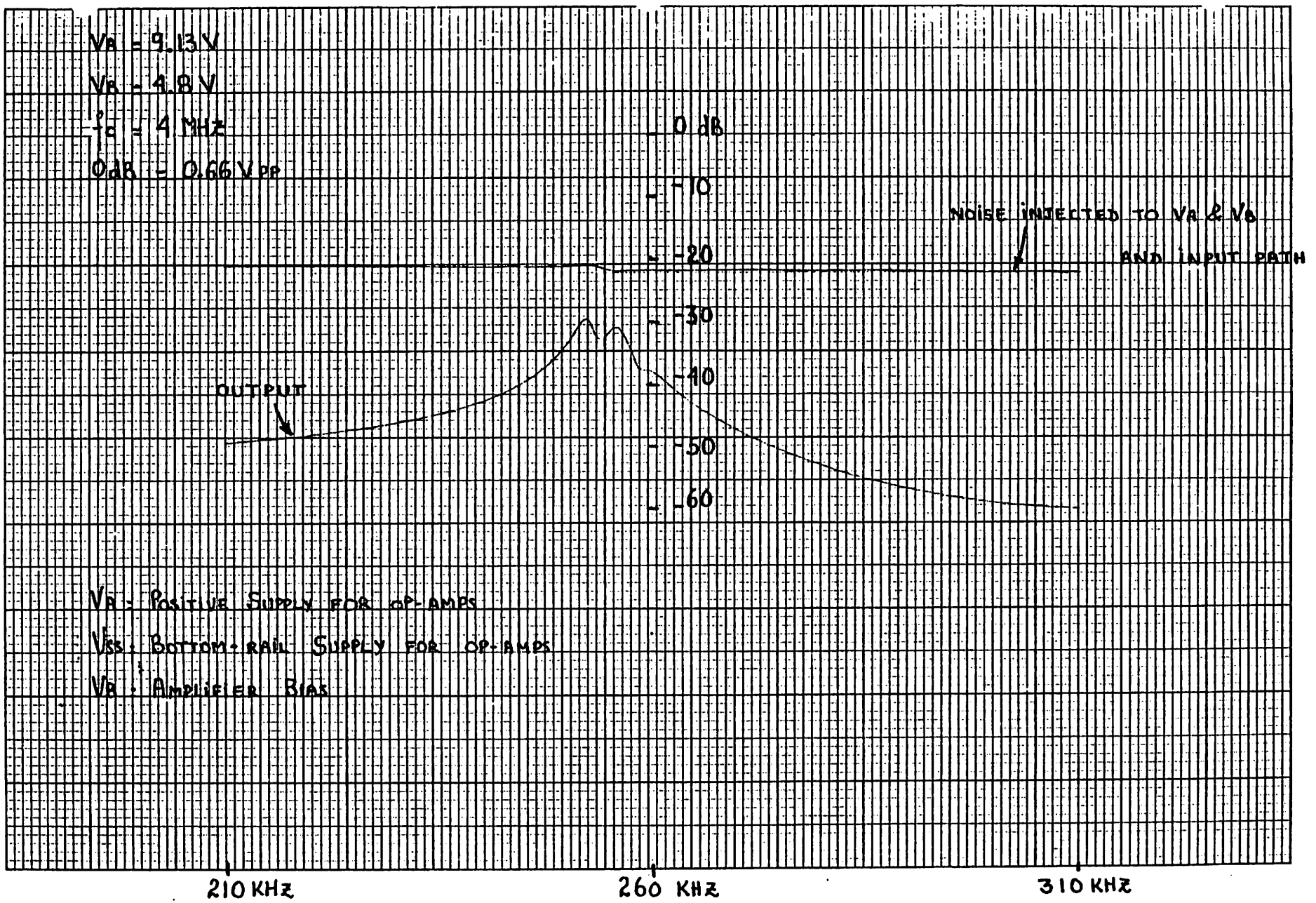


Fig. 15c POWER SUPPLY REJECTION OF Vss

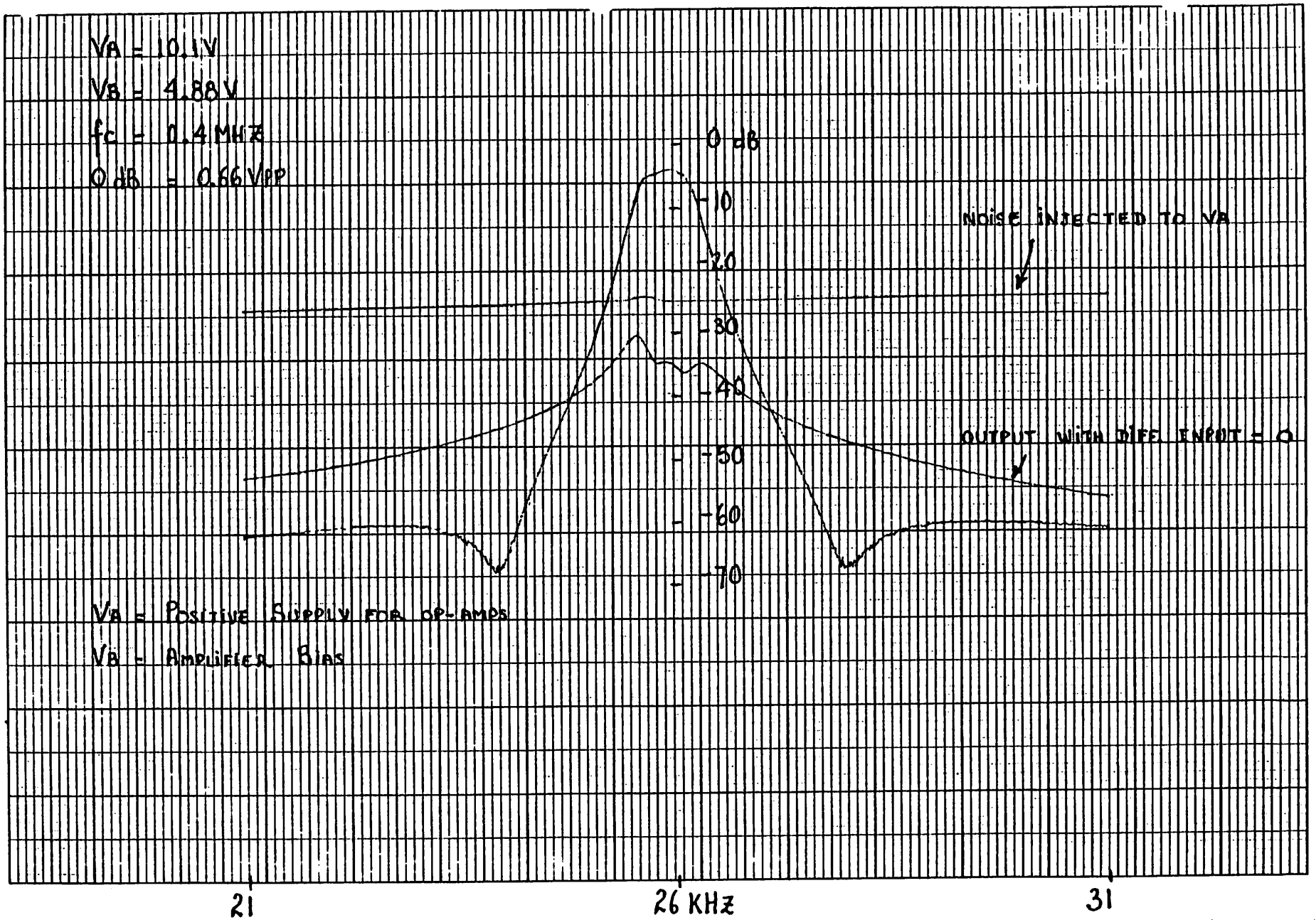


Fig. 16a POWER SUPPLY REJECTION OF VA AT f_c = 400 KHZ

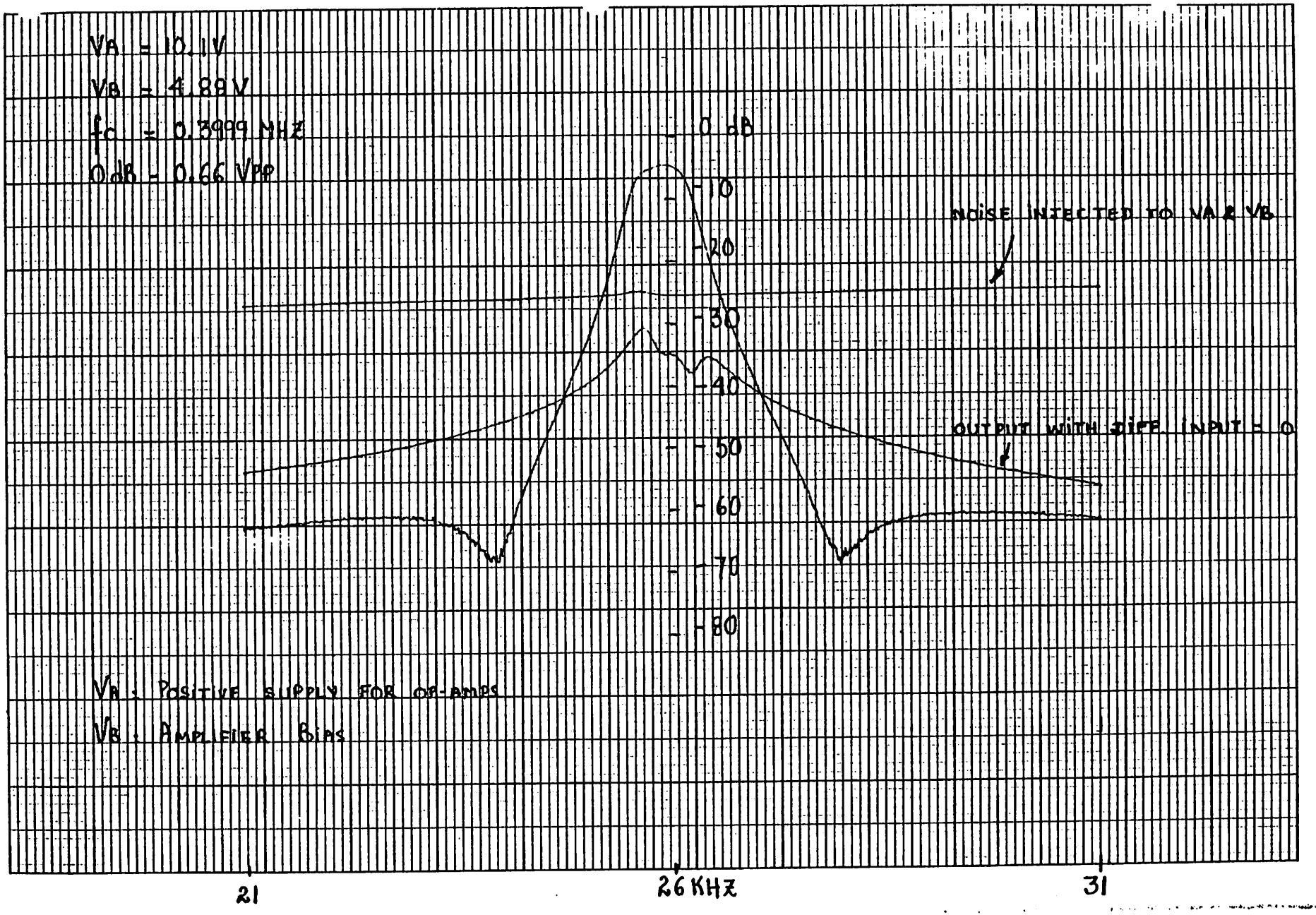


Fig. 16b POWER SUPPLY REJECTION OF VA AND VB AT fc = 400 KHZ

TABLE III

Performance Parameters of Filter

at Nominal Operating point

Clock rate f_c	4 MHz
Center frequency	259 KHz
Selectivity Q	40
In-band Gain	-6 dB
Ripple	1.3 dB
Stopband Rejection	-61 dB
Total In-band Noise	517 μV_{rms}
Power Supply Rejection	17 dB

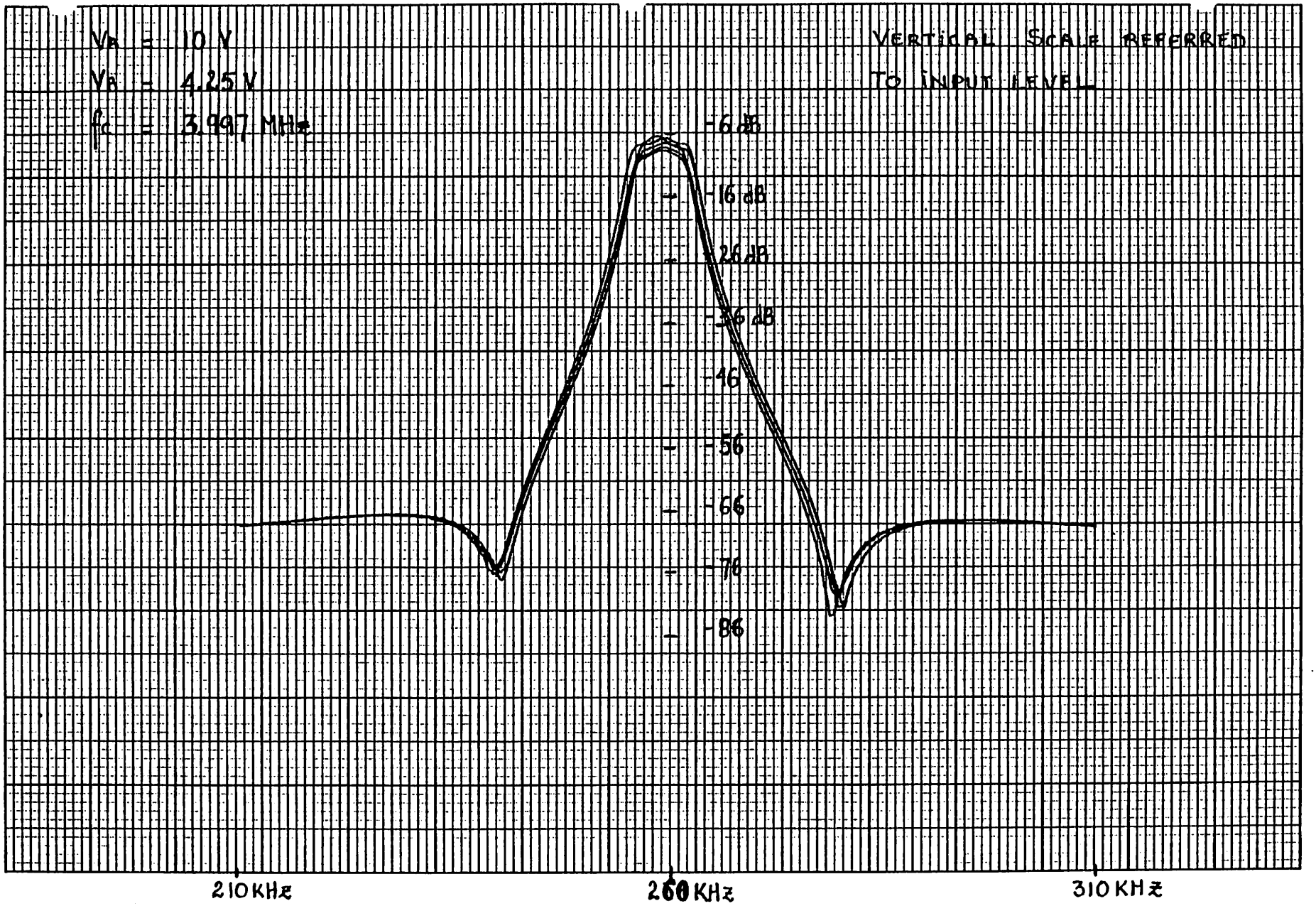


Fig. 17a FREQUENCY RESPONSES OF 5 DIFFERENT UNITS AT NOMINAL CLOCK FREQUENCY

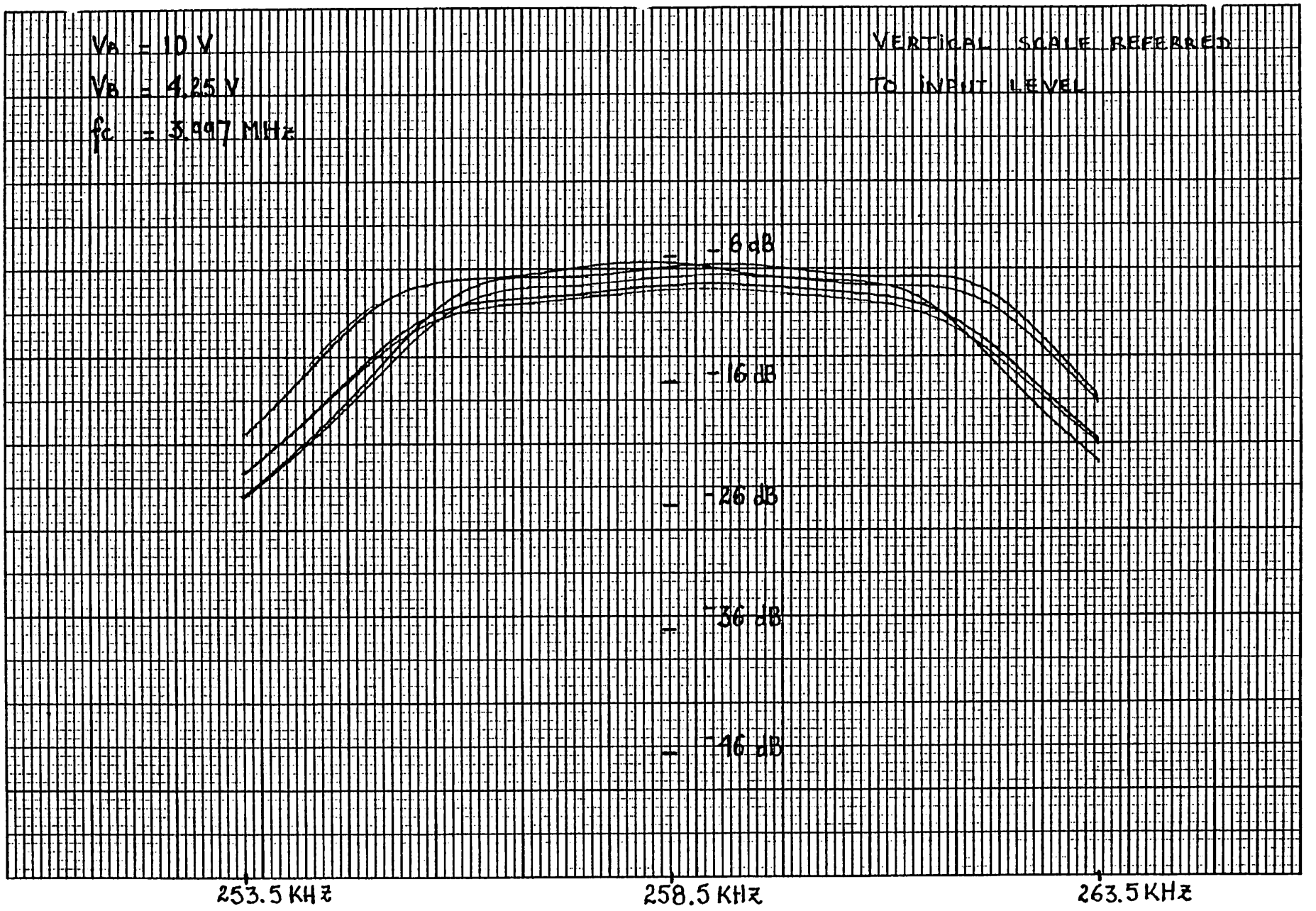


Fig. 17b PASSBANDS OF 5 DIFFERENT UNITS AT NOMINAL CLOCK FREQUENCY

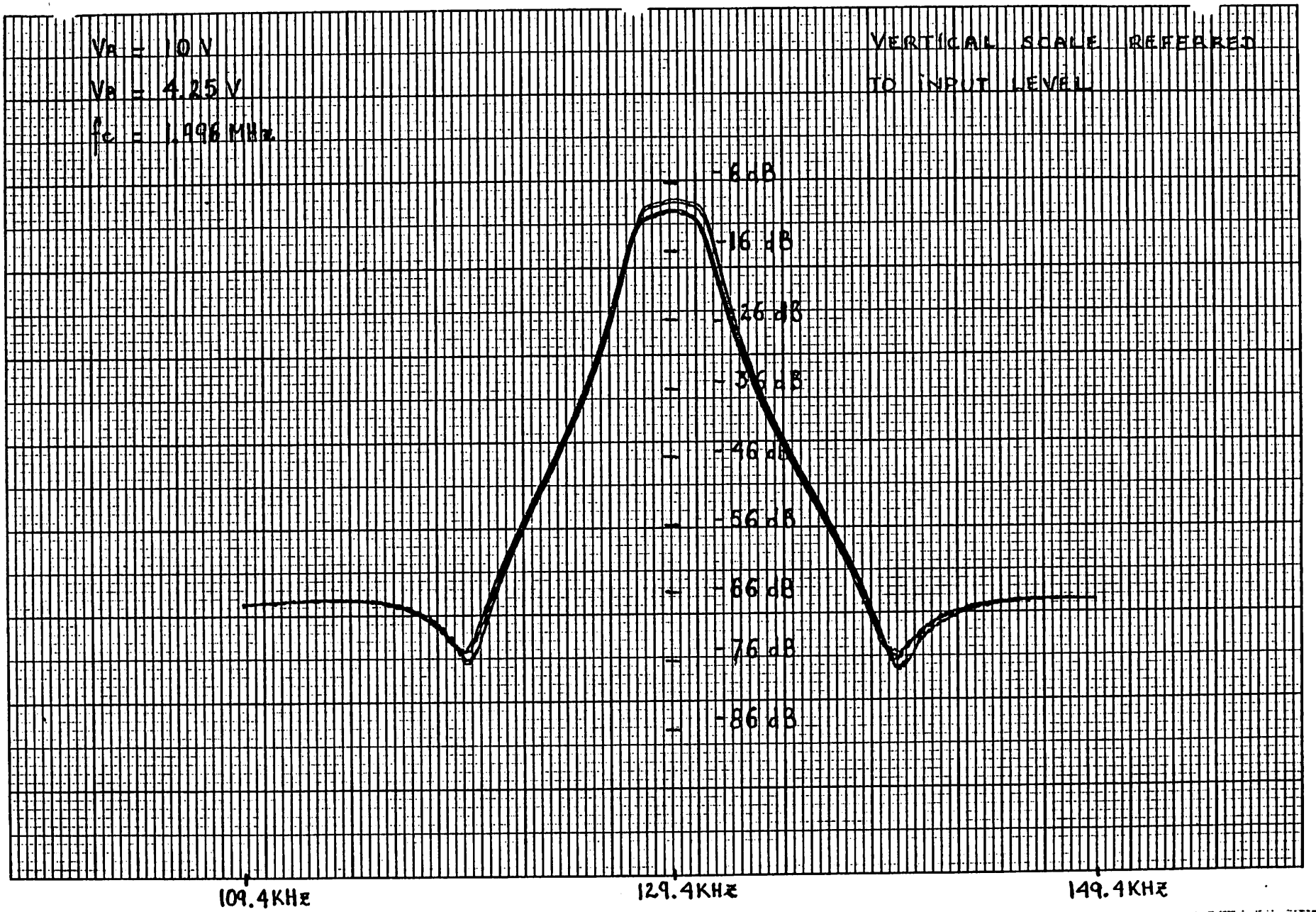


Fig. 18a FREQUENCY RESPONSES OF 5 DIFFERENT UNITS AT HALF CLOCK FREQUENCY

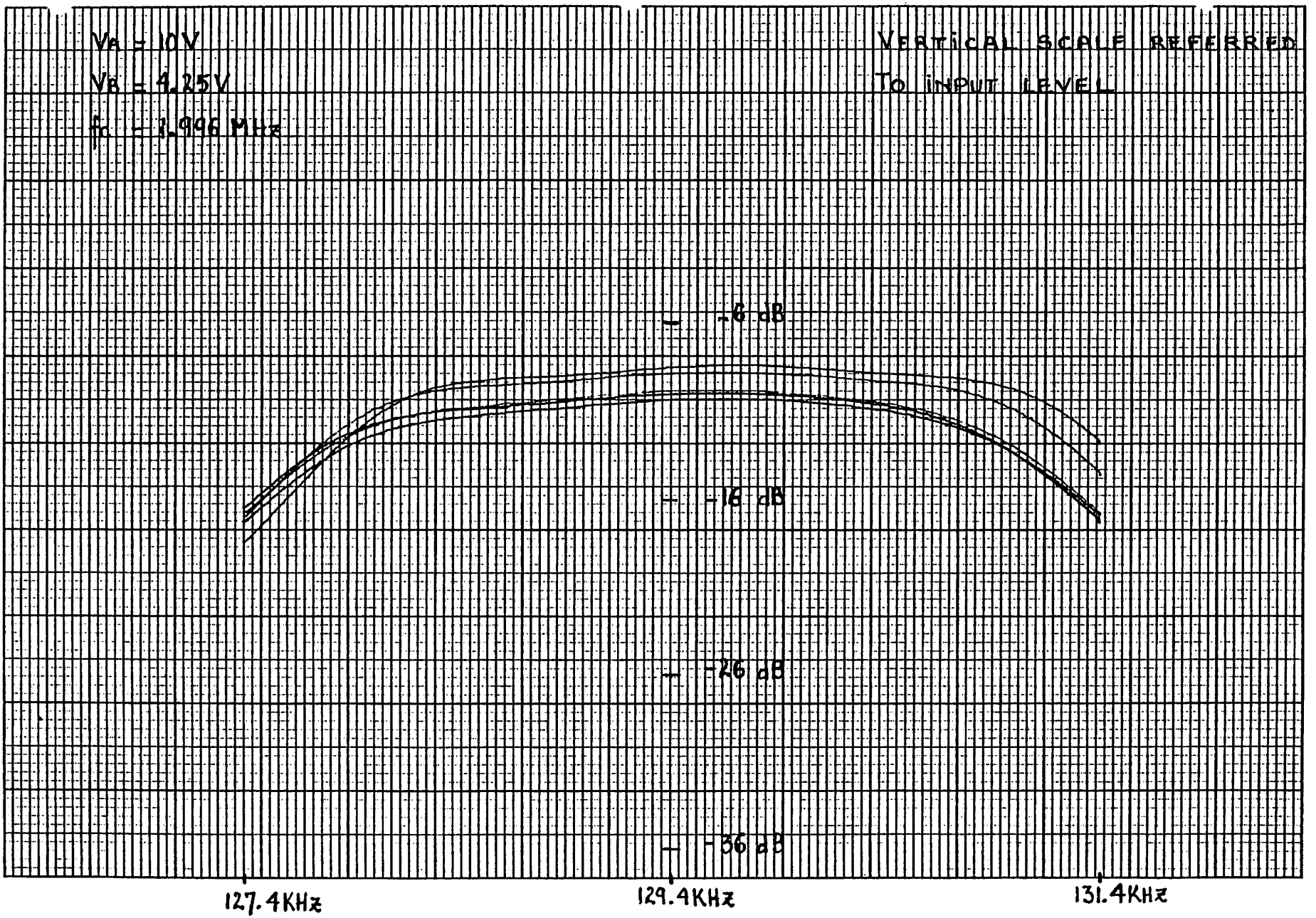


Fig. 18b PASSBANDS OF 5 DIFFERENT UNITS AT HALF CLOCK FREQUENCY

OSWITCHED-CAPACITOR FILTER

0**** INPUT LISTING TEMPERATURE = 27.000 DEG C

0**

```
 VIN 1 0 AC 2
 C0 1 3 0.0195074PF
 C4 3 4 1.3820273726PF
 E1 4 0 0 3 1MEG
 I1 3 0 DC 0
 R1 4 5 0.4463743MEG
 E2 6 0 0 5 1MEG
 I2 5 0 DC 0
 E3 7 0 6 0 -1
 C5 5 6 1.3820273726PF
 R2 7 3 0.4463743MEG
 C6 6 3 0.0201814PF
 C9 6 10 0.029548PF
 C12 10 11 1.3820273726PF
 E4 11 0 0 10 1MEG
 I3 10 0 DC 0
 E5 12 0 11 0 -1
 R3 12 13 0.4463743MEG
 C12A 13 14 1.3820273726PF
 E6 14 0 0 13 1MEG
 I4 13 0 DC 0
 R4 14 10 0.4463743MEG
 C13 14 3 0.0201814PF
 C16 14 17 0.0201814PF
 C19 17 18 1.3820273726PF
 E7 18 0 0 17 1MEG
 I5 17 0 DC 0
 R5 18 19 0.4463743MEG
 C20 19 20 1.3820273726PF
 E8 20 0 0 19 1MEG
 I6 19 0 DC 0
 E9 21 0 20 0 -1
 R6 21 17 0.4463743MEG
 C21 20 17 0.0201814PF
 C24 20 10 0.029548PF
 C27 6 25 0.0205976PF
 C30 25 26 1.5419782504PF
 C31 21 25 1.5419782504PF
 R7 25 26 2.5MEG
 E10 26 0 0 25 1MEG
 I7 25 0 DC 0
 .AC LIN 200 230K 290K
 .PLOT AC VDB(26)
 .NOISE V(26) VIN
 .PLOT NOISE ONOISE
 .WIDTH OUT=80
 .END
```

1*******09/01/82 ******** SPICE 2G.5 (04AUG81) ********13:06:51*****

OSWITCHED-CAPACITOR FILTER

0**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

0**

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.	(3)	0.	(4)	0.	(5)	0.
(6)	0.	(7)	0.	(10)	0.	(11)	0.
(12)	0.	(13)	0.	(14)	0.	(17)	0.
(18)	0.	(19)	0.	(20)	0.	(21)	0.
(25)	0.	(26)	0.				

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VIN 0. d+00

TOTAL POWER DISSIPATION 0. d+00 WATTS

1*******09/01/82 ******** SPICE 2G.5 (04AUG81) ********13:06:51*****

OSWITCHED-CAPACITOR FILTER

0**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0

0**** VOLTAGE-CONTROLLED VOLTAGE SOURCES

0	E1	E2	E3	E4	E5	E6	E7
V-SOURCE	0.	0.	0.	0.	0.	0.	0.
I-SOURCE	0. d+00	0. d+00	0. d+00	0. d+00	0. d+00	0. d+00	0. d+0

0	E8	E9	E10
V-SOURCE	0.	0.	0.
I-SOURCE	0. d+00	0. d+00	0. d+00

1*******09/01/82 ******** SPICE 2G.5 (04AUG81) ********13:06:51*****

OSWITCHED-CAPACITOR FILTER

0**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

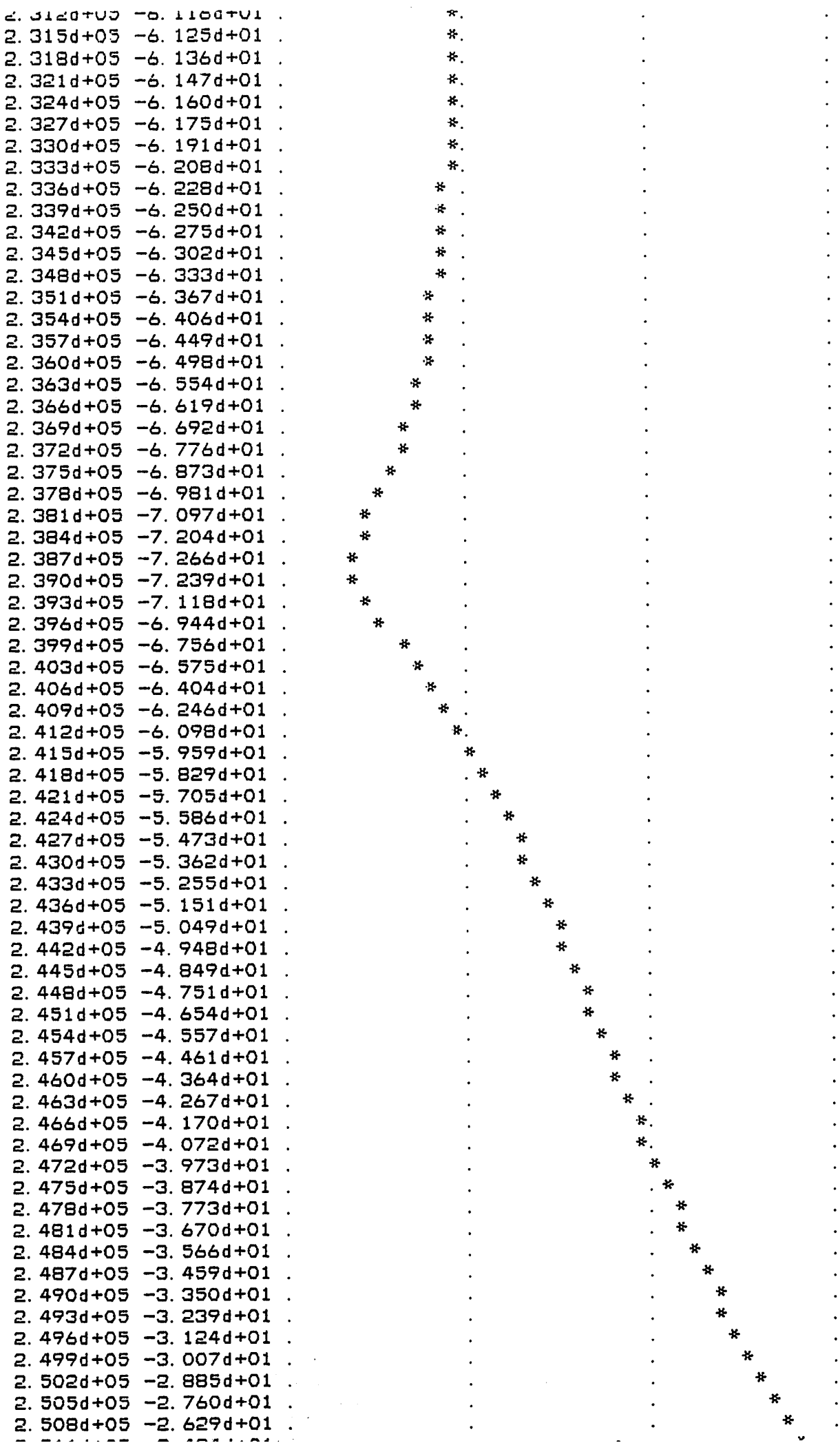
0**********

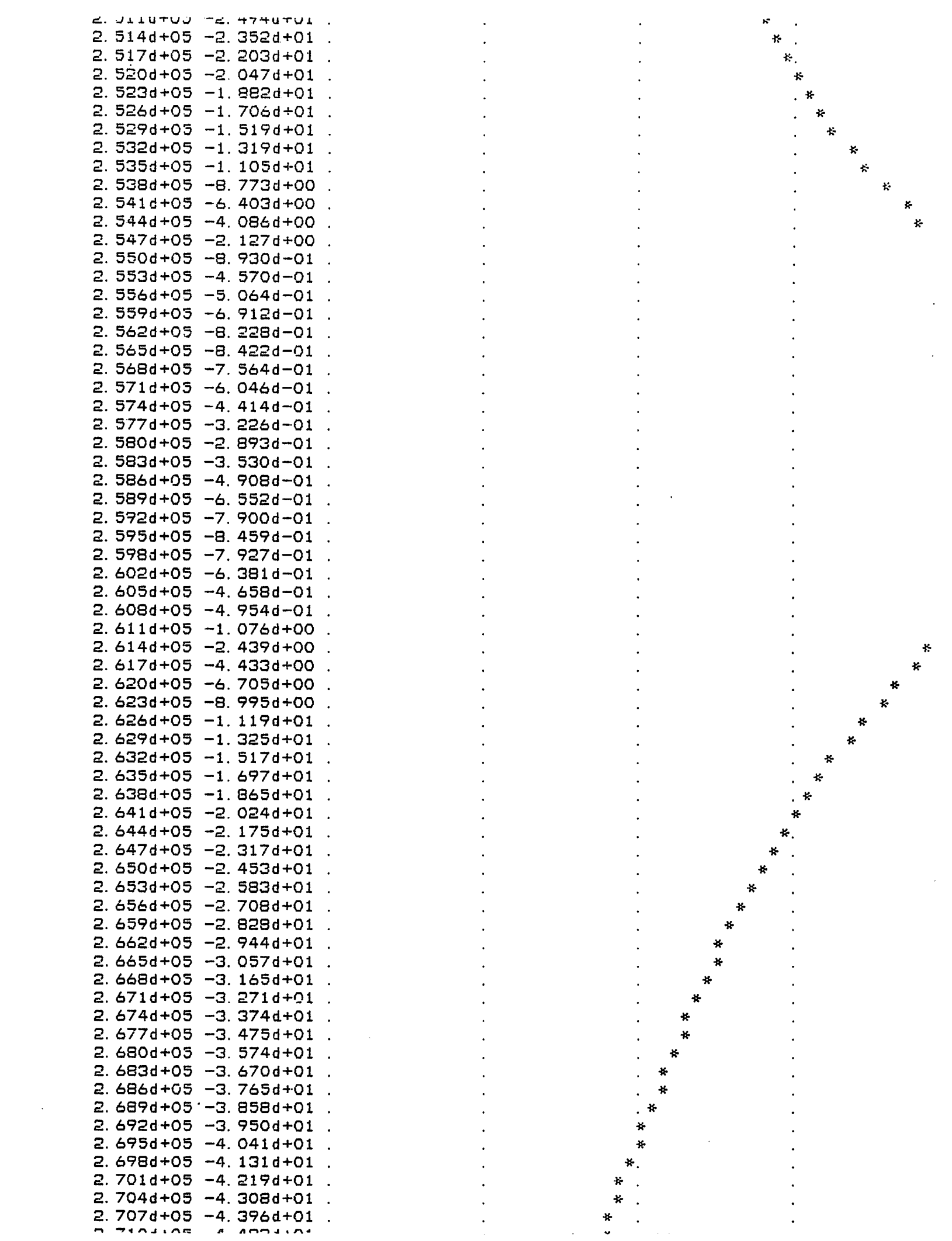
X

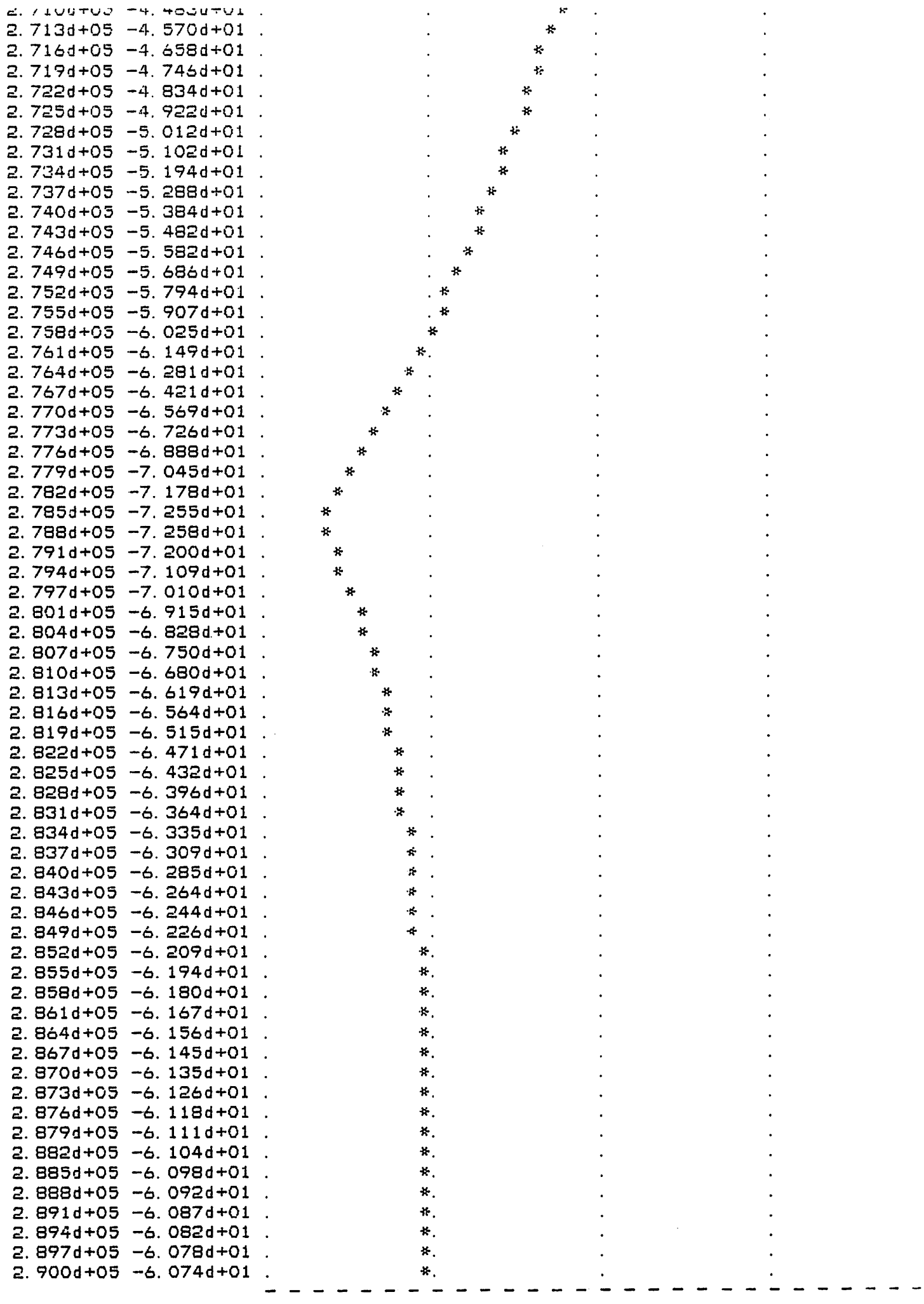
FREQ VDB(26)

X -8.000d+01 -6.000d+01 -4.000d+01 -2.000d+01 0. d

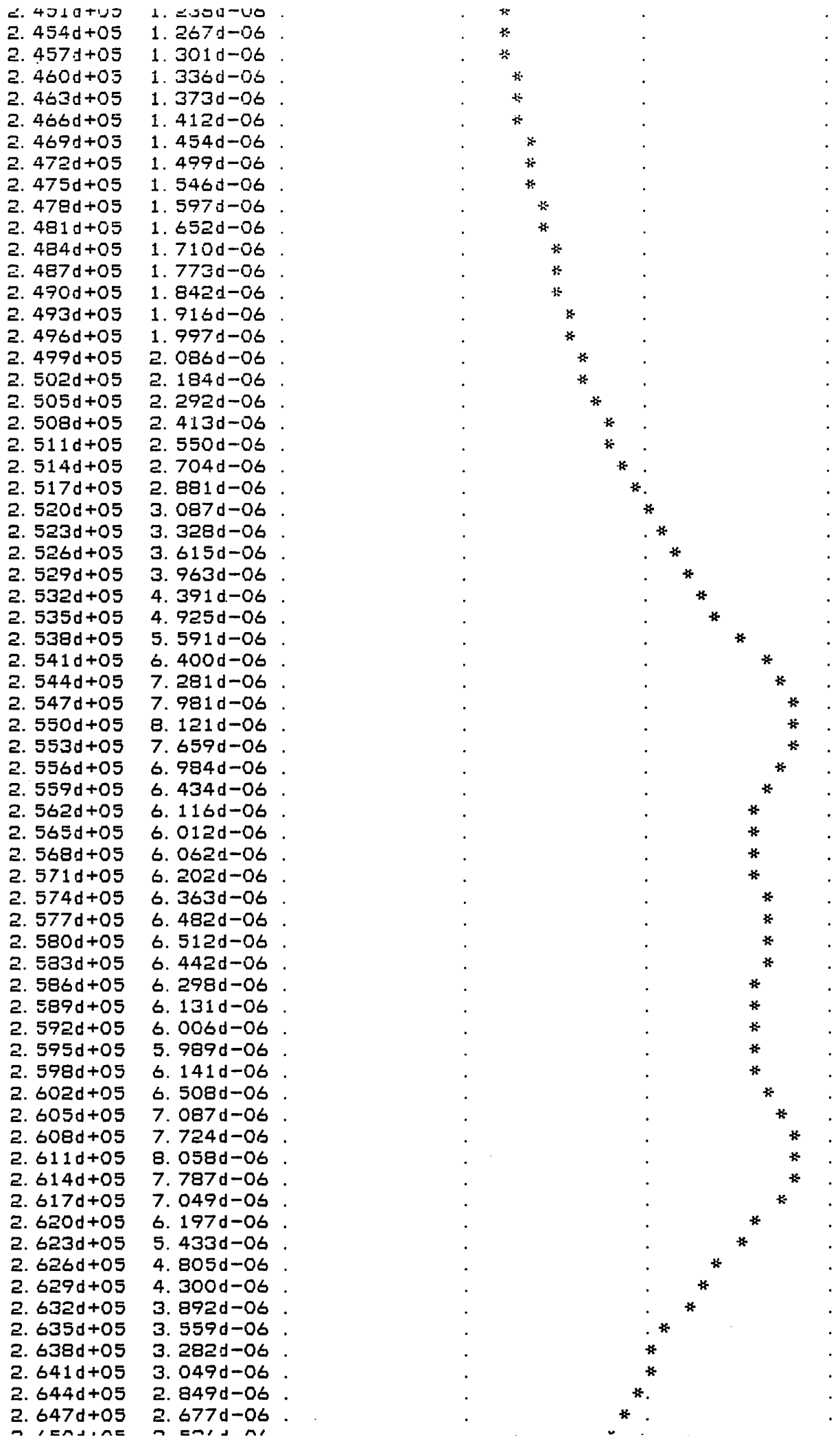
2.300d+05	-6.087d+01	.	*.	.	.
2.303d+05	-6.093d+01	.	*.	.	.
2.306d+05	-6.100d+01	.	*.	.	.
2.309d+05	-6.107d+01	.	*.	.	.

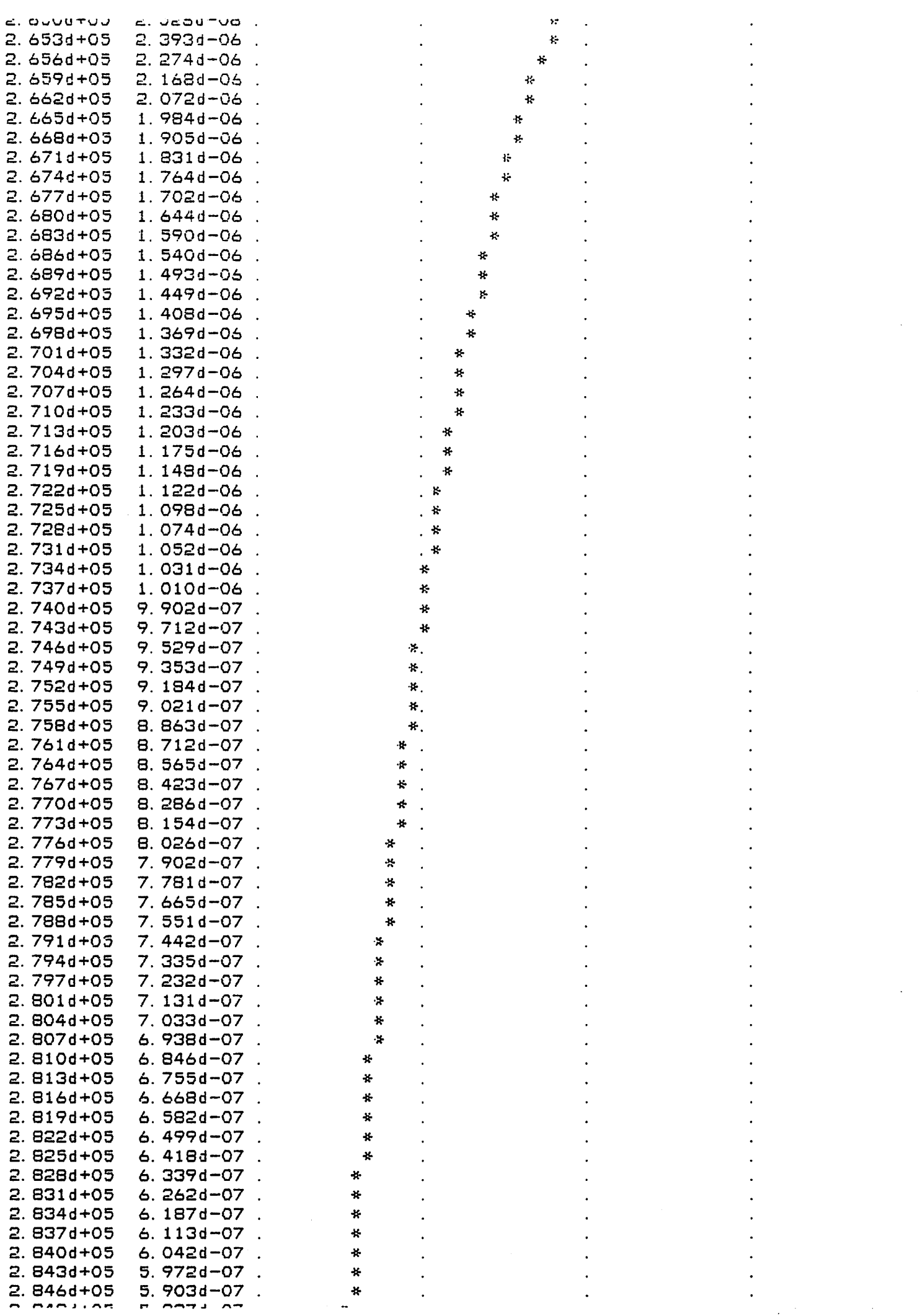

2.312d+05 -6.116d+01
2.315d+05 -6.125d+01
2.318d+05 -6.136d+01
2.321d+05 -6.147d+01
2.324d+05 -6.160d+01
2.327d+05 -6.175d+01
2.330d+05 -6.191d+01
2.333d+05 -6.208d+01
2.336d+05 -6.228d+01
2.339d+05 -6.250d+01
2.342d+05 -6.275d+01
2.345d+05 -6.302d+01
2.348d+05 -6.333d+01
2.351d+05 -6.367d+01
2.354d+05 -6.406d+01
2.357d+05 -6.449d+01
2.360d+05 -6.498d+01
2.363d+05 -6.554d+01
2.366d+05 -6.619d+01
2.369d+05 -6.692d+01
2.372d+05 -6.776d+01
2.375d+05 -6.873d+01
2.378d+05 -6.981d+01
2.381d+05 -7.097d+01
2.384d+05 -7.204d+01
2.387d+05 -7.266d+01
2.390d+05 -7.239d+01
2.393d+05 -7.118d+01
2.396d+05 -6.944d+01
2.399d+05 -6.756d+01
2.403d+05 -6.575d+01
2.406d+05 -6.404d+01
2.409d+05 -6.246d+01
2.412d+05 -6.098d+01
2.415d+05 -5.959d+01
2.418d+05 -5.829d+01
2.421d+05 -5.705d+01
2.424d+05 -5.586d+01
2.427d+05 -5.473d+01
2.430d+05 -5.362d+01
2.433d+05 -5.255d+01
2.436d+05 -5.151d+01
2.439d+05 -5.049d+01
2.442d+05 -4.948d+01
2.445d+05 -4.849d+01
2.448d+05 -4.751d+01
2.451d+05 -4.654d+01
2.454d+05 -4.557d+01
2.457d+05 -4.461d+01
2.460d+05 -4.364d+01
2.463d+05 -4.267d+01
2.466d+05 -4.170d+01
2.469d+05 -4.072d+01
2.472d+05 -3.973d+01
2.475d+05 -3.874d+01
2.478d+05 -3.773d+01
2.481d+05 -3.670d+01
2.484d+05 -3.566d+01
2.487d+05 -3.459d+01
2.490d+05 -3.350d+01
2.493d+05 -3.239d+01
2.496d+05 -3.124d+01
2.499d+05 -3.007d+01
2.502d+05 -2.885d+01
2.505d+05 -2.760d+01
2.508d+05 -2.629d+01




2.710d+05 -4.483d+01
2.713d+05 -4.570d+01
2.716d+05 -4.658d+01
2.719d+05 -4.746d+01
2.722d+05 -4.834d+01
2.725d+05 -4.922d+01
2.728d+05 -5.012d+01
2.731d+05 -5.102d+01
2.734d+05 -5.194d+01
2.737d+05 -5.288d+01
2.740d+05 -5.384d+01
2.743d+05 -5.482d+01
2.746d+05 -5.582d+01
2.749d+05 -5.686d+01
2.752d+05 -5.794d+01
2.755d+05 -5.907d+01
2.758d+05 -6.025d+01
2.761d+05 -6.149d+01
2.764d+05 -6.281d+01
2.767d+05 -6.421d+01
2.770d+05 -6.569d+01
2.773d+05 -6.726d+01
2.776d+05 -6.888d+01
2.779d+05 -7.045d+01
2.782d+05 -7.178d+01
2.785d+05 -7.255d+01
2.788d+05 -7.258d+01
2.791d+05 -7.200d+01
2.794d+05 -7.109d+01
2.797d+05 -7.010d+01
2.801d+05 -6.915d+01
2.804d+05 -6.828d+01
2.807d+05 -6.750d+01
2.810d+05 -6.680d+01
2.813d+05 -6.619d+01
2.816d+05 -6.564d+01
2.819d+05 -6.515d+01
2.822d+05 -6.471d+01
2.825d+05 -6.432d+01
2.828d+05 -6.396d+01
2.831d+05 -6.364d+01
2.834d+05 -6.335d+01
2.837d+05 -6.309d+01
2.840d+05 -6.285d+01
2.843d+05 -6.264d+01
2.846d+05 -6.244d+01
2.849d+05 -6.226d+01
2.852d+05 -6.209d+01
2.855d+05 -6.194d+01
2.858d+05 -6.180d+01
2.861d+05 -6.167d+01
2.864d+05 -6.156d+01
2.867d+05 -6.145d+01
2.870d+05 -6.135d+01
2.873d+05 -6.126d+01
2.876d+05 -6.118d+01
2.879d+05 -6.111d+01
2.882d+05 -6.104d+01
2.885d+05 -6.098d+01
2.888d+05 -6.092d+01
2.891d+05 -6.087d+01
2.894d+05 -6.082d+01
2.897d+05 -6.078d+01
2.900d+05 -6.074d+01

```
Y
1*******09/01/82 ********  SPICE 2G.5 (04AUG81)  ********13:06:51******

OSWITCHED-CAPACITOR FILTER

0****      AC ANALYSIS                          TEMPERATURE =   27.000 DEG C

0*****************************************************************************


X
     FREQ       ONOISE

X                    3.162d-07      1.000d-06      3.162d-06      1.000d-05  3.162d
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  2.300d+05  5.571d-07 .       *       .              .              .
  2.303d+05  5.632d-07 .       *       .              .              .
  2.306d+05  5.695d-07 .       *       .              .              .
  2.309d+05  5.759d-07 .       *       .              .              .
  2.312d+05  5.824d-07 .       *       .              .              .
  2.315d+05  5.891d-07 .        *      .              .              .
  2.318d+05  5.960d-07 .        *      .              .              .
  2.321d+05  6.030d-07 .        *      .              .              .
  2.324d+05  6.102d-07 .        *      .              .              .
  2.327d+05  6.175d-07 .        *      .              .              .
  2.330d+05  6.251d-07 .        *      .              .              .
  2.333d+05  6.328d-07 .        *      .              .              .
  2.336d+05  6.408d-07 .         *     .              .              .
  2.339d+05  6.489d-07 .         *     .              .              .
  2.342d+05  6.573d-07 .         *     .              .              .
  2.345d+05  6.658d-07 .         *     .              .              .
  2.348d+05  6.746d-07 .         *     .              .              .
  2.351d+05  6.837d-07 .         *     .              .              .
  2.354d+05  6.930d-07 .          *    .              .              .
  2.357d+05  7.025d-07 .          *    .              .              .
  2.360d+05  7.123d-07 .          *    .              .              .
  2.363d+05  7.224d-07 .          *    .              .              .
  2.366d+05  7.328d-07 .          *    .              .              .
  2.369d+05  7.436d-07 .          *    .              .              .
  2.372d+05  7.546d-07 .           *   .              .              .
  2.375d+05  7.660d-07 .           *   .              .              .
  2.378d+05  7.777d-07 .           *   .              .              .
  2.381d+05  7.898d-07 .           *   .              .              .
  2.384d+05  8.023d-07 .           *   .              .              .
  2.387d+05  8.152d-07 .            *  .              .              .
  2.390d+05  8.285d-07 .            *  .              .              .
  2.393d+05  8.423d-07 .            *  .              .              .
  2.396d+05  8.565d-07 .            *  .              .              .
  2.399d+05  8.713d-07 .            *  .              .              .
  2.403d+05  8.865d-07 .             *.              .              .
  2.406d+05  9.024d-07 .             *.              .              .
  2.409d+05  9.188d-07 .             *.              .              .
  2.412d+05  9.358d-07 .             *.              .              .
  2.415d+05  9.535d-07 .             *.              .              .
  2.418d+05  9.719d-07 .              *              .              .
  2.421d+05  9.911d-07 .              *              .              .
  2.424d+05  1.011d-06 .              *              .              .
  2.427d+05  1.032d-06 .              *              .              .
  2.430d+05  1.053d-06 .               *             .              .
  2.433d+05  1.076d-06 .               *             .              .
  2.436d+05  1.100d-06 .               *             .              .
  2.439d+05  1.124d-06 .               *             .              .
  2.442d+05  1.150d-06 .                *            .              .
  2.445d+05  1.177d-06 .                *            .              .
  2.448d+05  1.206d-06 .                *            .              .
```





```
2.849d+05   5.637d-07 .        *        .                .                .
2.852d+05   5.771d-07 .        *        .                .                .
2.855d+05   5.707d-07 .        *        .                .                .
2.858d+05   5.645d-07 .        *        .                .                .
2.861d+05   5.584d-07 .        *        .                .                .
2.864d+05   5.524d-07 .        *        .                .                .
2.867d+05   5.466d-07 .        *        .                .                .
2.870d+05   5.409d-07 .        *        .                .                .
2.873d+05   5.353d-07 .       *         .                .                .
2.876d+05   5.298d-07 .       *         .                .                .
2.879d+05   5.244d-07 .       *         .                .                .
2.882d+05   5.192d-07 .       *         .                .                .
2.885d+05   5.140d-07 .       *         .                .                .
2.888d+05   5.090d-07 .       *         .                .                .
2.891d+05   5.040d-07 .       *         .                .                .
2.894d+05   4.992d-07 .       *         .                .                .
2.897d+05   4.944d-07 .      *          .                .                .
2.900d+05   4.897d-07 .      *          .                .                .
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - -


Y
0
          JOB CONCLUDED
0          TOTAL JOB TIME            27.62
1*******09/01/82 ********  SPICE 2G.5 (04AUG81)  ********13:06:51*****

0

0****      INPUT LISTING                        TEMPERATURE =    27.000 DEG C

0******************************************************************************


0*ERROR*:   .END CARD MISSING
```