AN NMOS INTEGRATED VECTOR-LOCKED LOOP

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Ph. D.   EECS

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ABSTRACT

This dissertation presents and analyzes experimental results for a system that can be regarded as an extension of the phase-lock loop (PLL) concept. In a standard PLL, one error signal is developed representing the phase difference between a frequency reference and the output of an internal voltage-controlled oscillator (VCO). The input, output and error signal can be defined as *one dimensional vectors*.

The system described herein is capable of simultaneously tracking two independent parameters, namely the phase (or frequency) and amplitude of an input signal. In other words, by generating two simultaneous error signals the VCO output contains information not only about the phase but also about the amplitude of the input signal. Thus the input, output and error signals can be considered as *two dimensional vectors*. This condition led to naming the device *Vector-Lock Loop* (VLL).

frequency, phase modulation and demodulation; and automatic circuit gain controlling and precision filtering.

In this research an NMOS monolithic prototype was fabricated in order to demonstrate and evaluate the principles involved. The VLL was used to implement a *replica-type* (master and slave) bandpass filter capable of operating between $50kHz$ and $500kHz$, which is the intermediate frequency range of many subsystems in communications equipment.

Described herein is the theory of operation of the VLL; the analysis of the spectral characteristics of the output waveform and error signals; the circuit design approach for the implementation of each of the individual blocks; the tools used for the design, measurements and characterization of the prototype; and conclusions and topics for future studies.

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CHAPTER 1

INTRODUCTION

Until a very few years ago, there were close ties between each monolithic integrated circuit technology and their applications. For example, analog circuits were implemented almost invariably using bipolar processes. For digital circuits the choices were bipolar or CMOS for medium scale (MSI) logic; and PMOS, CMOS and NMOS for large scale circuits (LSI) such as microprocessor and memory chips.

Two factors made the rate of development not the same for all technologies: firstly, the demand for LSI parts because of the boom of the computer market clearly favored investment in MOS over others and secondly, bipolar was already closer to the ultimate design limit. Thus the following question arose: Is it possible to use MOS technology for the implementation of analog-integrated circuits? The positive answer to this question came about through the following evolutionary path.

Integrated electronic subsystems are composed of cells implemented using circuit techniques that usually belong to a given technology (i.e. bipolar). Rather than attempting to translate the circuitry for each individual cell from one technology to another, a more appropriate solution is to look into the overall definitions of the system functions and use this as a starting point for the implementation. Based on this approach, new circuit concepts emerged. Charge redistribution techniques for analog-to-digital conversion and filtering [1], [2], and charge transfer devices for analog delay lines used in transversal filters are some examples of these ideas [3].

Along with the development of these new techniques came the need for compatible building blocks such as operational amplifiers, comparators, multipliers, etc., to be used as support circuitry. Thus several NMOS and CMOS implementations of these functions emerged, using some techniques that are well-known in bipolar circuit technology, and others that are exclusive to MOS technology.

Another very important aspect of the development of the LSI technology is dimensional shrinking. Both analog and digital integrated circuits seem to benefit from this, but the electrical implications of the scaling process favor the digital circuit more [4]. This fact seems to jeopardize the further development of all analog circuits in any technology, for as the saying goes: "Everything will be done digitally". The statement is very logical and possible, except for the fact that at one point some sort of interface has to be placed between the real world signals, many of which are analog by nature, and the digital, signal-processing element (DSP). Usually this interface implies an analog-to-digital converter, and when the required output is analog, a digital-to-analog converter is also needed. The amount of overhead created by these elements can be very significant in any dedicated signal processor. Furthermore, some specific operations require very powerful, digital arithmetic units. Presently, DSPs operate in the audio-frequency range [5]. Therefore, politics aside, the final implementation decision must be based on a cost/performance/reliability argument. As an example in favor of the analog implementation, a two-pole analog in-and-out filter can be fully implemented with only two operational amplifiers, a few capacitors and analog switches, whereas a digital approach requires an analog-to-digital converter, an arithmetic unit, some registers, and a digital-to-analog converter. In the above case, with the present state of technology, the analog implementation yields a considerably smaller integrated circuit chip area and higher processing speed [6], [7] than the digital approach. However as signal processing becomes more

complex, the digital approach proves to be a better choice, not only because of real estate considerations but also in terms of power consumption and ease of design. This last factor is of prime importance when effects such as element parasitics, stability of the active circuits, noise, etc., have to be considered for the analog design. As an example, in the case of a 20th order filter it would be very difficult to justify using a complex analog implementation if a device such as a digital signal processor were available. When the implementation is digital, the performance (analog interfaces aside) is determined primarily by the program, which can be much more easily and rapidly modified and improved than a circuit configuration which requires circuit simulation and chip layout. Because of this faster turnaround time, the digital approach is preferred, even at an extra area cost, when the volume of devices needed is small.

But research in analog circuitry must continue in its trend of growth and improvement without being hindered by the existence of the digital world. As a matter of fact, the system implementation will benefit on the whole from this research, if future hybrid combinations of both techniques are used.

The main topic of this thesis is the analysis, development and NMOS implementation of a multiple-feedback system named Vector-Lock Loop, believed to be an original concept, presented here for the first time. This work is presented as an analog system, but the basic concepts are not restrictive, for it is possible to envision potential digital implementations of the same idea. As part of this research, different MOS circuit techniques are developed and explored for this application that can also be used in areas such as communications, signal processing, waveform shaping, etc.

CHAPTER 2

THEORY OF OPERATION OF THE VECTOR-LOCK LOOP

2.1. The Vector-Lock Loop Concept

The concept of the vector lock loop (VLL) is an extension of the well-known phase-lock loop (PLL) system.

Figs. 2.1a and 2.1b show, respectively, the basic block diagrams for both systems. In the PLL, the error signal is the phase difference between the input frequency variable and the output of the voltage-controlled oscillator (VCO) [8]. In contrast, the VLL has two input variables - a frequency and an amplitude signal.
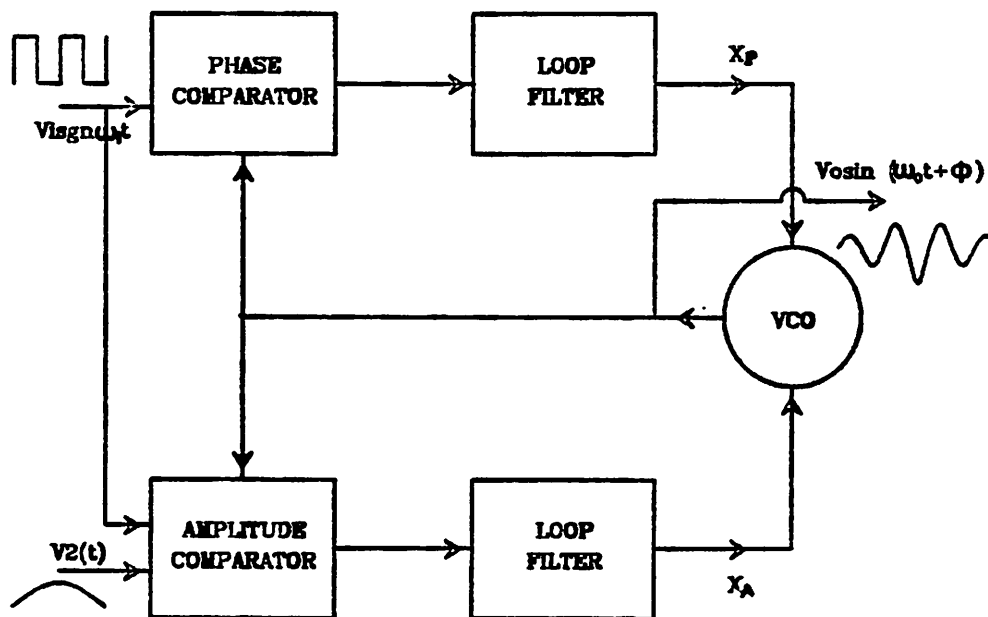
Figure 2.1a. Block Diagram of the VLL
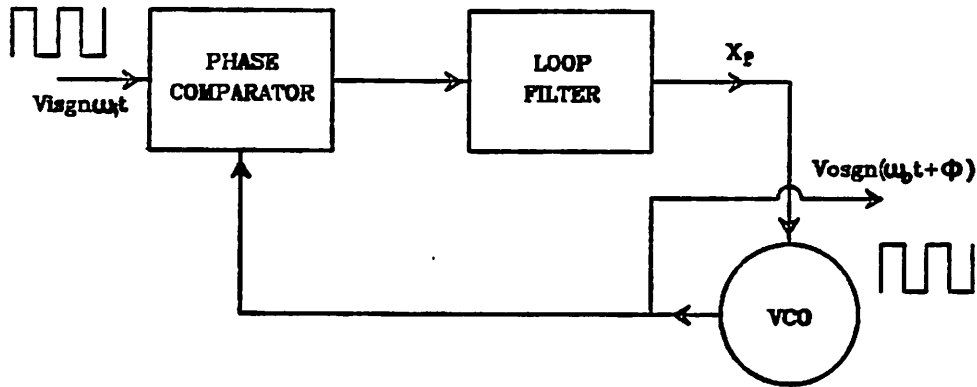
Figure 2.1b. Block Diagram of a PLL

These inputs generate two error signals - a phase difference between the frequency input variable and the VCO output (as in the PLL), and an amplitude difference between the corresponding input and the amplitude of the VCO output. This simultaneous multiplicity of feedback loops, which can be seen as the components of a vector, lead to naming the system "Vector-Lock Loop".

PLLs are often classified according to the nature of the waveforms of the input and output. When both the input and output are square waves, the system is defined as a digital PLL. In one type of digital PLL, sometimes called a sampled-data PLL, the controlling signal for the VCO has a digital format, while in another type this controlling signal is of an analog nature, i.e., a continuous voltage. When either the input or output or other waveform in which the amplitude information must be preserved are sinusoidal, the system is called analog. According to this classification the VLL belongs to the analog type.

Some analog PLL's accept analog input signals but produce a square wave output. In this case a relaxation type of VCO is often used. These oscillators are

characterized by simplicity of design, but unless special precautions are taken, their performance, in terms of phase noise and frequency stability (important parameters for the evaluation of PLL's), is poor [9].

One way to reduce the phase noise or improve the stability of the free-running frequency is to replace the relaxation type of oscillator with a high-Q harmonic oscillator. In this case the oscillating frequency is usually determined by a quartz crystal or a combination of inductance and capacitance (resonator). The definition of the amplitude is done by a mechanism which uses the peak value of the VCO's output signal to modify its loop gain. Some of the harmonic products generated by this nonlinear process are filtered out by the narrow, spectral characteristics of the oscillator. The quartz crystal is characterized by its high Q which allows a very stable oscillating frequency. On the other hand its main drawback is that it lacks the means for significantly varying the oscillation frequency. When a combination of inductance and capacitance is used, it is possible to change the resonant frequency. As in the case of the crystal oscillator, the spectral purity of the output waveform is directly related to the Q of the timing elements, and the deviation of the absolute value of the center frequency is proportional to the square root of the values of the LC product. This square root function, being a *slower* function than the direct proportionality makes the frequency definition less sensitive to spread in the component values, representing an important improvement over the case of relaxation oscillators in which the frequency is directly proportional to the element values. However the LC oscillator also has a very important shortcoming in that it poses difficulty in integrating inductors and variable capacitors on the same chip using standard, integrated circuit technology.

In the VLL, the VCO is implemented with a harmonic oscillator that does not require adding external components such as crystals or inductances. Moreover, since the amplitude is another controllable parameter, asynchronous limiters are not needed either.

2.2. The Voltage Controlled Oscillator

In a resonator (see Fig. 2.2a), both inductance and capacitance can be regarded as integrating elements. In the case of the inductor, the current is the integral of the voltage applied to it; in the case of the capacitor, the voltage is the integral of the current. Therefore a closed-loop cascade connection of two ideal integrators, as depicted in Fig. 2.2b, is an active equivalent of a second-order resonator composed of an inductance and a capacitance. Each ideal integrator has a single pole that is located at the origin of the $(\sigma, j\omega)$ plane (see Fig. 2.3). As shown in Fig. 2.4, when the loop is closed these poles split along the $j\omega$ axis to define a complex pair equivalent to an oscillating frequency $\omega_0 = \sqrt{K_1 K_2}$, where K_i represent the gain constants of the integrators. Thus two important characteristics result from the connection of these ideal elements:
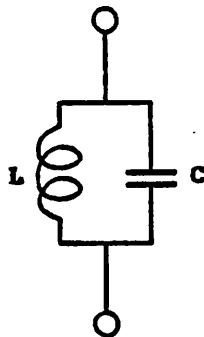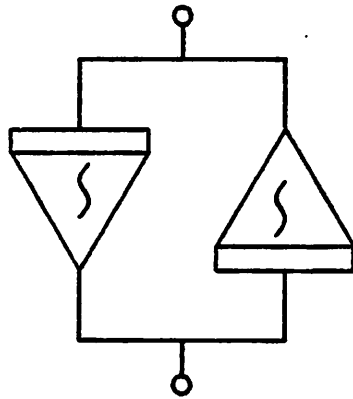

Figure 2.2a. LC Resonator

Figure 2.2b. Active Equivalent of a Resonator
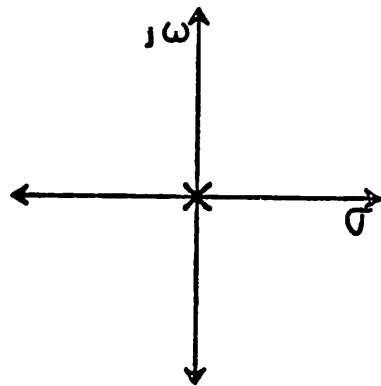
Figure 2.3. Pole Location of an Ideal Integrator
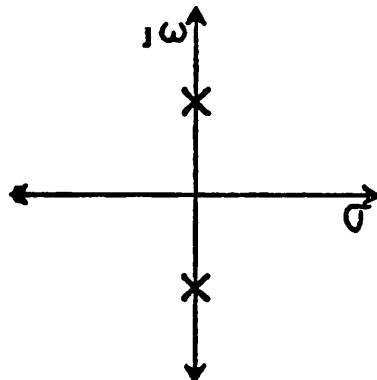
Figure 2.4. Complex Pole Pair of an Ideal Resonator

(1) The complex pair lies exactly on the $j\omega$ axis, and

(2) The natural frequency of oscillation is the geometric mean of the individual constants of each integrator, and the waveform is a sinusoid with a constant amplitude determined by the initial injection of energy into the system.

A higher Q of the resonator in a linear harmonic oscillator yields better performance in terms of phase noise, spectral purity and frequency stability [10], compared to a relaxation oscillator. The equivalent of the Q in the active implementation is the voltage gain of the integrators, hence this parameter has to be as large as possible. In the general case of real integrators, the gain constant, sometimes referred to as the time constant, has an unknown absolute value. In addition to the dominant pole (which is near but not exactly at the origin), real integrators may have other singularities almost anywhere in the complex plane. The dominant pole is not at the origin but shifted along the σ axis by an amount that is a function of the losses of the integrators. In general, this dominant pole location is in the left-half plane, which indicates that the losses are positive, but it could be that the losses are sometimes negative [7]. When the loop is closed, these non-idealities result in a complex pair that lies on the left- or right-half plane depending on the combination of all the singularities. The actual location of the pole pair can be analyzed using root-locus rules. For example, the presence of non-dominant poles on the left-half plane pushes the complex pair towards the right plane, and a real zero on the right plane has a similar effect.

A time-domain view of the behavior of the real resonator shows the following:

(1) An oscillating frequency that will depart slightly from the one expected, and

(2) An output sinusoid of exponentially growing or decaying amplitude.

Here the uncertainty of the gain constant has the same effect as an undefined value of the free-running frequency of the relaxation oscillator in a standard PLL, but the amplitude element of the VLL does not correspond to any equivalent parameter of the PLL.

In order to make the VCO of the vector lock loop system with a real resonator as described before, two controlling inputs must be available - one that controls the integrating constant, and another that controls the amplitude of the oscillation. The integrators are implemented using open-loop operational amplifiers (OPAMPs), therefore the integrating constant is approximately proportional to the reciprocal of the unity gain frequency. The unity gain frequency may be varied by changing the gain constant. The parasitic roots generally associated with OPAMPs (left half plane real poles and right half plane transmission zeros) cause an excess phase at the unity gain point on the frequency scale, so that the total phase shift at the output is greater than $\frac{\pi}{2}$.

In the $j\omega$ plane the effect of the additional phase-shift results in a shift of the complex pair toward the right side of the $j\omega$ axis. In the time domain, this shift in the location of the complex pair results in an exponentially growing sinusoidal output. Thus the second element that has to be varied is the phase shift at the unity gain frequency. This task is achieved by introducing an additional variable singularity in the transfer function of the integrators. A root locus of the actual resonator (see Fig. 2.5) describes these combined effects.

In this implementation, each operational amplifier is composed of two gain stages. The variation of the unity gain frequency is achieved by modifying the transconductance of the first stage. Regarding the phase-shift variation, the circuit has an adjustable element that creates a variable real zero in the response
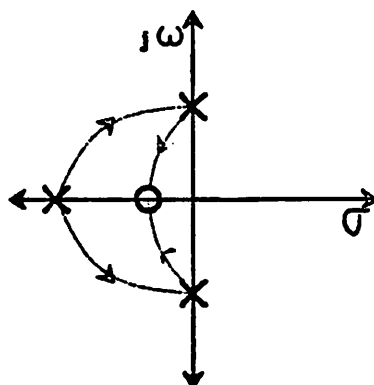
Figure 2.5. Root Locus of a Real Integrator

that cancels the effects of the transmission zero and/or non-dominant poles (The detailed circuits solutions will be shown in Chapter 4).

2.3. Description of the Comparator Functions

As is shown in Fig. 2.1a, the main role of the amplitude and phase comparators is to generate two simultaneous error signals, which are fed back into the VCO. The most important aspect of this operation is the interlocked nature of the production of these errors signals (a unique feature of the VLL). This means that the only possible steady-state condition occurs when both loops are operating correctly. For example, it is not possible to have the amplitude loop at a normal operating point without also having the frequency (or phase) in the locked condition, and vice-versa.

The analysis is done first for the simple case in which the input V_1 is assumed to be sinusoidal, then for the actual case in which V_1 is a square wave.

2.3.1. Sinusoidal Input

The block diagram shown in Fig. 2.6 will be used to describe the operation of one of the two identical comparators.

$V_1 \sin\omega_i t$ is a sinusoidal input representing the frequency variable (constant amplitude).

$\bar{V}_2(t)$ is an input representing the amplitude variable.

$\bar{V}_0 \sin(\omega_0 t + \psi)$ is the output vector.

$\bar{X}(t)$ is the error signal.

P_1 and P_2 are four quadrant multipliers.

J_1, J_2, J_3 are phase shifters of φ_i amount.

$k\Sigma$ is a linear summer with a scaling factor K.

The block diagram depicted in Fig. 2.6 shows the error signal $\bar{X}(t)$ to be:
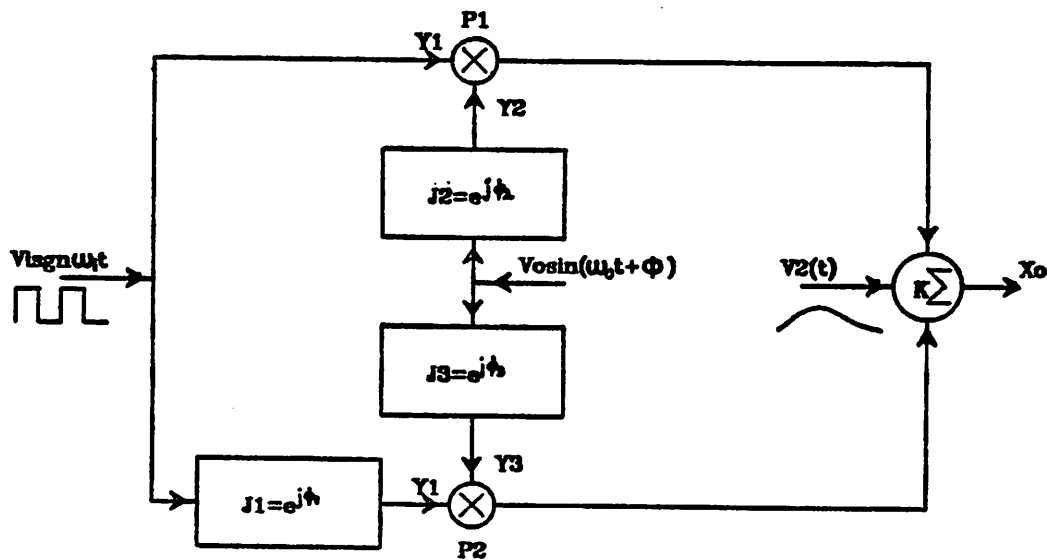
Figure 2.6. Phase or Amplitude Comparator

$$\bar{X}(t)= V_1\sin(\omega_i t)\times \bar{V}_0\sin(\omega_0 t +\psi+\varphi_2)+ V_1\sin(\omega_i t +\varphi_1)\times \bar{V}_0\sin(\omega_0 t +\psi+\varphi_3)+k\,\bar{V}_2 \quad (2.1)$$

Proper choice of the values for φ_i and k yields either a phase or amplitude comparator, as follows:

(a) *Phase comparator:* $\varphi_1= \dfrac{\pi}{2}$, $\varphi_2=0$, $\varphi_3= \dfrac{\pi}{2}$, $k=0$.

$$\bar{X}_P(t)= V_1\,\bar{V}_0\cos((\omega_0-\omega_i)t +\psi) \quad (2.2)$$

(b) *Amplitude comparator:* $\varphi_1= \dfrac{\pi}{2}$, $\varphi_2=- \dfrac{\pi}{2}$, $\varphi_3=0$, $k=K$.

$$\bar{X}_A(t)= V_1\,\bar{V}_0\sin((\omega_0-\omega_1)t +\psi)+K\bar{V}_2 \quad (2.3)$$

If the system is in synchronism, then $\omega_1=\omega_0$. Substituting this condition in equations (2) and (3) gives:

$$\begin{aligned} \bar{X}_{P_0}&= V_1\,\bar{V}_0\cos\psi \\ \bar{X}_{A_0}&= V_1\,\bar{V}_0\sin\psi+K\bar{V}_2 \end{aligned} \quad (2.4)$$

Equations (2.4) describe the behavior of the system for small input variations. The steady-state condition is achieved when both $\bar{X}_P(t)=0$ and $\bar{X}_A(t)=0$. By introducing this condition into (2.4), a simultaneous set of two equations can be obtained:

$$\begin{aligned} V_1 V_{0s}\sin\psi_s +K\bar{V}_2&=0 \\ V_1 V_{0s}\cos\psi_s &=0 \end{aligned} \quad (2.5)$$

The solution is:

$$V_{0s} =- \frac{K\bar{V}_2}{V_1}; \quad \psi_s= \frac{\pi}{2} \quad (2.6)$$

It is important to analyze the interaction between $\bar{X}_P(t)$ and $\bar{X}_A(t)$ for the steady-state values found for V_{0s} and ψ_s:

$$\frac{\partial \bar{X}_P(t)}{\partial \bar{V}_0}\bigg|_{\psi_s= \frac{\pi}{2},\ V_{0s}=- \frac{K\bar{V}_2}{V_1}} =V_1\cos\psi_s =0 \quad (2.7)$$

$$\left.\frac{\partial \overline{X}_P(t)}{\partial \psi}\right|_{\psi_s = \frac{\pi}{2}, V_{0s} = -\frac{K\overline{V}_2}{V_1}} = V_1 \overline{V}_{0s}(-\sin\psi_s) = K\overline{V}_2 \tag{2.8}$$

$$\left.\frac{\partial \overline{X}_A(t)}{\partial \overline{V}_0}\right|_{\psi_s = \frac{\pi}{2}, V_{0s} = -\frac{K\overline{V}_2}{V_1}} = V_1 \sin\psi_s = V_1 \tag{2.9}$$

$$\left.\frac{\partial \overline{X}_A(t)}{\partial \psi}\right|_{\psi_s = \frac{\pi}{2}, V_{0s} = -\frac{K\overline{V}_2}{V_1}} = V_1 \overline{V}_0 \cos\psi_s = 0 \tag{2.10}$$

Equations (2.7) through (2.10) represent the small signal gain of each of the comparators with respect to both error signals. The zero values found for $\overline{X}_P(t)$ with respect to $\overline{V}_0$ [equation (2.7)], and $\overline{X}_A(t)$ with respect to ψ [equation (2.10)], indicate the orthogonality between those variables. This implies a great deal of simplification in the calculation of some of the elements of the system, in particular the loop filters as will be shown later.

An interesting aspect of equations 2.4 is that there are no higher harmonic products at the outputs of the comparators. Note that no simplification was done on their derivation. This represents an advantage over the case in which a single multiplier is used as a comparator, yielding an undesired component at twice the fundamental frequency. In other words, if V_1 is sinusoidal, and P_1 and P_2 are four quadrant multipliers, there are no higher harmonic components in the error signals, which implies that there is no need for loop filters.

2.3.2. Square Wave Input

Here the block diagram depicted in Fig. 2.6 still applies, but with the following differences:

$V_1 \sin\omega_i t$ is replaced by a square wave input frequency variable $V_1 \text{sgn}\omega_i t$

P_1 and P_2 are sign multipliers, each with output $Y_0 = B(Y_1 \times sgn(Y_2))$ where B is a constant.

As in the sinusoidal case, the error signal is calculated as follows:

$$\bar{X}(t)=B[\bar{V}_0\sin(\omega_0 t+\psi+\varphi_2)\times\mathrm{sgn}\omega_i t+\bar{V}_0\sin(\omega_0 t+\psi+\varphi_3)\times\mathrm{sgn}(\omega_i t+\varphi_1)]+k\bar{V}_2 \quad (2.11)$$

The Fourier expansion of the *sgn* function of the input is given by:

$$X_1(t)=\mathrm{sgn}(\omega_i t)=\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin(2n+1)\omega_i t \quad (2.12)$$

Equation (2.12) is substituted in (2.11), and after some trigonometric manipulation we have:

$$\bar{X}(t)=\frac{4BV_0}{\pi}\sum_{n=0}^{\infty}\frac{1}{2(2n+1)}\{\ \cos[(\omega_0-(2n+1)\omega_i)t+\psi+\varphi_2]$$
$$-\cos[(\omega_0+(2n+1)\omega_i)t+\psi+\varphi_2] \quad (2.13)$$
$$+\cos[(\omega_0-(2n+1)\omega_i)t+\psi+\varphi_3-(2n+1)\varphi_1]$$
$$-\cos[(\omega_0+(2n+1)\omega_i)t+\psi+\varphi_3+(2n+1)\varphi_1]\}+k\bar{V}_2$$

Assuming that the system is in synchronism, then $\omega_0=\omega_1$, and just as in the sinusoidal case, the selection of the values for φ_i yields either a phase or amplitude comparator.

(a) *Phase comparator:* $\varphi_1=\frac{\pi}{2}$, $\varphi_2=0$, $\varphi_3=\frac{\pi}{2}$, $k=0$.

$$\bar{X}_P(t)=\frac{4BV_0}{\pi}\sum_{n=0}^{\infty}\frac{1}{2(2n+1)}[\ \cos(-2n\omega_i t+\psi)$$
$$+\cos(-2n\omega_i t+\psi-n\pi) \quad (2.14)$$
$$-\cos(2(n+1)\omega_i t+\psi)$$
$$-\cos(2(n+1)\omega_i t+\psi+(n+1)\pi)]$$

The first five terms of the expansion are:

$$\bar{X}_P(t)=\frac{4BV_0}{\pi}[\ \cos\psi-\frac{1}{3}\cos(4\omega_i t+\psi)+\frac{1}{5}\cos(-4\omega_i t+\psi)$$
$$-\frac{1}{7}\cos(8\omega_i t+\psi)+\frac{1}{9}\cos(-8\omega_i t+\psi)+\ldots\ ] \quad (2.15)$$

(b) *Amplitude comparator:* $\varphi_1=\frac{\pi}{2}$, $\varphi_2=-\frac{\pi}{2}$, $\varphi_3=0$, $k=K$.

$$\overline{X}_A(t) = \frac{4BV_0}{\pi} \sum_{n=0}^{\infty} \frac{1}{2(2n+1)} [\; \cos(-2n\,\omega_i t + \psi - \frac{\pi}{2})$$

$$+ \cos(-2n\,\omega_i t + \psi - (2n+1)\frac{\pi}{2})$$

$$- \cos(2(n+1)\omega_i t + \psi - \frac{\pi}{2})$$

$$- \cos(2(n+1)\omega_i t + \psi + (2n+1)\frac{\pi}{2})] + K\overline{V}_2 \qquad (2.16)$$

which leads to the expansion:

$$\overline{X}_A(t) = \frac{4BV_0}{\pi} [\; \sin\psi - \frac{1}{3}\sin(4\omega_i t + \psi) + \frac{1}{5}\sin(-4\omega_i t + \psi)$$

$$- \frac{1}{7}\sin(8\omega_i t + \psi) + \frac{1}{9}\sin(-8\omega_i t + \psi) + \ldots] + K\overline{V}_2 \qquad (2.17)$$

As in the sinusoidal case, the steady-state condition is achieved when both $\overline{X}_P(t)=0$ and $\overline{X}_A(t)=0$. Introducing this condition into (2.15) and (2.17) yields the following simultaneous set of two equations (DC terms only):

$$\frac{4BV_{0s}}{\pi}\sin\psi_s + K\overline{V}_2 = 0$$

$$\frac{4BV_{0s}}{\pi}\cos\psi_s = 0$$

The solution is:

$$V_{0s} = -\frac{K\pi\overline{V}_2}{4B}; \quad \psi_s = \frac{\pi}{2} \qquad (2.18)$$

Replacing the values of equation (2.18) back into expressions (2.15) and (2.17) yields the following, final, steady-state Fourier expansion for both error signals $\overline{X}_P(t)$ and $\overline{X}_A(t)$:

$$\overline{X}_{Ps}(t) = K\overline{V}_2 \sum_{n=0}^{\infty} (\; \frac{1}{4n-1} + \frac{1}{4n+1})\sin 4n\,\omega_i t$$

$$\overline{X}_{As}(t) = K\overline{V}_2 \sum_{n=0}^{\infty} (\; \frac{1}{4n-1} - \frac{1}{4n+1})\cos 4n\,\omega_i t \qquad (2.19)$$

Equations (2.19) show the presence of harmonics that are multiples of $4\omega_i$. Regarding the requirements of the loop filters, this implies an improvement over those comparators that deliver second harmonic products.

The initial assumption that there is no DC component at the output of the VCO is not very realistic. For most actual systems there are voltage offsets that introduce the equivalent of a DC component in $\overline{V}_0$. As can be seen after multiplying expression (2.12) by a constant, this results in the presence of not only the fundamental frequency, but also a chain of harmonics.

CHAPTER 3

DEFINITION OF THE SYSTEM PARAMETERS

Circuits such as waveform generators, filters, modulators/demodulators, etc.,based upon discrete component technologies are characterized by their ability to operate at frequencies ranging from a few hundred kilohertz to several megahertz. Presently, for reasons related to circuit design or technology limitations, VLLs cannot cover the same wide spectrum of frequencies. Thus, here the design objectives are directed towards a VLL of limited bandwidth.

In this chapter parameters such as the free running frequency of the VCO, the maximum frequency deviation, the gain of the loops, the loop filters and noise performance are analyzed; the details of the circuit design at the transistor level are left for the next chapter.

3.1. The Intermediate Frequency Channel

The VLL under study here was designed to be used for the circuits associated with the intermediate frequency (IF) channel of superheterodyne amplitude modulation (AM) radios. The architecture of this type of receiver, which was originally developed in the early 1930s, is depicted in Fig. 3.1. The signal from the antenna is applied to a tunable band-pass filter and further amplified by a variable gain radio-frequency (RF) amplifier. At the output of this amplifier there is another band-pass filter identical to the first one. Both filters have their tuning capacitors mechanically coupled to track over the whole frequency spectrum. This band-limited output signal is multiplied (or *mixed*) by the signal generated by the local oscillator, whose resonator also has its variable capacitor in tandem with the ones corresponding to the band-pass filters. The modulation products

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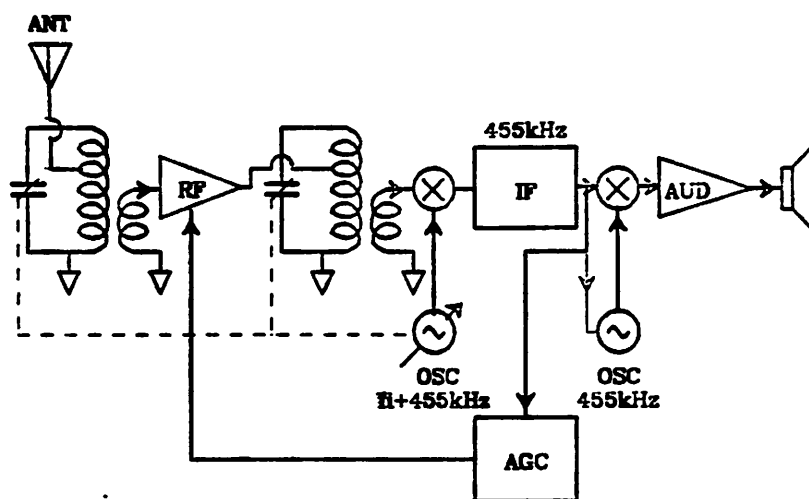
Figure 3.1. Single-Conversion Receiver

are injected into the intermediate channel network (IF) which consists of fixed band-pass filters and variable gain amplifiers. The IF output is further demodulated by another mixer or product detector, but using a signal that is synchronous with the IF carrier. In more economical receivers the IF output is demodulated by simple rectification or peak detection. The demodulated signal is also processed by a low-frequency low-pass filter that provides a DC voltage proportional to the amplitude of the carrier or audio output that is to be used to control the gain of the amplifiers (AGC). In this simple configuration there are two frequency conversion processes including the final signal demodulation, but it is customary to call this system a single conversion receiver.

For medium-wave broadcasting receivers this configuration works quite well, and is still widely used. But some problems arise when the range of frequency bands desired is above a few megahertz (HF):

(1) *Image rejection*

If the input signal frequency is f_I, and the local-oscillator frequency f_0, two primary components are generated in the first conversion process:

$$f_1 = f_0 - f_I$$
$$f_2 = f_0 + f_I$$
(3.1)

generally the intermediate frequency f_{IF} is assumed to be f_1. But an input signal of a frequency $f_I + 2f_{IF}$, defined as the image frequency that is not rejected by the input filters, also generates f_{IF} after the conversion process. The following numerical example illustrates this effect:

If $f_I = 1MHz$ and $f_{IF} = 455kHz$ (which is a value commonly used for commercial AM radios) then $f_0 = 1.455MHz$. Therefore the image frequency of $1.91MHz$ when mixed with the local oscillator signal gives a component at $455kHz$. But if each band-pass filter has a $Q = 50$, the relative rejection at this image frequency is $>80dB$ (for $40\frac{dB}{dec}$ of attenuation). If $f_I = 30MHz$, then the image frequency is located at $30.91MHz$. Band-pass filters at this center frequency with a $Q = 50$ only provide a rejection of $24dB$, which is unacceptable.

(2) *Local oscillator tracking*

The non-linear relationship between the resonator capacitance and the oscillation frequency ($\omega_0 = (LC)^{-\frac{1}{2}}$) complicates the implementation of the constant frequency offset needed between the local oscillator frequency and the input signal. A commonly used solution for this is to combine fixed capacitors with the variable one of the local oscillator in order to achieve optimum tracking at different points of the the band spectrum. An example of this is the three point adjustment (see Fig. 3.2). Another approach is to shape the geometry of the plates of the variable capacitor in order to linearize the rela-
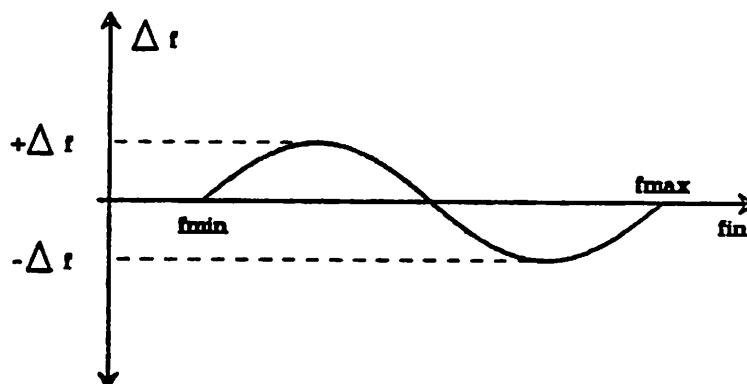
Figure 3.2. Three-Point Tracking Adjustment

tionship between the angle position of the capacitor-tandem and the frequency. None of these solutions are completely satisfactory, and the tracking problem becomes more critical as the Q of the front-end filter increases and also as the relative *distance* between f_0 and f_I decreases, conflicting with the image rejection performance.

(3) *Local Oscillator Stability*

As the input frequency increases, so does the local oscillator frequency. If the relative frequency stability performance for the oscillator is constant, the absolute offset between f_I and f_0 degrades as the frequency of operation increases, pushing the signal out of the pass-band of the IF filter. Careful selection of the resonator components in terms of temperature coefficients helps to improve the short and long term stability, but other effects such as component aging and power supply variations present a more difficult problem to solve. Frequency synthesis is a solution that is becoming more popular in the last few years because of the availability of dedicated LSI circuits.

A solution to improve the image rejection performance in high frequency receivers consists in raising the value of the IF frequency. But then the design of the IF filter becomes more complicated because the absolute selectivity is reduced, assuming that the elements have the same quality factor Q. The compromise between all these variables dictates using multiple conversion schemes, that is, having more than one IF along the signal path.

Different system configurations evolved for multiple conversion receivers in which each scheme maximized the possibilities of the relative state of the art in circuitry design.

(1) Fig. 3.3a shows the configuration of a primitive double conversion receiver. Values commonly used are $1.6MHz$ for the first IF and $100kHz$ for the second. A configuration like this one gives satisfactory performance in terms of image rejection, but since it has its variable local oscillator operating at a
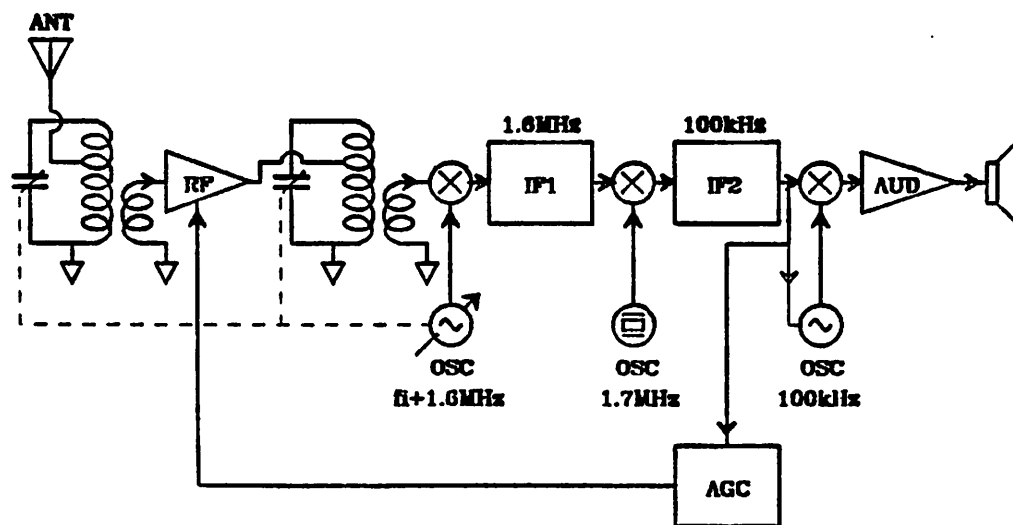
Figure 3.3a. Double-Conversion Receiver

frequency close to the input signal, its design with respect to stability remains critical.

(2) Fig. 3.3b depicts a configuration that attacks both the problems of image rejection and high frequency stability. The first conversion is done with a fixed crystal oscillator that provides excellent short and long term stability. Hence the tuning is done in the first IF stage, which because of operating at a lower frequency range than the input signal has better absolute stability performance. But this configuration does not solve the tracking problem, in fact it further complicates the matter because it requires simultaneously tuning the IF and the high frequency front-end filter. Separate tuning knobs for the IF and the front-end filter are sometimes used, but they represent a more complicated operation of the equipment.
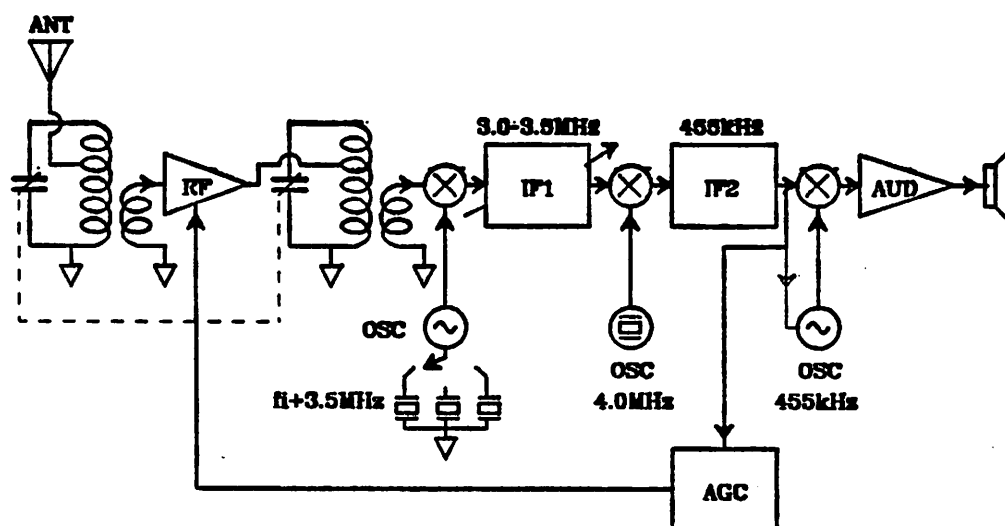
Figure 3.3b. Double-Conversion Receiver

(3) Finally, the scheme depicted in Fig. 3.3c solves all the problems of image rejection, tracking and local oscillator stability. The front-end filter is now a fixed broad-band band-pass filter that covers all the operating frequencies of the receiver. The local oscillator is a frequency synthesizer derived from a crystal reference, and the first IF operates at a very high frequency (in the order of $80MHz$ for a HF receiver). The subsequent conversions are implemented by fixed crystal oscillators.

In conclusion, the three different schemes shown need band-pass filters, demodulators, etc., operating in a frequency range from $100kHz$ to $500kHz$. Integrated versions of these networks will certainly alleviate the system design stages as well as cut costs, and the research time invested will lead to future extensions of these new schemes.
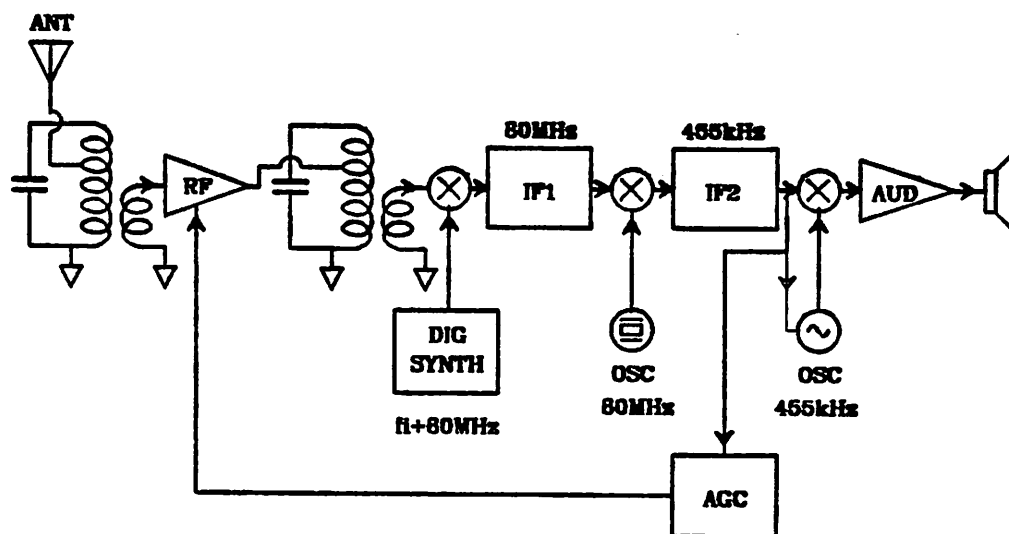
Figure 3.3c. Double-Conversion Receiver

3.2. VCO Parameters

Since NMOS is the technology used to implement this device, it is quite obvious that in order to define a continuous time constant using only the internal components provided by the process, two types of elements are needed: a capacitor and a resistor. For the first type, the trivial choice is the MOS capacitor, while for the second type several impedances can be devised, such as a channel resistor, a polysilicon resistor, and a combination of a threshold voltage and a current. But the need for a linear harmonic oscillator rules out the latter because of its inherent nonlinear nature. Moreover since the time constant has to be variable, the resistance has to be adjustable, eliminating the possibility of using fixed resistors, such as polysilicon ones for example. Another option is to use a variable capacitor such as a depletion capacitor, but this has a severe nonlinear behavior and also requires that one of the terminals always be grounded (substrate). Using a MOS capacitor is no solution either because unless special processing steps are taken, the variation range is not very large.

In characterizing a VCO, two very important parameters are the center frequency *definition* and the frequency *stability*. The first parameter defines the degree of uncertainity in assessing the absolute value of the free running frequency (FRF), whereas the second parameter defines how well the frequency is kept over environmental changes, i.e., changes in temperature, power supply, component aging, etc. In the approach presented here, the definition of the time constant is the product of two elements of completely different nature (resistance and capacitance), therefore there are no global cancellation properties that circuits using ratioed elements enjoy (e.g. switched capacitors). In the case of switched-capacitor networks, the time constant is defined by a ratio of the same type of physical quantities (capacitance) and the system clock (which has

very accurate absolute value). In other words, in order to get a well defined time constant, it is necessary to be able to accurately define the capacitor and the resistor independently. Another way to solve the problem, which is a more appropriate way to deal with *de facto* implementations such as ours, is to analyze the maximum frequency uncertainty and temperature variation, and make sure that the maximum deviation of the VCO is large enough to cover with a large margin such a spread plus the absolute tuning range desired.

By computing the sum of the uncertainty in the definition of the initial value of the resistance, which can be as high as 50%, the temperature caused deviation, 35% (analyzed in the next chapter), and the desired value of the modulation index, e.g. 15%, we extract the minimum deviation range of the VCO: ≈2:1.

3.3. Comparator Parameters

As was previously stated, the comparators are four quadrant sign multipliers [equation (2.11)]. In other words, the the square wave input is the reference signal or clock. Thus the amplitude may be as large as the total supply voltage. For the sinusoidal input, or the signal of the VCO, the amplitude is much smaller. This consideration is fundamental for the design of the circuit. Another important issue is that in order to avoid additional phase shift, the bandwidth of this circuit has to be considerably larger than the maximum operating frequency of the VCO.

Because of the particular circuit design possibilities given by the technology, the gain constant of the comparators has the dimension of a transconductance, but since the loop filters have the dimension of a trans-admittance, the combined output is dimensionless. This consideration slightly changes the format of the standard equations that define the basic stability parameters of the amplitude and phase loops.

3.4. Loop Filter Parameters

The steady-state error in a PLL as a function of frequency is given by:

$$1-H(s) = \frac{s}{s+KF(s)} \qquad (3.2)$$

where K is the product of the gain constants of the VCO (K_{VCO}) and phase comparator (K_C) and $F(s)$ is the frequency response of the loop filter. The theoretical minimum of this error occurs when the loop filter is removed ($F(s)=1$) and $K=K_{VCO}K_C \rightarrow \infty$. This condition is usually defined as a first order loop. Nevertheless, because of noise immunity considerations [see equation (3.45)], it is recommended to limit the bandwidth of the loop. If the band-limiting filter has a single real pole (with or without a zero), the system is known as a second order loop.

Both the phase and amplitude loops of the VCO perform integration operations. In the case of the phase loop the condition is well known: $\varphi_0 = K_{VCO} \int \overline{X}(t) \, dt$, where φ_0 is the phase at the output of the VCO; while the output amplitude $u(t)$ changes according to: $u(t) = U_{pk}(1 + \int -\omega_0 \rho(t) dt)$ or $\frac{\Delta u(t)}{U_{pk}} = -\int \omega_0 \rho(t) dt$ where U_{pk} is the normalized steady-state amplitude of the VCO, ω_0 the angular center frequency, and $\rho(t)$ the internal damping factor of the VCO. The double integration effect of the loop filters and the VCO requires that the loop filter have a real zero ($\frac{1}{\tau_z}$) in addition to a real pole ($\frac{1}{\tau_p}$) in order to achieve a phase shift less than π at the unity gain frequency. This type of arrangement gives the possibility of choosing independently the natural angular frequency of the loop (ω_n) and the overall loop damping factor (ζ). In this case, the open-loop transfer function of the loop is:

$$F(s) = \frac{1+s\tau_z}{s\tau_p} \qquad (3.3)$$

which gives a closed-loop error function equal to:

$$1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.4}$$

$$= \frac{s^2}{D(s)}$$

For this type of filter the characteristic parameters of the loop are given by:

$$\omega_n^2 = \frac{K}{\tau_p}$$

$$2\zeta\omega_n = \frac{K\tau_z}{\tau_p} \tag{3.5}$$

The parameters ζ and ω_n are the damping factor and natural frequency of the loop composed of the VCO and the phase and amplitude comparators. Equations (3.5) are all the necessary formulae for designing the loop filters. The following is a typical design procedure: once the circuit is defined, the constant K can be extracted. Given the desired ω_n and ζ or the equivalent phase margin, the constants τ_p and τ_z are calculated.

As a note to avoid confusion, the damping factor ζ and angular frequency ω_n are parameters for the whole loop, while ρ and ω_0 are only for the VCO.

In the next chapter all the detailed calculations are carried out using the parameters extracted from the circuit configurations.

3.5. Noise Considerations

The combined signal present at the output of the VLL resonator (sine wave plus noise) can be written as:

$$
\begin{aligned}
x_c(t) &= V_{pk} + n(t) \\
&= V_{pk} + n_1(t)\cos(\omega_0 t + \varphi) + n_2(t)\sin(\omega_0 t + \varphi)
\end{aligned} \tag{3.6a}
$$

where $n_1(t)$ and $n_2(t)$ are the two independent Gaussian random processes, V_{pk} the peak amplitude of the output sine wave, and ω_0 the angular frequency of resonance of the VCO. Equation (3.6a) can be pictured as the sum of two vectors, one representing the sine wave of amplitude (with zero phase) V_{pk} (see Fig. 3.4), and

another randomly rotating vector representing the noise fluctuations.

A shorter form of expressing equation (3.6a) is:

$$x_c(t) = [V_{pk} + n(t)]\cos[\omega_0 t + \psi + \varphi(t)] \qquad (3.6b)$$

where $n(t) = \sqrt{n_1^2(t) + n_2^2(t)}$ and $\varphi(t) = -\tan^{-1}\dfrac{n_2(t)}{n_1(t)}$. Given the mathematical

constructions of $\varphi(t)$ and $n(t)$, their distributions are *rectangular* and Raleygh respectively [11].

The object of this study is to analyze the spectral characteristics of expression (3.6b) first assuming that the VCO is acting independently, that is, the phase and amplitude loops of the VLL are open, then including the *cleaning* effects of the VLL action on the VCO signal.

The VCO power spectrum resulting from the superposition of white additive noise of power density N_O [$\sqrt{N_O}$ is the long term root-mean-square (*rms*) amplitude of $n(t)$] is equally divided into two components [12]:

(1) A *phase* noise power density (*phase jitter* component) equal to:

$$N_{OP} = \frac{N_O}{2} \qquad (3.7a)$$

(2) An *amplitude* noise power density equal to:

$$N_{OA} = \frac{N_O}{2} \qquad (3.7b)$$

Once the total power spectrum of the VCO is found, equations (3.7a) and (3.7b) are used to find each of the components.

3.5.1. Noise Bandwidth of the Harmonic VCO

Fig. 3.5 shows the VCO in which uncorrelated noise sources have been included at the inputs of each integrator. These lumped sources are the referred input noise of the integrators that are calculated according to the internal characteristics of the circuit. (This calculation will be carried out in Chapter 4

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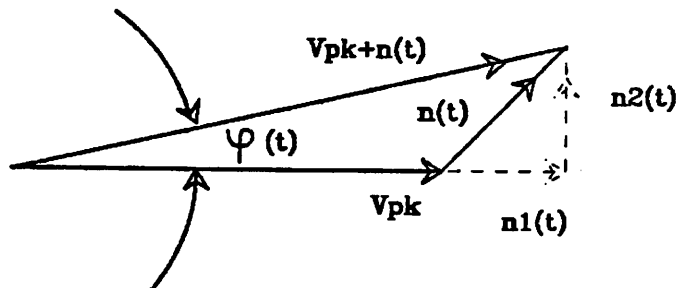
Figure 3.4. Vector Composition of Phase Noise
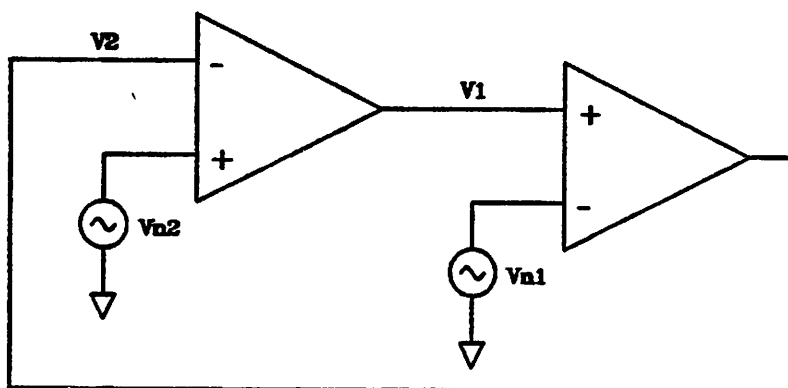
Figure 3.5. VCO with Noise Inputs

for the flicker and thermal components). Since the frequency of operation of the VCO ($\approx 455kHz$) is much larger than the corner frequency of the flicker component, the noise bandwidth calculation is greatly simplified by assuming that the power spectrum of the noise sources is flat.

Under the initial assumption that the signals v_{N1} and v_{N2} are nonrandom, the following relationships are extracted from Fig. 3.5:

$$v_2(s) = [v_1(s) - v_{N1}(s)]h_o(s)$$
$$v_1(s) = [-v_2(s) + v_{N2}(s)]h_o(s)$$

(3.8)

where $h_o(s)$ is the transfer function of the real integrators given in Chapter 4 as:

$$h_o(s) = k\frac{s\tau_1+1}{s\tau_2+1}$$

(4.39)

The output at one of the integrators is obtained by combining equations (3.8):

$$v_o(s) = v_2(s) = \frac{h_o(s)^2}{1+h_o(s)^2}v_{N2}(s) - \frac{h_o(s)}{1+h_o(s)^2}v_{N1}(s)$$

(3.9)

Combining equations (3.9) and (4.39) and making $s = j\omega$ we obtain:

$$v_o(\omega) = \frac{k^2\left[\dfrac{j\omega\tau_1+1}{j\omega\tau_2+1}\right]^2 v_{N2}(\omega)}{1+k^2\left[\dfrac{j\omega\tau_1+1}{j\omega\tau_2+1}\right]^2} - \frac{k\left[\dfrac{j\omega\tau_1+1}{j\omega\tau_2+1}\right]v_{N1}(\omega)}{1+k^2\left[\dfrac{j\omega\tau_1+1}{j\omega\tau_2+1}\right]^2}$$

(3.10a)

which can be written as:

$$v_o(\omega) = \frac{k}{\tau_2^2+k^2\tau_1^2}\left[\frac{k\dfrac{(j\omega\tau_1+1)^2}{2j\omega\omega_0\rho}v_{N2}(\omega)}{1+j\dfrac{\omega^2-\omega_0^2}{2\omega\omega_0\rho}} - \frac{\dfrac{(j\omega\tau_1+1)(j\omega\tau_2+1)}{2j\omega\omega_0\rho}v_{N1}(\omega)}{1+j\dfrac{\omega^2-\omega_0^2}{2\omega\omega_0\rho}}\right]$$

(3.10b)

where ω_0 and ρ are given by (see Chapter 4):

$$\omega_0 = \left[\frac{1+k^2}{\tau_2^2+k^2\tau_1^2}\right]^{1/2}$$

$$\rho = \frac{1}{\sqrt{1+k^2}}\frac{\tau_2+k^2\tau_1}{\sqrt{\tau_2^2+k^2\tau_1^2}}$$

(4.42)

By making $\Delta\omega = \omega - \omega_0$ and assuming that $\Delta\omega \ll \omega_0$ and $\tau_1 \approx 0$, equation (3.10b) becomes:

$$v_o(\omega) \approx \frac{1}{2}k\left[\frac{v_{N2}(\omega)}{1+j\dfrac{\Delta\omega}{2\omega_0\rho}} - \frac{v_{N1}(\omega)}{1+j\dfrac{\Delta\omega}{2\omega_0\rho}}\right]$$

(3.11)

which is equivalent to:

$$v_o(f) \approx \frac{1}{2}k\left[\frac{v_{N2}(f)}{1+j\dfrac{\Delta f}{2\rho f_0}} - \frac{v_{N1}(f)}{1+j\dfrac{\Delta f}{2\rho f_0}}\right]$$

(3.12)

The modulus of the left side is less than or equal to the sum of the modulus of each of the terms on the right side:

$$|v_o(f)| \leq \frac{1}{2}k\left[\left(\frac{v_{N2}(f)}{1+(\frac{\Delta f}{2\rho f_0})^2}\right)^{\frac{1}{2}} + \left(\frac{v_{N1}(f)}{1+(\frac{\Delta f}{2\rho f_0})^2}\right)^{\frac{1}{2}}\right] \quad (3.13)$$

Considering again that both v_{N1} and v_{N2} are white noise random sources of equal power contents $((v_{N1})^2=(v_{N1})^2\equiv(V_N)^2)$, the output noise power V_{on}^2 is therefore given by:

$$\begin{aligned}
V_{on}^2 &= \int_{-\infty}^{+\infty} |v_o(f)|^2 df = \frac{1}{4}\times 2k^2\times 2\int_0^{+\infty} \frac{(V_N)^2}{1+(\frac{\Delta f}{2\rho f_0})^2} df \\
&= k^2 V_N^2 2\rho f_0 \left[\tan^{-1}(\frac{\Delta f}{2\rho f_0})\right]_0^\infty \\
&= k^2 V_N^2 \pi\rho f_0 = k^2 V_N^2 \frac{\pi}{2}\frac{1}{Q}f_0 \\
&= k^2 V_N^2 \frac{\pi}{2}\Omega
\end{aligned} \quad (3.14)$$

where Ω is the $3dB$ bandwidth of the resonator. In order to find the effective noise bandwidth Ω', V_{on}^2 has to be divided by the power gain of the resonator circuit, that is k^2, thus:

$$\Omega' = \frac{V_{on}^2}{k^2 V_N^2} = \pi\rho f_0 = \frac{\pi}{2}\frac{f_0}{Q} \quad (3.15)$$

Equation (3.15) implies that the effective noise bandwidth is $\frac{\pi}{2}$ times larger than the $3dB$ bandwidth (Ω).

3.5.2. Noise Power Density of the VCO

If $P\approx\frac{V_{pk}^2}{2}$ is the total VCO output power, the output noise density is given by:

$$N_O = \frac{P}{k^2\frac{\pi}{2}\Omega} \quad (3.16)$$

The noise input power is $=\frac{\pi}{2}\Omega\times 2V_N^2$, thus the power gain is:

$$A_P = \frac{P}{\frac{\pi}{2}\Omega \times 2 V_N^2} \tag{3.17}$$

The power gain can also be extracted from equation (3.13):

$$A_P = \frac{k^2}{1+(\frac{\Delta f}{2\rho f_0})^2} \tag{3.18}$$

After combining equations (3.16), (3.17) and (3.18) the noise density-to-carrier ratio is obtained:

$$S_{\vartheta} = \frac{N_0}{P} = 4\frac{V_N^2}{V_{pk}^2}\frac{1}{1+(\frac{\Delta f}{2\rho f_0})^2} \tag{3.19}$$

To simplify the notation $\Delta f \equiv f$, and for frequencies far from the resonance point, we have that $(\frac{\Delta f}{2\rho f_0})^2 \gg 1$, thus equation (3.19) can be written as:

$$\begin{aligned} S_{\vartheta} = \frac{N_0}{P} &\approx 4\frac{V_N^2}{V_{pk}^2}(\frac{2\rho f_0}{f})^2 \\ &= 4\frac{V_N^2}{V_{pk}^2}\frac{1}{Q^2}(\frac{f_0}{f})^2 \end{aligned} \tag{3.20}$$

Now the results of equation (3.7a) and (3.7b) are used to find the noise density-to-carrier ratio of the phase and amplitude components.

$$S_{\vartheta_{OP}} = \frac{N_{OP}}{P} = 2\frac{V_N^2}{V_{pk}^2}\frac{1}{Q^2}(\frac{f_0}{f})^2 \tag{3.21}$$

$$S_{\vartheta_{OA}} = \frac{N_{OA}}{P} = 2\frac{V_N^2}{V_{pk}^2}\frac{1}{Q^2}(\frac{f_0}{f})^2 \tag{3.22}$$

In conclusion, the oscillator's phase and amplitude noise densities are of the form $\frac{\beta}{f^2}$ in the range where the referred input noise is considered to have a Gaussian uniform spectrum of value β, where β is a constant expressed in $\frac{V^2}{Hz}$. However at lower frequencies the intermodulation of the flicker noise with the carrier gives a frequency dependence of the type $\frac{\alpha}{f^3}$ [13].

Fig. 3.7 depicts the details of the model for an input-referred noise with an input spectrum such as shown in Fig. 3.6, summarizing the decrease of $S_\varphi(\omega)$ as
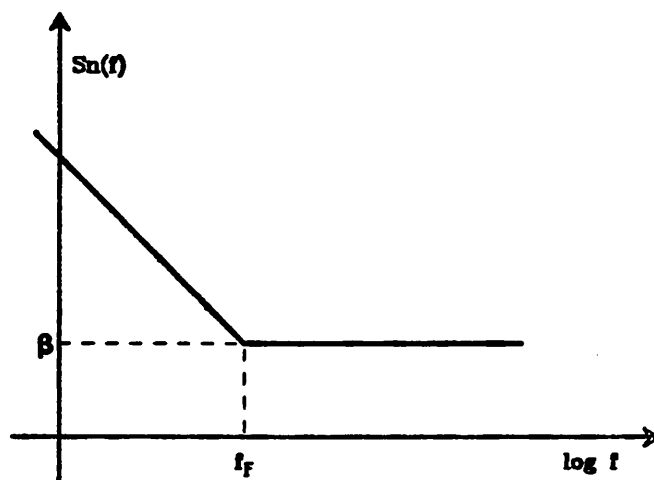

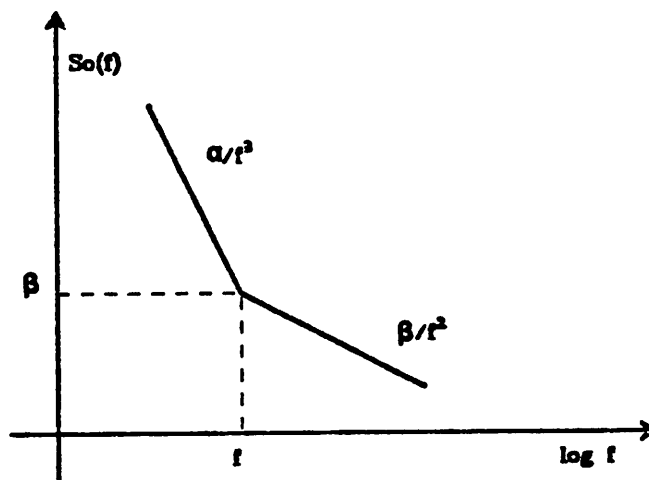**Figure 3.6.** Spectral Distribution of the Integrator Input Noise

Figure 3.7. Noise Density Distribution of the VCO

follows:

(a) At $30\dfrac{dB}{dec}$ up to the corner frequency of the $\dfrac{1}{f}$ component.

(b) At $20\dfrac{dB}{dec}$ from the previous breakpoint.

3.5.3. Integrated Noise Power of the VCO

Given the spectral characteristics of the noise densities of the phase and amplitude components of the VCO, the total noise power $\chi^2_{\vartheta_{OP}}$ over the frequency band $-BW$ to BW is given by the integral of the function depicted in Fig. 3.7 (the subindex ϑ_{OP} indicates that the VCO is operating in open loop, as opposed to the case in which the phase (and amplitude) comparator are connected, defined as $\chi^2_{\vartheta_P}$.

$$\chi^2_{\vartheta_{OP}} = \int_{-BW}^{+BW} S_{\vartheta_{OP}}(f)\, df \qquad (3.23)$$

If $BW \to \infty$, the integral is defined as the variance of the random process. In the case of the VCO working in the open-loop condition, the integration from $-\infty$ to $+\infty$ is not possible because the integration of the function $\dfrac{1}{f^3}$ gives a singularity at $f = 0$. To overcome this convergence problem the spectral characteristics of the input-referred noise given in Fig. 3.6 are modified according to the plot shown in Fig. 3.8, which is synthesized as follows:

$$S_n(f) = \begin{cases} \varepsilon & \text{for } |f| < f_Z \\ \dfrac{\alpha}{f} & \text{for } f_Z \le |f| < f_F \\ \beta & \text{for } f_F \le |f| \end{cases} \qquad (3.24)$$

Based on this spectral distribution, equation (3.23) becomes:
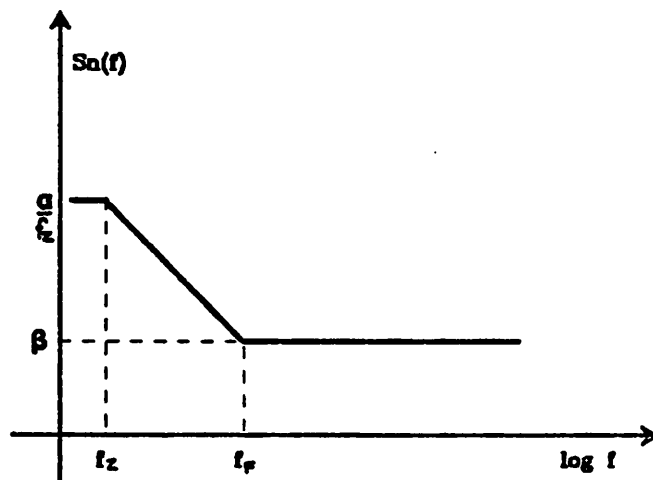
Figure 3.9. Modified Spectral Distribution of Integrator Noise

$$\chi^2_{\vartheta_{OP}} = 2\int_{f_Z}^{f_F} \alpha \, \frac{df}{f^3} + 2\int_{f_F}^{BW} \beta \, \frac{df}{f^2} \tag{3.25}$$

$$= I_2' + I_3'$$

This expression can also be integrated in the ω domain by substituting $\omega=2\pi f$ as follows:

$$\chi^2_{\vartheta_{OP}} = 8\pi^2 \int_{2\pi f_Z}^{2\pi f_F} \alpha \, \frac{d\omega}{\omega^3} + 4\pi \int_{2\pi f_F}^{2\pi BW} \beta \, \frac{d\omega}{\omega^2}$$

$$= 8\pi^2 \alpha \left[-\frac{2}{\omega^2} \right]_{2\pi f_Z}^{2\pi f_F} + 4\pi\beta \left[-\frac{1}{\omega} \right]_{2\pi f_F}^{2\pi BW} \tag{3.26}$$

If $BW \to \infty$ then:

$$\chi^2_{\vartheta_{OP}} = I_{2_0}' + I_{3_0}'$$

$$= 4\alpha \frac{f_F^2 - f_Z^2}{f_Z^2 f_F^2} + 2\frac{\beta}{f_F} \tag{3.27}$$

Equation (3.27) will be used later to see the effects of the VLL loops over the spectral characteristics of the VCO.

3.5.4. Effect of the VLL Loops on the VCO Signal Spectrum

In this analysis the noise modulation of the phase and amplitude components of the carrier is considered to be a disturbance *preceding* the VCO. (Fig. 3.9 shows the block diagram of the VLL combined with the linear contribution of the noise sources $n_A(t)$ and $n_P(t)$). The results obtained using such an approach are equivalent to those obtained when the disturbance is considered to be *following* the VCO. However, in the first approach it is simpler to include the noise contributions of the phase and amplitude comparators as part of $n_A(t)$ and $n_P(t)$. Furthermore, given the orthogonality of the transfer functions of the phase and amplitude components, the analysis is done only for the phase loop and the
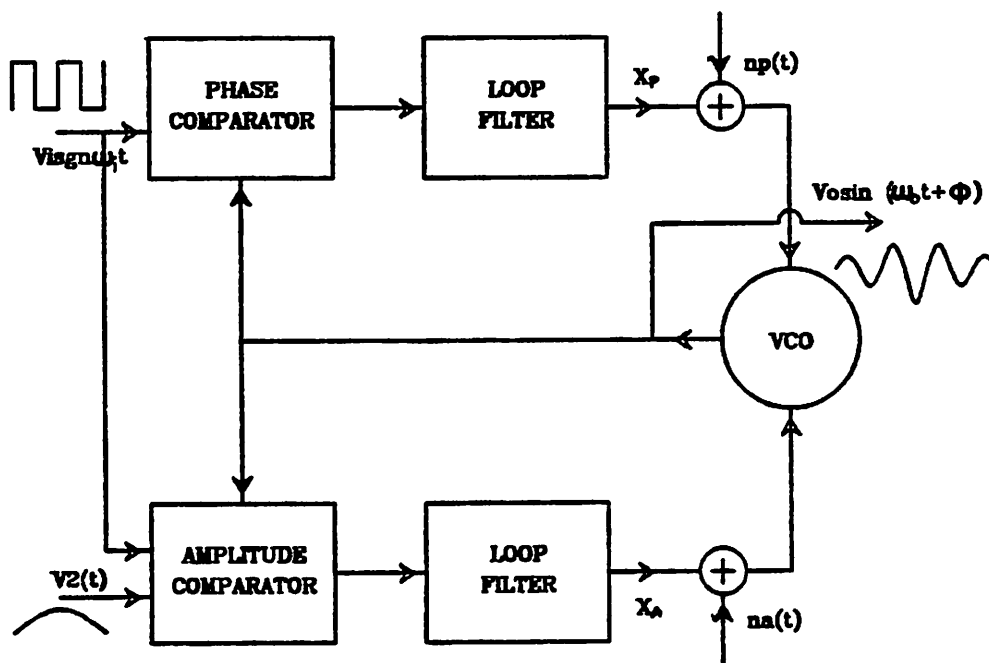

Figure 3.8. VLL with Noise Sources

results can be extended to the amplitude loop by simply changing the corresponding gain parameters (the phase and amplitude noise densities are also equal according to equations (3.6a) and (3.6b).

The phase loop with the noise-modulated VCO is shown in Fig. 3.9. The gain constant of the VCO (K_{VCO_P}) is used to find the relationship between the phase $\vartheta_P(t)$ and the modulation input $n_P(t)$:

$$\frac{d\vartheta_P(t)}{dt} = K_{VCO_P} n_P(t) \tag{3.28}$$

Under the assumption that the signal $n_P(t)$ is a nonrandom process the phase modulation can be expressed in the s domain as $\Theta_P(s)$. Hence using equation (3.28) the output of the VCO becomes:

$$s\Theta_P(s) = K_{VCO_P}[N_P(s) + \bar{X}_P(s)] \tag{3.29}$$

$\bar{X}_P(s)$ is the signal at the output of the phase comparator given by:

$$\bar{X}_P(s) = -K_{C_P}F(s)\Theta_P(s) \tag{3.30}$$

where $F(s)$ is the frequency response of the loop filter. The combination of equations (3.29) and (3.30) gives the resulting VCO closed-loop response to the modulating signal $N_P(s)$:

$$\frac{\Theta_P(s)}{N_P(s)} = \frac{K_{VCO_P}}{s + K_{VCO_P}K_{C_P}F(s)}$$
$$= \frac{K_{VCO_P}}{s + K_P F(s)} \tag{3.31}$$

The error function of a PLL was already given by equation (3.2) and is repeated here for the phase loop of the VLL [14]:

$$1 - H(s) = \frac{s}{s + K_P F(s)} \tag{3.32}$$

Combining equations (3.31) and (3.32) we get:

$$\frac{\Theta_P(s)}{N_P(s)} = K_{VCO_P}\frac{1 - H(s)}{s} \tag{3.33}$$

The open-loop phase modulation is obtained by making $\bar{X}_P(s)=0$ in equation (3.29):

$$s\,\Theta_{PO}(s) = K_{VCO_P}N_P(s)$$ (3.34)

Equations (3.33) and (3.34) are combined to give:

$$\frac{\Theta_P(s)}{\Theta_{PO}(s)} = 1-H(s)$$ (3.35)

Bearing in mind that $\vartheta(t)$ is a random process with an open-loop spectral density $S_{\vartheta_{OP}}(f)$, the closed-loop spectral density is therefore:

$$S_{\vartheta_P}(f) = |1-H(j2\pi f)|^2 S_{\vartheta_{OP}}(f)$$ (3.36)

The total noise power of the VCO under the closed loop condition is given by the integral of expression (3.36).

$$\chi_{\vartheta_P}^2 = \int_{-BW}^{+BW} |1-H(j2\pi f)|^2 S_{\vartheta_{OP}}(f)\,df$$ (3.37)

where BW is the bandwidth. Using the spectral distribution $S_{\vartheta_{OP}}$ given by equation (3.24), we obtain:

$$\chi_{\vartheta_P}^2 = 2\int_0^{f_Z} \alpha\,\frac{|1-H(j2\pi f)|^2}{f^2}df$$
$$+2\int_{f_Z}^{f_F} \alpha\,\frac{|1-H(j2\pi f)|^2}{f^3}df$$ (3.38)
$$+2\int_{f_F}^{BW} \beta\,\frac{|1-H(j2\pi f)|^2}{f^2}df$$

Which is equivalent to:

$$\chi_{\vartheta_P}^2 = 4\pi\int_0^{2\pi f_Z} \alpha\,\frac{|1-H(j\omega)|^2}{\omega^2}d\omega$$
$$+8\pi^2\int_{2\pi f_Z}^{2\pi f_P} \alpha\,\frac{|1-H(j\omega)|^2}{\omega^3}d\omega$$ (3.39)
$$+4\pi\int_{2\pi f_F}^{2\pi BW} \beta\,\frac{|1-H(j\omega)|^2}{\omega^2}d\omega$$

Replacing the value of $|1-H(j\omega)|$ given by equation (3.4), we obtain:

$$\chi^2_{\delta_P} = 4\pi \int_0^{2\pi f_Z} \alpha \, \frac{\omega^2}{(\omega_n^2 - \omega^2)^2 + (2\zeta\omega_n\omega)^2} \, d\omega$$

$$+ 8\pi^2 \int_{2\pi f_Z}^{2\pi f_P} \alpha \, \frac{\omega}{(\omega_n^2 - \omega^2)^2 + (2\zeta\omega_n\omega)^2} \, d\omega \qquad (3.40)$$

$$+ 4\pi \int_{2\pi f_P}^{2\pi BW} \beta \, \frac{\omega^2}{(\omega_n^2 - \omega^2)^2 + (2\zeta\omega_n\omega)^2} \, d\omega$$

$$= I_1 + I_2 + I_3$$

The integrals I_i represent the total noise power under the different portions of the noise spectrum distribution, namely: the arbitrary flat portion from 0 to f_Z gives I_1, from f_Z to f_P gives I_2 and from f_P to BW gives I_3. The following solutions for I_1, I_2 and I_3 are valid only if $\zeta \geq 1$. Such is our case, as will be shown in the calculation of the loop filter elements (see Chapter 4).

$$I_1 = 4\pi \int_0^{2\pi f_Z} \alpha \, \frac{\omega^2}{[\omega^2 + (\zeta - \sqrt{\zeta^2-1})^2 \omega_n^2][\omega^2 + (\zeta + \sqrt{\zeta^2-1})^2 \omega_n^2]} \, d\omega$$

$$= 4\pi\alpha \int_0^{2\pi f_Z} \left[\frac{(\zeta - \sqrt{\zeta^2-1})^2}{4\zeta\sqrt{\zeta^2-1}} \, \frac{d\omega}{\omega^2 + (\zeta - \sqrt{\zeta^2-1})^2 \omega_n^2} \right.$$

$$\left. - \frac{(\zeta + \sqrt{\zeta^2-1})^2}{4\zeta\sqrt{\zeta^2-1}} \, \frac{d\omega}{\omega^2 + (\zeta + \sqrt{\zeta^2-1})^2 \omega_n^2} \right] \qquad (3.41)$$

$$I_1 = 4\pi\alpha \left[\frac{\zeta - \sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}} \tan^{-1} \frac{\omega}{\omega_n(\zeta - \sqrt{\zeta^2-1})} \right.$$

$$\left. - \frac{\zeta + \sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}} \tan^{-1} \frac{\omega}{\omega_n(\zeta + \sqrt{\zeta^2-1})} \right]_0^{2\pi f_Z}$$

For the portion in which the flicker noise dominates, the integration is done as follows:

$$I_2 = 8\pi^2 \int_{2\pi f_Z}^{2\pi f_P} \alpha \, \frac{\omega}{[\omega^2 + (2\zeta^2-1)\omega_n^2]^2 - (2\zeta\sqrt{\zeta^2-1}\omega_n^2)^2} \, d\omega$$

$$= 8\pi^2\alpha \left[\frac{1}{4\zeta\omega_n^2\sqrt{\zeta^2-1}} \ln \frac{\omega^2 + (\zeta + \sqrt{\zeta^2-1})^2 \omega_n^2}{\omega^2 + (\zeta - \sqrt{\zeta^2-1})^2 \omega_n^2} \right]_{2\pi f_Z}^{2\pi f_P} \qquad (3.42)$$

The maximum of I_2 will occur when $f_Z = 0$ and $f_P = \infty$, a condition that yields:

$$I_{2_0} = 8\pi^2\alpha \frac{1}{4\zeta\omega_n^2\sqrt{\zeta^2-1}}\ln\frac{\left(\zeta+\sqrt{\zeta^2-1}\right)^2}{\left(\zeta-\sqrt{\zeta^2-1}\right)^2} \tag{3.43}$$

The solution for I_3 is the same as that for I_1, but with the lower and upper integration limits ranging from 0 to $2\pi f_P$ and from $2\pi f_Z$ to $2\pi BW$ respectively.

$$I_3 = 4\pi\beta \left[\frac{\zeta-\sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}}\tan^{-1}\frac{\omega}{\omega_n(\zeta-\sqrt{\zeta^2-1})}\right.$$
$$\left.- \frac{\zeta+\sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}}\tan^{-1}\frac{\omega}{\omega_n(\zeta+\sqrt{\zeta^2-1})}\right]_{2\pi f_P}^{2\pi BW} \tag{3.44}$$

The limit case (variance) occurs when $f_P=0$ and $BW=\infty$, yielding:

$$I_{3_0} = 4\pi\beta \frac{\pi}{4\zeta\omega_n} \tag{3.45}$$

3.5.5. Comparison Between Open and Closed Loop Noise Performance

It is interesting to compare the open-loop integrated noise with the respective closed-loop value over equal frequency bands. This is done in the $\frac{1}{f}$ region by dividing I_2 by I_2', values that are given respectively by equations (3.42) and (3.26):

$$\frac{I_2}{I_2'} = \frac{\left[\dfrac{1}{4\zeta\omega_n^2\sqrt{\zeta^2-1}}\ln\dfrac{\omega^2+(\zeta+\sqrt{\zeta^2-1})^2\omega_n^2}{\omega^2+(\zeta-\sqrt{\zeta^2-1})^2\omega_n^2}\right]_{2\pi f_Z}^{2\pi f_P}}{\left[-\dfrac{2}{\omega^2}\right]_{2\pi f_Z}^{2\pi f_P}} \tag{3.46}$$

A similar procedure is used in the uniform spectral region using equations (3.44) and (3.26):

$$\frac{I_3}{I_3'} = \frac{1}{\left[-\dfrac{1}{\omega}\right]_{2\pi f_P}^{2\pi BW}} \left[\frac{\zeta-\sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}}\tan^{-1}\frac{\omega}{\omega_n(\zeta-\sqrt{\zeta^2-1})}\right.$$
$$\left.- \frac{\zeta+\sqrt{\zeta^2-1}}{4\zeta\omega_n\sqrt{\zeta^2-1}}\tan^{-1}\frac{\omega}{\omega_n(\zeta+\sqrt{\zeta^2-1})}\right]_{2\pi f_P}^{2\pi BW} \tag{3.47}$$

The overall noise power reduction η over the frequency band $-BW$ to BW is:

$$\eta = \frac{I_2 + I_3}{I_2' + I_3'} \qquad (3.48)$$

By inspecting equations (3.26), (3.42) and (3.44) large values of ζ and ω_n minimize the factor η. The factor given by equation (3.48) will be numerically calculated in Chapter 4.

CHAPTER 4

NMOS BUILDING BLOCKS FOR THE VLL

4.1. The Integrator

As was previously stated, an open-loop, single-pole, operational amplifier functions as an integrator. The timing characteristics of the whole system are determined by the integrating constant (unity gain-bandwidth) and phase of this OPAMP. The first parameter defines the oscillating frequency and the second the amplitude.

Fig. 4.1 shows a simplified schematics of the NMOS operational amplifier [15]. There are two basic differences between this circuit and a standard OPAMP:
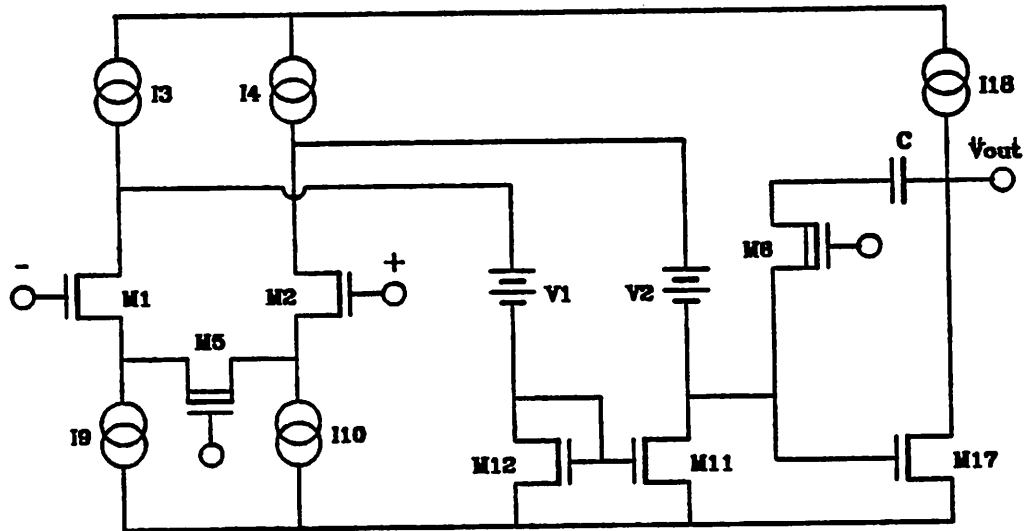

Figure 4.1. Conventional NMOS OPAMP

(1) The sources of the input differential pair M_1 and M_2 are not connected together. Instead the transistor M_5 acting as a variable resistor connects M_1 and M_2. The gain-bandwidth product is a function of its gate potential.

(2) The transistor M_6 is used to eliminate the effects of the transmission zero. Its gate allows the continuous variation of its ON resistance. The adjustable zero obtained is used to vary the overall phase shift.

In other words, the amplifier's complex frequency response $H(\omega) = \rho(\omega)e^{\psi(\omega)}$ can be modified by the two controlling voltages applied to the gates of M_5 and M_6 (ρ is the amplitude response and ψ the phase response).

In a single-channel circuit like this the key elements are the level shifters V_1 and V_2. Depending on the type of application, these elements must be capable of either tracking the difference between the positive and negative supplies to maximize the input common-mode range, or making the output insensitive to power supply induced noise. Fig. 4.2 shows in more detail the level shifters together with the differential-to-single-ended converters. The current sources I_{19} and I_{20} are derived from a replica bias that generates, in conjunction with M_7 and M_8, the proper value of voltage shift. The small signal impedance is approximately given by $\frac{1}{g_{m\,13}}$ or $\frac{1}{g_{m\,14}}$. It should be noted that the small signal impedance presented to the outputs of the differential pair by the differential-to-single-ended converter M_{11}, M_{12} is increased by the series impedance of V_1 and V_2, or $\approx \frac{1}{g_{m\,12}} + \frac{1}{g_{m\,14}}$. This additional series impedance is important for the analysis of the excess phase-shift.

One of the basic design considerations is to ensure that the impedance of the level shifters does not increase because of a bias current reduction under slewing conditions. This is done by making each of the values of the current sources I_3
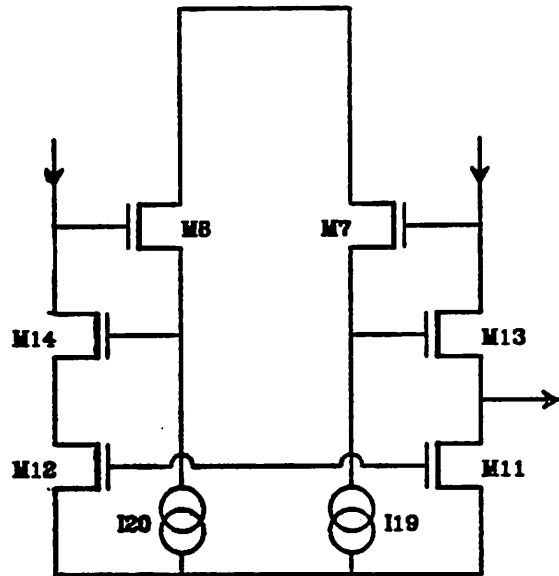
Figure 4.2. NMOS Level Shifters

and I_4 equal to or greater than the sum of I_9 and I_{10} in Fig. 4.1. Another reason for doing this is that if the values of I_3 and I_4 are much smaller than I_9+I_{10}, noise performance and low-frequency gain degrade.

Another circuit approach for the level shifters is depicted in simplified form in Fig. 4.3. In this case, V_1 and V_2 translate voltage signals rather than current signals. This variation has some advantages over the previous scheme:

(a) As shown in Fig. 4.4, the actual implementation is simplified. The pair M_{13} and M_{14} has disappeared, making the small signal impedance of the left branch of the current mirror $\approx \dfrac{1}{g_{m\,12}}$. Assuming that the same impedance as in the previous scheme is desired, the net effect is a reduction in area of four times, provided that the sizes of M_{13} and M_{14} are equal to those of M_{11} and M_{12}.
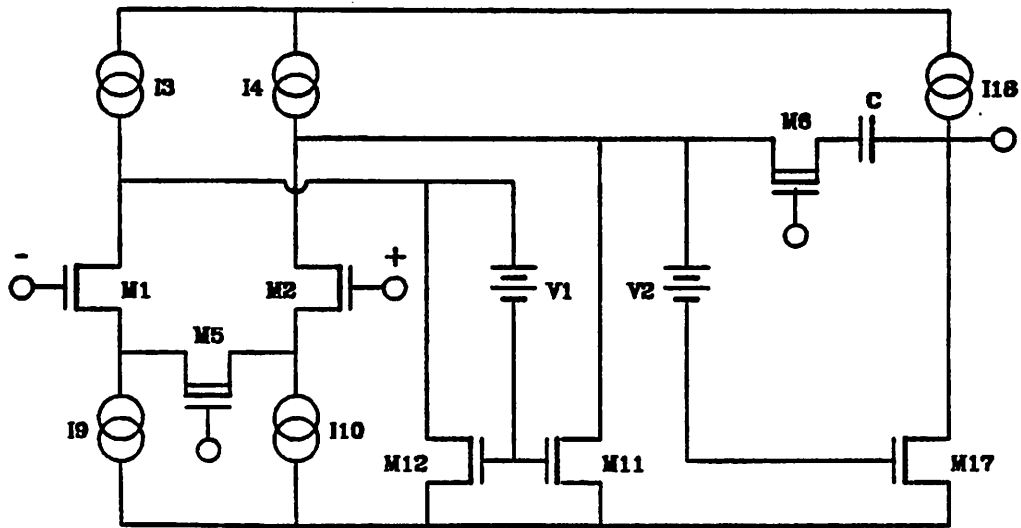
Figure 4.3. Modified NMOS OPAMP
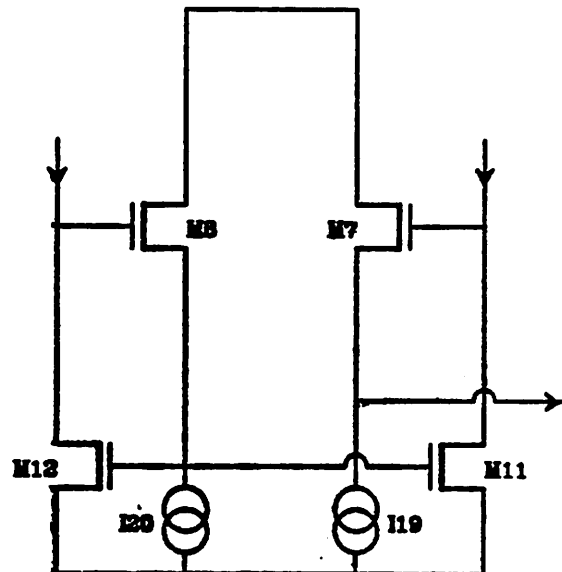
Figure 4.4. Modified NMOS Level Shifters

(b) By means of a replica bias circuitry, the compensation capacitor is now con-
nected between the output and a node that can be referred to the reference
potential (i.e. ground) and not to the negative potential, thus reducing the
power supply coupling to the output.

Fig. 4.5 shows the complete schematic diagram of the integrator.

Since all the DC connections are internal to the integrated circuit, and the
interface to the external world is done in AC, there is no need for a split power
supply, therefore the negative potential for the whole chip is ground. Further-
more, the input-common-mode range is limited to a few hundred millivolts. Thus

Figure 4.5. Circuit Schematics of NMOS Integrator

the voltage at the drains of the input pair may be referred to ground. This reduces the power supply coupling to the output. With these considerations in mind, the bias circuit is described as follows (see Fig. 4.6).
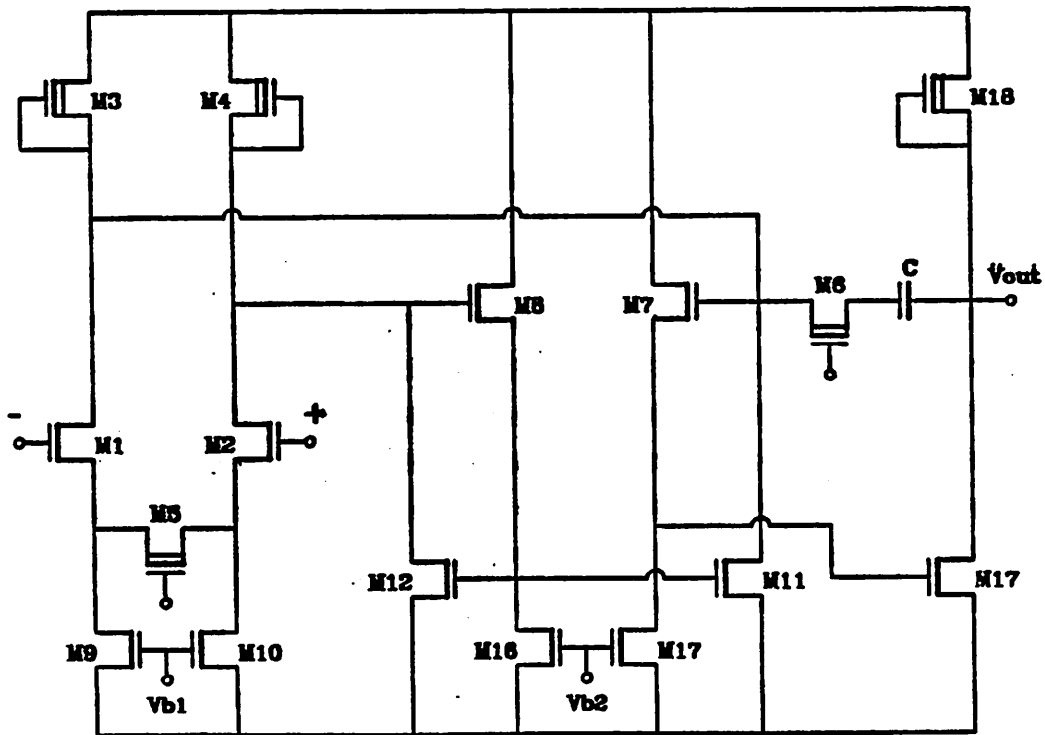
The voltage V_{b0} is used as a reference for all the inputs of the integrators, and the voltage V_{b1} is used to bias the current sources of the OPAMPs. If the $\frac{W}{L}$ ratio of all the enhancement devices is $\gg 1$, the potential at the drains of the input pairs of the OPAMPs is approximately $2V$. For this application in which there is no input common-mode voltage, this voltage is adequate to assure that the input devices remain saturated.

4.2. Detailed Circuit Design

The integrating action of this OPAMP can be modeled as follows (Fig. 4.7):

The voltage-controlled current source (VCCS) g_{m1} represents the combined action of the variable resistor M_5 and the amplifier's input pair. Given the $\frac{W}{L}$
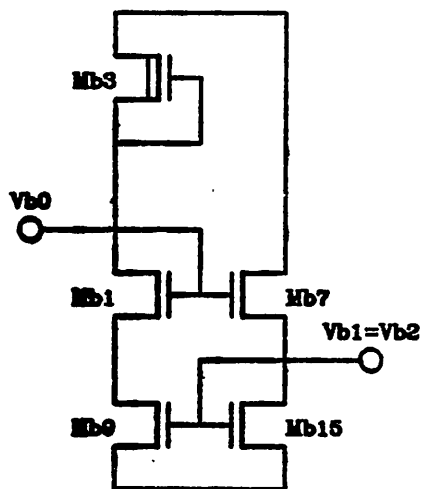

Figure 4.6. Bias Circuit
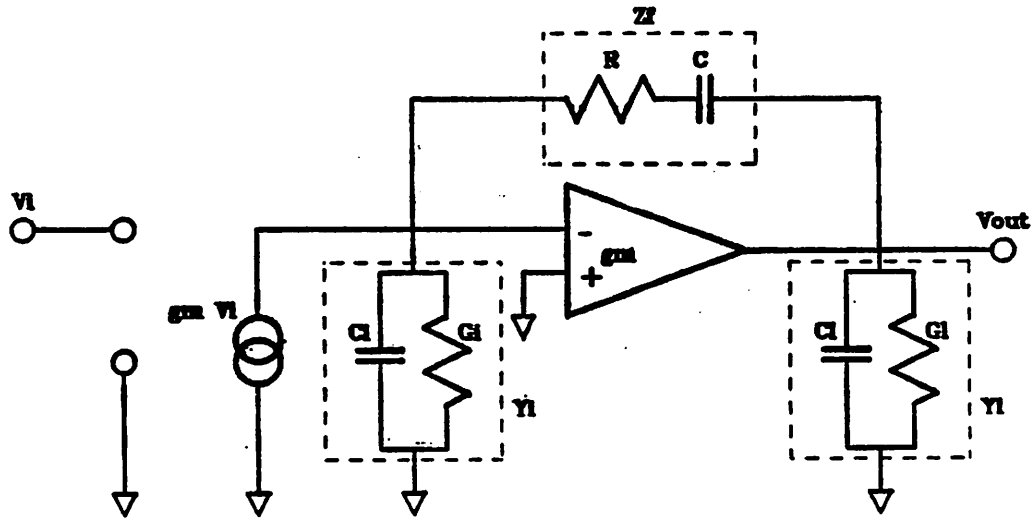
Figure 4.7. Small-Signal Equivalent of the Integrator

ratios between M_1 (or M_2) and M_5, the transconductance of this VCCS is approximately equal to the ON conductance of M_5. The second stage of the OPAMP functions as the active element of the integrator. The voltage gain is a function of the transconductance g_{m2}, the input and output loading elements Y_i and Y_i and the feedback impedance Z_f.

In order to reduce inaccuracies at the range of operating frequencies desired for the system, i.e. $\approx 455kHz$, it is important to keep the excess phase shift to a minimum. This is done by designing the composite amplifier (first and second stages) in such way that all the internal parasitic poles are located at frequencies much larger than $455kHz$.

To obtain the desired operating frequency $\frac{\omega_n}{2}\pi$ given by the the fixed ratio $\frac{g_{m1}}{C}$, both g_{m1} and C can be arbitrarily defined. As the value of g_{m1} increases, the noise performance improves and also the value of C decreases, pushing the

location of the second pole away from the operating frequency so that the excess phase-shift is also decreased. However, a very small value for C makes the relative effects of parasitic capacitances more significant. If g_{m1} is decreased, the noise performance degrades and as an added effect the charging time (slew rate) for a given bias current increases, creating a potential distortion problem. Computer simulation is used to help optimize the element combination, given the amount of available power and area, and the parameters of the NMOS process used in this work. The optimum value found for C is $14pF$.
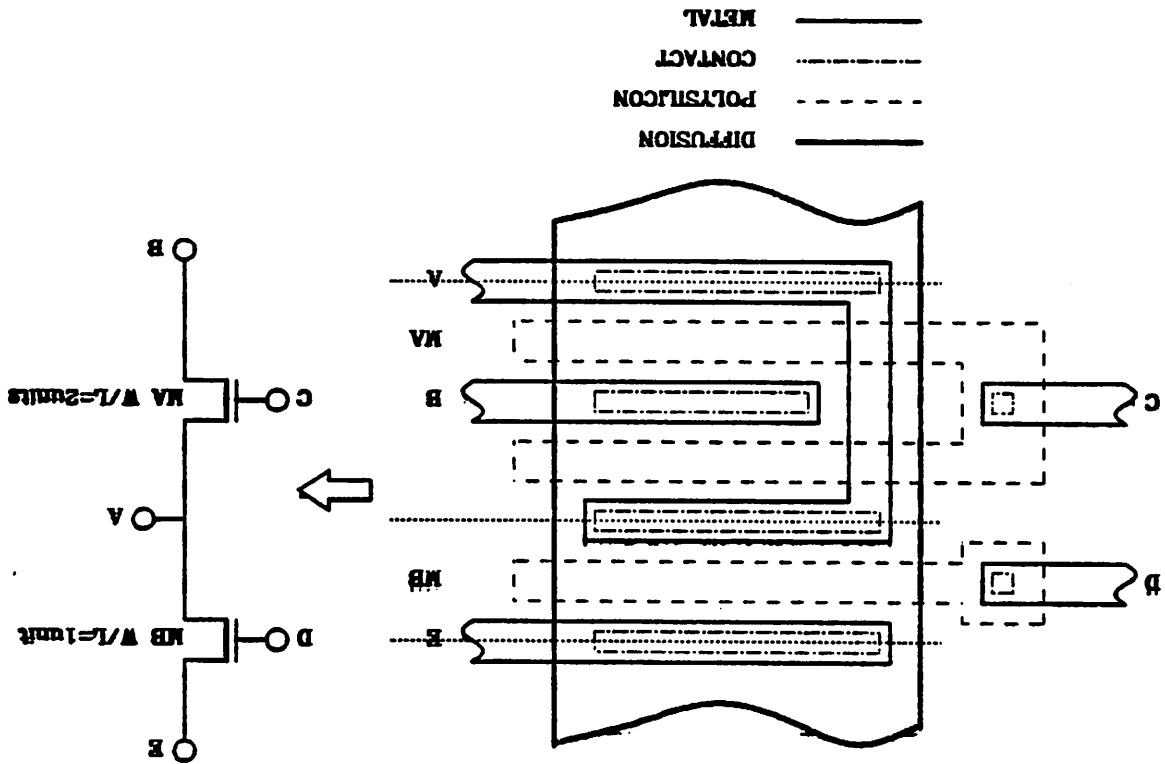
A very important consideration in designing the $\frac{W}{L}$-ratios of the transistors is a layout strategy based on minimizing the amount of field area that separates the different elements within the circuit (mostly diffusion regions). Generally speaking, this minimum spacing is one of the most limiting design rules in MOS technology, and it does not provide any useful function. The strategy used here imposes a pattern in which all the transistors are defined by stacking horizontal polysilicon lines across a large single diffusion area (thin oxide) and making the interconnections between the drains (or sources) with vertical lines of metal (Fig. 4.8). Thus several diffusion areas with a common potential (e.g. ground) can be found at different "geometrical" levels. In order to make this arrangement possible, the transistors must be composed of an integer number of unit elements chosen according to the desired channel conductance. Therefore arbitrary $\frac{W}{L}$-ratios are not allowed. As shown in the following design procedure, this does not represent any limitation in the design, for in most practical cases this technique is perfectly compatible with the transistor ratios usually encountered in analog circuits.

In a typical two stage operational amplifier, the phase margin is a function of the ratio between the first and second pole locations. As this ratio becomes larger, the phase shift becomes smaller. These frequencies are given by the

ratios $\frac{g_{m1}}{C}$ and $\frac{g_{m15}}{C+C_1}$ respectively, where C_1 is the loading capacitance. This means that the transconductance (thus the $\frac{W}{L}$ ratio) of the first stage has to be smaller than the one of the second stage.

Similarly, with respect to the large signal performance, the bias current of the first stage has to be smaller than the corresponding current of the second stage in order to achieve a good transient response under slewing conditions. For a two stage amplifier to be used with capacitive loading only, no output buffer is necessary, thus it is of standard practice to make the value of the integrating capacitor several times larger than the maximum capacitive load. In this way the slew rate is determined primarily by the bias current of the first stage and the value of the integrating capacitor. This bias current is calculated based on the

Figure 4.8. MOS Stacked Layout

DIFFUSION ——————
POLYSILICON - - - - -
CONTACT -··—··—··-
METAL ——————

MA W/L=5mmμ
MB W/L=1mmμ

B   C   A   D   E   VA   VB

minimum slew rate needed, which is the slope of the output sinusoid at the zero crossing point, or:

$$SR = V_{pk}\omega_0 \tag{4.1}$$

where V_{pk} is the maximum peak voltage of the signal present at the output ($< 100mV$), and ω_0 is the free running angular frequency ($2\pi 455kHz$), therefore $SR \geq 0.7\dfrac{V}{\mu sec}$. In reality this value has to be much larger, because the start up signal size is much larger than $100mV$. The final value chosen for the slew rate was based on computer simulations of the locking acquisition process (described in Chapter 6): $SR \approx 3.0\dfrac{V}{\mu sec}$. Thus:

$$\frac{I_3}{2} = \frac{I_4}{2} = SR \times C = 3.0\frac{V}{\mu sec} \times 12pF = 36.0\mu A \tag{4.2}$$

Now the Shichman-Hodges model can be used to calculate the dimension of the transistor that defines the current unit. The current of a MOS transistor in the saturation mode is:

$$I_{DS} = \frac{W}{L}\frac{\beta}{2}(V_{GS} - V_{TH_D})^2 \tag{4.3}$$

where β is the *gain* of the transistor given in $\dfrac{A}{V^2}$ (a function of the process, $\approx 3.0 \times 10^{-5}$), and V_{TH_D} is the depletion *threshold*, also a processing parameter ($\approx -3.0V$). The threshold of the depletion mode device is used because it defines the current in the amplifier. Now the value of $\dfrac{W}{L}$ can be found from equation (4.3), ($V_{GS} = 0$):

$$\frac{W}{L} \approx 0.13$$

The final drawn dimension of the current unit is $W = 12\mu m$ and $L = 40\mu m$ (the further safety factor of 2 is taken into account for processing variations and the lateral shrinking of the devices because of the local oxidation process, $W_{EFF} \approx 11\mu m$). It is important to note that the second-stage bias current must

be several times greater than the first-stage current for the charging of the capacitor (one unit). The factor chosen for this was 4. Thus all the current sources are a parallel connection of several of these current units: $I_3 = I_4 = 2$ units and $I_{18} = 4$ units.

The *gain* transistors should also be separated into units according to the layout strategy. The unit width chosen for the gain devices was $90\mu m$, and the channel length is $9\mu m$ for all transistors except for M_1 and M_2, in which case the channel length is $8\mu m$. Transistor M_{17} has four units, and all the other enhancement transistors have one unit. Fig. 4.9 shows the final drawing of the layout of the integrator, where each transistor is separated by dotted lines.

Now the second pole location (ω_2) and the excess phase shift (ψ_2) can be calculated using the following expression:

$$\omega_2 = \frac{g_{m2}}{C}$$

$$\psi_2 = \tan^{-1}(\frac{\omega_0}{\omega_2}) \tag{4.4}$$

where C is the integrating capacitance, ω_0 the gain constant of the integrator, and g_{m2} the transconductance of the second stage, given by:

$$g_{m2} = \sqrt{2 I_{18}(\frac{W}{L})_{17}\beta_E} \tag{4.5}$$

By first substituting I_{18} in equation (4.5) with the Shichman-Hodges expression:

$$g_{m2} = \left[2\left[(\frac{W}{L})_{18}\frac{\beta_D}{2}(-V_{TH_D})^2 \right](\frac{W}{L})_{17}\beta_E \right]^{\frac{1}{2}} \tag{4.6}$$

then replacing the corresponding values in equation (4.6):

$$g_{m2} = \left[2\left[4 \text{ } {}^*MOS\frac{11}{40}\times\frac{3.0\times10^{-5}}{2}(3.0)^2 \right]\times4\times\frac{90}{9}\times3.0\times10^{-5} \right]^{\frac{1}{2}}$$
$$= 4.42\times10^{-4}\Omega^{-1}$$

Finally, substituting this and the value of C back into equation (4.4), we obtain:

$$\omega_2 = \frac{4.42 \times 10^{-4} \Omega^{-1}}{12.0 pF}$$

$$= 36.8 \times 10^6 rad$$

$$\psi_2 = \tan^{-1}\left(\frac{2\pi 0.455 \times 10^6}{36.8 \times 10^6}\right)$$

$$= 4.4^{\circ}$$

We conclude that the additional phase-shift is very small because of the location of the second pole in the second stage. Probably other factors such as the right-half plane zero and higher order poles because of the parasitic capacitances have a stronger effect on the overall phase margin, which is compensated for by the action of the loop.

The transistor M_5 serving as a variable resistor has a value that in conjunction with C, sets the gain constant of the integrator. Three different criteria can be used to define its dimensions:

(a) *Maximum dynamic range*

The possible adjusting range is given by its transconductance and the maximum output of the phase comparator (the whole power supply voltage). For this reason it is convenient to have a high transconductance device to maximize this range.

(b) *Low distortion*

A high transconductance transistor operates at a low gate overdrive voltage ($V_{GS} - V_T$), making it susceptible to a resistance modulation effect with the signal applied to the input of the integrator (intermodulation distortion). The amount of distortion is lower if M_5 is a low transconductance transistor. This implies the need of a larger overdrive voltage to sustain the required resistance value. Hence the relative effect of the signal over the value of channel conductance is reduced.
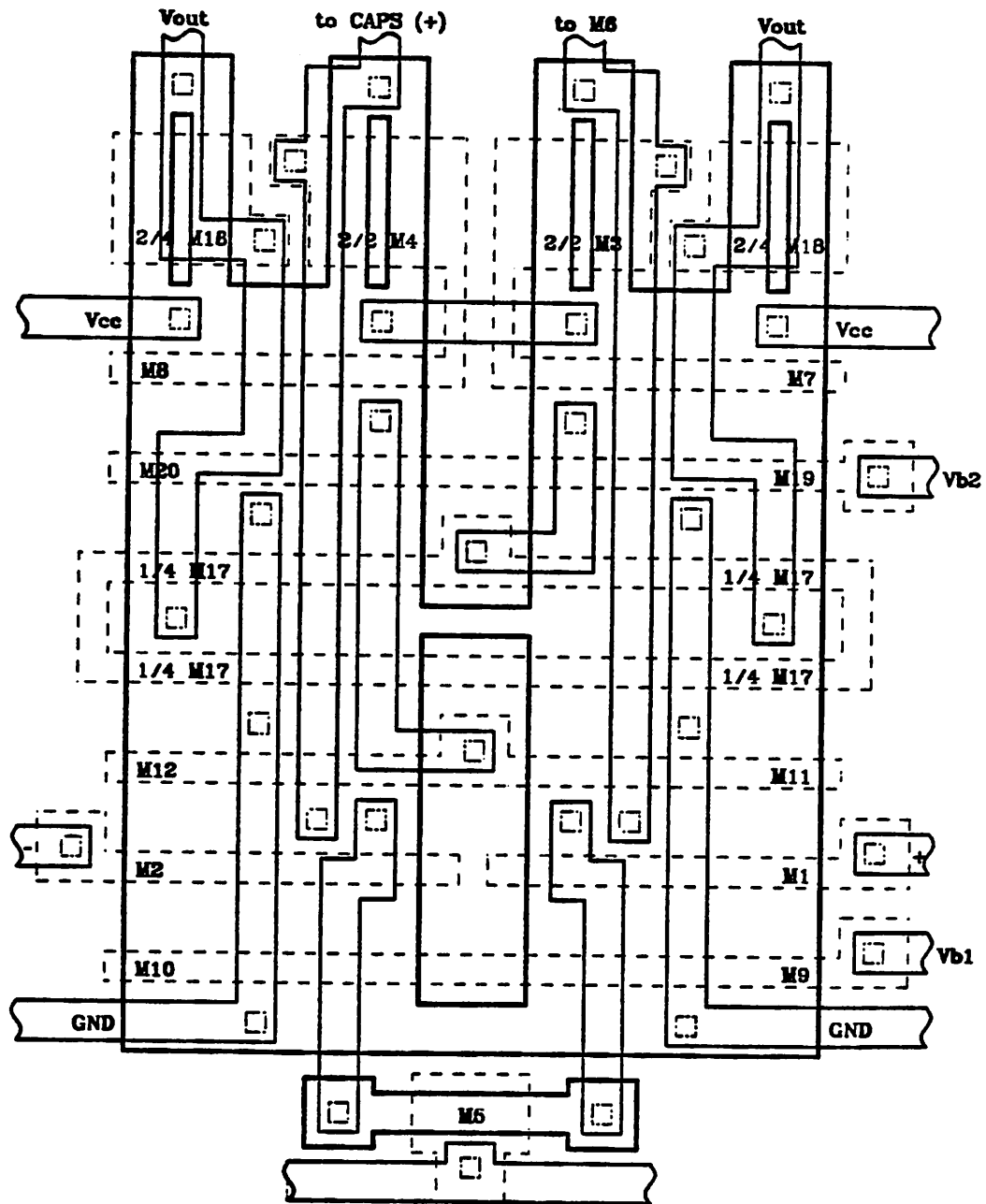
Figure 4.9. Lay-out of NMOS Integrator

(c) *Minimum temperature coefficient*

One of the single most important performance parameters in any PLL system

is the temperature stability of the free running frequency, which in our case is referred to as the stability of the gain constant. Since considerations (a) and (b) serve only to define boundary values, this new topic helps to define more convincingly the dimensions of M_5.

The current in a MOS transistor in the triode region is given by:

$$I_{DS} = \mu C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$ (4.7)

where:

I_{DS} is the current in the channel,

μ the majority carrier (electrons) mobility,

C_{OX} the oxide capacitance per unit area,

W the effective channel width,

L the effective channel length,

V_{GS} the gate-to-source applied voltage,

V_{TH} the threshold voltage,

and V_{DS} the drain-to-source voltage.

By taking the derivative of the current with respect to the drain voltage, the channel conductance G_0 is obtained:

$$\frac{dI_{DS}}{dV_{DS}} = G_0 = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})$$ (4.8)

The time constant τ_0 is given by:

$$\tau_0 = \frac{C}{G_0}$$ (4.9)

where the MOS capacitance C_0 is given by:

$$C_0 = C_{OX} A_0$$ (4.10)

where A_0 is the area of the capacitor.

By replacing the value of G_0 from equation (4.8) and C from equation (4.9) into equation (4.10), we get:

$$\tau_O = \frac{A_O}{\mu \frac{W}{L}(V_{GS} - V_{TH} - V_{DS})} \qquad (4.11)$$

The factor C_{OX} disappears from expression (4.11), making the temperature dependence a function of μ and V_{TH} only. After some algebraic manipulation and taking the derivative with respect to the absolute temperature T, we obtain:

$$\frac{1}{\tau_0} \frac{d\tau_0}{dT} = -\frac{1}{\mu} \frac{d\mu}{dT} + \frac{1}{V_{GS} - V_{TH} - V_{DS}} \frac{dV_{TH}}{dT} \qquad (4.12)$$

From the lattice scattering theory, the dependence of mobility on temperature is given by:

$$\frac{\mu}{\mu_0} = (\frac{T}{T_0})^{-\frac{3}{2}} \qquad (4.14)$$

where μ_0 is the mobility at temperature T_0. The relative variation of μ is found by taking the derivative of equation (4.14):

$$\frac{1}{\mu} \frac{d\mu}{dT} = -\frac{3}{2} \frac{1}{T} \qquad (4.15)$$

Replacing equation (4.15) into (4.12) we get:

$$\frac{1}{\tau_0} \frac{d\tau_0}{dT} = -\frac{3}{2} \frac{1}{T} + \frac{1}{V_{GS} - V_{TH} - V_{DS}} \frac{dV_{TH}}{dT} \qquad (4.16)$$

By making the temperature coefficient $\frac{d\tau_0}{dT}$ in equation (4.15) equal to 0, we find the optimum quiescent overdrive voltage ($V_{GS} - V_T - V_{DS}$) to be:

$$V_{GS} - V_T - V_{DS} = \frac{2}{3} T \frac{dV_{TH}}{dT} \qquad (4.17)$$

Experimental data shows that $\frac{dV_T}{dT} \approx \frac{\Delta V_T}{\Delta T} = -2\frac{mV}{°C}$, and assuming that the applied voltage V_{DS} is equal to 0 and the temperature equal to 300 $°K$, we get:

$$V_{GS} - V_{TH} = 0.4 V$$

From the optimum gate overdrive voltage just found for M_6 and the desired steady-state value of conductance, we can easily calculate the dimensions using equation (4.8) for $V_{DS} = 0$. Either an enhancement or depletion type of transistor can be chosen, but for maximizing the variation of resistance in both directions (above and below the nominal value), the first type is preferable because the potential at the sources of M_1 and M_2 is only one enhancement threshold above ground potential.

In the prototype built, transistor M_5 is not designed based on the optimum temperature coefficient. Instead, the second alternative related to minimum channel modulation is used, and the type is depletion. The geometry calculated $((\frac{W}{L})_s = \frac{12}{40})$ is based on the given power supply voltage and the minimum and maximum conductance excursion required.

To compute the temperature coefficient of the timing constant of the prototype, a large value of $V_{GS} - V_T$ is applied instead of the one given by equation (4.17). Thus equation (4.16) is modified to become:

$$\frac{1}{T_0} \frac{dT_0}{dT} = -\frac{3}{2} \frac{1}{T} \tag{4.18}$$

For a center temperature of 330 °K and a maximum deviation of 70 °K, the timing variation is $\approx 35\%$.

Considerations (a) through (c) can be applied for the design of transistor M_6, which is the phase controlling variable resistor. But the approach chosen in our implementation was based on the assumption that the gate-to-source voltage of M_6 should be zero (to imitate the condition in which the gate is not driven but connected to its own source).

The function of M_6 is to cancel the effects of the right-half plane zero that occurs because of the finite transconductance of M_{17}. The location of this zero in

the ω axis is $\omega_{RH} = \dfrac{g_{m\,17}}{C}$. Therefore to achieve perfect cancellation g_{D6} should

be equal to $g_{m\,17}$. Given this condition the dimensions of M_6 are derived as follows:
The transconductance of transistor M_{17} operating in the saturation region is given
by:

$$g_{m\,17} = \sqrt{2\beta_E (\frac{W}{L})_{17} I_{17}} \qquad (4.19)$$

where:

$$I_{17} = I_{18} = \frac{\beta_D}{2} (\frac{W}{L})_{18} (V_{GS} - V_{TH_D})^2 \qquad (4.20)$$

By replacing the expression of I_{17} given by equation (4.20) into equation (4.19)
and making $V_{GS} = 0$, we get:

$$g_{m\,17} = \sqrt{\beta_E (\frac{W}{L})_{17} \beta_D (\frac{W}{L})_{18} (-V_{TH_D})^2} \qquad (4.21)$$

Now equation (4.8) can be used to find the value of the ON conductance of M_6 in
which $V_{GS} = V_{DS} = 0$:

$$G_{D6} = \beta_D (\frac{W}{L})_6 (-V_{TH_D}) \qquad (4.22)$$

By equating (4.21) and (4.22), and solving for $(\frac{W}{L})_6$, we obtain:

$$(\frac{W}{L})_6 = \sqrt{\frac{\beta_E}{\beta_D} (\frac{W}{L})_{17} \times (\frac{W}{L})_{18}} \qquad (4.23)$$

For the process used in the fabrication of this device, $\beta_E = \beta_D$, thus:

$$(\frac{W}{L})_6 = \sqrt{4 \times \frac{90}{9} \times 4 \times \frac{11}{40}}$$
$$= \sqrt{48} = 6.6$$

and the channel length L_6 is the same as L_{17}. The actual $(\frac{W}{L})_6$ is reduced by 20%

in order to further shift the zero towards the left-half plane so that the excess

phase shift caused by other parasitic poles is compensated.

4.3. The Phase (Amplitude) Comparator

The structure of the phase comparators, including the loop filters, is very similar to the integrator circuit regarding the level shifters and the input and output stage. The main difference is that in the phase (amplitude) comparators the input stages are switched on and off by the action of a digital clock signal applied to transistors M_{5_i}, whereas in the integrators the signal applied to transistor M_5 is an analog voltage that continuously changes the gain. Fig. 4.10a shows the sign multipliers P_1 and P_2 used in each comparator and the loop filter. The analog inputs are M_{1A}, M_{2B} and M_{2A} for P_1; and M_{1B}, M_{1C}, M_{2D}, M_{2C}, and M_{1D} for P_2. The digital inputs are M_{5A}, M_{5B} for P_1; and M_{5C}, M_{5D} for P_2. When the digital input is high, the source coupling for each differential amplifier is large, i.e., equivalent to a multiplication by plus one. When the digital input is low, the adjacent differential amplifier is active, providing a multiplication by minus one. The pair M_7, M_8 implements the level shifter, and the pair M_{11}, M_{12} implements the differential-to-single-ended converter. These configurations are similar to the ones in the integrator circuit.

The active element of the loop filter is a common-source stage composed of M_{17} and M_{18} as an integrator with phase compensation. The calculation of the value of these feedback elements will be described later. Transistors M_1, M_2, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{15}, M_{16}, M_{17} and M_{18} have the same dimensions as the corresponding transistors in the integrator. The switches M_5 are now of minimum size in order to decrease the amount of clock noise coupled in common mode by the displacement current across the gate. The other important difference is that the quiescent current in transistors M_3 and M_4 corresponds to five units each instead of two in order to sustain the additional current drained by four differential pairs instead of one. KV_2 indicates the amplitude current signal,
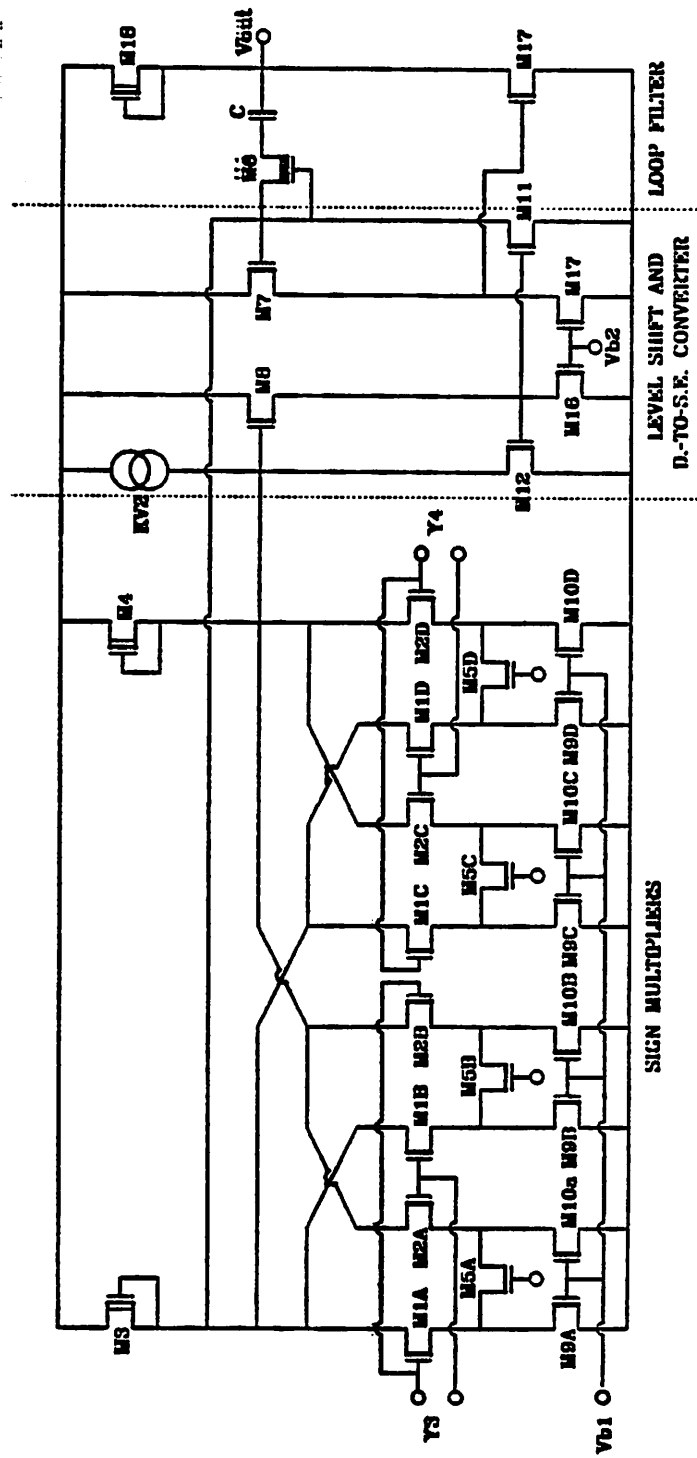
Figure 4.10a Circuit Schematic of the Phase and Amplitude Comparators

which is described in Chapter 5. Fig. 4.10b shows the clock signals applied to the switches M_{5a}, M_{5b}, M_{5c} and M_{5d}.

4.4. The Loop Filter

The first step in the design of the loop filter is to derive the transfer function of the phase and amplitude comparators. Thus a simple differential amplifier is analyzed first.

4.4.1. The Transfer Function of the Comparators

The output signal current I_n in a differential amplifier (Fig. 4.11a) is given by:

$$I_n = \begin{cases} \dfrac{I_0}{2}\left\{1 + \left[1-\left[1-\dfrac{\beta}{2}(\dfrac{W}{L})_{1,2}\dfrac{v_{in}^2}{I_0}\right]^2\right]^{\frac{1}{2}}\right\} & \text{for } v_{in} \geq 0 \\[4mm] \dfrac{I_0}{2}\left\{1 - \left[1-\left[1-\dfrac{\beta}{2}(\dfrac{W}{L})_{1,2}\dfrac{v_{in}^2}{I_0}\right]^2\right]^{\frac{1}{2}}\right\} & \text{for } v_{in} \leq 0 \end{cases} \qquad (4.24)$$

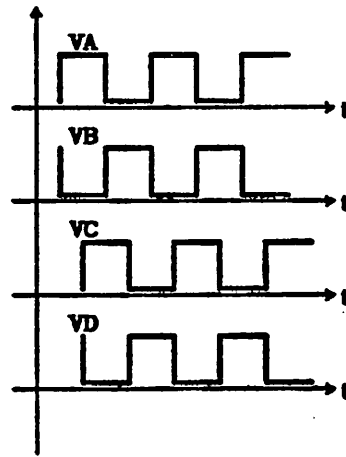where I_0 is the quiescent current of the differential amplifier, and β the transcon-

Figure 4.10b. Comparator's Clock Signals

ductance of the individual transistors (in $\frac{A}{V^2}$). A normalized variable

$$u = \sqrt{\frac{\beta}{2}(\frac{W}{L})_{1,2} \frac{v_{in}^2}{I_0}}$$ represents the analog input signal that is used in equation (4.24) to yield:

$$I_n = \begin{cases} \dfrac{I_0}{2}\left[1+\sqrt{1-(1-u^2)^2}\right] & \text{for } u \le 0 \\ \dfrac{I_0}{2}\left[1-\sqrt{1-(1-u^2)^2}\right] & \text{for } u \ge 0 \end{cases} \tag{4.25}$$

Fig. 4.11b represents equation (4.25) in which the current I_n has been replaced by the normalized variable $\frac{I_n}{I_0}$. By defining the total incremental current variation as $\Delta I_n = I_n \pm \frac{I_0}{2}$, equation (4.25) becomes:
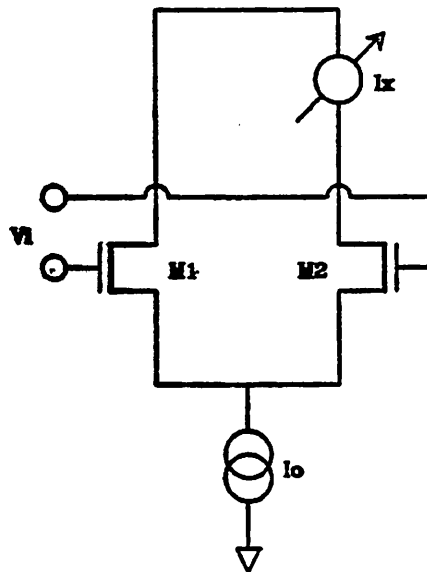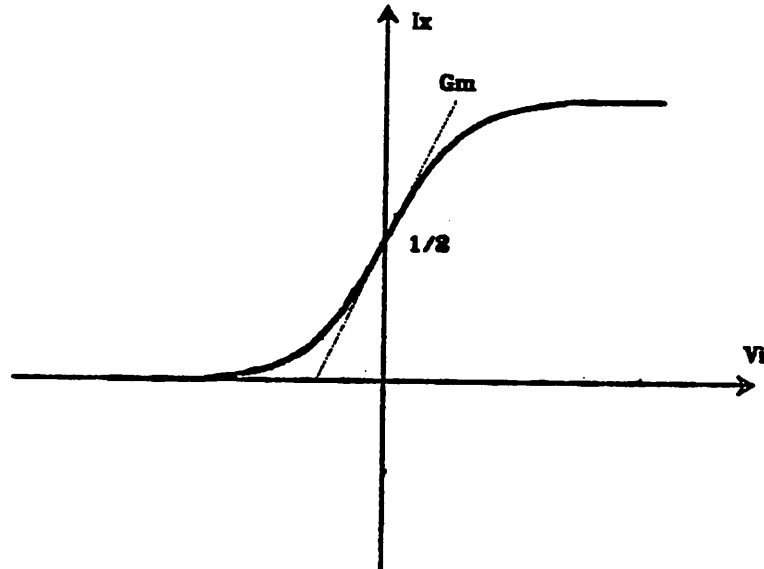

Figure 4.11a NMOS Differential Pair

Figure 4.11b. Differential Pair Transfer Function

$$\Delta I_n = I_0 \sqrt{1-(1-u^2)^2} \qquad (4.26)$$

As was previously explained, each sign multiplier is composed of two differential amplifiers that are clocked by supplementary signals (180° out of phase). At the same time, complementary clocks (90° out of phase) are used to drive the corresponding pairs between sign multipliers, as shown in Fig. 4.12. The next step is to integrate the sum of the currents of each pair developed at the output of the loop filter. From the mathematical point of view, this is equivalent to performing an integration of equation (4.26) in the time domain. The variation of this integrated current with respect to the phase and amplitude is the desired gain transfer functions.

The input voltage v_{in} is a periodic waveform of the angular frequency ω and the phase difference φ with respect to the clock: $v_{in} = V_{pk}\sin(\omega t + \varphi)$. For this type of sign multiplier with two differential amplifiers, the transconductance β
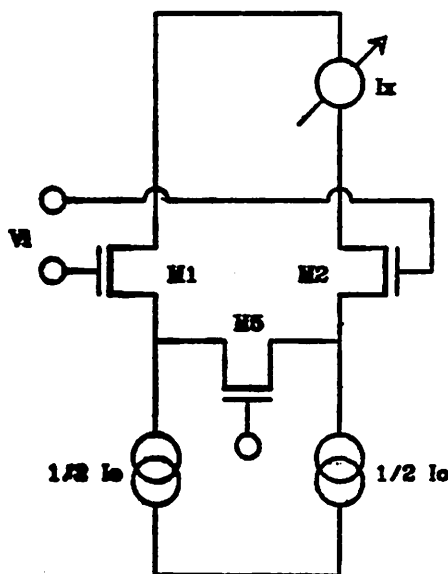
Figure 4.12. Differential Pair for the Comparators

found in the definition of the normalized variable u, is not constant. The clock makes the β of pair A equal to a nonzero value β_0 when M_{5A} is ON and zero for the adjacent pair B (M_{5B} off). The process is reversed in the other half-cycle. In other words, the effective β of one sign multiplier is given by:

$$\beta(A) = \begin{cases} \beta_0 \text{ for } 0 \leq \omega t < \pi \\ 0 \text{ for } \pi \leq \omega t < 2\pi \end{cases}$$

$$\beta(B) = \begin{cases} 0 \text{ for } 0 \leq \omega t < \pi \\ \beta_0 \text{ for } \pi \leq \omega t < 2\pi \end{cases}$$

$$(4.27)$$

Ψ is defined as the total integrated current over the period $0 \rightarrow 2\pi$ divided by I_0:

$$\Psi = 2\int_0^{2\pi} \frac{\Delta I_n}{I_0} d(\omega t)$$

$$(4.28)$$

The factor of 2 in front of the integral sign represents the contribution of two sign multipliers per comparator. By the addition property of the integration:

$$\Psi = 2\int_0^\pi \frac{\Delta I_n}{I_0} d(\omega t) + 2\int_\pi^{2\pi} -\frac{\Delta I_n}{I_0} d(\omega t) \qquad (4.29)$$

The integrand in the second term is negative because the outputs of the differential amplifiers are cross-coupled within a sign multiplier. Using expression (4.27) and the value of v_{in} in equation (4.29), we obtain:

$$\Psi = 2\int_0^\pi \sqrt{1-(1-U_{pk}^2\sin^2(\omega t+\varphi))^2}\, d(\omega t)$$
$$\qquad\qquad (4.30)$$
$$-2\int_\pi^{2\pi} \sqrt{1-(1-U_{pk}^2\sin^2(\omega t+\varphi))^2}\, d(\omega t)$$

where $U_{pk} = \sqrt{\frac{\beta}{2}(\frac{W}{L})_{1,2}\frac{V_{pk}^2}{I_0}}$. The periodic function inside the integrand is

even, thus: $\int_\pi^{2\pi} = -\int_0^\pi$, and equation (4.30) becomes:

$$\Psi = 4\int_0^\pi \sqrt{1-(1-U_{pk}^2\sin^2(\omega t+\varphi))^2}\, d(\omega t) \qquad (4.31)$$

The solution of equation (4.31) is given by:

$$\Psi = \frac{4}{\pi} U_{pk}^2 \left\{ \cos^2\varphi \left[1+\frac{2-U_{pk}^2}{(U_{pk}\cos\varphi)^2} \right]^{\frac{1}{2}} \right.$$
$$\left. +\left[\frac{2-U_{pk}^2}{U_{pk}^2}\right]\tanh^{-1}\left[1+\frac{2-U_{pk}^2}{(U_{pk}\cos\varphi)^2}\right]^{-\frac{1}{2}} \right\} \qquad (4.32)$$

The transfer gain functions for the amplitude and phase comparators are the derivatives with respect to the amplitude V_{pk} and the phase φ of the denormalized function Ψ (multiplied by I_0):

$$K_{C_A} = \frac{\partial\Psi}{\partial V_{pk}}I_0 = \frac{\partial\Psi}{\partial U_{pk}}\frac{\partial U_{pk}}{\partial V_{pk}}I_0$$
$$= \frac{8}{\pi} U_{pk} \left\{ \cos\varphi_A \left[\cos^2\varphi_A + \frac{2-U_{pk}^2}{U_{pk}^2}\right]^{\frac{1}{2}} \right.$$
$$\left. -\tanh^{-1}\left[1+\frac{2-U_{pk}^2}{(U_{pk}\cos\varphi_A)^2}\right]^{-\frac{1}{2}} \right\} \frac{\partial U_{pk}}{\partial V_{pk}}I_0 \qquad (4.33)$$
$$K_{C_P} = \frac{\partial\Psi}{\partial\varphi}I_0 = -\frac{8}{\pi} U_{pk}^2\sin\varphi_P \left[\cos^2\varphi_P + \frac{2-U_{pk}^2}{U_{pk}^2}\right]^{\frac{1}{2}} I_0$$

The different subindexes A and P indicate the different phase angles for the

amplitude and phase comparators that are in quadrature, as explained in Chapter 2. This can also be seen from expressions (4.33) which are maximized when $\varphi_A = 0$ and $\varphi_P = \dfrac{\pi}{2}$.

In order to calculate the elements of the loop filter the value of U_{pk} (or V_{pk}) must be known. But in the general case in which the VLL has to track a variable amplitude, U_{pk} (or V_{pk}) is not defined. Instead, a maximum value consistent with the relative signal magnitudes is used for the design in order to keep the whole system operating in the linear range ($U_{pk} < 1$).

Equation (4.24) was derived based on a conventional source coupled pair such as the one shown in Fig. 4.11, but the actual configuration chosen for the comparators (see Fig. 4.12) adds an extra component of resistance r_s corresponding to the switch between the sources of the differential amplifier. The original value of U_{pk} can be written as follows:

$$U_{pk} = \sqrt{\frac{\beta}{2}\left(\frac{W}{L}\right)_{1,2}\frac{V_{pk}^2}{I_0}} = \sqrt{2\beta\left(\frac{W}{L}\right)_{1,2}I_0}\ \frac{V_{pk}}{2I_0}$$

$$= g_{m1,2}\ \frac{V_{pk}}{2I_0}$$

The effect of the resistance r_s is included in $g_{m1,2}$:

$$g'_{m1,2} = \left(\frac{1}{g_{m1,2}} + r_s\right)^{-1}$$

Replacing in equation (4.33) the corresponding steady-state values of $\varphi_A = \dfrac{\pi}{2}$, $\varphi_P = \dfrac{\pi}{2}$ and U_{pk} gives the following:

$$K_{C_A} \approx \frac{4\sqrt{2}}{\pi} g'_{m1,2}$$

$$= \frac{4\sqrt{2}}{\pi} 9.10 \times 10^{-5}$$

$$K_{C_P} \approx \frac{4\sqrt{2}}{\pi} g'_{m1,2} V_{pk}$$

$$= \frac{4\sqrt{2}}{\pi} 9.10 \times 10^{-5} V_{pk}$$

The numerical values used for computing $g'_{m1,2}$ are based on $(\frac{W}{L})_{1,2} = \frac{90}{8}$, $\beta = 3.0 \times 10^{-5}$ and $I_0 = 2I_u = 8.0 \times 10^{-5}$ (I_u is the current generated by a unit depletion transistor with a $\frac{W}{L} = \frac{12}{40}$) which yields:

$$r_s = \frac{1}{\beta_s (\frac{W}{L})_5 (V_{GS_5} - V_{TH_g})}$$

$$= \frac{1}{3.0 \times 10^{-5} \times \frac{10}{6} \times 3} = 6.66 k\Omega$$

4.4.2. Phase (Amplitude) Transfer Gain of the VCO

The next step is to derive the expressions for the transfer gain of the phase and amplitude portions of the VCO, based on the small signal model of the integrators (Fig. 4.7). The open loop transfer gain of the integrator is given by:

$$h_o(s) = \frac{v_o}{v_i} = \frac{g_{m1}(g_{m2} Z_f - 1)}{g_{m2} + Z_f Y_l Y_i + Y_i + Y_l} \tag{4.34}$$

After expanding the admittances Y's and impedance Z_f in their composing elements, we obtain the following:

$$h_o(s) = k \frac{s\tau_1 + 1}{a_3 s^3 + a_2 s^2 + a_1 s + 1} \tag{4.35}$$

where:

$$k = \frac{g_{m1} g_{m2}}{G_l G_i}, \quad \tau_1 = C(R - \frac{1}{g_{m2}}), \quad a_3 = \frac{RC_i C_l C}{G_l G_i}, \quad a_2 = RC(\frac{C_i}{G_l} + \frac{C_i}{G_i}) + \frac{C_i C_l}{G_l G_i} \text{ and}$$

$$a_1 = C(R + \frac{1}{G_l} + \frac{1}{G_i} + \frac{g_{m2}}{G_l G_i}).$$

Obviously the denominator of h_o will be of a higher order if other parasitic elements not shown in Fig. 4.7 are considered, but such an expansion is unnecessary, in fact further simplification can be done without loss of generality.

As was previously mentioned, the VCO is implemented by connecting two integrators back-to-back (Fig. 4.13). The transfer function of this system, $H_c(s)$, can be found by using the classical expression of feedback theory:

$$H_c(s) = \frac{v_o}{v_i} = \frac{h_{1o}(s)h_{2o}(s)}{1+h_{1o}(s)h_{2o}(s)} \qquad (4.36)$$

The closed-loop transfer function in the s domain is derived by replacing the value of the h_o's found in expression (4.35). To obtain the time domain response for an input step (or a decaying exponential, in general), the closed loop expression has to be multiplied by $\frac{1}{s}$ or $\frac{1}{s-a}$ respectively. The resulting expression is of the type $\frac{p(s)}{q(s)}$ where $q(s)$ is represented as a factorized polynomial: $q(s) = (s-\alpha_1)(s-\alpha_2) \ldots (s-\alpha_m)$. The time domain response is the Laplace anti-transformation:
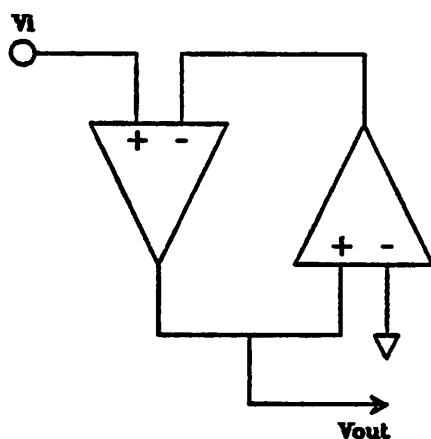

Figure 4.13. Active Resonators

$$x_C(t) = \sum_{n=1}^{n=m} \frac{p(\alpha_n)}{q'(\alpha_n)} e^{\alpha_n t} \tag{4.37}$$

In any real feedback system, the roots α_i's are either complex conjugate ($\alpha_1 = \overline{\alpha_2}$) or real. Hence the expression (4.37) can also be written as:

$$x_C(t) = X_{pk} \sum_{n=1}^{n=m} e^{[Re(\alpha_n)t + \vartheta_n]} \sin[Im(\alpha_n)t + \psi] \tag{4.38}$$

where the $Re(\alpha)$'s and $Im(\alpha)$'s are the real and imaginary parts of the roots α's respectively, X_{pk} the peak value of the signal, and ϑ and ψ real constants. The index m is now the sum of the total number of pairs of the complex and individual real roots. For the particular element values found in our case, the real part of the higher order roots lies in the left-half plane. Such a condition makes all the terms but one in equation (4.38) decay to zero because of the real exponential.

To compute the roots of the polynomial denominator $q(s)$, a simplified model of the integrators is used in which the only source of extra phase-shift is the transmission zeroes (this simplification is equivalent to having the capacitive part of the loading admittances Y_l and Y_i equal to zero):

$$h_o(s) = k\frac{s\tau_1 + 1}{s\tau_2 + 1} \tag{4.39}$$

where τ_1 was previously defined with equation (4.35) and $\tau_2 = C\dfrac{g_{m2} + RG_l\,G_i + G_i + G_l}{G_l\,G_i}$

The expression $h_o(s)$ given by equation (4.39) is replaced twice in equation (4.36) in order to obtain the coefficients of the polynomial denominator $q(s)$ ($h_{1o}(s) = h_{2o}(s) = h_o(s)$ because the integrators are considered identical):

$$q(s) = s^2 + 2\left(\frac{\tau_2 + k^2\tau_1}{\tau_2{}^2 + k^2\tau_1{}^2}\right)s + \frac{1 + k^2}{\tau_2{}^2 + k^2\tau_1{}^2} \tag{4.40}$$

which can be abbreviated as:

$$q(s) = s^2 + 2\rho\omega_0 s + \omega_0{}^2 \tag{4.41}$$

where the natural angular frequency ω_0 and the damping factor ρ are given by:

$$\omega_0 = \left[\frac{1+k^2}{\tau_2^2+k^2\tau_1^2}\right]^{\frac{1}{2}}$$

$$\rho = \frac{1}{\sqrt{1+k^2}}\frac{\tau_2+k^2\tau_1}{\sqrt{\tau_2^2+k^2\tau_1^2}}$$

(4.42)

Now it becomes easy to find the roots of $q(s)$, and equation (4.38) can be written as:

$$x_0(t) = v_{in}(t) = V_{pk}e^{-(\rho\omega_0 t+\vartheta)}\sin(\omega_0\sqrt{1-\rho^2}t+\psi)$$

(4.43)

where X_{pk} is replaced by the actual value of the peak voltage V_{pk}.

(1) *Amplitude transfer gain*

The amplitude-gain constant of the VCO is defined as the variation of the rate of change $R(v_{in})$ of the signal amplitude with respect to the amplitude controlling voltage V_P (the gate voltage of M_8). This rate of change is given by the partial derivative of v_{in} with respect to time:

$$R[v_{in}(t)] = \frac{\partial v_{in}(t)}{\partial t} = -V_{pk}\rho\omega_0 e^{-(\rho\omega_0 t+\vartheta)}\sin(\omega_0\sqrt{1-\rho^2}t+\psi')$$

(4.44)

where $\psi' = \psi+\tan^{-1}(\frac{\sqrt{1-\rho^2}}{\rho})$, which is valid as long as $\rho < 1$. The gain constant is computed at $t = 0$ using the quasi-static condition $\rho = 0$ (constant amplitude):

$$
\begin{aligned}
K_{VCO_A} &= \frac{\partial[R(v_{in}(t))]}{\partial V_A}\bigg|_{\substack{t=0\\\rho=0}} \approx V_{pk}\frac{\partial(\rho\omega_0)}{\partial V_A}\bigg|_{\rho=0}\\
&= V_{pk}\,\omega_0\frac{\partial\rho}{\partial V_A}\bigg|_{\rho=0} + V_{pk}\,\rho\frac{\partial\omega_0}{\partial V_A}\bigg|_{\rho=0}\\
&= V_{pk}\,\omega_0\frac{\partial\rho}{\partial V_A}\bigg|_{\rho=0}\\
&= V_{pk}\,\omega_0 k^2\frac{\tau_2^2-\tau_1\tau_2}{(\tau_2+k^2\tau_1)(\tau_2^2+k^2\tau_1^2)}\frac{\partial\tau_1}{\partial V_A}\bigg|_{\rho=0}
\end{aligned}
$$

(4.45)

Equation (4.42) shows that the steady-state condition $\rho = 0$ is equivalent to $\tau_2 = -k^2\tau_1$, which is used in equation (4.45) to yield:

4.4.3. Calculation of the Loop-Filter Elements

The next step is to combine the gain constants of the phase and amplitude comparators with the values just found for the phase and amplitude portions of the VCO. As was previously stated, the open loop transfer function of the phase and amplitude loops is of the type $\frac{1+s\,\tau_n}{s\,\tau_d}$ (integrator with phase correction network). Thus the significant constants that describe the dynamics of the whole system are given by:

$$2\zeta\omega_n = K^{(C)}K^{(VCO)}R_n$$
$$\omega_n^2 = \frac{K^{(C)}K^{(VCO)}}{C_n} \tag{4.48}$$

where C_n is the integrating capacitor of the loop filters and R_n is the resistance of transistor M_8 in series with C_n.

In order to find the values of the elements of the loop filter, equations (4.48) can be combined to yield the damping factor ζ :

$$\zeta = \frac{1}{2}R_n\sqrt{K^{(C)}K^{(VCO)}C_n} \tag{4.49}$$

The individual expressions of ζ for the amplitude and phase loops are the following:

$$\zeta_A = \frac{1}{2}R_{nA}\sqrt{K_{C_A}K_{VCO_A}C_{nA}}$$
$$\zeta_P = \frac{1}{2}R_{nP}\sqrt{K_{C_P}K_{VCO_P}C_{nP}} \tag{4.50}$$

which lead to:

$$C_{nA} = \left(2\frac{\zeta_A}{R_{nA}}\right)^2 \frac{1}{K_{C_A}K_{VCO_A}}$$
$$C_{nP} = \left(2\frac{\zeta_P}{R_{nP}}\right)^2 \frac{1}{K_{C_P}K_{VCO_P}} \tag{4.51}$$

The phase margin and peaking of the loop is a direct function of the value of ζ [16]. The maximally flat amplitude response corresponds to a value of $\zeta=\frac{1}{\sqrt{2}}$ and

a phase margin of $\frac{\pi}{4}$. A safety margin of ≈ 2 is used to compensate for any

component-value spread, so that $\zeta = \sqrt{2}$. The resistor R_n is layed out as a $\frac{10}{80}$

self-biased depletion transistor that has a resistance value of $100k\Omega$; and the

oscillation amplitude is $V_{pk} = 0.1 V$, thus:

$$C_{nA} = 158pF$$
$$C_{nP} = 50pF$$

Since the phase and amplitude comparators are identically layed out, an average

value of $100pF$ was chosen for both capacitors, that is $C_{nA} = C_{nP} = 100pF$, therefore:

$$\zeta_A = 1.12$$

$$\zeta_P = 2.00$$

It is interesting to compute the natural frequencies of both loops using equation (4.48):

$$\omega_{n_A} = 2.25 \times 10^5 \frac{rad}{sec} \cong 35kHz$$

$$\omega_{n_P} = 4.00 \times 10^5 \frac{rad}{sec} \cong 63kHz$$

4.5. Noise Calculations

Chapter 3 described the derivation for the model used to estimate the power

spectral density of the additive and phase components of the noise present at the

VCO output. MOS operational amplifiers present an input-referred noise spectrum

that is similar to that of a single transistor. This referred input power spectrum

has a similar expression to that of equation (3.24):

$$v_n^2(f) = \begin{cases} \dfrac{\alpha'}{f} & \text{for } 0 \leq |f| < f_F \\ \beta' & \text{for } f_F \leq |f| \end{cases} \qquad (4.52)$$

The constant $\alpha' = V_f^2$ (flicker component) expressed in V^2 for an MOS device is given

by:

$$\alpha' = V_f^2 = \frac{K_f}{WLC_{OX}} \tag{4.53}$$

where K_f is a constant that depends on the process ($\approx 10^{-24}$ in our case), C_{OX} is

the oxide capacitance $(4.92 \times 10^{-8} \frac{F}{cm^2})$ and W and L are the channel width and

length of the transistor respectively. The constant term β', expressed in $\frac{V^2}{Hz}$ otherwise known as the thermal or Johnson component, is given by:

$$\beta' = 4kT(\frac{2}{3g_m})f_F \tag{4.54}$$

where k is the Boltzmann constant (1.38×10^{-23}), T the absolute temperature and g_m the transconductance of the transistor. The total input referred noise for each of the two components is given by [17]:

$$V_{eq_{TOT}}^2 = V_{eq_1}^2 + V_{eq_2}^2 + \left[(g_{m11})(\frac{1}{g_{m1}} + \frac{1}{g_{o5}})\right]^2 (V_{eq_{11}}^2 + V_{eq_{12}}^2) \tag{4.55}$$

where the subindices correspond to the numbers assigned to the transistors of the integrator shown in Fig. 4.3. Equation (4.55) is used together with equation (4.53) to find the total input-referred flicker component:

$$
\begin{aligned}
V_{f_{TOT}}^2 &\approx 2V_f {}_1^2 + \left[(g_{m11})(\frac{1}{g_{m1}} + \frac{1}{2g_{o5}})\right]^2 2V_f {}_{11}^2 \\
&\approx 2V_f {}_1^2 + \left[\frac{g_{m11}}{g_{o5}}\right]^2 V_f {}_{11}^2 \\
&= \left[\frac{2K_f}{(WL)_1 C_{OX}} + \left[\frac{\sqrt{2\beta_{11}(\frac{W}{L})_{11} I_{11}}}{C\omega_0}\right]^2 \frac{K_f}{(WL)_{11} C_{OX}}\right] \\
&= 5.7 \times 10^{-11} \ (V^2)
\end{aligned} \tag{4.56}
$$

where g_{o5}, the ON conductance of transistor M_5 is calculated using the integrating capacitor C and the oscillating frequency ω_0 $(g_{o5} = \omega_0 C)$.

The thermal component of the total input referred noise is calculated using equations (4.55) and (4.54) as follows:

$$V_{th_{TOT}}^2 = \left\{ 4kT\frac{4}{3}(\frac{1}{g_{m1}} + \frac{1}{2g_{o5}}) + \left[(g_{m11})(\frac{1}{g_{m1}} + \frac{1}{2g_{o5}})\right]^2 2\times4kT\frac{1}{3g_{m11}} \right\}$$

$$\approx \left[4kT\frac{2}{3}(\frac{1}{g_{o5}}) + \left[\frac{g_{m11}}{g_{o5}}\right]^2 4kT \frac{1}{3g_{m11}} \right]$$

$$= \left[4kT\frac{2}{3}(\frac{1}{C\omega_0}) + \left[\frac{\sqrt{2\beta(\frac{W}{L})_{11}I_{11}}}{C\omega_0}\right]^2 4kT \frac{1}{3\sqrt{2\beta(\frac{W}{L})_{11}I_{11}}} \right] \quad (4.57)$$

$$= 1.0\times10^{-15} \ (\frac{V^2}{Hz})$$

The breakpoint of the power noise spectrum of the additive and phase components of the VCO occurs where the thermal and flicker contributions become equal, or: $V_{th_{TOT}}^2 = V_{f_{TOT}}^2$. From equations (4.56) and (4.57) we obtain:

$$f_F = \frac{V_{f_{TOT}}^2}{V_{th_{TOT}}^2}$$
$$= \frac{5.7\times10^{-11}}{1.0\times10^{-15}} \quad (4.58)$$
$$= 5.7\times10^4 \ (Hz)$$

All the necessary parameters for the calculation of equations (3.26), (3.42), (3.44), (3.46), (3.47) and (3.48) are available. As an example, we will calculate the improvement of the total integrated phase and amplitude noise of the VCO due to the action of the VLL loops (equation (3.48). The value of f_Z will be arbitrarily chosen to be $1kHz$.

(1) *Phase Loop*

$$\eta_{P_0} = \frac{I_{2_P} + I_{3_P}}{I_{2_P}' + I_{3_P}'}$$
$$= \frac{1.07\times10^{-20}+1.23\times10^{-20}}{2.28\times10^{-18}+2.00\times10^{-18}} \quad (4.59)$$
$$= 1.00\times10^{-4} = -80dB$$

(2) *Amplitude Loop*

$$\eta_{A_0} = \frac{I_{2_A} + I_{3_A}}{I_{2_A}{}' + I_{3_A}{}'}$$

$$= \frac{2.07 \times 10^{-19} + 3.92 \times 10^{-20}}{2.28 \times 10^{-16} + 2.00 \times 10^{-18}}$$

$$= 1.07 \times 10^{-3} = -60 dB$$

(4.60)

CHAPTER 5

THE FILTER DESIGN

5.1. Motivation

The main goal of this project was to design a band-pass filter using a replica technique similar to the one previously reported by Tan and Gray [18]. In this case a low-pass filter, together with a harmonic PLL, were built in the same chip (Fig. 5.1). The value of the constants of the integrators, which were two-stage operational amplifiers working in open loop, were varied by using the error signal of the PLL to adjust the transconductance of the first stage within each amplifier. Since all the first stages were matched, the integrating constants were made proportional to the clock frequency by choosing the proper ratioed capacitors in the second stage of the integrators.

Since the ratio between the operating frequency of the filter and the unity gain bandwidth of the second stage of the amplifiers was low (low Q), the errors resulting from the excess phase-shift were negligible, thus eliminating the need for controlling the phase shift within each integrator. In the VCO, which is the equivalent of an unloaded filter (infinite Q), the excess phase-shift generated a growing exponential at the output, so that a limiter was introduced to avoid saturation. But if the ratio had been closer to unity, or the Q filters higher, it would have also been necessary to control the phase-shift within each integrator. This is where the concept of the VLL, which allows a closed loop control over both the frequency and amplitude of the VCO, was applied to implement the new, two-variable replica system.
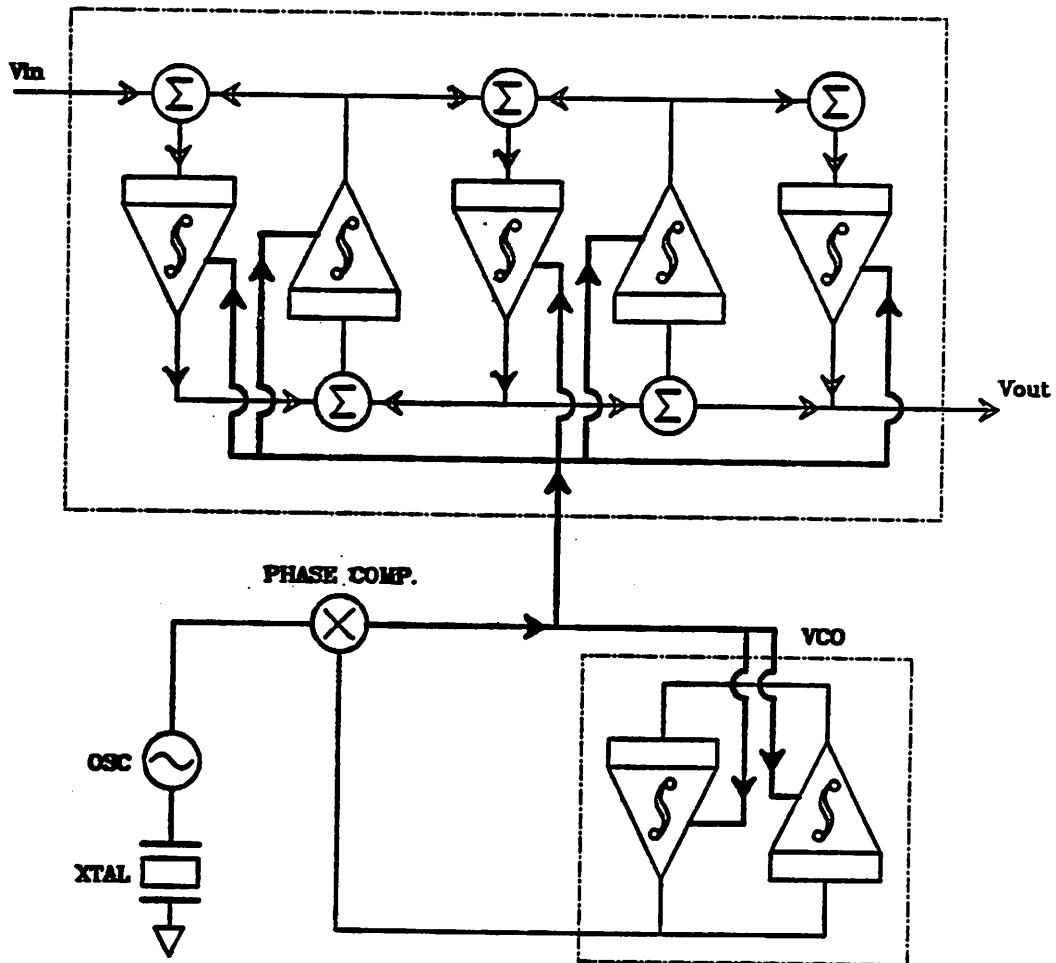
Figure 5.1. Single-Variable Replica Filter

The two-variable replica system is represented in Fig. 5.2. It is composed of a VLL (*master* filter) running at the same frequency as the center of the passband of the filter section. The sixth order elliptic filter (*slave* filter) is an active implementation of an LC ladder using the same integrators as those in the VCO (this will be described later). The pole-zero constellation is shown in Fig. 5.3. The matching requirements between the master and slave can be seen from two different points of view:

Figure 5.2. Two-Variable Replica Filter

Circuitry: Matching the nominal, equivalent components at two levels, namely: *microscopic* (capacitance, transconductance, etc.) and *macroscopic* (integrators, phase and amplitude detectors, etc.)

Layout: The variation of the values of parasitics encountered in two nominally identical circuits with different layouts can be very significant. Consequently, the difference between the normal operating points of these circuits can also be very significant.
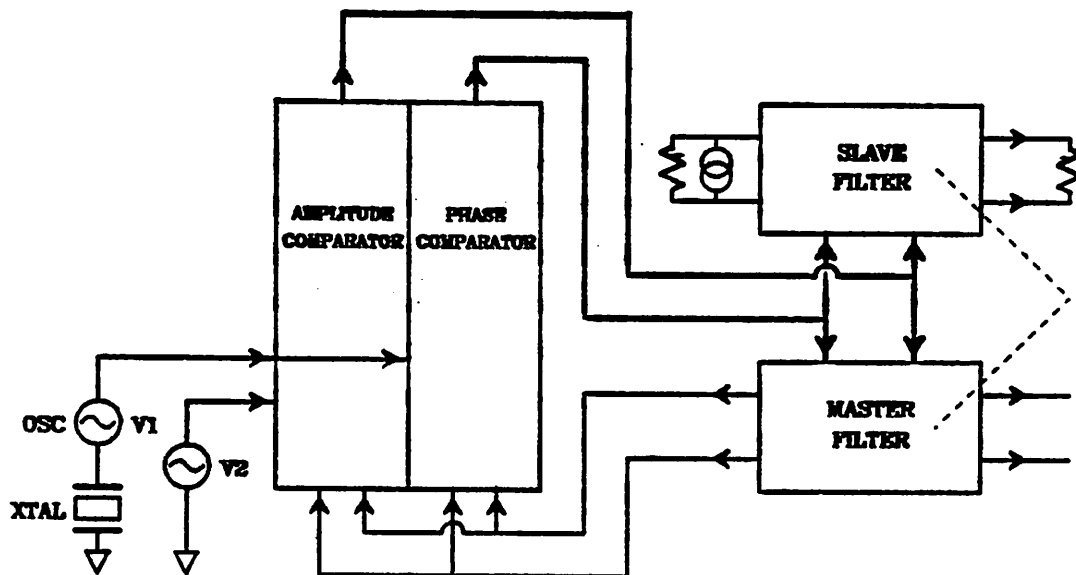
Another way of explaining the action of the VLL is as follows: the departure of the phase-shift from the ideal 90°, or the transconductance from the nominal values in each integrator, tends to move the poles and zeroes of the master and slave filters in horizontal or vertical directions, respectively (Fig. 5.4). Thus, for this particular application, the function of the VLL is to adjust the position of the singularities in the (σ, ω) plane of the master filter in order to control the corresponding singularities of the slave filter. This tracking mechanism is aided
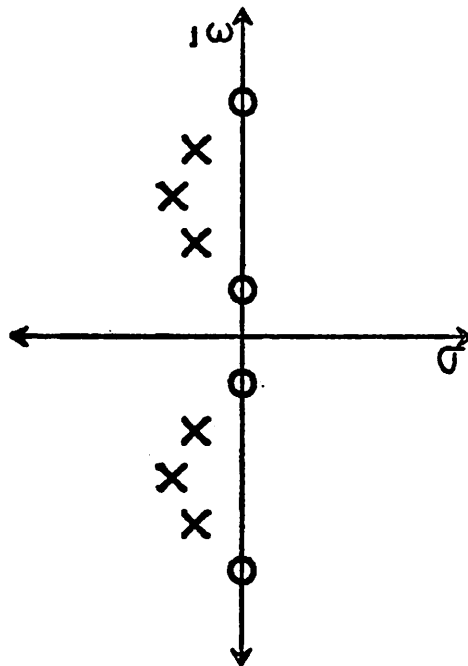
Figure 5.3. Bandpass Pole-Zero Location

by the good matching properties between devices of identical layout in a monolithic implementation.

In principle, the VCO should consist only of a pair of integrators that form the resonator. However the sixth-order filter needs three interconnected resonators, each one having different loading conditions. This could affect the matching performance between the blocks corresponding to the master and slave filters. A solution to this intrinsic mismatch is to compute the different loading effects of the interconnections and then replicate them on the VCO by lumped elements. Another approach is to implement the VCO as a lossless network identical to the slave filter representing a complex structure of six integrators. In this last approach, the only difference between the master and slave filters is that in the first one the elements representing the losses, i.e., the terminations, are
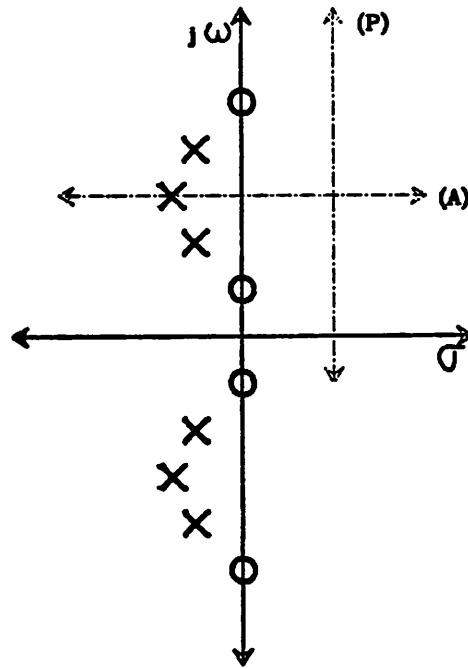
Figure 5.4. Effect on the Pole-Zero Location by the Two Loops

removed. The ideal pole-zero location of this master filter is shown in Fig. 5.5. This is a costly solution in terms of real estate, but it is very attractive from the following points of view:

Design confidence

There is no need for computing the effects of the different loading conditions of the resonators within the filter in order to reproduce them in the design of the VCO.

Turn-around time

The design stage, which includes simulation and layout, can be expedited considerably if automated design tools are used. For example, in our case
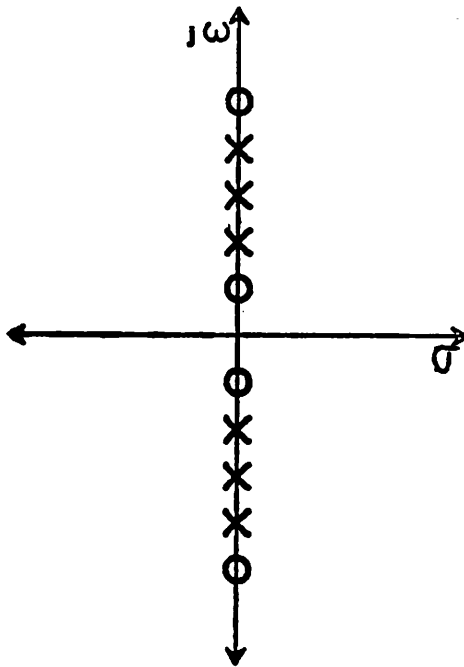
Figure 5.5. Pole-Zero Location of Lossless Filter

the whole filter was reproduced twice by means of a simple command in the layout program (the modification for removing the terminations was trivial).

5.2. Filter Design

The specifications of a band-pass filter are usually represented using a tolerance scheme such as the one shown in Fig. 5.6. The filter frequency response has to be circumscribed to the clear areas. A minimum stopband rejection of $40dB$ and bandwidth of $9.0kHz$ are typical specifications for an IF strip of a medium-priced AM receiver.

Based on these specifications, a table of normalized filters [19] having entries corresponding to the order of the filter and nominal reflection values (or ripple)
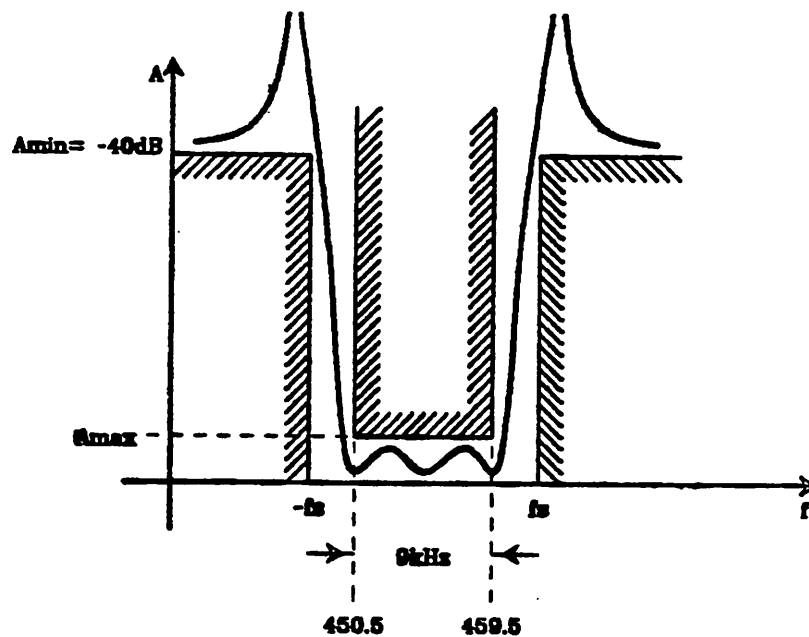
Figure 5.6. Tolerance Scheme

was used. Since this table only lists low-pass filters, a low-pass to band-pass transformation was implemented. This transformation consists in converting each capacitor and inductor into a parallel and series resonator, respectively (Fig. 5.7). The transformation equations are the following:

$$C_p = qC' \frac{1}{R_r \omega_r} \tag{5.1a}$$

$$L_p = \frac{1}{qC'} \frac{R_r}{\omega_r} \tag{5.1b}$$

$$L_s = qL' \frac{R_r}{\omega_r} \tag{5.1c}$$

$$C_s = \frac{1}{qL'} \frac{1}{R_r \omega_r} \tag{5.1d}$$

where ω_r is the angular frequency of resonance, L' and C' the normalized values given in the catalog, q the relative bandwidth of the filter given by $q = \frac{\omega_r}{\Delta \omega}$, and
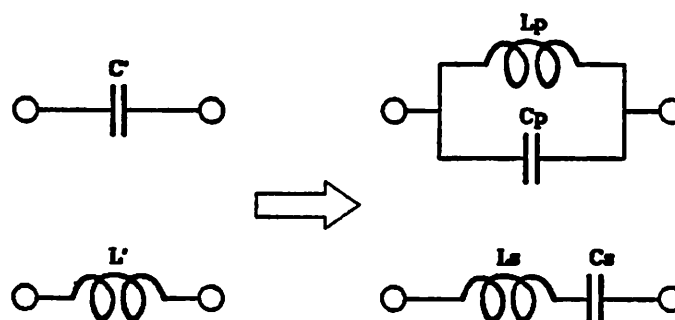
Figure 5.7. LC Low-pass to Band-pass Transformation

R_r the normalizing resistance that is assumed to be 1Ω. The normalized elliptic filter that meets the above specifications has the catalog number CC 03 25 19 [20]. Fig. 5.8 depicts the LC ladder prototype of the band-pass filter.

5.3. Active Implementation

The flow-graph that is associated with an electrical network represents the relationships between governing state variables [21]. Mason showed an analytical method for obtaining explicit equations directly from this flow-graph. However, some rules for the direct manipulation of the flow-graph that do not require the extraction of analytical expressions prove to be very useful for the transformation from an LC prototype to an active implementation [22]. In our case these rules are used for implementing several of the transformations that represent the particular characteristics of the active elements available.

Integrator characteristics

Figs. 4.3 and 4.7 show only one differential integrating input available - the one corresponding to the input-coupled pair. However, as shown in Fig. 4.7, another type of input that can be implemented is a constant multiplier,
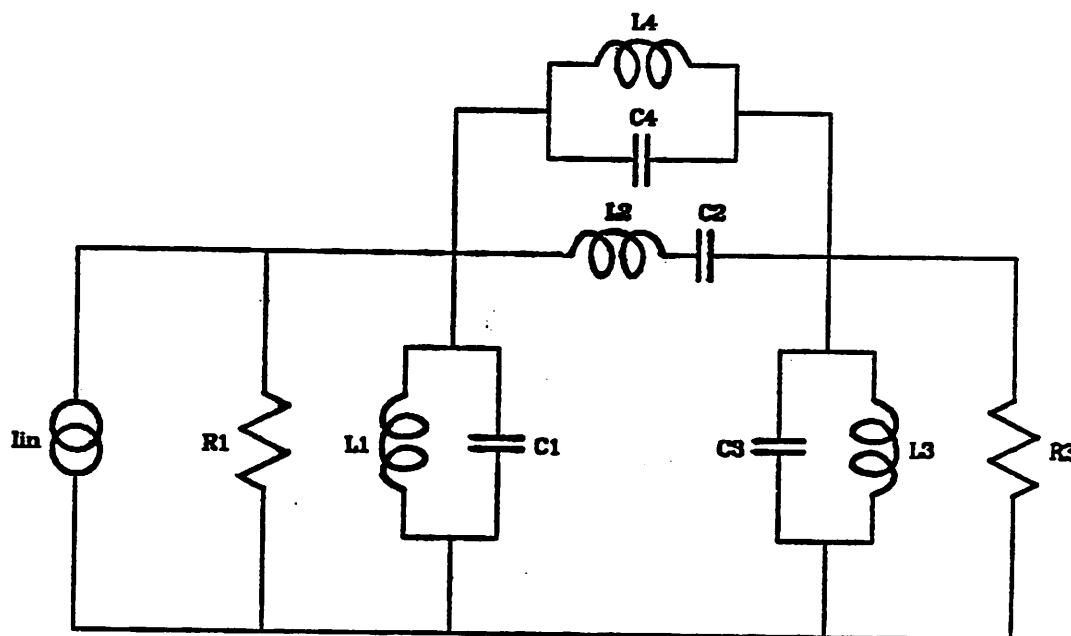
Figure 5.8. LC Ladder Prototype

consisting of a capacitor connected to the summing node of the amplifier. Since several of these capacitors can be placed, the flow-graphs have to be constructed based on this feature. Figs. 5.9a and 5.9b show the simplified, electrical model of the integrator, with the integrating constant equal to $\nu = \frac{g_m}{C}$, the two multiplying inputs $(\gamma_1 = -\frac{C_1}{C}$ and $\gamma_2 - \frac{C_2}{C})$, and the corresponding nodal flow-graph.

Flow-graph construction

A standard active implementation of the flow-graph is the direct replacement of each reactance in the LC prototype by an integrator. This requires eight integrators, six for the basic all-pole part of the network, and two for implementing the transmission zeroes. This approach, which seems simple enough, has two drawbacks:
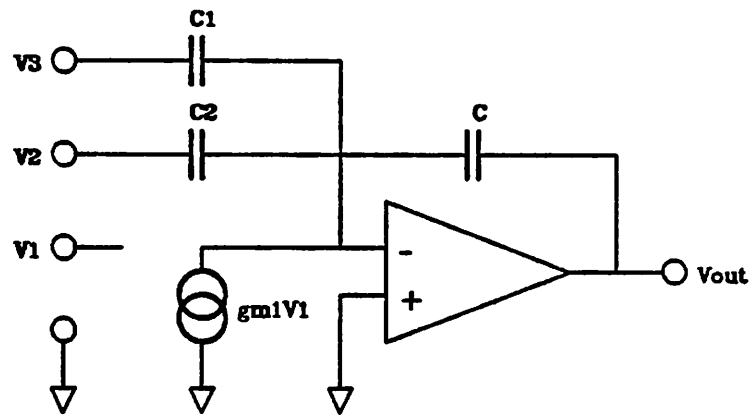
Figure 5.9a. Linear Model of Integrator
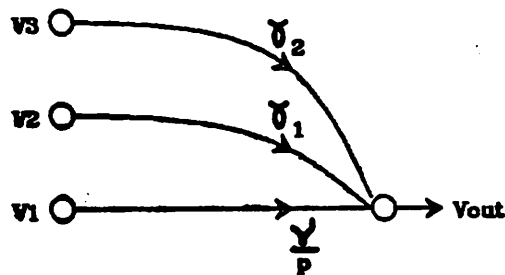
Figure 5.9b. Flow-graph Equivalent of an Integrator

(1) It requires two integrators more than the theoretical minimum, which is supposed to be equal to the order of the filter - in this case, six.

(2) It should be noted that in Fig. 5.8, L_1, L_4 and L_3 form a loop of inductances that has to be mapped into an equivalent loop of integrators. Any DC offset in the amplifiers will be amplified and may lead the outputs into saturation.

In order to avoid these drawbacks, the reactances representing the transmission zeroes are replaced by controlled generators, and an equivalent circuit constructed (Fig. 5.10), where:
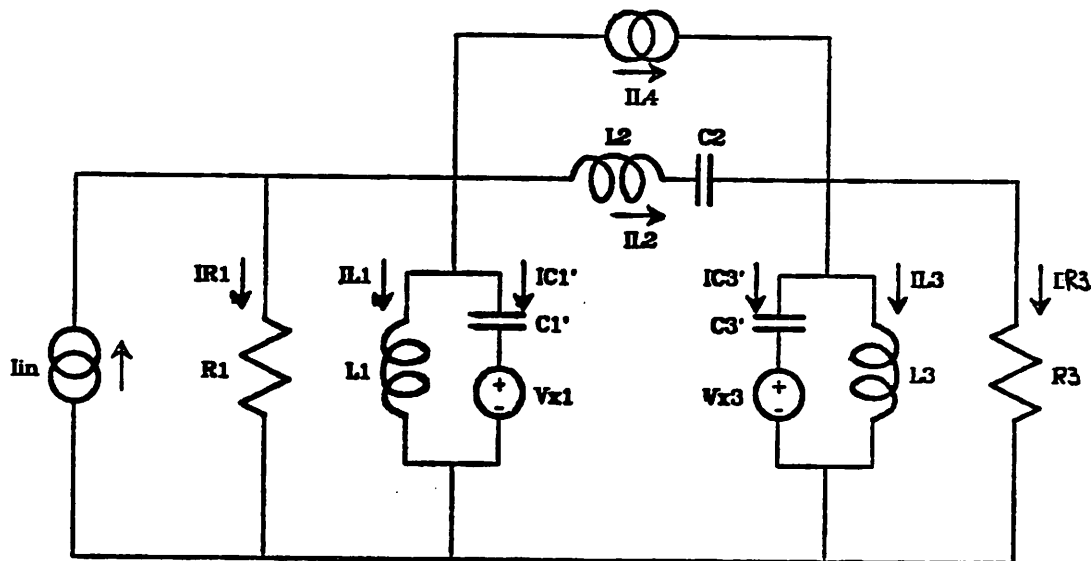
Figure 5.10. Modified LC Ladder Prototype

$$V_{x1} = \frac{C_4}{C_1 + C_4} V_3$$

$$V_{x3} = \frac{C_4}{C_3 + C_4} V_1 \tag{5.2}$$

$$I_{L4} = I_{L1} \frac{L_1}{L_4} - I_{L3} \frac{L_3}{L_4}$$

A flow-graph can then be constructed that directly represents the modified network (Fig. 5.11a). The key modification lies in the change of the connections between the branch $\frac{1}{pL_1}$ and $\frac{L_1}{L_4}$ (and $\frac{1}{pL_3}$ and $-\frac{L_3}{L_4}$) to accommodate for the particular characteristics of the integrators, as described in Fig. 5.8b. The transformation from Fig. 5.11a to 5.11b implies two approximations that are valid when the losses are low or $\frac{pL_1}{R_1} \approx 0$ (and $\frac{pL_3}{R_3} \approx 0$):

(1) In this approximation the contribution of the signal from V_1 through the path composed by branches G_1, -1 and $-\frac{L_1}{L_4}$ into the node I_{L4} (and G_3, -1 and
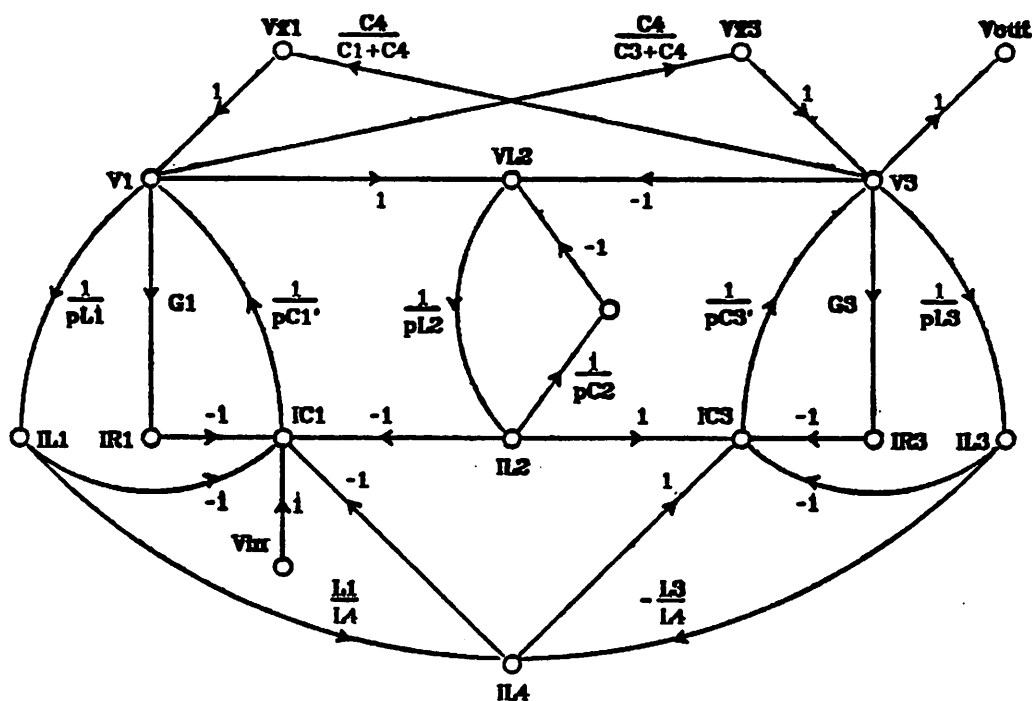
Figure 5.11a. Initial Flow-graph of LC Prototype

$\dfrac{L_3}{L_4}$ from V_3) is ignored. The net effect of this approximation can be shown as a slight shift of the transmission zeroes towards the left-half plane.

(2) In this approximation the signal input at node I_{L4} equal to $V_{in}\dfrac{L_1}{L_4}$ is ignored.

(Figs. 5.11c,d and e show the consecutive steps used to reach the topology that can be implemented with the integrators available).

The next step is to scale all the resonators to allow for identical integrators. This equalizes the signal levels in all the nodes and also eliminates large ratios for the coupling capacitors between resonators. Every node must be scaled by the desired factor, which implies that every in-coming and out-going branch to these nodes must also be respectively multiplied and divided by that number.
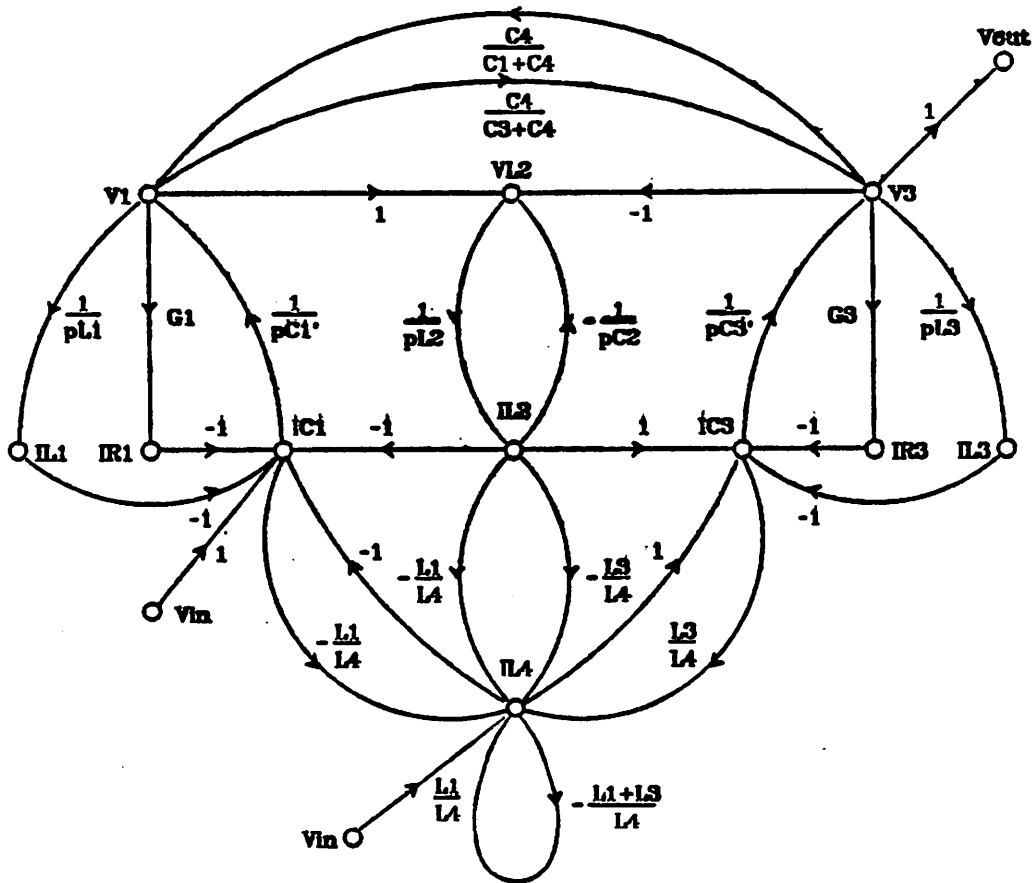
Figure 5.11b.

The node V_{L_2} in Fig. 5.11e is scaled by a factor k_2, which is obtained as follows:

$$\frac{1}{k_2 p C_2} = k_2 \frac{1}{p L_2}$$

$$k_2 = \sqrt{\frac{L_2}{C_2}}$$

(5.3)

This is combined with equations (5.1c and 5.1d) to give:

$$k_2 = \frac{1}{qL'_2 R_r}.$$ (5.4)

The normalized values shown in the catalog for the filter CC 03 25 19 are:

$C'_1 = C'_3 = 1.2880$; $L'_2 = 1.0693$; and $C'_4 = 0.0754$. The relative bandwidth q is calculated by using the limit values of the tolerance scheme shown in Fig. 5.6:

$$q = \frac{\sqrt{450.5 \times 459.5}}{9} = 50.55$$

thus:
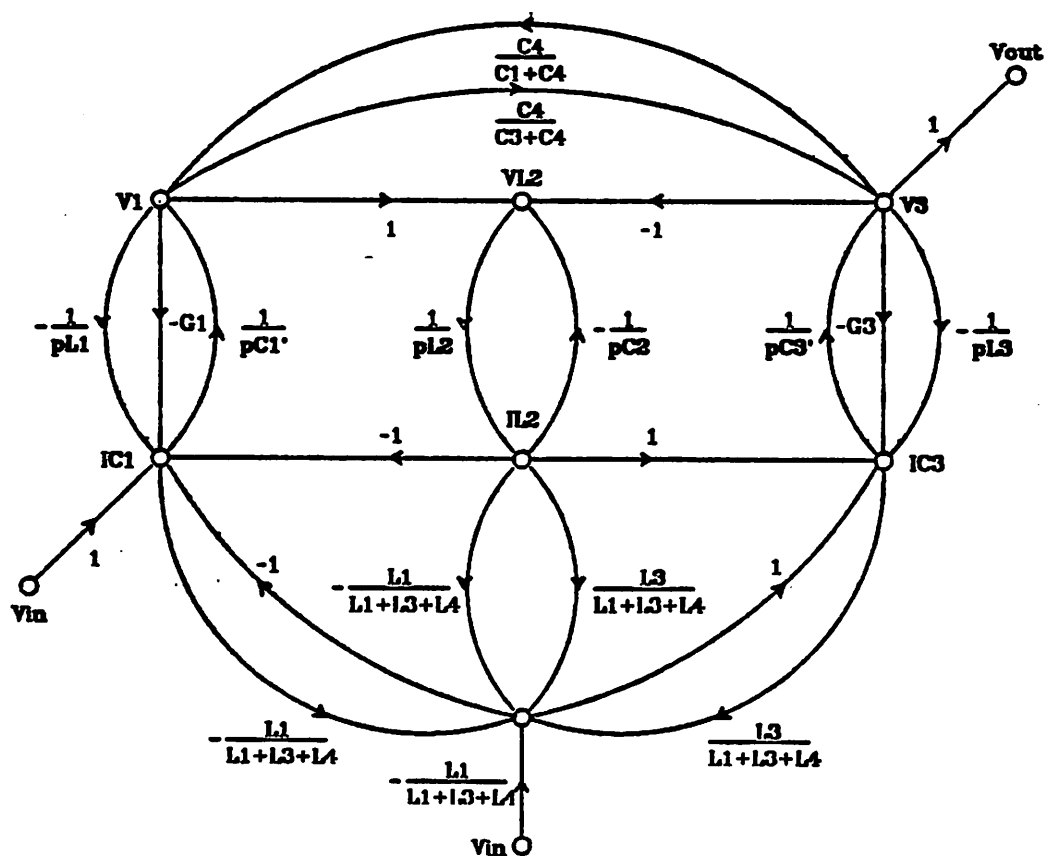
Figure 5.11c.

$$k_2 = 0.0185$$

The coupling branches (Fig. 5.11e) from the adjacent resonators that are equal to 1 have to be multiplied by this number.

The same procedure is used with nodes I_{C_1} and I_{C_3}:

(1) For I_{C_1}:

$$k_1 = \sqrt{\frac{(L_3+L_4)L_1}{(L_1+L_3+L_4)(C_1+C_4)}}$$

$$= R_r \frac{1}{q} \left[\frac{(\frac{1}{C'_3}+\frac{1}{C'_4})\frac{1}{C'_1}}{(\frac{1}{C'_1}+\frac{1}{C'_3}+\frac{1}{C'_4})(C'_1+C'_4)} \right]^{\frac{1}{2}} \quad (5.5)$$

$$= 0.01453$$

The branch representing the termination in the first resonator equal to
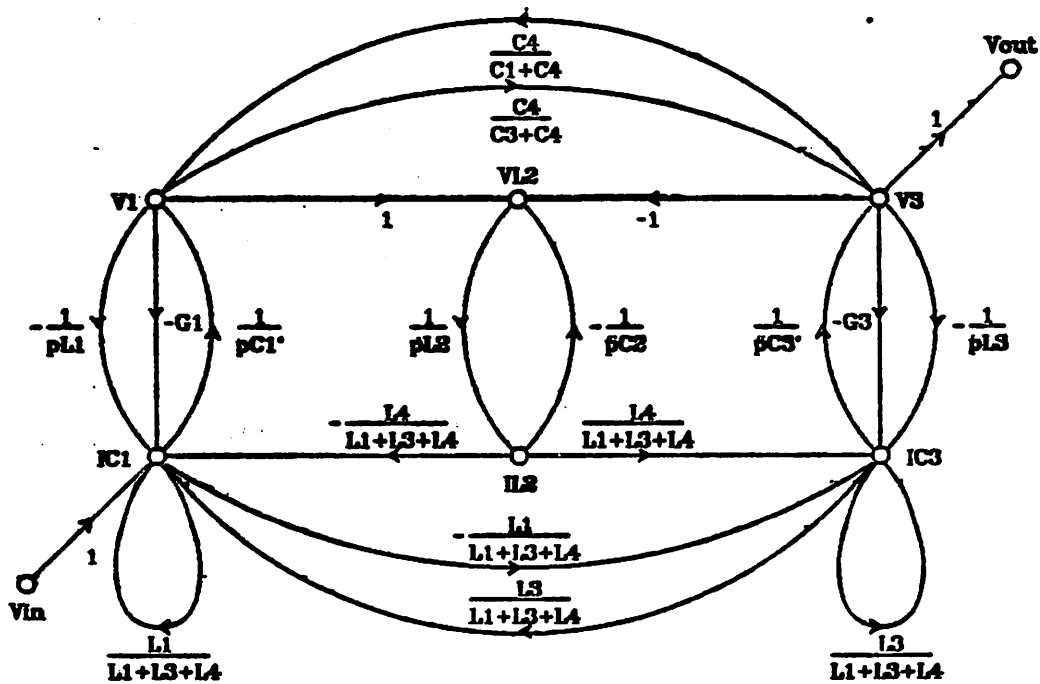
Figure 5.11d

$$-G_1 \frac{L_1 + L_3 + L_4}{L_3 + L_4} \text{ becomes a normalized } G'_1:$$

$$G'_1 = G_1 R_r \frac{1}{q} \left[\frac{(\frac{1}{C'_1} + \frac{1}{C'_3} + \frac{1}{C'_4}) \frac{1}{C'_1}}{(\frac{1}{C'_3} + \frac{1}{C'_4})(C'_1 + C'_4)} \right]^{\frac{1}{2}} \tag{5.8}$$

$$= 0.01533$$

(by definition the product $G_1 R_r = 1$).

The branch coming from the node I_{L_2} equal to $-\dfrac{L_4}{L_3 + L_4}$ becomes:
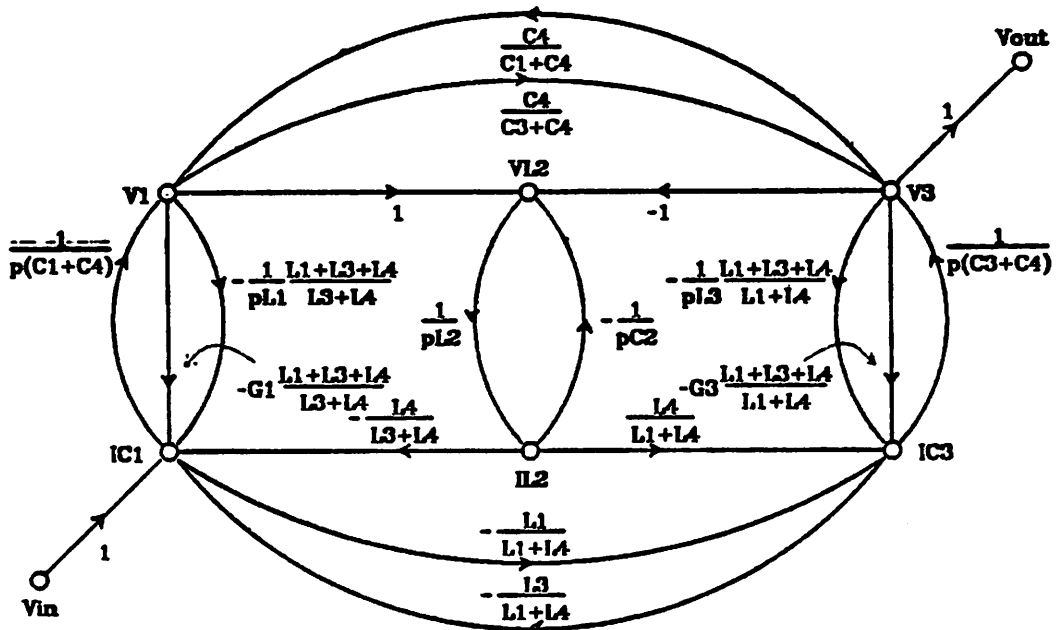
Figure 5.11e.

$$-\frac{L_4}{L_3+L_4} \rightarrow R_r \frac{1}{q} \frac{1}{C'_4} \left[\frac{\frac{1}{C'_1}}{(\frac{1}{C'_1}+\frac{1}{C'_3}+\frac{1}{C'_4})(C'_1+C'_4)(\frac{1}{C'_3}+\frac{1}{C'_4})} \right]^{\frac{1}{2}} \quad (5.7)$$

$$\rightarrow 0.01373$$

(2) For I_{C_3}:

$$k_3 = \sqrt{\frac{(L_1+L_4)L_3}{(L_1+L_3+L_4)(C_3+C_4)}}$$

$$= R_r \frac{1}{q} \left[\frac{(\frac{1}{C'_1}+\frac{1}{C'_4})\frac{1}{C'_3}}{(\frac{1}{C'_1}+\frac{1}{C'_3}+\frac{1}{C'_4})(C'_3+C'_4)} \right]^{\frac{1}{2}} \quad (5.8)$$

$$= 0.01453$$
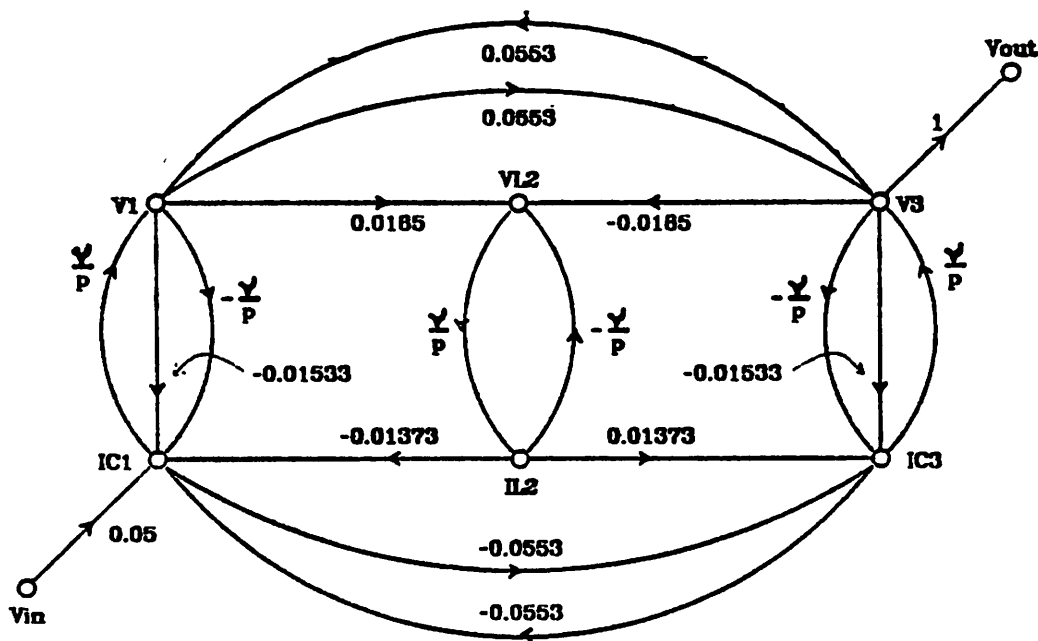
Figure 5.11f. Final Flow-graph
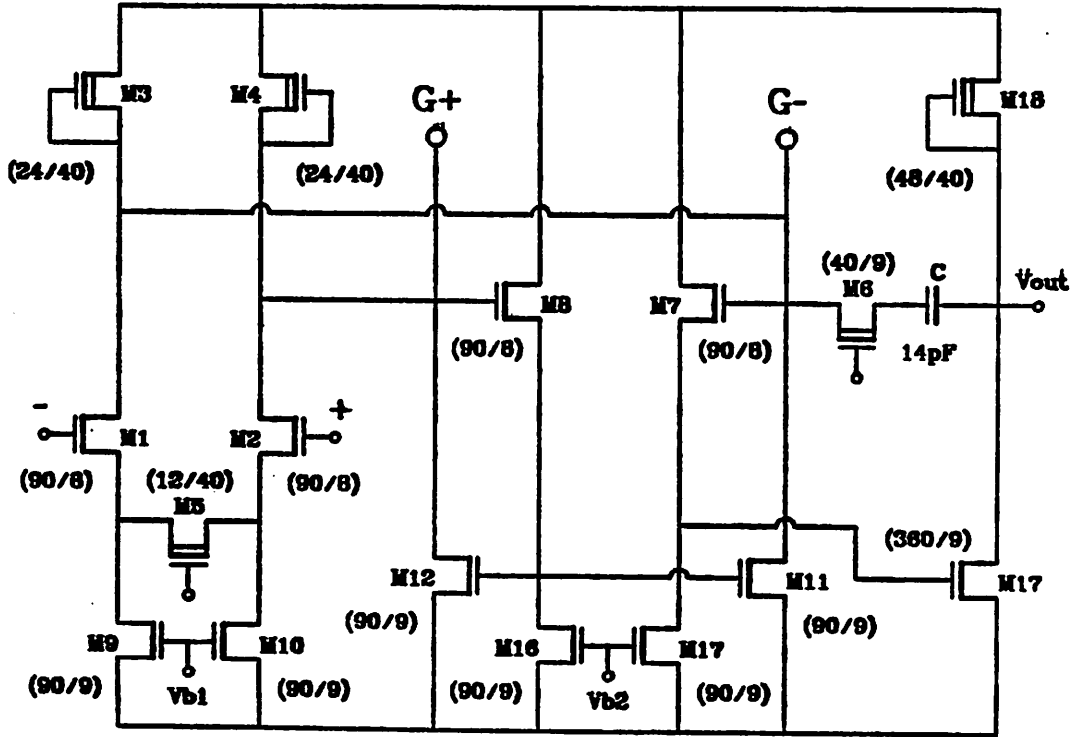
Figure 5.12. Integrator Showing Multiplying Inputs

$$G'_3 = G_3 R_r \frac{1}{q} \left[\frac{(\frac{1}{C'_1} + \frac{1}{C'_3} + \frac{1}{C'_4}) \frac{1}{C'_3}}{(\frac{1}{C'_1} + \frac{1}{C'_4})(C'_3 + C'_4)} \right]^{\frac{1}{2}} \tag{5.9}$$

$$= 0.01533$$

$$-\frac{L_4}{L_1 + L_4} \rightarrow R_r \frac{1}{q} \frac{1}{C'_4} \left[\frac{\frac{1}{C'_3}}{(\frac{1}{C'_1} + \frac{1}{C'_3} + \frac{1}{C'_4})(C'_3 + C'_4)(\frac{1}{C'_1} + \frac{1}{C'_4})} \right]^{\frac{1}{2}} \tag{5.10}$$

$$\rightarrow 0.01373$$

Fig. 5.11f shows the final result.

It is convenient to divide the integrating capacitors into as many units as the inverse of the smallest capacitor ratio, which is given by the coupling between the nodes I_{L_1} and I_{C_1} or I_{C_1}), described by equations (5.7) and (5.10) as $\frac{1}{0.01373} \approx 73$. The other ratio, which is the coupling corresponding to the terminations of the first resonator or the third (given by equations (5.6) and (5.9)), is $\frac{1}{0.01533} \approx 65$ and can be implemented by using a capacitor that is slightly larger than a single unit, or $\frac{0.01533}{0.01373} = 1.12$.

Because of an initial calculation error, the number of units in the integrator capacitors is 69 instead of 73. But the difference is not so significant as to generate an appreciable error.

Fig. 5.12 shows the circuit schematics of the integrator including the two nodes G^+ and G^- used to implement the inputs to the constant multipliers (non-integrating inputs). These inputs are represented in the final circuit schematics of the filter (Fig. 5.13) as the + and − nodes at the sides of the integrators. In order to optimize the matching between integrators and also to simplify the layout, the total capacitance loading on every multiplying node is made equal. The rest of the capacitors that are not used to implement the flow-graph of Fig. 5.11f are grounded.

5.4. Oscillation Amplitude Control

Equation (4.32) gives the total integrated current Ψ at the outputs of the sign multipliers over a complete clock cycle 2π. Regarding the phase detector, it is desirable that under the steady-state condition the integrated current be equal to zero, which is equivalent to having the phase difference equal to $\frac{\pi}{2}$ (the locking condition). However, in the case of the amplitude comparator the situation is
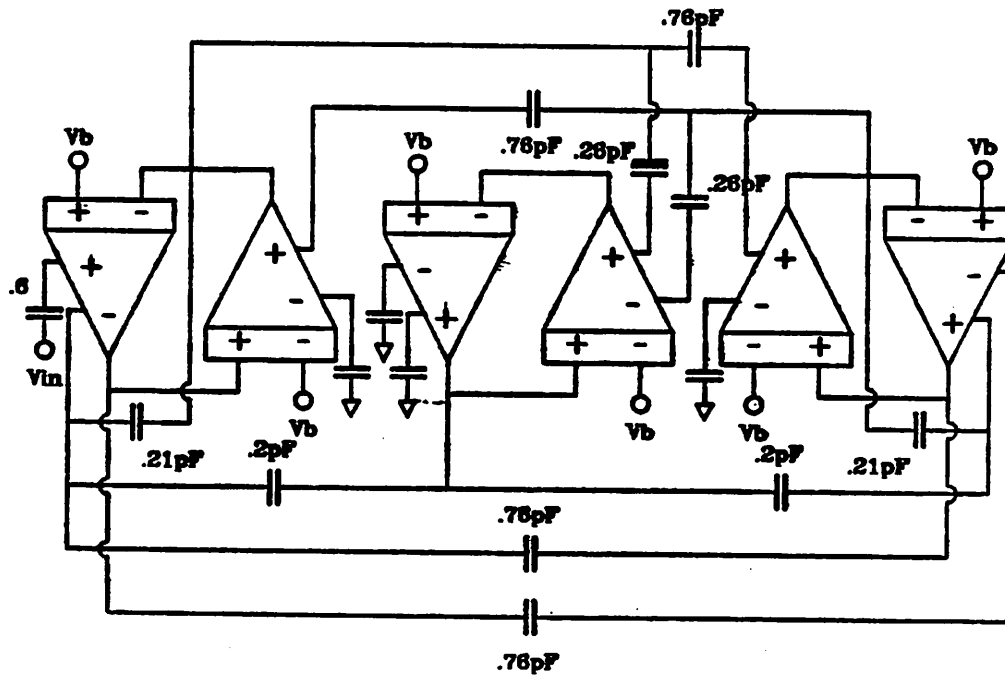
Figure 5.13. Final filter Implementation

different because a zero value for the integrated current would imply an amplitude equal to zero. Therefore the value of Ψ has to be modified to allow the input signal to reach the correct amplitude. This is done by introducing a constant current source KV_2 into one of the output nodes of the sign multipliers (see Fig. 4.10a). Throughout the amplitude comparator and amplitude control of the VCO, the action of the closed-loop feedback forces the input signal to have a value such that after being *sign* multiplied, it generates a current of the same absolute value as KV_2, but with the opposite polarity.

The implementation of this current source is done by creating an offset between the two active loads in the sign multipliers. In the case of a perfect balance (as in the case of the phase comparator), each active load should consist of 5 units of current, which correspond to the number of legs in the sign multipliers

plus the corresponding unit for the differential-to-single-ended converter.

Fig. 5.14 shows the portion of the amplitude comparator that includes the level shifters, the differential-to-single-ended converter, and one unit of the active loads with the offsets indicated by $1+\varepsilon$ and $1-\varepsilon$.

The procedure to find the value of ε is the following:

The value of the desired VCO output voltage, V_{pk}, is used to find the normalized variable U_{pk} which was given in Chapter 4 as:

$$U_{pk} = \sqrt{\frac{\beta}{2}\left(\frac{W}{L}\right)_E \frac{V_{pk}^2}{I_0}}$$

Since the current I_0 is derived from a depletion-mode transistor in the bias cir-
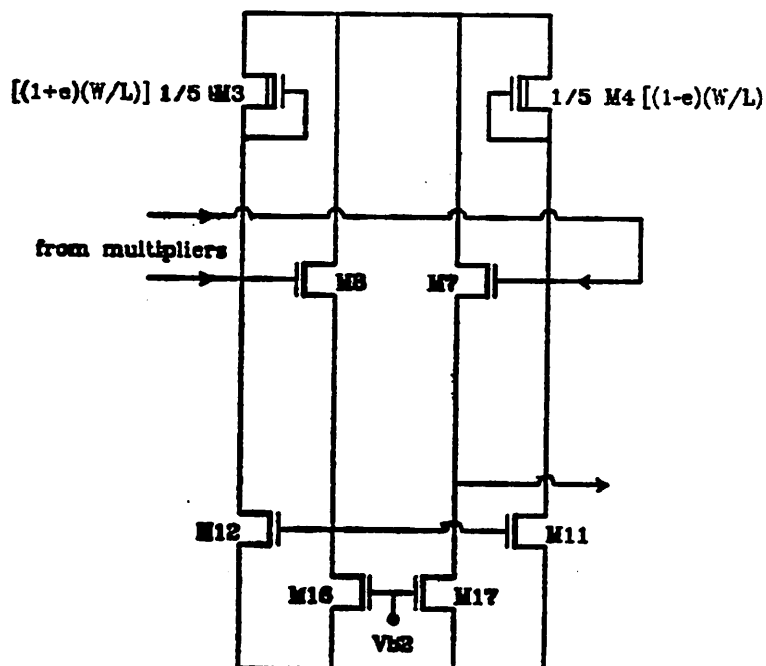
Figure 5.14. Level Shifter with Constant Amplitude Reference

cuit, its value can be replaced in the expression of U_{pk} to give:

$$U_{pk} = \left[\frac{(\frac{W}{L})_E}{(\frac{W}{L})_D}\left[\frac{V_{pk}}{V_{TH_D}}\right]^2\right]^{\frac{1}{2}}$$

The β is approximately the same for both the depletion and enhancement mode transistors. The amplitude chosen is $60mV_{peak}$, which is a value consistent with the signal levels usually encountered in the slave filter. Since the parameters of the transistors used in the sign multipliers are: $(\frac{W}{L})_E = \frac{90}{8}$, $(\frac{W}{L})_D = \frac{11}{40}$ and $V_{TH_D} = -3.0V$, then $U_{pk} = 0.14$. This value, along with the value of $\cos\varphi = 1$ (the phase difference between the clock and input signal for the amplitude comparator), is also used in expression (4.32) to give $\Psi \approx \frac{1}{4}$. This offset is relative to a current unit, which means that on one side of the sign multipliers the currents are equal to 5.11 units, while on the other side they are equal to 4.88 units.

5.5. Mismatch Effects

As in any replica system, the tracking performance of the slave with respect to the master filter is directly related to the accuracy of the matching between them. The most important parameters to consider are the frequency and amplitude tracking conditions based on the matching capabilities of the devices within the integrated circuit.

If the phase and amplitude gain constants are assumed to be linear functions of the absolute phase and amplitude expressions, then they can be used to compute the effects of the mismatches. The amplitude and phase gain constants of the VCO that were given in equations (4.45) and (4.46) respectively, are repeated here:

$$K_{VCO_A} \approx \omega_0 g_{m1}R^2\beta_6 \tag{4.45}$$

$$K_{VCO_P} \approx \omega_0 \frac{1}{g_{m1}} \beta_5 \qquad (4.46)$$

Since the value R is the ON resistance of transistor M_8 in Fig. 4.3, equation (4.45) can be rewritten as follows:

$$K_{VCO_A} \approx \omega_0 \frac{g_{m1}}{\beta_8 (V_{GS8} - V_{TH})^2} \qquad (5.11)$$

where V_{GS8} is the controlling voltage of transistor M_8, and V_{TH} the threshold voltage. The relative errors are calculated by taking the absolute differential of the natural logarithms of both sides of equation (5.10):

$$\frac{\Delta K_{VCO_A}}{K_{VCO_A}} = -\frac{\Delta \beta_8}{\beta_8} - 2 \frac{\Delta (V_{GS8} - V_{TH})}{(V_{GS8} - V_{TH})} \qquad (5.12)$$

The same procedure is used to calculate the mismatch effects on the frequency:

$$\frac{\Delta K_{VCO_P}}{K_{VCO_P}} = -\frac{\Delta \beta_5}{\beta_5} - 2 \frac{\Delta (V_{GS5} - V_{TH})}{(V_{GS5} - V_{TH})} \qquad (5.13).$$

As equation (5.13) shows, when the relationship between the frequency variation and the gain constant of the VCO is linear, a mismatch of 5% in the net overdrive voltage of transistor M_5 (which includes the threshold variation), gives a 10% error in the center frequency. Similarly, when the transconductance has a 5% mismatch factor, the frequency error is 5%. Simultaneous mismatches of 5% in the overdrive voltage and transconductance yield a frequency error of 15%.

CHAPTER 6

COMPUTER AIDED DESIGN

Given the complexity of today's digital LSI chips, it would be very difficult if not impossible to design and implement a reliable device without computer-aided-design (CAD) programs such as logic simulators, circuit simulators, and layout systems including routing programs and reticle generators. The integration level of analog circuits is becoming as complex as that of digital ICs. Switched-capacitor filters, analog-to-digital converters, and others are typical examples of this growing complexity. The implementation of a typical analog LSI system such as a switched-capacitor filter involves the following design steps:

(1) Using a program for the simulations of digital filters (e.g. DINAP) [23]

(2) Using a circuit simulator for the active circuits such as switches, operational amplifiers, and storage capacitors (SPICE [24]).

(3) Using computer programs for the layout and artwork generation.

DINAP only simulates networks composed of ideal elements such as delays, adders and scalers. On the other hand, SPICE is not suited to obtain the impulse or frequency response of a sampled data system (unless some modifications are done on the basic algorithms).

Recently, a program that combines the capabilities of a digital filter simulator and a circuit simulator has been developed (DIANA) [25]. The main advantage of this is that it eliminates the need for separately analyzing the sampled-data path (e.g. frequency response in a switched-capacitor filter using DINAP) and the performance of the active circuits (e.g. operational amplifiers using SPICE).

To some extent, the availability of good circuit simulators has lowered the standards of circuit design, for many engineers use these programs to design, rather than to verify, by randomly changing the connections and/or values of the elements in the circuits until the computer output shows satisfactory results. Needless to say, it is easier to punch some numbers on a computer terminal than to elaborate a proper solution. However, ideally the engineer should be able to estimate *a priori* the characteristics of the proposed circuit with hand calculations and logical thinking. This surely yields a more reliable, economical and satisfactory design. Thus programs should do what they do best, circuit verification, not designing.

6.1. Circuit Simulations

For purely continuous systems such as the VLL and the slave filter, there is no need for digital filter simulators, hence the analysis and verification of the performance are done by means of only the circuit simulator SPICE. These simulations are performed for both sections of the chip:

(1) For the slave filter, a linear network is simulated to verify the frequency response.

(2) For the VLL, which includes the simulation of the VCO (the master filter) and the phase and amplitude comparators, a transient analysis is used to verify the accuracy of the hand calculations and to check for other unforeseen effects, especially those concerning the stability of the loops and the characteristics of the generated signals.

Each of these simulations will now be described in detail.

6.1.1. The Slave Filter

(1) A linear analysis of the LC ladder is done to verify the coefficients given by the filter tables. Since this is a very simple task, no further comments on this will be made.

(2) The flow-graphs of the transformation from the LC prototype to the active implementation described in the previous chapter, are used as an interconnection model for the active network.

The simplified linearized model for each integrator consists of a voltage-controlled current source and a voltage-controlled voltage source representing the first and second stages respectively (see Fig. 6.1). For the first generator, the parameter defining the transfer function is the transconductance that is made equal to $1\Omega^{-1}$ to simplify the scaling process. Thus the values of the capacitors in the model are inversely proportional to the integrating constants of the flow-graph shown in Fig. 5.11f. The second generator is characterized by its voltage gain. This parameter is arbitrarily made large to check the validity of the flow-graph transformations (from Fig. 5.11a to 5.11f). Fig. 6.2 shows the global small-signal equivalent to the flow-graph seen in Fig. 5.11f. The SPICE listing for the network is shown in appendix A1. The plots of the amplitude outputs as a function of frequency are shown in Fig. 6.3.

Instead of ideal controlled sources, it is preferable to use the complete circuit of the amplifiers. In this case, once the DC operating point of the whole circuit is found by SPICE, it automatically performs a linear expansion of every single transistor into ideal elements such as controlled sources, resistors and capacitors. All the second order effects, such as the finite gain of the amplifiers, the loading effects, the additional phase-shift, etc, are automatically computed in this analysis and a very accurate prediction of the behavior of the circuit can be
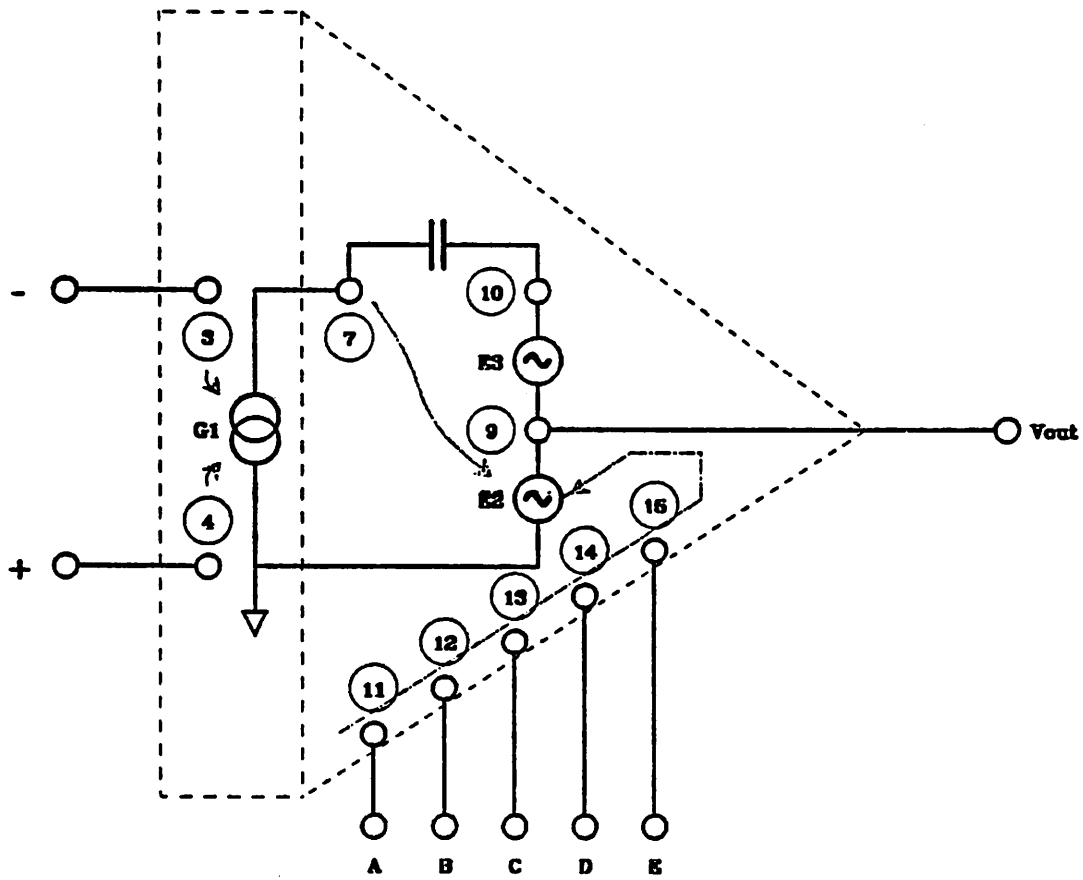
Figure 6.1. Linear Model of the Integrator
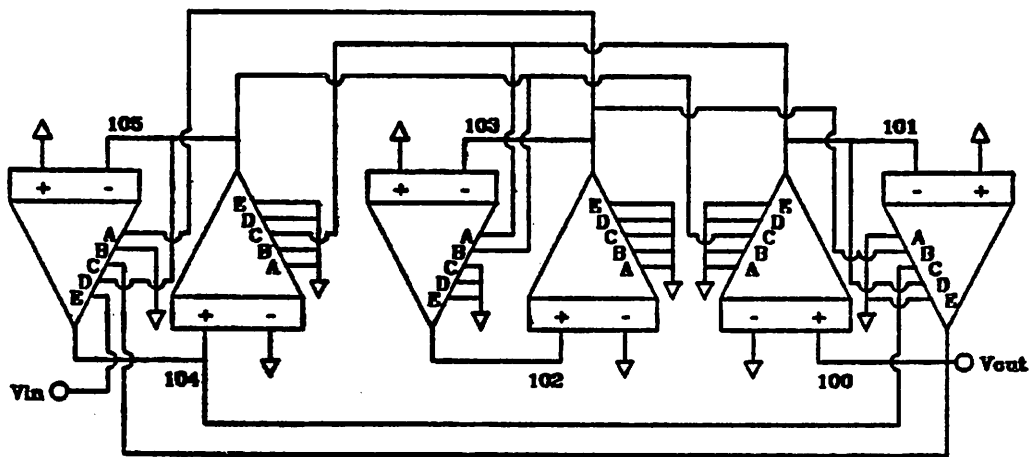
Figure 6.2. Active Implementation of the Flow-graph
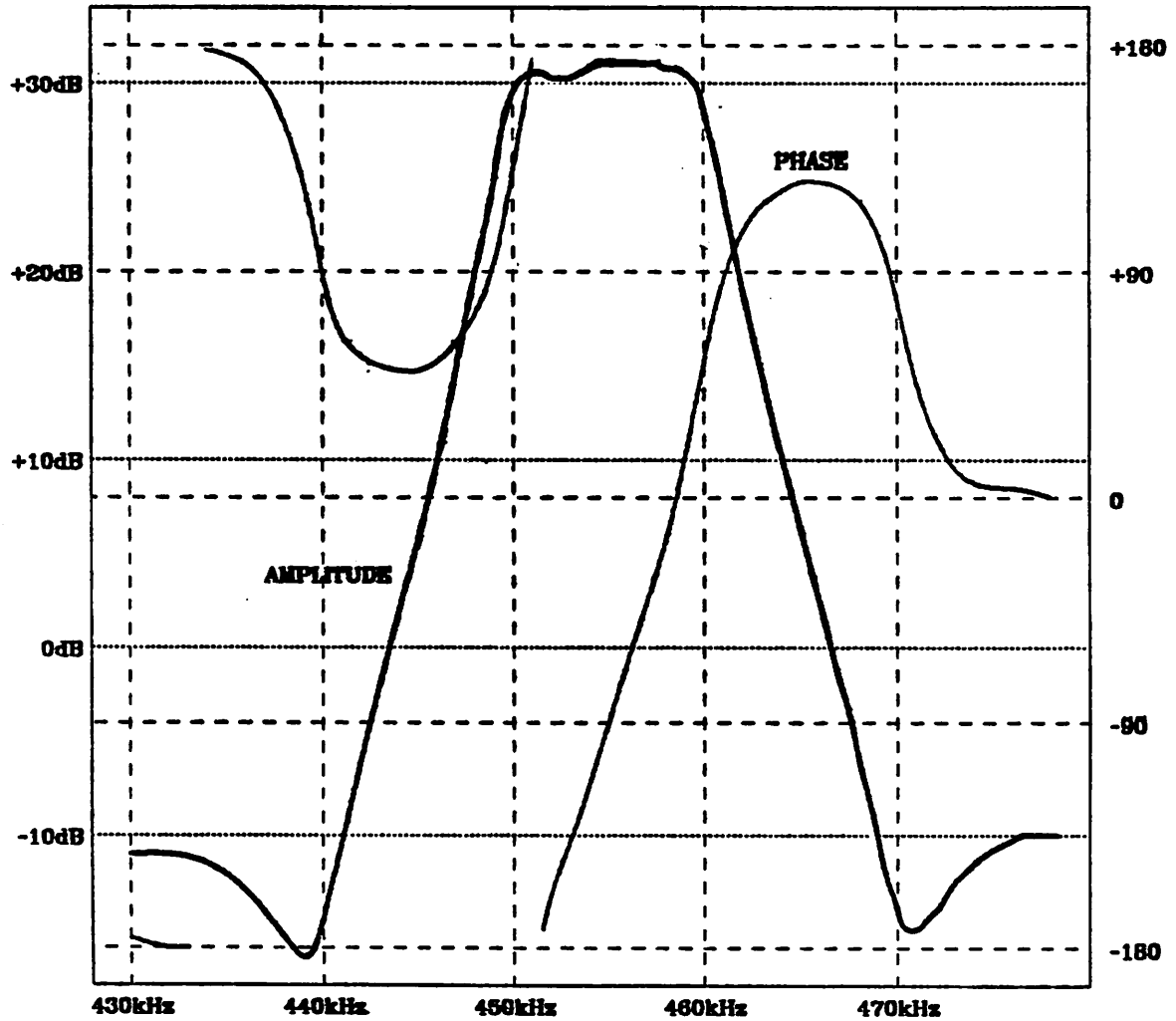
Figure 6.3. Amplitude and Phase Plots of the Filter

made.

Unfortunately, at the time in which these simulations were made, SPICE did
not have a feature in which a predefined set of voltage values could be assigned to

each node. Hence for very complicated circuits like this one having six integra-
tors (the equivalent of 120 transistors) and large values of loop gain, problems of
DC convergence prevented the program from finding the right operating point.
Therefore the elimination of all the transistors lead to an equivalent linear net-
work much simpler than the one that would have been created by the SPICE
automatic self-expansion.

6.1.2. VLL Transient Simulation

In this particular case, given the nonlinear nature of the locking acquisition
process, a transient analysis is mandatory for the design. The interconnection
scheme used here was similar to the one shown in Fig. 6.2, but there were no
simplifications of the circuit, hence every transistor was present in this simula-
tion.

Given the characteristics of the algorithms used by SPICE in the transient
analysis, the problem of convergence is not as severe as in the case of the DC
analysis. This property was used to overcome the limitation encountered in the
simulation of the VLL without the DC operating points in the following way: the
power supply was replaced by a pulsed voltage generator that was forced at the
beginning of the transient analysis to be equal to $0V$, hence the solution for
finding the DC operating points was trivial, i.e., since all the nodes had $0V$ the
currents were also null. After a few microseconds in the transient analysis, the
power supply was pulsed to its final value, $5V$. It should be noted that this
approach could not be used for linear analysis because older versions of SPICE
did not permit the use of DC operating points based on a transient analysis.

Appendix A2 shows the SPICE listing for the transient analysis of the whole
VLL. The total number of time steps in the transient analysis, or total analysis
time used, was a combination of two contributions:

(1) A linear portion based on the evaluation of the number of time constants (τ_a for the amplitude loop and τ_P for the phase loop) after which the system could be considered to have reached the final steady-state condition (usually 10τ).

(2) A start-up time that was a non-linear transient phenomenon. The estimation of this time was too complicated to be done by hand calculations, hence several test simulations were made to that effect.

There were no appreciable transient effects after $60\mu sec$, hence the transient analysis was done over a total period equal to this time and with a time-step equal to $50nsec$ (1200 time-points). Only the last $20\mu sec$ were displayed in order to save computer paper using a feature of SPICE that gives an output of a smaller time window than the total analysis time. This simulation required more than two hours of CPU time on a Cyber 175 computer.

The initial simulations showed excellent agreement with the hand calculations. Among the observed parameters were: the acquisition behavior, the stability of the loops under different start-up conditions, the amplitude of the signals generated by the VCO, and the waveform of the error signals corresponding to the Fourier expansions theoretically derived. But the simulations showed an unexpected distortion of the VCO signals. This distortion consists of a high frequency oscillation occurring in a portion of the sinusoid output where the slope reached its maximum positive value (see Fig. 6.4). The source of this anomaly can be attributed to the action of the variable resistor M_8 of the integrators (see Fig. 4.3), which depending on the sign of the displacement current across the integrating capacitor C, acted as a transistor with either positive or negative transfer gain for the small signals injected to its gate. In other words the node that connects the capacitor C and the transistor M_8 is either the source or the
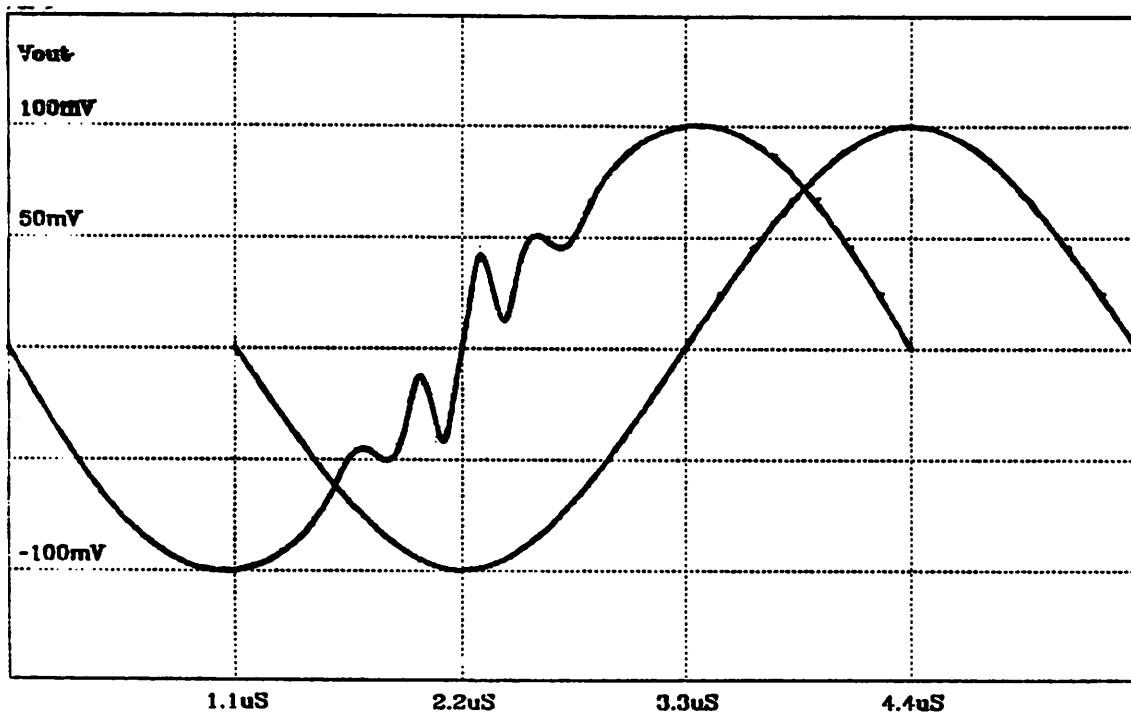
Figure 6.4. Initial High Frequency Distortion

drain of the latter depending on the sign of the current. This peculiarity can be related to the operation of the phase and amplitude comparators in the following way.

From the analysis of the VLL operation (Chapter 4), it can be seen that both outputs of each resonator, which consists of two integrators, are used by the phase and amplitude comparators to generate the error signals. By inspection of the loop composed of transistor M_8, and the phase (or amplitude) comparator (see Fig. 6.5), it can be observed that there is no phase inversion for one of the two VCO signals at the time in which the gain of this loop reaches a maximum, which occurs when the value of the clock is a logical "one". Since the steady-state condition of the VLL makes the phase difference between the clock (or reference
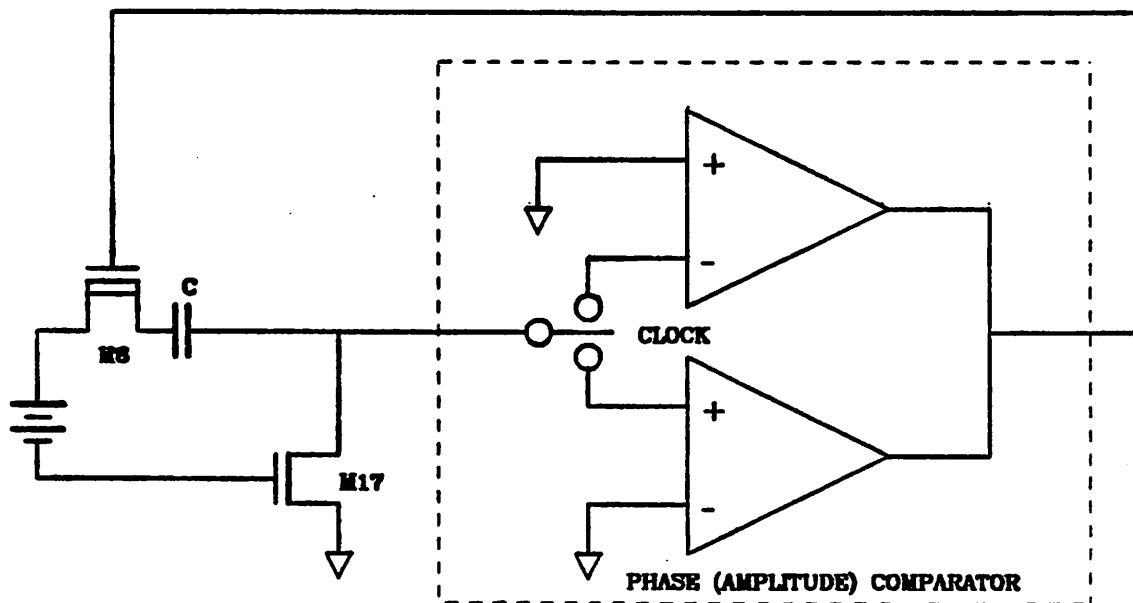
Figure 6.5. Model for the Positive Feedback Effect

frequency) and the VCO signals equal to $\pm\frac{\pi}{2}$, there is coincidence between the times at which both the positive feedback and the oscillation take place. This positive-gain loop can reach a value considerably larger than 1 because of the large voltage gain of the loop composed of the sign multipliers, the loop filters and the amplifying action of M_8, which is enhanced because at that particular time (maximum signal slope) the displacement current across the integrating capacitor C of the integrators reaches the maximum value, thus maximizing the transconductance of this transistor.

The solution used to overcome this problem consisted in eliminating the connection between the amplitude comparator and the amplitude-control input (the gate of M_8) which created the positive feedback loop. Hence only one integrator

of the resonator is connected to the output of the amplitude comparator (the one that preserves a negative feedback condition at all times in which that loop is active). The gate of transistor M_8 which is not used is connected to the gate of transistor M_7 of the same integrator. The justification for this solution is as follows:

The integrator that does not have its amplitude control node connected to the amplitude comparator has a fixed loss that is generally negative. The other integrator (the one connected to the amplitude comparator) has an adjusted loss of the same absolute value but with the opposite sign. Thus, correcting the amplitude only requires making the overall phase-shift within a resonator equal to π, regardless of whether the individual phase-shift of each integrator is not exactly $\frac{\pi}{2}$.

The high-frequency oscillation disappeared after the SPICE data file was changed. The only observable distortion of the VCO signals can be attributed to non-linearities of the circuits. The total harmonic distortion observed is less than 2%. The amplitude and phase error signals that are also plotted show (see Fig. 6.6) the presence of harmonics that are multiples of four, as predicted by the Fourier analysis.

6.2. Computer-aided Layout

For the layout of the chip, the FICLS system was used. This software package developed at Hewlett-Packard consists of two different stages that perform the following tasks:

(1) The first stage allows the conversion of the rectangle data file (generated by a digitizer) into a format suitable for an editor that operates on a Tektronix 4014 graphics-terminal;
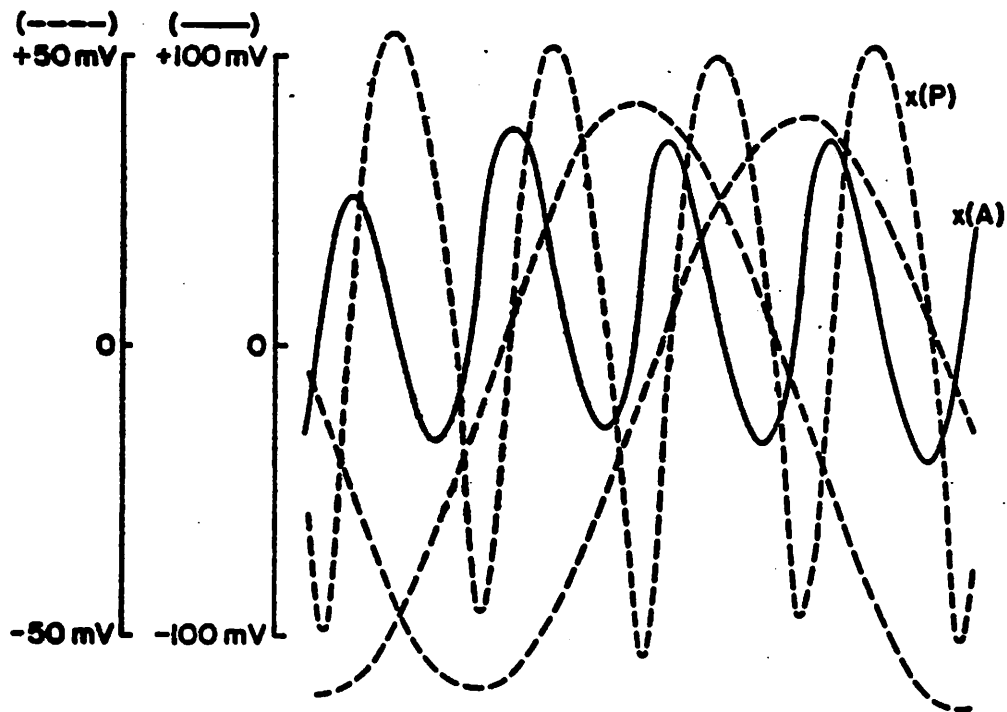
Figure 6.6. VLL Signal Outputs

(2)   The second stage converts the file containing all the rectangle information into a format suitable for driving a Mann-3000 reticle generator.

Initially, all the basic cells including the integrators, the amplitude and phase comparators, the bias circuit and the interconnecting lines between them were drawn on a large piece of Mylar. Later this drawing was digitized and further transferred to the computer for the editing session. The inconvenience of handling such large drawings, the inaccuracies resulting from having to merge lines between the individual pieces, and the amount of erasing needed were convincing factors to change the approach and transfer all the tasks to the graphic-terminal sessions. Therefore the input of data, and editing and verification were all done interactively with the graphics terminal. Presently, the usage of this system has

been abandoned at UC and replaced by a more versatile system (KIC).

The layout of the device is organized into cells of three hierarchical levels. This organization allows a fast and error-free implementation by retrieving these cells from the computer memory whenever they are needed. The levels are divided as follows:

(1) The first level is composed of two cells - a unit capacitor and an enhancement transistor unit (see Figs. 6.7a and 6.7b). The bottom plate of the capacitor cell is made of diffusion, and the top plate is made of polysilicon. The transistor cell includes the drain and source diffusions, the polysilicon gate, the contacts, and the metalization over the diffusion areas.

(2) The second level is composed of complete circuits such as integrators and comparators. The integrators consist of a number of interconnected transis-
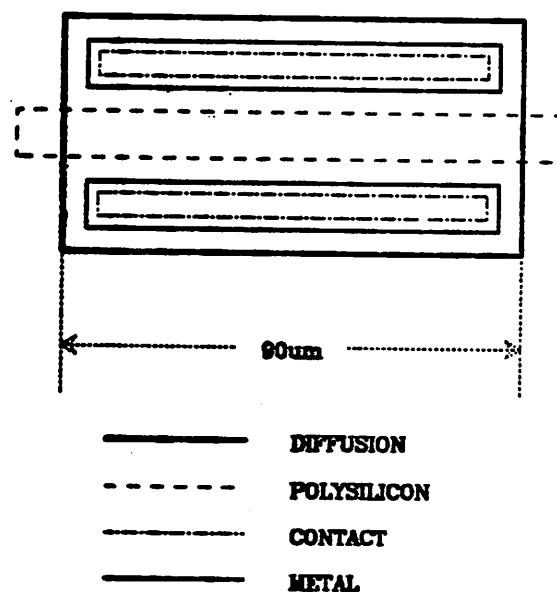
Figure 6.7a. Transistor Cell
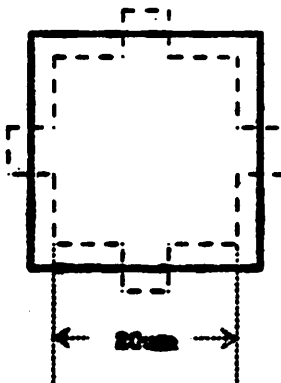
Figure 6.7b. Capacitor Cell

tor and capacitor cells. The stacked-layout of these circuits is very adequate for using the unit-transistor-cell approach because every transistor is an integer multiple of these units.

(3) The third level is composed of filters as a collection of integrators, capacitors and interconnecting lines. The termination capacitors, which make the only difference between the master and slave filters, are individually placed over the area corresponding to the latter.

Fig. 6.8 depicts the complete layout of the device, showing the master filter at the bottom, the slave filters at the top (above the master filter), the comparators on the left, and some test structures on the left.
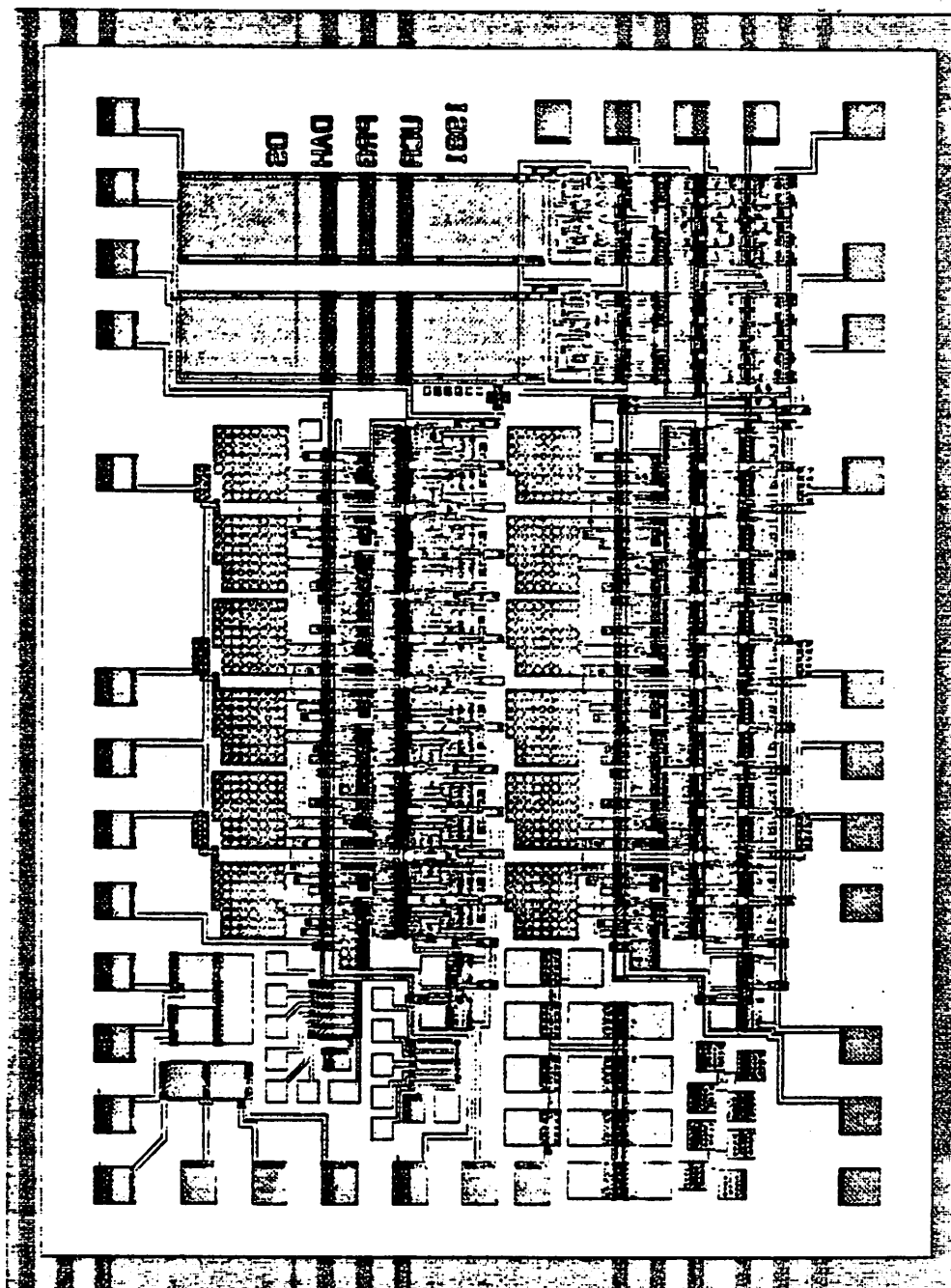
Figure 6.8. Chip Layout

CHAPTER 7

EXPERIMENTAL RESULTS AND CONCLUSIONS

The importance of a process-insensitive design becomes very apparent in a situation like the one encountered in this research. Instead of determining *a priori* the exact characteristics of the process in terms of transistor parameters, breakdown voltage, etc, we carried out the design using estimated values based on already-existing industrial technologies. Obviously it is very difficult, if not impossible, to fabricate a device that has the identical intrinsic parameters as those estimated for the design. However if the design is done using process independent techniques, such differences are no longer important and a successful implementation can be expected.

This chapter deals with the two types of experimental results encountered during the implementation of the device:

(1) Those related to the performance at the processing level, i.e., those related to the breakdown voltage, transistor and capacitor parameters, etc.

(2) Those related to the system level, i.e., the locking range, frequency response of the slave filter, etc.

7.1. Processing Parameters

In appendix B all the processing steps in the fabrication are described.

All the measurements of the basic parameters of the transistors were made on devices having a geometry ratio of $\frac{W}{L} = \frac{100\mu}{100\mu}$. These dimensions were chosen in order to avoid any of the effects related to small geometries such as short and narrow channel. The measurements of the field inversion and breakdown voltages

were done on structures laid out as transistors having the same dimensions as those of the devices previously mentioned. Table 7.1 shows the measured, as well as the designed parameters (in parentheses).

It can be seen that for some parameters such as the threshold voltages, the relative error is excellent, i.e. within 20%, while for others such as the enhancement body effect the measured value is twice as large as the expected one. But in any case, as will be described later, the departure from the values originally expected did not create more than a shift in the operating condition of the circuits.

Parameter	Device			
	Enhancement Transistor	Depletion Transistor	Field (Poly) Transistor	Field (Metal) Transistor
Threshold Voltage (V_{TH}) (in V)	1.06 (0.7)	−3.2 (−3.0)	25.0 (20.0)	36.0 (20.0)
Gain (β) (in $\frac{A}{V^2}$)	2.3×10^{-5} (3.0×10^{-5})	2.3×10^{-5} (3.0×10^{-5})	—	—
Body Effect (γ) (in $\sqrt{V}$)	0.53 (0.3)	0.22 (0.3)	—	—
Sheet Resistance (ρ) (in $\frac{\Omega}{\blacksquare}$)	Poly		Diffusion	
	20.0 (20.0)		50.0 (30.0)	
Junction Breakdown (V_{BCO}) (in V)	25.0 (20.0)			

Table 7.1. Measured Process Parameters

7.2. System Measurements

Since measuring the characteristics of the slave filter requires that the master filter or VLL be in the locking condition, the initial step taken was to connect the device in the setup shown in Fig. 7.1.

7.2.1. Master Filter

In order to allow the system to acquire the locking condition, the frequency of the signal generator was varied around the nominal expected value ($455kHz$)
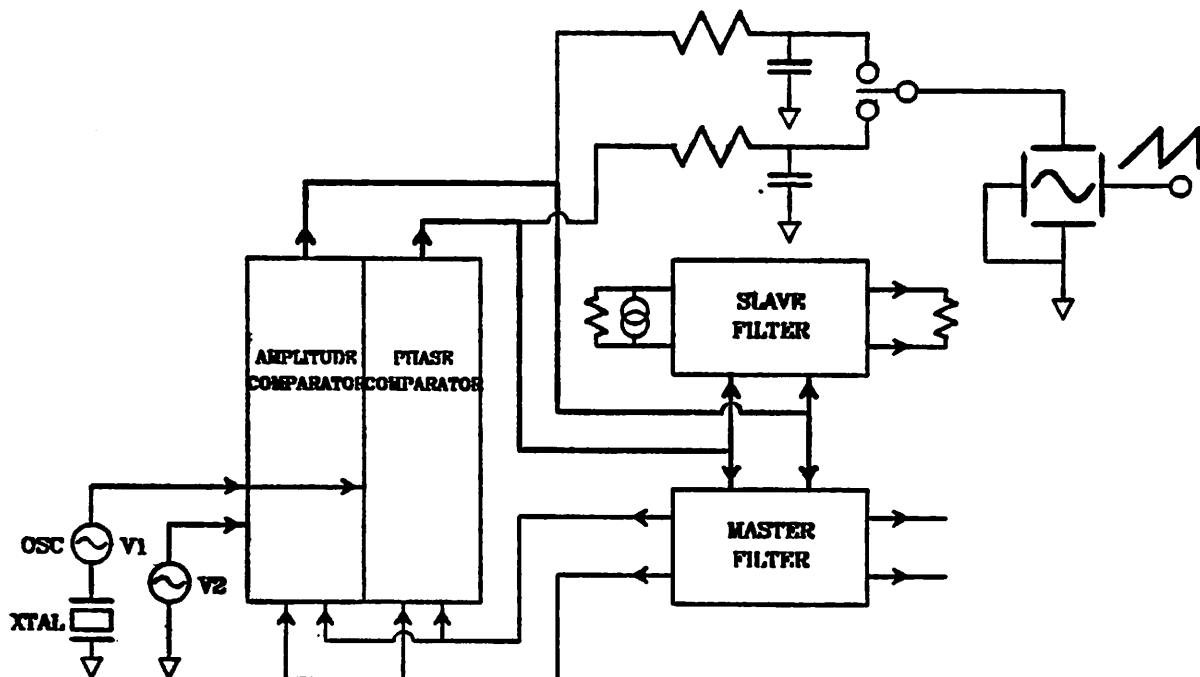
Figure 7.1. Measuring Setup

until the amplitude and phase error signal reached the steady state operating voltage. The locking condition was verified by incrementally changing the frequency of the generator and observing the VCO signals. The sinusoidal waveform of Fig. 7.2 (the DC values are offset from the real ones to permit a clearer picture) corresponds to one of the two identical outputs of the VCO. The measured peak-to-peak amplitude of $200mV$ is in agreement with the calculated value. The total harmonic distortion in the VCO output measured using the spectrum analyzer is <5%, which is greater than what the simulation predicted (2%). The other two traces in Fig. 7.2 are the error signals at the outputs of the amplitude and phase comparator, respectively. Here is where the major distortion with respect to the simulations occurred. As predicted by the theoretical analysis described in Chapter 4, the overall DC offset at the inputs of the comparators created a departure consisting in the presence of a large amount of the fundamental frequency
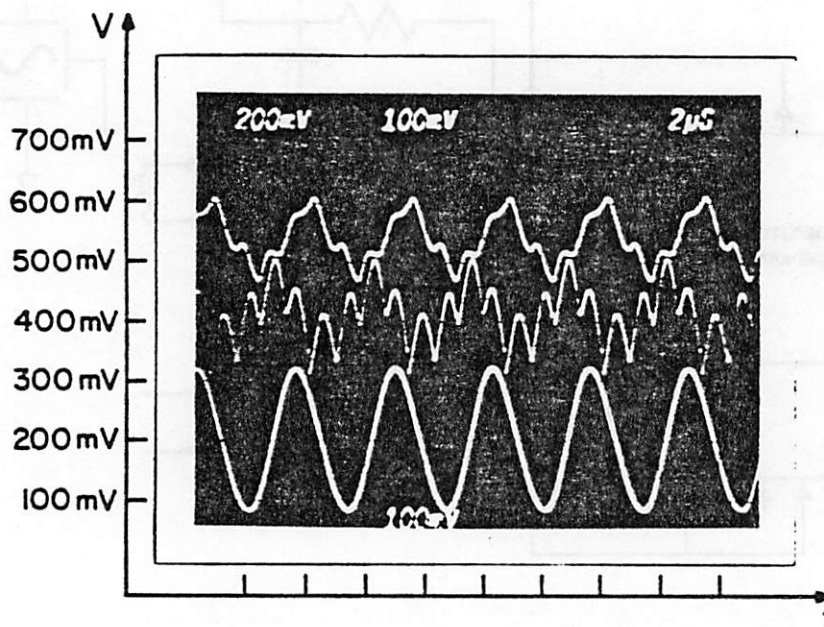
Figure 7.2. Observed VLL Signals

component. Hence the waveform of the error signals is a superposition of this fundamental component with the expected multiple-of-four harmonics.

Another measurement taken using the setup shown in Fig. 7.3 was the locking and capture range for both the amplitude and phase loops. The measurement setup consisted of a voltage-controlled frequency generator, an oscilloscope with the horizontal input connected to the same frequency-controlling voltage, and a single pole RC low-pass filter (the same RC network used to filter the high frequency components from the error signals in the connection to the slave filter). The frequency controlling voltage was a saw-tooth waveform obtained from another signal generator. The resulting oscillogram is shown in Fig. 7.4. The gap
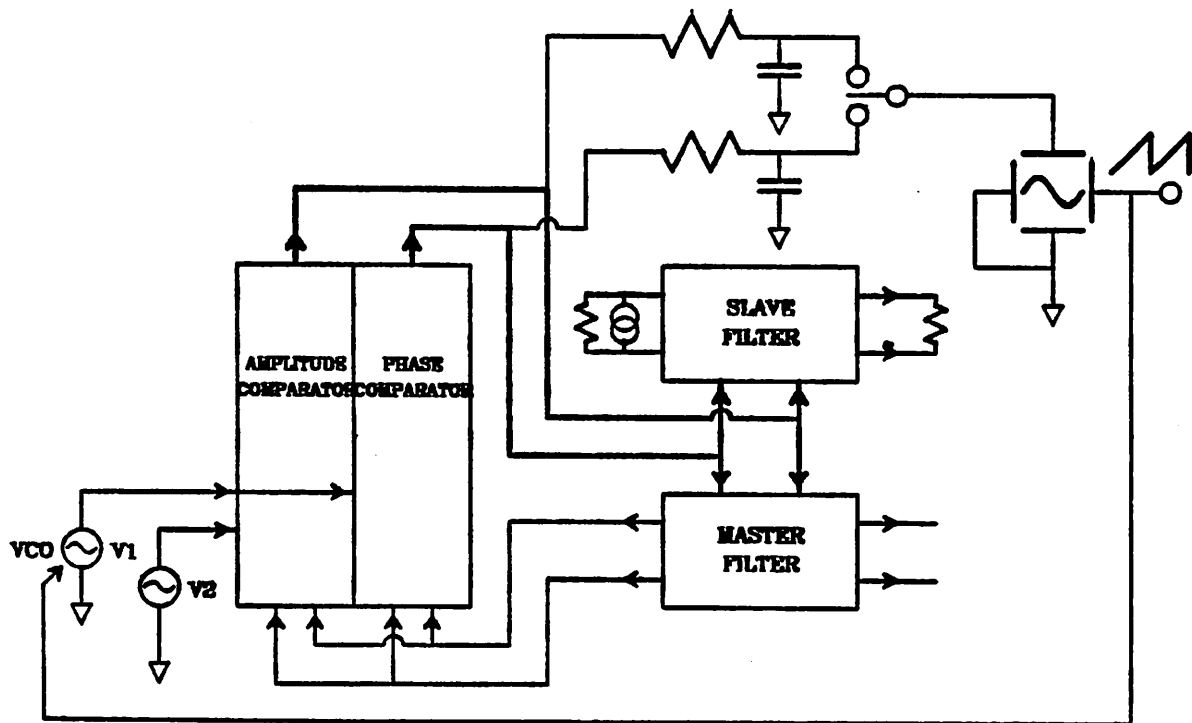
Figure 7.3. Setup to Measure Locking and Capture Range
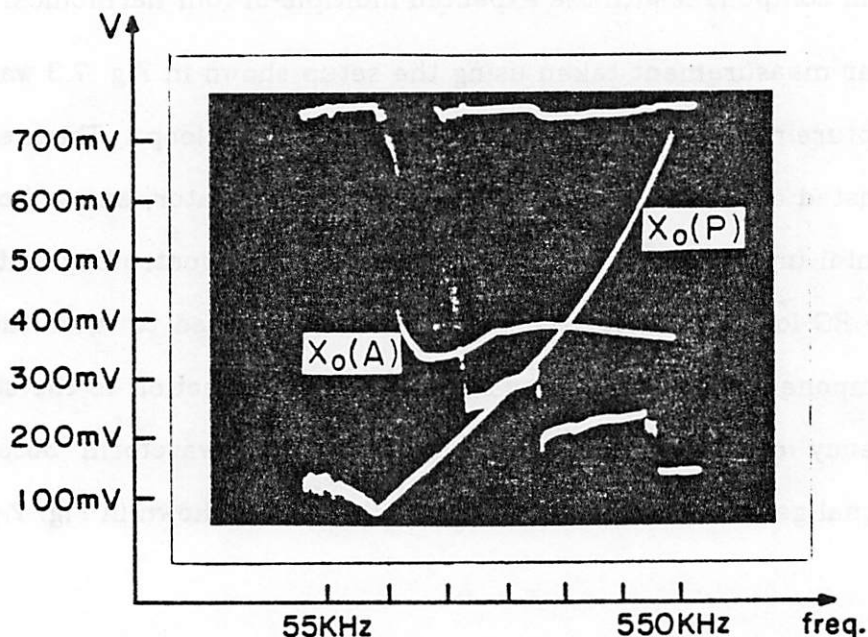
Figure 7.4. DC Control Signals of the Comparators

shown between the two top traces is the *capture* range, while the *smooth* regions of $X_o(P)$ and $X_o(A)$ indicate the *locking* range. A considerable asymmetry between the center of the locking range with respect to the center of the capture range can be observed. This non-linear effect is due to the fact that when the system is out of lock, the amplitude can reach values that are limited only by the power supply voltage. In our case the slew rate of the amplifier limited the maximum attainable free-running frequency. Thus the external frequency had to be lowered to a value that had a slope equal to the slew-rate. Under this condition the system acquired the locking state for both variables (the frequency and amplitude). Once under the steady-state condition the frequency could be further increased because the amplitude was already under control ($\approx 200mV$). Actually this problem of reduced capture could have been alleviated by simply

introducing some form of asynchronous limiter to keep the free-running output at a low amplitude. However, during the design stage it was decided that no extra circuitry should be added in order to ease the debugging process. The locking range was $\approx 250kHz$, and the measured capture range was $\approx 50kHz$.

7.2.2. Slave Filter

Once the master filter is in the locking condition, the slave filter should automatically reach a condition in which the frequency response meets the design specifications at every frequency of the master clock within the locking range. But this situation did not happen. Instead a much smaller valid filtering interval within the locking range was obtained. The observable effect was a loss of selectivity of the frequency response when the clock frequency was lowered, and an enhancement of selectivity when the clock was increased. In the latter case, the filter reached an unstable condition and broke into an oscillation when it was beyond a given clock frequency that was close to the point of optimum response. This behavior can be attributed to the initially low gain of the amplifiers, which is equivalent to a high loss of the resonator in the open-loop condition. This implies that unless the slave filter was very close to the point of optimum response, the internal loss of the integrators created a stronger effect than the filter terminations, in terms of the selectivity of the response.

Fig. 7.5 shows the amplitude response of the filter for a clock frequency of $275kHz$. The measured ripple ($\approx 6dB$) is greater than the expected one ($\approx 0.5dB$) due to several effects such as Q enhancement (excess phase shift of the integrators) and departure of the values of the terminating elements from the nominal values.

The presence of the fundamental component in the error signals is amplified by the gain of the filter at a given frequency, which in this case turned out to be
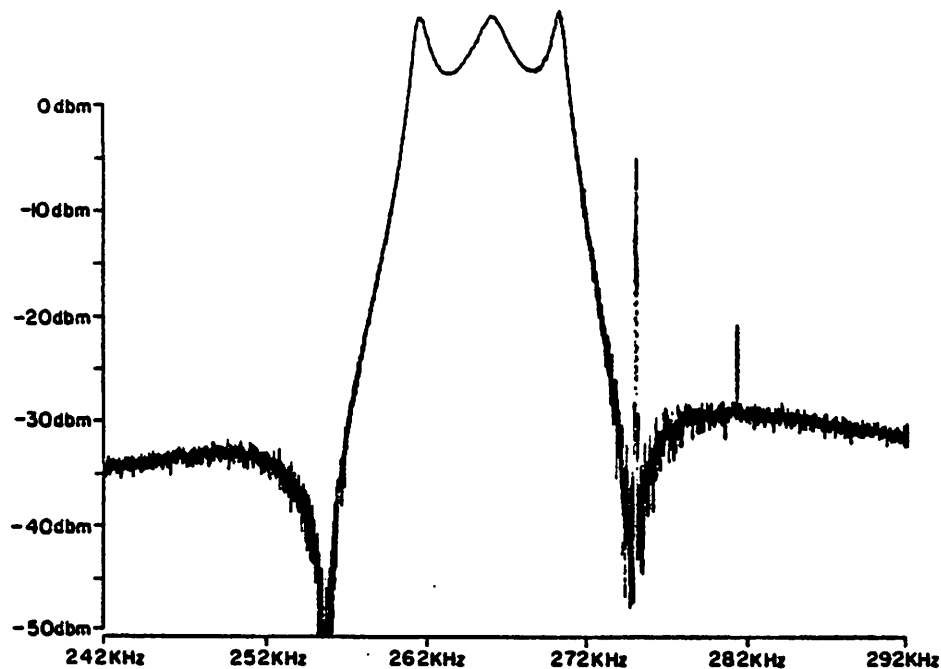
Figure 7.5. Frequency Response of the Slave Filter

the same center frequency as that of the slave filter. To some extent the introduction of low-pass filters between the error signals and the controlling inputs of the slave filter reduces this effect. But as can be observed from the pictures, there is still a considerable amount of clock feed-through present.

The microphotograph of the die is shown in Fig. 7.6. The dimensions are $3500\mu m \times 2700\mu m$. The area could have been reduced by 20% if the monitoring devices for the process had not been included.

Table 7.2 summarizes the measurements taken for the system:
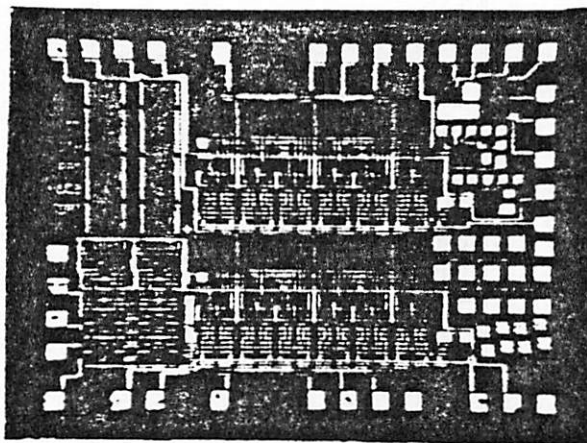
Figure 7.6. Microphotograph of the Chip

Parameter	Value
Free Running Frequency (in kHz)	250.0
Master Filter Locking Range (in kHz)	250.0
Master Filter Capture Range (in kHz)	50.0
VCO Peak Amplitude (in mV)	100.0
VCO Total Harmonic Dist. (in %)	5.0
Slave Filter $3dB$ Bandwidth (in kHz)	12.0
Slave Filter Ripple (in dB)	3.0
Slave Filter Stopband Reject. (in dB)	40.0

Table 7.2. Measured System Parameters

7.3. Conclusions

In order to draw some conclusions about the device under study, it is convenient to analyze the device in two different ways:

(1) First as a bandpass filter (with the slave filter) and

(2) Second as a stand-alone VLL (without the slave filter).

7.3.1. Replica-type Filter

One of the basic requirements to ensure a reliable performance for the filter portion is a good matching between the master and the slave filters. This matching requirement can be regarded as *macroscopic* because it concerns all the possible parameters of both sections, namely the phase shift and integrating constants of the integrators, the coupling between adjacent resonators, the terminating elements, etc. This complex set of interacting effects results in a final performance that is not simple to predict. This uncertain situation is further enhanced by the fact that if the filter were to have a very narrow relative passband (high Q), reliable operation avoiding oscillations or completely distorted passbands might not be possible at all.

In contrast, a switched capacitor filter only requires obtaining good matching between capacitors within sections (*microscopic* matching), assuming that the amplifiers have very large gain. Thus, if each integrating section settles down to a sufficiently small error, the effect of the internal phase shift of the amplifiers is irrelevant to the performance of sampled-data filters. Furthermore, the phase shift throughout the filter is a predictable function of the sampling scheme, allowing a considerably simpler design. Unlike the replica-type filters, switched capacitor filters do not require having the same structure replicated twice, thus saving a considerable amount of chip area.

Another drawback of the replica-type filter is that since the feed-through of the fundamental component of the clock frequency is located within the passband of the filter (or close to it), an unacceptable *beat* effect with the carrier of the incoming signal can occur which, depending on the amplitude of the feed-through might drive the filter into saturation. In the case of switched-capacitor filters, the clock frequency is several times larger than the center of the passband so

that the problems associated with the clock feed-through are avoided. Lastly, the replica-type filter is sensitive to process variations through the definition of the value of the channel resistance, whereas switched capacitor filters are not.

In summary of the drawbacks of the replica-type filter, we have:

(1) Complicated design

(2) Unreliable performance

(3) Duplication of structures

(4) Clock component located at the center of the passband

(5) Process dependent

However, one advantage of replica-type filters over sampled-data filters is that because of the continuous nature of their operation, there are no aliasing effects, eliminating the need for additional continuous antialiasing filters.

7.3.2. The Stand-alone VLL

Since the VLL is an extension of the PLL, all the applications in which the latter is used can also be performed and enhanced (or simplified) by a VLL. For example, a VLL can perform the following functions:

(1) *Sine-wave generation*

(2) *Amplitude modulation*

By varying the current source KV_2 (see Fig. 4.10a), the output of the VCO can have an amplitude whose peak value is approximately proportional to KV_2.

(3) *Amplitude and frequency demodulation*

These functions can be implemented by re-configurating the system such as shown in Fig. 7.7.
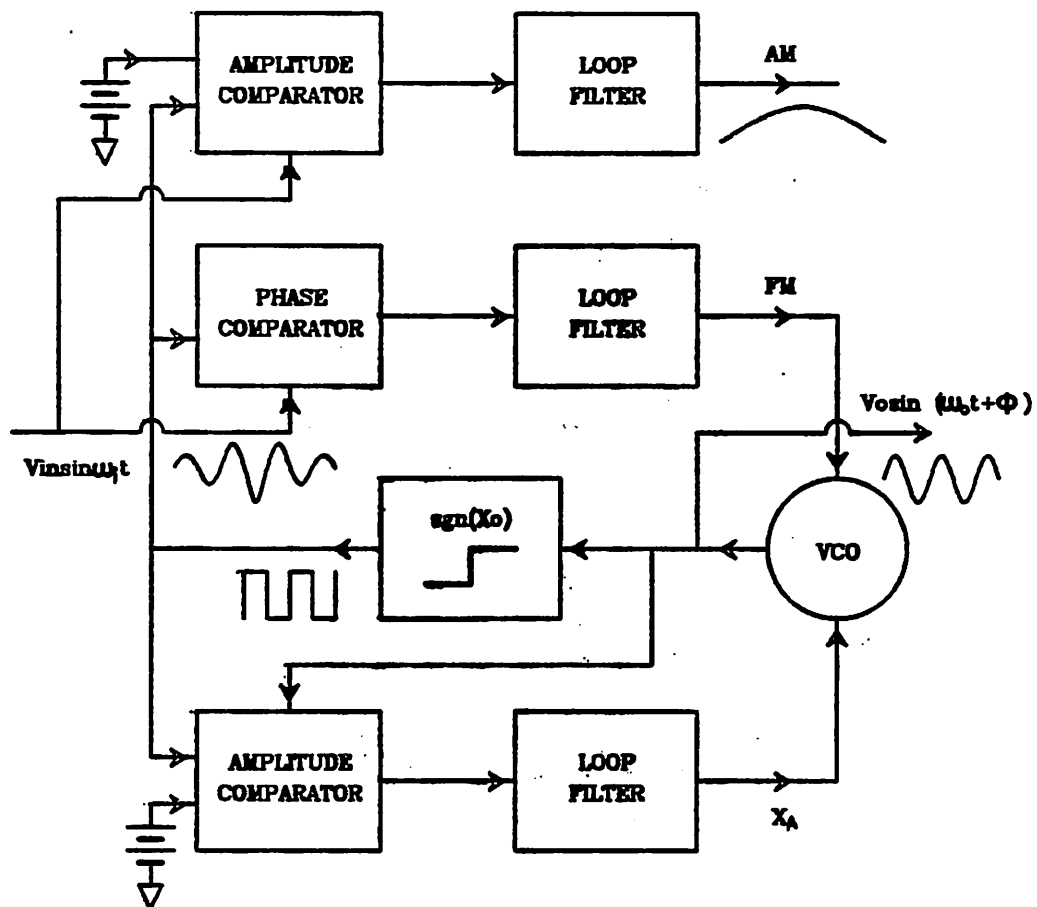
Figure 7.7. System Configuration for Amplitude and Frequency Demodulation

7.4. Topics for Future Studies

Based on the above arguments, we may conclude that unless special design precautions are taken, replica-type filters are not practical. The system is most useful for applications which would usually be performed by PLLs. However, even for these functions some design aspects of the system have to be revised and if possible, improved in order to make the VLL a system easy to design and use. These revisions and possible improvements can serve as topics for future studies, among them we can list:

(1) *Definition of the free running frequency*

Presently the oscillation frequency of the VCO is determined by the **product** of resistance and capacitance. It would be very desirable to make **this frequency** a function of a ratio of two elements of the same type, such **as capacitors**.

(2) *Process independence*

This aspect is directly related to the previous one.

(3) *Gain constant enhancement*

The spectral characteristics of the output waveform could be greatly improved by making the gain larger (higher Q).

(4) *Develop new configurations*

It would be much better to make the system less dependent on the circuit at the transistor level by devising new methods for adjusting the gain constant and phase shift throughout the integrators.

APPENDIX A

Computer Simulation Programs

A.1. Linear Simulation of the Slave Filter

The following is a listing of the SPICE simulation of the linear model of the slave filter, using voltage-controlled current sources and voltage-controlled voltage sources.

Each integrator is composed of a *poly* source and a voltage-controlled current source. The *poly* source includes all the fixed coefficients found in the flow-graph representation of the slave filter and the voltage controlled source provides the function of the integrating input.

```
CAUER FILTER TEST
.SUBCKT INTEGR1  3  4  9 11  12  13  14  15
G1  7  0  POLY(1)  3  4  0.0  1.0  IC=0.0
E2  9 10  POLY(5)  11 0 12 0 13 0 14 0 15 0 0.0 -1.373E-2 1.373E-2
+ 5.53029E-2 -1.533E-2 1.0 IC=0.0,0.0,0.0,0.0,0.0
E3  9  0  POLY(1)  7 0 0.0 -1.0E6 IC=0.0
C  7 10  3.49791E-07
R  7  0  1.0E12
.ENDS INTEGR1
.SUBCKT INTEGR2  3  4  9 11  12  13  14  15
G1  7  0  POLY(1)  3  4  0.0  1.0  IC=0.0
E2  9 10  POLY(5)  11 0 12 0 13 0 14 0 15 0 0.0 -1.373E-2 1.373E-2
+-5.53029E-2 -1.533E-2 1.0 IC=0.0,0.0,0.0,0.0,0.0
E3  9  0  POLY(1)  7 0 0.0 -1.0E6 IC=0.0
C  7 10  3.49791E-07
R  7  0  1.0E12
.ENDS INTEGR2
.SUBCKT INTEGR3  3  4  9 11  12  13  14  15
G1  7  0  POLY(1)  3  4  0.0  1.0  IC=0.0
E2  9 10  POLY(5)  11 0 12 0 13 0 14 0 15 0 0.0 -1.85E-2 1.85E-2
+ 5.53029E-2 -1.533E-2 1.0 IC=0.0,0.0,0.0,0.0,0.0
E3  9  0  POLY(1)  7 0 0.0 -1.0E6 IC=0.0
C  7 10  3.49791E-07
R  7  0  1.0E12
.ENDS INTEGR3
X1  101   0  100   0  103 104 101   0  INTEGR1
X2   0  100 101   0   0  105   0   0  INTEGR2
X3  103   0  102 101 105   0   0   0  INTEGR3
X4   0  102 103   0   0   0   0   0  INTEGR3
X5   0  104 105   0   0  101   0   0  INTEGR2
X6  105   0  104 103   0  100 105 106  INTEGR1
VIN 106   0  DC 0.0  AC 1.0
RIN 106   0  1.0MEG
.AC  DEC 2000  430.0KHZ  480.0KHZ
.PRINT AC  VDB(100)  VP(100) VDB(102) VP(102) VDB(104) VP(104) VDB(105)
+ VP(105)
.PRINT AC  VDB(101) VP(101) VDB(103) VP(103)
.PLOT AC  VDB(101) VP(101) VDB(103) VP(103)
.PLOT AC  VDB(100) VP(100) VDB(102) VP(102) VDB(104) VP(104) VDB(105)
+ VP(105)
.END
```

A.2. Simulation of the VLL

The next listing shows the data input for the simulation of the locking acquisition process of the VLL. The waveforms plotted are the VCO outputs and the amplitude and phase error signals. A calculation of the total harmonic distorsion is also included in the simulation.

"for number sequence only"

```
PHASE LOCK LOOP
.SUBCKT INTEGR   3  4  6  7 14 15 19 30  1  2
M1   6   4   5   2   MES  W=90.0E-6  L=7.0E-6   AD=1.0E-9    AS=1.0E-9
M2   7   3   8   2   MES  W=90.0E-6  L=7.0E-6   AD=1.0E-9    AS=1.0E-9
M3   1   6   6   2   MDL  W=22.0E-6  L=40.0E-6  AD=2.0E-10   AS=1.0E-9
M4   1   7   7   2   MDL  W=22.0E-6  L=40.0E-6  AD=2.0E-10   AS=1.0E-9
M5   5  14   8   2   MDL  W=11.0E-6  L=60.0E-6  AD=1.0E-10   AS=1.0E-10
M6   6  15   9   2   MDL  W=52.0E-6  L=8.0E-6   AD=5.2E-10   AS=4.0E-8
M7   1   6  10   2   MES  W=90.0E-6  L=7.0E-6   AD=9.0E-10   AS=9.0E-10
M8   1   7  11   2   MES  W=90.0E-6  L=7.0E-6   AD=9.0E-10   AS=9.0E-10
M9   5  30   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=9.0E-10
M10  8  30   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=9.0E-10
M11  6  11   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=1.5E-9
M12  7  11   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=1.5E-9
M13 19  10   0   2   MES  W=360.0E-6 L=8.0E-6   AD=3.6E-9    AS=5.0E-9
M14  1  19  19   2   MDL  W=44.0E-6  L=40.0E-6  AD=4.0E-10   AS=2.0E-9
M15 10  30   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=1.5E-9
M16 11  30   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=1.5E-9
C1   9  19  12.20E-12
.ENDS INTEGR
.SUBCKT COUPLED 3  4  6  7  9  10  1  2
M1   6   3   5   2   MES  W=90.0E-6  L=7.0E-6   AD=8.0E-10   AS=2.0E-9
M2   7   4   8   2   MES  W=90.0E-6  L=7.0E-6   AD=8.0E-10   AS=2.0E-9
M3   5  10   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M4   8  10   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M5   5   9   8   2   MES  W=10.0E-6  L=5.0E-6   AD=2.0E-10   AS=2.0E-10
.ENDS COUPLED
.SUBCKT PHASER 53  54  55  58  64  65  66  67  56  57  79  60  1  2
X1  54  53  56  57  64  60  1  2  COUPLED
X2  53  54  56  57  65  60  1  2  COUPLED
X3  58  55  56  57  66  60  1  2  COUPLED
X4  55  58  56  57  67  60  1  2  COUPLED
M5   1  56  56   2   MDL  W=53.5E-6  L=40.0E-6  AD=5.0E-10   AS=2.0E-9
M6   1  57  57   2   MDL  W=53.5E-6  L=40.0E-6  AD=5.0E-10   AS=2.0E-9
M7  56  71   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M8  57  71   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M9   1  56  71   2   MES  W=90.0E-6  L=7.0E-6   AD=9.0E-10   AS=9.0E-10
M10  1  57  72   2   MES  W=90.0E-6  L=7.0E-6   AD=9.0E-10   AS=9.0E-10
M11 71  60   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M12 72  60   0   2   MES  W=90.0E-6  L=8.0E-6   AD=9.0E-10   AS=2.0E-9
M13 57  57  80   2   MDL  W=50.0E-6  L=8.0E-6   AD=8.0E-10   AS=2.0E-9
M14 79  72   0   2   MES  W=360.0E-6 L=8.0E-6   AD=3.6E-9    AS=5.0E-9
M17  1  79  79   2   MDL  W=44.0E-6  L=40.0E-6  AD=4.0E-10   AS=2.0E-9
M18 57  57  59   2   MDL  W=11.0E-6  L=40.0E-6  AD=3.0E-10   AS=3.0E-10
M19 59  59  78   2   MDL  W=11.0E-6  L=40.0E-6  AD=3.0E-10   AS=2.0E-7
C1  79  78 100.00E-12
C2  79  80   3.00E-12
.ENDS PHASER
X1  61 101 100  61  64  65  66  67  18  27  15  60  1  2  PHASER
X2 100  61 101  61  64  65  66  67  28  29  14  60  1  2  PHASER
X3  61 100 107 108  14 107 101  60  1  2  INTEGR
X4 101  61 109 110  14  15 100  60  1  2  INTEGR
X5  61 102 111 112  14 111 103  60  3  2  INTEGR
```

```
X6 103 61 113 114 14 15 102 60  3  2 INTEGR
X7  61 104 115 116 14 115 105 60  5  2 INTEGR
X8 105 61 117 118 14 15 104 60  5  2 INTEGR
C5  109  0  2.0E-12
C6  113  0  2.0E-12
C7  117  0  2.0E-12
C8  109  0  0.18E-12
C9  110 104 0.675E-12
C10 113  0  0.675E-12
C11 110 103 0.2E-12
C12 114 105 0.2E-12
C13 113 101 0.2E-12
C14 117  0  0.18E-12
C15 117 103 0.2E-12
C16 118 100 0.675E-12
C17 113  0  0.18E-12
C18 109  0  0.2E-12
C19 118  0  0.2E-12
C20 105 107 0.675E-12
C21 101 115 0.675E-12
M4   1 18 18  2 MDL W=3.0E-6  L=40.0E-6 AD=1.0E-10 AS=5.0E-10
M5   1 28 28  2 MDL W=1.5E-6  L=40.0E-6 AD=1.0E-10 AS=5.0E-10
M6   1 29 29  2 MDL W=1.5E-6  L=40.0E-6 AD=1.0E-10 AS=5.0E-10
M7   1 61 60  2 MES W=90.0E-6 L=7.0E-6  AD=9.0E-10 AS=1.5E-9
M8  61 61 62  2 MES W=90.0E-6 L=7.0E-6  AD=9.0E-10 AS=1.5E-9
M9  60 60  0  2 MES W=90.0E-6 L=8.0E-6  AD=9.0E-10 AS=1.5E-9
M10 62 60  0  2 MES W=90.0E-6 L=8.0E-6  AD=9.0E-10 AS=1.5E-9
M11  1 61 61  2 MDL W=11.0E-6 L=40.0E-6 AD=3.0E-10 AS=3.0E-10
VDD1  1 0  PULSE(0.00 5.00 0.0 20.0NS 20.0NS 1.0 2.0)
VDD3  3 0  PULSE(0.00 5.00 2.0US 20.0NS 20.0NS 1.0 2.0)
VDD5  5 0  PULSE(0.00 5.00 4.0US 20.0NS 20.0NS 1.0 2.0)
VBS   0 2  DC 0.00
V64  64 0  PULSE(0.00 5.00 0.00US 25.0NS 25.0NS 1.05US 2.20US)
V65  65 0  PULSE(0.00 5.00 1.10US 25.0NS 25.0NS 1.05US 2.20US)
V66  66 0  PULSE(0.00 5.00 0.55US 25.0NS 25.0NS 1.05US 2.20US)
V67  67 0  PULSE(0.00 5.00 1.65US 25.0NS 25.0NS 1.05US 2.20US)
.TRAN 50.0NS 60.0US 40.0US
.PLOT TRAN V(100 )V(101) V(14) V(15)
.PRINT TRAN I(VDD1) V(102) V(105) V(101) V(103) V(104) V(14) V(15)
.PRINT TRAN V(107) V(108) V(61) V(60)
.FOUR 454.545KHZ V(101) V(100) V(14) V(15) V(102) V(103) V(104) V(105)
.OPTIONS LIMTIM=10 LIMPTS=100000 ITL5=400000 LVLCOD=1 ACCT
.OPTIONS ITL1=10000
.MODEL MES NMOS(LEVEL=2 CGS=1.00E-10 CGD=1.00E-10 GAMMA=0.324
+        TOX=0.7E-7 PB=0.6 NSUB=7.72E14 VTO=0.803 XJ=1.0E-6 LD=0.1
+        UO=784.904 UCRIT=2.537E4 UEXP=0.00828 UTRA=0.25)
.MODEL MEL NMOS(LEVEL=2 CGS=1.00E-10 CGD=1.00E-10 GAMMA=0.348
+        TOX=0.7E-7 PB=0.6 NSUB=8.86E14 VTO=0.99 XJ=1.0E-6 LD=0.1
+        UO=642.999 UCRIT=1.596E5 UEXP=0.188 UTRA=0.25)
.MODEL MDS NMOS(LEVEL=2 CGS=1.00E-10 CGD=1.00E-10 GAMMA=0.355
+        TOX=0.7E-7 PB=0.6 NSUB=9.274E14 VTO=-3.17 XJ=1.0E-6 LD=0.1
+        UO=593.387 UCRIT=6.136E4 UEXP=-0.141 UTRA=0.25)
.MODEL MDL NMOS(LEVEL=2 CGS=1.00E-10 CGD=1.00E-10 GAMMA=0.323
```

```
+       TOX=0.7E-7 PB=0.6 NSUB=7.66E14 VTO=-2.86 XJ=1.0E-6 LD=0.1
+       UO=716.999 UCRIT=1.526E5 UEXP=-0.108 UTRA=0.25)
.END
```

APPENDIX B

Process Flow Description

The single-layer of polysilicon NMOS process used [26] is characterized by the following features:

(1) The photolithography is done using positive resist and a projection aligner.

(2) The field-oxide regions are made by local oxidation.

(3) Ion implantation is used for all the predeposition steps including: field implant, threshold shifting, source and drain diffusions, and capacitor-bottom plate.

(4) Both the silicon nitride and the polysilicon areas are etched using a barrel type of plasma reactor.

(5) The glass which isolates the poly regions from the metal layer is done by fully oxidizing an extra layer of phosphorus-doped polysilicon. This approach was chosen to solve a problem related to the unreliable functioning of the VAPOX deposition system existing at the ERL laboratory.

The process flow is described together with a sequence of Figs. showing the resulting cross-section. The dimensions in the figures are not in scale.

B.1. Silicon Gate NMOS Process

(1) *Initial Wafer Cleaning - P-type*, 20–40Ωcm, <100>

    a.   TCE clean, 60°C, 10min (Degrease) (Watch temperature : Boiling TCE will shatter wafers)

    b.   Dip in acetone

    c.   Dip in methyl alcohol

    d.   Rinse in De-ionized (DI) water

    e.   Piranha etch $(H_2SO_4 : H_2O_2$ - 5:1) for $10min$.

    f.   Rinse thoroughly in running DI water

    g.   Dip in $HF : H_2O$ (1:10) for 20 seconds

    h.   Rinse in DI water

    i.   Blow dry

    j.   Inspect under collimated light for dust. (If dust remains, repeat from h.; if that doesn't work, repeat from a.)

(2) *Initial Oxidation - 700Å, Initial Oxide Furnace*

    a.   Dry O_2, 920°C, $60min$. (temperature setting =925)

    b.   Dry N_2 (anneal), 900°C, $20min$.

(3) *Nitride Deposition* - 1000Å, Nitride Deposition Furnace

    a.   Time $50min$, boat position first mark on push rod.

(4) *Positive Photoresist (PR) Step, Mask #1 : Diffusion mask.*

    a.   HMDS treatment (module 1)

        1. N_2 purge, $5min$.

        2.   Load wafers

        3.   Bubble HMDS, $1min$.

        4. N_2 purge, $5min$.

b.   Spin AZ 1450J, 6000 rpm, 30 seconds. (PR thickness =1.4μm) (module 2)

c.   Soft-bake, 85–90°C, 15-20 italic "min" (module 3).

d.   Align and expose (module 4) (Blow off dust on top and bottom)

e.   Develop, AZ developer (DI H_2O :Developer - 1:1), 1min (module 5).

f.   Rinse in DI water and blow dry (module 6)

g.   Inspect (module 7)

h.   Hardbake, 110–120°C, 20 italic "min" (module 8).

i.   PR de-scum, 5min, 65°C, pressure ≈0.76Tor of O_2 (module 9)

j.   Plasma etch, wafer perpendicular to barrel axis, pressure ≈0.1Tor of

SF_6 etch rate ≈70$\frac{\AA}{min}$, total time ≈25min, etch until clears and 30%

overetch (See plasma etcher instructions).

(5) *Field Implant Step*

(See Fig. B.1)

Implant Boron (B_{11}), Dose =3.5×10^{13}, energy = 70keV, angle =8°

(6) *Local Oxidation Step (LOCOS)* (≈1μm)

a.   Piranha Clean, H_2SO_4 : H_2O_2 - 5:1, 5min (module 10).

b.   Wet O_2, 925°C, 720min, flow-meter setting =4cm

c.   Dry N_2, 925°C, 20min, flow-meter setting =4cm

(7) *Bottom-plate Capacitor: Mask #2*

a.   Plasma etch, wafer perpendicular to barrel axis, pressure ≈0.1Tor of

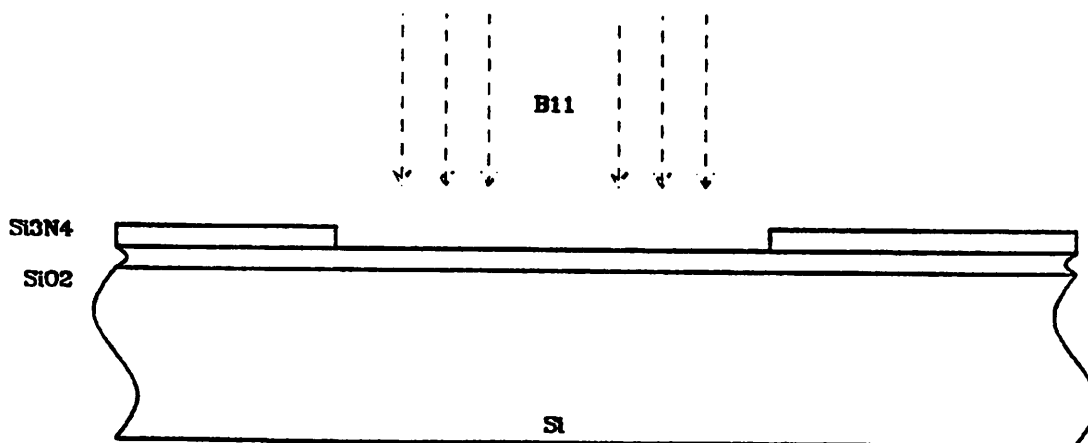SF_6 etch rate ≈70$\frac{\AA}{min}$, total time ≈25min, etch until clears and 30%

overetch

Figure B.1.

b. Oxide etch, HF (H_2O : HF - 10:1) etch rate $\approx 250 \frac{\text{Å}}{min}$ (etch time $\approx 3.0min$)

c. Piranha Clean, (module 10). (To create a very thin layer of oxide which helps the adhesion of the PR).

d. Positive Photoresist (PR) Step, Mask #2 : Capacitor bottom-plate mask. (modules 1 through 9)

(8) *Capacitor Implant*

Implant Arsenic, Dose $= 1.0 \times 10^{14}$, energy $= 120keV$, angle $= 8°$

(9) *Depletion Mask: Mask #3*

a. Piranha clean (module 10)

b. Positive Photoresist (PR) Step, Mask #3 : Depletion mask. (modules 1 through 9)

(10) *Depletion Implant*

Implant Arsenic, Dose $=1.0\times10^{12}$, energy $= 120keV$, angle $=8°$

(11) *Gate Oxide Step*

(See Fig. B.2)

a. Piranha clean (module 10)

b. TCE clean P+ drive-in furnace at least 12 hours before use

c. Grow 300$\overset{\circ}{A}$ of oxide:

    1. Dry O_2, temperature $=1025°C$, time $=15min$,

    2. Dry N_2 (anneal), temperature $=900°C$, time $=20min$.

d. Oxide etch to bare silicon, HF (H_2O : HF - 10:1) etch rate $\approx 250\dfrac{\overset{\circ}{A}}{min}$

    (etch time $\approx 1.0min$)

e. Grow 700$\overset{\circ}{A}$ of oxide:

    1. Dry O_2, temperature $=1025°C$, time $=15min$,

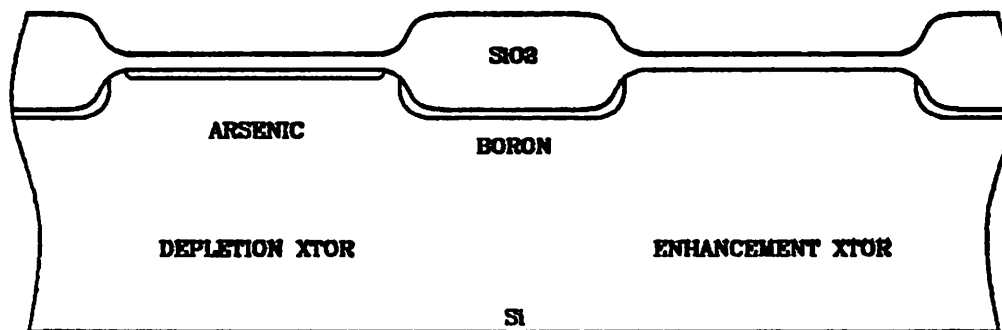**Figure B.2.**

2. Dry N_2 (anneal), temperature =900°C, time =20min.

(12) *Enhancement Mask: Mask #4*

a. Positive Photoresist (PR) Step, Mask #3 : Depletion mask. (modules 1 through 9)

(13) *Enhancement Implant*

Implant Boron (B_{11}), Dose =4.0×10^{11}, energy = 50keV, angle =8°. (The implant is done through the gate oxide).

(14) *Poly Deposition*

a. Piranha clean (module 10)

b. Polysilicon deposition, thickness ≈5000$\overset{\circ}{A}$, boat inserted to first mark of push rod, pressure =0.6Tor (see instructions for poly deposition system).

c. Phosphorus predeposition, temperature =950°C (module 11)

   1. 5min push in N_2 at 5.0cm

   2. 5min in N_2, O_2 at 5.0cm and 2.5cm respectively

   3. 20min in $POCL$ (source)

   4. 15min anneal in N_2 at 5.0cm

d. P oxide dip, 1min in HF (H_2O : HF - 10:1)

(15) *Polysilicon Mask: Mask #5*

a. Piranha Clean, (module 10). (To create a very thin layer of oxide which helps the adhesion of the PR).

b. Positive Photoresist (PR) Step, Mask #5 : Polysilicon gate mask. (modules 1 through 9)

(16) *Polysilicon Etch*

Plasma etch, wafer perpendicular to barrel axis, pressure $\approx 0.1\,Tor$ of SF_6 etch rate $\approx 300\,\frac{\mathring{A}}{min}$; total time $\approx 18min$, etch until clears and 10% overetch

(17) *Source and Drain Implant*

(See Fig. B.3)

a. PR plasma etch, wafer perpendicular to barrel axis, pressure $\approx 0.76\,Tor$ of O_2, power $=150\,Watts$, total time $\approx 30min$,

b. Piranha clean (module 10)

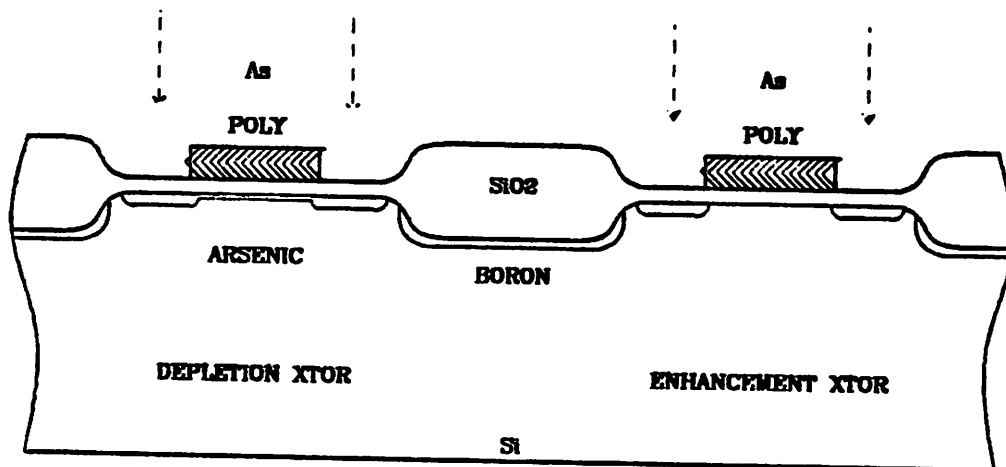c. Implant Arsenic, Dose $=3.0\times 10^{15}$, energy $=200keV$, angle $=8°$

Figure B.3.

(18) *Polysilicon Deposition*

(source of oxide)

   a.   Piranha clean (module 10)

   b.   Polysilicon deposition, thickness $\approx 3000\mathring{A}$, boat inserted to first mark of push rod, pressure $=0.6 Tor$ (see instructions for poly deposition system).

   c.   Phosphorus predeposition, temperature $=950°C$ (module 11).

(19) *Source and Drain Drive-in and Polysilicon Oxidation*

   a. N_2, 1025°C, 20min, flow-meter setting $=4cm$

   b.   Wet O_2, 925°C, 200min, flow-meter setting $=4cm$ ($\approx 0.7\mu m$)

   c.   Dry N_2, 925°C, 20min, flow-meter setting $=4cm$

(20) *Contact Mask: Mask #6*

   a.   Positive Photoresist (PR) Step, Mask #6 : Contact mask. (modules 1 through 9)

   b.   Oxide etch, buffered HF (NH_4F : HF - 5:1) etch rate $\approx .115\frac{\mu}{min}$ (etch time $=6.0min$).

(21) *Polysilicon Deposition*

(to avoid spiking of the Al into the silicon and to improve step coverage)

   a.   Piranha clean (module 10)

   b.   Dip in HF : H_2O (1:10) for 20 seconds

   c.   Polysilicon deposition, thickness $\approx 1000\mathring{A}$, boat inserted to first mark of push rod, pressure $=0.6 Tor$ (see instructions for poly deposition system).

    d.   Phosphorus predeposition, temperature $=950°C$ (module 11).

(22) *Metal Deposition*

9000$\overset{\circ}{A}$ Aluminum

    a.   *HF* dip (*HF* :water - 1:10), 10 sec. (just until back of wafer repeals water)

    b.   Rinse in DI water

    c.   Bake under IR lamp, 15min.

    d.   Metal deposition, (use big VEECO and thickness monitor for more accurate results), two staples is usually enough.

(23) *Metal Mask: Mask #7*

Positive Photoresist (PR) Step, Mask #7 : Metal mask. (modules 1 through 9)

(24) *Aluminum Patterning*

(See Fig. B.4)

    a.   Etch half of the metal thickness at 45–50°C ($\approx$1.5min)

    b.   Rinse very gently in DI water for 1min

    c.   Hardbake to reflow the resist at 140°C during 25min

    d.   Etch the rest of the metal at 45–50°C, until it clears, (time $\approx$1.5min)

    e.   Plasma etch, wafer perpendicular to barrel axis, pressure $\approx$0.1Tor of SF_6 etch rate $\approx$300$\dfrac{\overset{\circ}{A}}{min}$, total time $\approx$4min, etch until clears and 10% overetch
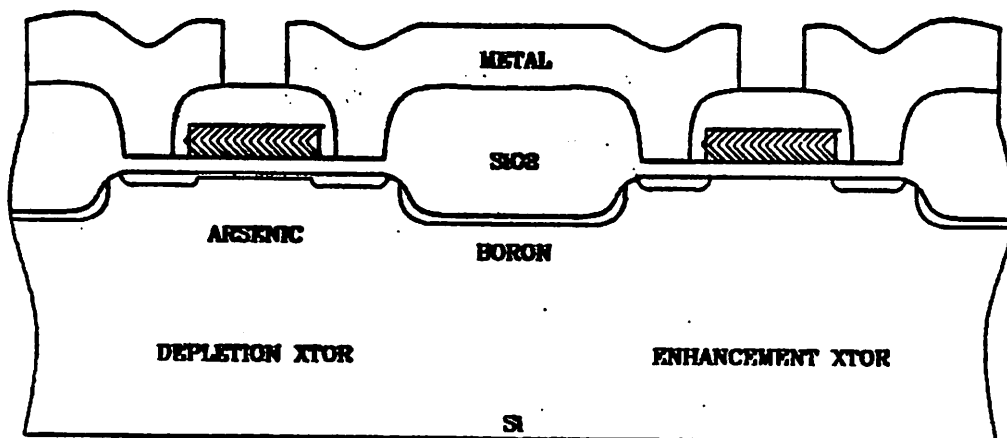
(25) *Aluminum Sintering*

Figure B.4.

a.   Dry the wafer very carefully by exposing to an IR light source for 15*min*

b.   Remove PR with RT_2 or AZ stripper, don't use Piranha etching because it will also etch the aluminum.

c.   Use the sintering furnace with the following settings: temperature $=450°C$, time $=15min$, with forming gas 14 cm.

(26) *Backside Etching*

a.   Immediately after sintering the aluminum spin a thick layer of AZ photoresist at 3000*rpm*

b.   Hardbake at $130°C$ during 25*min*

c.   Oxide etch, buffered HF (NH_4F : HF - 5:1) etch rate $\approx.115\frac{\mu}{min}$; (etch time $\approx 10min$) Let the wafer float with face up, this decreases the risk of PR lift-off.

    d.   Rinse in DI water for $1min$

    e.   Dry under the IR light source for $15min$

    f.   Strip the PR with RT_2

(27) **GOOD LUCK!**

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