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BIPOLAR-JFET-MOSFET NEGATIVE RESISTANCE DEVICES[†]

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ABSTRACT

A unified approach is given for generating all negative-resistance circuits made of 2 transistors and linear positive resistors only. The 2 transistors may be bipolar (npn or pnp), JFET (n-channel or p-channel), MOSFET (n-channel or p-channel), or their combinations. Since the circuits do not require an internal power supply, they are passive and can be integrated as a 2-terminal device in monolithic form.

Two algorithms are given for generating a negative-resistance device which exhibits either a type-N v-i characteristic similar to that of a tunnel diode, or a type-S v-i characteristic similar to that of a four-layered pnpn diode.

Hundreds of new and potentially useful negative resistance devices have been generated. A selected catalog of many such prototype negative-resistance devices is included for future applications.

[†]This research is support in part by the Joint Services Electronics Program Contract F49620-79-C-0178.

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1. INTRODUCTION

The announcement of the first negative-resistance device in 1918 [1] was greeted with skeptism by some and fascination by others. As the name "negative resistance" seems to suggest that the device obeys Ohms law ($v = Ri$) with $R < 0$, many physicists and engineers had dismissed this announcement as nonsense because it clearly violates the conseration of energy. This controversy was quickly resolved when it became clear that the device is actually nonlinear and that the term "negative resistance" implies only that the slope is negative at a certain region of the v-i characteristic. So long as this characteristic lies within the first and third quadrants of the v-i plane, the device is passive and is therefore physically realizable without an external source of energy, e.g., a battery.

Spurred by the discovery of the dynatron, and its many potential applications, many vacuum tube negative-reistance circuits have since been invented and reported in the literature [2-18].

The invention of the transistor in 1948 has naturally triggered a search for solid state negative-resistance devices. Unlike vacuum tubes, however, the physics of solid state devices is much more complex. It was not until 1958 before the first negative-resistance solid state device, called the tunnel diode, was invented by Esaki [19]. In fact, so exotic was the physical mechanism responsible for the negative resistance that a Nobel prize in physics was awarded to Esaki in 1973. It took another 8 years before another promising 2-terminal solid state negative-resistance device, called the Gunn diode, was invented [20]. Even more exotic is the physical mechanism responsible for this differential negative resistance that it took another researcher to explain the Gunn effect [21].

Nothwithstanding the much more difficult challenge (compared to that of the vacuum tube era), the search for new solid state negative-resistance devices has continued unabated over the years [22-55]. While some of the negative-resistance devices reported in [22-55] are bulk semiconductor devices, most consist of combination of bipolar transistors, JFETs, and MOSFETs.

Almost all of the negative-resistance devices reported in the literature so far were discovered either by accident, or with the help of intuition and various ad hoc techniques. This is why most papers on this subject are concerned only with one negative-resistance circuit. Moreover, since the circuit is usually presented as if "pulling a rabbit out of a hat," the

reader is often left with the perplexed question of how the circuit was originally conceived.

One of our objectives in this paper is to remove the mystery behind the discovery of these circuits by showing how they can be systematically derived via a unified approach. In particular, we will present two simple algorithms for generating negative-resistance devices using only linear positive resistors and two transistors, which may be bipolar JFET, or MOSFET [56], or their combinations.

Unlike many negative-resistance circuits in the literature which require an internal power supply, all circuits generated by our algorithm are source free. Hence, once integrated and encapsulated in a standard package, our circuit becomes a 2-terminal negative-resistance device, just like the tunnel diode, and the Gunn diode.

In fact, the main contribution of this paper is the wholesale presentation of numerous new two-transistor negative-resistance circuit configurations†, both in the body of the paper, and in the form of a selected catalog in the Appendix. Each of these circuit configurations is potentially a useful 2-terminal negative-resistance device.

A type-N device is characterized by a continuous non-monotonic voltage-controlled v-i curve having at most one maximum (peak) and one minimum (valley), as shown in Fig. 1(a). The "dual" characteristic shown in Fig. 1(b) defines a type-S device.

Using our algorithm, all negative-resistance circuits reported in the literature (using only linear positive resistors, and two bipolar, JFET or MOSFET transistors, or their combinations) can be generated. Consequently, only a few typical circuits will be presented in this paper to illustrate our algorithm. The symbols for the bipolar, JFET, and MOSFET transistors are shown in Fig. 2.

In Section 2, several type-N devices using at most 2 linear positive resistors are presented first. The algorithm for generating type-N devices is then given without proof.

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†This is in sharp contrast with previous papers on this subject [1-55] which, with few exceptions, contained only one new circuit in each paper.

In Section 3, several type-S devices using at most 2 linear positive resistors are presented first. The algorithm for generating type-S devices is then given without proof.

The theory behind the algorithms presented in Sections 2 and 3 is given in Section 4.

For future reference, a selected catalog of negative-resistance devices generated using the algorithms in Sections 2 and 3 is given in the Appendix, along with their typical v-i characteristics.

2. TYPE-N (VOLTAGE-CONTROLLED) DEVICES

A. Intrinsic Type-N Devices

A type-N device is said to be intrinsic if it contains no resistors. Using the type-N algorithm to be presented below, we have generated the 3 circuits shown in Fig. 3: the circuit in Fig. 3(a) is made of 2 complementary MOSFETs, that in Fig. 3(b) is made of 2 complementary JFETs, and the circuit in Fig. 3(c) is made of an N-channel JFET and a P-channel MOSFET. These are the only intrinsic type-N devices made of 2 transistors.†

We have simulated these circuits using typical device parameters. One typical v-i characteristic for each of these circuits is shown in Figs. 3(a), (b), and (c), respectively.

B. Type-N Devices Requiring One Resistor

Three type-N devices requiring one resistor are shown in Fig. 4. In addition, the circuit requires 2 complementary MOSFETs in Fig. 4(a), 2 complementary JFETs in Fig. 4(b), and a P-channel MOSFET and an n-channel JFET in Fig. 4(c). The v-i characteristic for each circuit corresponding to a typical value of R is shown in Figs. 4(a), (b), and (c), respectively.

C. Type-N Devices Requiring Two Resistors

Twelve type-N devices requiring two resistors are shown in Figs. 5-8. In addition, the 3 circuits in Fig. 5 contain 2 complementary MOSFETs; the

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†Two transistors are said to be complementary if one is N-channel and the other is P-channel. Actually, for circuits involving MOSFETs, there are a few more circuit variations that can be obtained by connecting the substrate terminal to another terminal of the circuit. However, this distinction is only minor and we prefer to regard all these variations as basically the same circuit.

3 circuits in Fig. 6 contain 2 complementary JFETs; the 3 circuits in Fig. 7 contain a bipolar transistor and a MOSFET or a JFET; the 3 circuits in Fig. 8 contain an N-channel MOSFET and a P-channel JFET.

A typical v-i characteristic is shown below each of these circuits.

D. Type-N Algorithm

In general, any type-N device can be systematically generated using the following procedure:

Step 1. Start with the two-transistor feedback structure shown in Fig. 9, where transistor T_1 or T_2 can assume any one of the device symbols shown in Figs. 10, 11, and 12. Here, the terminal marked with an asterisk (*) always corresponds to the horizontal terminal in Fig. 9.

Step 2. Connect a current source via a soldering-iron entry across a pair of nodes in the feedback structure obtained from Step 1. There are only 3 distinct ways of doing this: they are shown in Figs. 13(a), (b), and (c), respectively.

Step 3. Connect "n" linear positive resistors to any of the 3 circuit configurations obtained from Step 2, where n = 0,1,2,..., etc. Here, each resistor may be inserted through any wire via a plier-type entry, or across any pair of nodes via a soldering-iron entry. As will be shown in Section 4, there is no need to connect a resistor either in series, or in parallel, with the current source.

For example, if we pick the circuit configuration in Fig. 13(a) and choose n = 1, we would generate a maximum of 7 topologically distinct circuits, as shown in Fig. 14.

Step 4. Each circuit generated from Step 3 is a candidate for a type-N negative-resistance device. However, not all such candidates will exhibit a negative resistance characteristic. In other words, Steps 1-3 are necessary but not sufficient conditions for a 2-transistor circuit to be a type-N negative resistance device. The final step in this algorithm therefore consists of actually simulating the circuit using a computer simulation program, such as SPICE [57] for different driving-point currents I_S. If no negative resistance characteristic is obtained for all values of resistances and device

parameters[†], the candidate is rejected.

There are a number of inspection methods which allow one to eliminate a candidate from Step 3 without computer simulation. These methods are described in Section 4.

Using the above algorithm, we have generated hundreds of type-N devices using bipolar, JFET, and MOSFET transistors. A small subset of these circuits are collected in Appendix A along with a typical family of v-i characteristics corresponding to different values of the resistances.

3. TYPE-S (CURRENT-CONTROLLED) DEVICES

A. Intrinsic Type-S Devices

No intrinsic type-S device made of only 2 transistors (bipolar, JFET, MOSFET or their combination) exists.

B. Type-S Devices Requiring One Resistor

The only type-S device made of 2 transistors and one resistor is shown in Fig. 15, along with a typical v-i characteristic.

C. Type-S Devices Requiring Two Resistors

Eight type-S devices requiring two resistors are shown in Figs. 16-18. In addition, the 2 circuits in Fig. 16 contain 2 complementary bipolar transistors; the 3 circuits in Fig. 17 contain a bipolar transistor and a MOSFET; the 3 circuits in Fig. 18 contain 2 MOSFETs in (a), a bipolar and a JFET transistor in (b), and a MOSFET and a JFET transistor in (c), respectively.

A typical v-i characteristic is shown below each of these circuits.

D. Type-S Algorithm

In general, any type-S device can be systematically generated using the following "dual" procedure:

[†]In practice, only a few resistance values and device parameters are usually adequate to eliminate a candidate.

Step 1. Start with the two-transistor feedback structure shown in Fig. 9, where transistor T_1 or T_2 can assume any one of the device symbols shown in Figs. 10, 11, and 12. Here, the terminal marked with an asterisk (*) always corresponds to the horizontal terminal in Fig. 9.

Step 2. Connect a voltage source via a plier-type entry through a terminal in the feedback structure obtained from Step 1. There are only 3 distinct ways of doing this: they are shown in Figs. 19(a), (b), and (c), respectively.

Step 3. Connect "n" linear positive resistors to any of the 3 circuits obtained from Step 2, where n = 0,1,2,...,etc. Here, each resistor may be inserted through any wire via a plier-type entry, or across any pair of nodes via a soldering-iron entry. As will be shown in Section 4, there is no need to connect a resistor either in series, or in parallel, with the voltage source.

For example, if we pick the circuit configuration in Fig. 19(c) and choose n = 1, we would generate a maximum of 7 topologically distinct circuits, as shown in Fig. 20.

Step 4. Each circuit generated from Step 3 is a candidate for a type-S negative-resistive device. However, not all such candidates will exhibit a negative resistance characteristic. In other words, Steps 1-3 are necessary but not sufficient conditions for a 2-transistor circuit to be a type-S negative resistance device. The final step in this algorithm therefore consists of actually simulating the circuit using a computer simulation program, such as SPICE [57] for different driving-point voltages V_s. If no negative resistance characteristic is obtained for all values of resistances and device parameters, the candidate is rejected.

4. THE UNIFIED APPROACH

To derive the two algorithms presented in the previous sections for systematically generatingall 2-transistor negative-resistance devices, consider the current-driven one-port N_I shown in Fig. 21(a) and the voltage-driven one-port N_V shown in Fig. 22(a). N_I and N_V are assumed to contain exactly 2 transistors and "n" linear positive resistors. The 2 transistors may be any combination of bipolar (npn or pnp), JFET (n-channel or p-channel), and MOSFET (n-channel or p-channel) transistors.

Let $\hat{N}_I$ be a simplified one-port obtained by replacing each resistor inside N_I by either a short circuit, or by an open circuit. We will refer to the circuit in Fig. 21(b) as the open-circuited one-port $\hat{N}_I$ associated with N_I (since the port is open circuited).

Let N_V be a simplified one-port obtained by replacing each resistor inside N_V by either a short circuit, or by an open circuit. We will refer to the circuit in Fig. 22(b) as the short-circuited one-port $\hat{N}_V$ associated with N_V (since the port is short-circuited).

Note that $\hat{N}_I$ and $\hat{N}_V$ contain only 2 transistors and connecting wires. We say that the open-circuited one-port $\hat{N}_I$ in Fig. 21(b), or the short-circuited one-port $\hat{N}_V$ in Fig. 22(b), exhibits a feedback structure if, and only if, it can be redrawn into the "cross-coupled" configuration shown in Fig. 9.

Our algorithms in Sections 2 and 3 are based on the following remarkable result due to Nielsen and Willson [58-59]:

Theorem. (Nielsen and Willson)

Let each bipolar transistor be modeled by the Ebers-Moll equation as in [58]. Let each JFET or MOSFET be described by the typical family of v-i characteristics assumed in [59].

1. A necessary condition for the current-driven one-port N_I in Fig. 21(a) to have multiple solutions is that the open-circuited one-port $\hat{N}_I$ associated with N_I exhibits a feedback structure.

2. A necessary condition for the voltage-driven one-port N_V in Fig. 22(a) to have multiple solutions is that the short-circuited one-port $\hat{N}_V$ associated with N_V exhibits a feedback structure.

Corollary 1. In order for a 2-transistor one-port N to exhibit a type-N (voltage-controlled) negative resistance v-i characteristic, it is necessary that the open-circuited one-port $\hat{N}_I$ in Fig. 21(b) exhibits a feedback structure.

Proof. By definition, a one-port is type-N if there exists at least one port current $i = I_s$ such that there correspond more than one port voltage. Hence Corollary 1 follows upon driving the one-port N_I by a current source and invoking the necessary condition from the above theorem. □

Corollary 2. In order for a 2-transistor one-port N to exhibit a type-S (current-controlled) negative resistance v-i characteristic, it is necessary that the short-circuited one-port $\hat{N}_V$ in Fig. 22(b) exhibit a feedback structure.

Proof. Follows by duality.

Remarks.

The open-circuited one-port $\hat{N}_I$ in Fig. 21(b), or the short-circuited one-port $\hat{N}_V$ in Fig. 22(b) cannot exhibit a feedback structure under the following situations:

(a) Terminal (*) of T_1 is connected to terminal (*) of T_2, where terminal (*) denotes either the base (for a bipolar transistor) or the gate (for a JFET or MOSFET) of the transistor (see Figs. 10-11).
(b) A pair of terminals of T_1 (resp., T_2) are short-circuited.
(c) A terminal of either T_1 or T_2 is open-circuited.
(d) N contains only one trnasistor.

Corollary 3. In order for N to exhibit a negative resistance, it is necessary that both transistors be operating in the normal active region† of the device over the entire dynamic range of the negative resistance.

Proof. If a bipolar, JFET, or MOSFET transistor is not biased in the normal active region, then it can be realistically modeled by a circuit made of linear resistors, batteries and/or current sources, using the techniques described in [60]. Since the resulting circuit in effect contains only one transistor, it cannot have a feedback structure in view of Remark (d).

We are now ready to derive the algorithms in Sections 2 and 3.

A. Type-N Algorithm

Applying Corollary 1, we find there are only 3 distinct configurations for a current-driven 2-transistor circuit without resistors to posses a feedback structure; namely, the configurations in Figs. 13(a), (b), and (c). Since all type-N circuits must reduce to one of these 3 configurations after each resistor is replaced by either a short circuit, or an open circuit, we can systematically generate candidates for type-N negative resistance circuits

†By normal active region, we mean the region where the device is biased for small-signal amplification.

by connecting "n" resistors to the circuit via all possible combinations of plier-type and soldering-iron entries.

There is no need, however, to connect a resistor either in series, or in parallel with the current source I_s. Indeed, if N' is a type-N device, then connecting a linear positive resistor in series as shown in Fig. 23(a) could lead to a multivalued v-i characteristic, which is no longer type-N, as shown in Fig. 23(b). Similarly, connecting a linear positive resistor in parallel as shown in Fig. 23(c) could lead to a monotone-increasing v-i characteristic which is no longer type-N, as shown in Fig. 23(d). In either case, the addition of the linear resistor either in series, or in parallel, will only reduce the chances of obtaining a type-N v-i characteristic.

As we let $n = 0,1,2,\ldots$, we would systematically generate all type-N circuit candidates containing, $0,1,2,\ldots$, resistors.

Since the "feedback structure" is only a necessary condition for the above candidates to be a type-N device, it is essential to simulate the v-i characteristic using a circuit-simulation program with different values of the resistors and device parameters.

The type-N circuits given in Section 2 and in Appendix A are generated using this algorithm.

B. Type-S Algorithm

Applying Corollary 2, we find there are only 3 distinct configurations for a voltage-driven 2-transistor circuit without resistors to possess a feedback structure; namely, the configurations in Figs. 19(a), (b), and (c). Since all type-S circuits must reduce to one of these 3 configurations after each resistor is replaced by either a short circuit, or an open circuit, we can systematically generate candidates for type-S negative-resistance circuits by connecting "n" resistors to the circuit via all possible configurations of plier-type and soldering-iron entries.

There is no need, however, to connect a resistor either in series, or in parallel with the voltage source V_s. Indeed, if N' is a type-S device, then connecting a linear positive resistor in series as shown in Fig. 24(a) could lead to a monotone-increasing v-i characteristic, which is no longer type-S, as shown in Fig. 24(b). Similarly, connecting a linear positive resistor in parallel as shown in Fig. 24(c) could lead to a multivalued v-i characteristic, which is no longer type-S, as shown in Fig. 24(d). In either

case, the addition of the linear resistor either in series, or in parallel, will only reduce the chances of obtaining a type-S v-i characteristic.

As we let n = 0,1,2,..., we would systematically generate all type-S circuit candidates containing 0,1,2,..., resistors.

The type-S circuits given in Section 3 and in Appendix B are generated using this algorithm.

5. CONCLUDING REMARKS

We have applied both algorithms in Sections 2 and 3 and generated hundreds of type-N and type-S devices, containing up to 5 linear resistors. For future reference, we have included a small catalog of some selected type-N devices in Tables 1 and 2 of Appendix A. Also included in Appendix A are families of v-i characteristics (parameterized by different resistor values) for the last circuit in each column of Table 1 (Figs. A-1 to A-5) and Table 2 (Figs. A-6-A-7).

A small catalog of some selected type-S devices is given in Tables 3 and 4 of Appendix B. Also included in Appendix B are families of v-i characteristics (parametrized by different resistor values) for the last circuit in each column of Table 3 (Figs. A-8 to A-11) and Table 4 (Figs. A-12 to A-14).

Another catalog of selected type-N and type-S devices using only bipolar transistors and linear resistors is given in [61].

An extensive collection of families of v-i characteristics for each of the circuits listed in Tables 1-4 of Appendix A and Appendix B (except the last circuit in each column) is given in Appendix C and Appendix D.

These families of v-i characteristics are extremely useful because they show the effects of the different resistors on the shape of the characteristics. Depending on the application, one circuit may be preferred over another. In any event, the catalog of circuits given in Appendix A, Appendix B, and in [61-62] should be adequate for most applications.

It is not our objective to evaluate which of the numerous circuit configurations presented in this paper are better. Such an evaluation would depend not only on the IC technology being chosen, but also on the applications in mind. Indeed, some configurations are clearly superior for low-frequency high-power applications. Others are clearly better for high-frequency operations. This is the reason why we included a selected catalog of potentially useful prototype negative-resistance circuit configurations.

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FIGURE CAPTIONS

Fig. 1. (a) A type-N device characterized by a non-monotonic voltage-controlled v-i curve with one maximum and one minimum.
(b) A type-S device characterized by a non-monotonic current-controlled v-i curve with one maximum and one minimum.

Fig. 2. Transistor symbols: (a) npn transistor; (b) pnp transistor; (c) N-channel JFET (d) P-channel JFET; (e) N-channel MOSFET; and (f) P-channel MOSFET.

Fig. 3. (a) Type-N device made of 2 complementary MOSFETs ($V_{tO_1} = -6V$, $V_{tO_2} = +6V$).
(b) Type-N device made of 2 complementary JFETs (simulated by SPICE 2G with default values).
(c) Type-N device made of an N-channel JFET and a P-channel MOSFET ($V_{tO_1} = -2V$, $V_{tO_2} = +4V$).

Fig. 4. (a) Type-N device made of 2 complementary MOSFETs and 1 resistor ($R = 50$ kΩ, $V_{tO_1} = -6V$, $V_{tO_2} = +6V$).
(b) Type-N device made of 2 complementary JFETs and 1 resistor ($R = 100$ kΩ, JFETs simulated by SPICE 2G with default values).
(c) Type-N device made of a P-channel JFET and an N-channel MOSFET and 1 resistor ($R = 50$ kΩ, $V_{tO_1} = -6V$, JFET simulated by SPICE 2G with default values).

Fig. 5. Type-N devices made of 2 complementary MOSFETs and 2 resistors:
(a) $R_1 = 200$ kΩ, $R_2 = 200$ kΩ, $V_{tO_1} = -6V$, $V_{tO_2} = +6V$
(b) $R_1 = 300$ kΩ, $R_2 = 75$ kΩ, $V_{tO_1} = -4V$, $V_{tO_2} = +4V$
(c) $R_1 = 1$ kΩ, $R_2 = 5$ kΩ, $V_{tO_1} = -4V$, $V_{tO_2} = +4V$

Fig. 6. Type-N devices made of 2 complementary JFETs and 2 resistors:
(a) $R_1 = 100$ kΩ, $R_2 = 100$ kΩ; (b) $R_1 = 1$ kΩ, $R_2 = 20$ kΩ; (c) $R_1 = 1$ kΩ, $R_2 = 100$ kΩ.
(JFETs simulated by SPICE 2G with default values).

Fig. 7. (a) Type-N device made of an npn transistors, a P-channel MOSFET, and 2 resistors: $R_1 = 100$ kΩ, $R_2 = 200$ kΩ, $V_{tO_2} = +2V$.

(b) Type-N device made of an npn transistor, a P-channel JFET, and 2 resistors: $R_1 = 25$ kΩ, $R_2 = 100$ kΩ, (JFET simulated by SPICE 2G with default values).

(c) Type-N device made of a pnp transistor, an N-channel JFET, and 2 resistors: $R_1 = 150$ kΩ, $R_2 = 6$ kΩ, $V_{tO_1} = -2V$.

Fig. 8. Type-N devices made of an N-channel MOSFET, a P-channel JFET and 2 resistors:

(a) $R_1 = 200$ kΩ, $R_2 = 200$ kΩ, $V_{tO_2} = +6V$

(b) $R_1 = 300$ kΩ, $R_2 = 50$ kΩ, $V_{tO_1} = -4V$

(c) $R_1 = 10$ kΩ, $R_2 = 5$ kΩ, $V_{tO_1} = -4V$

(JFETs simulated by SPICE 2G with default values).

Fig. 9. Two-transistor "cross-coupled" feedback structure.

Fig. 10. npn or pnp transistor replacement for T_1 or T_2 in Fig. 9. The "base" in this case is the starred terminal.

Fig. 11. N-Channel or P-channel replacement for T_1 or T_2 in Fig. 9. The "gate" in this case is the starred terminal.

Fig. 12. N-channel or P-channel replacement for T_1 or T_2 in Fig. 10. The "gate" in this case is the starred terminal.

Fig. 13. Three <u>distinct</u> ways of driving the feedback structure in Fig. 9 with a <u>current source</u> I_s via a <u>soldering-iron entry</u>.

Fig. 14. Seven distinct ways of connecting one resistor to the circuit in Fig. 13(a) by either a plier-type or a soldering-iron entry.

Fig. 15. Type-S device made of 2 complementary bipolar transistors and 1 resistor ($R = 5$ kΩ).

Fig. 16. Type-S devices made of 2 complementary bipolar transistors and 2 resistors:

(a) $R_1 = 500$ Ω, $R_2 = 10$ kΩ ; (b) $R_1 = 400$ Ω, $R_2 = 2$kΩ.

Fig. 17. (a) Type-S device made of an npn transistor, an N-channel MOSFET and 2 resistors ($R_1 = 600$ kΩ, $R_2 = 10$ kΩ, $V_{tO_1} = -5V$).

(b) Type-S device made of a pnp transistor, a P-channel MOSFET and 2 resistors ($R_1 = 3.4$ kΩ, $R_2 = 300$ kΩ, $V_{tO_2} = -4V$).

(c) Type-S device made of an npn transistor, a P-channel MOSFET and 2 resistors ($R_1 = 100$ kΩ, $R_2 = 500$ kΩ, $V_{t0_1} = -1V$).

Fig. 18. (a) Type-S device made of 2 complementary MOSFETs and 2 resistors ($R_1 = 200$ kΩ, $R_2 = 5$ kΩ, $V_{t0_1} = -5V$, $V_{t0_2} = +1V$).

(b) Type-S device made of an npn transistor, an N-channel JFET and 2 resistors ($R_1 = 50$ kΩ, $R_2 = 2$kΩ, $V_{t0_1} = -5V$).

(c) Type-S device made of an N-channel MOSFET, an N-channel JFET and 2 resistors ($R_1 = 100$ kΩ, $R_2 = 10$ kΩ, $V_{t0_1} = -5V$, $V_{t0_2} = +1V$).

Fig. 19. Three distinct ways of driving the feedback structure in Fig. 9 with a voltage source V_s via a plier-type entry.

Fig. 20. Seven distinct ways of connecting one resistor to the circuit in Fig. 19(c) by either a plier-type, or a soldering-iron entry.

Fig. 21. (a) Current-driven one-port N_I containing 2 transistors and linear positive resistors.

(b) Simplified one-port $\hat{N}_I$ obtained by open-circuiting the current source, and by replacing each resistor by either a short-circuit, or an open circuit.

Fig. 22. (a) Voltage-driven one-port N_V containing 2 transistors and linear positive resistors.

(b) Simplified one-port $\hat{N}_V$ obtained by short-circuiting the voltage source, and by replacing each resistor by either a short-circuit, or an open-circuit.

Fig. 23. (a) Connecting a resistor in series with N'.

(b) v-i characteristics of N and N' for (a).

(c) Connecting a resistor in parallel with N'.

(d) v-i characteristics fo N and N' for (b).

Fig. 24. (a) Connecting a resistor in series with N'.

(b) v-i characteristics of N and N' for (a).

(c) Connecting a resistor in parallel with N'.

(d) v-i characteristics of N and N' for (b).

Fig. A-1. v-i characteristics of the last circuit (column 1) in the MOSFET family in Table 1: $V_{tO_1} = -4V$, $V_{tO_2} = +4V$

vertical scale: 0.01 mA per division
horizontal scale: 3V per division

Fig. A-2. v-i characteristics of the last circuit in the JFET family (column 2) in Table 1: JFETs simulated by SPICE 2G with default values

vertical scale: 0.01 mA per division
horizontal scale: 3V per division

Fig. A-3. v-i characteristics of the last circuit in the bipolar transistor MOSFET family in Table 1: $V_{tO1} = -4V$

vertical scale: 0.015 mA per division
horizontal scale: 1.5V per division

Fig. A-4. v-i characteristics of the last circuit in the bipolar transistor -JFET family in Table 1: JFET simulated by SPICE 2G with default values

vertical scale: 0.01 mA per division
horizontal scale: 1V per division

Fig. A-5. v-i characteristics of the last circuit in the JFET-MOSFET family in Table 1: $V_{tO_1} = -4V$, JFET simulated by SPICE 2G with default values

vertical scale: 0.015 mA per division
horizontal scale: 3V per division

Fig. A-6. v-i characteristics of the last circuit in the MOSFET family in Table 2: $V_{tO_1} = V_{tO_2} = +2V$

vertical scale: 0.08 mA per division
horizontal scale: 3V per division

Fig. A-7. v-i characteristics of the last circuit in the bipolar transistor MOSFET family in Table 2: $V_{tO_2} = +2V$

vertical scale: 0.2 mA per division
horizontal scale: 2V per division

Fig. A-8. v-i characteristics of the last circuit in the MOSFET family in Table 3: $V_{t0_1} = -5V$, $V_{t0_2} = +1V$
vertical scale: 0.1 mA per division
horizontal scale: 6V per division

Fig. A-9. v-i characteristics of the last circuit in the bipolar transistor-MOSFET family in Table 3: $V_{t0_1} = -5V$
vertical scale: 0.05 mA per division
horizontal scale: 4V per divison

Fig. A-10. v-i characteristics of the last circuit in the bipolar transistor-JFET family in Table 3: $V_{t0_1} = -5V$
vertical scale: 0.3 mA per division
horizontal scale: 3V per division

Fig. A-11. v-i characteristics of the last circuit in the JFET-MOSFET family in Table 3: $V_{t0_1} = -5V$, $V_{t0_2} = +1V$
vertical scale: 0.1 mA per division
horizontal scale: 6V per division

Fig. A-12. v-i characteristics of the last circuit in the MOSFET family in Table 4: $V_{t0_1} = -1V$, $V_{t0_2} = +1V$
vertical scale: 3 μA per division
horizontal scale: 1V per division

Fig. A-13. v-i characteristics of the last circuit in the bipolar transistor-MOSFET family in Table 4: $V_{t0_1} = -1V$
vertical scale: 3 μA per division
horizontal scale: 1V per division

Fig. A-14. v-i characteristics of the circuits in the bipolar transistor-JFET family in Table 4: JFET simulated by SPCIE 2G with default values
(a) first circuit:
vertical scale: 0.4 mA per division
horizontal scale: 1V per division
(b) second circuit:
vertical scale: 0.48 mA per division
horizontal scale: 2V per division
(c) last circuit:
vertical scale: 0.48 mA per division
horizontal scale: 4V per division

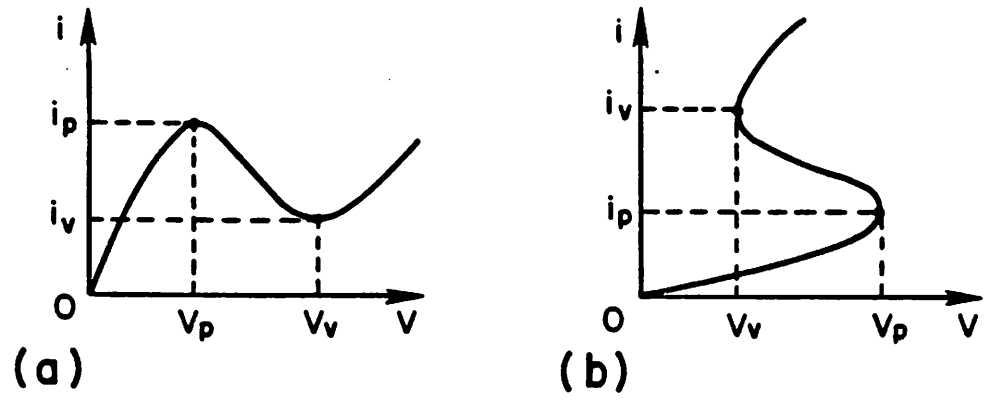


Fig. 1

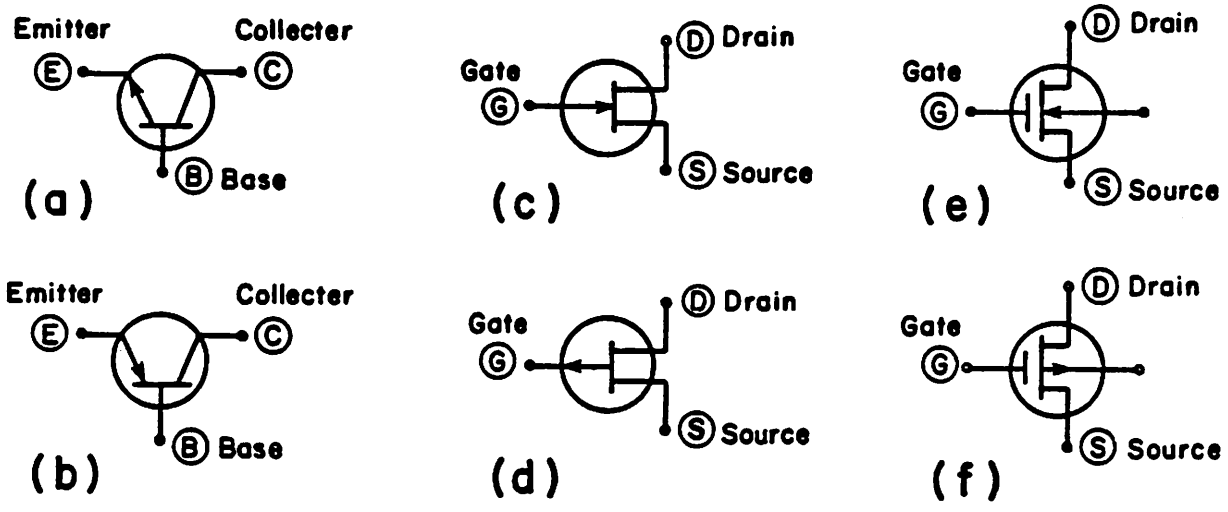


Fig. 2

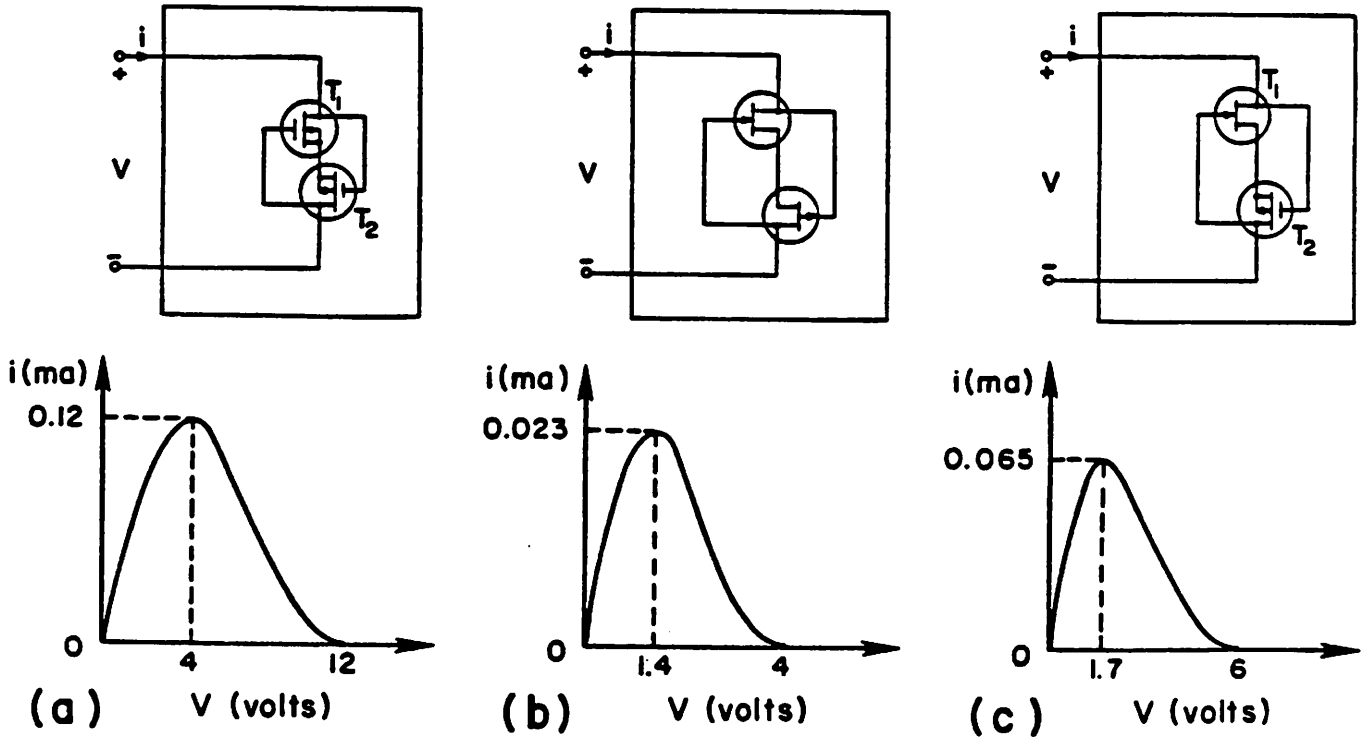


Fig. 3

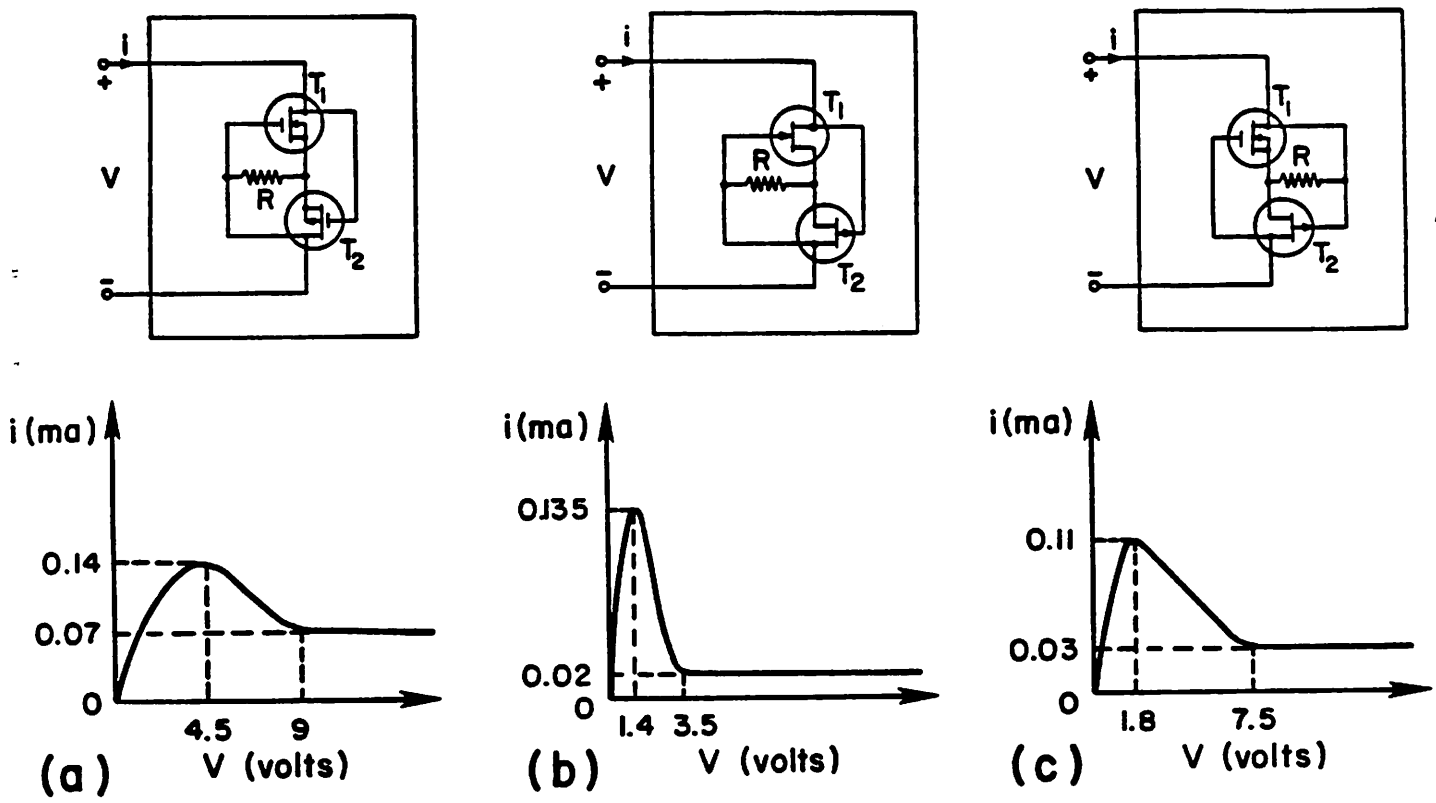

i
+
V
−
T1
R
T2
i(ma)
0.14
0.07
0
4.5
9
V (volts)
(a)
0135
0.02
1.4
3.5
(b)
0.11
0.03
1.8
7.5
(c)

Fig. 4

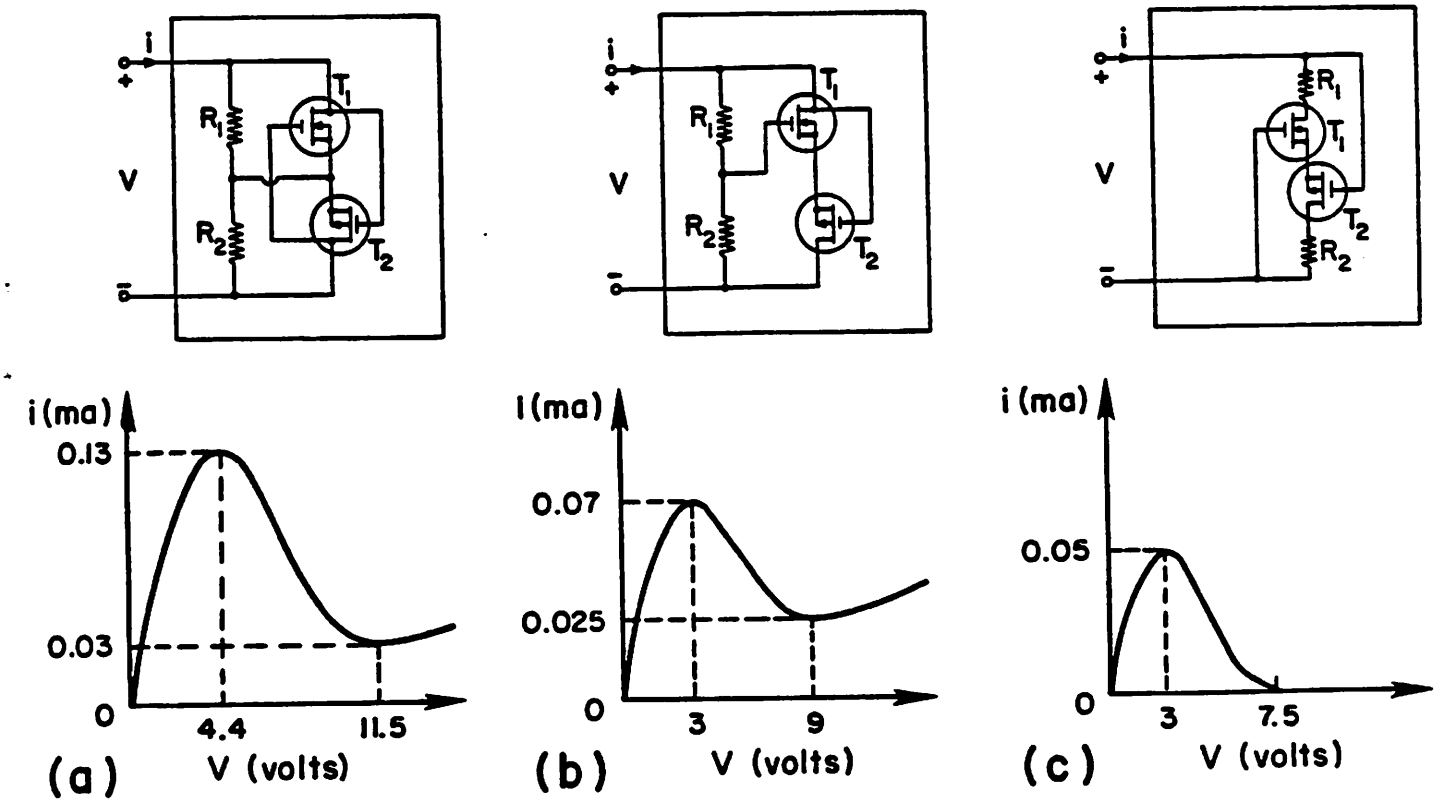

i
+
V
−
T1
T2
R1
R2
i(ma)
0.13
0.03
0
4.4
11.5
V (volts)
(a)
I(ma)
0.07
0.025
3
9
(b)
0.05
7.5
(c)

Fig. 5

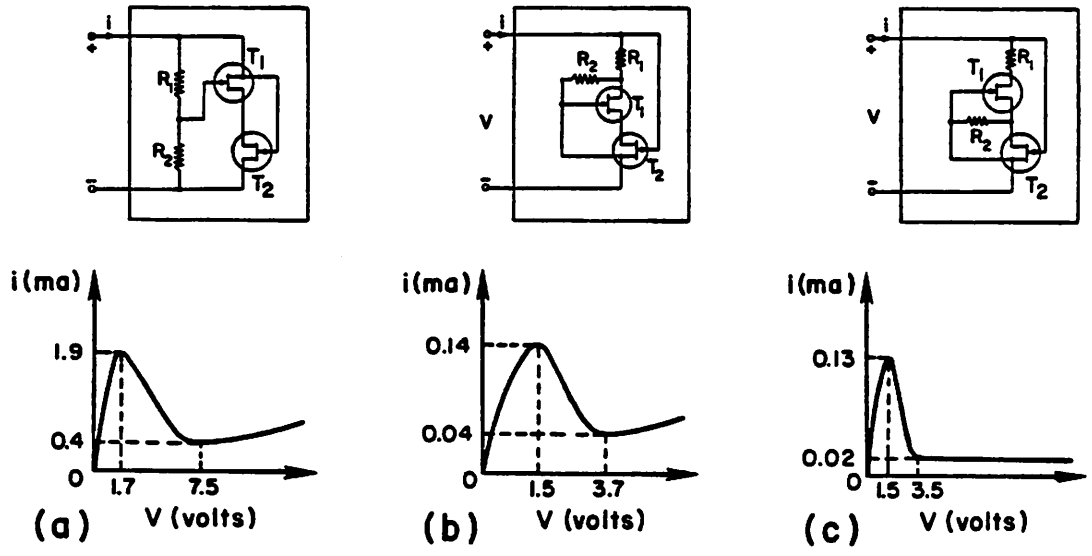


Fig. 6

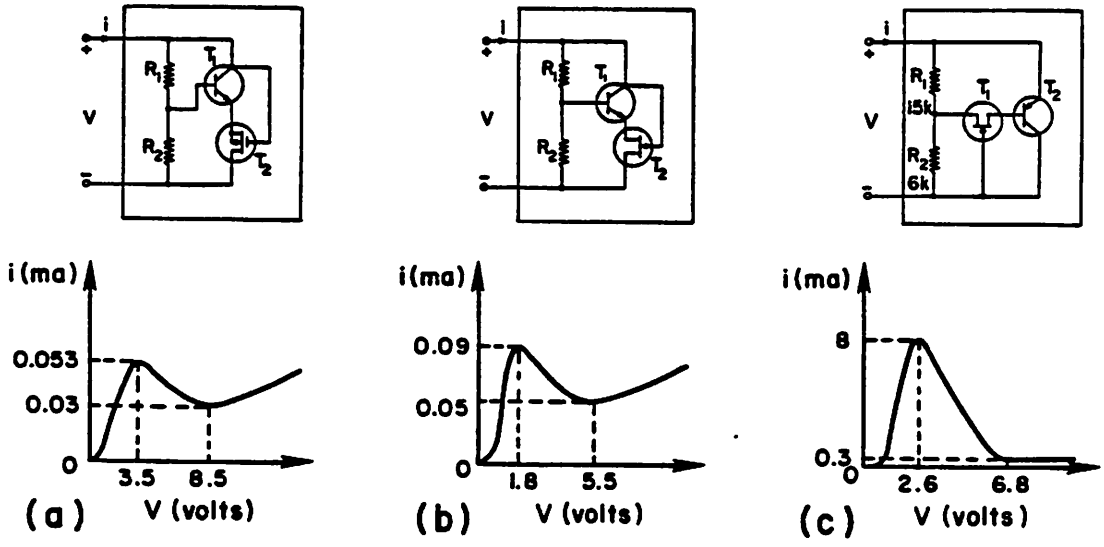


Fig. 7

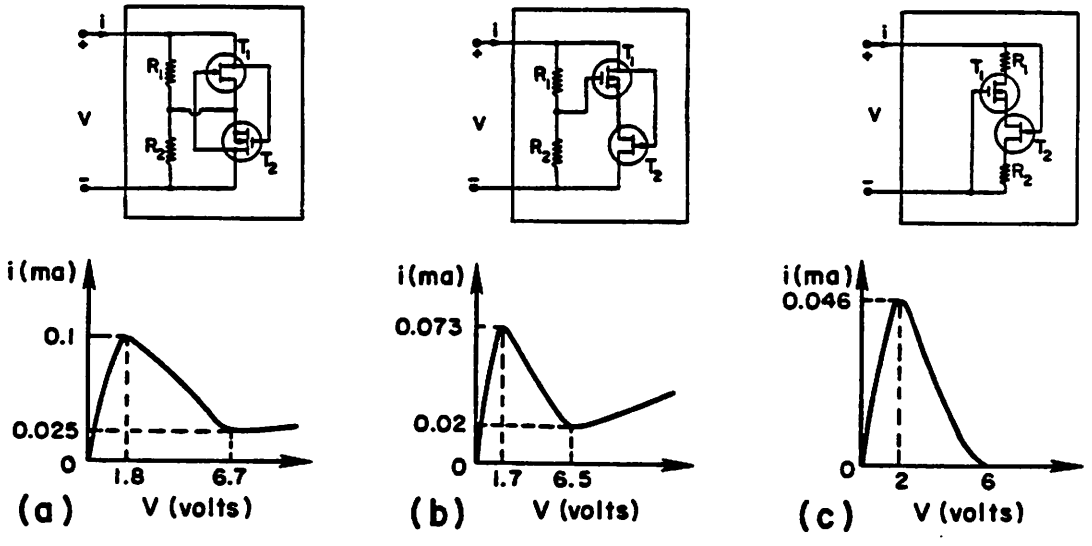


Fig. 8

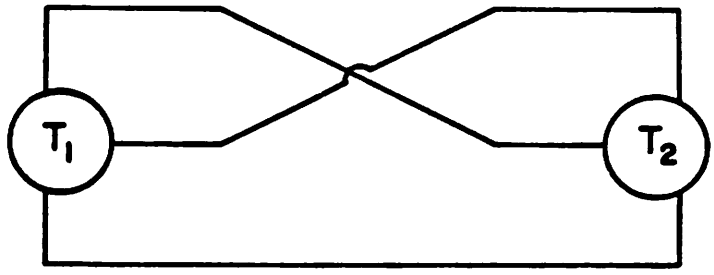


Fig. 9

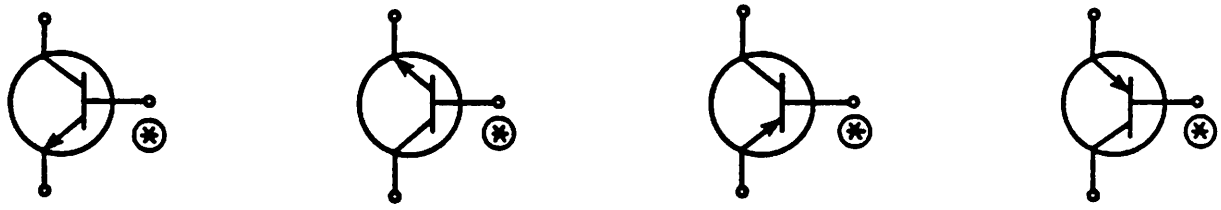


Fig. 10

Fig. 11

Fig. 12

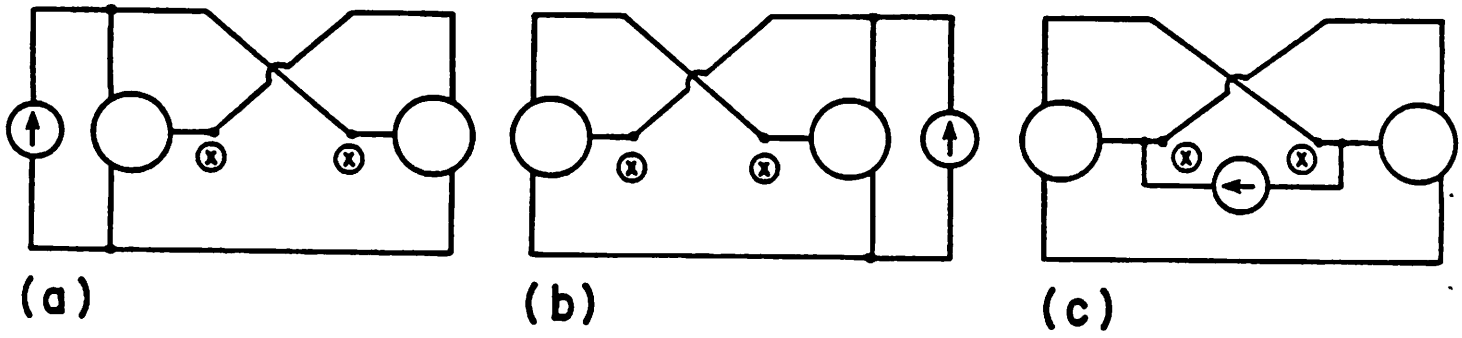


Fig. 13

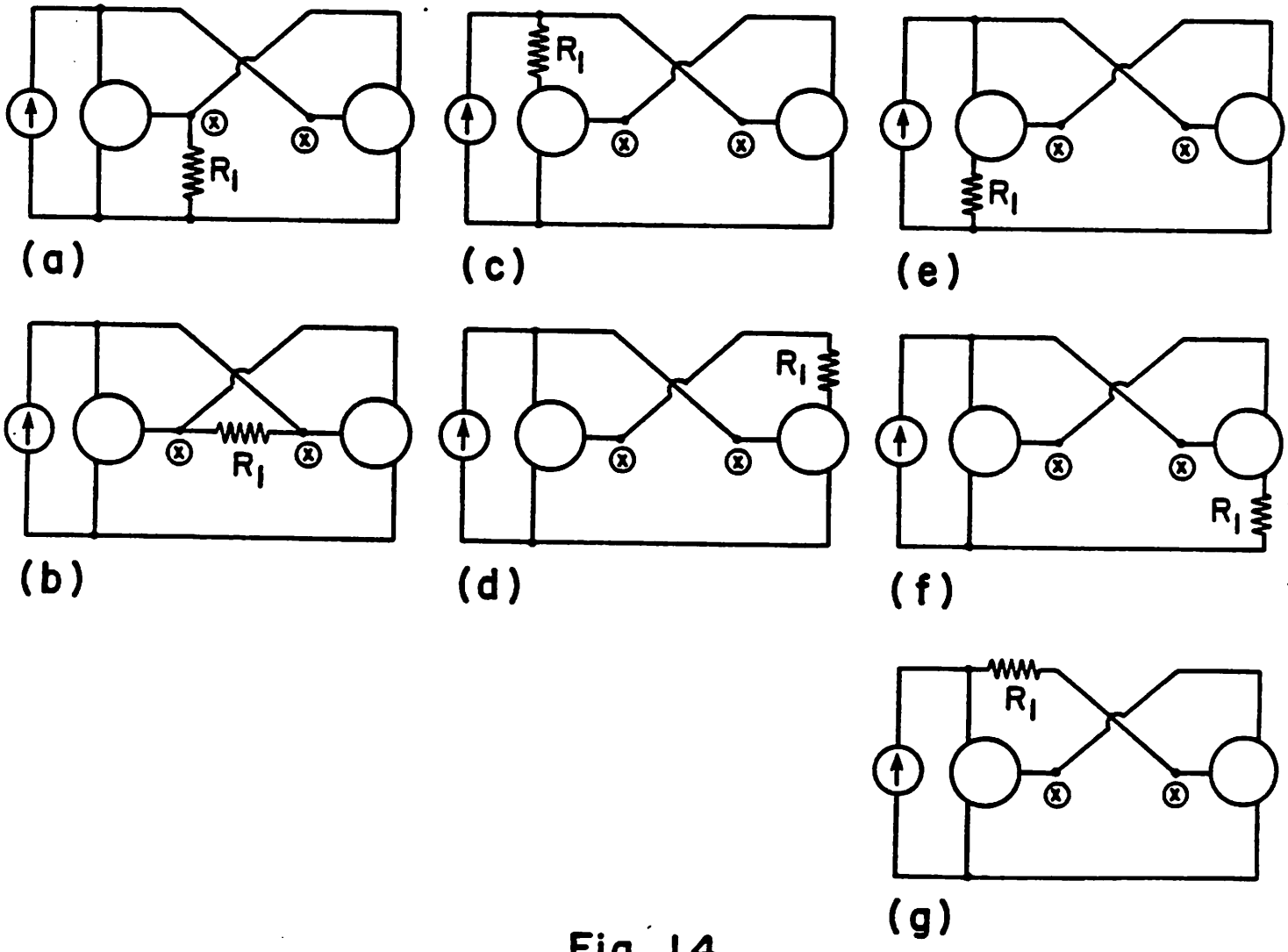


Fig. 14

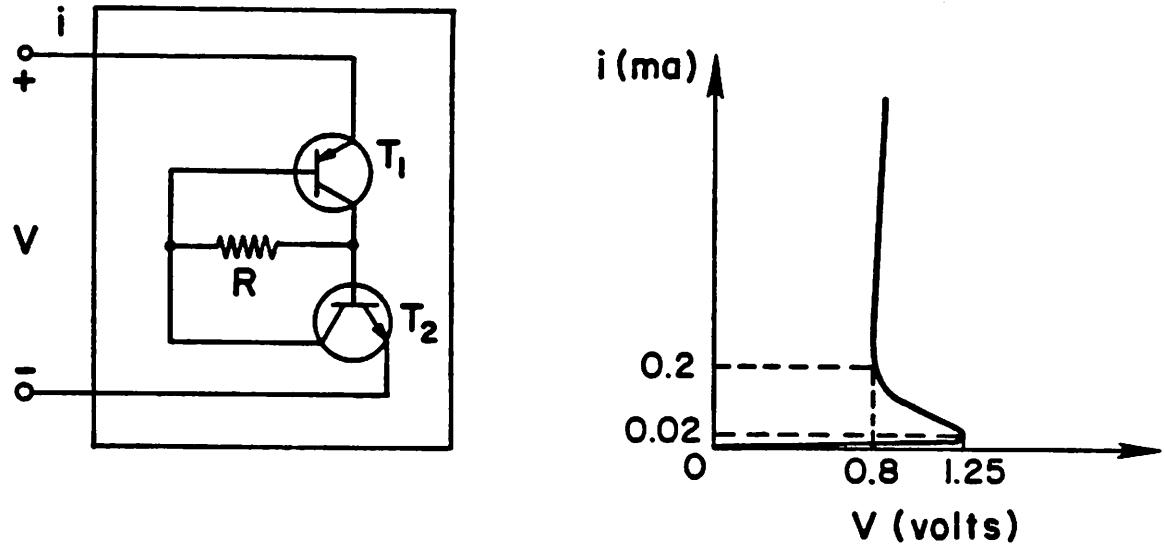

i
+
V
−
T1
R
T2
i (ma)
0.2
0.02
0
0.8
1.25
V (volts)

Fig. 15

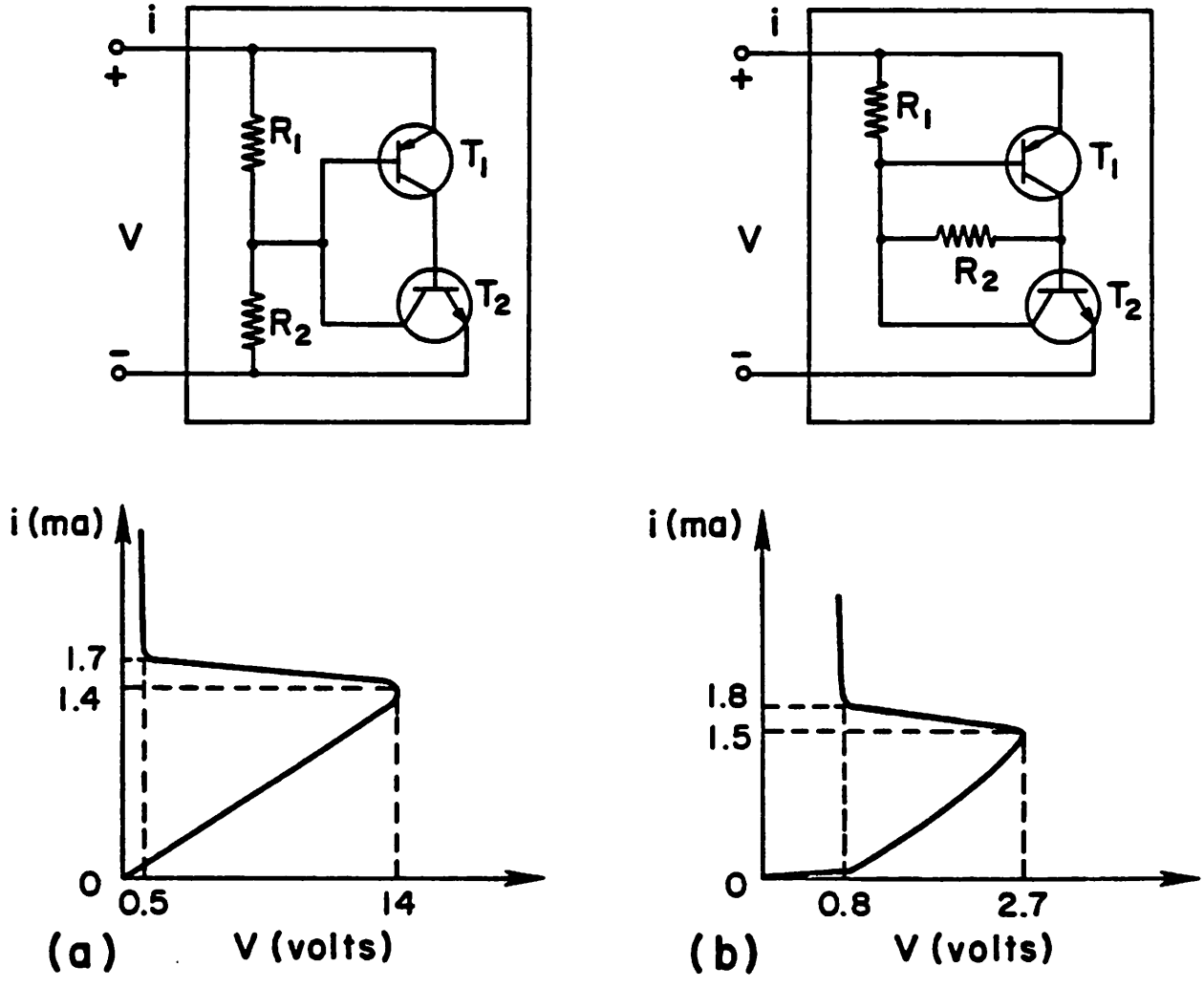

i
+
V
−
R1
T1
R2
T2
i (ma)
1.7
1.4
0
0.5
14
(a)
V (volts)
i (ma)
1.8
1.5
0
0.8
2.7
(b)
V (volts)

Fig. 16

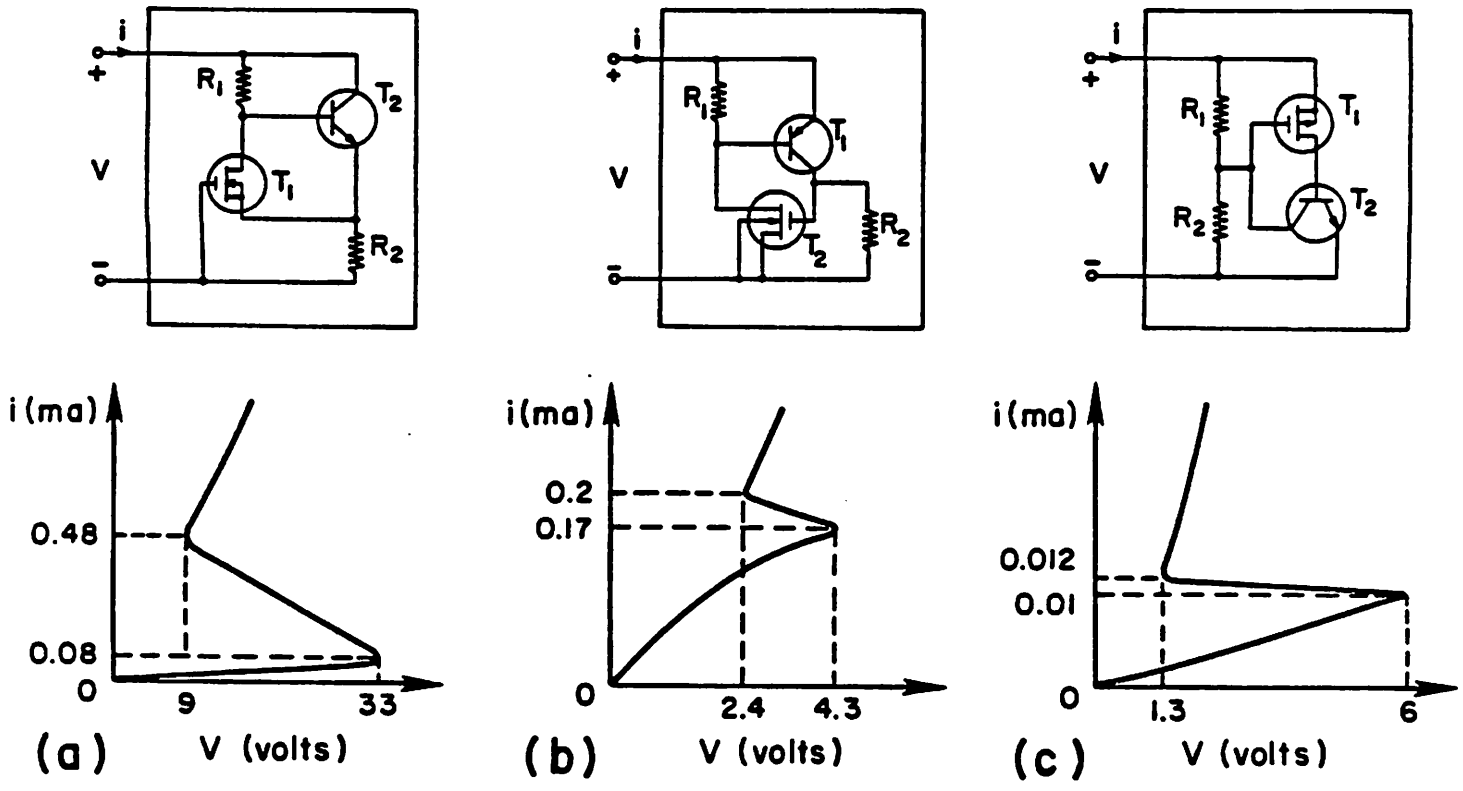

i
+
V
−
R1
T2
T1
R2
i(ma)
0.48
0.08
0
9
33
V (volts)
(a)
T1
R2
0.2
0.17
2.4
4.3
(b)
R1
T2
0.012
0.01
1.3
6
(c)

Fig. 17

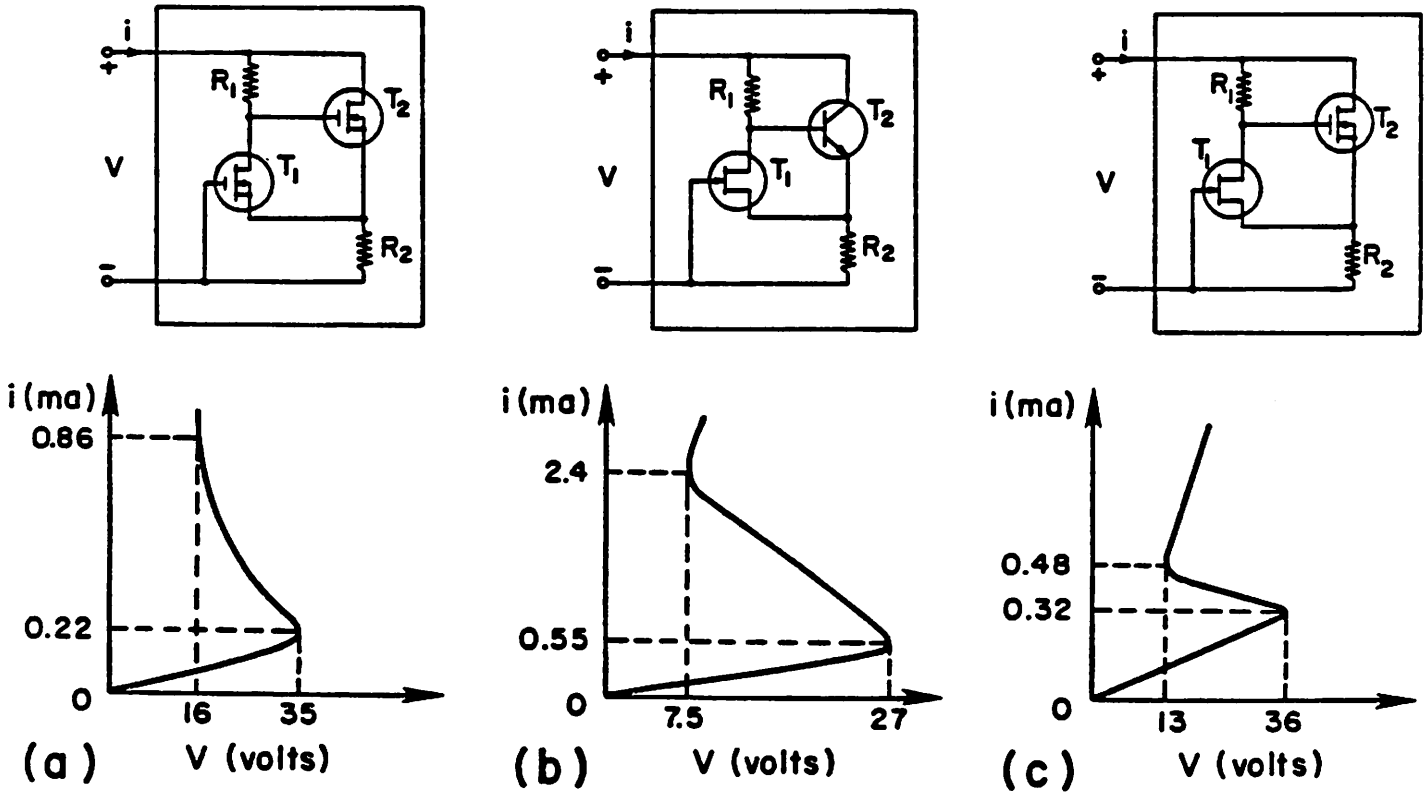

i
+
V
−
R1
T2
T1
R2
i(ma)
0.86
0.22
0
16
35
V (volts)
(a)
2.4
0.55
7.5
27
(b)
0.48
0.32
13
36
(c)

Fig. 18

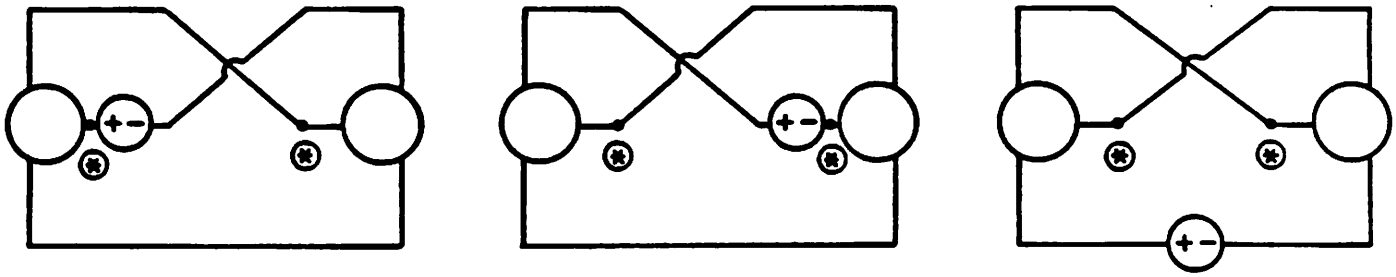


Fig. 19

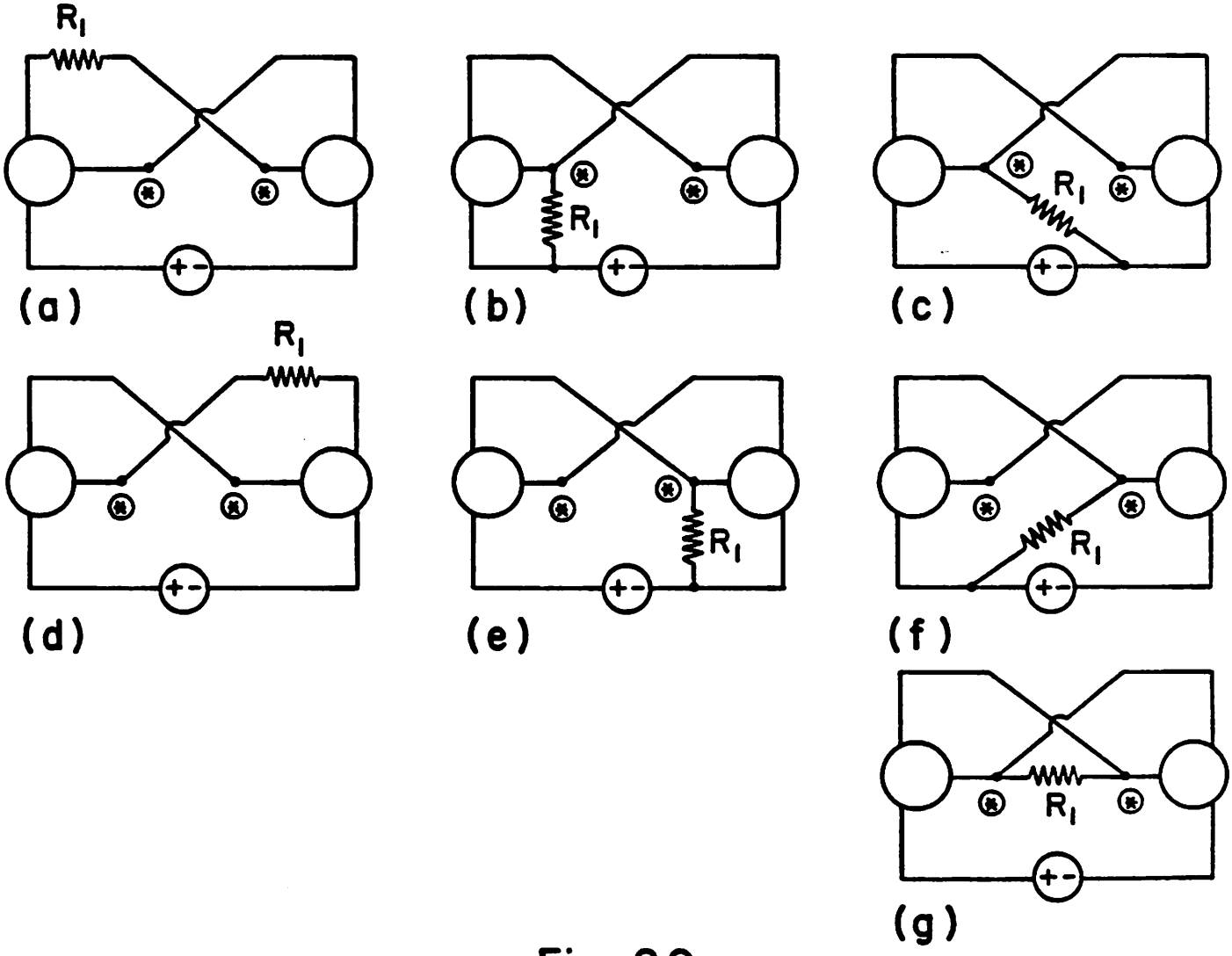


Fig. 20

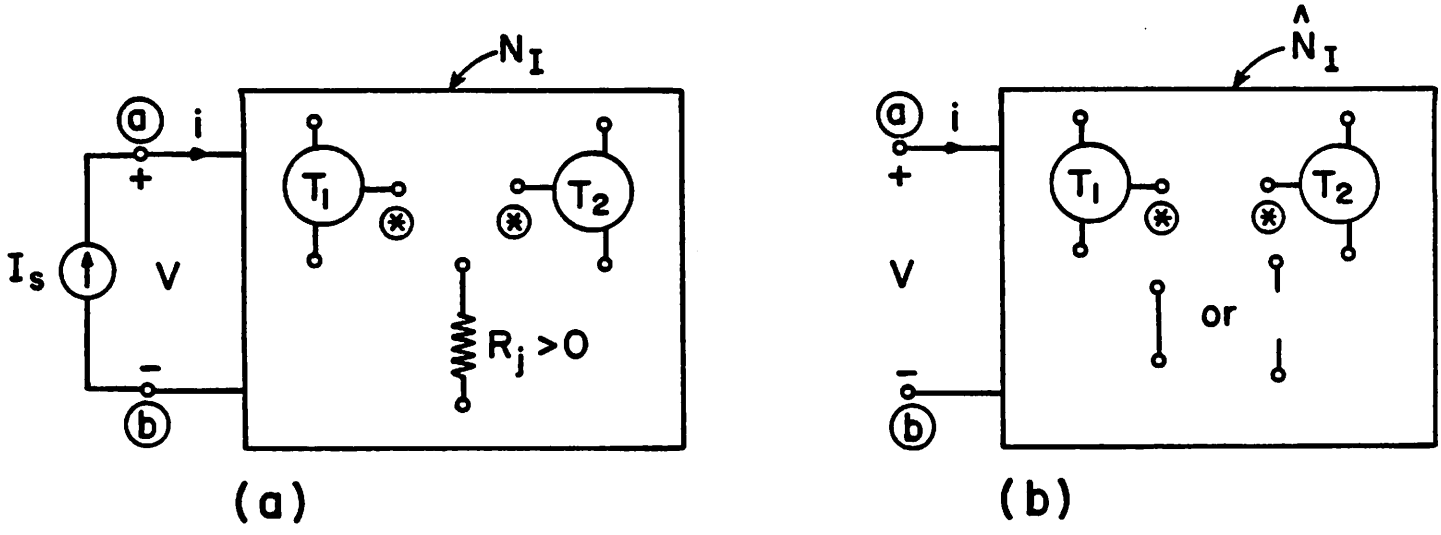

N_I
a
i
+
I_s
V
−
b
T_1
T_2
$R_j > 0$
(a)
$\hat{N}_I$
a
i
+
V
−
b
T_1
T_2
or
(b)

Fig. 21

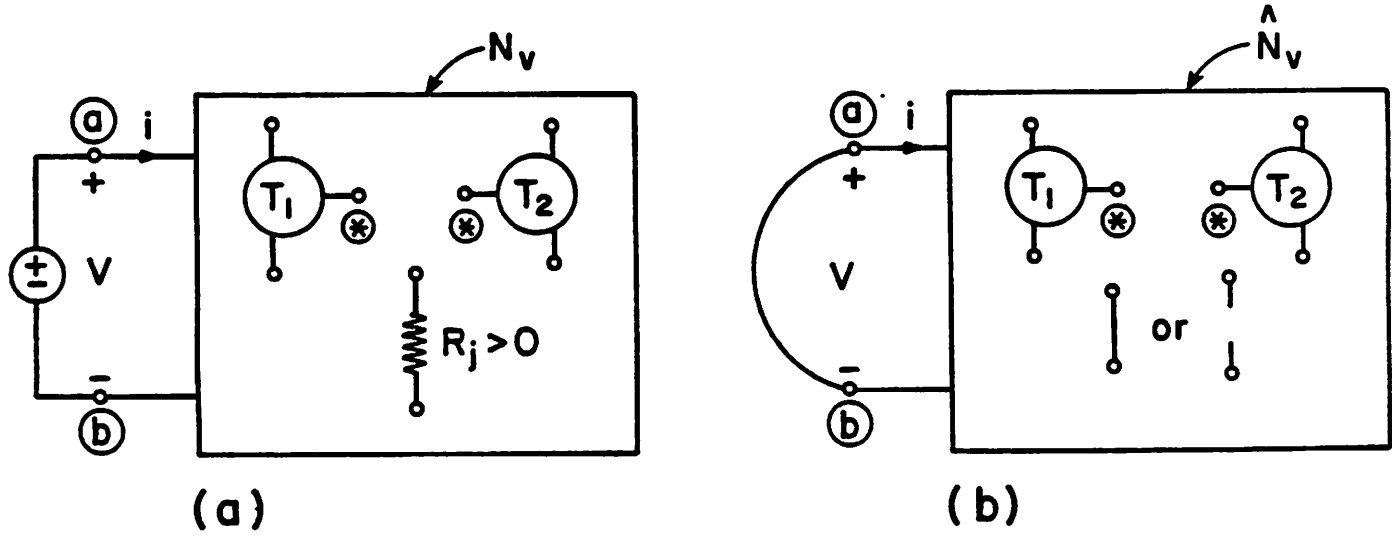

N_V
a
i
+
V
−
b
T_1
T_2
$R_j > 0$
(a)
$\hat{N}_V$
a
i
+
V
−
b
T_1
T_2
or
(b)

Fig. 22

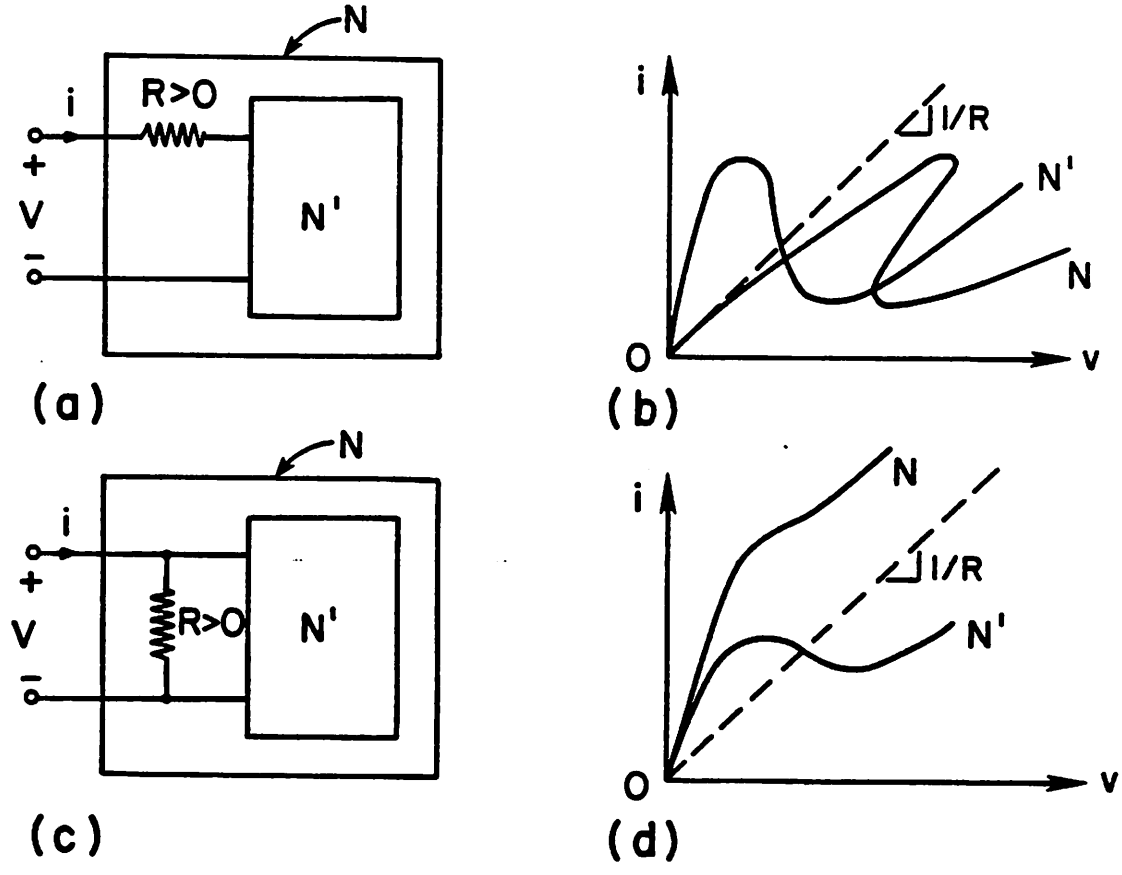

N
i
R>O
+
V
−
N'
(a)
i
I/R
N'
N
O
v
(b)
N
i
+
V
−
R>O
N'
(c)
i
N
I/R
N'
O
v
(d)

Fig. 23

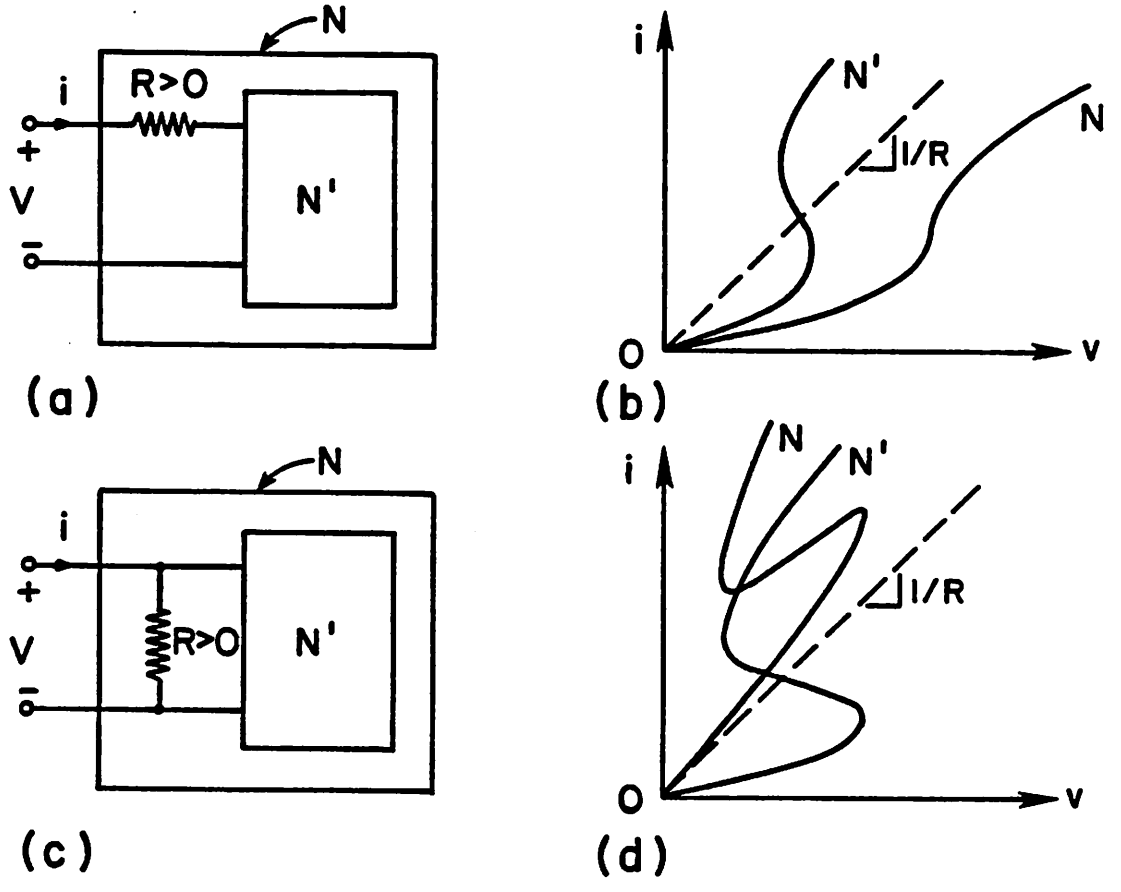

N
i
R>O
+
V
−
N'
(a)
i
N'
I/R
N
O
v
(b)
N
i
+
V
−
R>O
N'
(c)
i
N
N'
I/R
O
v
(d)

Fig. 24

I

APPENDIX A. SELECTED CATALOG OF TYPE-N DEVICES

Table I

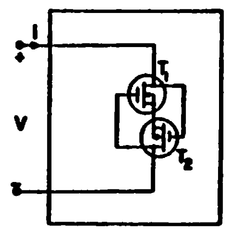
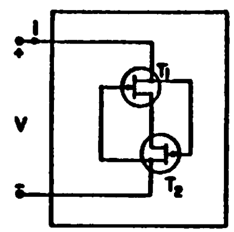
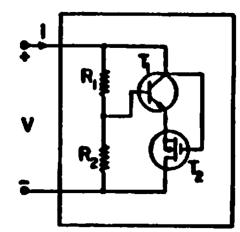
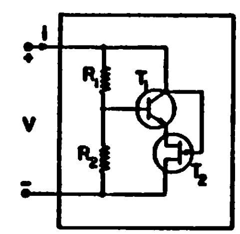
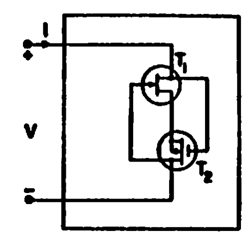
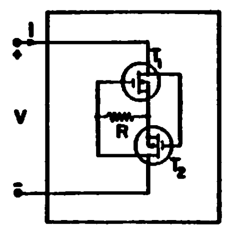
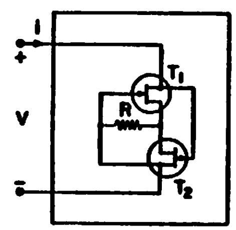
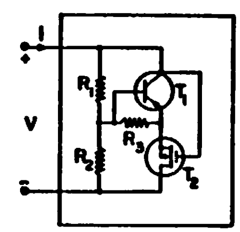
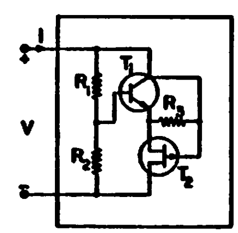
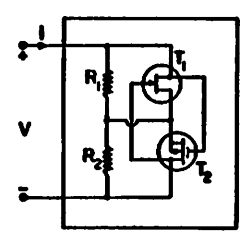
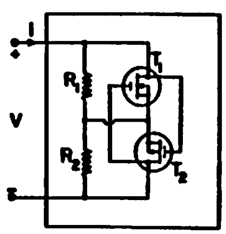
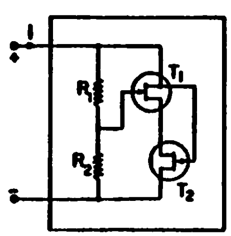
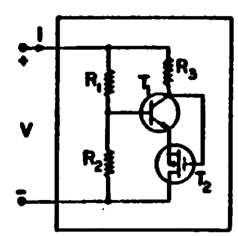
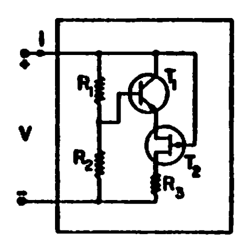
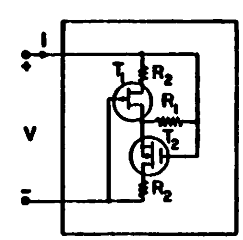
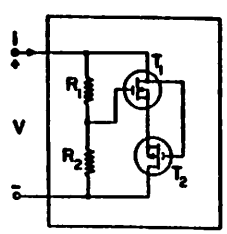
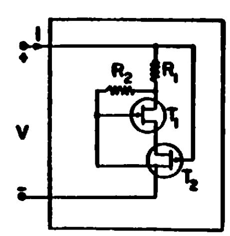
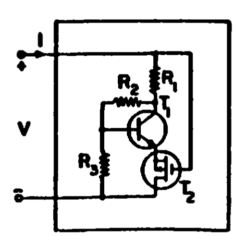
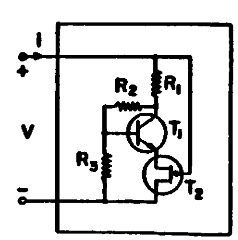
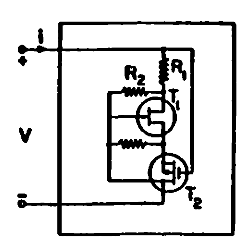
Voltage-Controlled NDR Devices (Complementary Case)				
MOSFET Family	JFET Family	Bipolar Transistor - MOSFET Family	Bipolar Transistor - JFET Family	JFET-MOSFET Family
				
				
				
				

Table I (continuation)

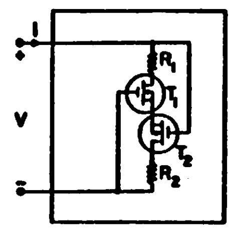
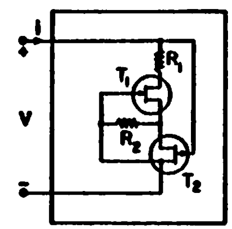
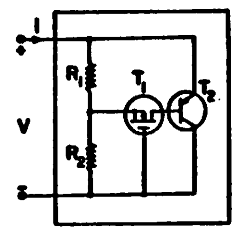
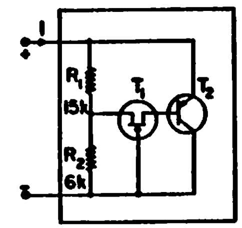
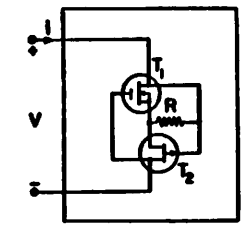
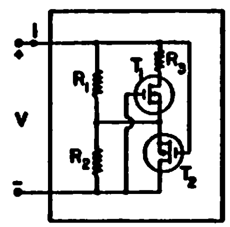
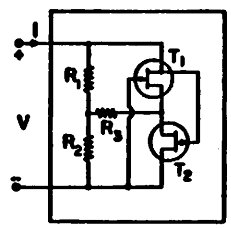
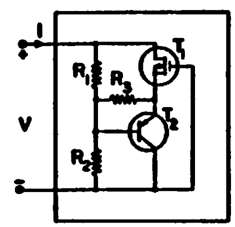
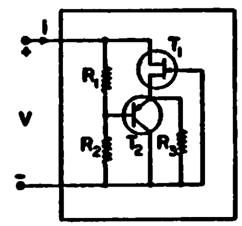
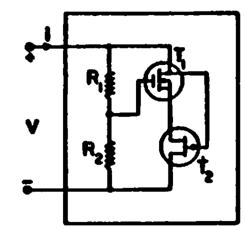
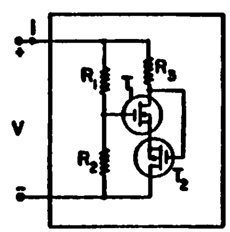
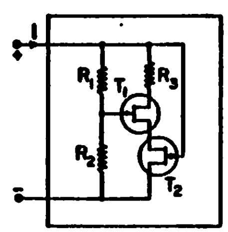
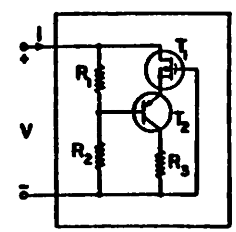
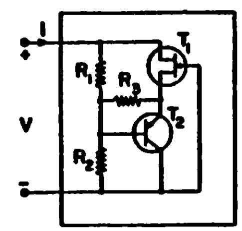
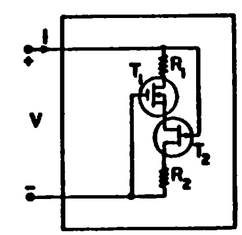
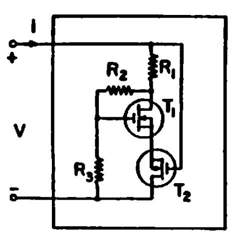
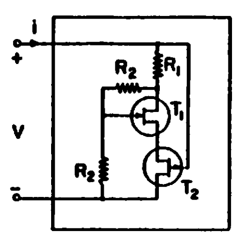
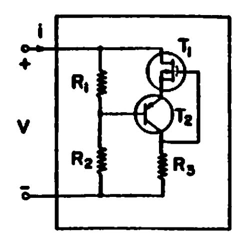
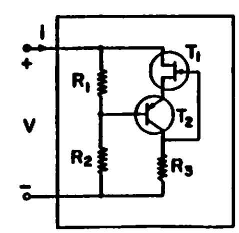
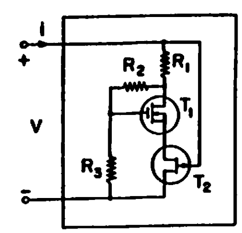
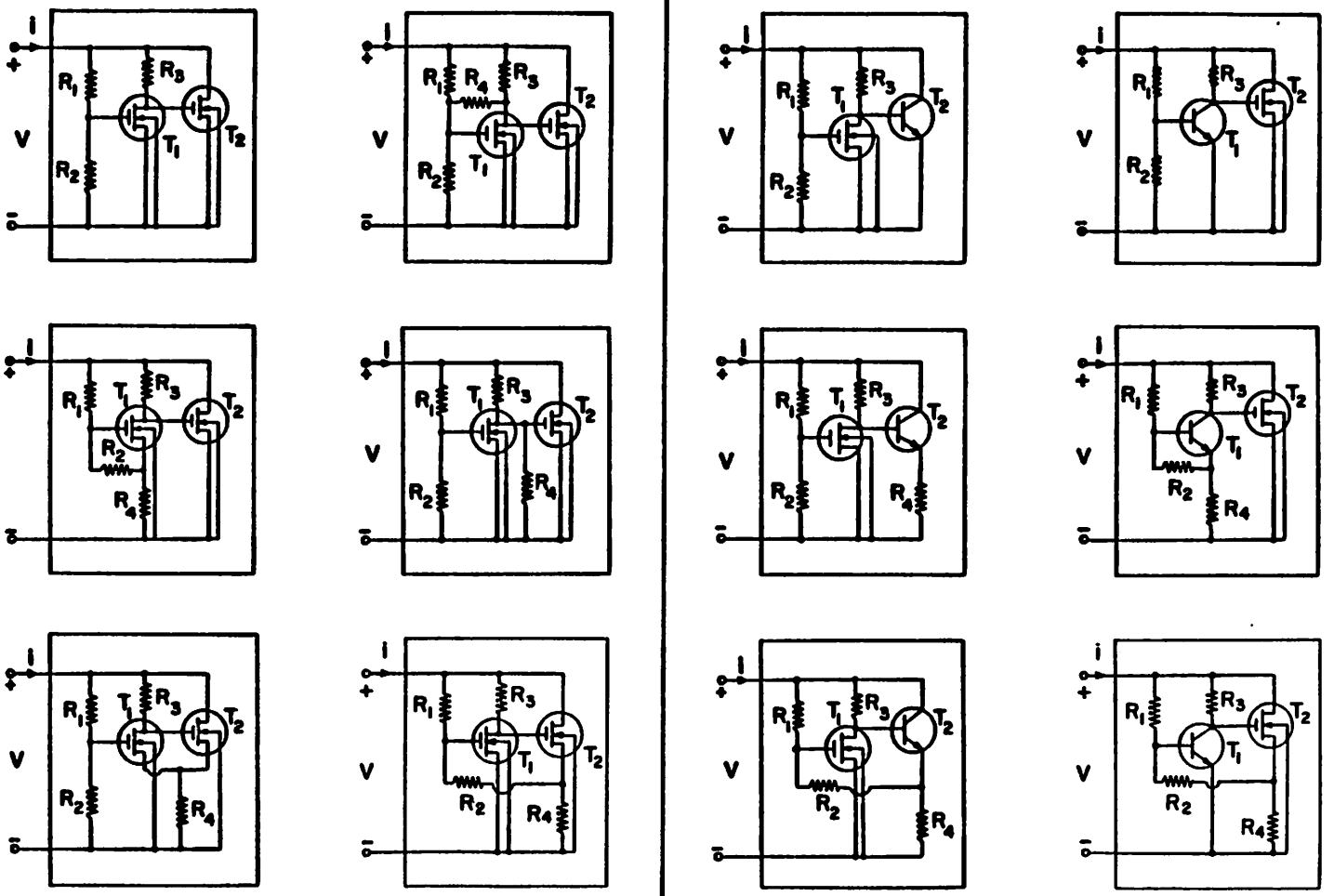
MOSFET Family	JFET Family	Bipolar Transistor-MOSFET Family	Bipolar Transistor-JFET Family	JFET-MOSFET Family
				
				
				
				

Table 2

Voltage-Controlled NDR Devices (Pure Configuration)

MOSFET Family	Bipolar Transistor-MOSFET Family



APPENDIX B. SELECTED CATALOG OF TYPE-S DEVICES

Table 3

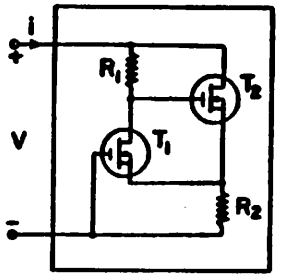
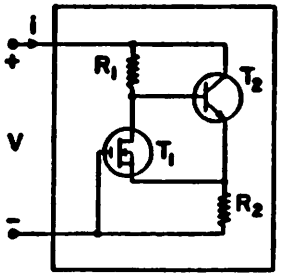
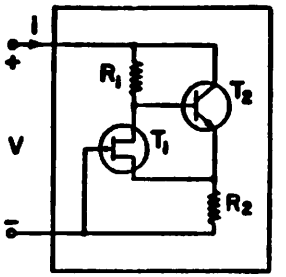
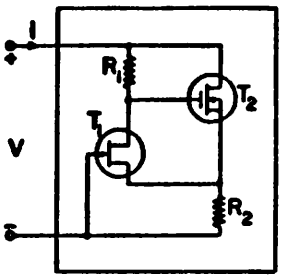
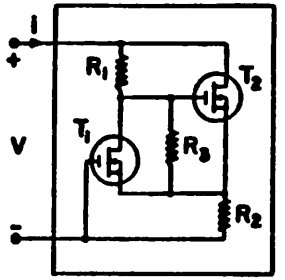
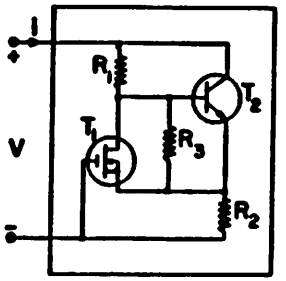
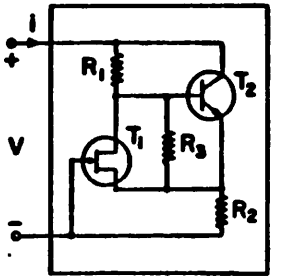
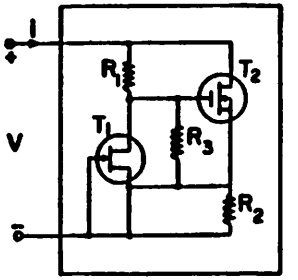
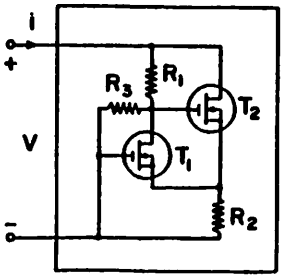
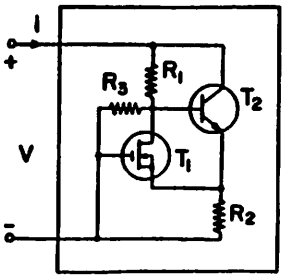
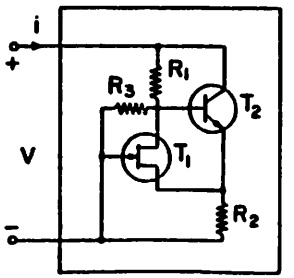
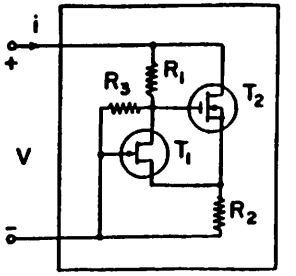
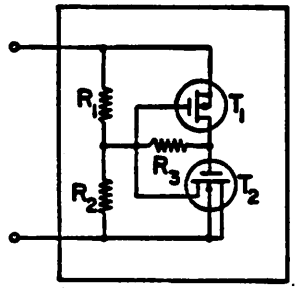
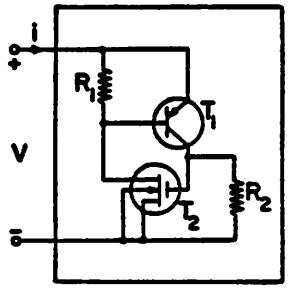
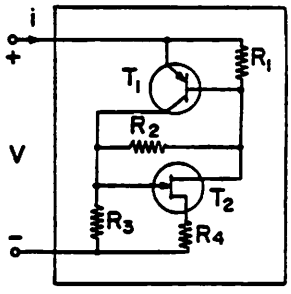
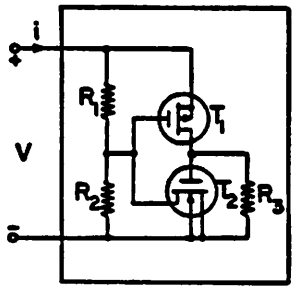
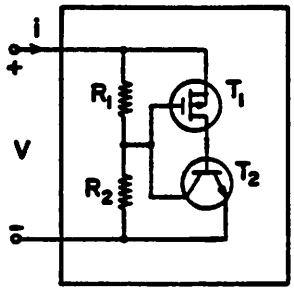
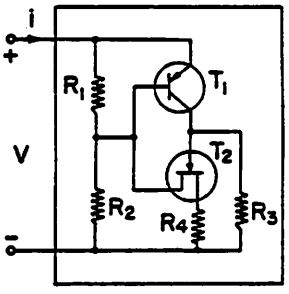
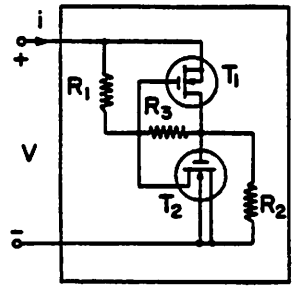
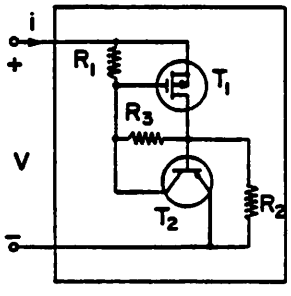
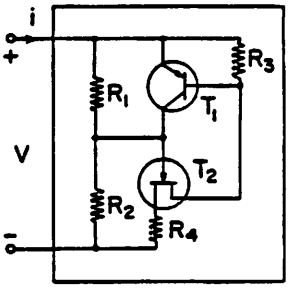
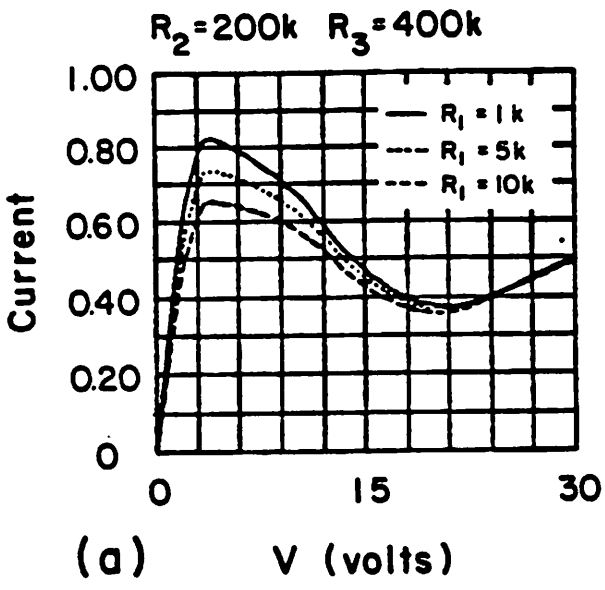
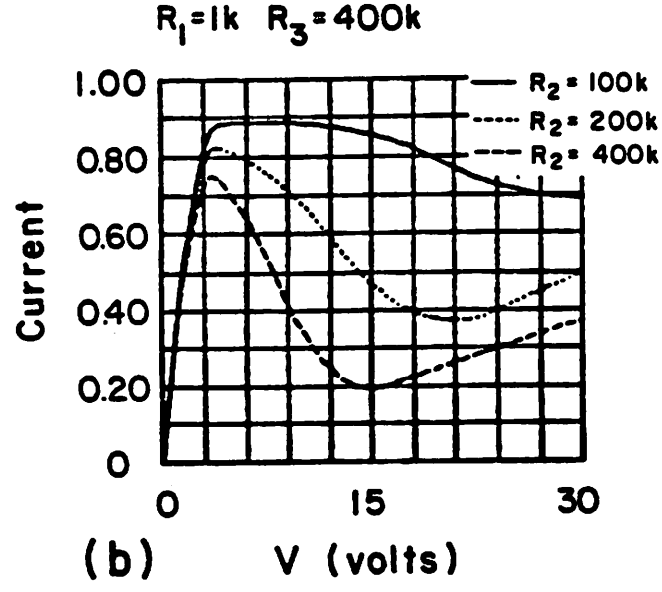
Current-Controlled NDR Devices (Pure Configuration)			
MOSFET Family	Bipolar Transistor-MOSFET Family	Bipolar Transistor-JFET Family	JFET-MOSFET Family
			
			
			

Table 4

Current-Controlled NDR Devices (Complementary Case)		
MOSFET Family	Bipolar Transistor-MOSFET Family	Bipolar Transistor-JFET Family
		
		
		


R_2=200k R_3=400k
1.00
0.80
0.60
0.40
0.20
0
Current
R_1 = 1k
R_1 = 5k
R_1 = 10k
0
15
30
(a)
V (volts)


R_1=1k R_3=400k
1.00
0.80
0.60
0.40
0.20
0
Current
R_2 = 100k
R_2 = 200k
R_2 = 400k
0
15
30
(b)
V (volts)

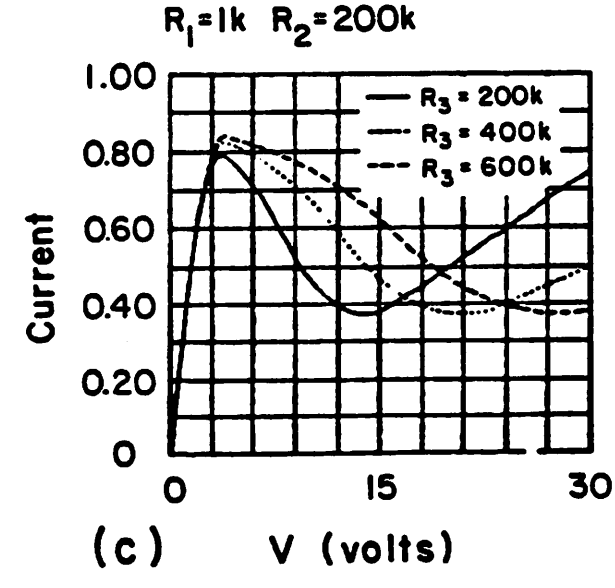
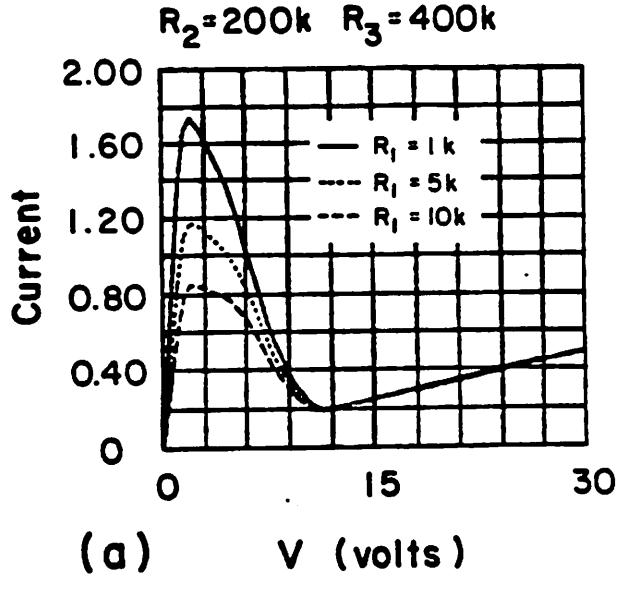
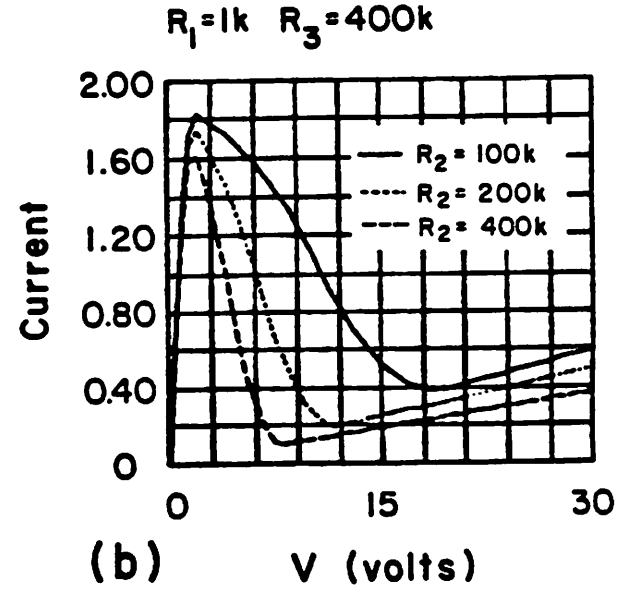

R_1=1k R_2=200k
1.00
0.80
0.60
0.40
0.20
0
Current
R_3 = 200k
R_3 = 400k
R_3 = 600k
0
15
30
(c)
V (volts)

Fig. A-1


R_2=200k R_3=400k
2.00
1.60
1.20
0.80
0.40
0
Current
R_1 = 1k
R_1 = 5k
R_1 = 10k
0
15
30
(a)
V (volts)


R_1=1k R_3=400k
2.00
1.60
1.20
0.80
0.40
0
Current
R_2 = 100k
R_2 = 200k
R_2 = 400k
0
15
30
(b)
V (volts)

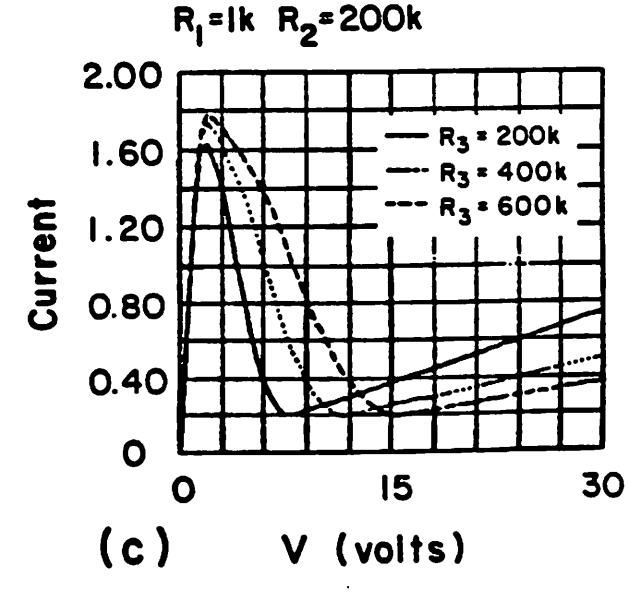
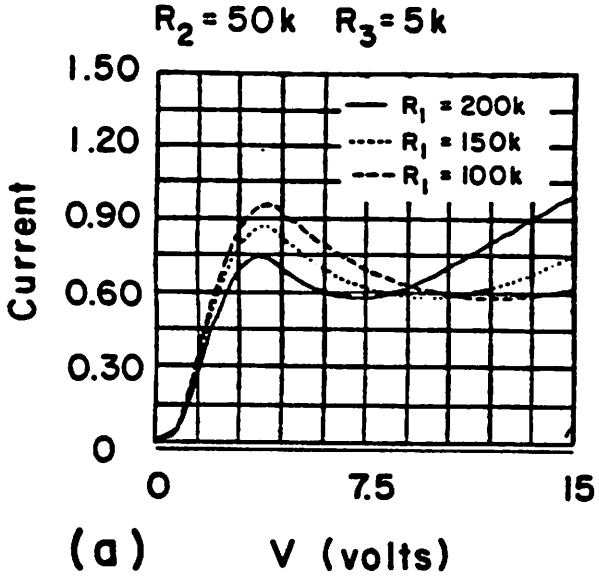
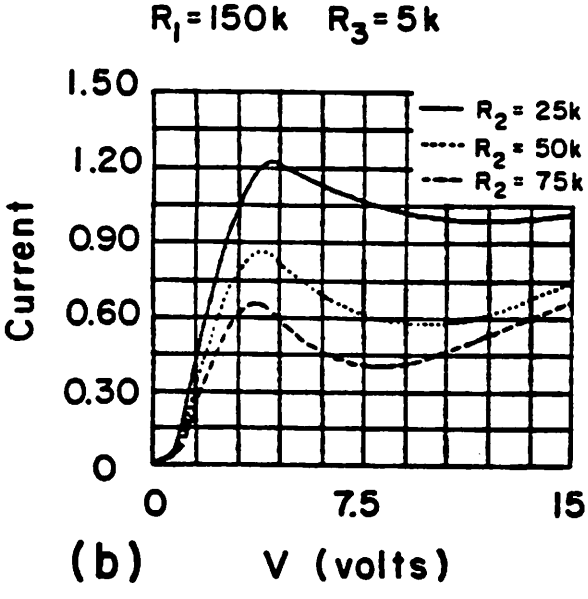

R_1=1k R_2=200k
2.00
1.60
1.20
0.80
0.40
0
Current
R_3 = 200k
R_3 = 400k
R_3 = 600k
0
15
30
(c)
V (volts)

Fig. A-2


$R_2 = 50k \quad R_3 = 5k$
1.50
1.20
0.90
0.60
0.30
0
Current
$R_1 = 200k$
$R_1 = 150k$
$R_1 = 100k$
0
7.5
15
(a)
V (volts)


$R_1 = 150k \quad R_3 = 5k$
1.50
1.20
0.90
0.60
0.30
0
Current
$R_2 = 25k$
$R_2 = 50k$
$R_2 = 75k$
0
7.5
15
(b)
V (volts)

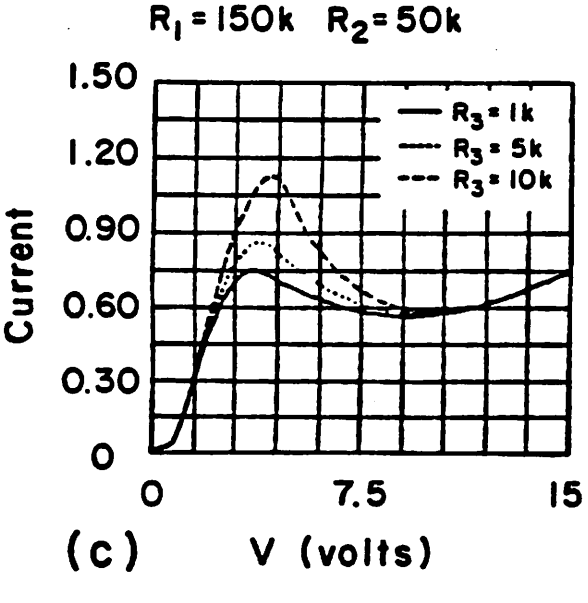
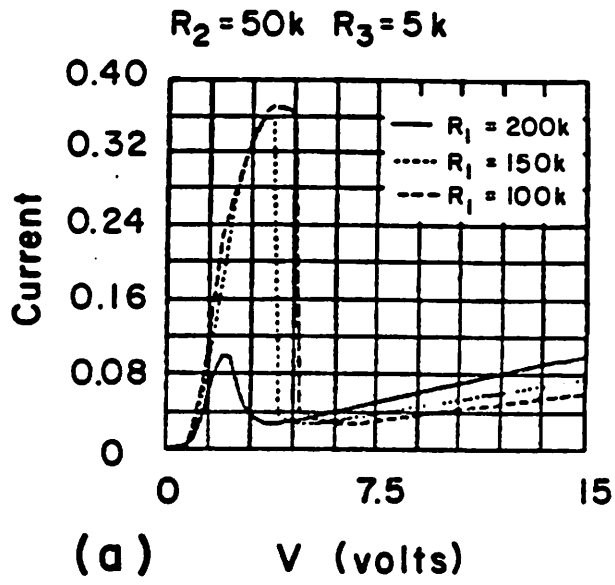
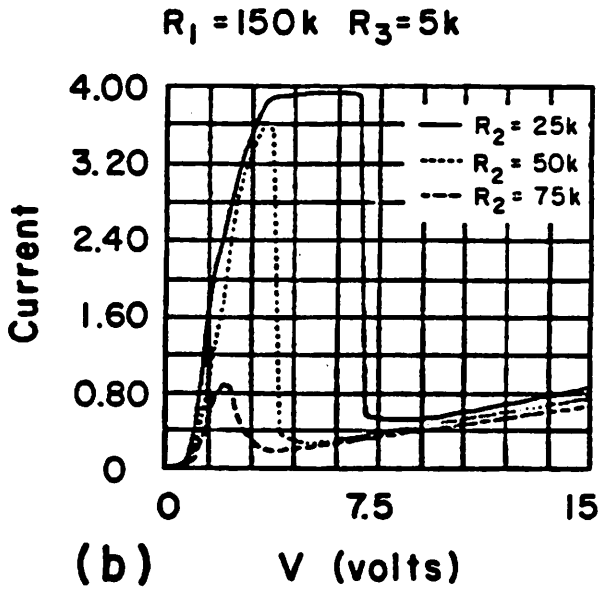

$R_1 = 150k \quad R_2 = 50k$
1.50
1.20
0.90
0.60
0.30
0
Current
$R_3 = 1k$
$R_3 = 5k$
$R_3 = 10k$
0
7.5
15
(c)
V (volts)

Fig. A-3


$R_2 = 50k \quad R_3 = 5k$
0.40
0.32
0.24
0.16
0.08
0
Current
$R_1 = 200k$
$R_1 = 150k$
$R_1 = 100k$
0
7.5
15
(a)
V (volts)


$R_1 = 150k \quad R_3 = 5k$
4.00
3.20
2.40
1.60
0.80
0
Current
$R_2 = 25k$
$R_2 = 50k$
$R_2 = 75k$
0
7.5
15
(b)
V (volts)

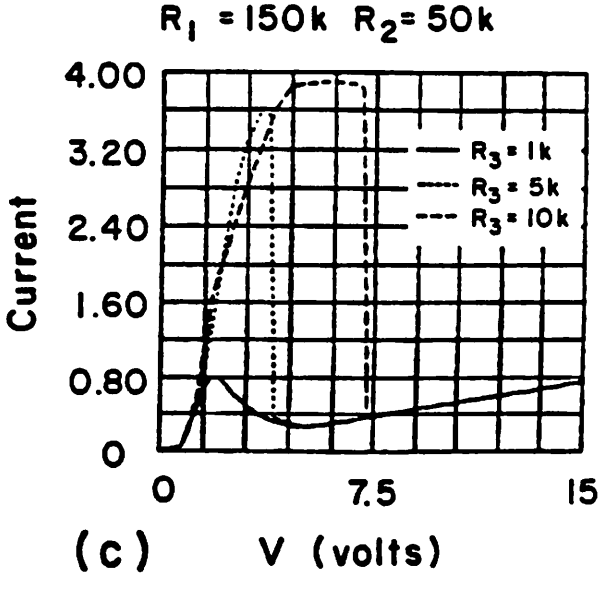
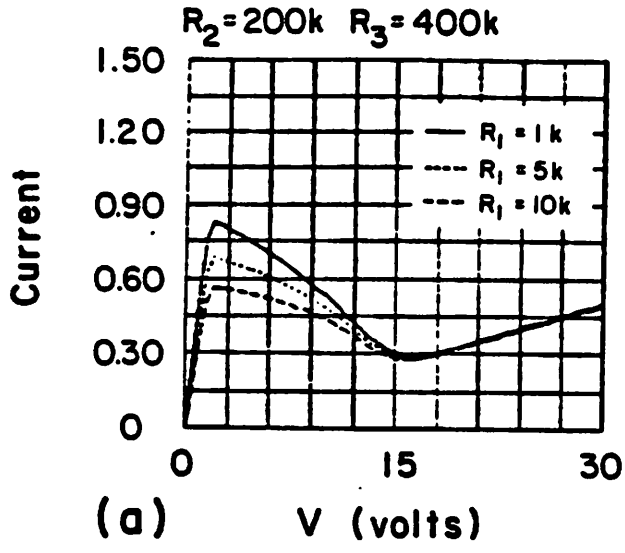
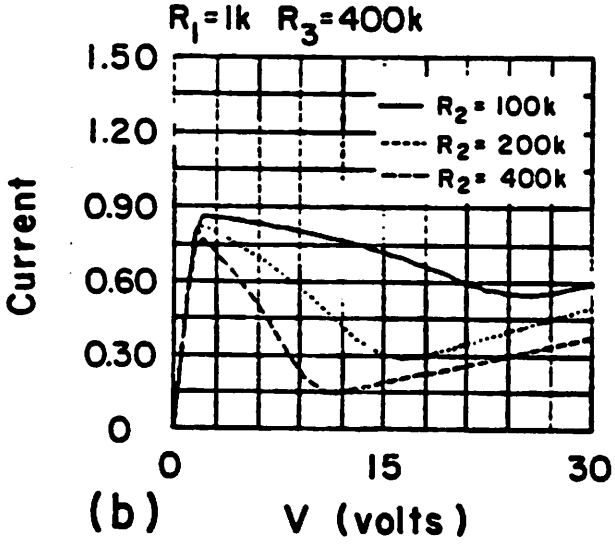

$R_1 = 150k \quad R_2 = 50k$
4.00
3.20
2.40
1.60
0.80
0
Current
$R_3 = 1k$
$R_3 = 5k$
$R_3 = 10k$
0
7.5
15
(c)
V (volts)

Fig. A-4


R2=200k R3=400k
1.50
1.20
0.90
0.60
0.30
0
Current
R1 = 1k
R1 = 5k
R1 = 10k
0
15
30
(a)
V (volts)


R1=1k R3=400k
1.50
1.20
0.90
0.60
0.30
0
Current
R2 = 100k
R2 = 200k
R2 = 400k
0
15
30
(b)
V (volts)

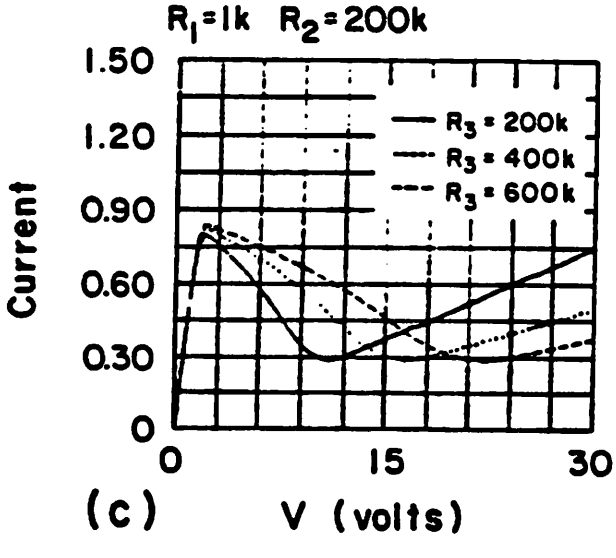
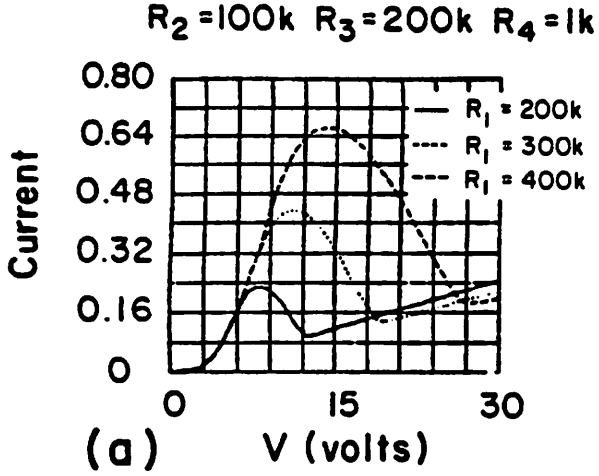
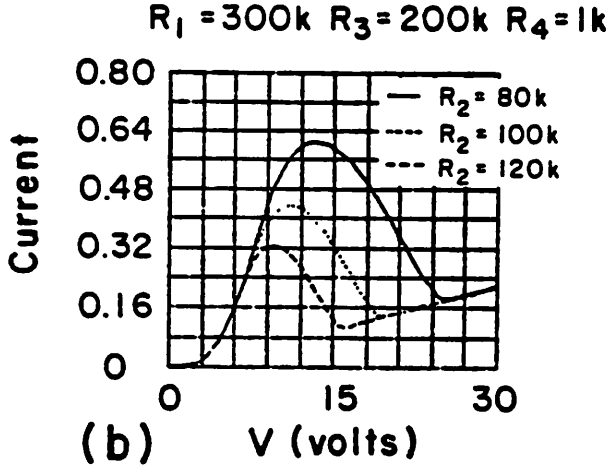
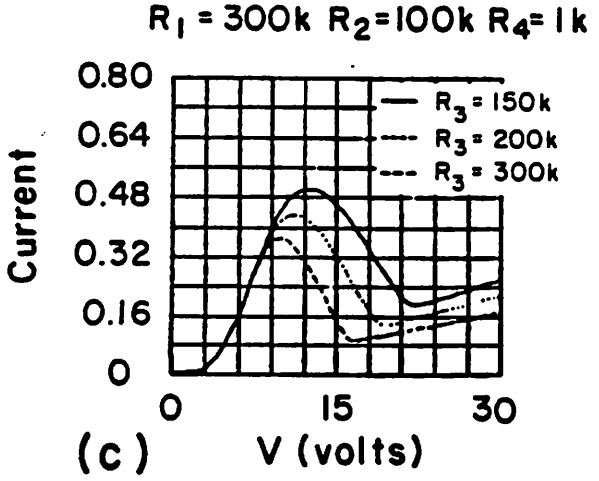

R1=1k R2=200k
1.50
1.20
0.90
0.60
0.30
0
Current
R3 = 200k
R3 = 400k
R3 = 600k
0
15
30
(c)
V (volts)

Fig. A-5


R_2 =100k R_3=200k R_4=1k
Current
0.80
0.64
0.48
0.32
0.16
0
0
15
30
R_1 = 200k
R_1 = 300k
R_1 = 400k
(a)
V (volts)


R_1 =300k R_3=200k R_4=1k
Current
0.80
0.64
0.48
0.32
0.16
0
0
15
30
R_2 = 80k
R_2 = 100k
R_2 = 120k
(b)
V (volts)


R_1 = 300k R_2=100k R_4= 1k
Current
0.80
0.64
0.48
0.32
0.16
0
0
15
30
R_3 = 150k
R_3 = 200k
R_3 = 300k
(c)
V (volts)

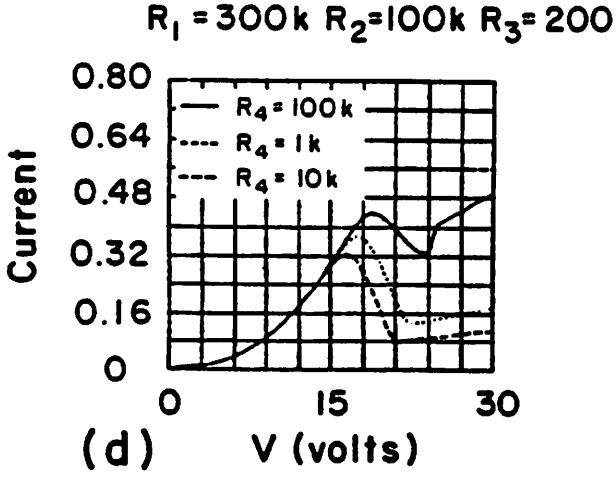
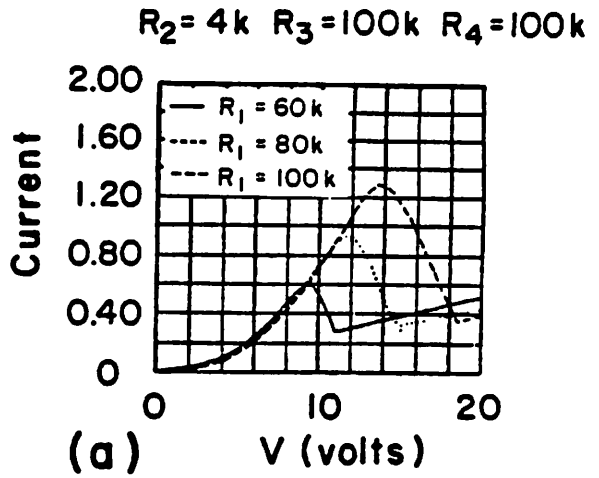
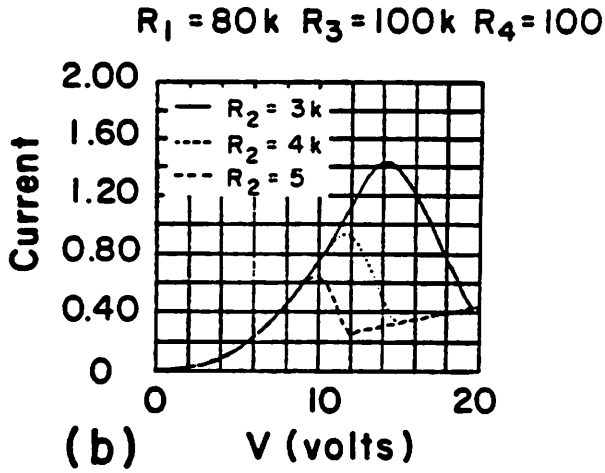
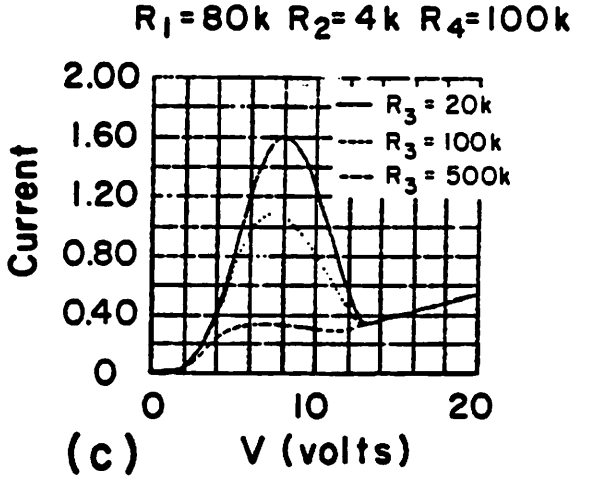

R_1 =300k R_2=100k R_3= 200k
Current
0.80
0.64
0.48
0.32
0.16
0
0
15
30
R_4 = 100k
R_4 = 1k
R_4 = 10k
(d)
V (volts)

Fig. A-6


R_2= 4k R_3=100k R_4=100k
Current
2.00
1.60
1.20
0.80
0.40
0
0
10
20
R_1 = 60k
R_1 = 80k
R_1 = 100k
(a)
V (volts)


R_1 =80k R_3=100k R_4=100k
Current
2.00
1.60
1.20
0.80
0.40
0
0
10
20
R_2 = 3k
R_2 = 4k
R_2 = 5
(b)
V (volts)


R_1=80k R_2= 4k R_4=100k
Current
2.00
1.60
1.20
0.80
0.40
0
0
10
20
R_3 = 20k
R_3 = 100k
R_3 = 500k
(c)
V (volts)

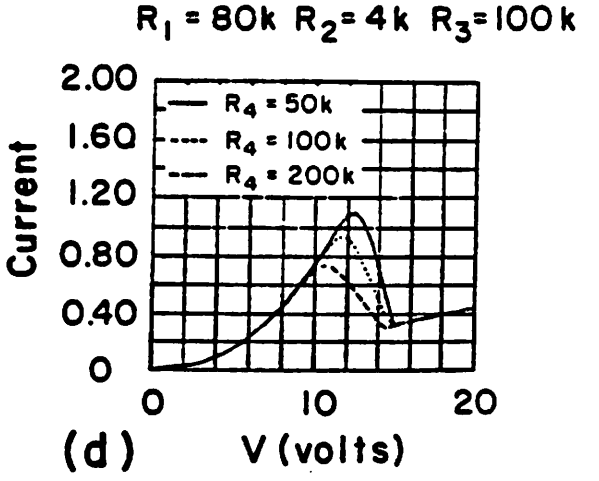
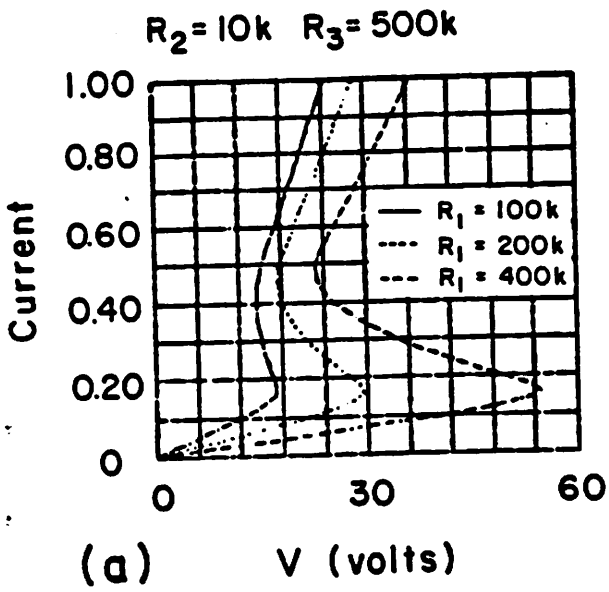
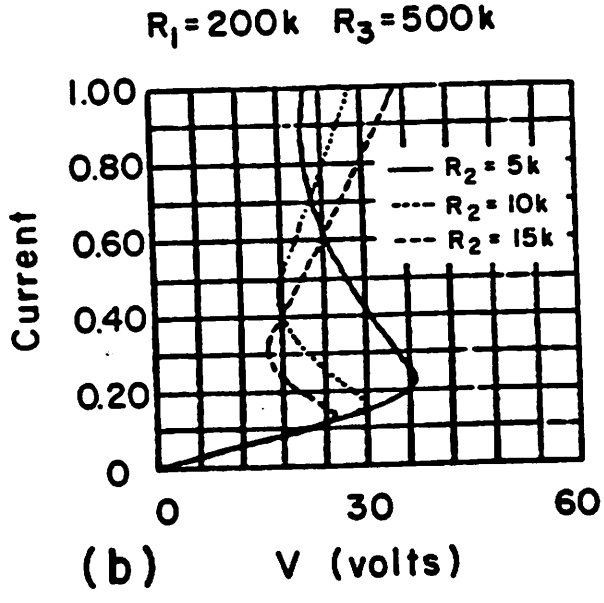

R_1 = 80k R_2= 4k R_3=100k
Current
2.00
1.60
1.20
0.80
0.40
0
0
10
20
R_4 = 50k
R_4 = 100k
R_4 = 200k
(d)
V (volts)

Fig. A-7


R_2 = 10k R_3 = 500k
1.00
0.80
0.60
0.40
0.20
0
Current
R_1 = 100k
R_1 = 200k
R_1 = 400k
0
30
60
(a) V (volts)


R_1 = 200k R_3 = 500k
1.00
0.80
0.60
0.40
0.20
0
Current
R_2 = 5k
R_2 = 10k
R_2 = 15k
0
30
60
(b) V (volts)

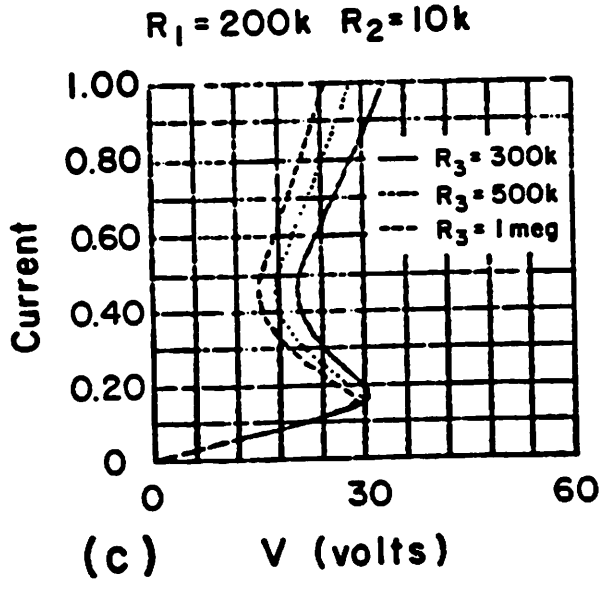
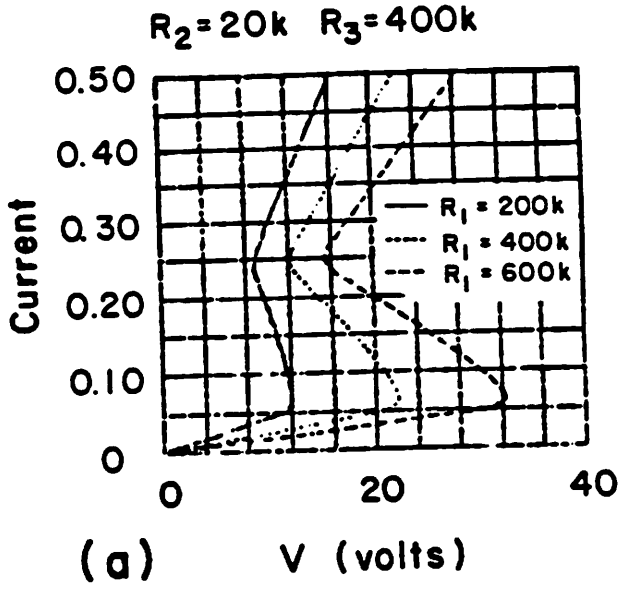
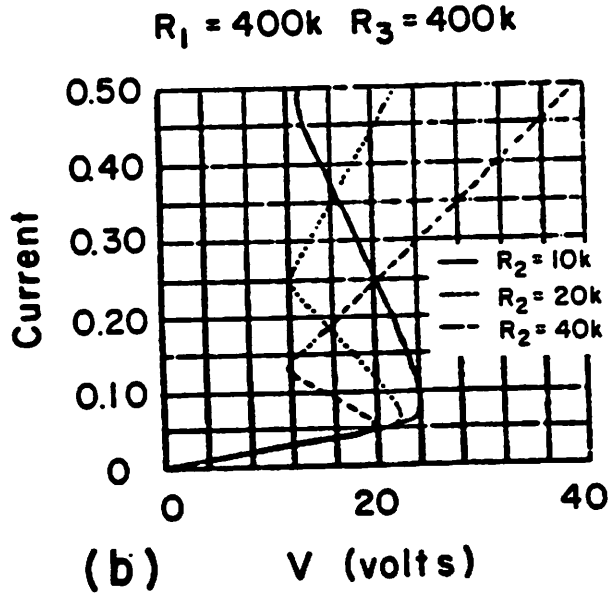

R_1 = 200k R_2 = 10k
1.00
0.80
0.60
0.40
0.20
0
Current
R_3 = 300k
R_3 = 500k
R_3 = 1 meg
0
30
60
(c) V (volts)

Fig. A-8


R_2 = 20k R_3 = 400k
0.50
0.40
0.30
0.20
0.10
0
Current
R_1 = 200k
R_1 = 400k
R_1 = 600k
0
20
40
(a) V (volts)


R_1 = 400k R_3 = 400k
0.50
0.40
0.30
0.20
0.10
0
Current
R_2 = 10k
R_2 = 20k
R_2 = 40k
0
20
40
(b) V (volts)

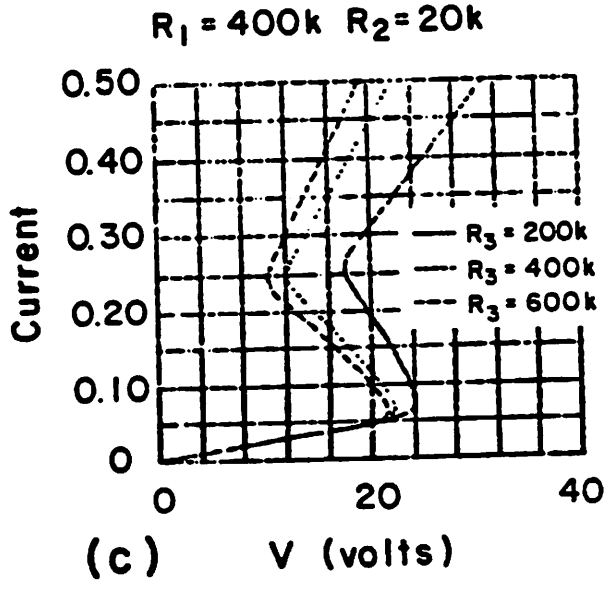
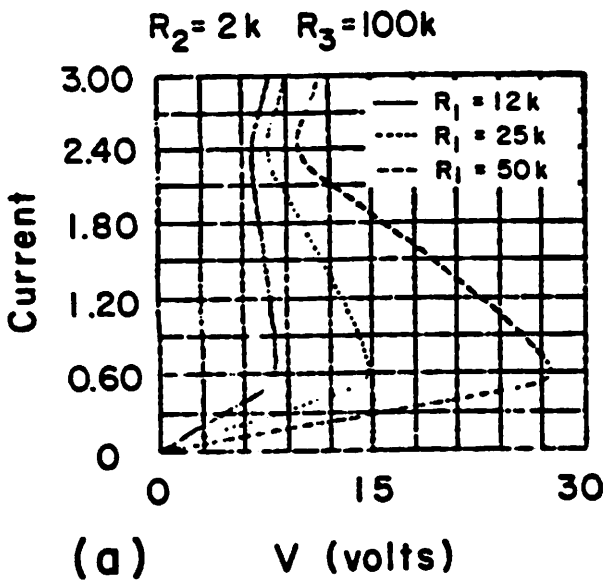
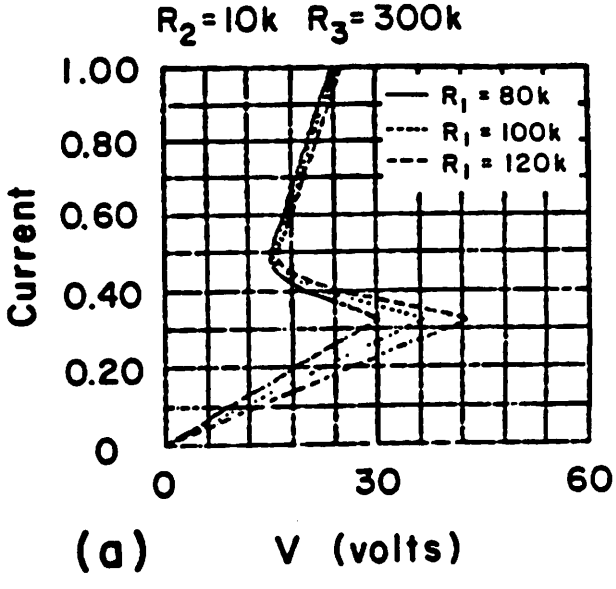
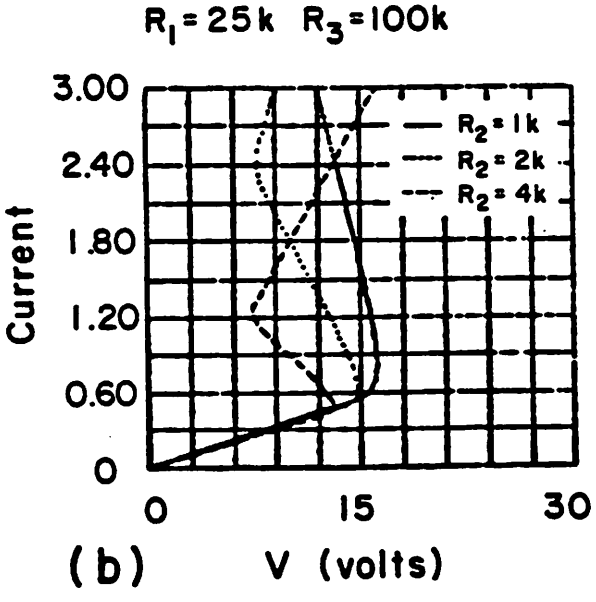
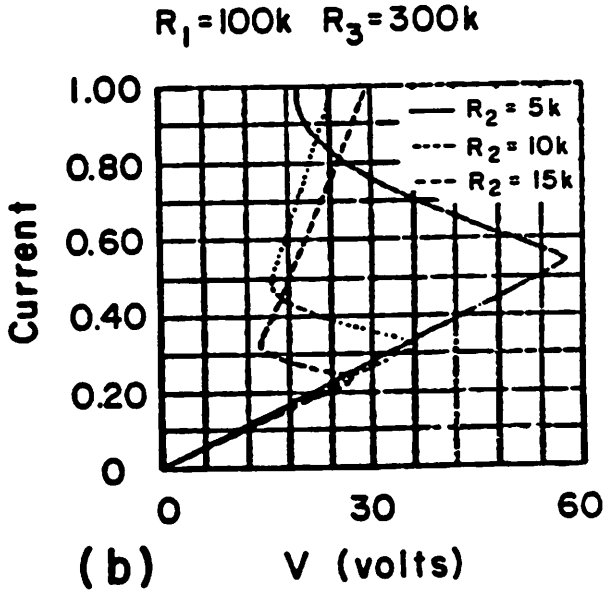

R_1 = 400k R_2 = 20k
0.50
0.40
0.30
0.20
0.10
0
Current
R_3 = 200k
R_3 = 400k
R_3 = 600k
0
20
40
(c) V (volts)

Fig. A-9









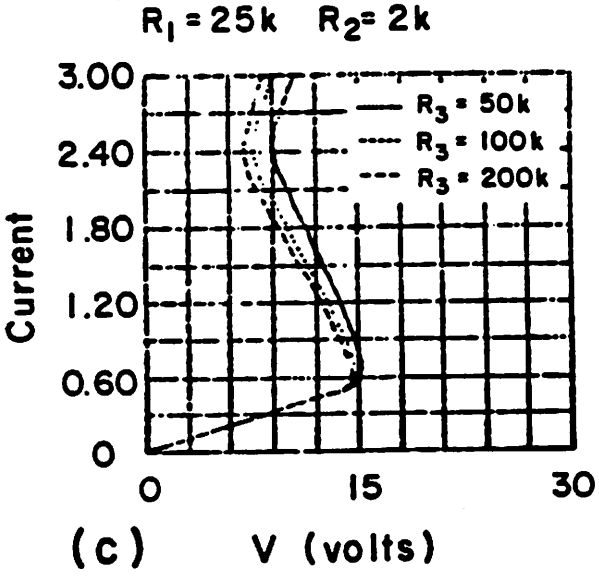


Fig. A-10

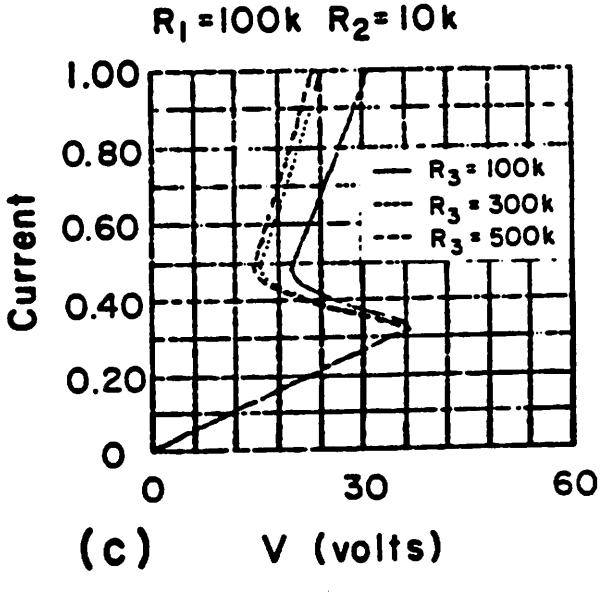
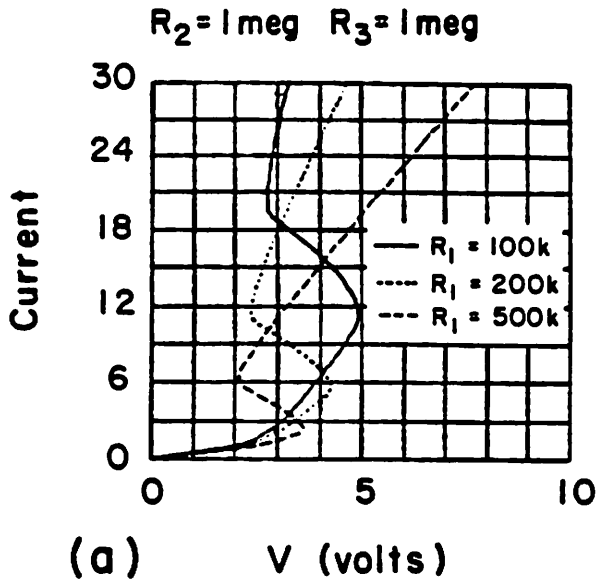
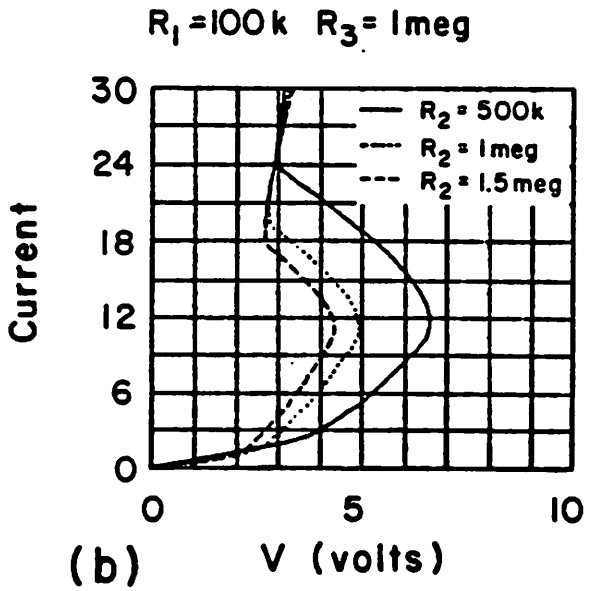


Fig. A-11





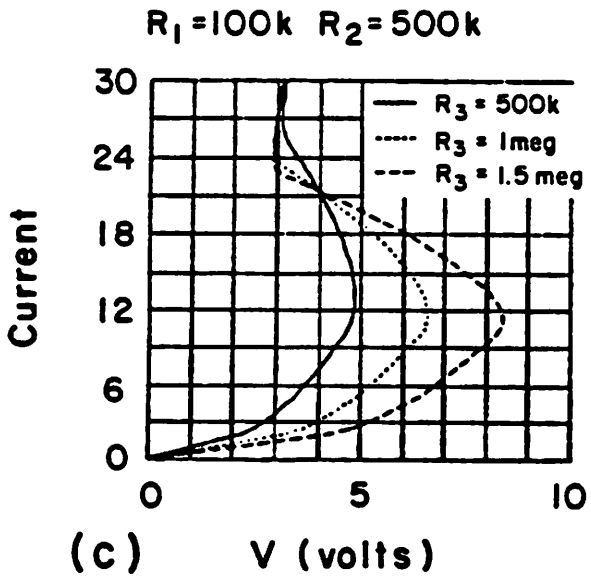
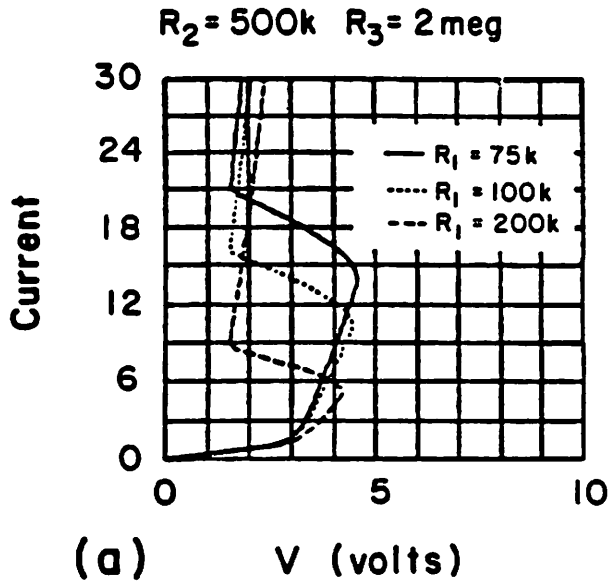
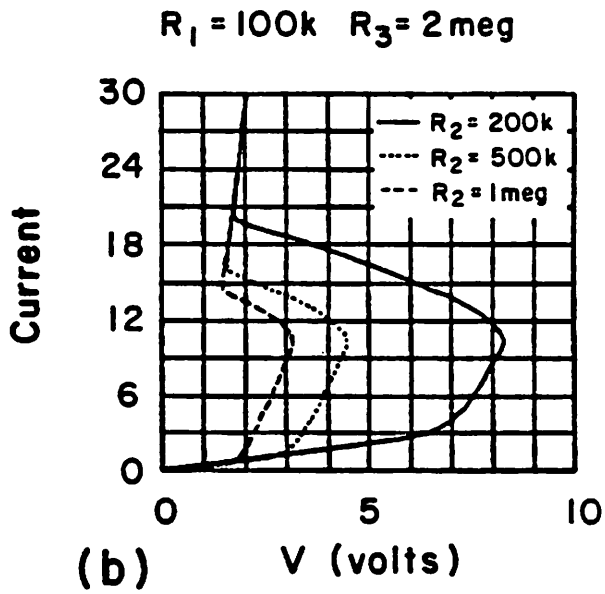


Fig. A-12





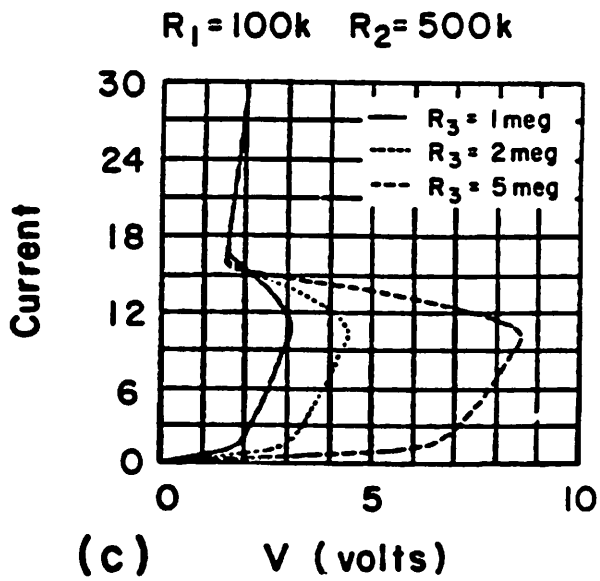
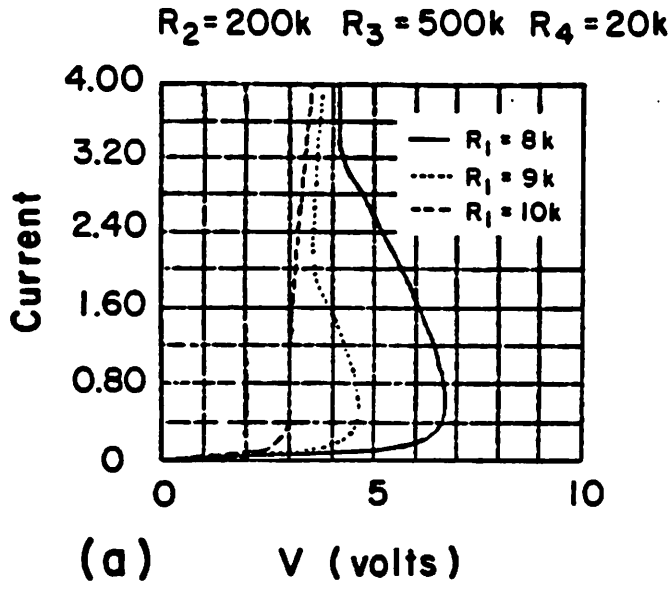
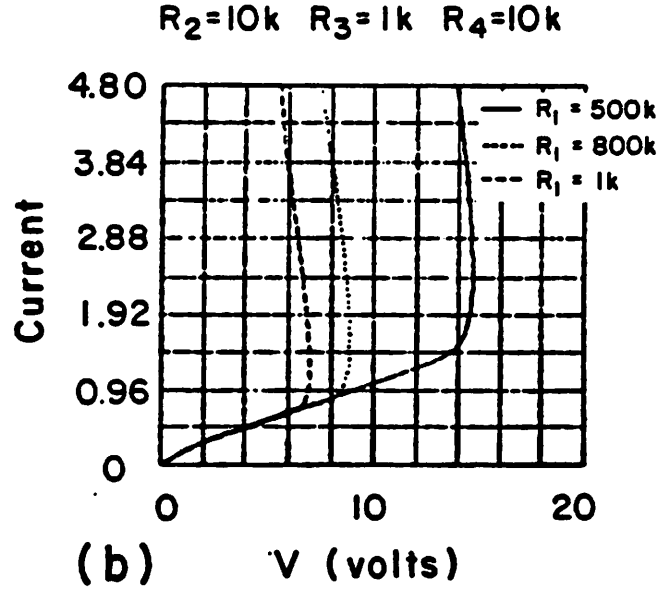


Fig. A-13


R_2=200k R_3=500k R_4=20k
4.00
3.20
2.40
1.60
0.80
0
Current
R_1 = 8k
R_1 = 9k
R_1 = 10k
0
5
10
(a)
V (volts)


R_2=10k R_3=1k R_4=10k
4.80
3.84
2.88
1.92
0.96
0
Current
R_1 = 500k
R_1 = 800k
R_1 = 1k
0
10
20
(b)
V (volts)

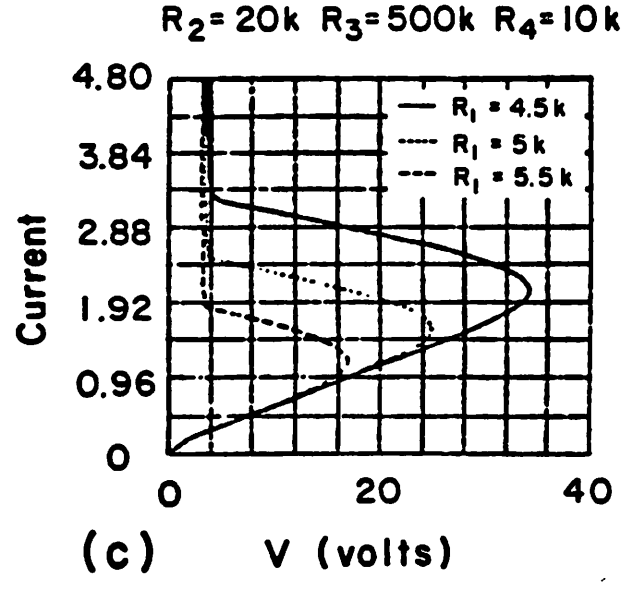

R_2= 20k R_3=500k R_4=10k
4.80
3.84
2.88
1.92
0.96
0
Current
R_1 = 4.5k
R_1 = 5k
R_1 = 5.5k
0
20
40
(c)
V (volts)

Fig. A-14

Appendix C: Family of V-I Characteristics for Type-N Devices Cataloged in Table 1 and Table 2 (Figures A-15 to A-60)

Legend:

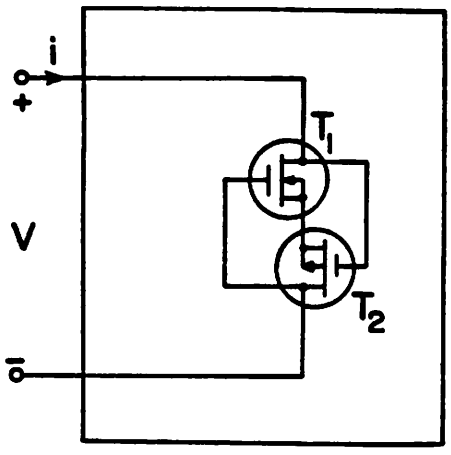
vto denotes "threshold voltage" of FET

KP denotes "transconductance parameter" of FET

Area denotes the "area factor" of JFET

Remarks:

1. All MOSFETs in Figs. A-15 to A-22 are "depletion mode" devices.
2. All JFETS in Figs. A-23 to A-29 are simulated by SPICE 2G with default value.
3. All MOSFETs in Figs. A-30 to A-36 have vto = 4V unless otherwise specified.
4. All JFETs in Figs. A-37 to A-51 are simulated by SPICE 2G with default values. All vto in these circuits denote the "threshold voltage" of the MOSFETs.



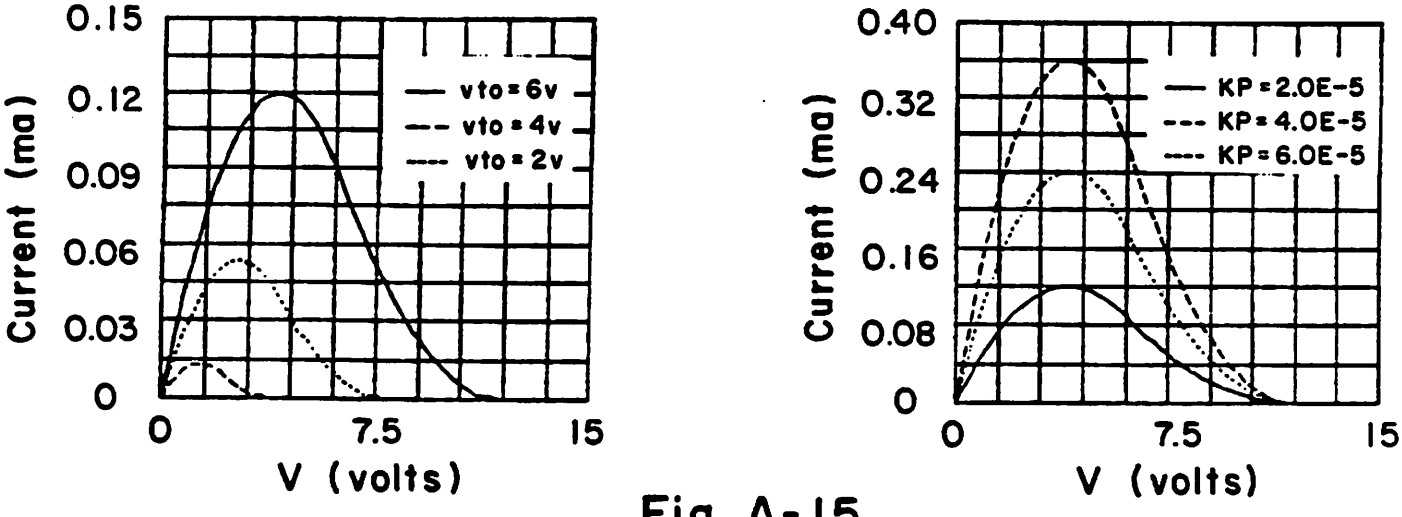


Fig. A-15

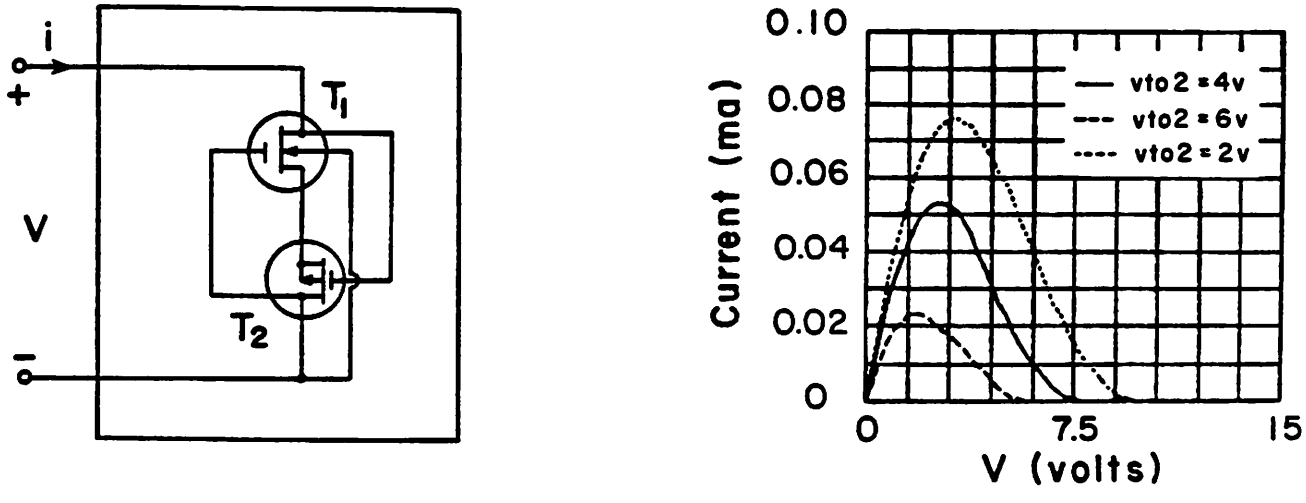
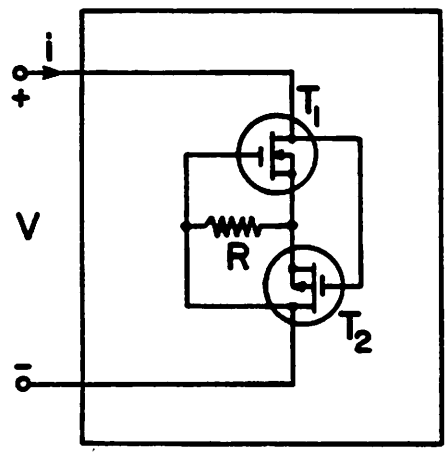


Fig. A-16



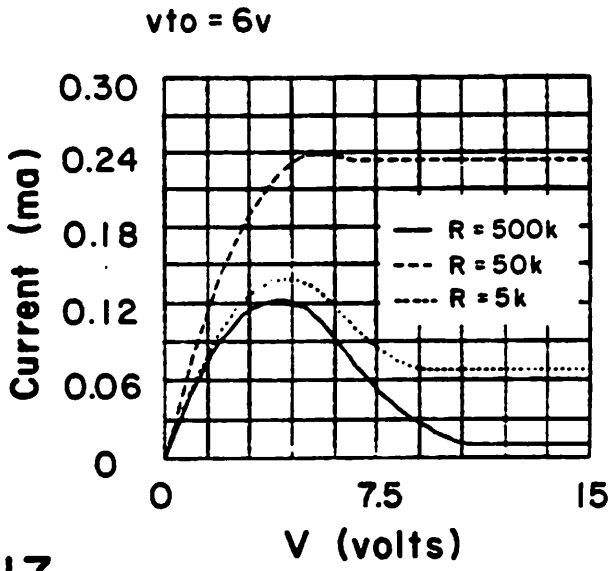
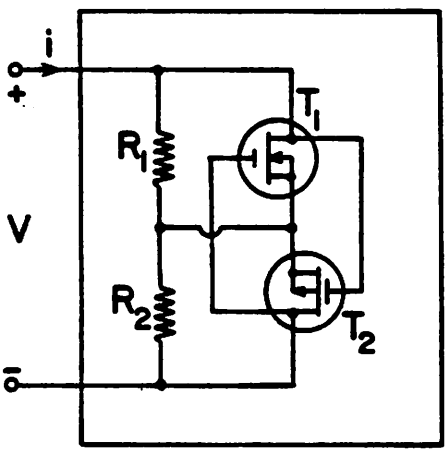


Fig. A-17



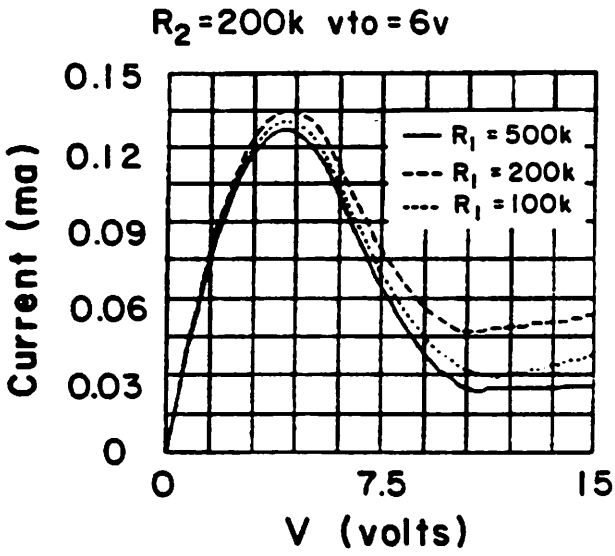


Fig. A-18

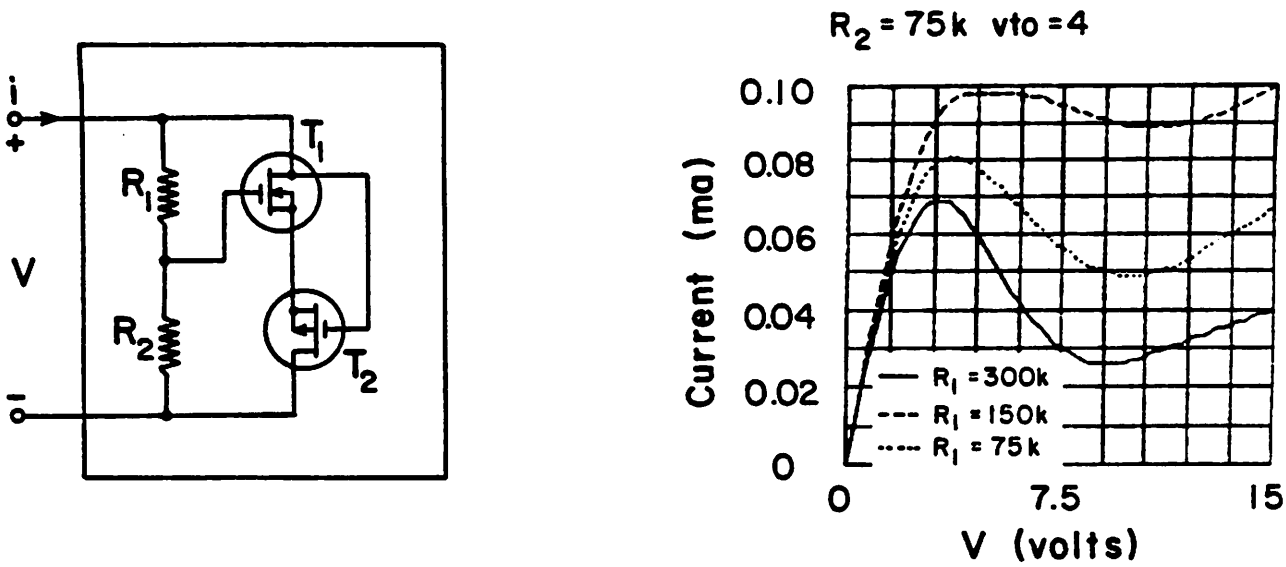
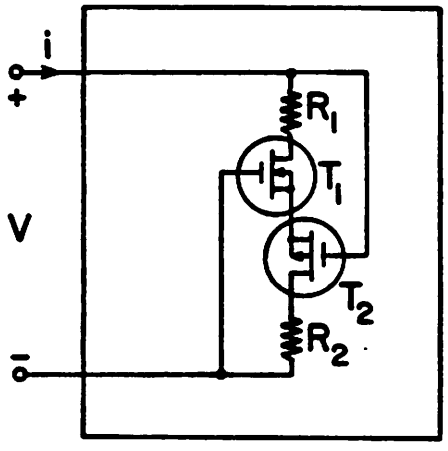
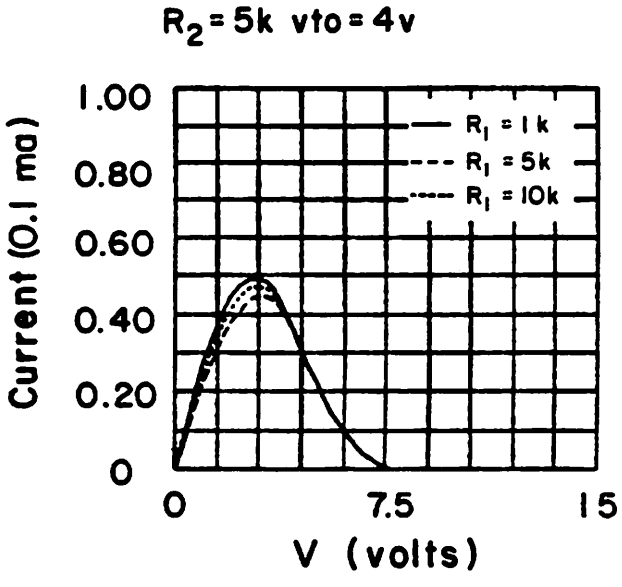

i
+
V
−
R1
R2
T1
T2
R2 = 75k vto = 4
Current (ma)
0.10
0.08
0.06
0.04
0.02
0
R1 = 300k
R1 = 150k
R1 = 75k
0
7.5
15
V (volts)

Fig. A-19


i
+
V
−
R1
T1
T2
R2


R2 = 5k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
R1 = 1k
R1 = 5k
R1 = 10k
0
7.5
15
V (volts)

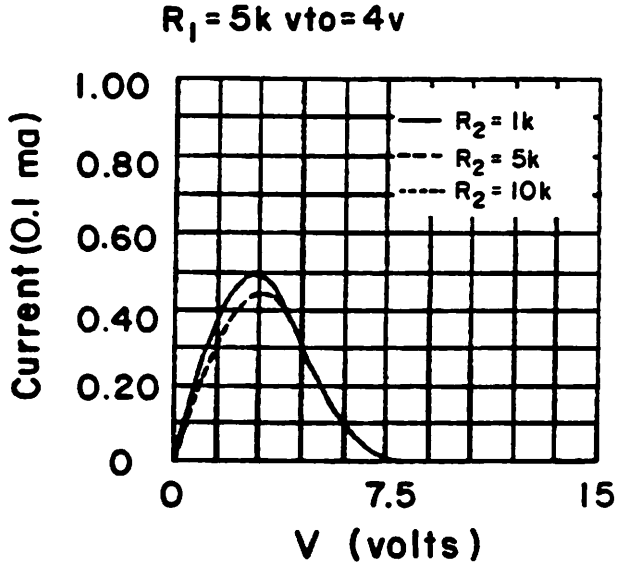
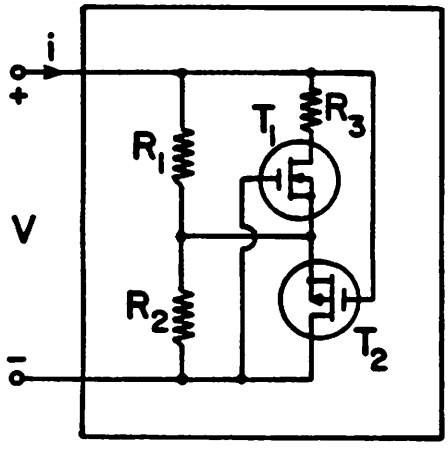
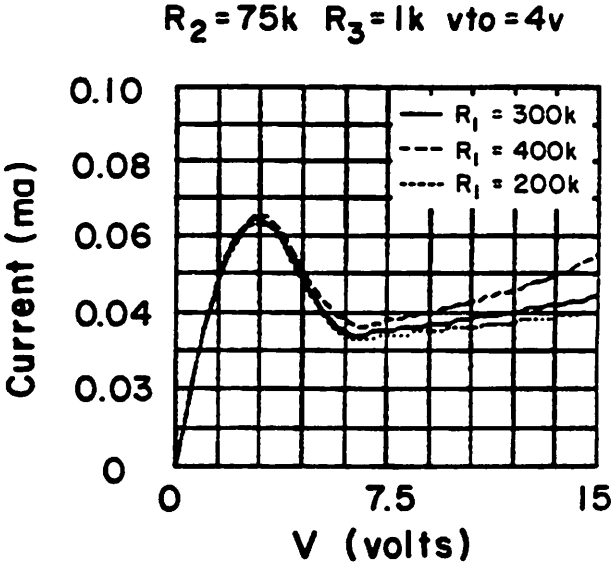
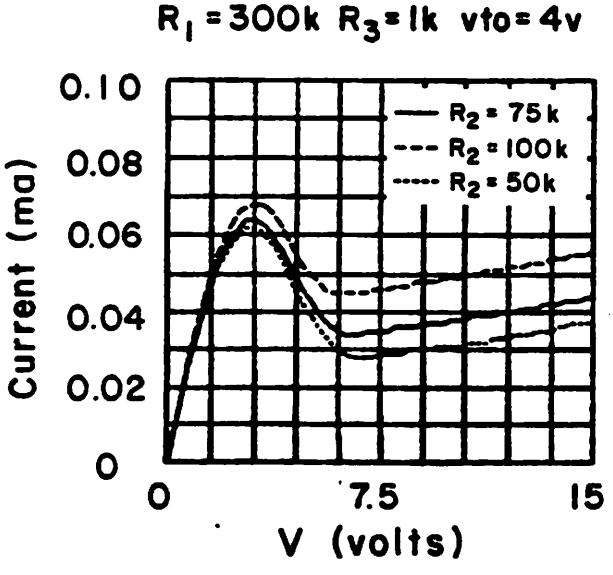

R1 = 5k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
R2 = 1k
R2 = 5k
R2 = 10k
0
7.5
15
V (volts)

Fig. A-20


i
+
V
−
R1
R2
R3
T1
T2


R2 = 75k R3 = 1k vto = 4v
0.10
0.08
0.06
0.04
0.03
0
Current (ma)
R1 = 300k
R1 = 400k
R1 = 200k
0
7.5
15
V (volts)


R1 = 300k R3 = 1k vto = 4v
0.10
0.08
0.06
0.04
0.02
0
Current (ma)
R2 = 75k
R2 = 100k
R2 = 50k
0
7.5
15
V (volts)

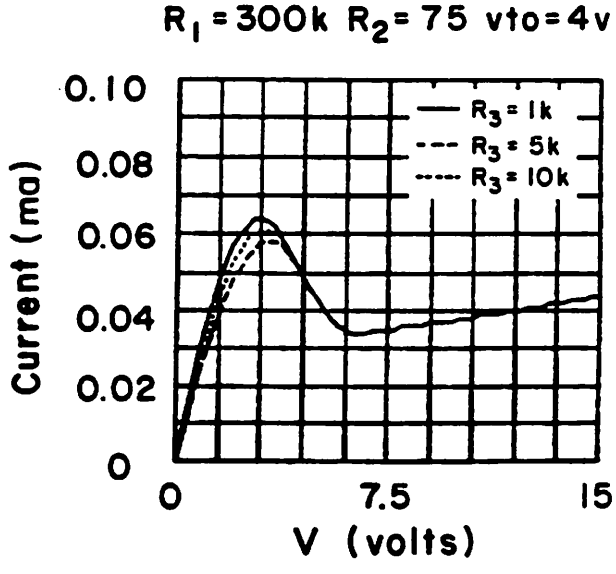
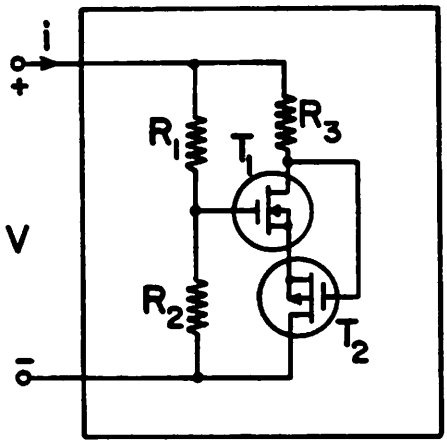
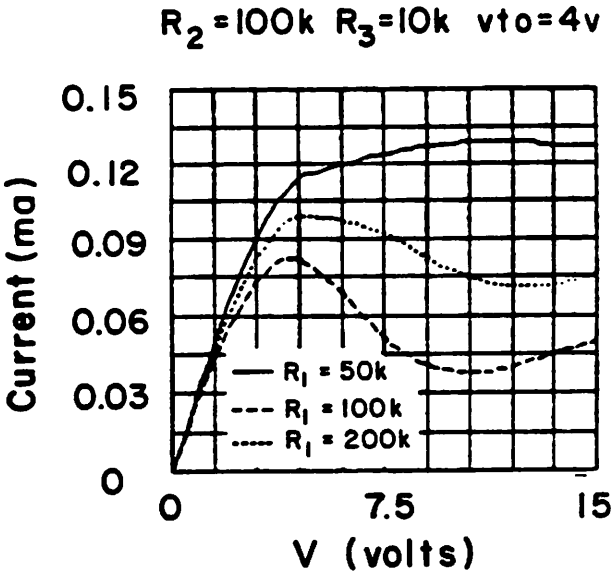
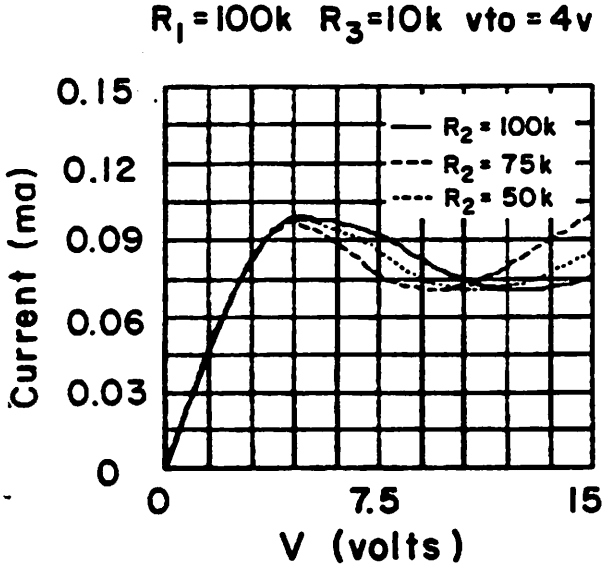

R1 = 300k R2 = 75 vto = 4v
0.10
0.08
0.06
0.04
0.02
0
Current (ma)
R3 = 1k
R3 = 5k
R3 = 10k
0
7.5
15
V (volts)

Fig. A-21


i
+
V
−
R1
T1
R3
R2
T2


R2 = 100k R3 = 10k vto = 4v
0.15
0.12
0.09
0.06
0.03
0
Current (ma)
R1 = 50k
R1 = 100k
R1 = 200k
0
7.5
15
V (volts)


R1 = 100k R3 = 10k vto = 4v
0.15
0.12
0.09
0.06
0.03
0
Current (ma)
R2 = 100k
R2 = 75k
R2 = 50k
0
7.5
15
V (volts)

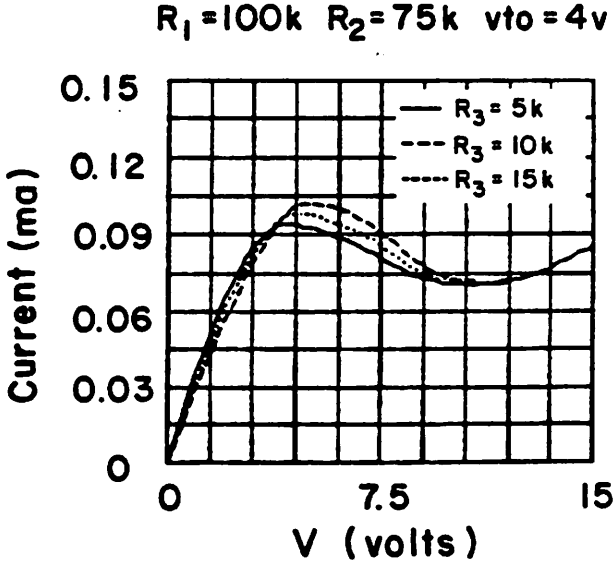
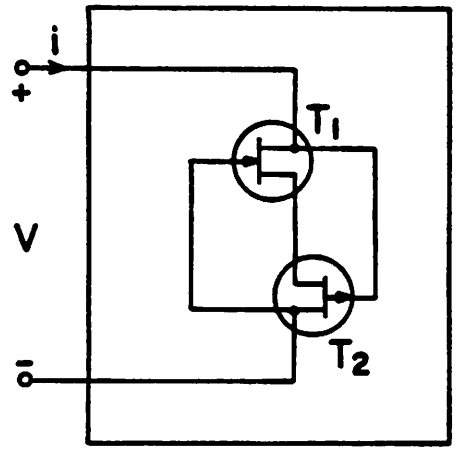

R1 = 100k R2 = 75k vto = 4v
0.15
0.12
0.09
0.06
0.03
0
Current (ma)
R3 = 5k
R3 = 10k
R3 = 15k
0
7.5
15
V (volts)

Fig. A-22



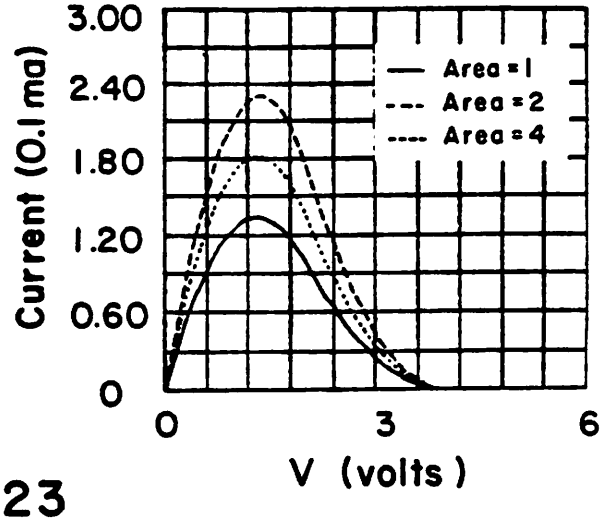
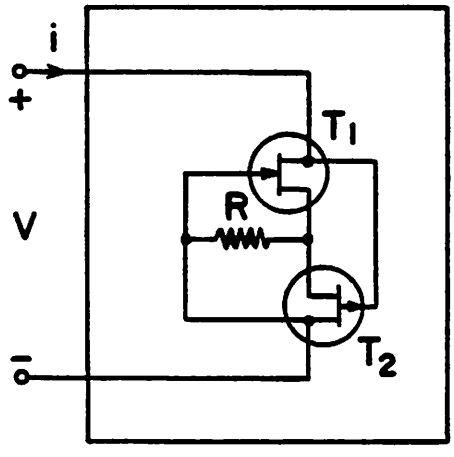


Fig. A-23



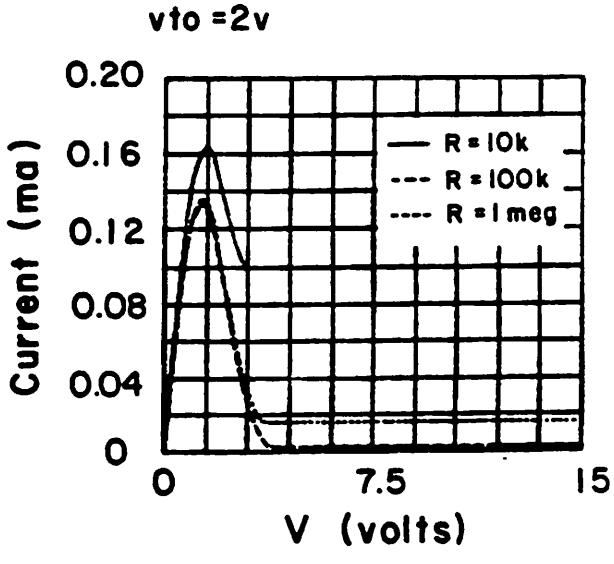
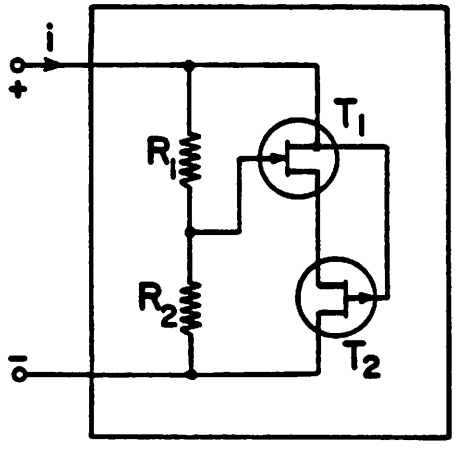
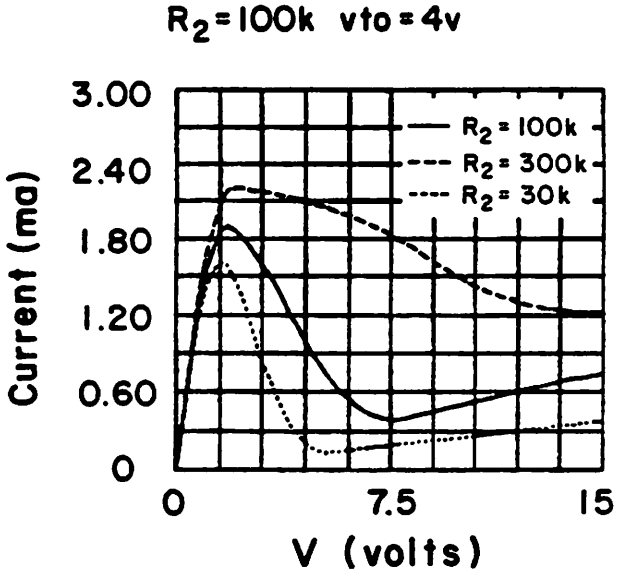


Fig. A-24


i
+
-
R_1
R_2
T_1
T_2


R_2 = 100k vto = 4v
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
0
7.5
15
V (volts)
R_2 = 100k
R_2 = 300k
R_2 = 30k

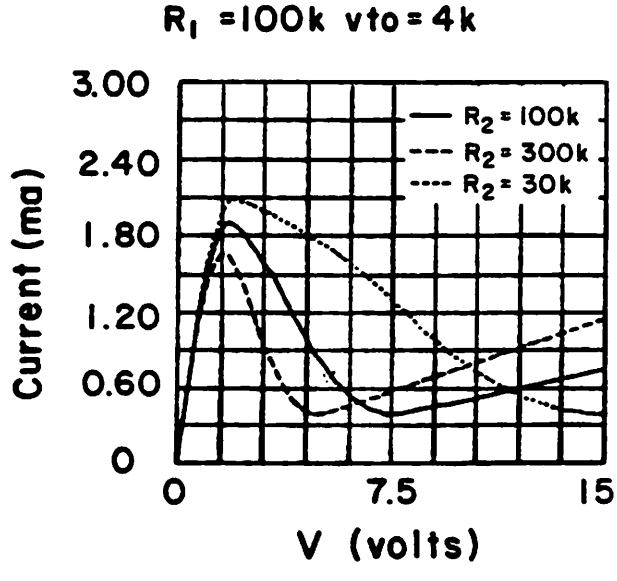
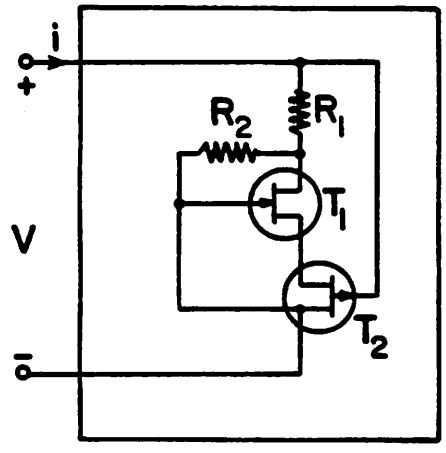
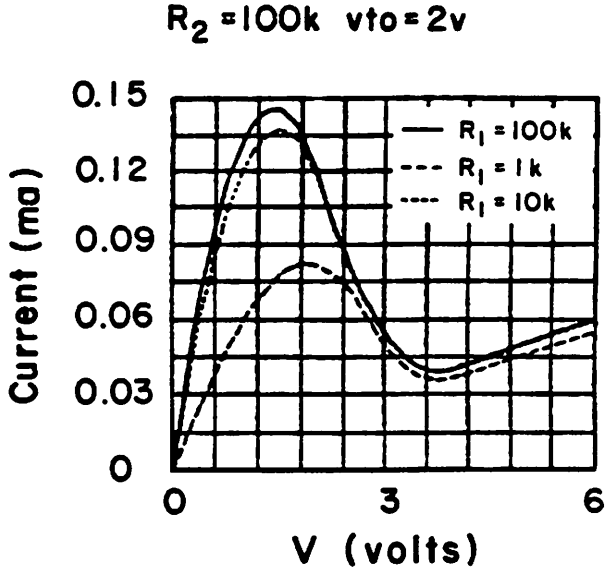

R_1 = 100k vto = 4k
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
0
7.5
15
V (volts)
R_2 = 100k
R_2 = 300k
R_2 = 30k

Fig. A-25


i
+
R2
R1
T1
V
T2
-


R2 = 100k vto = 2v
0.15
0.12
0.09
0.06
0.03
0
Current (ma)
R1 = 100k
R1 = 1k
R1 = 10k
0
3
6
V (volts)

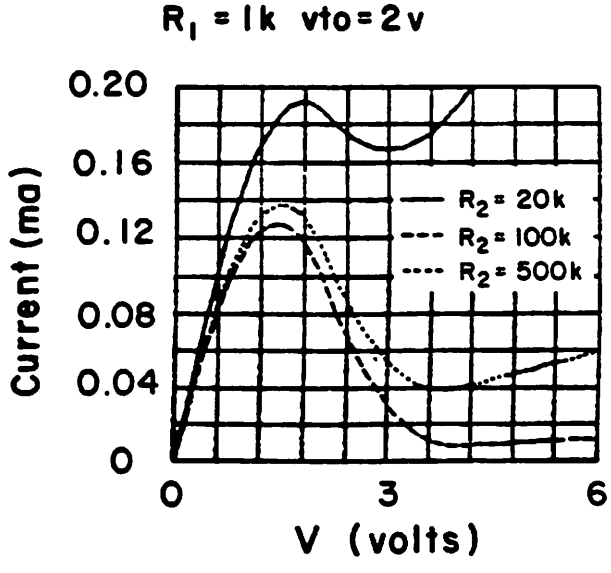
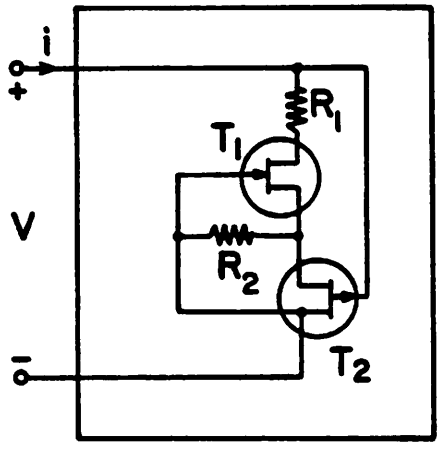
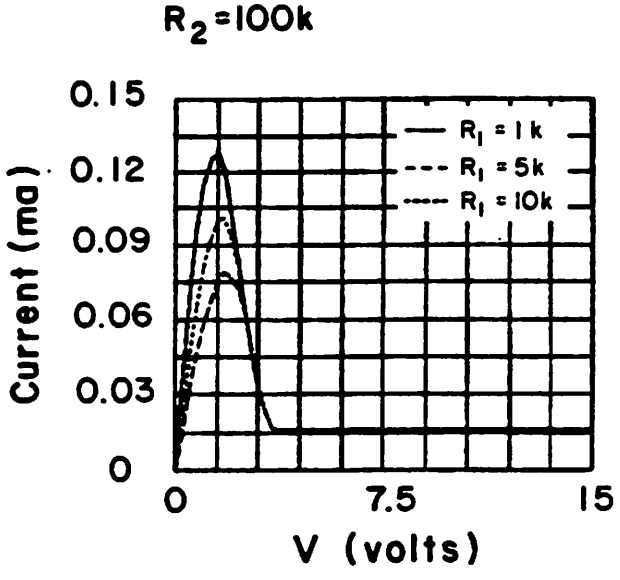

R1 = 1k vto = 2v
0.20
0.16
0.12
0.08
0.04
0
Current (ma)
R2 = 20k
R2 = 100k
R2 = 500k
0
3
6
V (volts)

Fig. A-26


i
+
V
−
R_1
T_1
R_2
T_2


R_2 = 100k
0.15
0.12
0.09
0.06
0.03
0
Current (ma)
R_1 = 1k
R_1 = 5k
R_1 = 10k
0
7.5
15
V (volts)

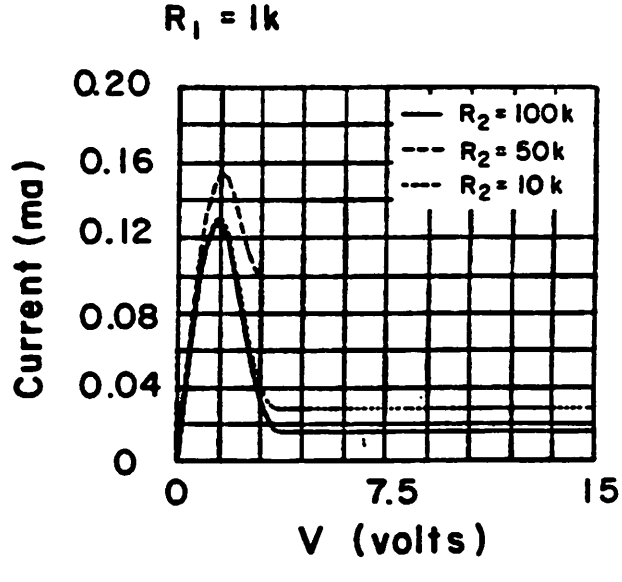
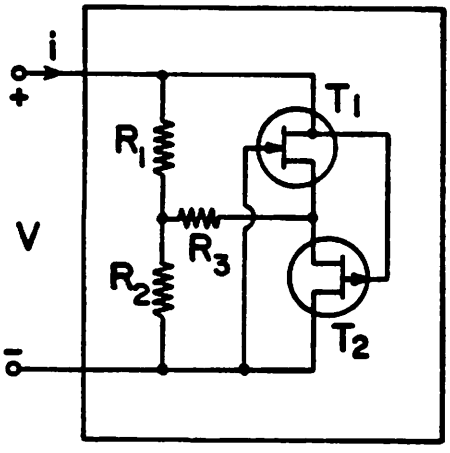
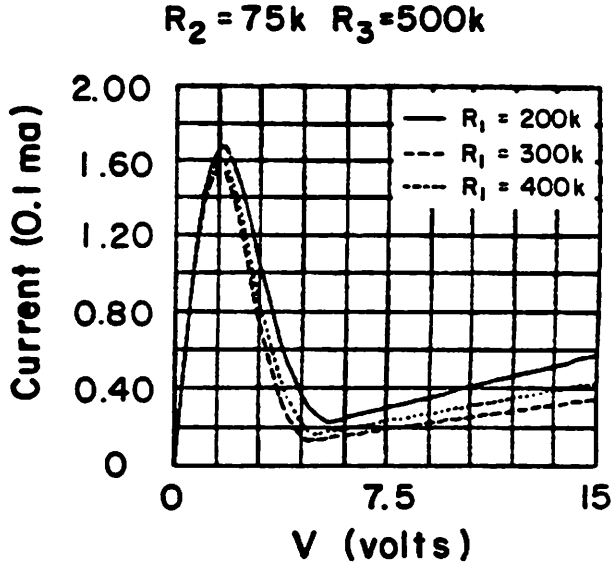
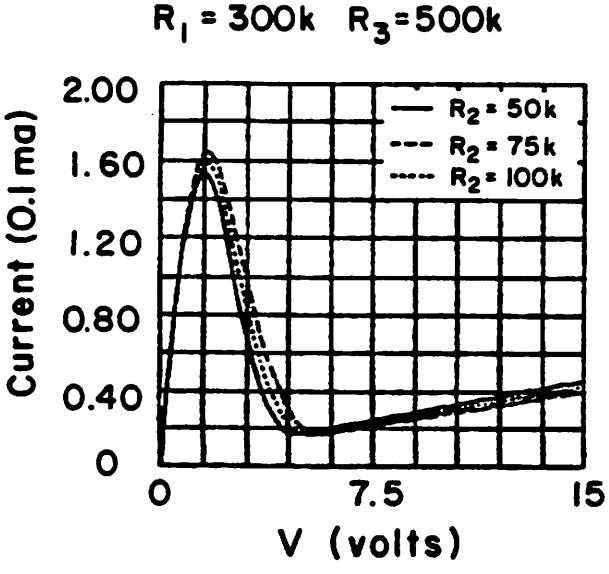

R_1 = 1k
0.20
0.16
0.12
0.08
0.04
0
Current (ma)
R_2 = 100k
R_2 = 50k
R_2 = 10k
0
7.5
15
V (volts)

Fig. A-27


i
+
V
−
R1
R2
R3
T1
T2


R2 = 75k R3 = 500k
Current (0.1 ma)
2.00
1.60
1.20
0.80
0.40
0
0
7.5
15
V (volts)
R1 = 200k
R1 = 300k
R1 = 400k


R1 = 300k R3 = 500k
Current (0.1 ma)
2.00
1.60
1.20
0.80
0.40
0
0
7.5
15
V (volts)
R2 = 50k
R2 = 75k
R2 = 100k

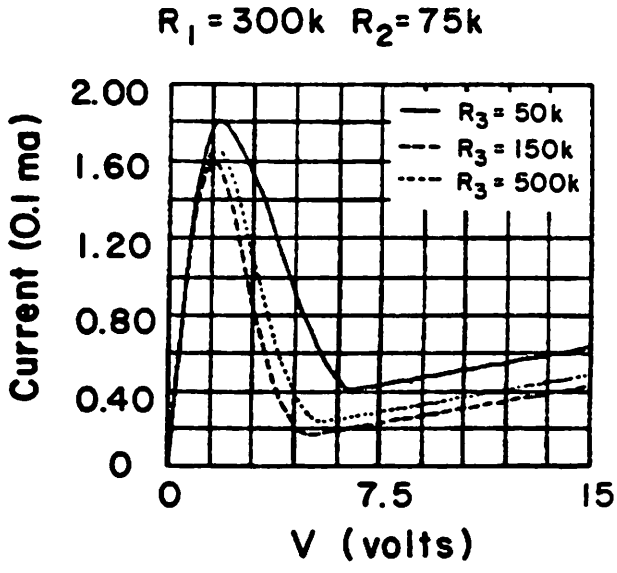
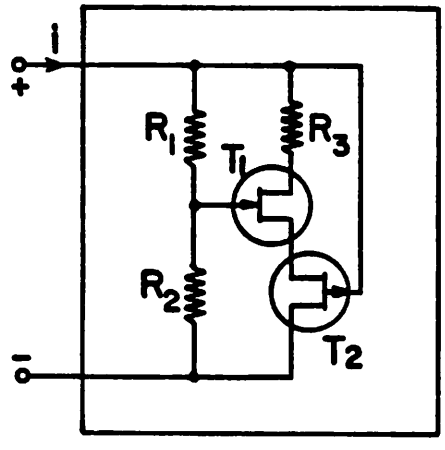
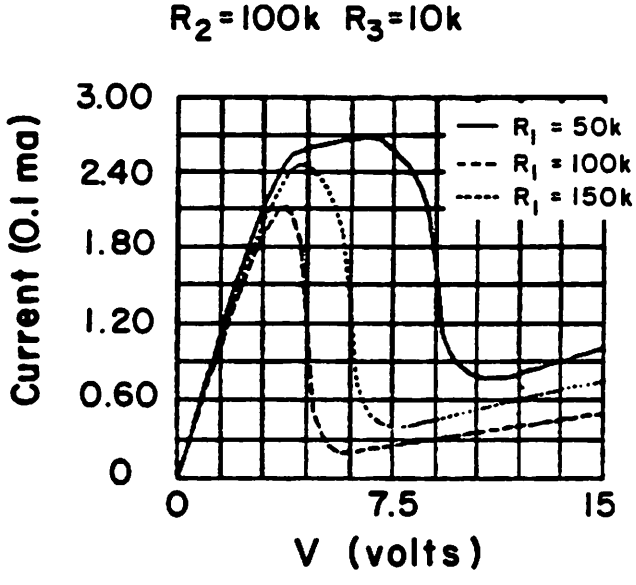
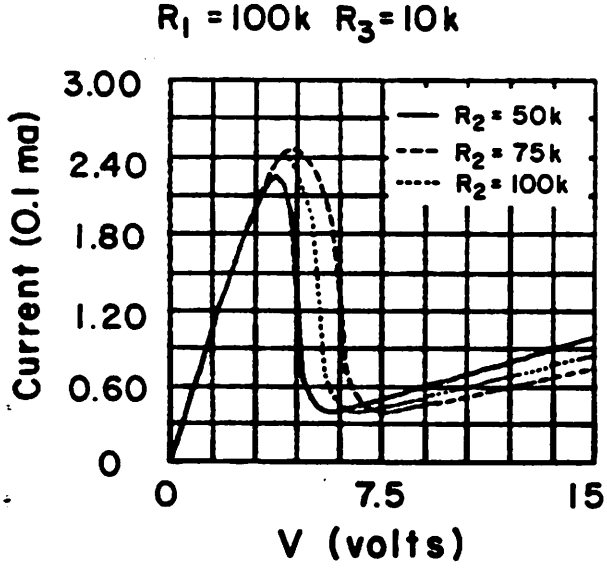

R1 = 300k R2 = 75k
Current (0.1 ma)
2.00
1.60
1.20
0.80
0.40
0
0
7.5
15
V (volts)
R3 = 50k
R3 = 150k
R3 = 500k

Fig. A-28


I
+
-
R1
R3
T1
R2
T2


R2 = 100k R3 = 10k
3.00
2.40
1.80
1.20
0.60
0
Current (0.1 ma)
R1 = 50k
R1 = 100k
R1 = 150k
0
7.5
15
V (volts)


R1 = 100k R3 = 10k
3.00
2.40
1.80
1.20
0.60
0
Current (0.1 ma)
R2 = 50k
R2 = 75k
R2 = 100k
0
7.5
15
V (volts)

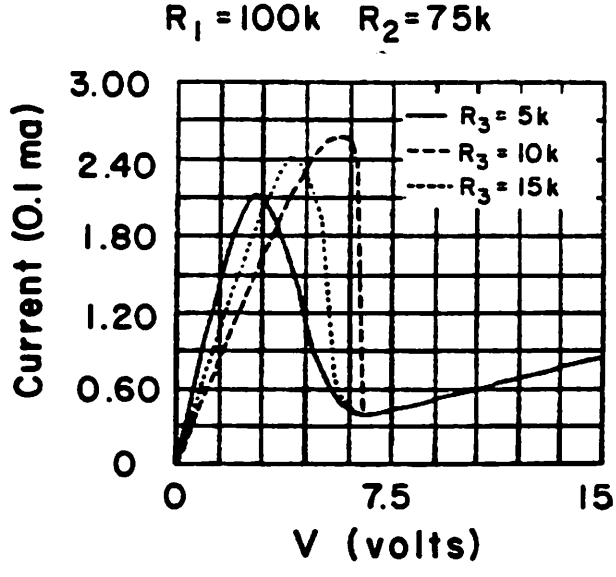
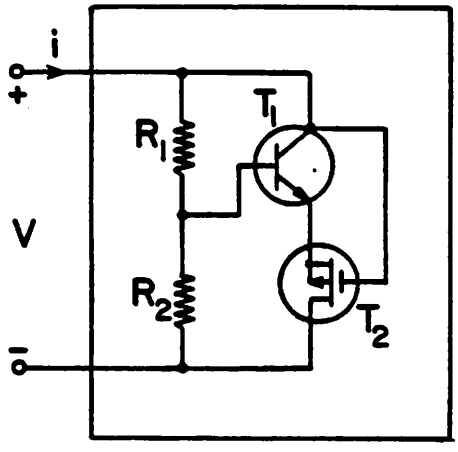
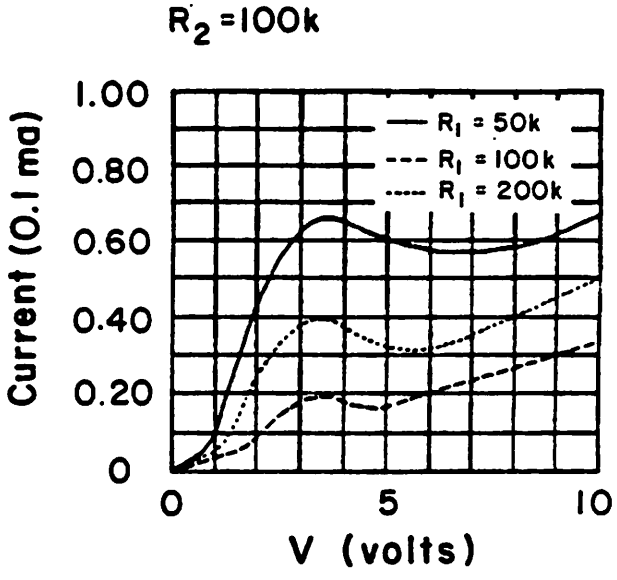

R1 = 100k R2 = 75k
3.00
2.40
1.80
1.20
0.60
0
Current (0.1 ma)
R3 = 5k
R3 = 10k
R3 = 15k
0
7.5
15
V (volts)

Fig. A-29


i
+
V
−
R1
R2
T1
T2


R2 = 100k
1.00
0.80
0.60
0.40
0.20
0
Current (0.1 ma)
R1 = 50k
R1 = 100k
R1 = 200k
0
5
10
V (volts)

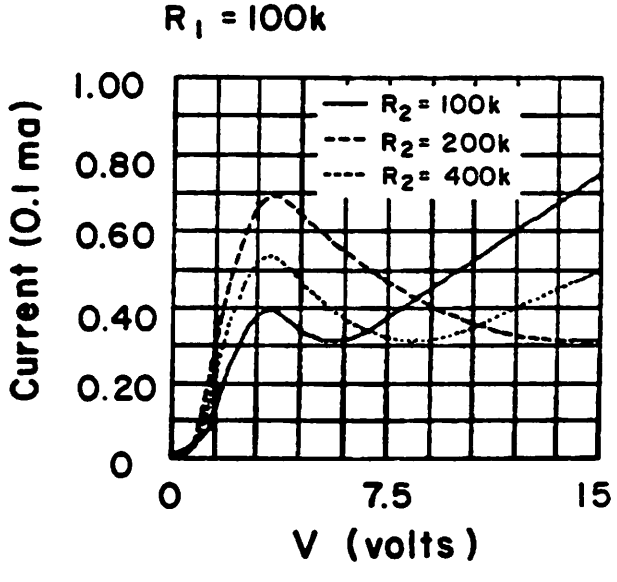
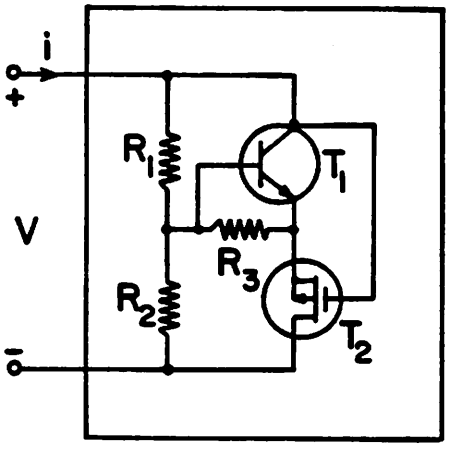
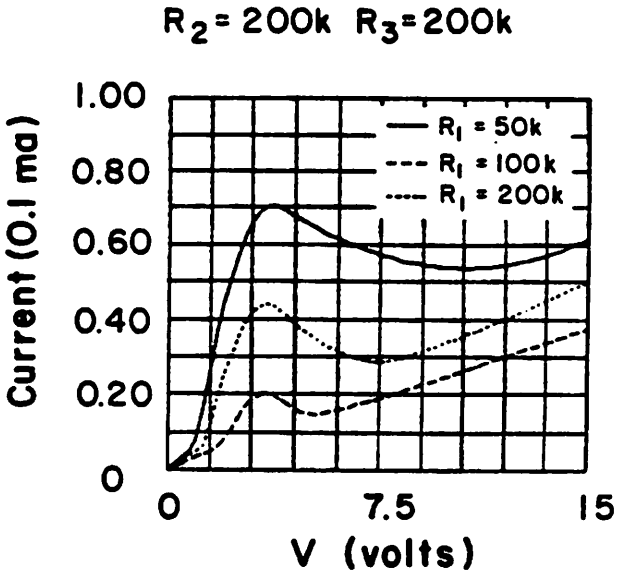
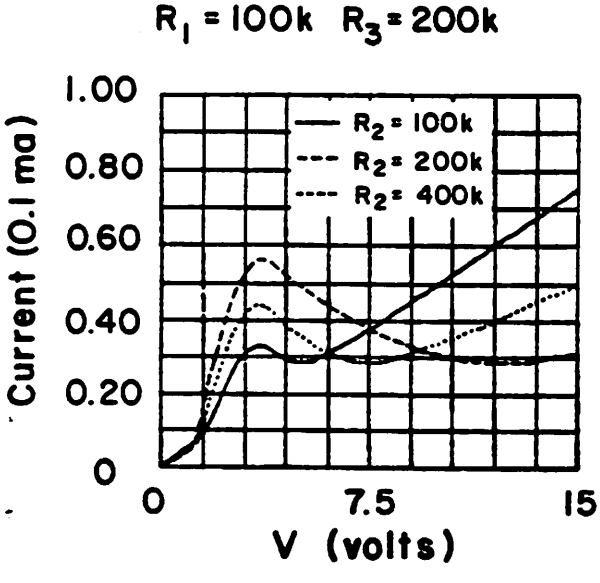

R1 = 100k
1.00
0.80
0.60
0.40
0.20
0
Current (0.1 ma)
R2 = 100k
R2 = 200k
R2 = 400k
0
7.5
15
V (volts)

Fig. A-30


i
+
V
-
R1
R2
R3
T1
T2


R2 = 200k R3=200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R1 = 50k
R1 = 100k
R1 = 200k


R1 = 100k R3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

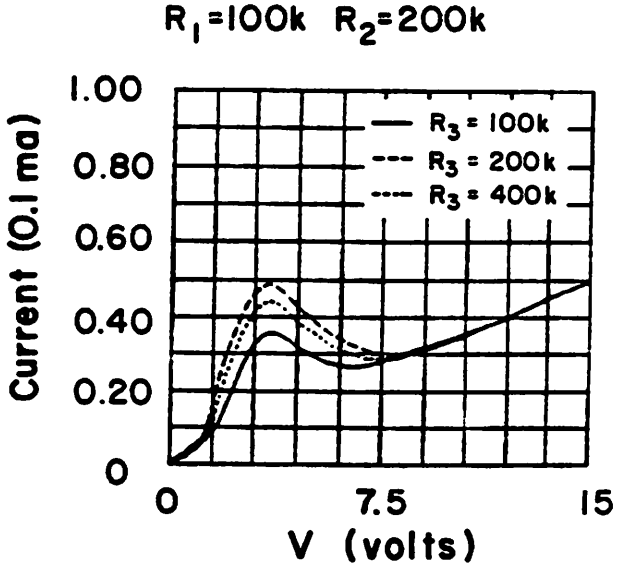
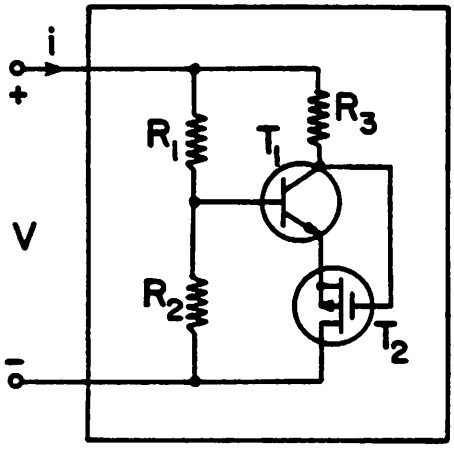
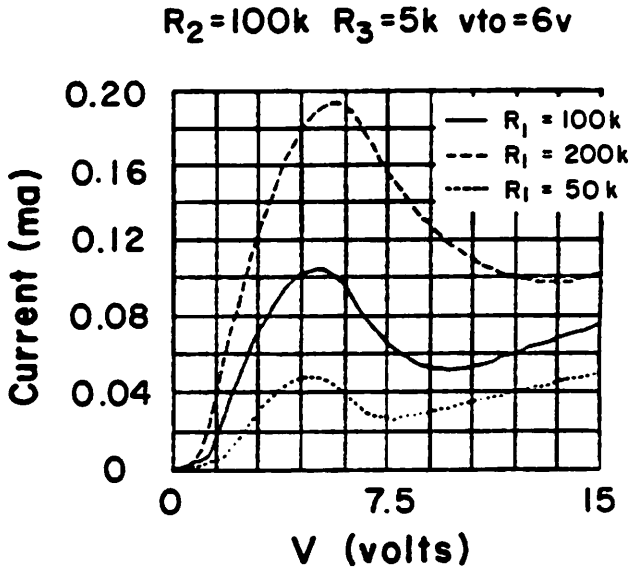
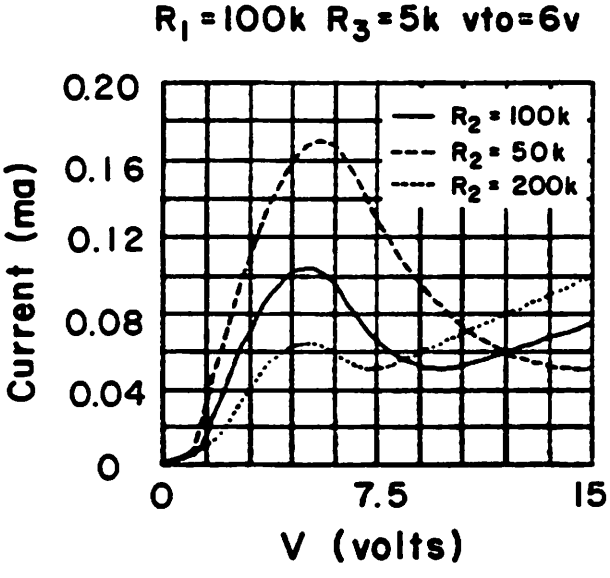

R1=100k R2=200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R3 = 100k
R3 = 200k
R3 = 400k

Fig. A-31


i
+
V
−
R1
R2
R3
T1
T2


R2=100k R3=5k vto=6v
0.20
0.16
0.12
0.08
0.04
0
Current (ma)
0
7.5
15
V (volts)
R1 = 100k
R1 = 200k
R1 = 50k


R1=100k R3=5k vto=6v
0.20
0.16
0.12
0.08
0.04
0
Current (ma)
0
7.5
15
V (volts)
R2 = 100k
R2 = 50k
R2 = 200k

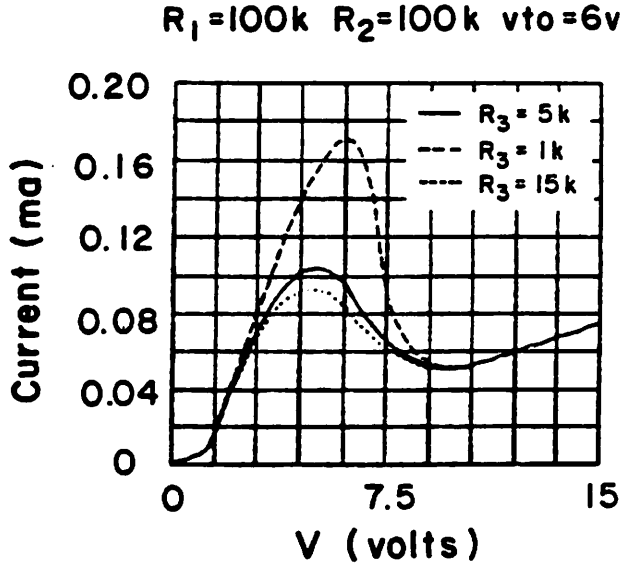
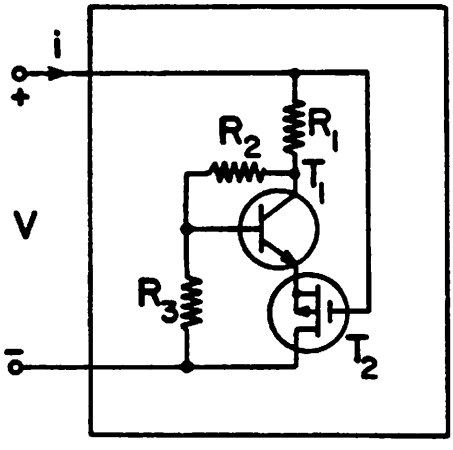
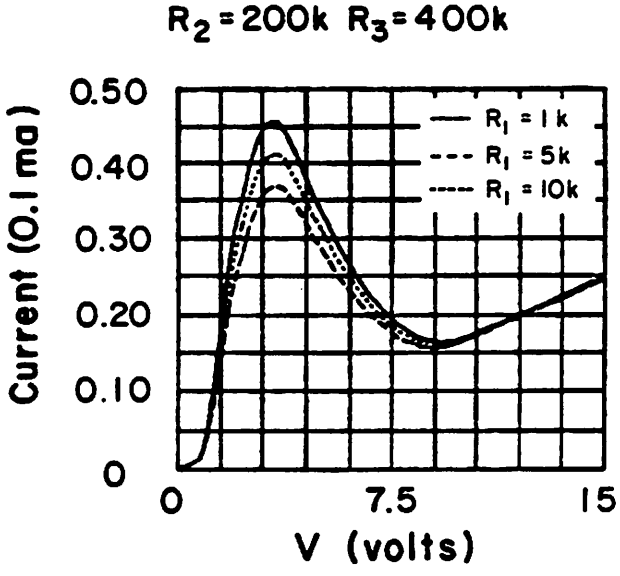
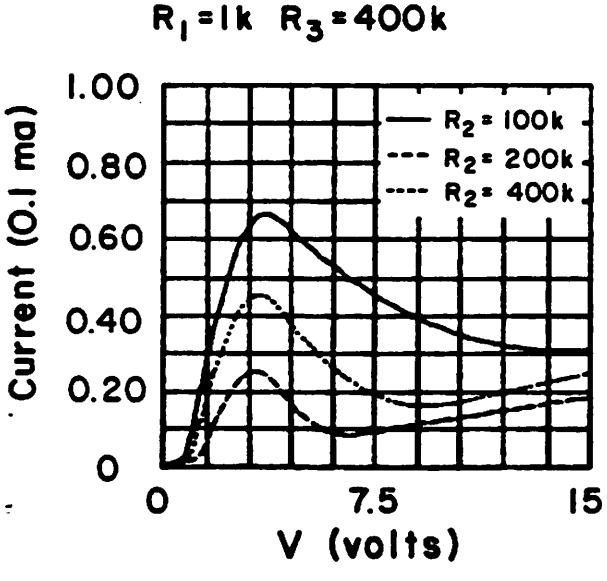

R1=100k R2=100k vto=6v
0.20
0.16
0.12
0.08
0.04
0
Current (ma)
0
7.5
15
V (volts)
R3 = 5k
R3 = 1k
R3 = 15k

Fig. A-32


i
+
V
-
R2
R1
T1
R3
T2


R2 = 200k R3 = 400k
Current (0.1 ma)
0.50
0.40
0.30
0.20
0.10
0
0
7.5
15
V (volts)
R1 = 1 k
R1 = 5k
R1 = 10k


R1 = 1k R3 = 400k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

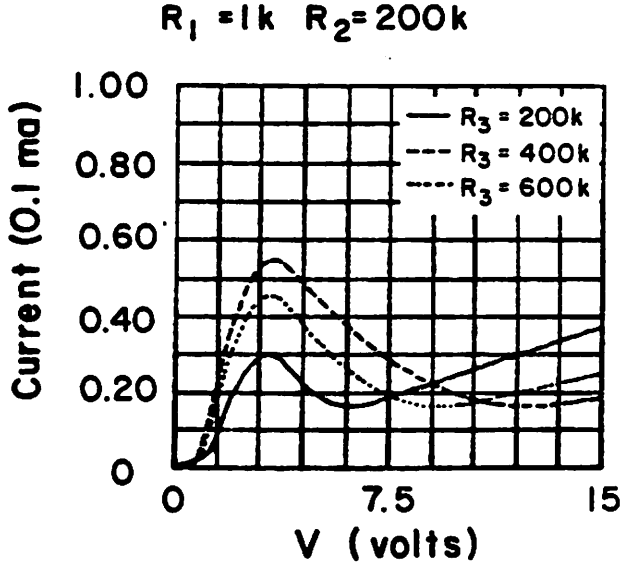
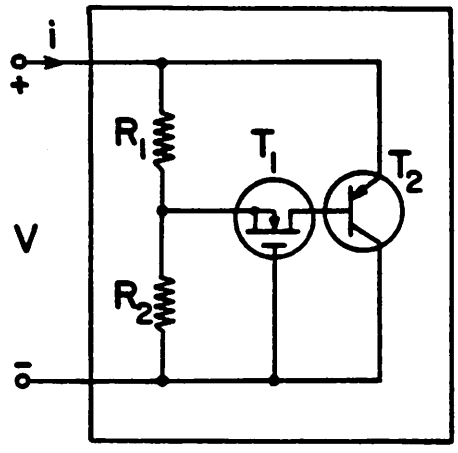
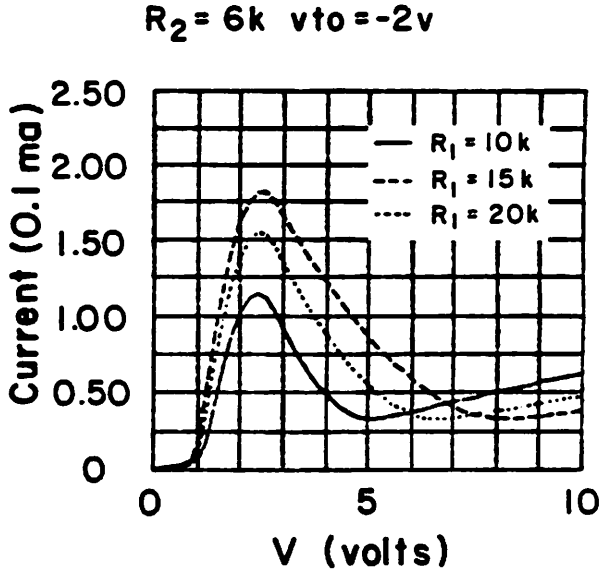

R1 = 1k R2 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R3 = 200k
R3 = 400k
R3 = 600k

Fig. A-33


i
+
R1
T1
T2
V
R2
-


R2 = 6k vto = -2v
Current (0.1 ma)
2.50
2.00
1.50
1.00
0.50
0
R1 = 10k
R1 = 15k
R1 = 20k
0
5
10
V (volts)

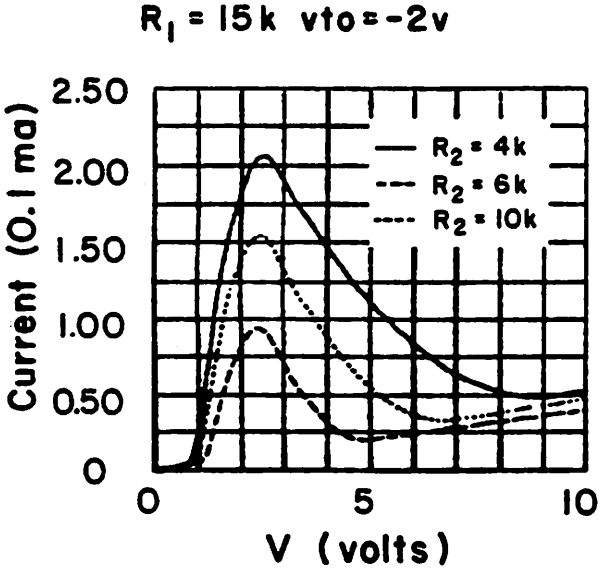
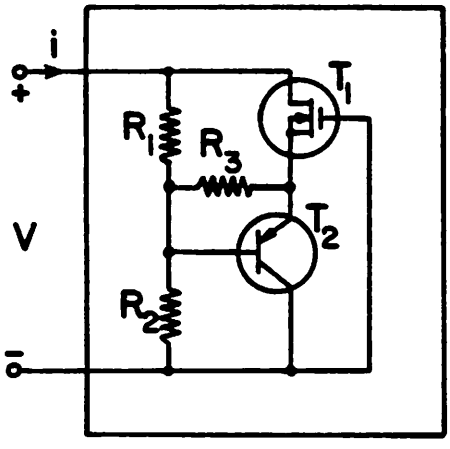
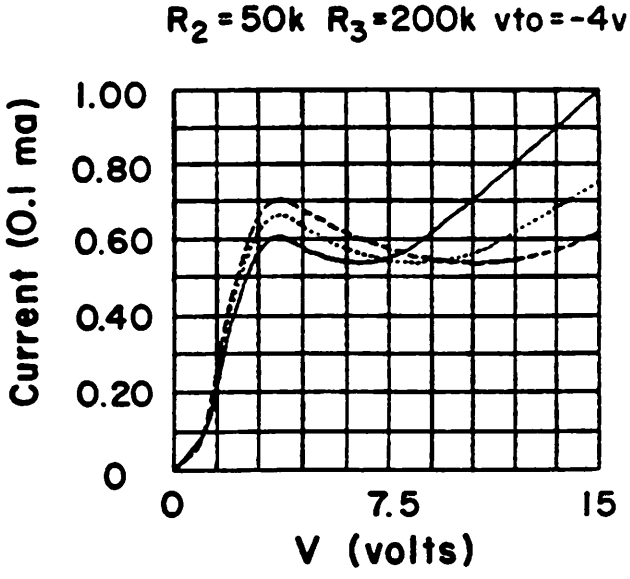
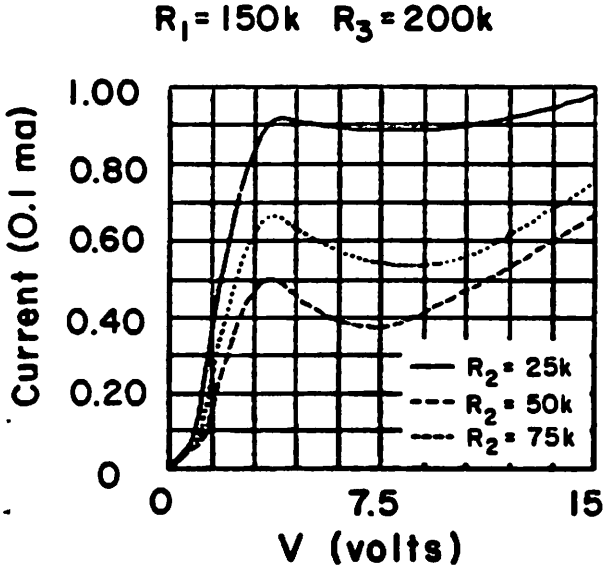

R1 = 15k vto = -2v
Current (0.1 ma)
2.50
2.00
1.50
1.00
0.50
0
R2 = 4k
R2 = 6k
R2 = 10k
0
5
10
V (volts)

Fig. A-34


i
+
V
−
R1
R3
R2
T1
T2


R2 = 50k R3 = 200k vto = -4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)


R1 = 150k R3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R2 = 25k
R2 = 50k
R2 = 75k

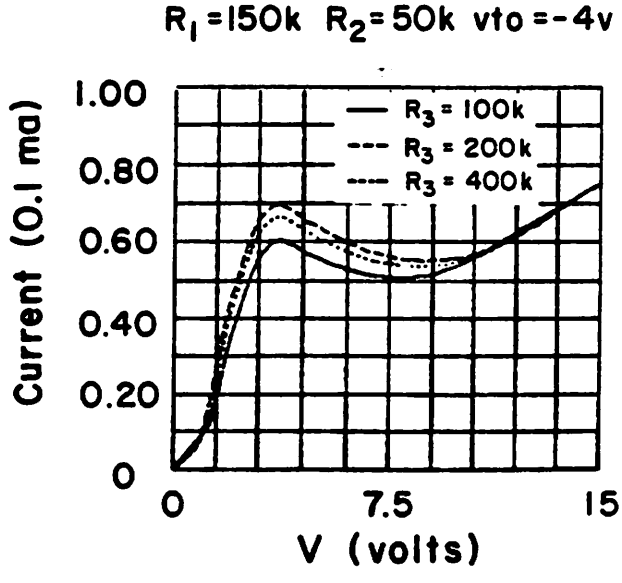
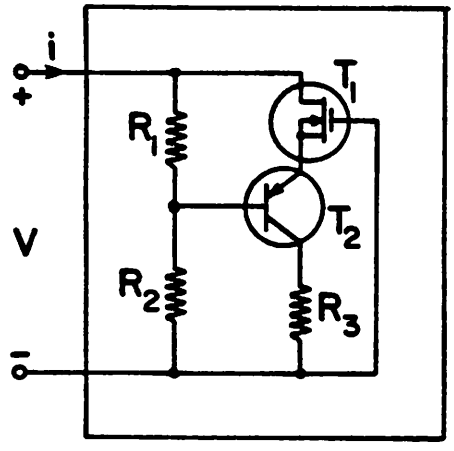
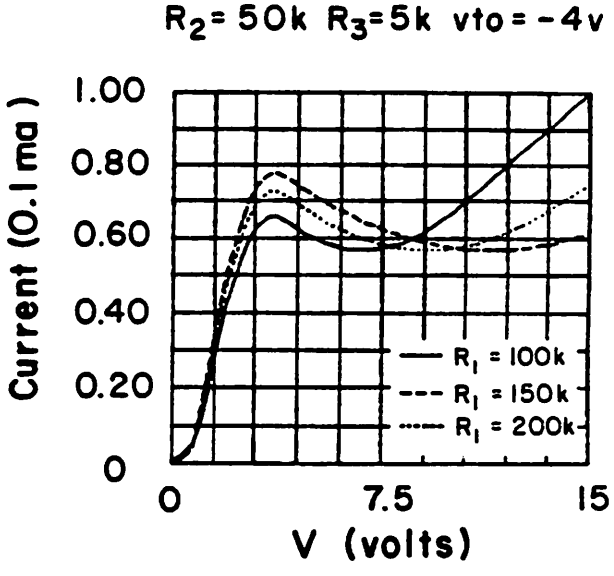
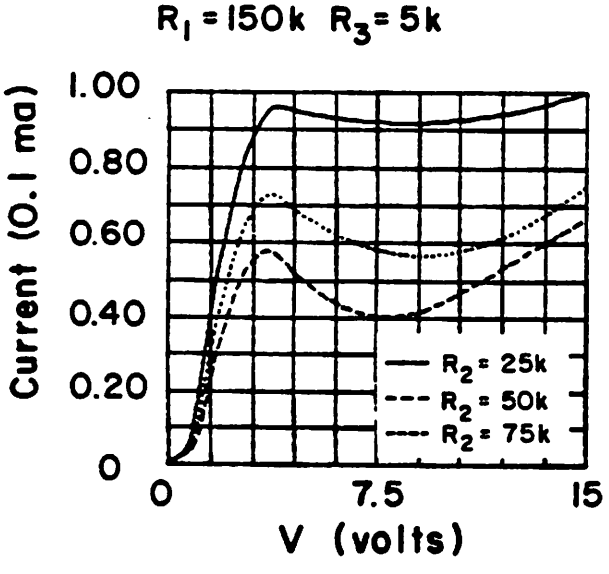

R1 = 150k R2 = 50k vto = -4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R3 = 100k
R3 = 200k
R3 = 400k

Fig. A-35


i
+
V
−
R1
R2
R3
T1
T2


R2 = 50k R3 = 5k vto = -4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R1 = 100k
R1 = 150k
R1 = 200k


R1 = 150k R3 = 5k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R2 = 25k
R2 = 50k
R2 = 75k

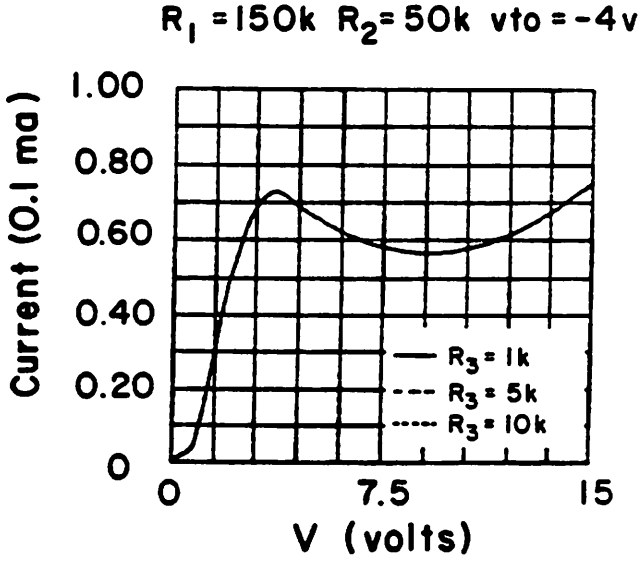
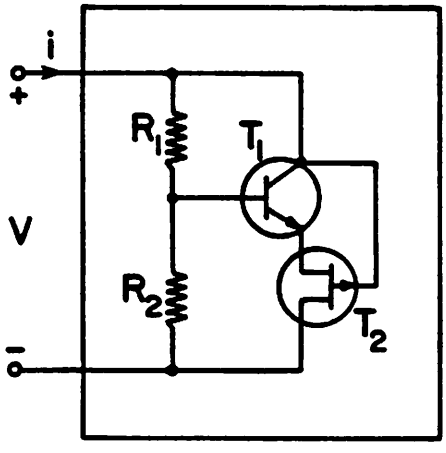
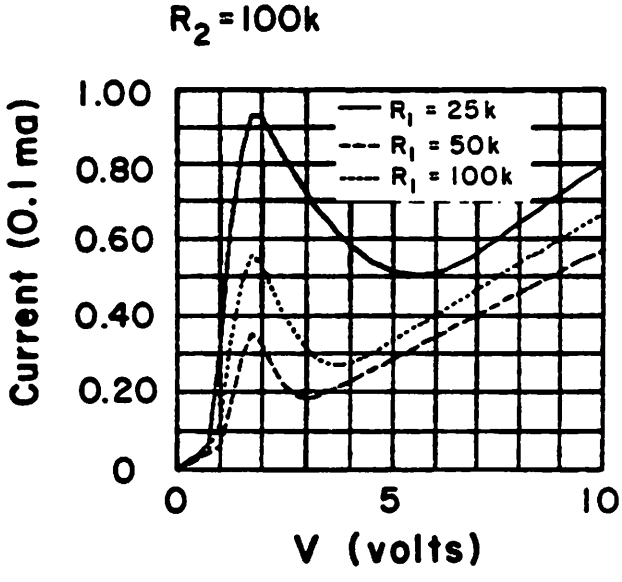

R1 = 150k R2 = 50k vto = -4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R3 = 1k
R3 = 5k
R3 = 10k

Fig. A-36


i
+
V
-
R1
T1
R2
T2


R2 = 100k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
5
10
V (volts)
R1 = 25k
R1 = 50k
R1 = 100k

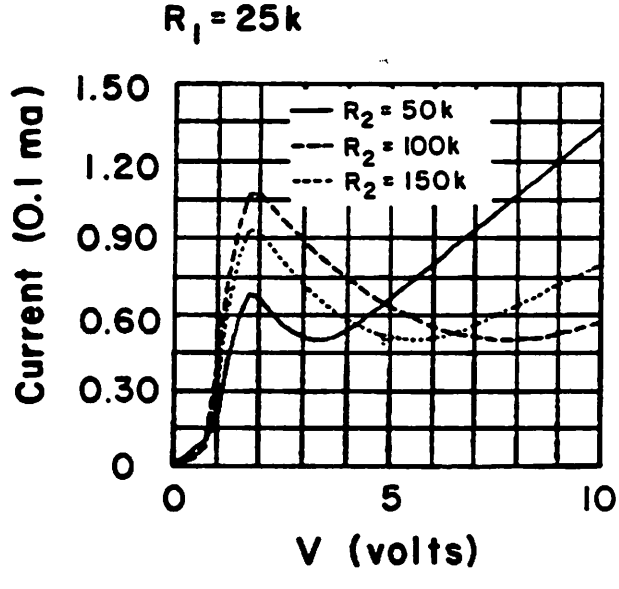
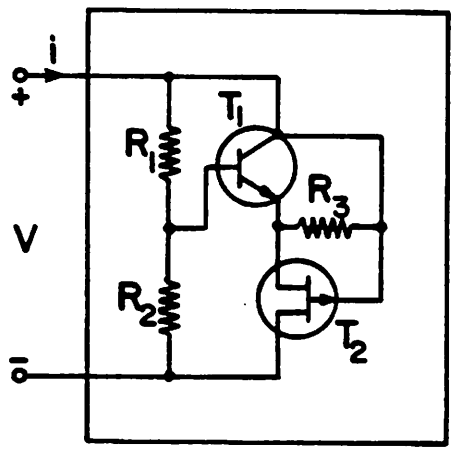
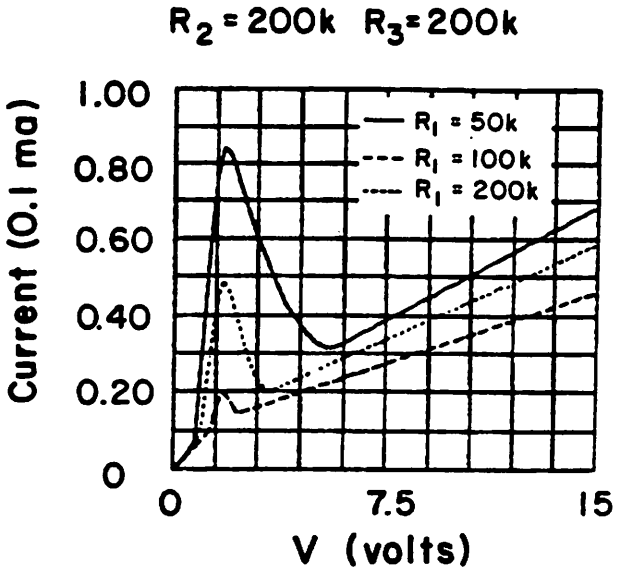
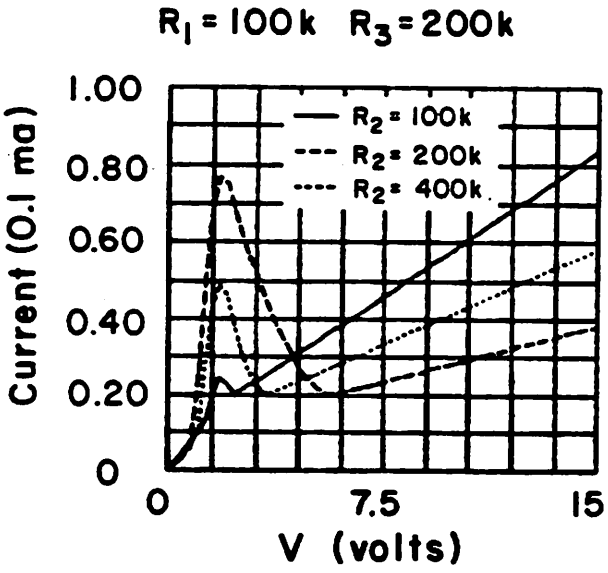

R1 = 25k
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
5
10
V (volts)
R2 = 50k
R2 = 100k
R2 = 150k

Fig. A-37


i
+
V
−
R_1
T_1
R_3
R_2
T_2


R_2 = 200k R_3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
R_1 = 50k
R_1 = 100k
R_1 = 200k
0
7.5
15
V (volts)


R_1 = 100k R_3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
R_2 = 100k
R_2 = 200k
R_2 = 400k
0
7.5
15
V (volts)

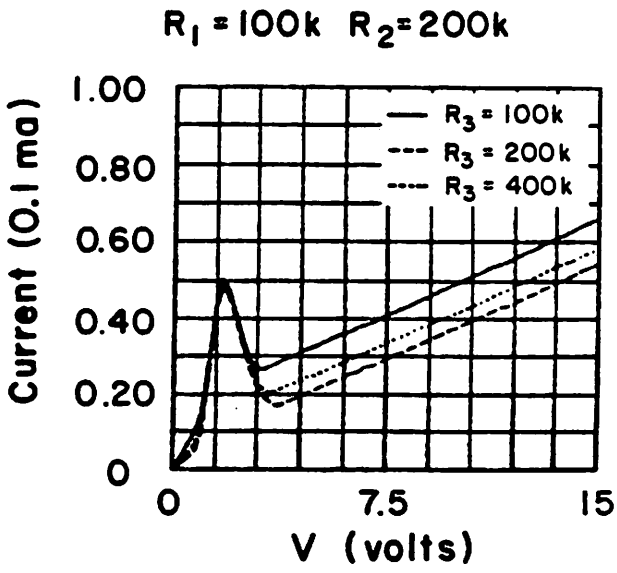
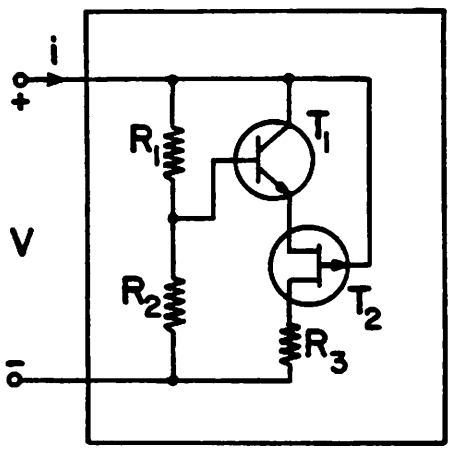
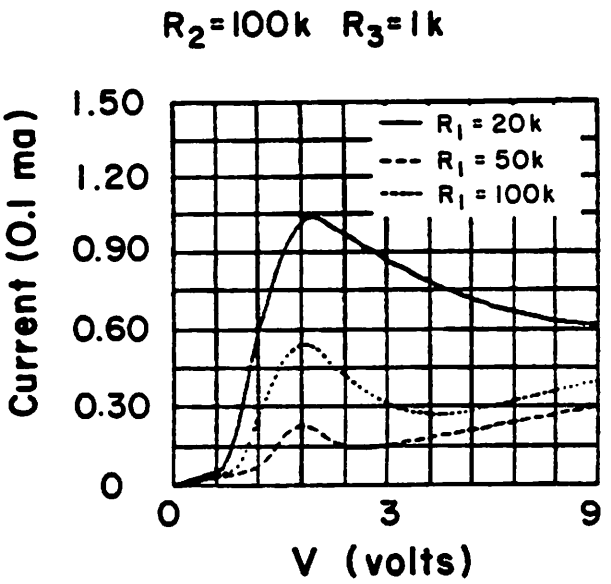
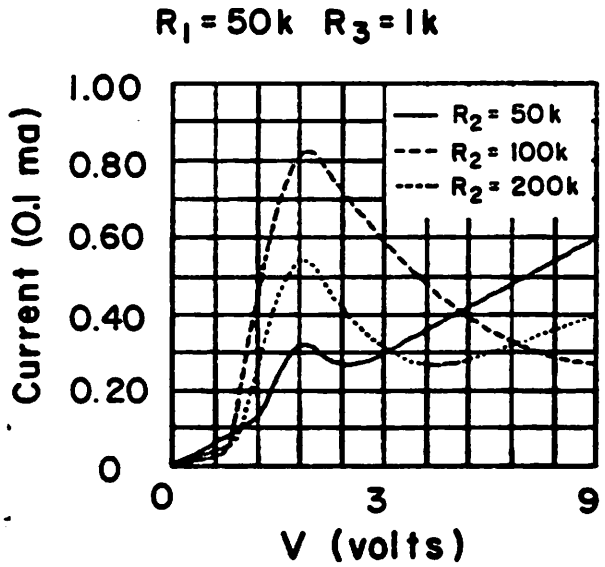

R_1 = 100k R_2 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
R_3 = 100k
R_3 = 200k
R_3 = 400k
0
7.5
15
V (volts)

Fig. A-38


i
+
V
−
R1
R2
R3
T1
T2


R2=100k R3=1k
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
3
9
V (volts)
R1 = 20k
R1 = 50k
R1 = 100k


R1 = 50k R3 = 1k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
3
9
V (volts)
R2 = 50k
R2 = 100k
R2 = 200k

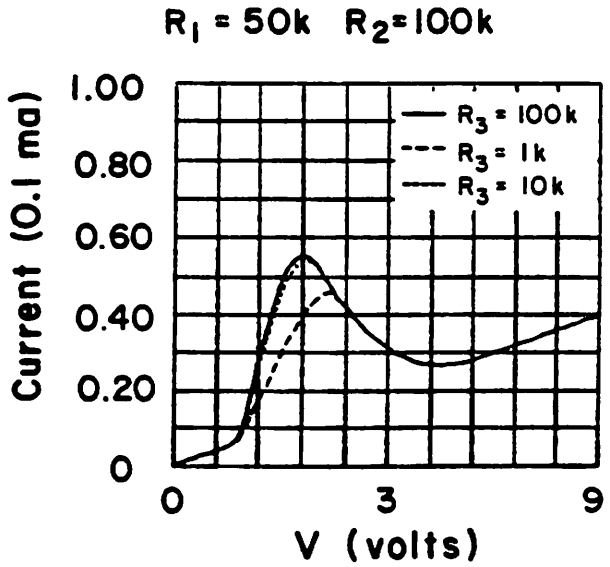
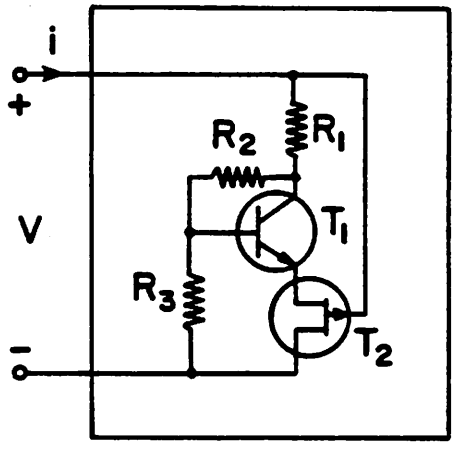
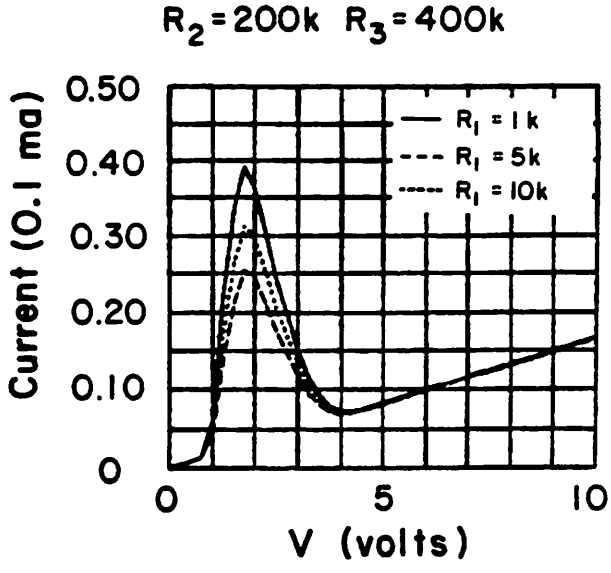
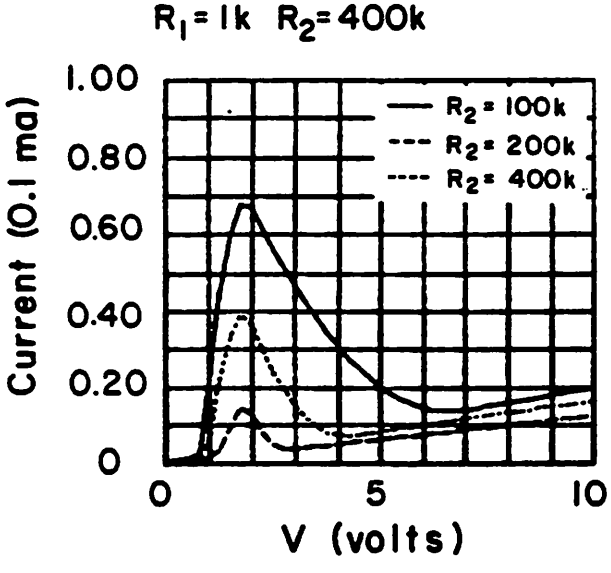

R1 = 50k R2=100k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
3
9
V (volts)
R3 = 100k
R3 = 1k
R3 = 10k

Fig. A-39


i
+
V
-
R2
R1
T1
R3
T2


R2 = 200k R3 = 400k
Current (0.1 ma)
0.50
0.40
0.30
0.20
0.10
0
0
5
10
V (volts)
R1 = 1k
R1 = 5k
R1 = 10k


R1 = 1k R2 = 400k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
5
10
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

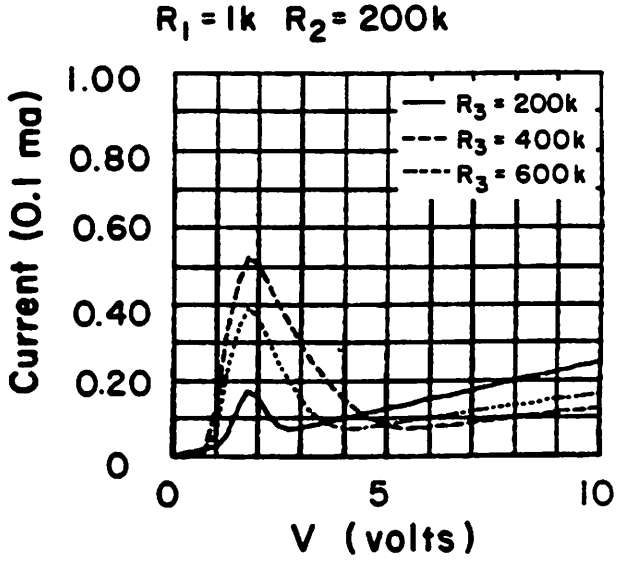
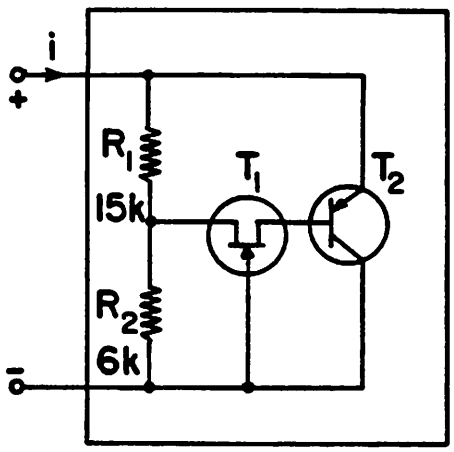
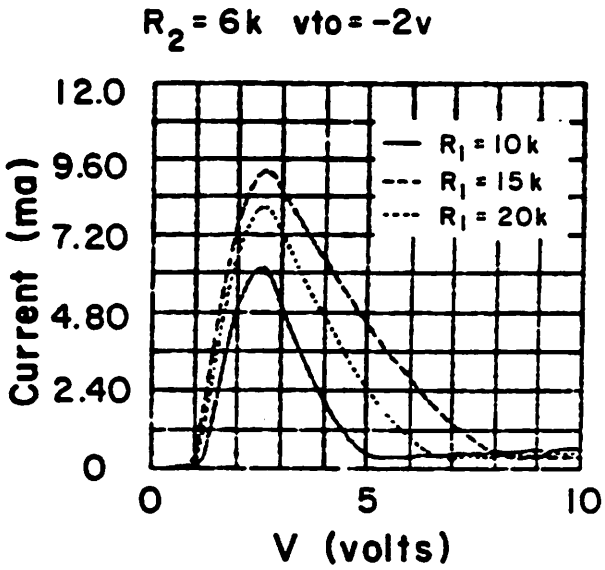

R1 = 1k R2 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
5
10
V (volts)
R3 = 200k
R3 = 400k
R3 = 600k

Fig. A-40


i
+
R1
15k
T1
T2
R2
6k
-


R2 = 6k vto = -2v
12.0
9.60
7.20
4.80
2.40
0
Current (ma)
R1 = 10k
R1 = 15k
R1 = 20k
0
5
10
V (volts)

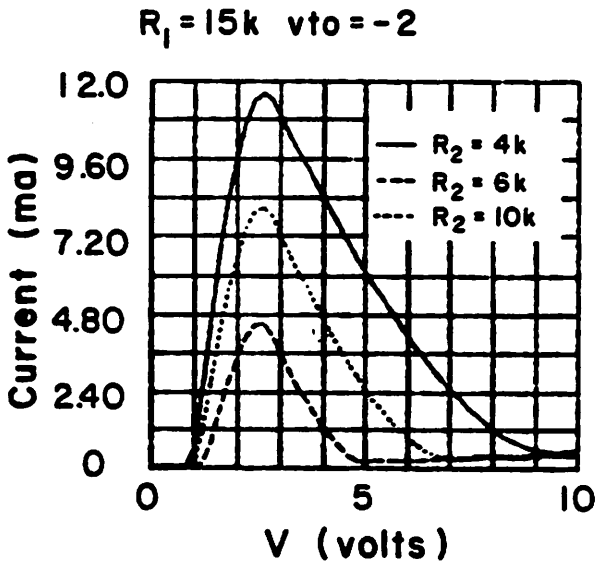
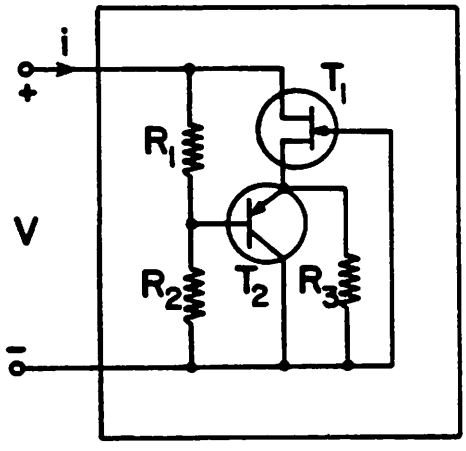
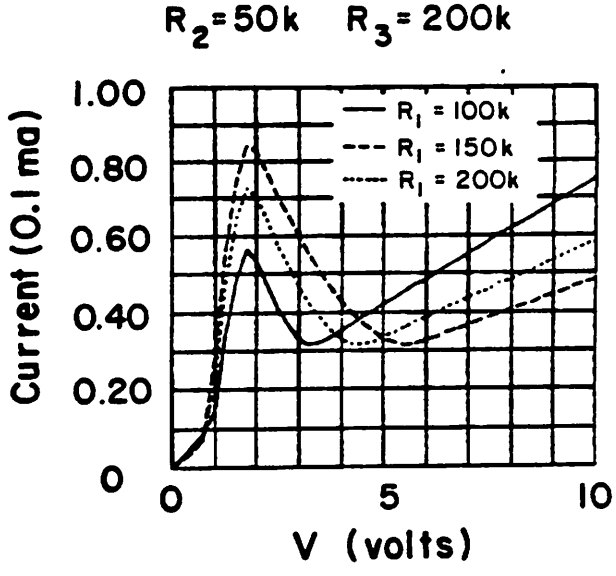
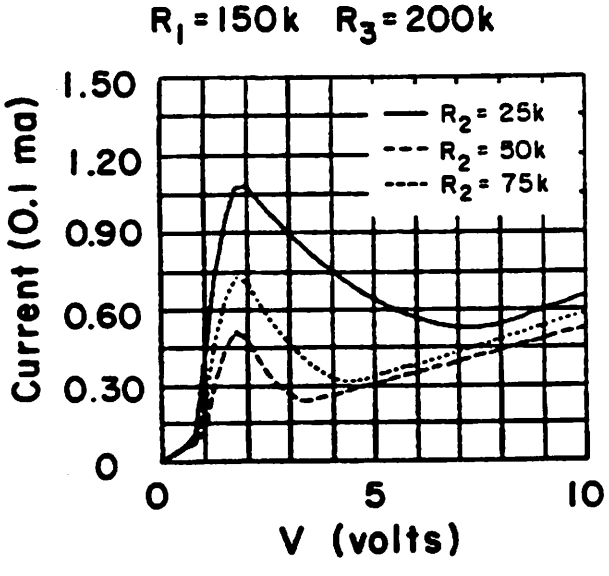

R1 = 15k vto = -2
12.0
9.60
7.20
4.80
2.40
0
Current (ma)
R2 = 4k
R2 = 6k
R2 = 10k
0
5
10
V (volts)

Fig. A-41


i
+
V
-
R_1
R_2
T_1
T_2
R_3


R_2=50k R_3=200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
5
10
V (volts)
R_1 = 100k
R_1 = 150k
R_1 = 200k


R_1 = 150k R_3 = 200k
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
5
10
V (volts)
R_2 = 25k
R_2 = 50k
R_2 = 75k

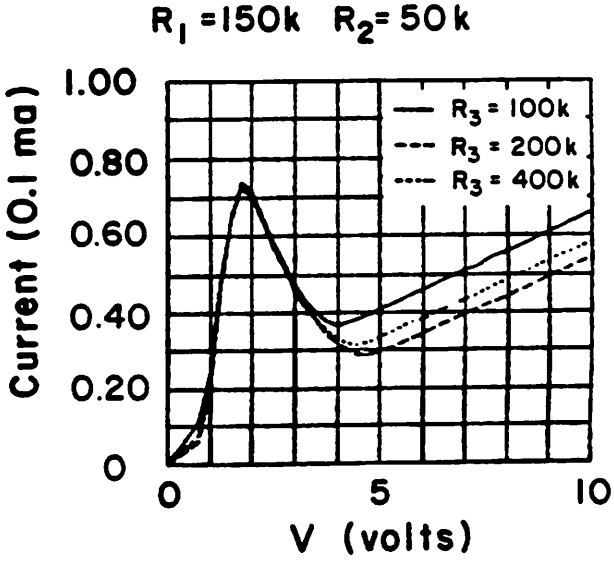
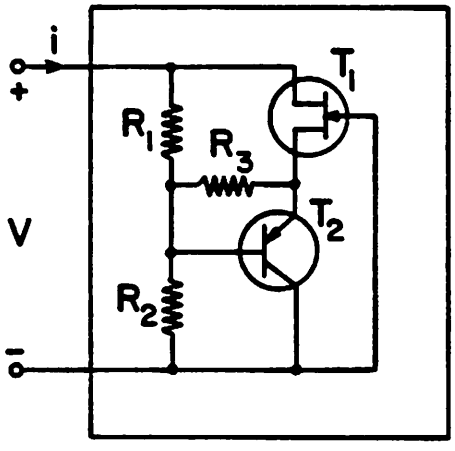
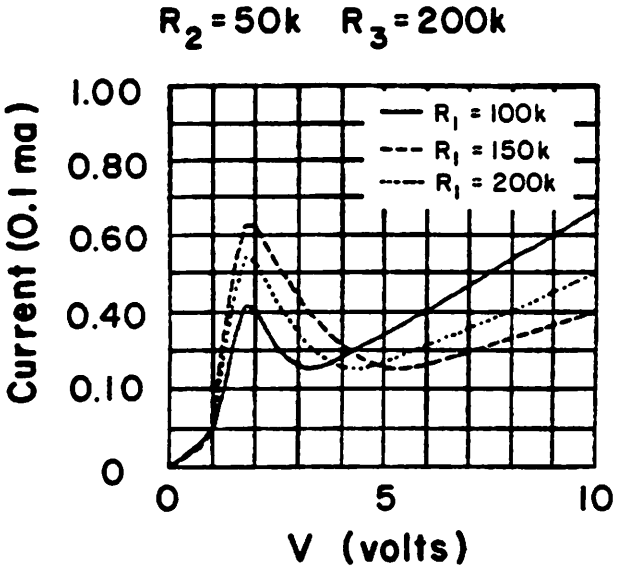
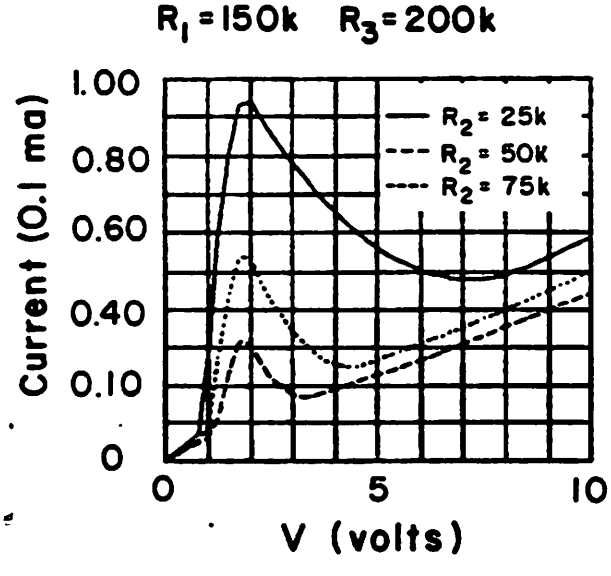

R_1 = 150k R_2 = 50k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
5
10
V (volts)
R_3 = 100k
R_3 = 200k
R_3 = 400k

Fig. A-42


i
+
V
−
R1
R3
R2
T1
T2


R2 = 50k R3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R1 = 100k
R1 = 150k
R1 = 200k


R1 = 150k R3 = 200k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R2 = 25k
R2 = 50k
R2 = 75k

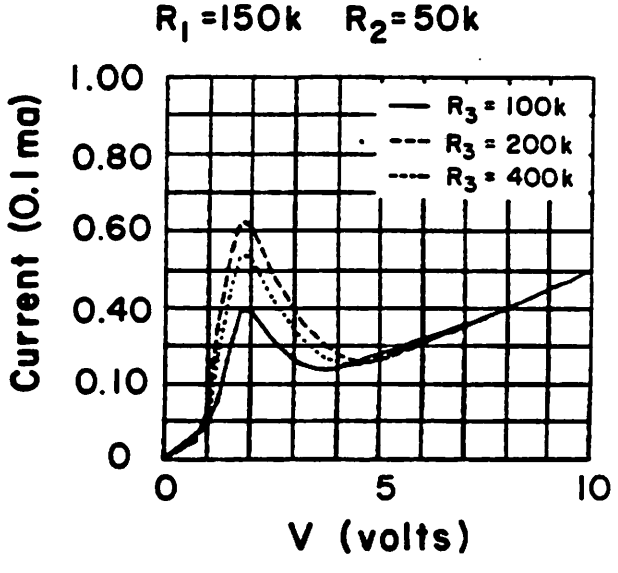

R1 = 150k R2 = 50k
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R3 = 100k
R3 = 200k
R3 = 400k

Fig. A-43

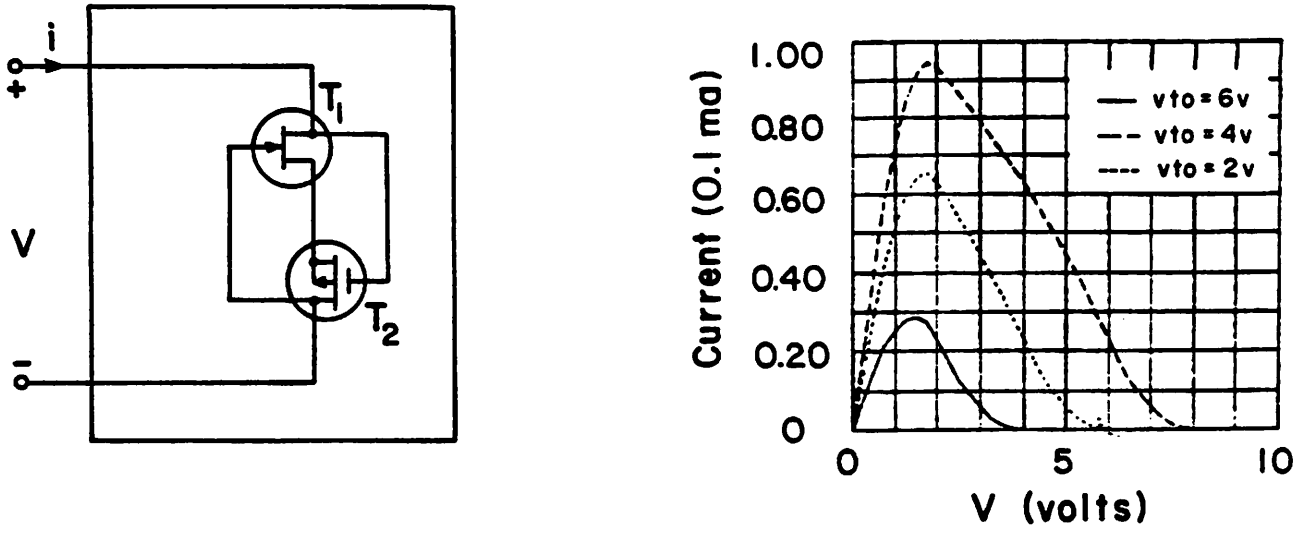
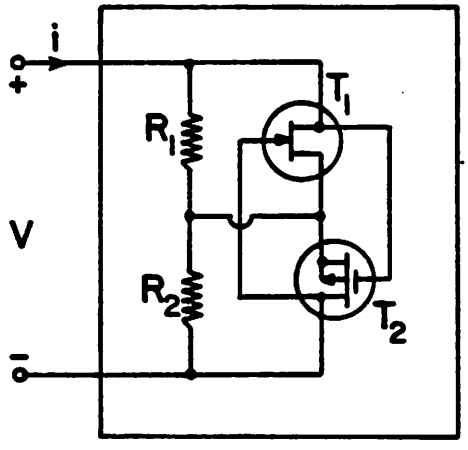
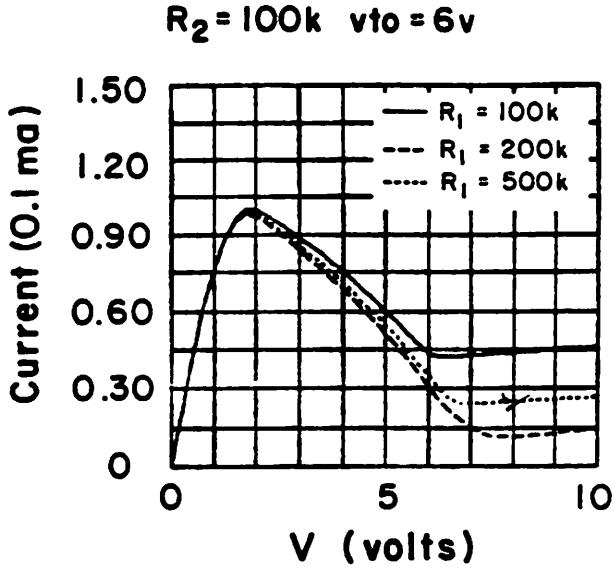

i
+
V
−
T1
T2
1.00
0.80
0.60
0.40
0.20
0
Current (0.1 ma)
vto = 6v
vto = 4v
vto = 2v
0
5
10
V (volts)

Fig. A-44


i
+
V
-
R1
R2
T1
T2


R2 = 100k vto = 6v
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
5
10
V (volts)
R1 = 100k
R1 = 200k
R1 = 500k

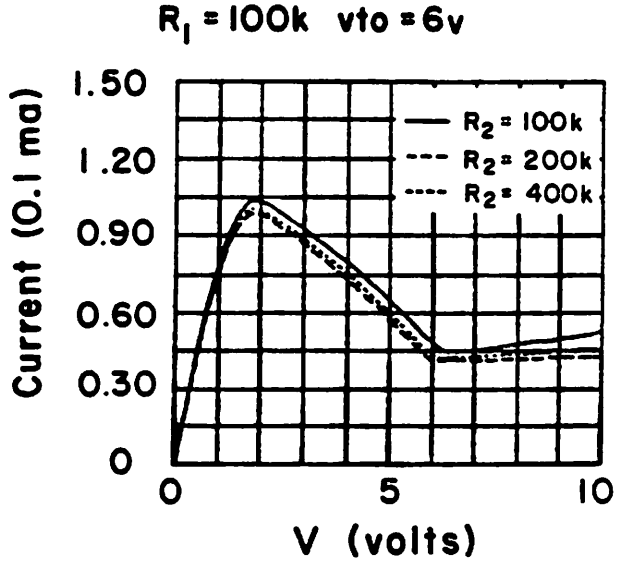
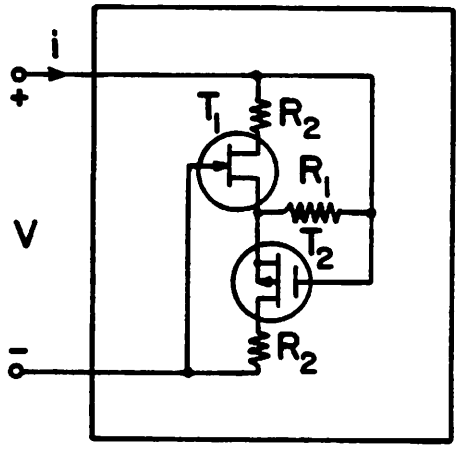
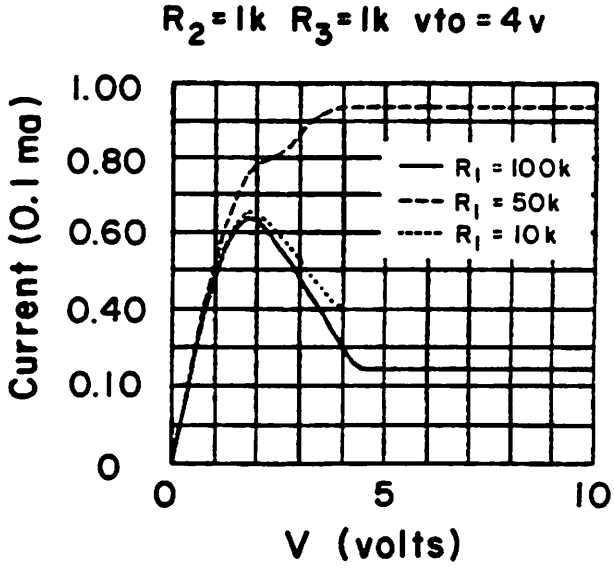
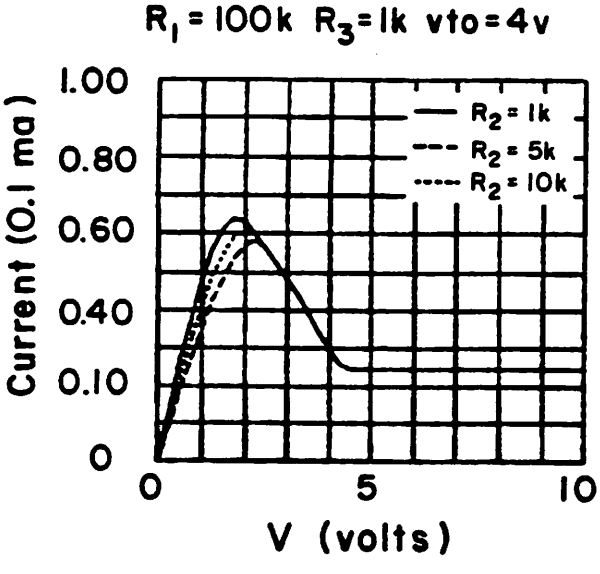

R1 = 100k vto = 6v
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
5
10
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

Fig. A-45


i
+
V
−
T1
R2
R1
T2
R2


R2 = 1k R3 = 1k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R1 = 100k
R1 = 50k
R1 = 10k


R1 = 100k R3 = 1k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R2 = 1k
R2 = 5k
R2 = 10k

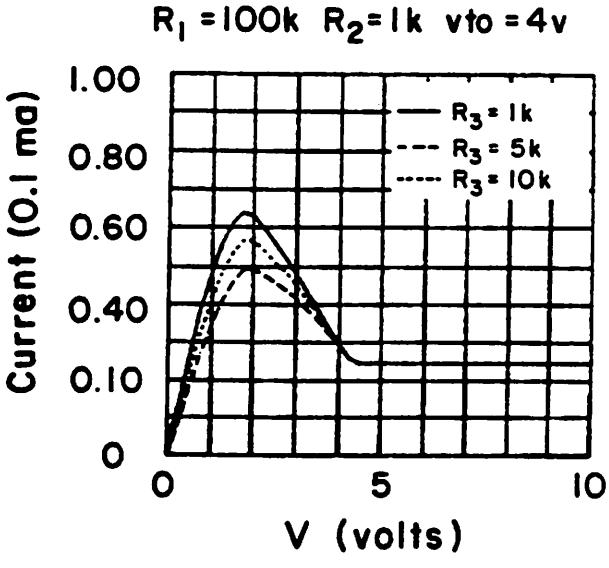
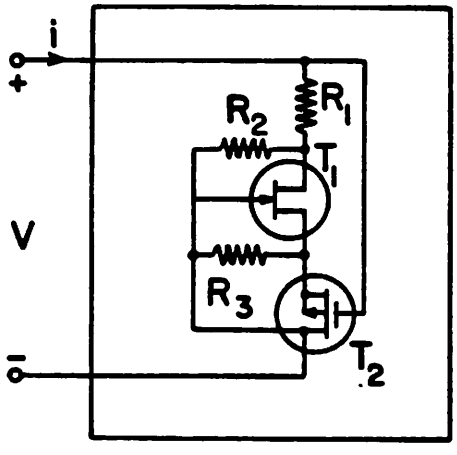
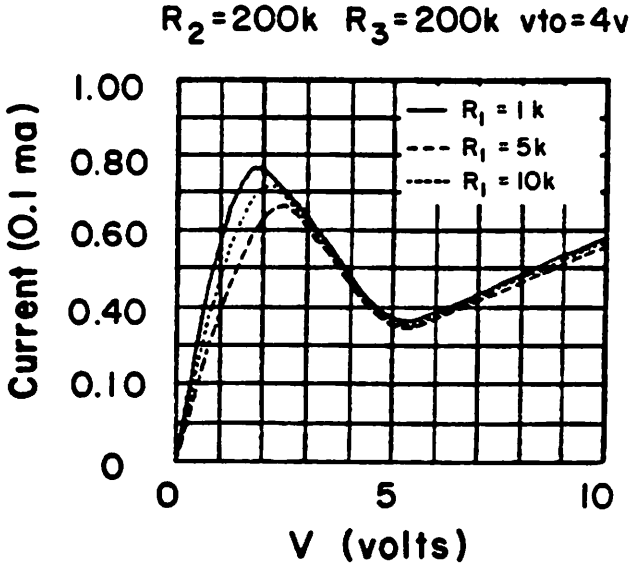
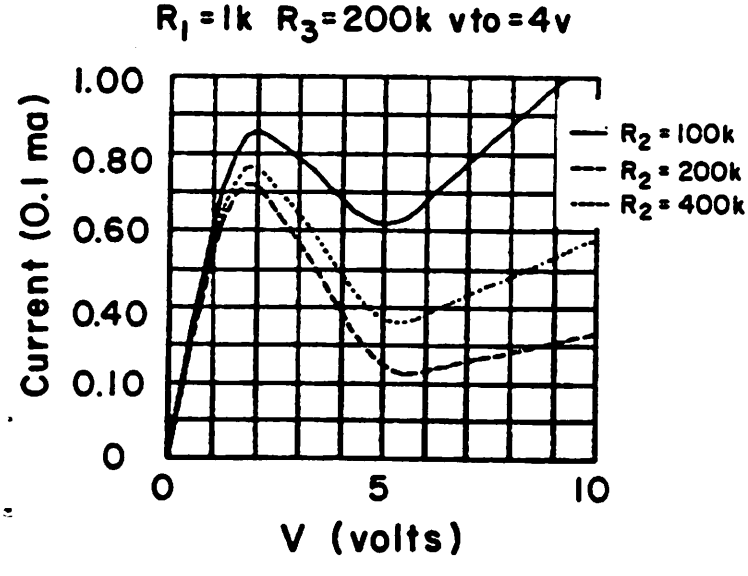

R1 = 100k R2 = 1k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R3 = 1k
R3 = 5k
R3 = 10k

Fig. A-46


i
+
V
-
R2
R1
T1
R3
T2


R2=200k R3=200k vto=4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R1 = 1k
R1 = 5k
R1 = 10k


R1 = 1k R3=200k vto=4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

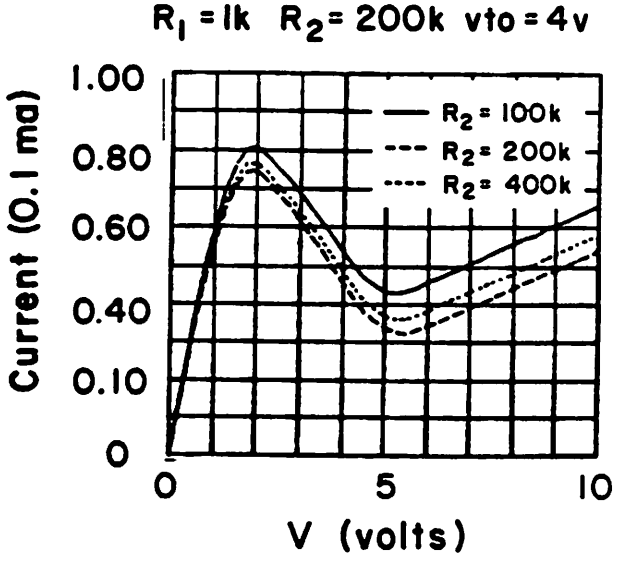

R1 = 1k R2= 200k vto = 4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.10
0
0
5
10
V (volts)
R2 = 100k
R2 = 200k
R2 = 400k

Fig. A-47

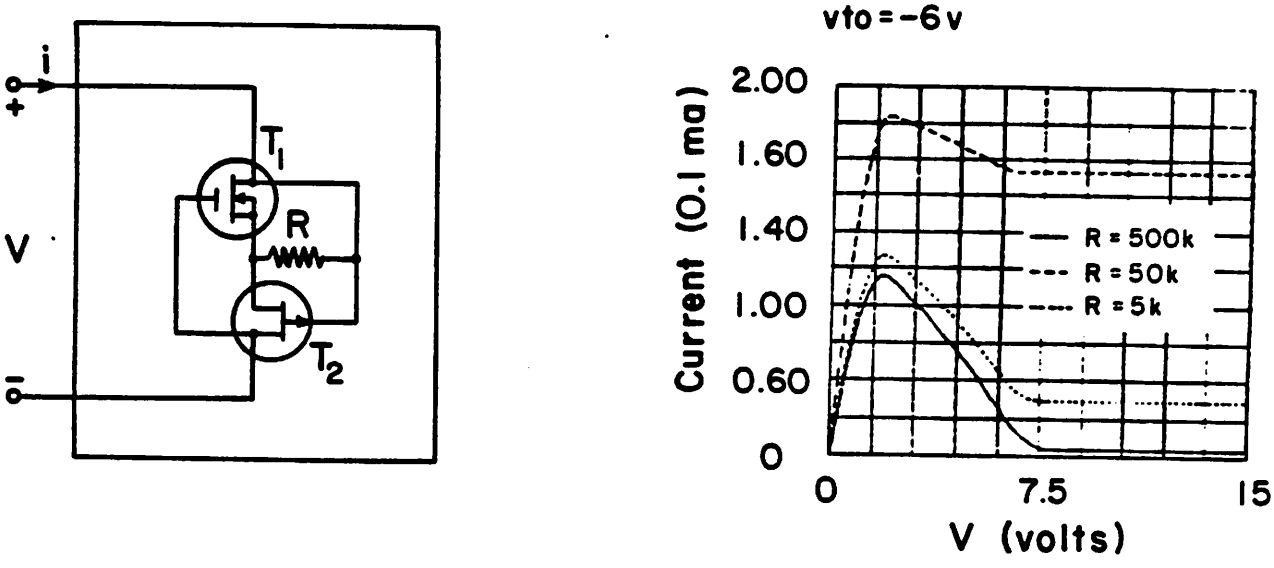
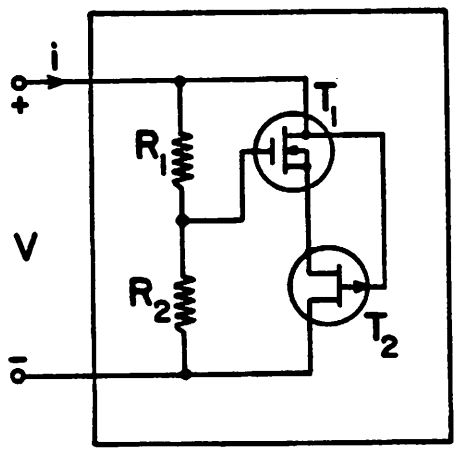
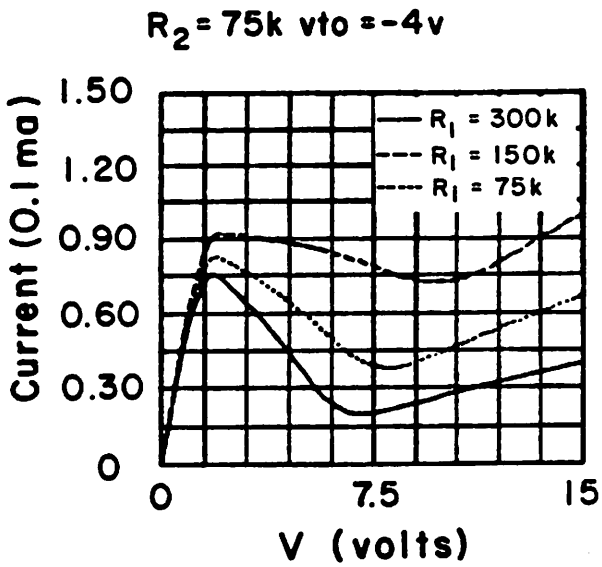

i
+
V
−
T_1
R
T_2
vto = −6v
Current (0.1 ma)
2.00
1.60
1.40
1.00
0.60
0
R = 500k
R = 50k
R = 5k
0
7.5
15
V (volts)

Fig. A-48


i
+
V
-
R1
R2
T1
T2


R2 = 75k vto = -4v
Current (0.1 ma)
1.50
1.20
0.90
0.60
0.30
0
0
7.5
15
V (volts)
R1 = 300k
R1 = 150k
R1 = 75k

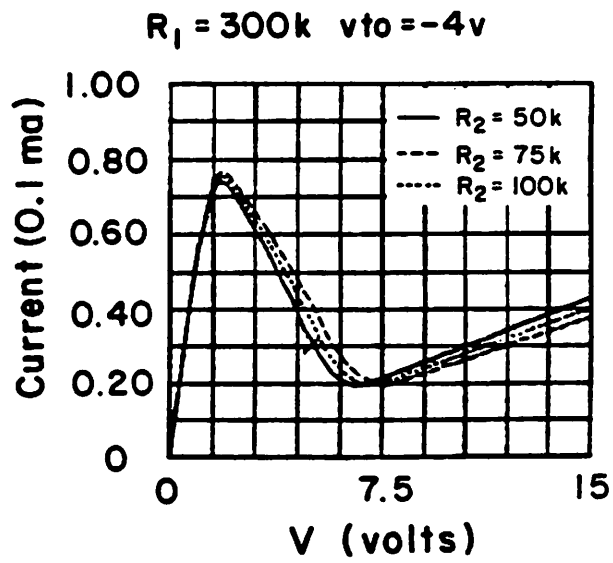
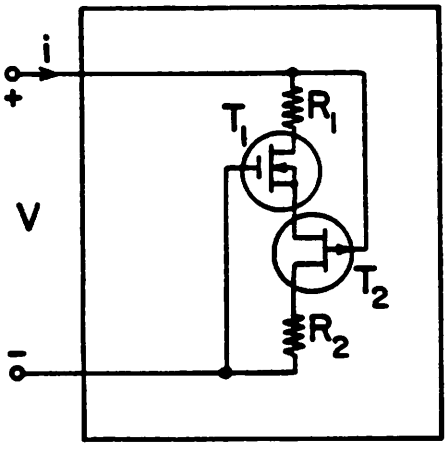
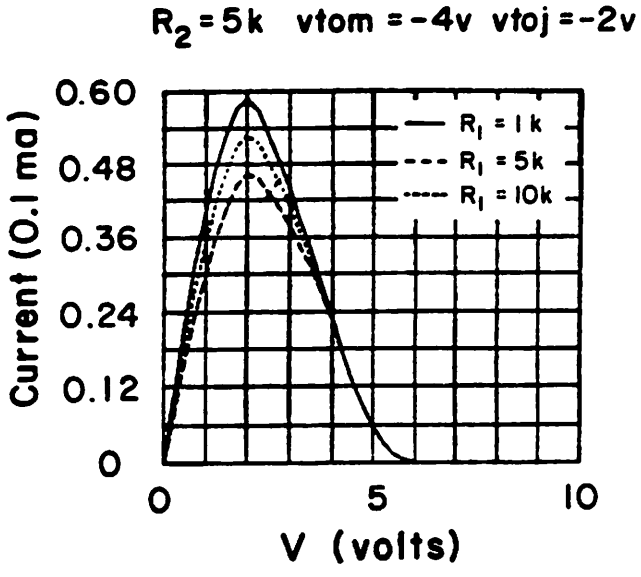

R1 = 300k vto = -4v
Current (0.1 ma)
1.00
0.80
0.60
0.40
0.20
0
0
7.5
15
V (volts)
R2 = 50k
R2 = 75k
R2 = 100k

Fig. A-49


i
+
V
-
T1
R1
T2
R2


R2 = 5k vtom = -4v vtoj = -2v
Current (0.1 ma)
0.60
0.48
0.36
0.24
0.12
0
0
5
10
V (volts)
R1 = 1k
R1 = 5k
R1 = 10k

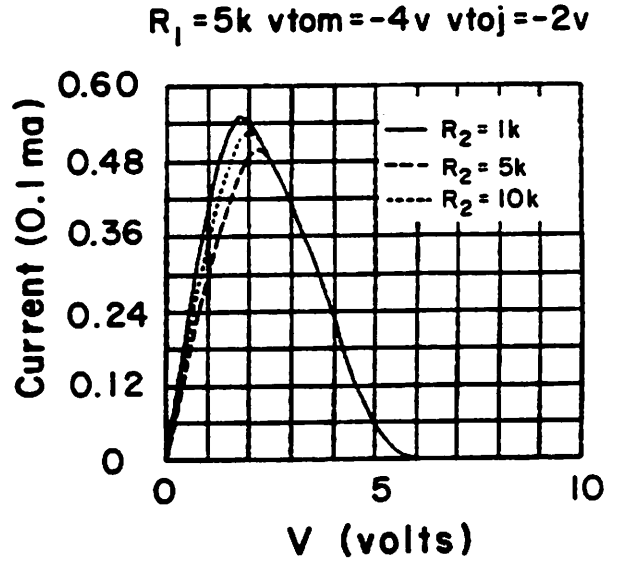
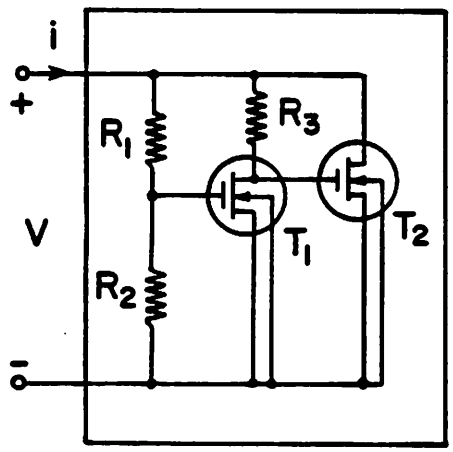
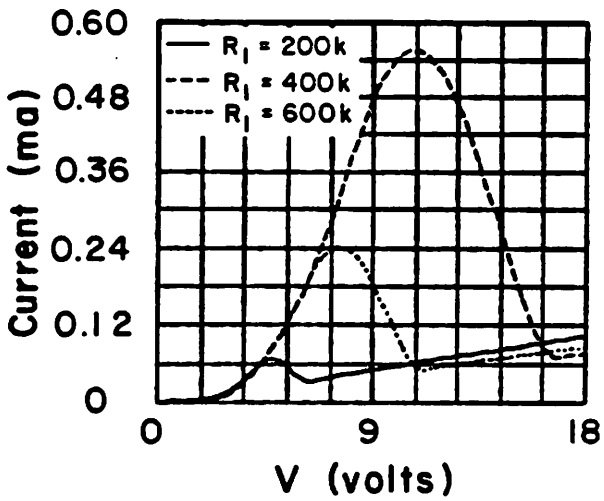

R1 = 5k vtom = -4v vtoj = -2v
Current (0.1 ma)
0.60
0.48
0.36
0.24
0.12
0
0
5
10
V (volts)
R2 = 1k
R2 = 5k
R2 = 10k

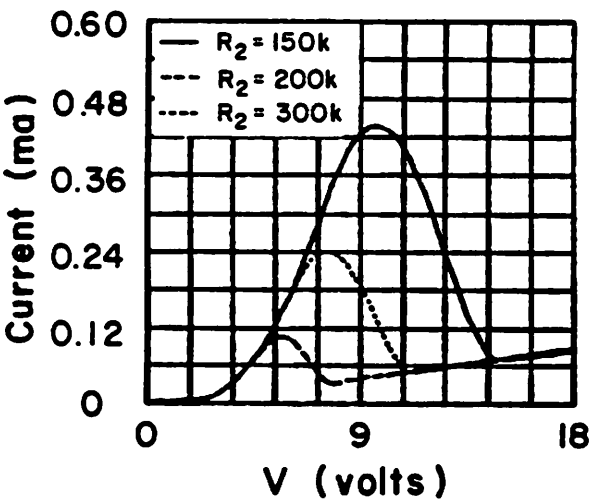
Fig. A-50



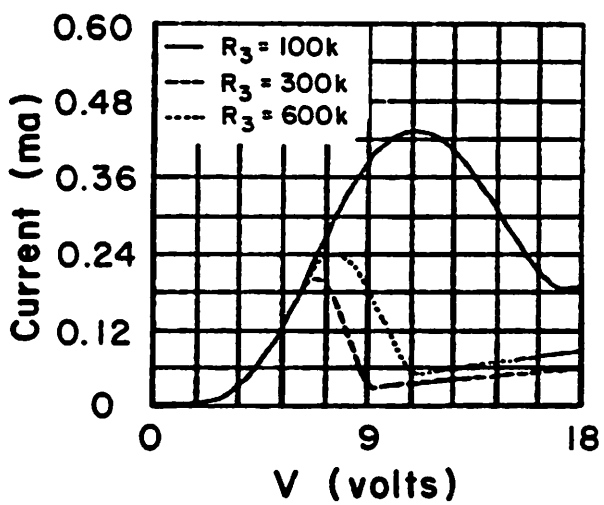
R_2=200k R_3=300k vto1=vto2=2v



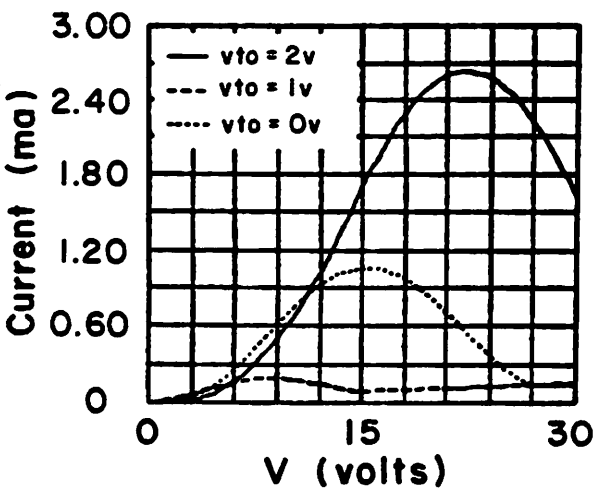
R_1=400k R_3=300k vto1=vto2=2v



R_1=400k R_2=200k vto1=vto2=2v



R_1=600k R_2=100k R_3=300k



R_1=500k R_2=50k R_3=180k

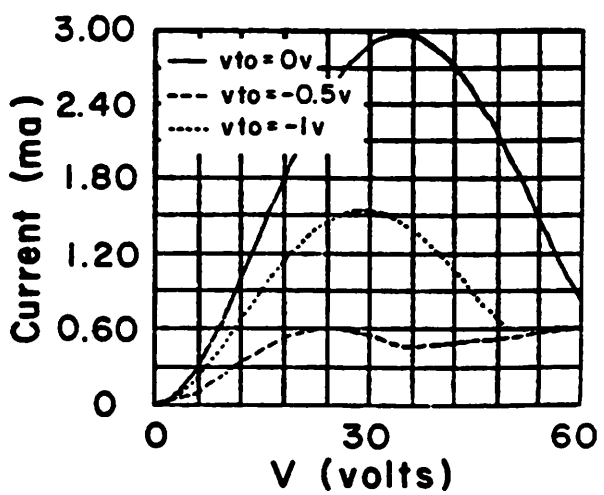
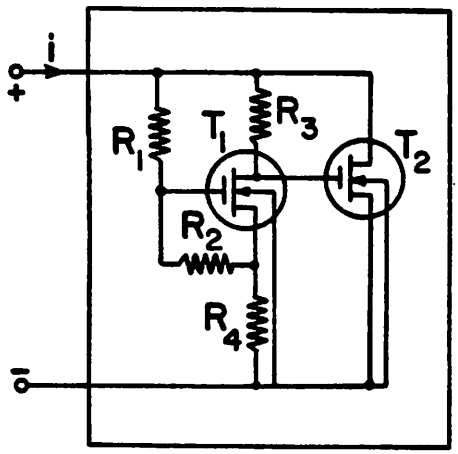
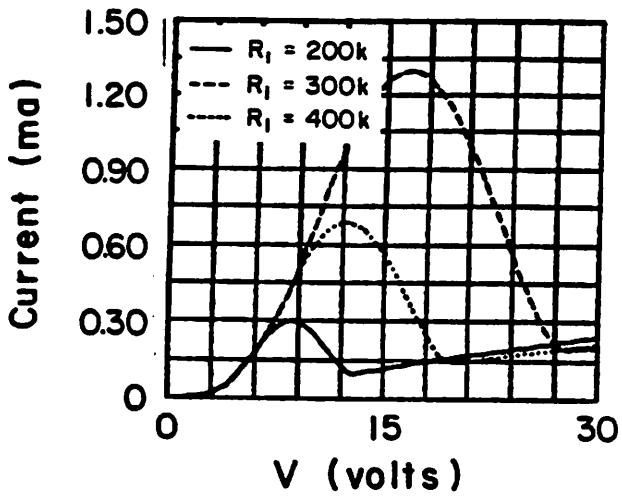


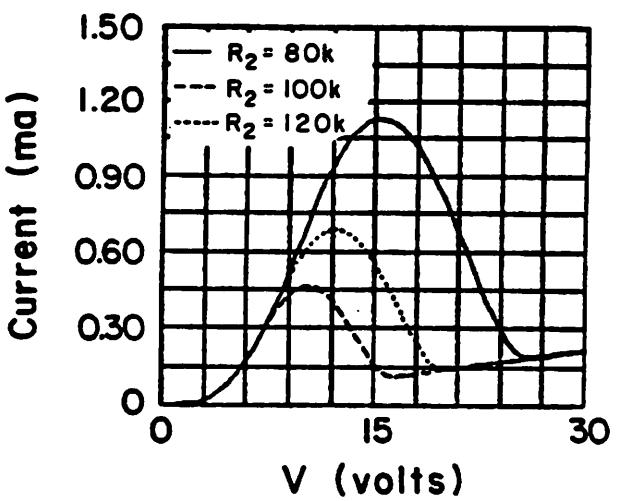
Fig. A-51



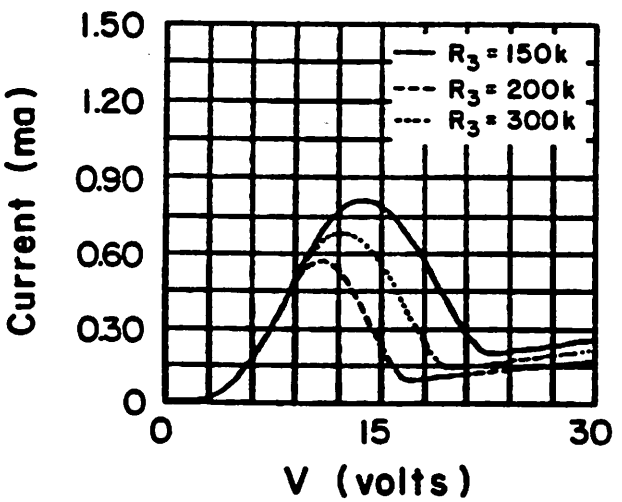
R_2 = 100k R_3 = 200k R_4 = 1k vtol = vto2 = 2v



R_1 = 300k R_3 = 200k R_4 = 1k vtol = vto2 = 2v



R_1 = 300k R_2 = 100k R_4 = 1k vtol = vto2 = 2v



R_1 = 300k R_2 = 100k R_3 = 200k vtol = vto2 = 2v

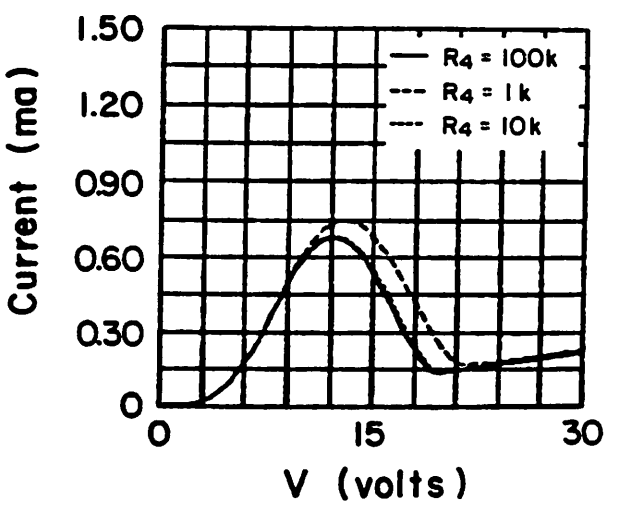
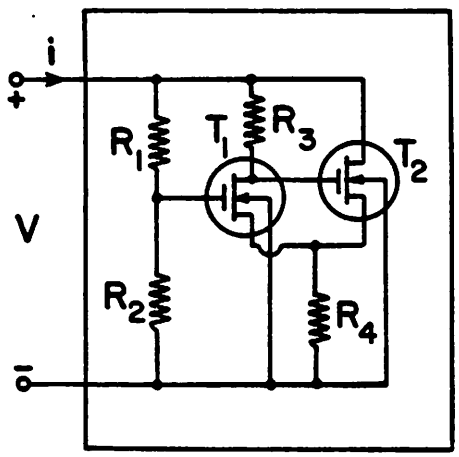
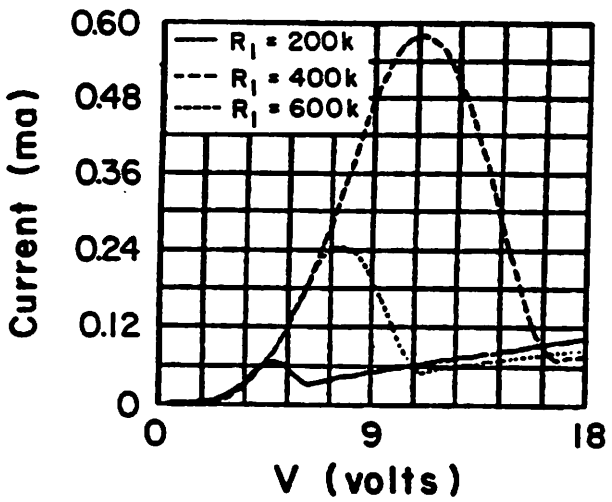


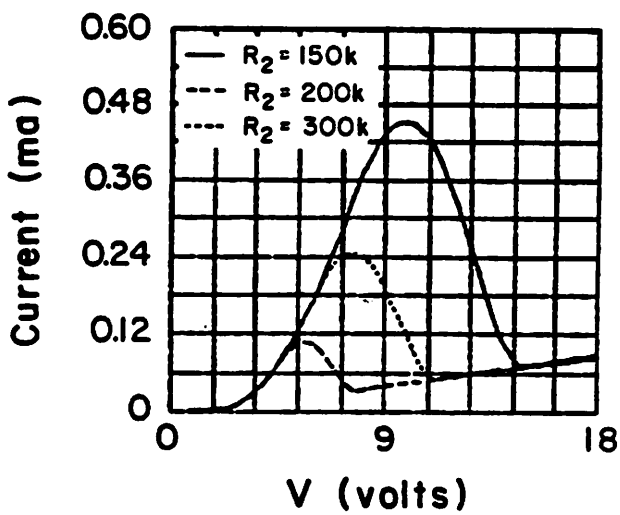
Fig. A-52



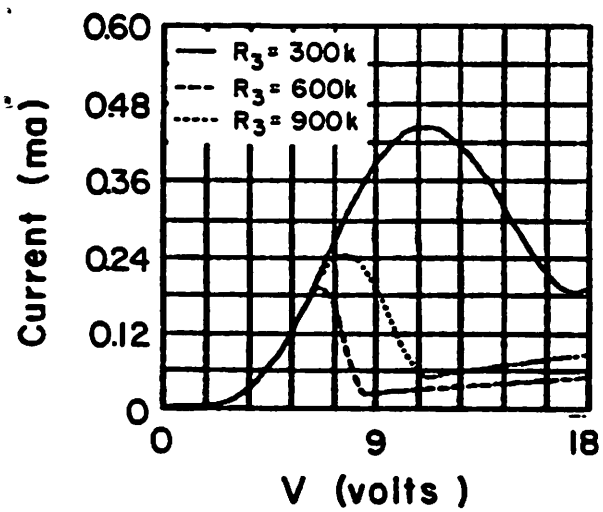
R_2=200k R_3=300k R_4=100k vtol=vto2=2v



R_1=400k R_3=300k R_4=100k vtol=vto2=2v



R_1=400k R_2=200k R_4=100k vtol=vto2=2v



R_1=400k R_2=200k R_3=300k vtol=vto2=2v

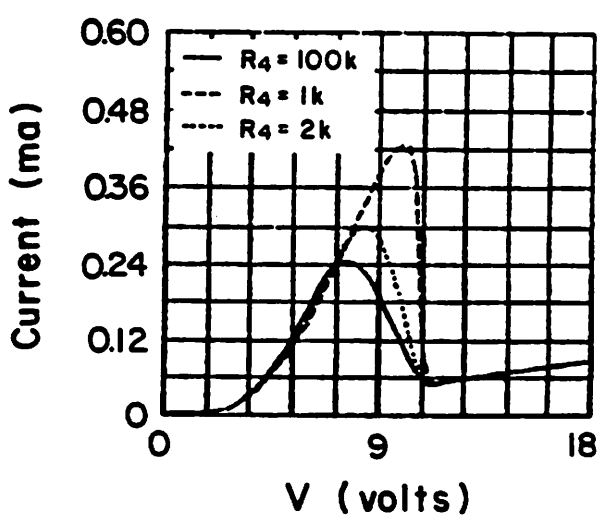
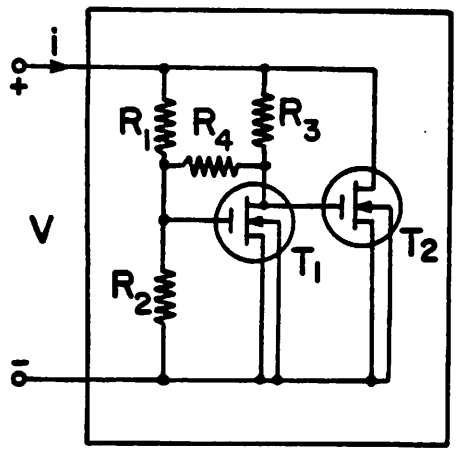
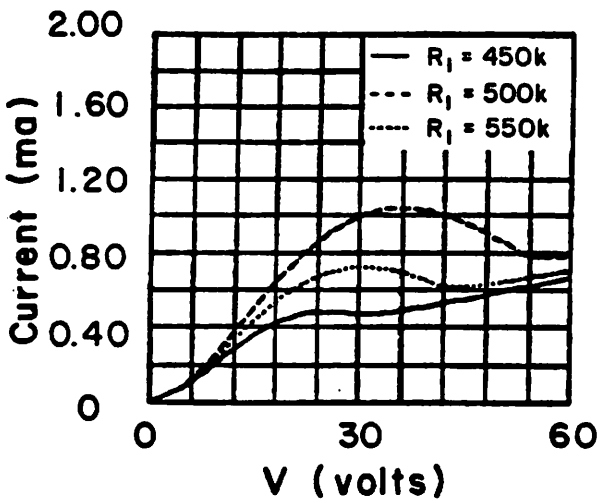


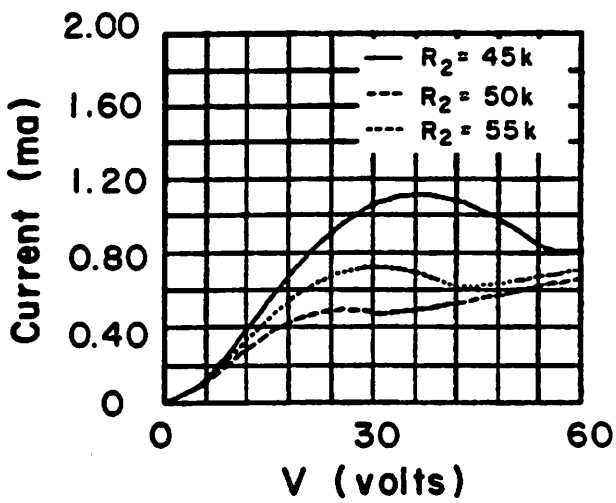
Fig. A-53



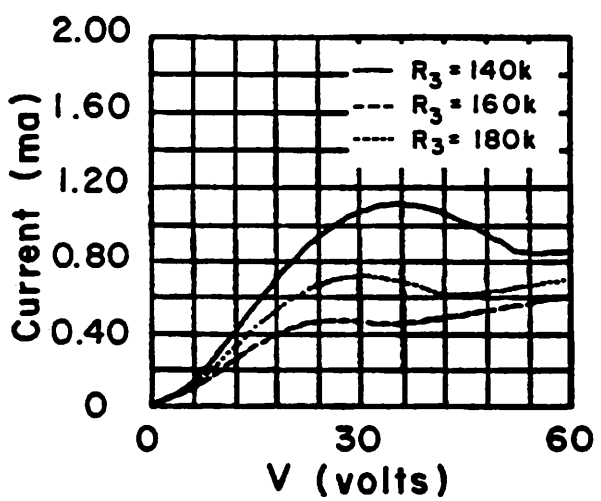
R_2=50k R_3=160k R_4=1.5meg vto=-1v



R_1=500k R_3=160k R_4=1.5meg vto=-1v



R_1=500k R_2=50k R_4=1.5meg vto=-1v



R_1=500k R_2=50k R_3=160k vto=-1v

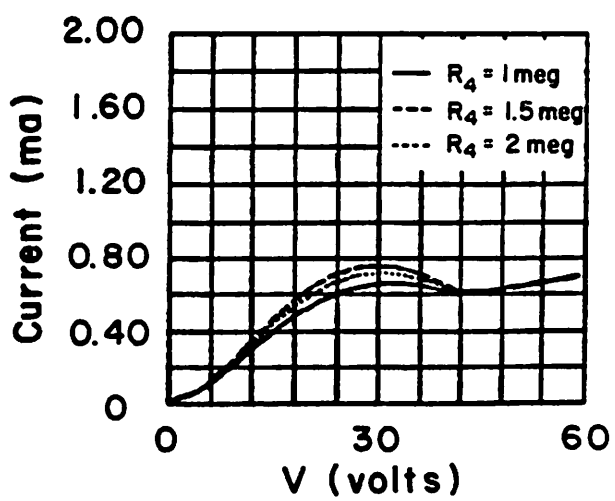
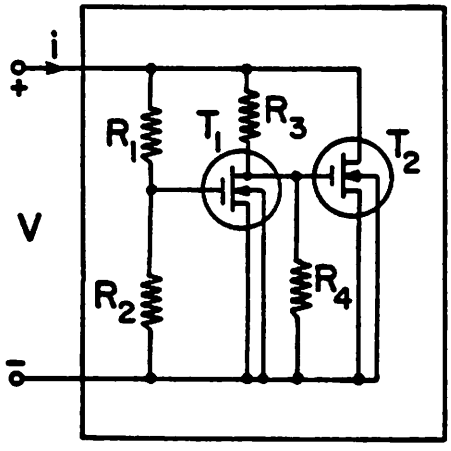
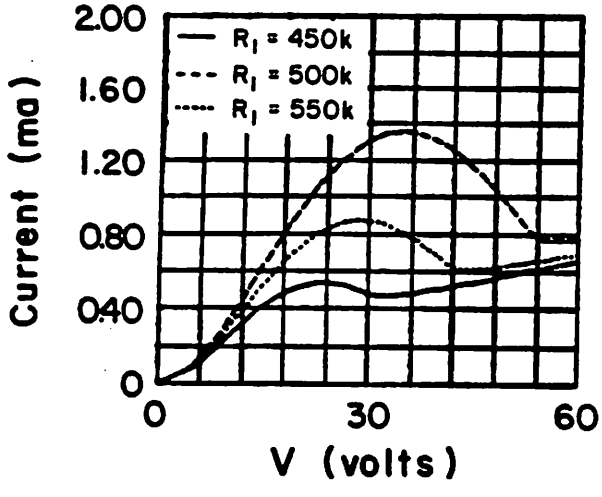


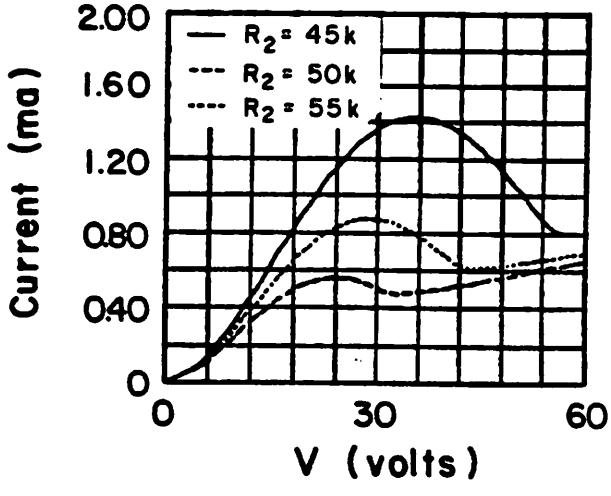
Fig. A-54



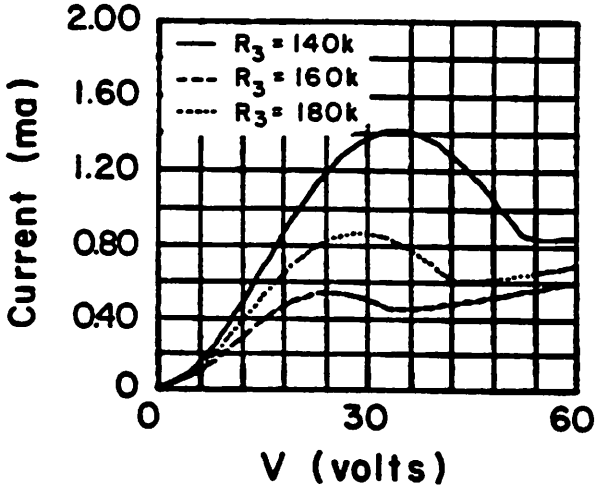
R_2=50k R_3=160k R_4=2meg vto=-1v



R_1 = 500k R_3=160k R_4=2meg vto=-1v



R_1 = 500k R_2=50k R_4= 2meg vto=-1v



R_1 = 500k R_2=50k R_3=160k vto=-1v

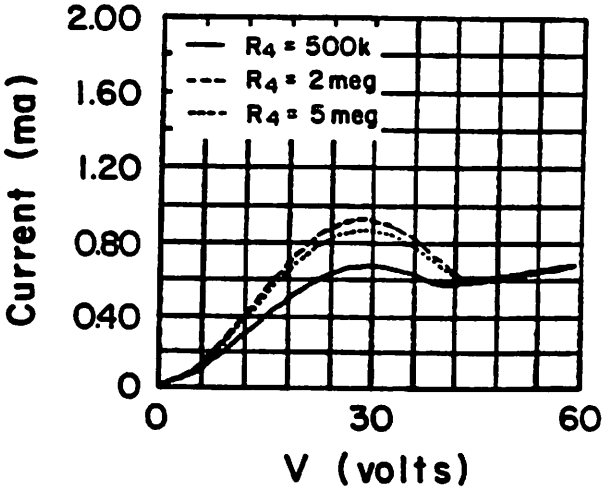
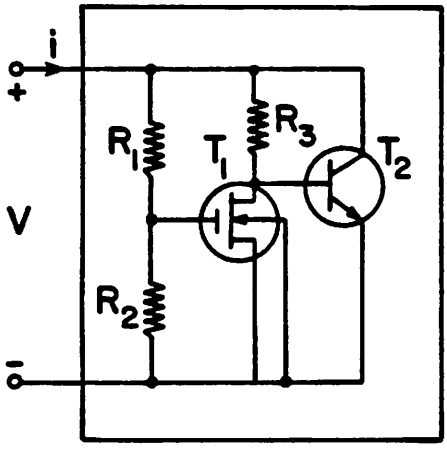
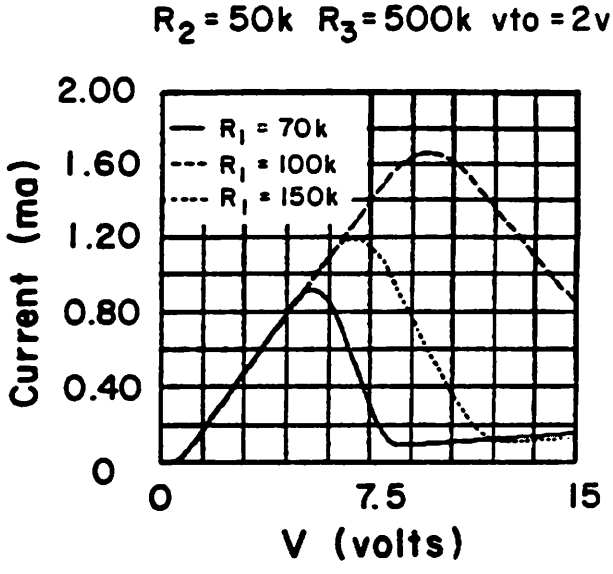
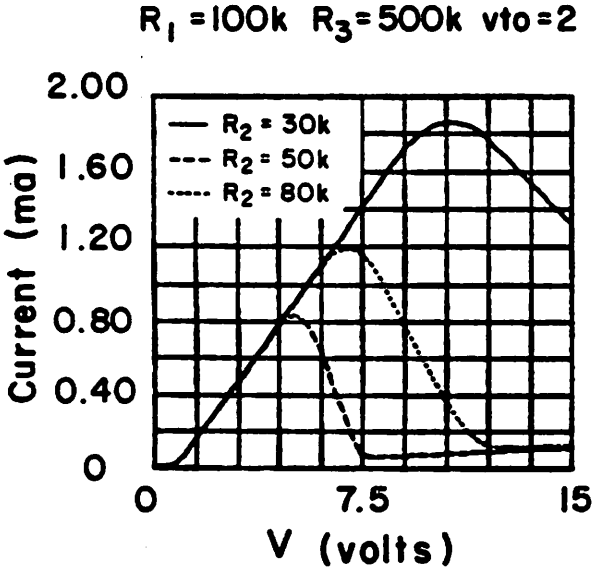


Fig. A-55


i
+
V
−
R1
R2
R3
T1
T2


R2 = 50k R3 = 500k vto = 2v
R1 = 70k
R1 = 100k
R1 = 150k
Current (ma)
2.00
1.60
1.20
0.80
0.40
0
0
7.5
15
V (volts)


R1 = 100k R3 = 500k vto = 2
R2 = 30k
R2 = 50k
R2 = 80k
Current (ma)
2.00
1.60
1.20
0.80
0.40
0
0
7.5
15
V (volts)

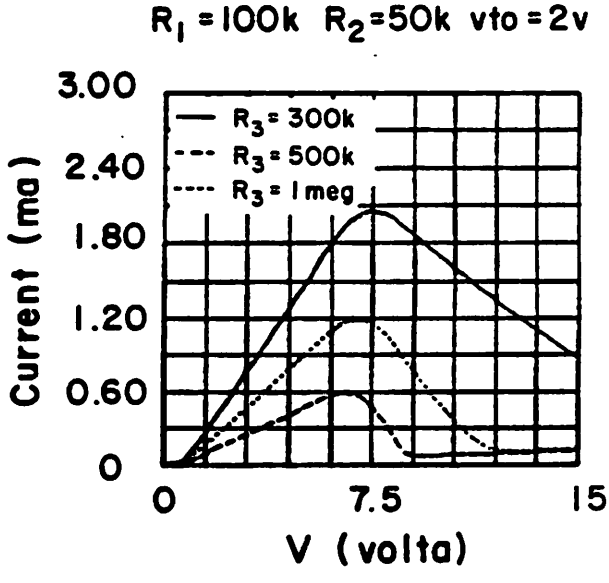
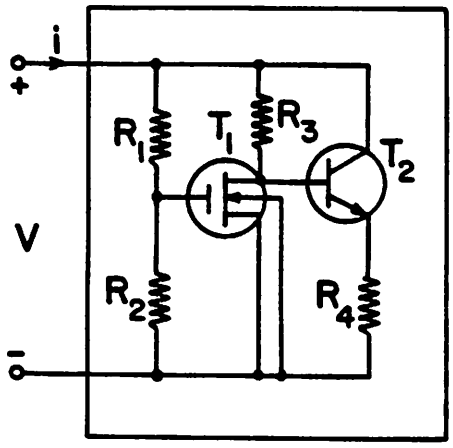
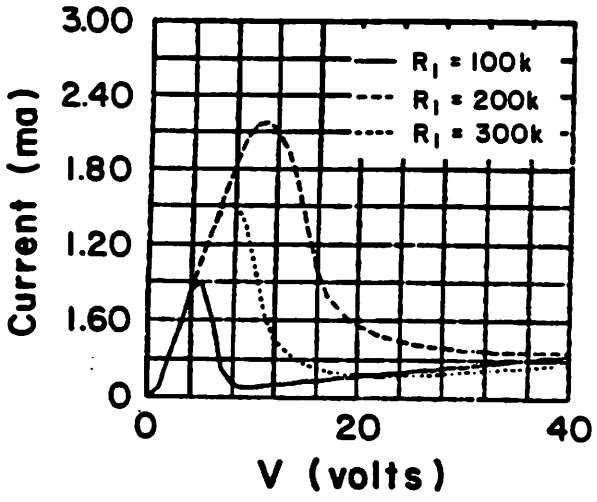

R1 = 100k R2 = 50k vto = 2v
R3 = 300k
R3 = 500k
R3 = 1meg
Current (ma)
3.00
2.40
1.80
1.20
0.60
0
0
7.5
15
V (volts)

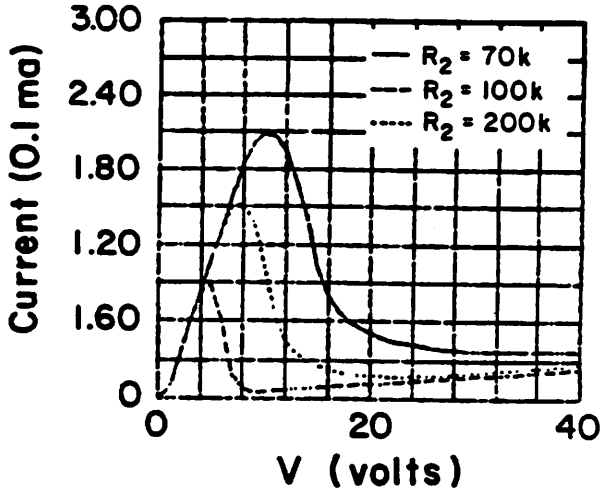
Fig. A-56



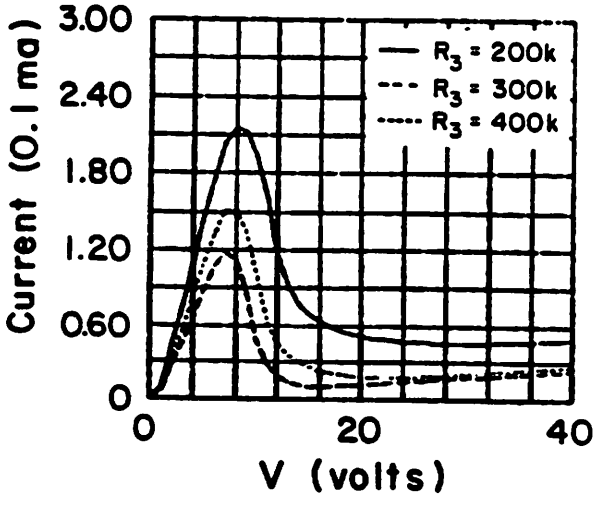
R_2=100k R_3=300k R_4=1k vtom=2v



R_1=200k R_3=300k R_4=1k vtom=2v



R_1=200k R_2=100k R_4=1k vtom=-2v



R_1=200k R_2=100k R_3=300k vtom=2v

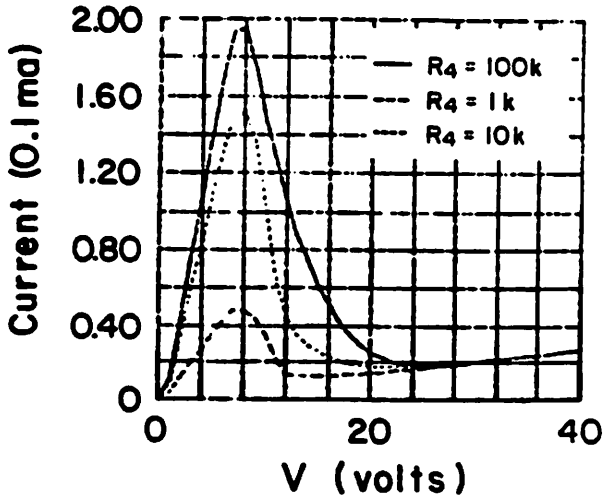
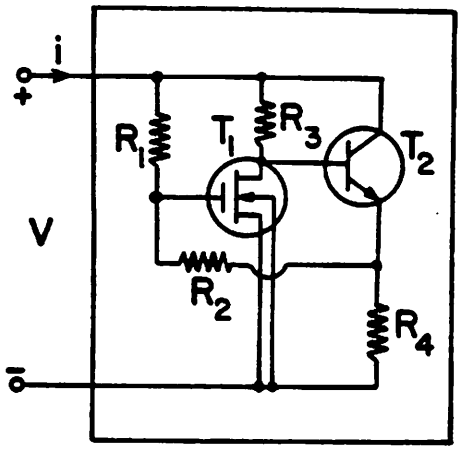
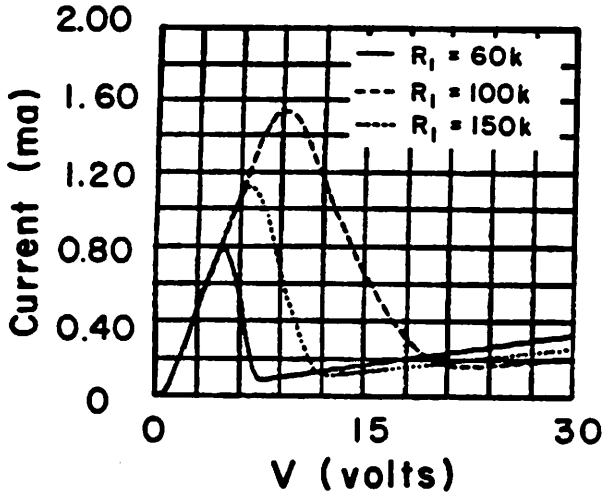


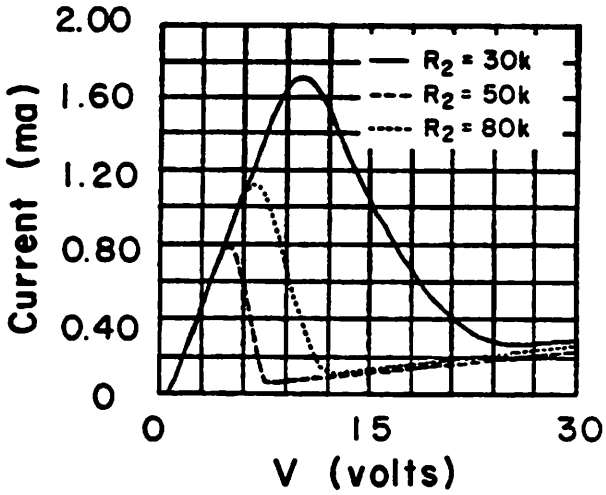
Fig. A-57



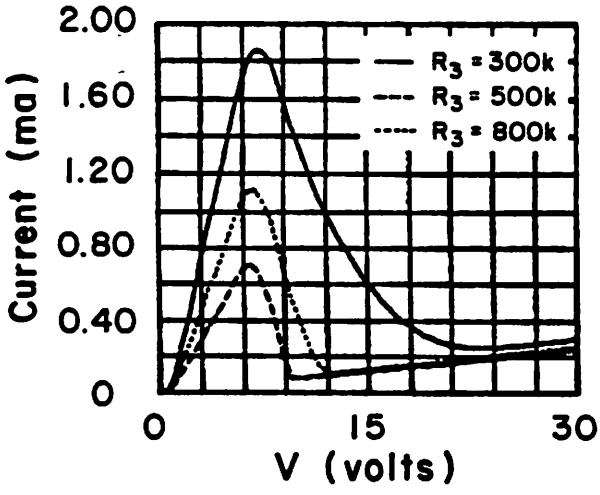
R_2 = 50k R_3 = 500k R_4 = 100k vto = 2v



R_1 = 100k R_3 = 500k R_4 = 100 vto = 2 v



R_1 = 100k R_2 = 50k R_4 = 100k vto = 2v



R_1 = 100k R_2 = 50k R_3 = 500k vto = 2v

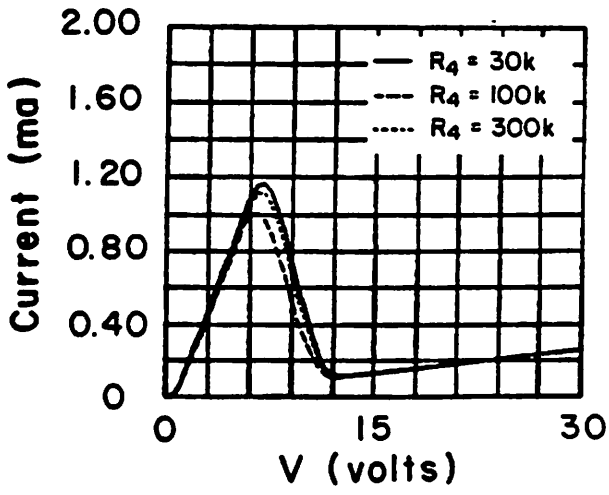
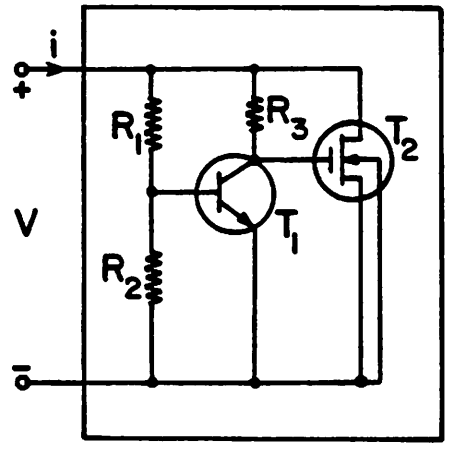
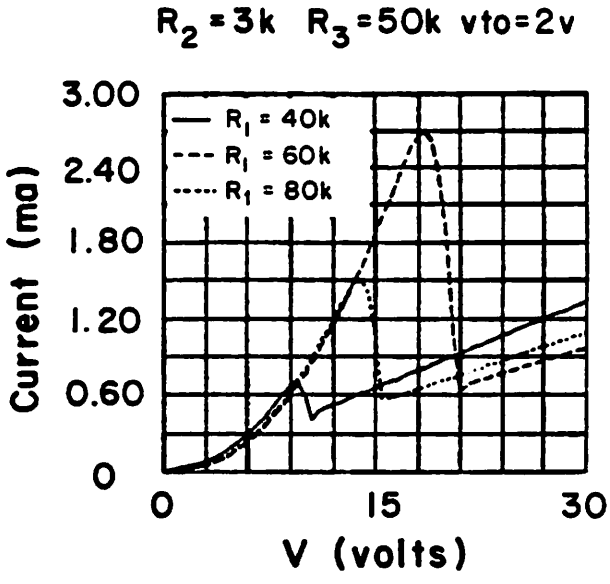
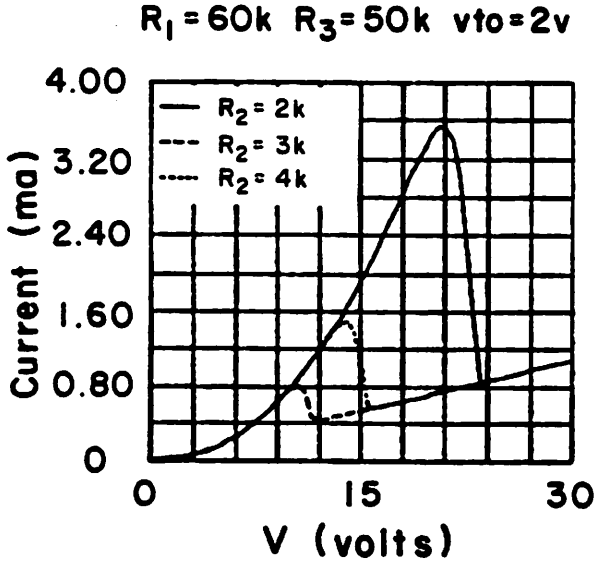


Fig. A-58


i
+
V
−
R1
R2
R3
T1
T2


R2 = 3k R3 = 50k vto = 2v
R1 = 40k
R1 = 60k
R1 = 80k
Current (ma)
3.00
2.40
1.80
1.20
0.60
0
0
15
30
V (volts)


R1 = 60k R3 = 50k vto = 2v
R2 = 2k
R2 = 3k
R2 = 4k
Current (ma)
4.00
3.20
2.40
1.60
0.80
0
0
15
30
V (volts)

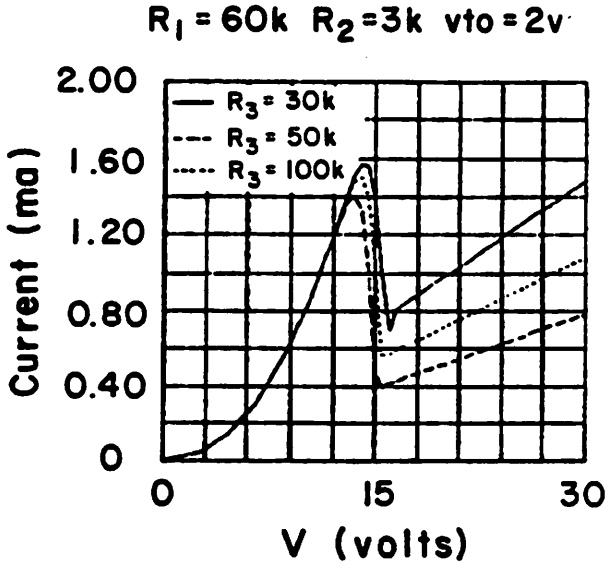
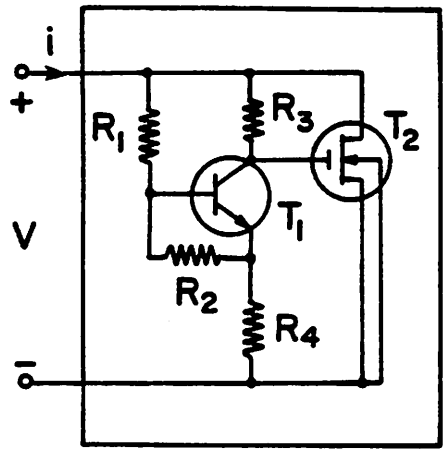
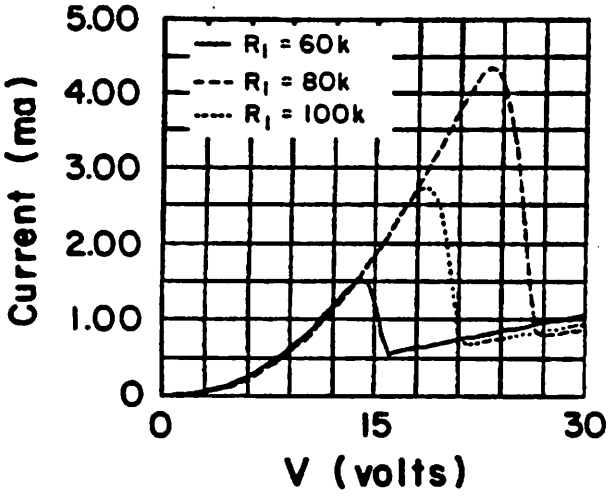

R1 = 60k R2 = 3k vto = 2v
R3 = 30k
R3 = 50k
R3 = 100k
Current (ma)
2.00
1.60
1.20
0.80
0.40
0
0
15
30
V (volts)

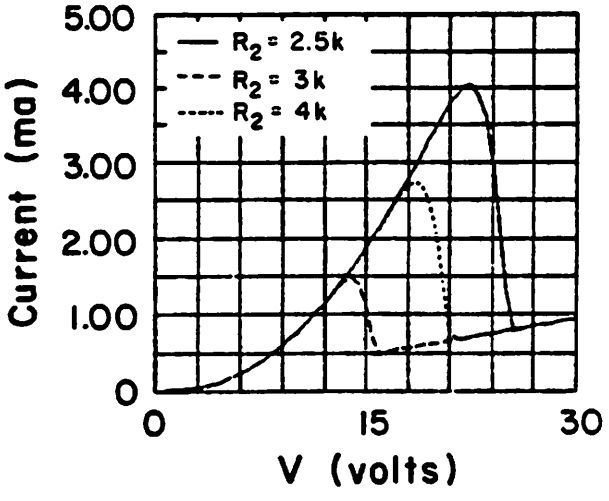
Fig. A-59



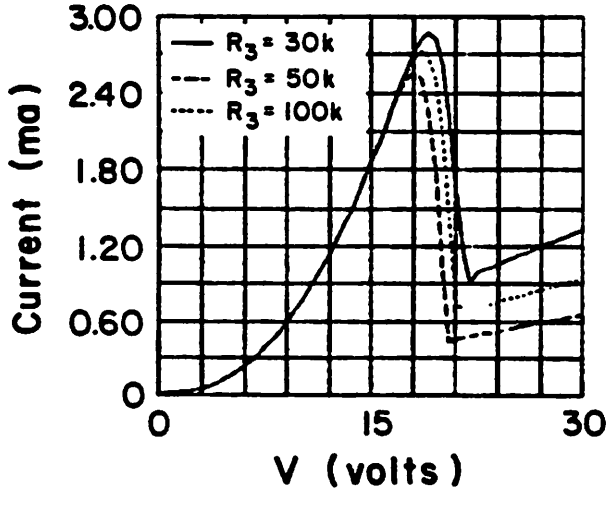
$R_2 = 3k$ $R_3 = 50k$ $R_4 = 500k$ vto = 2v



$R_1 = 80k$ $R_3 = 50k$ $R_4 = 500k$ vto = 2v



$R_1 = 80k$ $R_2 = 3k$ $R_4 = 500k$ vto = 2v



$R_1 = 80k$ $R_2 = 3k$ $R_3 = 50k$ vto = 2v

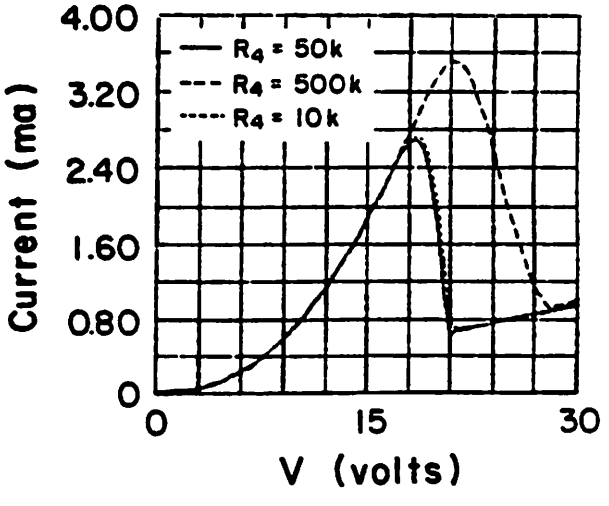
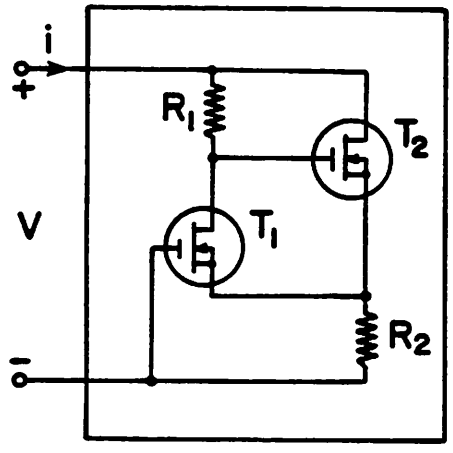
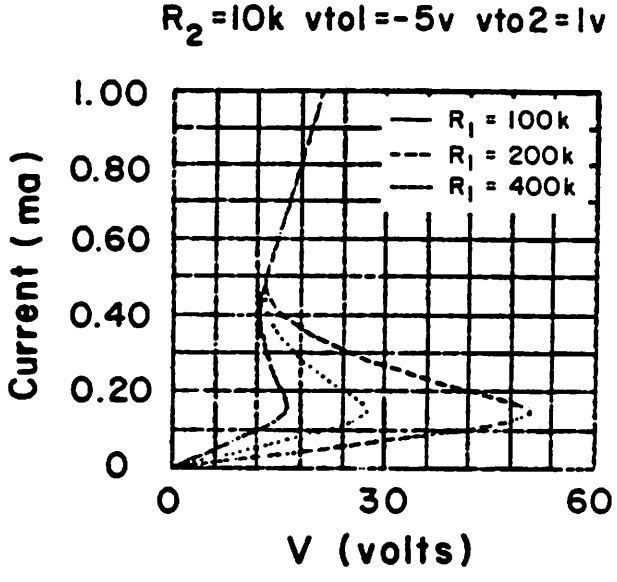


Fig. A-60

Appendix D: Family of V-I Characteristics for Type-S Devices Cataloged in Table 3 and Table 4 (Figures A-61 to A-72).


i
+
V
-
R_1
T_2
T_1
R_2


R_2 = 10k vtol = -5v vto2 = 1v
Current (ma)
1.00
0.80
0.60
0.40
0.20
0
0
30
60
V (volts)
R_1 = 100k
R_1 = 200k
R_1 = 400k

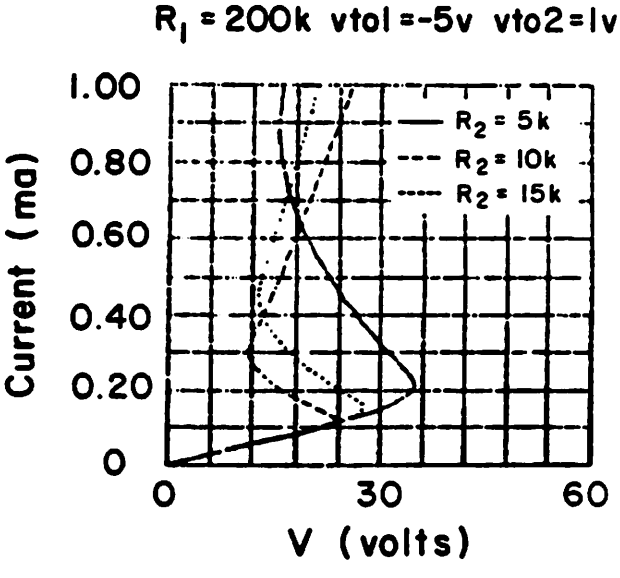
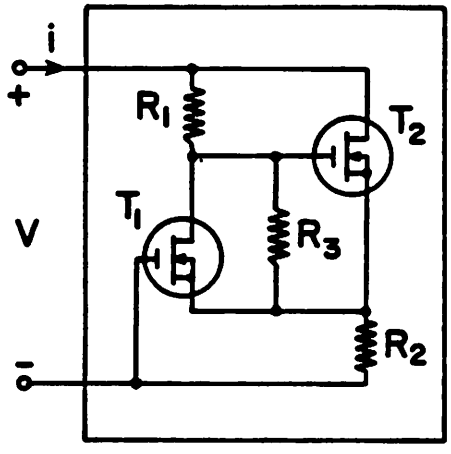
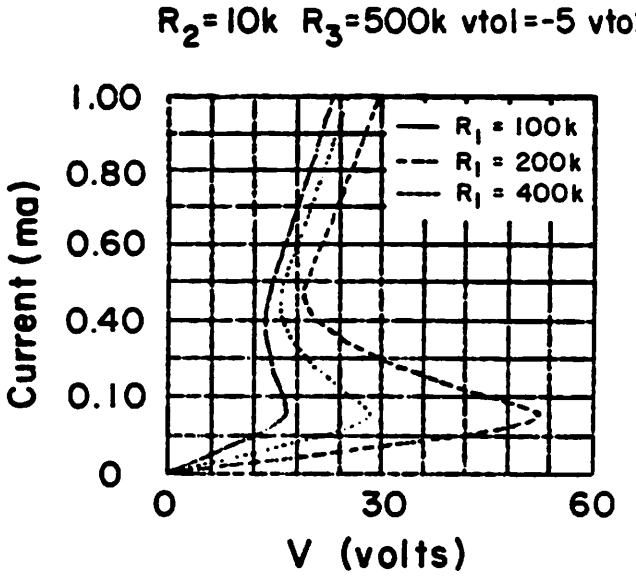
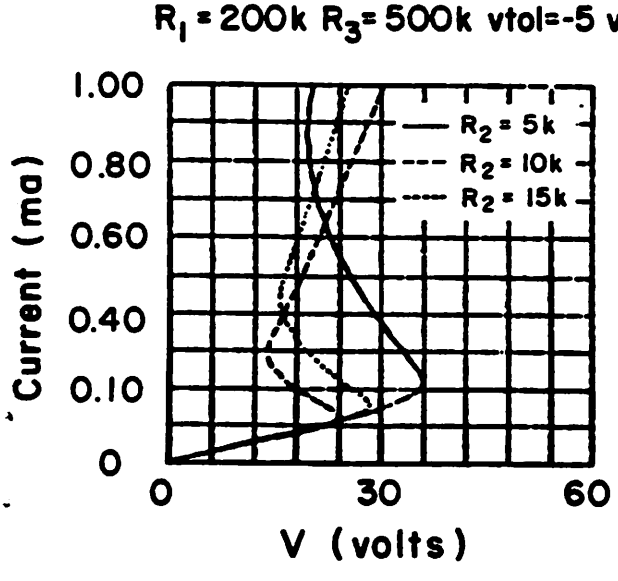

R_1 = 200k vtol = -5v vto2 = 1v
Current (ma)
1.00
0.80
0.60
0.40
0.20
0
0
30
60
V (volts)
R_2 = 5k
R_2 = 10k
R_2 = 15k

Fig. A-61


i
+
V
-
R1
T1
T2
R3
R2


R2 = 10k R3 = 500k vtol = -5 vto2 = 1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R1 = 100k
R1 = 200k
R1 = 400k
0
30
60
V (volts)


R1 = 200k R3 = 500k vtol = -5 vto2 = 1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R2 = 5k
R2 = 10k
R2 = 15k
0
30
60
V (volts)

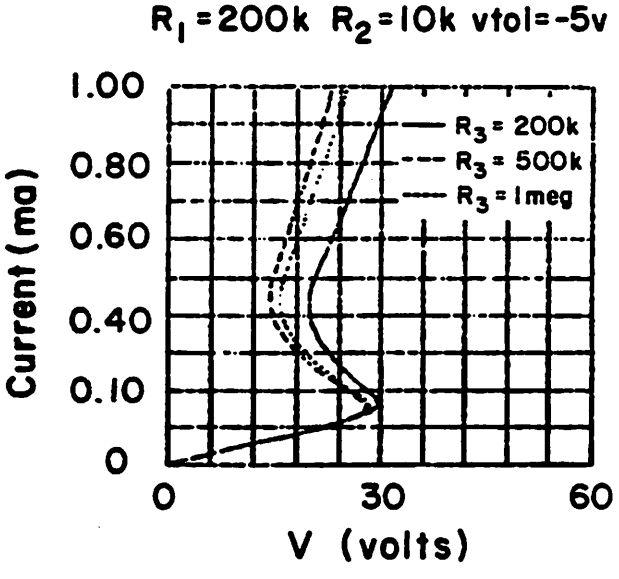
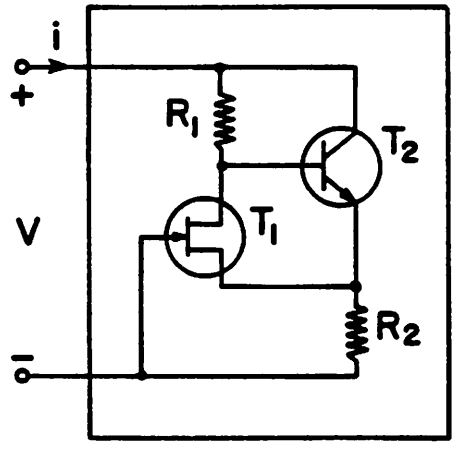
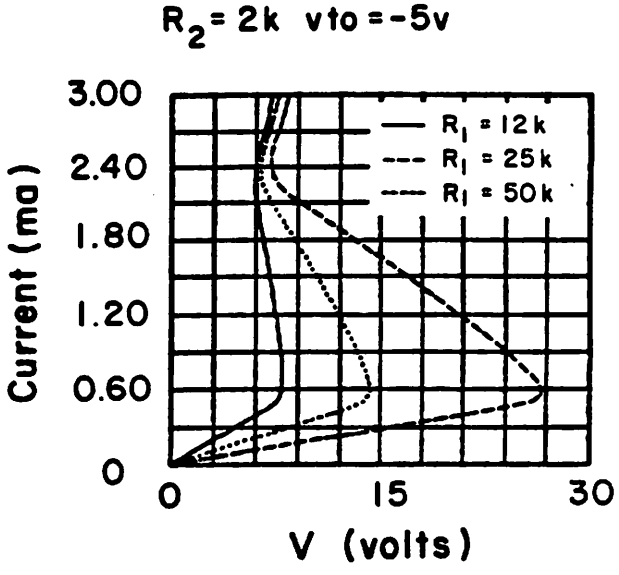
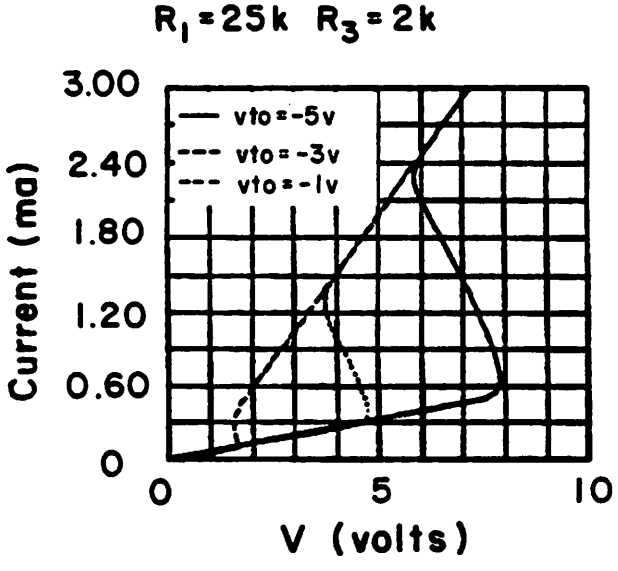

R1 = 200k R2 = 10k vtol = -5v vto2 = 1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R3 = 200k
R3 = 500k
R3 = 1meg
0
30
60
V (volts)

Fig. A-62


i
+
V
−
R1
T1
T2
R2


R2 = 2k vto = -5v
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
0
15
30
V (volts)
R1 = 12k
R1 = 25k
R1 = 50k


R1 = 25k R3 = 2k
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
0
5
10
V (volts)
vto = -5v
vto = -3v
vto = -1v

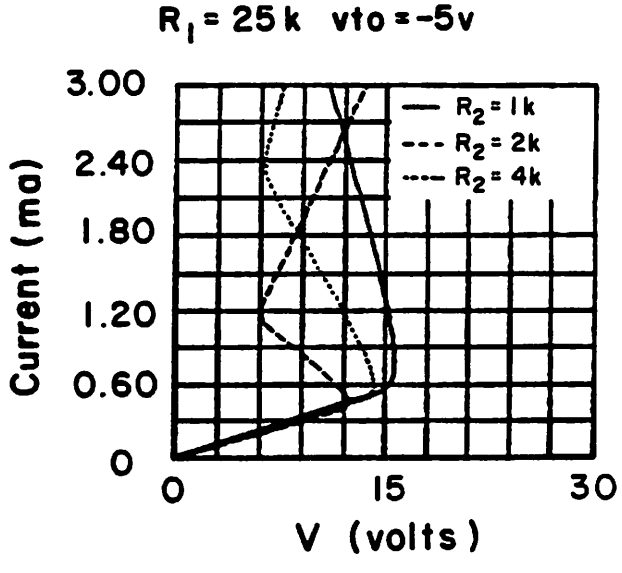
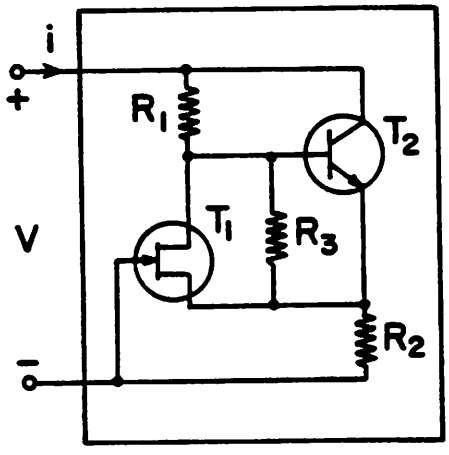
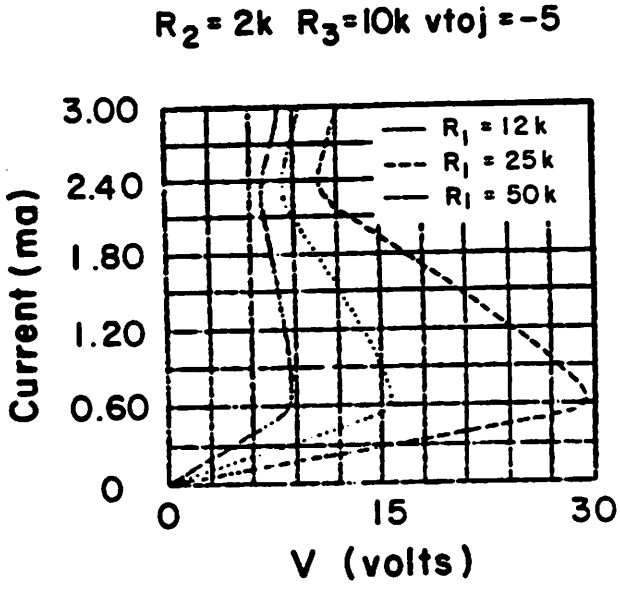
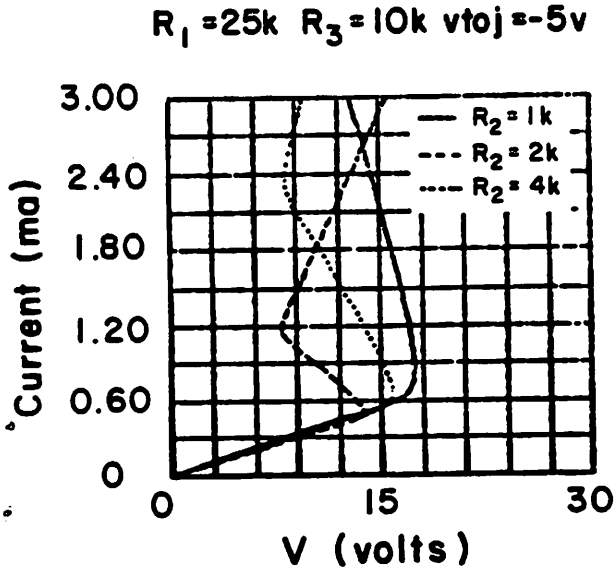

R1 = 25k vto = -5v
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
0
15
30
V (volts)
R2 = 1k
R2 = 2k
R2 = 4k

Fig. A-63


i
+
V
−
R1
T2
T1
R3
R2


R2 = 2k R3 = 10k vtoj = -5
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
R1 = 12k
R1 = 25k
R1 = 50k
0
15
30
V (volts)


R1 = 25k R3 = 10k vtoj = -5v
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
R2 = 1k
R2 = 2k
R2 = 4k
0
15
30
V (volts)

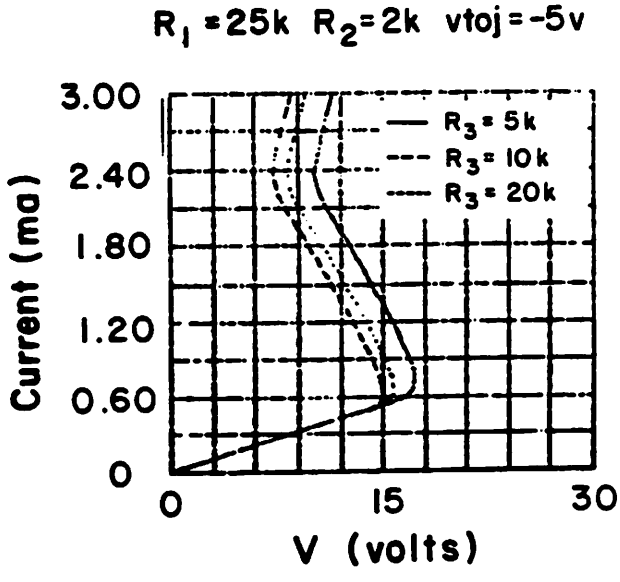
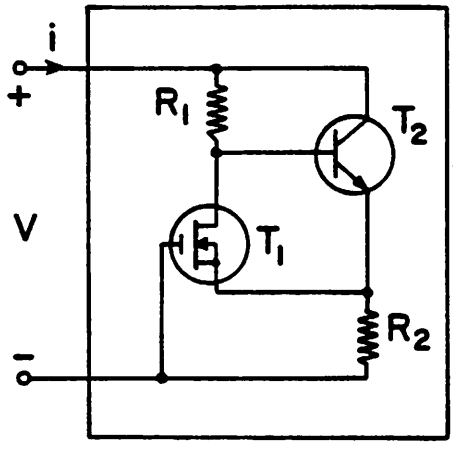
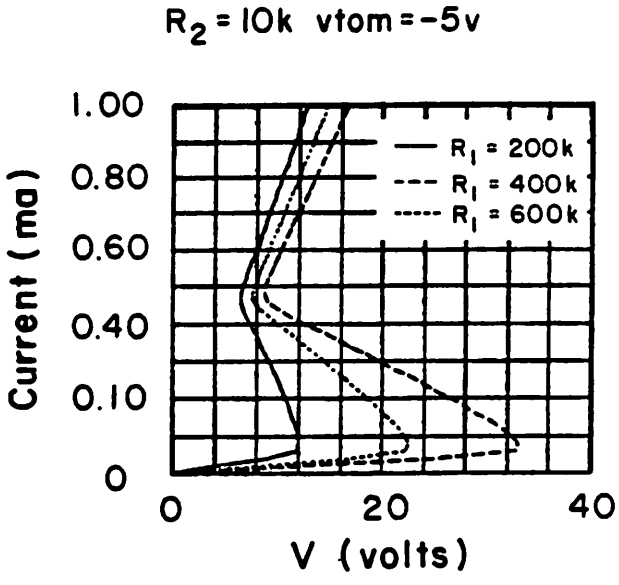
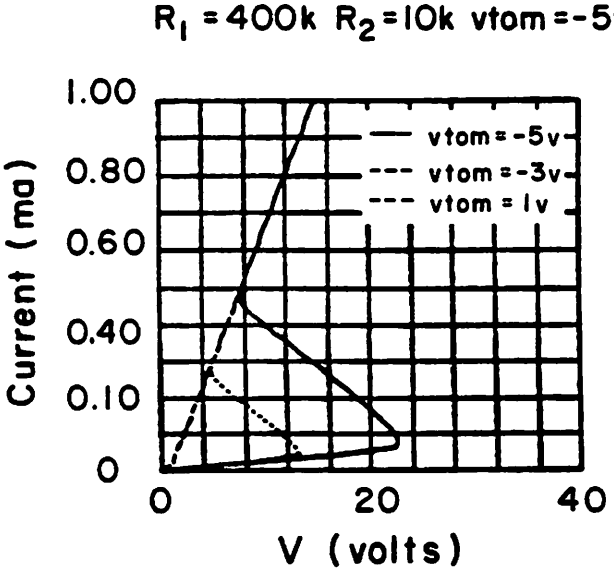

R1 = 25k R2 = 2k vtoj = -5v
3.00
2.40
1.80
1.20
0.60
0
Current (ma)
R3 = 5k
R3 = 10k
R3 = 20k
0
15
30
V (volts)

Fig. A-64


i
+
V
−
R1
T2
T1
R2


R2 = 10k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R1 = 200k
R1 = 400k
R1 = 600k
0
20
40
V (volts)


R1 = 400k R2 = 10k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
vtom = -5v
vtom = -3v
vtom = 1v
0
20
40
V (volts)

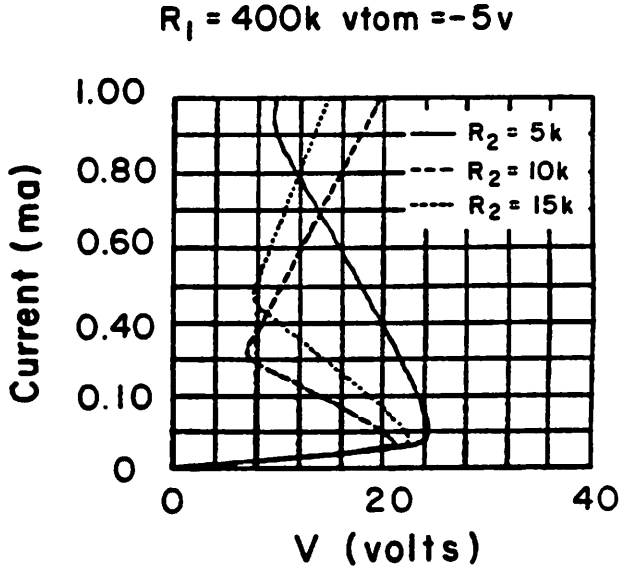
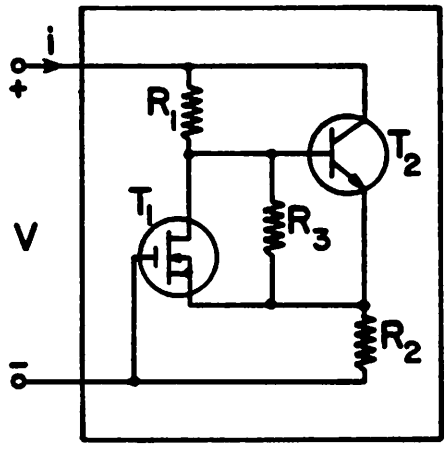
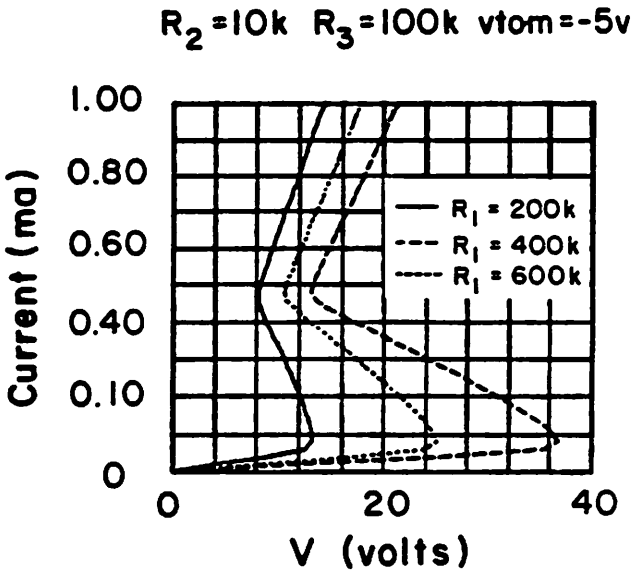
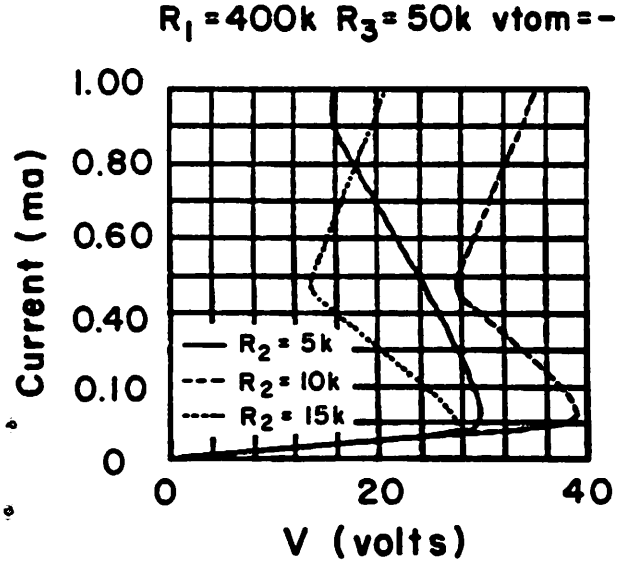

R1 = 400k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R2 = 5k
R2 = 10k
R2 = 15k
0
20
40
V (volts)

Fig. A-65


i
+
V
−
R1
T2
T1
R3
R2


R2 = 10k R3 = 100k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R1 = 200k
R1 = 400k
R1 = 600k
0
20
40
V (volts)


R1 = 400k R3 = 50k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R2 = 5k
R2 = 10k
R2 = 15k
0
20
40
V (volts)

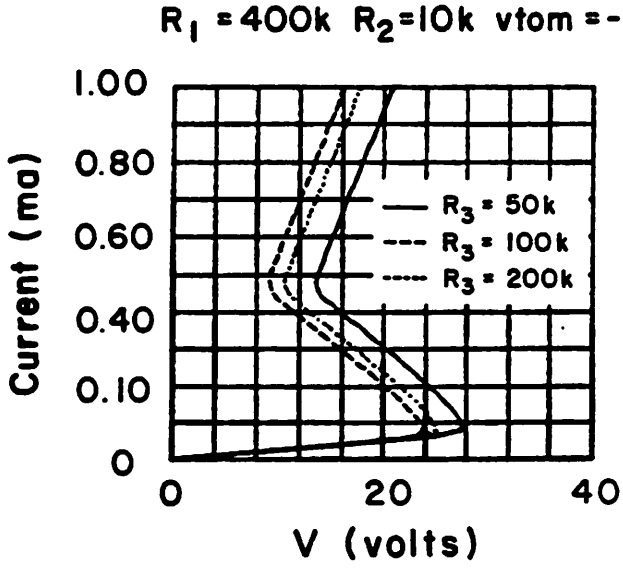
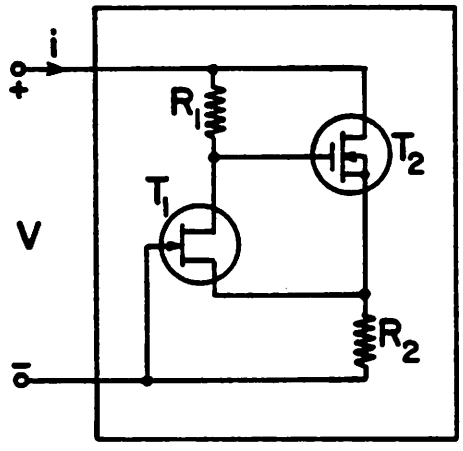
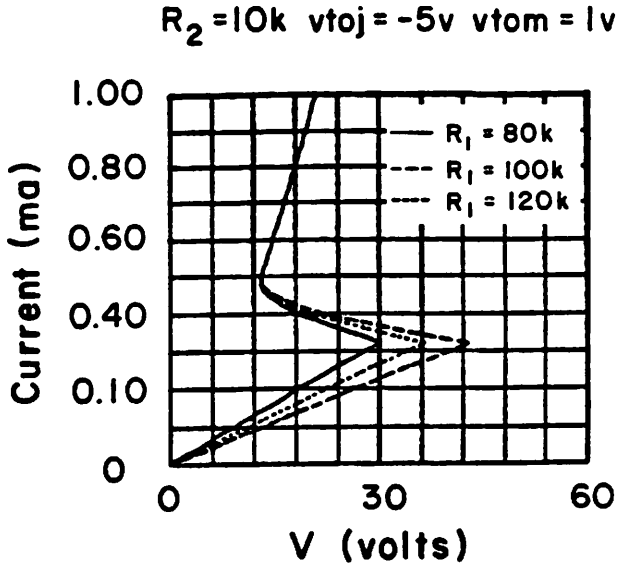
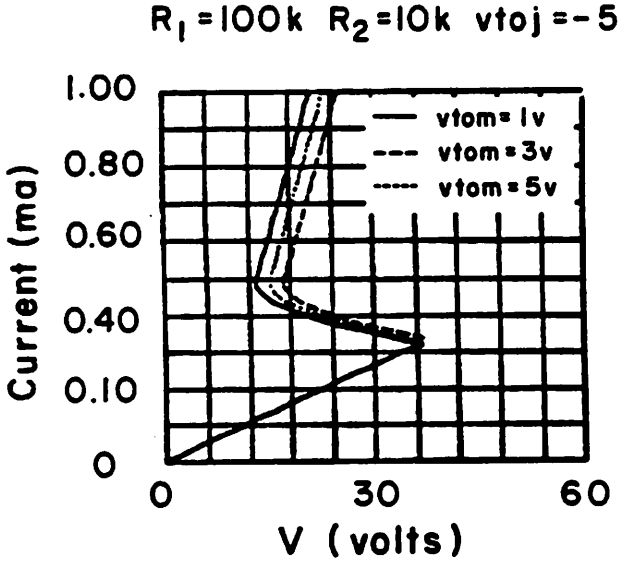

R1 = 400k R2 = 10k vtom = -5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R3 = 50k
R3 = 100k
R3 = 200k
0
20
40
V (volts)

Fig. A-66


i
+
R1
T2
T1
V
R2
-


R2 =10k vtoj = -5v vtom = 1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R1 = 80k
R1 = 100k
R1 = 120k
0
30
60
V (volts)


R1 =100k R2 =10k vtoj = - 5v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
vtom = 1v
vtom = 3v
vtom = 5v
0
30
60
V (volts)

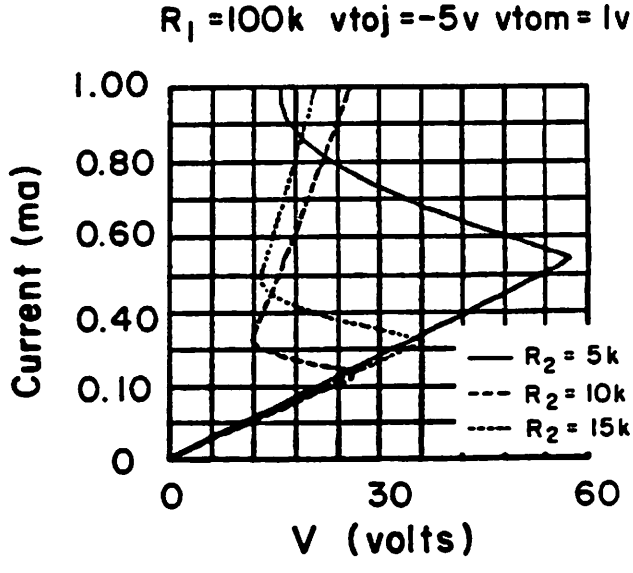
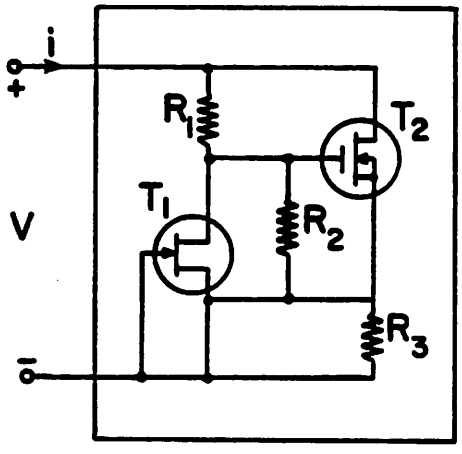
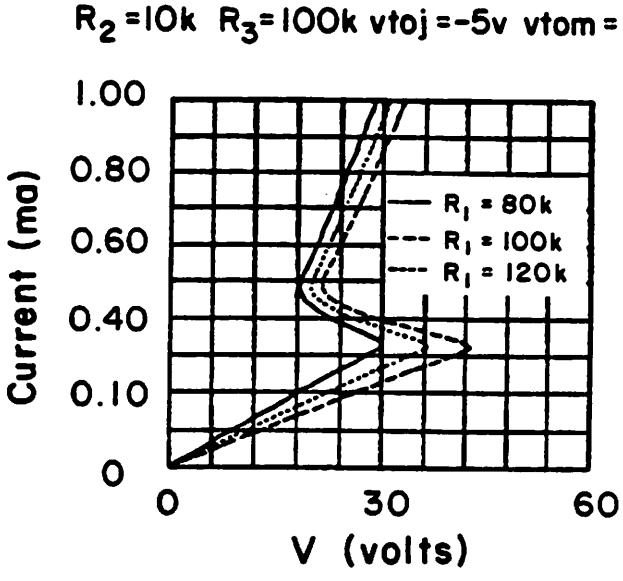
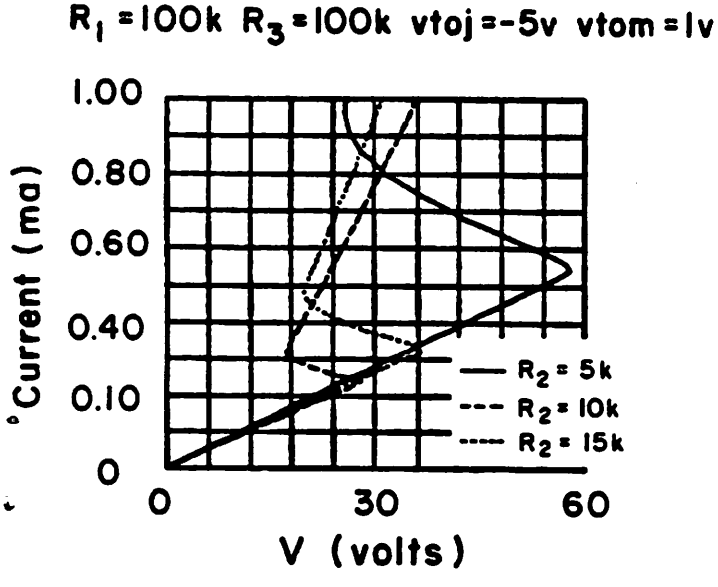

R1 =100k vtoj = -5v vtom = 1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R2 = 5k
R2 = 10k
R2 = 15k
0
30
60
V (volts)

Fig. A-67


i
+
R1
T2
T1
R2
V
R3
-


R2 =10k R3=100k vtoj=-5v vtom=1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R1 = 80k
R1 = 100k
R1 = 120k
0
30
60
V (volts)


R1 =100k R3=100k vtoj=-5v vtom=1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R2 = 5k
R2 = 10k
R2 = 15k
0
30
60
V (volts)

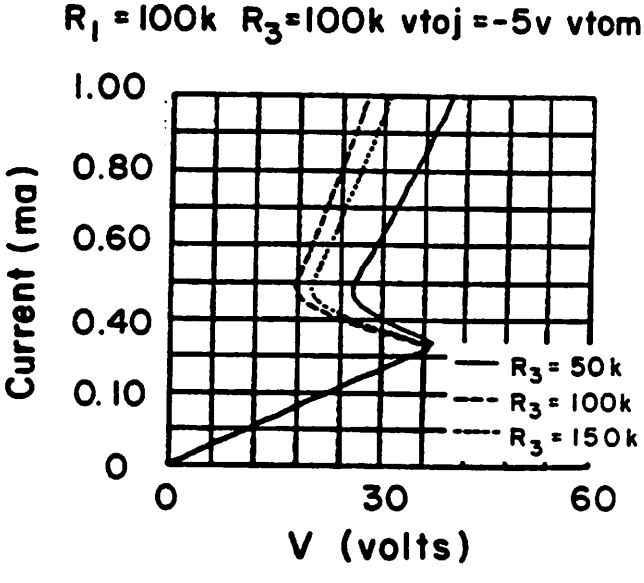
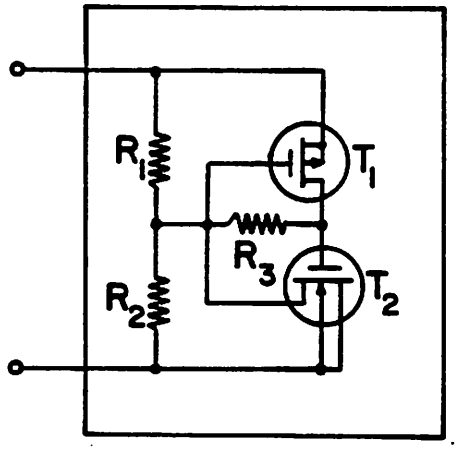
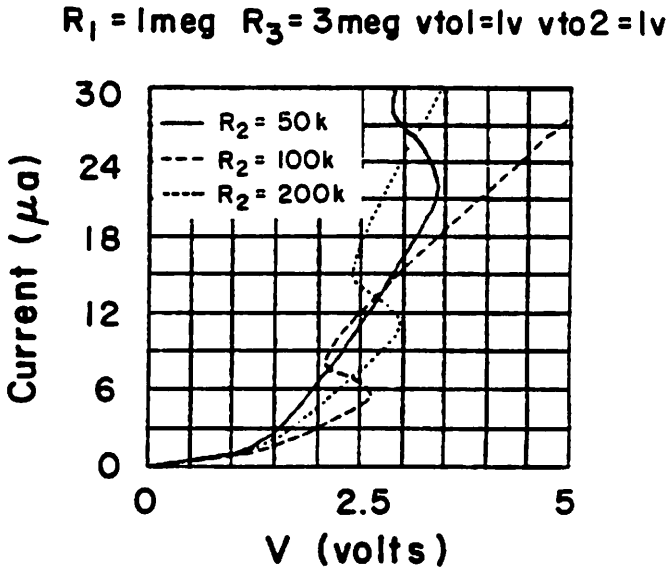
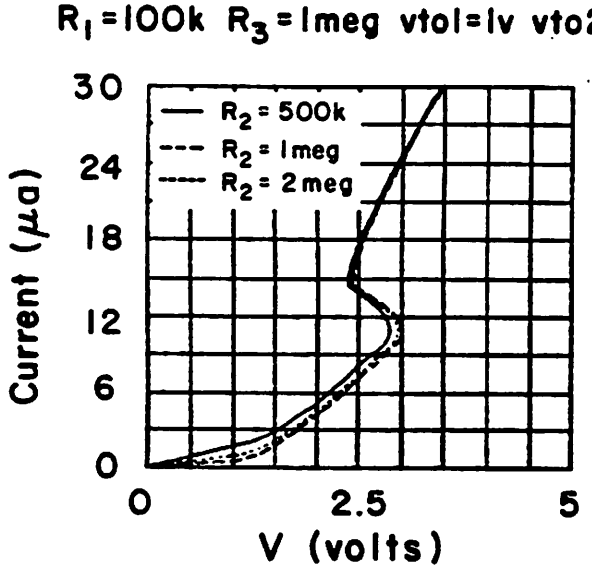

R1 = 100k R3=100k vtoj=-5v vtom=1v
1.00
0.80
0.60
0.40
0.10
0
Current (ma)
R3 = 50k
R3 = 100k
R3 = 150k
0
30
60
V (volts)

Fig. A-68


R1
T1
R3
R2
T2


R1 = 1meg R3 = 3meg vtol=1v vto2=1v
30
24
18
12
6
0
Current (μa)
R2 = 50k
R2 = 100k
R2 = 200k
0
2.5
5
V (volts)


R1=100k R3=1meg vtol=1v vto2=1v
30
24
18
12
6
0
Current (μa)
R2 = 500k
R2 = 1meg
R2 = 2meg
0
2.5
5
V (volts)

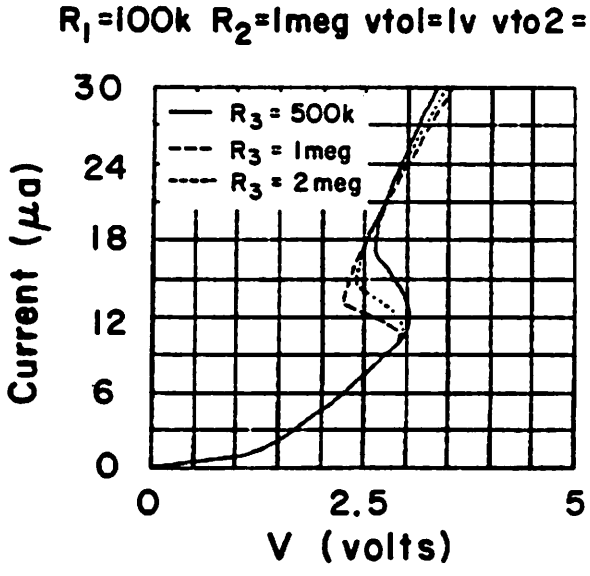
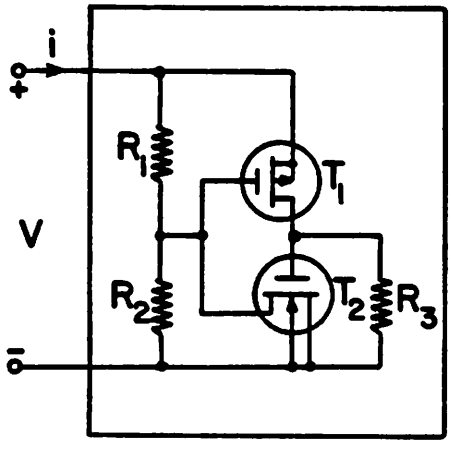
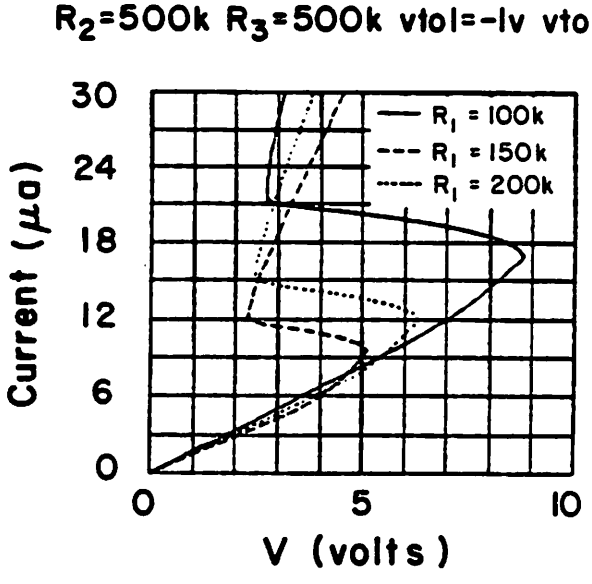
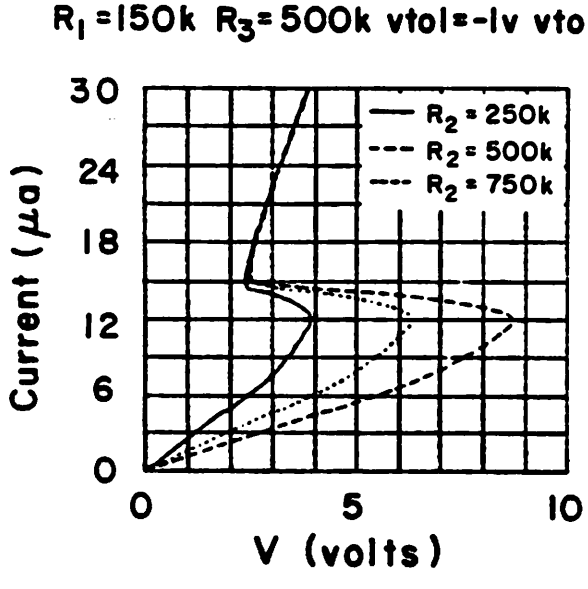

R1=100k R2=1meg vtol=1v vto2=1v
30
24
18
12
6
0
Current (μa)
R3 = 500k
R3 = 1meg
R3 = 2meg
0
2.5
5
V (volts)

Fig. A-69


i
+
V
−
R1
R2
T1
T2
R3


R2=500k R3=500k vtol=-1v vto2=1v
Current (μa)
30
24
18
12
6
0
0
5
10
V (volts)
R1 = 100k
R1 = 150k
R1 = 200k


R1=150k R3=500k vtol=-1v vto2=1v
Current (μa)
30
24
18
12
6
0
0
5
10
V (volts)
R2 = 250k
R2 = 500k
R2 = 750k

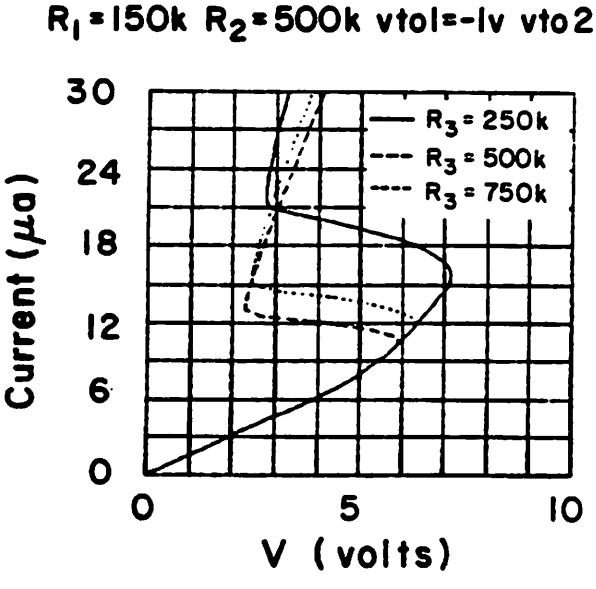
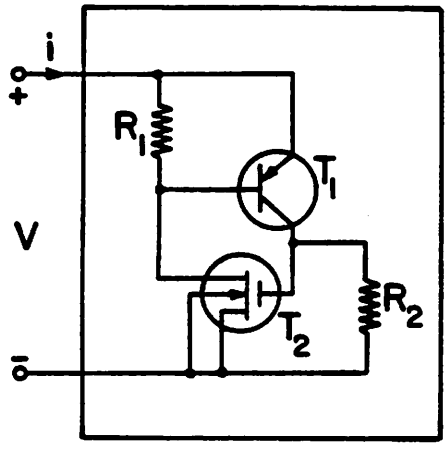
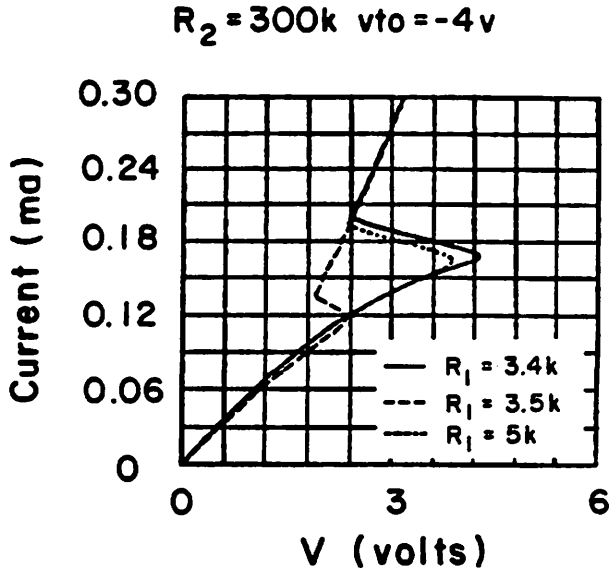

R1=150k R2=500k vtol=-1v vto2=1v
Current (μa)
30
24
18
12
6
0
0
5
10
V (volts)
R3 = 250k
R3 = 500k
R3 = 750k

Fig. A-70


i
+
R1
T1
V
T2
R2
-


R2 = 300k vto = -4v
0.30
0.24
0.18
0.12
0.06
0
Current (ma)
R1 = 3.4k
R1 = 3.5k
R1 = 5k
0
3
6
V (volts)

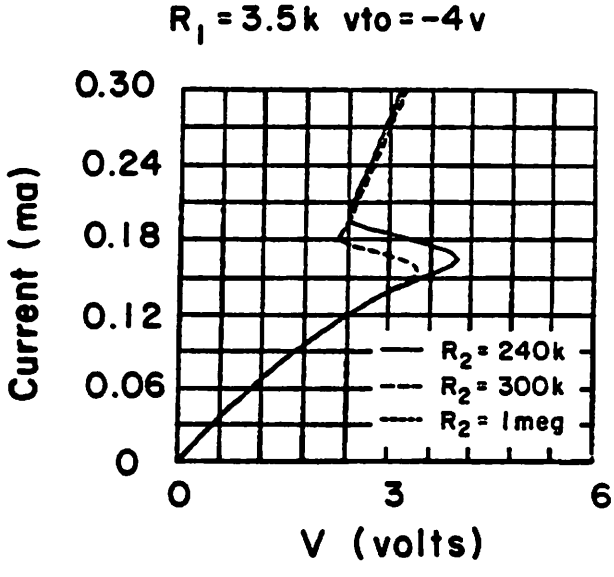
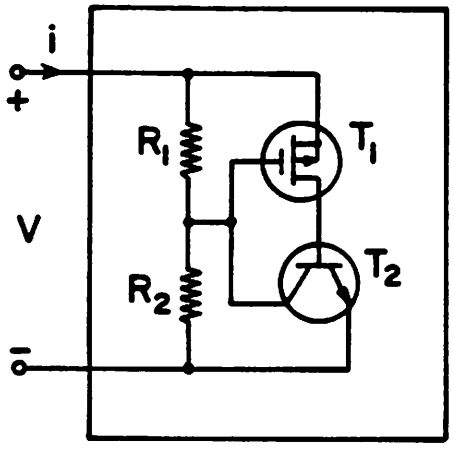
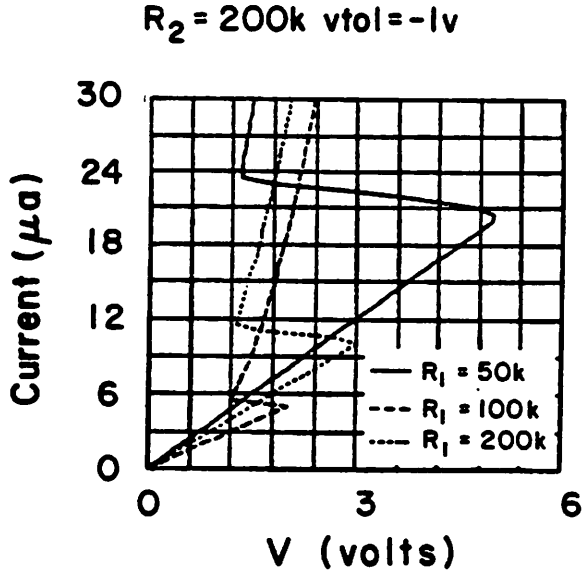

R1 = 3.5k vto = -4v
0.30
0.24
0.18
0.12
0.06
0
Current (ma)
R2 = 240k
R2 = 300k
R2 = 1meg
0
3
6
V (volts)

Fig. A-71


i
+
V
−
R1
R2
T1
T2


R2 = 200k vtol = -1v
Current (μa)
30
24
18
12
6
0
0
3
6
V (volts)
R1 = 50k
R1 = 100k
R1 = 200k

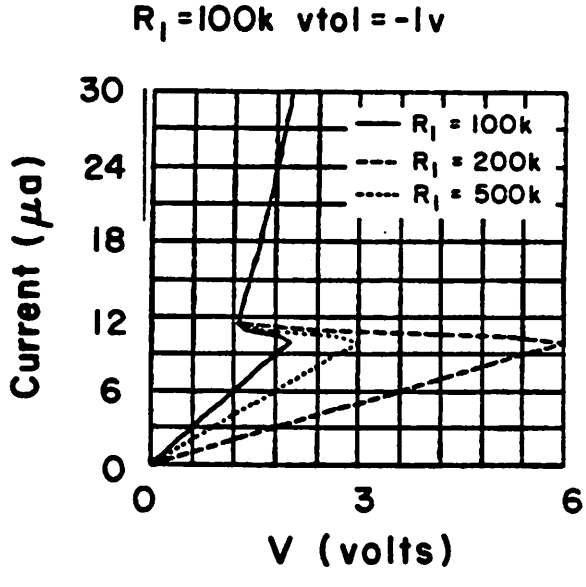

R1 = 100k vtol = -1v
Current (μa)
30
24
18
12
6
0
0
3
6
V (volts)
R1 = 100k
R1 = 200k
R1 = 500k

Fig. A-72