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ABSTRACT

This paper reports on studies concerning the feasibility of large-scale integrated realization of the circuits needed to provide hybrid-mode full-duplex digital transmission at 80 kb/s or higher rates over standard local telephone loops. Alternative means of achieving the required 60 dB or so of echo cancellation have been studied in detail. The conclusion is that a combination of analog and digital circuit techniques permit practical MOSLSI realization of the complete modem, including filters, echo canceller, timing recovery, and A/D and D/A converters, without need for external circuit elements, trimming, or adjustments.

The preferred system configuration has been evaluated by means of analysis, simulation, and laboratory and field measurements. A complete full-duplex system, including an experimental NMOS integrated circuit echo canceller, was built and tested. Measurements showed a bit error rate lower than 10^{-8} with line attenuation up to 40 dB, operating at 80 kb/s. We conclude that a fully-integrated MOSLSI circuit to implement all functions for a hybrid-mode digital local loop is entirely feasible.

1. INTRODUCTION

The trend towards digital networks in the telephone system and the need to provide digital transmission capability for the subscriber has prompted the investigation of the local loop as a means of transmitting digital data. For economic reasons it is desirable to transmit in both directions over the same pair of wires. Two techniques have emerged as promising for this purpose; namely, the *burst-mode* or *ping-pong* method, and the *hybrid* balancing method. The latter uses a hybrid transformer (or the electronic equivalent) to provide directional isolation, as in voice transmission. Adaptive echo cancellation is used to improve channel separation in order to achieve an adequate error rate.

Advantages of the hybrid balancing method over the ping-pong method are the smaller total transmitted signal bandwidth and the fact that long loops can be repeatered without accumulating delays. Trans-hybrid near-end crosstalk and echos, not a significant problem in a ping-pong system, must be minimized by echo cancellation when using the hybrid technique. If adequate cancellation can minimize the effect of near-end crosstalk and echo, the smaller signal bandwidth of the hybrid technique will result in a greater range of transmission than the ping-pong method for a given error rate. VLSI techniques will likely reduce the cost of the greater complexity involved in echo cancellation, making the hybrid system cost-competitive with ping-pong.

The objective of this work is to establish the feasibility of the large scale integration of full-duplex two-wire baseband modems using the hybrid method working at 80 kb/s or higher data rates. The 80 kb/s rate would permit, for instance, simultaneous use of a 64 kb/s PCM channel for voice communication, plus up to 16 kb/s of simultaneous data transmission. Switching equipment could be designed to permit independent connections for the voice and data

portions of the 80 kb/s channel.

The purpose of this paper is to give detailed consideration to several alternative methods of implementation of the echo canceller in MOSLSI. A couple of these methods have been implemented for experimental verification. Since the echo canceller operates in the context of the entire modem, a modem was implemented as described in Section 2. Section 3. then addresses the performance which can be expected from an MOSLSI realization of specifically the echo canceller, as obtained from theory, simulation, and experimentation. Section 4. presents the conclusions.

2. SYSTEM DESCRIPTION

Figure 1 shows a block diagram of the system under consideration. Two baseband modems communicate at 80 kb/s on a single pair of wires. One of them is located at the central office, the other at the subscriber set. Typical specifications include a transhybrid loss of 10 dB, a line attenuation of up to 40-45 dB for a 5 km subscriber loop (measured at half the data rate, where the spectral density peaks for the bipolar coded signal), and a required echo cancellation of 50-55 dB for 20 dB signal to noise ratio after cancellation. Even greater cancellation of the echo would be desirable if it could be achieved.

While the primary goal was to obtain a monolithic realization of the echo canceller, it was felt important to consider the design in the context of the entire system. The system configuration which was chosen is shown in greater detail in Figure 2. The following Sections discuss the design choices which were made.

2.1. Scrambler and Descrambler

Scrambling the incoming data ensures that the transmitted sequence is random (or pseudo-random) even during idle or repetitive data patterns [3]. A

random data sequence is required for the convergence of the echo canceller, to avoid placing discrete spectral components on the line (that would cause RFI and crosstalk interference), as well as to aid timing recovery in the receiver. The particular scrambler chosen is recommended by CCITT and performs a modulo 2 division by the polynomial $1+x^3+x^{20}$ [4], generating a pseudo-random sequence of length $2^{20}-1$. The descrambler, which is self-synchronizing, performs a modulo 2 multiplication by the same polynomial.

2.2. Bipolar Coder

Alternative line codes have recently received attention in the literature [5], and will not be discussed here. "Bipolar" or "alternate mark inversion (AMI)" coding has been chosen in this design in view of its simplicity and robustness; however, most of the techniques used here are readily adaptable to other codes. The bipolar transmitted signal is three-level, and it was desired to avoid building a canceller which accepted three-level data. One possibility is to input the same data to the line coder and the echo canceller. However, since the coder is then located in the echo path, that echo path would then be nonlinear if true bipolar coding were utilized. A modified technique is therefore used here, which consists simply of differentiating the input binary signal using an analog differentiator with a time constant much shorter than the baud period. A three-level signal is thus created which obeys the same constraint as the standard bipolar signal; namely, that the transmitted signal has no *dc* content. In addition, since the line coding is obtained through a linear operation, it is consistent with linear echo cancellation. In practice the analog differentiator is incorporated in the output filter making it into a *bandpass* instead of a *lowpass* filter. Thus the block named "bipolar coder" has conceptual rather than physical existence in the hardware implementation.

It should also be noted that the coding could be made into true bipolar by performing a modulo 2 running sum of the data sequence before entering it into the canceller and the transmit filter with differentiator, as suggested in [12]. This additional complexity was not included, however.

2.3. Transmit and Receive Filters

Minimal intersymbol interference filters [6] were used at the transmitter output and the receiver input. The transmit filter shapes the pulse placed on the line to minimize high frequency components that would unnecessarily increase crosstalk and radio frequency interference. Care must be exercised in its design to keep nonlinear distortion components (which a linear echo canceller cannot compensate) lower than approximately -60 dB relative to the transmitted signal level. This also requires that the input pulses be symmetrical to a similar degree. Perfectly square pulses would be desirable, but unfortunately the output of a logic gate departs significantly from that ideal due to rising and falling transients that are not equal in general. Satisfactory pulses have been obtained by clamping a CMOS gate with diodes as shown in Fig. 3.

Because of the high degree of symmetry between positive and negative pulses which is required, oscilloscope measurements in the time domain are generally not sufficient to evaluate the quality of the pulse generating circuitry. A better evaluation can be made by measuring the output signal with a spectrum analyzer. For a bipolar signal, spectral zeros are to be expected at multiples of the data rate. It is shown in Appendix A that in the presence of nonlinear distortion the departure from zero of the spectral density at multiples of the data rate provides a good indication of the transmitted pulse symmetry. A more quantitative result can be obtained driving the circuit with a sequence of alternating 1's and 0's. A periodic waveform with a fundamental frequency at half the data rate results at the output. The even harmonic content of that signal meas-

ures the nonlinear pulse asymmetry distortion.

A significant consideration in the design of the modem is timing recovery. It is possible, although perhaps foolhardy, to derive timing in a half-duplex mode during initialization. It was decided to take a more conservative design approach in which the canceller is capable of deriving timing properly when the data transmission in the two directions is asynchronous. This allows for proper recovery of timing during startup or after loss of timing, but also requires that the sampling be done at twice the transmitted pulse rate. One of the functions of the receive filter, in addition to removing the out-of-band noise, is thus to remove all potentially aliasing frequency components above the data rate. Aliasing distortion would impair the operation of the timing recovery circuits, although it has no adverse consequences on the echo cancellation and data detection. The receive filter used here provides only 27 dB of attenuation at the data rate. However, the signal has a spectral zero at that frequency, which further decreases the high frequency components. Experimental evaluation has shown that this filter is completely satisfactory.

2.4. Equalizer

A single-zero manually adjusted equalizer was used in this system. As in a standard automatic line build-out (ALBO) used in T-carrier systems, this equalizer had a single adjustable zero. Performance proved satisfactory under most circumstances. The adjustment of the zero frequency could be made automatic using standard techniques. Use of adaptive decision feedback equalization (DFE) after the echo cancellation would further improve the eye opening, particularly in the presence of bridge taps, but was not included. Eight taps of DFE or fewer should be completely sufficient.

2.5. Echo Canceller

Two different versions of the echo canceller have been constructed. They are described in Section 3.3.1, after several alternative realizations are discussed in detail in Section 3.1.

2.6. Detector

The output of the echo canceller is the far-end transmitted data signal, which has a three-level eye. Detection requires slicing it at two thresholds and conversion to a binary signal by the inverse of the differentiation introduced in the transmitter. This is done with logic circuits in this implementation. The binary signal is then descrambled with the circuit described in Section 2.1.

2.7. Reconstruction Filter

This filter reconstructs a continuous-time waveform from the samples at the output of the echo canceller to be used in the subsequent timing recovery circuit. Since a nonlinear operation will follow in the timing recovery circuit, and this will create high frequency components not present in the original spectrum, it is necessary to remove first the aliases generated by the sampling. The design of the filter is somewhat simplified using a bandpass instead of a lowpass characteristic. A fourth order maximally flat filter with a center frequency at half the data rate and a bandwidth of 0.4 times the center frequency has been used. It is shown in [7] that use of this filter minimizes the jitter in the timing waveform.

2.8. Full-wave Rectifier

Full-wave rectification creates a discrete line [7] in the spectrum at the data rate, even when the data signal has a continuous spectrum bandlimited to less than the data rate (typically between $0.5f_B$ and f_B).

2.9. Bandpass Filter

This filter recovers the spectral line created by the full-wave rectification and removes other spectral components whose presence would increase the jitter in the timing signal. A second order filter with a Q=100 has been used. The output of this filter is a nearly sinusoidal waveform with a significant amount of jitter.

2.10. Frequency Multiplier

The phase lock loop (PLL) locks to the timing tone obtained in the previous stage and, by using a very large loop time constant (τ=0.1sec) reduces the jitter. It simultaneously performs a frequency multiplication by a factor of 40, in order to obtain the processor clock at 3.2 MHz (in the second implementation of the echo canceller the processor clock frequency was f_c=1.6 Mhz but the same PLL was used in both receivers, adding a divide by 2 stage in the second).

Phase locking occurs after the echo canceller has converged, since an echo-free signal is required to recover the timing. Synchronous operation starts after an initial period during which first the echo canceller is allowed to converge and then the PLL locks. In the subscriber modem, the derived timing clock is also used as the transmit data clock. This synchronous operation is not required for the proper operation of this type of echo canceller [2], but is a requirement of the digital switch with which the modem must interface.

3. TECHNIQUES FOR LARGE SCALE INTEGRATION OF THE SYSTEM

The implementation complexity of hybrid mode digital subscriber loops would result in a high manufacturing cost for any realization using off-the-shelf components. Thus from an economic point of view the hybrid mode technique cannot compete with the burst mode technique, in spite of the recognized technical advantages of the former [1]. The high cost is mainly associated with

two sections of the echo canceller, namely

1. *The digital processor implementing the canceller adaptation* and/or transversal filtering, and
2. *The analog-to-digital and/or digital-to-analog converters.*

Large scale integration techniques have proven very effective in decreasing the cost of digital circuits. Thus, a monolithic implementation of this system will clearly overcome the cost factor associated with 1. However, the requirement of on-chip high performance data converters poses additional problems that have to be solved before the system can be fully integrated. This Section will address the problems associated with the data conversion in an integrated hybrid-method digital subscriber loop. Switched-capacitor filters are now a proven technique that can be used for the implementation of the various filters described in Section 2, and will not be considered here. In Section 3.1 we analyze available alternatives for the implementation of the echo canceller, in view of the problems associated with the data conversion. Three of the more attractive of these alternatives are explored in detail in Section 3.2 by means of analysis and computer simulation.

An MOS monolithic chip built to experimentally evaluate the feasibility of the implementation of an echo canceller with on-chip data converters is described in Section 3.3. Means for integration of the complete system are proposed in Section 3.4.

3.1. Alternative Implementations of the Echo Canceller

Four alternative configurations will be considered in this Section:

1. *An analog implementation of the echo canceller (Figure 4a).*
1. *A fully digital echo canceller with digital cancellation* and A/D conversion of the input signal (Figure 4b).

3. *A digital echo canceller with analog cancellation (Figure 4c).*

4. *Analog-digital echo canceller with analog cancellation (Figure 4d).*

Each of these alternatives will be discussed in the following four sub-sections.

3.1.1. Analog Echo Canceller

Figure 4a shows the structure of a completely analog echo canceller using switched-capacitor techniques. The coefficients of the transversal filter are stored in integrators, and the binary weighting is done using switched capacitors. A summing amplifier performs the convolution sum. The adaptation algorithm is also implemented by a switched capacitor circuit that adds a correction term to the coefficients stored in the integrators. The desired correction term is obtained by multiplying the cancellation error coming from the output of the summing amplifier by either +1 or -1, corresponding to the data bit at the corresponding tap. This technique is adequate to implement synchronous sampling echo cancellers, whose sample rate is synchronous to the data rate. These echo cancellers are usually combined with simultaneous decision feedback equalization [8].

Use of an AGC structure as described in [9] permits subtraction of all components associated with the far-end signal from the error signal used to adapt the coefficients. This requires use of a four phase clock. The first two phases are used to perform the transversal filtering operation associated with the echo cancellation and simultaneous decision feedback equalization. A decision is made regarding the received bit. An AGC tap is then weighted by the present bit and subtracted, yielding at the output of the summing amplifier the true cancellation error, which is used during the last phase to correct the coefficients. Since the error is free from received signal components, a high gain with corresponding rapid convergence can be used in the adaptation algorithm. A value of α=0.03 has been successfully used in a breadboard implementation of a

16 tap echo canceller combined with a 16 tap equalizer we built using this technique.

Since no well-proven techniques exist to perform timing recovery when the canceller samples synchronously at the received pulse rate, one must consider the asynchronous echo canceller as described in Section 2. In this instance, the far-end data signal cannot be removed from the error signal driving the canceller, and as a result an extremely low gain is required in the adaptive algorithm. This low gain cannot be reliably implemented with analog techniques. Thus, we have given no further consideration to the analog approach.

3.1.2. Fully Digital Echo Canceller

In this approach, shown in Fig. 4b, the canceller is implemented entirely with digital logic, and the received signal is sampled and A/D converted prior to the cancellation. This technique was used in the first breadboard version of the echo canceller described in Section 3.4. A monolithic implementation of this technique is impractical at present because A/D converters of adequate resolution and linearity have not been demonstrated in MOSLSI. Advances in monolithic data converters may change this situation in the future. For this reason, we will further analyze the effect of nonlinearities in the A/D converter in Section 3.2. A nonlinear echo cancellation approach discussed in another paper [11] would be applicable to this realization, but would be considerably more complicated than for the technique of Fig. 4c, as will be discussed in Section 3.2.

3.1.3. Digital Echo Canceller with Analog Cancellation

This implementation, is shown in Fig. 4c, uses an all-digital implementation of the canceller and converts the echo replica to analog using a D/A converter prior to cancellation in the analog domain. Resolution requirements for the data converters are reported in [2], where it is shown that at least 12 bits is required.

Not explicitly mentioned in that reference is the fact that 1/2 LSB integral linearity is also required in the D/A. MOS monolithic D/A converters of the required speed and resolution have been demonstrated [10]; however, the integral linearity of these converters cannot be guaranteed to be better than 7 or 8 bits unless laser trimming is used. Nonlinear distortion in the D/A greatly degrades the echo cancellation, as shown in Section 3.2. A low cost implementation of the system precludes the use of laser trimming, making this alternative not directly applicable to the monolithic implementation of the echo canceller. A technique in which nonlinear distortion introduced by the D/A and other sources is corrected digitally by a nonlinear echo cancellation algorithm is the subject of another paper [11] and will not be discussed here.

Since the A/D is used only to generate a feedback signal for the adaptation algorithm, it must be monotonic, but not necessarily linear. Furthermore, a resolution of only 8 bits is required [2]. The MOS monolithic implementation of these converters poses no major problems.

3.1.4. Analog/Digital Echo Canceller

An architecture in which the convolution sum and the echo cancellation are performed with analog techniques is shown in Fig. 4d. The adaptation algorithm is performed digitally, and the tap weights are converted to analog using a single time-shared D/A converter. The multiplications and additions are then performed in the charge domain, where the nonlinear distortion can be kept very small without special circuit design effort.

Since a large dynamic range and slow time-constant is still required in the adaptation algorithm, it cannot be implemented by analog means. Thus the use of a digital processor to perform the adaptation, while a switched capacitor analog transversal filter computes the convolution sum and cancels the echo in the received signal. The coefficients of the transversal filter are stored in sample

and hold (S/H) capacitors (Fig. 5) and refreshed periodically by the digital adaptation processor. In order to reduce the required speed of the D/A converter, only one of the S/H capacitors is refreshed each pulse period; however, all are updated in the digital processor. The consequences of this for echo canceller convergence are shown in the next Section to be negligible. The possibility of a slow D/A converter in this approach represents a significant advantage, since slow operation could be traded off for increased resolution and reduced die area and power consumption.

The design of the A/D converter for the cancellation error, as in the realization of Fig. 4c, represents no particular difficulty.

The effect of the inevitable nonlinearity in a monolithic D/A (or A/D) converter without laser trimming will be carefully considered in the next Section for the architectures of Fig. 4b, 4c, and 4d. It will be shown that Fig. 4d is the least sensitive to converter nonlinearity. This is due to the ability of the adaptation algorithm to compensate for any nonlinearity which is continuous and monotonic.

3.2. Effect of D/A Nonlinearity

In this section we analyze both theoretically and by computer simulation the effect of D/A (or A/D) nonlinearity on the echo canceller configurations of Figs. 4b, 4c, and 4d. In the process we will also be able to characterize the effect of any nonlinearities in the echo response, such as are introduced by transmitted pulse asymmetry.

It is natural to assume that the current echo sample or alternatively the current sample at the canceller output is given by some time-invariant but otherwise arbitrary nonlinear function of the current and last $N-1$ transmitted bits. Let C_k denote the current nominal transmitted level, which for purposes of this Section we will assume takes on the values $+1$ and -1 (other cases can be

handled similarly). It is shown in [11] that an arbitrary time-invariant nonlinear function of the current and the last N-1 bits $h(C_k, \ldots, B_{k-N+1})$ can be represented by the following expansion, which is analogous to a Volterra series expansion in continuous amplitude signals,

$$\begin{aligned} h(C_k, \ldots, C_{k-N+1}) = h_0 &+ \sum_{n=0}^{N-1} h_1(n) C_{k-n} \\ &+ \sum_{n_1 \neq n_2} h_2(n_1, n_2) C_{k-n_1} C_{k-n_2} \\ &+ \cdots \\ &+ \sum_{n_1 \neq n_2 \neq \cdots \neq n_L} h_L(n_1, n_2, \cdots, n_L) C_{k-n_1} C_{k-n_2} \cdots C_{k-n_L} \\ &+ \cdots \\ &+ h_N C_k C_{k-1} \cdots C_{k-N+1} \end{aligned} \tag{3.2.1}$$

where the general $L-th$ order sum is over all combinations of L of the N transmitted bits. The total number of terms is in this expansion is 2^N, which is the same as the number of values that the function h assumes.

This expansion can be used to represent both the echo response and the canceller output in the presence of arbitrary time-invariant nonlinearities. As a simplification of notation it is useful to define the "augmented transmitted symbol vector"

$$\begin{aligned} \mathbf{c}_k = (1, &C_k, \cdots, C_{k-N+1}, \\ &C_k C_{k-1}, C_k C_{k-2}, \cdots, C_{k-N+2} C_{k-N+1}, \\ &\cdots, C_k C_{k-1} \cdots C_{k-N+1})^T \end{aligned} \tag{3.2.2}$$

where the superscript T denotes transpose. There are 2^N components in this vector, one for each of the terms in (3.2.1). Also define the 2^N-dimensional vector

$$\mathbf{h} = (h_0, h_1(0), h_1(1), \ldots, h_1(N-1), h_2(0,1), \ldots, h_2(N-2, N-1), \ldots, h_N)^T \quad . \tag{3.2.3}$$

Then the expansion of (3.2.1) can be represented as the inner product

$$h(C_k, \ldots, C_{k-N+1}) = \mathbf{c}_k^T \cdot \mathbf{h} \ . \qquad (3.2.4)$$

When the data digits C_k are mutually independent and assume the values +1 and −1 with equal probability, it is easy to show that the components of the vector $\mathbf{c}_k$ are uncorrelated. This fact will be used when calculating the effect of nonlinearities in the canceller.

This nonlinear expansion can be used to determine the effect of nonlinearities in the echo response. For the general nonlinear case, if it is assumed that the current echo sample is a (nonlinear) function of the current and last $N-1$ data bits, then it can be written in the form

$$e_k = \mathbf{c}_k^T \cdot \mathbf{g} \qquad (3.2.5)$$

where $\mathbf{g}$ is an "augmented echo path vector" of the same form as (3.2.3) which has 2^N components. For the case of a linear echo response, only the components $g_1(0), \ldots, g_1(N-1)$ of vector $\mathbf{g}$ are nonzero (and equal to the samples of the echo path impulse response).

The representation of the canceller output is different for each of the three cases of Fig. 4c, 4d, and 4b so that they will now be considered separately.

3.2.1. Nonlinear Distortion in Fig. 4c

For the configuration of Fig. 4c, it is assumed that the D/A converter has an inherent undesired nonlinearity $d(\cdot)$. Since techniques are available to implement D/A converters which are inherently monotonic and have no discontinuities, it is reasonable to assume that the function $d(\cdot)$ is monotonically increasing and continuous. This implies that the inverse function $d^{-1}(\cdot)$ exists. The canceller can then be modelled as a linear combination of the N data bits followed by the nonlinear function $d(\cdot)$,

$$e_k = d\left(\sum_{n=0}^{N-1} a(n) C_{k-n}\right) \qquad (3.2.1.1)$$

where the tap-weights in the canceller summation are the $a(n)$. Since (3.2.1.1)

is a general nonlinear function of the form of (3.2.1), it can be written in the form

$$e_k = \mathbf{c}_k^T \cdot \mathbf{D}[\mathbf{a}] \qquad (3.2.1.2)$$

where $\mathbf{a}$ is the N-dimensional tap-weight vector and $\mathbf{D}[\mathbf{a}]$ is a 2^N-dimensional vector induced by the nonlinear function $d(\cdot)$. We thus see that the effect of the D/A nonlinearity is to add the terms of order two and higher in the expansion of the form of (3.2.1) into the echo replica. Those added terms are uncorrelated to the echo when the echo response is assumed to be linear, and contribute together with the noise and far-end data to the residual mean squared cancellation error.

The cancellation error is

$$r_k = \mathbf{c}_k \cdot (\mathbf{g} - \mathbf{D}[\mathbf{a}]) + s_k + n_k \qquad (3.2.1.3)$$

where s_k is the far-end signal and n_k is the noise. Since all the terms in (3.2.1.3) are uncorrelated, including the components of $\mathbf{c}_k$, the mean squared error (MSE) is

$$\rho = (\mathbf{g} - \mathbf{D}[\mathbf{a}])^T \cdot (\mathbf{g} - \mathbf{D}[\mathbf{a}]) + E[s_k^2] + E[n_k^2] \qquad (3.2.1.4)$$

where E stands for expected value. The condition for minimum MSE is to choose $\mathbf{a}$ so as to minimize the first term in (3.2.1.4). Because $\mathbf{a}$ only has N components, in general it is not possible to force this term to zero, even when the echo response is linear, except of course when $d(\cdot)$ is linear. The minimization of the MSE is further discussed in [11], where it is shown that in the case of small nonlinearity the familiar gradient technique applies.

The net effect of nonlinear distortion is to increase the residual error after cancellation, since it causes the first term in (3.2.1.3) to be non-zero. Further understanding of this effect can be obtained by grouping the terms in (3.2.1.3) in the manner

$$r_k = \sum_{n=0}^{N-1} [\mathbf{g} - \mathbf{D}[\mathbf{a}]]_{n+1} C_{k-n} + [\mathbf{g} - \mathbf{D}[\mathbf{a}]]_0 + v_k + s_k + n_k \qquad (3.2.1.5)$$

where the notation $[\cdot]_n$ denotes the n-th component of the vector. The first term in this residual cancellation error is a linear distortion which will be present due to the nonlinearity in the D/A. The minimum MSE is not necessarily achieved when the first term vanishes, since the second and third terms of (3.2.1.5) are also functions of **a**. The second term is a d.c. offset due to the nonlinearity, while v_k represents all the accumulated nonlinear distortion terms (defined as terms containing a product of two or more data bits). It is perhaps surprising that all these terms are uncorrelated with one another.

The representations of (3.2.1.3) through (3.2.1.5) are useful for gaining insight into the nature of the distortion introduced by the D/A nonlinearity. When it is desired to compute the MSE of the cancellation residual, however, it is more convenient to use the simpler relation

$$\rho = E[\mathbf{c}_k \cdot \mathbf{g} - d(\sum_{n=0}^{N-1} a(n) C_{k-n})]^2 + E[s_k^2] + E[n_k^2] \ . \qquad (3.2.1.6)$$

The additional residual echo introduced by D/A nonlinearity is illustrated by the computer simulations of the adaptive canceller shown in Fig. 6. A second order nonlinearity bx^2 in the D/A transfer function was considered here. The ratio of the mean squared error (averaged over 1000 samples) to the mean squared echo is plotted for b =0, 0.01, 0.005, and 0.001 . In order to achieve 60 dB of cancellation b must be less than 0.001, which requires 12 bit integral linearity in the D/A.

3.2.2. Nonlinear Distortion in Fig. 4d

Let $d_n(\cdot)$ be the nonlinear transfer function of the D/A combined with the nonlinear transfer function of the n^{th} S/H in Fig. 5. By allowing for nonlinearity and offset in the S/H's, their design can be simplified and chip area can be saved. Moreover, as we shall see later, the adaptation algorithm can easily

compensate for these impairments in the structure of Fig. 4d.

The echo replica in this instance is

$$e_k = \sum_{n=0}^{N-1} d_n(a(n))C_{k-n} \qquad (3.2.2.1)$$

If we define a new 2^N-component tap-weight vector

$$\mathbf{D}[\mathbf{a}] = (0,d_0(a(0)),d_1(a(1)),\ldots,d_{N-1}(a(n-1)),0,\ldots,0) \qquad (3.2.2.2)$$

which has only the N non-zero linear taps, then the cancellation error and MSE are again given by (3.2.1.3) and (3.2.1.4) with the new definition of $\mathbf{D}[\mathbf{a}]$. In this instance the condition for minimization of the MSE is much simpler; namely, from (3.2.1.4)

$$a(n) = d_n^{-1}(g_1(n)) \qquad (3.2.2.3)$$

which is valid whether or not the echo response is linear. As before the assumption of the existence of $d_n^{-1}(\cdot)$ is reasonable. While nonlinearity in the echo response does not affect the optimal tap-weight vector in (3.2.2.3), it will cause excess MSE in the minimized MSE as seen from (3.2.1.4). When the echo response is linear, the first term in (3.2.1.4) can be forced to zero, and there is no excess residual echo. This represents a significant advantage of the technique of Fig. 4d over 4c.

The MSE can be minimized adaptively using the gradient technique. The gradient of ρ is

$$(\nabla\rho)_n = -2(g_1(n)-d_n(a(n)))\cdot\frac{\partial d_n(a(n))}{\partial a(n)} \qquad (3.2.2.4)$$

Because $d_n(\cdot)$ is monotonic, $\frac{\partial d_n(a(n))}{\partial a(n)}$ is never zero, and hence the only minimum of ρ is associated with the solution (3.2.2.4), so that the gradient technique will be able to find the minimum. Furthermore, since for practical situations $\frac{\partial d_n(a(n))}{\partial a(n)}$ is close to unity (because the nonlinear distortion is small), the nonlinearity does not significantly slow convergence. As usual the gradient is

replaced by a noisy estimate, and the algorithm becomes

$$a_{k+1}(n) = a_k(n) + 2\alpha r_k C_{k-n} \qquad (3.2.2.5)$$

where a subscript k has been added to the tap-weights to indicate that they are now functions of time.

A further modification of the algorithm is introduced by the fact that in Fig. 5 the error is computed using the values of the coefficients stored in the S/H, which are not the latest versions since only one S/H is refreshed each pulse period (although the latest versions of *all* the coefficients are always available in the memory of the digital processor, refreshing only one S/H at a time considerably relaxes the speed requirements of the D/A). Thus in the definition of D[a] in (3.2.2.2), $a_k(n)$ must be replaced by $a_{k-m(n)}(n)$ where $m(n)$ is a cyclic permutation of the sequence (0,1,...,N-1). Which one of the N possible cyclic permutations it is depends on the initialization of the selector circuit, but no attempt is made to control that parameter. Since α is very small, the coefficients change very slowly and this modification does not appreciably alter the convergence.

The preceding analysis has been verified by computer simulation. Fig. 7 shows the convergence transient of the echo canceller when no external signal is present and an infinite resolution A/D converter is used. DAC's with 10 to 13 bits resolution and with infinite resolution were considered. It is interesting to observe that the speed of convergence is still experimentally determined to be

$$\nu_{20} = \frac{1.15}{\alpha} \qquad (3.2.2.8)$$

as predicted in [2], in spite of the modifications introduced in the algorithm. Although one particular case of nonlinearity is shown, we experimented with different nonlinearities and even with independent nonlinear functions for each tap (in anticipation of possibly different S/H nonlinearities), with results very similar to those of Fig. 7. We conclude that this technique is extremely insensi-

tive to nonlinear distortion in the D/A converter. It cannot, however, compensate for nonlinearities in the echo response, as can the technique described in [11].

3.2.3. Nonlinear Distortion in Fig.4b

The effect of nonlinear distortion in the all-digital organization of Fig. 4b is somewhat more involved than the previous two cases. That is why it was relegated to the end of this discussion. Since in Fig. 4b the nonlinear distortion introduced by the A/D affects the input signal *before* echo cancellation, intermodulation components between the far-end signal and the echo will be created. To see this in detail, let now $\{x_k\}$ be the sequence of transmitted bits (in slight departure from the previous notation) and $\{y_k\}$ the sequence of bits transmitted from the far-end of the line. Furthermore, let us assume that the received signal is a nonlinear function of only the last N near-end and M far-end transmitted bits. We can now define an $(N+M)$-dimensional transmitted symbol vector $\mathbf{C}_k$, such that

$$\mathbf{C}_k = (x_k, x_{k-1}, \ldots, x_{k-N+1}, y_k, y_{k-1}, \ldots, y_{k-M+1}) \qquad (3.2.3.1)$$

and a $2^{(N+M)}$-dimensional augmented transmitted symbol vector $\mathbf{c}_k$, defined as in (3.2.2), but with $(N+M)$ replacing N. An "augmented channel vector" $\mathbf{g}$ can also be defined such that for the most general nonlinear case, the input signal to the receiver is $\mathbf{c}_k^T \cdot \mathbf{g}$. If both the transmission and the echo path are linear, $\mathbf{g}$ will have only $(N+M)$ (out of $2^{(N+M)}$) nonzero components, which are the components $g_1(0), \ldots, g_1(N+M)$. The first N of them are the samples of the echo path impulse response, and the last M are the samples of the transmission path impulse response.

If a nonlinear A/D with transfer function $d(\cdot)$ is used in Fig. 4b, the input to the receiver is:

$$u_k = d(\mathbf{c}_k^T \cdot \mathbf{g}) = \mathbf{c}_k^T \cdot \mathbf{D}[\mathbf{g}] \qquad (3.2.3.2)$$

where $\mathbf{D}[\mathbf{g}]$ is a $2^{(N+M)}$-dimensional nonlinear transformation of $\mathbf{g}$. In general, all components of $\mathbf{D}[\mathbf{g}]$ may be different from zero, even when the echo response is linear. The terms of (3.2.3.2) which are linear functions of the near-end transmitted bits represent a linear echo. The terms which are linear functions of the far-end transmitted bits represent a linear received signal. The nonlinear terms in (3.2.3.2) include an offset term and, in addition,

a) *Nonlinear echo components* consisting of nonlinear interactions among the local transmitted data bits,

b) *Nonlinear far-end signal components* consisting of nonlinear interactions among the far-end transmitted data bits, and

c) *Intermodulation terms* consisting of nonlinear interactions among local and far-end transmitted signal bits.

All these nonlinear terms represent an uncancellable noise for a linear echo canceller.

A nonlinear echo canceller as described in [11] could remove component (a). In order to remove (b) and (c), a generalized transversal filter structure which is a nonlinear version of Mueller's combined echo cancellation and decision feedback equalization [8] could be used. This transversal filter would generate the most general nonlinear function of the last N transmitted and the last M received bits. However such a structure would be impractical because of the requirement for synchronous operation between the near-end and the far-end systems, as discussed in Section 3.1.1.

3.3. An Experimental Integrated Circuit Echo Canceller

From the analysis of Section 3.2, it is clear that the configuration of Fig. 4d is the most attractive of those presented for MOS realization. (Another attractive approach is discussed in [11].) This approach has been experimentally

evaluated by fabricating an MOS chip that implements the functions shown within dotted lines in Fig. 5. Two 8-tap programmable transversal filters operate in time-interleaved fashion, sampling at twice the data rate.

A circuit schematic is shown in Fig. 8. The data bits are shifted through the dynamic shift register formed by $E_n^{(1)}$ and $E_n^{(2)}$, where the subscript n identifies the tap number and the superscript (1,2) indicates which one of the 2 time-interleaved section is being considered. Capacitors $C_{A,n}^{(i)}$ are the sample and hold capacitors, with the associated sampling switch $M_{3,n}^{(i)}$ and source follower buffer $M_{1,n}^{(i)}$, $M_{2,n}^{(i)}$. Summing capacitors $C_{B,n}^{(i)}$ are initialized to ground when the corresponding data bit is 0, and to the S/H coefficient when the bit is 1. At the same time the input signal is sampled by capacitor C_s. During the next clock phase the position of the switches associated with the summing capacitors and with capacitor C_s are reversed, and the quantity

$$r_k = s_k - \sum_{n=1}^{N} a(n) x_{k-n} \qquad (3.3.1)$$

is computed in the charge domain and appears at the output of the summing amplifier.

While Section 3.2 concentrated on the effect of the D/A nonlinearity, in the context of Fig. 4d the following additional factors are worth considering:

1) *Linearity requirements on the sample /hold (S/H) circuits.*

2) *Linearity and gain requirements on the summing amplifier.*

3) *Linearity requirements on the sampling capacitors.*

With respect to 1), the S/H's are implemented as capacitors buffered by source followers. No attempt was made to linearize them or compensate their offset, since their effect is the same as D/A nonlinearity and is therefore taken care of by the adaptation algorithm, as shown in the Section 3.2. By keeping the S/H simple much die area can be saved, since a total of 16 are implemented on

chip.

To consider points 2) and 3), refer to Fig. 9, and assume that voltages

$$\begin{array}{l} V_1(2)-V_1(1) \\ \text{and} \\ V_2(2)-V_2(1) \end{array} \qquad (3.3.2)$$

are to be added using a switched capacitor summing amplifier as shown. The arguments 1 and 2 refer to the sampling and charge redistribution phases. This serves as a model of a single-tap transversal filter, with $V_1(1)$ equal to the input signal with echo, $V_1(2)=0$ and either

$$\begin{array}{l} V_2(1) = tap\ coefficient \\ V_2(2) = 0 \\ \text{or} \\ V_2(1) = 0 \\ V_2(2) = tap\ coefficient \end{array} \qquad (3.3.3)$$

depending on whether a weight of +1 or -1 is given to the tap coefficient (as determined by the corresponding data bit). The conclusions extracted from this simple model can be easily extended to a multitap transversal filter. Let also

$$V_0(k) = A(V_-(k)) \quad (k=1,2) \qquad (3.3.4)$$

be the (nonlinear) transfer function of the summing amplifier. It is *not* assumed here that the gain of the amplifier is high. Finally, let

$$q_r = h_r(V) \quad (r=0,1,2) \qquad (3.3.5)$$

define the (possibly nonlinear) capacitors of Fig. 9. Using charge conservation,

$$\begin{array}{l} h_0[A(V_-(2))-V_-(2)]-h_0(0) \\ = [h_1(V_1(1)-V_-(1))-h_1(V_1(2)-V_-(2))] + \\ + [h_2(V_2(1)-V_-(1))-h_2(V_2(2)-V_-(2))] \ . \end{array} \qquad (3.3.6)$$

In the case of linear capacitances

$$h_r(V) = C_r V \qquad (3.3.7)$$

and Eq. (3.3.6) becomes:

$$C_0[A(V_-(2))-V_-(2)] + (C_1+C_2)\,\Delta V_- = C_1\,\Delta V_1 + C_2 \Delta V_2 \qquad (3.3.8)$$

where

$$\Delta V_k = V_k(1) - V_k(2)$$

Solving (3.3.8) for $V_-(2)$, using the fact that $V_-(1)$ is a constant (the offset of the amplifier) and also using (3.3.4), the output $V_0(2)$ can be found as a function of the *linear* combination

$$C_1\Delta V_1 + C_2\Delta V_2 \tag{3.3.9}$$

This shows that in the case of *linear capacitors*, the nonlinear distortion of the summing amplifier affects the total sum, which for the echo canceller of Fig. 5 is the *residual signal*, after echo cancellation. Thus no uncancellable echo distortion components, or intermodulation components between the received signal and the echo, are created. Observe that this is true even in the case when the amplifier gain is relatively low, since no high gain assumption has been made.

Now consider the effect of a voltage coefficient in the capacitors. Assume that

$$h_k(V) = C_k V(1+\gamma V) \tag{3.3.10}$$

Then, substituting in (3.3.6) and collecting terms, it can be seen that the linear combination of (3.3.9) is corrupted by the distortion term:

$$\begin{aligned}&\gamma C_1[(V_1(1)-V_-(1))^2-(V_1(2)-V_-(2))^2] + \\ &\gamma C_2[(V_2(1)-V_-(1))^2-(V_2(2)-V_-(2))^2]\end{aligned} \tag{3.3.11}$$

Since only an upper bound for the voltage coefficient γ is required, let us assume that all the voltages in (3.3.11) are bounded by some voltage V_{max}. Then, in order to ensure a distortion lower than -60 dB, all we require is:

$$\gamma V_{max} \ll 10^{-3} \tag{3.3.12}$$

In MOS technology, low voltage coefficient capacitors can be easily obtained. One option is to use poly to poly capacitors, if a process with double layer of polysilicon is available. Another option (the one we used) are poly to n+ capacitors. A high dose implant forms the bottom plate of the capacitors, providing adequately low voltage coefficients. Reference [12] gives a voltage coefficient as low as 20 ppm for a bottom plate dope of $10^{20}\ cm^{-3}$. This ensures that (3.3.12) is

satisfied.

Figure 10 shows a photograph of the chip, fabricated in NMOS silicon gate process with 7 μm design rules. Chip size is 3 mm on each side (between centers of scribe lines). The area of the active parts is 1.5 mm^2, and can be decreased using smaller S/H capacitors (instead of the conservative 20 pF used here) and a more advanced process.

3.3.1. Experimental Results

An experimental breadboard modem has been built as described in Section 2. The first version used a completely digital processor built using 2901 bit slice microprocessors, with a 12 bit analog to digital converter at the input and a digital to analog converter at the output (Fig. 4b). This D/A converter had adequate linearity for this application, but for the reasons described earlier could not be realized in MOSLSI without trimming. The design of the digital processor followed criteria given elsewhere [2]. Internal arithmetic precision of the entire processor was 24 bits. The gain factor α of equation (16) of reference [2] could be chosen in our implementation over the range 2^{-13} to 2^{-17}.

The modem has received extensive laboratory as well as field testing, with line attenuations up to 44 dB. The field test was performed in Ora Loma, California, is a small (300 line) local office where the crosstalk and impulse noise impairments were minimal. Subscriber loops were remotely looped back so that both ends of the subscriber loop were available in the office. Because of the relatively ideal nature of this environment, these tests can be considered as indicative of the capabilities of the canceller itself in a realistic echo response environment, but not representative of the effect of crosstalk and impulse noise in a more severe environment. This is consistent with our goal of studying the effect of impairments due to the echo canceller implementation.

The degree of cancellation achieved was measured by measuring the SNR at the input and output of the canceller. Specifically, both SNR's were determined by measuring the peak far-end signal voltage (with the local transmitter turned off) and the peak echo signal (with the far-end signal turned off). By this measurement technique, the achieved degree of cancellation was 63 *dB*. Error rate measurements showed a BER (bit error rate) lower than 10^{-8} with line attenuations at 40 kHz up to 40 dB. BER increased to 10^{-4} when the line attenuation was 44 dB. This increase was attributed not to the echo canceller, but rather the noise from the digital circuitry and the effect of equalization errors due to the very simple equalizer that was used.

Figure 11 shows the eye diagram at the output of the transmitter. Figure 12a shows the eye diagram at the input of the echo canceller with the local transmitter turned off, while Fig. 12b shows the signal at the same point with the local transmitter on and set to the nominal output level of 600 mV peak. Note the different scales in the two pictures. Prior to echo cancellation, the echo was about 38 dB higher than the far-end signal. The eye diagram of the echo signal is closed because the equalizer has been adjusted to open the received signal eye, not the eye for the echo. Fig. 13 shows the eye diagram at the output of the echo canceller when operating with a line attenuation of 40 dB. The quantization error as well as the sampled nature of the signal can be clearly observed.

Impulse noise was the dominant source of errors we observed in both laboratory and field testing. Impulse noise almost always caused a single bit error on the line, which expanded to three errors in passing through the scrambler. Such errors are inconsequential for voice communication. For data communication, error detection followed by re-transmission might well provide a satisfactory solution. Alternatively, a simple form of burst error-correcting code would be highly effective in overcoming the impulse noise errors we observed. Digital circuitry for such encoding could be included on the same chip as the

functions described above.

Measurements were made to determine the magnitude of near-end crosstalk from other (unsynchronized) channels at 80 kb/s on adjacent pairs in typical cables. Of course, such crosstalk could not be reduced by the echo canceller. Measured crosstalk was at -70 to -80 dB relative to the transmitted signal level for a single interferer. At these levels, near-end crosstalk is not a limitation.

A custom chip has been built to evaluate the effect of nonlinear distortion in the digital-to-analog converter using the favorable technique of Fig. 4d. The chip performs only the transversal filtering operation, while the adaptation is performed off-chip by a digital processor, using again 2901 bit slice microprocessors. The A/D and D/A were also implemented off-chip.

Figure 14 compares the eye diagrams of the breadboard and the custom chip when operating with a line attenuation of 26 dB. The maximum measured echo cancellation of the modem using the custom chip (measured as previously described) was 40 dB, with the limiting factor being not nonlinear distortion but digital noise picked up by the analog circuits. In fact, the nonlinearity of the sample and hold circuits alone would have limited the cancellation to approximately 20 dB were the adaptation not able to compensate for this nonlinearity. We are confident that this 40 dB of cancellation can be substantially improved with additional effort in designing circuits with better common mode and power supply rejection ratios. In addition, monolithic integration of the entire modem would reduce the problems of digital noise pickup experienced in both implementations.

3.4. Integration of a Full-Duplex Hybrid Modem

We have made rough estimates of the die size and complexity of a complete MOSLSI realization of the system described in this paper. Figure 15 shows

approximate areas that would be required by the different functions to be implemented on-chip. The essential element of such a chip would be the analog-digital echo canceller discussed in previous sections of this paper. Switched-capacitor filters would be used at the input and output and for timing recovery. Phase-locked loop design in MOSLSI is described elsewhere [13]. Area would be about 30 mm^2, power dissipation 300 mW and transistor count about 6000, based upon use of a silicon-gate NMOS process with a minimum feature size of 5 μm. Density would be increased and power reduced through use of a more advanced fabrication process.

4. Conclusions

The design of the echo canceller for a hybrid-mode full-duplex data modem has been considered based upon analysis, simulation, and experimental studies. This paper has focussed on the effect of impairments introduced by the implementation of the echo canceller itself in MOSLSI. Techniques have been proposed which should eliminate these implementation-induced impairments as limitations on the modem performance, so that performance can approach fundamental limits determined by noise, crosstalk, and cable attenuation.

An experimental system was built, and tried out in a field environment. Again, the emphasis was on checking the performance of the echo canceller itself, rather than other system impairments. Measured performance of the experimental system was excellent.

It may well be possible to increase the transmitted bit rate to 144 kb/s for a system of this design. Measurements on real loops confirmed that attenuation is proportional to the square root of frequency. A very large fraction of all loops would show attenuation of 40 dB or less at 144 kb/s. Most importantly, circuit speed for the implementation approach proposed in this paper is certainly no barrier to 144 kb/s operation.

5. Acknowledgements

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Appendix A

This Appendix will establish that the components of the transmitted data signal at multiples of the bit rate is a direct and useful measure of transmitted pulse asymmetry. As is well known, the bipolar encoded signal has zeros in the power spectrum at all harmonics of the bit rate. This Appendix will show that in the presence of pulse asymmetry the transmitted signal in fact has a line component at the bit frequency.

Assume that the transmitted data bits assume the values $C_k = +1$ and $C_k = -1$, that the difference of successive data values are used to modulate a train of pulses, and that there is a asymmetry in the pulses such that a positive pulse has shape $h_+(t)$ and negative pulse has shape $h_-(t)$. Then the transmitted signal can be represented as

$$x(t) = \sum_k (f_+(C_{k-1}, C_k)h_+(t-kT) + f_-(C_{k-1}, C_k)h_-(t-kT)) \tag{A.1}$$

where f_+ is 1 when $C_k = 1, C_{k-1} = -1$, and 0 otherwise, and similarly f_- is 1 only when $C_k = -1, C_{k-1} = 1$. Since f_+ and f_- are nonlinear functions of C_k and C_{k-1}, the expansion of (3.2.1) is valid and it is simple to show that

$$\begin{aligned} f_+(C_{k-1}, C_k) &= \frac{1 + C_k - C_{k-1} - C_k C_{k-1}}{4} \\ f_-(C_{k-1}, C_k) &= \frac{1 - C_k + C_{k-1} - C_k C_{k-1}}{4} . \end{aligned} \tag{A.2}$$

Thus, (A.1) becomes

$$\begin{aligned} x(t) = &\frac{1}{4}\sum_k (1 - C_k C_{k-1})(h_+(t-kT) - h_-(t-kT)) \\ &\frac{1}{4}\sum_k (C_k - C_{k-1})(h_+(t-kT) + h_-(t-kT)) \end{aligned} \tag{A.3}$$

which demonstrates the nature of the nonlinearity introduced when there is pulse asymmetry: nonlinear distortion in the form of second order products of adjacent bits is introduced into the transmitted signal. This demonstrates the terms which would have to be added to the nonlinear canceller in [11] to compensate for pulse asymmetry.

Assume that the data bits C_k are independent and assume the value +1 with probability p. Then the average value of the transmitted signal is easily determined from (A.3) to be

$$E[x(t)] = p(1-p)\sum_k (h_+(t-kT) - h_-(t-kT)) \quad . \tag{A.4}$$

The total signal can then be written as a zero-mean random component plus the deterministic component of (A.4). The random component will have a continuous power spectrum, while the deterministic component consists of a line spectrum since it is periodic in T sec. Expanding (A.4) in a Fourier series,

$$E[x(t)] = \frac{p(1-p)}{T}\sum_n (H_+(n\frac{2\pi}{T}) - H_-(n\frac{2\pi}{T})) \quad . \tag{A.5}$$

Thus, the transmitted signal contains line components at multiples of the bit rate due to the pulse asymmetry. Taking into account the effect of the transmit filter, the only significant component will be that at the bit rate, which is proportional to the difference of the Fourier transforms of the positive and negative pulses at that frequency. As expected, this undesired component is maximum when the data is equally likely, and goes away when the data is always one polarity since the transmitted signal is zero in this case. Of course, it also goes away when the positive and negative pulses are equal, or even if they only have equal Fourier transforms at the bit frequency.

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Figure Captions

Fig. 1. A digital subscriber loop using echo cancellation techniques. Specifications include 40 dB of line attenuation, 10 dB of transhybrid loss, and 50 dB of required echo cancellation, for 20 dB of signal to noise ratio after cancellation.

Fig. 2. Block diagram of a baseband full-duplex modem.

Fig. 3. Clamping a CMOS gate provides symmetric pulses for transmission.

Fig. 4. a) Analog echo canceller. b) Digital echo canceller. c) Digital transversal filter with analog cancellation. d) Analog-digital echo canceller.

Fig. 5. Analog-digital echo canceller in more detail.

Fig. 6. Computer simulations of D/A nonlinear distortion effects. The convergence transient is shown for various degrees of D/A nonlinearity. Nonlinearity causes a saturation of the error characteristic.

Fig. 7. Computer simulation of convergence transient in echo canceller of Fig. 5. For the ideal case of infinite resolution, no limitations exist on the final amount of cancellation even in presence of DAC nonlinearity.

Fig. 8. a) Circuit schematic of transversal filter. Circuitry inside each box "Tap n" is shown in (b). $(Sample)_n^i$ represents the sampling signal for the S/H of tap n of the i^{th} of the two interleaved sections of the filter (i=1,2). b) Circuit schematic of tap n of echo canceller. Superscript (i) identifies each one of the two interleaved sections of the transversal filter.

Fig. 9. Model of a single-tap transversal filter to compute effect of nonlinearity.

Fig. 10. Experimental echo canceller chip.

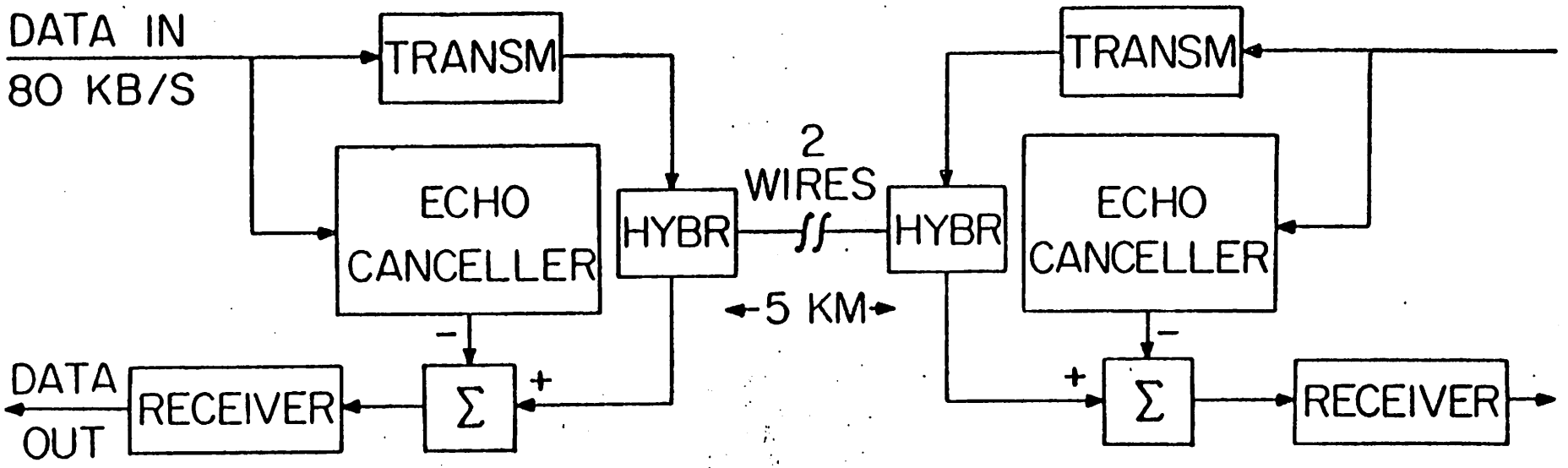
Fig. 11. a) Eye diagram at the output of the transmitter.Peak transmitted signal is 600 mV. b) Spectrum of transmitted signal at the output of the transmitter (top trace) and on an adjacent pair (bottom trace). Crosstalk loss is 70 dB. Also seen is the crosstalk from analog carriers above 80 kHz.

Fig. 12. Eye diagram at the input of the echo canceller. a) With local transmitter off. Scale: 20 mV/cm, 5 μs /cm. b) With local transmitter on. Scale: 1 V/cm, 5 μs /cm.

Fig. 13. Eye diagram at output of echo canceller with 40 dB of line attenuation.

Fig. 14. Eye diagrams at the outputs of the 2 receivers. a) Using the echo canceller of Fig. 4d. b) Using the echo canceller of Fig. 4b.

Fig. 15. Area and power dissipation estimates for a monolithic hybrid mode modem.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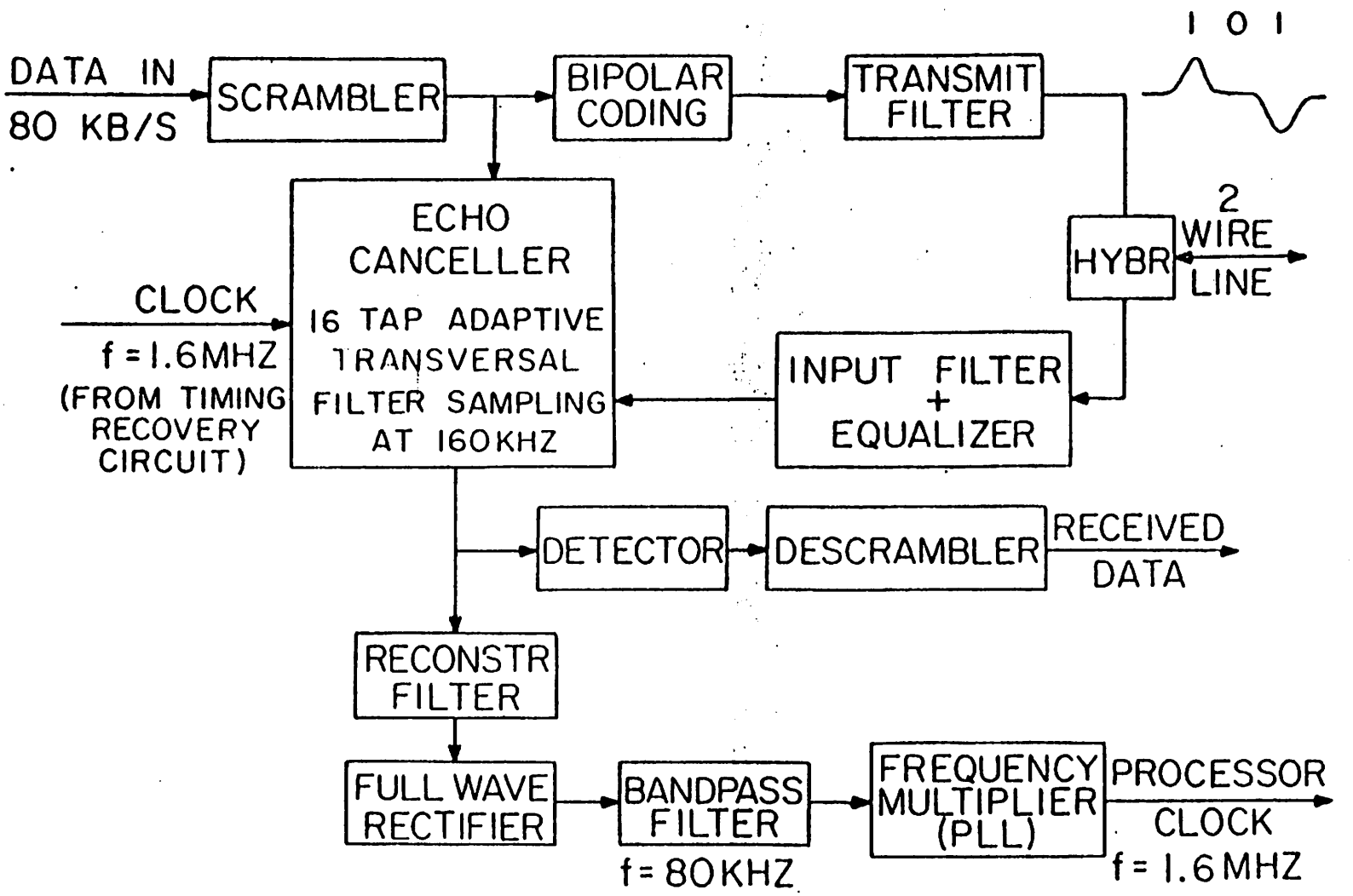
80 KB/S
TRANSM
ECHO
CANCELLER
HYBR
2
WIRES
HYBR
TRANSM
ECHO
CANCELLER
5 KM
DATA
OUT
RECEIVER
Σ
Σ
RECEIVER

Fig. 1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SCRAMBLER
BIPOLAR CODING
TRANSMIT FILTER
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2 WIRE LINE
HYBR
ECHO CANCELLER
16 TAP ADAPTIVE TRANSVERSAL FILTER SAMPLING AT 160KHZ
CLOCK
f = 1.6MHZ
(FROM TIMING RECOVERY CIRCUIT)
INPUT FILTER + EQUALIZER
DETECTOR
DESCRAMBLER
RECEIVED DATA
RECONSTR FILTER
FULL WAVE RECTIFIER
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PROCESSOR CLOCK
f = 1.6 MHZ

Fig. 2

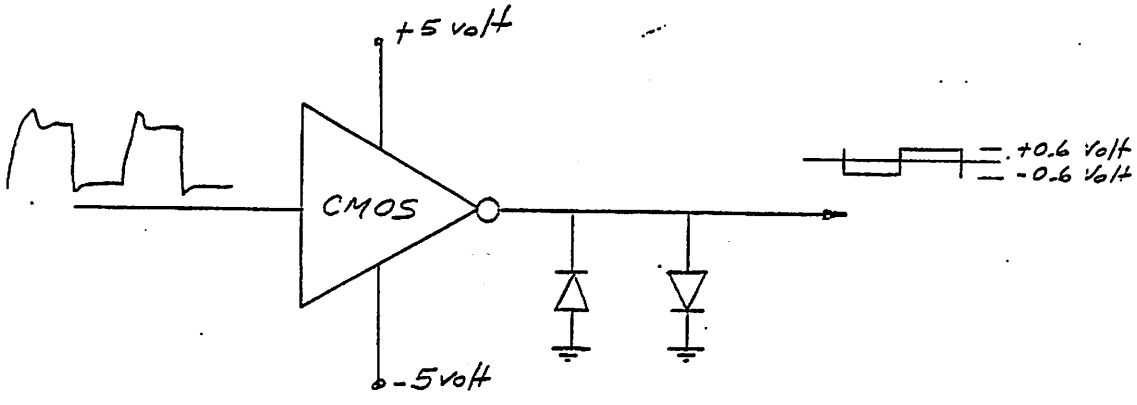


Fig. 3

Clamping a CMOS gate provides symmetric pulses for transmission.

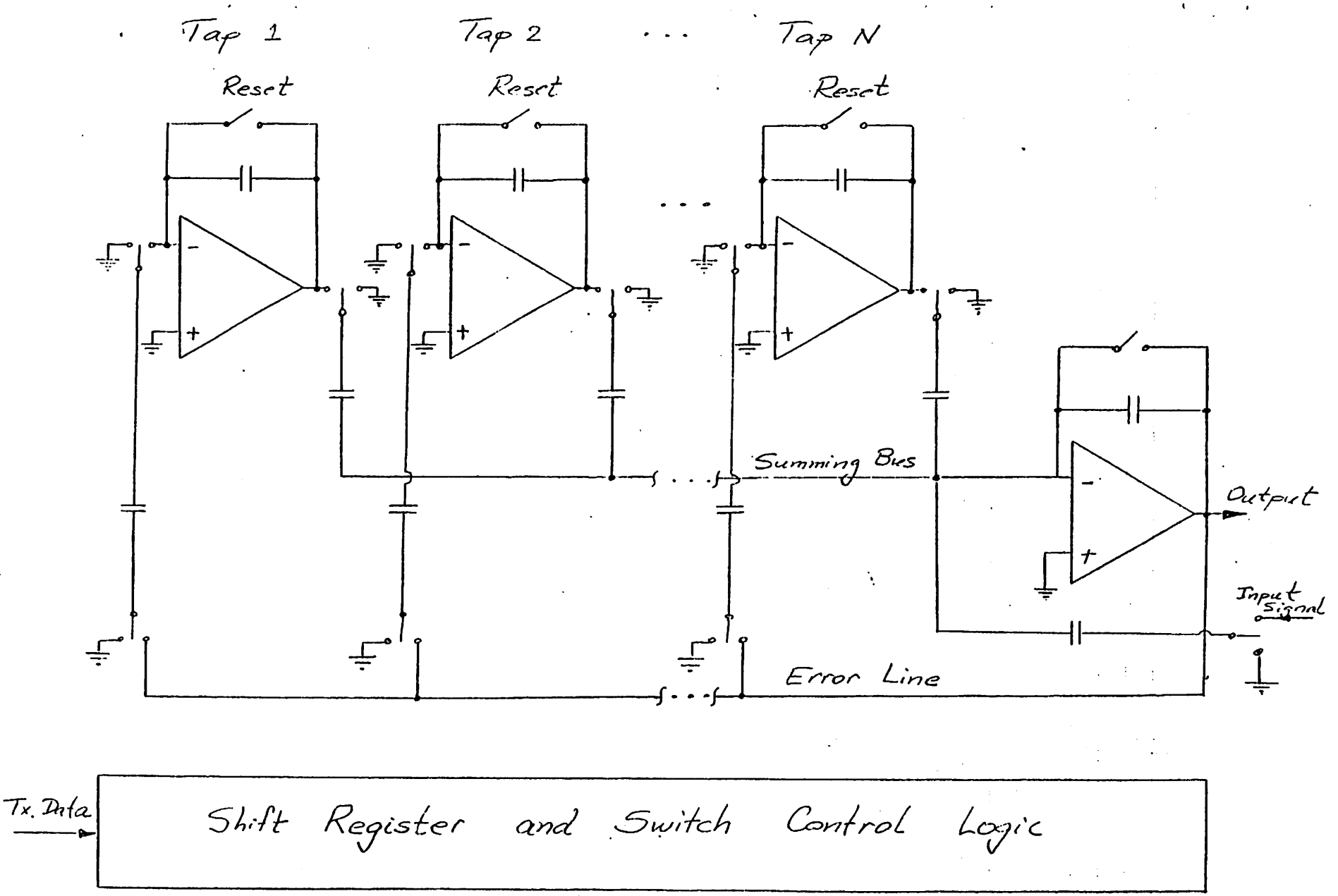


Fig. 4-a

Fully Analog Echo Canceller. Switch Control Omitted for Simplicity.

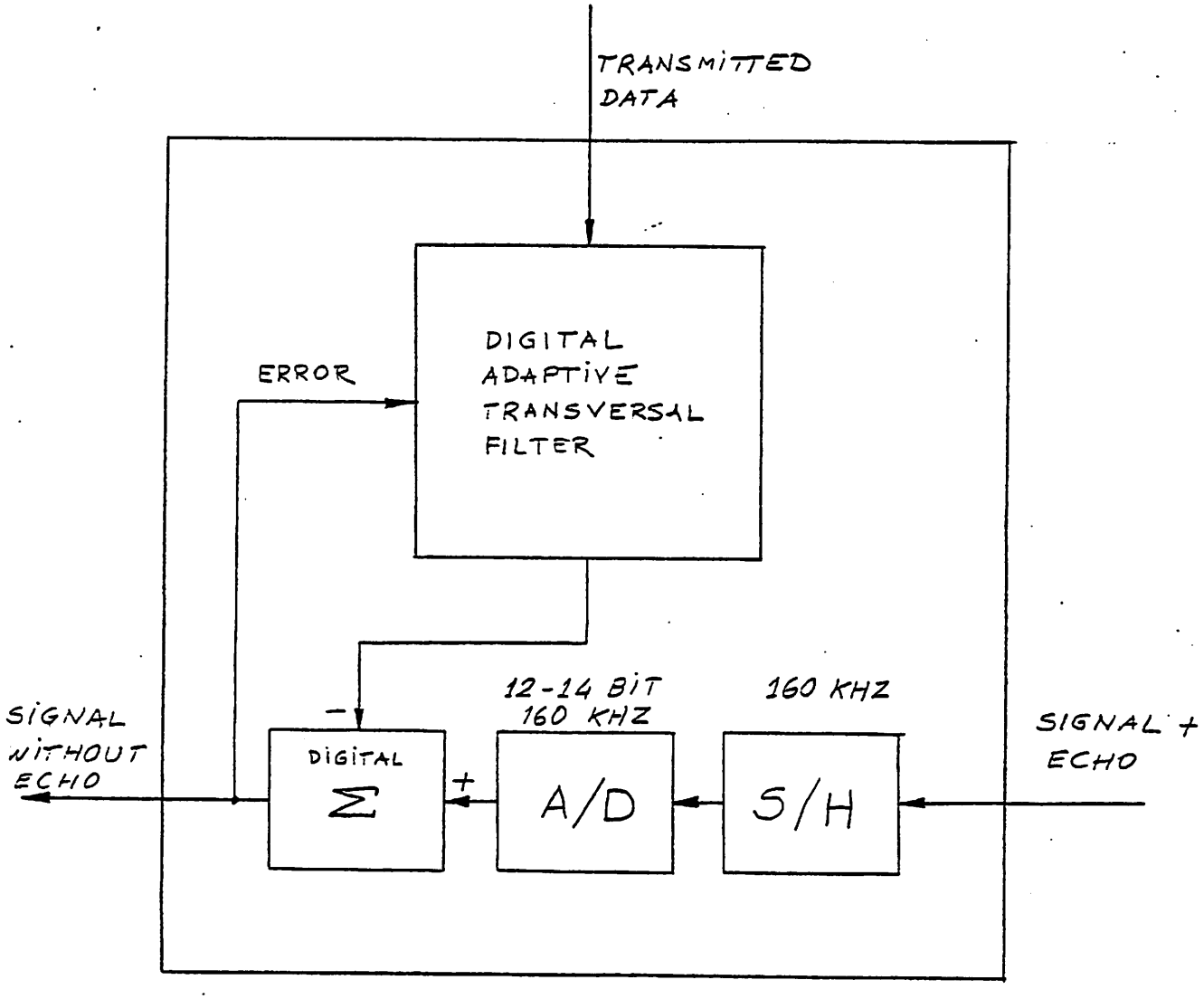


Fig 4b

Fully Digital Echo Canceller.

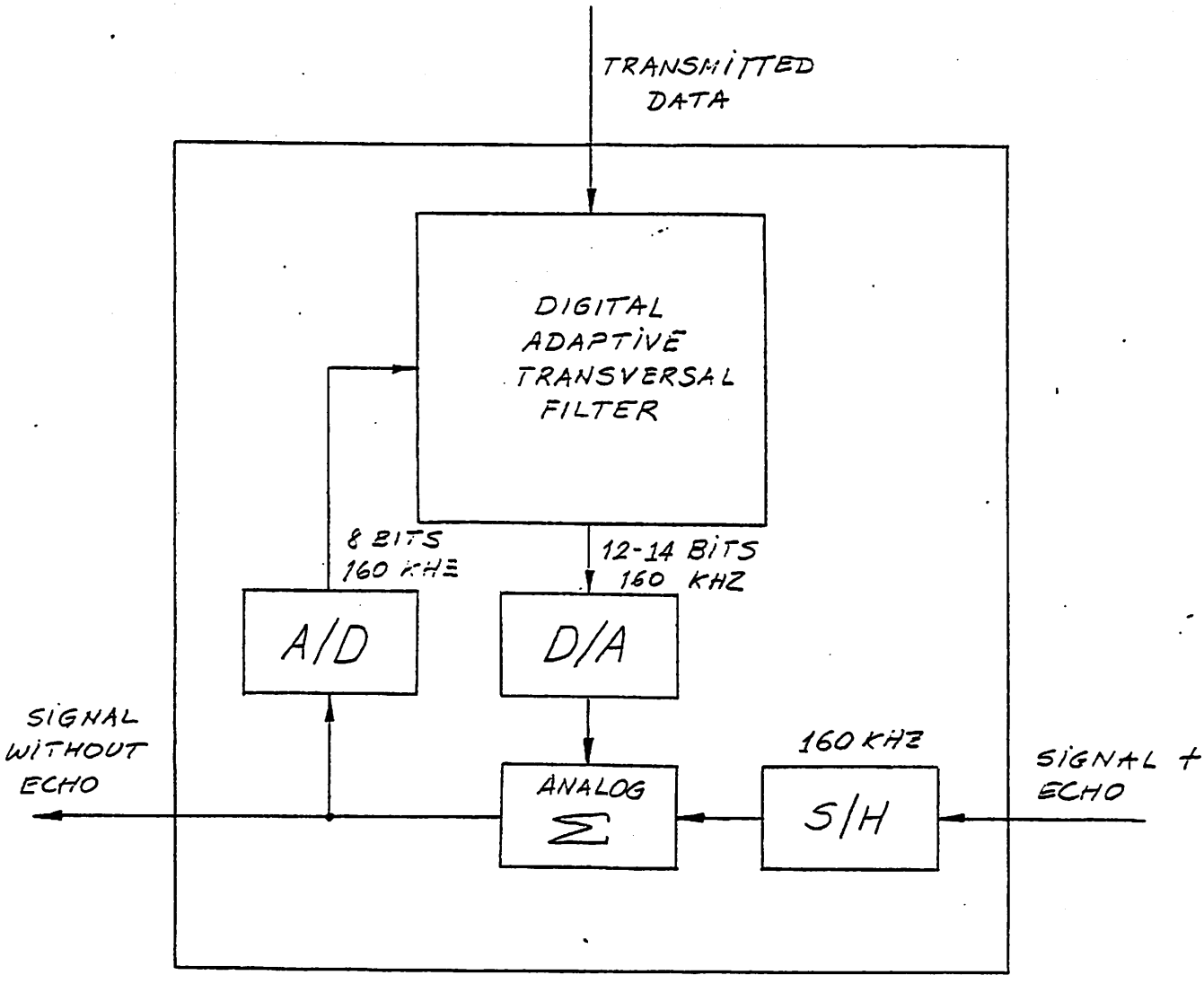


Fig. 4-C

Digital Echo Canceller with Analog Cancellation.

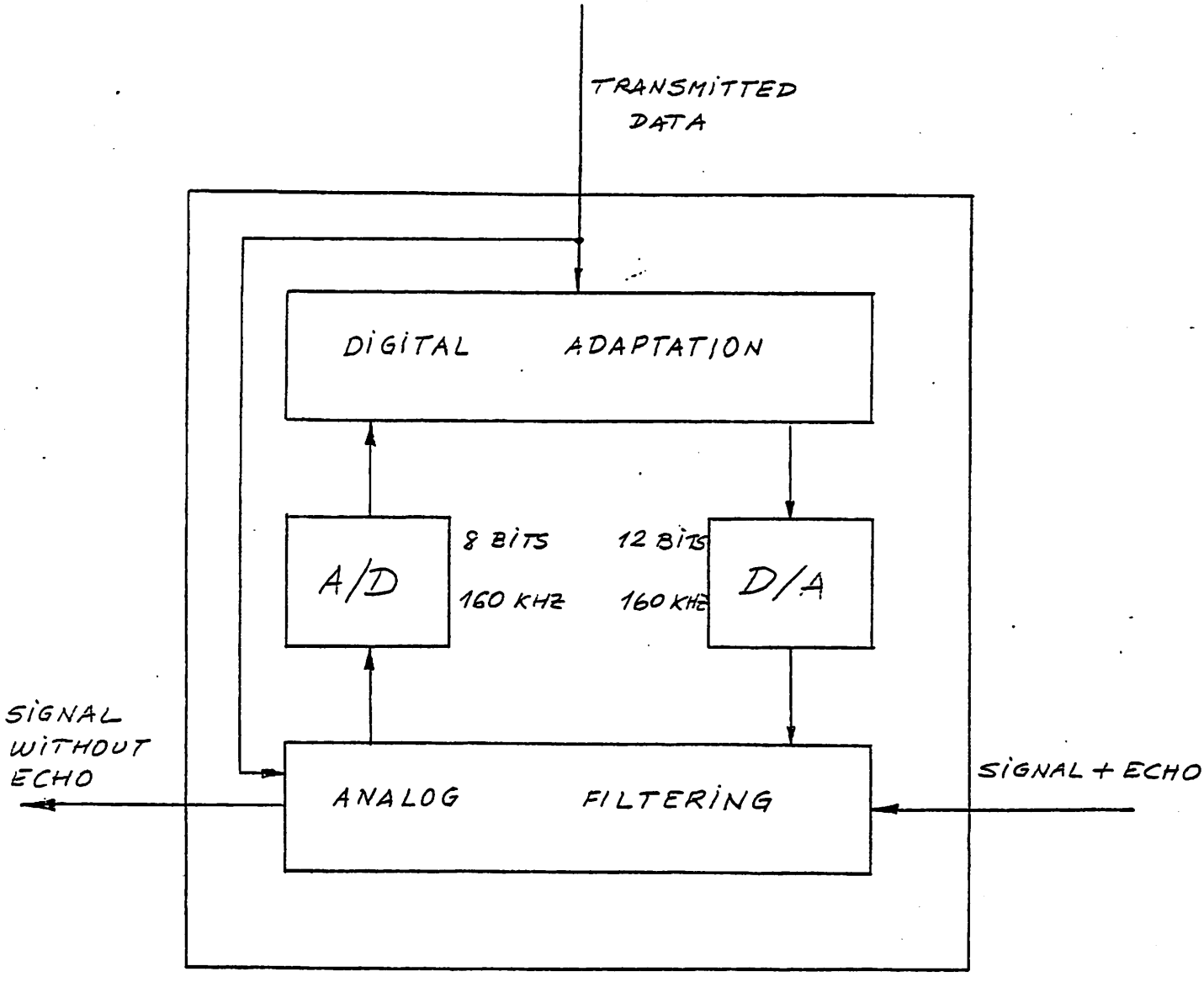


Fig. 4-d

Analog /Digital Echo Canceller

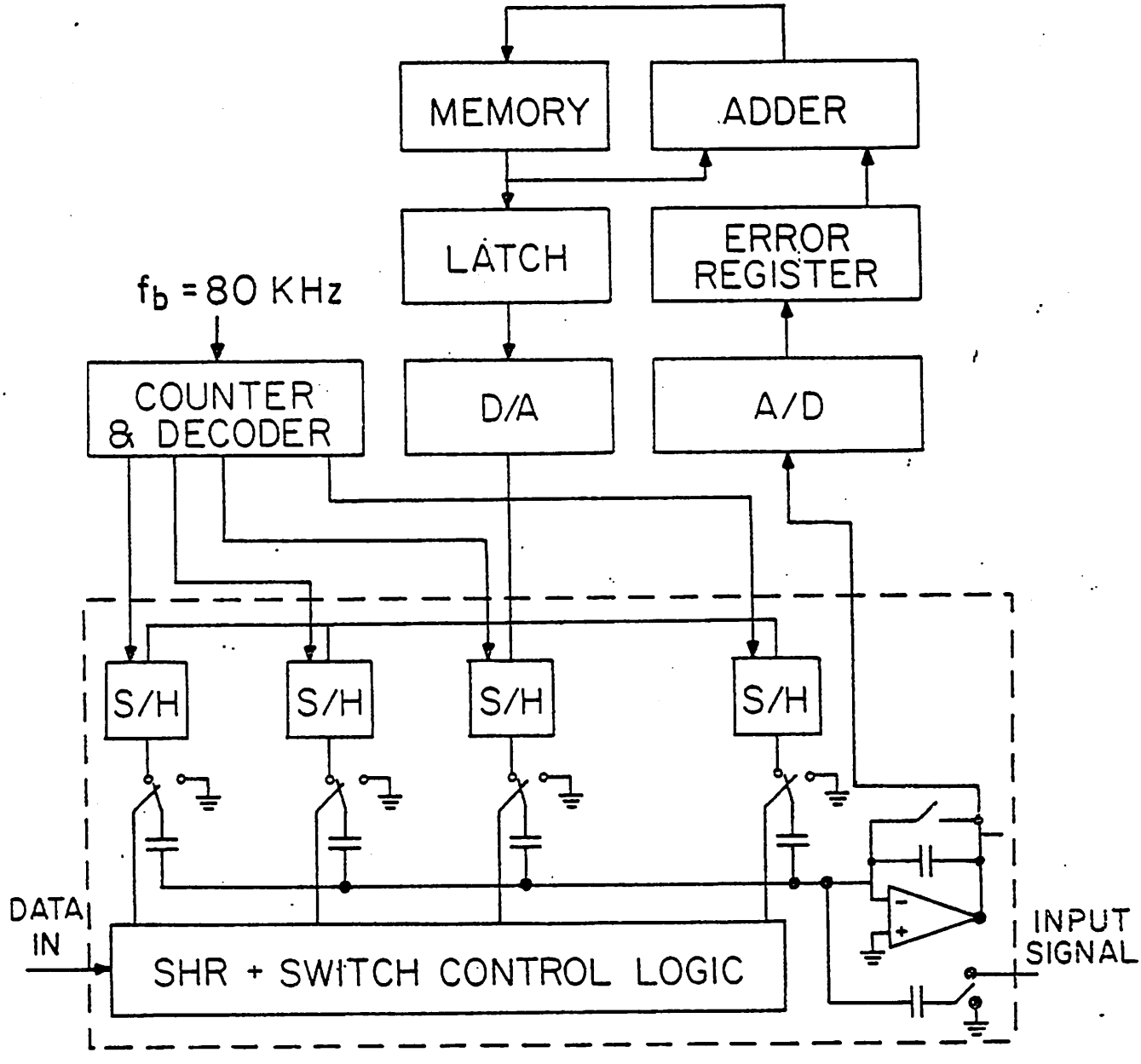

MEMORY
ADDER
LATCH
ERROR REGISTER
f_b = 80 KHz
COUNTER & DECODER
D/A
A/D
S/H
S/H
S/H
S/H
DATA IN
SHR + SWITCH CONTROL LOGIC
INPUT SIGNAL

Fig. 5

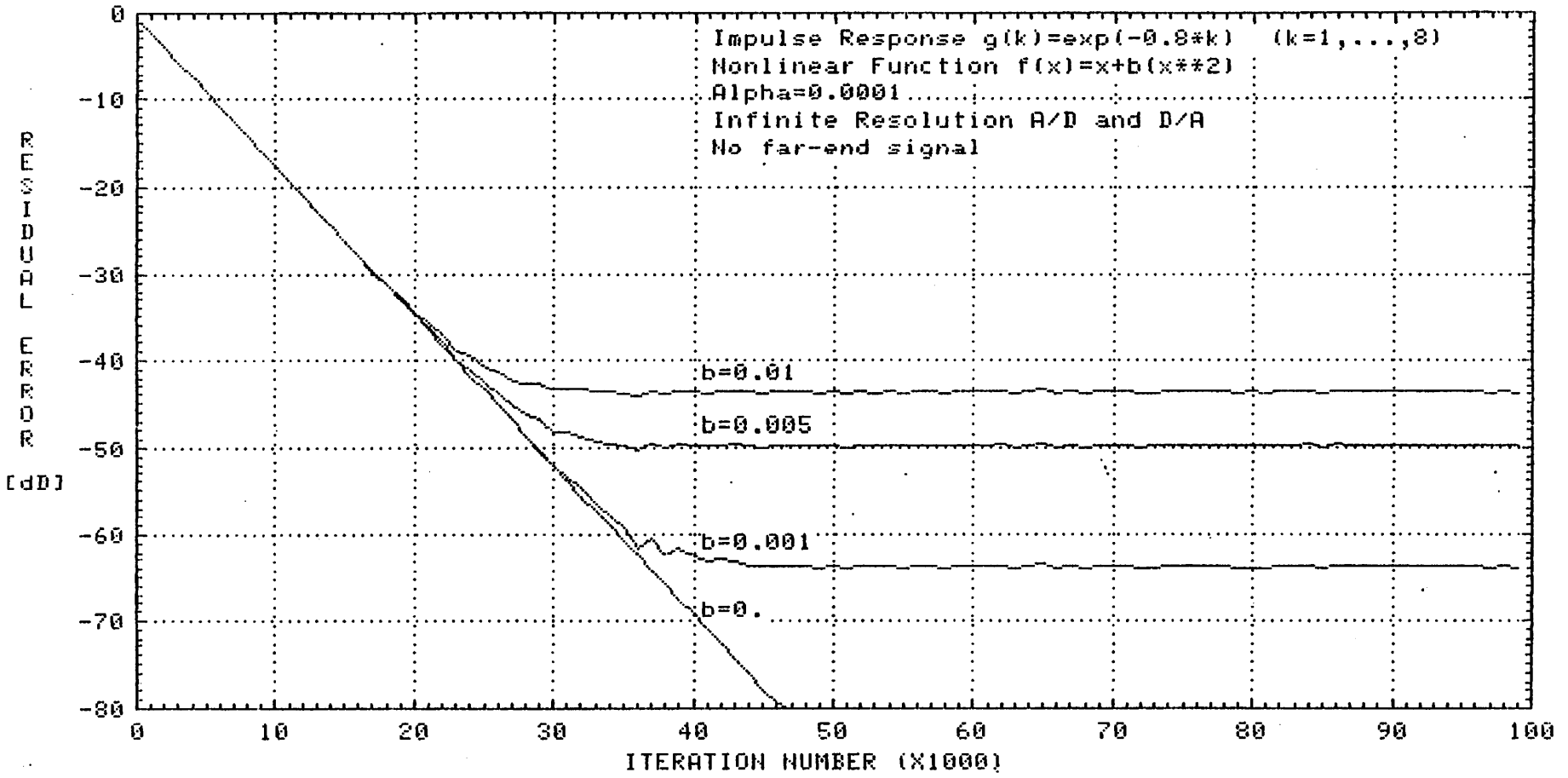

Impulse Response g(k)=exp(-0.8*k) (k=1,...,8)
Nonlinear Function f(x)=x+b(x**2)
Alpha=0.0001
Infinite Resolution A/D and D/A
No far-end signal
b=0.01
b=0.005
b=0.001
b=0.
RESIDUAL ERROR [dB]
0
-10
-20
-30
-40
-50
-60
-70
-80
0
10
20
30
40
50
60
70
80
90
100
ITERATION NUMBER (X1000)

Fig. 6

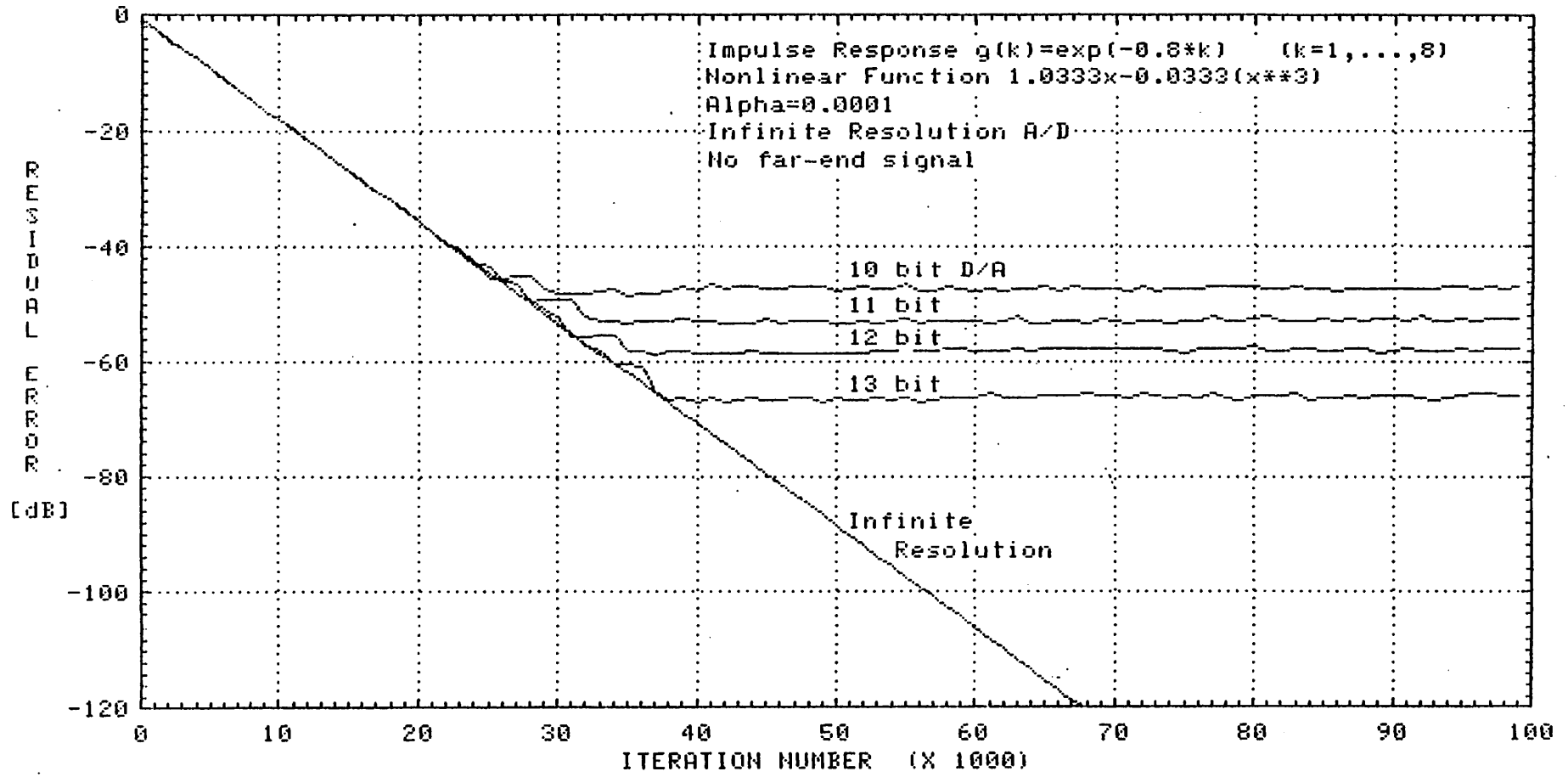

Impulse Response g(k)=exp(-0.8*k) (k=1,...,8)
Nonlinear Function 1.0333x-0.0333(x**3)
Alpha=0.0001
Infinite Resolution A/D
No far-end signal
10 bit D/A
11 bit
12 bit
13 bit
Infinite
Resolution
RESIDUAL ERROR
[dB]
0
-20
-40
-60
-80
-100
-120
0
10
20
30
40
50
60
70
80
90
100
ITERATION NUMBER (X 1000)

Fig. 7

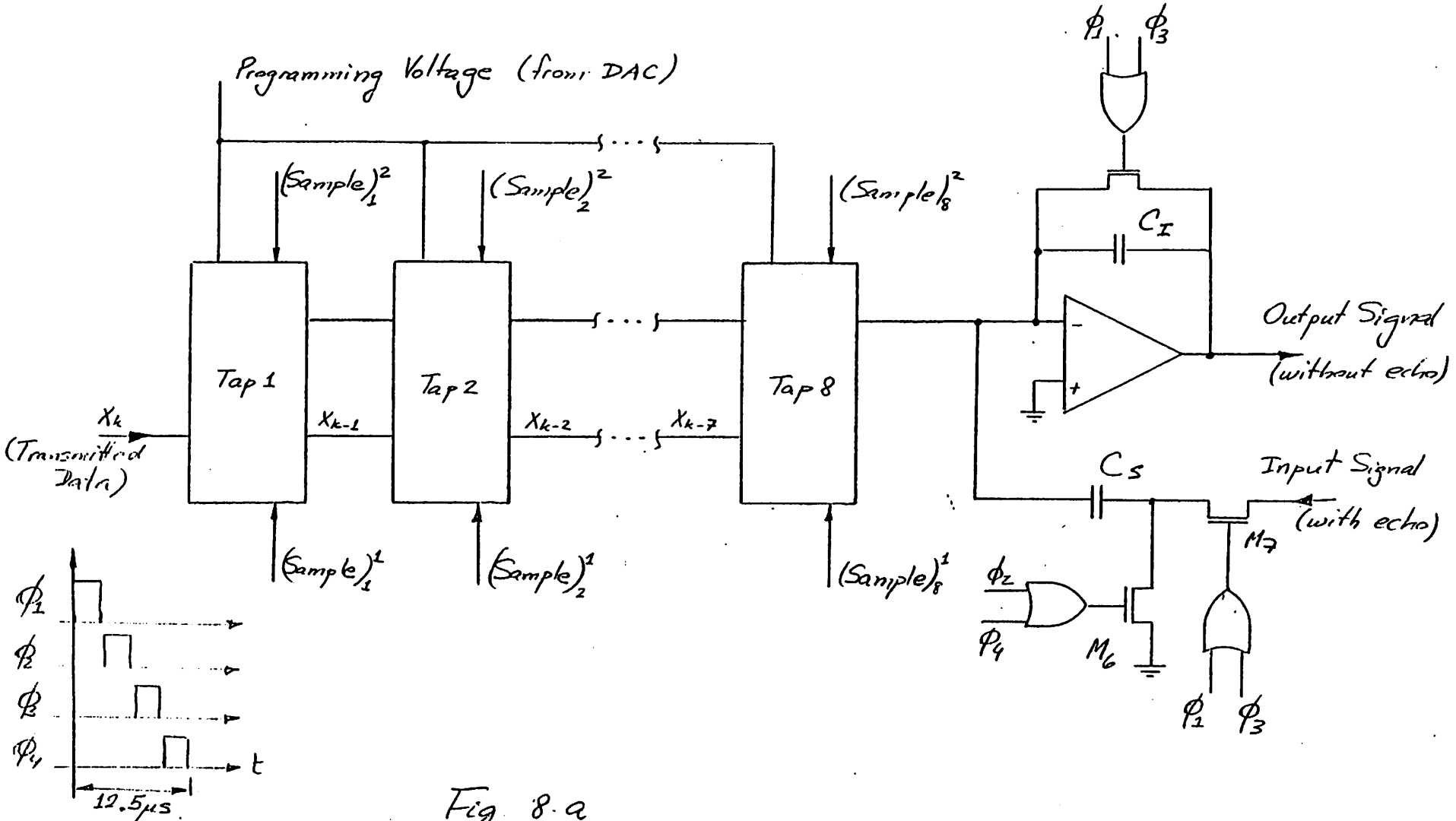


Fig 8.a

Circuit schematic of transversal filter. Circuitry inside each box "Tap n" is shown in Fig 8b. $(\text{Sample})_n^i$ represents the sampling signal for the S/H of tap n of the i^{th} of the 2 interleaved sections of the filter ($i=1,2$).

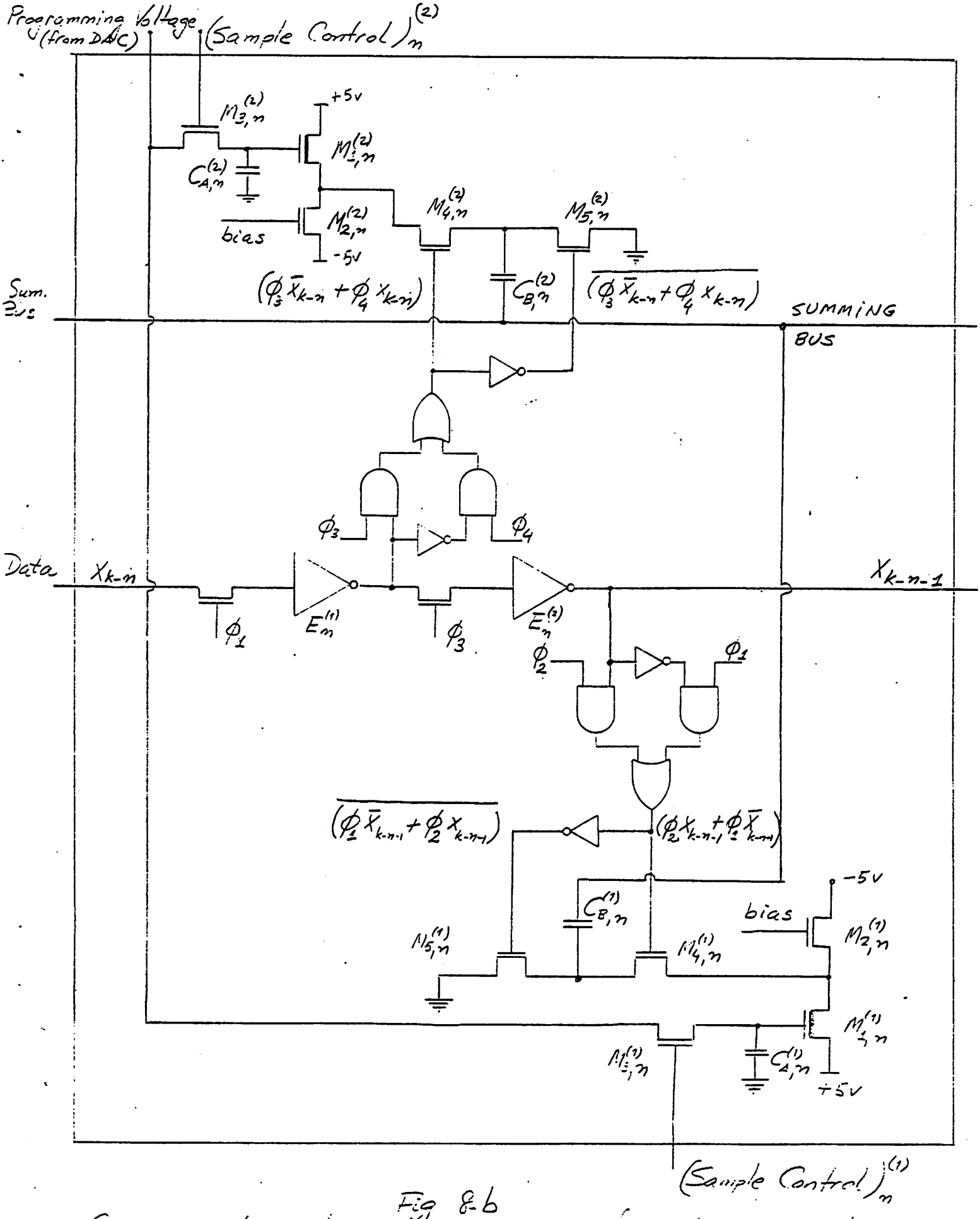


Fig 8-6

Circuit schematic of tap n of echo canceller

Superscript (i) identifies each one of the 2 interleaved sections of the transversal filter

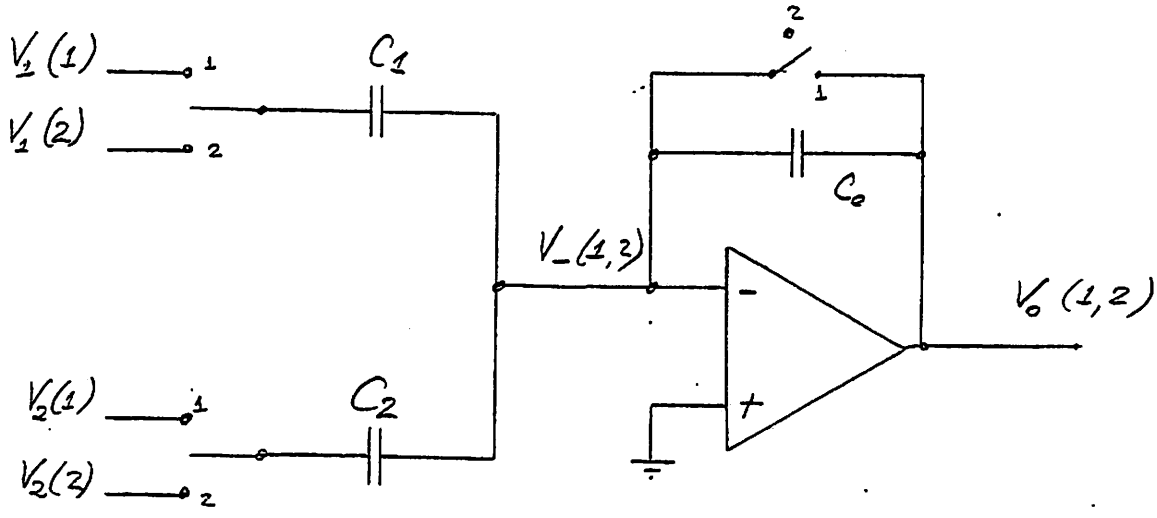


Fig. 9

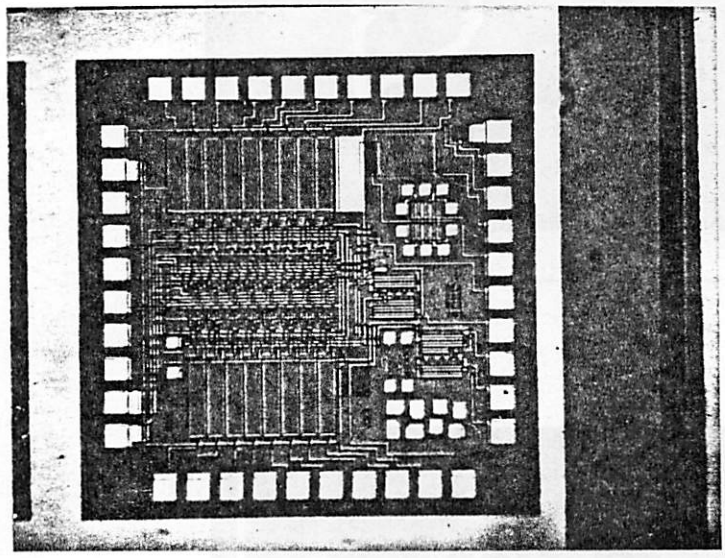
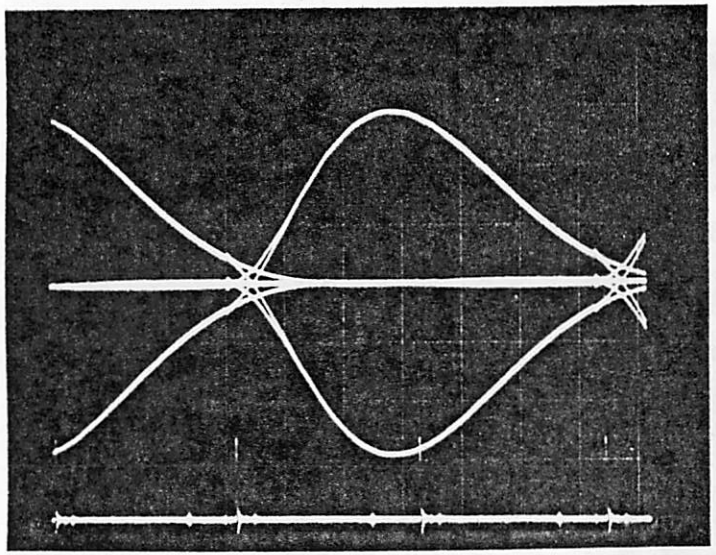
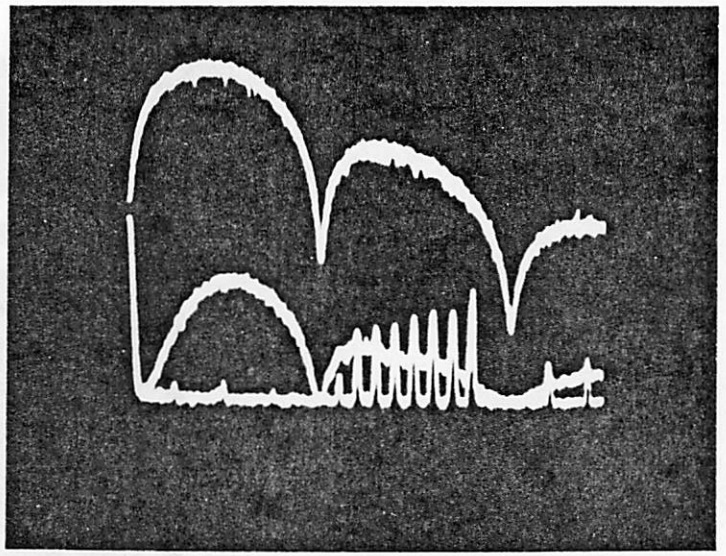


Fig. 10
Chip Photo



(a)

Transmitted pulse shape
200 mV/cm
2 μs/cm

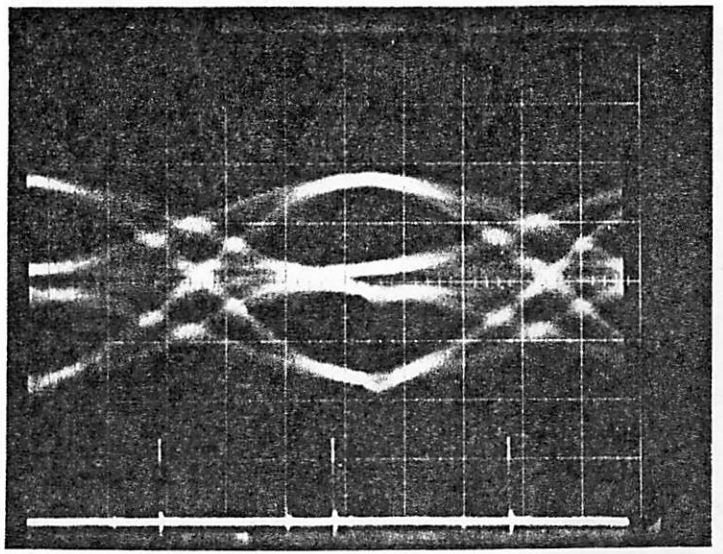


(b)

Transmitter spectrum
and crosstalk spectrum
20 dB/cm
20 kHz/cm
70 dB between spectra

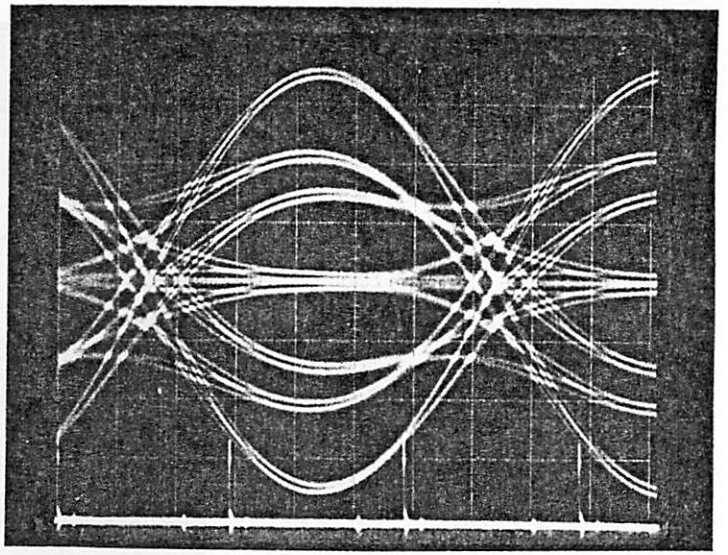
Fig. 11

EYE DIAGRAMS AT INPUT OF ECHO CANCELLER



(a)

Local transmitter off
20 mV/cm
2 μs/cm



(b)

Local transmitter on
1 V/cm
2μs/cm

Fig. 12

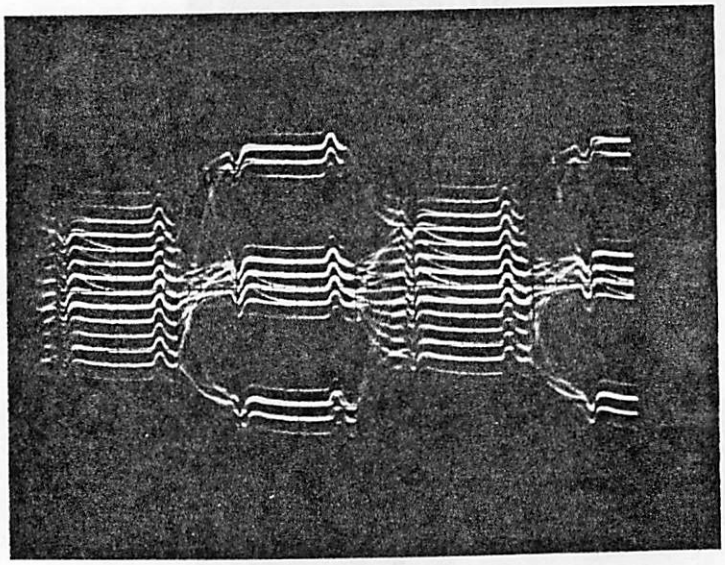
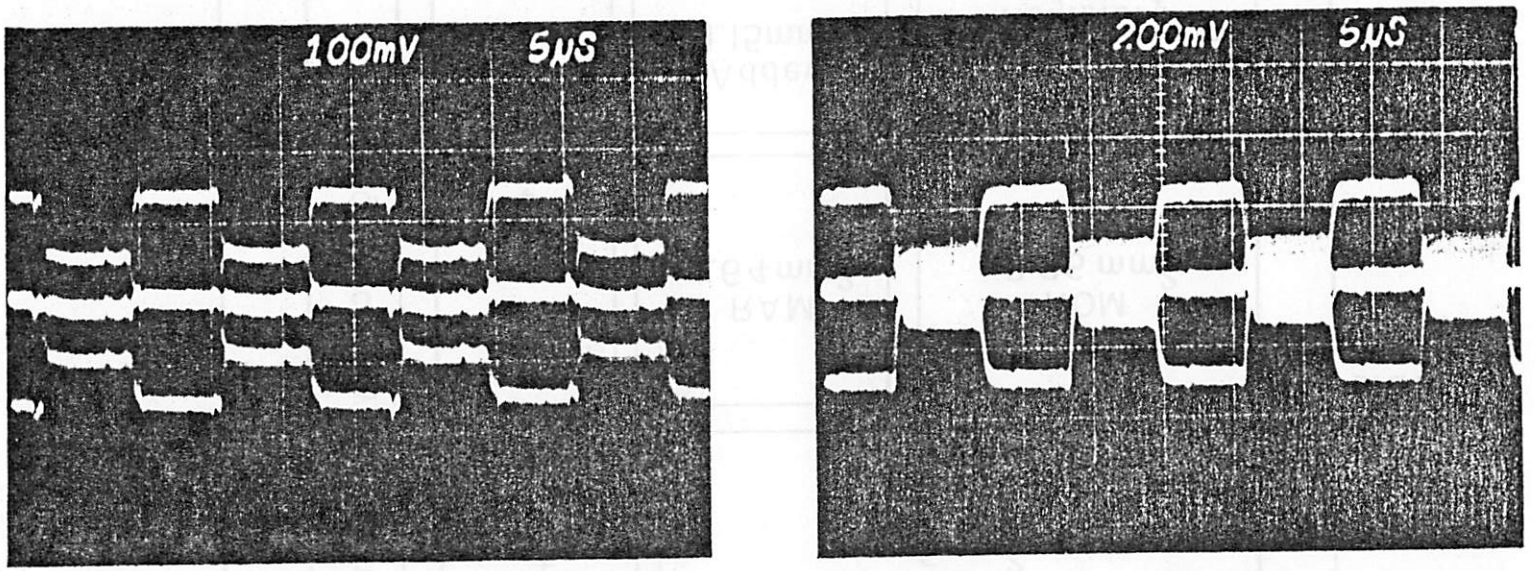


Fig. 13

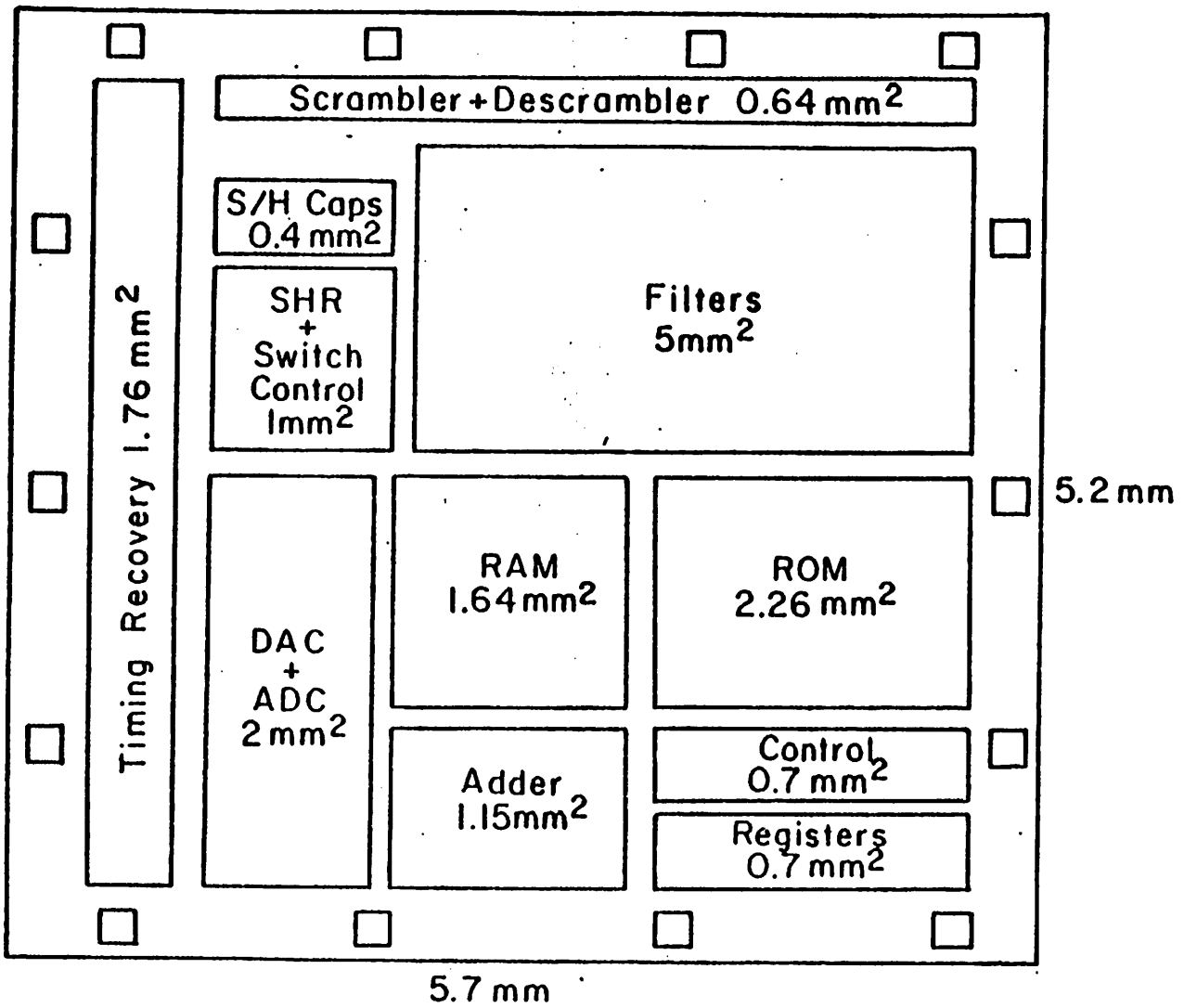
Eye diagram at output of Echo Canceller

2μs/cm 100 mV/cm.



(a) (b)

Fig. 14



Power Dissipation ≤ 300mW

Area ~30mm² in 5μ Si-Gate NMOS

Fig. 15