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TOPOLOGICAL CRITERIA FOR NONLINEAR RESISTIVE CIRCUITS CONTAINING CONTROLLED SOURCES TO HAVE A UNIQUE SOLUTION

by

T. Nishi and L.O. Chua

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Topological Criteria for Nonlinear Resistive Circuits Containing Controlled Sources to Have a Unique Solution†

Tetsuo Nishi, Senior Member, IEEE and Leon O. Chua, Fellow, IEEE††

ABSTRACT

This paper gives a definitive solution to the following fundamental problem: When does a network containing nonlinear monotone resistors (characterized by strictly-increasing onto function), dc sources (voltage and current sources), and linear controlled sources (all 4 types) possess a unique solution?

Our uniqueness criteria is couched in strictly topological terms. In particular, the uniqueness of a large class of practical nonlinear circuits can be determined, often by inspection, by checking for the presence of a new and fundamental topological structure called a cactus graph.

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††T. Nishi is with the Department of Computer Science and Communication Engineering, Kyushu University. Presently on leave at the University of California, Berkeley. L. O. Chua is with the Department of Electrical Engineering and Computer Sciences, and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

1. Introduction

In a remarkable theorem [1], Nielsen and Wilson demonstrated that a certain class C of nonlinear resistive circuits has a unique solution for all values of circuit parameters belonging to some parameter set P if and only if the circuit does not possess a certain topological structure S. In the case of the Nielsen-Willson theorem, C consists of circuits containing only transistors, linear passive resistors, and independent sources; P consists of all positive resistance values, all positive and negative values of dc sources, and all coefficients $0 < \alpha_f < 1$, $0 < \alpha_R < 1$ for the transistors; S consists of a 2-transistor feedback structure. Such graph-theoretic results are extremely useful because it allows the difficult "existence and uniqueness" question to be answered by a strictly topological analysis. For simple circuits, this analysis can often be done by inspection.

Our objective in this paper is to derive a similar type of topological result for a much more general class of nonlinear circuits; namely, circuits allowing all 4 types of linear controlled sources. They are current-controlled current sources (CCCS), voltage-controlled voltage sources (VCVS), current-controlled voltage sources (CCVS), and voltage-controlled current sources (VCCS). Without loss of generality, we assume all controlled source coefficients to be positive real numbers.[1]

Since resistors having a non-monotonic v-i characteristic will in general result in multiple solutions for certain values of biasing resistors and dc sources, we assume all nonlinear resistors to be 2-terminal resistors characterized by strictly-monotone increasing v-i curves. Moreover, to guarantee that the circuit has at least one solution, we assume the v-i characteristics to be onto functions, i.e., $v \to \infty$ as $i \to \infty$ and $v \to -\infty$ as $i \to -\infty$.

One is tempted to dismiss the above class of circuits as "too general" because it is well known that nonlinear circuits containing controlled sources usually exhibit multiple solutions. For example, all 4 circuits shown in Fig. 1 exhibit multiple solutions for some $R > 0$, and for the rather liberal choices of controlling coefficient α indicated. To see this, note first that the linear one-port to the right of the nonlinear resistor R_1 is equivalent to a linear negative resistor. Indeed, in Figs. 1(a) and 1(b), we have

$$v = -kRi = R_{eq} i \quad \text{where } R_{eq} \triangleq -kR < 0 \tag{1}$$

where k is a positive number depending on α. Similarly, $R_{eq} = -\alpha < 0$ in Fig. 1(c)

[1] If a controlled source coefficient is negative, simply transpose the 2 terminals to obtain a positive coefficient.

and $R_{eq} = -1/\alpha$ in Fig. 1(d). The resulting equivalent circuit in Fig. 2(a) can be solved graphically by the standard load-line method [2]. Note that so long as R_1 is nonlinear, a load line of appropriate slope (or equivalently, an appropriate value of $R_{eq} < 0$ in Fig. 2) can always be chosen to intersect the v_R-i_R curve in at least 2 points.

The above examples seem to support the belief that no general existence and uniqueness theorem could be derived, let alone the topological condition, for nonlinear circuits containing controlled sources.

To show that the task is far from hopeless, note that if we only transpose the 2 terminals of each controlled source in Fig. 1, then R_{eq} would become positive and all 4 "transposed" circuits would have only one solution for all $\alpha > 0$ (because the slope of the load line in Fig. 2(b) would become negative, resulting in only one intersection with any strictly monotone-increasing curve). This observation suggests the possibility that indeed it may be possible to derive some "topological structure" which guarantees uniqueness of solution.

Our main contribution in this paper is to derive several topological criteria for testing various classes of nonlinear circuits for unique solution.

Section 3 presents 6 topological criteria for testing the following 4 special classes of circuits by inspection:

1. Circuits containing one controlled source of any type.
2. Circuits containing two controlled sources of the same type.
3. Circuits containing two controlled sources of any type.
4. Circuits containing any number of controlled sources of the same type.

Section 4 presents the main theorems (Theorems 7 and 8) of this paper. Theorem 7 presents the topological criteria for testing circuits containing all 4 types of controlled sources subject only to an interconnection assumption which is satisfied in most practical circuits.

Theorem 8 presents the general topological criteria from which the criteria in Sections 3 and 4 are derived. This general result is applicable to any nonlinear resistive circuits containing all 4 types of controlled sources. The proof of the main topological criteria is extremely involved. Consequently, in Section 5 we have broken up the proof into several lemmas so that the trees can be separated from the forest. Because the proofs of the lemmas are rather technical, they are collected in the Appendix. Readers interested only in the applications may skip this section without loss of continuity.

2. Notations, Symbols, Graph Operations, and Assumption

In order to state the various topological criteria in this paper simply, and without ambiguity, it is essential that all notations, symbols, and graph operations be defined precisely. We will collect all of them here so that readers who have forgotten them can turn quickly to this short section for reference. To help the reader in remembering some of the more commonly used notations and terminologies, we have carefully chosen mnémonics for deciphering them.

A. Graph Notation

1. Each independent voltage source, independent current source, or 2-terminal resistor (linear or nonlinear) is represented by a directed edge whose direction can be arbitrarily assumed.
2. Each of the 4 types of controlled sources is represented by a pair of directed edges whose directions are specified in Table 1. Here, the directions are uniquely determined by the type of controlled source and must be adhered to religiously.

To help remembering the notation, note that

1) the edge associated with a + and - sign is directed from + to -. This applies to both the input edge (controlling voltage) of a VCCS or VCVS, and to the output edge (controlled voltage) of a CCVS and VCVS.
2) the input edge associated with the short-circuit (controlling current) of a CCVS or CCCS is directed in the same direction as the controlling current i.
3) the output edge associated with the controlled current source of a VCCS or CCCS is directed opposite to the arrow head inside the diamond-shaped symbol.[2]

B. Symbol

Node numbers are always enclosed by a circle. The 2 nodes associated with the input (resp., output) port of each controlled source are labelled by the same number with a prime to distinguish them; e.g., ⓐ and ⓐ' .

The 2 edges associated with each controlled source are labelled by the same number with a hat "^" added to that of the output edge. For example, edges 5 and $\hat{5}$ denote the input and output edge of controlled source 5, respectively.

C. Graph Operations

The topological criteria in the following sections require the given graph G to be reduced into various simpler graphs via a combination of the following graph operations:

[2]Unlike 1) and 2), this notation is somewaht unconventional if not occasionally confusing. However, much more is gained in the resulting simplicity of the topological criteria.

1. Open-circuit Operation $O(\cdot)$

Given an edge k, the operation $O(k)$ deletes the connecting line but leaves the nodes intact as shown in Fig. 3(a).

2. Short-circuit Operation $S(\cdot)$

Given an edge k, the operation $S(k)$ coalesces the 2 nodes into one node as shown in Fig. 3(b).

3. Open/Short Operation $O/S(\cdot)$

(a) Given a resistor edge R, the operation $O/S(R) \triangleq O(R)$ or $S(R)$, i.e., replace R by either Fig. 3(a) or Fig. 3(b).

(b) Given a pair of edges associated with a controlled sources CS of any type, the operation $O/S(CS)$ consists of open-circuiting one edge (either the input or output edge) and short-circuiting the second edge, as shown in Fig. 4.

4. Zero Operation $Z(\cdot)$

This operation sets an independent source, or a controlled source to zero in the usual way:

(a) Given an edge E_s corresponding to an independent voltage source, the operation $Z(E_s) \triangleq S(E_s)$; i.e., short-circuit E_s.

(b) Given an edge I_s corresponding to an independent current source, the operation $Z(I_s) \triangleq O(I_s)$; i.e., open-circuit I_s.

(c) Given a pair of edges associated with a controlled source of any type, the operation $Z(CS)$ transforms the 2 edges $(k,\hat{k})$ in accordance with that shown in Fig. 5 for each of the 4 types of controlled source.

D. Assumption

Throughout Sections 3 and 4, we make the following interconnection assumption (this assumption is extremely weak and is satisfied by most circuits of practical interest):

INTERCONNECTION ASSUMPTION

1. There is no loop made up exclusively of the following type of edges:
   1) DC voltage source
   2) Output (controlled) edge of CCVS or VCVS
   3) Input (controlling) edge of CCVS or CCCS
2. There is no cutset made up exclusively of the following type of edges:
   1) DC current source
   2) Output (controlled) edge of CCCS or VCCS
   3) Input (controlling) edge of VCVS or VCCS

Figures 6(a) and (c) (resp. 6(b) and (d)) give 2 examples of circuits which violate the condition 1 (resp. 2) of the Interconnection Assumption.

3. Topological Criteria by Inspection

In this section, as well as the following section, it is of fundamental importance to consider a particular graph having a special topological structure. Since this graph pertains only to a reduced network containing exclusively of controlled sources, the "input" edges will be labelled $1,2,\ldots,n$ and the "output" edges will be labelled $\hat{1},\hat{2},\ldots,\hat{n}$, as shown in Table 1. To help visualize this structure consider a typical cactus plant shown in Fig. 7(a), consisting of leaves (shaded area) "hinged" between the top and the bottom only. The graph made up of the boundaries of the leaves, as shown in Fig. 7(b), is called a cactus graph iff it satisfies the following properties: it is made of 2n edges $1,2,\ldots,n$, $\hat{1},\hat{2},\ldots,\hat{n}$ and:

1) it is connected
2) every loop is made of exactly 2 edges, k and $\widehat{k+1}$ ($k = 1,2,\ldots,n$; $\widehat{n+1} = \hat{1}$)
3) every cutset is made of exactly 2 edges

Formally, a cactus graph is defined by a fundamental loop matrix having the following structure

$$B = \begin{array}{c} \\ \hat{1} \\ \hat{2} \\ \hat{3} \\ \vdots \\ \hat{n} \end{array} \begin{array}{c} \begin{array}{cccccc|ccccc} 1 & 2 & 3 & \cdots & n & & \hat{1} & \hat{2} & \hat{3} & \cdots & \hat{n} \end{array} \\ \left[\begin{array}{ccccc|ccccc} 0 & & & & \varepsilon_n & 1 & & & & \\ \varepsilon_1 & 0 & & \bigcirc & & & 1 & & \bigcirc & \\ & \varepsilon_2 & 0 & & & & & 1 & & \\ & \bigcirc & \ddots & \ddots & & & & \bigcirc & & \\ & & \varepsilon_{n-1} & & 0 & & & & & 1 \end{array}\right] \end{array} \qquad (2)$$

where $\varepsilon_i = \pm 1$. In Figs. 7(c)-(e) are shown several cactus graphs.

Note that each leaf of a cactus graph consists of 2 edges labelled consecutively (except the last number or when the graph has only 2 edges), one pertaining to an input edge of one controlled source, the other to the output edge of another controlled source. These 2 edges form a loop. In the following topological criteria, each loop associated with a leaf of a cactus graph is said to be similarly directed iff the 2 edges are directed in the same direction (clockwise or counterclockwise).

In this section, we present 6 topological criteria for determining, by inspection, whether a given circuit belonging to the 4 special classes considered below has a unique solution. For each case, the criteria is applied to one or more simplified graphs obtained from the graph G by various graph operations described in Section 2. Here G denotes a connected graph associated with a resistive nonlinear

circuit N containing 2-terminal linear positive resistors, 2-terminal nonlinear resistors characterized by a continuous strictly-increasing onto function, independent sources, and linear controlled sources with positive controlling coefficients. Proofs will be given in Section 5 after the proofs of Theorems 7 and 8.

A. Circuits Containing One Controlled Source of Any Type

Theorem 1 (One Controlled Source)

Let N contain at most one controlled source. Then N has a unique solution for all circuit parameters[3] if and only if the associated graph G can not be reduced to the connected 2-edge graph[4] shown in Fig. 8, which is a one-leaf cactus graph with no similarly-directed loop, using only the following graph operations:

(a) Apply $Z(E_s)$ to each voltage source and $Z(I_s)$ to each current source.

(b) Apply $O/S(R)$ to each resistor.

Example 1 Applying Theorem 1 to the circuits shown in Fig. 9, we find only the graphs associated with Figs. 9(a), (c), (e) and (g) can not be reduced to the graph in Fig. 8 (recall from Table 1 that the output edge associated with the controlled current source should be directed opposite to that of the arrow head). Hence, only these 4 circuits have a unique solution. The other circuits on the right (obtained by transposing the controlled source terminals on the left) have multiple solutions for some circuit parameters.

Remark: After a little practice, Theorem 1 can be applied directly to the circuit without even drawing a graph.

B. Circuits Containing 2 Controlled Sources of the Same Type

Theorem 2 (Two Controlled Sources)

Let N contain 2 controlled sources of the same type. Then N has a unique solution for all circuit parameters if and only if the associated graph G can not be reduced to any one of the 2-leaves cactus graph in Fig. 10 with 0 or 2 similarly directed loops by using only operations (a)-(b) (from Theorem 1), or to the one-leaf cactus graph shown in Fig. 8 using only operations (a)-(b) and either operation (c) or (d) below:

(c) Apply Z(CS) (defined in Fig. 5) to one of the 2 controlled sources.

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[3]Throughout this paper, the phrase "for all circuit parameters" means for any choice of positive resistances for the linear resistors, any value of dc voltage and current sources, and any positive controlling coefficient α for the controlled sources.

[4]Note the edges labelled 1 and $\hat{1}$ are associated with the controlled source.

After operations (a) and (b), the resulting graph G_{CS} contains only 4 edges (associated with the 2 controlled sources). Relabel these edges as $\{1, \hat{1}\}$ for controlled source 1 and $\{2, \hat{2}\}$ for controlled source 2. The reduced graph G_{CS} is said to have a complementary tree structure if both input edges $\{1, 2\}$ and output edges $\{\hat{1}, \hat{2}\}$ form a tree of G_{CS}. Since operation (b) allows each resistor to be either open or short circuited, 2^m graphs G_{CS} may be generated for an m-resistor circuit, though not all of them will have a complementary tree structure.

(d) Applying O/S(CS) (defined in Fig. 4) to each reduced graph G_{CS} which possesses a complementary tree structure.

All the disallowed two-leaves cactus graphs are shown in Fig. A.1.

Example 2 Consider the circuit shown in Fig. 11(a). Applying operations (a) and (b), the only 4-edge subgraph of the form in Fig. 10 is shown in Fig. 11(b). However, this graph is allowed because the number of similarly directed loops is one.

So we proceed and apply operation (a) $O(I_s)$, (b) $S(R_1)$, $S(R_2)$, $S(R_3)$, $O(R_4)$ and (c) Z(CS) (to controlled source #1) and obtain the 2-edge graph shown in Fig. 11(c). But this too is allowed because the disallowed graph in Fig. 8 has an oppositely directed loop.

So we proceed further, this time we apply operation (a) $O(I_s)$, (b) $S(R_1)$, $S(R_2)$, $S(R_3)$, $O(R_4)$ and (c) Z(CS) (to controlled source #2) and obtain the 2-edge graph shown in Fig. 11(d). Since this graph is disallowed in Fig. 8, it follows from Theorem 2 that this circuit does not have a unique solution.

The reader should verify that if we reverse the reference direction of i_1 and/or i_2 in Fig. 11(a), the resulting circuit also does not have a unique solution.

Example 3 Consider the circuit shown in Fig. 12(a). Applying only operations (a) and (b), no disallowed 2-leaves cactus graph is found. We proceed further applying operations (a), (b), (c) and (a), (b), (d). In each case, we obtain either the one-leaf cactus graph shown in Fig. 12(b) or 12(c) respectively. Since neither is disallowed by Fig. 8, and since we have exhausted all combinations, we conclude that this circuit has a unique solution.

On the other hand, if we reverse the reference direction of i_1, the circuit does not have a unique solution.

Example 4 Consider the circuit shown in Fig. 13(a). It is easily seen that operations (a) and (b) can not give rise to any of the disallowed 2-leaves cactus graph. For example, applying $S(E_s)$, $O(I_s)$, $O(R_1)$, $S(R_2)$ and $S(R_3)$, we obtain the 4-edge graph shown in Fig. 13(b).

Applying operations (a), (b) and (c), or (a), (b) and (d), we find it is impossible to reduce the graph to a 2-edge graph in Fig. 8. For example, applying

operation Z(CS) to the controlled source edge $\{1, \hat{1}\}$ in Fig. 13(b) gives us a reduced graph with 2 self-loops in Fig. 13(c), which is not in the form of Fig. 8. Note that the graph in Fig. 13(b) (obtained by operations (a) and (b)) does <u>not</u> possess a complementary tree structure. Hence we do <u>not</u> have to apply operation (d) in this case.

All told, we conclude the circuit in Fig. 13(a) has a <u>unique</u> solution for all circuit parameters, and regardless of the reference direction of i_1 and i_2.

<u>Example 5</u> Consider the circuit in Fig. 14(a). Note that the reduced graph obtained by applying operations (a) and (b) can <u>never</u> possess a <u>complementary tree structure</u> because node ③ is connected only to <u>output</u> edges of the 2 controlled sources, thereby preventing the input edges to form a tree. Hence, operation (d) need not be carried out.

Remember, however, that we must exhaust all possible operations stipulated in Theorem 2 before drawing a conclusion. Indeed, applying operations (a), (b), and (c), it is possible to obtain either the graph shown in Fig. 14(b), or 14(c). Since neither graphs are of the form in Fig. 8, we conclude this circuit has a unique solution.

<u>Remark</u>: Theorem 2 is valid only if the 2 controlled sources are of the same type. To see this, consider the network shown in Fig. 15(a) which contains a CCCS and a CCVS. Note that applying operations $S(R_1)$ and O/S(CS) (controlled source #2) we obtain the graph shown in Fig. 15(b), which was disallowed in Fig. 8. Yet, using <u>Theorem 3</u> below, we will see that this circuit has a unique solution.

C. <u>Circuits Containing 2 Controlled Sources of Any Type</u>

<u>Theorem 3</u> (Two Controlled Sources)

Let N contain two controlled sources of any type. Then N has a unique solution for all circuit parameters if and only if by applying the operations (a), (b), and (c) (in Theorems 1 and 2), the associated graph G can not be reduced to any of the graphs disallowed in Theorem 2, or to any of the graphs described by (1)-(3) below.

(1) the graphs in Figs. 16(a) and (b)

(2) the graphs obtained from those in (1) by exchanging 1 and $\hat{1}$ by 2 and $\hat{2}$, respectively

(3) the graphs obtained from those in (1) and (2) by changing the directions of two edges among the edges 1, $\hat{1}$, 2, and $\hat{2}$.

<u>Example 6</u> Consider the circuit in Fig. 15(a). By inspection, we find the associated graph G can not be reduced to a two-leaves cactus graph, or to the graphs described in (1)-(3) above by using only operations (a) and (b). Furthermore by using

operations (a), (b), and (c) we cannot get a one-leaf cactus graph.[5] Thus the network has a unique solution.

However, if the direction of i_2 is changed, then the disallowed graph in Fig. 16(b) can be obtained. Therefore in this case the solution is not unique.

Example 7 Consider the network in Fig. 17(a). In this case we cannot obtain any 4-edges disallowed graph by applying operation (a) and (b). By applying the operations (a), (b) and (c) we have only two one-leaf cactus graphs in Figs. 17(b) and (c), both of which are allowed. Therefore the circuit has a unique solution.

However, if the direction of v_1 and/or i_2 is changed, then the solution is not unique.

D. Circuits Containing Any Number of Controlled Sources of the Same Type

Before stating the result we need to define some terminology and operations which are the generalization of those mentioned previously.

Let G_0 be a graph composed of n pairs of edges $(k,\hat{k})$ $(k = 1,2,\ldots,n)$ corresponding to n controlled sources. Then G_0 is said to have a complementary tree structure if it is connected and both the input edges $\{k;\ k = 1,2,\ldots,n\}$ and the output edges $\{\hat{k};\ k = 1,2,\ldots,n\}$ form a tree of G_0.

As the generalization of operations (c) and (d) the operations (c') and (d') are defined as

(c') Apply Z(CS) to some (possibly none) controlled sources.

(d') Apply *O/S*(CS) to some (possible none) controlled sources if the graph has a complementary tree structure.

Theorem 4

Let N contain only CCCS's or only VCVS's. Then N has a unique solution for all circuit parameters if and only if the associated graph cannot be reduced to any of the cactus graphs with an even number (including zero) of similarly-directed loops by applying operations (a), (b), (c') and (d').

Example 8 Consider the network in Fig. 18(a). Let the controlled sources be denoted by $(k,\hat{k})$ $(k = 1,2,3)$. By inspection we can see that the network has a unique solution as follows. We look for cactus graphs obtained from the associated graph G. Note that there exists no cactus graph including all edges k $(k = 1,2,3)$. By applying operations (a), (b) and (c') we can obtain the cactus graphs in Figs. 18(b) and (c). To apply operation (d'), we must first look for graphs with a complementary tree structure by applying operations (a), (b), (c'). These graphs are shown in Figs. (b)-(d). Applying operation (d') to the graph in Fig. (d), we

[5]Note that the 1-leaf cactus graph in Fig. 15(b) was obtained using operation (d) in Theorem 2. But this operation is not allowed in Theorem 3.

obtain the cactus graphs in Figs. (e) and (f). Since all cactus graphs obtained above have one similarly-directed loops, we conclude the network has a unique solution.

Example 9 Consider the network in Fig. 19(a). Let the controlled sources be denoted by $(k,\hat{k})$ $(k = 1,2,3)$ in the associated graph G. Let us look for all the cactus graphs obtained from G. Note that there exists no three-leaves cactus graphs. By inspection we see that there exists no cactus graph including edges 1 and 3, or edges 2 and 3. We can get the complementary tree structure graph in Fig. 19(b) by applying operations (a) and (b). Then by applying operation (d') to the graph in Fig. 19(b), we get the cactus graphs in Fig. 19(c) and (d). Furthermore we can get a cactus graph in Fig. 19(e) by applying operations (a), (b), and (c'). We can easily verify that the cactus graphs obtainable by operations (a), (b), (c') and (d') are only those shown in Figs. 19(c)-(e). Since the graph in Fig. 19(d) is disallowed, we see that the solution of the network is not unique.

However, if the direction of i_3 is reversed, then the network has a unique solution.

As is seen from Example 12 in Section 5, Theorem 4 cannot be applied to networks containing CCVS's or VCCS's. However the following two theorems hold.

Theorem 5 Let N contain only CCVS's or only VCCS's. Then N has a unique solution for all circuit parameters *if* the associated graph cannot be reduced to any of the cactus graphs with an even number (including zero) of similarly-directed loops by applying operations (a), (b), (c') and (d').

Theorem 6 Let N contain only CCVS's (resp. VCCS's). Suppose that each output edge of the CCVS's (resp. VCCS's) is in series (resp. parallel) with some linear or nonlinear resistor. Then the same conclusion as in Theorem 4 holds.

4. Main Theorems

Let G_0 denote a graph[6] with a complementary tree structure, and let B_T denote the left submatrix[7] of the fundamental loop matrix

$$B = [B_T \vdots \mathbb{1}] \tag{3}$$

Here, T denotes the tree made of the input edges and $\mathbb{1}$ means the identity matrix. Then G_0 is said to have a positive (resp. negative) complementary tree structure iff the determinant of B_T, namely, $|B_T|$ is positive (resp. negative).

[6]Here G_0 corresponds to a reduced network made of controlled sources only.

[7]The submatrix B_T will henceforth be referred to as the main part of the fundamental loop matrix B. Similarly, D_L is called the main part of the fundamental cutset matrix $D \triangleq [\mathbb{1} \vdots D_L]$.

Let N be a nonlinear resistive circuit composed of positive linear resistors, dc sources, nonlinear resistors, and controlled sources which satisfy the conditions mentioned in the Introduction. The following two theorems are the main results of this paper.

Theorem 7 Let N satisfy the interconnection assumption. Then N has a unique solution for all circuit parameters if and only if the associated graph G cannot be reduced to a graph with a negative complementary tree structure by applying operations (a), (b), and (c') (in Theorem 4).

Theorem 8 (General Case)

Let N be a general circuit. Then N has a unique solution for all circuit parameters if and only if by applying operations (a), (b), and (c') to the associated graph , we can obtain at least one graph with a positive complementary tree structure, or a graph with a negative complementary tree structure, but not both. (A one-node graph is regarded as a positive complementary tree structure graph.) In applying operation (c'), the following restriction must be kept.

Restriction: Suppose that in G there exist some loops (resp. cutsets) which do not satisfy the Interconnection Assumption. Then in applying operation (c') we have to keep intact a set of edges such that by opencircuiting (resp. short-circuiting) these edges the loops (resp. cutsets) violating the Interconnection Assumption disappear.

For example, in Fig. 6(c), at least one of the 3 edges $\{i_1 i_2, \alpha_1 i_1\}$ forming the violated loop must be kept intact.

The proofs of Theorems 7 and 8 are given in Section 5.

Example 10 Consider the network in Fig. 20(a), which satisfies the Interconnection Assumption. By applying operations (a), (b), and (c'), the graphs with a complementary tree structure are obtained as shown in Figs. 20(b)-(h). Since all these graphs have a positive complementary tree structure, it follows from Theorem 7 that the network has a unique solution.

Example 11 Consider the networks in Fig. 6 which do not satisfy the Interconnection Assumption.

For the network in Fig. 6(a) (resp. 6(b)) we can obtain only one complementary tree structure graph in Fig. 21(a) (resp. 21(b)). Note that a one-node graph cannot be obtained in virtue of the Restriciton in Theorem 8. Thus we conclude from Theorem 8 that both networks in Figs. 6(a) and (b) have a unique solution.

For the network in Fig. 6(c), we can obtain only two complementary tree structure graphs in Figs. 21(c) and (d). Since both graphs have a negative complementary tree structure, it follows from Theorem 8 that the network in Fig. 6(c) has a unique solution.

On the other hand, for the network in Fig. 6(d) we obtain two complementary tree structures in Figs. 21(e) and (f). The graphs in Figs. 21(e) and (f) has, respecitvely, a positive and a negative complementary tree structure. Therefore we conclude from Theorem 8 that the network does not have a unique solution.

However, if the direction of v_2 is reversed, then the network has a unique solution.

Example 12 Consider the network in Fig. 22(a), which contains 3 CCVS's. By applying operations (a), (b), and (c'), we obtain the graphs with a complementary tree structure in Figs. 22(b)-(h). Since all these graphs have a positive complementary tree structure, we conclude from Theorem 7 that the network has a unique solution (Note that the graph in Fig. 22(c) is not a cactus graph.)

By the way if we apply operations (a), (b), (c'), and (d') to this network, we can obtain the cactus graph in Fig 22(i), which has an even number of similarly directed loops. Therefore it follows that Theorem 4 cannot be applied to this network.

If in Fig. 22(a) there is a resistor in series with the controlled voltage source #3, then we can apply Theorem 6. In this case we can obtain the cactus graph in Fig. 22(i) by applying operations (a), (b), (c'), (d'). Therefore we conclude from Theorem 6 that the network does not have a unique solution.

5. Outline of the Proof of Theorems

First we consider the case where

the Interconnection Assumption is satisfied. (4)

Since a CCCS and a VCVS are realizable as a combination of a CCVS and a VCCS, we will restrict ourselves first to networks containing CCVS's and VCCS's only as controlled sources.

5.1. Analytical Condition for the Solution to Be Unique

Consider the network N in Fig. 23 which consists of k CCVS's, ℓ VCCS's, m nonlinear resistors, and a linear $(2k+2\ell+m)$-port N_0 composed of passive linear resistors and dc voltage and/or current sources. Let CCVS's be connected to the first 2k ports of N_0, VCCS's to the next 2ℓ ports and nonlinear resistors to the last m ports as shown in Fig. 23. Let the port-currents and the port-voltages be i_μ and v_μ $(\mu = 1,2,\ldots,2k+2\ell+m)$, respectively, and let

$$I_a = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_k \end{bmatrix} \qquad V_a = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_k \end{bmatrix}$$

$$I_b = \begin{bmatrix} i_{k+1} \\ \vdots \\ i_{2k} \end{bmatrix} \qquad V_b = \begin{bmatrix} v_{k+1} \\ \vdots \\ v_{2k} \end{bmatrix}$$

$$I_c = \begin{bmatrix} i_{2k+1} \\ \vdots \\ i_{2k+\ell} \end{bmatrix} \qquad V_c = \begin{bmatrix} v_{2k+1} \\ \vdots \\ v_{2k+\ell} \end{bmatrix}$$

$$I_d = \begin{bmatrix} i_{2k+\ell+1} \\ \vdots \\ i_{2k+2\ell} \end{bmatrix} \qquad V_d = \begin{bmatrix} v_{2k+\ell+1} \\ \vdots \\ v_{2k+2\ell} \end{bmatrix}$$

$$I_e = \begin{bmatrix} i_{2k+2\ell+1} \\ \vdots \\ i_{2k+2\ell+m} \end{bmatrix} \qquad V_e = \begin{bmatrix} v_{2k+2\ell+1} \\ \vdots \\ v_{2k+2\ell+m} \end{bmatrix}$$

The characteristics of CCVS's, VCCS's, and nonlinear resistors are represented by

$$V_a = 0 \tag{5a}$$

$$V_b = AI_a \tag{5b}$$

$$I_c = 0 \tag{5c}$$

$$I_d = BV_c \tag{5d}$$

$$-V_e = F(I_e) \tag{5e}$$

where

$$\begin{aligned} A &= \mathrm{diag}[\alpha_1, \alpha_2, \ldots, \alpha_k] \\ B &= \mathrm{diag}[\beta_1, \beta_2, \ldots, \beta_\ell] \end{aligned} \tag{6a}$$

$$\begin{aligned} 0 < \alpha_\mu < \infty \quad (\mu = 1,2,\ldots,k) \\ 0 < \beta_\mu < \infty \quad (\mu = 1,2,\ldots,\ell) \end{aligned} \tag{6b}$$

$$F(I_e) = \begin{bmatrix} f_1(i_{2k+2\ell+1}) \\ \vdots \\ f_m(i_{2k+2\ell+m}) \end{bmatrix} \tag{7a}$$

and

$f_\mu(\mu = 1,2,\ldots,m)$ are strictly monotone-increasing functions mapping R' onto R'. (7b)

Suppose for the moment the following assumption is satisfied.

Assumption 1 The $(2k+2\ell+m)$-port N_0 has an impedance representation.

The case where Assumption 1 does not hold will be treated in 5.4. Then N_0 can be represented by

$$\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix} = \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} & Z_{ad} & Z_{ae} \\ Z_{ba} & Z_{bb} & Z_{bc} & Z_{bd} & Z_{be} \\ Z_{ca} & Z_{cb} & Z_{cc} & Z_{cd} & Z_{ce} \\ Z_{da} & Z_{db} & Z_{dc} & Z_{dd} & Z_{de} \\ Z_{ea} & Z_{eb} & Z_{ec} & Z_{ed} & Z_{ee} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \end{bmatrix} + \begin{bmatrix} E_a \\ E_b \\ E_c \\ E_d \\ E_e \end{bmatrix} \tag{8}$$

Equations (5)-(8) are the basic equations for our present analysis. Set

$$\Delta = \begin{vmatrix} Z_{aa} & Z_{ab} & Z_{ad} & Z_{ae} \\ Z_{ba}-A & Z_{bb} & Z_{bd} & Z_{be} \\ Z_{ca} & Z_{cb} & Z_{cd}-B^{-1} & Z_{ce} \\ Z_{ea} & Z_{eb} & Z_{ed} & Z_{ee}+D \end{vmatrix} \tag{9}$$

where D is a positive definite diagonal matrix.[8]

Lemma 1 For any given values of linear resistors, the network in Fig. 23 has a unique solution for all A, B, and f_μ satisfying (6b) and (7b) if and only if

$$(-1)^\ell \Delta > 0 \text{ for all A, B and D} \tag{10}$$

[8]Throughout this section we assume that A, B, and f_μ satisfy (6b) and (7b), respectively, and that D is a positive definite diagonal matrix, unless otherwise stated.

Proof: See Appendix 1.

Let K and L be sets of numbers $\{1,2,\ldots,k\}$ and $\{1,2,\ldots,\ell\}$, respectively. Let K_1 and K_2 (resp. L_1 and L_2) be a partition of K (resp. L). That is, $K = K_1 \cup K_2$ and $K_1 \cap K_2 = \phi$, and so on. Some of K_μ and L_μ ($\mu = 1,2$) may possibly be the null set. Set

$$\begin{array}{c} \begin{array}{cccc} \overbrace{\phantom{Z_{aa}}}^{k} & \overbrace{\phantom{Z_{ab}}}^{k} & \overbrace{\phantom{Z_{ad}}}^{\ell} & \overbrace{\phantom{Z_{ae}}}^{m} \end{array} \\ \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ad} & Z_{ae} \\ Z_{ba} & Z_{bb} & Z_{bd} & Z_{be} \\ Z_{ca} & Z_{cb} & Z_{cd} & Z_{ce} \\ Z_{ea} & Z_{eb} & Z_{ed} & Z_{ee}+D \end{bmatrix} \end{array} = [p_1 p_2 \cdots p_k \vdots q_1 \cdots q_k \vdots r_1 \cdots r_\ell \vdots s_1 \cdots s_m] \quad (11)$$

and

$$\Delta_\infty = |t_1 t_2 \cdots t_k \vdots q_1 \cdots q_k \vdots u_1 \cdots u_\ell \vdots s_1 \cdots s_m| \quad (12)$$

where

$$t_\mu = \begin{cases} p_\mu & \text{for } \mu \in K_2 \\ \text{zero column vector except for the } (k+\mu)\text{-th element} = -1 & \text{for } \mu \in K_1 \end{cases} \quad (13a)$$

$$u_\mu = \begin{cases} r_\mu & \text{for } \mu \in L_2 \\ \text{zero column vector except for the } (2k+\mu)\text{-th element} = -1 & \text{for } \mu \in L_1. \end{cases} \quad (13b)$$

Lemma 2 The condition (10) is equivalent to the following condition (14).

$$(-1)^\ell \Delta_\infty \geqq 0 \quad \text{for all D and for any partition of K and L} \quad (14a)$$

and

$$(-1)^\ell \Delta_\infty > 0 \quad \text{for some D and for at least one partition of K and L} \quad (14b)$$

Proof: See Appendix 2.

It is easily verified by (4) that

$$(-1)^\ell \Delta_\infty > 0 \quad \text{for } K_1 = K,\ K_2 = \phi,\ L_1 = \phi,\ L_2 = L \text{ and } D \to \infty.^9 \quad (15)$$

Thus the condition (14b) is always satisfied.

Therefore it remains to investigate only the condition (14a).

[9] $D \to \infty$ means that each diagonal element of D is sufficiently large.

5.2. Analysis of the Linear Network

We will investigate the condition for (14a) to hold for all values of linear resistors and for all D. Let

$$\tilde{Z} = \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} & Z_{ad} & Z_{ae} \\ Z_{ba} & Z_{bb} & Z_{bc} & Z_{bd} & Z_{be} \\ Z_{ca} & Z_{cb} & Z_{cc} & Z_{cd} & Z_{ce} \\ Z_{da} & Z_{db} & Z_{dc} & Z_{dd} & Z_{de} \\ Z_{ea} & Z_{eb} & Z_{ec} & Z_{ed} & Z_{ee}+D \end{bmatrix} \tag{16}$$

Equation (16) is the impedance matrix of the network in Fig. 24 where $\tilde{N}_0$ is the network obtained by short-circuiting dc voltage sources and open-circuiting dc current sources, and γ_μ ($\mu = 1,\ldots,m$) denote the linear (positive) resistors. In order to investigate the condition (14a) it suffices to consider $\tilde{Z}$.

The associated graph $\tilde{G}$ of the network in Fig. 24 is defined as the graph obtained from Fig. 24 by replacing each resistor (including γ_μ), each port μ ($\mu = 1,2,\ldots,k$), each port $\mu+k$ ($\mu = 1,2,\ldots,k$), each port $2k+\mu$ ($\mu = 1,2,\ldots,\ell$), each port $2k+\ell+\mu$ ($\mu = 1,\ldots,\ell$), and each port $2k+2\ell+\mu$ ($\mu = 1,\ldots,m$), respectively, by oriented edges R_μ, a_μ, b_μ, c_μ, d_μ, and e_μ. The direction of R_μ is arbitrarily chosen. In Section 5.2 the directions of a_μ, b_μ, c_μ, d_μ and e_μ are assumed to be the same as those of port currents, though

the directions of b_μ, c_μ and d_μ are <u>opposite</u> to those defined in Table 1. (17)

We call R_μ, a_μ, b_μ, c_μ, d_μ, and e_μ, respectively, R-, a-, b-, c-, d-, and e-edge. The graph $\tilde{G}$ is connected by assumption. We further assume that

<u>Assumption 2</u> $\tilde{G}$ has no loop consisting of a-, b-, c-, d-, and e-edges only.

The case where Assumption 2 does not hold will be treated in Section 5.4. Let

$$m_0 = \text{rank of } \tilde{G} - \text{total number of a-, b-, c-, d-, and e-edges} \tag{18}$$

From Assumption 2 it follows that $m_0 \geq 0$.

From Assumption 2 we can modify $\tilde{G}$ by adding m_0 g-edges g_μ ($\mu = 1,2,\ldots,m_0$) so that all the a-, b-, c-, d-, e- and g-edges form a tree, say T, of $\tilde{G}$. For simplicity, we denote hereafter the modified graph by the same symbol $\tilde{G}$. Let the main part of the fundamental cutset matrix of $\tilde{G}$ with respect to T be D_L and let the rows of D_L be arranged in the order of a-, b-, c-, d-, e-, and g-edges. Without loss of generality we will investigate the condition

$$(-1)^{\ell}\Delta_{\infty} \geqq 0 \tag{19}$$

for

$$\begin{aligned} K_1 &= \{1,2,\ldots,k_1\} \quad (0 \leqq k_1 \leqq k) \\ K_2 &= \{k_1+1,\ldots,k\} \\ L_1 &= \{1,2,\ldots,\ell_1\} \quad (0 \leqq \ell_1 \leqq \ell) \\ L_2 &= \{\ell_1+1,\ldots,\ell\} \end{aligned} \tag{20}$$

Set

$$\begin{aligned} k_2 &= k-k_1 \\ \ell_2 &= \ell-\ell_1 \end{aligned} \tag{21}$$

Then D_L can be written as in Fig. 25 where $M = \{1,2,\ldots,m\}$ and $M_0 = \{1,2,\ldots,m_0\}$, and a_{K_1} means the set of a-edges a_μ $(\mu \in K_1)$ and so on. Let

$$H = D_L \textcircled{H}^{-1} D_L' \tag{22}$$

where the prime means the transpose of a matrix and $\textcircled{H}$ is a diagonal matrix whose diagonal elements are the values of linear resistors (including γ_μ in Fig. 24).

<u>Lemma 3</u>

$$(-1)^{\ell}\Delta_{\infty} = (-1)^{\ell+\ell\ell_2+\ell_1+k_1}|H|^{-1}\delta_0 \tag{23}$$

where δ_0 is the determinant of the submatrix shaded by oblique lines in Fig. 26.

<u>Proof</u>: See Appendix 3.

Since $|H| > 0$, it is sufficient for us to consider the sign of $(-1)^{\ell+\ell\ell_2+\ell_1+k_1}\delta_0$. By using (22), we can rewrite δ_0 as

$$\delta_0 = |D_{L_1} \textcircled{H}^{-1} D_{L_2}'| \tag{24}$$

where D_{L_1} (resp. D_{L_2}) is the submatrix of D_L in Fig. 25 shaded by oblique (resp. vertical) lines.

Let $\textcircled{H}_0$ denote an arbitrary set of $k_1+\ell_1+\ell+m_0$ R-edges and δ_1 (resp. δ_2) be the determinant of the submatrix of D_{L_1} (resp. D_{L_2}) consisting of all the rows of D_{L_1} (resp. D_{L_2}) and the columns corresponding to $\textcircled{H}_0$ (See Figs. 25 and 27). Let

$$\delta = (-1)^{\ell+\ell\ell_2+\ell_1+k_1}\delta_1\delta_2 \ . \tag{25}$$

Then

Lemma 4 We can choose the values of resistors so that

$$(-1)^{\ell}\Delta_{\infty} < 0 \tag{26}$$

if and only if there exists a $\textcircled{H}_0$ such that

$$\delta < 0 \ . \tag{27}$$

Proof: See Appendix 4.

Suppose that (27) holds for some $\textcircled{H}_0$. Since δ_1 and δ_2 (and therefore δ) depend on only the rows a_{K_1}, b_{K_1}, C_L, d_L, and g_{M_0} and the columns $\textcircled{H}_0$ of D_L, we define $D_L^{(0)}$ as shown in Fig. 27. Then δ_1 (resp. δ_2) is the determinant of the submatrix shaded by the oblique (resp. vertical) lines in Fig. 27. By carrying out the following operations (i)-(iii) appropriately, we can transform $D_L^{(0)}$ in Fig. 27 into $D_L^{(1)}$ in Fig. 28 where Γ_1, Γ_2, and Γ_3 are nonsingular diagonal matrix whose elements are ± 1 and

$$\begin{bmatrix} Q_1 \\ Q_2 \end{bmatrix} = -\mathbb{1} \ . \tag{28}$$

(i) Multiply some columns by ± 1.

(ii) Add the above columns to other columns

(iii) Interchange the columns.

Set

$$P = \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}, \quad Q = \begin{bmatrix} Q_1 \\ Q_2 \end{bmatrix} \ (=-\mathbb{1}). \tag{29}$$

Since

$$\left.\begin{aligned} \delta_1 &= \varepsilon|\Gamma_1||\Gamma_2||\Gamma_3||P| \\ \delta_2 &= (-1)^{\ell_1\ell_2}\varepsilon|\Gamma_1||\Gamma_2||\Gamma_3||Q| \qquad (\varepsilon=\pm 1) \\ &= (-1)^{\ell_1\ell_2+k_1+\ell_2}\varepsilon|\Gamma_1||\Gamma_2||\Gamma_3|, \end{aligned}\right\} \tag{30}$$

we have by (30) and (25)

$$\delta = (-1)^{\ell_2}|P|. \tag{31}$$

Set

$$D^{(2)} = \begin{array}{c} \\ a_{K_1} \\ c_{L_2} \end{array} \begin{array}{c} \begin{array}{cc} a_{K_1} c_{L_2} & b_{K_1} d_{L_2} \end{array} \\ \left[\begin{array}{c:c} \mathbb{I} & P \end{array}\right] \end{array} . \tag{32}$$

5.3. Graph Theoretical Interpretation of $D^{(2)}$

Lemma 5 · Let $G^{(2)}$ be the graph obtained from $\tilde{G}$ by the following operations:

(i) Apply $S(\cdot)$ to each e-edge and $O(\cdot)$ to each g-edge

(ii) Apply $S(\cdot)$ to R-edges belonging to $\textcircled{H}_0$ and $O(\cdot)$ to all of the remaining R-edges.

(iii) Apply $S(\cdot)$ to edges a_{K_2} and b_{K_2} and $O(\cdot)$ to edges c_{L_1} and d_{L_1}.

Then $G^{(2)}$ is a connected graph with a complementary tree structure and has a fundamental cutset matrix $D^{(2)}$ in (32) if and only if $\delta \neq 0$.

Proof: See Appendix 5.

Lemma 6 Suppose that $G^{(2)}$ obtained in Lemma 5 has a complementary tree structure. Then δ in (31) is positive (resp. negative) if and only if $G^{(2)}$ has a positive (resp. negative) complementary tree structure.

Proof: See Appendix 6.

Lemma 7 Under the Interconnection Assumption we can obtain a (connected) one-node graph by applying operations (a), (b), and (c') to G.

Proof: See Appendix 7.

From Lemmas 1 to 7, we conclude that Theorem 7 is true for the networks in Fig. 23 if Assumptions 1 and 2 are satisfied.

5.4. On the Interconnection Assumption and Assumptions 1 and 2

Lemma 8 Theorem 7 holds for the network in Fig. 23. (That is, Assumptions 1 and 2 are not necessary.)

Proof: See Appendix 8. Finally we obtain

Lemma 9 Theorem 8 holds for the network in Fig. 23.

Proof: See Appendix 9.

5.5. The Case Where Four Types of Controlled Sources Are Included

Let N be an original circuit containing four types of controlled sources. As is well known, a CCCS and a VCVS in Figs. 29(a) and (b) can be realized by a cascade connection of a CCVS and a VCCS as shown in Figs. 29(c) and (d), respectively. Let N_m be the circuit obtained from N by replacing CCCS's and

VCVS with its equivalents in Figs. 29(c) and (d). Let the graphs associated with N and N_m be G and G_m, respectively. Note that if G satisfies the Interconnection Assumption, then so do G_m.

Consider first a CCCS. Renumber the edges of the CCCS and its equivalent as shown in Fig. 30. Since N_m contains only CCVS's and VCCS's, we can apply Lemma 8 to N_m. Let one of the complementary tree structure graphs derived from G_m by operations (a), (b), and (c') be G_{m_0}. Then there exist at most four cases:

1) Edges 1', $\hat{1}$', 1", and $\hat{1}$" in Fig. 30(b) remain in G_{m_0}.
2) Edges 1' and $\hat{1}$' are short-circuited and edges 1" and $\hat{1}$" remain in G_{m_0}.
3) Edges 1' and $\hat{1}$' remain in G_{m_0} and edges 1" and $\hat{1}$" are open-circuited
4) Edges 1' and $\hat{1}$' are short-circuited and edges 1" and $\hat{1}$" are open-circuited.

However, the cases 2) and 3) never occur since G_{m_0} has a complementary tree structure. In case 2), for example, edge 1" form a self-loop.

Applying to G the same operations carried out to G_m by identifying 1' and $\hat{1}$" as 1 and $\hat{1}$, respectively, yields the graph G_0. Then the cases 1) and 4) mentioned above correspond, respectively, to

1') edges 1 and $\hat{1}$ remain in G_0
4') edge 1 is short-circuited and edge $\hat{1}$ is open-circuited.

To avoid ambiguity, let us introduce the following: Let $\hat{G}$ be a graph with a complementary tree structure. Then we denote the main part of the fundamental loop matrix of $\hat{G}$ with respect to a cotree $\bar{T}$ by $MFL(\hat{G};\bar{T})$.

Let

$$\begin{aligned} B_{moT} &= MFL(B_{m_0};\ \text{output edges}) \\ B_{oT} &= MFL(G_0;\ \text{output edges}) \end{aligned} \tag{33}$$

Then referring to Figs. 30(a) and (b), we can write B_{moT} and B_{oT} as follow:

$$B_{moT} = \begin{array}{c} \\ \hat{1}' \\ \hat{1}'' \\ \vdots \end{array} \begin{array}{c} \begin{array}{ccc} 1' & 1'' & \cdots \end{array} \\ \left[\begin{array}{c|c|c} \beta_{11} & \beta_{12} & \beta_{13} \\ \hline -1 & 0 & 0 \\ \hline \beta_{31} & \beta_{32} & \beta_{33} \end{array}\right] \end{array} \tag{34}$$

$$B_{oT} = \begin{array}{c c} & \begin{array}{cc} 1 & \cdots \end{array} \\ \begin{array}{c} \hat{1} \\ \vdots \end{array} & \left[\begin{array}{c|c} \beta_{12} & \beta_{13} \\ \hline \beta_{32} & \beta_{33} \end{array}\right] \end{array} \quad . \tag{35}$$

From (34) and (35) it follows that

$$|B_{moT}| = |B_{oT}| \tag{36}$$

As easily seen, Eq. (36) holds for the case where there are many CCCS's.

In the case of VCVS's we obtain the same result as (36) since the graph representation of Fig. 29(d) is also given by Fig. 30(b).

Thus we conclude that if a graph with a positive (resp. negative) complementary tree structure is obtained from G_m, then (another) graph with a positive (resp. negative) complenentary tree structure can also be obtained from G by operations (a), (b), and (c'). Therefore it is unnecessary to replace CCCS's and VCVS's by the more complicated equivalent circuits in Figs. 29(c) and (d). That is, Theorems 7 and 8 hold for circuits containing 4 types of controlled sources.

5.6. On Theorems 1 to 6

Theorems 1 and 3 follow immediately as special cases of Theorem 7. For Theorems 2, 4, 5, and 6, we need only consider circuits containing CCCS's and CCVS's. For circuits containing VCCS's and VCVS's, the dual discussion holds.

5.6.1. Proof of Theorem 4 for the case of CCCS

Let N be a circuit which satisfies the Interconnection Assumption and does not have a unique solution and let G be its associated graph. Then by Theorem 7 we can obtain a graph G_0 with a negative complementary tree structure by applying operations (a), (b), and (c') to G.

Let

$$B_T = \mathrm{MFL}(G_0;\ \text{output edges}) \tag{37}$$

Then by definition

$$|B_T| < 0 \tag{38}$$

Lemma 10 Let $B_T^{(1)}$ denote an arbitrary principal submatrix of B_T. There exists an operation (c') which operates on G_0 to produce a graph $G^{(1)}$ such that

$$B_T^{(1)} = \mathrm{MFL}(G^{(1)};\ \text{output edges}) \ . \tag{39}$$

Proof: See Appendix 10.

We can find such a principal submatrix, $B_T^{(2)}$, of B_T satisfying the following condition:

1) $|B_T^{(2)}| < 0$

2) Each principal minor (except for $|B_T^{(2)}|$) of $B_T^{(2)}$ is positive or zero.

Suppose that some principal minors of $B_T^{(2)}$ are positive. Then we can choose a principal submatrix $B_T^{(3)}$ such that:

1) $|B_T^{(3)}| > 0$

(2) Each principal minor (except for $|B_T^{(3)}|$ and $|B_T^{(2)}|$) of $B_T^{(2)}$ which includes $B_T^{(3)}$ in it is zero.

Without loss of generality we can rewrite $B_T^{(2)}$ as

$$B_T^{(2)} = \left[\begin{array}{c|c} B_T^{(3)} & B_{12} \\ \hline B_{21} & B_{22} \end{array}\right] \ . \tag{40}$$

Set

$$B_T^{(4)} = B_{22} - B_{21} B_T^{(3)^{-1}} B_{12} \ . \tag{41}$$

Lemma 11 $B_T^{(4)}$ in (41) has the following properties.

1) $|B_T^{(4)}| < 0$ (42)

2) Each principal minor (excluding $|B_T^{(4)}|$) is zero (43)

3) There exists a graph $G^{(4)}$ such that

$$B_T^{(4)} = \mathrm{MFL}(G^{(4)};\ \text{output edges})$$

Proof: See Appendix 11.

Lemma 12 $G^{(4)}$ in Lemma 11 is a cactus graph with an even number of similarly directed loops.

Proof: See Appendix 12.

Lemma 13 The process of obtaining $B_T^{(1)}$, $B_T^{(2)}$ and $B_T^{(3)}$ corresponds to the operation (c') and that of obtaining $B_T^{(4)}$ corresponds to the operation (d').

It follows from Lemmas 10-13 that Theorem 4 holds for the case of CCCS.

5.6.2. Proof of Theorem 5 for the case of CCVS

Let N contain CCVS's. Suppose that we obtain a graph G_0 with a complementary tree structure by applying operations (a), (b), (c'). Let

$$B_T = \mathrm{MFL}(G_0;\ \text{output edges})\ . \tag{44}$$

Suppose that N has a unique solution. Then we have

$$|B_T| \geq 0 \tag{45}$$

Since Lemma 10 does not necessarily hold for N, the statement

each principal minor of B_T is positive or zero (46)

is not necessarily true. However, we can verify that for networks satisfying (45) and (46) we cannot obtain any cactus graph with an even number of similarly directed loops. Conversely, if we cannot obtain such a cactus graph then (45) and (46) hold.

From this and from Lemmas 11-13 Theorem 5 follows

5.6.2. Proof of Theorem 6 for the case of CCVS

Consider the network N in which each controlled voltage source is in series with some resistor. For this network we can prove easily that Lemma 10, as well as Lemmas 11-13 are applicable. From this we conclude Theorem 6.

Theorem 6 can also be proved as follows: By applying Thevenin's Theorem, we can transform controlled voltage sources (with a series resistor) into controlled current sources (with a parallel resistor). Then we can apply Theorem 4 to this modified network. Now we can easily prove that

if for the modified network we can obtain a graph with a positive (or negative) complementary tree structure, then the same is true for the original network. (46)

5.6.3. Proof of Theorem 2

The case of CCCS is a special case of Theorem 4. So we prove Theorem 2 for the case of the CCVS.

Necessity: Suppose that the network N does not have a unique solution. Then we see from Theorem 3 that one of the graphs in Fig. 16 or one- or two-leaves cactus graphs with zero or two similarly-directed loops can be obtained by operations

(a), (b), (c). If one of the graphs in Fig. 16 is obtained, then we can get at least one graph in Fig. 8 by applying operation (d).

Sufficiency: Suppose that we obtain a cactus graph G_0 with zero or two similarly-directed loops by applying operations (a), (b), or operations (a), (b), (c), or operations (a), (b), (d). If operations (a), (b) or operations (a), (b), (c) are used to derive G_0, then it is apparent from Theorem 3 that the solution is not unique.

Suppose that operations (a), (b), (d) are used to derive G_0. (In this case, of course, G_0 is a one-leaf cactus graph.) Let G_1 be a graph to which operation (d) is applied. Then G_1 has a complementary tree structure. Furthermore we can verify that G_1 is either one of the graphs in Fig. 16. Therefore we see from Theorem 3 that the solution of this network is not unique.

In order to complete the proof we have to show that we can obtain the graph G_0 by applying operations (a), (b), (c). We will omit the detail, but we can show this by using the following facts:

1) the network satisfies the Interconnection Assumption,

2) the graph G_1 in Fig. 16 can be derived from the network.

Appendix 1. Proof of Lemma 1

Necessity: Consider the case where f_μ ($\mu = 1,\ldots,m$) are linear functions, that is,

$$F(I_c) = DI_c \ . \tag{A1.1}$$

Then Eqs. (5) and (8) can be written as

$$\begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ad} & Z_{ae} \\ Z_{ba}-A & Z_{bb} & Z_{bd} & Z_{be} \\ Z_{ca} & Z_{cb} & Z_{cd}-B^{-1} & Z_{ce} \\ Z_{ea} & Z_{eb} & Z_{ed} & Z_{ee}+D \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ BV_c \\ I_e \end{bmatrix} = - \begin{bmatrix} E_a \\ E_b \\ E_c \\ E_e \end{bmatrix} \tag{A1.2}$$

Equation (A1.2) has a unique solution for all A, B, D and E if and only if

$$\Delta \neq 0 \text{ for all A, B and D} \ . \tag{A1.3}$$

From (9) it is easily seen that as $D \to \infty$, $A \to 0$, and $B \to 0$, we have

$$\Delta \to (-1)^{\ell} \begin{vmatrix} Z_{aa} & Z_{ab} \\ Z_{ba} & Z_{bb} \end{vmatrix} |B^{-1}||D| \ . \tag{A1.4}$$

Since the impedance matrix in (8) is nonnegative definite,

$$\begin{vmatrix} Z_{aa} & Z_{ab} \\ Z_{ba} & Z_{bb} \end{vmatrix} \geqq 0 \tag{A1.5}$$

holds in general. The equality in (A1.5) however does not hold because of the Interconnection Assumption. Since $|B| > 0$ and $|D| > 0$, the sign of the right hand side of (A1.4) is the same as $(-1)^{\ell}$. Therefore from (A1.3) and the continuity of the function, we obtain (10). Thus the condition (10) is necessary for the network to have a unique solution.

Sufficiency: Suppose that (10) holds. Let

$$\left.\begin{aligned} Z_{11} &= \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ad} \\ Z_{ba}-A & Z_{bb} & Z_{bd} \\ Z_{ca} & Z_{cb} & Z_{cd}-B^{-1} \end{bmatrix} \\ Z_{12} &= \begin{bmatrix} Z_{ae} \\ Z_{be} \\ Z_{ce} \end{bmatrix}, \quad Z_{21} = [Z_{ea}\ Z_{eb}\ Z_{ed}] \\ Z_{22} &= Z_{ee} \ . \end{aligned}\right\} \tag{A1.6}$$

Since (10) holds even if $D \to \infty$, we have

$$(-1)^{\ell}|Z_{11}| > 0 \text{ for all } A \text{ and } B,^{10} \tag{A1.7}$$

which means Z_{11} is nonsingular. On the other hand, we have from (5)-(8)

$$F(I_e) + A_0 I_e = B_0 \tag{A1.8}$$

where

$$\left.\begin{aligned} A_0 &= Z_{22} - Z_{21} Z_{11}^{-1} Z_{12} \\ B_0 &= -E_e + Z_{21} Z_{11}^{-1} \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \end{aligned}\right\} \tag{A1.9}$$

The following lemma is well known.

<u>Lemma A.1</u> (Sandberg and Willson [3]) Equation (A1.9) has a unique solution for all B_0 and all F if and only if $A_0 \in P_0$.

$A_0 \in P_0$ means that

$$|A_0 + D| \neq 0 \text{ for all } D. \tag{A1.10}$$

Since $|A_0 + D| > 0$ as $D \to \infty$, Eq. (A1.10) means that

$$|A_0 + D| > 0 \text{ for all } D \tag{A1.11}$$

From the identity

$$\begin{bmatrix} I & 0 \\ -Z_{21}Z_{11}^{-1} & I \end{bmatrix} \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22}+D \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ 0 & A_0+D \end{bmatrix} \tag{A1.12}$$

we have

$$\Delta = |Z_{11}||A_0 + D| \ . \tag{A1.13}$$

From Eqs. (10), (A1.7) and (A1.13) we conclude that (A1.11) is satisfied. This completes the proof.

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[10] Note that the equality does not hold in (A1.7). For, suppose that $|Z_{11}| = 0$ for some A and some B. Since A and B belong to open neighborhoods, there exist some A and B such that $(-1)^{\ell}|Z_{11}| < 0$, which is not allowed.

Appendix 2

Consider first the following:

Lemma A.2. Let $f(x_1,x_2,\ldots,x_n)$ be a function of degree one in each variable x_μ ($\mu = 1,2,\ldots,n$). Let S be an open set of points such that $S = \{x|\alpha_\mu < x_\mu < \beta_\mu;\ \mu = 1,2,\ldots,n\}$. Then

$$f > 0 \text{ for all } x \in S \tag{A2.1}$$

if and only if the function f evaluated at the "boundary" points where $x_\mu = \alpha_\mu$ or β_μ ($\mu = 1,2,\ldots,n$) is nonnegative (at least one of them must be positive).

Proof of Lemma A.2: By the assumption of Lemma A.2, f can be written as

$$f = (x_1-\alpha_1)\ f_0 + (\beta_1-x_1)f_1 \tag{A2.2}$$

where

$$\left.\begin{aligned} f_0 &= f_0(x_2,x_3,\ldots,x_n) = \frac{1}{\beta_1-\alpha_1}\ f(\beta_1,x_2,x_3,\ldots,x_n) \\ f_1 &= f_1(x_2,x_3,\ldots,x_n) = \frac{1}{\beta_1-\alpha_1}\ f(\alpha_1,x_2,x_3,\ldots,x_n) \end{aligned}\right\} \tag{A2.3}$$

Similarly f_0 and f_1 can be written as

$$\left.\begin{aligned} f_0 &= (x_2-\alpha_2)f_{00} + (\beta_2-x_2)f_{01} \\ f_1 &= (x_2-\alpha_2)f_{10} + (\beta_2-x_2)f_{11} \end{aligned}\right\} \tag{A2.4}$$

where

$$\left.\begin{aligned} f_{00} &= f_{00}(x_3,\ldots,x_n) = \frac{1}{\beta_2-\alpha_2}\ f_0(\beta_2,x_3,\ldots,x_n) \\ f_{01} &= f_{01}(x_3,\ldots,x_n) = \frac{1}{\beta_2-\alpha_2}\ f_0(\alpha_2,x_3,\ldots,x_n) \\ f_{10} &= f_{10}(x_3,\ldots,x_n) = \frac{1}{\beta_2-\alpha_2}\ f_1(\beta_2,x_3,\ldots,x_n) \\ f_{11} &= f_{11}(x_3,\ldots,x_n) = \frac{1}{\beta_2-\beta_2}\ f_1(\alpha_2,x_3,\ldots,x_n) \end{aligned}\right\} \tag{A2.5}$$

Continuing this recursive procedure, we finally obtain

$$\begin{aligned} f = {} & (x_1-\alpha_1)(x_2-\alpha_2)\ \ldots\ (x_n-\alpha_n)f_{00\ldots0} \\ & + (x_1-\alpha_1)(x_2-\alpha_2)\ \ldots\ (x_{n-1}-\alpha_{n-1})(\beta_n-x_n)f_{00\ldots01} \\ & + \ldots \\ & + (\beta_1-x_1)(\beta_2-x_2)\ \ldots\ (\beta_n-x_n)f_{11\ldots1} \end{aligned} \tag{A2.6}$$

where $f_{\varepsilon_1\varepsilon_2\ldots\varepsilon_n}$ is a constant and is obtained by replacing x_μ by α_μ (when $\varepsilon_\mu = 1$) or by β_μ (when $\varepsilon_\mu = 0$). Now if all of $f_{\varepsilon_1\ldots\varepsilon_n}$ are nonnegative and at least one of them is positive, then f is positive for all $x \in S$.

Conversely, if some of $f_{\varepsilon_1\varepsilon_2\ldots\varepsilon_n}$ is negative, then f can be made negative for some $x \in S$. If all of $f_{\varepsilon_1\varepsilon_2\ldots\varepsilon_n}$ are zero, then f vanishes identically. This completes the proof of Lemma A.2.

Lemma A.2 holds even if some α_μ and β_μ are not finite, as demonstrated in the following example:

<u>Example A.1</u> Let

$$f(x_1,x_2) = \begin{vmatrix} a_{11}+b_{11}x_1, & a_{12}+b_{12}x_2 \\ a_{21}+b_{21}x_1, & a_{22}+b_{22}x_2 \end{vmatrix} . \tag{A2.7}$$

The function f satisfies the condition of Lemma A.2. Let S be an open set such that $S = \{x | 0 < x_\mu < \infty;\ \mu = 1,2\}$. Then $f > 0$ for all $x \in S$ if and only if

$$\left.\begin{array}{ll} \begin{vmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{vmatrix} \geqq 0 & \begin{vmatrix} a_{11} & b_{12} \\ a_{21} & b_{22} \end{vmatrix} \geqq 0 \\ \\ \begin{vmatrix} b_{11} & a_{12} \\ b_{21} & a_{22} \end{vmatrix} \geqq 0, & \begin{vmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{vmatrix} \geqq 0 \end{array}\right\} \tag{A2.8}$$

where at least one of the above equalities does not hold.

<u>Proof of Lemma 2</u>. Consider Δ in Eq. (9) as a function of α_μ ($\mu = 1,\ldots,k$) and β_μ ($\mu = 1,\ldots,\ell$) satisfying (6b). Applying Lemma A.2 to Δ, we obtain Lemma 2.

Appendix 3. Proof of Lemma 3

First we shall describe the relation between the matrix H in (22) and the impedance matrix $\tilde{Z}$ of the network in Fig. 24.

In order to calculate $\tilde{Z}$, we connect current sources J to each of the a-, b-, c-, d-, and e-edges, as well as the g-edges. Here, the elements of J are arranged in the order of a-, b-, c-, d-, e-, and g-edges and

$$J = \begin{bmatrix} j_1 \\ \vdots \\ j_{2k+2\ell+m} \\ 0 \end{bmatrix} \begin{matrix} \left.\vphantom{\begin{matrix} j_1 \\ \vdots \\ j_{2k+2\ell+m} \end{matrix}}\right\} 2k+2\ell+m \\ \left.\vphantom{0}\right\} m_0 \end{matrix} \tag{A3.1}$$

Let the voltage vector of the current source J be U. Then we have the standard cutset equation

$$-HU = J \tag{A3.2}$$

(The minus sign in (A3.2) is cue to the fact that the positive directions of the voltages are taken opposite to those of the current sources.) From (A3.2) it follows that $\tilde{Z}$ is given as the upper left $(2k+2\ell+m) \times (2k+2\ell+m)$ principal submatrix of H^{-1}.

Next consider Δ_∞ for K_1, K_2, L_1 and L_2 in (20). Let Z_1 be the matrix $\tilde{Z}$ in Fig. A.2 with the columns a_{K_1} and d_{L_1} replaced, respectively, by

$$\begin{bmatrix} 0 \\ -\mathbb{I} \\ 0 \end{bmatrix} \begin{matrix} \}k \\ \}k_1 \\ \}k_2+2\ell+m \end{matrix} \quad \text{and} \quad \begin{bmatrix} 0 \\ -\mathbb{I} \\ 0 \end{bmatrix} \begin{matrix} \}2k \\ \}\ell_1 \\ \}\ell_2+\ell+m \end{matrix} .$$

Then Δ_∞ is equal to the determinant of the shaded submatrix of Z_1 in Fig. A.2. For the calculation of the above determinant, we can apply Laplace expansion with respect to the columns a_{K_1} and d_{L_1}. Consequently, we have

$$\Delta_\infty = (-1)^{k_1+\ell_1+kk_1} |Z_2| \tag{A3.3}$$

where Z_2 is the submatrix of $\tilde{Z}$ consisting of the rows a_K, b_{K_2}, C_{L_2}, e_M and the columns a_{K_2}, b_K, d_{L_2}, e_M. We can relate $|Z_2|$ with a minor of H by the following well-known lemma.

Lemma A.3 [4] Let A be a nonsingular matrix of order n. If $B = A^{-1}$, then for arbitrary

$$\left(1 \leq \begin{matrix} i_1 < i_2 < \cdots < i_p \\ h_1 < h_2 < \cdots < h_p \end{matrix} \leq n\right)$$

$$B\begin{pmatrix} i_1 i_2 \cdots i_p \\ h_1 h_2 \cdots h_p \end{pmatrix} = \frac{(-1)^{\sum_1^p i_\mu + \sum_1^p h_\mu} A\begin{pmatrix} h'_1 h'_2 \cdots h'_{n-p} \\ i'_1 i'_2 \cdots i'_{n-p} \end{pmatrix}}{A\begin{pmatrix} 1,2,\ldots,n \\ 1,2,\ldots,n \end{pmatrix}} \tag{A3.4}$$

where $i_1 < i_2 < \cdots < i_p$ and $i_{1'} < i'_2 < \cdots < i'_{n-p}$ form a complete system of indices $1,2,\ldots,n$, as do $h_1 < h_2 < \cdots < h_p$ and $h'_1 < h'_2 < \cdots < h'_{n-p}$.

Since Z_2 is the submatrix of H^{-1}, we can apply Lemma A.3 to $|Z_2|$. By setting

$$\begin{aligned}
A &= H \\
n &= 2k+2\ell+m+m_0 \\
p &= k+k_2+\ell_2+m \\
i_\mu &= \mu(\mu = 1,2,\ldots,k) \\
i_{k+\mu} &= k+k_1+\mu(\mu = 1,2,\ldots,k_2) \\
i_{k_2+k+\mu} &= 2k+\ell_1+\mu(\mu = 1,2,\ldots,\ell_2) \\
i_{k+k_2+\ell_2+\mu} &= 2k+2\ell+\mu(\mu = 1,2,\ldots,m) \\
h_\mu &= k_1+\mu(\mu = 1,2,\ldots,k_2) \\
h_{k_2+\mu} &= k+\mu(\mu = 1,2,\ldots,k) \\
h_{k+k_2+\mu} &= 2k+\ell+\ell_1+\mu(\mu = 1,2,\ldots,\ell_2) \\
h_{k+k_2+\ell_2+\mu} &= 2k+2\ell+\mu(\mu = 1,2,\ldots,m)
\end{aligned}$$

we have

$$|Z_2| = (-1)^{k^2+kk_2+\ell\ell_2}|H|^{-1}\delta_0 \tag{A3.5}$$

From (A3.3) and (A3.5), we get Eq. (23).

Appendix 4. Proof of Lemma 4

Suppose that we calculate δ_0 in (24) by using the Binet-Cauchy's formula [4]. Since δ_1 and δ_2 depend on the choice of $Ⓗ_0$, we write them temporarily as $\delta_1(Ⓗ_0)$ and $\delta_2(Ⓗ_0)$. Let the principal minor of Ⓗ corresponding to $Ⓗ_0$ be $\eta(Ⓗ_0)$. Then Binet-Cauchy's formula says that

$$\delta_0 = \Sigma\delta_1(Ⓗ_0)\ \delta_2(Ⓗ_0)\eta^{-1}(Ⓗ_0) \tag{A4.1}$$

where the summations are taken over all possible combinations of $Ⓗ_0$. Note that $\eta^{-1}(Ⓗ_0)$ is positive. If $\delta \geqq 0$ for each $Ⓗ_0$, then we have by (23), (25) and (A4.1) $(-1)^{\ell}\Delta_{\infty} \geqq 0$.

Conversely suppose that there exists a $Ⓗ_0$ such that $\delta < 0$. Then by (A4.1) we can make $(-1)^{\ell}\Delta_{\infty}$ negative by choosing the values of resistors included in $Ⓗ_0$ sufficiently small and those of all other resistors sufficiently large. This completes the proof.

Appendix 5. Proof of Lemma 5

First we introduce some notations. Let G_0 be a graph having a set E of edges and a tree T. Let E_1 and E_2 be subsets of E such that $E_1 \cap E_2 = \phi$. Then $G_0(E_1; E_2)$ is defined as the graph obtained from G_0 by applying $S(\cdot)$ to each of the edges in E_1 and $O(\cdot)$ to each of the edges in E_2.

Let $MFC(G_0; T)$ denote the main part of the fundamental cutset matrix of G_0 with respect to T. It is well known that

1) Deletion of a row of $MFC(G_0; T)$ corresponds to applying operation $S(\cdot)$ to an edge belonging to the tree T. (A5.1)
2) Deletion of a column of $MFC(G_0; T)$ corresponds to applying operation $O(\cdot)$ to an edge belonging to the cotree $\bar{T}$.

Let

$$G^{(0)} = \tilde{G}(e_M; R_{Ⓗ-Ⓗ_0}) . \tag{A5.2}$$

Then it follows from (A5.1) that $G^{(0)}$ is connected and

$$D_L^{(0)} = MFC(G^{(0)}; a_{K_1}, b_{K_1}, c_L, d_L, g_{M_0}) . \tag{A5.3}$$

In order to understand the graphical meaning of $D^{(2)}$, we need the following lemma.

Lemma A.4. Let G_0 be a connected graph with a tree, T, and let $D_{0L} = MFC(G_0; T)$. Suppose that the element (i,j) of D_{0L} is nonzero. Then we multiply the j-th column of D_{0L} by 1, -1, or 0 and add them to all the other columns so that all the elements of the i-th row except for the element (i,j) vanish. We call this operation "sweeping out by the pivot (i,j)." Let the new matrix obtained by the above operation be $\hat{D}_{0L}$. Let $\hat{G}_0$ be the (connected) graph derived from G_0 by

1) short-circuiting the edge j of the cotree, and
2) inserting the new edge j so that the edge j and the edge i (tree branch) are in series, and the edges i and j have the same (opposite) direction in the fundamental cutset of $\hat{G}_0$ if they have the same (opposite) direction in the fundamental cutset of G_0 (see Fig. A.3).

Then the edges in T form a tree $\hat{T}$ of $\hat{G}_0$ and

$$\hat{D}_{0L} = MFC(\hat{G}_0; \hat{T}). \tag{A5.4}$$

In addition, applying $O(\cdot)$ to the edges i and j of $\hat{G}$ leaves a connected graph.

Since the proof of Lemma A.4 is rather involved, it is omitted here. However, we will give an example illustrating Lemma A.4.

<u>Example A.2</u> Let G_0 be a graph shown in Fig. A.4(a). We choose a tree T as {a,b,c}. Then D_{0L} is given by

$$D_{0L} = \begin{array}{c} \\ a \\ b \\ c \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} & 1 & & 1 & \\ 1 & & & -1 & -1 \\ & & 1 & -1 & -1 \end{bmatrix} \end{array} \tag{A5.5}$$

Applying the "sweeping out by the pivot (b,5)" operation we get

$$\hat{D}_{0L} = \begin{array}{c} \\ a \\ b \\ c \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} & 1 & & 1 & \\ & & & & -1 \\ -1 & & 1 & & -1 \end{bmatrix} \end{array} \tag{A5.6}$$

Then $\hat{D}_{0L} = MFC(\hat{G}_0; \hat{T})$ where $\hat{G}_0$ is the graph shown in Fig. A.4(b).

Suppose that

$$\left.\begin{array}{l} \delta_1 \neq 0 \\ \delta_2 \neq 0 \end{array}\right\} \tag{A5.7}$$

Under the condition (A5.7) we can continue to apply the sweeping out by appropriate privots operation until $D_L^{(1)}$ in Fig. 28 is obtained. Then from Lemma A.4 it follows that

$$D_L^{(1)} = MFC(G^{(1)}; a_{K1}, b_{K1}, C_L, d_L, g_{M0}) . \tag{A5.8}$$

Here, $G^{(1)}$ is the graph obtained from $G^{(0)}$ by short-circuiting each R-edge and inserting it in series with one of b_{K1}, C_{L1}, d_{L1}, d_{L2} and g_{M0} as stated in Lemma A.4. Let

$$\hat{D}^{(2)} = \begin{array}{c} \\ a_{K1} \\ c_{L2} \\ b_{K1} \\ d_{L2} \end{array} \begin{array}{c} \textcircled{H}_4 \\ \left[\begin{array}{c} P \\ \hline Q \end{array}\right] \end{array} \quad (Q = -\mathbb{1}) \tag{A5.9}$$

and

$$\hat{G}^{(2)} = G^{(1)}(c_{L1}, d_{L1}, g_{M0}; \textcircled{H}_1, \textcircled{H}_2, \textcircled{H}_3) \tag{A5.10}$$

where $\textcircled{H}_i (i = 1,2,3,4)$ are sets of R-edges corresponding to the columns Γ_1, Γ_2, Γ_3 and P in Fig. 28. Then it follows from (A5.1) that

$$\hat{D}^{(2)} = \mathrm{MFC}(\hat{G}^{(2)};\ a_{K1}, b_{K1}, c_{L2}, d_{L2}) \tag{A5.11}$$

and that

each R-edge in $\hat{G}^{(2)}$ is in series with one of b_{K1} and d_{L2} and has the same direction with it. (A5.12)

Let

$$\hat{\hat{G}}^{(2)} = \hat{G}_2(\phi;\ \textcircled{H}_4) \tag{A5.13}$$

Then from (A5.12) we have

$$P = \mathrm{MFC}(\hat{\hat{G}}^{(2)};\ a_{K1}, c_{L2}) \ . \tag{A5.14}$$

From the definitions of $G^{(2)}$ and $\hat{\hat{G}}^{(2)}$, we conclude that

$$G^{(2)} = \hat{\hat{G}}(2) \ , \tag{A5.15}$$

from which the first part of Lemma 5 follows.

We can also verify that

if $\delta_1 = 0$ or $\delta_2 = 0$ then the graph $G^{(2)}$ obtained in Lemma 5 is not connected or does not have a complementary tree structure. (A5.16)

Proof of (A5.16) is omitted.

Appendix 6 Proof of Lemma 6

Until now we have adopted the direction (17). If we adopt the direction in Table 1, then we have to reverse the direction of b-, c-, and d-edges. We represent MFC(•) and MFL(•) (defined in Section 5.5) based on the direction in Table 1 by $MFC_{T1}(\cdot)$ and $MFL_{T1}(\cdot)$, respectively.

Since the graph $G^{(2)}$ includes k_1 b-edges, ℓ_2 c-edges, and ℓ_2 d-edges, respectively.

$$|MFC_{T1}(G^{(2)};\ a_{K1},c_{L2})| = (-1)^{k_1+2\ell_2}|MFC(G^{(2)};\ a_{K1},c_{L2})| \tag{A6.1}$$
$$= (-1)^{k_1+2\ell_2}|P|$$

It therefore follows from (31) that

$$\delta = (-1)^{k_1+\ell_2}|MFC_{T1}(G^{(2)};\ a_{K1},c_{L2})| \tag{A6.2}$$

Since $MFL_{T1}(G^{(2)};\ b_{K1},d_{L2})$ is equal to $-[MFC_{T1}(G^{(2)};\ a_{K1},c_{L2})]'$, it follows that

$$|MFL_{T1}(G^{(2)};\ b_{K1},d_{L2})| = (-1)^{k_1+\ell_2}|MFC_{T1}(G^{(2)};\ a_{K1},c_{L2})|\ . \tag{A6.3}$$

From (A6.2) and (A6.3) it follows that

$$\delta = |MFL_{T1}(G^{(2)};\ b_{K1},d_{L2})|\ . \tag{A6.4}$$

From (A6.4) and from the definition of a positive (or negative) complementary tree structure, Lemma 6 follows.

Appendix 7 Proof of Lemma 7

Applying $Z(\cdot)$ to all the elements in the network, we get a connected one-node graph. For, otherwise, there exists a cutset consisting of dc current sources, controlled current sources, and voltage controlling edges. This contradicts the Interconnection Assumption.

Appendix 8 Proof of Lemma 8

First consider Assumption 2. Since each e-edge is in series with an R-edge, it suffices to consider a loop $\mathcal{L}$ consisting of a-, b-, c-, and d-edges only. For simplicity we assume that Assumption 1 still holds. From the Interconnection Assumption we see that $\mathcal{L}$ includes some c- or d-edges. Let one of them be ξ. Then we modify the associated graph G by inserting an R-edge, say R_0, in series with ξ. Since this corresponds to inserting a resistor in series with an input of a VCCS or VCVS, or with an output of a VCCS or CCCS, this does not affect the currents and voltages of each element (except for ξ) of the network. Thus the insertion of the R-edge R_0 does not affect the uniqueness of the solution. Let the modified graph be G_m. Since G_m satisfies Assumptions 1 and 2, we can apply Theorem 7 to G_m. Let us investigate whether the edge R_0 should be open-circuited or short-circuited when applying operations (a), (b) and (c').

Suppose first that ξ is open-circuited in operation (c'). Then the resultant graph does not depend on whether R_0 is open-circuited or short-circuited because ξ and R_0 were in series. In this case therefore we can regard that R_0 is short-circuited.

Suppose that the edge ξ remains after operations (a), (b), (c'). Then since ξ must be a branch of a tree in the resultant graph,[11] R_0 should be short-circuited in this case.

After all we can regard that the edge R_0 should always be short-circuited in operation (b). This means that we need not insert the new edge R_0 at all. Thus we conclude that Theorem 5 still holds even if Assumption 2 is not satisfied.

Next consider Assumption 1. For simplicity we assume that Assumption 2 holds. Suppose that Assumption 1 is not satisfied. Then there exists a cutset C consisting of a-, b-, c-, d-, and e-edges only. From the Interconnection Assumption it follows that C contains at least one a-, b-, or e-edge. Let it be ξ.

We modify the associated graph G by inserting an R-edge, say R_0, in parallel with ξ. Let the modified graph be G_m. Insertion of the R-edge R_0 corresponds to the following operations.

1) If ξ is an a-edge, then connect a resistor in parallel with an input port of a CCVS or CCCS.

[11] Note that the resultant graph must have a complementary tree structure.

2) If ξ is a b-edge, then connect a resistor in parallel with an output port of a VCVS or CCVS.

3) If ξ is an e-edge, then replace a nonlinear resistor in Fig. A.5(a) by the network in Fig. A.5(b).

Apparently cases 1) and 2) do not affect the uniqueness of the solution. It is not true that the nonlinear resistor f always has an equivalent network in Fig. A.5(b) where f and $\tilde{f}$ satisfy (7b) and $\tilde{R}$ is positive. In spite of this, the replacement of Fig. A.5 is valid for our discussion. For, assume that the original network has a unique solution for all circuit parameters (including nonlinear characteristics). Then since the network in Fig. A.5(b) belongs to a class of nonlinear resistors, the modified network also has a unique solution.

Conversely assume that the original network has more than one solution for some circuit parameters. Then let the operating points of the nonlinear resistor f be (v_1,i_1) and (v_2,i_2) in Fig. A.6. We can replace the nonlinear resistor f by the network in Fig. A.5(b) which has the same operating points (v_1,i_1) and (v_2,i_2). Thus the network obtained by the replacement has more than one solution.

Thus we see that case 3) does not affect the uniqueness of the solution. Now we can apply Theorem 7 to G_m. Let us investigate whether the R-edge R_0 should be open-circuited or short-circuited in operation (b). If ξ is an e-edge, then we can regard that R_0 is open-circuited because R-edges ξ and R_0 are in parallel in G_m. Suppose that ξ is an a- or a b-edge. If ξ is short-circuited in operation (c'), then we can regard that R_0 is open-circuited. If ξ remains after operation (c'), then R_0 must be open-circuited. For, ξ must be a tree branch of a resultant graph (otherwise, ξ forms a self-loop). Thus we can regard that R_0 should always be open-circuited in operation (b). Consequently, we conclude that the insertion of R_0 is not necessary. That is, Theorem 7 holds even if Assumption 1 is not satisfied.

Even in the case where neither Assumption 1 nor 2 is satisfied, similar discussion holds.

Appendix 9 Proof of Lemma 9

By referring to Lemma 7, it is seen that the difference between Theorems 7 and 8 is that Theorem 8 includes the case where the Interconnection Assumption is not satisfied. So we consider only this case for the network in Fig. 23.

If the Interconnection Assumption is not satisfied, then in the associated graph G there occurs at least one of the following situations.

1) There exist loops consisting of a-edges only or b-edges only.

2) There exist cutsets consisting of c-edges only or d-edges only.

3) There exist loops consisting of both a-edges and b-edges.

4) There exist cutsets consisting of both c-edges and d-edges.

Suppose that case 1) occurs. For simplicity we assume that cases 2), 3), 4) do not occur. Then since the rows (and columns) a_K and b_K of $\tilde{Z}$ are linearly dependent, Δ in (9) vanishes identically independent of A, B and D. Therefore we see that the solution is not unique in this case. On the other hand we cannot obtain any graph with a complementary tree structure by applying operations (a), (b), (c') in virtue of the Restriction in Theorem 8. Therefore we conclude that Theorem 8 holds for case 1).

Since case 2) is the dual of case 1), similar discussion holds.

Next consider case 3). For simplicity we assume that cases 1), 2), and 4) don't occur. Then the impedance matrix in (8) satisfies

$$\begin{vmatrix} Z_{aa} & Z_{ab} \\ Z_{ba} & Z_{bb} \end{vmatrix} = 0 \tag{A9.1}$$

Therefore in this case (10) is not necessary for the network to have a unique solution. Instead of (10) however we can show that either of the condition (A9.2) must be satisfied.

$$(-1)^{\ell}\Delta > 0 \quad \text{for all A, B, and D} \tag{A9.2a}$$

$$(-1)^{\ell}\Delta < 0 \quad \text{for all A, B, and D.} \tag{A9.2b}$$

Equation (A9.2a) is the same as (10). Note that there exist networks satisfying (A9.2b). For example, the networks in Figs. 6(a) and (c) satisfy (A9.1) and (A9.2b) and therefore have a unique solution.

Let us investigate the condition (A9,2a) or (A9,2b). In case (A9.1) we can insert m_1 resistors ε_μ ($\mu = 1,\ldots,m_1$) in series with some a-edges so that the modified network N_m satisfies the Interconnection Assumption and Assumptions 1 and 2. Here, the number m_1 is equal to the number of independent loops consisting of a-edges and b-edges only. The values of resistors ε_μ are assumed to be sufficiently small. For the modified network N_m we can follow the discussion described in Sections 5.1-5.5. However, note that in this case $\textcircled{H}_0$ in Fig. 25 must always include all ε_μ ($\mu = 1,2,\ldots,m_1$). This means from the graph-theoretical point of view that the Restriction in Theorem 8 must be satisfied.

In case 4) the dual situation holds.

This completes the proof.

Appendix 10 Proof of Lemma 10

Let G_0 be a graph with a complementary tree structure, let T and $\bar{T}$ denote a tree and a cotree of G_0, and let

$$\underline{B}_{oT} = MFL(G_0;\ \bar{T}) \tag{A10.1}$$

Then it is well known that

1) the deletion of a row of B_{oT} corresponds to open-circuiting an edge belonging to $\bar{T}$, and

2) the deletion of a column of B_{oT} corresponds to short-circuiting an edge belonging to T.

Since operations (c') for CCCS's means the operations *S* (input edge) and *O* (output edge), we obtain Lemma 10.

Appendix 11 Proof of Lemma 11

Property 1) follows immediately from the identity

$$|B_T^{(2)}| = \begin{vmatrix} B_T^{(3)} & B_{12} \\ B_{21} & B_{22} \end{vmatrix}$$

$$= |B_T^{(3)}|\,|B_{22}-B_{21}B_T^{(3)^{-1}}B_{12}| \quad . \tag{A11.1}$$

To prove 2), suppose that the upper left $n_2 \times n_2$ principal submatrix $B_T^{(5)}$ ($\neq B_T^{(4)}$) is nonsingular. Let $B_T^{(3)}$ be an $n_1 x n_1$ matrix. Then we can easily verify that the upper left $(n_1+n_2) \times (n_1+n_2)$ principal minor of $B_T^{(2)}$ is nonzero (more exactly, positive by the definition of $B_T^{(2)}$. This contradicts the definition of $B_T^{(3)}$.

Let

$$B^{(2)} = \begin{array}{c} \\ b_{K_1} \\ \\ \end{array}\begin{array}{c} \overbrace{\qquad\qquad\qquad\qquad}^{b_{K_1}} \quad \overbrace{\qquad\qquad\qquad\qquad}^{a_{K_1}} \\ \begin{array}{cc|cc|cc|cc} b_{K_{11}} & b_{K_{12}} & a_{K_{11}} & a_{K_{12}} \end{array} \\ \begin{array}{c} b_{K_{11}} \\ b_{K_{12}} \end{array}\left[\begin{array}{c|c|c|c} I & 0 & B_T^{(3)} & B_{12} \\ 0 & I & B_{21} & B_{22} \end{array}\right] \end{array} \quad . \tag{A11.2}$$

Then $B^{(2)}$ is the fundamental loop matrix of $G^{(2)}$ with respect to a cotree b_{K_1}. Multiplying the row $b_{K_{11}}$ by $B^{(3)-1}$ and adding it to the row $b_{K_{12}}$, we get

$$\tilde{B}^{(2)} = b_{K_1}\begin{cases} b_{K_{11}}\{ \\ b_{K_{12}}\{ \end{cases}\left[\begin{array}{c|c|c|c} B_T^{(3)^{-1}} & 0 & I & B_T^{(3)^{-1}}B_{12} \\ \hline -B_{21}B_T^{(3)^{-1}} & I & 0 & B_T^{(4)} \end{array}\right] \quad . \tag{A11.3}$$

The matrix $\tilde{B}_T^{(2)}$ is the fundamental loop matrix of $G^{(2)}$ with respect to a cotree $b_{K_{12}}$ and $a_{K_{11}}$. Open-circuiting edges $a_{K_{11}}$ and short-circuiting edges $b_{K_{11}}$ we get a graph $G^{(4)}$ of which the fundamental loop matrix is given by

$$B^{(4)} = \begin{array}{c} \begin{array}{cc} {}^{b}K_{12} & {}^{a}K_{12} \end{array} \\ {}^{b}K_{12}\begin{bmatrix} I & B_T^{(4)} \end{bmatrix} \end{array} . \qquad \text{(A11.4)}$$

This proves property 3).

Appendix 12 Proof of Lemma 12

Let

$$S = \mathrm{MFL}(G^{(4)};\ \text{output edges}) \tag{A12.1}$$

Lemma A.5 Suppose that

1) S is nonsingular

2) each principal minor (except for $|S|$) is zero (A12.2)

Then $G^{(4)}$ is a cactus graph

Proof of Lemma A.5 Let $S = [S_{ij}]$ be an nxn matrix. By (A12.2) we have

$$S_{ii} = 0 \ (i = 1,2,\ldots,n) \tag{A12.3}$$

Without loss of generality we assume that

$$S_{21} = \varepsilon_1 \neq 0 \ . \tag{A12.4}$$

From (A12.3) and (A12.4) it follows that

$$S_{12} = 0 \ . \tag{A12.5}$$

For, otherwise

$$\begin{vmatrix} 0 & S_{12} \\ S_{21} & 0 \end{vmatrix} \neq 0 \ ,$$

which contradicts (A12.2). Similarly we can assume

$$S_{32} = \varepsilon_2 \neq 0 \ , \tag{A12.6}$$

from which

$$S_{13} = S_{23} = 0 \tag{A12.7}$$

follows. Continuing this process, we conclude that S has the form

$$S = \begin{bmatrix} 0 & 0 & \cdots & 0 & \varepsilon_n \\ \varepsilon_1 & 0 & 0 & & 0 \\ & \varepsilon_2 & 0 & \ddots & \vdots \\ & & \ddots & \ddots & 0 \\ & & & \varepsilon_{n-1} & 0 \end{bmatrix} \tag{A12.8}$$

where $\varepsilon_i = \pm 1$.

We have to show that each element of the shaded part in (A12.8) is zero. Let $S(n_1, n_2, \ldots, n_t)$ denote the principal minor of S consisting of rows $n_1, n_2, \ldots, n_t$ and columns $n_1, n_2, \ldots, n_t$. Then we can conclude that $S_{ij} = 0$ (for $i > j+1$) using the following relations:

$$\left.\begin{array}{l} \left\{\begin{array}{l} S(1,n) = 0 \Rightarrow S_{n1} = 0 \\ S(1,2,n) = 0 \Rightarrow S_{n2} = 0 \\ S(1,2,3,n) = 0 \Rightarrow S_{n3} = 0 \\ \quad\vdots \\ S(1,2,\ldots,n-2,n) = 0 \Rightarrow S_{n,n-2} = 0 \end{array}\right. \\ \left\{\begin{array}{l} S(1,n-1,n) = 0 \Rightarrow S_{n-1,1} = 0 \\ S(1,2,n-1,n) = 0 \Rightarrow S_{n-1,2} = 0 \\ \quad\vdots \\ S(1,2,\ldots,n-3,n-1,n) = 0 \Rightarrow S_{n-1,n-3} = 0 \end{array}\right. \\ \left\{\begin{array}{l} S(1,n-2,n-1,n) = 0 \Rightarrow S_{n-2,1} = 0 \\ \quad\vdots \end{array}\right. \end{array}\right\} \tag{A12.9}$$

Finally we obtain

$$S = \begin{bmatrix} 0 & & & & \varepsilon_n \\ \varepsilon_1 & 0 & & \bigcirc & \\ & \varepsilon_2 & 0 & & \\ & \bigcirc & \ddots & \ddots & \\ & & & \varepsilon_{n-1} & 0 \end{bmatrix} \tag{A12.10}$$

Therefore $G^{(4)}$ is a cactus graph, by definition. From (A12.10) we have

$$|S|(=|B_T^{(4)}|) = (-1)^{n-1}\varepsilon_1\ \varepsilon_2 \ldots \varepsilon_n \quad . \tag{A12.11}$$

Let n_+ (resp. n_-) denote the number of positive (resp. negative) ε_i. Then we see that

$$|S| < 0 \tag{A12.12}$$

if and only if

$$\left.\begin{array}{l} \text{both } n \text{ and } n_- \text{ are even} \\ \text{or} \\ \text{both } n \text{ and } n_- \text{ are odd .} \end{array}\right\} \tag{A12.13}$$

Equation (A12.12) can be summarized as follows

$$n_+(= n - n_-) \text{ is even .} \tag{A12.14}$$

This completes the proof of Lemma 12.

References

[1] R. O. Nielsen and A. N. Willson, "A fundamental result concerning the topology of transistor circuits with multiple equilibria," Proc. IEEE, vol. 68, pp. 196-208, February 1980.

[2] L. O. Chua, Introduction to Nonlinear Network Theory, McGraw-Hill, New York, NY 1969.

[3] I. W. Sandberg and A. N. Willson, "Some theorems on properties of dc equations of nonlinear networks," Bell Syst. Tech. J., vol. 48, pp. 1-34, January 1969.

[4] F. R. Gantmacher, The Theory of Matrices, Chelsea Pub. Co., New York, NY 1959.

Figure Caption

Fig. 1. Simple circuit containing one controlled source (4 different types) and a strictly monotone-increasing resistor.

Fig. 2. Load line intersecting v_R-i_R curve in at least 2 points.

Fig. 3. (a) Open-circuit operation $k \mapsto \mathcal{O}(k)$
(b) Short-circuit operation $k \mapsto \mathcal{S}(k)$

Fig. 4. $(k,\hat{k}) \mapsto (\mathcal{O}(k), \mathcal{S}(k))$ or $(\mathcal{S}(k); \mathcal{O}(k))$

Fig. 5. Definition of the operation $Z(CS)$

Fig. 6. Circuits which do not satisfy the Interconnection Assumption

Fig. 7. Cactus graphs

Fig. 8. Disallowed graph: edge 1 is associated with the input (controlling) variable and edge $\hat{1}$ is associated with the output (controlled) variable of the controlled source.

Fig. 9. Circuits for Example 1 ($\alpha>0$): only circuits on the left have a unique solution.

Fig. 10. 2-leaves cactus graph in which the direction of edges is not assigned. Edges $\{1, \hat{1}\}$ are associated with controlled source 1; edges $\{2, \hat{2}\}$ are associated with controlled source 2. Disallowed 2-leaves cactus graph is defined as the graph with zero or two similarly-directed loops in Fig. 10.

Fig. 11. Circuit for Example 2: the disallowed graph in (d) implies the solution is not unique.

Fig. 12. Circuit for Example 3: No disallowed graphs are found; hence the solution is unique.

Fig. 13. Circuit for Example 4

Fig. 14. Circuit for Example 5

Fig. 15. Circuit containing 2 different types of controlled sources.

Fig. 16. Typical disallowed 4-edge graphs which are different from 2-leaves cactus graph.

Fig. 17. Circuit for Example 7

Fig. 18. Circuit for Example 8

Fig. 19. Circuit for Example 9

Fig. 20. Circuit for Example 10

Fig. 21. Complementary tree structure graphs obtained from networks in Fig. 6.

Fig. 22. Circuit for Example 12

Fig. 23. Circuit containing "k" CCVS's, "ℓ" VCCS's and "m" nonlinear resistors.

Fig. 24. Linear resistance $(2k+2\ell+m)$-port corresponding to $\tilde{Z}$ in (16).

Fig. 25. The main part of the fundamental cutset matrix of the graph $\tilde{G}$. The a-, b-, c-, d-, e-, and g-edges are chosen to be the tree.

Fig. 26. The coefficient matrix H associated with the cutset equation in (A3.2).

Fig. 27. Submatrix of D_L in Fig. 25. This is identified as the main part of the fundamental cutset matrix of the graph $G^{(0)}$.

Fig. 28. Matrix obtained from $D_L^{(0)}$ by applying the "sweeping-out-by-some-pivots" operations. This is indentified as the main part of the fundamental cutset matrix of the graph $G^{(1)}$.

Fig. 29. Equivalent circuits of a CCCS and a VCVS by using a CCVS and a VCCS.

Fig. 30. Graph representation of the networks in Fig. 29.

Fig. A.1. Disallowed 2-leaves cactus graph.

Fig. A.2. Impedance matrix $\tilde{Z}$ of the network in Fig. 24.

Fig. A.3. Graph-theoretical interpretation of "sweeping-out-by-the-pivot (i,j)" operation.

Fig. A.4. Graphs for Example A.2. Figs (a) and (b) correspond to (A5.5) and (A5.6), respectively.

Fig. A.5. Replacement of nonlinear resistor f by the parallel combination of $\tilde{f}$ and R_0.

Fig. A.6. Characteristic v-i curve of a nonlinear resistor.

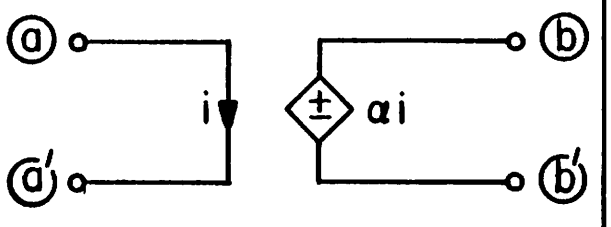
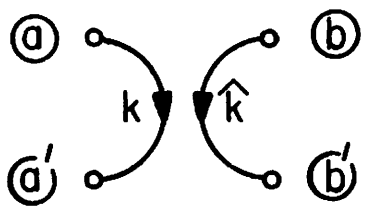
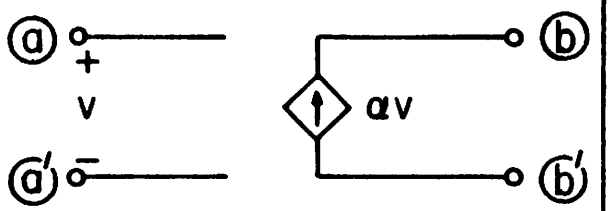
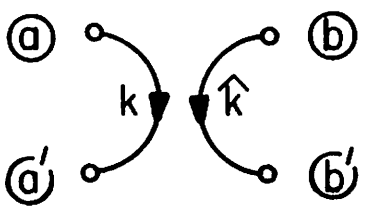
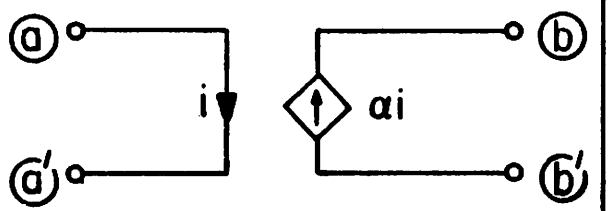
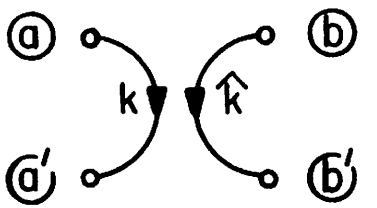
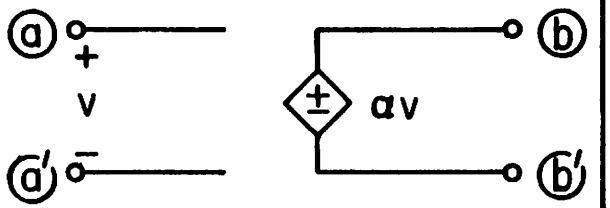
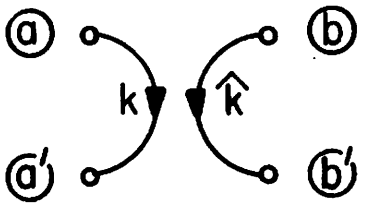
TYPE OF CONTROLLED SOURCE	SYMBOL	ASSOCIATED GRAPH
CURRENT-CONTROLLED VOLTAGE SOURCE (CCVS)		
VOLTAGE-CONTROLLED CURRENT SOURCE (VCCS)		
CURRENT-CONTROLLED CURRENT SOURCE (CCCS)		
VOLTAGE-CONTROLLED VOLTAGE SOURCE (VCVS)		

Table I

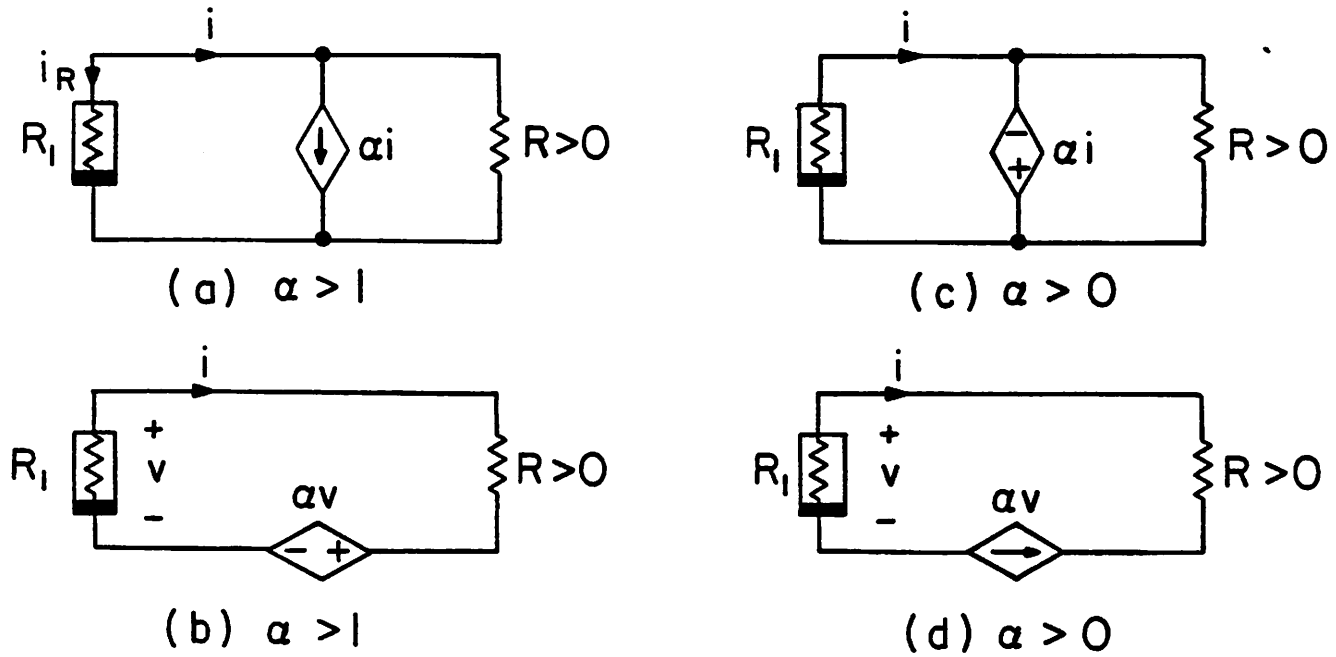


Fig. 1

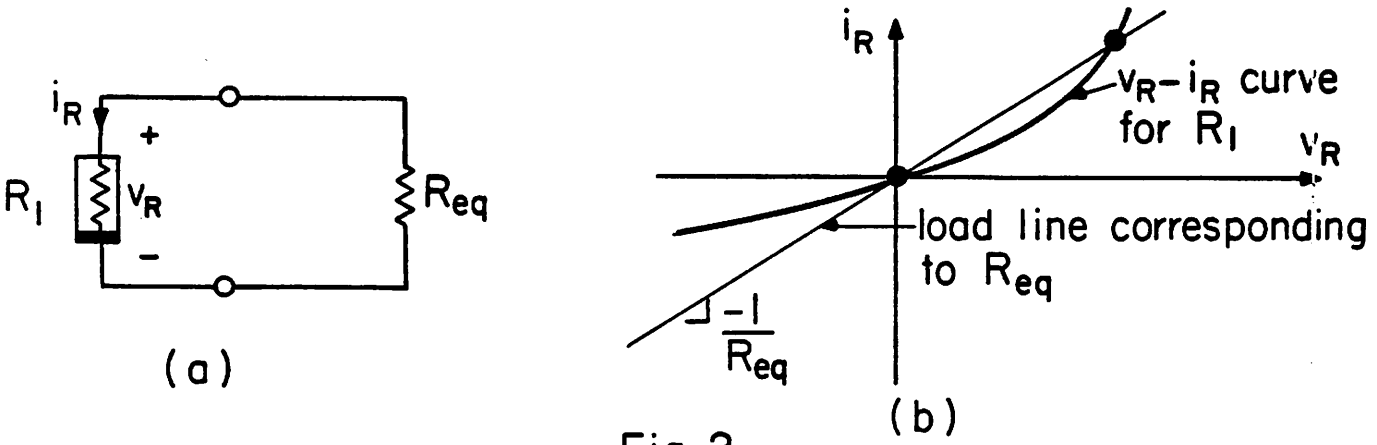


Fig. 2

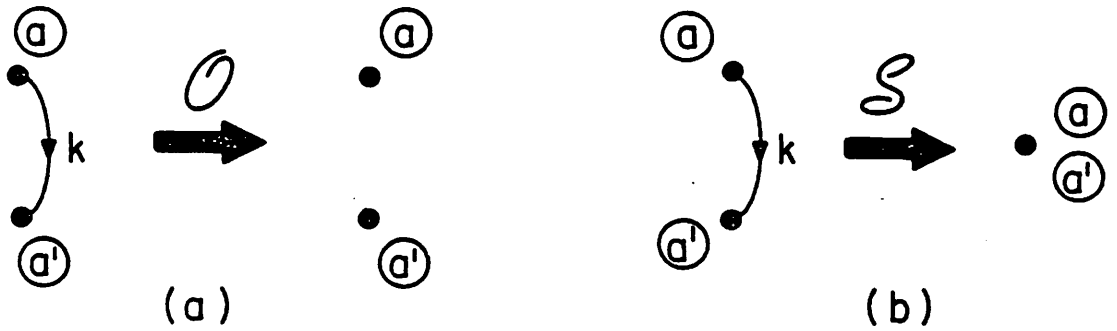


Fig. 3

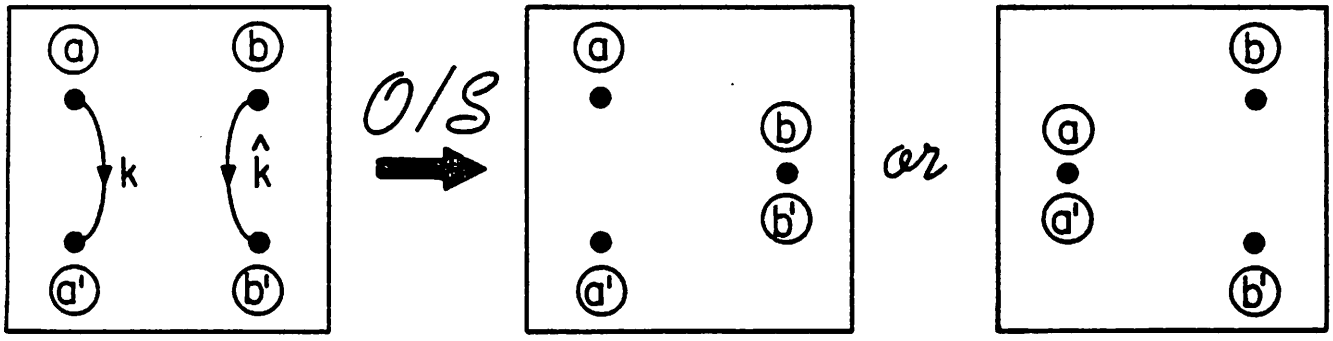


Fig. 4

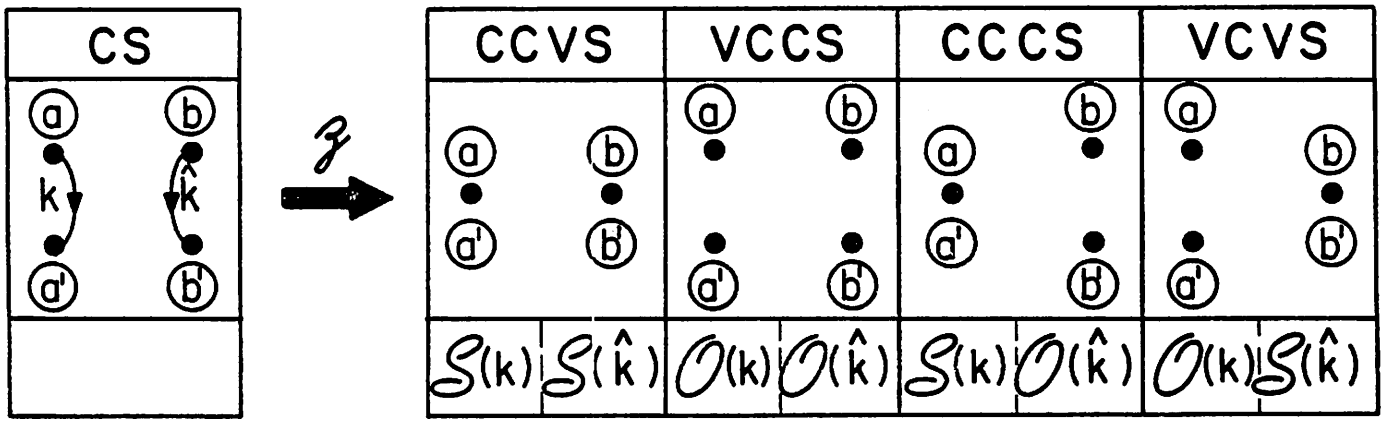


Fig. 5

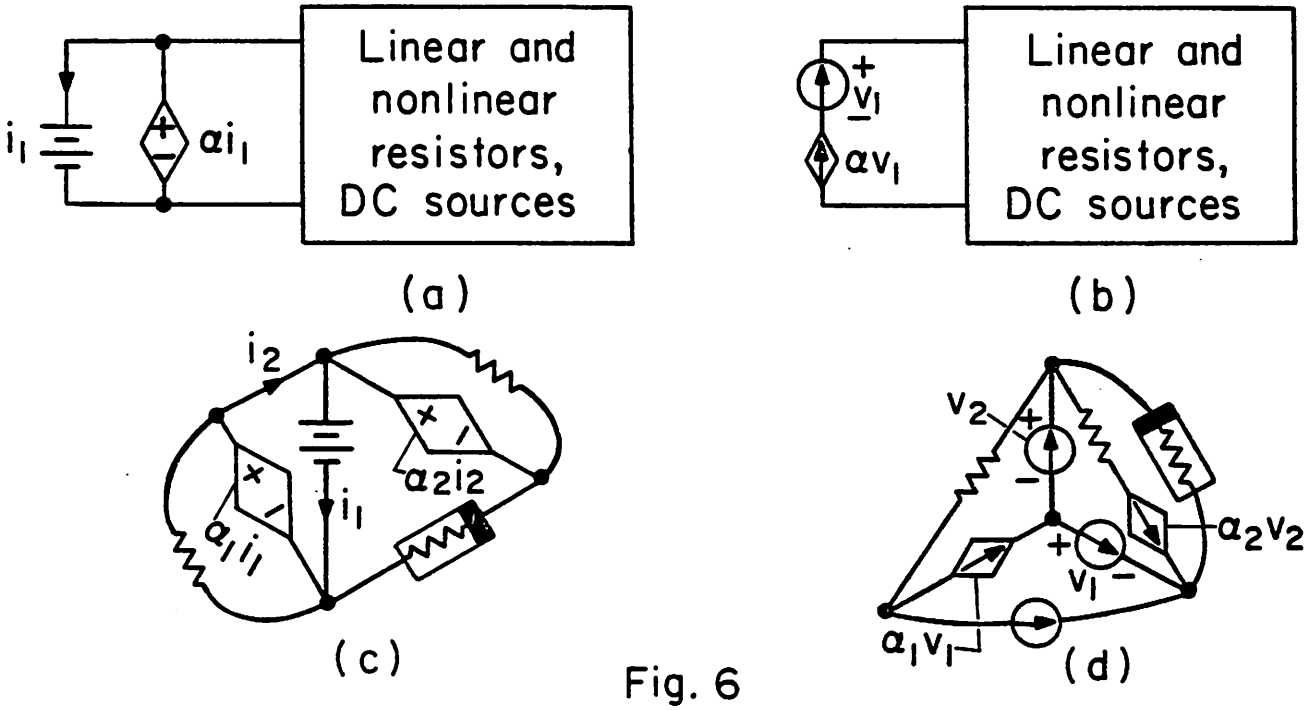


Fig. 6

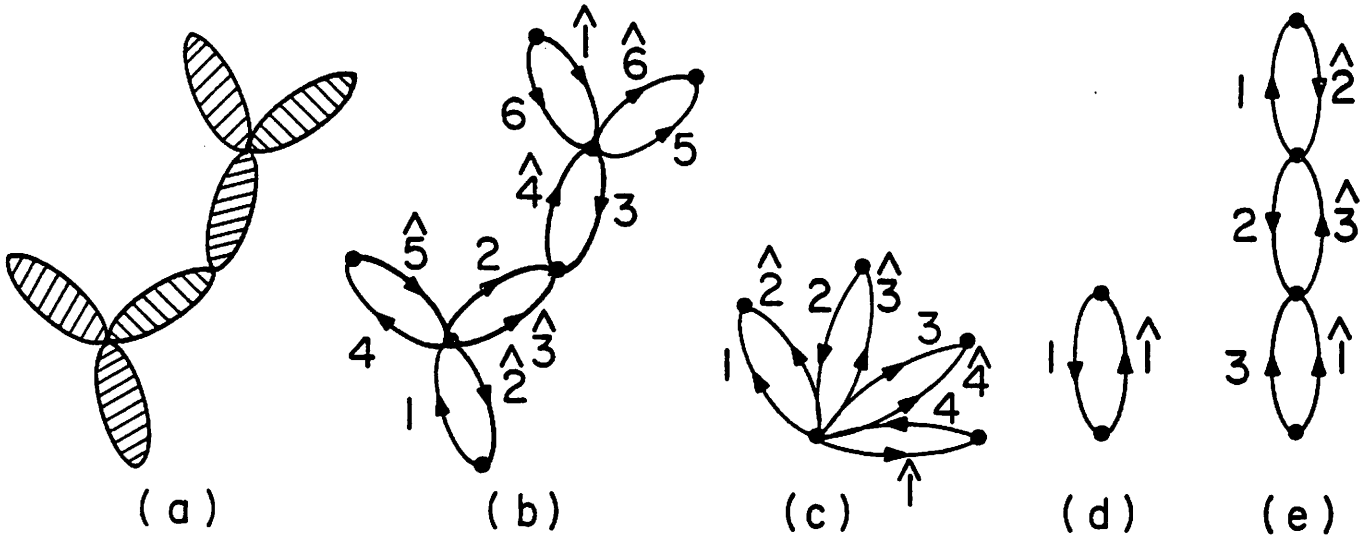


Fig. 7

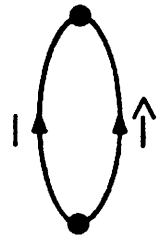


Fig. 8

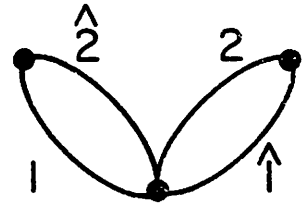


Fig. 10

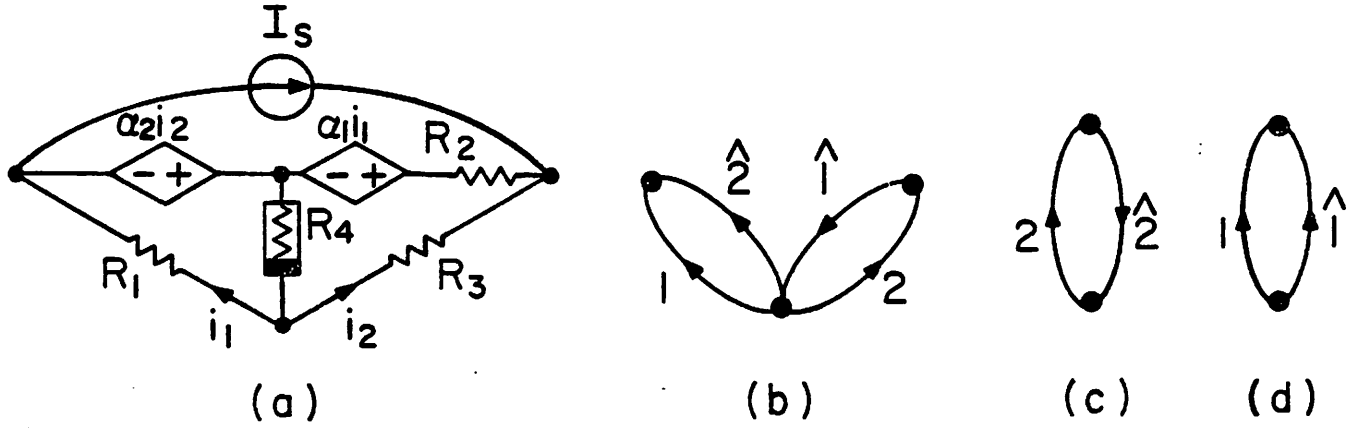


Fig. 11

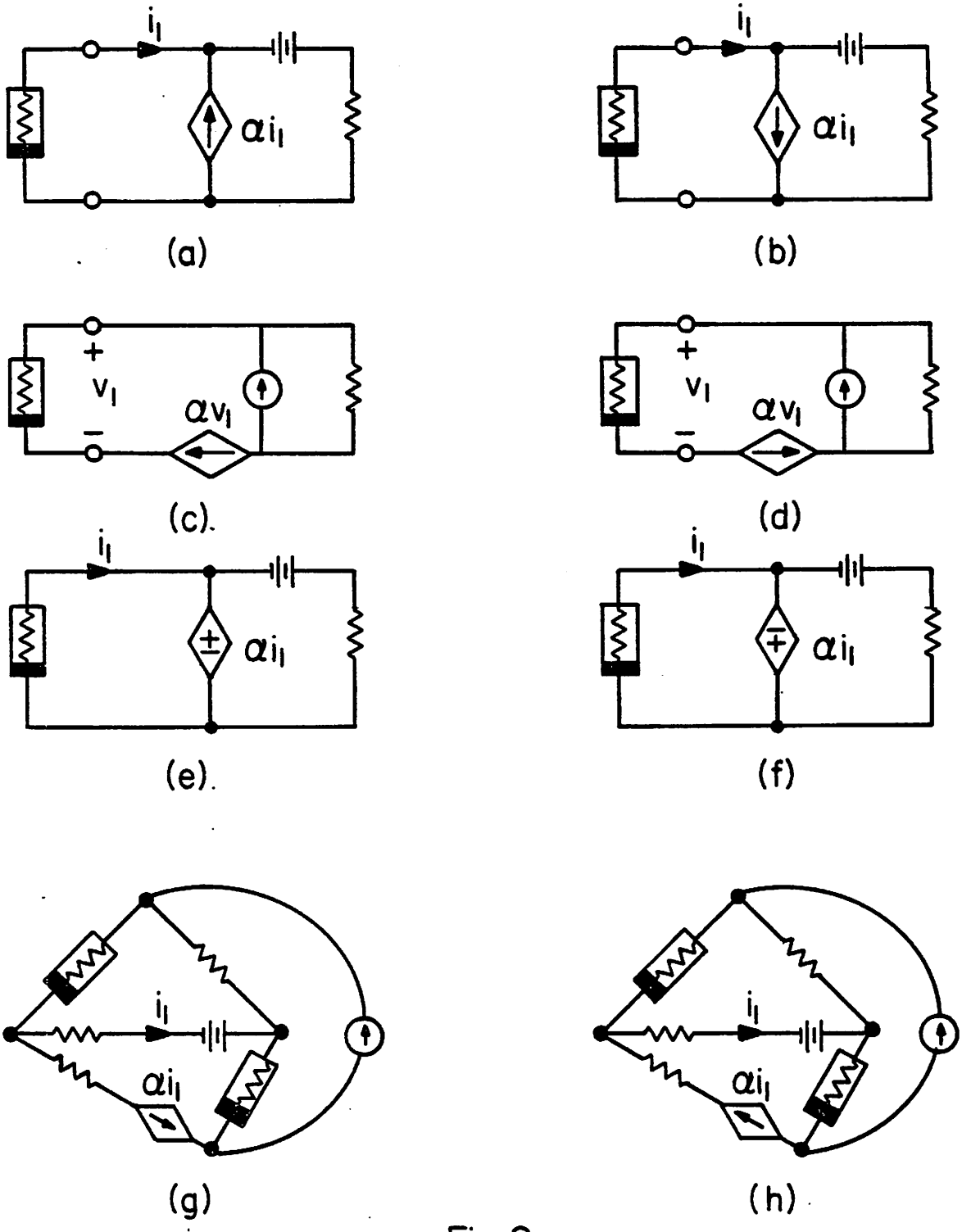

i_1
αi_1
(a)
i_1
αi_1
(b)
+
v_1
−
αv_1
(c)
+
v_1
−
αv_1
(d)
i_1
αi_1
(e)
i_1
αi_1
(f)
i_1
αi_1
(g)
i_1
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Fig. 9

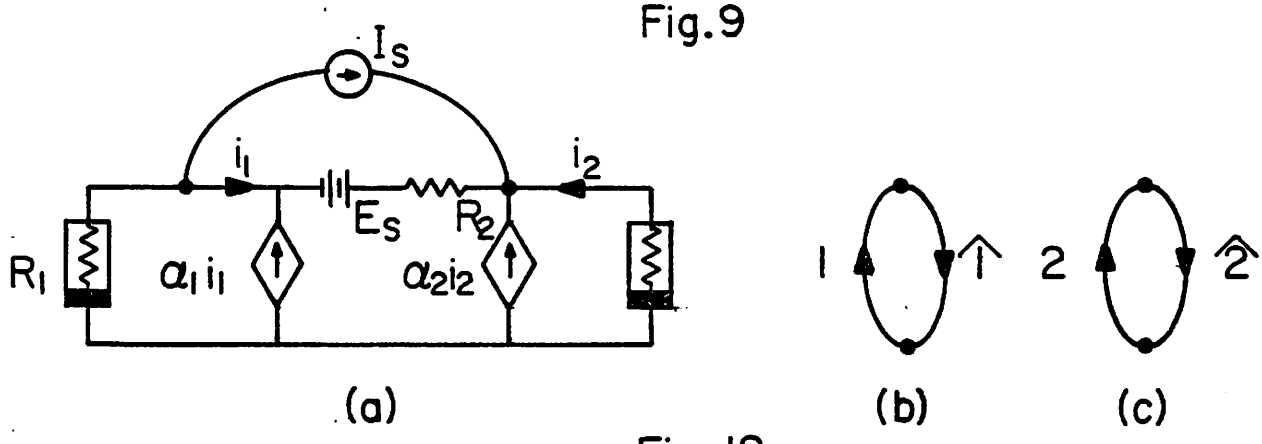
I_s
i_1
i_2
E_s
R_2
R_1
$\alpha_1 i_1$
$\alpha_2 i_2$
(a)
1
$\hat{1}$
(b)
2
$\hat{2}$
(c)

Fig. 12

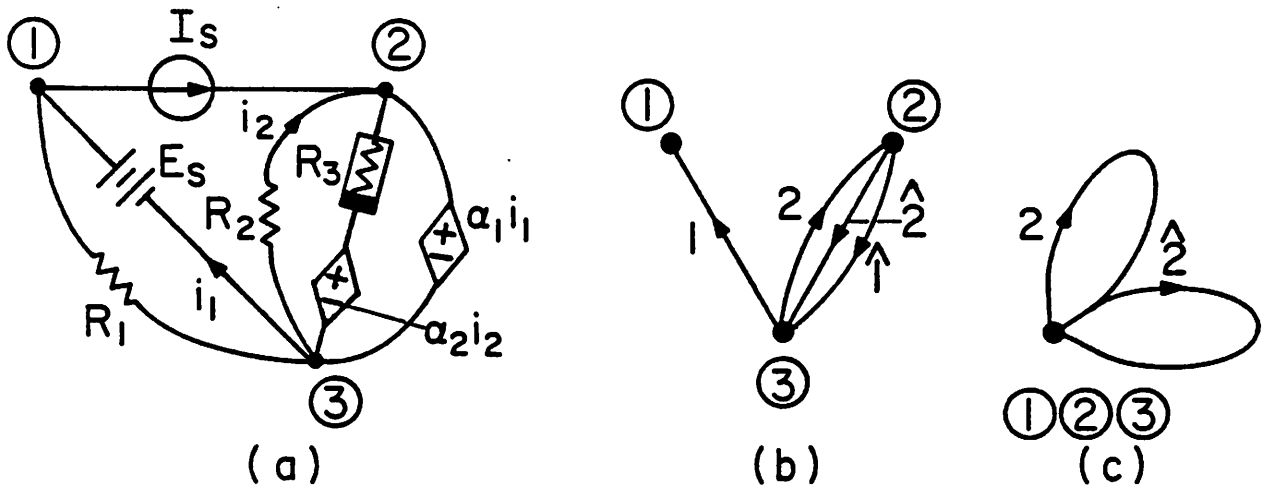

Fig. 13

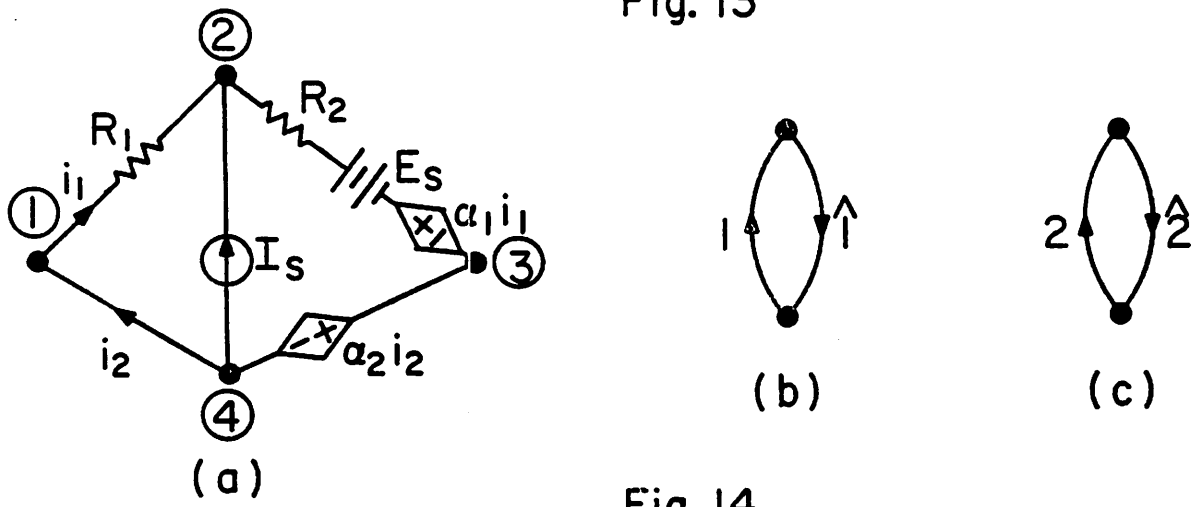

Fig. 14

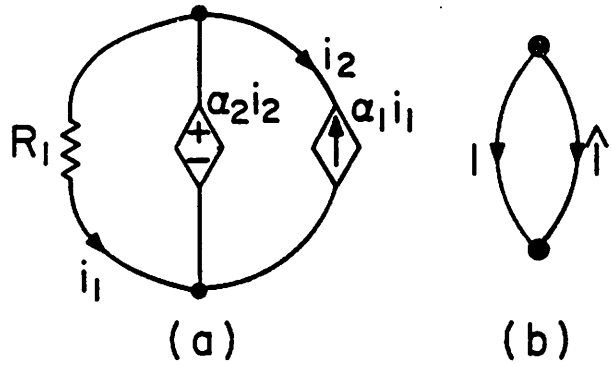

Fig. 15

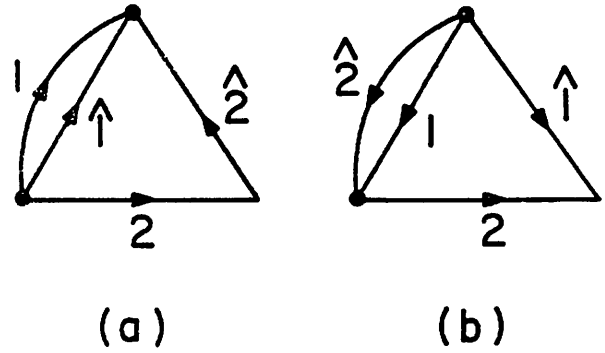

Fig. 16

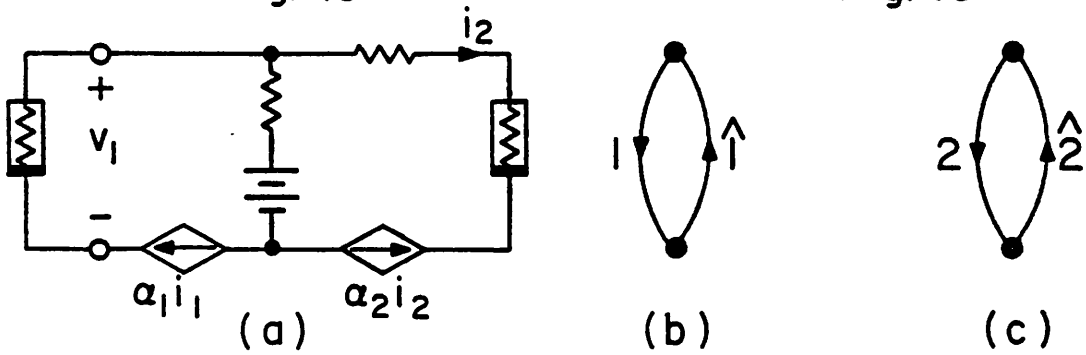

Fig. 17

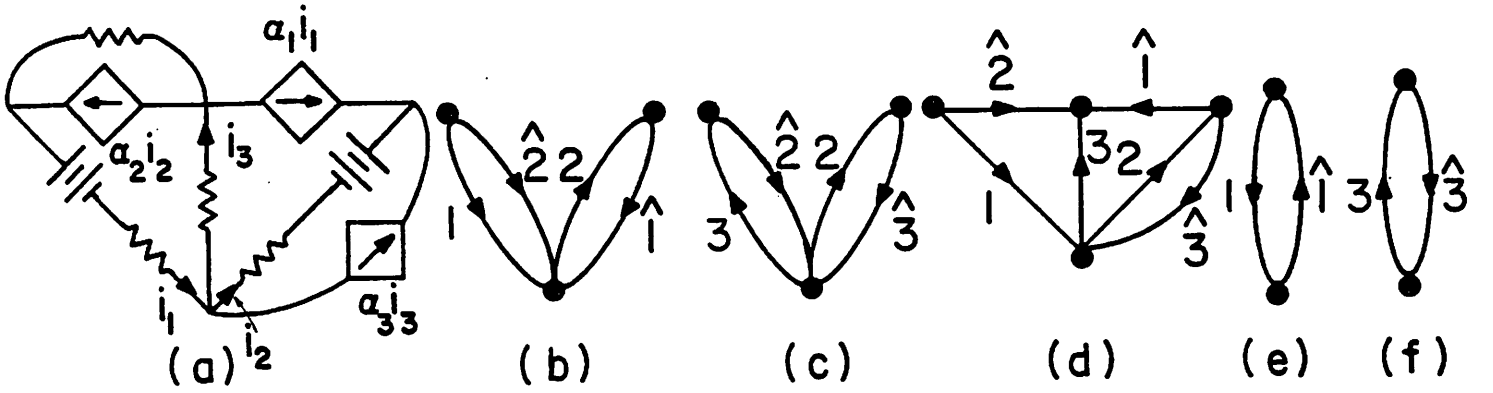

Fig. 18

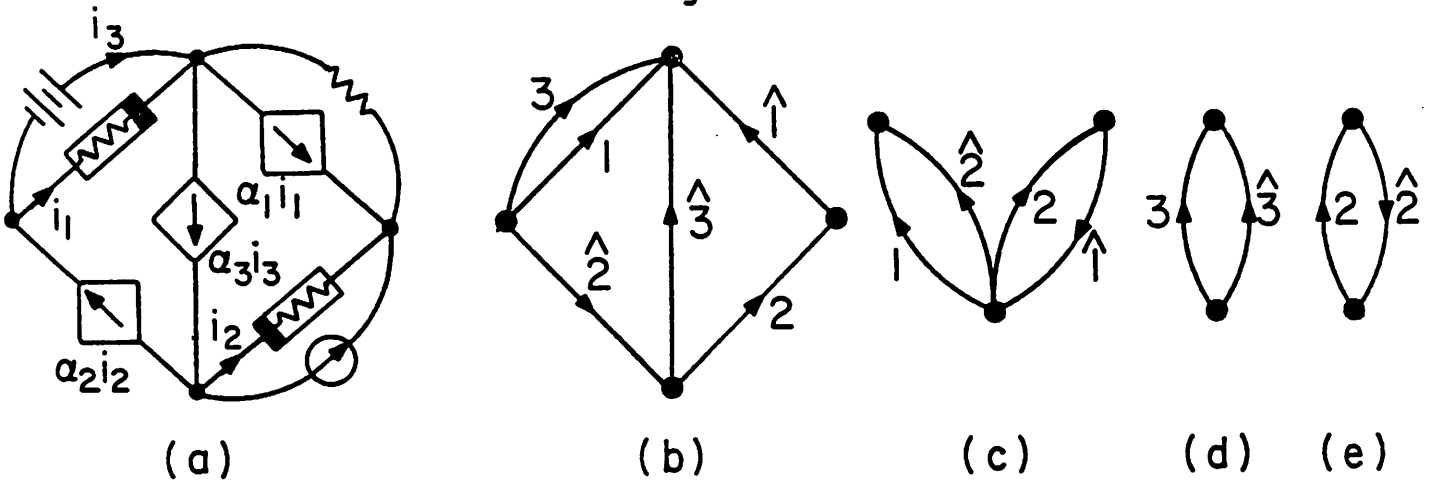

Fig. 19

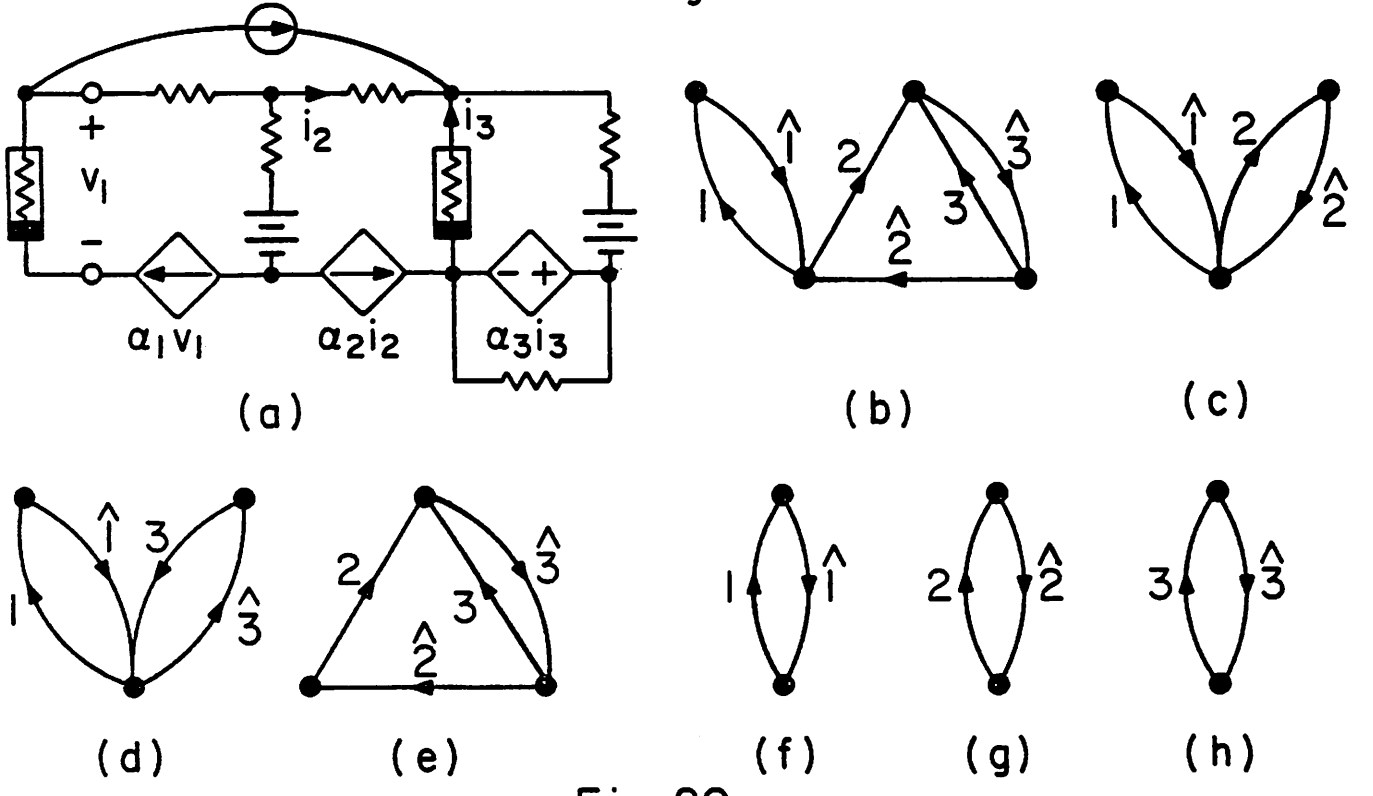

Fig. 20

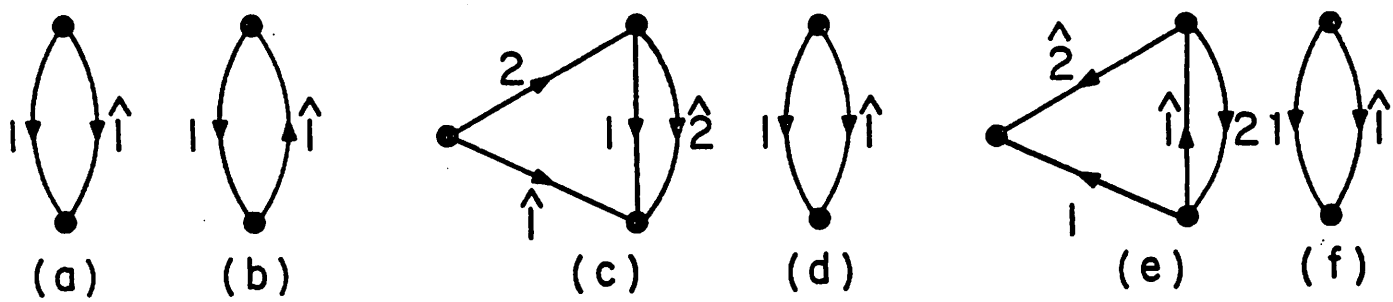

Fig. 21

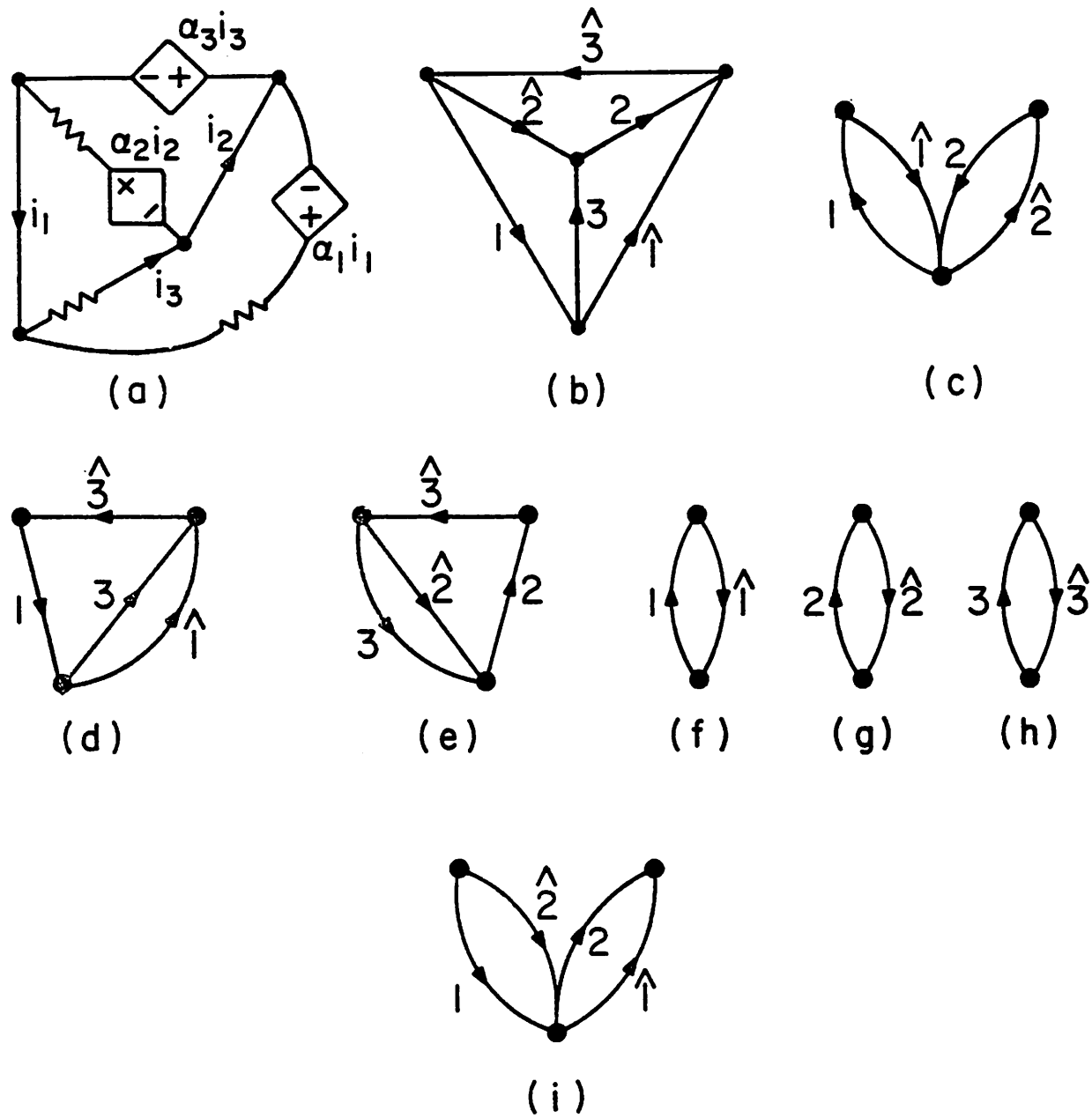

Fig. 22

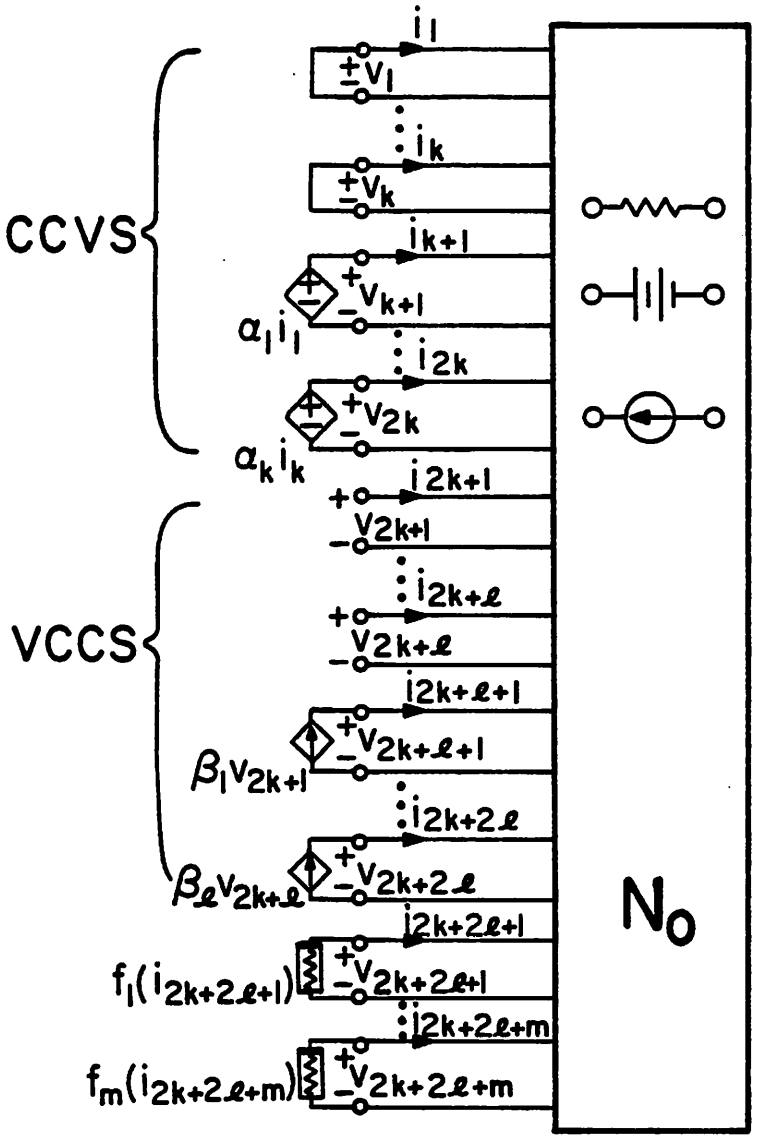

Fig. 23

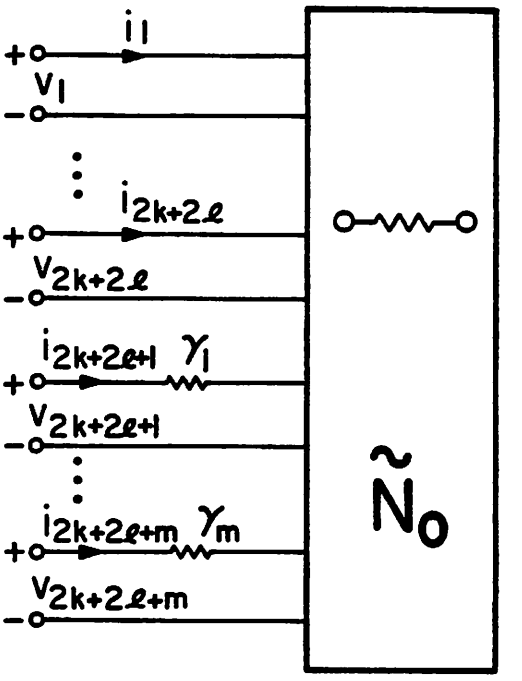

Fig. 24

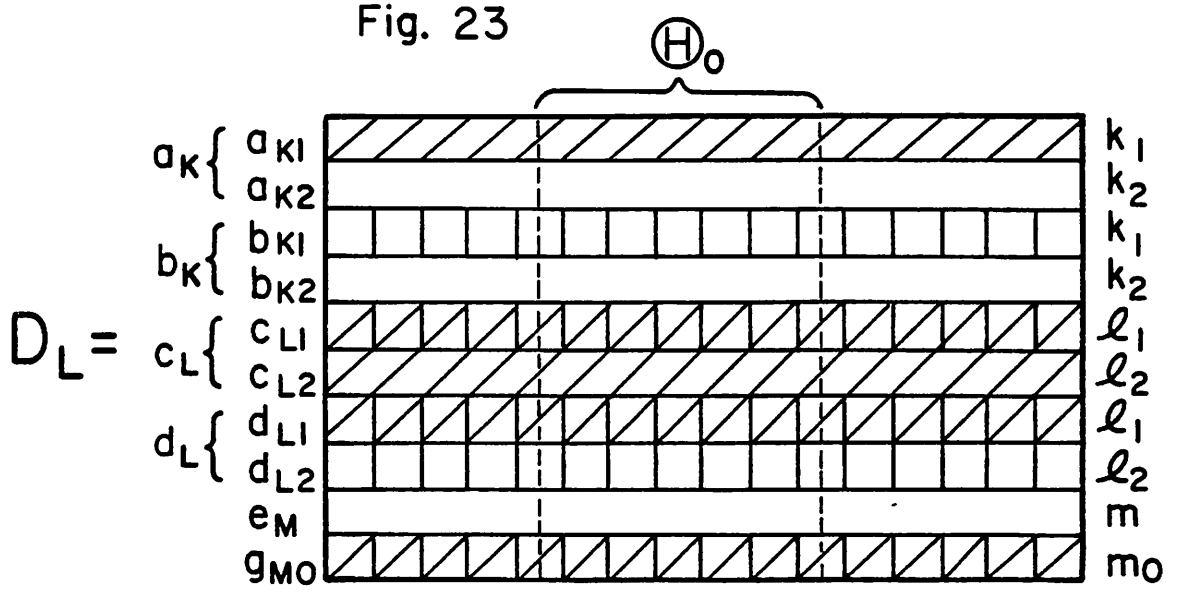

Fig. 25

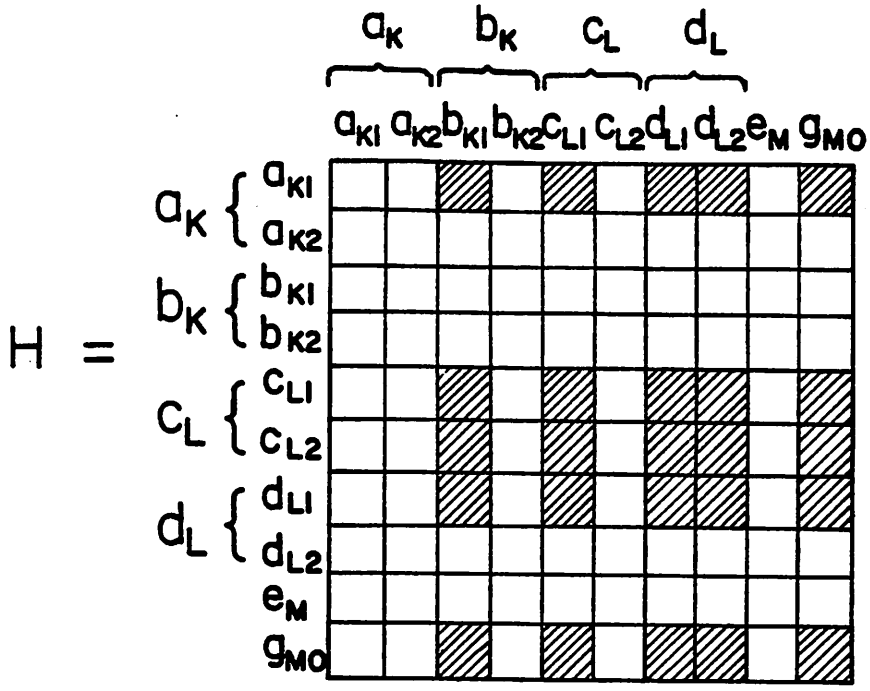

Fig. 26

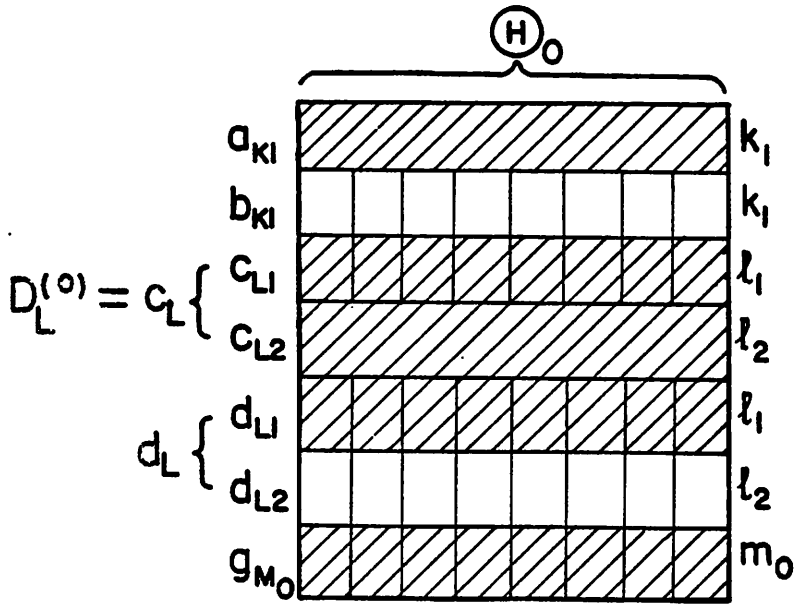

Fig.27

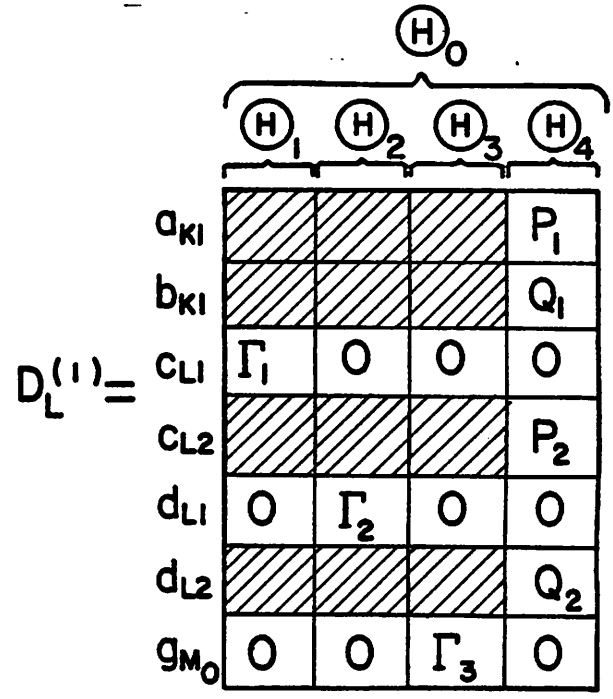

Fig.28

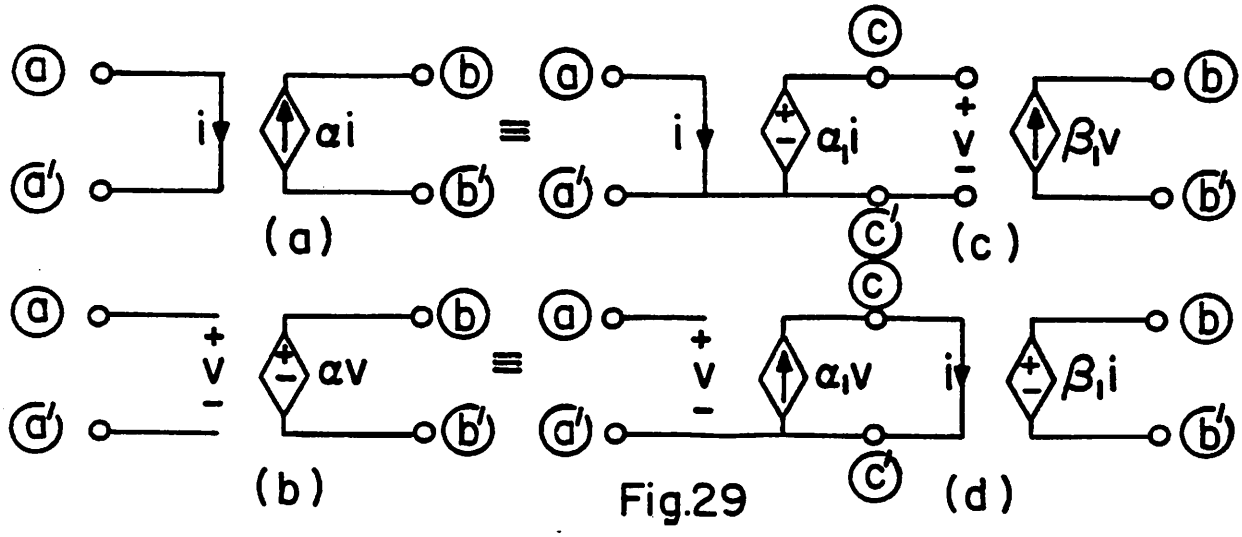

Fig.29

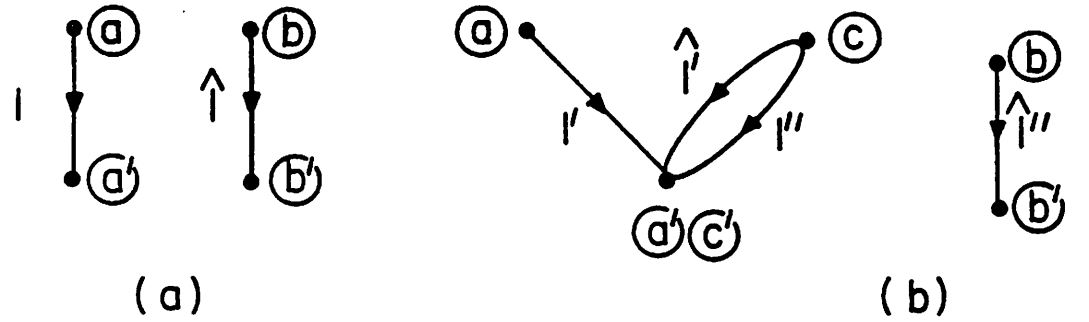

Fig. 30

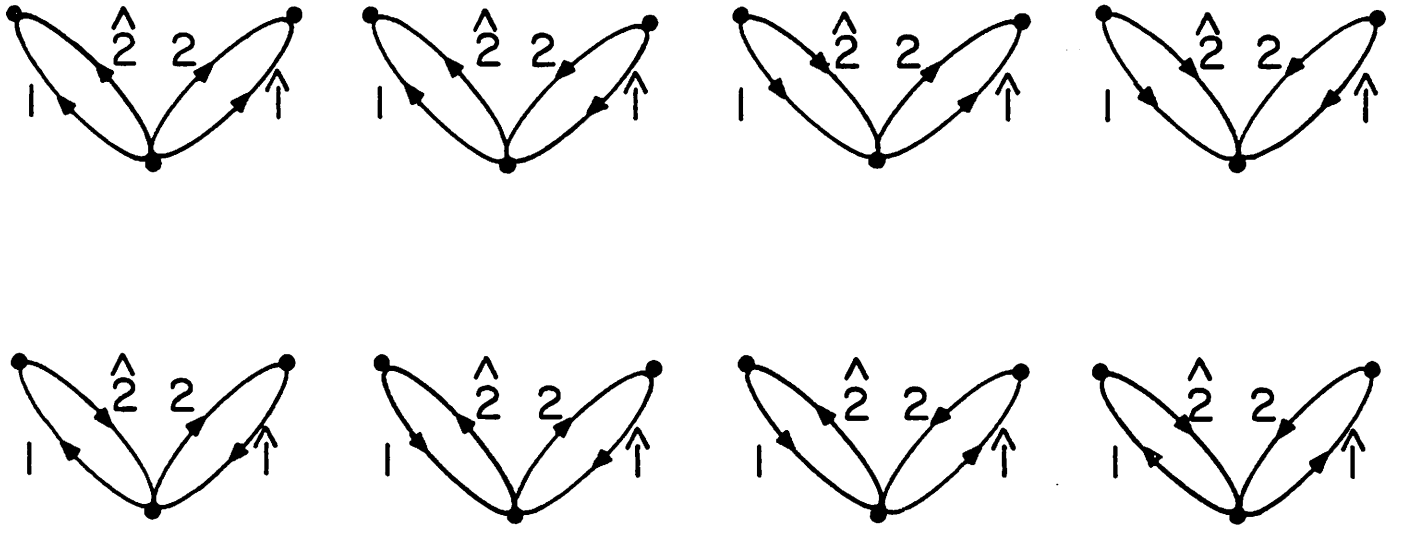

Fig. A.1

$$
\tilde{Z} = \begin{array}{c|c|cccccc}
 & & a_{K1} & a_{K2} & b_{K1} & b_{K2} & c_{L1} & c_{L2} & d_{L1} & d_{L2} & e_M \\
\hline
a_K & a_{K1} & Z_{aa} & & Z_{aa} & & Z_{ac} & & Z_{ad} & & Z_{ae} \\
 & a_{K2} & & & & & & & & & \\
b_K & b_{K1} & Z_{ba} & & Z_{bb} & & Z_{bc} & & Z_{bd} & & Z_{be} \\
 & b_{K2} & & & & & & & & & \\
c_L & c_{L1} & Z_{ca} & & Z_{cb} & & Z_{cc} & & Z_{cd} & & Z_{ce} \\
 & c_{L2} & & & & & & & & & \\
d_L & d_{L1} & Z_{da} & & Z_{db} & & Z_{dc} & & Z_{dd} & & Z_{de} \\
 & d_{L2} & & & & & & & & & \\
 & e_M & Z_{ea} & & Z_{eb} & & Z_{ec} & & Z_{ed} & & Z_{ee} + D
\end{array}
$$

Fig. A.2

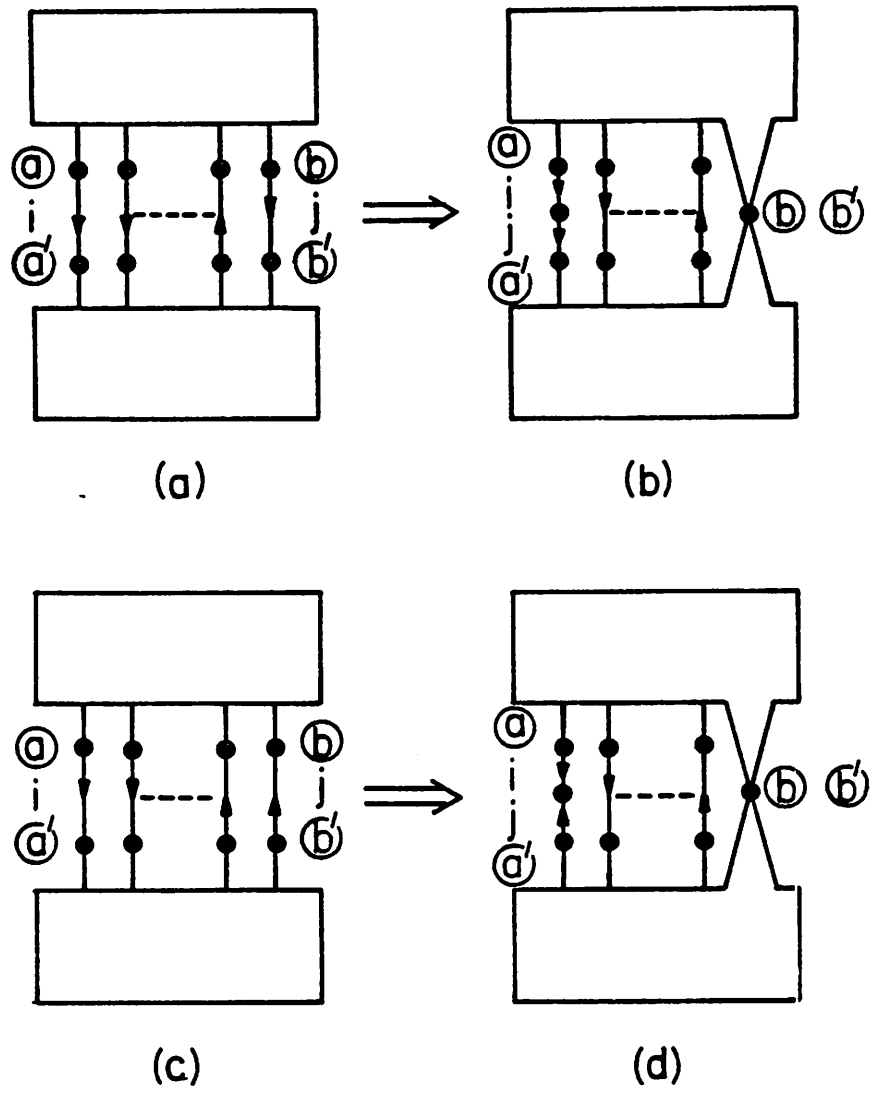

Fig. A.3

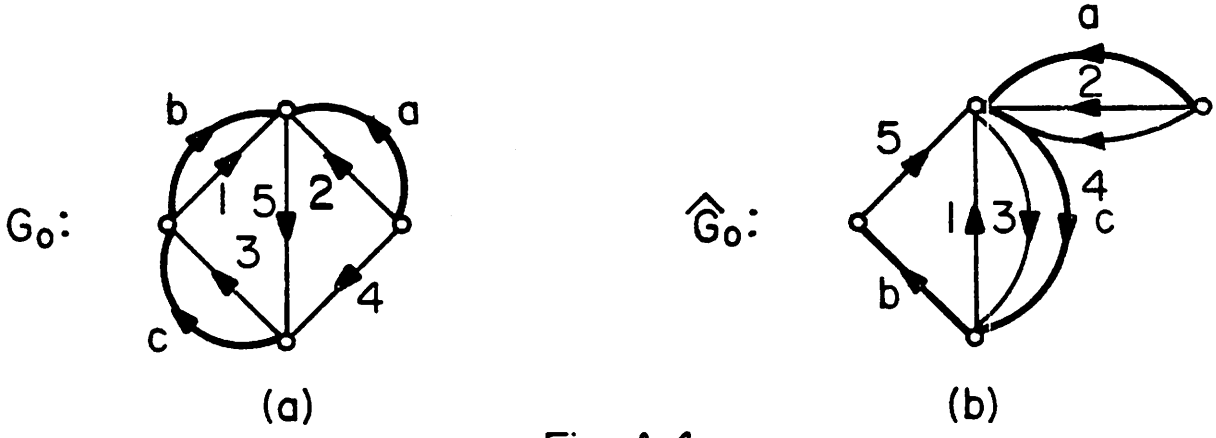

Fig. A.4

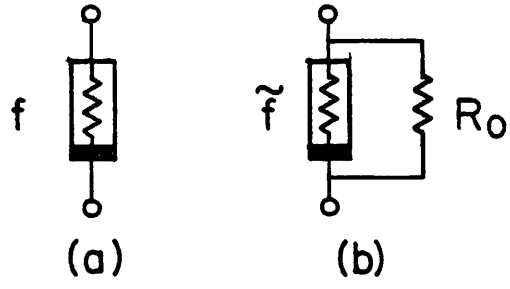

Fig. A.5

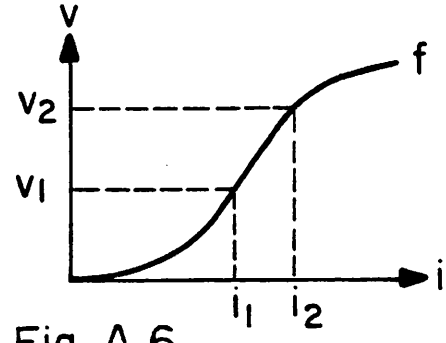

Fig. A.6