RATIO INDEPENDENT CYCLIC A/D AND D/A CONVERSION USING A RECIRCULATING REFERENCE APPROACH

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Abstract

In this letter, a new method is described which uses switched capacitor techniques to implement cyclic A/D and D/A converters. By periodically modifying the reference voltage to compensate for the non-ideal signal transfer loop gain, it is possible in principle to build analog-digital and digital-analog converters whose linearity is independent of component ratios and which occupy only a small die area. These converters require two moderate-gain MOS operational amplifiers, one comparator and a few capacitors.

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Introduction

Previously described approaches to digital-analog and successive-approximation analog-digital conversion have relied on circuit techniques which require the matching of on-chip precision passive components to an accuracy comparable with the integral nonlinearity required in the converter. R-2R ladders, resistor strings, and capacitor array DACs fall into this category. The realization of the required matching has typically required laser trimming or other forms of trimming in order to achieve nonlinearity smaller than .2%. Recently, a new technique has been described which allows the automatic calibration of a capacitor array-based analog-digital converter. While very promising, this approach requires considerable complexity in implementation[1].

This letter describes a new approach to the implementation of high-speed analog-digital and digital-analog conversion which achieves an absolute linearity which is independent of the matching accuracy of the passive components used to implement the converter. This is achieved by the use of a modified form of the algorithmic converter in which the reference voltage is circulated around the loop as well as the signal, thereby canceling the gain error in the loop, in contrast to previously described approaches[2]. Experimental fully differential CMOS prototype of this approach is currently being fabricated. Experimental results from this prototype will be reported in a later publication.

1. Cyclic A/D Conversion

The technique described in this letter is a modification of the "cyclic" or "algorithmic" conversion technique[3]. The technique described here is an approach to making an MOS implementation of such a converter which displays a differential and integral linearity that is independent of the capacitor ratios within the converter. Traditional cyclic or algorithmic conversion involves comparison , reference subtraction if applicable ,and multiplication of the result by

a factor of two. The first step in the process is the decision as to whether the signal is in the upper or lower half of the full range. If the signal is in the upper range, the reference is subtracted from the signal and the difference is doubled. The most significant bit of the digital output is set to one. If in the lower half, the input signal is simply doubled and the most significant bit is set to zero. In the next cycle, the remainder from the previous cycle is used as the input and the process is repeated. Following the procedure, the signal can be encoded into a 12 bit digital output in 12 iterations.

In the D/A operation the least significant bit is decoded first. The reference voltage is added depending on the digital input code and the sum is divide by two each time. At the end of 12 cycles, the analog output is derived from the digital code. The principal sources of error in these converters is offsets in the loop and a loop gain which is not precisely two or one half. If the loop gain is not precisely two or one half, both integral and differential nonlinearity is introduced into the converter transfer characteristic.

The switched-capacitor implementation of the cyclic conversion requires an amplifier with gain of two, a sample and hold circuit and a comparator. The basic structure of the converter is shown in Fig. 1. An operation of sampling and transferring the signal twice will result in multiplication of the signal by a factor of C1/C2. If C1 and C2 are equal, this will give a gain of two. However, deviations from equal values in C1 and C2 will result in conversion errors. Taking into account of the capacitor ratio inaccuracy and other high order errors existing in the loop, the loop transfer equation is :

$$T(x) = 2x + \sum_{i=0}^{N} E_i x^i$$

where

E_0: dc offset

E_1: Loop gain error due to capacitor mismatch etc.

E_2 , E_3: Other high order distortions

These deviations result in both integral and differential nonlinearity.

2. Reference Refresh Principle

In order to remove the gain errors in the loop, it is necessary to use a switching sequence which removes the dependence of the effective gain factor on capacitor ratios. It can be recognized that an equivalent result to a precise gain of two would be obtained if the reference was modified on each cycle by a factor which was the same as the factor by which the loop gain was different from two. In other words, the gain error E_1 can algorithmatically corrected by modifying the reference voltage (V_{hfs}) at each cycle based on the loop error. The reference voltage of the circuit is not fixed in the processing but is updated once each cycle. The effective reference voltage(V_{hfs}^{k}) at the k-th cycle will be $V_{hfs}(1+\frac{E_1}{2})^k$. The following example explicitly shows the correction effect for an 3 bit A/D conversion .

$$A\left\{A[\,A(V_{in}-B_0V_{hfs}^{\hat{0}})-B_1V_{hfs}^{\hat{1}}]-B_2V_{hfs}^{\hat{2}}\right\}$$

$$= A^3[\,V_{in}-B_0V_{hfs}^{\hat{0}}-B_1\frac{V_{hfs}^{\hat{1}}}{A}-B_2\frac{V_{hfs}^{\hat{2}}}{A^2}\,]$$

$$= A^3\left[V_{in}-B_0V_{hfs}-B_1\frac{V_{hfs}}{2}-B_2\frac{V_{hfs}}{2^2}\right]$$

where

$$A = 2\,(1+\frac{E_1}{2})$$

Through the use of the reference refresh operation, A/D and D/A linearity is made independent of the mismatch of capacitors. The great advantage of this technique is that as long as the reference and the signal are passed through the same loop, the errors related to charge injection and finite operational amplifier

gain are automatically canceled, as long as they contribute only gain errors. This fact greatly simplifies the implementation of high-resolution converters.

3. Reference Refresh Implementation

The reference recirculation technique can be implemented so as to give both ratio independent analog-to-digital conversion and digital-to-analog conversion. The signal flow through the circuit shown as Fig. 1 is briefly described below. The signal is first sampled on C_1 and transferred to C_2. The reference is next subtracted from the signal by changing one end of C_3 from ground to $-V_{hfs}$. If the signal is smaller than the reference, simply reconnecting the C_3 back to ground will make the signal return to its initial value. The new outcome is doubled by sampling the voltage on C_3 and dumping the charge twice on C_4 without discharging C_4 at the second time. At this moment, the reference is also sampled on C_1 and transferred to C_2. When the signal is transferred back to C_2, the reference is passed through C_3 and C_4 without being doubled. When the reference is needed at the next cycle to determine the signal level, the newly changed reference is used. This reference is at the output of the second operational amplifier will experience the same gain error as the signal did. This whole process is repeated 12 times to derive a 12 bit digital output.

For digital to analog conversion, the least significant bit is processed first. If the bit is one, the reference is added to the temporary result and the temporary result is divided by two. At next frame, the reference is refreshed by passing through the loop. Unlike the A/D, the loop gain of the D/A is one half instead of two. In order to achieve the unity gain for the reference voltage, this time the reference voltage is integrated twice. For the same reason as the A/D conversion, reference refreshing must be interleaved during the development of the analog output. By implementing the above correction method, the D/A can also be ratio independent. A comparison of the D/A with and without the reference

refresh technique is shown in Fig. 2.

4. Simulation results

4.1. Gain Error

Simulation of the reference recirculation technique have shown that indeed it removes the sensitivity of the converter linearity to capacitor ratio mismatch and finite operational amplifier gain. Figs. 3a and 3b show the transfer curve of a 4-bit algorithmic A/D converter with a capacitor mismatch error of 10% with and without reference refreshing.

4.2. Offset Errors

The presence of dc offset voltages in the loop of a magnitude comparable with an lsb results in both integral and differential nonlinearity in the converter transfer characteristic. Since for a 13 bit converter with a reference voltage of 3 volts one lsb is less than 1 mV, the removal of offsets from the loop is essential.

The principal contributions to offset voltage are the operational amplifier offset voltage and the offsets resulting from mismatches in charge injection from the MOS switches. Fig. 4 shows the transfer curve of a 4 bit A/D with dc offset in the operational amplifier. The offset error distorts not only the signal itself but also the refreshed reference.

The proposed experimental implementation of this converter utilizes fully differential operational amplifiers with multi-phase active offset compensation[4]. This permits offset voltages in the loop to be nulled to an arbitrary degree of precision, in this case chosen to be approximately 0.1mV assuming a 10% mismatch in the gate capacitance of a minimum sized switch pair.

5. CONCLUSIONS

A new approach to algorithmic A/D and D/A conversion has been described which combines the techniques of switched capacitor cyclic conversion and reference voltage refreshing. The performance of the converter is capacitor ratio independent and the analog portion of the coverter can be realized by two operational amplifiers, one comparator, and a few small capacitors in the range of a few pico farads. Because of the ratio independent aspect, very small component values can be used and as a result the die area required for this circuitry can be scaled as technological feature sizes are reduced.

References

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[3] McCharles, R. H., "Charge Circuits for Analog LSI", IEEE Transactions on Circuits and Systems, Vol CAS-25, pp490-497, July 1978.

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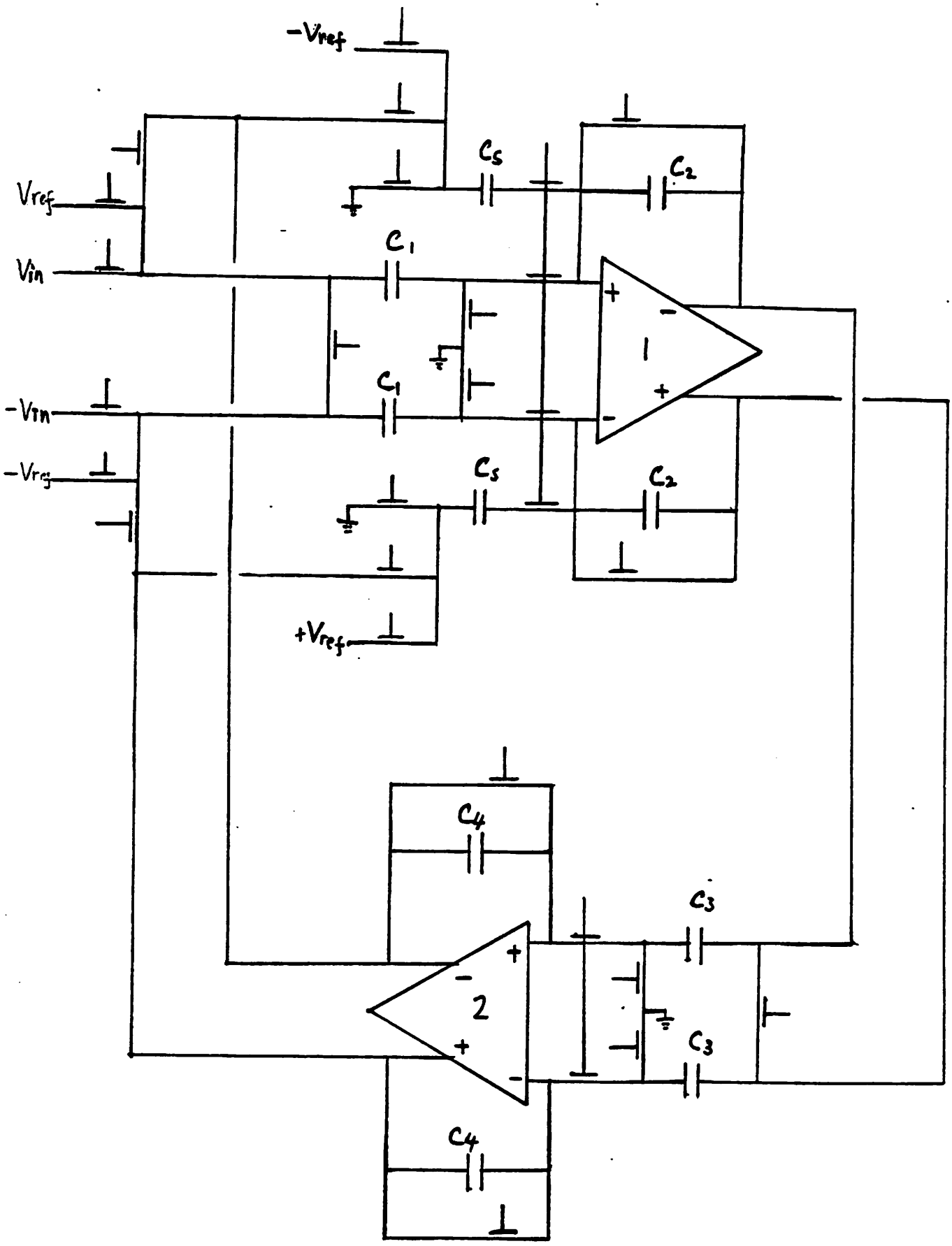
Fig. 1 Fully differential switched capacitor implenmentation
of the converter

Fig. 2 D/A with 10% gain error,
(a) No reference refreshing
integral nonlinearity = 1/4 LSB, diffferential nonlinearity = 1/2 LSB
(b) With reference refreshing
integral nonlinearity = 0 LSB, diffferential nonlinearity = 0 LSB

Fig. 3 4 bit A/D with 20% gain error,
(a) No reference refreshing,
integral nonlinearity = 1 LSB, differential nonlinearity = 7/4 LSB
(b) With reference refreshing
integral nonlinearity = 0 LSB, diffferential nonlinearity = 0 LSB

Fig. 4 4 bit A/D with 1.06 LSB operational amplified offset
integral nonlinearity = 1/2 LSB
diffferential nonlinearity = 1 LSB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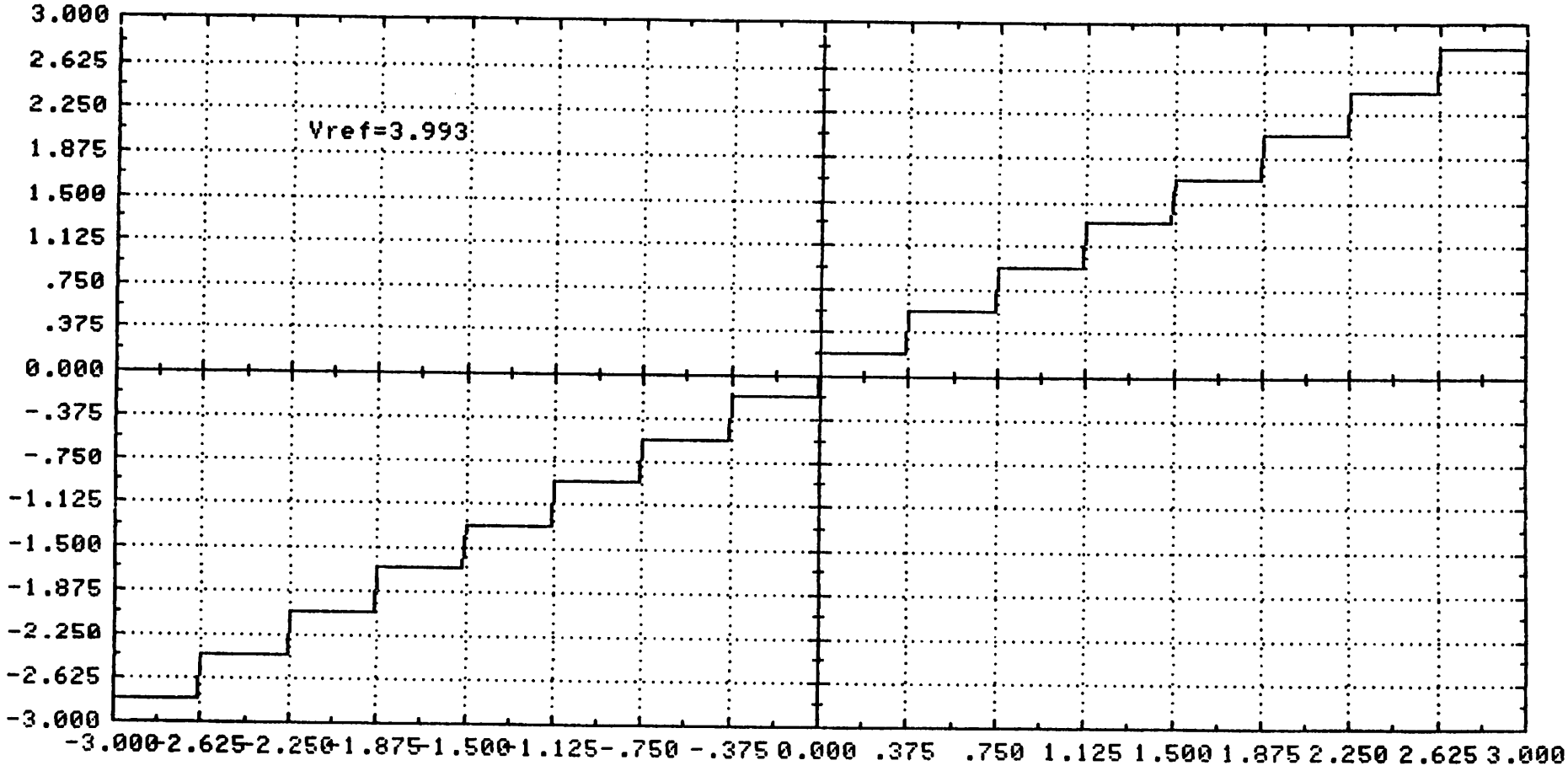
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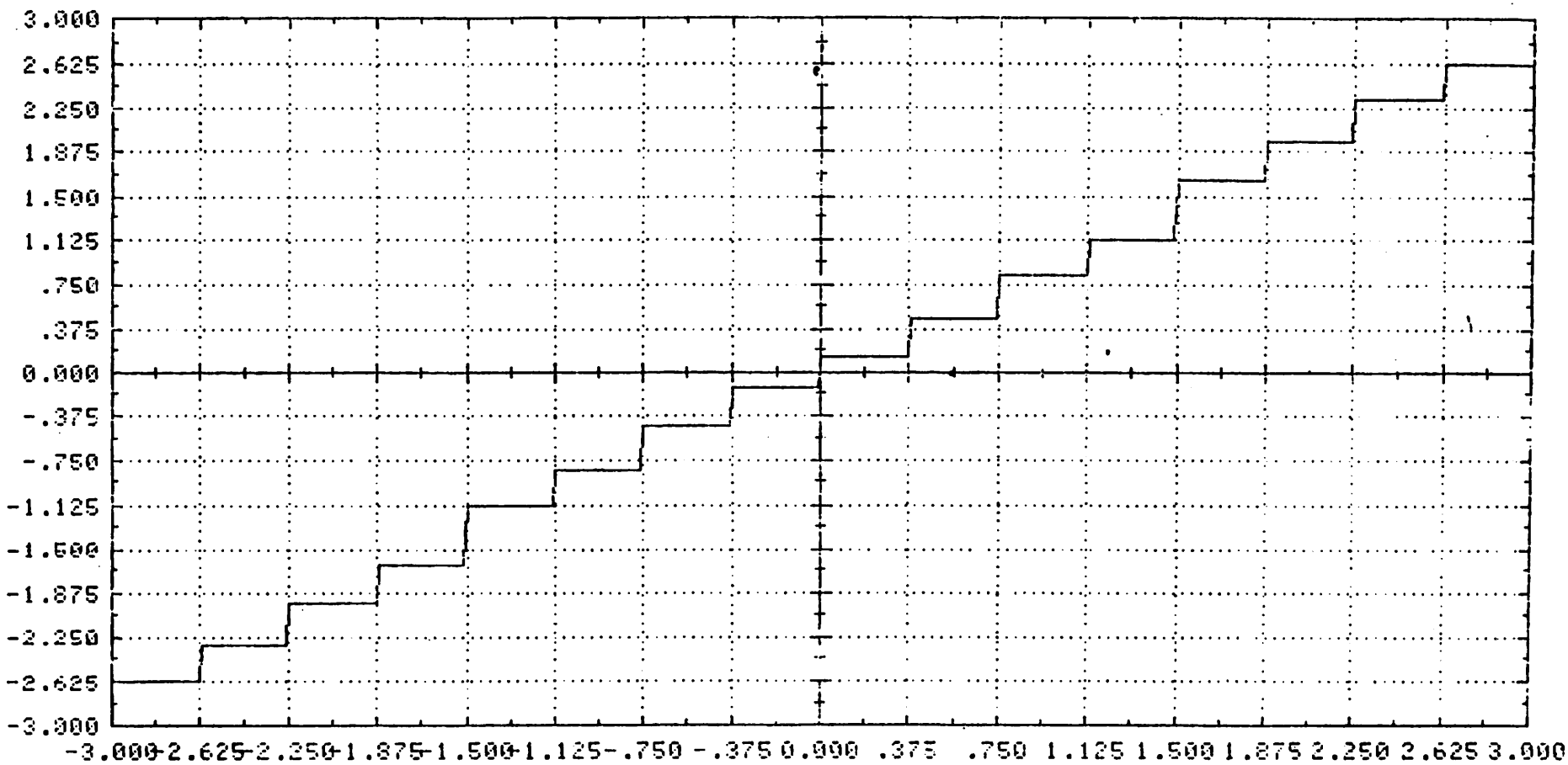
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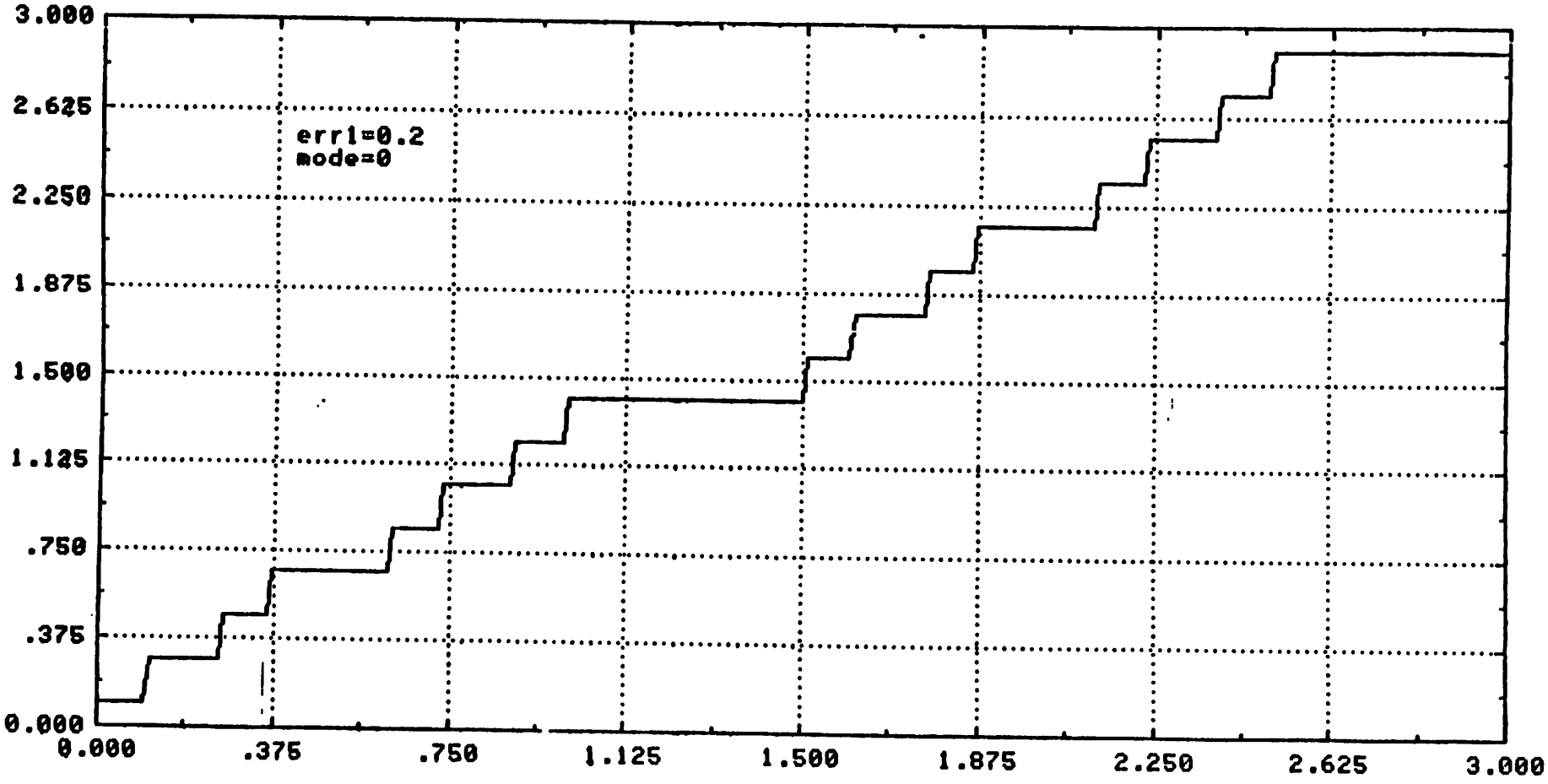
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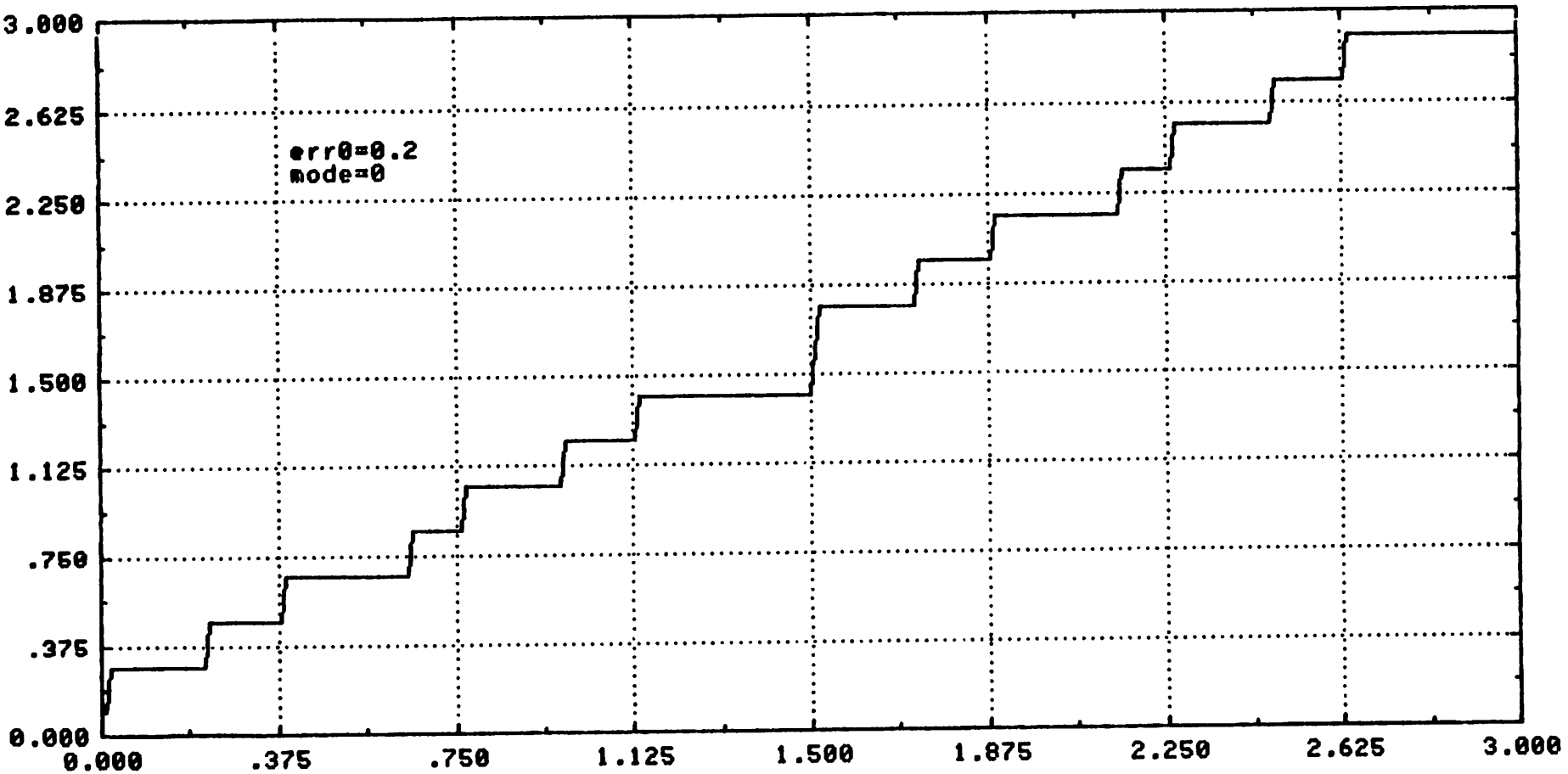
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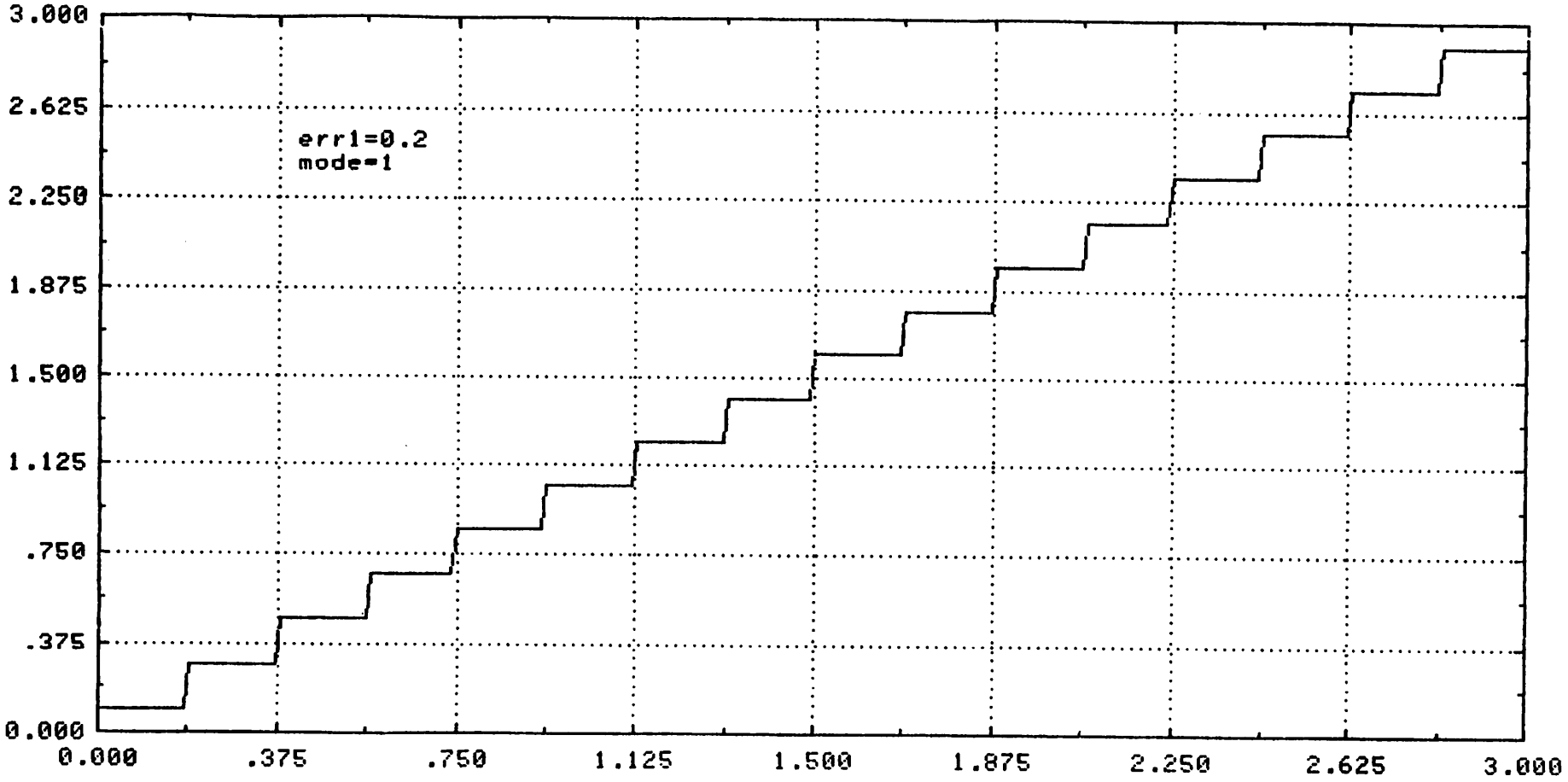
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