CIRCUIT AND TECHNOLOGY CONSIDERATIONS FOR HIGH FREQUENCY SWITCHED-CAPACITOR FILTERS

by

Ronald T. Kaneshiro

Memorandum No. UCB/ERL M83/42

18 July 1983

Cover

Rinaldo Castello
386

CIRCUIT AND TECHNOLOGY CONSIDERATIONS FOR HIGH FREQUENCY SWITCHED-CAPACITOR FILTERS

by

Ronald T. Kaneshiro

Memorandum No. UCB/ERL M83/42

18 July 1983

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Circuit and Technology Considerations

For High Frequency

Switched-Capacitor Filters

Ronald Takeshi Kaneshiro

Ph. D. EECS

Paul R. Gray
Chairman of Committee

ABSTRACT

Since its inception in the late 1970's, the switched-capacitor filtering technique has been very widely applied in the telecommunications field. If this technique can be extended into a much higher frequency range, its applicability can be broadened into areas that are currently dominated by non-monolithic design methods.

Past attempts to design practical and reproducible high frequency and high selectivity filters have been hindered by the problems related to the filter architecture, high speed monolithic amplifier design, and integrated circuit technology. In this dissertation the problems of high speed amplifier design and integrated circuit technology in relation to the realization of practical high frequency switched-capacitor filters are addressed and investigated.

This research was sponsored by National Science Foundation Grant NSF ENG-7907055 and DARPA Grant N00039-81-K-0251.

ACKNOWLEDGEMENTS

I am deeply indebted to Professor Paul R. Gray for his guidance, patience and continuous support throughout the course of my Ph. D. research work. I hope that I have gained some of his keen insight and developed an intuitive feel in the field of analog integrated circuit design by being exposed to him.

I am also grateful to Professors Bob Brodersen, Dave Hodges, Robert Meyer and Bill Oldham for their helpful advice.

I would like to thank my partner, Tat C. Choi, with whom I have carried out this research work, for his very helpful suggestions and most important of all, for his constant support. Last but not the least, I wish to express my gratitude to my fellow colleagues and the my teammates of the RSB softball team.

DEDICATION

I dedicate this dissertation to my sister Lorraine who was struck down by cancer at the young age of 23. Sis, you're the one who inspired me to go for the Ph. D. This one is for you.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

Switched-capacitor filters have been very widely used to filter signals in the audio frequency range. If the switched-capacitor filtering technique can be extended into the high KHz and the MHz range, new avenues of application will be opened. For example, intermediate frequency filtering, clock recovery in data communication systems and video signal processing for TV receivers can be performed using this technique. Thus, the successful monolithic implementation of these functions will eventually lead to a higher degree of integration of data communication systems.

In the past, the practical and reproducible realization of high frequency and high selectivity monolithic filters has been hindered by the problems related to the filter architecture, amplifier design and IC technology. The maturation of high performance CMOS technology has improved the prospect of applying the switched-capacitor concept to make such monolithic filters. In this dissertation, the circuit design and technology considerations for high frequency and high selectivity switched-capacitor filters will be presented. The filter architecture aspect is covered in ref [1].

CHAPTER 2

THE EFFECTS OF AMPLIFIER NON-IDEALITIES IN SCF'S

The non-ideal characteristics of operational amplifiers can cause the frequency response of active filters to deviate from their designed response. In particular, the finite gain of the amplifier can cause the passband of the filter to droop. The finite bandwidth of the amplifier can induce excess phase shift that can result as peaking at the band-edge and Q-enhancement for high selectivity filters.

In order to determine the effects of the amplifier non-idealities on active filters, the frequency response of a resonator implemented using non-ideal integrators will be examined. The resulting analysis will be extended to study their effects on switched-capacitor filters.

2.1. The Non-ideal Integrator

The integrator is the principal building block for active filters realized by the leapfrog or the active ladder synthesis technique. Any non-ideal characteristics of the integrator will degrade the frequency response of the filter. Therefore, in order to design a well-behaved active filter, the effects of these non-idealities must be understood and controlled.

The frequency response of an ideal and a non-ideal integrator are shown in Fig. 2.1. The "real" or the non-ideal integrator has a finite gain of $\frac{\omega_o}{p_1}$ at DC. The finite gain at low frequencies is due to the presence of the low frequency pole p_1.

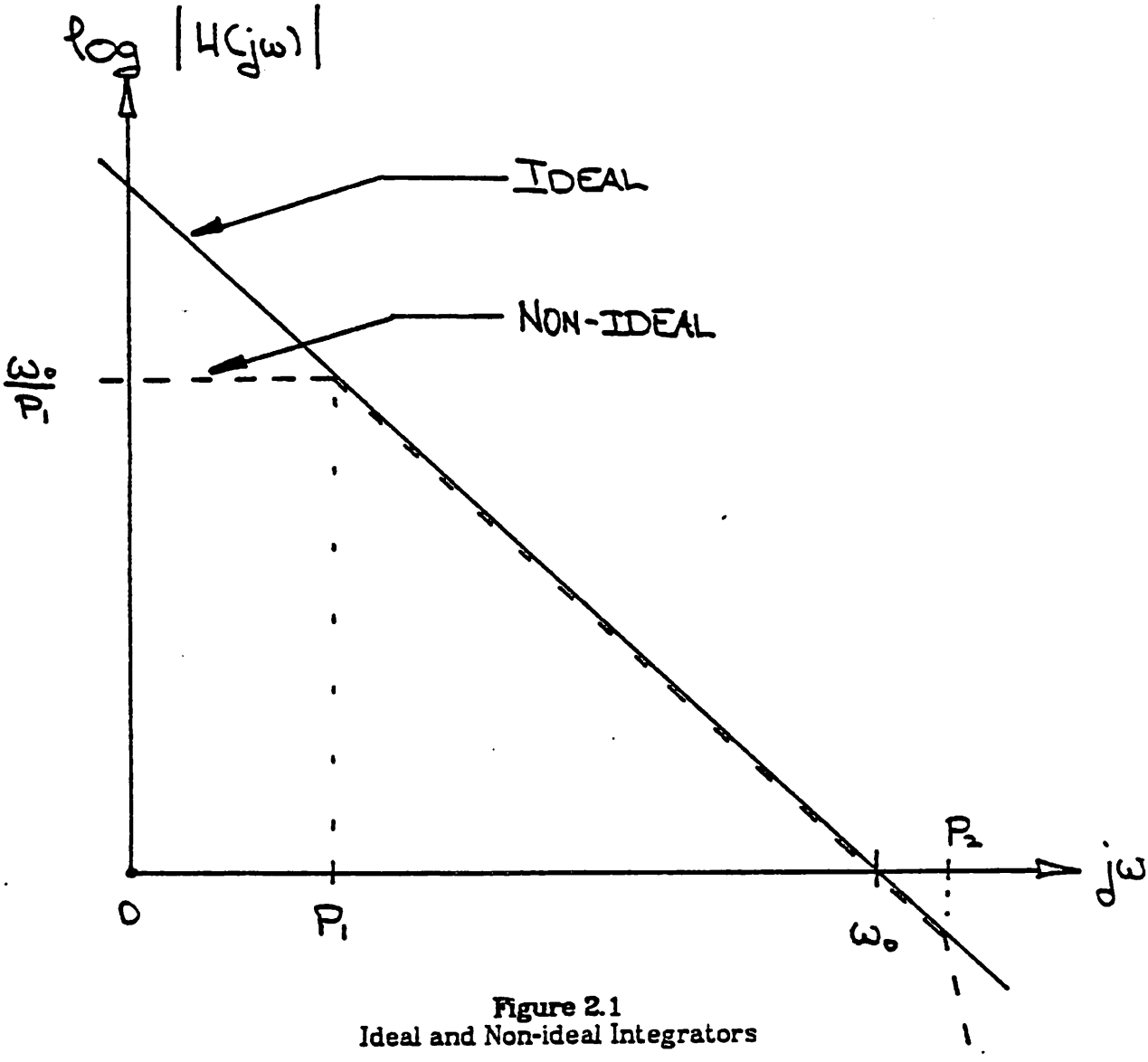


Figure 2.1
Ideal and Non-ideal Integrators

The integrator also exhibits a small amount of excess phase shift in the vicinity of its unity gain frequency ω_0. This phase shift is the result of the spurious high frequency pole p_2 which is typically located far beyond ω_0. The transfer function of such a "real" integrator can be modeled as

$$H(s) = \frac{\omega_0}{s + p_1} e^{-\frac{s}{p_2}}. \qquad (2.1)$$

The denominator $s + p_1$ models the finite gain of the integrator at low frequencies. The exponential term $e^{-\frac{s}{p_2}}$ represents the phase error that is caused by the spurious high frequency pole p_2. It is assumed that as long as $p_2 \gg \omega_o$ and in the vicinity of ω_o, the phase error dominates over the magnitude error; thus, the latter is small enough to be neglected.

In order to determine the effects of the non-ideal characteristics of the integrator, a resonator will be examined in detail. The signal flow graph of such a resonator is shown in Fig. 2.2. The integrators are assumed to be ideal and have the transfer function of $H(s) = \frac{\omega_o}{s}$. The bandpass output $\frac{V_o}{V_n}$ is

$$\frac{V_o}{V_n} = -a_o \frac{\omega_o s}{s^2 + s\frac{\omega_o}{Q_o} + \omega_o^2}. \tag{2.2}$$

The peaking frequency ω_{peak} and the selectivity Q can be obtained by finding the roots of the denominator polynomial [2]. They are

$$\omega_{peak} \approx \omega_o \left[1 - \frac{1}{8Q_o^2}\right] \tag{2.3a}$$

$$Q = Q_o . \tag{2.3b}$$

To simplify the analysis for the case of the "real" integrator, the finite integrator gain and the integrator excess phase shift effects will be considered independently.

2.1.1. Finite Integrator Gain

Assuming that the errors due to p_2 are small enough to be ignored, the transfer function of the integrator can be represented as

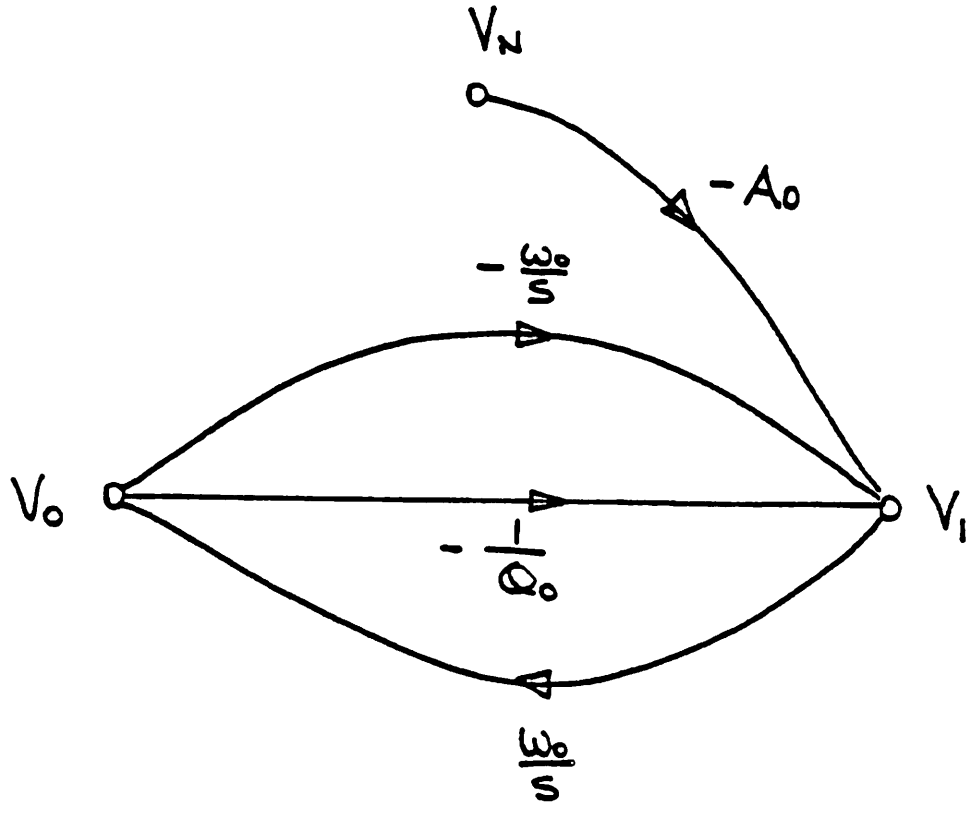


Figure 2.2
Signal Flow Graph of a Resonator

$$H(s) = \frac{\omega_0}{s + p_1} \tag{2.4}$$

where $\omega_0 \gg p_1$. The bandpass output $\frac{V_0}{V_n}$ is

$$\frac{V_0}{V_n} = -a_0 \frac{\omega_0 (s + p_1)}{s^2 + s\left\{2p_1 + \frac{\omega_0}{Q_0}\right\} + \left\{\omega_0^2 + p_1^2 + \frac{\omega_0 p_1}{Q_0}\right\}}. \tag{2.5}$$

Once again the peaking frequency and the selectivity are determined by finding

the roots of the denominator polynomial.

$$\omega_{peak} \approx \omega_o \left[1 - \frac{1}{8Q_o^2}\right] \tag{2.6a}$$

$$\frac{1}{Q} \approx \frac{1}{Q_o} + 2\left[\frac{p_1}{\omega_o}\right] \tag{2.6b}$$

$$\left|H(j\omega_o)\right| \approx a_o Q_o \left\{1 - 2Q_o\left[\frac{p_1}{\omega_o}\right]\right\}. \tag{2.6c}$$

For high selectivity filters, the finite integrator gain reduces both the gain and the Q of the filter, while the peaking frequency remains essentially unchanged. Note that the term $\frac{p_1}{\omega_o}$ is commonly referred to as the quality factor "Q" of the integrator [3]. Thus, an integrator with a large Q is essential to implement a narrow-band filter.

2.1.2. Finite Integrator Bandwidth (Excess Phase Shift)

If only the excess phase shift of the integrator is considered, the transfer function is equal to

$$H(s) = \frac{\omega_o}{s} e^{-\frac{s}{p_2}} \tag{2.7}$$

where the exponential term represents the phase error. The bandpass output becomes

$$\frac{V_o}{V_n} = -a_o \frac{\omega_o s e^{-\frac{s}{p_2}}}{s^2 + s\frac{\omega_o}{Q_o} e^{-\frac{s}{p_2}} + \omega_o^2 e^{-2\frac{s}{p_2}}}. \tag{2.8}$$

The exponential terms are approximated as

$$e^{-\frac{s}{p_2}} \approx 1 - \frac{s}{p_2}$$

$$e^{-2\frac{s}{p_2}} \approx 1 - 2\frac{s}{p_2}.$$

The peaking frequency, the selectivity and the filter gain are

$$\omega_{peak} \approx \omega_o \left[1 + \frac{1}{Q_o}\frac{\omega_o}{p_2} - \frac{1}{4Q_o^2} - \left[\frac{\omega_o}{p_2}\right]^2\right] \tag{2.9a}$$

$$\frac{1}{Q} \approx \frac{1}{Q_o} - 2\frac{\omega_o}{p_2} \tag{2.9b}$$

$$\left|H(j\omega_o)\right| \approx a_o Q_o \left\{1 + \frac{1}{2}\frac{\omega_o}{p_2}\left[\frac{\omega_o}{p_2} + 4Q_o\right]\right\}. \tag{2.9c}$$

The results clearly indicate that the excess phase shift initially increases the peaking frequency but eventually decreases it, enhances the Q of the filter, and peaks the gain at ω_o. The term $\frac{\omega_o}{p_2}$ is the total excess phase shift incurred by the integrator at its unity gain frequency ω_o. From Fig. 2.1 we can see by inspection that

$$\varphi_{excess}(\omega = \omega_o) = -\tan^{-1}\left[\frac{\omega_o}{p_2}\right] \tag{2.10}$$

$$\approx -\frac{\omega_o}{p_2}\ radians,$$

if $p_2 \gg \omega_o$. For high selectivity filters, the enhancement of Q is more pronounced than the shift in the peaking frequency. Therefore, in order to minimize the Q enhancement caused by excess phase, the high frequency pole p_2 must be at least $100Q_o$ times the integrator unity gain frequency ω_o for a resonator.

2.1.3. The Composite Response

The effects of finite gain and bandwidth of the non-ideal integrator are listed in Table 2.1. It is clearly evident that the finite gain and the bandwidth of the

	PEAKING FREQUENCY	SELECTIVITY
Ideal Integrator	$\omega_o\left[1-\frac{1}{8Q_o^2}\right]$	Q_o
Integrator Finite Gain	$\omega_o\left[1-\frac{1}{8Q_o^2}\right]$	$Q_o\left\{1-2Q_o\frac{p_1}{\omega_o}\right\}$
Integrator Finite Bandwidth	$\omega_o\left[1+\frac{1}{Q_o}\frac{\omega_o}{p_2}\right]$	$Q_o\left\{1+2Q_o\frac{\omega_o}{p_2}\right\}$

Table 2.1
Peaking Frequency and Selectivity of a Bandpass Filter
For Ideal and Non-ideal Integrator Response

integrator strongly affect the Q for highly selective filters. The sensitivity of the filter to integrator non-idealities is on the order of the designed selectivity Q_o of the filter.

$$Q_{overall} = Q_o\left\{1 + 2Q_o\left[\frac{\omega_o}{p_2} - \frac{p_1}{\omega_o}\right]\right\}. \qquad (2.11)$$

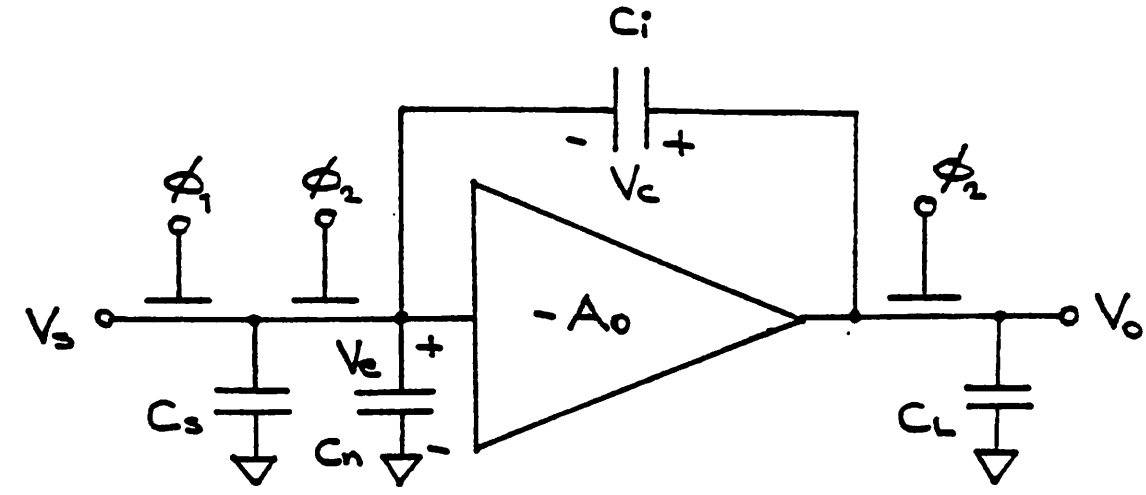
Eqn. 2.11 shows the selectivity of a resonator that incorporates both major non-idealities of the integrator. It is interesting to note that the term $\frac{\omega_o}{p_2} - \frac{p_1}{\omega_o}$ represents the total phase error of an integrator. p_1 contributes phase lag, while p_2 causes phase lead. The overall deviation of Q for a resonator that is synthesized by the leapfrog method is a function of the sum of the phase error introduced by both integrators.

2.2. The Switched-Capacitor Integrator

In Fig. 2.3 an LDI switched-capacitor integrator is shown. Φ_1 and Φ_2 are the non-overlapping two phase clocks; C_s, C_i, and C_n are the sampling, the integration, and the parasitic input capacitance, respectively; and α_o is the open loop DC gain of the amplifier. The non-idealities of the operational amplifier can distort the frequency response of the switched-capacitor integrator. Specifically, the finite open loop gain of the amplifier introduces a low frequency pole which limits the DC gain of the integrator. The settling error present at the end of the charge integration cycle induces excess phase shift in the phase response. This error is caused by the finite bandwidth of the operational amplifier. To better understand these effects, an analytical expression of the frequency response of a "real" switched-capacitor integrator must be formulated. In the subsequent sections, the frequency response of an LDI switched-capacitor integrator will be derived. To simplify the analysis, the finite gain and the finite bandwidth effects will be treated separately.

2.2.1. The Finite Gain Effect

A representative LDI switched-capacitor integrator, which is shown in Fig. 2.3, samples and stores the input signal V_s during the on time of the clock Φ_1. When Φ_1 goes low and Φ_2 comes up, the stored signal charge is transferred from the sampling capacitor C_s into the integrating capacitor C_i. Because the amplifier has a finite gain of α_o, there will always be a small error voltage V_e at the summing node. It is this error voltage that causes the integrator to have finite gain at low frequencies.



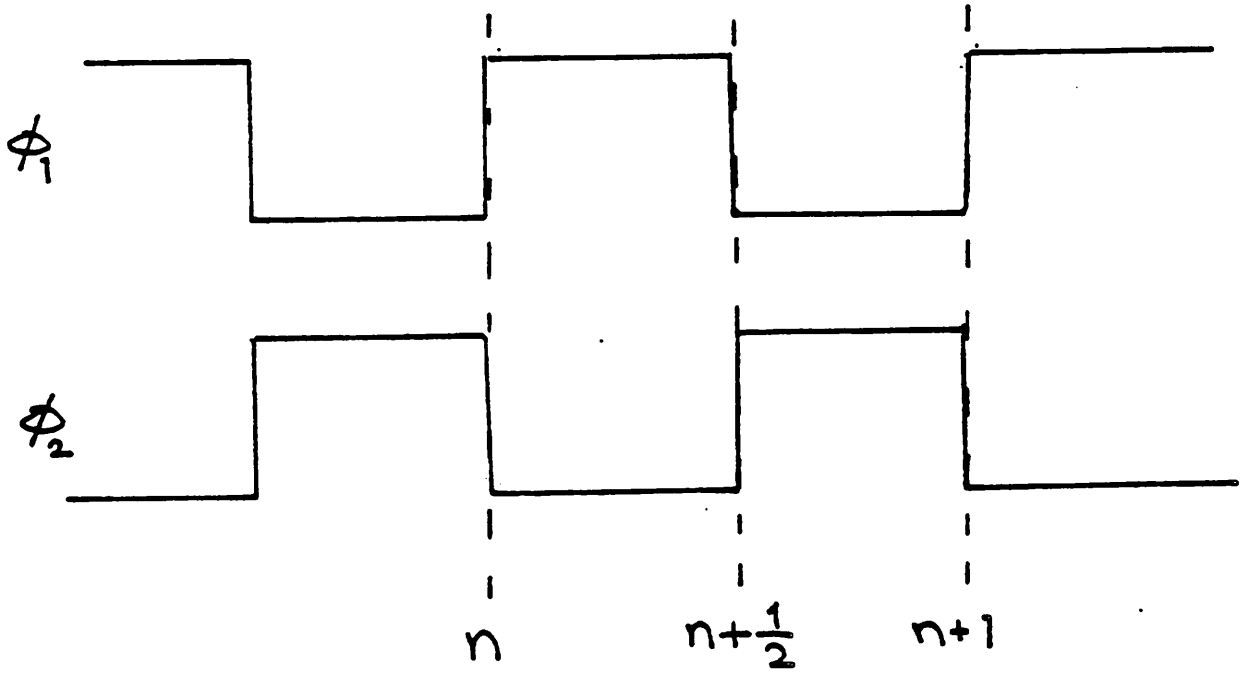


Figure 2.3
An LDI Switched-Capacitor Integrator with Finite Amplifier Gain

At time $t = n + 1$, the output voltage V_o of the switched-capacitor integrator is described by the following relationship:

$$V_o(n + 1) = V_c(n + 1) + V_e(n + 1) \tag{2.12}$$

where V_o is the output voltage, V_c is the voltage across the integration capacitor, and V_e is the summing node error voltage. The error signal V_e is simply the output voltage divided by the open loop gain of the amplifier,

$$V_e(n + 1) = -\frac{V_o(n + 1)}{a_o}. \tag{2.13}$$

The voltage across the integration capacitor can be expressed as

$$V_c(n + 1) = \frac{Q_c(n + 1)}{C_i}. \tag{2.14}$$

The charge $Q_c(n + 1)$ is the sum of the charge $Q_c(n)$ stored during the previous clock cycle and of that which has been transferred to C_i during the current cycle. Thus,

$$Q_c(n + 1) = Q_c(n) + Q_i(n + \tfrac{1}{2}) - Q_e(n + 1) \tag{2.15}$$

$$Q_i(n + \tfrac{1}{2}) = C_s\, V_i(n + \tfrac{1}{2}) \tag{2.16}$$

$$Q_e(n + 1) = -\frac{C_s + C_n}{a_o} V_o(n + 1) \tag{2.17}$$

Combining Eqns. 2.12 through 2.17, and taking the Z-Transform, we obtain the following transfer function

$$H(z) = \frac{V_o(z)}{V_i(z)} \tag{2.18a}$$

$$= -\frac{C_s}{C_i} \frac{z^{\frac{1}{2}}}{z\left[1 + \frac{1}{a_o f}\right] - \left[1 - \frac{1}{a_o}\right]} \tag{2.18b}$$

where $f = \dfrac{C_i}{C_i + C_s + C_n}$. For a very large amplifier gain, Eqn. 2.18b simplifies to

$$H(z) \approx -\frac{C_s}{C_i}\frac{z^{\frac{1}{2}}}{z-1} \tag{2.19}$$

which is the ideal transfer function of an LDI switched-capacitor integrator. If the frequency of interest is much less than the clock frequency $\frac{1}{T}$, the frequency response can be obtained by letting $z = e^{j\omega T} \approx 1 + j\omega T$. Then we have

$$H(j\omega) = -\frac{C_s}{C_i}\frac{1}{j\omega T + \frac{1}{a_0 f}}. \tag{2.20}$$

The low frequency pole, which corresponds to p_1 in Fig. 2.1, is

$$p_1 = \left\{\frac{1}{a_0 f}\frac{1}{T}\right\} \tag{2.21a}$$

$$= \left\{\frac{1}{T}\frac{1}{a_0\frac{C_i}{C_s + C_n + C_i}}\right\}. \tag{2.21b}$$

The pole location is inversely proportional to the **loop gain** of the switched-capacitor integrator. Therefore, the finite amplifier gain of a_0 induces a phase error of approximately $+\frac{p_1}{\omega_0}$ radians

$$\frac{p_1}{\omega_0} \approx +\left\{\frac{1}{T}\frac{1}{a_0\frac{C_i}{C_s + C_n + C_i}}\right\}\left\{\frac{C_i T}{C_s}\right\}$$

$$\approx +\left\{\frac{1}{a_0}\frac{C_s + C_n + C_i}{C_s}\right\}. \tag{2.22}$$

2.2.2. The Finite Bandwidth Effect

An amplifier that has a finite bandwidth requires a certain delay before its output reaches the final value. In Fig. 2.4, an LDI switched-capacitor integrator

that is implemented using an operational amplifier having a very large DC gain but a finite bandwidth ω_u is shown. The two phase non-overlapping clocks, which operate at a duty cycle of m, drive the three MOS transfer gates. During the charge integration phase when Φ_2 is high, the integrator must settle its output within the designated time of mT_c. If the amplifier does not have sufficient bandwidth, settling error will be present at the output of the integrator. This error is a function of the closed loop bandwidth ω_u of the amplifier and of the available integration time mT. The error, therefore, is directly related to the settling behavior of the amplifier. That is,

$$Error \;\alpha\; \exp\left\{-mT\,\omega_u\right\}. \tag{2.23}$$

In order to obtain a frequency domain transfer function representation that incorporates the finite bandwidth of the amplifier, the integrator must be first analyzed in the sampled-data domain. The z-domain transfer function is then mapped into the frequency domain by means of the following transform pair $z = e^{j\omega T}$. [4].

The transient behavior of the output voltage V_o and the summing node error voltage V_e of an LDI switched-capacitor integrator is shown in Fig. 2.4. At time $t = n + 1$, the output voltage V_o is equal to the sum of the voltage V_c across the integration capacitor C_i and the error voltage V_e at the summing node:

$$V_o(n+1) = V_c(n+1) + V_e(n+1). \tag{2.24}$$

The voltage $V_c(n+1)$ is the sum of the voltage $V_c(n)$ during the previous cycle, and of the updating voltage.

$$V_c(n+1) = V_c(n) - \frac{C_s}{C_i}\left\{V_s(n+\tfrac{1}{2}) - V_e(n+1)\right\}. \tag{2.25}$$

$V_e(n+1)$ is the residual summing node voltage at the very end of the charge integration period. To be exact, it consists of the residual error voltage of the

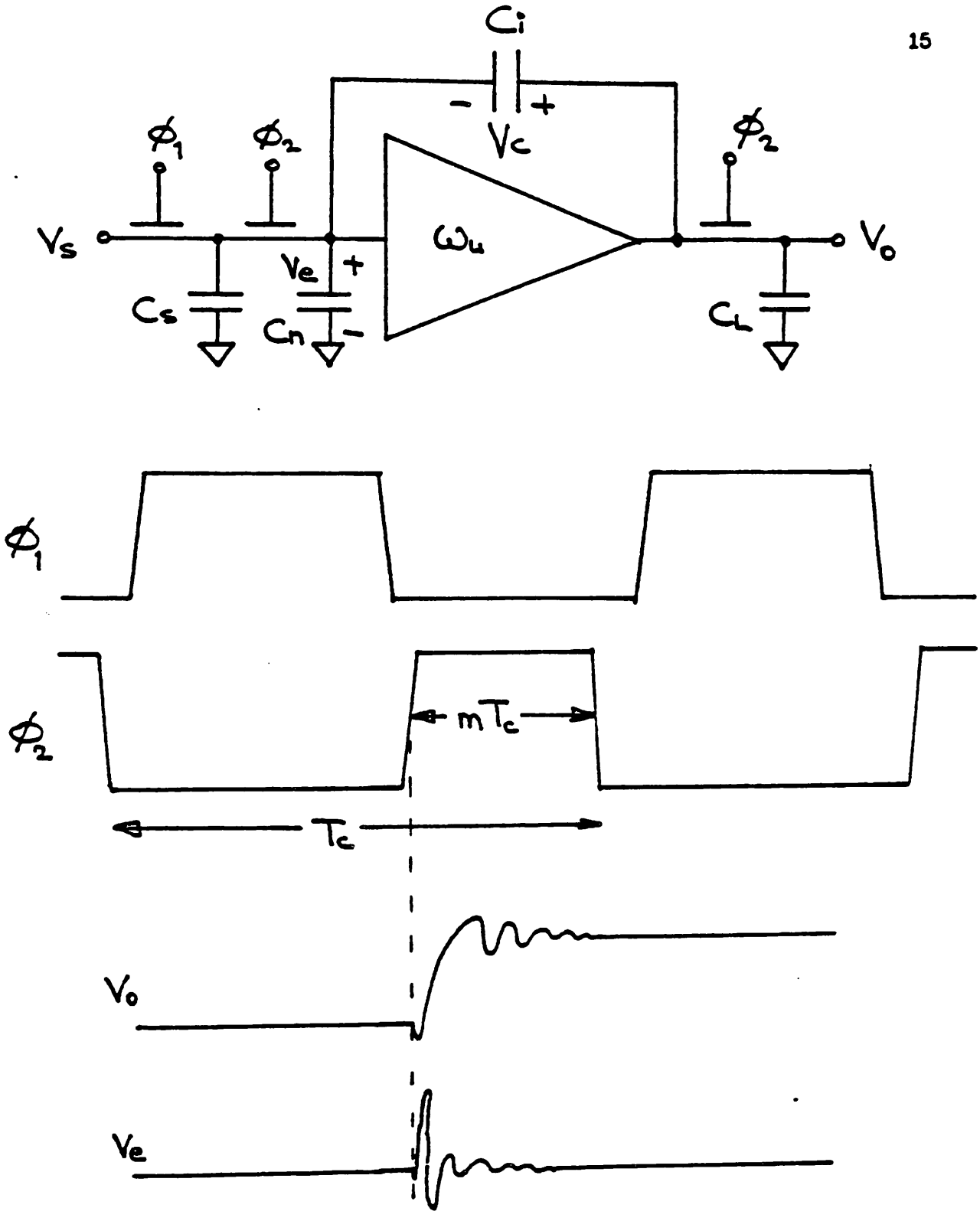


Figure 2.4
An LDI Switched-Capacitor Integrator with Finite Amplifier Bandwidth

most recent integration cycle and of all the previous cycles. Mathematically, it is given by

$$V_o(n+1) = \frac{C_s}{C_s + C_n + C_i} V_s\left(n + \frac{1}{2}\right) e^{-mT\omega_{u_o}} + V_o(n) e^{-mT\omega_u} e^{-(1-m)T\omega_{u_o}}$$

$$= \frac{C_s}{C_s + C_n + C_i} e^{-a_2} \sum_{p=0}^{\infty} V_s\left(n - p + \frac{1}{2}\right) e^{-p(a_1 + a_2)} \qquad (2.26)$$

where $a_1 = (1-m)T\omega_{u_o}$ and $a_2 = mT\omega_u$. ω_u is the closed loop bandwidth of the amplifier when Φ_2 is high, and ω_{u_o} is the bandwidth when Φ_2 is low. It is important to differentiate these two cases since the loading of the amplifier and the loop gain vary depending on the state of the clock Φ_2. The z-transformed representations of Eqns. 2.24 through 2.26 are

$$V_o = V_c + V_e \qquad (2.27a)$$

$$V_c = -\frac{C_s}{C_i} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} V_s + \frac{C_s}{C_i} \frac{1}{1 - z^{-1}} V_e \qquad (2.27b)$$

$$V_e = \frac{C_s}{C_s + C_n + C_i} \frac{z^{-\frac{1}{2}} e^{-a_2}}{1 - z^{-1} e^{-(a_1 + a_2)}} . \qquad (2.27c)$$

The z-domain transfer function is obtained by combining Eqns. 2.27a through 2.27c.

$$H(z) = \frac{V_o}{V_s} \qquad (2.28)$$

$$= \left\{ -\frac{C_s}{C_i} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \right\} \left\{ \frac{\left[1 - R_s e^{-a_2} - \frac{C_i}{C_s} R_s e^{-a_2}\right] - z^{-1}\left[e^{-(a_1 + a_2)} - R_s e^{-a_2}\right]}{1 - z^{-1} e^{-(a_1 + a_2)}} \right\}$$

where $R_s = \frac{C_s}{C_s + C_n + C_i}$, $a_1 = (1-m)T\omega_{u_o}$, and $a_2 = mT\omega_u$. The expression enclosed within the first pair of braces is the ideal LDI transfer function. The second braced expression represents the error due to the finite amplifier bandwidth. The frequency domain representation of the error term is obtained

by substituting $z = e^{j\omega T} \approx 1 + j\omega T$. Thus,

$$H_{error}(j\omega) = \frac{\left\{1 - e^{-(a_1+a_2)} - \frac{C_i}{C_s + C_n + C_i}e^{-a_2}\right\} + j\omega T\left\{e^{-(a_1+a_2)} - \frac{C_s}{C_s + C_n + C_i}e^{-a_2}\right\}}{\left\{1 - e^{-(a_1+a_2)}\right\} + j\omega T e^{-(a_1+a_2)}} \quad (2.29)$$

The expression is simplified by using the fact that $e^{-(a_1+a_2)} \ll e^{-a_2} \ll 1$.

$$H_{error}(j\omega) \approx \frac{1 - j\omega T\frac{C_s}{C_s + C_n + C_i}e^{-a_2}}{1 + j\omega T e^{-(a_1+a_2)}} \quad (2.30a)$$

$$= \frac{1}{1 + \omega^2 T^2 e^{-2(a_1+a_2)}}\left\{\left[1 - \omega^2 T^2 e^{-(a_1+2a_2)}\right] - j\omega T e^{-a_2}\right\} . \quad (2.30b)$$

If we let

$$1 - \omega^2 T^2 e^{-(a_1+2a_2)} = 1 - \delta$$

and

$$\omega T e^{-a_2} = \varphi ,$$

we have

$$H_{error}(j\omega) \approx (1 - 2\delta)\, e^{-j\varphi} . \quad (2.31)$$

Therefore, the magnitude and the phase errors attributed to the settling error of the amplifier are

$$Magnitude\ Error \approx 2\omega^2 T^2 e^{-(a_1+2a_2)} \quad (2.32a)$$

$$Phase\ Error \approx -\omega T e^{-a_2} . \quad (2.32b)$$

In the vicinity of the unity gain frequency of the integrator, the phase error overwhelms the magnitude error. The phase error evaluated at the unity gain frequency $\omega_o = \frac{C_s}{TC_i}$ is

$$\varphi_{excess}(\omega = \omega_o) = -\frac{C_s}{C_i}e^{-mT\omega_u} . \quad (2.33)$$

Under the assumption that the excess phase is small, the location of the spurious high frequency pole p_2 of the integrator can be approximated.

$$\varphi_{excess}(\omega = \omega_0) = -\tan\left[\frac{\omega_0}{p_2}\right]$$

$$\approx -\frac{\omega_0}{p_2} \quad \text{if } p_2 \gg \omega_0 \ .$$

Thus,

$$p_2 \approx -\frac{1}{T}\exp\left[mT\ \omega_u\right] \ . \tag{2.34}$$

The amount of excess phase can be reduced by pushing p_2 out. This can be accomplished by increasing the duty cycle m of the clock or by using an amplifier that has a broader bandwidth.

It should be noted that the previous analysis is valid only for small settling errors. As the settling error becomes larger, Eqn. 2.29 can no longer be approximated by Eqn. 2.30 since the condition $e^{-(a_1 + a_2)} \ll e^{-a_2} \ll 1$ no longer holds. Eqn. 2.29 indicates that for moderate settling errors the magnitude error dominates over the phase error. Under this condition, the integrator will appear very lossy as if the amplifier has a very low gain.

2.2.3. The Composite Response

The approximate performance of a switched-capacitor resonator can be predicted by using the results obtained thus far. The results tabulated in Table 2.1 clearly show that the Q can deviate significantly for highly selective filters. The change in the Q is a function of the *total phase error* incurred by the two integrators. The phase deviations due to finite gain and bandwidth are listed in Table 2.2. In order to keep this error small, the amplifier must have a large open loop gain and a wide closed loop bandwidth. Because the phase errors attributed

to these two non-idealities are offsetting, the total Q deviation is not as serious as it appears to be.

	PHASE ERROR (RADIANS)
Finite Amplifier Gain, a_0	$+\frac{1}{a_0}\frac{C_s + C_n + C_i}{C_s}$
Finite Amplifier Bandwidth, ω_u	$-\frac{C_s}{C_i}e^{-mT\omega_u}$

Table 2.2
Phase Error of an LDI Switched-Capacitor Integrator with Amplifier Non-idealities

CHAPTER 3

DESIGN CONSIDERATIONS FOR HIGH SPEED AMPLIFIERS

The design of a fast settling amplifier is one of the key for the successful implementation of high frequency and high selectivity switched-capacitor filters. In this chapter, the frequency and transient response of closed loop amplifiers are examined in detail. The results of this study are used to determine the characteristics of an amplifier having the best speed performance.

3.1. Relationship Between Frequency and Transient Response

In general, fast settling amplifiers are synonymous of broadband amplifiers. However, the converse in not always true. Fig. 3.1 shows the frequency response of two broadband amplifiers which have nearly identical frequency response. The response of amplifier B includes a pole-zero doublet at ω_d. This minor difference causes the transient response of amplifier B to differ from that of amplifier A [5]. In an unity gain feedback configuration, the transient response of the latter is characterized by $e^{-\frac{t}{\omega_u}}$. However, the transient response of the former is governed by both $e^{-\frac{t}{\omega_u}}$ and $e^{-\frac{t}{\omega_d}}$. Their respective output response to an unit step input are

Amplifier A

$$V_{out}(t) = 1 - e^{-\frac{t}{\omega_u}} \tag{3.1}$$

Amplifier B

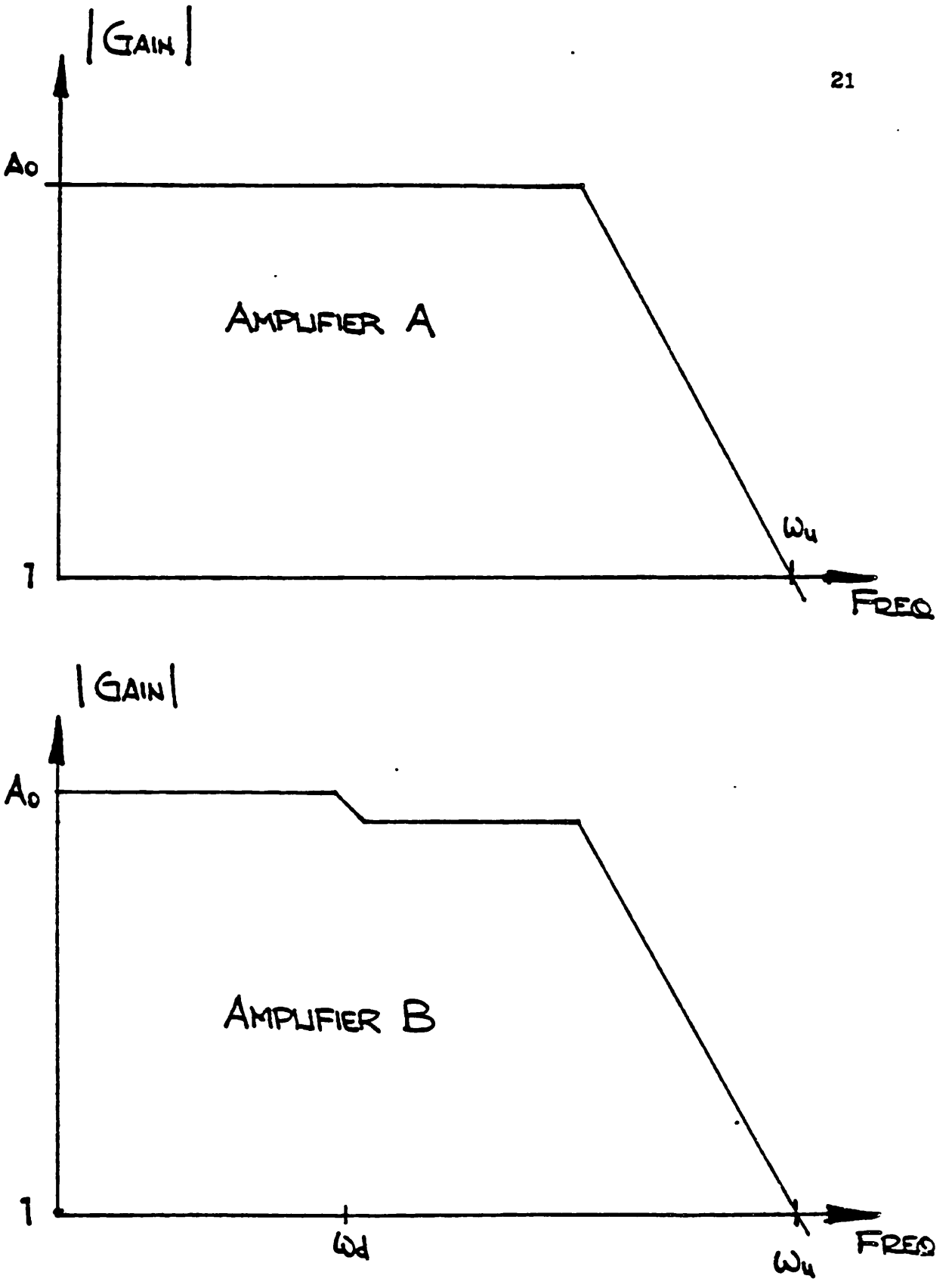


Figure 3.1
The Frequency Response of Broadband Amplifiers

$$V_{out}(t) = 1 - e^{\frac{-t}{\omega_u}} - e^{-\frac{t}{\omega_d}} . \tag{3.2}$$

If $\omega_d \ll \omega_u$, then amplifier B responds much slower than amplifier A does. Thus, a fast settling amplifier must not only have a broad bandwidth, but must also have no pole-zero doublets below its unity gain frequency ω_u. In addition to these constraints, the presence of non-dominant poles must also be considered. In certain feedback configurations, the non-dominant poles can adversely affect the response of the amplifier. Therefore, the key issues involved in the design of high speed, closed loop amplifiers are

1. the open loop frequency response of the amplifier;
2. the root locus of the closed loop amplifier;
3. and the frequency compensation for optimal transient response.

3.1.1. The Ideal Feedback Amplifier

Whenever feedback is applied around an amplifier, the pole location is modified. In Fig. 3.2 the root loci for three different amplifiers are illustrated.

Case 1

Here, the basic amplifier has only one pole. With increasing feedback, the pole s_1 moves toward $-\infty$ along the real axis σ. For a loop gain of A_{loop}, the closed loop bandwidth of the amplifier is $A_{loop}s_1$. Since the closed loop pole is real, the transient response is purely exponential.

Case 2

In this case, the amplifier is assumed to have a dominant pole s_1 and a high frequency, non-dominant pole s_p. When the loop is closed, and with increasing negative feedback, the two poles converge and form a complex pole pair which

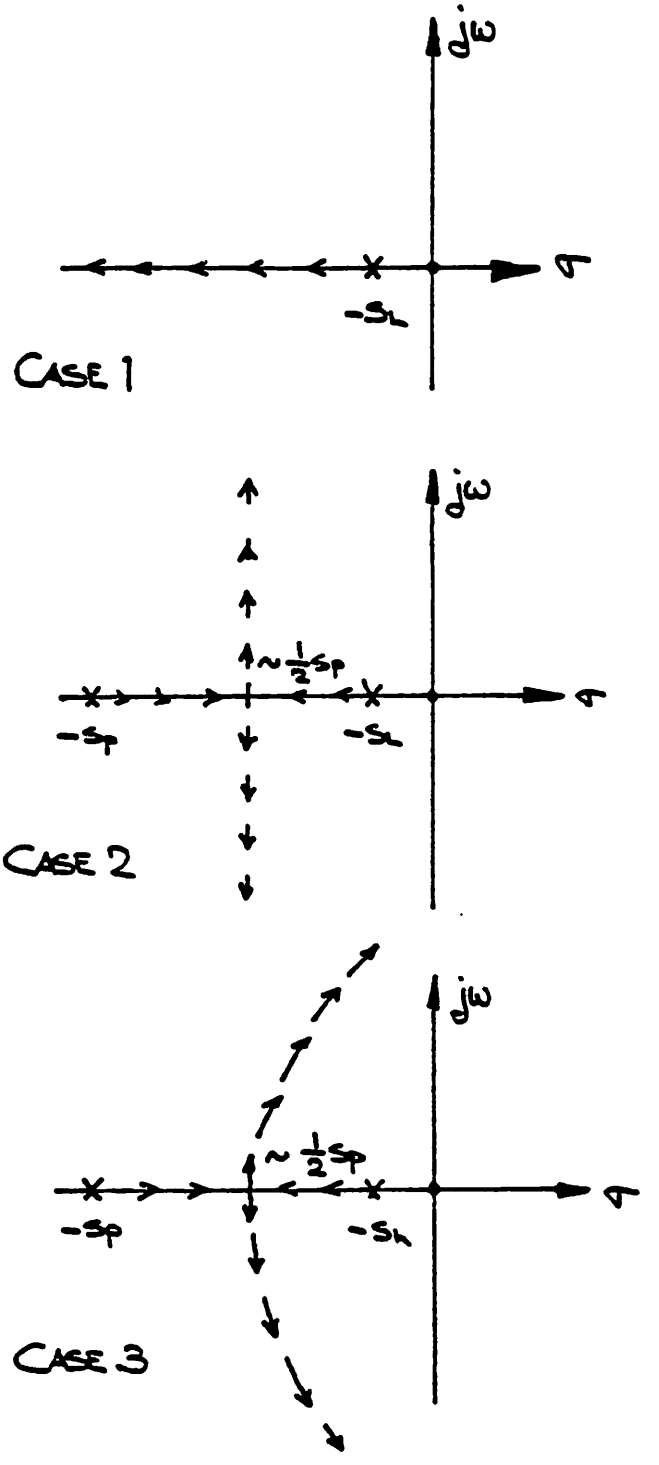


Figure 3.2
Root Loci of Feedback Amplifiers With One, Two, and Three Poles

travels parallel to the imaginary axis $j\omega$. The break-away occurs at approximately $-\frac{1}{2}s_p$. Since the poles are complex, the step response may overshoot and ring.

Case 3

Now the amplifier contains a second high frequency, non-dominant pole s_h, in addition to the two poles, s_l and s_p. In a closed loop configuration, s_h tends toward $-\infty$ while s_l and s_p converge at approximately $-\frac{1}{2}s_p$ and subsequently form a complex pole pair. With further increase in loop gain, the complex pole pair bends and travels into the right-half plane. The transient response is almost totally determined by the complex pole pair.

From the viewpoint of practical amplifier design, the situation in case 1 is highly unrealistic. No matter how simple the amplifier is, there always will be one or more high frequency, non-dominant poles. Cases 2 and 3 represent a more realistic situation. Note that the root loci in case 3 asymptotically approaches that in case 2 as s_h is pushed out farther. Thus, in most cases, the basic amplifier can be modeled adequately as a two pole system.

3.1.2. The Two-pole Feedback Amplifier

A detailed root loci of a two-pole feedback amplifier is shown in Fig. 3.3. Under moderate amount of loop gain $\left(A_{loop} > 100\right)$, the poles are complex. The location of the pole pair is given by

$$s = \sigma_p \pm j\omega_p \tag{3.3}$$

where $\sigma_p \approx -\frac{1}{2}s_p$. The exact behavior of the step response is determined by σ_p and ω_p. The time constant of the exponential rise is inversely proportional to σ_p.

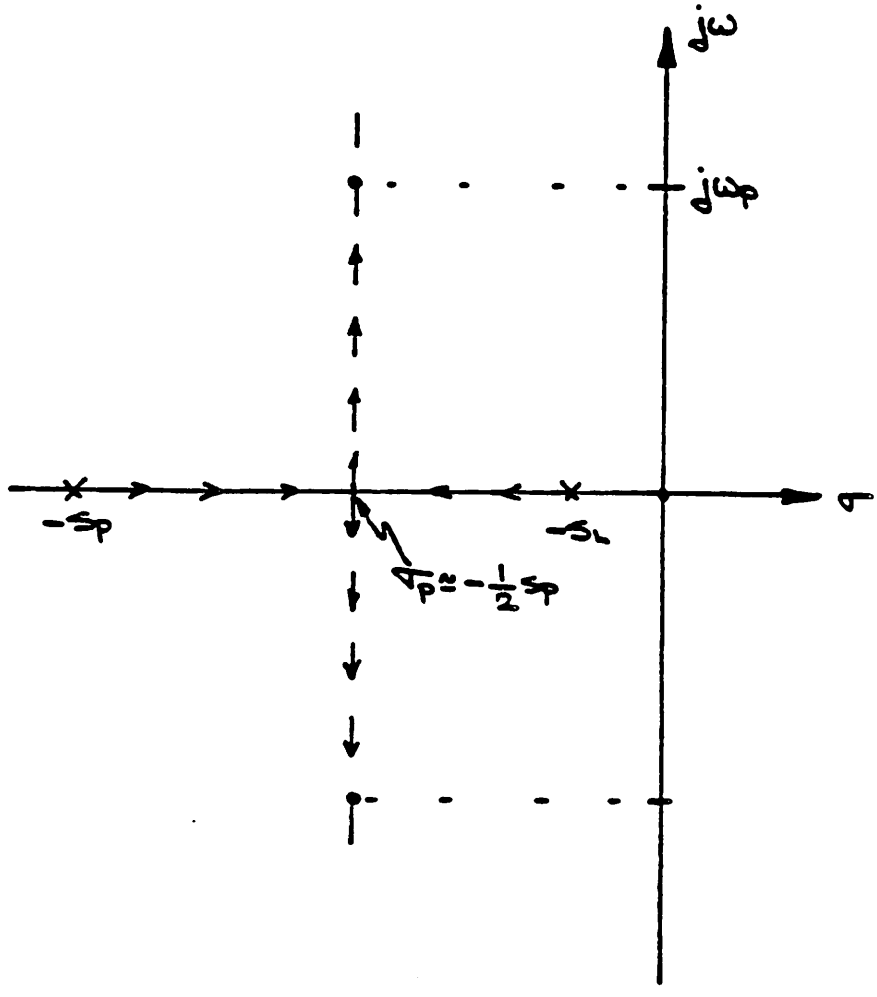


Figure 3.3
A Detailed Root Loci of a Two-pole Feedback Amplifier

---

while the ringing frequency is given by ω_p. The ratio $\frac{\omega_p}{|\sigma_p|}$ or the Q of the poles dictates the extent of overshooting and ringing [6]. For a well-behaved settling response, the Q should be less than one. The exponential time constant σ_p determines the speed of the settling behavior. Therefore, in order to attain a fast and

well-behaved settling response, σ_p must be made as large as possible while keeping Q below one. This implies that s_p be made as large as possible since $\sigma_p \approx -\frac{1}{2}s_p$. Thus, the basic amplifier must have a very high frequency, non-dominant pole s_p. There is, however, a limit to the maximum attainable closed loop bandwidth. The maximum bandwidth ω_{max} of a closed loop amplifier that has a loop gain of A_{loop}, and open loop poles of s_l and s_p is

$$\omega_{max} = \begin{cases} -\frac{1}{2}s_p & \text{if } A_{loop} \geq \frac{1}{4}\frac{s_p}{s_l} \\ A_{loop}s_l & \text{if } A_{loop} < \frac{1}{4}\frac{s_p}{s_l} \end{cases} \tag{3.4}$$

In an unity gain feedback configuration, the above expression can be rewritten as

$$\omega_{max}(\textit{unity gain}) = \begin{cases} -\frac{1}{2}s_p & \text{if } A_o s_l \geq \frac{1}{4}s_p \\ A_o s_l & \text{if } A_o s_l < \frac{1}{4}s_p \end{cases} \tag{3.5}$$

where A_o is the open loop gain of the amplifier. The term $A_o s_l$ corresponds to the open loop gain-bandwidth product of the amplifier. Therefore, the crux for designing a high speed, two-pole amplifier is to maximize the gain-bandwidth product and to push s_p out as far out as possible. This, however, does not necessarily guarantee that the settling response is well-behaved. To be more specific, the Q of the complex pole pair could be greater than one. Because the open loop gain A_o can vary significantly, controlling the Q of the poles becomes an important design task.

3.1.3. The Two-Pole, One-Zero Feedback Amplifier

The proper design of a fast settling feedback amplifier requires a technique to tailor the Q of the complex pole pair. It is not absolutely necessary to be able to pin down the poles at pre-determined locations. It will often suffice if the Q of

the poles is guaranteed to be less than a prescribed maximum value.

Perhaps the simplest and the most effective way to frequency compensate the closed loop amplifier is to add a real left-half plane zero to its transfer function. Fig. 3.4 shows the modified root loci after the zero insertion. The zero can be placed in three different regions:

1. below the dominant pole s_l;
2. between the dominant and the first non-dominant pole s_p;
3. and beyond the non-dominant pole [7].

In cases 1 and 2, with sufficient loop gain, the dominant pole converges to the zero z_o and forms a pole-zero doublet, while the non-dominant pole veers toward $-\infty$ [8].

The resulting closed loop amplifier will have a broad bandwidth; however, the transient response is limited in speed due to the presence of the pole-zero doublet. The consequence of the pole-zero doublet on transient response was discussed in section 3.1. For high speed amplifier design these two cases are undesirable.

In case 3 the zero forces the complex pole pair to take a circular trajectory which is centered at $-z_o$. The break away point remains unchanged at $-\frac{1}{2}s_p$. The complex pole pair re-enters the negative real axis at approximately $-2z_o + \frac{1}{2}s_p$. Thereafter, one pole tends toward $-\infty$ while the other converges to the zero $-z_o$. The advantage of this compensation scheme becomes obvious when we examine a detailed drawing of case 3, which is shown in Fig. 3.5. In the absence of any other non-dominant poles, the circular trajectory of the complex pole pair has a radius of $z_o - \frac{1}{2}s_p$. Thus, the radius of this circle is determined by the location of the zero for a fixed s_p. For a well-behaved transient response,

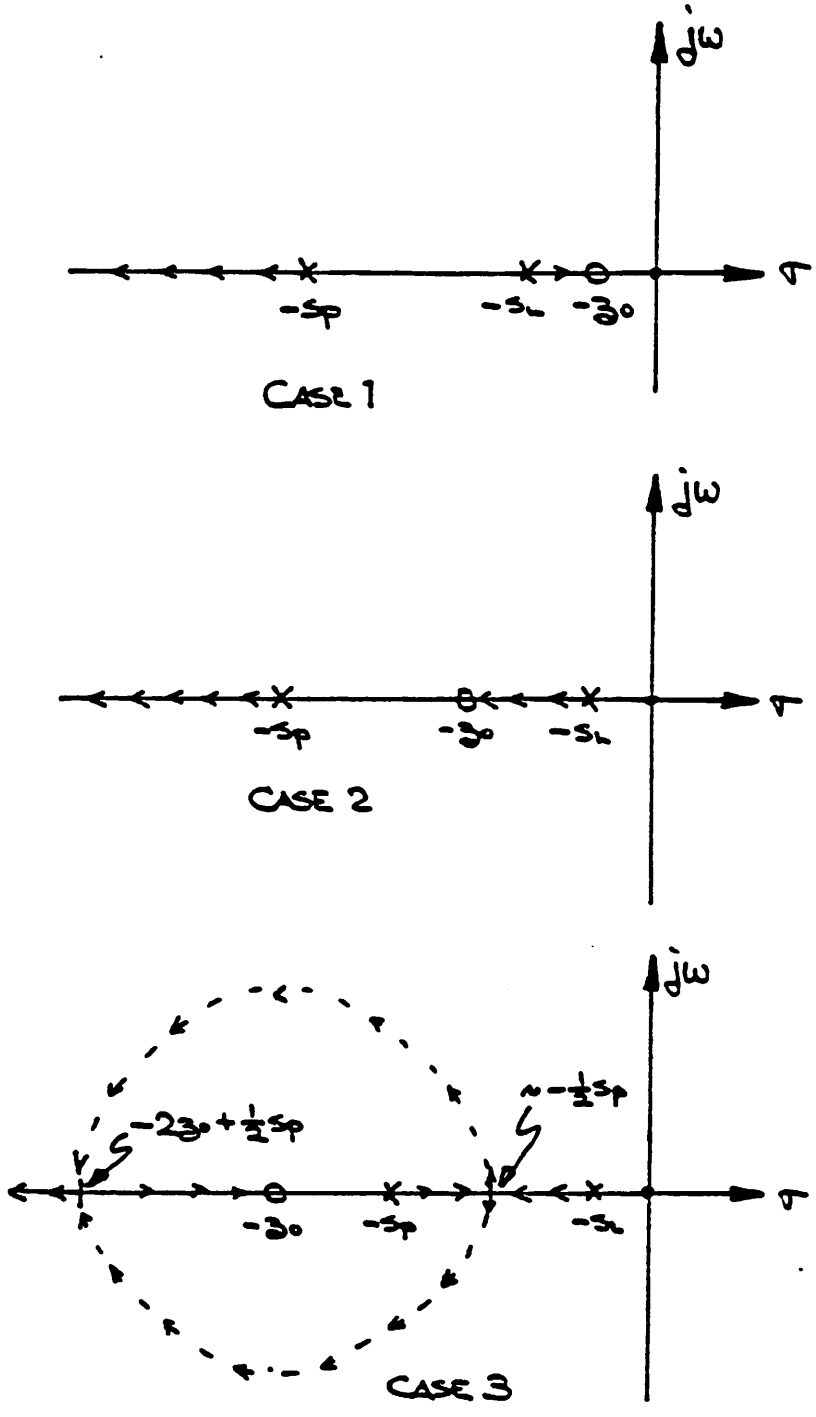


Figure 3.4
Root Loci of a Two-Pole, One-Zero Feedback Amplifiers

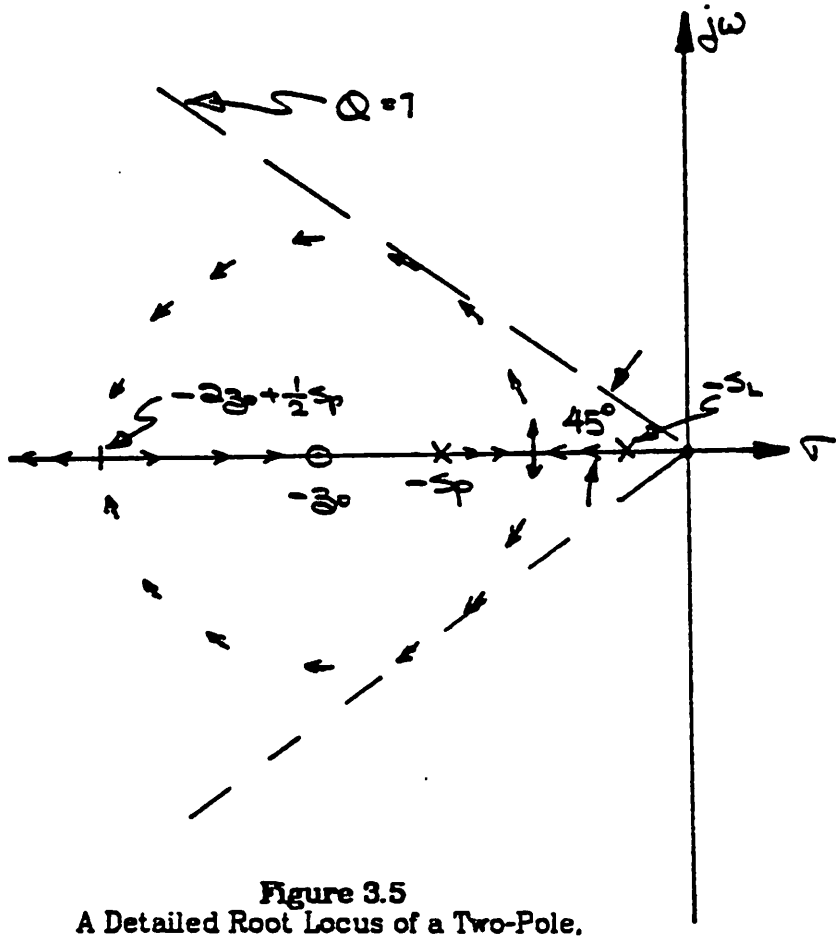


Figure 3.5
A Detailed Root Locus of a Two-Pole, One-zero Feedback Amplifier

the maximum Q of the complex pole should be less than unity. In other words, the circular trajectory must be contained inside the field defined by $Q = 1$. Geometrically, the optimum zero location $z_0\,(opt)$ for a fixed s_p is obtained.

$$z_0(opt) = -s_p\left[1+\frac{\sqrt{2}}{2}\right] . \tag{3.6}$$

The maximum possible Q under this condition is one. This means that this feedback amplifier will exhibit a well-behaved transient response even if the open loop gain varies over a wide range.

If sufficient loop gain is available, the closed loop bandwidth can easily exceed s_p in value. The maximum attainable bandwidth is approximately

$$\omega_{max} \approx s_p\left[\frac{3}{2}+\sqrt{2}\right] \tag{3.7}$$

with a maximum pole Q of 1. The ω_{max} for the two-pole, one-zero configuration is significantly larger than that of the two-pole case (see Eqn. 3.5). Thus, the insertion of a real left-half plane zero at $z_0(opt)$ speeds up the transient response and also guarantees a well-behaved response.

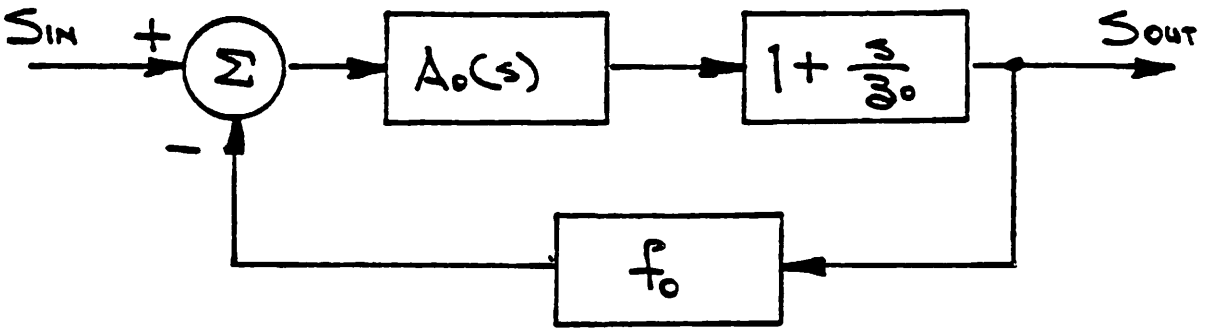
3.1.4. Real Left-Half Plane Zero Insertion

The real left-half plane zero z_0 is inserted in the feedback loop through either the feedback path or the forward gain path of the amplifier. The block diagrams of these two cases are shown in Fig. 3.6. In both situations, the loop gain expressions are identical, and are given by

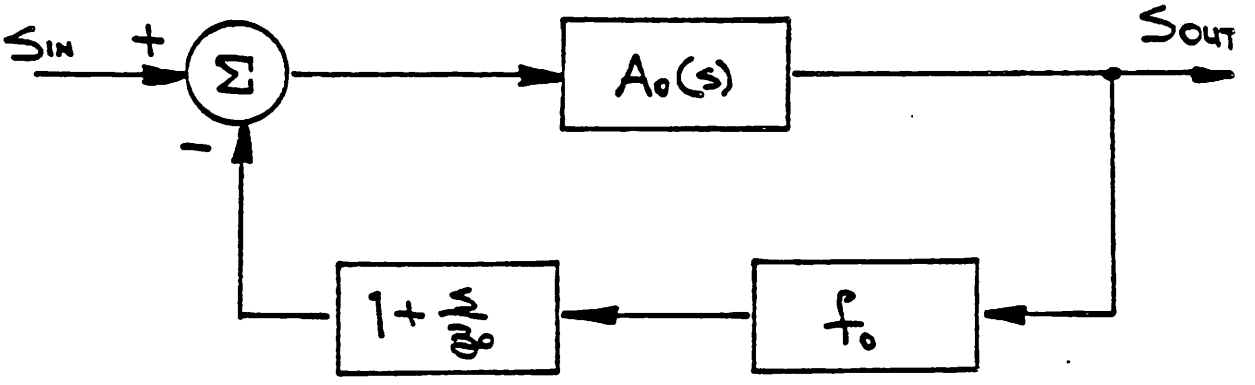
$$A_{loop} = -A_0(s)f_0\left[1+\frac{s}{z_0}\right] . \tag{3.8}$$

The closed loop transfer function $\frac{S_0}{S_{in}}$ are different, however. The transfer function with the zero in the forward path is

$$H_{forward}(s) = \frac{A_0(s)\left\{1+\frac{s}{z_0}\right\}}{1+A_0(s)f_0\left\{1+\frac{s}{z_0}\right\}} . \tag{3.9}$$



ZERO IN FEEDFORWARD PATH



ZERO IN FEEDBACK PATH

Figure 3.6
Left-Half Plane Zero Insertion

The transfer function with the zero in the feedback path is

$$H_{feedback}(s) = \frac{A_0(s)}{1 + A_0(s) f_0 \left\{1 + \frac{s}{z_0}\right\}} . \tag{3.10}$$

If the amplifier block is represented as a two-pole system, the resulting closed loop transfer functions are

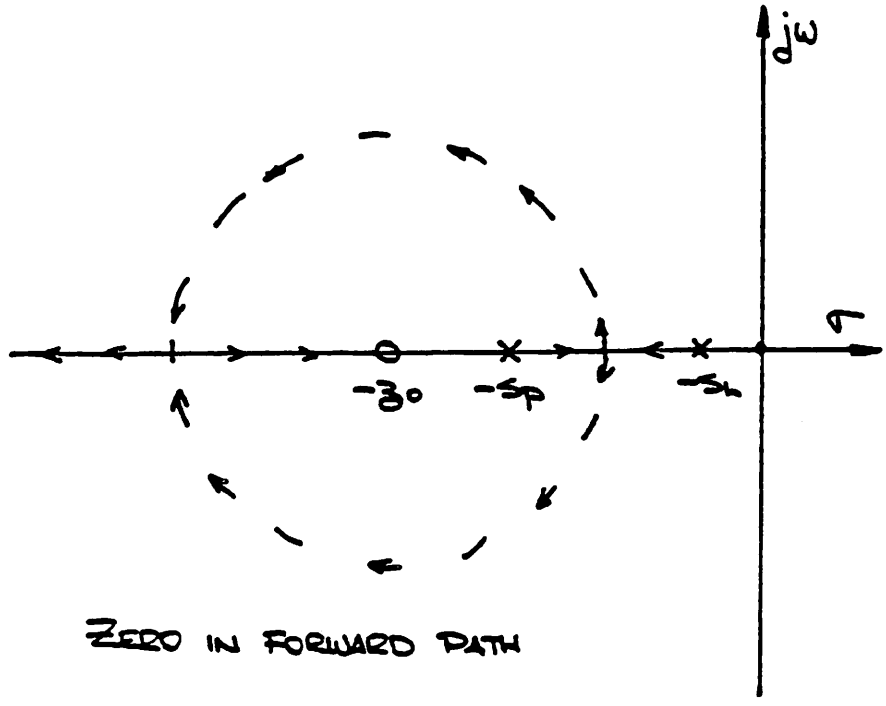
$$H_{forward}(s) = \frac{a_0 \left[1 + \frac{s}{z_0}\right]}{\left[1 + \frac{s}{s_p}\right]\left[1 + \frac{s}{s_l}\right] + a_0 f_0 \left[1 + \frac{s}{z_0}\right]} \tag{3.11}$$

$$H_{feedback}(s) = \frac{a_0}{\left[1 + \frac{s}{s_p}\right]\left[1 + \frac{s}{s_l}\right] + a_0 f_0 \left[1 + \frac{s}{z_0}\right]} . \tag{3.12}$$

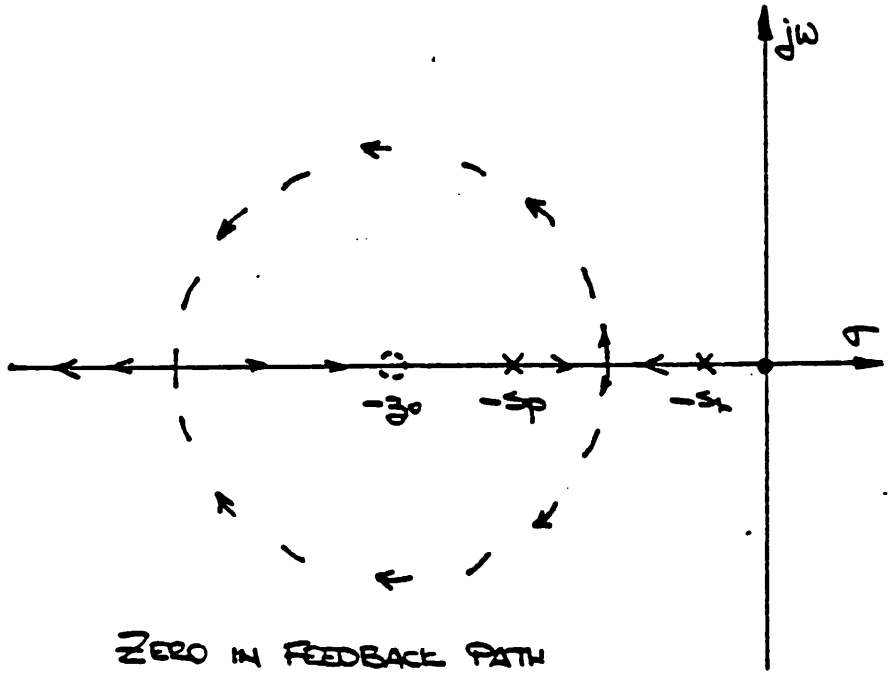
The corresponding root loci are illustrated in Fig. 3.7. In the latter, although the zero is present in the loop gain expression, it does not manifest itself in the closed loop transfer function. Such a zero is called a phantom zero [9]. As described earlier, the pole trajectory is identical in both compensation schemes.

It appears so far that either scheme will produce the desired results. However, in practice this is not the case. From the standpoint of circuit implementation, it is impossible to introduce a left half-plane zero without either adding additional stray poles or loading down the already existing poles. The effects of these second order non-idealities on the root loci need to be investigated in order to determine the best compensation scheme.

To simplify the analysis, it is assumed that the zero insertion creates a single stray high frequency pole s_s which is located beyond the zero z_0. Then, the zero block in Fig. 3.6 becomes $\frac{1 + \frac{s}{z_0}}{1 + \frac{s}{s_s}}$ instead of $1 + \frac{s}{z_0}$. For a two-pole amplifier block, the resulting closed loop transfer functions are



ZERO IN FORWARD PATH



ZERO IN FEEDBACK PATH

Figure 3.7
Root Loci of Forward and Feedback Path Compensated Amplifier

$$H_{forward}(s) = \frac{a_0\left(1+\frac{s}{z_0}\right)}{\left(1+\frac{s}{s_p}\right)\left(1+\frac{s}{s_l}\right)\left(1+\frac{s}{s_s}\right)+a_0 f_0\left(1+\frac{s}{z_0}\right)} \tag{3.13}$$

$$H_{feedback}(s) = \frac{s_0}{\left(1+\frac{s}{s_p}\right)\left(1+\frac{s}{s_l}\right)\left(1+\frac{s}{s_s}\right)+a_0 f_0\left(1+\frac{s}{z_0}\right)}. \tag{3.14}$$

The root loci are plotted in Fig. 3.8. Since the loop gain expressions are identical for both, the root loci are also the same. The presence of the stray high frequency pole s_s can prevent the complex pole pair from traveling in a circular path. Therefore, it is paramount that s_s be moved to a remote location. If the pole s_s is pushed out far enough, a root locus, as shown in Fig. 3.9, results. Here, the stray high frequency pole is located at far enough distance such that its effect on the locus at moderate loop gain is negligible. However, for very large loop gain, a second complex pole pair can form. This type of frequency compensation has been used effectively to design wideband monolithic amplifiers [10].

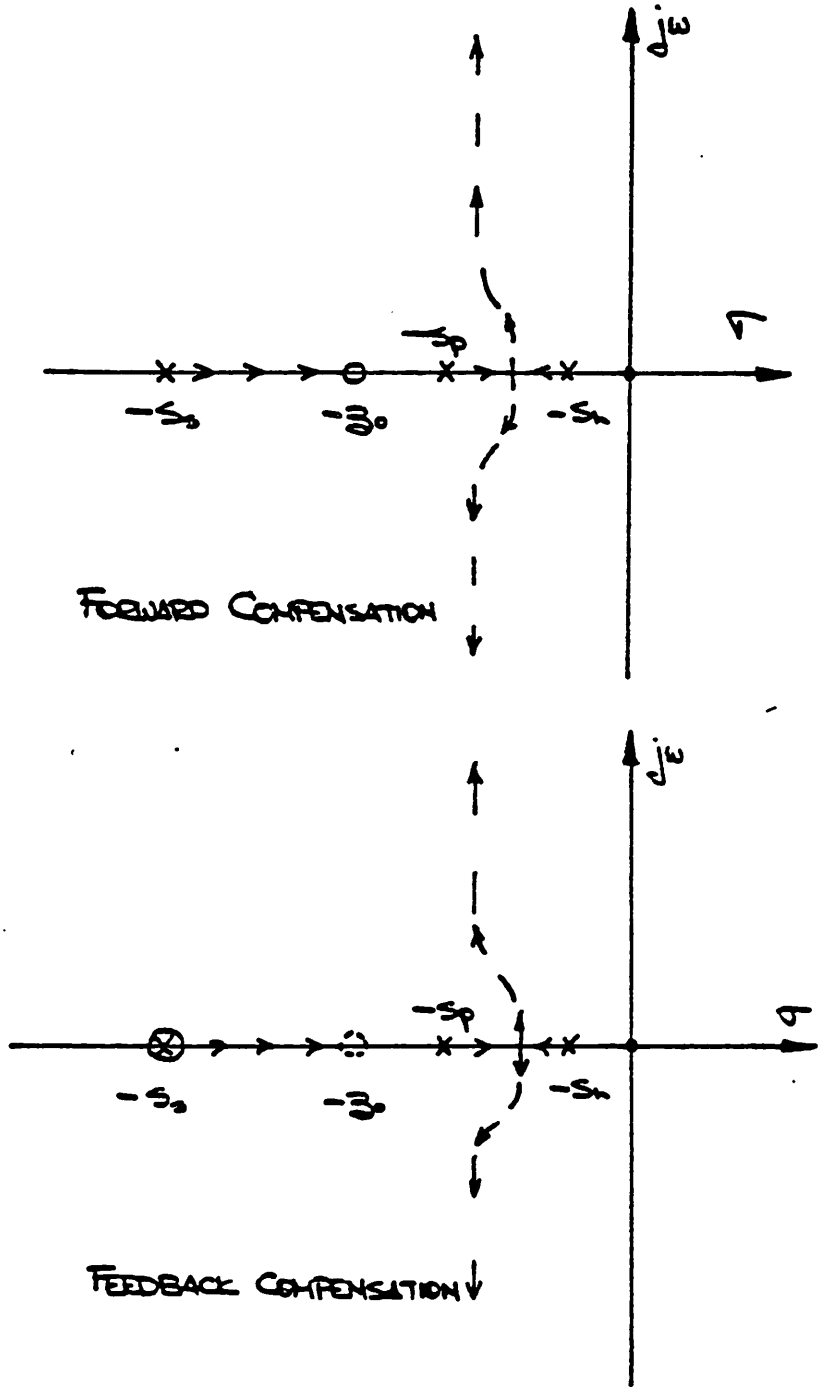
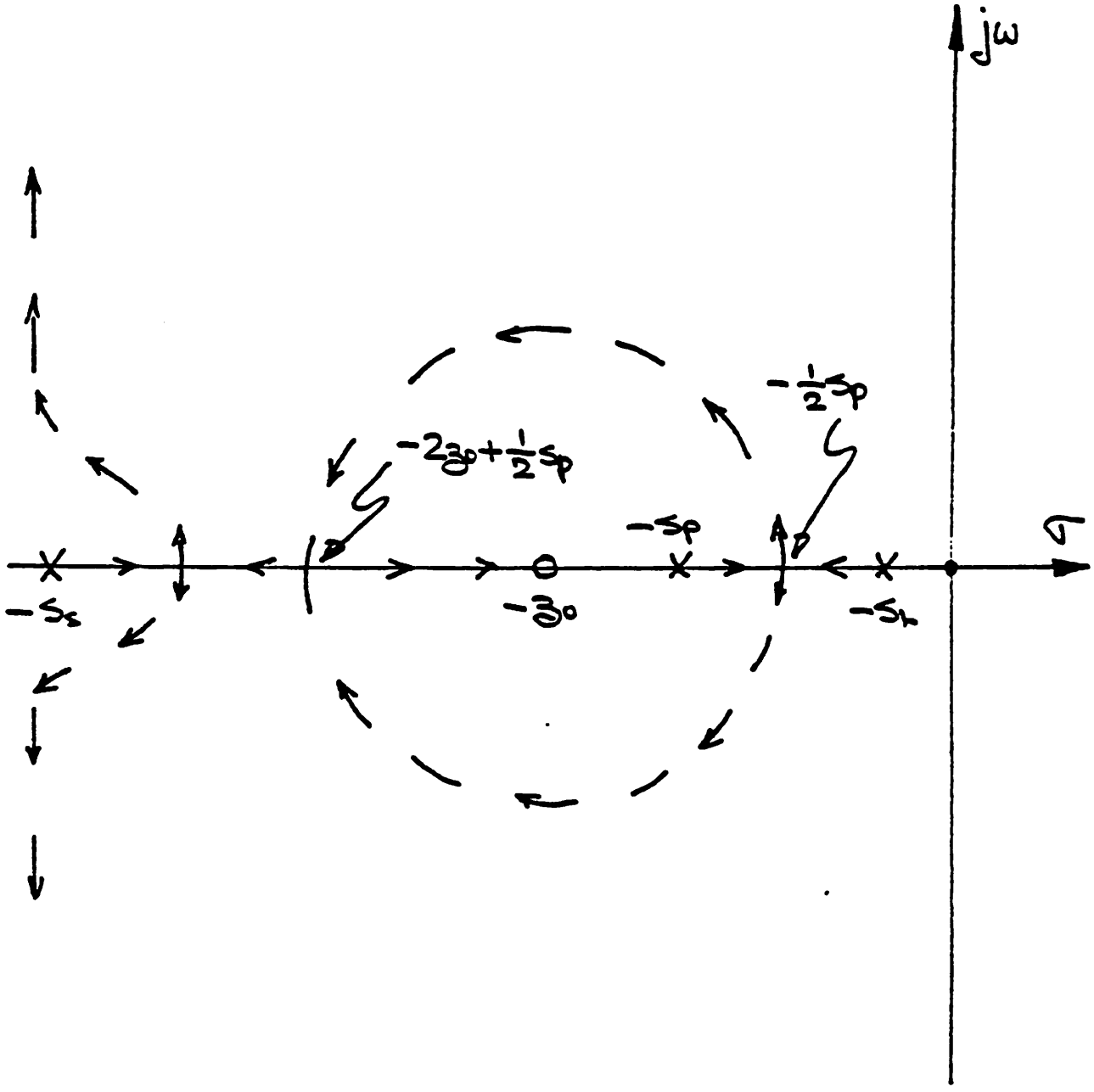


Figure 3.8
Root Loci of Three-Pole, One-Zero System


jω
σ
$-\frac{1}{2}s_p$
$-2z_0+\frac{1}{2}s_p$
$-s_p$
$-s_s$
$-z_0$
$-s_h$

3.2. The Switched-Capacitor Integrator

The frequency compensation or the time response tailoring scheme, described in the preceding section, applies primarily to feedback amplifiers that have unilateral signal paths. In general, signal is fed in both forward and reverse directions through any two port networks. It is generally assumed that the magnitude of the signal through the feedback network in the reverse direction is much larger than that in the forward direction. The validity of this assumption becomes questionable when the transconductance of the amplifier is small, which is the case for most MOS amplifiers [11]. A small signal equivalent representation of an LDI switched-capacitor integrator during the charge integration mode is shown in Fig. 3.10. The amplifier has been modeled as a frequency dependent transconductance block. The nodal equations are

$$V_e = \frac{C_s}{C_s + C_n + C_i} V_n + \frac{C_i}{C_s + C_n + C_i} V_o \tag{3.15}$$

$$V_o = \frac{sC_i - G_m}{sC_i + sC_l + G_l} V_e \ . \tag{3.16}$$

A block diagram of the feedback system that is represented by the above equations is shown in Fig. 3.11. The term $\frac{sC_i}{sC_i + sC_l + G_l} V_e$ in Eqn. 3.16 represents the signal that is fed forward through the feedback capacitor C_i. This signal can be neglected if it is small in comparison to $\frac{G_m}{sC_i + sC_l + G_l} V_e$, which is the signal amplified by the amplifier. For high frequency and high speed applications, this signal component cannot be ignored. It will be shown in the subsequent sections that this feedforward path can alter the response of the closed loop system.

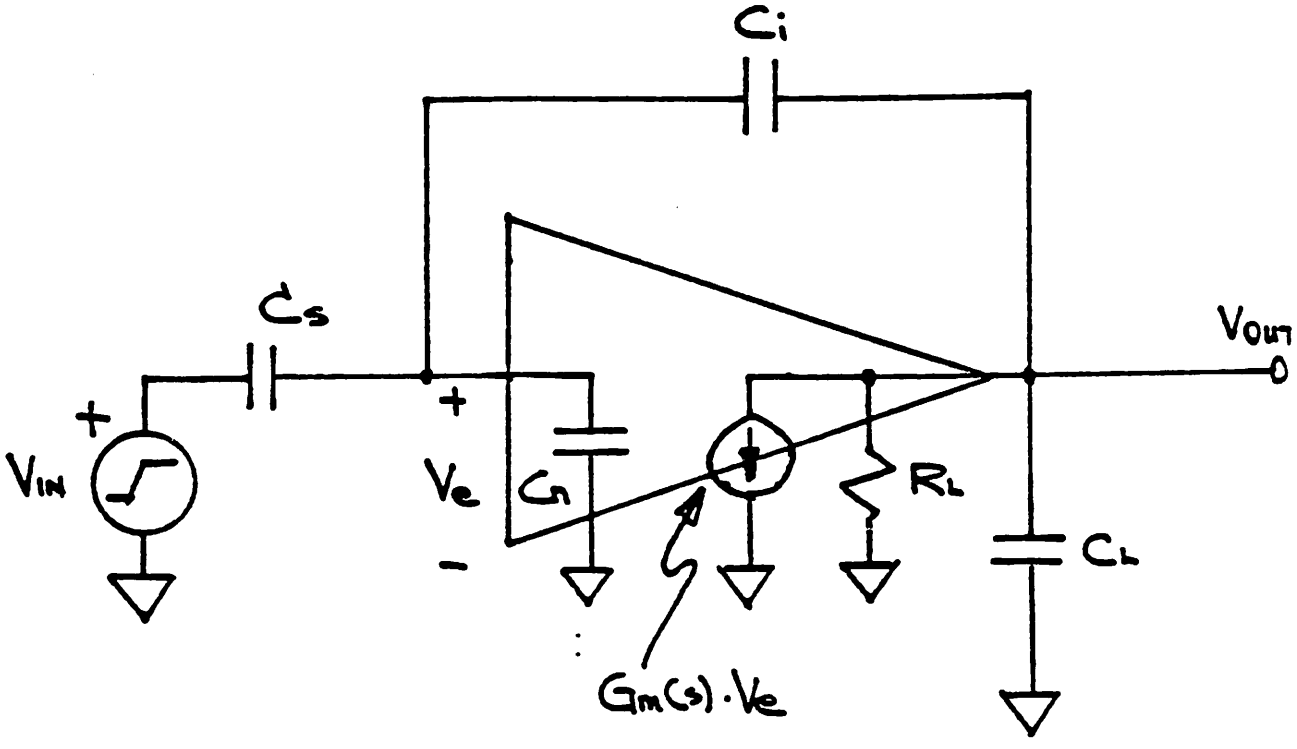


Figure 3.10
A Small Signal Equivalent Model
of the Switched-Capacitor Integrator

3.2.1. The Effects of the Feedforward Path

The loop gain expression for an LDI switched-capacitor integrator during the charge integration mode is given below.

$$A_{loop}(s) = \frac{C_i}{C_s + C_n + C_i} \frac{sC_i - G_m}{sC_i + sC_l + G_l} . \tag{3.17}$$

The feedforward path through the feedback capacitor C_i interacts with the amplifier to produce a real right-half plane zero at $\frac{G_m}{C_i}$. The presence of this zero can potentially cause instability. The closed loop pole location is given by

$$s = -A_0 s_l \frac{1}{1 - \frac{A_0 s_l}{z_f}} \tag{3.18}$$

where

$s_l = \frac{1}{R_l\left[C_i + C_l\right]}$ is the dominant pole,

$z_f = \frac{G_m}{C_i}$ is the feedforward right half-plane zero, and

$A_0 = \frac{C_i}{C_s + C_n + C_i} \frac{G_m}{G_l}$ is the low frequency loop gain.

The system will be stable as long as $A_0 s_l$, which is approximately equal to the open loop unity gain frequency, is smaller in magnitude than z_f. Therefore, it is paramount that z_f is kept above the unity gain frequency.

3.2.2. The Effects of Feedforward Path on Two-Pole Systems

Almost all amplifiers can be accurately modeled as a two-pole system. By replacing the voltage controlled current source G_m by $G_m \frac{1}{1 + \frac{s}{s_p}}$, the small sig-

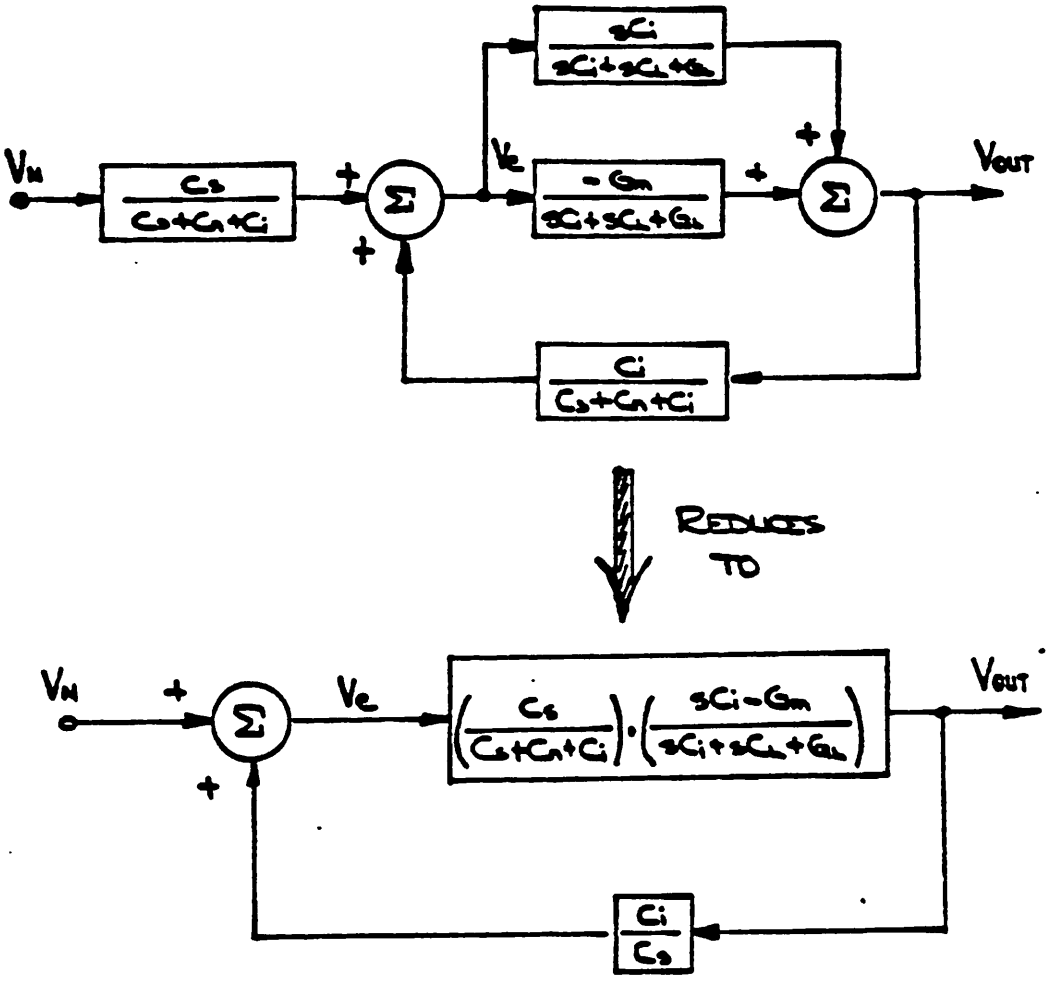


Figure 3.11
Block Diagram of the Switched-Capacitor Integrator

nal model of the switched-capacitor integrator (Fig. 3.10) becomes a two-pole system. s_p represents the high frequency, non-dominant pole that is inherent to the amplifier. The loop gain and the closed loop transfer function expressions are given below:

$$A_{loop} = a_o f_o \frac{\frac{s}{z_f}\left[1 + \frac{s}{s_p}\right] - 1}{\left[1 + \frac{s}{s_l}\right]\left[1 + \frac{s}{s_p}\right]} \tag{3.21a}$$

$$H(s) = -\frac{C_s}{C_i} \frac{\frac{s}{z_f}\left[1 + \frac{s}{s_p}\right] - 1}{\left[1 + \frac{s}{s_l}\right]\left[1 + \frac{s}{s_p}\right] - a_o f_o\left\{\frac{s}{z_f}\left[1 + \frac{s}{s_p}\right] - 1\right\}} \tag{3.21b}$$

where the terms are defined as follows:

$a_o f_o = G_m R_l \frac{C_i}{C_n + C_s + C_i}$ is the low frequency loop gain;

$s_l = \frac{1}{R_l\left(C_i + C_l\right)}$ is the dominant pole;

$z_f = \frac{G_m}{C_i}$ is the real right-half plane zero attributed to the feedforward path; and

s_p is the high frequency, non-dominant pole internal to the amplifier.

Under moderate amount of loop gain, the poles form a complex pair. Then, Eqn. 3.21b can be re-expressed in the following form:

$$H(s) = -\frac{C_s}{C_i} \frac{\left[1 + \frac{s}{z_l}\right]\left[1 - \frac{s}{z_r}\right]}{\frac{s^2}{\omega_n^2} + 2\frac{\sigma}{\omega_n^2}s + 1} \tag{3.22}$$

where the terms are defined as follows:

$z_l = -\frac{1}{2}s_p - \sqrt{s_p z_f}$ is the real left-half plane zero;

$z_r = -\frac{1}{2}s_p + \sqrt{s_p z_f}$ is the real right-half plane zero;

$$\frac{1}{\omega_n^2} = \frac{1}{s_p}\left\{-\frac{1}{z_f} + \frac{1}{a_o f_o s_l}\right\}; \text{ and}$$

$$\frac{2\sigma}{\omega_n^2} = \frac{1}{a_o f_o}\left\{\frac{1}{s_p} + \frac{1}{s_l}\right\} - \frac{1}{z_f}.$$

The loop gain (Eqn. 3.21a) and the closed loop transfer function expressions (Eqn. 3.21b) now contain both a left-half and a right-half zero. If the feedforward path is eliminated in Fig. 3.11, then both of these zeroes disappear from the expressions. The zeroes are symmetrically located about the break-away point $-\frac{1}{2}s_p$ of the complex pole pair and are spaced apart by $\sqrt{s_p z_f}$ which is the geometric mean of the non-dominant pole and the feedforward zero frequencies. Since the right-half zero is lower in frequency than the left-half zero, the complex pole pair will eventually cross over into the right-half plane. The criterion for stability is determined by examining the real part of the complex pole pair σ

$$\sigma = -\frac{1}{2}s_p \frac{\frac{1}{a_o f_o}\left\{\frac{1}{s_p} + \frac{1}{s_l}\right\} - \frac{1}{z_f}}{\frac{1}{a_o f_o s_l} - \frac{1}{z_f}}. \tag{3.23}$$

When the numerator becomes zero, the poles lie on the imaginary axis. This occurs when

$$a_o f_o s_l \approx z_f \tag{3.24}$$

or simply when the right-half plane feedforward zero falls below the single-pole, closed loop corner frequency $a_o f_o s_l$. For a transconductance amplifier in an unity gain feedback configuration, Eqn. 3.24 becomes

$$\frac{C_i + C_l}{G_m} > \frac{C_i}{G_m}. \tag{3.25}$$

As long as some parasitic capacitance loads down the amplifier, the stability of a two-pole transconductance amplifier is guaranteed.

3.2.3. The Effects of Feedforward Path on Two-Pole, One-Zero Systems

It has been shown in section 3.1.3 that a two-pole amplifier that is compensated with a real left-half plane zero will yield the most controllable transient response. Unfortunately, the analysis was performed for an ideal feedback system with no feedforward path through the feedback network. In this section, the two-pole, one-zero feedback system is re-examined by taking the effects of the feedforward path into account.

First, a feedback system with a left-half zero incorporated in the forward gain path of the amplifier is examined. The transconductance G_m in Fig. 3.11 is now replaced by $G_m \dfrac{1 + \dfrac{s}{z_o}}{1 + \dfrac{s}{s_p}}$ where s_p is the sole high frequency, non-dominant pole and z_o is the open loop left-half zero. The loop gain and the closed loop transfer function expressions are:

$$A_{loop} = a_o f_o \frac{\dfrac{s}{z_f}\left[1 + \dfrac{s}{s_p}\right] - \left[1 + \dfrac{s}{z_o}\right]}{\left[1 + \dfrac{s}{s_l}\right]\left[1 + \dfrac{s}{s_p}\right]} \tag{3.26a}$$

$$H(s) = -\frac{C_s}{C_i} \frac{\dfrac{s}{z_f}\left[1 + \dfrac{s}{s_p}\right] - \left[1 + \dfrac{s}{z_o}\right]}{\left[1 + \dfrac{s}{s_l}\right]\left[1 + \dfrac{s}{s_p}\right] - a_o f_o \left\{\dfrac{s}{z_f}\left[1 + \dfrac{s}{s_p}\right] - \left[1 + \dfrac{s}{z_o}\right]\right\}} \tag{3.26b}$$

where the terms are defined as follows:

$a_o f_o = G_m R_l \dfrac{C_i}{C_s + C_n + C_i}$ is the low frequency loop gain;

$s_l = \dfrac{1}{R_l\left(C_i + C_l\right)}$ is the dominant pole;

$z_f = \dfrac{G_m}{C_i}$ is the real right-half plane zero;

z_o is the real left-half plane zero within the amplifier; and

s_p is the high frequency, non-dominant pole.

The numerator of the loop gain expression determines the location of the closed loop zeroes.

$$N(s) = s^2 + s\left\{s_p\left[1 - \frac{z_f}{z_o}\right]\right\} - z_f s_p \cdot \tag{3.26c}$$

The open loop left-half zero z_o dictates the closed loop zero locations. If $z_o \gg z_f$, the closed loop zeroes approach those of the two-pole feedback system. We are interested in the case in which $s_p < z_o < z_f$. If this criterion is satisfied, the closed loop zeroes are approximately given by

$$z_r \approx + z_f \frac{s_p}{z_o} \text{ and}$$

$$z_l \approx= - z_o.$$

Under this condition, the pole trajectory of the complex pair is tightly controlled by the closed loop left-half plane zero z_l. The closed loop transfer function can now be expressed as

$$H(s) = - \frac{C_s}{C_i} \frac{\left[1 + \frac{s}{z_r}\right]\left[1 + \frac{s}{z_l}\right]}{\frac{s^2}{\omega_n^2} + 2\frac{\sigma}{\omega_n^2}s + 1} \cdot \tag{3.27}$$

The terms are defined as follows

$z_r = + z_f \frac{s_p}{z_o}$ is the closed loop right-half plane zero;

$z_l = - z_o$ is the closed loop left-half plane zero;

$\frac{1}{\omega_n^2} = \frac{1}{s_p}\left\{- \frac{1}{z_f} + \frac{1}{a_o f_o s_l}\right\}$; and

$2\frac{\sigma}{\omega_n^2} = \frac{1}{a_o f_o}\left\{\frac{1}{s_p} + \frac{1}{s_l}\right\} + \frac{1}{z_o} - \frac{1}{z_f}$

The real part of the complex pole pair is given by

$$\sigma = -\frac{1}{2}s_p\left\{1 - \frac{a_0 f_0 s_p + z_0}{a_0 f_0 s_l - z_f}\frac{s_l z_f}{s_p z_0}\right\} \tag{3.28a}$$

$$\approx -\frac{1}{2}s_p\left\{1 + \frac{a_0 f_0 s_l}{z_0}\right\} \tag{3.28b}$$

which is valid as long as $\frac{1}{4}s_p < a_0 f_0 s_l < 4\frac{z_0^2}{s_p}$ and if $z_f > a_0 f_0 s_l$.

In order for the system to be stable and well-behaved, the following conditions must be satisfied.

1. $a_0 f_0 s_l < z_f$, and

2. $z_0 < z_f$.

If the above requirements are met, the effects of the feedforward path become minimal. Then, the compensation scheme that was described in section 3.1.3 can be utilized directly. Note that as long as $a_0 f_0 s_l < z_f$, the system is unconditionally stable, even if $z_f < z_0$. However, the closed loop zeroes are no longer given by $+ z_f \frac{s_p}{z_0}$ and $- z_0$. Because of this, the poles now follow a completely different trajectory. Note that when $z_0 \gg z_f$, the root locus asymptotically approaches that of the two-pole feedback system.

Another viable method to tailor the transient response involves the insertion of a left-half zero through the feedback path. A block diagram of such a system is depicted in Fig. 3.12. The feedforward path through the feedback network has been merged together with the forward gain path of the amplifier. The admittance of the feedback network is designated as Y_f. If a zero is introduced in the loop gain expression via Y_f, two additional poles appear. Although these nondominant poles are at high frequencies, they are sufficiently close to the zero such that the desired circular root locus can not be attained. The situation gravi-

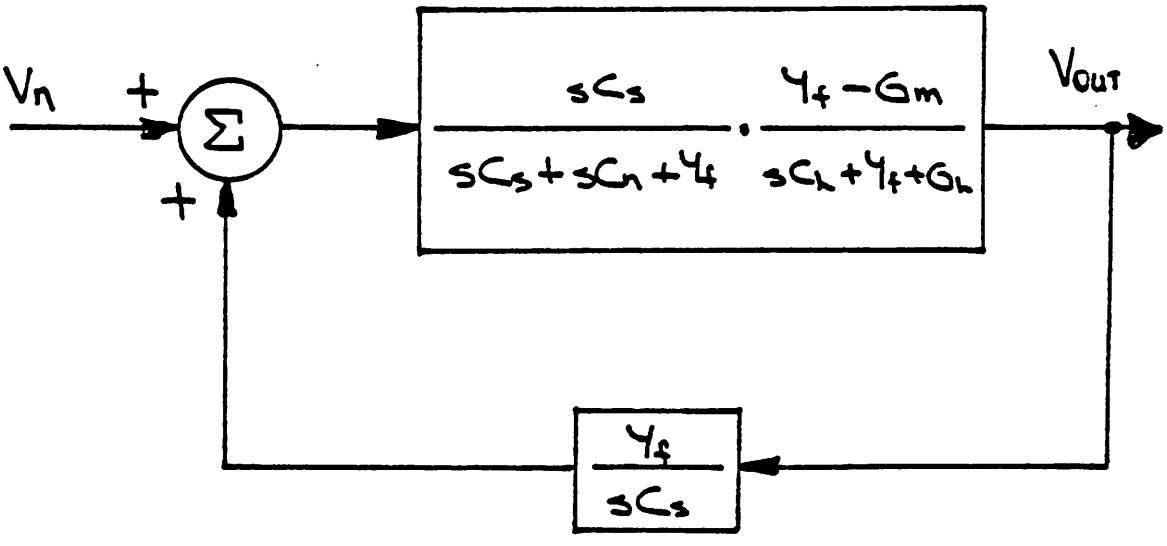


Figure 3.12
Zero Insertion Through the Feedback Network

tates when the amplifier is assumed to contain an internal non-dominant pole. Now the closed loop system is characterized as a four-pole system—one dominant pole and three high frequency poles which are all in the vicinity of the zero. Under this condition, it is extremely difficult to design a controllable feedback system.

To demonstrate this point, qualitative sketches of two possible root loci are shown in Fig. 3.13.

3.3. Theoretical Limit of Maximum Attainable Bandwidth

So far in this chapter, we have described and analyzed a frequency compensation scheme that yields a fast and well-behaved step response. For a given set of open loop parameters of an amplifier, what is the maximum attainable bandwidth (speed) that is theoretically possible? An attempt will be made to shed some light to this question.

As mentioned earlier, most amplifiers can be accurately characterized as a second order system. The parameters that describe such amplifiers are

s_l the dominant pole;

s_p the lowest non-dominant pole;

z_o the left-half plane zero; and

a_o the open loop low frequency gain.

In a closed loop configuration, the denominator of the transfer function can be generally expressed in the following form:

$$D(s) = \frac{s^2}{\omega_n^2} + 2\frac{\sigma}{\omega_n^2}s + 1 \cdot \tag{3.29}$$

The coefficients of the polynomial for the two-pole and for the two-pole, one-zero feedback systems are given below.

Two-Pole System

$$\frac{1}{\omega_n^2} \approx \frac{1}{s_p}\frac{1}{a_o f_o s_l} \tag{3.30a}$$

$$|\sigma| \approx \frac{1}{2}s_p \tag{3.30b}$$

Two-Pole, One-Zero System

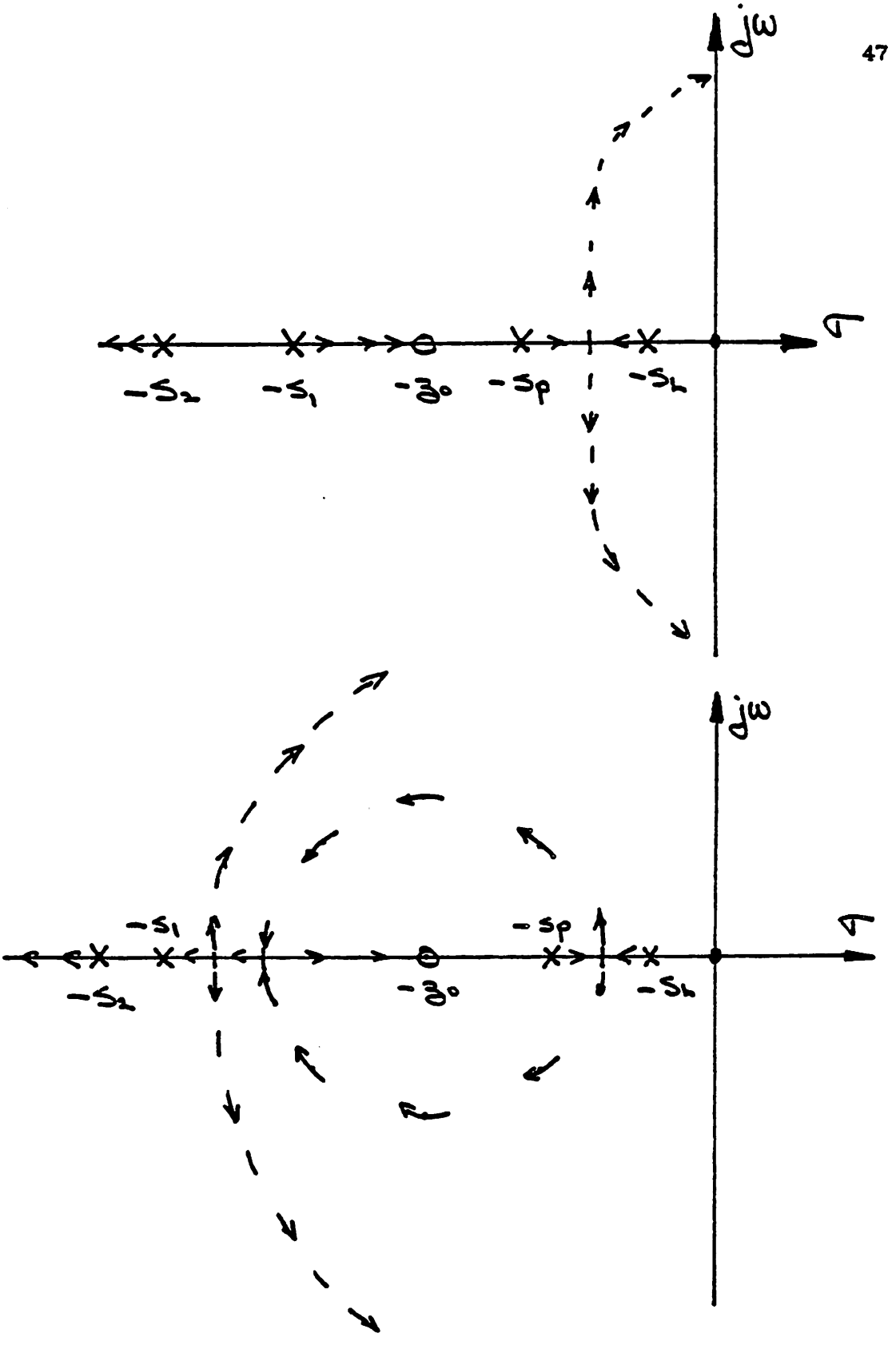


Figure 3.13
Root Loci of the Four-Pole Closed Loop System

$$\frac{1}{\omega_n^2} \approx \frac{1}{s_p}\frac{1}{a_o f_o s_l} \tag{3.30c}$$

$$|\sigma| \approx \frac{1}{2}s_p\left\{1 + \frac{a_o f_o s_l}{z_o}\right\}. \tag{3.30d}$$

In both systems, if $a_o f_o s_l$ is greater than $\frac{1}{4}s_p$, the poles become complex. Then, ω_n is the magnitude of the complex pole, and σ represents its real part. An example is illustrated in Fig. 3.14. To obtain a stable and well-behaved system, the open loop feedforward right-half zero z_f must satisfy the following constraints:

$$z_f > a_o f_o s_l \text{ and } z_f > z_o.$$

Eqns. 3.30a through 3.30d contain a wealth of important information.

1. ω_n is a fixed quantity for a given loop gain $a_o f_o$. If the poles are negative and real, their geometric mean is *always* equal to ω_n. If the poles are complex, their magnitude is also **always** equal to ω_n. In such a case, increasing the real part σ, decreases the imaginary part ω_p. Therefore, increasing the speed (large σ) lowers the Q of the poles. This is exactly what is done by the zero insertion compensation.

2. To design for maximum bandwidth and speed, both the open loop unity gain frequency $a_o s_l$ *and* the non-dominant pole frequency s_p should be maximized.

3. The single-pole, closed loop corner frequency $a_o f_o s_l$ must be in excess of $\frac{1}{4}s_p$ to force the formation of the complex pole pair. If $a_o f_o s_l < \frac{1}{4}s_p$, it is advised not to insert the zero. The zero compensation improves the system response only when the loop gain is sufficient to form a complex pole pair. Otherwise, the zero degrades the step response of the system.

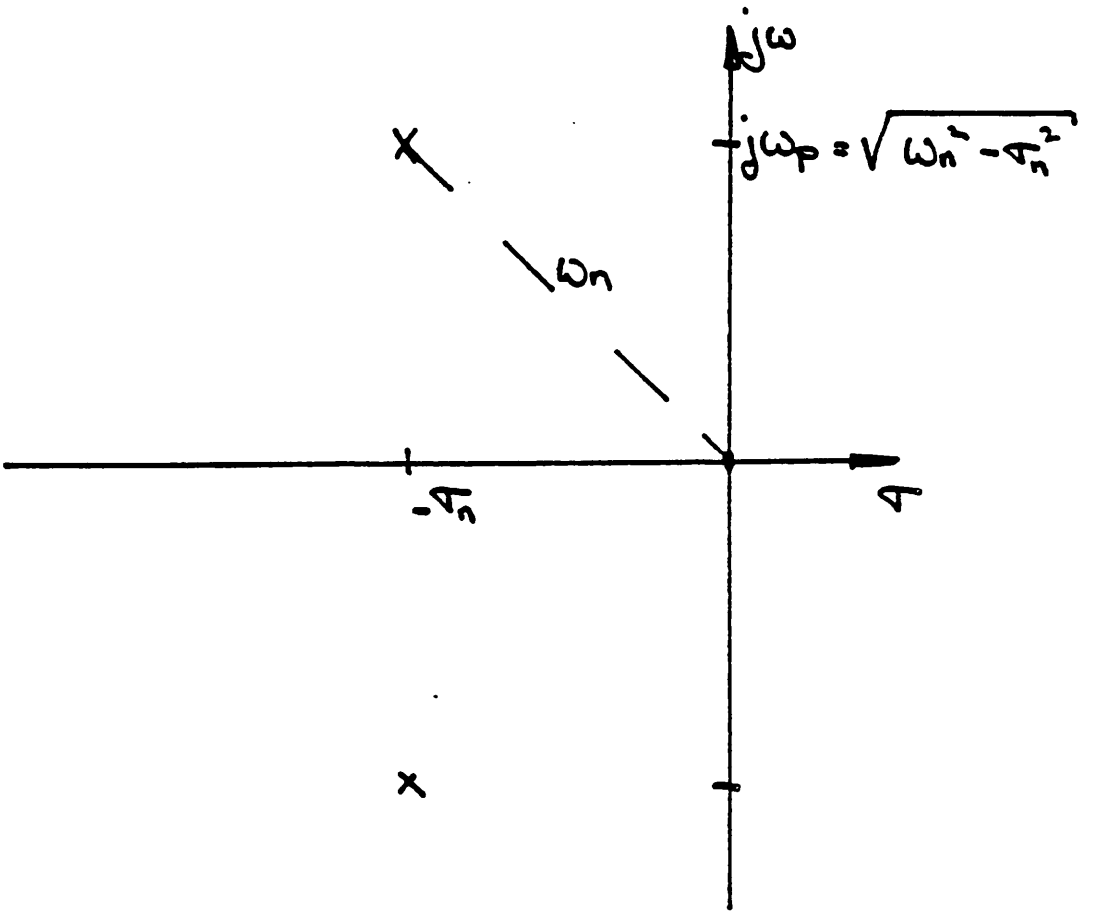


Figure 3.14
Complex Pole Pair in the S-Plane

4. To reap the full benefits of the zero insertion compensation, the open loop zero z_o must be located beyond, but as close to s_p as possible. Under such condition, the real part of the complex pole is at its maximum for the given loop gain. Furthermore, the Q of the complex pole pair is guaranteed to be

less than unity. The real part is

$$|\sigma| \approx \frac{1}{2}s_p + \frac{1}{2}a_o f_o s_l.$$

The results of the analysis are recapitulated in Table 3.1.

Criteria for stability and controllability

$$z_f > a_o f_o s_l \text{ and}$$

$$z_f > z_o$$

MAXIMUM USABLE BANDWIDTH	
Two-Pole System	$\frac{1}{2}s_p$ *if* $a_o f_o s_l \geq \frac{1}{4}s_p$ $a_o f_o s_l$ *if* $a_o f_o s_l < \frac{1}{4}s_p$
Two-Pole, One-Zero System	$\frac{1}{2}s_p + \frac{1}{2}a_o f_o s_l$ *if* $a_o f_o s_l \geq \frac{1}{4}s_p$ $\frac{1}{2}a_o f_o s_l$ *if* $a_o f_o s_l < \frac{1}{4}s_p$

Table 3.1
Maximum Bandwidth for Two-Pole and Two-Pole, One-Zero Systems

CHAPTER 4

THE SELECTION OF AMPLIFIER TOPOLOGY

In chapter 2 the conditions that are necessary to design a fast and well-behaved amplifiers were determined. In this chapter the results of this investigation are used to explore the trade-offs that are involved in the design of high speed integrators for switched-capacitor filters. An amplifier topology that is best suited for such an application is presented.

4.1. Performance Requirements of the Amplifier

The fast settling amplifiers that are used to implement high frequency and high selectivity switched-capacitor filters must satisfy the following requirements.

1. a_o, the minimum open loop gain. This is dictated by the gain stability and the selectivity Q of the filter.
2. $a_o s_l$, the minimum gain-bandwidth product. This is one of the parameter that determines the closed loop bandwidth.
3. s_p, the minimum frequency location of the first non-dominant pole. s_p, in conjunction with $a_o s_l$, sets the maximum attainable closed loop bandwidth and speed. The clock frequency and the required selectivity of the filter dictate the minimum frequency of s_p.
4. G_m, the minimum transconductance of the amplifier. Although G_m affects the gain and the bandwidth, the primary concern in switched-capacitor applications is the stability. $\frac{G_m}{C_i}$ must exceed $a_o f_o s_l$ at all times.

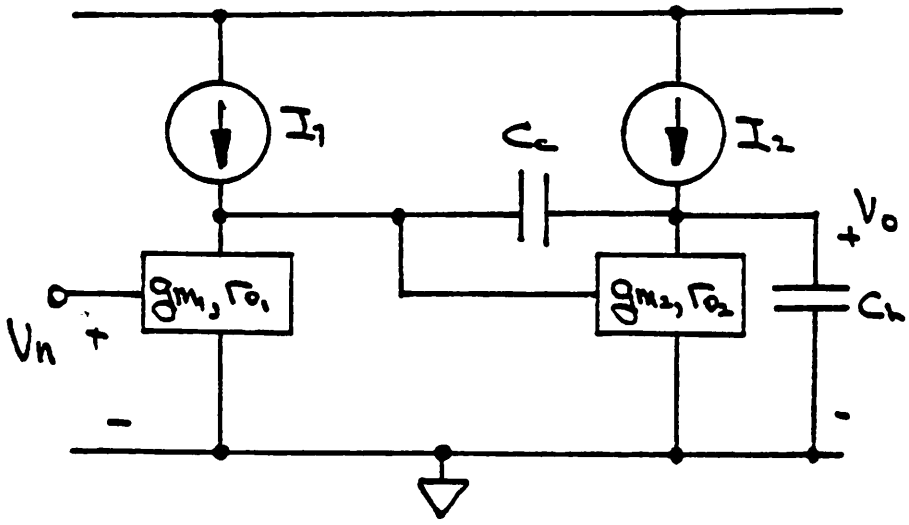
5. SR, the minimum slew rate. The slew rate along with the maximum load capacitance sets the minimum bias current requirement for the amplifier.

4.2. Single-Stage and Two-Stage Amplifiers

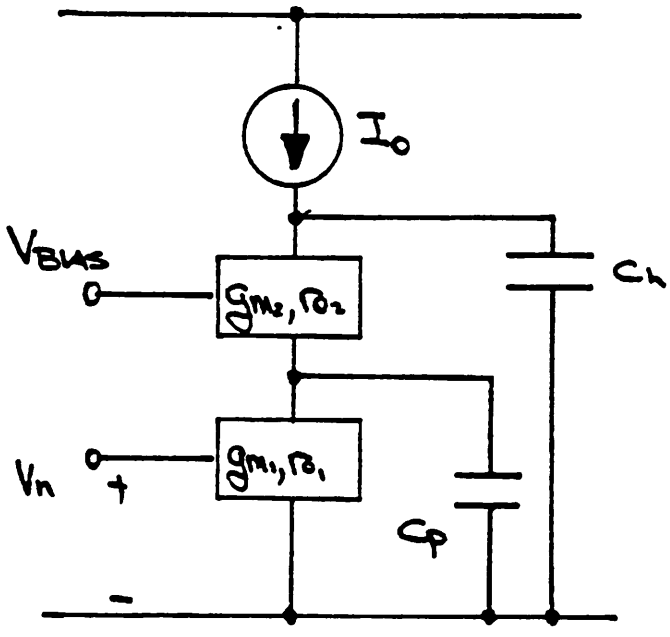
In order to attain high speed operation, the number of poles of the amplifier must be kept to a minimum. Preferably, there should be no more than two poles. This restriction limits the possible amplifier topologies to a single-stage or a two-stage design. A very general representation of the two topologies are presented in Fig. 4.1. The three terminal small-signal model of the active devices are characterized by a transconductance of g_m and an output resistance of r_o. For the sake of simplicity, all load elements are assumed to be perfect loads and are depicted as ideal current sources.

The two-stage amplifier, which drives a capacitive load of C_l, consists of a cascade of two inverters. To guarantee stability, a Miller capacitor C_c frequency compensates the amplifier. The dominant pole s_l appears at the output node of the first stage, and is equal to $\frac{1}{r_{o1}\left\{g_{m2}r_{o2}C_c\right\}}$. The sole non-dominant pole s_p, due to the interaction between the load capacitor C_l and the transconductance of the second stage, is given by $\frac{g_{m2}}{C_l}$. The low frequency gain is $\left\{g_{m1}r_{o1}\right\}\left\{g_{m2}r_{o2}\right\}$ which is the product of the gain of the two stages. The gain-bandwidth product is $\frac{g_{m1}}{C_c}$. To be consistent with the notation used in Chapter 2, the low frequency gain is denoted as a_o, the dominant pole as s_l, the non-dominant pole as s_p, and the gain-bandwidth product as $a_o s_l$.

The single-stage cascode is composed of the driver D_1, the cascode device D_2, and an ideal current source as the load. It drives a capacitive load C_l which also acts as the compensation capacitor. C_p is the lumped parasitic capacitance present at the low impedance cascode node. The dominant pole, which appears at the output node, is approximately equal to $\frac{1}{\left\{r_{o2}g_{m2}r_{o1}\right\}C_l}$. The sole non-dominant



TWO-STAGE AMPLIFIER



SINGLE-STAGE AMPLIFIER

Figure 4.1
Single-Stage and Two-Stage Amplifier Topologies

pole at the cascode node is given by $\frac{g_{m2}}{C_l}$. The low frequency gain is described by the following relationship

$$a_o = -\left\{g_{m1}\left[r_{o1} // \frac{1}{g_{m2}}\left\{1 + \frac{R_l}{r_{o2}}\right\}\right]\right\}\left\{g_{m2}\left[r_{o2} // R_l\right]\right\} \tag{4.1}$$

where R_l is the output resistance of the current source load. If R_l is greater than the output resistance r_{o2} of the cascode, the gain expression reduces to

$$a_o \approx -\left\{g_{m1}r_{o1}\right\}\left\{g_{m2}r_{o2}\right\} . \tag{4.2}$$

This is the same overall gain as the two-stage amplifier. However, if $R_l < r_{o2}$, the gain is

$$a_o \approx -g_{m1}r_{o2} . \tag{4.3}$$

Thus, it is essential to make $R_l \gg r_{o2}$ to obtain a high gain. The gain-bandwidth product is $\frac{g_{m1}}{C_l}$.

To compare the performance of these two amplifiers, we will impose the following conditions: $C_c = C_l$, $C_p < C_c$, and $I_1 = I_2 = I_o$. This forces both amplifiers to have identical slew rates. The four key performance parameters are tabulated in Table 4.1.

PARAMETER	SINGLE-STAGE	TWO-STAGE
a_o, low frequency gain	$\left\{g_m r_o\right\}^2$	$\left\{g_m r_o\right\}^2$
s_l, dominant pole	$\frac{1}{\left\{r_o g_m r_o\right\} C_l}$	$\frac{1}{r_o \left\{g_m r_o C_l\right\}}$
s_p, non-dominant pole	$\frac{g_m}{C_p}$	$\frac{g_m}{C_l}$
$a_o s_l$, gain-bandwidth product	$\frac{g_m}{C_l}$	$\frac{g_m}{C_l}$

Table 4.1
The Performance of Single-Stage
and Two-Stage Amplifiers

The only difference between the single-stage and the two-stage amplifiers is the location of the non-dominant pole. In general, since $C_p < C_c$, the single-stage topology has a much higher frequency s_p than the two-stage. This is a very important consideration in light of the results presented in Chapter 2. For maximum speed and bandwidth, the product $a_o f_o s_l s_p$ must be maximized. Thus, it is clearly evident that the single-stage amplifier has the potential for high speed operation. The single-stage has another significant advantage over the two-stage. The non-dominant pole of the former is totally independent of any parameter external to the amplifier; while that of the latter is determined by C_l, the capacitive load of the amplifier. Thus, the closed loop performance of the former is very predictable and controllable.

4.3. Single-Stage Amplifiers

An MOS implementation of the single-stage cascode amplifier is shown in Fig. 4.2. The transistors M_1 and M_2 are the driver and the cascode devices, respectively. C_l is the capacitive load, and C_{p1} and C_{p2} represent the parasitic capacitance that are present at the cascode node. In this schematic, C_{p1} is the gate-to-

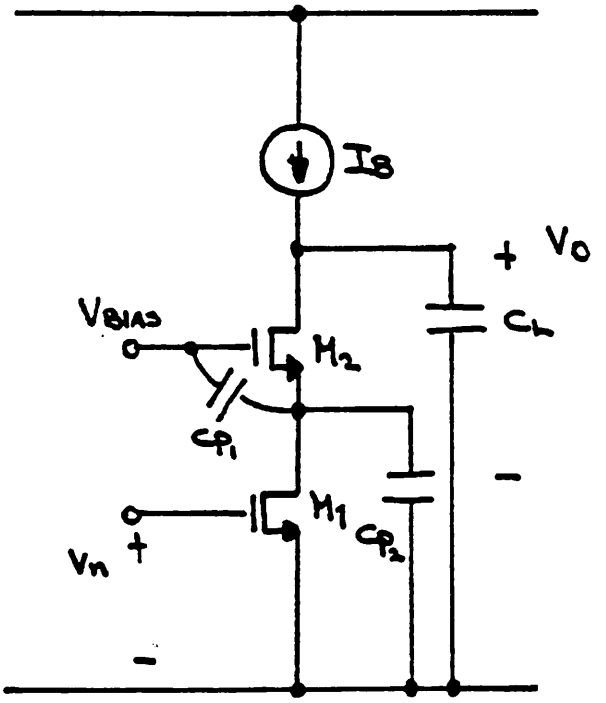


Figure 4.2
An MOS Single-Stage Cascode Amplifier

source capacitance of the cascode device, and C_{p2} is the junction capacitance of the diffusions of M_1 and M_2. Typically, C_{p1} overwhelms C_{p2}. Thus, the non-dominant pole s_p is approximately equal to $\frac{g_{m2}}{C_{gs2}}$, which is the f_T of the cascode device. If the amplifier is properly designed, its closed loop bandwidth can be made to approach and even exceed $\frac{1}{2}f_T$ of the cascode element.

The transconductance of MOSFETs is proportional to the square root of the bias current, and the output resistance is inversely proportional to the current. Therefore, the overall gain is inversely proportional to the current, and the non-dominant pole goes as the square root of the bias current. Thus, to design for high gain, the bias current must be kept low, but for high speed operation, it should be made as large as possible. These conflicting constraints make the design of high gain and high speed amplifiers very difficult. The basic limitation becomes clear when the amplifier in Fig. 4.2 is scrutinized. The slew rate and the capacitive load set the lower limit of the bias current. The minimum gain requirement, which is dictated by the filter, establishes the upper limit of the current. Staying within these two bounds, both the gain-bandwidth product and the non-dominant pole location must be maximized. In this configuration, since the same current source biases both the driver and the load devices, a_o, s_p, and $a_o s_l$ can not be controlled and optimized independently.

A very simple solution to this problem is shown in Fig. 4.3. In this configuration, an additional current source I_2 boosts the bias current flowing through the driver. Now, s_p and $a_o s_l$ can be independently optimized to obtain the desired gain and frequency characteristics.

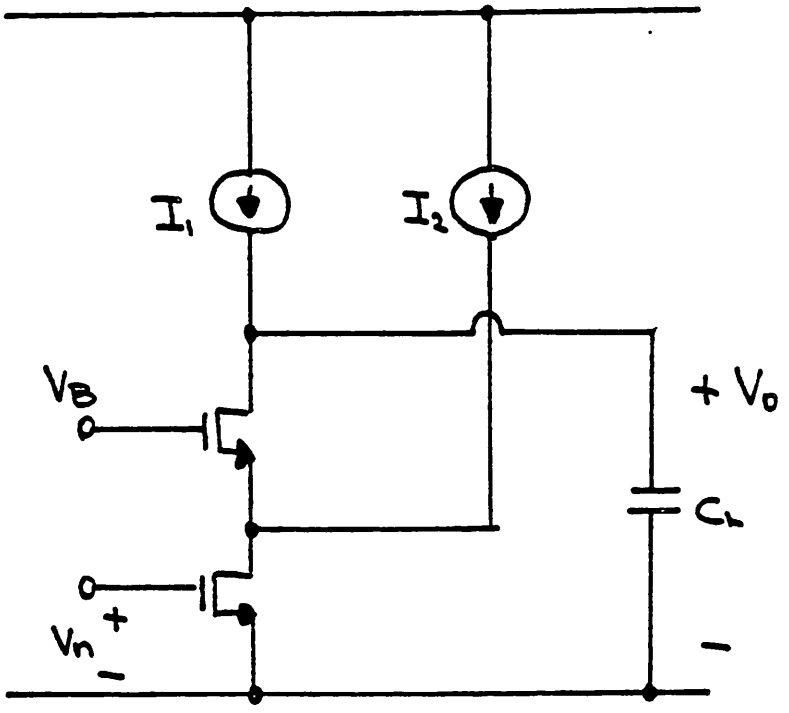


Figure 4.3
An Improved Single-Stage Cascode Amplifier

4.4. Current Mirroring and Current Steering Amplifiers

Two single-stage amplifiers that allow independent current control of the load and driver are shown in Fig. 4.4. The circuit in Fig 4.4a is dubbed a "current steering" circuit since the current is "steered" between the driver and the load. In the circuit depicted in Fig. 4.4b, the current is "mirrored" between the load

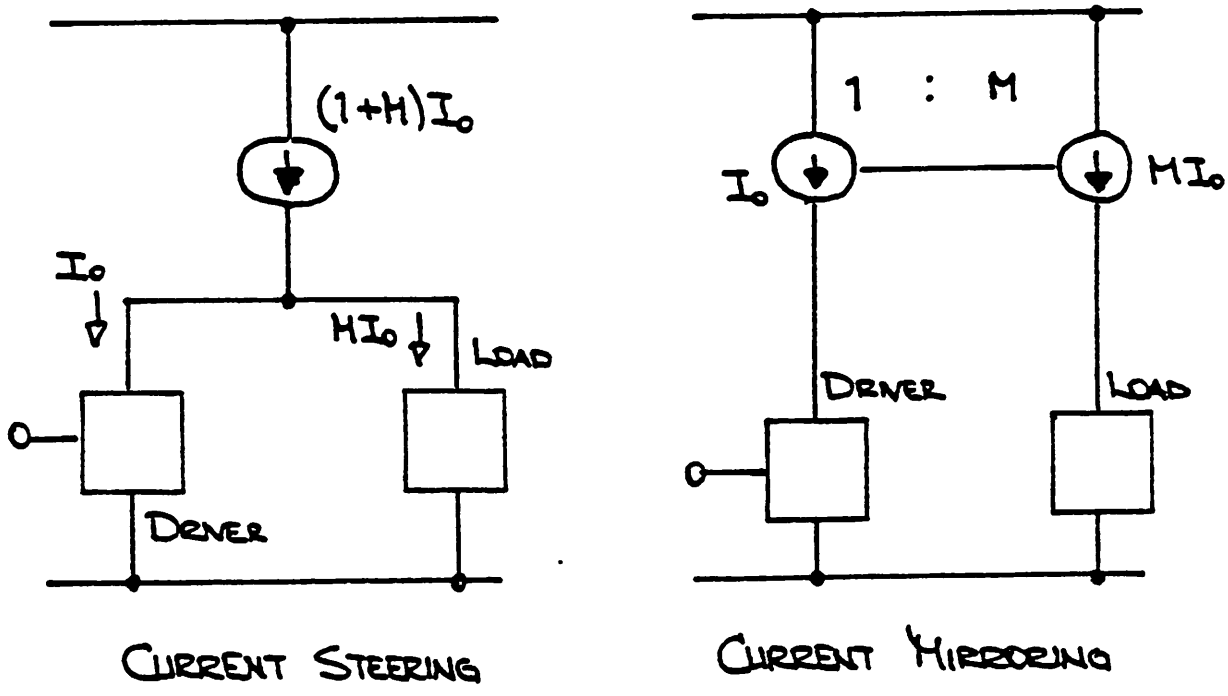


Figure 4.4
Current Steering and Current Mirroring Amplifiers

and the driver by means of a current mirror. The simplicity of these two topologies applies very well for very high speed operation.

The CMOS implementation of the current mirroring and the current steering amplifiers are shown in Figs. 4.5 and 4.6, respectively. Their differential mode, small-signal half-circuits are also shown. For both topologies, C_p is the total parasitic capacitance at node A, C_l is the load capacitance, and R_l is the

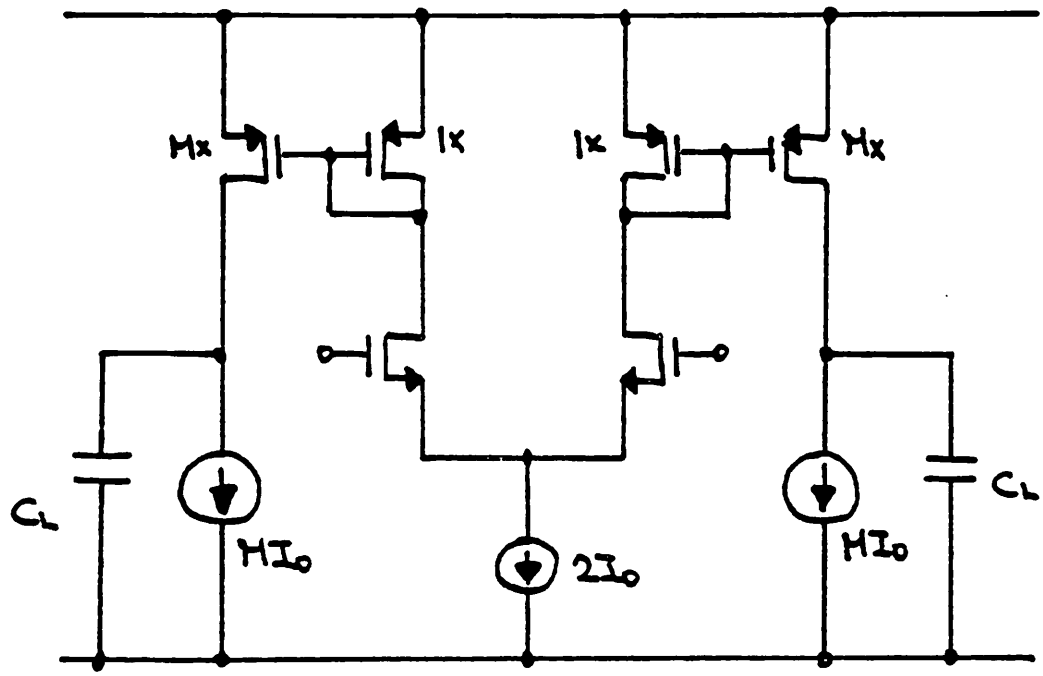


Figure 4.5
A CMOS Current Mirroring Amplifier

equivalent output resistance of the current source load. It is assumed that $R_l \gg r_{o2}$ and $R_l \gg r_{o3}$. The key performance parameters of both amplifiers are listed in Table 4.2.

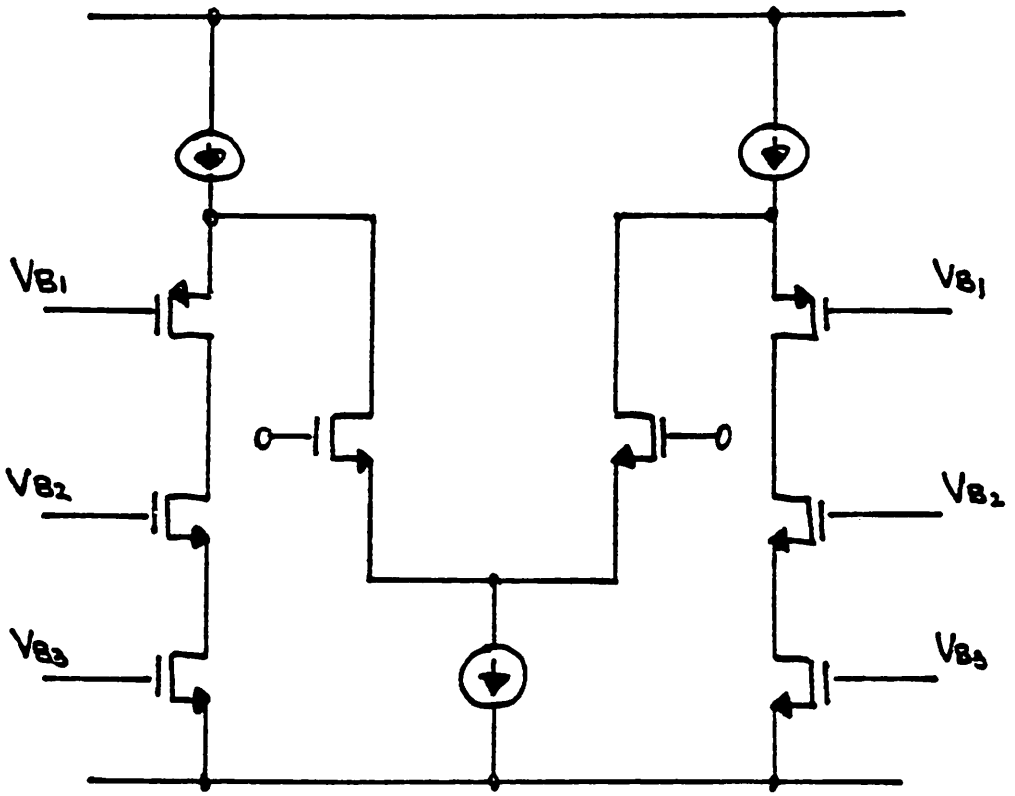


Figure 4.6
A CMOS Current Steering Amplifier

	CURRENT MIRRORING AMPLIFIER	CURRENT STEERING AMPLIFIER
a_o, open loop gain	$Mg_{m1}r_{o3}$	$g_{m1}r_{o1}\,g_{m2}r_{o2}$
s_l, dominant pole	$\frac{1}{r_{o3}C_l}$	$\frac{1}{C_l r_{o2} g_{m2} r_{o1}}$
$a_o s_l$, gain-bandwidth product	$M\frac{g_{m1}}{C_l}$	$\frac{g_{m1}}{C_l}$
s_p, non-dominant pole	$\frac{g_{m2}}{C_p}$	$\frac{g_{m2}}{C_p}$

Table 4.2
Performance Parameters of the Current Mirroring and the Current Steering Amplifiers

If the open loop gain is the only concern, both configurations can easily meet the minimum gain requirement. This is done by selecting the right bias currents for the driver and the load branches in manner similar to a two-stage amplifier design. The major difference between the two lies in the non-dominant pole location. If only the gate-to-source capacitance is considered, C_p of the current mirroring amplifier is equal to the sum of the gate-to-source capacitance of the current mirror M_2 and M_3, while C_p of the current steering amplifier is the gate-to-source capacitance of M_2. Therefore, the non-dominant pole of the latter is at a much higher frequency than that of the former. As a consequence, the current steering configuration exhibits a superior frequency and transient response.

4.5. The Folded-Cascode Amplifier

The current steering amplifier that is shown in Fig. 4.6 is a common-source, common-gate or a cascode amplifier. This amplifier is folded over at the cascode node giving it the alias of folded-cascode amplifier. In order to implement our experimental high frequency filters, a fully-differential version of the folded-cascode amplifier is required [1, 12]. In Fig. 4.7 a fully-differential version is shown. The high impedance current source loads are implemented by a pair of cascoded n-channel devices, M_1 through M_4. The p-channel current sources M_5 and M_6 provide the bias current for the amplifier. The proper apportioning of this current between the load and the driver branches is effected through the n-channel current sources M_{11}, M_3 and M_4. The ratio of the $\frac{W}{L}$ of M_3 and M_4 to M_{11} determines the load to driver current ratio.

4.5.1. Differential Mode Behavior

The differential mode half-circuit is shown in Fig. 4.8. To simply the analysis, the p-channel current sources M_5 and M_6 are represented as R_s which is their equivalent output resistance; the cascode current source loads M_1 through M_4 are modeled by R_l; and the output and the cascode node capacitive loads are shown as C_l and C_p, respectively.

Low Frequency Gain

The low frequency gain is given by the following expression

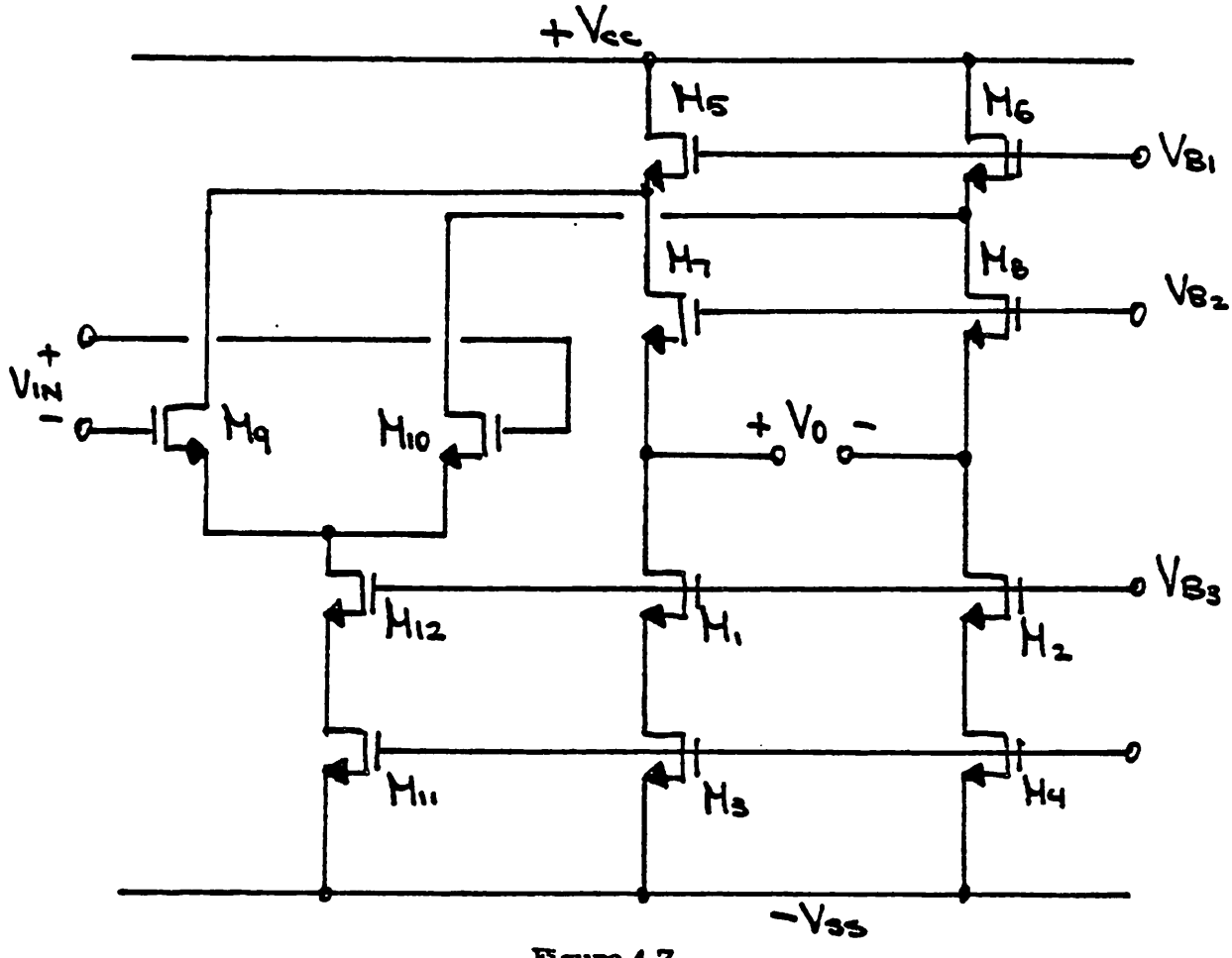


Figure 4.7
The Fully-Differential Folded-Cascode Amplifier

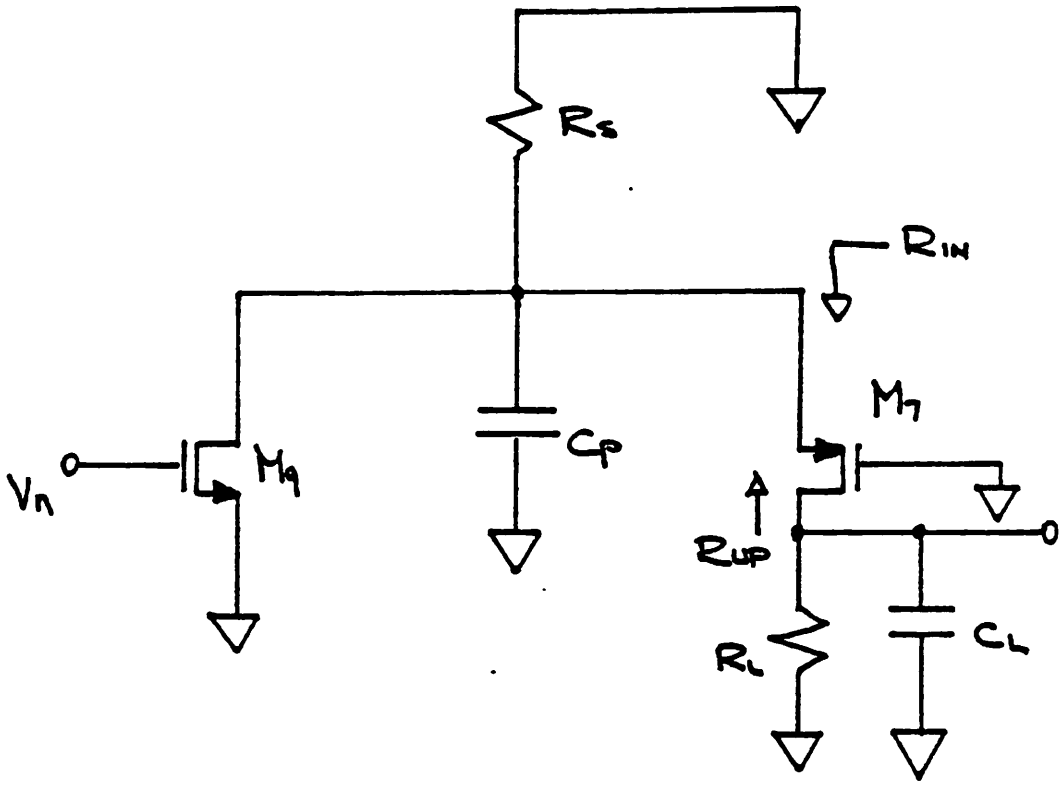


Figure 4.8
Differential Mode Half-Circuit

$$G = -\left\{g_{m9}\frac{G_{in}}{g_{o9} + G_s + G_{in}}\right\} R_l$$

$$R_l = r_{o2}\left\{1 + g_{m2}r_{o4}\right\} \qquad (4.4)$$

$$R_{in} = \frac{1}{G_{in}} = \frac{1}{g_{m7}}\left\{1 + \frac{R_l}{r_{o7}}\right\}$$

The terms are defined as follows:

g_{m9} is the transconductance of the input driver;

g_{o9} is the output conductance of the driver;

G_s is the output conductance of the p-channel current sources M_5 and M_6; and

$\frac{1}{G_{in}}$ is the incremental resistance seen looking into the source of the cascode element M_7.

It is interesting to note that R_{in} is larger than $\frac{1}{g_{m7}}$ when the load resistance R_l exceeds the output resistance r_{o7} of the cascode device. A re-arranged form of Eqn. 4.4 is shown below

$$G = -g_{m9}r_{o9}\,g_{m7}r_{o7}\left\{\frac{1}{1+\frac{r_{o9}}{R_s}+\frac{r_{o9}}{R_{in}}}\right\}\left\{\frac{1}{1+\frac{r_{o7}}{R_l}}\right\} \tag{4.5}$$

When $R_l \gg r_{o7}$, $R_{in} \gg r_{o9}$, and $R_s \gg r_{o9}$, the overall gain asymptotically approaches that of a two-stage amplifier. However, if $R_l < r_{o7}$ the gain drops to

$$G \approx -g_{m9}\,R_l \tag{4.6}$$

which is the gain for a simple inverter. Thus, to attain high gain, R_l and R_s should be made to exceed the output resistance of both the driver and the cascode devices.

Frequency Response

The folded-cascode amplifier has two major poles, the dominant pole at the output node, and a non-dominant pole at the cascode node. The dominant pole is given by

$$
\begin{aligned}
s_l &= -\frac{1}{C_l\left[R_l // R_u\right]} \\
R_l &= r_{o2}\left\{1 + g_{m2} r_{o4}\right\} \\
R_u &= r_{o7}\left\{1 + g_{m7}\left[R_s // r_{o6}\right]\right\} .
\end{aligned}
\tag{4.7}
$$

R_u is the effective resistance looking into the drain of the cascode device M_7. The non-dominant pole is given by

$$
\begin{aligned}
s_p &= -\frac{1}{C_p\left\{r_{o8} // R_s // \frac{1}{g_{m7}}\right\}} \\
&\approx -\frac{g_{m7}}{C_p} .
\end{aligned}
\tag{4.8}
$$

C_p is the total capacitance that is present at the cascode node. It is comprised of the gate-to-source capacitance C_{gs} of the cascode device and the sum of the junction capacitance C_d associated with the diffusions of the driver, the p-channel current source, and the cascode device. To optimize the speed performance of the amplifier, s_p must be maximized. s_p can be re-expressed as

$$
\begin{aligned}
\left|\frac{1}{s_p}\right| &= \frac{C_{gs}}{g_{m7}} + \frac{C_d}{g_{m7}} \\
&= \tau_i + \tau_e .
\end{aligned}
\tag{4.9}
$$

For a constant current biasing, it can be shown that

$$
\begin{aligned}
\tau_i &\propto C_{ox} W^{\frac{1}{2}} L^{\frac{3}{2}} \\
\tau_e &\propto C_j W^{\frac{1}{2}} L^{\frac{1}{2}} D .
\end{aligned}
\tag{4.10}
$$

C_{ox} is the gate oxide capacitance per unit area, and C_j is the junction capacitance per unit area. W is the channel width, L is the channel length, and D is the minimum width of contacted source and drain diffusion. C_{ox}, C_d and D are fixed parameters for a given technology. The intrinsic and extrinsic delays, τ_i and τ_e,

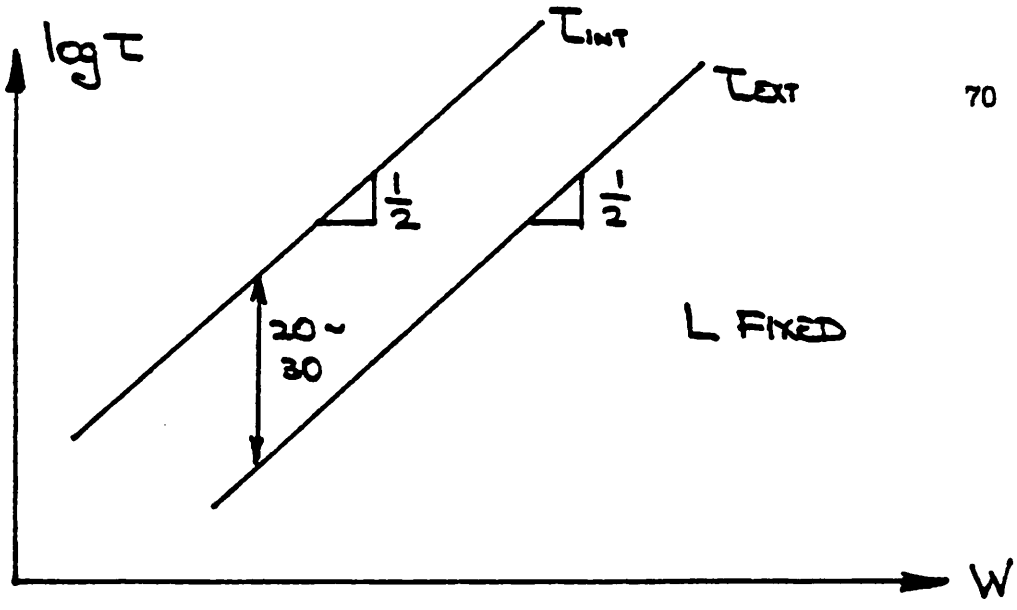
are plotted qualitatively as a function of W and L in Fig. 4.9. For a typical 3 μm CMOS technology, C_{ox} is approximately 20 to 30 times C_j, and D is on the order of 10 μm. Even at the minimum channel length of 3 μm, the intrinsic delay dominates over the extrinsic delay. Thus, in order to minimize the total delay, a minimum channel length device should be used as the cascode element. However, if the junction capacitance of both the p-channel current source and the driver is included, τ_e becomes comparable to τ_i. In such a case, s_p is approximately equal to $\frac{1}{2} f_T$. A typical numerical example is shown below.

Example

$$\frac{W}{L} = \frac{100}{3} \ (\mu m)$$
$$I_{bias} = 100 \ \mu A$$

$$s_p(NMOS) \approx 200 \ MHz$$
$$s_p(PMOS) \approx 100 \ MHz$$

Typically, an NMOS cascode has a 2 to 1 advantage in speed over a PMOS version owing to the difference in mobility. It seems that the former implementation will result as a faster circuit than the latter. This, however, is not entirely true. If the n-channel devices are replaced by p-channel devices and vice versa, in the circuit depicted in Fig. 4.7, the performance actually degrades. In order to account for the mobility difference, the $\frac{W}{L}$ of the devices needs to be increased. This results as a proportionate increase in the gate-to-source capacitance of the drivers which ultimately decreases the loop gain of the closed loop system, and thus reduces



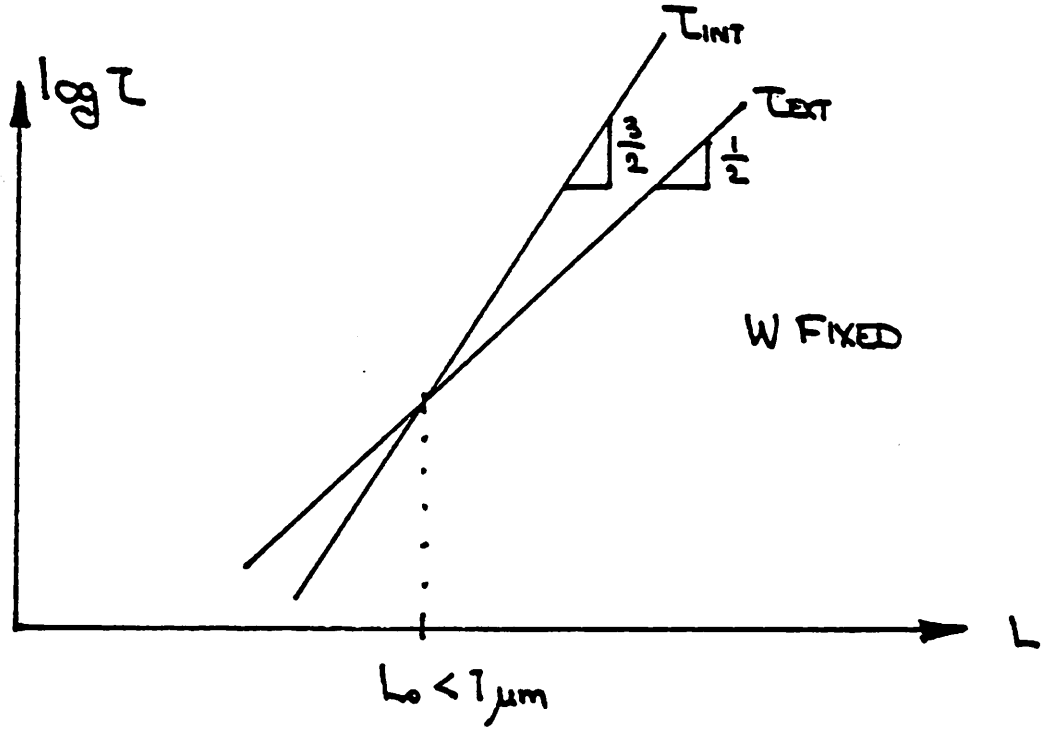


Figure 4.9
Intrinsic and Extrinsic Delays

the bandwidth. Furthermore, the p-channel devices exhibit poorer output characteristics compared with the n-channel devices, especially at high current levels. This results as a reduction of the overall gain.

Optimization of the Transient Response

If adequate loop gain is available (i.e. if $a_o f_o s_t > \frac{1}{4}s_p$), it is recommended to insert a left-half plane zero in the transfer function of the amplifier. This zero is incorporated in the folded-cascode amplifier by adding a feedforward capacitor C_{ff} across the cascode element. The circuit schematic and the differential mode, small-signal equivalent half-circuit are shown in Fig. 4.10. The addition of C_{ff} loads both the output and the cascode nodes, but it does not create any additional poles. The zero and the new non-dominant pole locations are

$$\begin{aligned} z_o &= = \frac{g_{m7}}{C_{ff}} \\ s_p^* &= -\frac{g_{m7}}{C_p + C_{ff}} \\ &= -\frac{1}{\frac{1}{s_p} + \frac{1}{z_o}} \end{aligned} \tag{4.11}$$

At first glance due to the additional loading of the cascode node by the feedforward capacitor, it appears that the closed loop bandwidth may be lower than the uncompensated case. To compare the two cases, the real parts of the corresponding complex pole pair are shown below.

Uncompensated Case

$$\sigma \approx \frac{1}{2}s_p$$

Compensation with a Zero

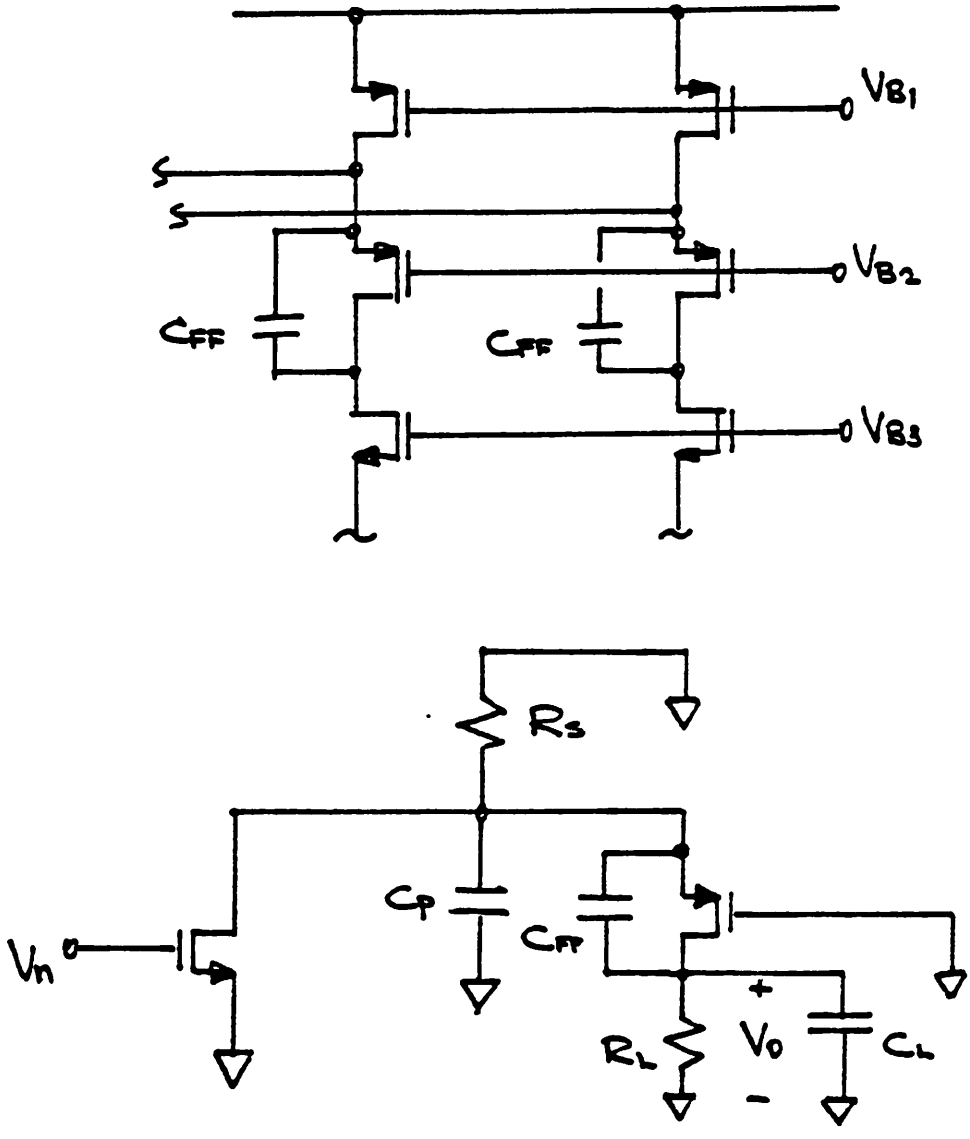


Figure 4.10
Insertion of the Left-Half Plane Zero

$$\sigma^{\bullet} \approx \frac{1}{2}s_p^{\bullet} + \frac{1}{2}\frac{a_0 f_0 s_1 s_p^{\bullet}}{z_0} \text{ where } s_p^{\bullet} = \frac{s_p z_0}{s_p + z_0}.$$

$$\frac{\sigma^*}{\sigma} = \frac{1 + \frac{a_0 f_0 s_l}{z_0}}{1 + \frac{s_p}{z_0}} \tag{4.12}$$

Typically, $z_0 > s_p$ and $a_0 f_0 s_l > s_p$. Thus, it is safe to conclude that σ^* is greater than σ. Even with the additional loading due to C_{ff}, it is still beneficial to compensate with a left-half zero.

4.5.2. Common Mode Behavior

One of the difficulties encountered in designing a fully-differential amplifier is controlling its common mode behavior. Specifically, the amplifier must have sufficient common mode signal rejection and a well-defined quiescent DC output voltage. Furthermore, for high speed operation the common mode transient response needs to be as fast as the differential mode response. Thus, a fully-differential amplifier can be thought of as a merged amplifier. A conceptual diagram of a merged amplifier is shown in Fig. 4.11. In order to control the common mode response, the common mode amplifier samples the outputs v_{o1} and v_{o2}, and feeds back a common mode correction signal to the differential mode amplifier [13]. This CM amplifier should have a very low DM-to-CM and CM-to-DM conversion gain. A schematic diagram of a fully-differential, folded-cascode amplifier with common mode feedback is shown in Fig. 4.12. The CMFB block feeds the common mode error signal to the gates of M_3 and M_4 in order to stabilize the common mode component of the output voltages. This feedback loop attempts to control the common mode output by decreasing the common mode output resistance. The common mode, small-signal half-circuit is shown in Fig. 4.13. R_u is the equivalent resistance seen looking into the drain of the cascode element (Eqn. 4.7), and C_0 is the gain of the common mode feedback block. The loop gain and the resulting common mode output resistance are

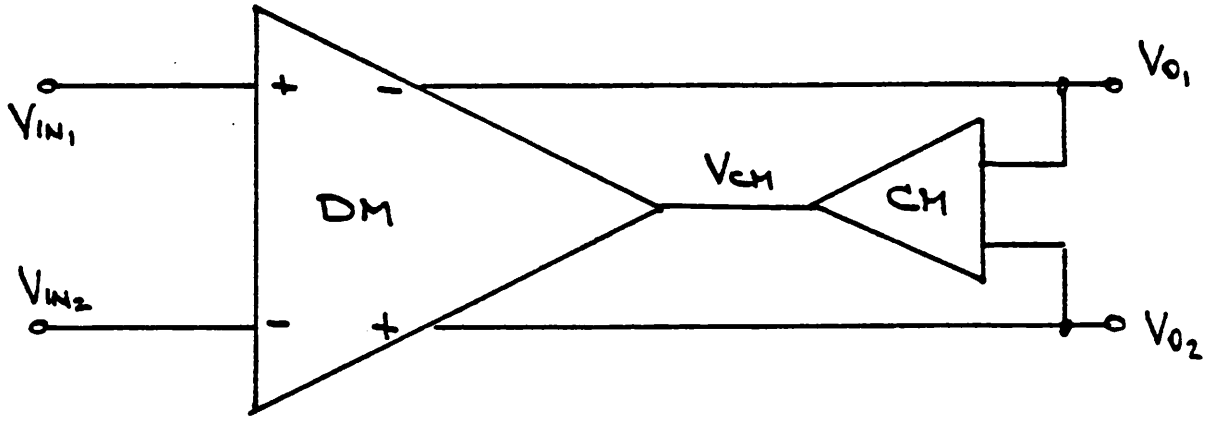


Figure 4.11
Conceptual Representation of a Fully-Differential Amplifier

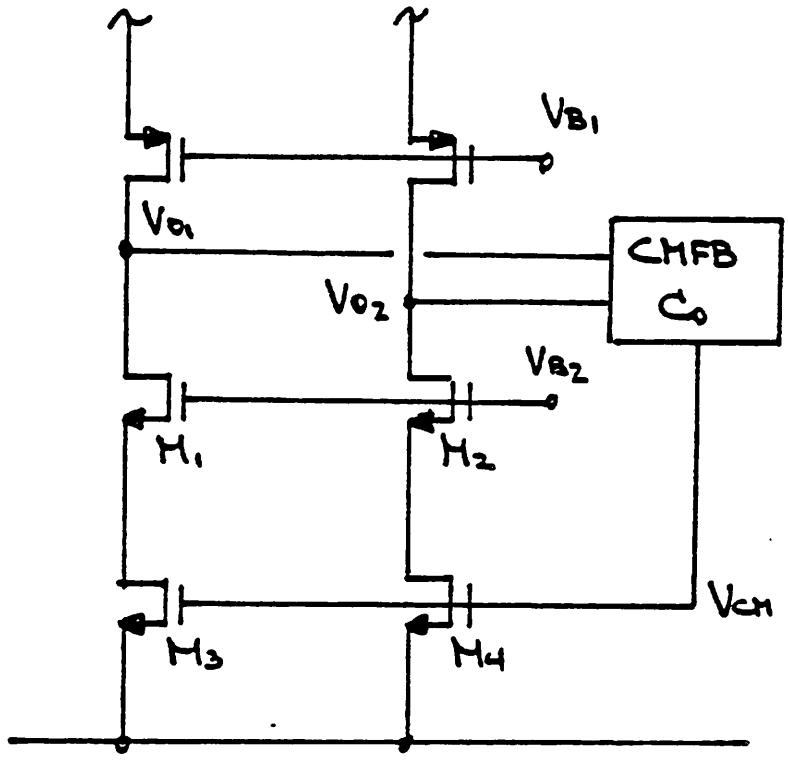


Figure 4.12
A Fully-Differential, Folded-Cascode Amplifier with Common Mode Feedback

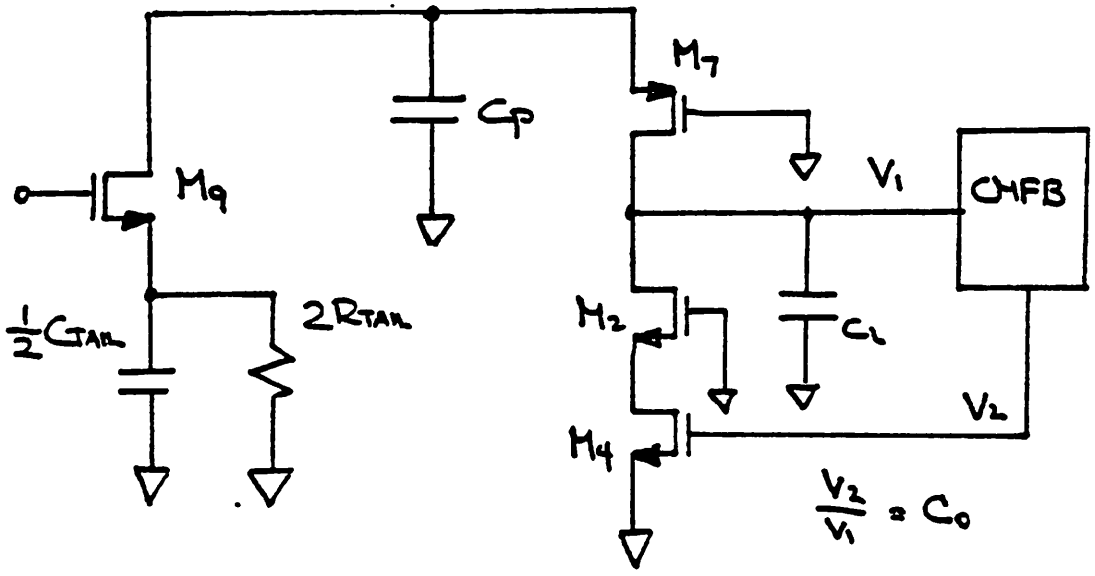


Figure 4.13
Common Mode, Small-Signal Half-Circuit

$$A_{loop} \approx - C_0 \, g_{m4} r_{o4} \, g_{m2} r_{o2} \tag{4.13}$$

$$R_{ocm} \approx \frac{1}{C_0 \, g_{m4}} . \tag{4.14}$$

In order to preserve the high differential mode gain, the common mode feedback circuit must not feed any differential mode signal into the gates of M_3 and M_4. Asymmetry within the CMFB block results as a non-zero signal. V_{cm} even fro pure differential outputs. the spurious V_{cm} amplified by M_1 and M_4 is then fed back to the output. Negative feedback is applied to one output, while positive feedback is applied to the other. However, as long as M_1 through M_4 are perfectly matched, the amount of feedback that is applied to either output is the same. Therefore, the correction signal is purely common mode, and thus, the

differential output remains unaffected by the asymmetry within the CMFB block.

In presence of a small mismatch in M_1 through M_4 in addition to the asymmetry in the CMFB block, the correction signal to the output consists of both common mode and differential mode components. The fractional differential mode correction signal due to the mismatch is

$$\frac{V_{od}^{\bullet}}{V_{od}} \approx -C_0 g_{m2}^{\bullet} r_{o2}^{\bullet}\, g_{m4}^{\bullet} r_{o4}^{\bullet} \left\{ 2\frac{\Delta r_{o2}}{r_{o2}^{\bullet}} + 2\frac{\frac{\Delta r_{o3}}{r_{o4}^{\bullet}}}{g_{m4}^{\bullet}} \right\} \tag{4.17}$$

where

$$g_{m2}^{\bullet} = \frac{1}{2}(g_{m1} + g_{m2}),\ g_{m4}^{\bullet} = \frac{1}{2}(g_{m3} + g_{m4}),$$

$$\Delta g_{m2} = g_{m2} - g_{m1},\ \Delta g_{m4} = g_{m4} - g_{m3},$$

$$r_{o2}^{\bullet} = \frac{1}{2}(r_{o2} + r_{o1}),\ r_{o4}^{\bullet} = \frac{1}{2}(r_{o4} + r_{o3}),$$

$$\Delta r_{o2} = r_{o2} - r_{o1},\ \text{and}\ \Delta r_{o4} = r_{o4} - r_{o3}.$$

Several types of process variation can cause the transconductance and output resistance mismatches. W and L variations caused by photolithography and thin film etching are the major causes of mismatch. Because analog circuits employ devices whose gate width is much larger than its length, the channel length variation ΔL creates a larger fractional mismatch in g_m and r_o. The fractional mismatches $\frac{\Delta g_m}{g_m}$ and $\frac{\Delta r_o}{r_o}$, that are the result of ΔL tend to offset each other since g_m is proportional to $\frac{1}{L}$, while r_o is proportional to L. From Fig. 4.13, the differential mode output resistance, in presence of all possible mismatches within the common mode feedback loop, can be determined. The computed differential mode output resistance is

$$R_{odiff} \approx \frac{R_u}{1 + g_{m4} R_u \left\{ \Delta C_0 \frac{\Delta g_{m4}}{g_{m4}} \right\}} \tag{4.18}$$

where R_u is the equivalent resistance seen looking into the drain of the cascode device, ΔC_0 is the fractional mismatch of the gain of the CMFB block, and $\frac{\Delta g_{m4}}{g_{m4}}$ is the fractional mismatch of M_4. For a typical 4 sigma tolerance in photolithography and thin film etching, the fractional variation in L is a few percent. Thus, the decrease in the differential mode output resistance is nominally less than one percent. Therefore, device mismatch within the common mode feedback loop has a minimal effect on the differential mode performance.

Transient Response

Since the common mode gain is intentionally made very small, the resulting closed loop pole location is nearly identical to that of the open loop case. The common mode transfer function contains at least three poles. The approximate location of the poles are

$$\begin{aligned} s_{lcm} &\approx \frac{C_0 g_{m4}}{C_l} \\ s_{pcm} &\approx \frac{g_{m7}}{C_p} \\ s_{cm} &\approx \frac{2 g_{m9}}{C_{tail}} \end{aligned} \tag{4.18}$$

The pole s_{lcm} associated with the output node is at a much higher frequency due to the lowering of the output resistance by the common mode feedback. s_{pcm} is identical to s_p, the differential mode cascode node pole, and is the highest frequency pole of the three. For a common mode input, the source node of the input differential pair can no longer be considered as a virtual ground. Thus, the capacitance $\frac{1}{2} C_{tail}$, which is approximately equal to the gate-to-source capacitance of

the input driver M_9, contributes an additional pole s_{cm}. This pole is on the order of the f_T of M_9. Therefore, the common mode transient response is determined primarily by s_{lcm}, which is the lowest pole. Thus, to attain a fast common mode response, the transconductance of M_4 should be made as large as possible.

In reality, there are several other poles present within the local common mode feedback loop. There is a pole at the source node of M_2. The CMFB block may also contribute an additional pole. Because the loop gain is large for this local feedback loop, the poles may become complex. Thus, frequency compensation may be necessary to guarantee a well-behaved response.

The local common mode feedback can be implemented in several ways. Fig. 4.14 shows one of the implementations. In this scheme M_A and M_B, which operate in their triode region, sample the output voltages V_{o1} and V_{o2}, and feed a common mode error signal to the source of M_3 and M_4. Because M_A and M_B operate in the triode region, the CMFB block transfer gain C_o is much less than unity. If C_o is defined as the ratio $\frac{V_x}{V_{oc}}$, where V_{oc} is the common mode component of the output, we obtain

$$\begin{aligned} C_o &= g_m r_o \\ &= \frac{V_x}{V_{oc} - V_T} \frac{1}{1 - \frac{V_x}{V_{oc} - V_T}} \end{aligned} \tag{4.19}$$

where C_o represents the small-signal common mode gain $\frac{\Delta V_x}{\Delta V_{oc}}$ about the operating point. In order to obtain maximum output swing, V_x is held at several hundred millivolts. Thus, C_o is on the order of 0.2 at most. This low value results as a substantially higher common mode output resistance that ultimately limits the speed of the common mode response.

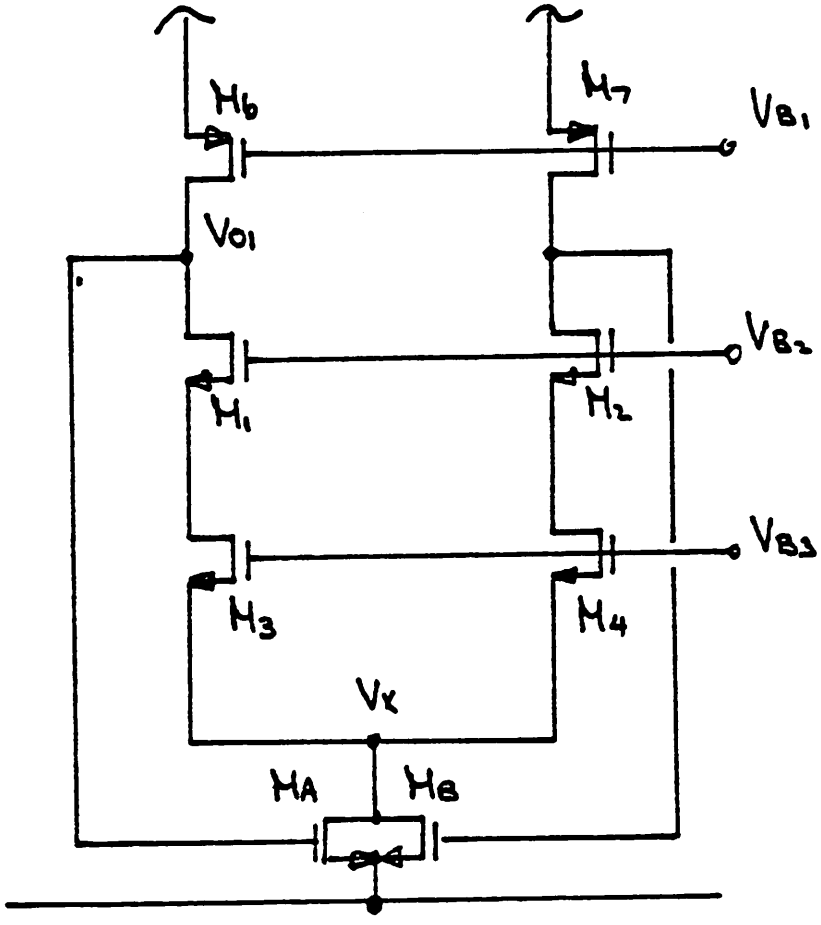


Figure 4.14
CMFB Using the Triode Operated Devices

As previously mentioned, the CMFB block should have a very small differential mode to common mode conversion gain A_{cm-dm}. Fig. 4.15 shows the schematic representation of the triode region operated CMFB block. V_{o1} and V_{o2} are the output voltages and I_o is the bias current. The relationship between the outputs and the correction common mode signal V_x is given by

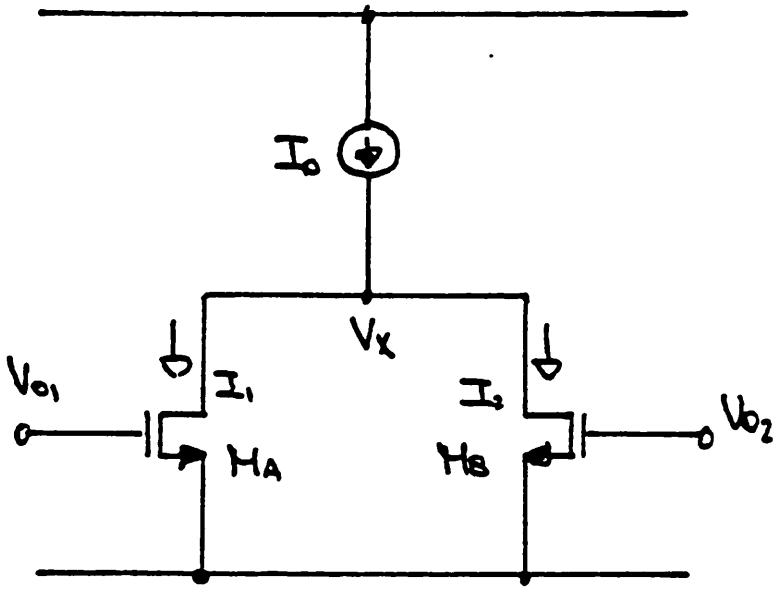


Figure 4.15
Triode Region Operated CMFB Block

$$I_o = G(\frac{V_d}{2} + V_{ss} - V_T - \frac{V_x}{2})V_x + G(-\frac{V_d}{2} + V_{ss} - V_T - \frac{V_x}{2})V_x \qquad (4.20)$$

Here, the outputs are assumed to be pure differential signals. The small-signal, differential-to-common mode conversion gain A_{cm-dm} is found by computing $\frac{dV_x}{dV_d}$, and is equal to

$$A_{cm-dm} = 0 \qquad (4.21)$$

Thus, barring any mismatch between M_A and M_B, the triode operated common mode feedback has no adverse effect on the differential response of the cascode amplifier. The sole disadvantage is that the common mode response is slow.

In order to improve the common mode transient performance, the common mode output resistance needs to be reduced. This requires a large gain of the CMFB block. A scheme that utilizes a differential source follower as the CMFB block is shown in Fig. 4.16. The source followers M_A and M_B sample the outputs V_{o1} and V_{o2}, and apply a common mode correction voltage V_x to the gates of M_3 and M_4. If R_o is large in comparison to $\frac{1}{g_m}$ of M_A and M_B, C_o will be approximately equal to unity. Then the common mode output resistance is given by $\frac{1}{g_{m4}}$. This assures a reasonably fast common mode response. Since M_A and M_B operate

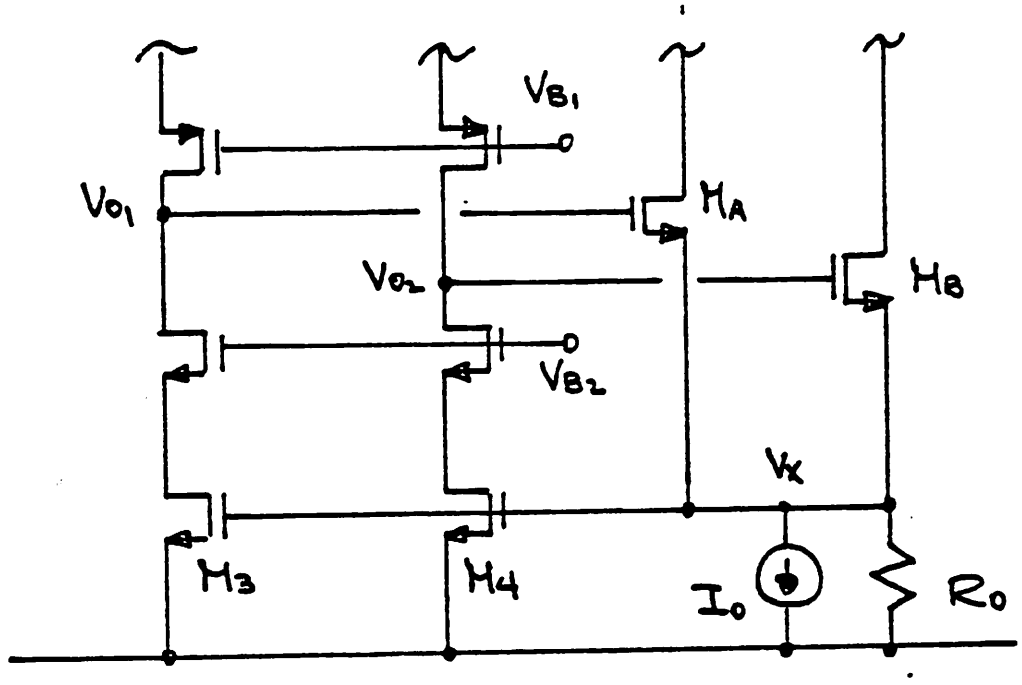


Figure 4.16
CMFB Using Differential Source Follower

in the square law regime, V_x is no longer linearly related to V_{o1} and V_{o2}. This non-linear distortion becomes noticeable when the output swing becomes large. Assuming a purely differential mode operation, the relationship between V_x and the output is described by

$$\frac{V_x + V_{ss}}{R_o} + I_o = G\left[\frac{V_d}{2} - V_x - V_T\right]^2 + G\left[-\frac{V_d}{2} - V_x - V_T\right]^2 \tag{4.22}$$

The small-signal differential-to-common mode conversion gain A_{cm-dm} is given by $\frac{dV_x}{dV_d}$, and is

$$\frac{dV_x}{dV_d} = -\frac{V_d}{4V_x - 4V_T - \frac{1}{GR_o}} \tag{4.23}$$

where $G = \frac{1}{2}\frac{W}{L}k$. The above can be approximated as

$$A_{cm-dm} \approx \frac{1}{4}\frac{V_d}{V_{ss} + V_T} \tag{4.24}$$

Thus, A_{cm-dm} increases as the differential output swing increases. However, this conversion gain will not exceed 0.25.

4.5.3. Biasing Circuit

The fully-differential folded-cascode amplifier, which is shown if Fig. 4.7, requires four bias voltages. A string of diode-connected devices that replicate M_5 through M_8 can be utilized to generate the bias voltages. Such a simple scheme, however, severely limits the output voltage swing. As an example, the negative going output swing is limited to approximately $-V_{ss} + V_T + \Delta V_{M4} + \Delta V_{M2}$ where ΔV is defined as

$$\Delta V = \sqrt{\frac{2I_d}{\frac{W}{L}k_n}} \tag{4.25}$$

The voltage swing limitation is even more severe in the positive direction due to a

smaller intrinsic gain factor k_p of the PMOS devices and due to the larger current conducted by the P-channel current sources.

A biasing circuit that overcomes this output swing problem is shown in Fig. 4.17a. A level shifting DC voltage source whose voltage is equal to the threshold voltage V_T is inserted between the gates of M_{AL} and M_{AR}. If the devices have the same $\frac{W}{L}$ ratio, the lower device M_{AR} is biased at the edge of saturation with a drain-to-source voltage equal to ΔV. Under this condition, the voltage across the cascode current source can drop to within $2\Delta V$ of the negative supply rail. A practical implementation of the high-swing cascode bias is shown in Fig. 4.17b. All devices have identical channel length and width, except M_A whose channel width is only one-fourth of the rest. This forces the lower cascode device to be biased at the edge of saturation with a drain-to-source voltage of ΔV.

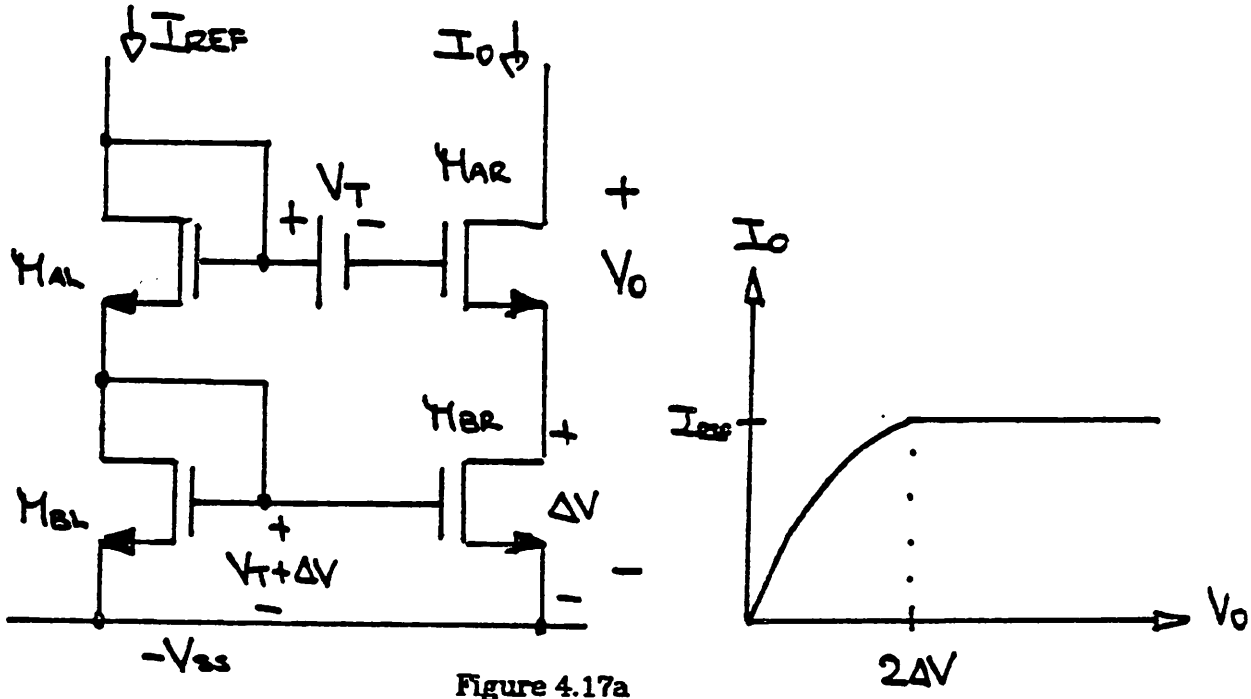


Figure 4.17a
Concept of High-Swing Cascode Bias

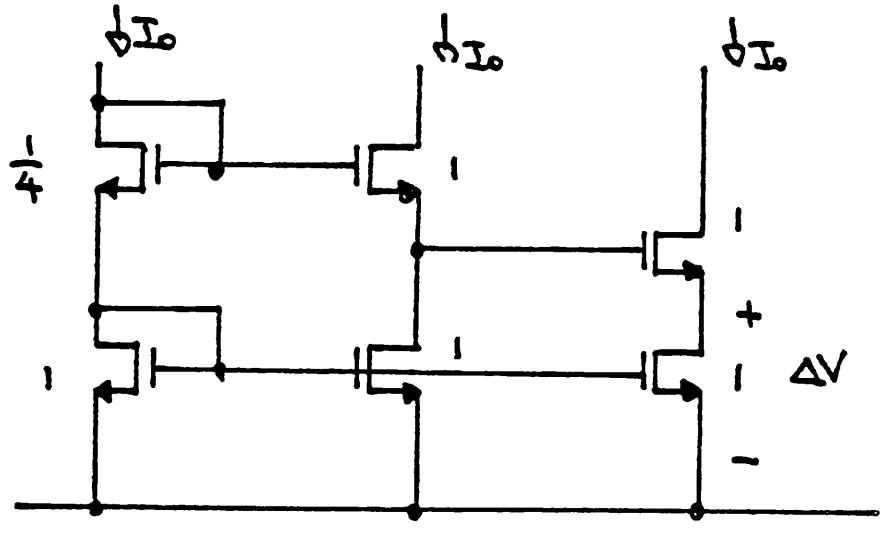


Figure 4.17b
A Practical Implementation of the High-Swing Cascode Bias

CHAPTER 5

TECHNOLOGY CONSIDERATIONS

The technology ultimately limits the performance of any analog or digital system. In the analog MOS world, the CMOS technology is preferred over the NMOS because of improved gain and frequency performance due to its complementary devices. Bulk CMOS technologies can be subdivided into the P-Well, N-Well, or Twin-Tub processes. Currently, the majority of CMOS technology is of the N-Well type. However, the fifth generation CMOS (one micron and sub-micron feature size) processes will most likely be either P-Well or Twin-Tub variety. The suppression of the unwanted parasitic devices, such as the lateral and vertical bipolar structures, necessitates the switch away from the N-Well topology.

As the effective channel length falls below the $3\,\mu m$ mark, device design begins to play a very important role. The first order device parameters – output conductance, threshold voltage, body-effect parameter, incremental junction capacitance and punchthrough voltage – are all affected by three basic processing parameters; the substrate doping, the channel doping and the drain-source junction depth. As the device and the interconnect features are scaled down, the second and third order effects begin to affect the device performance. Velocity saturation, finite channel thickness and diffusion resistance begin to degrade the transconductance of the MOS transistor. The fringing electric field begins to play a major part in the interconnect and the overlap capacitances. Thus, at the one micron level and below, the system level performance is determined by the parasitic and the extrinsic device characteristics.

In this chapter, we will present the design considerations for an high performance CMOS technology aimed for analog LSI applications. Some of the anticipated problems in technology and circuit design will be presented.

5.1. The CMOS Technology

High frequency analog systems require amplifiers that have a wide closed-loop bandwidth. From the discussion presented in chapter 2, such amplifiers must have a large open loop gain and a very high frequency non-dominant pole. The CMOS technology is especially suited to implement such high performance amplifiers in the simplest circuit configuration. The complementary active loads produce a large gain without resorting to sophisticated gain enhancement techniques [13, 14]. The simple circuit configurations result in a very wide bandwidth.

The majority of the current 3 μm CMOS processes are of the N-Well version. The main reason behind this choice is the fact that the NMOS devices, which are fabricated in the lightly doped substrate, have smaller junction capacitance and lower body-effect parameter than those of the P-Well type. This results as very high performance NMOS devices. The Twin-Tub process is also a viable technology. Its strong point, perhaps, is the flexibility to independently tailor the device performance of the PMOS and NMOS transistors. This, however, comes at the expense of added process complexity. At device geometry of $3\mu m$, the N-Well process will yield both NMOS and PMOS transistors that operate as well as those fabricated in the Twin-Tub process. However, for CMOS with device geometry of $1\mu m$ and below, the P-Well and the Twin-Tub processes will be required, primarily due to latch-up problems.

5.2. Device Performance—First Order Effects

The device parameters that affect the gain and the frequency response of an amplifier are the channel length modulation parameter λ, the threshold voltage V_T, the body-effect parameter γ, the incremental junction capacitance C_j, and the drain-to-source punchthrough voltage V_{PT}. These parameters are interrelated and are affected by the substrate and the channel doping concentration.

5.2.1. Channel Length Modulation

The depletion region X_{dd} between the channel and the drain diffusion modulates the effective electrical channel length L_{eff}. This depletion width is a function of the threshold voltage, the drain-to-source voltage, and the channel doping N_{ch}. From the conventional formula for the depletion region of an n^+–p junction, the drain end depletion width is expressed as

$$X_{dd} = \sqrt{\frac{2\varepsilon_s (V_d - V_{dsat})}{qN_{ch}}} \tag{5.1}$$

The drain current can then be represented as

$$I_d = \frac{L}{L - X_{dd}} I_{dsat} \tag{5.2}$$

where

$$I_{dsat} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox} V_{dsat}^2$$

$$V_{dsat} = V_g - 2\Phi_B + \frac{\sqrt{2\varepsilon_s q N_{ch} V_g}}{C_{ox}}$$

[15] The output conductance is given by

$$g_o = \frac{\partial I_d}{\partial V_d} = \frac{I_{dsat}}{2L\sqrt{\frac{qN_{ch}\,\varepsilon_s (V_d - V_{dsat})}{2\varepsilon_s}} - (V_d - V_{dsat})} \tag{5.3}$$

The MOS equivalent Early Voltage V_A can be defined as

$$V_A = 2\left\{L\sqrt{\frac{qN_{ch}(V_d - V_{dsat})}{2\varepsilon_s}} - (V_d - V_{dsat})\right\} \tag{5.4}$$

Now the output resistance is expressed as

$$r_o = \frac{V_A}{I_{dsat}} \tag{5.5}$$

>From Eqn. 5.4 the output resistance can be improved by increasing the channel doping near the $S_i - S_iO_2$ interface where the channel exists. However, N_{ch} also affects the threshold voltage. Thus, the upper limit of N_{ch} is determined by the threshold voltage.

Typically, the channel doping concentration is controlled by a single ion-implantation. For a 3 μm process, the implantation energy and dose are adjusted so that the surface concentration is on the order of $10^{16}\ cm^{-3}$. The depth of the implant is nominally between 0.2 μm to 0.7 μm. Fig. 5.2 shows a profile of the channel doping that was generated by SUPREM II. In order not to increase the body sensitivity, the depth of the implant x_{j2} is tailored so that, under nominal gate-to-body voltages, the implanted impurities are contained within the depletion region under the channel.

5.2.2. Threshold Voltage and Channel Length Modulation Trade-off

Eqn. 5.6 gives the threshold voltage expression for a long channel NMOS transistor with an n^+ poly gate.

$$V_T = -0.55\ V + |\Phi_{fn}| - \left|\frac{Q_{ss}}{C_{ox}}\right| + \left|\frac{Q_{imp}}{C_{ox}}\right| + \left|\frac{Q_B}{C_{ox}}\right| \tag{5.6}$$

Here, Φ_{fn} is the surface potential of the channel region; Q_{ss} is the surface state charge density; Q_{imp} is the channel implantation dosage; and Q_B is the ionized substrate charge under the channel. The channel implant affects the Φ_f and the

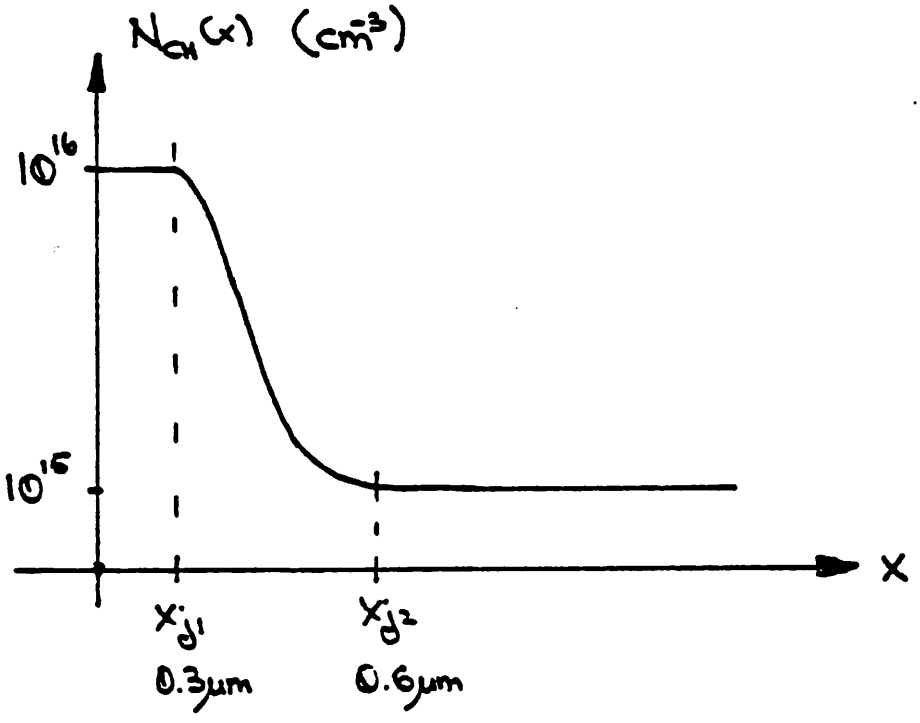


Figure 5.2
Channel Doping Profile

Q_{imp} terms. For a typical $3\,\mu m$ N-Well CMOS process, $\left|\frac{Q_{ss}}{C_{ox}}\right| = 0.41V$ and $\left|\frac{Q_B}{C_{ox}}\right| = 0.28V$, assuming an N_A of $5 \times 10^{14}\,cm^{-3}$, $V_{BS} = 0V$, and $x_{ox} = 50\,nm$. Thus, to obtain a threshold voltage of $0.7V$,

$$\left|\frac{Q_{imp}}{C_{ox}}\right| + \left|\Phi_{fn}\right| = 1.38V \qquad (5.7)$$

If the channel doping distribution can be approximated as a "box" distribution, we have

$$\frac{q\ N_{ch}\ x_j}{C_{ox}} + V_T \ln\left[\frac{N_{ch}}{n_i}\right] = 1.38\ V \qquad (5.8)$$

where $x_j = \frac{1}{2}(x_{j1} + x_{j2})$. Solving for $N_{ch}\ x_j$, which is equal to the total implant dose, we obtain

$$Q_{imp} = \frac{N_{ch}\ x_j}{q} = 5 \times 10^{11}\ cm^{-2}.$$

X_j is nominally designed to be equal to the junction depth of the source-drain diffusions. For a 3 μm technology, x_j is about 0.35 μm. The resulting channel doping concentration N_{ch} is $1.0 \times 10^{16}\ cm^{-3}$. A device that is biased right at the edge of saturation will have a $V_d - V_{dsat} \approx 2\Phi_f$. The corresponding Early voltage V_A of such a 3 μm channel device is 12.6 V. Its output resistance is 126 $K\Omega$ at a bias current of 100 μA. Table 5.1 lists the measured and the computed Early voltages of NMOS devices operating at $V_d - V_{dsat}$ of 2 V. In order to improve the output characteristic of the short-channel devices, the channel doping must be increased; however, this results as an increase in the threshold voltage.

CHANNEL LENGTH (μm)	MEASURED V_A (V)	COMPUTED V_A (V)
3.3	27	21
4.3	31.5	29
6.3	51	45

TABLE 5.1

Measured and Computed Early Voltages

5.2.3. Threshold Voltage of Short-Channel Devices

As the channel length decreases, the threshold voltage also decreases. If the channel length is reduced even more, the drain current becomes independent of the gate voltage. This is due to the fact that the field lines emanating from the drain terminate in the channel instead of in the substrate. Under this condition the drain controls the I-V characteristics of the device. [16]. The influence of the drain voltage on the channel can be reduced by decreasing the junction depth of the source-drain diffusions and by increasing the substrate concentration. Increasing the doping concentration of the substrate, however, enhances the body sensitivity. For analog circuits applications, the modulation of the threshold voltage due to source-to-body voltage induces non-linear distortion. Thus, the drain-induced threshold modulation must be suppressed by other methods.

By tailoring the channel doping profile as is shown in Fig. 5.3, the short-channel threshold voltage sensitivity to drain voltage can be reduced without increasing the body sensitivity. [17] A double implantation process generates this desired profile. A very shallow implant determines the surface concentration of the channel. A second deep implant, whose dose is slightly higher than the first, creates the sub-surface peak that is placed beneath the n^+ source-drain diffusion. This sub-surface peak shields the channel from the field lines emanating from the drain diffusion. Furthermore, since the depth of the deep channel implant is about $0.7\,\mu m$, at the nominal operating voltage the depletion region under the channel extends beyond the implanted region. This assures a low body sensitivity. It should be noted that the doubly implanted channel profile is necessary only for

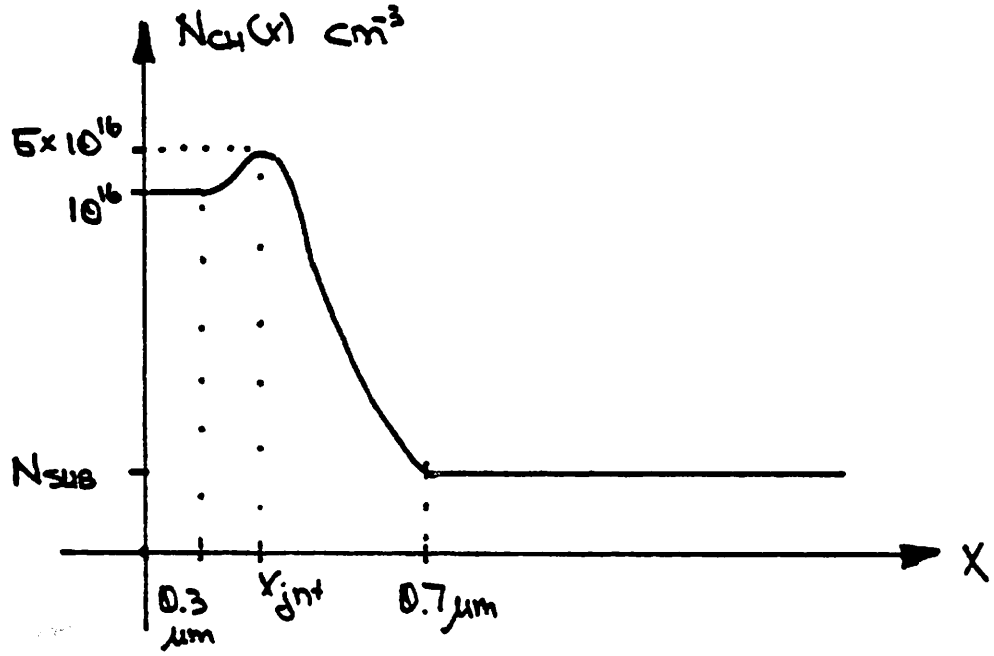


Figure 5.3
Improved Channel Doping Profile

2.0 μm technologies and beyond. For a typical 3 μm technology, a channel doping profile shown in Fig. 5.2 will suffice.

5.2.4. Punchthrough Voltage and Junction Capacitance

When the drain-to-source voltage is large enough to cause the electric field from the drain to terminate at the source, a very large sub-surface drain-to-source current conducts. This condition is termed as the sub-surface punchthrough. Thus, when punchthrough occurs, shunt current flows in the bulk to

augment the conduction current in the surface inversion layer. An approximate expression [18] for the punchthrough voltage V_{PT} is

$$V_{PT} = \frac{q\ N_A}{2\varepsilon_s}\left\{L_{eff} - \sqrt{\frac{2\varepsilon_s\ (V_{sb} + V_{bi})}{q\ N_A}}\right\}^2 - (V_{bi} - V_{sb}) \qquad (5.9)$$

Fig. 5.4 shows the plot of the punchthrough voltage for different effective channel lengths. If the channel is doped at $10^{16}\ cm^{-3}$, for channel lengths in excess of $2\ \mu m$, the device breakdown is caused by avalanche and not by punchthrough. Thus, a channel doping level of $10^{16}\ cm^{-3}$ is adequate to realize a 10 V $3\ \mu m$ CMOS process. In order for the devices to exhibit a good high frequency response, the incremental junction capacitance must be minimized. Under nominal operating voltages, the depletion region under the source-drain diffusions must range beyond the doped channel region. If such a condition is met, the small-signal capacitance is determined solely by the substrate doping level. Using the channel doping profile that is shown in Fig. 5.2 and employing the one-sided step junction approximation, a reverse bias voltage of 3.8 V between the source-drain diffusion and the substrate is sufficient to carry the depletion region past the highly implanted channel area.

Another component of the junction capacitance is the peripheral capacitance that is associated with the channel stop implantation. The cross section of an NMOS device that shows this capacitive component is illustrated in Fig. 5.5. For a typical $3\ \mu m$ CMOS process, the depth of the p-field channel stop implantation is about $1\ \mu m$ with an average surface concentration of $5 \times 10^{16}\ cm^{-3}$. The segment X_i of the n^+ diffusion that butts against the field implant is approximately $\frac{1}{4}\pi\ x_{jn^+}$. The peripheral capacitance C_p can no longer be neglected in analog-type devices whose channel width is large compared to its channel length.

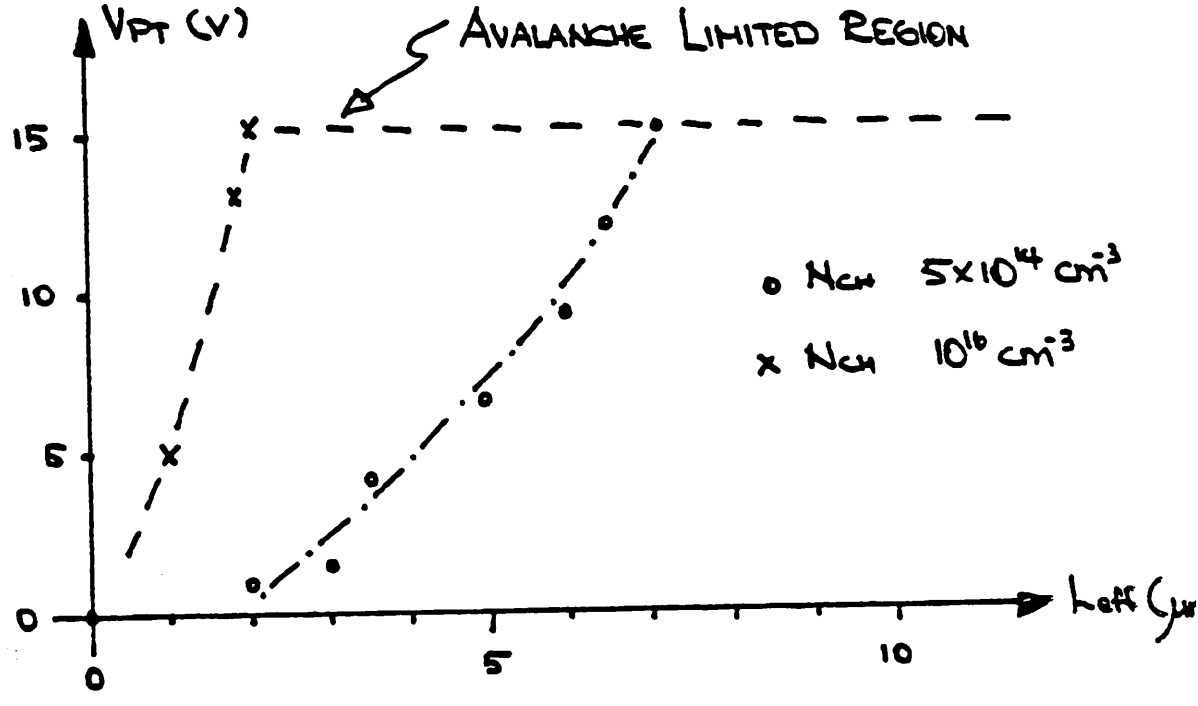


Figure 5.4
Punchthrough Voltage as a Function of Channel Length

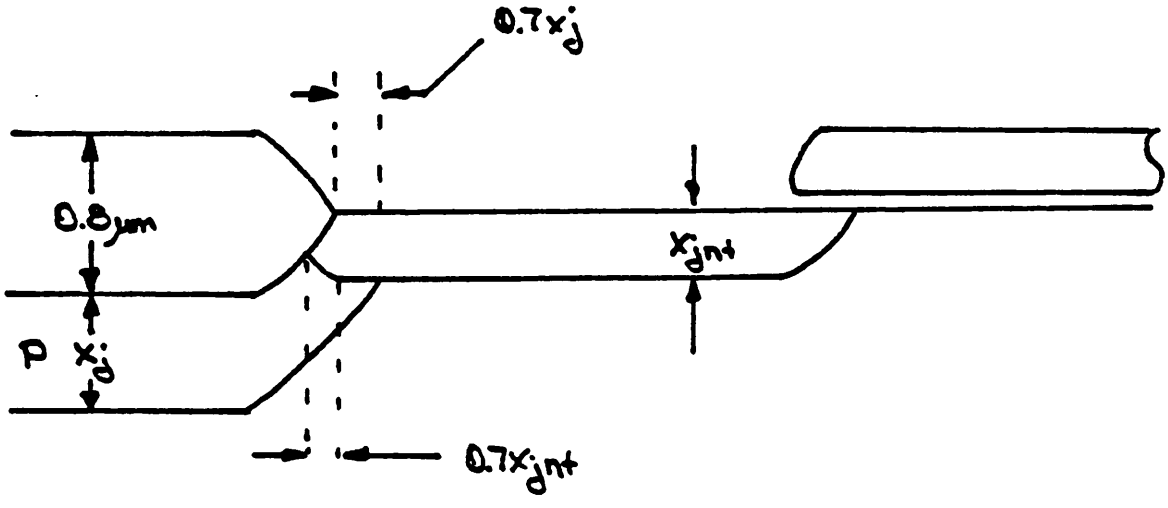


Figure 5.5
Lateral Encroachment of Channel-Stop Implant

Example

Consider a device with $\frac{W}{L} = \frac{300\ \mu m}{3\ \mu m}$ fabricated in $3\ \mu m$ technology. The minimum via size and the minimum spacing between features are $3\ \mu m$. The n^+ diffusion depth is $0.4\ \mu m$. The dimensions of the diffusion is W by D or $300\ \mu m\ x\ 9\ \mu m$. The ratio of the peripheral capacitance to the bottom-plate capacitance is

$$\frac{C_p}{C_b} \alpha \sqrt{\frac{N_F}{N_A}}\left(\frac{x_l}{D} + \frac{2x_l}{W}\right)$$

$$= \left(\frac{5 x 10^{18}}{5 x 10^{14}}\right)^{\frac{1}{2}} \frac{\frac{1}{4}\pi(0.4)}{9} \approx \frac{1}{3} \qquad (5.10)$$

The capacitance ratio of Eqn. 5.7 is plotted in Fig. 5.6. For wide channel devices, the ratio remains fixed at 1:3. However, as the channel width is reduced to the critical width W_c, the peripheral capacitance begins to dominate. For a 3 μm technology W_c is on the order of 10 μm.

	high dose deep implant	high dose shallow implant	low dose deep implant	low dose shallow implant	no implant
V_T	++	0	+	0	0
γ	-	0	-	0	0
τ_0	++	+	+	0	0
V_{PT}	++	0	+	0	0
C_{j0}	--	0	0	0	0

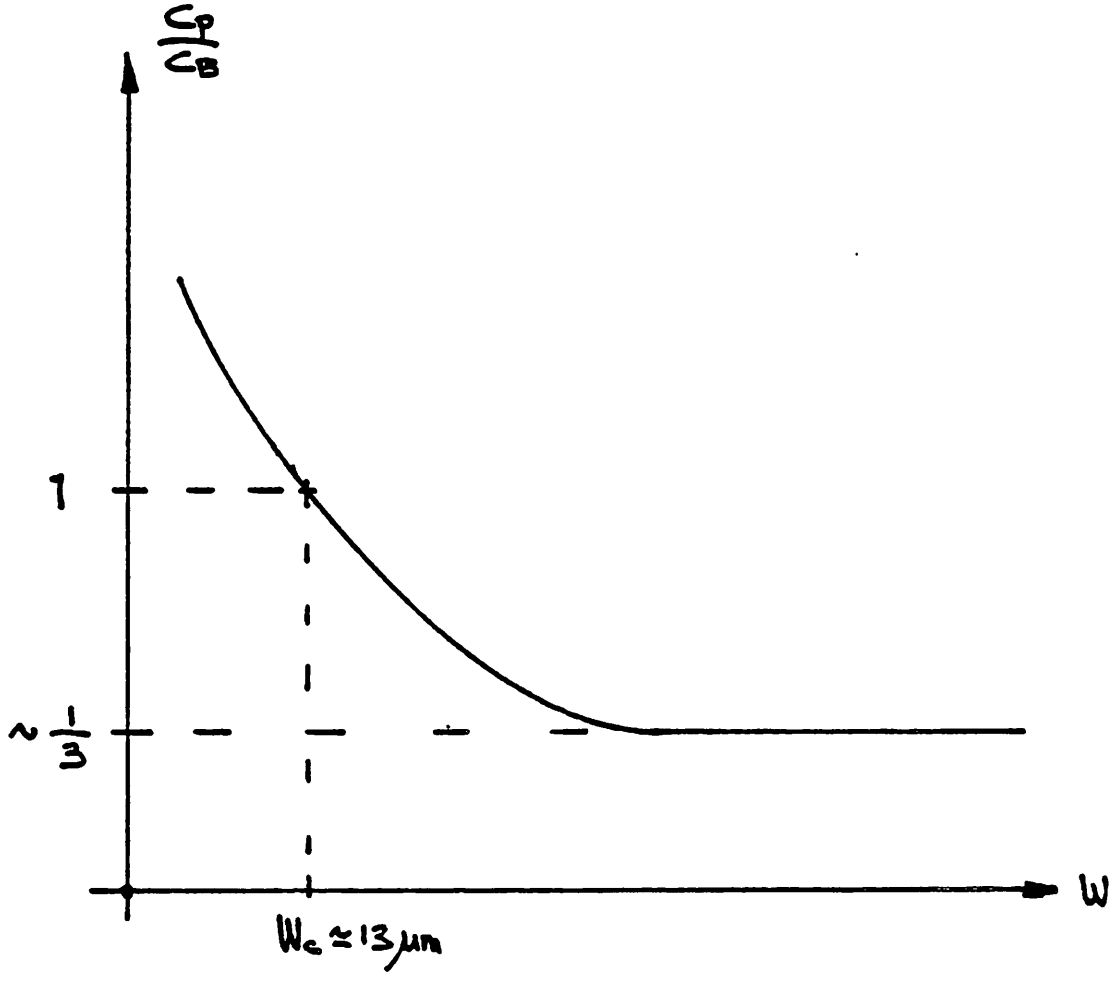
Table 5.2

Effects of Channel Profile on Device Performance

+ improves
- degrades
0 no change

5.2.5. Optimal Channel Doping Profile

Table 5.2 summarizes how the channel doping profile affects the device parameters. The change in the device parameters are compared to the unimplanted case. + denotes improvement, - degradation, and 0 no change. The table shows that a fairly deep channel implant (depth of on the order of the source-drain junction) improves the short-channel characteristics. However, heavy dosage degrades the body sensitivity parameter and increase the incremental junction capacitance. Thus, the optimal channel implant is a deep and moderate dosage implantation. For a 3 μm CMOS, N_{ch} is on the order of $10^{16}\ cm^{-3}$ with a



$\frac{N_{PP}}{N_A} = 100$

$D = 9\mu m$

$x_{jnt} = 0.4\mu m$

$W_c = 10\pi x_{jnt}$

Figure 5.6
Peripheral vs Bottom-Plate Capacitance Ratio

	high dose deep implant	high dose shallow implant	low dose deep implant	low dose shallow implant	no implant
V_T	++	0	+	0	0
γ	-	0	-	0	0
τ_o	++	+	+	0	0
V_{PT}	++	0	+	0	0
C_{jo}	--	0	0	0	0

Table 5.2

Effects of Channel Profile on Device Performance

+ improves
- degrades
0 no change

5.2.5. Optimal Channel Doping Profile

Table 5.2 summarizes how the channel doping profile affects the device parameters. The change in the device parameters are compared to the unimplanted case. + denotes improvement, - degradation, and 0 no change. The table shows that a fairly deep channel implant (depth of on the order of the source-drain junction) improves the short-channel characteristics. However, heavy dosage degrades the body sensitivity parameter and increase the incremental junction capacitance. Thus, the optimal channel implant is a deep and moderate dosage implantation. For a 3 μm CMOS, N_{ch} is on the order of $10^{16}\ cm^{-3}$ with a

depth of 0.6 μm.

5.3. Scaled CMOS

If the effective channel length is reduced to 1 μm and below, second and third order effects begin to dominate the device performance. The transconductance levels off due to velocity saturation; finite channel resistance and diffusion sheet resistance reduce the current gain; and the frequency response degrades due to the increase in parasitic capacitance caused by fringing field. Furthermore, to overcome the latch-up problem, a major structural change becomes necessary.

5.3.1. Velocity Saturation

To understand the device operation when the velocity saturates, a first order model is derived. Let us assume that, on the average, the drift velocity of the carriers within the channel approaches the limiting value of v_{sat}. The transit time from the source to the drain is

$$t_{TR} = \frac{L_{eff}}{v_{sat}} \tag{5.11}$$

Due to velocity saturation, the transit time is no longer affected by the drain-to-source voltage V_{ds}. The drain current is given by

$$I_d = \frac{Q_{ch}}{t_{TR}} \tag{5.12}$$

where Q_{ch} is the total channel charge [19]

$$Q_{ch} = WL\, C_{ox}\, (V_g - V_T) \tag{5.13}$$

Thus, under the condition of velocity saturation, the drain current is independent of V_{ds} and is represented as

$$I_d \approx W v_{sat} C_{ox} (V_g - V_T) \tag{5.14}$$

The transconductance $\frac{\partial I_d}{\partial V_g}$ is now independent of the gate bias voltage V_g. Furthermore, $I_d - V_{ds}$ characteristic is now flat; that is, the output resistance is infinite. However, for a real device, I_d increases with V_{ds}. For a short-channel device, moderate V_{ds} can modulate the drain current through DIBL (drain-induced barrier lowering) [20], and avalanche at the drain. Thus, Eqn. 5.3 is no longer valid for devices with channel lengths less than 1 μm.

5.3.2. Diffusion and Contact Resistance

As the dimensions are scaled down, the parasitic resistance of the diffusion and the contact begins to play an increasingly important role in determining the device performance. At the source end of the device, any parasitic resistance that appears in series with the channel degrades the transconductance. The drain current can be expressed as

$$I_d = \frac{1}{2} \frac{W}{L} \mu C_{ox} \left[\frac{1}{1 + \frac{R_s}{R_{ch}}} \right] \left(V_{gs} - V_T \right)^2 \tag{5.15}$$

where R_s is the total parasitic resistance at the source and R_{ch} is the channel resistance,

$$\frac{1}{R_{ch}} = \frac{W}{L} \mu C_{ox} \left(V_{gs} - V_T \right) \tag{5.16}$$

The source resistance R_s consists of the diffusion resistance and the contact resistance. Both components increase in magnitude with scaling.

The diffusion resistance is inversely proportional to the junction depth. Since short-channel devices require very shallow diffusions to suppress DIBL, as a consequence, the sheet resistivity increases. One method to overcome this problem is to employ a double implanted diffusion as is shown in Fig. 5.7. [21]. In this

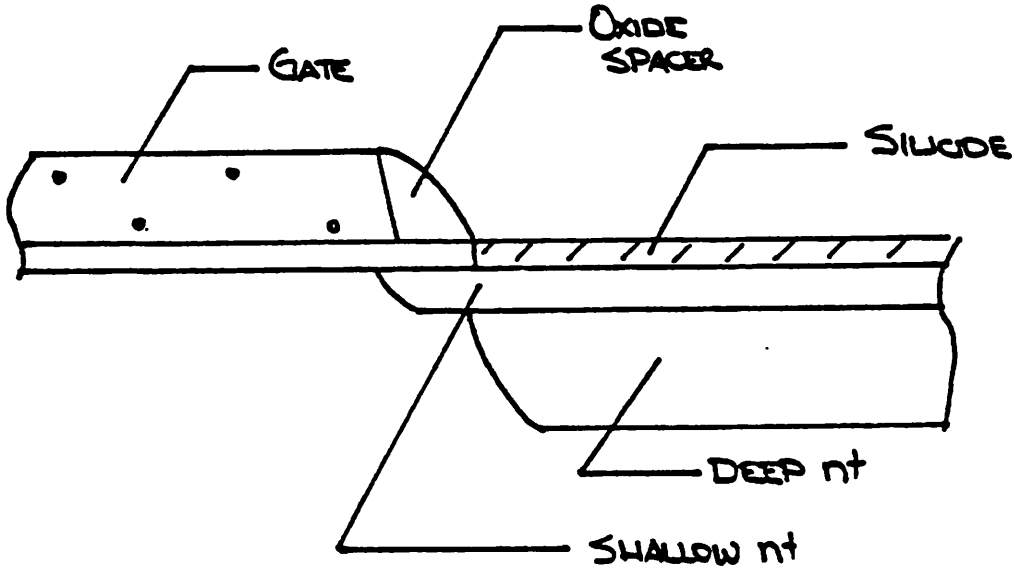


Figure 4.7
Double Implanted Diffusion

structure, the channel modulation by the drain is suppressed by the shallow n diffusion. The series ohmic resistance is minimized by the deep, heavily doped n^+ diffusion. Further reduction of the parasitic resistance is achieved by forming a silicide layer on top of the diffusion. Now most of the current is conducted though the low resistance silicide layer.

5.3.3. Finite Channel Thickness

A cross sectional view of an NMOS device is shown in Fig. 5.8. In the figure x_{ox} and x_{ch} are the gate oxide thickness and the channel thickness, respectively. The induced channel charge Q_{ch} is proportional to the voltage that is dropped across the oxide. If the channel capacitance is taken into account, the channel charge is

$$\begin{aligned} Q_{ch} &= C_{ox}\, V_{ox} \\ &= C_{ox}\,(V_{gs} - V_T)\,\frac{C_{ch}}{C_{ox} + C_{ch}} \end{aligned} \tag{5.17}$$

Typically, x_{ch} is on the order of 5 nm. If x_{ox} is larger than x_{ch}, Eqn. 5.14 can be

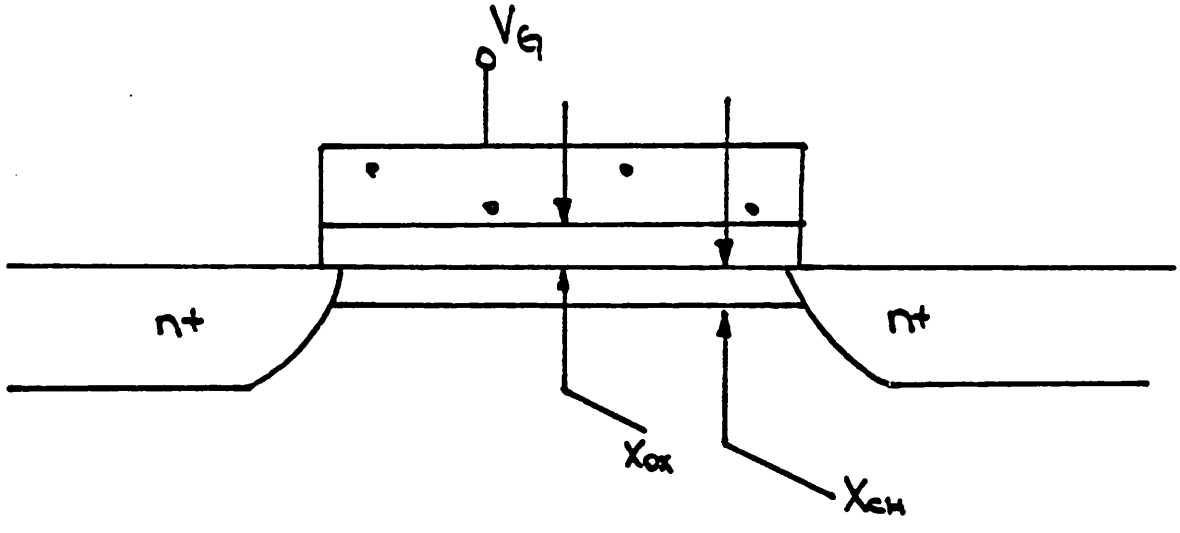


Figure 5.8
Finite Channel Thickness

approximated as

$$Q_{ch} \approx C_{ox} \frac{1}{1 + \frac{C_{ox}}{C_{ch}}}(V_{gs} - V_T) \tag{5.18}$$

For a typical 3 μm process, the decrease in the channel charge due to finite channel tickness is only 1.6%. However, this effect can no longer be ignored for processes with thin gate dielectric.

5.3.4. Composite Effects

The effects of velocity saturation, parasitic source resistance and the finite channel thickness can be combined to obtain the expression for transconductance g_m [22]

$$g_m = \frac{W}{L} C_{ox} \mu_n \frac{1}{1 + \frac{\mu_n}{E v_{sat}}} \frac{1}{1 + \frac{C_{ox}}{C_{ch}}} \frac{1}{1 + \frac{R_s}{R_{ch}}}(V_g - V_T) \tag{5.19}$$

As the device dimensions shrink, the transconductance initially increases due to the improvement of the average mobility value. Once velocity saturation sets in, the g_m levels off. Further scaling degrades the transconductance due to the finite channel thickness and parasitic source resistance.

5.3.5. Hot Carrier Effects

As the channel length decreases, the diffusions are made shallower to suppress drain-induced barrier lowering and electrostatic feedback from the drain. The doping concentration of the diffusion is increased in order to reduce the sheet resistance. This, in turn, causes the electric field near the drain to approach the critical value. Impact ionization due to the high field creates electron-hole pairs. The electrons are swept toward the gate, and the holes drift

into the substrate. The energetic electrons that are swept by the gate-to-drain electric field may become trapped within the gate dielectric material. The trapped electrons cause the threshold voltage to shift in the positive direction. This may lead to long-term reliability problems.

The holes created through impact ionization drift into the substrate. Part of them find their way to the source diffusion. If the magnitude of this hole current is large enough to cause a substantial ohmic voltage drop, the pn diode (source-substrate diode) may turn on. The injected minority carriers (electrons) are swept into the collector (drain diffusion). Now, this parasitic lateral bipolar transistor causes the MOS device to latch-up [23]. The maximum drain-to-source voltage that can be applied is a function of the gate voltage, the channel length and the substrate resistivity. A large gate voltage increases the channel current and, in turn, enhances the impact ionization hole current. High resistivity substrate results as higher ohmic voltage drop. Therefore, a low resistivity substrate is necessary to suppress the turn-on of the lateral parasitic bipolar transistor.

5.3.6. Latch-Up Control

In CMOS technology, the parasitic NPN and PNP devices can turn on under certain set of conditions.This results in the disruption of the normal operation of the MOS transistors. There are two "latch-up" mechanisms. First is the lateral bipolar latch-up where an NPN or a PNP transistor that appear in parallel to an MOS device turns on. Fig. 5.9a. Second is the SCR latch-up due to the merged NPN-PNP structure. Fig. 5.9b.

The Lateral Bipolar Latch-up

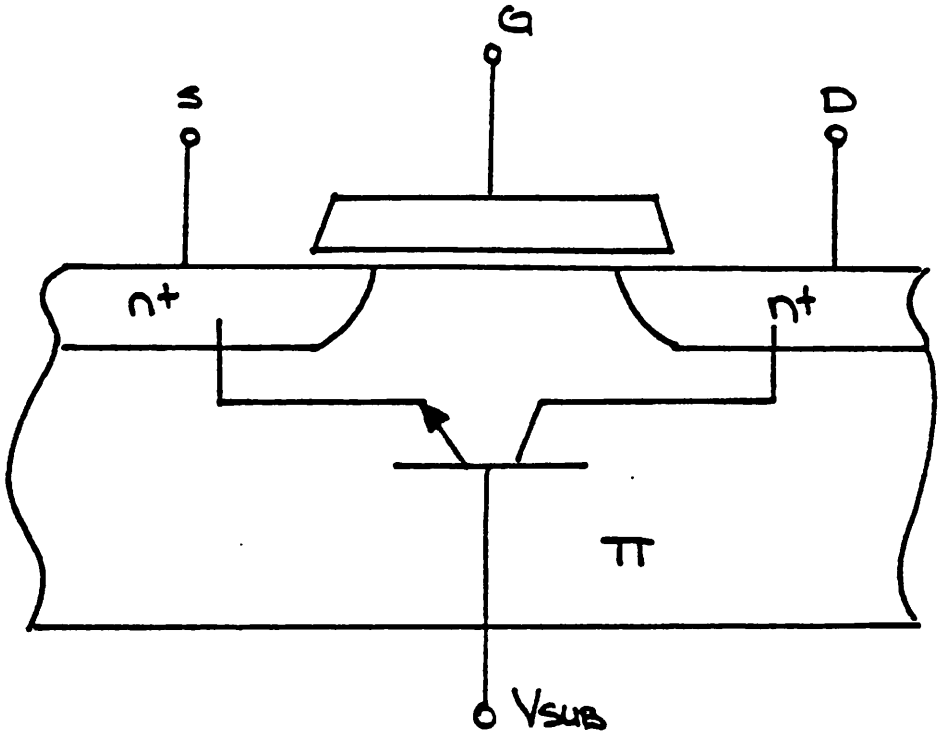


Figure 5.9a
Lateral Bipolar Device

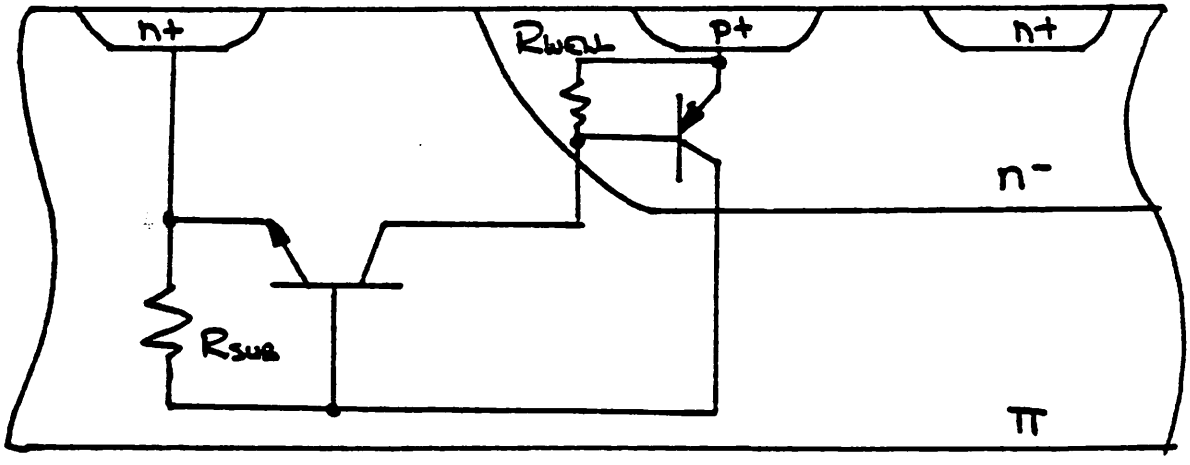


Figure 5.9b
Parasitic SCR Device

The mechanisms for the lateral bipolar latch-up was presented in section 5:3.5. In

order to suppress this latch-up, the electric field at the drain needs to be reduced, and the substrate resistivity must be decreased. The former can be accomplished by using the LDD structure. The use of an epitaxial substrate ($p-p^+$) aids in increasing the turn on voltage of the parasitic device. The built-in electric field at the high-low junction tends to sweep the holes generated at the drain region into the substrate. Thus, fewer holes will find their way to the source diffusion.

SCR Latch Up

Referring to Fig. 5.9b, the SCR latch-up occurs when the ohmic drop across R_{subs} or R_{nwell} is large enough to forward bias the base-emitter junction of either the PNP or the NPN transistors. For an N-Well process, the NPN lateral transistor is formed between the N-Well and the adjacent n^+ diffusion. The PNP devices, both vertical and lateral, are comprised of the well, substrate and the p^+ diffusion. The lateral NPN can turn on if the hole current injected from the N-Well (PNP base) causes sufficient IR drop within the p-type substrate to forward bias the n^+ diffusion. This risk can be reduced by utilizing an epitaxial substrate. The built-in electric field at the high-low junction sweeps the holes into the substrate, thereby minimizing the chance to forward bias the junction. This, however, does not completely eliminate the problem. For a CMOS technology scaled to 1 μm, the epitaxial substrate is perhaps insufficient to suppress SCR latch-up. One viable method is to oxide isolate the devices using a trench filled with dielectric material.

CHAPTER 6

EXPERIMENTAL RESULTS

An experimental high frequency and high selectivity switched-capacitor filter was designed and fabricated using our design method. The prototype filter is an elliptic bandpass filter with a center frequency of 260 KHz and a Q of 40. The details of the filter architecture and its design considerations are discussed in Ref. [1]. In this chapter, the performance requirements of the amplifier and the measured results of the filter and the amplifier are presented.

6.1. Amplifier Specifications

The minimum performance specifications for the amplifier are dictated by the filter. The filter parameters are listed in Table 6.1. The maximum pole Q of 120 along with the 4 MHz clock frequency sets the minimum bandwidth of the amplifier. The minimum bias current level is determined by the sampling and the integration capacitors which limit the slew rate. The open loop gain is fixed by the maximum pole Q of the filter.

FILTER PARAMETERS	
Clock Frequency	4 MHz
Filter Q	40
Maximum Pole Q	120
Sampling Capacitor	0.8 pF
Integration Capacitor	2.0 pF

Table 6.1

Filter Parameters

6.1.1. Minimum Gain and Bandwidth Requirements

For a resistively terminated LC filter, the fractional change in the magnitude within the passband can be expressed as

$$\frac{\Delta T(\omega)}{T(\omega)} \approx \frac{1}{2}\left\{\frac{1}{Q_I} + \frac{1}{Q_C}\right\} \omega \tau(\omega) \qquad (6.1)$$

where Q_I and Q_C are the quality factors of the integrators that synthesize the inductors and the capacitors, respectively; $\tau(\omega)$ is the filter group delay; and ω is the frequency of interest [24]. The quality factor of an integrator is approximately equal to the inverse of the total phase error incurred by the integrator. From the analysis presented in Chapter 2, the finite gain causes phase lead, while finite bandwidth induces phase lag. In light of this, the "Q" of a switched-

capacitor integrator can be expressed as

$$\frac{1}{Q} = \Phi_e(finite\ gain) + \Phi_e(finite\ bandwidth)$$
$$= \frac{1}{A_0}\frac{C_s + C_n + C_i}{C_s} - \frac{C_s}{C_i}e^{-T_s\omega_{cl}} \qquad (6.2)$$

The terms are defined as follows:

A_0 is the open loop gain of the amplifier;

C_s, C_n and C_i are the sampling, input parasitic, and the integration capacitors, respectively;

T_s is the total available integration time;

and ω_{cl} is the closed-loop bandwidth of the amplifier.

The 260 KHz elliptic filter was designed to have a nominal Q of 40 and an inband ripple of 1 dB. It is desired that the finite "Q" of the integrators introduce a maximum error within the passband of less than 0.1 dB. From FILSYN simulation results, it is known that the group delay $\tau(\omega)$ is at its maximum at the lower and upper edges of the passband. Using these points as the worst case conditions, the minimum "Q" requirement of the integrators can be computed and are listed in Table 6.2. For a 0.1 dB passband gain error, an integrator Q of approximately

100 is required.

INTEGRATOR REQUIREMENTS			
Bandedge Frequency	Group Delay	Filter Attenuation	Integrator Q
254 KHz	125 μs	-7 dB	88.1
266 KHz	124 μs	-7 dB	91.5

Table 6.2

Minimum Integrator Requirements

Because the phase errors due to finite gain and finite bandwidth have opposite signs, the net phase error is smaller than the individual parts. However, to be safe, both phase errors should be minimized independently.

Gain Requirement

From Eqn. 6.2 we obtain the following relationship

$$A_{omin} = Q \frac{C_s + C_n + C_i}{C_s} \tag{6.3}$$

For the prototype elliptic filter, the value of the parameters are $Q = 100$, $C_s = 0.8\,pF$, $C_i = 2\,pF$, and $C_n = 1\,pF$. The minimum required open loop gain is

$A_{0min} = 475.$

Bandwidth Requirement

Assuming a duty cycle of 40%, the time available for integration is 100 ns. >From Eqn. 6.2 we have that

$$\omega_{cl} = \frac{1}{T_s} \ln\left\{Q \frac{C_s}{C_i}\right\} \tag{6.4}$$

For a $Q = 100$ and $T_s = 100\,ns$, the minimum required closed loop bandwidth is 5.86 MHz. The corresponding unity gain frequency is equal to 9 MHz. This result is in agreement with that presented in ref. [25].

6.2. Differential Amplifier

Two versions of the folded cascode amplifier were designed and fabricated. One version incorporated a triode region operated common mode feedback circuit, while the other uses a saturation region operated feedback. The complete schematic diagrams for both circuits are given in Figs. 6.1 and 6.2.

6.3. Measured Performance

The prototype 260 KHz elliptic bandpass filter was thoroughly evaluated [26]. The effects of amplifier finite gain and bandwidth are evident from the filter response shown in Figs. 6.3. For a large amplifier bias current, the bandwidth is broad but the gain is low. The filter attenuation, therefore, is higher, but the center frequency remains at 260 KHz. This is as predicted from the argument presented in Chapter 1. As the bias current is reduced, the gain of the amplifier

improves but the bandwidth decreases. The finite amplifier bandwidth causes excessive peaking at the bandedge of the filter where the group delay is the largest. Furthermore, the center frequency of the filter shifts down. This is exactly what is observed from the measured response in Figs. 6.3. The theoretical analysis also predicts a small increase in the center frequency for a very small excess phase shift. If the traces of Fig. 6.3.. are examined very carefully, this effect is indeed observed.

Fig. 6.4 shows the frequency response of the filter as a function of the clock frequency. Note that the filter oscillates at a clock frequency of 4.475 MHz. Theoretically, the filter is predicted to operate up to a 7 MHz clock. However, this upper limit has been extrapolated from the differential frequency response of the amplifier. If the common mode frequency response is used instead, the upper limit is approximately 5 MHz clock. This clearly shows that the common mode settling behavior plays a major role in determining the maximum operating frequency of differential switched-capacitor filters.

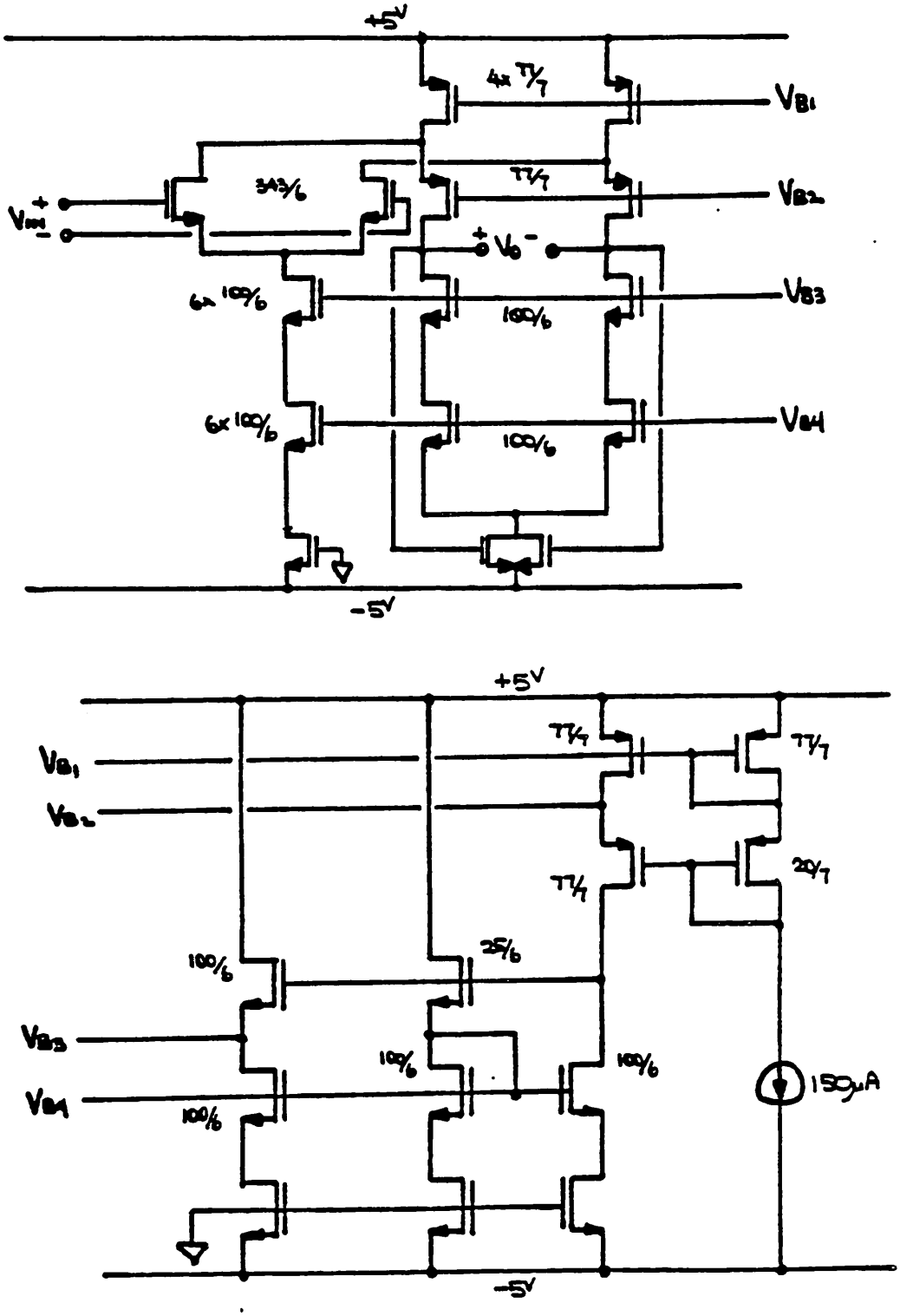


Figure 6.1

Folded-Cascode Amplifier with Triode Feedback

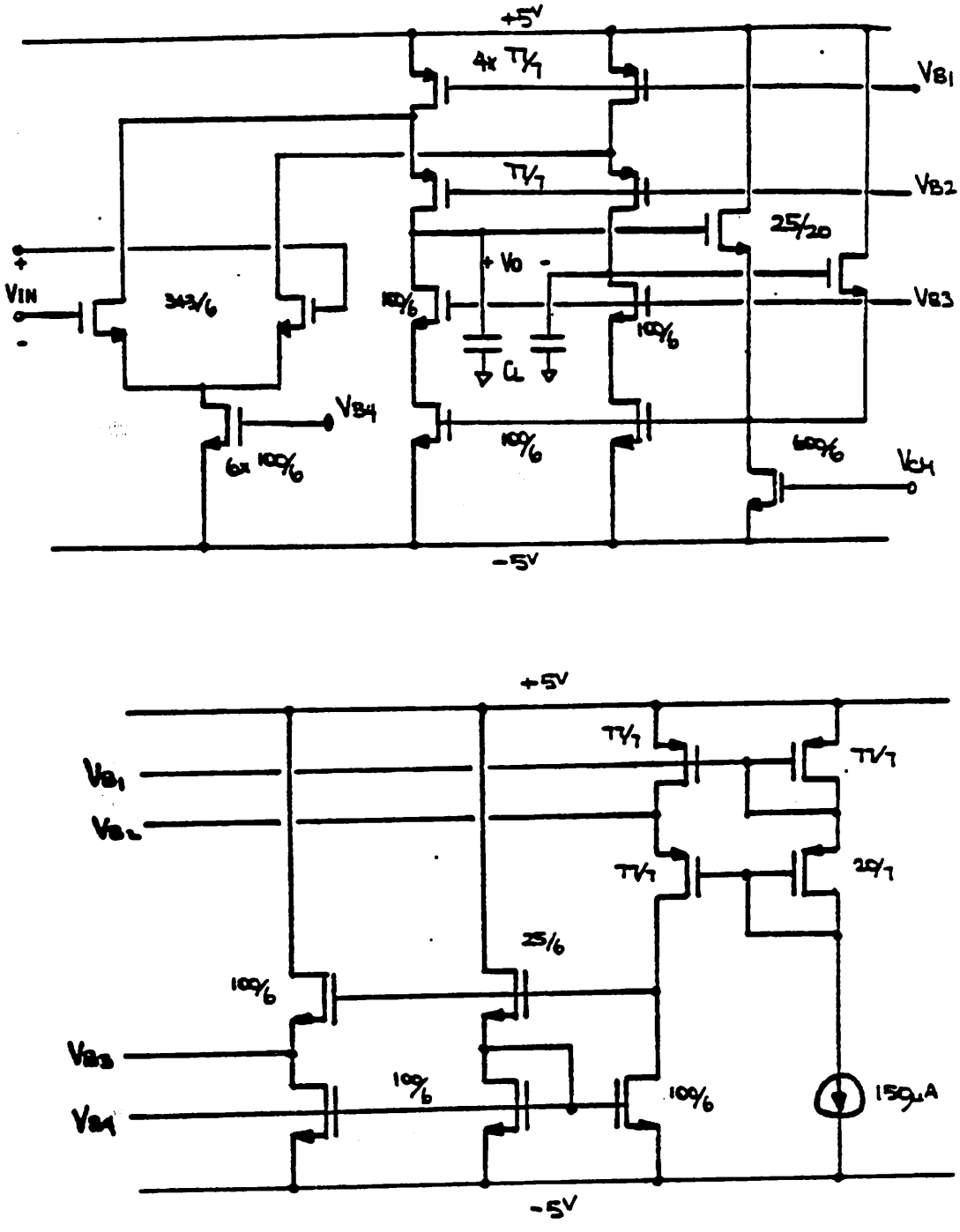


Figure 6.2

Folded-Cascode Amplifier with Saturation Feedback

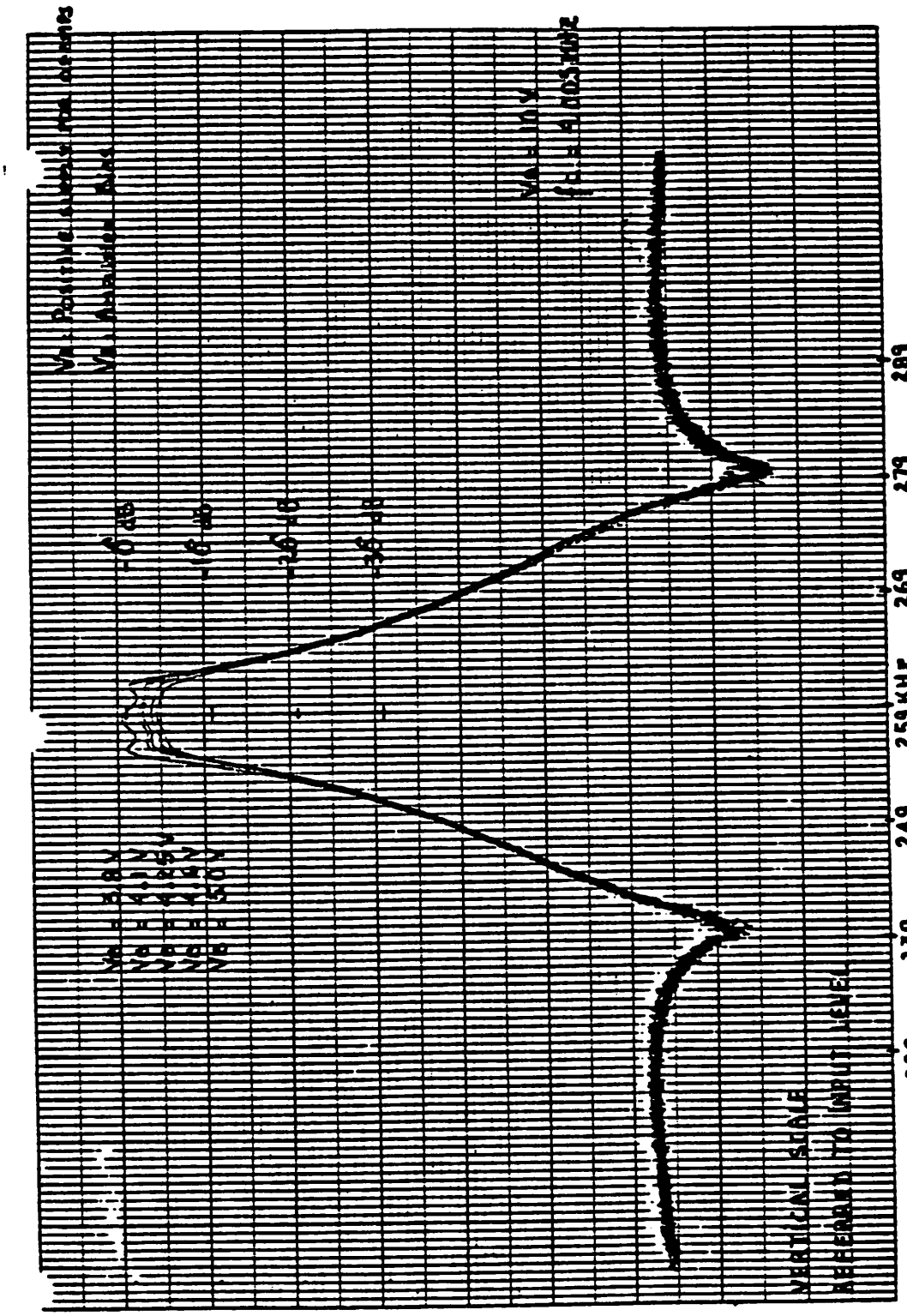


Figure 6.3

Filter Frequency Response as a Function of Bias Current

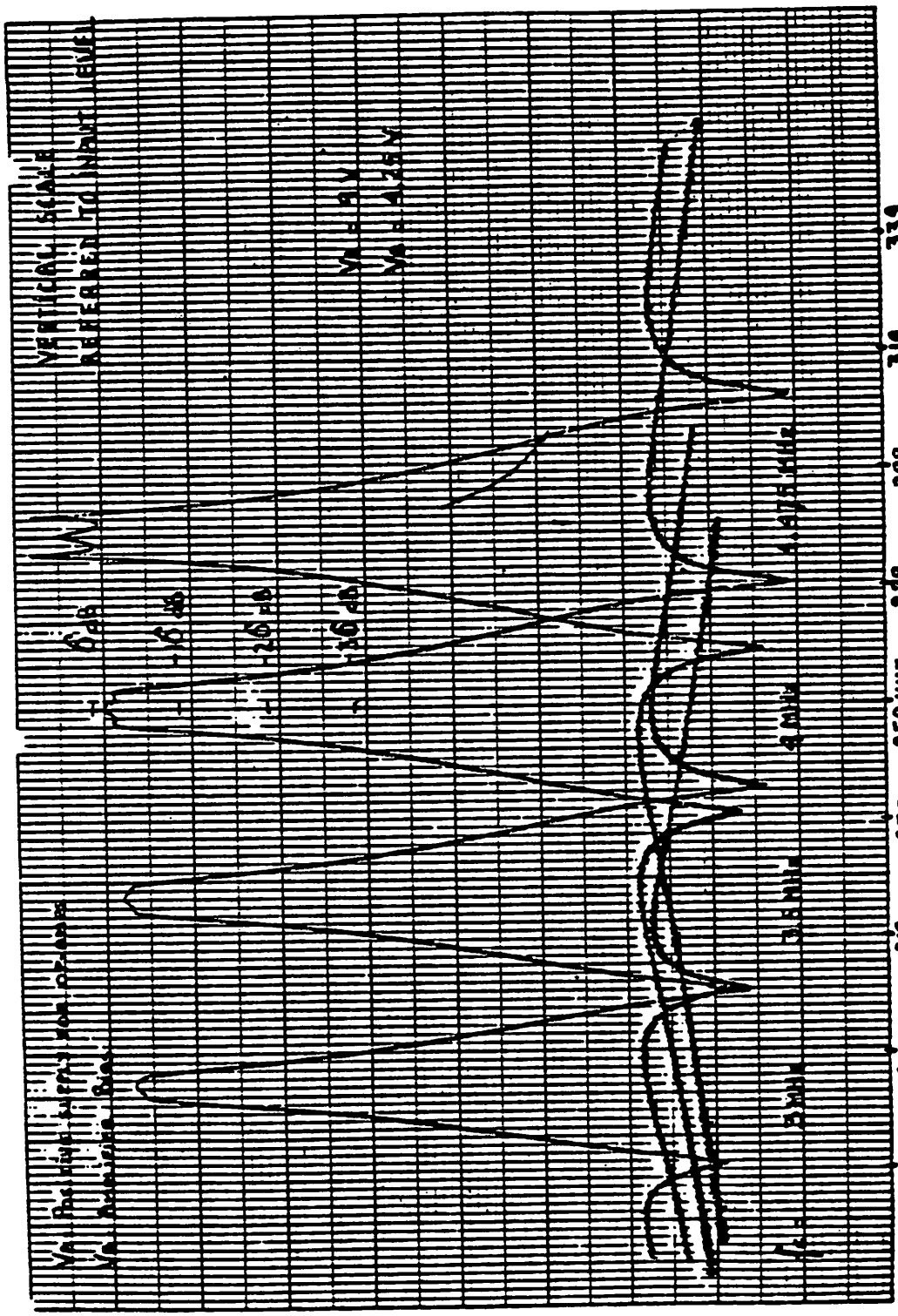


Figure 6.4

Filter Frequency Response as a Function of Clock Frequency

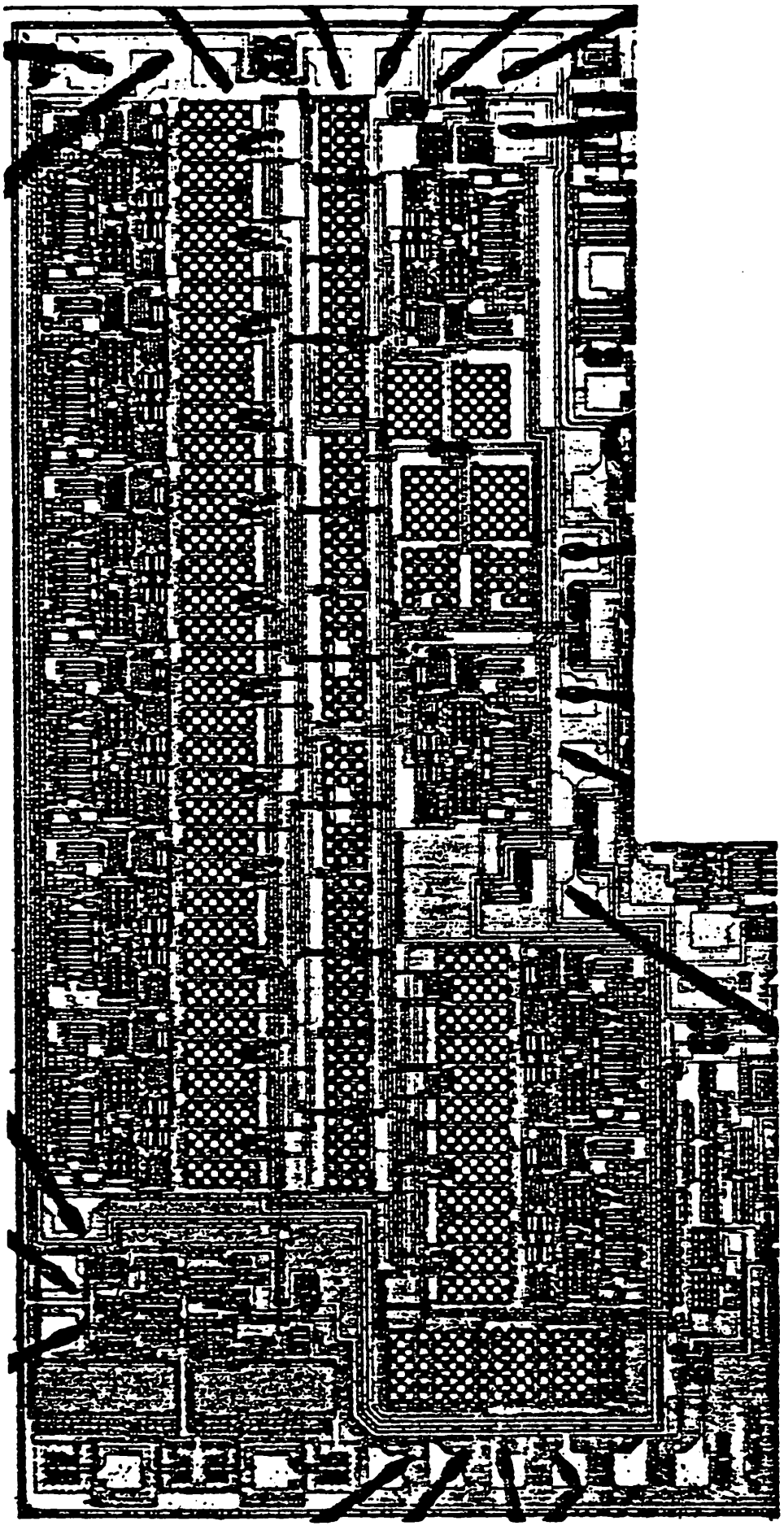


Figure 6.5
Die Photo

CHAPTER 7

CONCLUSION

The experimental results obtained from the sixth order elliptic filter show that high selectivity and high frequency monolithic filters can be realized using the switched-capacitor filtering technique. Using a 4 μm double poly P-Well CMOS technology, a well-behaved 260 KHz bandpass filter can be made with ease.

One clear conclusion can be drawn at this point. The extension of the switched-capacitor filtering technique to higher frequency range will not be limited by the filter architecture. The main obstacle will come from technology and circuit related limitations. A scaled CMOS process will undoubtedly yield faster devices. However, both the transconductance and the output resistance of an MOS transistor degrade as the channel length is reduced to 1 μm and below. Thus, although a fast settling amplifier can be designed using a scaled technology, it is doubtful whether high gain and fast settling amplifier can be made. To complicate the matter even further, to overcome the low breakdown voltage limitation, low voltage MOS design technique need to be developed.

The intrinsic speed of an 1 μm MOS device will be very fast. However, on the system level, the interconnect parasitic capacitance will wreak havoc. In all current CMOS technologies, the interconnect capacitance (that is, the capacitance between two adjacent parallel conductors) is negligible. However, at submicron levels, although the linewidth and the spacing of the metal lines are scaled, the vertical dimension -- metal thickness -- remains essentially unchanged. This dramatically increases the capacitive coupling between two adjacent metal lines, while all other parasitic capacitance are reduced by scaling. Eventually, with

further scaling, the system level performance will reach the point of diminishing return.

From the view point of circuit design, scaled versions of monolithic filters should be of fully-differential configuration. Because of the increase in the parasitic coupling capacitance, a fully balanced signal path will be a necessity. This will bring about some new challenges for the circuit designer. Fast settling, large signal handling differential-to-single ended and single ended-to-differential conversion circuits will be required. Also, a fast settling and low distortion common mode feedback circuit need to be designed for the fully-differential amplifier.

Employing a scaled technology, the realization of high frequency filters that operate in the MHz range is definitely possible. But designing high frequency and high selectivity filters will be difficult primarily due to the low amplifier gain. A multiple filtering approach [1] is one method to get around the low gain limitation; however, at the expense of increased filter complexity. Nonetheless, further refinements and innovation of the amplifier or the integrator are necessary.

REFERENCES

1. T. C. Choi, "CMOS High Frequency Switched-Capacitor Filters," PhD Dissertation, University of California, Berkeley, California, June 1983.

2. K. K. Clarck and D. T. Hess, Communication Circuits: Analysis and Design, Addison-Wesley Publishing Company, Inc., 1971, pp. 25 - 38.

3. P. O. Brackett and A. S. Sedra, "Active Compensation for High Frequency Effects in Op Amp Circuits with Applications to Active RC Filters," IEEE Trans. Circuits Syst., Vol CAS-23, Feb. 1976, pp. 68 - 72.

4. K. Martin and A. Sedra, "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched Capacitor Filters," IEEE Trans. Circuits Syst., Aug. 1981.

5. B. Y. Kamath, R. G. Meyer and P. R. Gray, "Relationship Between Frequency Response and Settling Time of Operational Amplifiers," IEEE Jour. Solid State Circuits, Vol SC-9, No 6, Dec. 1974, pp. 347 - 352.

6. J. G. Graeme, G. E. Tobey and L. P. Huelsman, Operational Amplifiers Design and Applications, McGraw-Hill, 1971, pp. 186 - 197.

7. P. E. Gray and C. L. Searle, Electronic Principles: Physics, Models and Circuits, John Wiley, Inc., 1969, pp. 673 - 719.

8. R. G. Meyer, "Class Notes for EECS 241," University of California, Berkeley, California, 1979.

9. R. G. Meyer, "Class Notes for EECS 240," University of California, Berkeley, California, 1980.

10. J. E. Solomon and G. R. Wilson, "A Highly Desensitized, Wideband Monolithic Amplifier," IEEE Jour. Solid State Circuits, Vol SC-1, No 1, Sept. 1966.

11. P. R. Gray, D. A. Hodges and R. W. Brodersen, Analog MOS Integrated Circuits, IEEE Press, 1980.

12. K. C. Hsieh, "Noise Limitations in Switched-Capacitor Filters," PhD Dissertation, University of California, Berkeley, CA, May 1982.

13. D. Senderowicz, S. F. Dryeyer, J. H. Huggins, C. F. Rahim and C. A. Laber, "A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip," IEEE Jour. of Solid State Circuits, Vol SC-17, No 6, Dec. 1982.

14. E. Toy, "An N:MOS Operational Amplifier," Digest IEEE Int'l. Solid State State Circuits Conference, Feb. 1979.

15. V. K. Reddi and C. T. Sah, "Source to Drain Resistance Beyond Pinch-off in MOS Transistors," IEEE Elect. Devices, Vol ED-12, 1965, p. 139.

16. R. H. Dennard, F. H. Gaenssler, E. J. Walker and P. W. Cook, "1 Micron MOSFET VLSI Technology: Part II -- Device Designs and Characteristices for High Performance Logic Applications," IEEE Trans. Elect. Devices, Vol ED-26, No 4, Apr. 1979, pp. 325 - 333.

17. L. Risch, C. Werner, W. Muller and A. Wieder, "Deep-Implant 1 Micron MOSFET Structure with Improved Threshold Control For VLSI Circuitry," IEEE Trans. Elect. Devices, Vol ED-29, No. 4, Apr. 1982, pp. 601 - 606.

18. J. Barnes, K. Shimohigashi and R. Dutton, "Short-Channel MOSFET's in the Punchthrough Current Mode," IEEE Trans. Elect. Devices, Vol ED-26, No. 4, Apr. 1979, pp. 446 - 452.

19. R. S. Muller and T. I. Kamins, Device Electronics For Integrated Circuits, John Wiley and Sons, Inc., 1977.

20. R. R. Troutman, "VLSI Limitations from Drain-Induced Barrier Lowering," IEEE Trans. Elect. Devices, Vol ED-26, No 4, Apr. 1979, pp. 461 - 467.

21. S. Ogura, P. J. Tsang, W. W. Walker, D. L. Critchlow and S. F. Sheperd, "Design and Characteristics of Lightly Doped Drain-Source (LDD) Insulated Gate Field-Effect Transistor," IEEE Trans. Elect. Devices, Vol ED-27, No 8, Aug. 1980, pp. 1352 - 1358.

22. Y. El Mansy, "Limitations of Scaled MOS Technology," IEEE Symp. VLSI Technology, Aug. 1981.

23. F. C. Hsu, P. K. Ko, S. Tam, C. Hu and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," IEEE Trans. Elect. Devices, Vol ED-29, No 11, Nov. 1982, pp. 1735 - 1740.

24. L. T. Bruton, "Multiple-Amplifier RC-Active Filter Design with Emphasis on GIC Realizations," IEEE Trans. Circuits Syst., Vol CAS-25, Oct. 1978, pp. 830 - 845.

25. K. Martin and A. Sedra, "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., Aug. 1981.

26. C. L. Hoang, "Evaluation of a Fully-Integrated High Frequency Switched-Capacitor Bandpass Filter," MS Report, University of California, Berkeley, California, Sept. 1982.