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HIGH SPEED DIGITAL-TO-ANALOG CONVERSION

by

V. W-K. Shen

Memorandum No. UCB/ERL M83/70

10 November 1983

(Crown)
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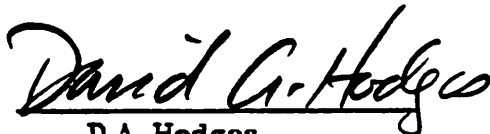
ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

TITLE PAGE

Vivian Wah-Kwan Shen

Ph.D Electrical Engineering
and Computer Sciences



D.A. Hodges
Chairman of Committee

ABSTRACT

This thesis reports on a study of fundamental techniques for improving the performance of high speed digital-to-analog (D/A) conversion. A new configuration to be described eliminates previous 1) component matching requirement for differential linearity 2) slew rate suppression for low output glitch 3) bipolar or hybrid technology dominance in speed. The sequential current selection (SCS) configuration consists of $2^N - 1$ identical, independently controlled current sources which are monotonically selected via 2-dimensional linear string decoding. A simple glitch-free current cell design eliminating residual glitch sources is also developed.

Advantages of the new converter configuration were verified by design and fabrication of 8 bit SCS D/A converter fabricated in NMOS polysilicon gate technology. Measurements showed that output current settling time is 80 ns under external loading of 180 Ω and 20 pF. The converter output waveform exhibits no glitch for input skew under 25ns.

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i

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TABLE OF CONTENTS

ii

Chapter 1- INTRODUCTION.....	1
Chapter 2- HIGH SPEED D/A CONVERTER CIRCUIT CONFIGURATION.....	4
2.1 Classical Current Steering D/A Converter.....	5
2.2 Fast Bipolar and MOS Current Steering D/A Converters.....	12
2.3 Sequential Current Selection D/A Converter.....	17
2.4 Glitch Performance of SCS D/A converter.....	20
Chapter 3 - LINEAR STRING DECODING.....	27
3.1 Monotonic Decoder Design.....	27
3.2 Linear String Monotonic Decoder.....	31
Chapter 4 - CURRENT SOURCE DESIGN.....	43
4.1 Current Cell Configuration.....	43
4.2 Resolution Limitation of Converter.....	45
4.3 Possible Error Types in SCS D/A converter.....	50
4.4 Output Noise of SCS D/A Converter.....	51
Chapter 5 - PERFORMANCE EVALUATION AND CONCLUSION.....	54
5.1 Performance Evaluation.....	54
5.2 Conclusion and Future Design Consideration.....	58
APPENDIX I - ERROR TYPES OF D/A CONVERTER.....	62
APPENDIX II - PROCESS FLOW.....	63
REFERENCES.....	71

INTRODUCTION

Digital-to-analog converters for high performance signal processing systems are required to have 8 to 12 bits resolution, below 100 ns conversion time, and less than $\frac{1}{2}$ least significant bit (LSB) output glitch amplitude. 12 bits resolution data conversion is readily achievable via techniques such as component trimming [1], digital error correction [2], or conversion process partitioning [3]. Conventional output deglitching approach usually employs high speed amplifiers in a feedback configuration to suppress glitch magnitude [4]. However, the design of a D/A converter becomes more critical when high resolution and low glitch requirement are compounded with the need for fast settling time.

Currently, monolithic D/A converters meeting these requirements are available only in bipolar technology. The high current driving capability of bipolar devices is necessary in fast amplifier designs for use in the deglitching and/or conversion circuits. High performance D/A converters are also available in higher cost hybrid technology which combine optimum components from different technologies to achieve the required performance. However, with the current availability of MOS VLSI technology, it would be cost and speed effective to integrate a high performance MOS D/A converter with a digital signal processor on the same chip. The focus of this research is to develop fundamental circuit design techniques for achieving high performance D/A converters in MOS VLSI technology. The realization of a high performance MOS D/A converter will also demonstrate the potential of MOS technology in certain high performance analog circuits which have been dominated by bipolar or hybrid technologies.

A conventional high speed D/A converter technique used in both bipolar and hybrid realization is current steering [5]. Contributing binary weighted current sources are differentially switched to the output load based directly on the input code. In order to minimize the output voltage swing and its loading effect on the current source, the LSB unit current is kept at low microampere range. At such constant, low current the high driving power of bipolar devices is never utilized. Thus conversion time is determined mainly by device switching time and output resistive and capacitive loading, rather than by device driving capability as would otherwise be true in a complicated circuit.

Under these conditions, comparable speed performance could be achieved if the current steering D/A converter configuration were implemented in MOS technology. However, there are two types of problem in the design of a MOS current steering D/A converter. First is the poor matching of active MOS transistors which might define ratio accurate current sources. Secondly, the strong transient glitches normally associated with a current steering D/A configuration require deglitching sample-and-hold amplifiers. The deglitching circuits realized in MOS technology are too slow to be useful in high speed D/A converters.

A new D/A conversion configuration proposed in this dissertation has two major advantages:

- (1) differential linearity of the converter does not depend upon the matching the unit current sources,
- (2) the design eliminates the need of complicated circuits normally used to deglitch the output waveform.

The proposed circuit techniques were demonstrated through a prototype D/A converter. It was realized in NMOS polysilicon gate technology. The power

dissipated is low because of low unit current. The NMOS current cell design is very simple which does not require P-channel devices. In single stage design which the new D/A converter configuration is primarily comprised of, CMOS technology may suffer because of double Miller effect and no substrate bias to reduce junction capacitance. However, when complicated digital functions are integrated together with the D/A converter, CMOS technology might yield definite advantage.

The sequential current selection (SCS) D/A conversion technique is presented in Chapter 2. In Chapter 3, a new linear string decoding scheme is described. This decoding scheme achieves monotonic decoding in two dimensions to minimize circuit complexity and decoding delay. Chapter 4 addresses the design of unit current source and the performance limitations associated with SCS D/A conversion scheme. Performance evaluation of the experimental D/A converter and conclusion are presented in Chapter 5.

CHAPTER 2

HIGH SPEED D/A CONVERTER CIRCUIT CONFIGURATION

MOS technology provides the most economical realization of complicated digital functions. It is inferior to bipolar technology in speed performance. MOS devices have relatively low current/area and transconductance/area compared to bipolar devices. MOS devices have additional gate capacitances which load down previous stages. These inherent drawbacks have led to poor frequency response in MOS amplifiers. Therefore, weighted capacitor [6,7] and R-2R resistive ladder [8] D/A circuit configurations requiring amplifiers in closed-loop configuration are not suitable for fast MOS D/A converters. Other parallel D/A techniques such as resistive string [9] produce a direct voltage output. In certain applications, the voltage output can directly drive a resistive load or long lengths cable with proper termination. This situation eliminates the need of a unity gain buffer amplifier and yields considerable speed improvement. But the choice of direct voltage conversion variable results in high on-chip impedance and is not the optimum design for a high speed D/A converter.

Currently, video D/A converters implement a current steering algorithm. Typical bipolar and MOS implementations of current steering D/A converters are described in Section 2.1. In Section 2.2, an alternative high speed D/A conversion algorithm is proposed to which achieves better resolution and output glitch performance while maintaining design simplicity which is crucial for high speed operation. In Section 2.3, output glitch performance of both earlier and the proposed current steering D/A converter designs will be discussed.

2.1. CLASSICAL CURRENT STEERING D/A CONVERTER

A block diagram of conventional steering D/A converter is illustrated in Figure 2.1. In this configuration, there is no decoding stage. Data conversion is accomplished by having the array of current sources binary ratioed. The digital input code is applied directly to the switches at the top. Each bit, being either a one or zero, controls the switch position to be either at the right or left respectively. The binary weighted current sources below are then passed either to the true output line or to an output complement line. An analog output current proportional to the digital input code is therefore produced. To develop an analog output voltage, the output current can drive into a configuration as shown in Figure 2.2. The D/A converter current driving into a feedback resistor, R_F , produces an output voltage given in the expression below:

$$V_{out} = -I_{out} R_F \quad (2.1)$$

Because the D/A converter output is driving into amplifier's summing node, the effective input impedance is expressed as:

$$R_{in} = \frac{R_F}{1+A_{OL}} \quad (2.2)$$

A_{OL} is the amplifier open loop gain. Therefore, D/A converter's output voltage swing is minimized. Amplifier's output voltage swing is maximized by using a large feedback resistor. If current sources were also defined by resistors, an on-chip R_F promotes optimum temperature tracking. Output voltage drifts is lower than when an external feedback resistor is used. However, this will limit the amount of voltage swing.

To match the high speed performance of the core D/A converter, the output settling response of the amplifier must also be optimized. A critical requirement of fast settling op-amp is to possess a single-pole open loop gain

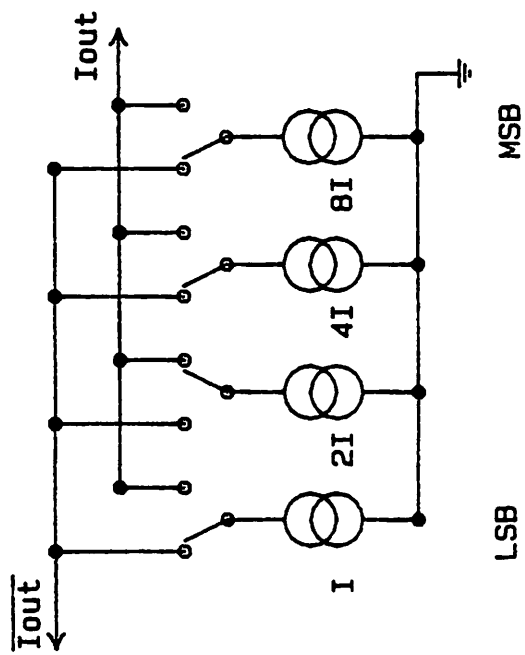


Fig.2.1 Current Steering DAC Block Diagram

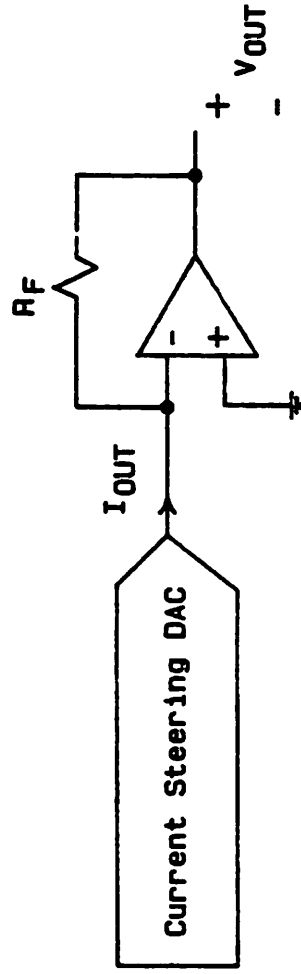


Fig.2.2.2 Current - Voltage Conversion Buffer

characteristics as shown in Figure 2.3. Figure 2.4 is a plot of percentage output error versus single time constant τ where

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f} \quad (2.3)$$

f is defined to be the closed loop 3dB bandwidth of the amplifier. For 8 bit resolution, seven τ is the calculated minimum. In practice, a single pole amplifier can take much longer to settle than predicted. This is due to slew rate limitation, higher order poles, and overload recovery time. For ultra high speed operation, this output configuration is primarily limited to modular hybrid, or monolithic bipolar technology implementation.

An alternative output circuit which MOS VLSI technology potentially can provide 30 MHz operation is shown in Figure 2.5. In this current to voltage conversion circuit, the D/A converter output current drives directly a load resistor, R_{Load} , typically in the range of 50 Ω to 500 Ω . The voltage drop across the load resistor is amplified and buffered through the wideband amplifier. The final output voltage is expressed as follows:

$$V_{out} = -A_v I_{out} R_{load} \quad (2.4)$$

A prototype of a NMOS wideband amplifier designed by Soo [10] is fabricated at Bell Laboratories, Holmdel.

Current steering D/A converter accuracy depends upon current sources matching. For identical resolution, current source matching requirements can be reduced by cascading several lower order D/A converters. However, such a conversion scheme tends to result in slower performance than a single stage design because of the added signal delay in propagating through several stages.

The conversion speed of a current steering D/A converter is limited by switching circuits' delay and output RC delay. Typically, the RC factor

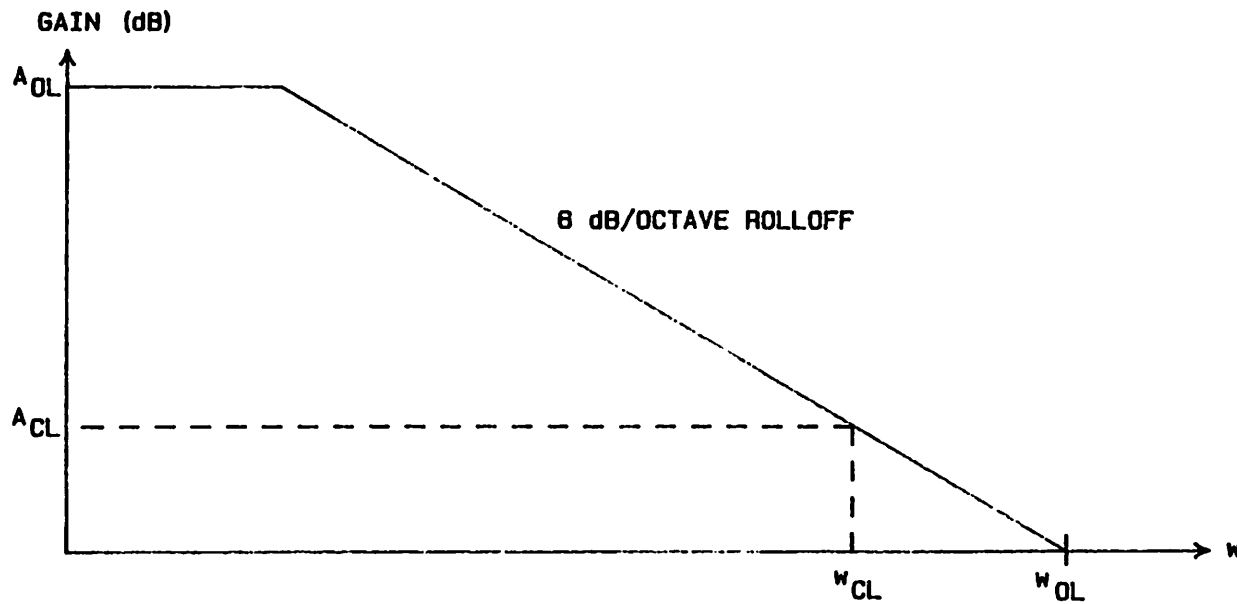


Fig.2.3 Op-Amp Gain Curve with Single Pole Roll-Off

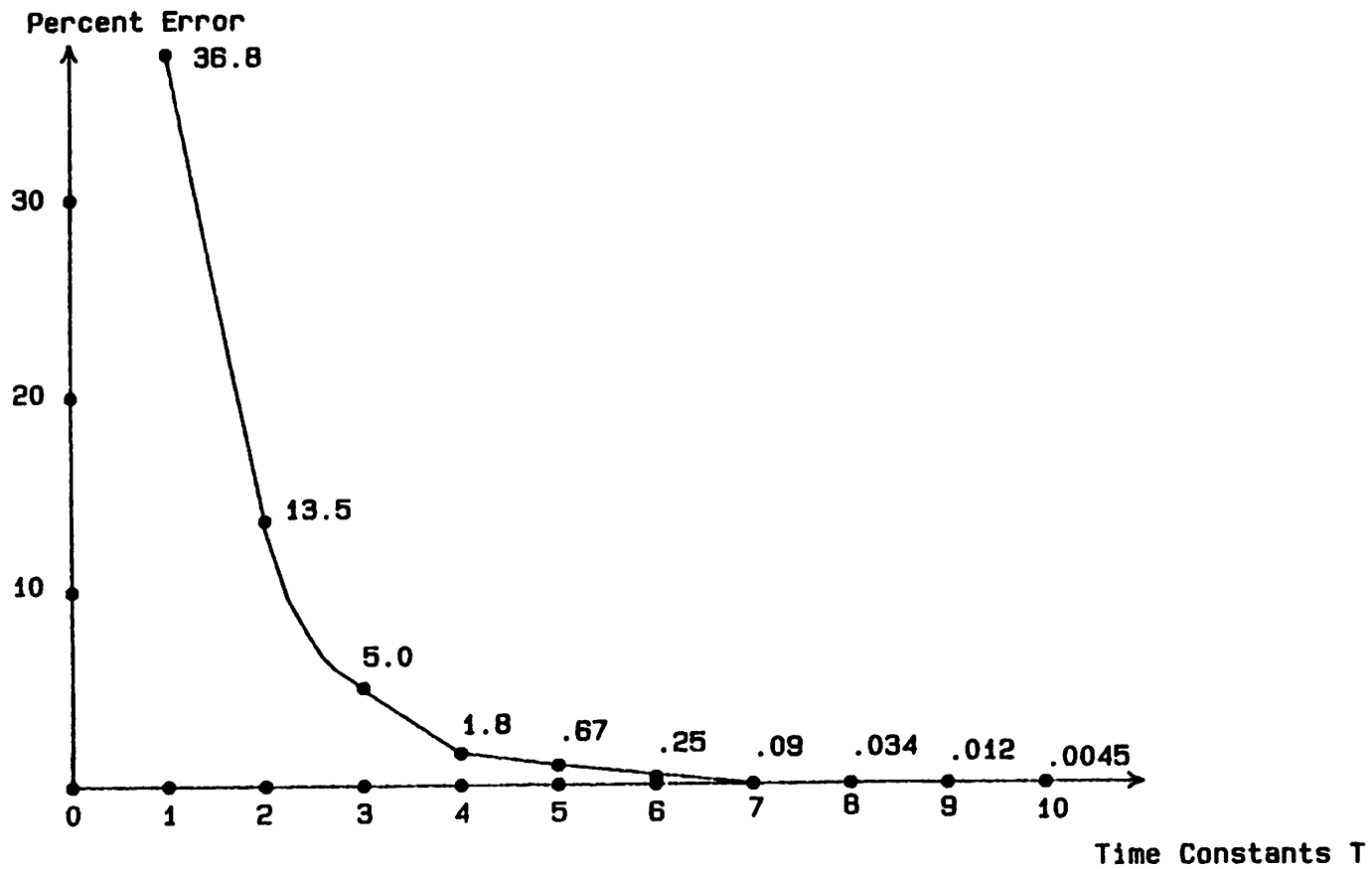


Fig.2.4 Output Error versus Time Constants

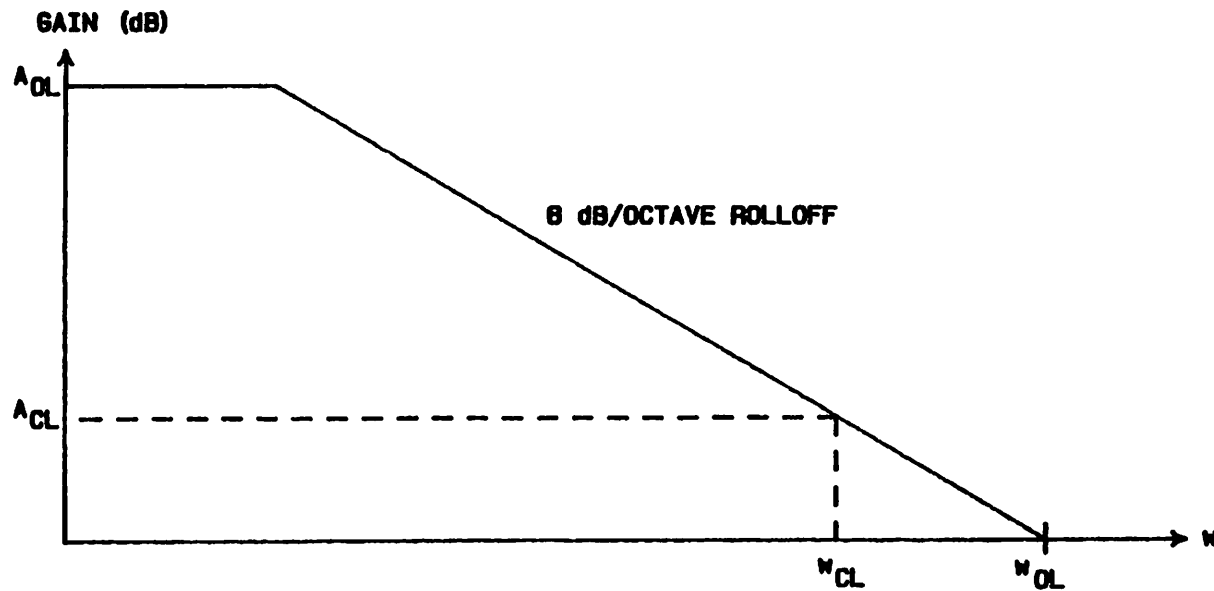


Fig.2.5 Op-Amp Open Loop Voltage Gain vs Frequency

dominates. An equivalent output circuit of a current steering D/A converter is shown in Figure 2.6. I_{out} is the total output current. C_{out} is the lumped parasitic capacitance. R_{out} is the effective load resistance. For high speed operation, both R_{out} and C_{out} must be minimized.

In a 10 or 12 bit current steering D/A converter, unit current is generally in the low range of $5 \mu A$ or $2 \mu A$, respectively. The goal is to achieve low voltage swing and thereby more stable ratio accurate constant current sources. At such low current level, the device current driving capability becomes insignificant in determining circuit operating speed. Therefore, current steering D/A converter circuit configuration can universally be implemented in any technology. Under identical operating conditions, speed performance should be fairly uniform. In the next section, different current steering D/A converter designs which have been implemented in different monolithic technologies will be described.

2.2. PAST BIPOLAR AND MOS CURRENT STEERING D/A CONVERTERS

A typical bipolar implementation of this type of converter is shown in Figure 2.7. The ratio accurate current sources are generated through a resistor network which is connected to the emitters of collector switched NPN devices. The general expression for collector current is:

$$I = \frac{g_m V_{bias}}{R (1 + g_m R)} \quad 1 \leq n \leq N \quad (2.5)$$

For bipolar devices, $g_m R \gg 1$, thus I is dependent only on the emitter resistor R . The R-2R network has the advantage of minimizing total resistance unit and requiring only two accurate values of R and $2R$. The converter transfer function is always monotonic even if the resistors are greatly mismatched. Therefore, matching and tracking of resistors are simplified. Diffused resistors with high temperature and voltage coefficients, and high sensitivity to processing can be

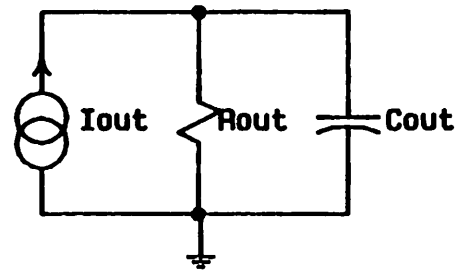


Fig.2.6 Output Model of Current Steering DAC

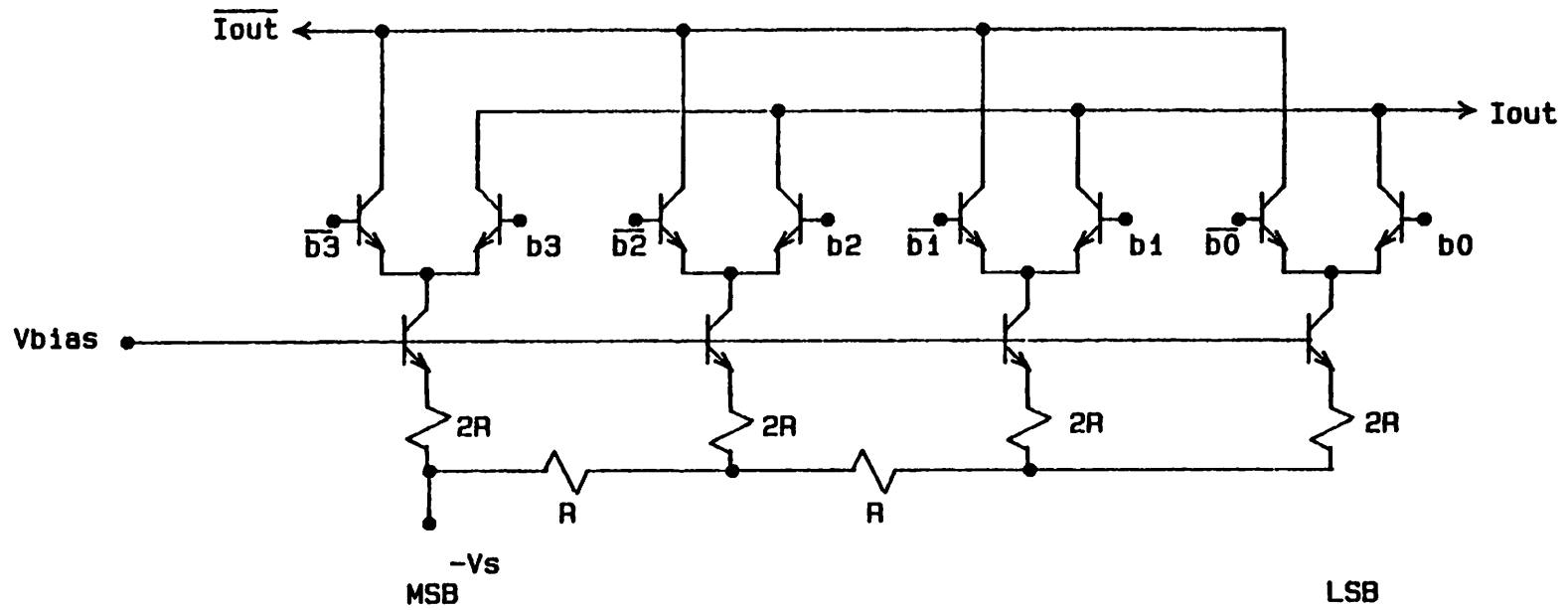


Fig.2.7 Bipolar R-2R Current Steering DAC

utilized. With temperature coefficient of diffused resistors around 1500ppm/°C from 0°C to 125°C, this type of D/A converter is limited to 8 bit resolution. 10 bit resolution can be achieved with added provision of external laser trimming of higher order bit resistors.

A similar D/A circuit configuration as shown in Figure 2.8 has more stringent component matching requirement. For optimum matching, each binary ratioed constant current contains a binary collection of unit current. Each unit current is defined as:

$$I = \frac{g_m V_{bias}}{R(1 + g_m R)} \quad (2.6)$$

For $g_m R \gg 1$, I is equal to $\frac{V_{bias}}{R}$. A total of 255 unit resistors R are required for 8 bit resolution. To guarantee monotonicity, the resistor pair must match to $\frac{1}{2}$ LSB. This implies that less than .195% of component mismatch is allowed for an 8 bit D/A converter of this type. Ion-implanted resistors with better than .1% matching have been reported to be used by Saul [5]. Optimum matching among current sources is also promoted because identical voltage drops appears across all current defining resistors. Thus, this type of converter exhibits better linearity characteristics than the previous R-2R network converter in which potentials appearing across precision resistors are binary ratioed. In both bipolar current steering D/A converter configuration, a reference amplifier and reference control resistor are used to bias the current sources from a stable external voltage reference.

In MOS technology, the implementation of the current steering D/A configuration is similar to the bipolar case except for the weighted current sources. At a 10 μ A current level, MOS devices have about 40 times lower transconductance than bipolar devices. Typical diffused resistors available with

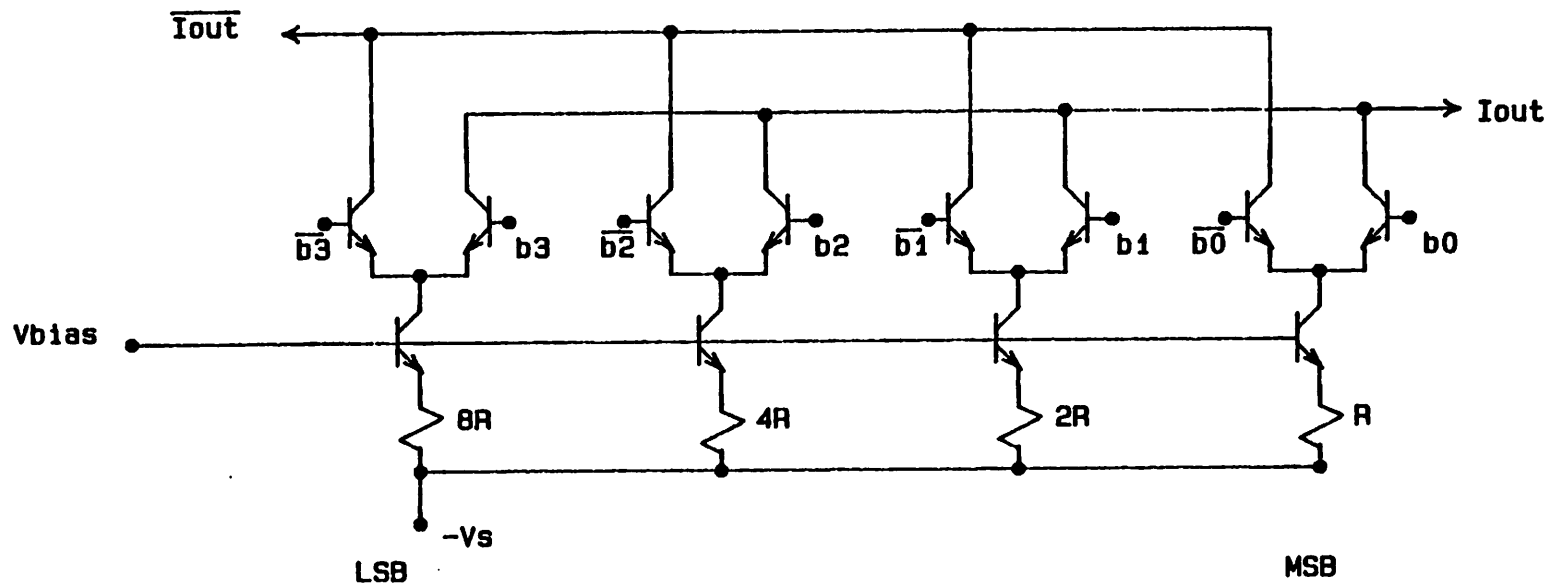


Fig.2.8 Bipolar Current Steering DAC

standard NMOS technology are in the range of 40~60 Ω /square. Higher valued, better controlled ion-implanted resistors are not readily available in standard NMOS process. The on-resistance of MOSFETs in linear region can be made sufficiently high to compensate for the low g_m . However, the body bias effect on the emitter degenerated MOS device would limit the final feedback factor to approximately 20. This is an order of magnitude lower than that attainable in an equivalent bipolar circuit. Resistor R controlling each branch current becomes an added variable rather than the effective element defining the unit current. Thus, in MOS technology, the current array can be realized with active MOS devices biased into the saturation region. A general configuration is shown in shown in Figure 2.9. The unit drain current is defined as follows:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{Z}{L} (V_{bias} - V_T)^2 \quad (2.7)$$

Current produced from active devices may vary due to the combined effect of geometry, mobility, threshold voltage, doping, and oxide thickness variations. Therefore, matching quality of active devices is poorer than that of passive resistors or capacitors. A pair of nominally identical 1 mil^2 gate area MOS transistors has been reported to be matched to .3% in drain current after processing [3]. Based on this data, 8 to 10 bit differential linearity is potentially difficult to achieve without partitioning the conversion. However, settling time of a serial converter will be increased. A new D/A circuit configuration is proposed to remove component matching requirements which prevails in all existing D/A converter designs.

2.3. SEQUENTIAL CURRENT SELECTION D/A CONVERTER

The sequential current selection D/A configuration shown in Figure 2.10 employs $2^N - 1$ identical current sources, but each is independently controlled.

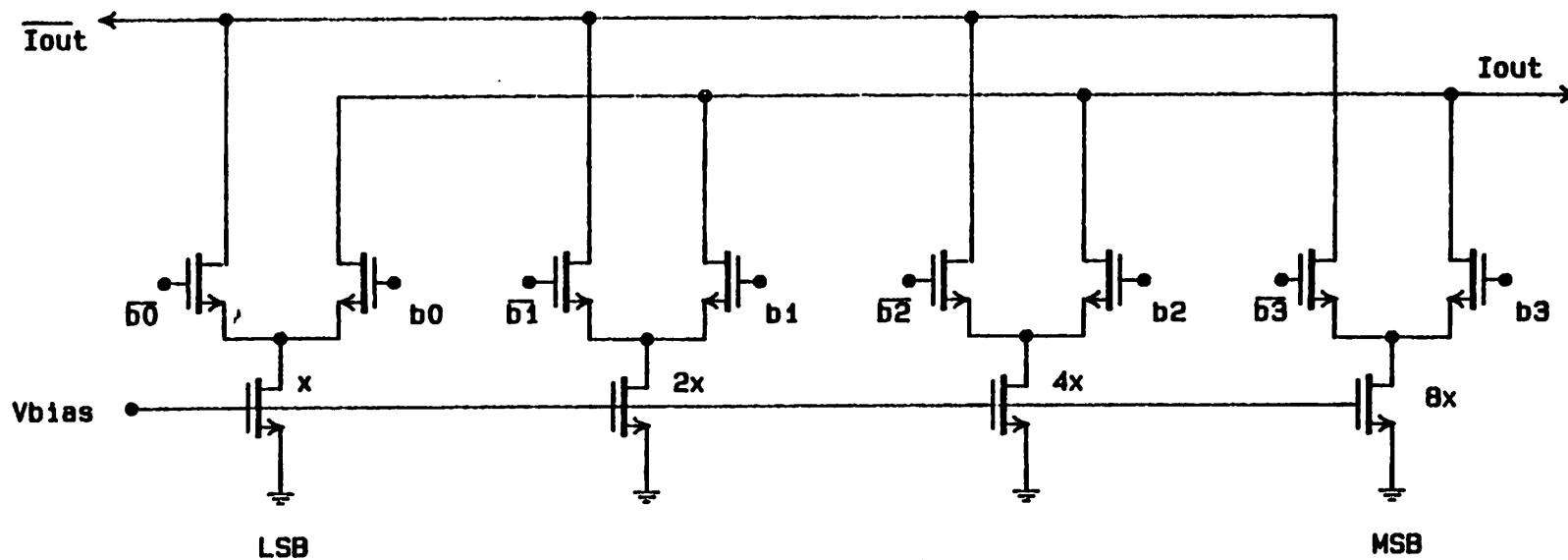


Fig.2.9 MOS Current Steering DAC

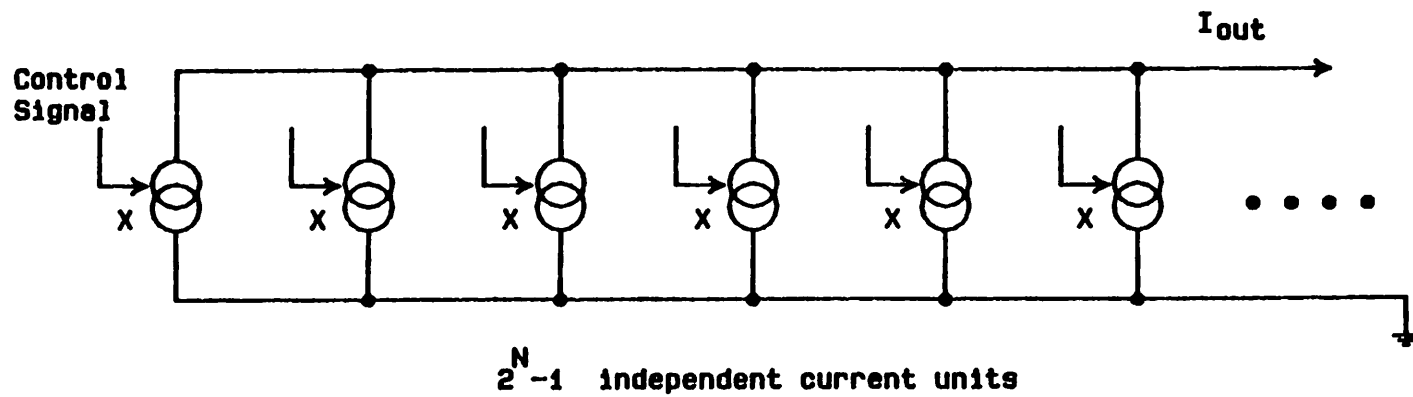


Fig.2.10 Sequential Current Selection DAC

The increased circuit complexity is acceptable for monolithic MOS implementation. The current sources are addressed in linear order. A group of current sources are turned on and summed at the output. The group size is increased by adding adjacent unit currents when the input code increases. When the input code decreases, the group size is decreased by turning off existing unit current. In this addressing format, steady state monotonicity is guaranteed because each analog step increment corresponds to adding another unit current to the existing output. For this design a voltage output is developed by passing the final output current through a low output resistor, typically 50 Ω , to match transmission line impedance. Thus the fundamental limit on converter resolution is the ratio of net current source output resistance to the load resistance.

2.4. GLITCH PERFORMANCE OF SCS D/A CONVERTER

Most high speed D/A converters used in interfacing digital video signals to the CRT displays must exhibit less than $\frac{1}{2}$ LSB output glitch amplitude. This avoids character or figure distortions in the displays. The D/A converter transfer function should be as shown in Figure 2.11a whereby each new step is a smooth, continuous transition from the previous one. The waveform in Figure 2.11b exhibits output spikes. Thus a pertinent requirement for video D/A converter is to guarantee both transient and steady state monotonicity.

Most video D/A converter products available today are deglitched with extra circuits which are mostly in hybrid technology because of the critically high speed. A circuit used by Burr-Brown [4] to deglitch its hybrid high performance D/A converter is shown in Figure 2.12. It requires high speed amplifier, diode bridge, high speed Schottky register, and driver. The diode bridge clamps the summing junction as close to ground potential, thereby suppressing the D/A converter's current glitch so it does not reach the amplifier. The diodes when

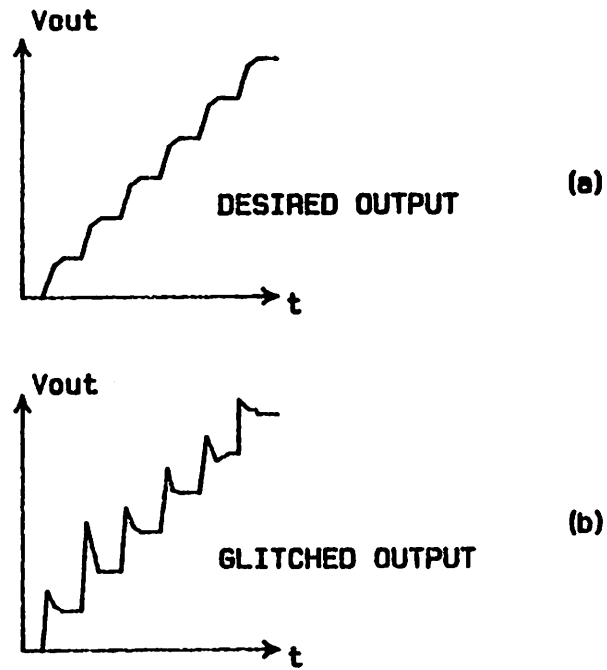


Fig.2.11 DAC Output Waveform

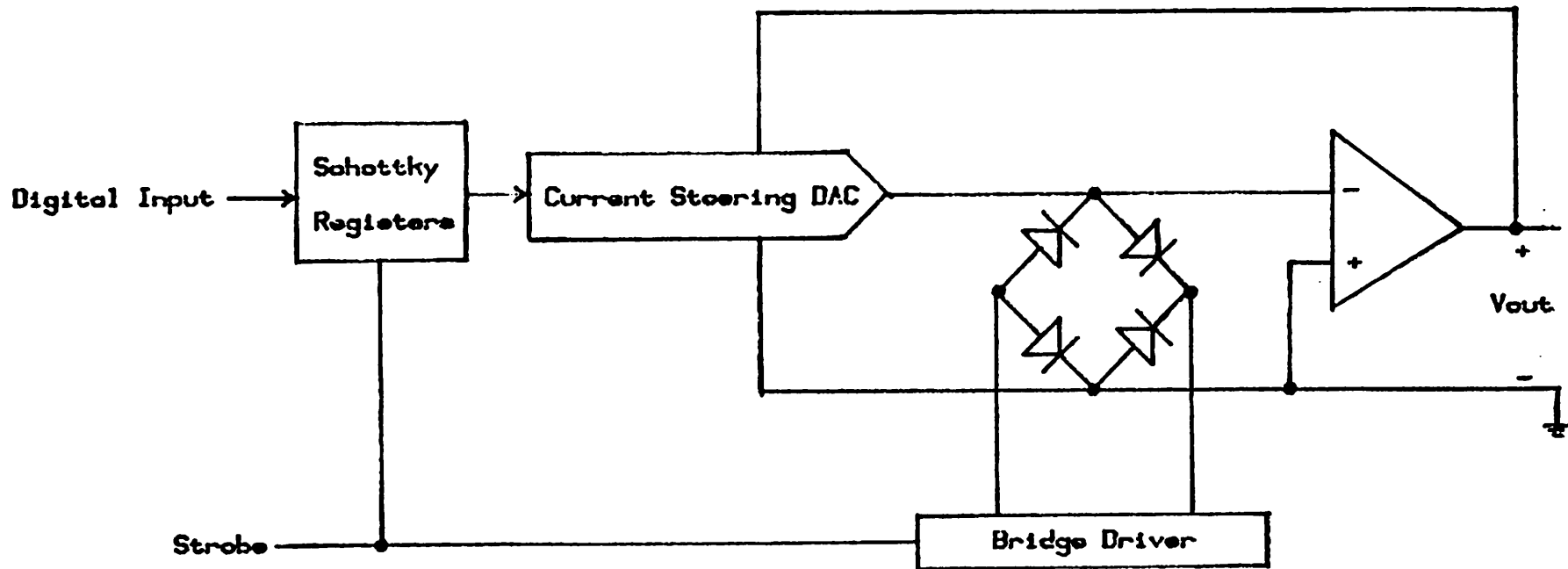


Figure 2.12 Feedback Deglitched Bridge

turned on by a glitch pulse provide a low impedance path for the glitch to flow to ground. Both this method and the sample-and-hold technique which is most suitable for MOS technology, require amplifier in feedback configuration. Because of the relatively poor frequency response of MOS amplifiers, the settling time would be too slow.

An alternative method is to filter the D/A converter current output. A large output resistive load with the parasitic capacitance constitute a low-pass filter stage to dampen output transients. As mentioned earlier, conversion speed is directly related to output RC time constant. Therefore, this approach would lead to slower speed performance. To depart from traditional methods of glitch amplitude suppression at the output node, a more fundamental approach of eliminating potential glitch sources in the design is taken so as to achieve a low glitch output response in the proposed D/A converter.

A major distinction between past current steering and sequential current selection D/A configurations is illustrated in Figures 2.13 and 2.14. This difference is crucial in achieving improved glitch performance in the proposed D/A converter design. In past current steering D/A converters, the constant current sources are separated from the output terminal by switching circuits which harbor several glitch sources. The switching is accomplished in differential mode because it minimizes voltage swing and is thus faster. However, differential switching causes glitches when:

- 1) rise and fall time of true and complement input are unequal,
- 2) device turn-on and turn-off physical processes are mismatched,
- 3) residual channel charge are injected to the output,
- 4) signals are capacitively coupled to the output,

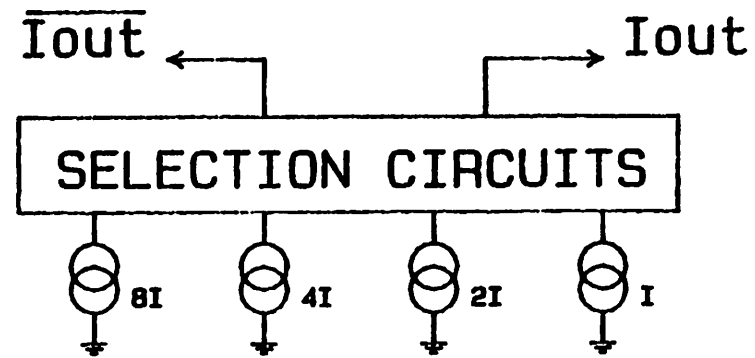


Fig.2.13 Past Current Steering DAC Block Diagram

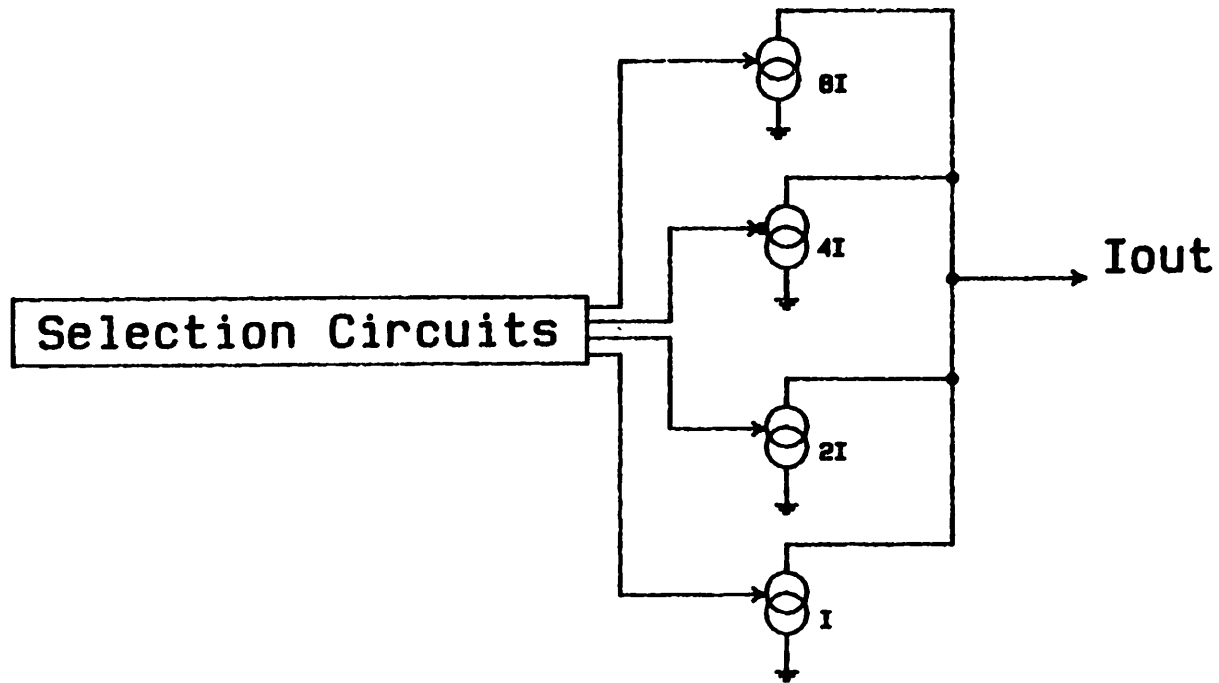


Fig.2.14 Sequential Current Selection DAC Block Diagram

5) devices are switched into the linear region from an off state causing electrons to backflow into the channel region from the drain electrode.

These glitch contributors are almost impossible to eliminate. Furthermore, in the past current steering D/A converter algorithm, a new analog output may be produced by switching between two or among several different groups of current sources. The small time mismatch in the multiple switching operations due to imperfect synchronization is another source of glitches.

For the sequential current selection D/A converter, a new analog output is never achieved as difference between current added and current subtracted. This eliminates the potential problem of synchronizing multiple operations. Referring to Figure 2.14, all necessary decoding and current source control for sequential current selection D/A converter are developed and performed at the front-end. Only unit currents are connected to the output. Potential glitch sources in the selection circuits are isolated from output. To achieve the desired output waveform, it remains only to develop a suitable unit current cell design as described in the Chapter 4.

CHAPTER 3

LINEAR STRING DECODING

The key circuit element required for a sequential current selection D/A converter is a monotonic decoder. A past circuit design providing such function proposed by Schoeff [9] is described in the first part of this Chapter. However, the complexity of this decoder has limited its usage to decoding only 3 or 4 bits. In the proposed D/A converter configuration, sequential control signals are generated with a two-dimensional linear string decoder. The new monotonic decoding scheme is simple and thus requires minimum additional chip area. A detailed description of linear string decoder is presented in the second part of this chapter.

3.1. MONOTONIC DECODER DESIGN

In typical binary N bit decoding, a single output is selected from among $2^N - 1$ possible outputs. Change in code results only in another selection while the selected quantity remains equal to one. A transfer function for a binary 3 bit decoder shown in Figure 3.1 is discontinuous and contains discrete points. In binary N bit monotonic decoding, k items for $0 \leq k \leq 2^N - 1$ are selected simultaneously. Thus, a change in input code corresponds to change in the number of selected items. The incremental growth in group size is achieved sequentially or monotonically by adding the next unit element. A transfer function for a monotonic 3 bit decoder is shown in Figure 3.2.

A bipolar circuit which yields such a transfer curve has been developed by Schoeff [9] and depicted in Figure 3.3. All current sources in the bottom array are identical. An input code of 000 to terminals labelled B1 B2 B3 is designed to

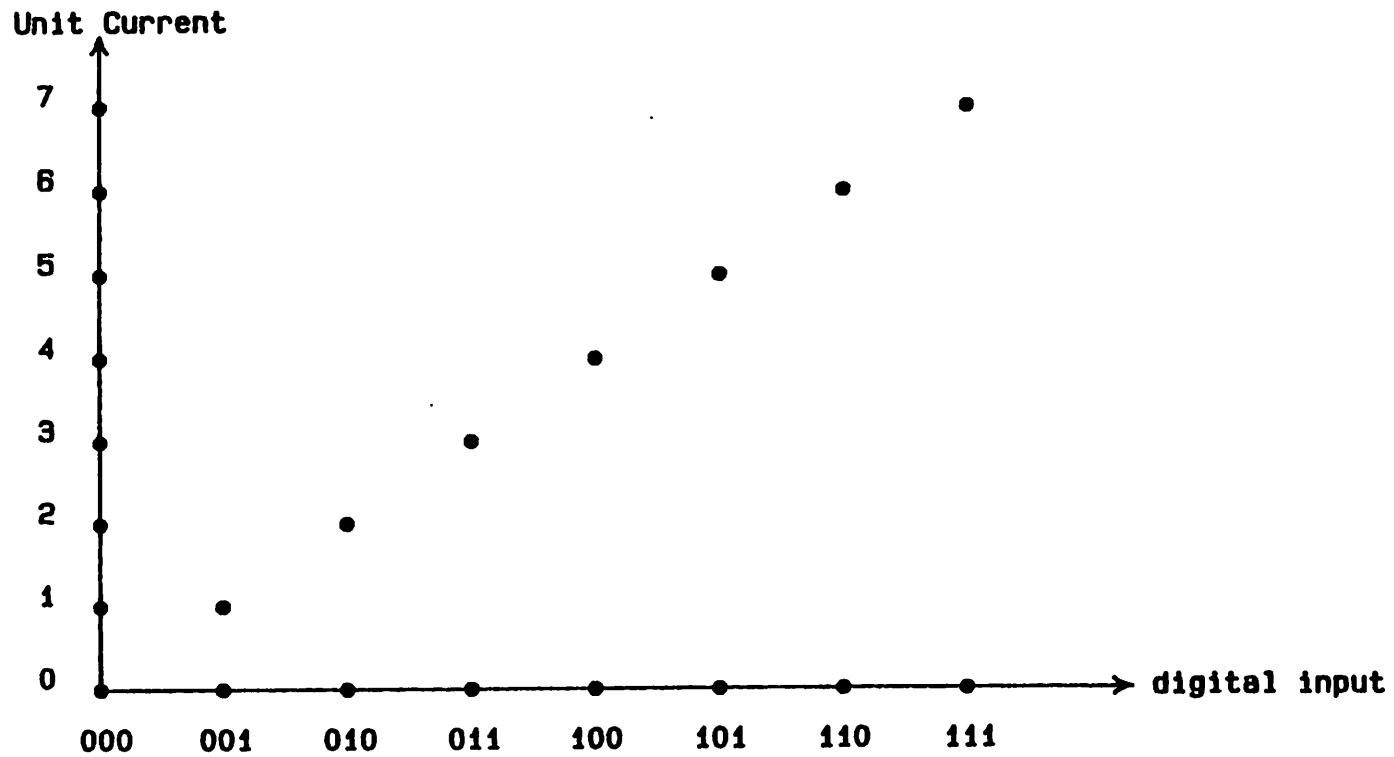


Fig.3.1 3 Bit Binary Decoder Transfer Curve

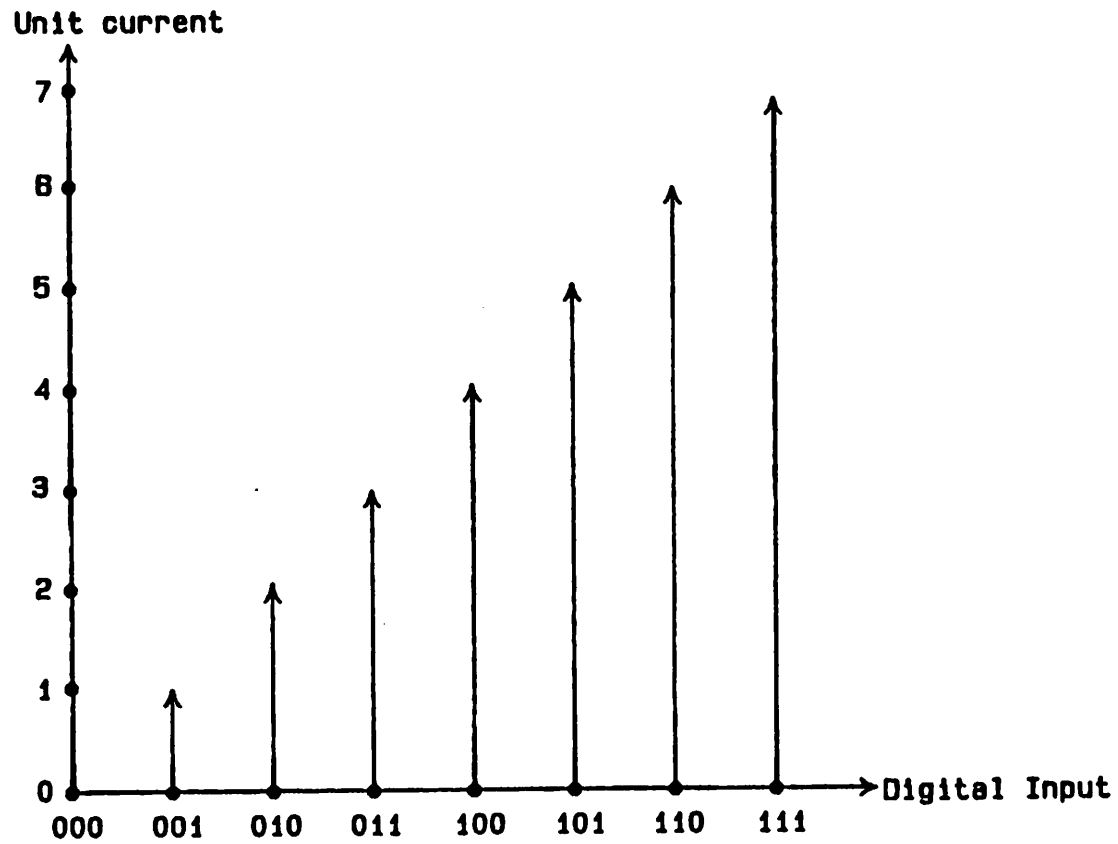


Figure 3.2 3 bit Monotonic Decoder Transfer Curve

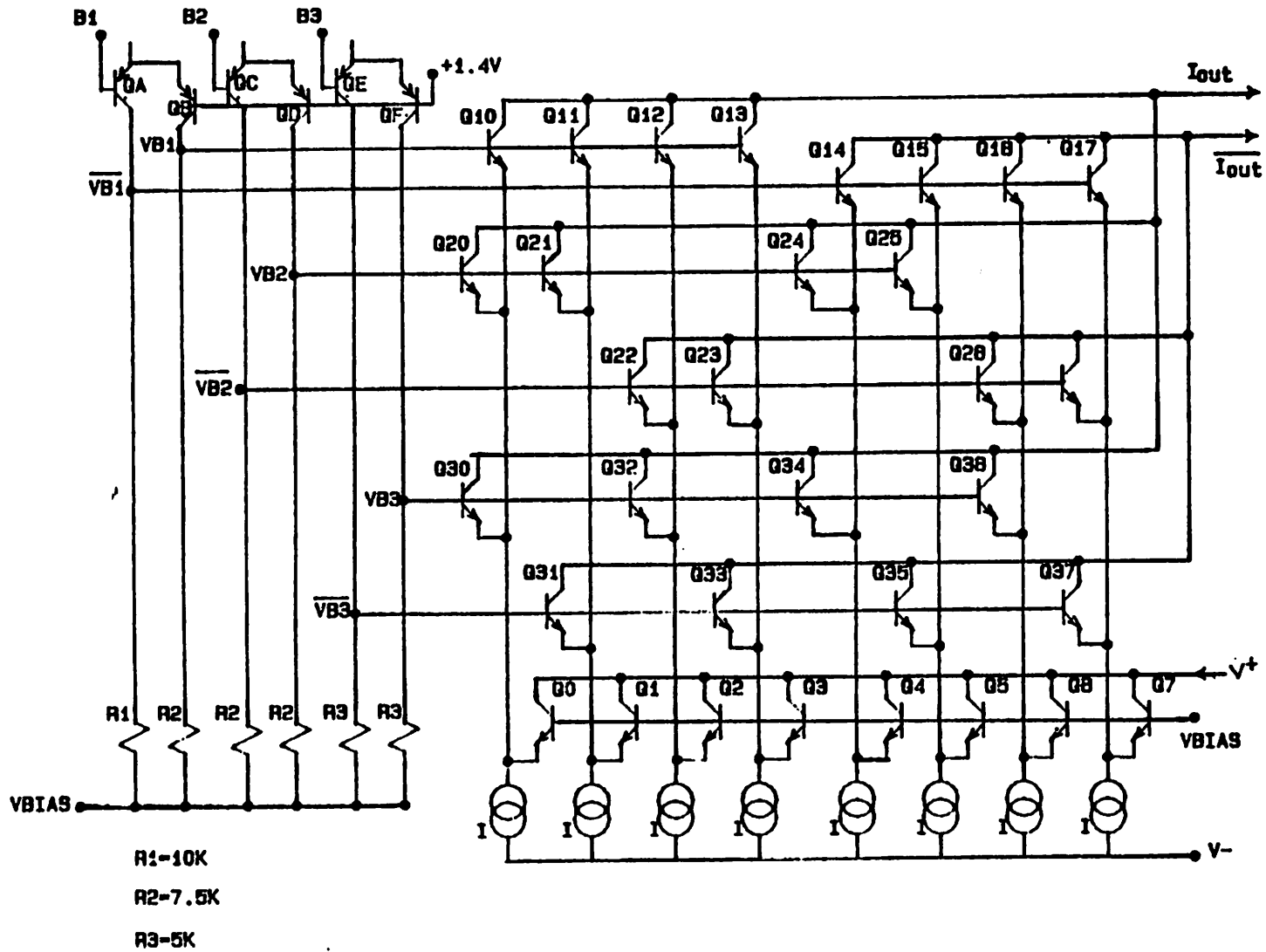


Figure 3.3 Bipolar Monotonic Decoder

produce current I to the output. The series of operations achieving this is as follows: Q_A , Q_C , and Q_E are turned off as result of the input bits status. The node voltages designated as V_{B1} , V_{B2} , V_{B3} fall to .5 V below the bases of Q_0 to Q_7 . Transistors Q_{10} , Q_{20} , and Q_{30} are subsequently turned off. The leftmost unit current is then passed to the output through Q_0 .

The basic limitation in this decoder is the number of voltage steps of size V_{BE} than can be produced with a fixed power supply. This number decreases in a MOS implementation of this decoder configuration because of the body bias effect and the larger value of MOSFETs' nominal V_T as compared to bipolar devices' V_{BE} . Furthermore, the decoding circuits definitely outweigh core converter circuitries. In this 3 bit example, the number of decoding devices is about 3 times that of current sources devices. Therefore, this multilevel switching network is not feasible for producing $2^N - 1$ control signals for large N .

In the proposed 8 bit sequential current selection D/A converter, the required decoding is achieved through binary decoding and partitioning operations. The binary decoding phase identifies the last unit current to be selected. The remaining partitioning mechanism of dividing into current sources selected and unselected groups is performed through the proposed linear string circuits as discussed in the next section.

3.2. LINEAR STRING MONOTONIC DECODER

A row of linear string decoder which consists of series transmission gates is shown in Figure 3.4a. The switches are driven by the decoded output of the input bits. The selected output are held low while all remaining unselected outputs are held high. During each conversion cycle, only one switch is selected low and held open while the remaining switches are closed. For different endpoint voltages, a left segment with value V_{off} and a right segment of value V_{on} , are

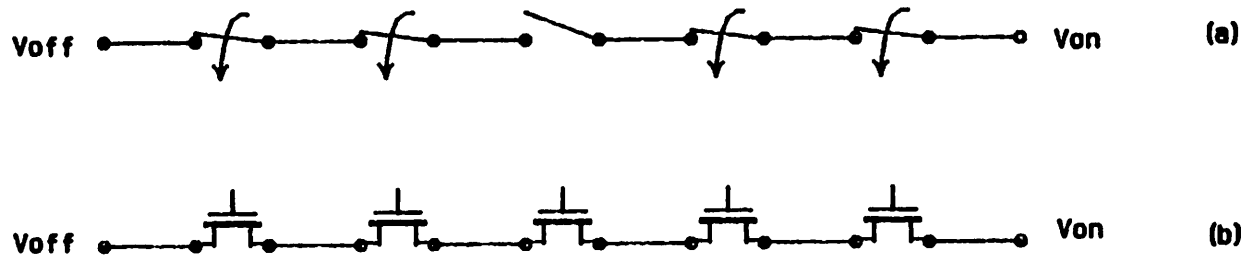


Fig.3.4 Proposed Linear String Decoding Technique

created. Current sources connected alternatively between switches to the left of the breakpoint are selected by the V_{on} signal while those to the right of the breakpoint are deactivated by the V_{off} signal. As the breakpoint shifts rightward corresponding to an increasing input code, additional unit currents are addressed sequentially. Likewise, moving the breakpoint leftward as a result of reducing the input code deselects current sources. To minimize decoding delay and input skew, it is crucial that input code be decoded in the preceding clock phase. The predecoded signals are dynamically stored and strobed in to all current sources. Dynamic storage is most suitable for the high speed operation. It consumes no additional power dissipation nor area. Using the gate capacitance of the current source as storage node, .01 pF of storage capacitance is achievable. In implementation as shown in Figure 3.4b, the switches are realized each by a MOS device, the simplest possible type of circuit configuration. Thus linear string decoding technique achieves monotonic decoding with the minimum amount of additional chip area to the core converter. In steady state, or standby mode, the power dissipation is virtually zero since no current flows in either the left or right segments.

A one dimensional 8 bit linear string decoder requires 256 eight-input NOR gates. The inverted outputs drive a string of 256 switches in series connection. Although this circuit complexity is feasible with very large scale integration in NMOS polysilicon gate technology, the delay through the linear string decoder and the extra output loading would be too large for very high speed operation. An alternative approach developed to minimize both circuit complexity and delay is the two dimensional linear string structure shown in Figure 3.5. A 4 bit D/A converter with partial decoding example is used to illustrate the basic operation of two dimensional linear string decoding. Sixteen current sources are arranged in a 4 X 4 matrix. The sixteenth current unit is always disabled

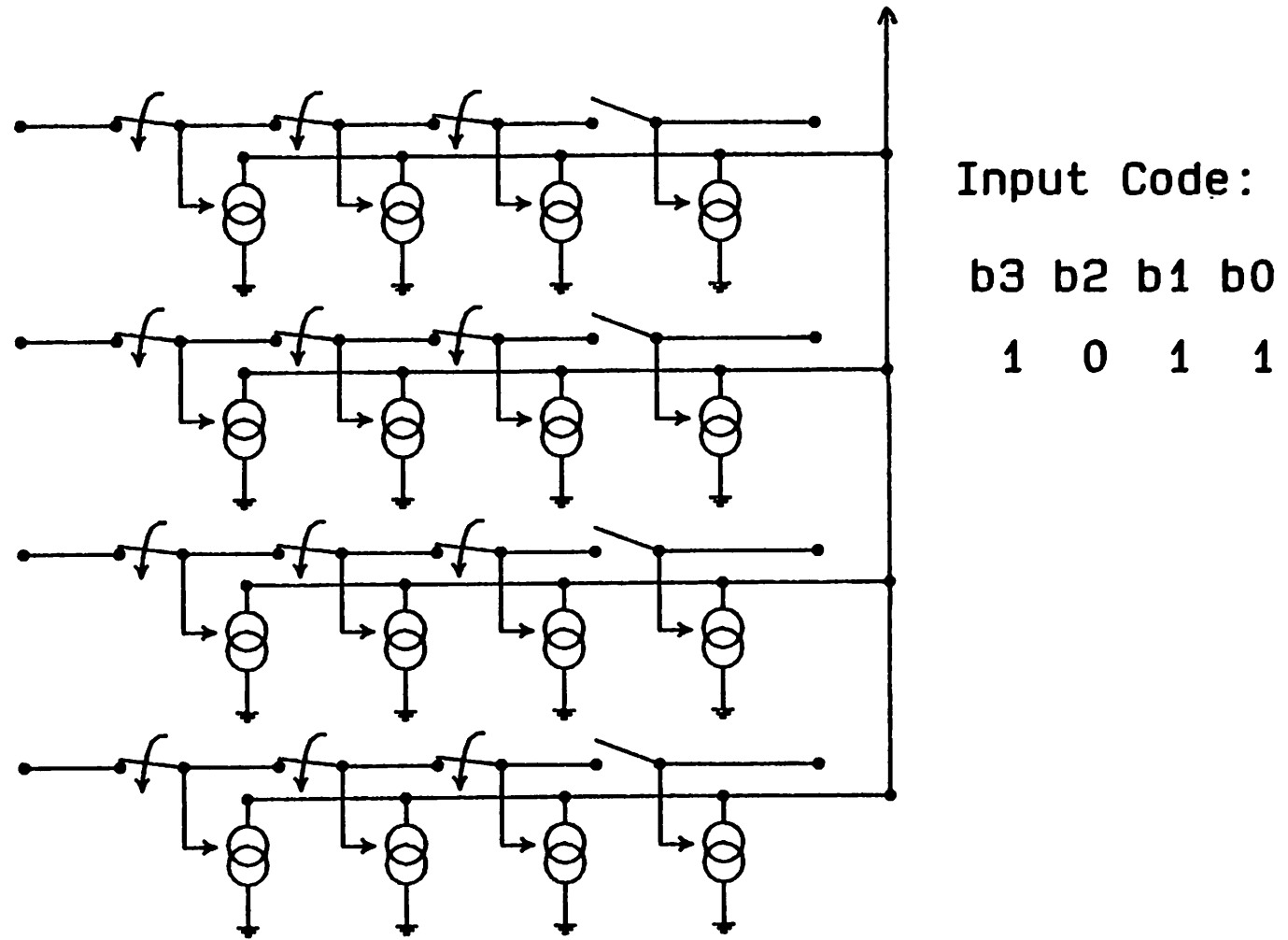


Fig.3.5 4-Bit D/A Converter Partial Configuration

since analog zero typically consumes one state. There are four column control lines driven by the inversion of the decoded output of the lower bit pair. Thus, one column select lines will always be low and the respective switches in this column will be unselected. For the particular input code of 1011 (MSB..LSB), the lower bit pair input (11) deselects the fourth column control line. Therefore, all fourth column switches are left open. To select the first 11 units of current, endpoint voltages for each of the four rows must be as follows: V_{on} applied to all end nodes in the first and second rows activates the first eight unit currents. Different voltages V_{on} and V_{off} applied to the third row activate only the first three unit current and disables the last one. V_{off} applied to both end nodes in the last row deactivates all current sources. Thus a total of 11 unit currents are summed at the output as required. Notice that the side voltage patterns are offset from one side to another. In addition, each pattern contains a breakpoint which separates a series of V_{on} and V_{off} . Linear string decoders are again used to generate the breakpoint effects in the terminal voltage patterns. The breakpoint in each side linear string decoder is produced by decoding the upper bit pair 10. In Figure 3.6, a complete block diagram for the 4 bit D/A converter is drawn.

In general, a N bit digital input can be divided into two arbitrary groups of M bits and $N-M$ bits. 2^M M inputs NOR gates and $2^{(N-M)}$ $N-M$ inputs NOR gates are utilized to produce the control signals for the switches. In Figure 3.7, the transfer curve is given for the total number of devices needed versus variable M for specific case of $N=4$. The optimum case for hardware minimization is to choose $M = \frac{1}{2}N$. The worst cases $M=0$ and $M=N$ correspond to the one dimensional decoding scheme.

To estimate the propagation delay of a linear string decoder of length N , a normalized RC ladder model as shown in Figure 3.8 is used. The specific case of

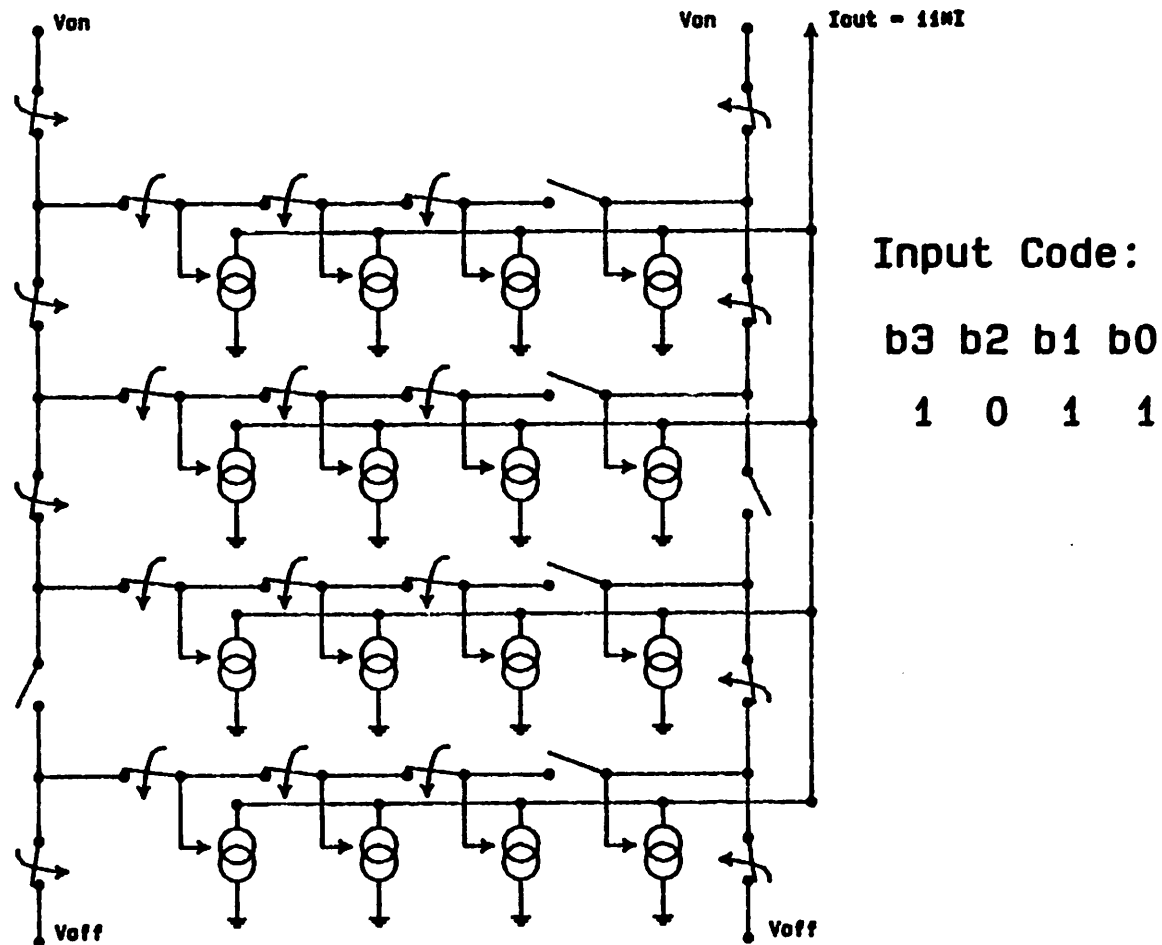


Fig.3.6 Complete 4-Bit D/A Converter

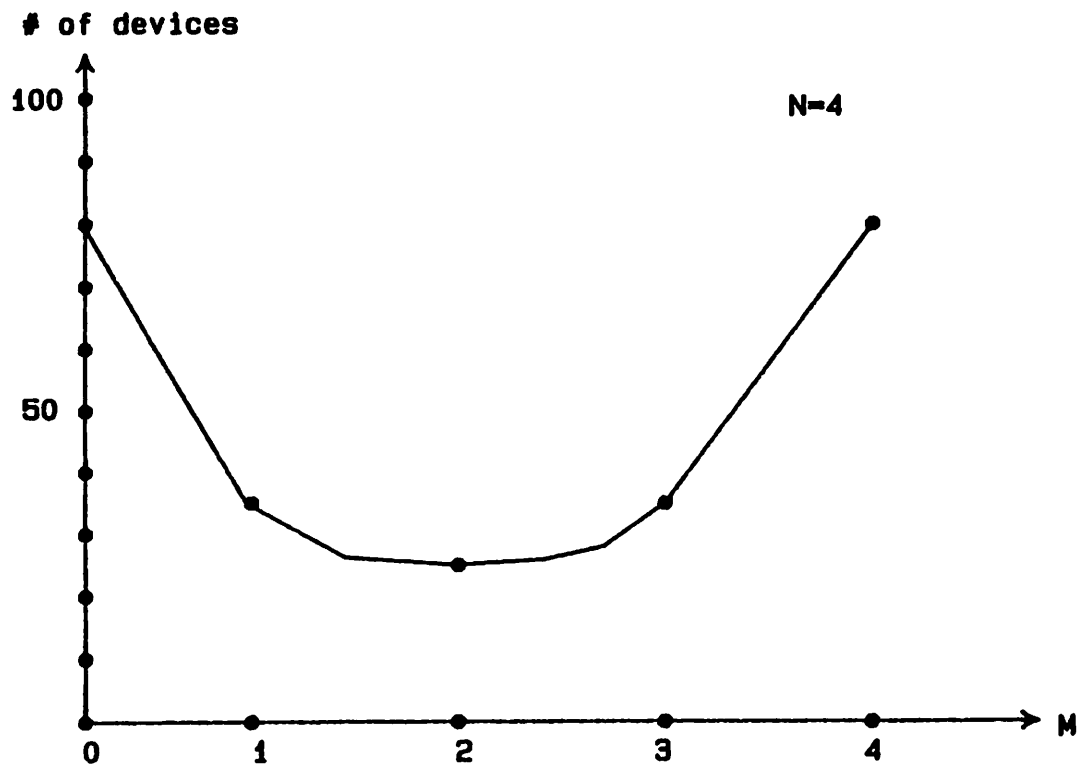


Fig.3.7 Number of Peripheral Devices vs M

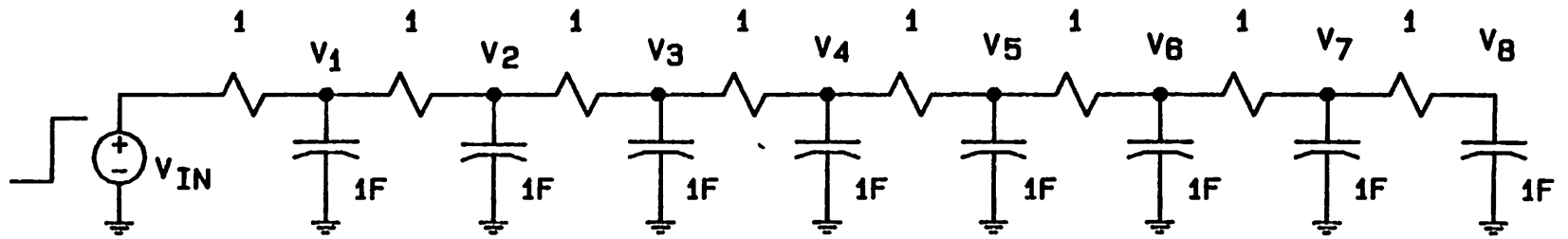


Fig.3.8 Normalized R-C Ladder Network

$N=8$ is considered. Resistive element R represents switch on-resistance. Capacitor C accounts for parasitic line and the current cell gate capacitances. A computer simulation of such configuration yields the 0-90% response time at each nodes for an applied step input is listed in Table 1.

TABLE I
NORMALIZED RC LADDER TRANSIENT RESPONSE

NODE	0 to 90% rise time (seconds)
V1	30
V2	60
V3	78
V4	90
V5	98
V6	103
V7	108
V8	112

The largest delay observed occurs at node V2 where loading is heaviest. Based on process parameters and layout, an estimated delay of 9 ns is introduced by a

linear string decoder of length 8. In a two dimensional decoder structure, a maximum string length is generated when the input code are either all zero or one. For all zero digital input, the longest string is a cascade of:

$$(\text{switches in the top row}-1) + (\text{switches in the side decoder}-1)$$

By symmetry, the string length for all ones digital input is equal to

$$(\text{switches in the last row} - 1) + (\text{switches in the side decoder} - 1)$$

As a means of reducing propagation delay through a long linear string, repeaters can be added along the linear string path to limit loading.

Several variations on the linear string decoding structure are possible. Nesting and multi-dimensional arrangements of linear string decoder are ways that realize further reduction in the amount of logical hardware. An example of two-level nesting for 4 bit decoding is illustrated in Figure 3.9. This scheme eliminates approximately 84 devices. One main disadvantage of the nesting technique is the requirement of higher power supply voltage levels. For MOS technology, this method becomes impractical when stacking exceeds four layers. An alternative approach to achieve identical objective of hardware minimization but maintain low power supply is a multi-dimensional structure. Figure 3.10 depicts the framework of a three dimensional decoding system. New dimensions are added by attaching another linear string decoder to the open terminals labelled V_{on} and V_{off} . A comparison in device count required for a $2 \times 2 \times 2$ versus a 3×3 decoding configuration yields an estimated 25% reduction. As both N and dimensions are increased, greater benefit are realized. In a multi-dimensional array, the length of each string is shortened. However, the delay through the matrix might not decrease proportionally since the compact nature of the matrix is lost when it is decomposed for integration.

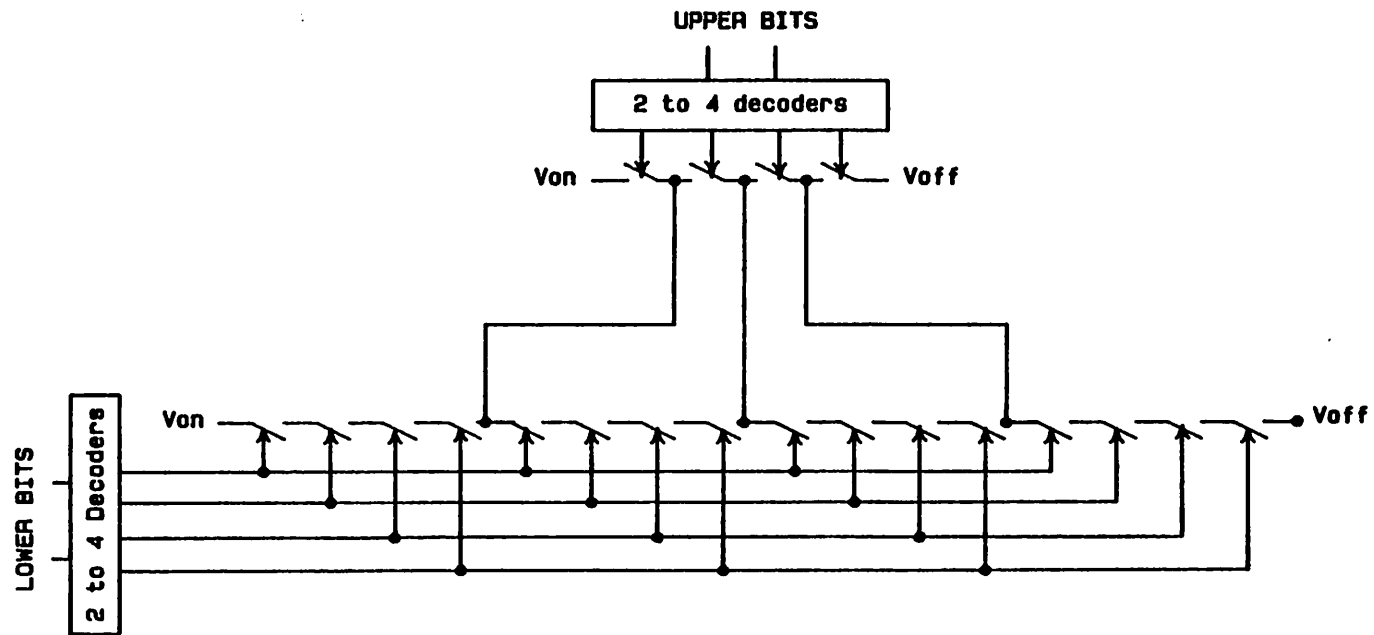
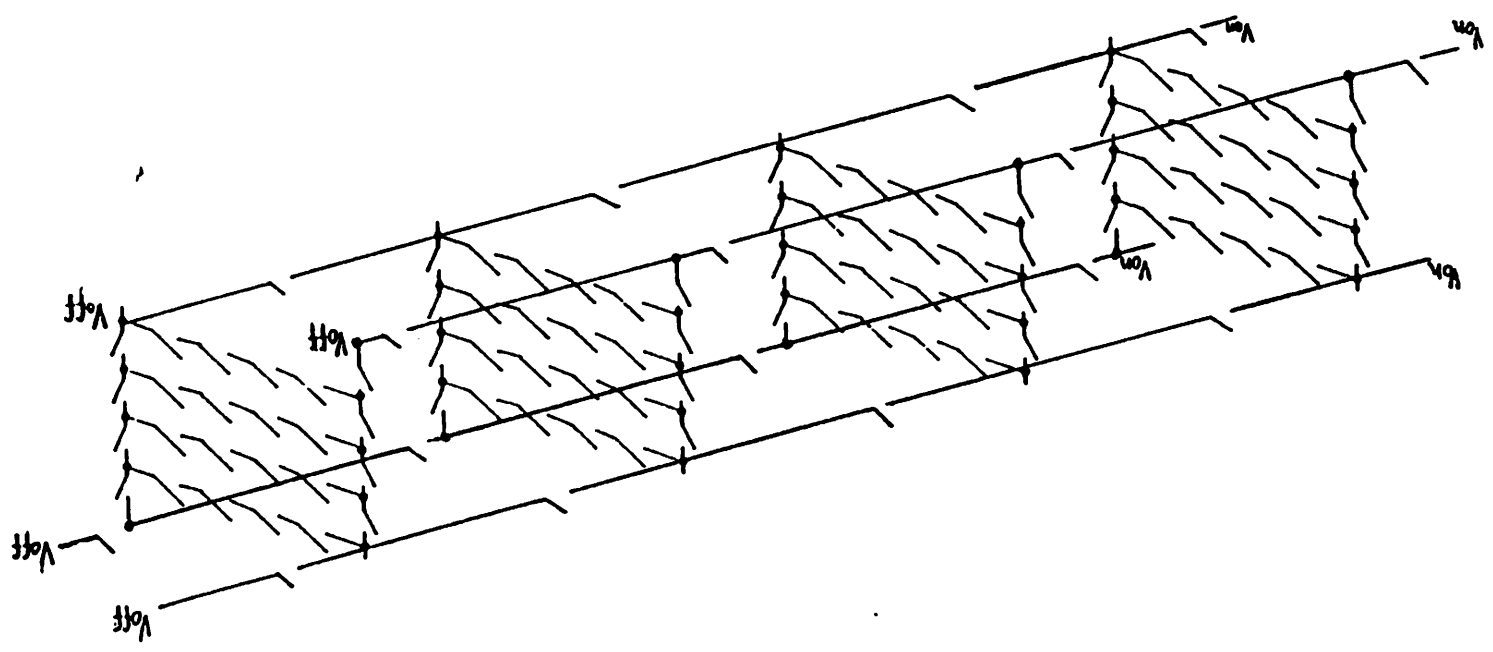


Fig.3.9 4-Bit Stacked Linear String Decoder

Figure 3.10 3 Dimensional Linear String Decoding Structure



CHAPTER 4

CURRENT SOURCE DESIGN

In the sequential current selection D/A converter, the unit current source design determines not only resolution and linearity as in past current steering D/A converter, but also glitch performance. A simple current source design which optimizes these parameters is presented in the first Section. In subsequent sections, theoretical limitations on the proposed converter performance are discussed.

4.1. CURRENT CELL CONFIGURATION

The proposed current source configuration is shown in Figure 4.1. A stable reference voltage applied to the gate of transistor M_I activates the current cell to be turned on into the saturation region. Transistor M_I sets the 1 LSB current level which is $10 \mu\text{A}$ for our case. Transistor M_B is also biased in the saturation mode. When M_B begins to turn on, channel charges are supplied from the source electrode. Electrons are prevented to backflow from the drain electrode by the depletion region at the drain. This eliminates a source of glitch. M_B buffers the output node from input pulses and increases current cell output impedance. Because M_B is source controlled rather than gate controlled, its turn-on process is more gradual and self-synchronized. Therefore, the turn-on transient of M_B is glitch-free. The combination of these two devices forms a cascoded inverter. The discharge operation of this configuration is very slow. This is because when the current cell is deselected the charge stored at the drain node of M_I can only discharge through the ever rising effective impedance, $\frac{1}{gm}$, of M_B . In the limit of $\frac{1}{gm}$ approaching infinity, the output requires

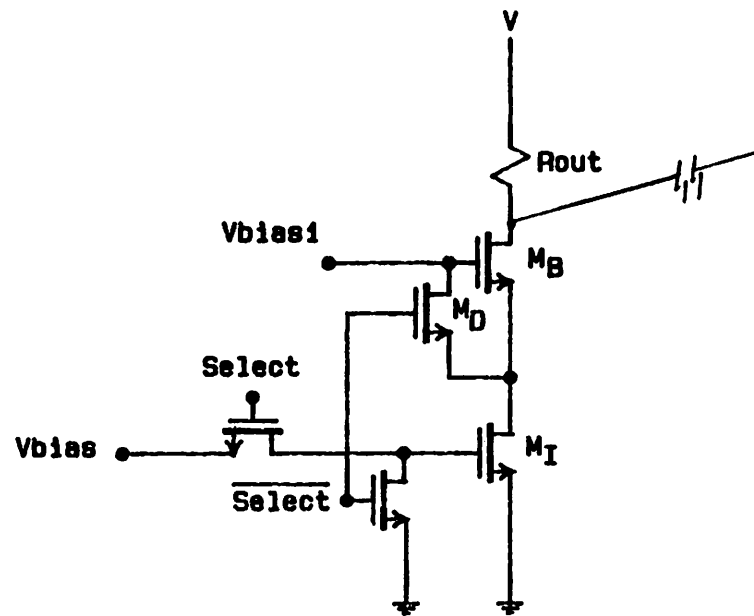


Fig.4.1 Unit Current Cell Circuit Configuration

infinite amount of time to decay to zero. The settling time for 8 bit resolution is several microseconds. With the addition of a switch, M_D , a low impedance discharge path is established. Figure 4.2 simulates output rise and fall times of 1023 unit currents of $10 \mu\text{A}$ each, with an output load of 50Ω , and without M_D . The 0 to 90% fall time requires only 7 ns. However, the remaining settling time to 10 bit accuracy requires over 100 ns. Figure 4.3 illustrates the case of single current source settling time with M_D . The 0 to 100% fall time is only 15 ns. The simulated rise time is approximately 15 ns. In general, with each current cell behaving independently, and for constant RC loading, the settling time is unchanged by the amount of current cells selected.

4.2. RESOLUTION LIMITATION OF SCS D/A CONVERTER

The resolution of sequential current selection D/A converter is constrained by the ratio of load resistance to output impedance of the current sources. An expression for this constraint is:

$$\frac{R_{load}}{R_{out}} < \frac{1}{2^{(N+1)}} \quad (4.1)$$

For $R_{load} = 50 \Omega$, the calculated maximum N can be obtained by estimating the R_{out} of the current cell. An equivalent circuit model shown in Figure 4.4 is used. Writing KCL at node x gives:

$$i_x = -g_{m2}v_i - g_{m27}v_i + i_{r_{ds1}} \quad (4.2)$$

$$v_i = i_x r_{ds1} \quad (4.3)$$

Substituting (4.3) into (4.2) and solve for $i_{r_{ds1}}$

$$i_{r_{ds1}} = i_x r_{ds1} (1 + g_{m2} + g_{m27}) \quad (4.4)$$

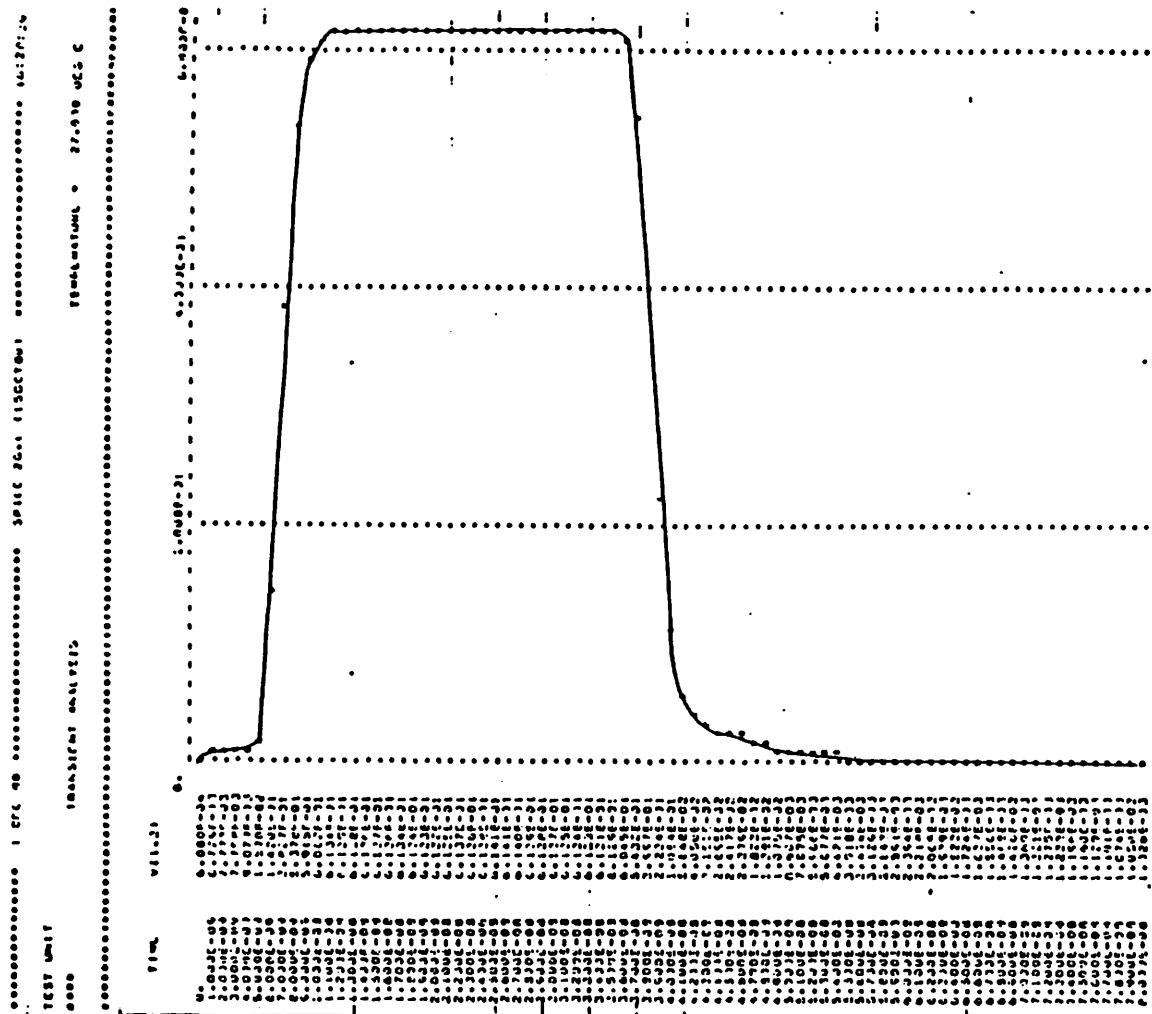


Figure 4.2 Output Waveform of 1023 Current Sources Turning ON/OFF Without M_D , $R_{out}=50$

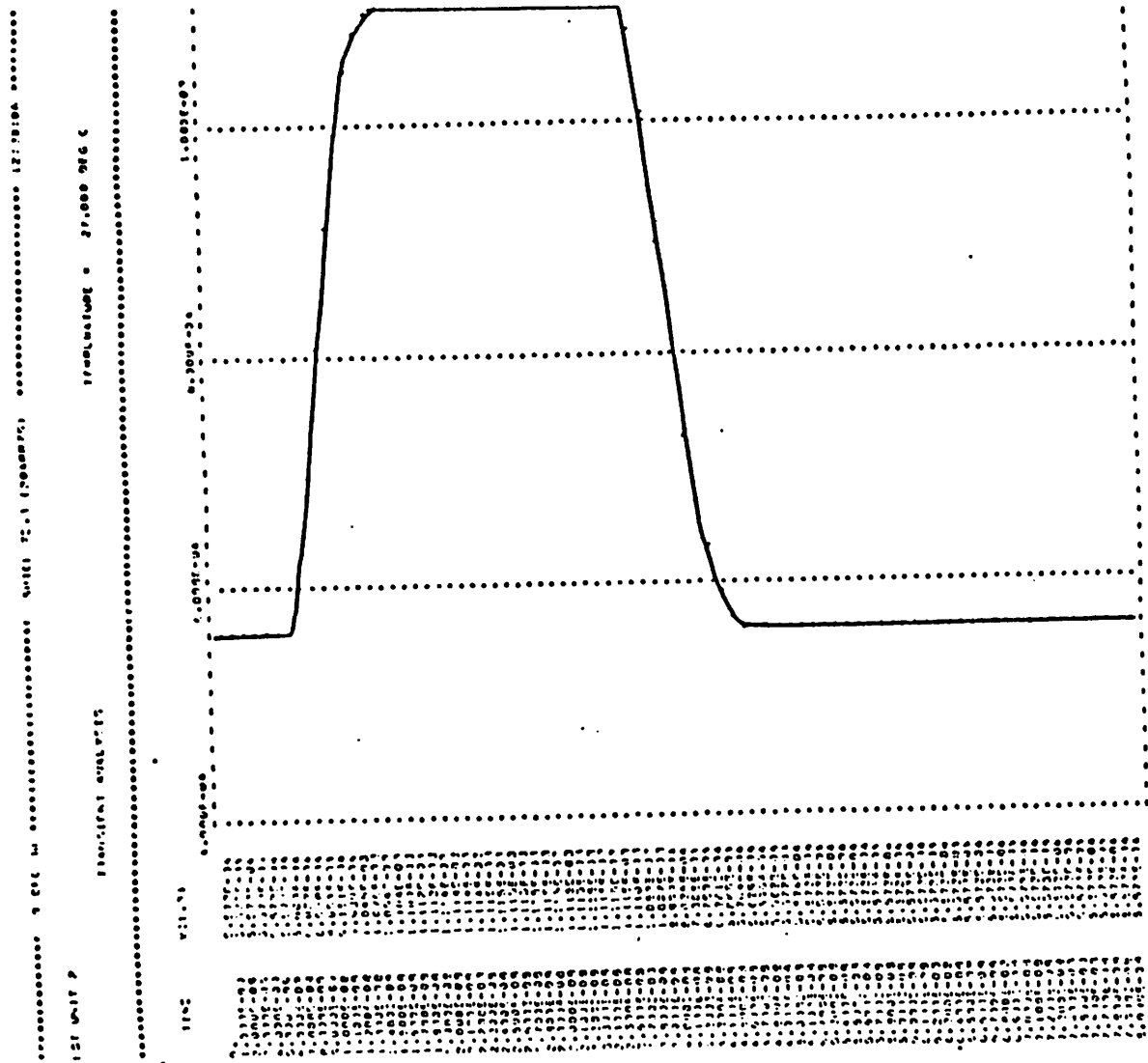


Figure 4.3 Single Current Source Turning ON/OFF
With M_D , $R_{out}=50$

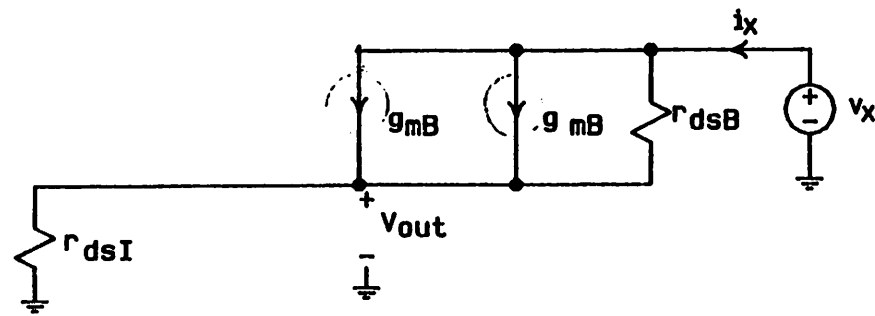


Fig.4.4 Small Signal Circuit of Current Cell

Write KVL for output loop gives:

$$v_s = v_{r_{ds1}} + v_{r_{ds2}} \quad (4.5)$$

Substituting (4.3) and (4.4) into (4.5) results in the following:

$$v_s = i_s r_{ds1} \left(1 + g_{m2} r_{ds2} + g_{m2\gamma} r_{ds2} + \frac{r_{ds2}}{r_{ds1}} \right) \quad (4.6)$$

Thus,

$$R_{out} = v_s / i_s = r_{ds1} \left(1 + g_{m2} r_{ds2} + g_{m2\gamma} r_{ds2} + \frac{r_{ds2}}{r_{ds1}} \right) \quad (4.7)$$

For $\frac{1}{r_{ds1}} \ll g_{m2}, g_{m2\gamma}$

$$R_{out} = r_{ds1} (1 + g_{m2} r_{ds2} + g_{m2\gamma} r_{ds2}) \quad (4.8)$$

For the designed values as follows:

$$I_D = 10 \mu\text{A}$$

$$L_{MI} = 14 \mu$$

$$\lambda_{MI} = .01$$

$$L_{MB} = 10 \mu$$

$$\lambda_{MB} = .03$$

$$V_{BS} = .3\text{v}$$

$$\gamma = .2$$

The calculated $R_{out} = 730\text{M}\Omega$. Thus $N_{max} = 11$.

Chip area consumed by interconnection and peripheral circuits can be reduced significantly with VLSI processing technology. However, a major area constraint is the size of a unit current. Current source transistors must be designed to have long channel length to achieve high output impedance. Thus

the cell size remains relatively fixed. This limits the number of current sources to be realized within a die and thus limits the converter resolution.

4.3. POSSIBLE ERROR TYPES IN SCS D/A CONVERTER

Offset error in the actual transfer curve is defined as the amount of uniform shift including analog zero point from the ideal transfer curve. In sequential current selection D/A converter, output current offset error is due to the 2^N-1 M_D drain leakage currents. This is on the order of picoampere is thus negligible when compares to $\frac{1}{2}$ LSB of current.

Gain error occurs when there is a slope change in the actual transfer function. In SCS D/A converter, there is no current gain error since new output is achieved through either a subtraction or an addition operation.

Differential linearity error is the deviation of any analog step or quantum from its ideal value. Deviation in step magnitude is due primarily to geometrical and electrical parameters mismatch among the nominally identical components. For MOS current steering D/A converter the ratio accurate elements are MOS devices. Suppose I_0 is the fabricated unit current value. Then, an adjacent nominally matched current source has output distribution $N(I_0, \sigma)$. $N(I_0, \sigma)$ is the normal probability density function with expected value I_0 and standard deviation σ . Any deviation from the expected value is considered an error. For SCS converter, each analog step corresponds to turning on the next identical current unit. Thus, the differential linearity error function is $N(I_0, \sigma)$ for all N within resolution bound. This is a major improvement in differential nonlinearity over current steering D/A converter.

The matching requirement of current steering D/A converter is between groups of devices rather than pairs of devices. The larger step size errors occur at transition into 2^{th} step for $1 \leq i \leq N-1$. Using central limit theorem [12],

the error for each possible i has the following general distribution:

$$N(2iI_0, \sqrt{2i} \sigma) \quad 1 \leq i \leq N-1 \quad (4.9)$$

As i increases, the spread of the error function widens. The tendency to deviate from the expected values increases. If the actual output falls below the expected value I_0 , the converter's transfer curve becomes nonmonotonic. This situation never happens with SCS converter. At worst, the next selected unit current fails completely and a step would be missed in the output.

Integral linearity error is the maximum deviation between zero and full scale of the actual transfer curve from the ideal curve. Since both current steering D/A converter and SCS D/A converter both utilize 2^N-1 identical unit currents, integral nonlinearity would be the same in both designs. However, sequential current selection D/A converter may have a smoother transfer curve than that of past current steering D/A converter.

4.4. OUTPUT NOISE OF SCS D/A CONVERTER

The noise model for the current cell is shown in Figure 4.5. The resistance of decoding switches and the lumped input capacitance C of transistor M_1 form an equivalent input noise voltage for each unit current I_0 expressed as follows [13]:

$$v_n^2 = \frac{kT}{C}$$

k is Boltzman's constant. T is temperature in degrees Kelvin. The noise of transistors M_1 and M_2 each has the following two dominant component

$$i_n^2 = 4kT \frac{2}{3} g_m f + IK \frac{f}{C_{gs} L^2 f^2}$$

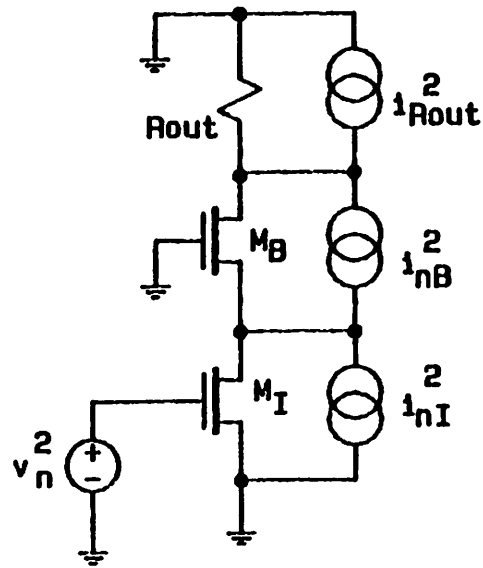


Fig.4.5 Current Source Noise Model

K contains factors such as charge q , surface state density N_{SS} , and mobility μ . a is a curve fitting constant. The first term represents thermal noise of channel resistance when the device operates in the saturation mode. The second factor is flicker noise induced by surface states trapping and releasing conduction carriers. The total output noise current of the D/A converter is given as follows:

$$i_{out}^2 = i_{Rout}^2 + (2^N - 1)(gm_f^2 v_n^2 + i_{nB}^2 + i_{nI}^2) \quad (4.12)$$

CHAPTER 5

PERFORMANCE EVALUATION AND CONCLUSION

In this chapter, the results of performance evaluation of an experimental sequential current selection D/A converter are presented. Due to the limited die size, and the relatively large amount of interconnection per current cell, only 84 current units and linear string decoding circuits are accommodated on chip. Test patterns for process characterization and functionality checks are placed on separate die within the same wafer. Suggestions for improved reliability and performance for future implementation are included.

5.1. PERFORMANCE EVALUATION

An experimental 8 bit sequential current selection D/A converter has been fabricated in single polysilicon NMOS technology. Photographs of the main converter die and separate test pattern die are shown in Figures 5.1 and 5.2 respectively. To achieve functional high density chip with this newly developed process, very conservative layout rules were adopted. Minimum related feature spacing were 7μ . Within the core converter section, minimum channel length is 5μ . In the peripheral decoding circuits, the minimum channel length is 4μ . The resulted 8 bit die size is 2.5 mm x 3 mm.

Although the first run did not yield perfect chips, adequate data were obtained from the partially functional die to verify the proposed circuit ideas. Shown in Figure 5.3 is a converter transfer curve. The output resistor used is 10 K Ω . The defect is related to the missing contact during metal mask generation. Consequently, the last row of current cells cannot be selected which results in the cyclical missing steps on the transfer function. To improve yield, future

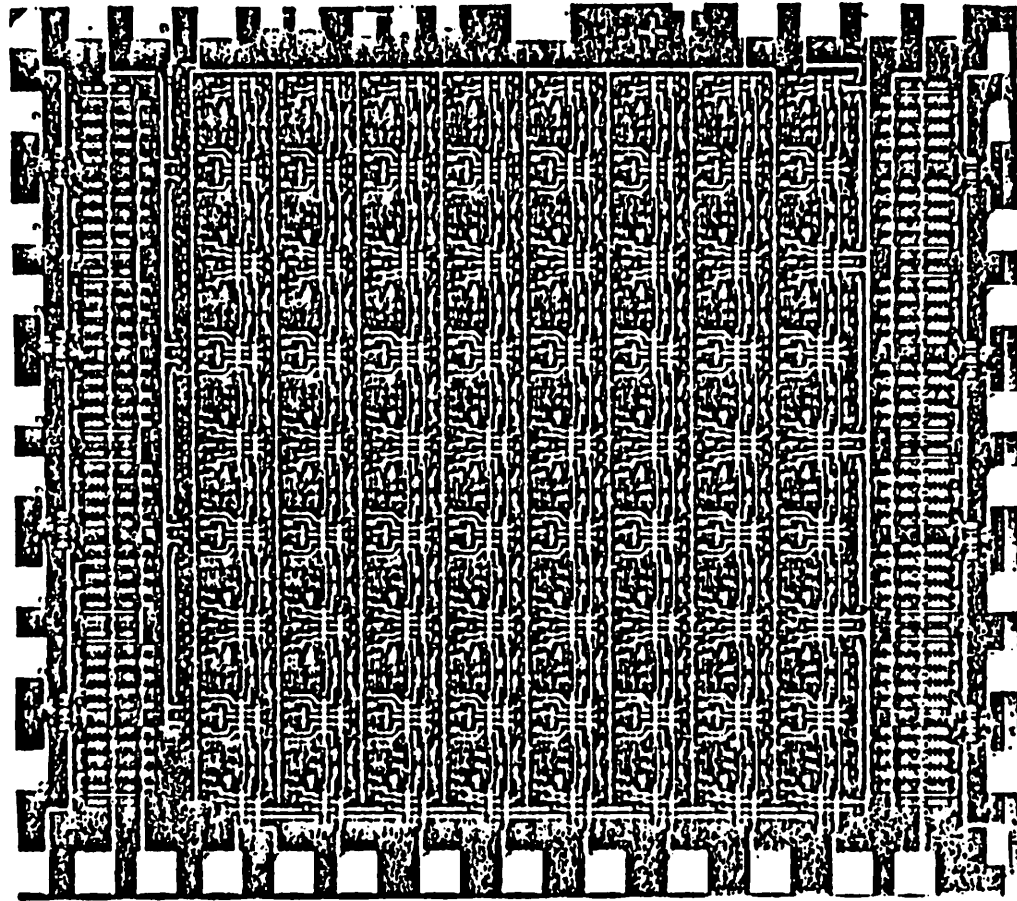


Figure 5.1 Sequential Current Selection DAC Die Photo

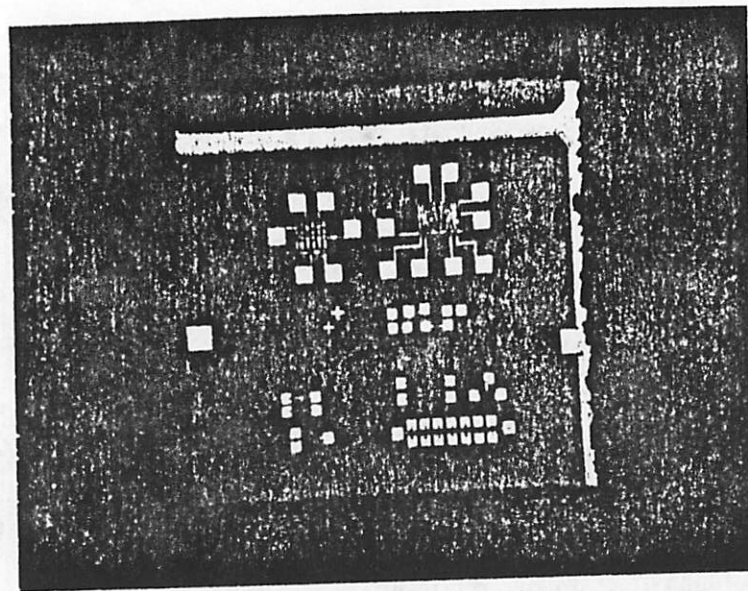
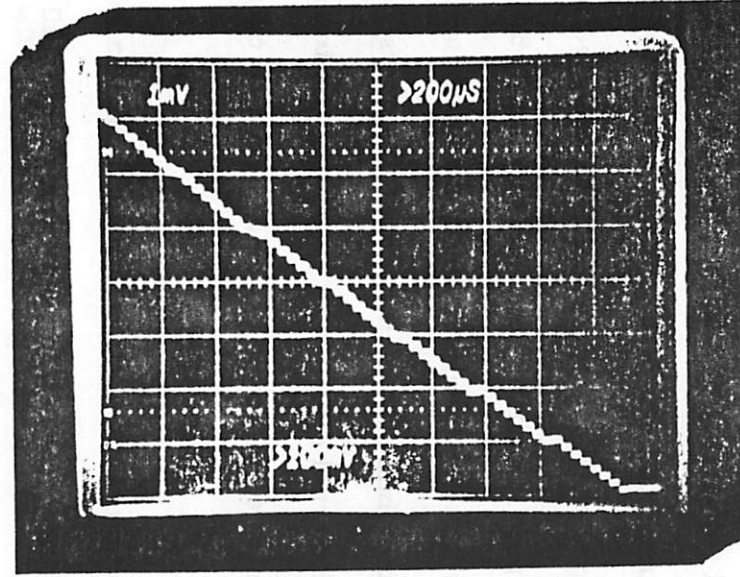


Figure 5.2 Die Photo of Test Circuits

Analog Output Voltage



Binary Input Code

Fig.5.3 DAC Output Transfer Function with $R_{out} = 10K \text{ Ohm}$

design may consider on-chip redundancy. Spare current cells, in single, row, or column formats could be electrically programmed during wafer probe to replace bad units. A less expensive alternative is on-chip digital correction which may increase conversion time.

Transient characteristics of the experimental converter are characterized with an output impedance of 160Ω . The estimated internal and external capacitive loading during measurement is approximately 50 pF. The major transition of 011111 to 100000 is observed repeatedly of different degrees of timing skew in input switching signals. In Figures 5.4a and 5.4b, the top traces are the output waveforms while the lower waveforms are the switching input pulses. These figures indicate that the output remains glitchless for input bit switching mismatch less than 20 ns. For the observed settling time of under 60 ns, this translates to a 33% skew tolerance margin which adequately covers skew due to inherent nonsynchronization. External data skews exceeding the tolerance window generally are reducible and the converter is not designed to correct these errors.

The matching uniformity among typical current cells is illustrated in Figure 5.5. The current units generating these seven steps span across 90 mils. The majority of current cells are observed to match better than 2%. Integral linearity is measured to be 3%.

5.2. CONCLUSION AND FUTURE DESIGN CONSIDERATION

To demonstrate the potential of NMOS technology in certain high performance analog VLSI circuits, a new sequential current selection D/A conversion algorithm has been proposed. The feasibility of the design is realized with the development of linear string monotonic selection technique which consumes minimal power and chip area. The experimental NMOS polysilicon gate 6 bit D/A

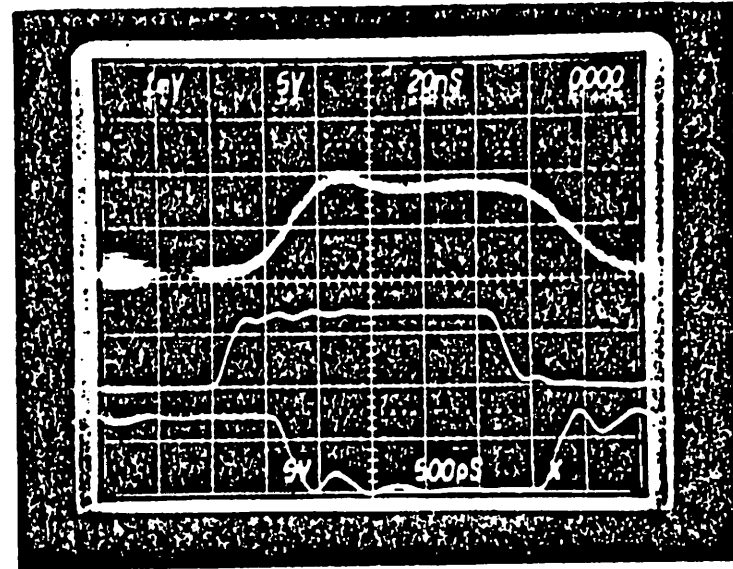
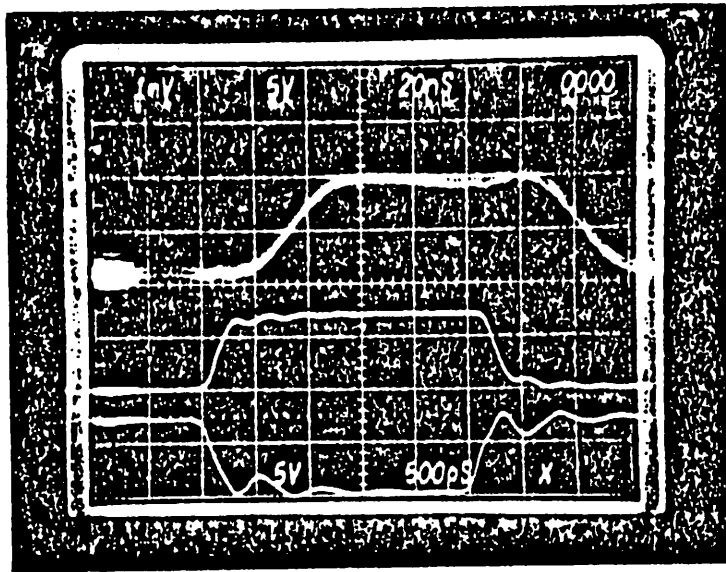


Figure 5.4 Half Scale Transition With Input Skew

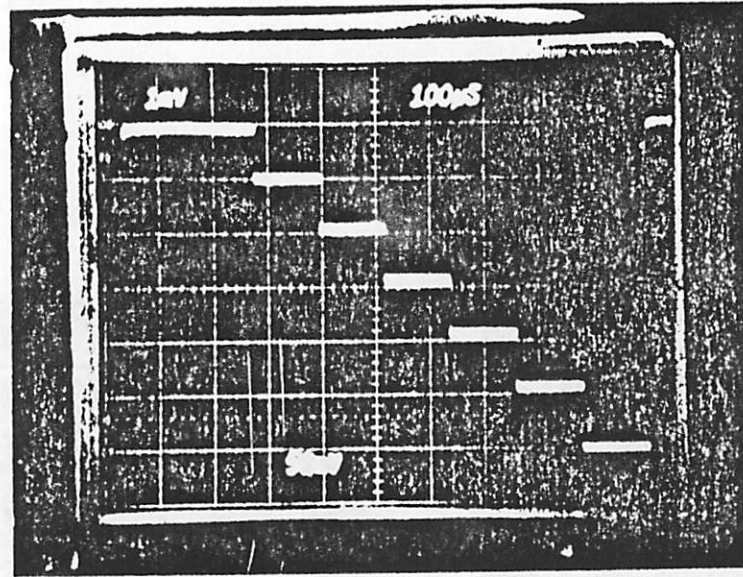


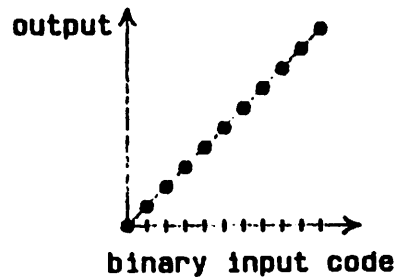
Fig.5.5 A Row of Current Sources

converter exhibits low glitch, monotonic, and fast performance. The die active area is 5mm^2 .

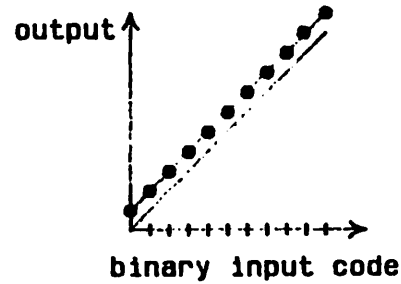
Using 3μ VLSI technology, 10 bit resolution should easily be achievable with die size of 25mm^2 . Both CMOS and NMOS technologies are suitable for implementing the converter. With CMOS technology, the core current source array remains entirely N-channel because the P channel device offers no advantage. In the peripheral digital section, complementary devices can save power. This converter configuration is not quite suitable for bipolar technology because of the lack of good, simple bipolar voltage switch for implementing linear string decoder.

Appendix I Error Types of D/A Converter

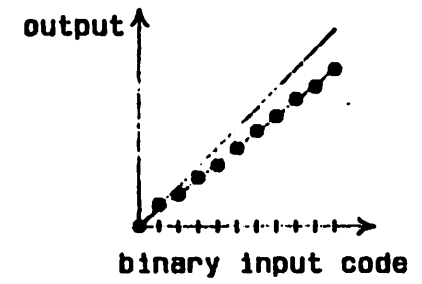
IDEAL CASE



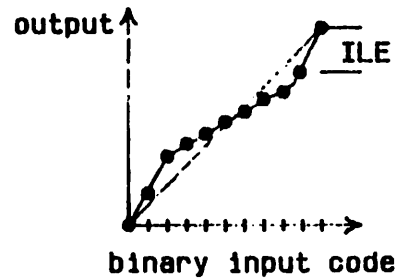
OFFSET ERROR



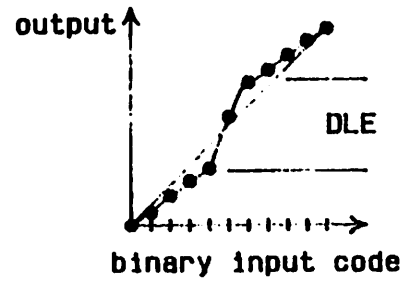
GAIN ERROR



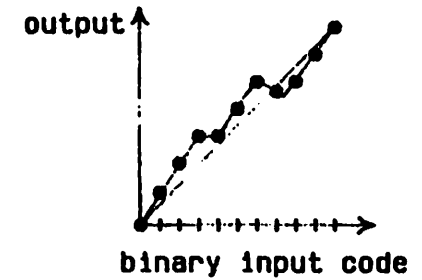
INTEGRAL LINEARITY ERROR



DIFFERENTIAL LINEARITY ERROR



NON-MONOTONICITY ERROR



APPENDIX II

LOCOS POLYSILICON GATE NMOS IC PROCESS

The process developed by Yen [14] is as follows:

1. STARTING MATERIAL

boron doped p-type wafer

25 ~ 50 ohm-cm resistivity

<100> crystal orientation

2. INITIAL WAFER CLEANING

visual inspection under strong light

piranha $H_2SO_4 : H_2 O_2$ 5:1 10min

deionized water (DI) rinse, N_2 blow dry

HF:DI 1:10 dip 20sec

DI rinse and N_2 blow dry

3. INITIAL OXIDATION ~ 1000 angstroms

N_2 4.0cm 1000 deg C push 3min

O_2 6.5cm 1000 deg C oxide 110min

O_2 6.5cm 1000 deg C oxide 110min

N_2 4.0cm 900 deg C anneal 10min

N_2 4.0cm 900 deg C pull 3min

4. NITRIDE DEPOSITION-LPCVD $Si_3 N_4$ ~700 angstroms

wafer cleaned and very dry

low pressure chemical vapor deposition (LPCVD) furnace

NH_4 : SiH_4 600mT-100mT 450 deg C, 40min

5. MASK #1 ACTIVE AREA DEFINITION

HMDS vapor wafer surface treatment 5min

nitrogen gas purge 10min

AZ1350J positive photoresist(PR), 8000 rpm 30sec

prebake at 90 deg C 20min

projection alignment and exposure

AZ developer:DI 1:1 60sec

postbake at 110 deg C 30min

6. NITRIDE ETCH

barrel type plasma reactor

descum. O_2 .76 torr, 10 watt, 150 deg F, 5min

nitride etch. SF_6 O_2 .1torr, 15watt, 150 deg F

14 min etch until patterns clear

7. FIELD IMPLANT

implant through initial oxide

use PR as implant mask

Dose= Boron, $140 \cdot 10^{13}$ atoms/cm²

implant energy= 110keV, angle= 8 deg

strip off PR

8. LOCAL OXIDATION - .7 μ m

piranha clean

drive-in furnace

O₂: 6.5 cm 1000 deg C push 3 min

O₂: 6.5cm 1000 deg C drive in 20 min

O₂: 3.0cm 900 deg C wet oxide 280 min

N₂: 4.0cm 900 deg C anneal 15 min

N₂: 4.0cm 900 deg C pull 3 min

HF:DI 1:100 dip 90sec

9. MASK #2 DEPLETION THRESHOLD IMPLANT DEFINITION

10. DEPLETION THRESHOLD VOLTAGE IMPLANT

implant through gate oxide

use PR as implant mask

dose: Phosphorous, $1.044 \cdot 10^{12}$ atoms/cm²

implant energy: 150 keV, angle: 8 degree

requires noise compensation for implant

strip off PR

11. ENHANCEMENT THRESHOLD VOLTAGE IMPLANT

implant through gate oxide

no implant mask required

dose: Boron, 2.38×10^{11} atoms / cm^2

implant energy: 50keV, angle: 8 degree

requires noise compensation for implant

12. POLYSILICON DEPOSITION - .45 μm

plasma descum, O_2 .76 torr, 80 watt, ~10min

piranha clean, very dry

LPCVD furnace, 600 deg C, SiH_4 600 mT, 35min

13. PHOSPHORUS PREDEPOSITION

$O_2 : N_2$ 2.5cm : 5cm 950 deg C push 3min

$O_2 : N_2 : POCL$ 2.5cm : 5cm : 9cm 950 deg C pre-dep 15min

$O_2 : N_2$ 2.5cm : 5cm 950 deg C anneal 5min

$O_2 : N_2$ 2.5cm : 5cm 950 deg C pull 3min

HF:DI 1:10 dip 30sec ~

14. MASK #3 POLYSILICON LAYER DEFINITION

15. POLYSILICON ETCH

barrel type plasma reactor

descum O_2 .76torr, 10watt, 150 deg F, 5min

poly etch, SF_6 O_2 .1torr, 15watt, 150 deg F, 4.5 min

etch until color change stabilized

16. SOURCE AND DRAIN N+ IMPLANT

HF dip off source/drain oxide

strip off PR

use poly and field oxide as implant mask

dose: Arsenic, $1.0 \cdot 10^{18}$ atoms/cm²

implant energy: 200 keV, anlg: 8 degree

plasma descum, O_2 .76torr, 80watt, 20min

17. IMPLANT ANNEALLING

N_2 : 4cm 900 deg C push 3min

N_2 : 4cm 900 deg C anneal 40min

N_2 : 4cm 900 deg C pull 3min

18. CVD OXIDE DEPOSITION - 1.0 μ m

SiH_4 : N_2 : P 8.8cm:5cm:9cm, N_2 diluent: 5cm

450 deg C, ~25min

19. CVD OXIDE REFLOW AND SOURCE/DRAIN As DRIVE IN

O_2 : N_2 2.5cm:5.0cm 1000 deg C push 3min

$O_2 : N_2$: POCL 2.5cm:5cm:9cm 1000 deg C pre-dep 20min

N_2 5.0cm 1000 deg C anneal 5min

N_2 5.0cm 1000 deg C pull 3min

20. MASK #4 CONTACT DEFINITION

21. CONTACT ETCH

buffer HF NH_4OH : HF 5:1 ~8min

use two step etch to avoid over etch

strip off PR

22. PHOSPHORUS PLUG AND GETTERING

wafer back side HF etch

piranha clean

$O_2 : N_2$ 2.5cm : 5.0 cm 1000 deg C push 3min

$O_2 : N_2$: POCL 2.5cm:5cm;9cm 1000 deg c pre-dep 20min

N_2 : 5.0 cm 1000 deg C anneal 5min

N_2 : 5.0 cm 1000 deg C pull 3min

23. MASK #5 CONTACT HOLE DIP

HF:DI 1:10 dip ~45sec

strip off PR 24. ALUMINUM DEPOSITION ~ 0.8 μm

piranha clean

HF:DI 1:10 dip ~10sec

DI rinse, nitrogen blow very dry

Al deposition with Veeco-Roger vacuum system, ~ .8um

25. MASK #6 METALLIZATION PATTERN DEFINITION

26. ALUMINUM ETCH

Al type A etchant, 27 deg C, ~ 6 min

DI rinse thoroughly

inspection

strip off PR

27. SINTERING

$H_2 : N_2$ 1:9 15cm, 350 deg C, 20min

28. BACKSIDE PREPARATION

use Q-tip HF dip off backside oxide

II.2 - DEVICE CHARACTERISTICS

enhancement device V_t : ~ 0.6 V
depletion device (buried channel) V_{td} : ~ 3.7 V
field threshold voltage : ~ 18 V
P-N junction breakdown voltage : ~ 23 V
punch through voltage (for $L \sim 6$ μm) : ~ 20 V
source & drain N+ resistivity : ~ 20 ohm/square
N+ doped poly resistivity : ~ 15 ohm/square
capacitor bottom plate resistivity : ~ 50 ohm/square
contact resistivity ($5\mu \times 7\mu$) : < 10 ohm/square
Al resistivity : $.02$ ohm

minimum contact size resolved : $3 \mu\text{m} \times 3 \mu\text{m}$
minimum device channel length resolved : $3 \mu\text{m}$

functional circuit yield at wafer stage : > 85 %

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