COMPACT SHORT-CHANNEL IGFET MODEL (CSIM) *And* A COMPACT IGFET CHARGE MODEL

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Title page

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ABSTRACT

The Compact Short-Channel IGFET Model (CSIM), described in this report, was especially formulated to have four important features: First, it is derived from basic device physics, and therefore characterizations can provide a link to process understanding and control. Second, it is compact and therefore suitable for incorporation in computer-aided circuit simulation programs. Third, it is hierarchical, where the lower levels are analogous to the Ebers-Moll to Gummel-Poon hierarchy established for bipolar models. However, at the highest level, model parameter values are extractable from measurements in a fully automated fashion. This important characteristic allows state-of- the-art processes to be characterized, for circuit design applications, without detailed analytical models of any higher-order device physics effects. In affect, a lower-order device physics model, with tabled entries for appropriate model parameters is employed to achieve accuracy, when the device physics understanding and modeling lags the process evolution. Fourth, the automated characterization applies to devices of various sizes, which results in an associated set of process models, formulated as a standard process file. The process file can be combined with appropriate mask dimensions, to calculate the set of electrical parameters for a particular device size within a circuit simulation program. This new model coupled with its inherent auto-characterization characteristics and immediate applicability to new processess, can form the basis for a standard interface between IC process facilities and integrated circuit designers.

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LIST OF SYMBOLS

a	conductance degradation coefficient
C_{ox}	oxide capacitance per unit area
dL/dW	process compensation of device length/width
E_{crit}	critical field for velocity saturation
g	coefficient of average body effect on drain current
I_{DS}	drain current
I_{DSAT}	drain current at saturation region
K_1	body effect coefficient of V_{th} with short- and narrow- channel effects
K_2	source/drain depletion charge sharing effect coefficient
L	channel length
L_D	lateral diffusion of source and drain junctions
L_M	masked channel length
N_B	substrate doping concentration
N_{ss}	surface state density
n_i	intrinsic carrier concentration
q	electronic charge
T_{ox}	oxide thickness
U_0	mobility degradation coefficient
U_{0B}	sensitivity of U_0 to substrate bias
U_{0Z}	U_0 at zero substrate bias
U_1	velocity saturation coefficient
U_{1B}	sensitivity of U_1 to substrate bias
U_{1D}	sensitivity of U_1 to drain-source voltage, at $V_{DS}=V_{DD}$
U_{1Z}	U_1 at zero substrate bias
V_{BS}	substrate-source voltage
V_{DS}	drain-source voltage
V_{DSAT}	saturation voltage
V_{FB}	flat-band voltage
V_{GB}	gate-substrate voltage
V_{GS}	gate-source voltage
V_{th}	threshold voltage
V_{t0}	threshold voltage for V_{BS} & $V_{DS}=0$
W	channel width
W_M	masked channel width
β	conductance coefficient
β_0	intrinsic conductance coefficient
β_Z	β_0 at zero substrate and drain-source biases
β_{ZB}	sensitivity of β_0 to substrate bias at $V_{DS}=0$
β_S	β_0 at zero substrate bias and $V_{DS}=V_{DD}$
β_{SB}	sensitivity of β_0 to substrate bias at $V_{DS}=V_{DD}$
β_{SD}	sensitivity of β_0 to drain-source bias at $V_{DS}=V_{DD}$
μ_{n0}	intrinsic surface mobility
φ_S	surface potential at strong inversion
φ_{ms}	gate to semiconductor work function
η	drain-induced barrier lowering coefficient
η_Z	η at zero substrate bias and V_{DD}
η_B	sensitivity of η to substrate bias
η_D	sensitivity of η to drain-source voltage

I. Introduction

With the current rapid development of high performance MOS IC technology, the minimum feature size has advanced from 10μm in production in 1971 to 2.5μm in 1981 [1]. The process of device shrinkage is continuing and is expected to result in a minimum feature size in the submicron domain, in the late 1980's. This continuous reduction in minimum feature size makes possible the explosive growth in the scale of circuit integration, and 1,000,000 transistor chips may become the norm in the future.

The purpose of the work reported herein is the development of an MOS transistor model, which will be the cornerstone of a facility for process-oriented circuit design, applicable over this period. This facility include a fully automated process characterization system and an IC process-oriented version of SPICE circuit simulation program. These latter efforts are described elsewhere [2][3]. The process-oriented simulator accepts the process file produced by the auto-characterization system. Designers need only describe the layout geometries of devices and parasitic elements, to execute process-oriented circuit simulations.

Many articles on IGFET modeling have appeared in the literature [4]-[13] and efforts to model ever smaller and more complex IGFET devices continue at a rapid pace. We begin by discussing the zero-order model, used in the early pMOS circuit simulation, where

$$I_{DS} = \beta_0 (V_{GS} - V_t - \frac{V_{DS}}{2}) V_{DS} \qquad (1)$$

below saturation and

$$I_{DS} = \frac{\beta_0}{2} (V_{GS} - V_t)^2 \qquad (2)$$

above saturation, and here the threshold voltage V_t is a constant. Saturation occurs when sufficient drain-source votage (V_{DSAT}) is applied to pinch off the

channel at the drain, $V_{DSAT} = V_{GS} - V_t$.

The zero-order model neglects a fundamental effect, which is the consequence of finite resistivity of the substrate. This bulk-doping or body effect acts as a back gate. That is, after the channel (in an n-channel device) is established, an "n-p" junction is formed at the back side of the channel. The p value is, of course, the substrate doping.

As a current flows in the channel, the "I-R" drop in effect induces a reverse bias across this n-p junction. The depletion region charge associated with this back gate must be accounted for according to Gauss Law. The result is a charge term varying as the square root of potential, which, when integrated along the channel from the source to drain, with potential as the running variable, leads to the following first-order model [2]:

$$I_{DS} = \beta_0 \left[(V_{GS} - \varphi_S - V_{FB}) V_{DS} - \frac{V_{DS}^2}{2} - \frac{2\sqrt{2 q \varepsilon_{si} N_B}}{3 C_{ox}} \right.$$
$$\left. * \left[(V_{DS} + \varphi_S - V_{BS})^{\frac{3}{2}} - (\varphi_S - V_{BS})^{\frac{3}{2}} \right] \right] \qquad (3)$$

The 3/2 power terms result from the integration of the square root dependent bulk-doping effect evaluated at the two limits of the integration. Furthermore, the threshold voltage (the value at which the above expression yields current) is

$$V_t = V_{t0} + \frac{\sqrt{2 q \varepsilon_{si} N_B}}{C_{ox}} \left[\sqrt{\varphi_S - V_{BS}} - \sqrt{\varphi_S} \right] \qquad (4)$$

where V_{t0} is the threshold voltage for zero substrate bias.

The expression for the saturation voltage V_{DSAT} for this first-order model is quite complex but is very simply defined. One differentiates the expression for I_{DS} with respect to V_{DS}; sets this to zero and solves for the resulting values of V_{DS} (V_{DSAT}) and I_{DS} (I_{DSAT}). For values of V_{DS} greater than this, I_{DS} is constant (saturated) at the value I_{DSAT}.

For many years the first-order theory was quite adquate for accurate IC design. Problems began appearing as more and more two-dimensional effects had to be taken into account for small size transistors.

A new approach, suitable for design, is the direct utilization of I-V tables for circuit simulation models [14]. This at first sounds attractive, but suffers from several fundamental problems. First, it is highly desirable to be able to evolve the proper device sizes while evolving the design. The direct table look-up approach assumes the number of device sizes to be employed in a design is known and small and I-V curves are available. Second, interpolation between points assumes noise-free and glitch-free data, neither of which can be guaranteed. Third, relatively little feedback to process and device engineers results from this approach. This point is very important when considering the level of characterization necessary to support a high performance MOS process.

The electrical characterization of IC processes must serve two areas, the process area and the design area. It is desirable that the chosen modeling and parameterization be suitable for both. The reason for this is to avoid the undesirable consequence of having two separate approaches which leads to potential confusion and resulting serious mistakes. The approach proposed in this paper is to characterize devices of different sizes and reduce this data to a device size independent set of process parameters. This "process file" provides feedback for control of the process. For circuit simulations, the process file is combined with the appropriate mask dimensions and the device electrical model parameters calculated in a simple front-end section of code. The new MOS device model, described in this paper, was especially constructed to meet the above criterion. It is accurate yet relatively simple. It relates to the fabrication process yet is especially suitable for circuit design. And finally, it lends itself to fully automatic characterization (extraction of the parameter values for the process file) from conventional I-V measurements. Such a model is referred to

as suitable for the support of Process-Oriented IC Design.

A process-oriented short-channel IGFET model is presented in this paper. This model builds upon an extended form of the Bell Labs CSIM (Compact Short-channel IGFET Model) [15]-[18]. The extensions include a term in the threshold voltage expression which accounts for the effects of depletion charge sharing by the source and drain [19], and incorporation of the effects resulting from a continuous velocity saturation characteristic. It is also extended to include the case of an ion-implanted channel device where a steplike profile for the impurity distribution is assumed. This profile proves to be adequate for the shallow implanted layers commonly encountered in modern IC technology.

In practice, it is found that some electrical parameters have dependence on drain-source (V_{DS}) and substrate-source (V_{BS}) applied voltages. Details of the formulaton will be given later, but at this stage the concept of table structured model coefficients is introduced. A simple illustration is given by the representation of β_0, from Eq.(1), as a table of entries, with a different entry for each applied value of V_{DS} and V_{BS}. The coefficient β_0 becomes a 2-D table[V_{DS}, V_{BS}]. The V_{GS} dependence is represented by an analytical formula, for example Eq.(1), while accuracy inherent in full 3-D (V_{DS}, V_{BS}, V_{GS}) table look-up model is obtained by a 2-D table, ($\beta_0[V_{DS}, V_{BS}]$), for the coefficient of the analytical formulation. Regional extraction is employed to obtain coefficient values (table entries) for parameters assured strictly constant in other models. In some cases the 2-D table is reduced to a 1-D one. For example, mobility is characterized in the limit as V_{DS} approaches zero, while velocity saturation (for suitably short-channel devices) is characterized as V_{DS} approaches the V_{DD} value for the process. In this way, the 2-D table formulation for some coefficients are reduced to an empirical analytical form, generally depending only on V_{BS}.

The extended CSIM has 8 electrical model parameters, four of which are found to have some bias (V_{DS} and V_{BS}) dependencies. In the process of examining the characteristics of a wide variety of p- and n-channel devices, ranging to sub-micron effective dimensions, an analytical representation with 17 electrical model parameters, per device size, evolved as the model CSIM2, reported herein.

The short-channel drain current model, with equations as simple as the zero-order model, is proposed in section II. Section III describes the 8 electrical parameters and their relationships with the process parameters. The characteristics of the 8 electrical parameters are analyzed and an extension to a 17 electrical parameter model is developed in section IV. Section V addresses the issue of combining design information (layout) with the process file information to generate the linked list of required electrical model parameters for accurate process-oriented circuit analysis. In section VI, comparison between simulated and measured data confirms the validity of the model. Conclusions are stated in section VII.

II. CSIM1 Model

The CSIM model evolved from an effort to describe compactly and accurately the characteristics of short-channel insulated gate field effect transistors (IGFET's) for efficient utilization in circuit analysis programs and also to directly relate these electrical (device) model parameters with process (the process file) parameters via a parameter calculator. An important additional aspect of the work is a technique of extracting values of the electrical (device) and process parameters from measurements on test structures.

The original CSIM model, called CSIM0, is defined by 8 model parameters [17,20]: the intrinsic conductance coefficient β_0, the flat-band voltage V_{FB}, the surface inversion potential φ_S, the body effect coefficient K_1, the source/drain

depletion charge sharing effect coefficient K_2, the mobility degradation coefficient U_0, the velocity saturation coefficient U_1, and the drain-induced barrier lowering coefficeint η.

In this work, we rederive this model as CSIM1. The detailed derivation is described in the appendix. The drain current equations are as follows:

Cut-off Region [$V_{GS} < V_{th}$],

$$I_{DS} = 0. \tag{5}$$

Triode Region [$V_{GS} > V_{th}$ and $0 < V_{DS} < V_{DSAT}$],

$$I_{DS} = \frac{\beta}{(1 + U_1 * V_{DS})}\left[(V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right] \tag{6}$$

$$\text{where} \quad \beta = \frac{\beta_0}{1 + U_0(V_{GS} - V_{th})} \tag{7}$$

Saturation Region [$V_{GS} > V_{th}$ and $V_{DS} > V_{DSAT}$],

$$I_{DS} = \frac{\beta(V_{GS} - V_{th})^2}{2aK} \tag{8}$$

$$\text{where} \quad K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2}, \quad v_c = \frac{U_1(V_{GS} - V_{th})}{a}$$

$$\text{and} \quad V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}} \tag{9}$$

The conductance coefficient β, conductance-degradation coefficient a, and threshold voltage V_{th}, which models small-geometry effects, are functions of bias. Additional detail on the derivation of CSIM1 model can be found in the appendix.

III. Characteristics of the Model Parameters

Electrical characteristics are controlled by the values of 8 electrical model parameters, for a particular (coded) device size (channel width, W and length, L). The first 5 electrical parameters, which model the threshold voltage, are extracted from electrical measurements of the threshold voltage, V_{th}.

$$V_{th} = V_{FB} + \varphi_S + K_1\sqrt{\varphi_S - V_{BS}} - K_2(\varphi_S - V_{BS}) - \eta V_{DS} \quad (10)$$

V_{FB} is related to processing by

$$V_{FB} = \varphi_{ms} - \frac{qN_{ss}}{C_{ox}} \quad (11)$$

φ_S is related to processing by

$$\varphi_S = 2\frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right) \quad (12)$$

For the case of an ion-implanted channel device, an effective φ_S corresponding to a step doping profile [21] is used.

K_1 is related to processing by

$$K_1 = \frac{\sqrt{2q\varepsilon_{si}N_B}}{C_{ox}} \quad (13)$$

The physical effect modeled by this term is the bulk doping (back-gate bias) effect.

The physical effect modeled by K_2 and η is the terminated depletion charges by electrical field lines starting from the source and drain. This effect is equivalent to effectively lowering the dopant concentration and is in general a function of channel length L. A group of analytical models which predict the reduction in the threshold voltage compared to the long-channel value assume geometric form for the source and drain depletion regions and how they merge with the gate-induced depletion region. While this approach is helpful for estimates of parametric behavior, it has limited validity to device design because it depends on the assumed geometry for the depletion regions. Ratnakumar, et al [19] developed a short-channel threshold voltage model based on an analytical solution to the two-dimensional Poisson equation in the depletion region of an MOS transistor. This threshold voltage lowering effect for short-channel devices is modeled by parameter K_2 and η in the CSIM model.

η is extracted from electrical measurements of threshold voltage and is related to processing approximately by

$$\eta = \eta_0 + \eta_n \frac{T_{ox}}{L} \tag{14}$$

where η_0 is a small empirical parameter, whereas η_n is approximately $\frac{\varepsilon_{si}}{\pi \varepsilon_{ox}}$. The physical origin of this term is similar to the K_2 effect. For short-channel devices, as V_{DS} is increased the associated two-dimensional drain-induced field lines terminate on charges in the channel region and, indeed, induce additional charges. This results in finite output conductance in the saturation region or alternately, a reduction in threshold voltage with increasing V_{DS}.

The last 3 electrical parameters model the drain current. The effective conductance coefficient β is defined by

$$\beta = \frac{\beta_0}{1 + U_0(V_{GS} - V_{th})} \tag{15}$$

β_0 is extracted from electrical measurements and has the classical form $\beta_0 = \mu_n C_{ox} \frac{W}{L}$, where μ_n is the low field electron mobility in an inverted IGFET channel.

U_0 is an extracted parameter. It models the degradation of channel mobility with increases in gate-source voltage above threshold. The two components modeled are associated with the vertical and horizontal components of the electrical field.

As devices are scaled to smaller dimensions, without an associated reduction in supply voltages, short-channel characteristics become dominated by carrier saturation effects. The consequence is a reduction in saturation current and a linear rather than a square dependence on $(V_{GS} - V_{th})$. In the extended CSIM model, the dependence of carrier velocity on horizontal electrical field takes the form

$$v = \mu_n E_y = \frac{\mu_{n0} E_y}{\left[1 + \frac{E_y}{E_{crit}}\right]} \tag{16}$$

where $E_{crit} = v_{sat}/\mu_{n0}$. Fig.1 shows the velocity versus electric field charateristic [22]. The velocity saturation coefficeint U_1 is defined by

$$U_1 = \frac{1}{E_{crit} L} \tag{17}$$

This model, which is referred to as CSIM1, contains eight electrical parameters. However, four of the parameters strictly model the threshold voltage characteristic is a function of back-gate bias ,V_{BS}, at zero drain-source voltage, V_{DS}. The other four parameters are truly constants only in a theoretical sense.

IV. Extension of the 8 Electrical Parameter CSIM1 Model to the 17 Electrical Parameter CSIM2 Model

The generalization of CSIM1 to one of tabled model coefficients is referred to as CSIM3. The reduction of these table to a form suitable for efficient circuit simulation is referred to as CSIM2. Fig.2 shows the hierarchy of CSIM-1, 2, and 3. The rationale for this is described below.

Device physics models suitable for integrated circuit design, evolve behind the IC process. This pattern has persisted for many years and is expected to continue indefinitely. The merchant semiconductor companies cope with this condition by close coupling of their process and circuit development teams. In the future this mode of new product development will become increasingly supplemented by what is referred to as design into silicon foundries. This creates a new pressure upon device model generation. We are approaching a period of rapid growth in applications and utilization of IC processes by a rapidly growing number of non-traditional designers. Competition in the market place will force a significant number to seek to employ relatively recent IC process generations, where adquate models are lacking for accurate circuit simulation. In many

cases the designer is not directly affiliated with the organization providing the process fabrication, greatly increasing the likelihood of incomplete or misinterpreted characterization information. The result is less than optimal exploitation in a timely fashion of the industries evolving capabilities.

The CSIM models proposed in this paper were developed specially to attack this problem by development of a fully automated MOS device characterization facility, which generates table-look-up models for device parameters, if the new process has evolved beyond the adequacy of the current models. This is similar to the direct utilization of I-V tables for circuit simulation models [12], but differs in that the analytical form of the model is still retained and exploited, and a table-look-up is only resorted to if necessary. Furthermore the tables are not current $I_{DS}(V_{DS}, V_{BS}, V_{GS})$, i.e. three dimensional, but are of model parameters, and are two dimensional, i.e. $\beta_0(V_{DS}, V_{BS})$. This greatly reduces the amount of data required to characterize a MOS process over a wide range of device sizes.

Shown in Fig. 3 is a typical example of the β_0/β_{00} as a function of V_{DS} and V_{BS}, where β_0 is the value extrapolated to $V_{GS} = V_{th}$ and β_{00} is the value extracted to $V_{GS} = V_{th}$ and $V_{DS} = V_{BS} = 0$. Note that the conductance coefficient in saturation region is some 50% greater than that in the linear region. Shown in Fig. 4 is the conventional plot of inverse β_0 versus masked channel length. Note that the electrical channel lengths obtained are essentially the same as extrapolated from linear (β_{00}) and saturation (β_0 for $V_{DS} = 5v$ and $V_{BS} = 0$) values. Fig. 5 displays the threshold voltage charateristic for this device. The drain-induced barrier lowering coefficient η, which models the effect of V_{DS} on the threshold voltage, has a dependence on V_{DS} and V_{BS}. Fig. 6 shows the extracted U_0 and U_1 charateristics for this device respectively.

Based on the observed electrical parameter characteristics, the 8-parameter CSIM1 model can be extended to a 17-parameter CSIM2 model to

accurately reflect the characteristics of modern MOS devices. The bias dependencies of the 4 CSIM1 parameters are described below, and form the basis for the 17 parameter model, CSIM2.

U_0 can be modeled by two parameters:

U_{0Z}, the value at zero substrate bias, and

U_{0B}, the sensitivity of U_0 to substrate bias.

U_1 can be modeled by two parameters:

U_{1Z}, the value at zero substrate bias,

U_{1B}, the sensitivity of U_1 to substrate bias, and

U_{1D}, the sensitivity of U_1 to drain-source voltage, at $V_{DS}= V_{DD}$.

η can be modeled by three parameters:

η_Z, the value at zero substrate bias and $V_{DS}=V_{DD}$

η_B, the sensitivity of η to substrate bias, and

η_D, the sensitivity of η to drain-source bias, at $V_{DS}= V_{DD}$.

β_0 can be modeled by five parameters:

β_Z, the value at zero substrate and drain-source biases,

β_{ZB}, the sensitivity of β_0 to substrate bias at $V_{DS} = 0$,

β_S, the value at zero substrate bias and at $V_{DS}=V_{DD}$,

β_{SB}, the sensitivity of β_0 to substrate bias at $V_{DS} = V_{DD}$, and

β_{SD}, the sensitivity of β_0 to drain-source bias at $V_{DS} = V_{DD}$.

V. Parameter Calculation

Each CSIM2 electrical parameter P is related to device size by

$$P = P_0\left(1 + \frac{P_L}{L} + \frac{P_W}{W}\right) \tag{18}$$

where P_0, P_L and P_W are obtained by analysis of P values over ranges of electrical channel length (L) and channel width (W). Note that the length (L) and width (W) of the device are the effective channel length and width. The masked length L_M,

and width W_M, are converted to the effective channel length and width by the following equations.

$$L = L_M + dL \qquad W = W_M + dW \tag{19}$$

where dL and dW is the difference between the final electrical and masked channel length and width.

The file containing the 54 parameter values (with P_0, P_L, P_W for each of the 17 parameters plus user supplied information for operating voltage, temperature, and gate oxide thickness) constitutes a "process file" for one type of device (enhancement- and depletion- mode nMOS and n- and p- channel CMOS). The process file is combined with the appropriate mask dimensions to generate 17 electrical parameter values for a particular device size. Fig. 7 shows how the CSIM2 model fits into circuit simulation programs such as SPICE [23].

During the model evaluation in circuit simulation, the eight electrical parameters are calculated out of the 17 CSIM2 parameters for a specific bias condition as follows:

V_{FB}, φ_S, K_1, K_2 are bias-independent,

$$U_0 = U_{0Z} + U_{0B} V_{BS} \tag{20}$$

$$U_1 = U_{1Z} + U_{1B} V_{BS} + U_{1D} (V_{DS} - V_{DD}) \tag{21}$$

$$\eta = \eta_0 + \eta_B V_{BS} + \eta_D (V_{DS} - V_{DD}) \tag{22}$$

β_0 is obtained by quadratic interpolation through three data, β_0 at $V_{DS} = 0$, β_0 at $V_{DS} = V_{DD}$, and the sensitivity of β_0 to V_{DS} at $V_{DS} = V_{DD}$, where

$$\beta_0 (\text{at } V_{DS} = 0) = \beta_Z + \beta_{ZB} V_{BS} \tag{23}$$

$$\beta_0 (\text{at } V_{DS} = V_{DD}) = \beta_S + \beta_{SB} V_{BS} \tag{24}$$

VI. Experimental Results

Experiments were carried out through a newly developed automatic parameter extraction system for CSIM2 model [2]. Sample wafers, fabricated with an

advanced CMOS process as well as a standard nMOS process in Xerox PARC, were used in the experiments. Gate oxide thickness of the CMOS process is 300 A, while the standard nMOS process has a gate oxide thickness of 700 A.

Fig. 8 shows output characteristics of a width/length=20μm/3.5μm nMOS transistor. Simulated data are plotted with solid lines while measured data are displayed with cross marks. Fig. 9 shows similar plots for a 20μm/2μm pMOS transistor. The output characteristics of long-channel transistors are shown in Fig. 10 and 11 for nMOS and pMOS 20μm/20μm transistors. Fig. 12 depicts similar plots for a 50μm/3.5μm nMOS transistor fabricated with the standard nMOS process.

As IGFET device size continues to shrink, the degradation of electrical characteristics induced by hot electron effects becomes increasingly severe. Device breakdown and substrate current due to impact ionization become a problem for these small devices. Recent work on lightly doped drain-source devices show the efforts to alleviate the above problems. In the LDD structure, self-aligned n- regions are introduced between the channel and the n+ drain-source diffusions. This structure increases the breakdown voltage and reduces impact ionization (and thus hot electron effects) by allowing the high electric field at the drain pinch-off region to extend into the n- region.

LDD test structures were fabricated on a P-type silicon wafer with resistivity of 1-2 Ω-cm in the HP IC Lab [24]. The n- region is formed by implanting 5E12 cm^{-2} phosphorus at 80Kev, followed by 0.3μm oxide spacer. Subsequent steps are similar to the process for the conventional device fabrication. Fig. 13 shows output characteristics of a 10μm/1.5μm nMOS transistor. The agreement between measured and simulated results, for conventional as well as LDD IGFET's, clearly indicate the power of CSIM2 and the auto-characterization system.

VII. Conclusion

A simple and accurate model for short-channel IGFET's has been presented. It is compact for efficiency in circuit simulation, and includes the depletion charge sharing, continuous velocity saturation, and nonuniform doping effects. The process file approach used in this model provides a powerful interface between fabrication capabilities and circuit designers. Simulated results agree with measured results at various bias conditions for different device sizes and gate oxide thicknesses. Therefore, this process-oriented CSIM model is well suited for circuit analysis, as well as for process monitoring.

Appendix A: Derivation of CSIM Model [15,16]

An idealized n-channel MOSFET with the coordinate system is illustrated in Fig. 14. The relationship between the electric field (E_{ox}) in the oxide, the gate voltage (V_{GB}) (with respect to the substrate potential), and the electrostatic potential (V_{sur}) at the oxide-semiconductor interface can be understood by considering the energy band diagram in Figure 11. By summing up the voltages on both the gate and the semiconductor side, one obtains

$$V_{ox} + X_m = V_{GB} + \varphi_F + \frac{E_G}{2} - V_{sur} + X_s \tag{A.1}$$

where X_m and X_s are respectively the gate and semiconductor work functions, V_{ox} the voltage across the oxide, E_G the energy bandgap. The gate to semiconductor work function φ_{ms} is defined as

$$\varphi_{ms} = X_m - X_s - \varphi_F - \frac{E_G}{2} \tag{A.2}$$

Combining Equations (A.1) and (A.2), we obtain

$$\begin{aligned} V_{ox} &= T_{ox} E_{ox} \\ &= V_{GB} - V_{sur} - \varphi_{ms} \end{aligned} \tag{A.3}$$

where T_{ox} is the gate oxide thickness. To determine the relationship between E_{ox} and the charge in the semiconductor, let us assume:

(1) The ratio T_{ox}/L is much smaller than 1. This assumption implies that E_{ox} is perpendicular to the gate plane.

(2) The horizontal (parallel to the channel) component E_y of the electric field in the semiconductor at the oxide-semiconductor interface is much smaller than its vertical component E_s. This assumption is reasonable in the region where the channel charge Q_c is substantial, but it is incorrect in the pinch-off regon where Q_c is small. Our main interest is to compute the drain current which is proportional to the integral of Q_c along the channel. In the pinch-off region, where the above assumption is invalid, the contribution to the integral is small. Hence, this assumption is reasonable for drain current computation.

By Gauss's law and assumptions 1 and 2, one obtains

$$\varepsilon_s E_s = \varepsilon_{ox} E_{ox} + Q_{ss} \tag{A.4}$$

where ε_{ox} and ε_s are the dielectric constants of the oxide and the semiconductor, and Q_{ss} the surface charge. E_s consists of three components

$$\varepsilon_s E_s = Q_c + Q_b + \varepsilon_s E_1 \tag{A.5}$$

where Q_b is the depletion charge in the semiconductor and, using the abrupt junction approximation, is given by

$$Q_b = \sqrt{2q\varepsilon_s N_B V_{sur}} \tag{A.6}$$

For short channel devices, this expression is modified due to the influence of the source and drain junction field. E_s in Eq.(A.5) contains a third component E_1 which originates from the drain and will be discussed in detail later.

A qualitative expression for the bulk charge can be derived by considering a MOS structure where alternatively, the source and drain, and the gate are ignored (Fig. 16a and 16b). These diagrams illustrate the influence of source and drain junction field on the bulk charge. According to Gauss's law (Fig. 16a), the electric field E_{ox} at the oxide-semiconductor interface will be balanced by the surface charge Q_{ss}, the channel charge Q_c, and the negative charge Q_b in the depletion region (A) of the substrate. In the absence of the gate (Fig. 16b), the electric field E_j at the junction will be balanced by the charge in the depletion layer (B) near the junction. Now consider the complete structure where the drain, source and substrate are at the same potential and a positive voltage is applied to the gate as shown in Fig. 16c. The depletion charge shown in area (C) has to balance both the electric field E_{ox} coming in from the oxide-semiconductor interface and E_j due to the source or drain to substrate junction. Let a fraction, t, of the charge (C) be used to balance E_j. Since this fraction of charge will not be available to balance E_{ox}, one could say the doping of the substrate is effectively lowered. This fraction, t, will depend on the position along the channel. As an approximation, t should be proportional to the ratio of

charge in (C) to the total depletion charge of $2X_j/L$. Since X_j is proportional to $1/\sqrt{N_A}$, it must be proportional to $1/(L\sqrt{N_A})$. Therefore, the effective fraction of charge f(L,N) that is available to balance E_{ox} can be expressed by

$$f(L,N) = 1 - \frac{K_{vt}}{L\sqrt{N_B}} \tag{A.7}$$

where K_{vt} is a constant. A more elaborate function for f(L,N) and a more rigorous derivation can be found in [8] and [25] which show that f(L,N)is also a function of V_{BS}. However, we found that the additional V_{BS} dependence tends to complicate the formulation and does not add much accuracy to the model. With the modified charge, Eq.(A.5) becomes

$$\varepsilon_s E_s = Q_c + f(L,N)\ \sqrt{2q\varepsilon_s N_A V_{sur}} \tag{A.8}$$

To derive the third component E_1 of the electric field E_s, let us consider the case that V_{DS} is zero but V_{GB} and V_{BS} are non-zero. The substrate is depleted according to the solution of the Poisson equation. When V_{DS} is non-zero, an additional potential will be imposed in the region already depleted. Since no additional charge appears in the Poisson equation (solution for V_{DS} =0), this additional potential will satisfy the Laplace equation. This Laplace equation can be solved under certain simplifying assumptions and the solution gives the additional electric field as shown in Fig. 17. This electric field terminates at the channel and induces additional channel charges which enhance the drain current and result in a finite output conductance in the saturation region.

The following approximations are made to derive a simple expression for E_1.
(1) The source and drain junction depths are small compared to channel length.
(2) Approximate boundary conditions for the Laplace equation (solution denoted by V_1) are V_1=0 at the oxide-semiconductor interface and $V_1 = V_{DS}$ at the drain region. This approximation is illustrated in Fig. 18.

By substitution, it can be shown that

$$V_1 = V_{DS}\,\frac{\theta}{\pi} \tag{A.9}$$

satisfies the Laplace equation in cylindrical coordinates,

$$\left[\frac{d^2V_1}{dr^2}\right] + \left[\frac{1}{r}\right]\left[\frac{dV_1}{dr}\right] + \left[\frac{1}{r^2}\right]\left[\frac{d^2V_1}{d\theta^2}\right] = 0 \tag{A.10}$$

and the boundary conditions. By differentiating V_1 with respect to y at the source, one obtains

$$E_1 = -\frac{V_{DS}}{\pi L} \tag{A.11}$$

With the addition of E_1, Eq.(A.8) becomes

$$\varepsilon_s E_s = Q_o + f(L,N)\sqrt{2qN_A V_{sur}} + \varepsilon_s E_1 \tag{A.12}$$

Combining Eq.(A.3), (A.4), and (A.12), one can express Qc in terms of V_{GB} and V_{sur}.

$$Q_c = C_{ox}\left[V_{GB} - V_{sur} - V_{FB} - K_1\sqrt{V_{sur}}\right] - \varepsilon_s E_1 \tag{A.13}$$

where

$$V_{FB} = \varphi_{ms} - \frac{Q_{ss}}{C_{ox}} \tag{A.14}$$

and

$$K_1 = f(L,N)\ \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \tag{A.15}$$

When the surface is inverted, the surface potential V_{sur} is approximately given by

$$V_{sur} = \varphi_n + \varphi_S - V_{BS} \tag{A.16}$$

where φ_n is the electron quasi-Fermi level. Then Eq.(A.13) becomes

$$Q_c = C_{ox}\left[(V_{GS} - \varphi_n - \varphi_S - V_{FB}) - K_1\sqrt{\varphi_n - V_{BS} + \varphi_S}\right] - \varepsilon_s E_1 \tag{A.17}$$

where

$$V_{GS} = V_{GB} + V_{BS} \tag{A.18}$$

To derive an expression for the drain current, the current flow is assumed to be parallel to the y axis such that

$$\left[\frac{d\varphi_n}{dx}\right]=0 \tag{A.19}$$

and

$$J=q\mu_n n\left[\frac{d\varphi_n}{dy}\right] \tag{A.20}$$

where μ_n is the electron mobility and n the electron density. When Eq.(A.20) is integrated with respect to x and z, one obtains

$$I_{DS}=\mu_n W Q_c\left[\frac{d\varphi_n}{dy}\right] \tag{A.21}$$

Integrating Eq.(A.21) with respect to y* and φ_n,

$$I_{DS}\int_0^L dy=\mu_n W\int_0^{V_{DS}} Q_o\, d\varphi_n \tag{A.22}$$

*If channel shortening, due to finite extent of drain depletion region is included, the upper limit is accordingly reduced.

Combining Eq.(A.17) and (A.22), the drain current is given by

$$I_{DS}=\beta\int_0^{V_{DS}}\left[(V_{GS}-\varphi_n-\varphi_S-V_{FB})-K_1\sqrt{\varphi_n+\varphi_S-V_{BS}}+\eta V_{DS}\right]d\varphi_n \tag{A.23}$$

where β is the conductance coefficient and η is the drain-induced barrier lowering coefficient.

When Eq.(A.23) is integrated with respect to φ_n in the triode region, one obtains

$$I_{DS}=\beta\left[(V_{GS}-\varphi_S-V_{FB})V_{DS}+(\eta-\frac{1}{2})V_{DS}^2-\frac{2}{3}K_1\left[(V_{DS}+\varphi_S-V_{BS})^{\frac{3}{2}}-(\varphi_S-V_{BS})^{\frac{3}{2}}\right]\right] \tag{A.24}$$

Note that Eq.(A.24) is exactly the Ihantola-Moll model [2] if $\eta=0$ and $K_1=\sqrt{2q\varepsilon_{si}N_B}/C_{ox}$, i.e., f(L,N)=1.

Expansion of Bulk Doping Term

The 3/2 power term can be approximated as shown below:

The function

$$F(V_{DS}, \varphi_S - V_{BS}) = \frac{2}{3}\left[(V_{DS} + \varphi_S - V_{BS})^{\frac{3}{2}} - (\varphi_S - V_{BS})^{\frac{3}{2}}\right] \tag{A.25}$$

can be approximated numerically in the range

$$0 < V_{DS} < 10 \text{ volts}$$

and $0.7 < \varphi_S - V_{BS} < 20.7$ volts

by

$$F(V_{DS}, \varphi_S - V_{BS}) = \sqrt{\varphi_S - V_{BS}}\, V_{DS} + \frac{0.25\, g\, V_{DS}^2}{\sqrt{\varphi_S - V_{BS}}} \tag{A.26}$$

where

$$g = 1 - \frac{1}{1.744 + 0.8364\,(\varphi_S - V_{BS})} \tag{A.27}$$

The details of this approximation are discussed in appendix B. Using approximation (A.27), the drain current in the triode region is given by

$$I_{DS} = \beta\left[(V_{GS} - V_{th})\, V_{DS} - \frac{a}{2} V_{DS}^2\right] \tag{A.28}$$

where

$$V_{th} = V_{FB} + \varphi_S + K_1 \sqrt{\varphi_S - V_{BS}} - K_2(\varphi_S - V_{BS}) - \eta V_{DS} \tag{A.29}$$

and

$$a = 1 + \frac{g K_1}{2\sqrt{\varphi_S - V_{BS}}} \tag{A.30}$$

The factor "a" given by equation (A.30) represents the bulk doping effect. The origin of the K_2 term has been explained in the text.

Channel Charge Modeling with Above Formulation

After (A.29) and (A.30) has been inserted into (A.17), the channel charge has the simplifying form

$$Q_c = -C_{ox}(V_{GS} - V_{th} - a\varphi_n) \tag{A.31}$$

Integrating Eq.(A.23) with continuous velocity saturation characteristic (see

Eq.21), one obtain the drain current in triode region to be

$$I_{DS} = \beta \left[(V_{GS} - V_{th} - I_{DS} R_{sat}) V_{DS} - \frac{a}{2} V_{DS}^2 \right] \tag{A.32}$$

where

$$R_{sat} = \frac{1}{W v_{sat} C_{ox}} \tag{A.33}$$

Equation (A.32) can be rearranged as

$$I_{DS} = \frac{\beta}{(1 + U_1 * V_{DS})} \left[(V_{GS} - V_{th}) V_{DS} - \frac{a}{2} V_{DS}^2 \right] \tag{A.34}$$

where

$$U_1 = \beta R_{sat} = \frac{1}{E_{crit} L} \tag{A.35}$$

The conventional definition of saturation voltage, V_{DSAT}, is obtained as from (A.31) with Q_c=0. This condition is not realistic for modern short-channel devices. A more realistic assumption is that at the point in the channel where φ_n goes to V_{DSAT}, the channel current is limited by velocity saturation, i.e.,

$$Q_c = \frac{I_{DSAT}}{W v_{sat}} = C_{ox} (V_{GS} - V_{th} - a V_{DSAT}) \tag{A.36}$$

Substitution of the above into (A.31) yields an upper limit for the integral (A.23) as

$$\varphi_n \longrightarrow V_{DSAT} = \frac{1}{a} [(V_{GS} - V_{th}) - I_{DSAT} R_{sat}] \tag{A.37}$$

Integrating (A.23) with Eq.(A.37) as the upper limit yields the following expression for the drain current in saturation:

$$I_{DSAT} = \beta [(V_{GS} - V_{th} - I_{DSAT} R_{sat}) V_{DSAT} - \frac{a V_{DSAT}^2}{2}] \tag{A.38}$$

Eq.(A.38) can be rearranged as

$$I_{DSAT} = a\beta (V_{GS} - V_{th} - I_{DSAT} R_{sat})^2 \tag{A.39}$$

hence, a quadratic equation for I_{DSAT}. To facilitate comparison to the usual expression, we define

$$I_{DSAT} = \frac{\beta (V_{GS} - V_{th})^2}{2aK} \tag{A.40}$$

where K is obtained by substitution of (A.40) into (A.39), i.e.,

$$K^2 - K\left[1 + \frac{(V_{GS} - V_{th})}{a E_{crit} L}\right] + \frac{(V_{GS} - V_{th})^2}{(2a E_{crit} L)^2} = 0 \tag{A.41}$$

or

$$K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2} \tag{A.42}$$

whereas

$$v_c = \frac{(V_{GS} - V_{th})}{a E_{crit} L} \tag{A.43}$$

If $v_c \ll 1$, then

$$K \longrightarrow 1 + \frac{(V_{GS} - V_{th})}{a E_{crit} L} \tag{A.44}$$

If $v_c \gg 1$, then

$$K \longrightarrow \frac{(V_{GS} - V_{th})}{2a E_{crit} L} \quad \text{and} \quad I_{DSAT} \longrightarrow C_{ox} v_{sat} W (V_{GS} - V_{th}) \tag{A.45}$$

The above expression is well known, and states that in the limit of carrier velocity fully saturated at v_{sat}, the current in saturation is linear and not squared with respect to $(V_{GS} - V_{th})$, and that its value is independent of channel length.

One can obtain the saturation drain voltage V_{DSAT} from (A.37) and (A.40).

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}} \tag{A.46}$$

In the case when $\frac{V_{GS}}{E_{crit} L} \ll 1$,

$$V_{DSAT} \longrightarrow \frac{V_{GS} - V_{th}}{a} \tag{A.47}$$

In the case when $\frac{V_{GS}}{E_{crit} L} \gg 1$,

$$V_{DSAT} \longrightarrow \left[\frac{2(V_{GS} - V_{th}) E_{crit} L}{a}\right]^{\frac{1}{2}} \tag{A.48}$$

Appendix B: Numerical Approximation of Function $F(V_{DS}, \varphi_S - V_{BS})$

The aim is to find an accurate approximation of $F(V_{DS}, \varphi_S - V_{BS})$ over a reasonable voltage range of V_{DS} and $(\varphi_S - V_{BS})$. For convenience, let $V_{KBG} = (\varphi_S - V_{BS})$. For small V_{DS}, the function $F(V_{DS}, V_{KBG})$,

$$K_1 F(V_{DS}, V_{KBG}) = \frac{2}{3} K_1 \left[(V_{DS} + V_{KBG})^{\frac{3}{2}} - (V_{KBG})^{\frac{3}{2}} \right] \tag{B.1}$$

can be expanded as

$$F(V_{DS}, Vjbg) = \sqrt{V_{KBG}}\, V_{DS} + \frac{0.25 V_{DS}^2}{\sqrt{V_{KBG}}} + ... \tag{B.2}$$

The above expansion is invalid when V_{KBG} is much greater than V_{DS}. To alleviate this problem, the expansion is modified to

$$F(V_{DS}, V_{KBG}) = \sqrt{V_{KBG}}\, V_{DS} + \frac{0.25\, g\, V_{DS}^2}{\sqrt{V_{KBG}}} \tag{B.3}$$

where $g(V_{KBG})$ is determined by requiring the expansion (B.3) to give the best fit to $F(V_{DS}, V_{KBG})$ in the desired voltage range.

The value of V_{KBG} are considered in the range 0.7 to 20.7 volts at 2-volt increments. For each fixed V_{KBG}, a parameter g is determined such that the expansion

$$\sqrt{V_{KBG}}\, V_{DS} + \frac{0.25\, g\, V_{DS}^2}{\sqrt{V_{KBG}}} \tag{B.4}$$

will give the best fit to $F(V_{DS}, V_{KBG})$ in a least-square sense, over a range of V_{DS} from 0 to 10 volts at 0.5-volt increments. Having determined g as a function of (V_{KBG}), it is found that it can be accurately represented by

$$\frac{1}{1-g} = P_1 + P_2 V_{KBG} \tag{B.5}$$

where P_1 and P_2 are determined by a least-square fitting over the range of V_{KBG} from 0.7 to 20.7 volts. The result is

$$P_1 = 1.744 \tag{B.6}$$

$$P_2 = 0.8364 \tag{B.7}$$

The root-mean-square error of approximation (B.3) using the above value of P_1 and P_2 is 2% and is illustrated by Fig.19.

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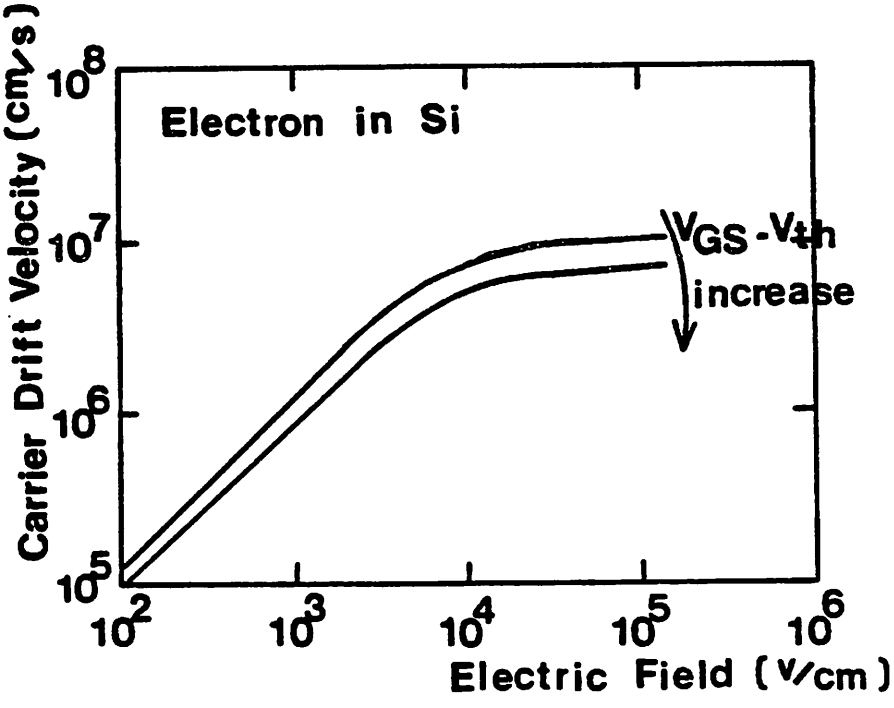

Fig.1 Carrier velocity versus electric field. (22)

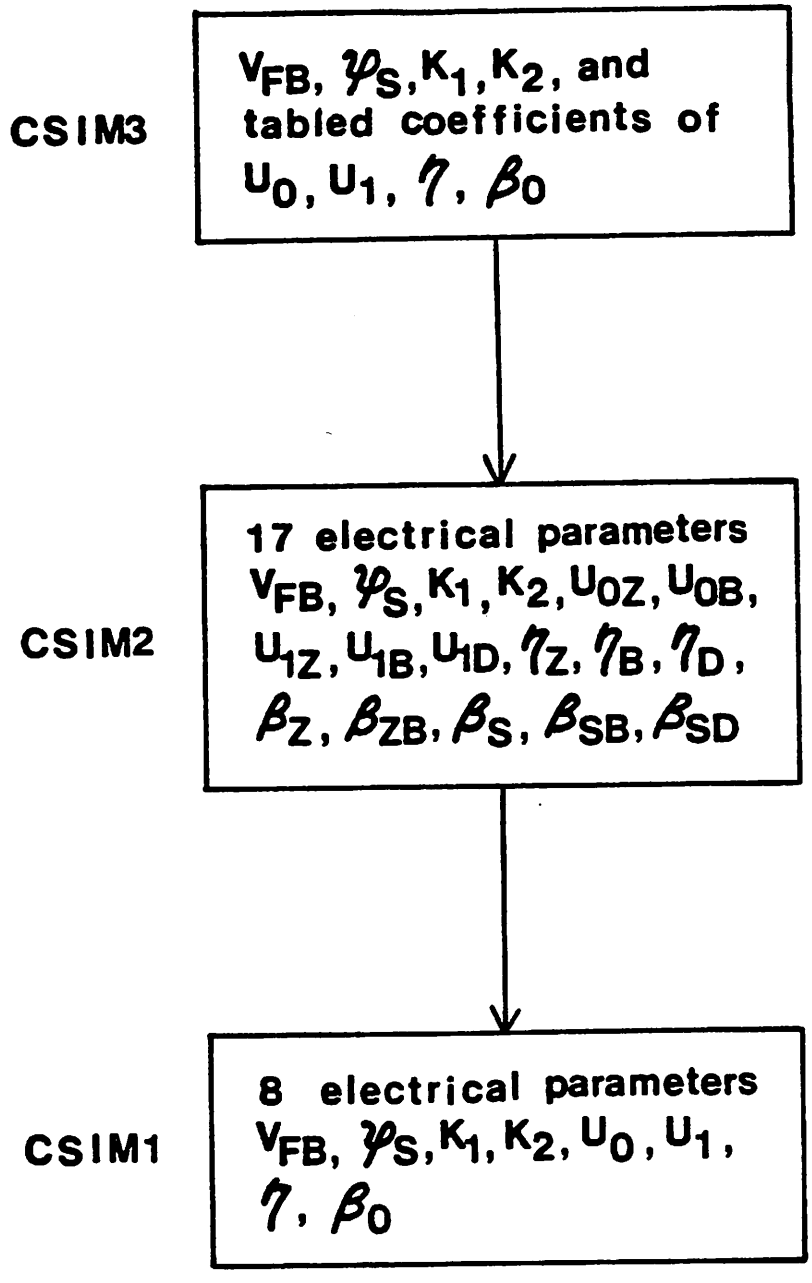

Fig.2 The hierarchy of CSIM-1, 2 and 3.

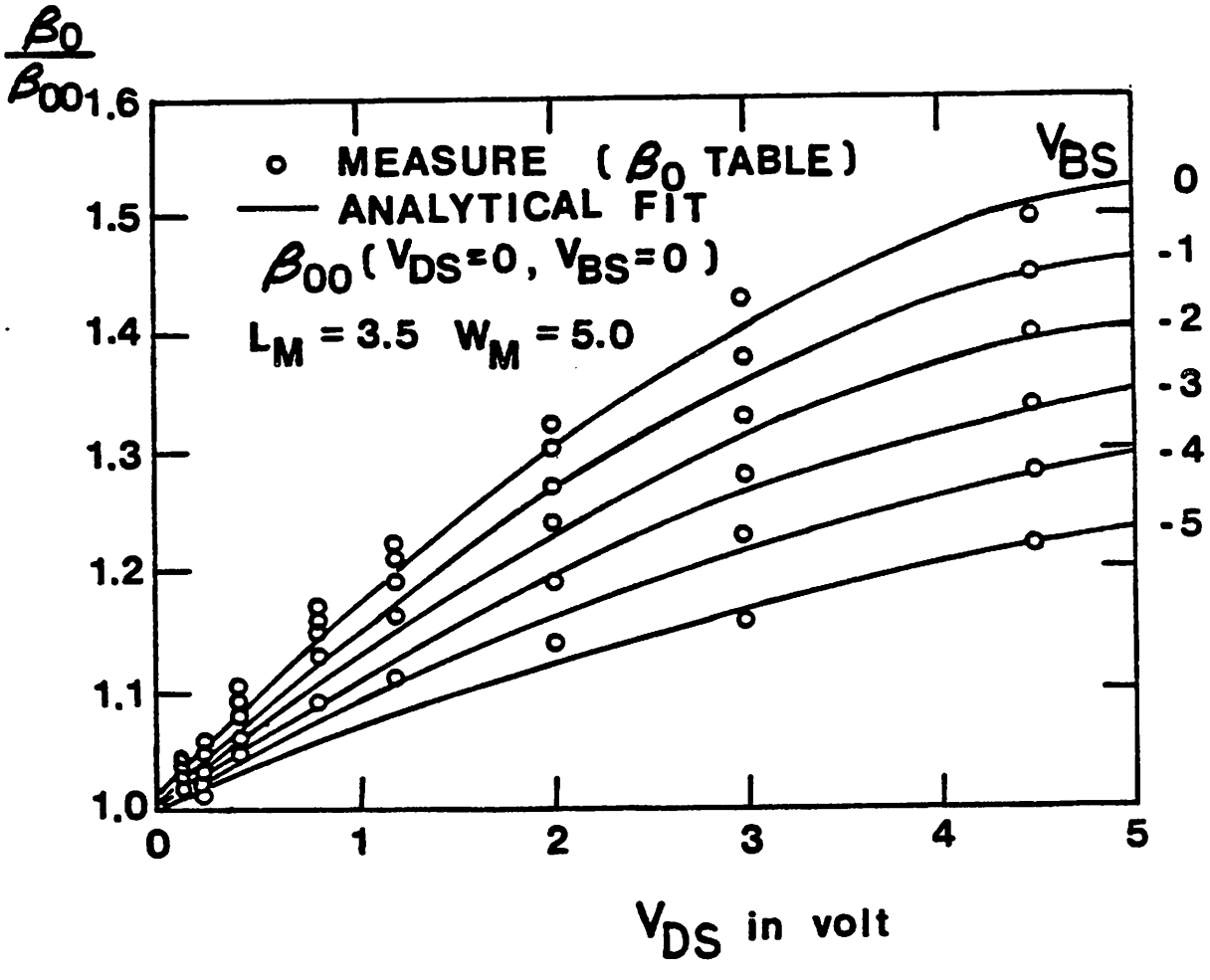

Fig.3 $\frac{\beta_0}{\beta_{00}}$ against drain-source voltage.

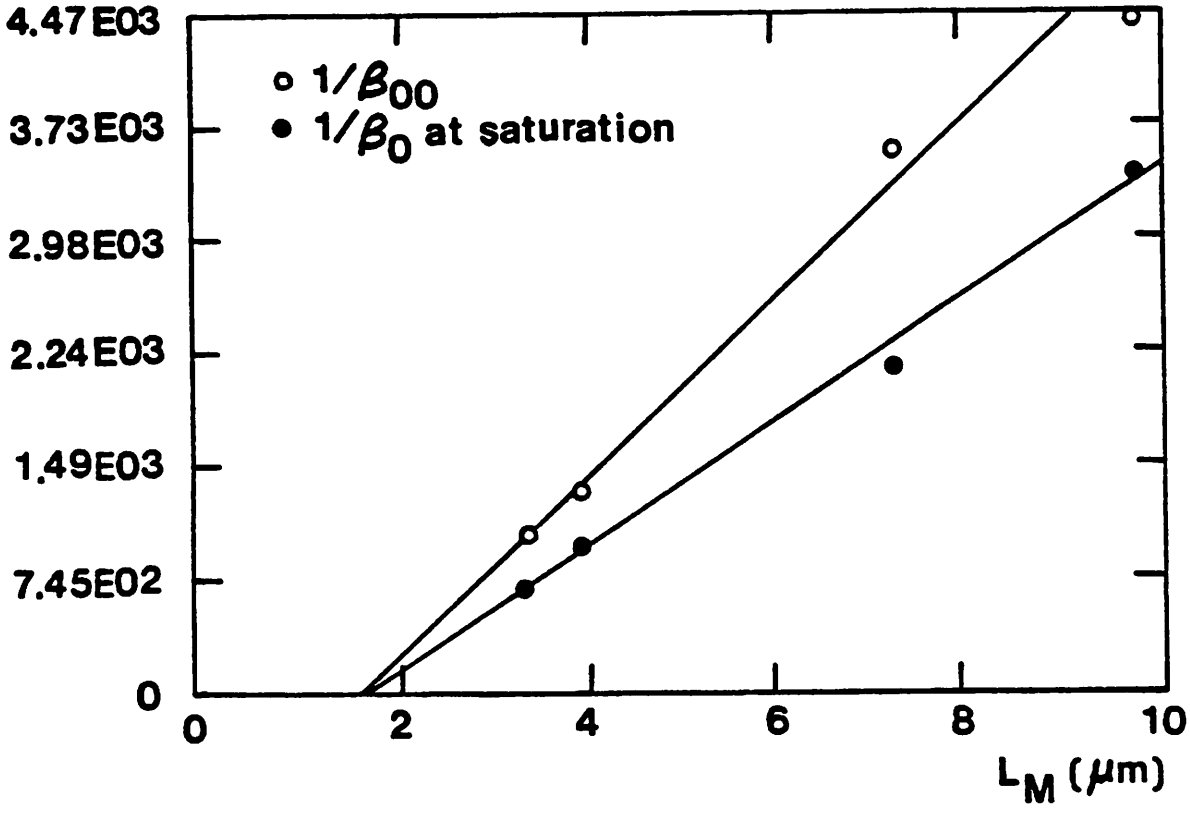

Fig.4 plot of inverse β_0 against masked channel length.

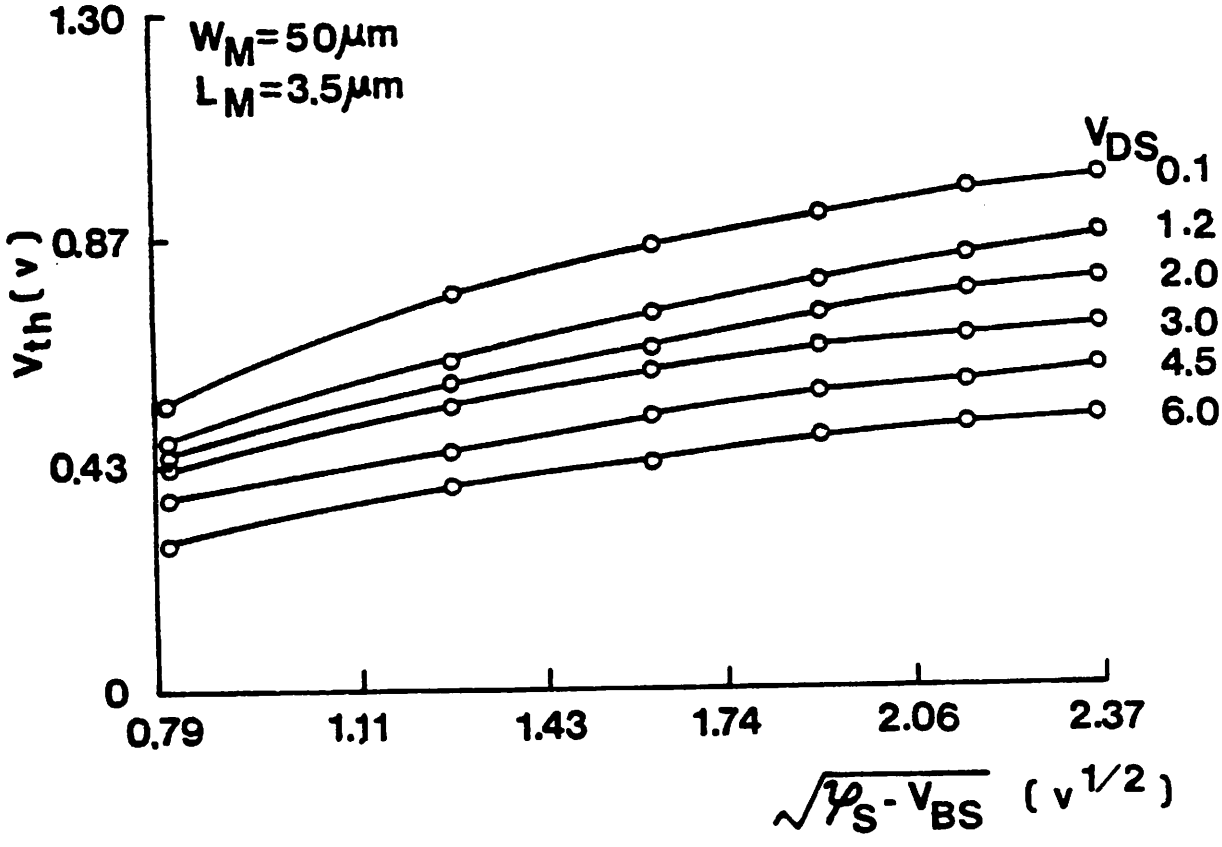

Fig.5 Threshold voltage against $\sqrt{\varphi_S - V_{BS}}$.

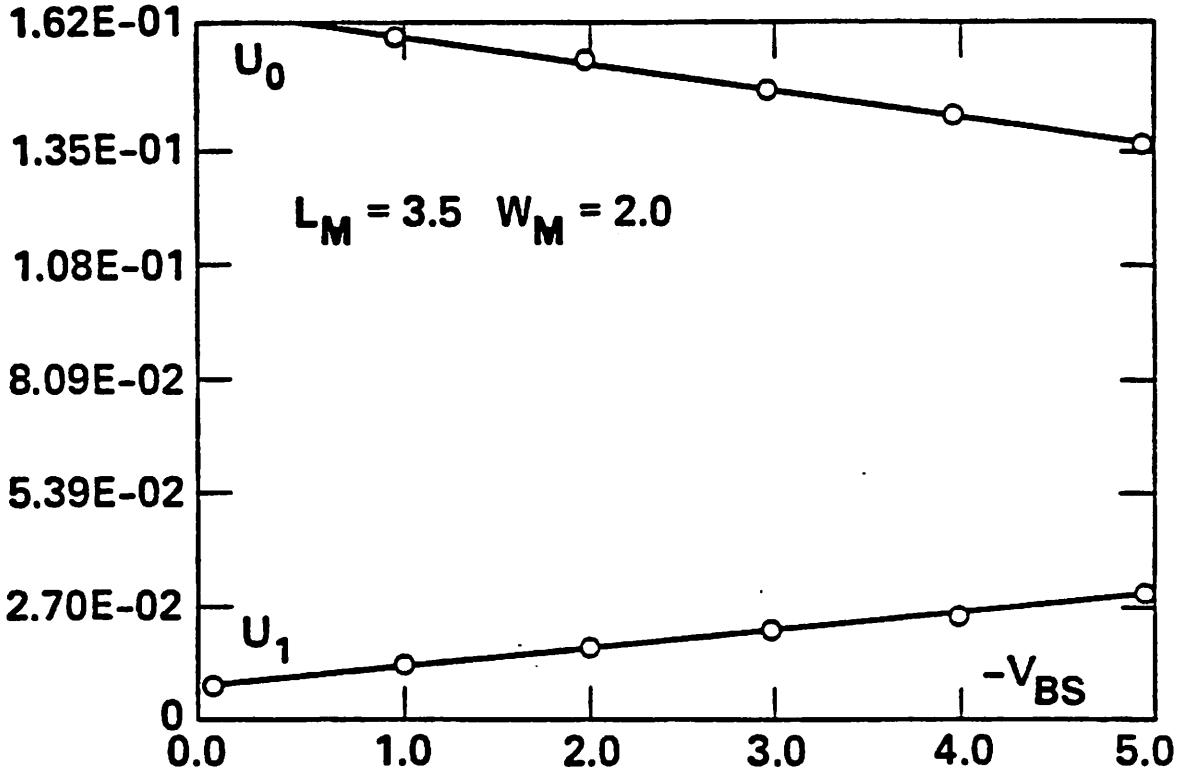

Fig.6 U_0 and U_1 against substrate-source voltage.

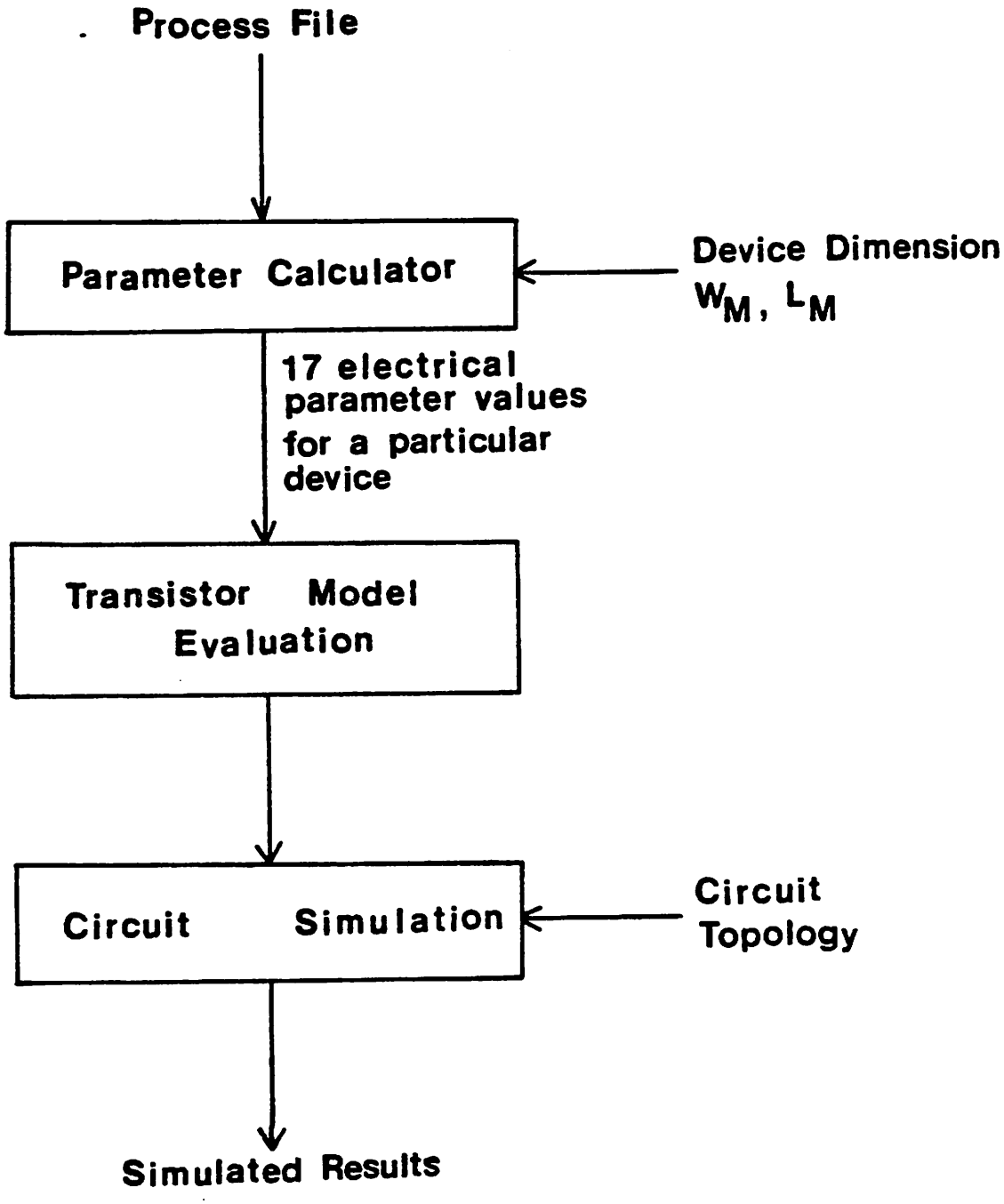

Fig.7 Parameter manipulations in a circuit simulator.

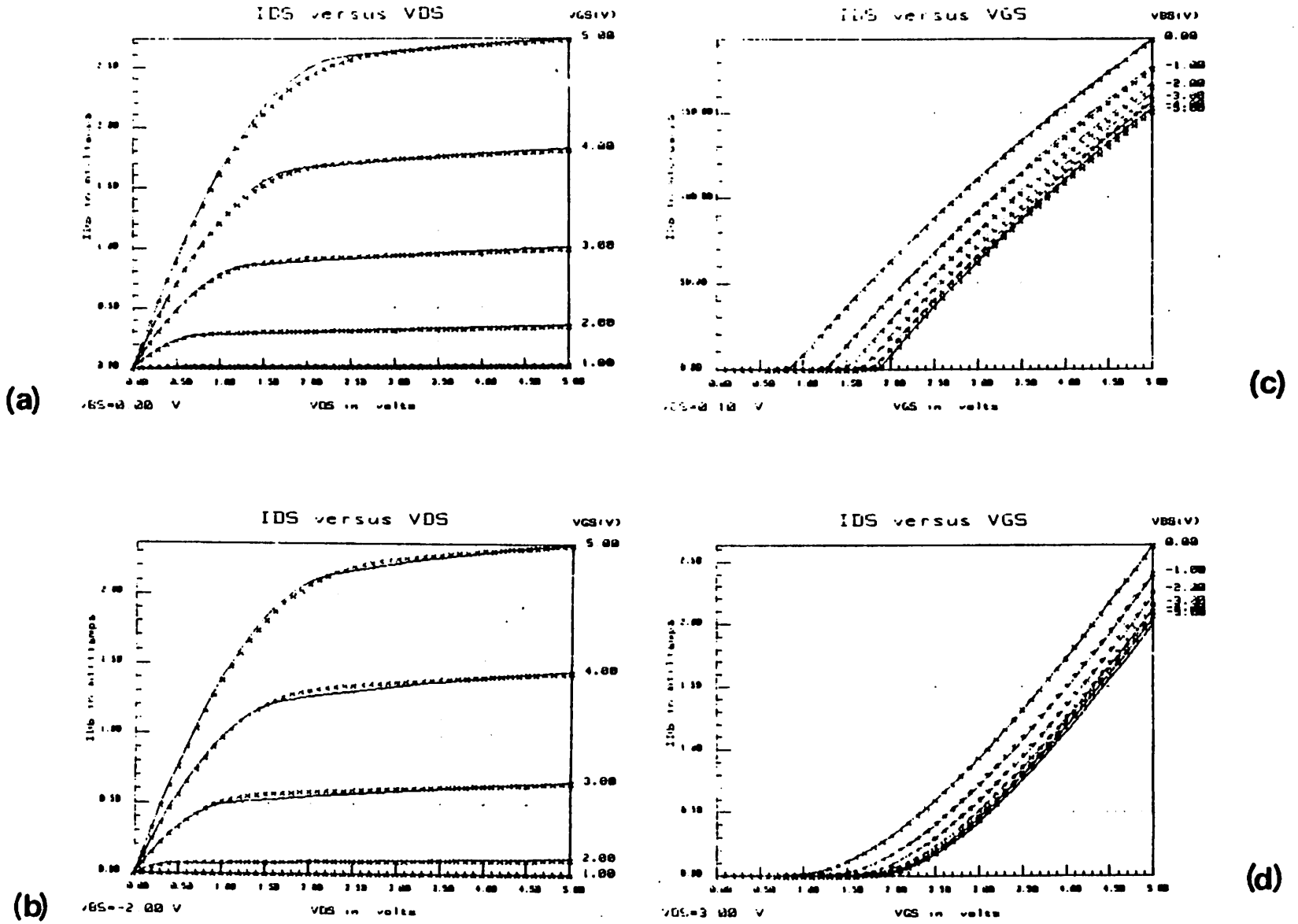

Fig.8 Output characteristics of a W_M/L_M=20μm/3.5μm masked size nMOS transistor. T_{ox}=300A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=-2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=0.1v, (d) I_{DS} verrsus V_{GS} at V_{DS}=3.0v.

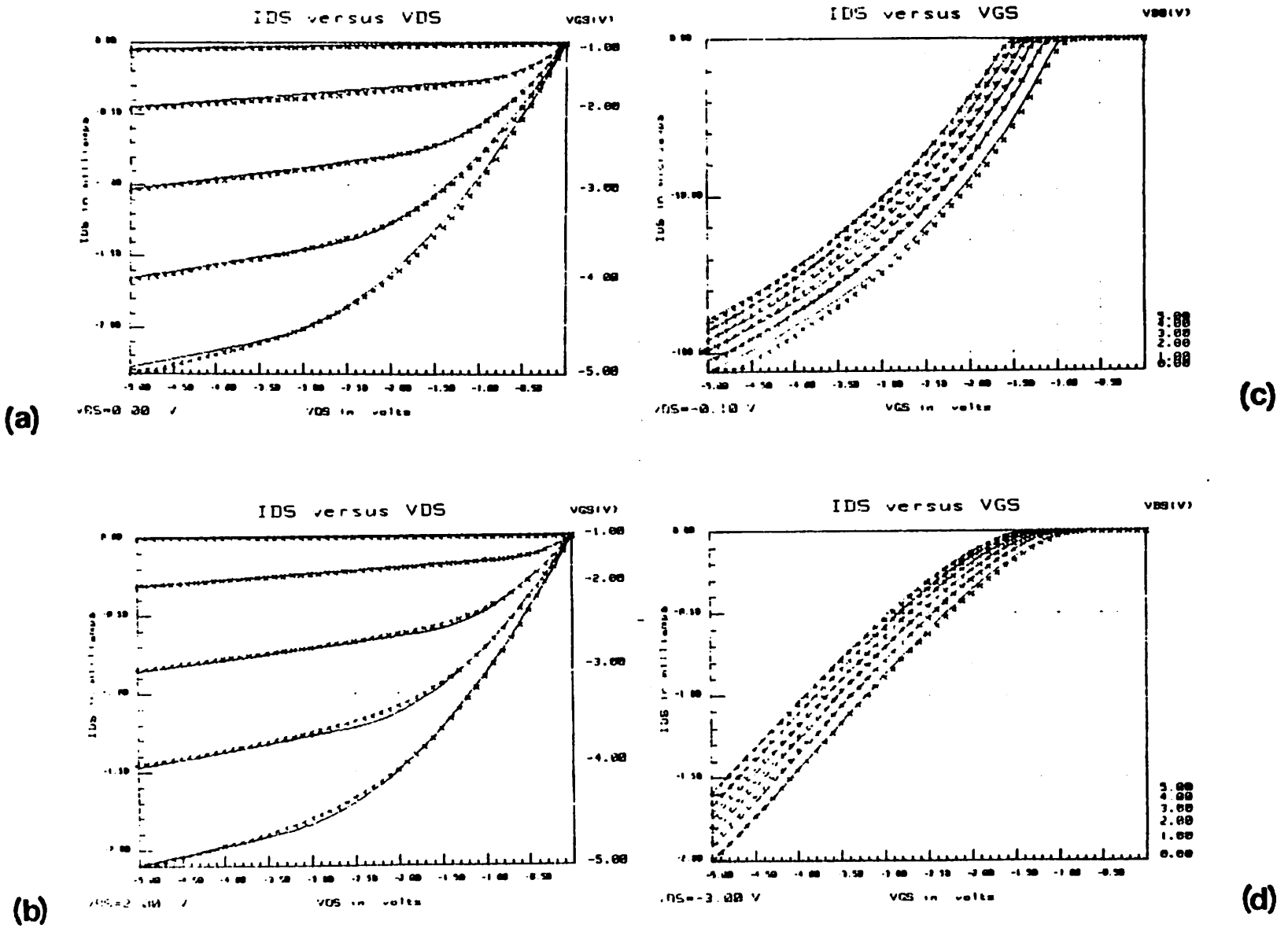

Fig.9 Output characteristics of a 20μm/2μm masked size pMOS transistor. T_{ox}=300A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=-0.1v, (d) I_{DS} verrsus V_{GS} at V_{DS}=-3.0v.

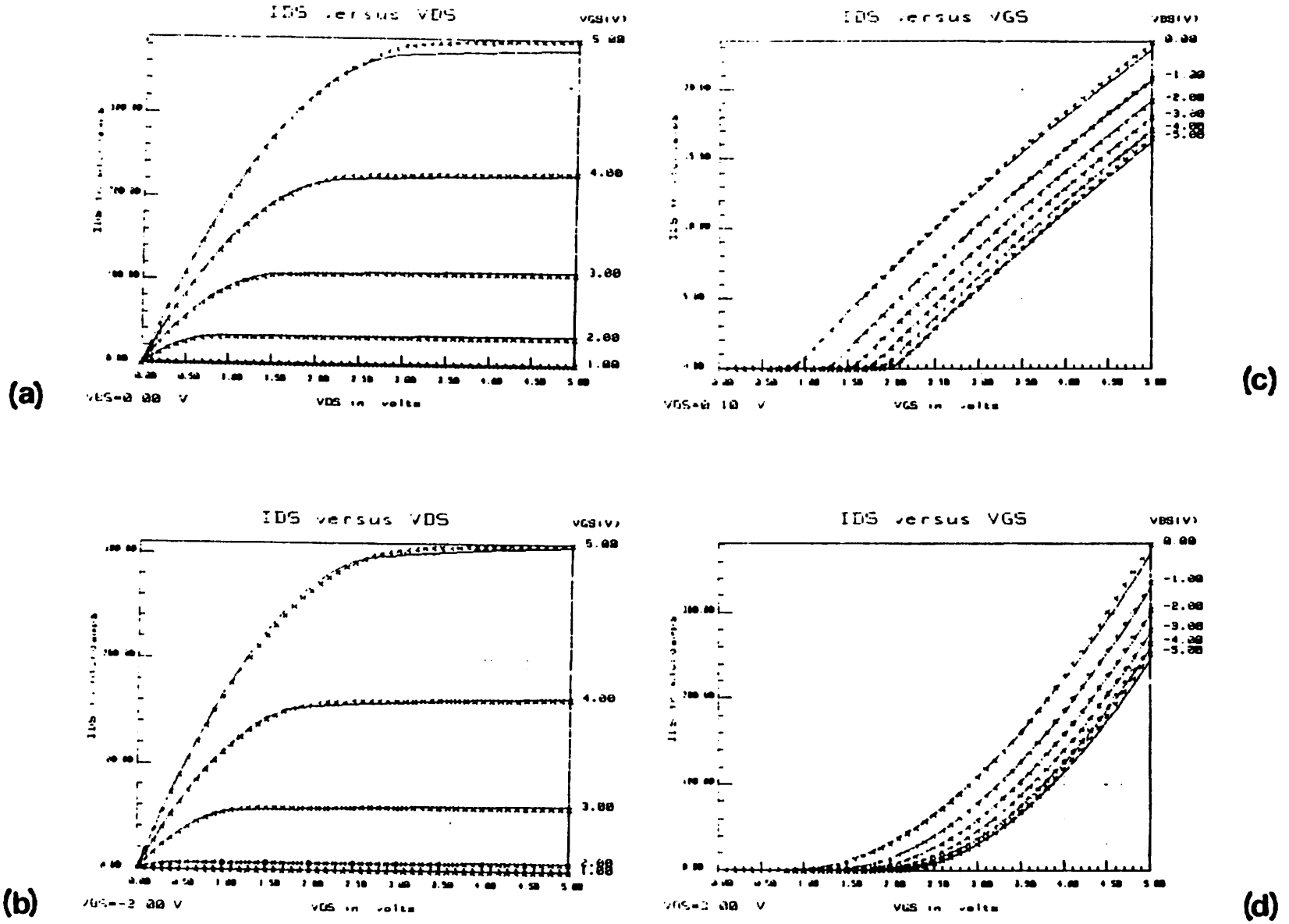

Fig.10 Output characteristics of a 20μm/20μm masked size nMOS transistor. T_{ox}=300A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=-2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=0.1v, (d) I_{DS} verrsus V_{GS} at V_{DS}=3.0v.

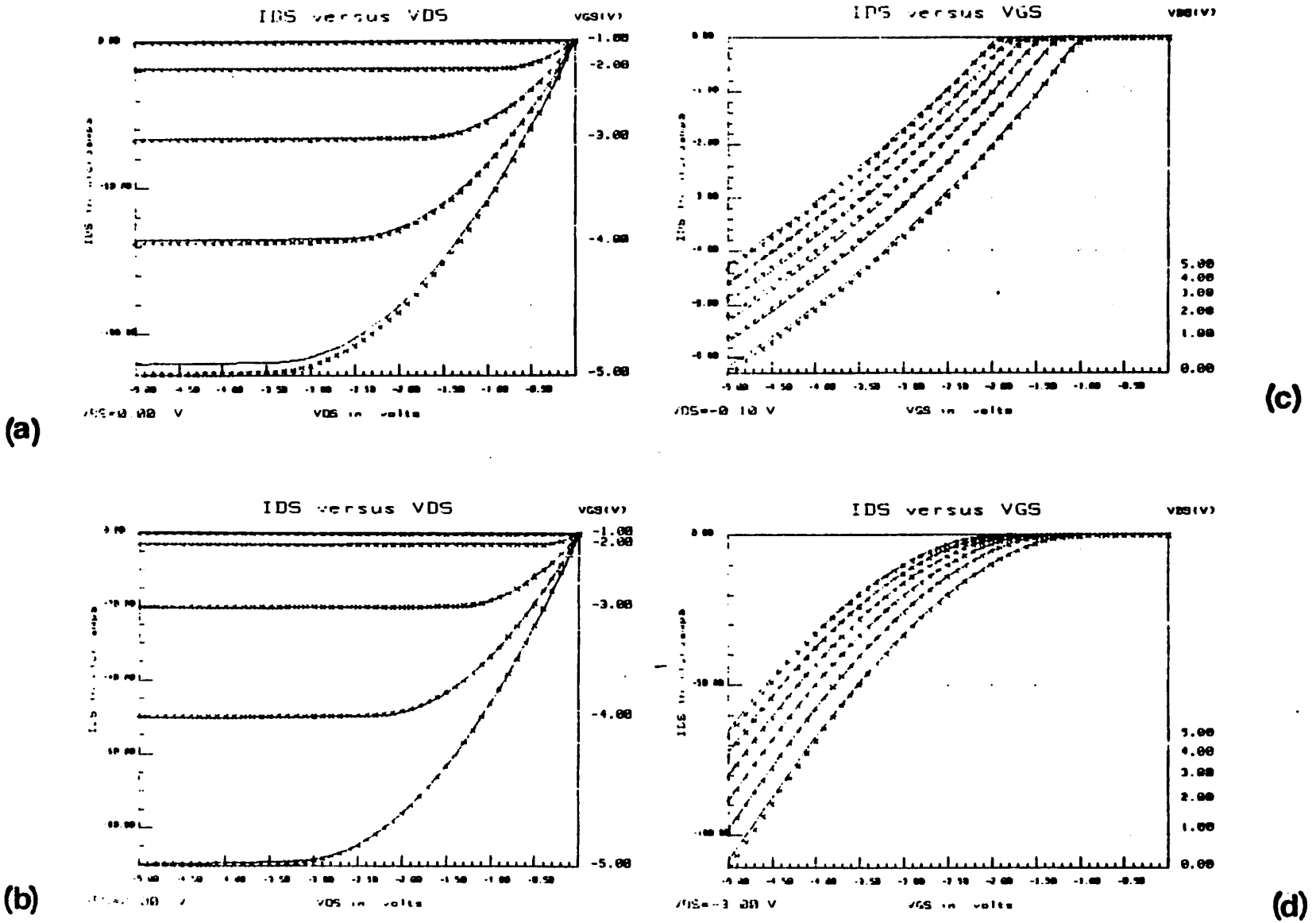

Fig.11 Output characteristics of a 20μm/20μm masked size pMOS transistor. T_{ox}=300A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=-0.1v, (d) I_{DS} verrsus V_{GS} at V_{DS}=-3.0v.

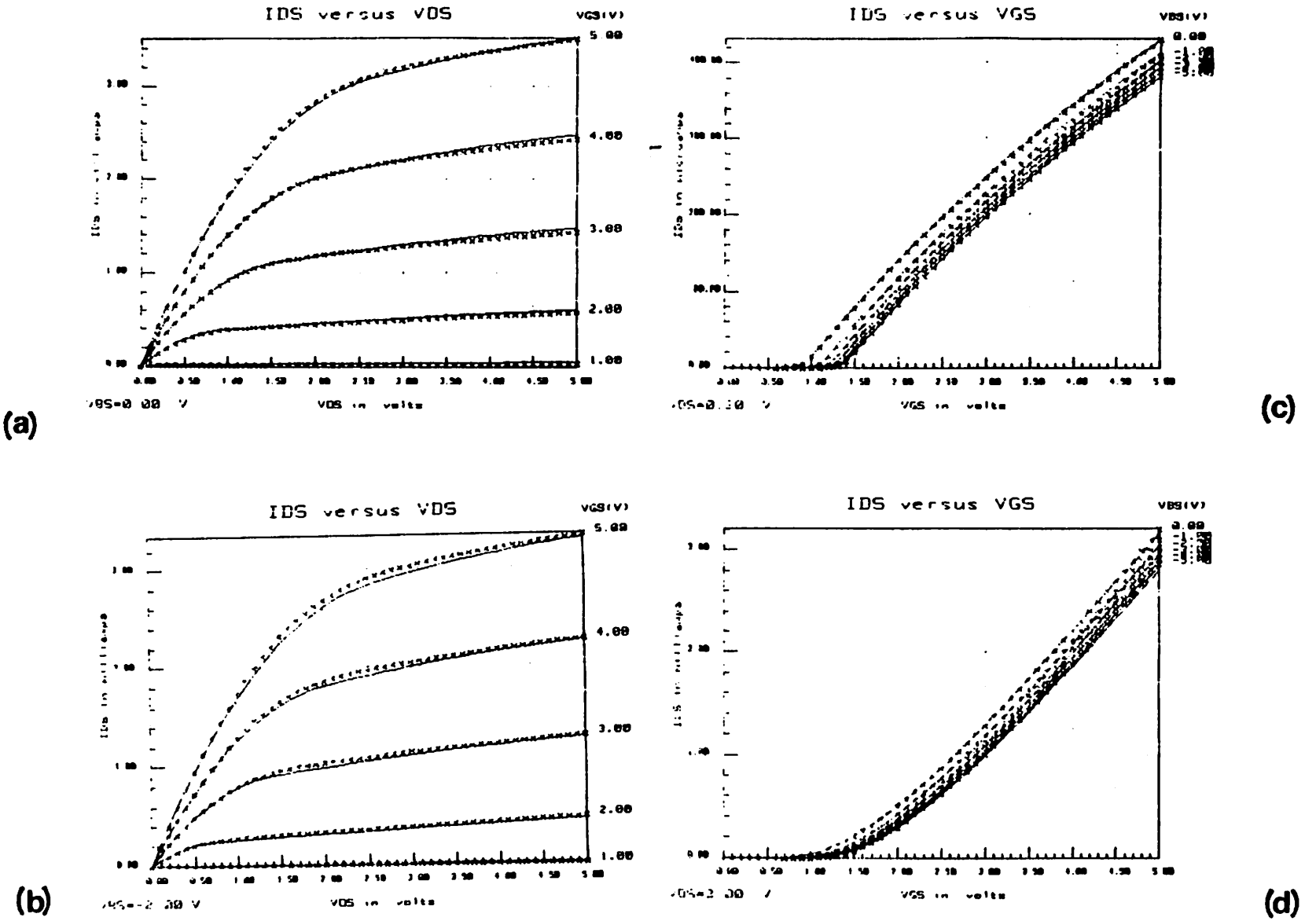

Fig. 12 Output characteristics of a 50μm/3.5μm masked size nMOS transistor. T_{ox}=700A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=-2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=0.2v, (d) I_{DS} verrsus V_{GS} at V_{DS}=3.0v.

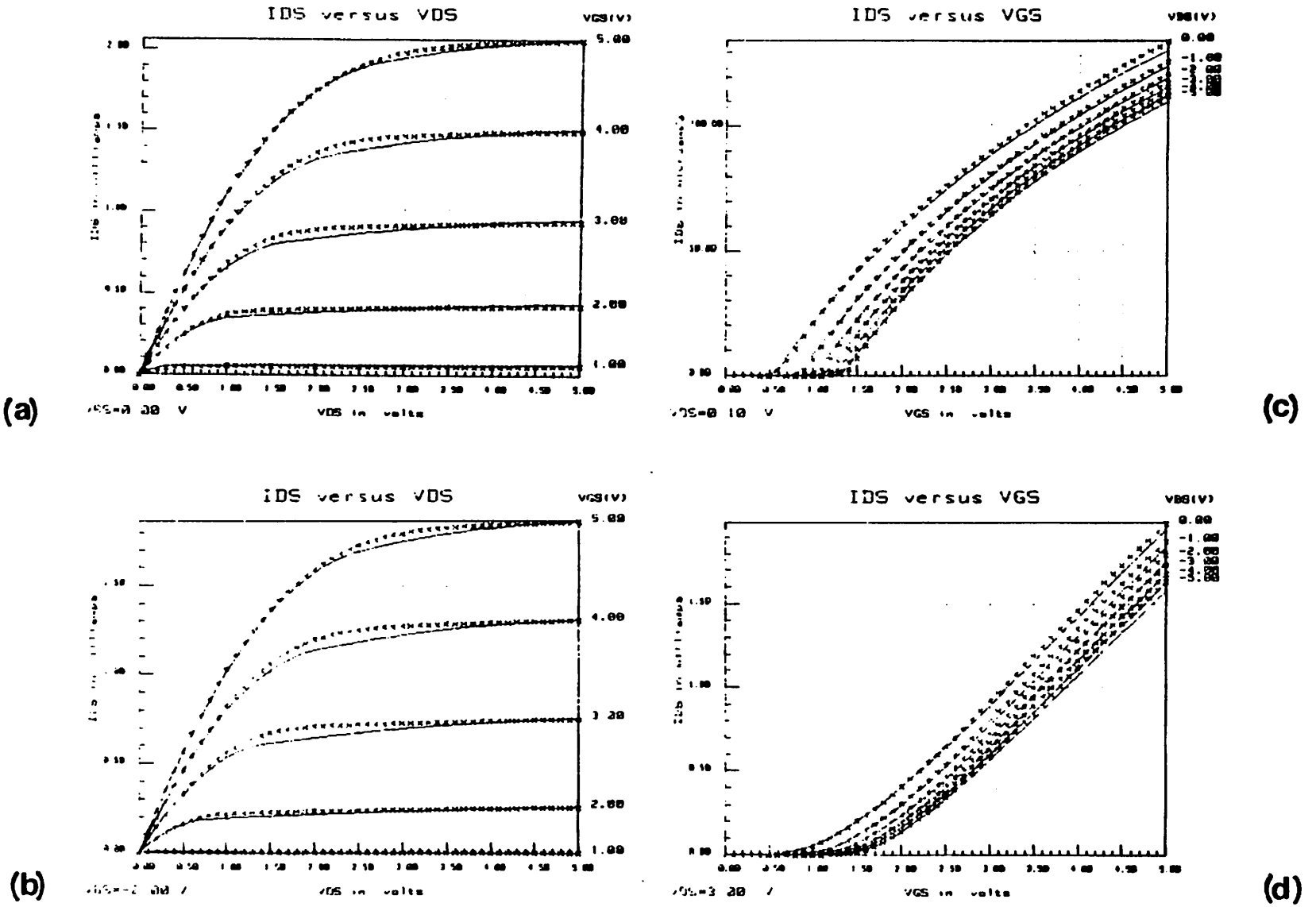

Fig.13 Output characteristics of a 10μm/1.5μm masked size nMOS transistor with LDD structure. T_{ox}=200A. (a) I_{DS} versus V_{DS} at V_{BS}=0.0v, (b) I_{DS} versus V_{DS} at V_{BS}=-2.0volt, (c) I_{DS} versus V_{GS} at V_{DS}=0.2v, (d) I_{DS} verrsus V_{GS} at V_{DS}=3.0v.

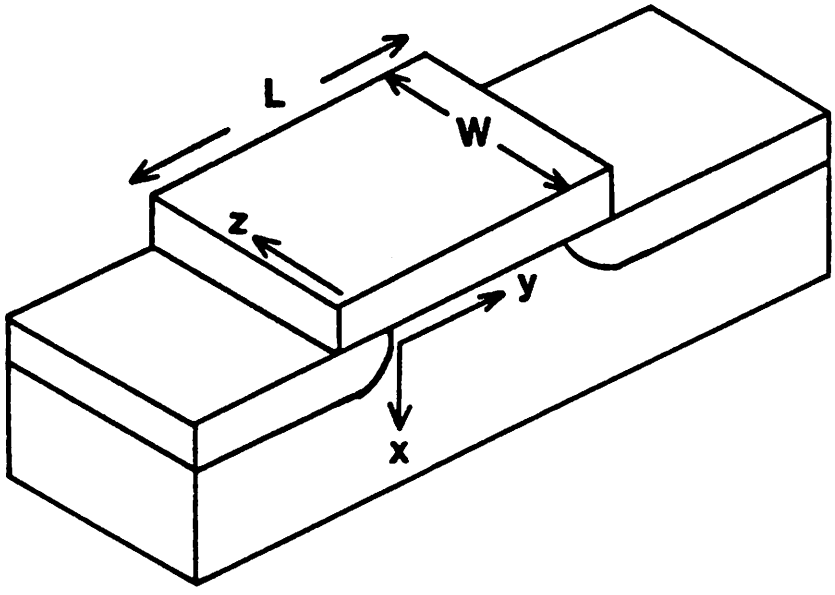

Fig.14 An idealized n-channel MOSFET.

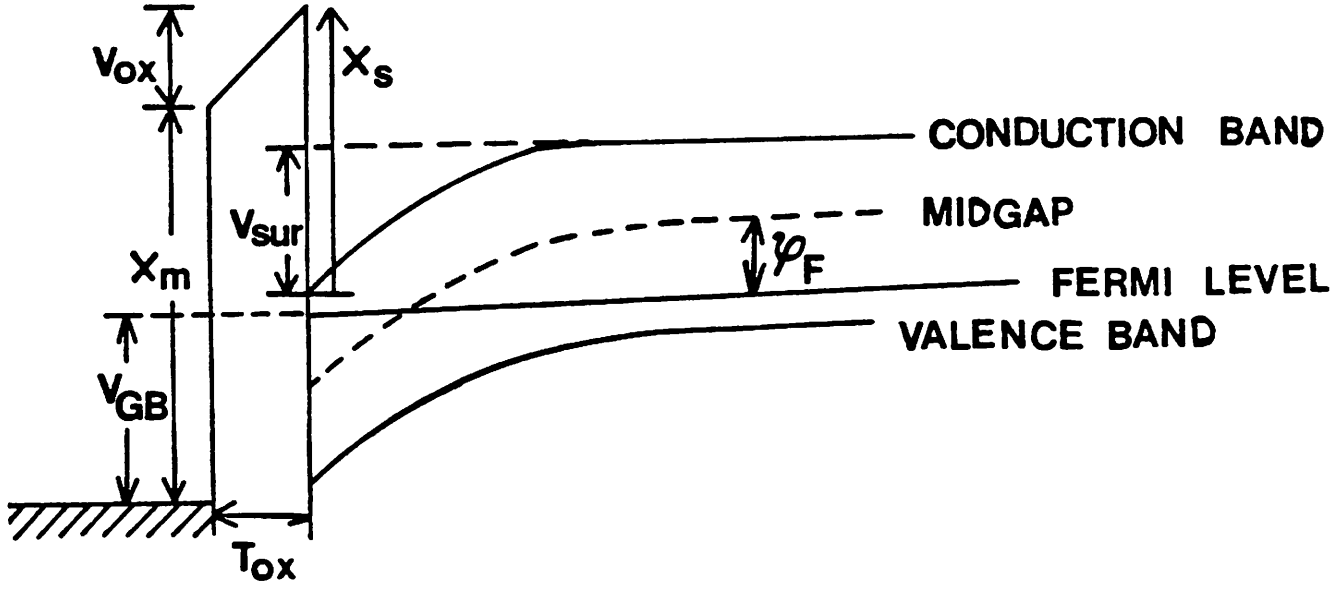

Fig.15 An energy band diagram.

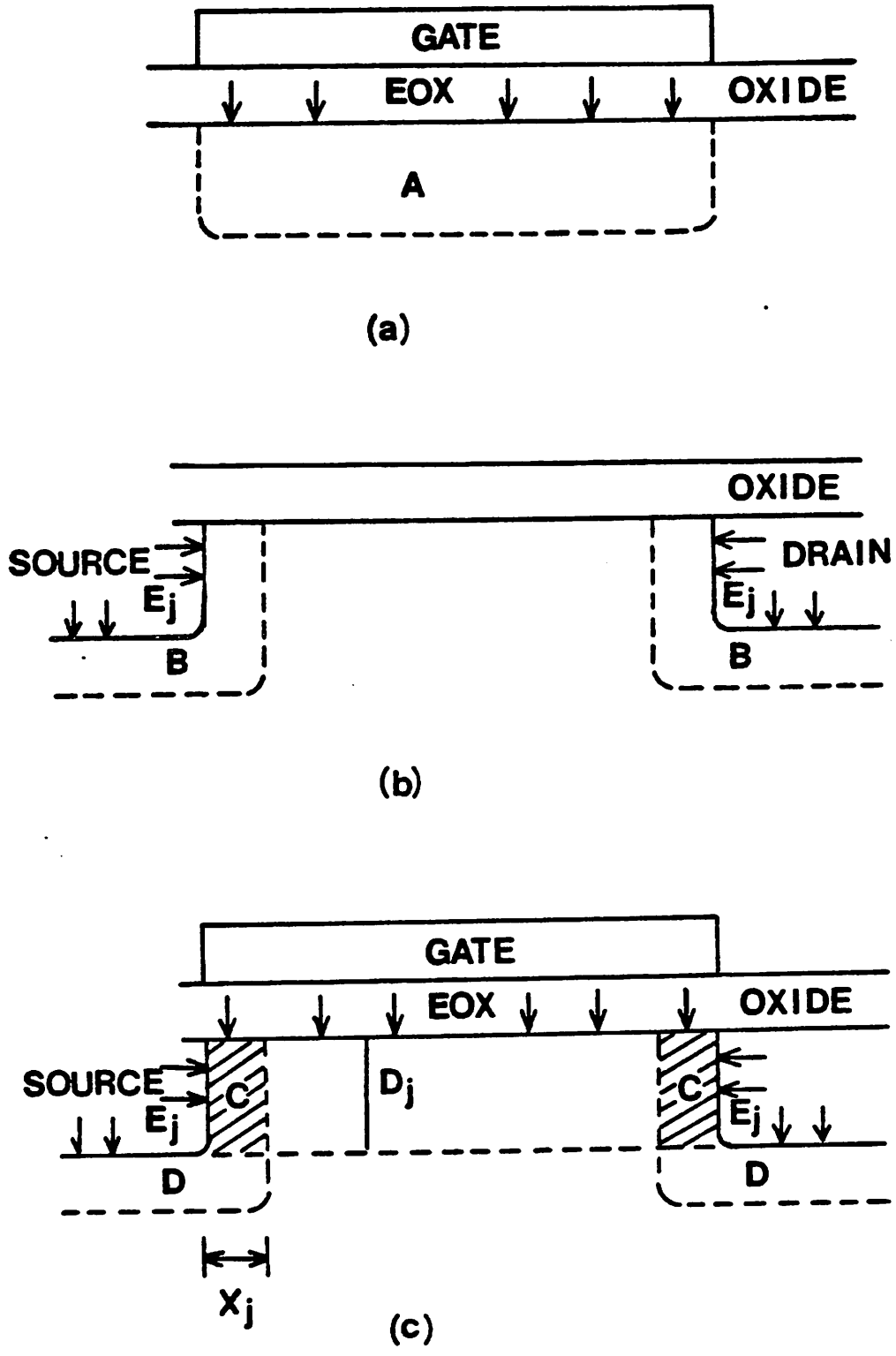

Fig.16 Diagram illustrating the effect of drain and source junction fields.

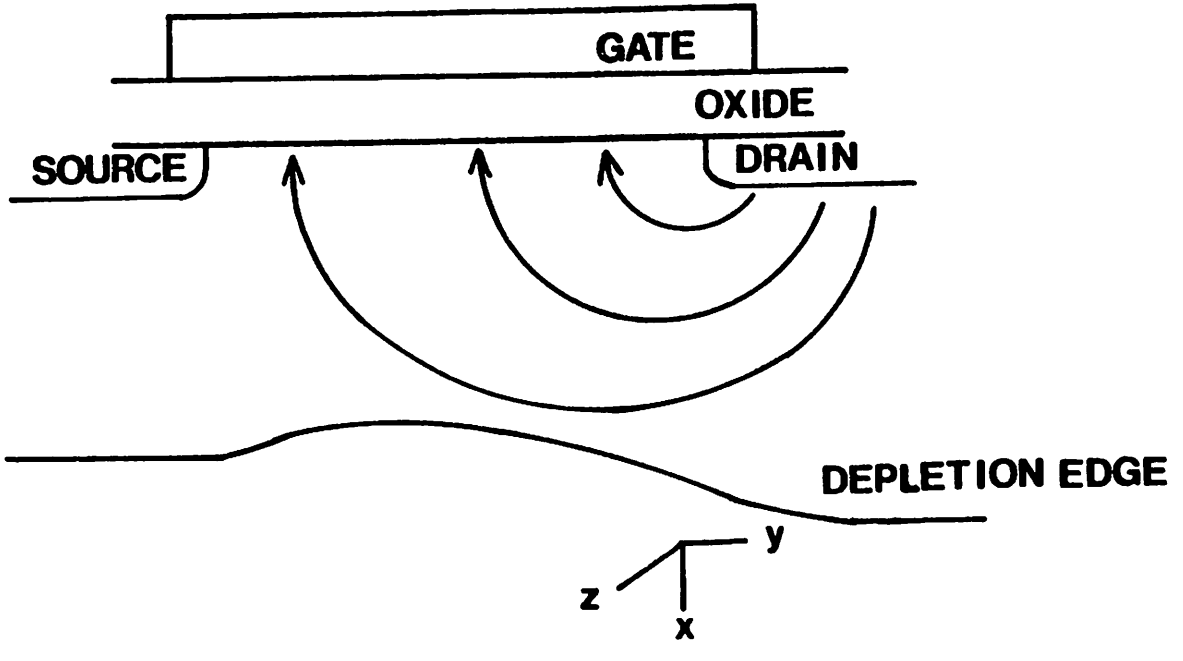

Fig.17 Diagram illustrating the drain modulation effect.

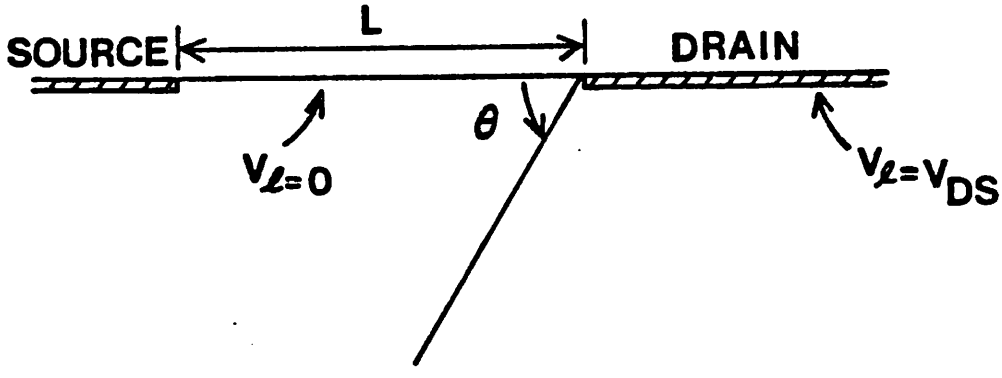

Fig.18 Diagram illustrating the simplified boundary condition for the Laplace equation.

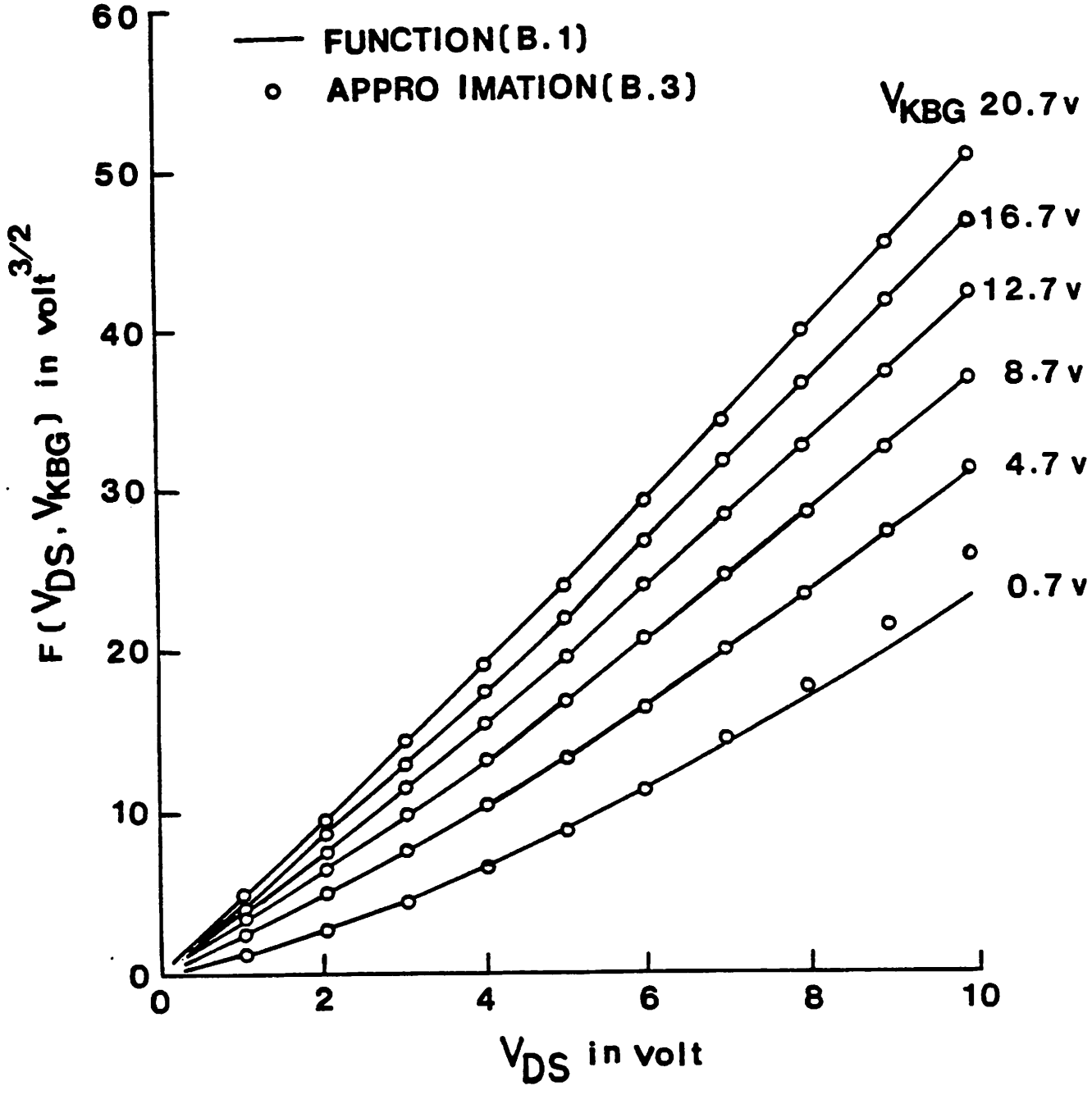

Fig.19 Approximating the function $F(V_{DS}, \varphi_S - V_{BS})$.

A Compact IGFET Charge Model

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ABSTRACT

A new IGFET charge model, consistent with the recently published Compact Short-Channel IGFET Model [1][2], is presented. It is simple, accurate, and suitable for circuit simulation applications. Charge conservation is guaranteed by using charge as the state variable. The partitioning of channel charge into drain and source components is given significant attention. This partitioning changes smoothly from 40/60 in the saturation region asymptotically to 50/50 in the triode region. The terminal charges are well behaved over all regions of operation. This charge model and its DC characteristic counterpart, derived from the same considerations of MOS device physics, form a unified model previously unavailable.

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I. Introduction

Much work has been devoted to the subject of modeling the DC characteristic of the MOS transistor. These models all show agreement between simulated and experimental results to within a few percent. However, insufficient effort has been devoted to obtaining satisfactory charge models suitable for transient and AC small signal circuit simulations. The issue of modeling MOS transistor charge storage [3],[4] has attracted the attention of IC designers since Ward and Dutton [5] pointed out that charge non-conservation could occur if the MOSFET capacitance model is not correctly formulated. This effect may cause serious errors in the simulations of switched-capacitor circuits, certain dynamic circuits, and other circuits sensitive to capacitive components of the MOSFET currents. Although there have been various solutions proposed in the literature, there is unanimous agreement that the solution to the charge non-conservation problem is to employ a charge-oriented capacitive coefficient model, i.e. a model based on the charge functions:

$$Q_G(V_G, V_S, V_D, V_B)$$

$$Q_B(V_G, V_S, V_D, V_B)$$

$$Q_S(V_G, V_S, V_D, V_B)$$

$$Q_D(V_G, V_S, V_D, V_B)$$

Q_G, Q_B, Q_S, Q_D are the charges associated with the gate, bulk (body), source, and drain terminals, and the capacitive current component of I_G, I_B, I_S, I_D, is the derivative of Q_G, Q_B, Q_S, Q_D with respect to time. The quasi-static approximation

has been assumed in formulating the above expressions.

Both transport current components and capacitive current components exist due to charge storage in the MOS transistor. Therefore the dc I-V model and charge model should be consistently derived. Some MOS models used in circuit simulators have a DC model part and a charge model part derived from different aspects. This has been confusing circuit designers for many years. In this paper, we present a charge model which shares the same information obtained from the DC characteristic measurements. The DC and charge models, derived from the same considerations of MOS device physics, form a unified model previously unavailable. The partitioning of channel charge into drain and source components is given significant attention. Body bias effects are properly incorporated and the physics behind the charge storage in the device are modeled and described.

II. DC Characteristic Counterpart of the Charge Model

The DC characteristic model in this paper is an evolution of the Bell Labs CSIM (Compact Short-Channel IGFET Model). A detailed description of that model can be found in the appendix of [1]. The dc current expressions are briefly summarized, with some notation changes, in the following [1]:

1) Cut-off Region [$V_{GS} < V_{th}$]:

$$I_{DS} = 0 \tag{1}$$

2) Triode Region [$V_{GS} > V_{th}$ and $0 < V_{DS} < V_{DSAT}$]:

$$I_{DS} = \beta[(V_{GS} - V_{th})V_{DS} - \frac{\alpha_x}{2}V_{DS}^2] \tag{2}$$

3) Saturation Region [$V_{GS} > V_{th}$ and $V_{DS} > V_{DSAT}$]:

$$I_{DS} = \frac{\beta}{2\alpha_x}(V_{GS} - V_{th})^2 \tag{3}$$

The threshold voltage "V_{th}" is defined by the equation

$$V_{th} = V_{FB} + \varphi_S + K_1\sqrt{\varphi_S - V_{BS}} - K_2(\varphi_S - V_{BS}) - \eta V_{DS} \tag{4}$$

The last two terms in the right hand side of (4) result from the short channel drain-induced barrier lowering effect.

The saturation voltage "V_{DSAT}" is defined by

$$V_{DSAT} = \frac{V_{GS} - V_{th}}{\alpha_x} \tag{5}$$

The effective conductance coefficient "β" is defined by the equation

$$\beta = \frac{\beta_0}{1 + U_0(V_{GS} - V_{th})} \tag{6}$$

The conductance-degradation coefficient "α_x" is defined by the equation

$$\alpha_x = a[1 + U_1(V_{GS} - V_{th})] \tag{7}$$

where

$$a = 1 + \frac{g K_1}{2\sqrt{\varphi_S - V_{BS}}} \tag{8}$$

$$g = 1 - \frac{1}{1.744 + 0.8364(\varphi_S - V_{BS})} \tag{9}$$

The body-effect coefficient "a" makes CSIM a close numerical approximation of the standard textbook model over a reasonable range of V_{DS} and V_{BS}.

III. The Charge Model

The expressions for the charge densities are similar in form to those of [6]. However, due to different ways of treating the physics behind the transistor operation, the functional dependence of α_x and channel charge partitioning are quite different. The charge equations in different regions are given below.

1) Triode Region:

$$q_g(y) = C_o(V_{GS} - V_{FB} - \varphi_S - V_y) \tag{10}$$

$$q_c(y) = -C_o(V_{GS} - V_{th} - \alpha_x V_y) \tag{11}$$

$$q_b(y) = -C_o[V_{th} - V_{FB} - \varphi_S - (1 - \alpha_x)V_y] \tag{12}$$

where V_y is the electron quasi-Fermi potential with respect to the source. Observe that

$$q_g + q_c + q_b = 0 \tag{13}$$

This follows the constraint of charge neutrality in the one dimensional MOS

capacitor structure.

Total stored charge contained in each of the gate, bulk, and channel regions is easily obtained by integrating the distributed charge densities, q_g, q_b, and q_c over the area of the active gate region (from y=0 to y=L and z=0 to z=W).

$$Q_G = W\int_0^L q_g(y)\,dy \tag{14}$$

$$Q_C = W\int_0^L q_c(y)\,dy \tag{15}$$

$$Q_B = W\int_0^L q_b(y)\,dy \tag{16}$$

Combining (10)-(12) into (14)-(16) and replacing the differential channel length "dy" with the corresponding differential potential drop "dV", we obtain the following expressions for the total gate, channel, and bulk charges in static equilibrium.

$$Q_G = W\int_0^L C_o(V_{GS}-V_{FB}-\varphi_S-V_y)\,dy$$

$$= WLC_o\left[V_{GS}-V_{FB}-\varphi_S-\frac{V_{DS}}{2}+\frac{V_{DS}}{12}\,\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right] \tag{17}$$

$$Q_C = -W\int_0^L C_o(V_{GS}-V_{th}-\alpha_x V_y)\,dy$$

$$= -WLC_o\left[V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS}+\frac{\alpha_x V_{DS}}{12}\cdot\,\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right] \tag{18}$$

$$Q_B = -W\int_0^L C_o[V_{th}-V_{FB}-\varphi_S-(1-\alpha_x)V_y]\,dy$$

$$= WLC_o\left[-V_{th}+V_{FB}+\varphi_S+\frac{(1-\alpha_x)}{2}V_{DS}-\frac{(1-\alpha_x)V_{DS}}{12}\cdot\,\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right] \tag{19}$$

It is clear that the three total stored charge components of the MOSFET, (17)-(19), also exhibit charge neutrality.

$$Q_G + Q_C + Q_B = 0 \tag{20}$$

It is necessary to partition channel charge into charge associated with the drain terminal "Q_D" and charge associated with the source terminal "Q_S". The question of charge partitioning has so far been dealt with by gross approximate partitioning or use of an arbitrary factor. Ward and Dutton [5] already noted this difficulty. They described many possibilities and chose the estimate of 50/50 partition between Q_D and Q_S, although their device simulation had indicated a 40/60 partition in the saturation region. Yang, et al [6] proposed to make the partition so as to satisfy the condition that Q_D and Q_S and their derivatives be continuous throughout the triode and saturation regions. They failed to note, however, that there are infinite ways to partition the charge to satisfy that requirement. Furthermore, they adopted the incorrect premise that Q_D is zero at the saturation region (0/100 partition).

A sound theoretical model for channel charge partitioning is of particular importance because if the partitioning is performed through the use of a parameter, then that parameter (actually a function of the bias voltage) is unusually difficult to extract from device measurements. In this work, the issue of channel charge partitioning is appropriately handled. It changes smoothly from 40/60 in the saturation region asymptotically to 50/50 in the triode region.

A physically meaningful channel charge partitioning method has been presented by Oh, et al [7] and is used here.

$$Q_S = -W\int_0^L \left(1 - \frac{y}{L}\right) q_c(y)\, dy \tag{21}$$

$$Q_D = -W\int_0^L \frac{y}{L} q_c(y)\, dy = Q_C - Q_S \tag{22}$$

Carrying out the integrations in (21) and (22), with q_c replaced by (11), we obtain the total charge associated with the source terminal and drain terminal,

$$Q_S = -WLC_o\left[\frac{V_{GS}-V_{th}}{2} + \frac{\alpha_x V_{DS}}{12}\cdot\frac{\alpha_x V_{DS}}{\left(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS}\right)}\right.$$

$$\left. - \frac{\alpha_x V_{DS}}{\left(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS}\right)^2}\left[\frac{(V_{GS}-V_{th})^2}{6} - \frac{\alpha_x V_{DS}(V_{GS}-V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40}\right]\right]$$

(23)

$$Q_D = -WLC_o\left[\frac{V_{GS}-V_{th}}{2}-\frac{\alpha_x V_{DS}}{2}+\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})^2}\left[\frac{(V_{GS}-V_{th})^2}{6}-\frac{\alpha_x V_{DS}(V_{GS}-V_{th})}{8}+\frac{\alpha_x^2 V_{DS}^2}{40}\right]\right]$$

(24)

2)Saturation Region:

$$Q_G = WLC_o(V_{GS}-V_{FB}-\varphi_S-\frac{V_{GS}-V_{th}}{3\alpha_x}) \quad (25)$$

$$Q_B = WLC_o(V_{FB}+\varphi_S-V_{th}+\frac{(1-\alpha_x)(V_{GS}-V_{th})}{3\alpha_x}) \quad (26)$$

$$Q_C = -\frac{2}{3}WLC_o(V_{GS}-V_{th}) \quad (27)$$

$$Q_S = -\frac{2}{5}WLC_o(V_{GS}-V_{th}) \quad (28)$$

$$Q_D = -\frac{4}{15}WLC_o(V_{GS}-V_{th}) \quad (29)$$

3) Subthreshold Region [$V_{FB}+V_{BS} \le V_{GS} \le V_{th}$]:

Let

$$K_{eff}\sqrt{\varphi_S-V_{BS}} = K_1\sqrt{\varphi_S-V_{BS}} - K_2(\varphi_S-V_{BS}) - \eta V_{DS} \quad (30)$$

then

$$Q_G = WLC_o\frac{K_{eff}^2}{2}\left[-1+\sqrt{1+\frac{4(V_{GS}-V_{FB}-V_{BS})}{K_{eff}^2}}\right] \quad (31)$$

$$Q_B = -Q_G \quad (32)$$

$$Q_C = 0 \quad (33)$$

4) Accumulation Region:

$$Q_G = W L C_o (V_{GS} - V_{FB} - V_{BS}) \tag{34}$$

$$Q_B = -Q_G \tag{35}$$

$$Q_C = 0 \tag{36}$$

IV. Comparison with Experiments and Conclusion

Fig. 1 shows the plots of the four normalized terminal charges. The dependence of normalized transcapacitive coefficients on the gate-source voltage and drain-source voltage are given in Fig. 2 and 3, respectively. Note that the charges and transcapacitive coefficients are all continuous at the boundary of the triode and saturation regions. Fig.4 compares theoretical calculations with the measurements given in [8] for a long channel device. Good agreement is found.

Of great significance in obtaining the accurate model for the charges and capacitances is the utilization of the Poon CSIM model [1], as extended [2], to model the DC characteristic and associated charge storage. Poon makes a close numerical approximation to the body effect. This simplies the DC characteristic model to a form similar to the Shichman-Hodges first order model. The charge and capacitance model also benifits from this approximation and has very simple expressions, as derived in this paper. This new set of IGFET model equations, with the DC characteristic part derived in [1],[2] and the charge-capacitance part derived here, is simple, accurate, and hence very suitable for circuit simulation applications.

Acknowledgment

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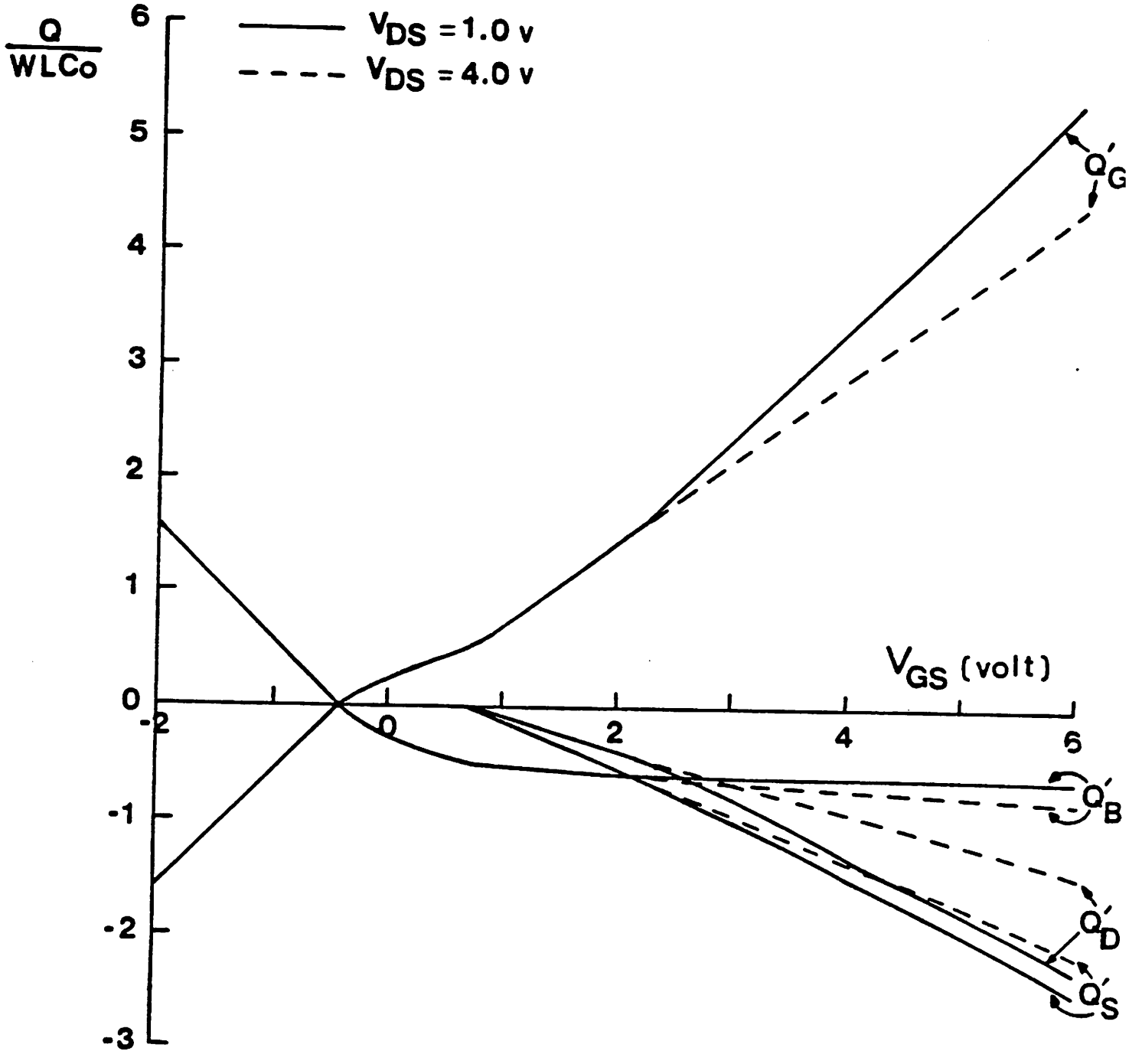
Figure Captions

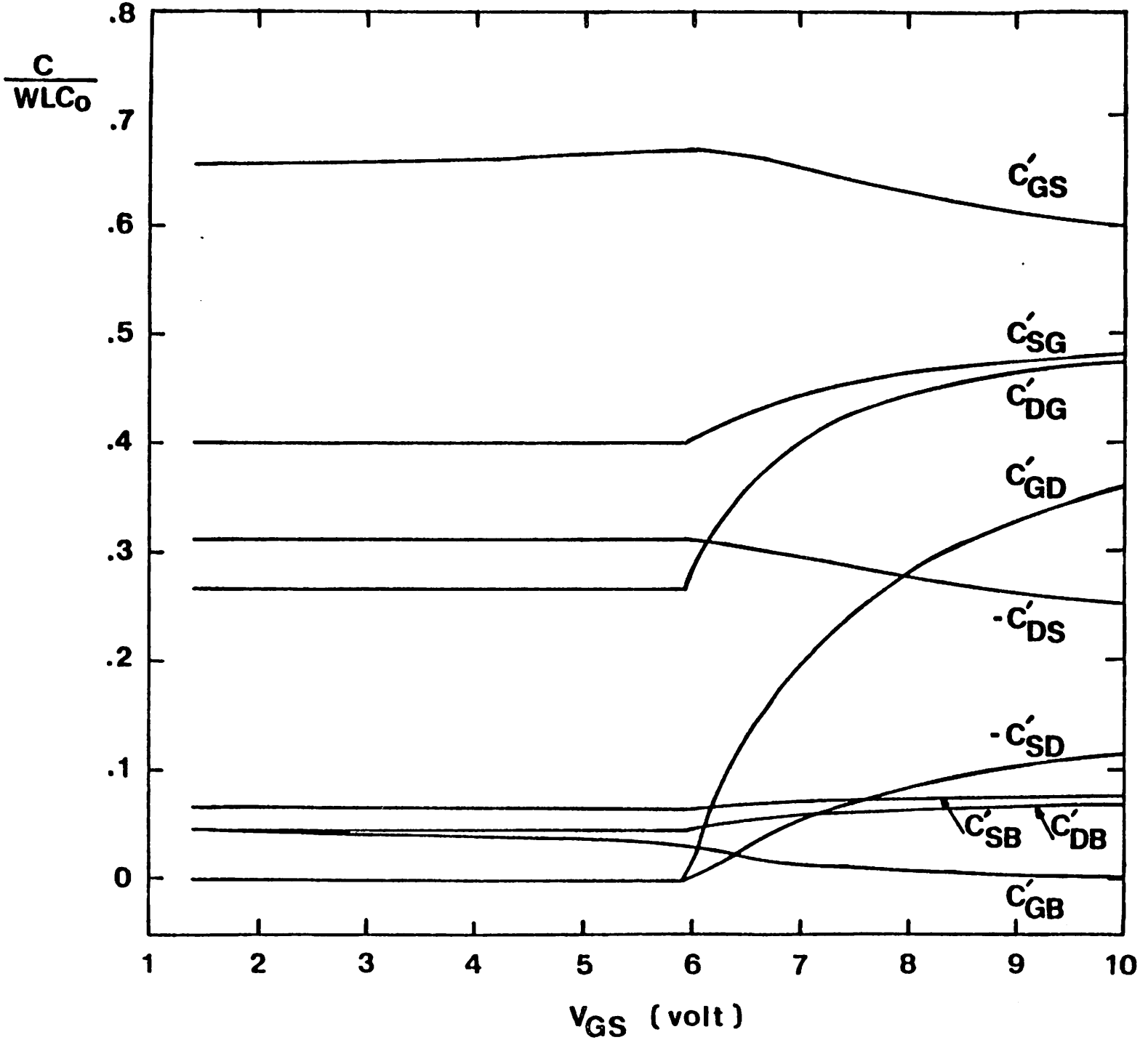
Fig.1 Charges associated with gate, bulk, source, and drain terminals. The parameters are V_{BS}=0.0v, V_{DS}=1.0v, a=1.224, V_{th}=0.70v, K_1=0.633, φ_S=0.625.

Fig.2 Normalized transcapacitive coefficients against gate-source voltage. The parameters are V_{BS}=-3.0v, V_{DS}=4.0v, a=1.131, V_{th}(V_{BS}=-3.0v)=1.40v, K_1=0.633, φ_S=0.625.

Fig.3 Normalized transcapacitive coefficients against drain-source voltage. The parameters are V_{BS}=-3.0v, V_{GS}=6.0v, a=1.131, V_{th}(V_{BS}=-3.0v)=1.40v, K_1=0.633, φ_S=0.625.

Fig.4 Comparison of several measured [8] and calculated transcapacitive coefficients against gate-source voltage. The parameters are V_{BS}=0.0v, V_{DS}=4.0v.


Q/WLCo
V_{DS} = 1.0 v
V_{DS} = 4.0 v
6
5
4
3
2
1
0
-1
-2
-3
-2
0
2
4
6
V_{GS} (volt)
Q'_G
Q'_B
Q'_D
Q'_S


C / WLC_O
.8
.7
.6
.5
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.3
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0
C'GS
C'SG
C'DG
C'GD
-C'DS
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C'GB
1
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3
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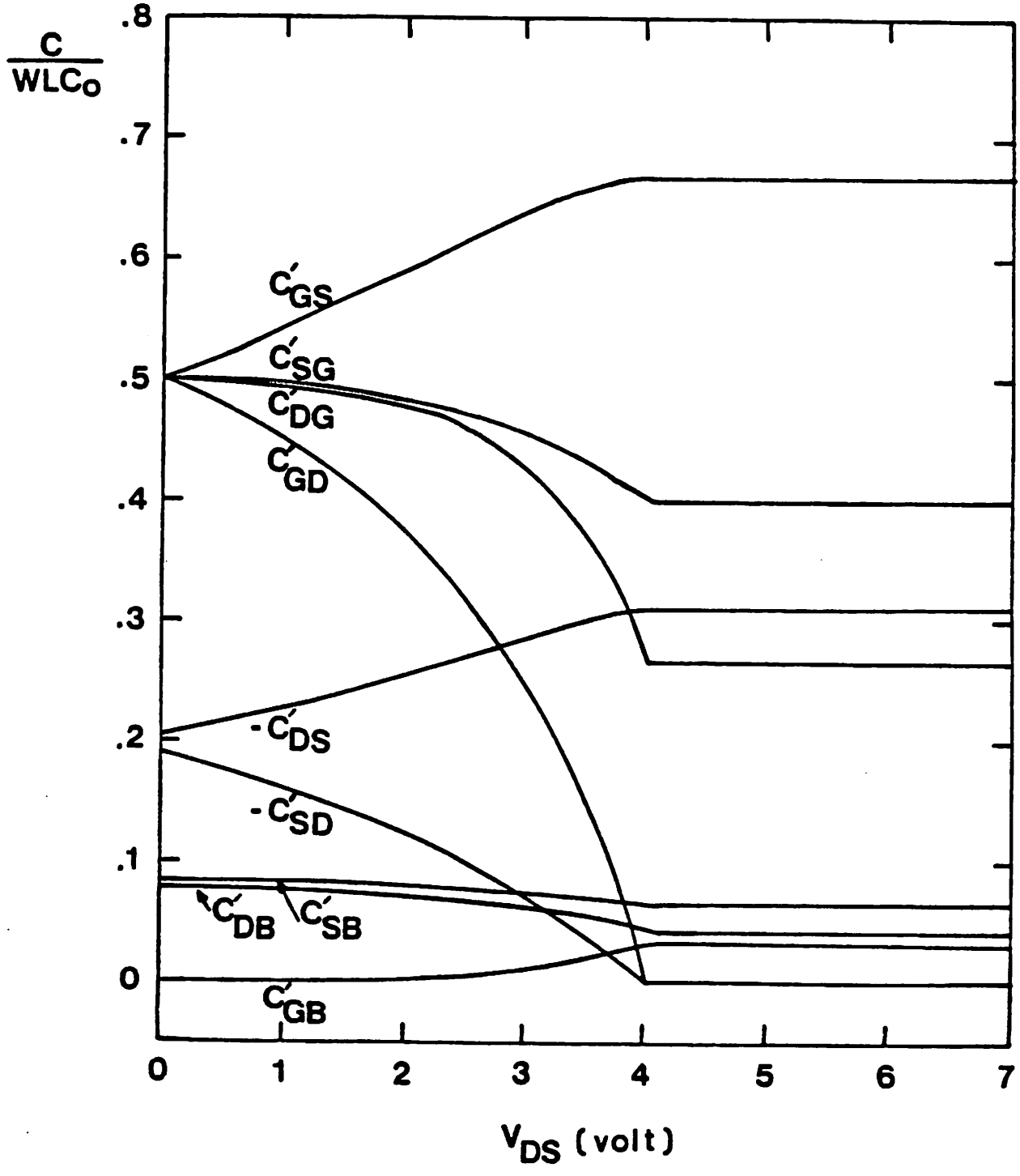
6
7
8
9
10
VGS (volt)


C / WLCo
.8
.7
.6
.5
.4
.3
.2
.1
0
C'GS
C'SG
C'DG
C'GD
-C'DS
-C'SD
C'DB
C'SB
C'GB
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1
2
3
4
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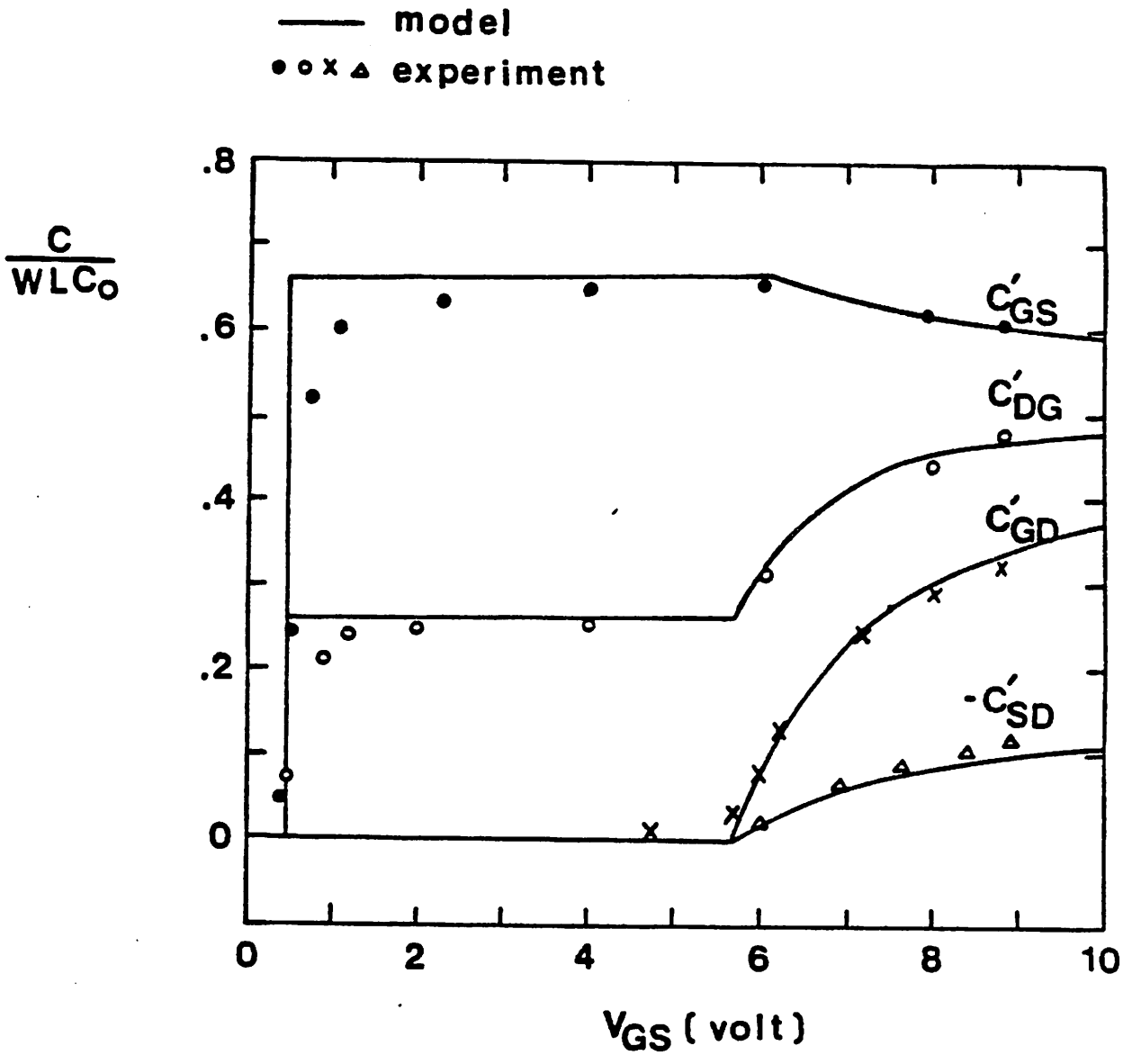
6
7
VDS (volt)


model
experiment
C / WLC_o
.8
.6
.4
.2
0
0
2
4
6
8
10
V_GS (volt)
C'_GS
C'_DG
C'_GD
-C'_SD