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SELF-CALIBRATION TECHNIQUES FOR SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTERS

by

Hae-Seung Lee

Memorandum No. UCB/ERL M84/33

10 April 1984

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Self-Calibration Techniques
for Successive Approximation Analog-to-Digital Converters

By

Hae-Seung Lee

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DISSERTATION

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Approved: David A. Hodges 4/10/84
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SELF-CALIBRATION TECHNIQUES FOR SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTERS

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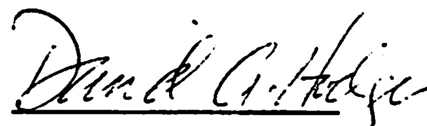

Chairman of Committee

Abstract

This thesis reports on an investigation of successive approximation analog-to-digital converters approaching the theoretical limit of resolution and linearity, implemented using metal-oxide-semiconductor large scale integration (MOSLSI).

A simple digital algorithm has been developed to correct the linearity error of monolithic CMOS analog-to-digital converters. A high degree of monotonicity and linearity is obtained without stringent component matching.

An experimental integrated circuit has been fabricated using 5-micron rule standard CMOS process. After the calibration typically performed each time the converter is powered up, the converter showed no larger than ± 0.65 lsb differential non-linearity and 0.8 lsb integral non-linearity at 15-bit level. The 15-bit conversion was carried out in 80 μs.

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DEDICATION

This manuscript is dedicated to my parents, Ki-Yong and Sook-Kyung Lee, for their supprot and encouragement throughout the course of my graduate study.

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CHAPTER 1

INTRODUCTION

Due to the rapid advance in the integrated circuit technology in recent years, very complex digital functions can now be implemented on a single monolithic integrated circuit. Digital signal processing circuits, which used to be impractical due to their complexity, have become commonplace.

Digital processing of analog signals has many advantages over analog signal processing. For example, digital processing is insensitive to many electrical parameters and also to fabrication process to which analog signal processing is sensitive. In addition, with the help of computer aided design tools, digital integrated circuit design has become a relatively simple, routine job.

Digital signal processing often requires a high performance analog-to-digital (A/D) and digital-to-analog (D/A) converters. In the past, implementation of high performance analog-to-digital converters with 12 bit or more resolution and sampling rate of over 10 kHz was very difficult, though not impossible. These converters were usually laser trimmed hybrid integrated circuits. The hybrid ICs were bulky, and the yield was often limited due to the special fabrication process and laser trimming. Moreover, converters with resolution over 14 bits were particularly rare.

In this dissertation, a new simple circuit technique which enables a monolithic implementation of very high performance analog-to-digital converters is described. It is shown that a complete 16 bit converter can be integrated on a relatively small chip using a standard fabrication process and without trimming.

CHAPTER 2

RATIO REDUCTION TECHNIQUES FOR HIGH RESOLUTION A/D CONVERTERS

2.1. Overview

High resolution A/D or D/A converters using binary weighted components usually require large ratios between the precision components such as current sources, resistors and capacitors with the exception of R-2R ladder configuration which will be discussed later. A 10 bit converter would need 1024 to 1 ratio in passive element value. In integrated circuits, the area occupied by ratioed elements is proportional to the ratio required. Thus, for high resolution converters, it becomes extremely difficult to accommodate components with the required large dimension ratios on monolithic ICs.

For the type of the converters where current sources are used as precision components, ratio reduction is relatively straightforward. Two digital-to-analog converters (DACs) each with half of the total resolution are linked through a current scaler (Fig. 2.1). The *main DAC* determines the most significant bits (MSBs), and the *sub DAC* determines the least significant bits (LSBs). Although the maximum ratio between the components is reduced, the matching requirement is not reduced. The main DAC has to match to the entire resolution.

The same concept can be applied to both resistive and capacitive converters. However, a voltage buffer is usually required between the main DAC and the sub DAC because neither resistive nor capacitive DACs are perfect voltage sources. This is clearly undesirable for high resolution converters due to non-

idealities of the buffer such as offset voltage, drift, settling etc.

Other methods to reduce component ratios include R-2R or C-2C ladders. While these approaches only require a ratio of 2, the matching requirement is still strict. Usually, a standard integrated circuit process employs ion implanted or polysilicon resistors and MOS capacitors. In practice, matching of these resistors is limited to 8 bits or less. Although MOS capacitors exhibit much better matching properties than resistors, a C-2C structure doesn't provide better linearity because of the parasitic capacitances.

Instead of using single type of components, composite structures can be used to reduce the ratio. Either a resistive-capacitive composite structure [1] or a capacitive-resistive composite structure [2] can be used depending on the application. While the former provides a good monotonicity, the latter gives an excellent integral linearity, when used with the self-calibration technique described in Chapter 3.

2.2. Resistive-Capacitive Composite Structure

In this approach, a resistor string DAC [3] serves as a main DAC and a binary weighted capacitor array DAC [4] is used as a sub DAC (Fig. 2.2). Since the capacitors have infinite impedance in DC steady state, the sub DAC has no loading effect on the main DAC, which enables a direct connection of the main DAC and the sub DAC without a buffer. The only requirement is that the maximum RC constant needs to be small enough to ensure the settling within the desired time.

Now that the resistor string DAC is inherently monotonic, the resulting converter is guaranteed to be monotonic if the capacitor array is monotonic. Therefore, a proper break point between the main DAC and the sub DAC should be

made to insure the monotonicity of the capacitor DAC. From capacitor matching data [4,5], it can be concluded that maximum of 9-10 bit can be assigned to the capacitor DAC without difficulty.

On the other hand, the integral linearity of a resistor string DAC is in general poor. With the exceptions of laser trimmed thin film resistors, the resistivity gradient of integrated resistors is generally large. Therefore, the integral linearity of a resistor string DAC is limited to 8 bits or less [1] [3].

2.2.1. Description of Operation

For the resistive-capacitive converter shown in Fig. 2.2, the resistor string has an M bit resolution and the capacitor array gives additional N bits of resolution resulting M+N bit total resolution.

The resistor string divides the reference voltage into 2^M segments. Nominal segment voltage V_{seg} is therefore :

$$V_{seg} = \frac{V_{ref}}{2^M} \tag{2.1}$$

This segment voltage is further divided into 2^N smaller steps by the capacitor array DAC. Thus,

$$1\ LSB = \frac{V_{seg}}{2^N} = \frac{V_{ref}}{2^{M+N}} \tag{2.2}$$

As in the case of ordinary capacitor array A/D converters, the operation of this converter consists of two phases, the input acquisition phase and the successive approximation search phase.

2.2.2. Input Acquisition Phase

During the input acquisition phase, an unknown input voltage V_i is sampled in the capacitor array. This is achieved by throwing all the bottom plate switches to the input voltage and the top plate switch to the ground. If cancellation of the offset voltage of the comparator is desired, the top plate is connected to the offset voltage of the comparator instead, usually by closing the loop around the comparator.

Enough time should be given to the input acquisition phase to assure correct input voltage is sampled with desired level of accuracy.

2.2.3. Successive Approximation Search Phase

In this phase, the sampled input voltage is converted into digital codes by a successive approximation search. First M bits are determined by the resistor string DAC, and the remaining N bits are determined by the capacitor array DAC.

After the input acquisition is completed, the top plate switch is turned off. At this point, the top plate of the capacitors is floating. Then, all the bottom plate switches are thrown to the output of the resistor string DAC. Thereafter, first M bits are searched in the same manner as an ordinary resistor string A/D converter.

After the main DAC conversion is completed, the two resistor tap voltages between which the input voltage lies are known. Then, one of the bottom plate busses (bus A) is connected to the higher tap voltage of the two, and the other bus (bus B) is connected to the lower tap voltage. Next, lower N bits are determined by the capacitor array in the same way as an ordinary capacitor array

A/D converter. The only difference of the lower N bit conversion from an ordinary capacitor array A/D conversion is that an unknown voltage between two tap voltages is determined instead of between ground and V_{ref}.

2.3. Capacitive-Resistive Composite Structure

Another obvious approach for the composite structure is to use the capacitor array as a main DAC and the resistor string as a sub DAC. This structure overcomes the poor integral linearity of the resistive-capacitive composite structure. MOS capacitors with metallic or heavily doped plates provide an excellent integral linearity, usually better than 10 bits.

A schematic diagram for this structure is shown in Fig. 2.3. The bottom plate of the smallest capacitor C_{1A} is connected to the output of the resistor string DAC. This way, the additional resolution is provided by the resistor string DAC to the capacitor array DAC. Since the value of the coupling capacitor C_{1A} is identical to the unit capacitor C, the voltage modulated by the sub DAC is :

$$1\ LSB = \frac{1}{2^M}\frac{V_{ref}}{2^N} \tag{2.3}$$

Again, N bit resolution is assumed on the main DAC and M bit on the sub DAC.

Although the capacitor array provides excellent integral linearity, monotonicity is not guaranteed for this type of converter. Although a switching scheme that assures monotonicity is available, it is not practical for high resolution converters due to a large number of switches needed for the monotonic switching. Also, physical trimming of the capacitors is extremely difficult. Therefore, some alternative way of correcting the nonmonotonicity of the capacitor array is needed to take the full advantage of this structure. A new circuit technique to

correct both non-monotonicity and non-linearity is described in Chapter 3.

2.3.1. Description of Operation

The operation of this type of the converter is similar to that of resistive-capacitive composite converters described in the previous sections. During the input acquisition phase, the input voltage is sampled on the capacitor array in the same manner as before. The coupling capacitor C_{1A} is kept grounded in this phase.

Upon completion of the input acquisition, a successive approximation search is performed by switching the capacitor array main DAC. After first N bits are determined by the main DAC, the sub DAC conversion begins the same way as an ordinary resistor string converter to determine the lower M bits.

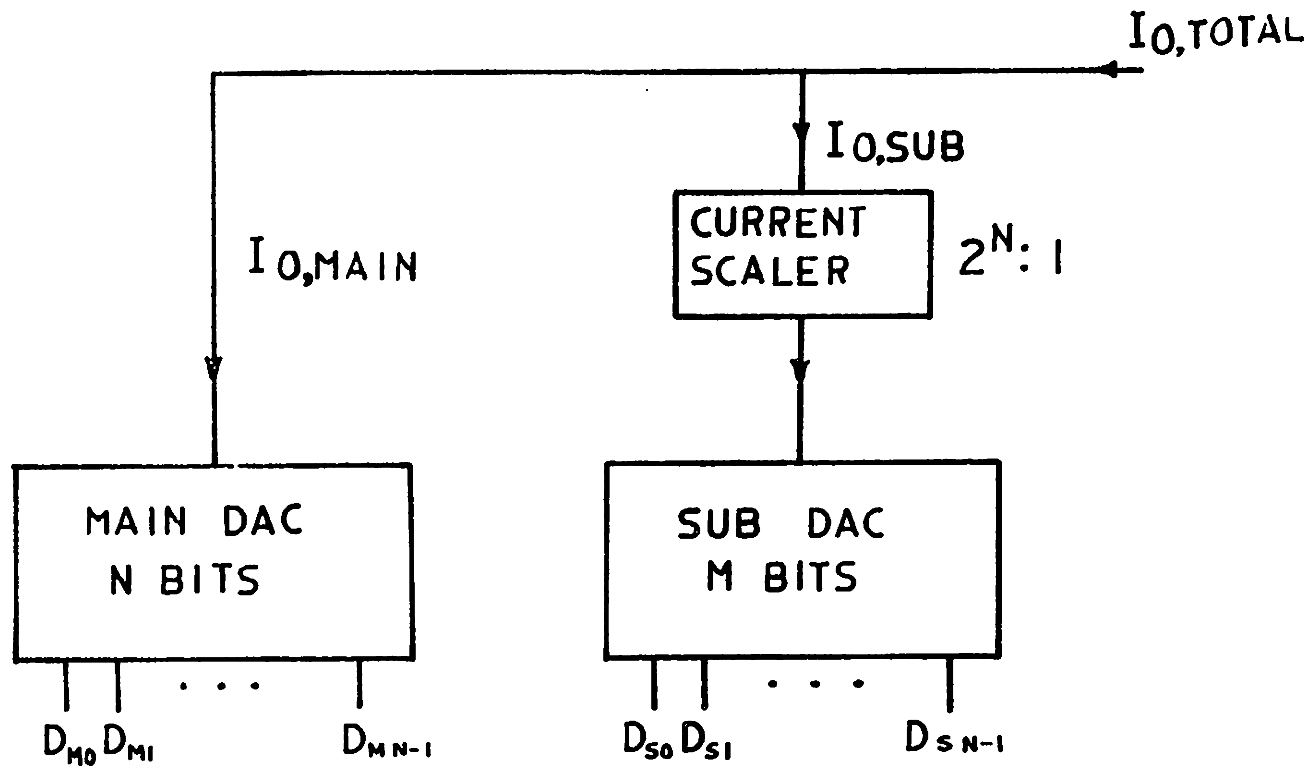


FIG. 2.1 RATIO REDUCUCTION FOR CURRENT SWITCHING DAC

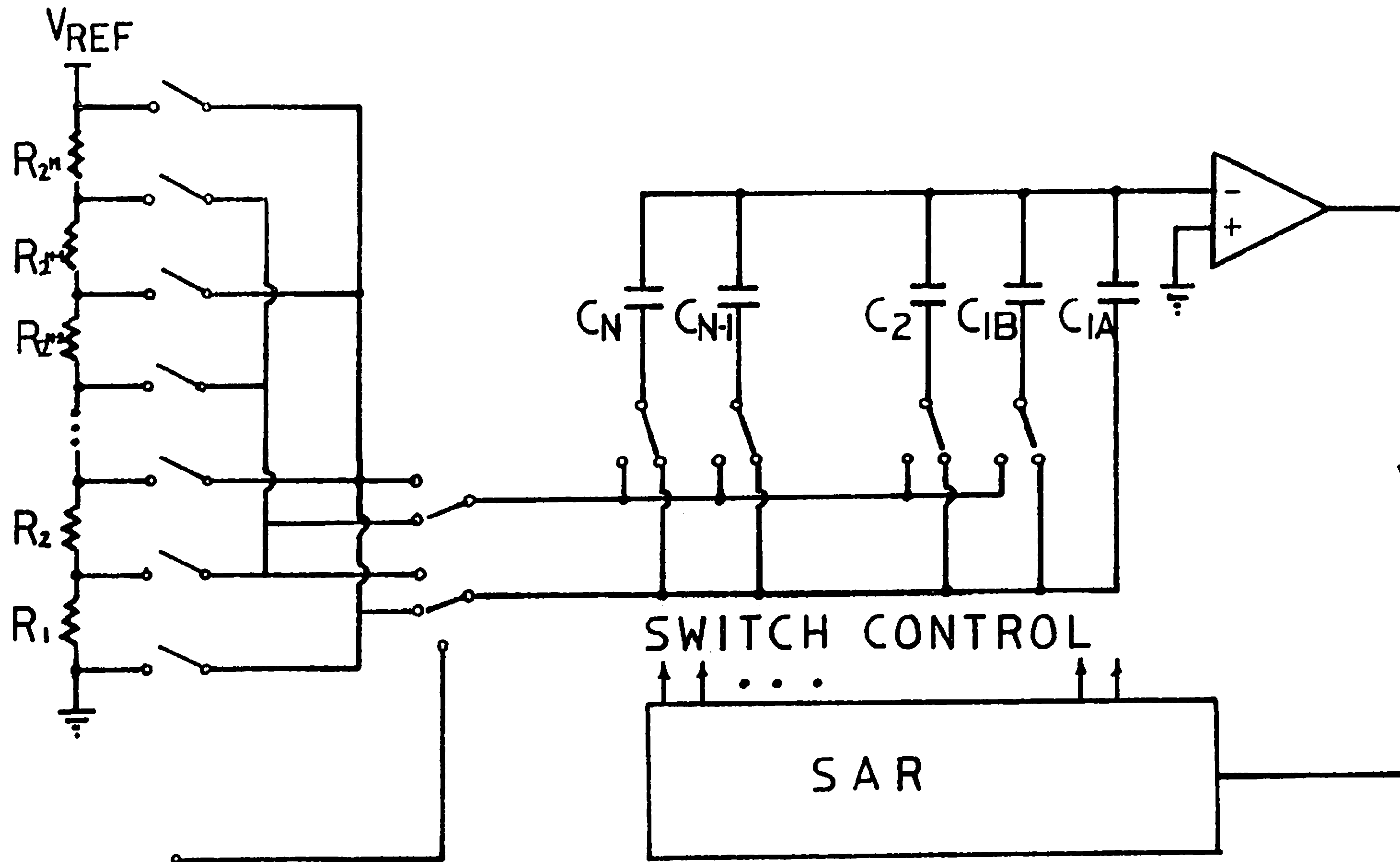


FIG. 2.2. RESISTIVE-CAPACITIVE ADC

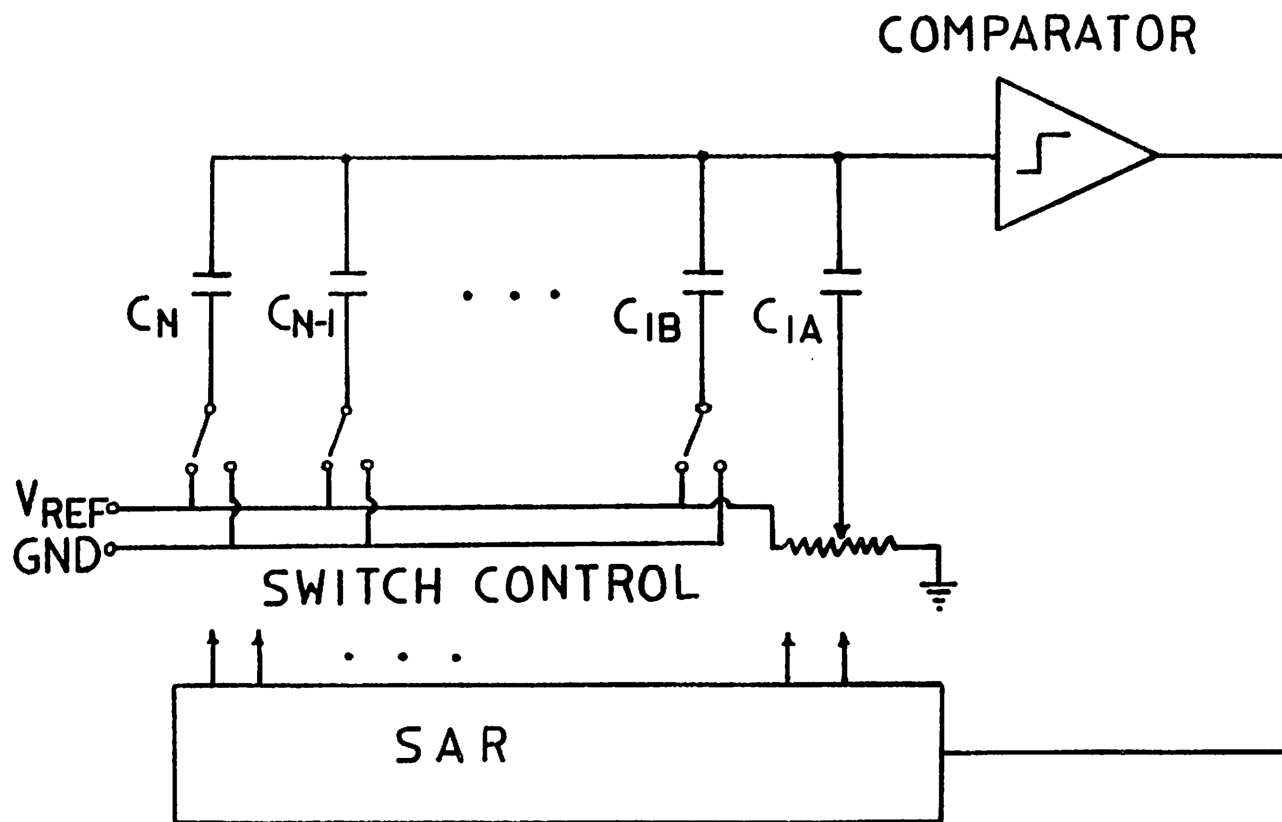


FIG. 2.3 CAPACITIVE-RESISTIVE ADC

CHAPTER 3

SELF-CALIBRATION TECHNIQUE FOR SUCCESSIVE APPROXIMATION A/D AND D/A CONVERTERS

3.1. Overview

In the past, the linearity level of untrimmed A/D or D/A converters was limited to 8 to 10 bits. Although integrating serial converters have higher linearity, they can be used only in digital voltmeters and other slow circuits. Therefore, for general purpose applications, low cost successive approximation A/D converters with high resolution are in great demand. Among the factors that limit the linearity of integrated circuit converters are photolithographic resolution, non-uniform etching and non-uniform doping. To achieve higher resolution and linearity, thin film technology is used together with laser trimming. With these techniques, cost of high resolution converters is relatively high.

Recently, several attempts have been made to build high resolution converters in completely monolithic forms. Some of these techniques are summarized in the following sections. Section 3.2 reviews a technique that uses a radix less than 2 to eliminate missing codes [6]. Each bit value is measured at the factory against a super-linear DAC. The difference of each bit value from the ideal bit value is taken and permanently recorded in programmable read-only memory (PROM). Although plausible as the first attempt to correct the linearity error without laser trimming, extensive factory testing is necessary when calibrated. Also, long term drift of analog parameters is a problem since the calibration is fixed in PROM.

In Section 3.3, a D/A converter that calibrates its linearity against an integrating converter is described [7]. While free from the disadvantages of the previous technique, an external capacitor is necessary for the slow integration. This capacitor can be the major factor that limits the overall converter linearity, because discrete capacitors have significant nonlinearity. In addition, a large RAM is necessary to calibrate to a very high linearity.

In Sections 3.4 and 3.5, recent two high resolution converter techniques without calibration are described. The dynamic component matching technique [8] provides an accurate current division by exchanging two closely matched current sources. Because smooth-out filtering is needed, close initial matching requirement of the current sources is desired to give a faster conversion time. Also, this technique poses a serious difficulty in the supply voltage requirement due to a need for stacking dynamic current dividers for a successive division of the current. In MOS technology where power supply voltage is usually limitied to 10 V and threshold voltages are higher, this is more difficult to implement.

A ratio-independent algorithmic converter [9] achieves an exact multiplication of 2 by a proper switching of capacitors together with a fully-differential operational amplifier. This converter takes significantly less die area than other converters. However, due to a large number of switchings , and settling of operational amplifier, the conversion speed and accuracy are limited. At any resolution level higher than 12 bits, $\frac{kT}{C}$ noise can be a limiting factor due to small capacitors and a large number of switchings.

In Section 3.6, a novel technique is introduced for linearity calibration. All the linearity errors are calibrated against its own reference voltage. Thus, no external sources are necessary for calibration. No external components are needed, and also calibration can be done much faster than with other techniques. The maximum number of registers to store non-linearity data is equal to

the number of bits on the main DAC. With 10 bits on the main DAC and 6 bit on the sub DAC, a maximum of only 10 registers are needed compared to 1024 for the converters described in Section 3.3.

3.2. Reduced Radix Technique

The reduced radix technique was proposed by Z.G. Boyacigiller *et. al.* [6]. A block diagram of such a converter is shown in Fig 3.1. The A/D converter has 17 bits of internal resolution to assure 14 bit final resolution. A modified R-2R ladder is used to generate a radix of 1.85 instead of 2. This reduced radix causes a redundancy of codes used to eliminate missing codes.

A modification on the switching sequence of an ordinary successive approximation register has to be made in addition to the reduced radix to cover any possible missing codes. When the n-th bit is being tested, both the n-th bit and (n+4)th bit are switched in together. If the bit decision is 1, the n-th bit is kept. Otherwise, the n-th bit is dropped. This procedure is identical to an ordinary successive approximation, except that about 8% of redundancy is provided by the (n+4)th bit for a keep decision. On the other hand, an error in drop decision is compensated by the reduced radix since the values of the succeeding bits add up to 1.18 instead of 1.

The actual bit values are measured after packaging in reference to an extremely accurate D/A converter. These bit values are stored in an EPROM in 17 bit words. Each of these bit values are added to the contents of the accumulator if the corresponding bit decision is keep.

One of the main disadvantages of this technique is that calibration can be performed only at the factory, thus long term drift cannot be compensated. Also, due to the fact that an accurate external source (a D/A converter) is

necessary, it is more subject to environmental noise during the calibration. Thin film resistors are necessary because implanted resistors do not provide required matching. A 17x17 bit EPROM can take considerable die area and requires a special process.

3.3. Integration Technique

A serial integrating A/D converter is very slow, but it can be very accurate. Therefore a self-contained integrating A/D converter can be used as a calibration source for a faster A/D or D/A converter. In their paper, K. Maio *et. al.* describe a current steering D/A converter utilizing this technique [7]. A block diagram for such a converter is shown in Fig. 3.2.

This converter has two operating modes, the calibration mode and the conversion mode. In the calibration mode, the digital input of the main DAC is incrementally stepped from zero to full scale. The resulting staircase analog output is compared with an ultra linear ramp generated by a Miller integrator. The differences are digitized by the sub DAC and the SAR, then stored in the RAM. In the conversion mode, the digital input is converted into an analog output in the normal manner. The linearity error previously measured is taken from the RAM and applied to the sub DAC. This compensates the non-linearity of the main DAC which is of the opposite polarity from the data in the RAM.

One of the advantages of this technique is that the calibration circuitry can be self-contained. Therefore, the calibration can be performed often, and it is possible to obtain better overall long term stability than previous techniques.

Instead of calibrating each bit value, this technique calibrates each data point. As a consequence, the size of the RAM increases exponentially with the number of bits that need calibration. If the main DAC has good initial linearity

only the few MSBs need to be calibrated. However, for high resolution converters over 12 bits, the number of bits that need calibration will be much larger. For example, even with a capacitor array DAC, which has the best potential matching property, a recent study [5] shows that upper 10 bits need be calibrated for 16 bit linearity. This necessitates 1024 registers, approximately 12 bits each, which makes 12288 bits of RAM. This is already excessive, and more so for more poorly matched main DACs such as an R-2R ladder or a current steering DAC without thin film technology or laser trimming.

It is not easy to generate a very slow ramp by analog means in monolithic ICs. Either a large capacitor or a small current source is necessary. Any integrated capacitor over 100 pF is virtually impractical, and current sources less than 1μA are very hard to generate. Also, at such level of resolution as 12 bits or more, the current source is desired to be larger to overcome any noise. Therefore, a large external capacitor is almost inevitably required. This gives rise to several practical problems. First, discrete capacitors tend to have large voltage coefficient and dielectric relaxation, which severely limit the linearity and reproducibility of the ramp. Second, the connection of the external capacitor should be made to the virtual ground of the operational amplifier which is a very susceptible point to noise.

Other problems related to this technique include synchronization and noise. The integration rate of the ramp should be accurate to provide synchronization between the staircase output of the DAC and the ramp. Also, due to the slow calibration process, it is more subject to 1/f noise.

3.4. Dynamic Component Matching Technique

In this technique, the reference current is divided into two nominally equal parts. Then, they are rapidly alternated to provide exactly matching current sources. A RC low-pass filter is needed to smooth out the ripple as a result of the initial mismatch of the currents. A longer time constant is needed for a larger mismatch. However, the response time of the DAC is limited by the RC constant. Therefore, for a faster conversion, good initial matching between the current sources is required.

Dynamically matched current sources should be stacked for a successive division of the current. This is a difficult constraint for the power supply because each dynamically matched current source requires 1.5-2 V.

3.5. Ratio Independent Algorithmic Converter

Algorithmic A/D converters are simple, and requires a very small die area. The accuracy of an algorithmic converter can be improved by a ratio independent multiplication technique [9].

The ratio independent multiply-by-two circuit is a switched capacitor integrator with a gain of one. The signal voltage is integrated twice on the integrating capacitor to multiply the signal by two. Due to capacitor ratio error, however, an exact gain of 2 is not obtained this way. The effect of ratio error in the capacitors is cancelled by exchanging the sampling capacitor and the integrating capacitor after the multiplication.

Other non-idealities such as clock charge feed-through and voltage coefficient of the capacitors are reduced by matched switches and fully differential configuration.

One of the disadvantages of this technique for the application of fast, high-resolution A/D converters is the relatively slow speed associated with a large number of switching and settling sequences. In addition, the residual offset voltage, the residual voltage coefficient and $\frac{kT}{C}$ noise can significantly contribute to the differential non-linearity.

3.6. Self-Calibration Technique

As was discussed in Sections 3.2 through 3.5, previous error-correction techniques for high resolution A/D or D/A converters involve various disadvantages. In this section, a fully monolithic, versatile calibration technique is presented. This technique avoids all the disadvantages and practical problems related to previous error correction techniques.

In an ideal binary weighted D/A converter, the value of a bit is identical to the sum of rest of the smaller bits plus 1 LSB (complement of that bit). As an example, for a 10 bit converter, the value of the 3rd bit is equal to the combined values from the 4th to the 10th bit plus 1 LSB which equals the value of the 10th bit. In a non-ideal converter, these values will be different from one another. From the difference between a bit and the complement, each bit value, or the deviation of a bit value from ideal value, can be computed. These data can be stored in a RAM later to be used to correct each bit value.

Since the calibration is performed by comparing a bit to its own complement, no calibration source such as an accurate D/A converter is necessary, unlike other techniques discussed previously. Only a slight modification is needed on the existing SAR to provide appropriate switching for comparing a bit

and its complement. The difference is digitized by a separate calibration DAC and a SAR. The individual bit values are calibrated as in the case of reduced radix technique. However, instead of storing the whole bit values in a PROM, the deviation from the nominal values are recorded in a RAM. Therefore, the word length of the memory is much shorter than that of reduced radix technique. For a 14 bit converter, maximum of 8 words (10 bits each) need be stored compared to 17 words, 17 bit each. The difference will be more dramatic for a higher resolution converter.

Although this self-calibration technique can be implemented on other types of converters, a capacitive-resistive composite structure was selected for experimental verification of the technique. This was mainly due to the inherent sampling capability of capacitive DAC that makes the bit comparison easy.

Sections 3.4.1 through 3.4.3 discuss the theoretical background of the self calibration technique applied to capacitive-resistive composite A/D converter.

3.6.1. Description of Circuit

A block diagram of a capacitive-resistive A/D converter is shown with self-calibration circuitry in Fig 3.3. This circuit consists of an N bit capacitor array main DAC, an M bit resistor string DAC and a resistor string calibration DAC which generally has a few more bits of resolution than the sub DAC.

An initial calibration cycle, typically performed each time power is turned on, corrects the linearity error of the main DAC through use of the *calibration DAC*.

Digital control circuits govern capacitor switching during the calibration cycle, and store the nonlinearity correction terms in data registers. The ratio

errors of the sub DAC, and overall quantization errors accumulate during digital computation of error voltages. To overcome these errors for a 16 bit converter, 2 bits of additional resolution are needed during the calibration cycle.

3.6.2. Details of Operation

Fig. 3.4a shows an N-bit weighted capacitor DAC. Each weighted capacitor C_n is assumed to be off by a factor of $(1+\varepsilon_n)$ from the ideal value due to process variations.

$$C_n = 2^{n-1}C(1+\varepsilon_n), \quad n = 1A, 1B, \cdots, N \tag{3.1}$$

where the unit capacitor C is defined as the total capacitance divided by 2^N :

$$C = \frac{C_{total}}{2^N} = \frac{C}{2^N}\sum_{i=1A}^{N} 2^{i-1}(1+\varepsilon_i) = C + \sum_{i=1A}^{N} 2^{i-1}\varepsilon_i \tag{3.2}$$

And we get :

$$\sum_{i=1A}^{N} 2^{i-1}\varepsilon_i = 0 \tag{3.3}$$

The output voltage of a weighted capacitor DAC such as shown in Fig. 3.4a can be expressed in terms of capacitor values and corresponding digital input codes.

$$V_o = \frac{V_{ref}}{C_{total}}\sum_{i=1B}^{N} C_i D_i$$

$$= \frac{V_{ref}}{2^N(1+\sum_{i=1A}^{N} 2^{i-1}\varepsilon_i)}\sum_{i=1B}^{N} 2^{i-1}(1+\varepsilon_i)D_i$$

And by Equation 3.3 :

$$V_o = \frac{V_{ref}}{2^N}\sum_{i=1B}^{N} 2^{i-1}(1+\varepsilon_i)D_i \tag{3.4}$$

The ideal output voltage $V_{o,ideal}$ can be obtained by taking $\varepsilon_i=0$ for all i in Equation 3.4

$$V_{o,ideal} = \frac{V_{ref}}{2^N}\sum_{i=1B}^{N} 2^{i-1}D_i \tag{3.5}$$

The error voltage V_{error} is the difference between ideal and actual output voltages :

$$\begin{aligned} V_{error} &= V_o - V_{o,ideal} \\ &= \frac{V_{ref}}{2^N}\sum_{i=1B}^{N} 2^{i-1}\varepsilon_i D_i \end{aligned} \tag{3.6}$$

Define the error voltage $V_{\varepsilon n}$ due to the nth capacitor mismatch :

$$V_{\varepsilon n} \equiv \frac{V_{ref}}{2^N}2^{n-1}\varepsilon_n, \quad n = 1B, 2, \cdots, N \tag{3.7}$$

Then, Equation 3.6 becomes :

$$V_{error} = \sum_{i=1B}^{N} V_{\varepsilon i}D_i \tag{3.8}$$

The calibration cycle begins by measuring the nonlinearity due to the MSB capacitor C_N. This is done by sampling the reference voltage V_{ref} on all the capacitors except the MSB capacitor, as shown in Fig. 3.4b. At this time, the sampled charge in the capacitor array is :

$$\begin{aligned} Q &= -V_{ref}\sum_{i=1A}^{N-1} C_i \\ &= -CV_{ref}\sum_{i=1A}^{N-1} 2^{i-1}(1+\varepsilon_i) \end{aligned} \tag{3.9}$$

Next, charge is redistributed by reversing the switching configuration as shown in Fig. 3.4c. The residual charge at the top plate of the capacitor array is :

$$Q_{xN} = V_{ref}(C_N - \sum_{i=1A}^{N-1} C_i)$$

$$= CV_{ref}(2^{N-1}\varepsilon_N - \sum_{i=1A}^{N-1} 2^{i-1}\varepsilon_i) \tag{3.10}$$

From Equation 3.3, it follows :

$$\sum_{i=1A}^{N} 2^{i-1}\varepsilon_i = 2^{N-1}\varepsilon_N + \sum_{i=1A}^{N-1} 2^{i-1}\varepsilon_i = 0$$

Thus :

$$\sum_{i=1A}^{N-1} 2^{i-1}\varepsilon_i = -2^{N-1}\varepsilon_N \tag{3.11}$$

Substituting Equation 3.11 in Equation 3.10, we get :

$$Q_{xN} = CV_{ref}\, 2^N \varepsilon_N \tag{3.12}$$

The residual voltage V_{xN} is :

$$V_{xN} = \frac{Q_{xN}}{C_{total}} = 2V_{\varepsilon N} \tag{3.13}$$

Similarly, errors due to smaller capacitors are measured. In each case, a successive approximation search using the sub DAC is used.

It can be easily shown that the general relation between residual voltages (V_{xn}'s) and the error voltages or *correction terms* (V_ε's) is :

$$V_{\varepsilon n} = \frac{1}{2}(V_{xn} - \sum_{i=n+1}^{N} V_{\varepsilon i}), \quad n = 1B, 2, \cdots, N-1 \tag{3.14}$$

or in digital domain :

$$DV_{\varepsilon N} = \frac{DV_{xN}}{2} \tag{3.15}$$

$$DV_{\varepsilon n} = \frac{1}{2}(DV_{xn} - \sum_{i=n+1}^{N} DV_{\varepsilon i}), \quad n = 1B, 2, \cdots, N-1 \tag{3.16}$$

where $DV_{\varepsilon n}$ and DV_{xn} stand for digitized correction terms and digitized residual voltages *(residual terms)*, respectively.

Therefore, by digitizing residual voltages using the sub DAC, digital correction terms $DV_{\epsilon N}$, $DV_{\epsilon N-1}$, $\cdots$, $DV_{\epsilon 1B}$ can be computed subsequently by Equation 3.15 and Equation 3.16. All these correction terms are stored in digital memory.

During subsequent normal conversion cycles, the calibration logic is disengaged. The converter works the same way as an ordinary successive-approximation converter, except that error-correction voltages are added by proper adjustment of the sub DAC digital input code. When the nth bit is being tested, corresponding correction term $DV_{\epsilon n}$ is added to the correction terms accumulated from the first bit (MSB) through the $(n-1)^{th}$ bit. If the bit decision is 1, the added result is stored in the accumulator. Otherwise, $DV_{\epsilon n}$ is dropped, leaving the accumulator with the previous result. The content of the accumulator is converted to an analog voltage by the calibration DAC. This voltage is then subtracted from the main DAC output voltage through the capacitor C_{cal}. The overall operation precisely cancels the nonlinearity due to capacitor mismatches by subtracting V_{error} in Equation 3.8 from the actual output voltage V_o in Equation 3.4. The only extra operation involved in a normal conversion cycle is one 2's complement addition. The flow chart showing the normal conversion operation is shown in Fig 3.5a, and the memory organization is illustrated in Fig. 3.5b.

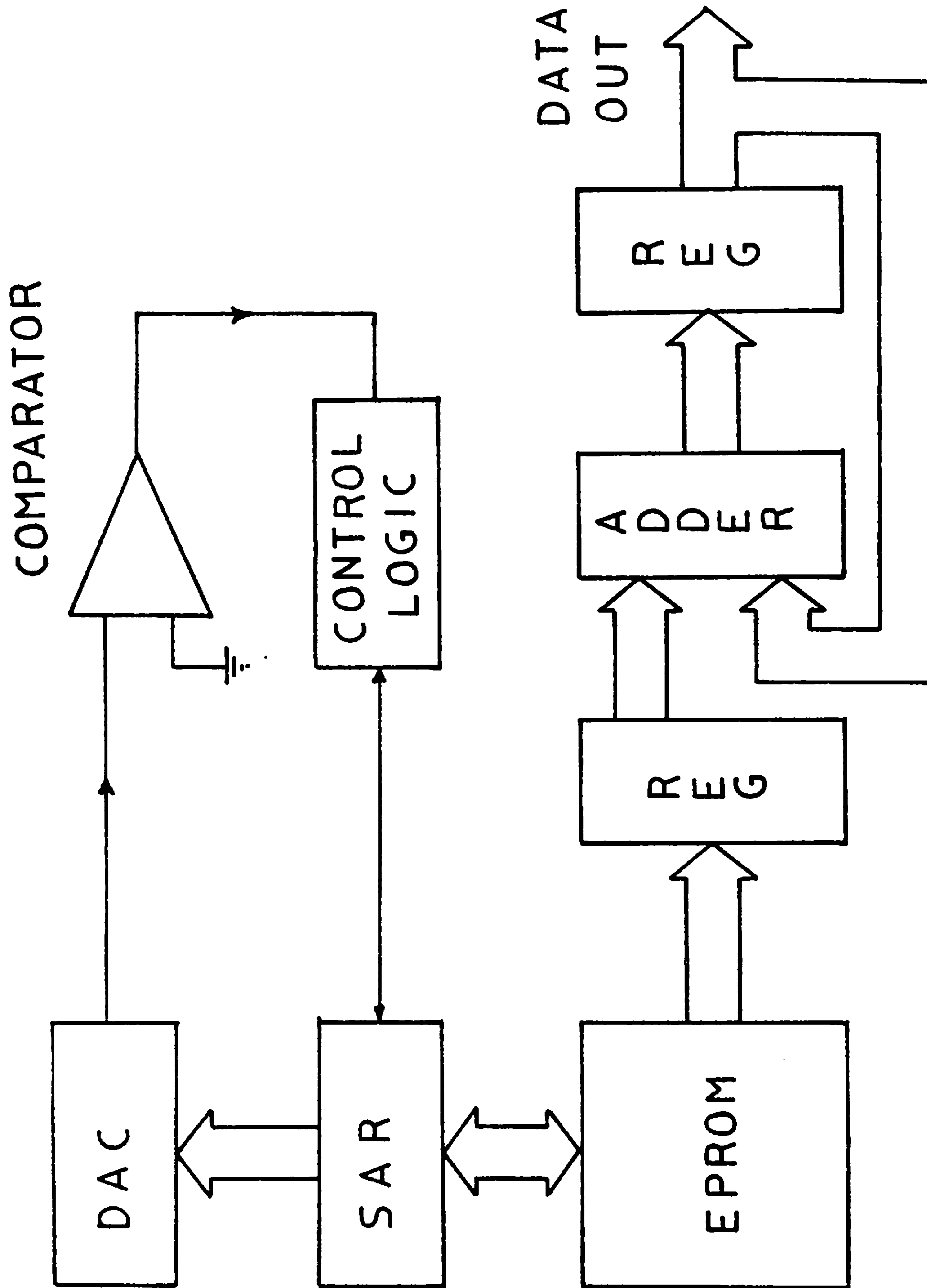


FIG.3.1 REDUCED RADIX ADC

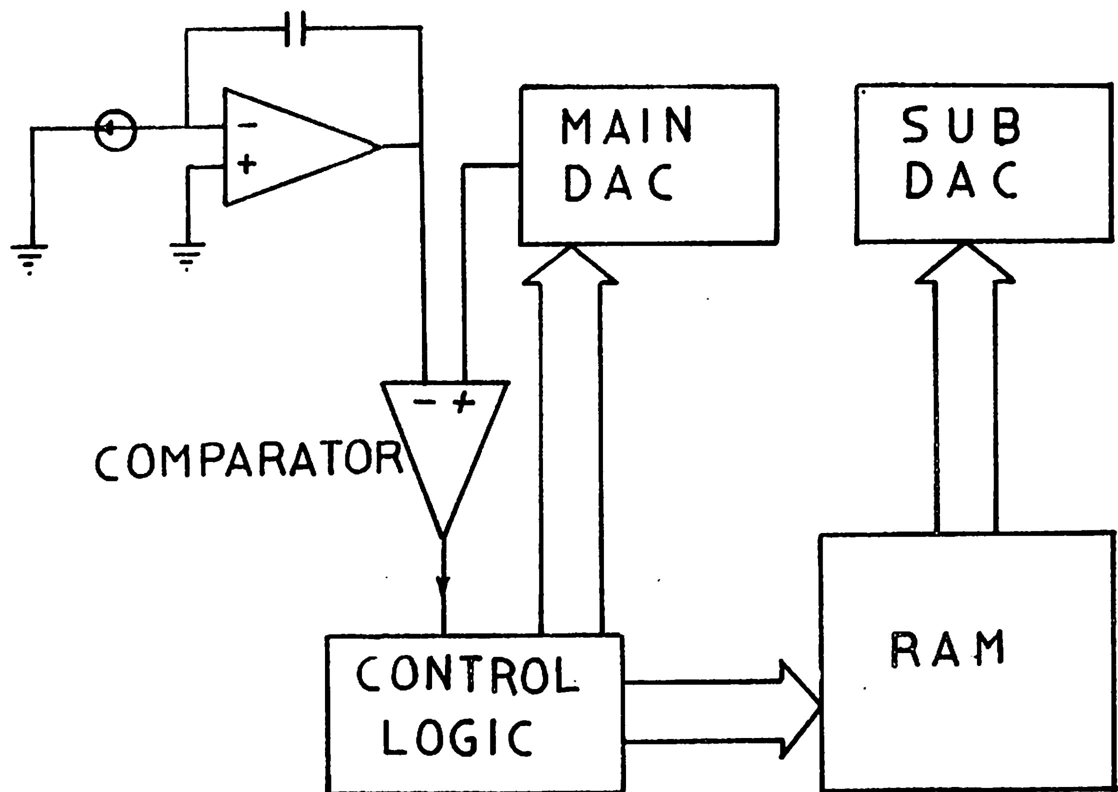


FIG. 3.2 ERROR-CORRECTING DAC

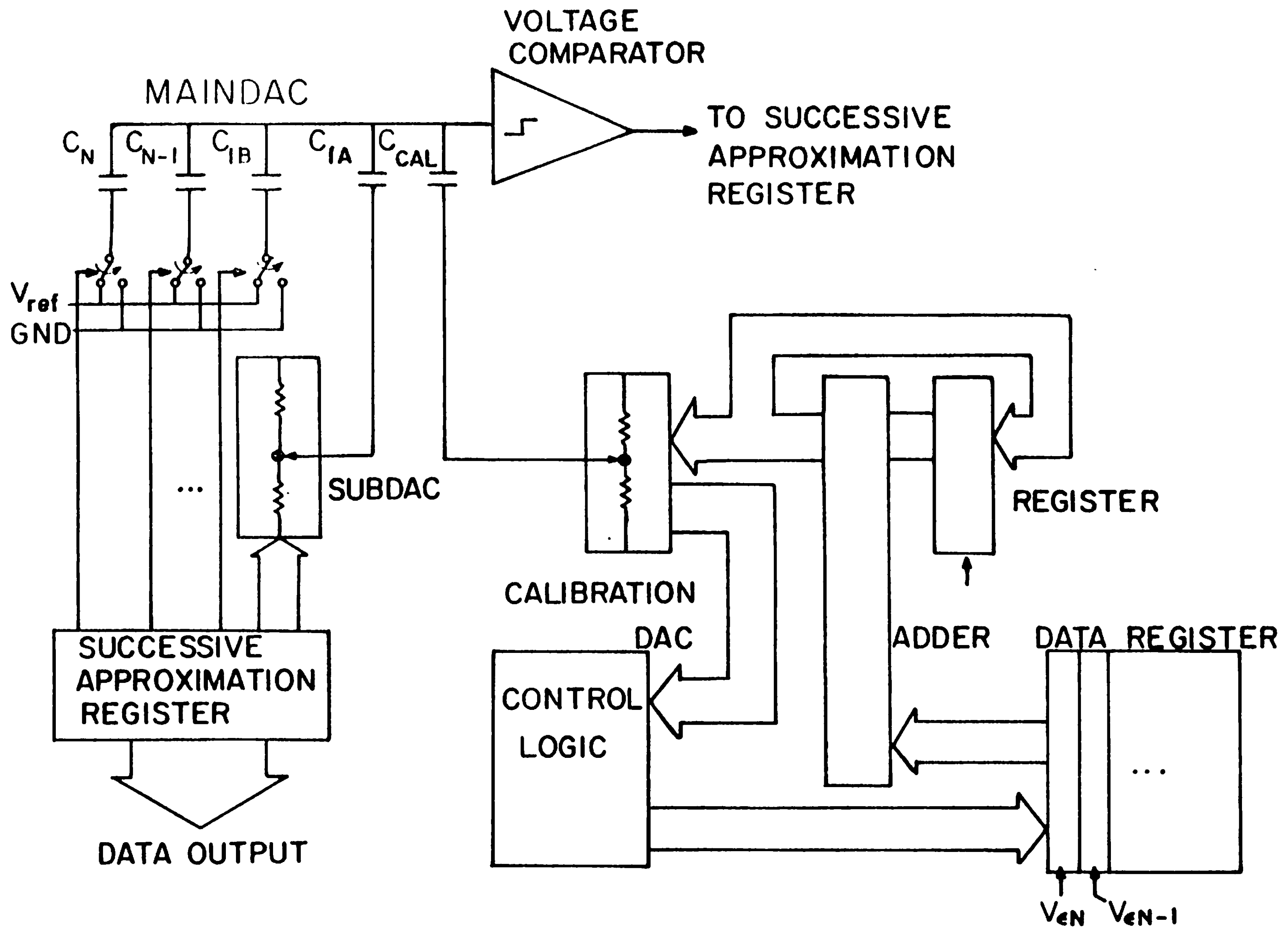
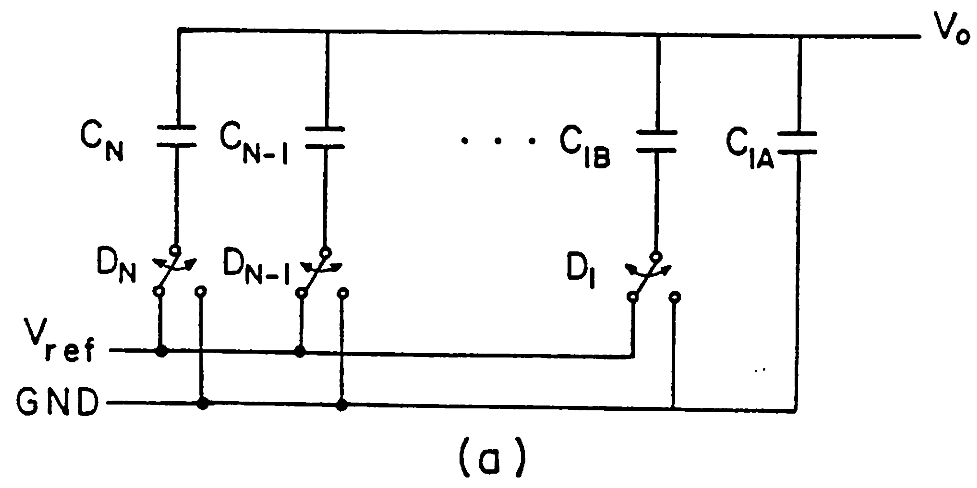
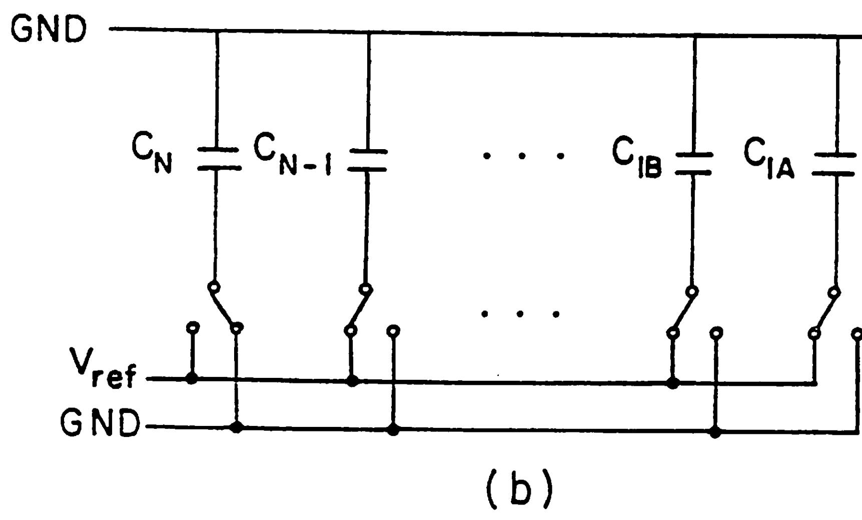


FIG. 3.3 SELF-CALIBRATING A/D CONVERTER





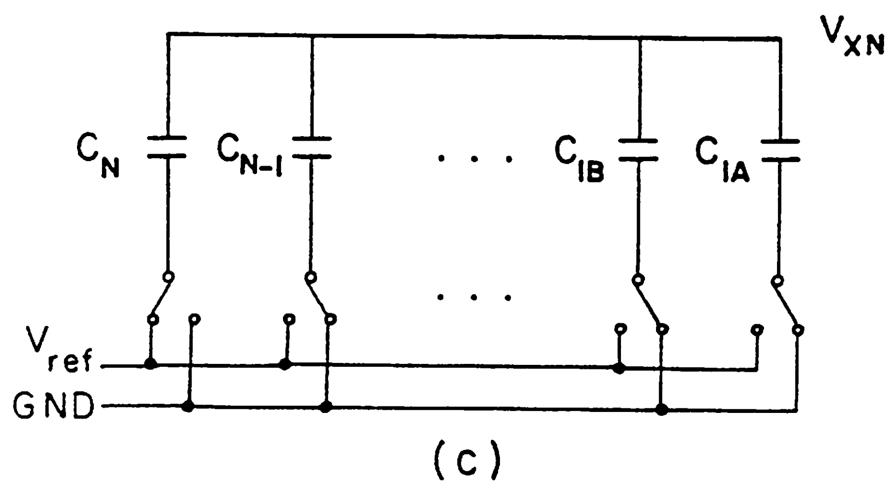


FIG. 3.4 a) WEIGHTED CAPACITOR DAC

b) PRECHARGE CYCLE

c) CHARGE REDISTRIBUTION

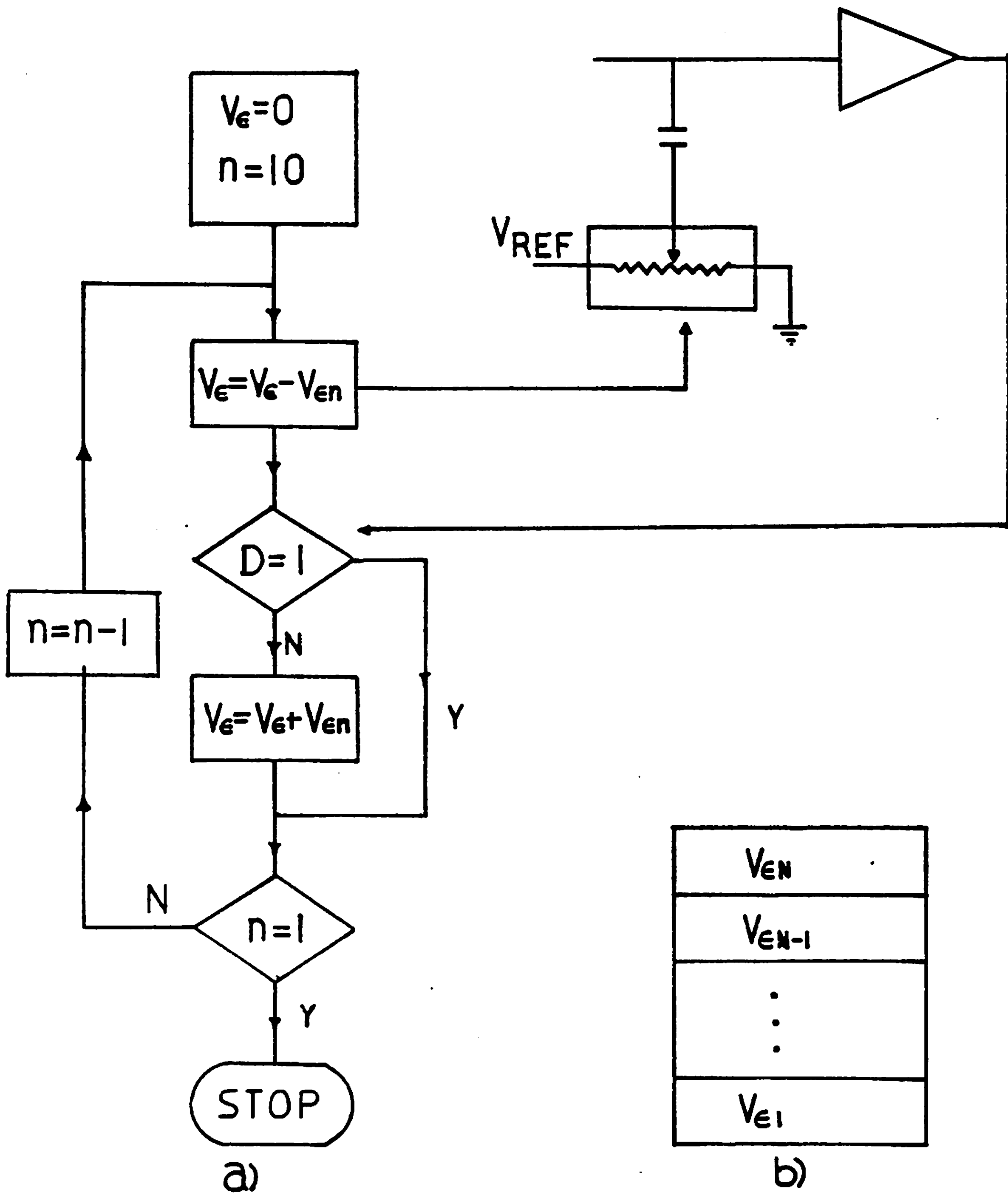


FIG. 3.5 a) CONVERSION FLOWCHART
b) MEMORY ORGANIZATION

CHAPTER 4

HIGH RESOLUTION CMOS COMPARATOR

4.1. Design Considerations for a High Resolution Comparator

In addition to the precision components, the comparator of an A/D converter also is critical in determining the performance of the converter. Therefore a successful design of a comparator is a vital factor in achieving high resolution and accuracy in an A/D converter.

The primary design specifications of a comparator include the minimum resolution, worst case delay and noise. Other parameters such as the offset voltage, power dissipation and power supply rejection should be considered as well.

The initial performance goal of the experimental circuit for the verification of the self-calibration technique was set to be 16 bit resolution and 50 kHz sampling rate. Widely accepted power supply voltages of 5V and -5V were chosen for the analog circuitry. Given these supply voltages, the size of an LSB is 150 μV assuming $\pm$ 5V reference voltages. Thus, the comparator should have better than 75 μV resolution and less than 500 ns worst-case delay to ensure an accurate 16 bit conversion in less than 20 μs. Also, for 16 bit final resolution, the calibration requires 2 additional bits of resolution to that of the sub DAC, requiring 20 μV resolution. To prevent the comparator output from erroneously changing, a latch is needed. To overcome digital switching noise, the strobe timing of the latch should be midway between the clock edges.

4.2. Selection of Technology

For the type of the converter described in Section 3.4, MOS technology is heavily preferred to bipolar technology. This is because MOS transistors are ideal for switching capacitors. Bipolar transistor switches have several millivolts of offset voltage between the collector and the emitter even at zero collector current. Also, because MOS transistors have negligible gate leakage current, a very low input current comparator can be built which is essential for the use with capacitor DAC.

In comparing two most popular MOS technologies, NMOS and CMOS, several factors should be considered. First of all the comparator should have a voltage gain exceeding 100 dB to amplify 20 μV of signal to a voltage high enough to trip the latch. It would be extremely difficult to realize this much gain with NMOS technology. Although it is possible to cascade many amplifier stages to get a large gain from NMOS technology, it is more desirable to have large gain per stage if offset cancellation is considered. Also, CMOS technology has an edge over NMOS technology in voltage swing. Since a complementary switch can turn on and off any voltages between the two supply voltages, the reference voltage can be very close to both supply rails. This is an advantage in maximizing LSB size.

For the previously mentioned reasons a CMOS technology is chosen for the experimental circuit. The technology chosen was a standard Berkeley CMOS process [10], with 6 μm minimum gate length and 5 μm minimum feature size. A brief description of the process flow are given in Appendix 1.

4.3. Circuit Topology Selection : Amplifier

4.3.1. General Considerations

The amplifier section of the comparator should provide a gain more than 100,000 with a minimum delay possible and input referred noise less than 20 μV.

It is very difficult to determine the optimum number of stages to minimize response time for the given gain. Although work has been done to obtain the optimum number of stages for the small signal case [11], a large signal analysis is needed here since the worst case response time will occur when the input swings from a large voltage to a very small voltage of the opposite sign. Due to the highly non-linear behavior of the devices at large signal level, the analysis is so complicated as to make computer simulation the only possible solution. Even with a fixed number of stages, the response time will be heavily dependent on the circuit configuration and the device geometry. Thus, rather than trying to optimize the number of stages, it would be more effective to select an optimum circuit configuration and device geometry for a chosen number of stages for other reasons.

Minimum number of stages should be used for ease in obtaining closed-loop stability. The loop can be closed around the amplifier to sample the offset voltage directly on the capacitor array. At least two stages are needed to provide enough gain for 16 bit resolution. For these reasons, a two stage amplifier is selected for the comparator.

A schematic diagram of a basic two stage differential input amplifier is shown in Fig 4.1. For this amplifier to be used as a comparator, the parasitic capacitances at the high impedance nodes should be minimized. This is because during comparisons, this amplifier is operated in the open loop configuration, and the dominant open loop poles are determined by the parasitic capacitances

at the high impedance nodes. To meet the requirement for low noise, the input transistors M1 and M2 should be very large. This is because thermal noise power is inversely proportional to the transconductance of a transistor which in turn has a square-root dependence on the device aspect ratio. Therefore, with a fixed gate length, a larger transistor provides less thermal noise at the same current level. Also, $\frac{1}{f}$ noise power is inversely proportional to the gate area of the transistor. [12]

The gate-to-drain overlap capacitance and the drain to bulk capacitance of M2 will be correspondingly large, and directly load the high impedance node 1. Also, the gate-to-source capacitance and Miller multiplied gate-to-drain capacitance of M6 will load the same node. And at the other high impedance node 2, the parasitic capacitances are from the gate-to-drain overlap capacitances and drain-to-bulk capacitances of both M6 and M7.

These parasitic capacitive loadings can be minimized by use of cascode stages and source follower stages. Consider an improved circuit of Fig. 4.2. Here, M8 and M9 are common gate stages which decouple the large parasitic capacitances from the high impedance node 1. M11 and M12 forms a source follower stage that isolates the capacitances associated with M6. M10 is an extra device for biasing M11. At the second stage, M13 and M14 keeps the capacitive loadings of M6 and M7 from node 2. With these modifications the open loop performance is drastically improved. However, due to the common gate stage and the biasing transistor M10, the positive power supply needs to be higher than the basic amplifier. Assuming nominal threshold voltages of ±.7V, operating this circuit with ±5V supply will not guarantee that all the transistors are in the saturation region. This problem is overcome by using a folded cascode amplifier.

4.3.2. Folded Cascode Amplifier

A folded cascode amplifier provides all the advantages of an ordinary cascode amplifier, while requiring less supply voltage. The final design of the amplifier employing a folded cascode input stage is shown in Fig. 4.3. As is shown in the schematic diagram, there are at most two transistors stacked on either side of the power supply. Thus, even with a large variation in threshold voltages, ±5V supply voltages are safe. Due to the folding of the first stage, the second stage is inverted. Now, the input transistor of the second stage is an n-channel transistor. This is another advantage in terms of gain because of a larger transconductance of an n-channel transistor.

4.3.3. Closed Loop Considerations ; Frequency Compensation

The effect of the offset voltage is canceled by closing the switch M19. However, charging the large DAC capacitor using only the bias current of the amplifier would be very slow. To help speeding up the charging, a large switch M20 is added. This transistor brings the capacitor voltage to the ground very quickly. Since the offset voltage will be very small (several tens of millivolts at most), settling time will be negligible from this point. After M20 is turned off and the capacitor voltage is at near ground, M19 is turned on, sampling the offset voltage on the capacitor. During this time the compensation capacitor C_C is connected to stabilize the amplifier. The approximate value of the compensation capacitor C_C can be calculated [13]. In the equivalent circuit of Fig. 4.4a for the basic two stage amplifier, the compensation capacitor C_C is driven by an ideal voltage follower to eliminate right half plane zero. Then the node voltage equations describing the circuits are :

$$gm_1V_1 + \frac{V_2}{R_1} + sC_1V_2 + sC_C(V_2 - V_0) = 0 \tag{4.1}$$

$$gm_2V_2 + \frac{V_0}{R_2} + sC_2V_0 = 0 \tag{4.2}$$

These equations can be solved for $\frac{V_0}{V_i}$:

$$\frac{V_0}{V_i} = \frac{a}{1+bs+cs^2} \tag{4.3}$$

where

$$a = gm_1gm_2R_1R_2$$

$$b = R_1R_2gm_2C_C + R_1(C_1+C_C) + C_2R_2$$

$$c = R_1R_2C_2(C_1+C_C)$$

Approximate locations of the poles can be calculated assuming the poles are widely spaced and $C_C, C_2 \gg C_1$:

$$p_1 = -\frac{1}{(1+gm_2R_2)C_CR_1} \tag{4.4}$$

$$p_2 = -\frac{gm_2}{C_2} \tag{4.5}$$

And the unity gain frequency is :

$$\omega_1 = -\frac{gm_1}{C_C} \tag{4.6}$$

For a good stability, the phase margin should be more than 60 degrees. The phase contribution from p_1 near the unity gain frequency ω_1 is close to 90 degrees. Hence, the phase contribution from p_2 should be less than 30 degrees at ω_1. Thus :

$$\frac{\omega_1}{p_2} < \tan^{-1}30^\circ = \frac{1}{\sqrt{3}} \tag{4.7}$$

Substituting the values for ω_1 and p_2 from the previous equations :

$$\frac{C_C}{C_2} > \frac{1}{\sqrt{3}} \frac{gm_1}{gm_2} \tag{4.8}$$

From this equation, it can be shown a 200 pF compensation capacitor would be needed for a 120 pF capacitor array load if the transconductances of the first and the second stages are comparable. A capacitor of this size would be impractical to be implemented on a monolithic IC and also would severely limit the slew rate and the settling time.

A pole-zero cancellation technique is used to reduce the size of the compensation capacitor as well as to improve closed loop performance. A left half plane zero is introduced by the source follower stage consisting of M17 and M18 that will match the non-dominant pole.

Consider the simplified equivalent circuit of Fig. 4.4b. In this equivalent circuit, the common gate stage of M8 and M9 as well as the source follower stage of M11 and M12 are neglected since the poles and zeroes associated with these stages lie well beyond the range of interest. The node voltage equations for this equivalent circuit are :

$$gm_1 V_1 + (\frac{V_2}{R_1} + sC_1) V_2 + \frac{sC_C}{1+s\frac{C_c}{gm_{17}}} (V_2 - V_0) = 0 \tag{4.9}$$

$$gm_5 V_2 + (\frac{1}{R_2} + sC_2) V_0 = 0 \tag{4.10}$$

Solving for $\frac{V_0}{V_1}$:

$$\frac{V_0}{V_1} = -\frac{a}{1+b's+c's^2+d's^3}(1+s\frac{C_C}{gm_{17}}) \tag{4.11}$$

where

$$a = gm_1 gm_6 R_1 R_2$$

$$b' = R_1(C_1+C_C) + R_2C_2 + gm_6 R_1 R_2 C_C + \frac{C_C}{gm}17$$

$$c' = R_1 R_2 C_2(C_1+C_2) + \frac{C_C}{gm_{17}}(R_1C_1+R_2C_2)$$

$$d' = \frac{R_1C_1C_CC_2R_2}{gm_{17}}$$

Assuming that the pole are widely spread and that $C_C, C_2 \gg C_1,\ R_1, R_2 \gg \frac{1}{gm_{17}}$,

$$p_1 = -\frac{1}{gm_6 R_1 R_2 C_C} \tag{4.12}$$

$$p_2 = -\frac{gm_6}{C_2} \tag{4.13}$$

$$p_3 = -\frac{gm_{17}}{C_1} \tag{4.14}$$

$$z = -\frac{gm_{17}}{C_C} \tag{4.15}$$

To eliminate the non-dominant pole p_2, it is required that :

$$z = p_2 \tag{4.16}$$

or

$$\frac{gm_{17}}{gm_6} = \frac{C_C}{C_L} \tag{4.17}$$

Also, as in the previous case, the compensation capacitor should be selected such that :

$$\frac{p_3}{\omega_1} = \sqrt{3} \tag{4.18}$$

or

$$\frac{gm_6}{gm_1}\frac{C_C}{C_1}\frac{C_C}{C_L} = \sqrt{3} \tag{4.19}$$

For MOS capacitors, major component of C_1 is the junction capacitance between the capacitor bottom plate and the substrate. Using the measured value [14] for the zero bias junction capacitance $C_{j0} = 64\times10^{-4} pF/\mu^2$, $\varphi = .8V$ and bottom plate bias $V_a = -3V$

$$C_j = \frac{C_{j0}}{\sqrt{1-\frac{V_a}{\varphi}}}$$

$$= 3\times10^{-5} pF/\mu^2$$

For 1000 Å oxide, C_{OX} is :

$$C_{OX} = 3.45\times10^{-4} pF/\mu^2$$

Thus :

$$\frac{C_C}{C_1} = \frac{C_{OX}}{C_j} \approx 9$$

Using this value, Equation (4.19) becomes :

$$\frac{C_C}{C_L} \approx .2\frac{gm_1}{gm_6}$$

For $gm_1 \approx gm_6$ and $C_L = 120pF$:

$$C_C = 24pF$$

Compared with 200 pF for the simple pole-splitting compensation, this is a great reduction.

The transconductances of n-channel transistors M6 and M17 should be scaled in proportion to the ratio between the compensation capacitor and the array capacitor. Theoretically, it is possible to scale the transconductances of

transistors by scaling the aspect ratio. The transconductances of M6 and M17 are :

$$gm_6 = \{2K\left(\frac{Z_6}{L}\right)I_{D6}\}^{1/2} \tag{4.20}$$

$$gm_{17} = \{2K\left(\frac{Z_{17}}{L}\right)I_{D17}\}^{1/2} \tag{4.21}$$

The drain current of M17 is :

$$I_{D17} = I_{D18} = \frac{K}{2}\left(\frac{Z_{18}}{L}\right)(V_{GS18}-V_T)^2 \tag{4.22}$$

Thus :

$$gm_{17} = \left\{K^2\left(\frac{Z_{18}}{L}\right)\left(\frac{Z_{17}}{L}\right)(V_{GS18}-V_T)^2\right\}^{1/2}$$

$$= K(V_{GS18}-V_T)\left(\frac{Z_{17}}{L}\right)^{1/2}\left(\frac{Z_{18}}{L}\right)^{1/2} \tag{4.23}$$

Since $V_{GS6}-V_T = V_{GS18}-V_T$ for $V_i = 0$,

$$\frac{gm_{17}}{gm_6} = \frac{\left(\frac{Z_{17}}{L}\right)^{1/2}\left(\frac{Z_{18}}{L}\right)^{1/2}}{\left(\frac{Z_6}{L}\right)} \tag{4.24}$$

Assuming M17 and M18 are identical :

$$\frac{gm_{17}}{gm_6} = \frac{\left(\frac{Z_{17}}{L}\right)}{\left(\frac{Z_6}{L}\right)} = \frac{Z_{17}}{Z_6} \tag{4.25}$$

This equation shows that the ratio of the transconductances can be scaled by directly scaling the width of the two transistors. In reality, due to the different body bias the transconductances of M6 and M17 cannot match pre-

cisely. The result of the mismatch will be the slow settling component during transient [15]. The amplitude of the slow settling component can be shown to be:

$$V_{SS} \approx V_i \frac{\Delta\omega}{\omega_1} \qquad (4.26)$$

where V_{SS} is the amplitude of the slow settling component, V_i is the input voltage, $\Delta\omega$ is mismatch between the pole and the zero, ω_1 is the unity gain angular frequency. The input voltage V_i is the offset voltage of the comparator plus the charge injection from the big grounding switch, which will not exceed 100 mV. Assuming 20% mismatch of transconductances, zero frequency of 400 kHz and unity gain bandwidth of 4 MHz, the initial amplitude of the slow settling component is less than 2 mV. Approximately 5 time constants of the slow settling component would be required to attain less than 20 μV error. SPICE simulation shows that 1.5 μs is needed for the amplifier to settle within 20 μV of the final value. This is of no importance because the loop is closed only once per conversion which would take 20 μs. The device sizes and the drain currents are summarized in Table 4.1. The performance of the amplifier simulated by spice is shown in Table 4.2.

4.3.4. Effect of the Feedback Switch

To hasten the settling when the loop is closed to sample the offset voltage on the capacitor, a large MOS switch M20 is turned on to connect the top plate to the ground Since the offset voltage is small, this already brings the top plate voltage close to its final value. Then this switch is opened and another switch is turned on to close the loop. This switch should be small to minimize the charge injection which will cause residual offset voltage.

In the following analysis, it is shown that the pole arising from the small feedback switch is at a very high frequency and can be neglected.

In Fig. 4.5, the equivalent circuit of the output stage and the feedback switch is shown. Here, R_1 is the output resistance of the amplifier, C_1 is the parasitic capacitance at the output node, C_L is the load capacitance, and R_S is series ON resistance of the switch. For an ideal feedback switch (Fig. 4.5a), the series resistance of the switch is 0 and C_1 and C_L are shunted. For a non-ideal switch, the transfer function for $\frac{V_2}{V_1}$ is :

$$\frac{V_2}{V_1} = \frac{1}{1+s(C_L R_S + C_L R_1 + C_1 R_1) + s^2 C_1 C_L R_1 R_S} \quad (4.27)$$

For $R_1 \gg R_2$, $C_L \gg C_1$:

$$\frac{V_2}{V_1} \approx \frac{1}{1+sC_L R_1} \cdot \frac{1}{1+sC_1 R_S} \quad (4.28)$$

For the amplifier of Fig. 4.3, following values are computed :

$$R_1 = 750\,k\Omega$$

$$R_S = K\frac{Z}{L}(V_{GS} - V_{TH})$$

Assuming $K = 35\mu A/V^2$, $Z = 10\mu$, $L = 6\mu$ and $V_{GS} - V_{TH} = 4V$:

$$R_S = 5k\Omega$$

$$C_1 = 0.3\,pF,\ C_L = 120\,pF$$

Then the pole due to R_S becomes :

$$\frac{1}{2\pi C_1 R_S} \approx 100MHz$$

This high frequency pole can be neglected and the equivalent circuit of Fig. 4.5b becomes identical to the ideal switch case of Fig. 4.5a.

4.4. Selection of Circuit Topology : Latch

The latch is shown in Fig. 4.6. This is a simple regenerative circuit activated by the STROBE signal. STROBE signal will be delayed from the clock edges to avoid switching noise [16]. M1, M2, M3, and M4 consist regenerative circuit. M7 and M8 form a source follower to prevent feed-through from the latch to the high impedance output of the amplifier, adversely affecting the regeneration. Another source follower formed by M9 and M10 is added for symmetry.

In order to increase the driving capability of the latch, a source follower and an inverter are added to the output. This latch is expected to drive 30 to 100 pF of external load.

The device dimensions and SPICE simulation results of the latch are shown in Table 4.3 and Table 4.4.

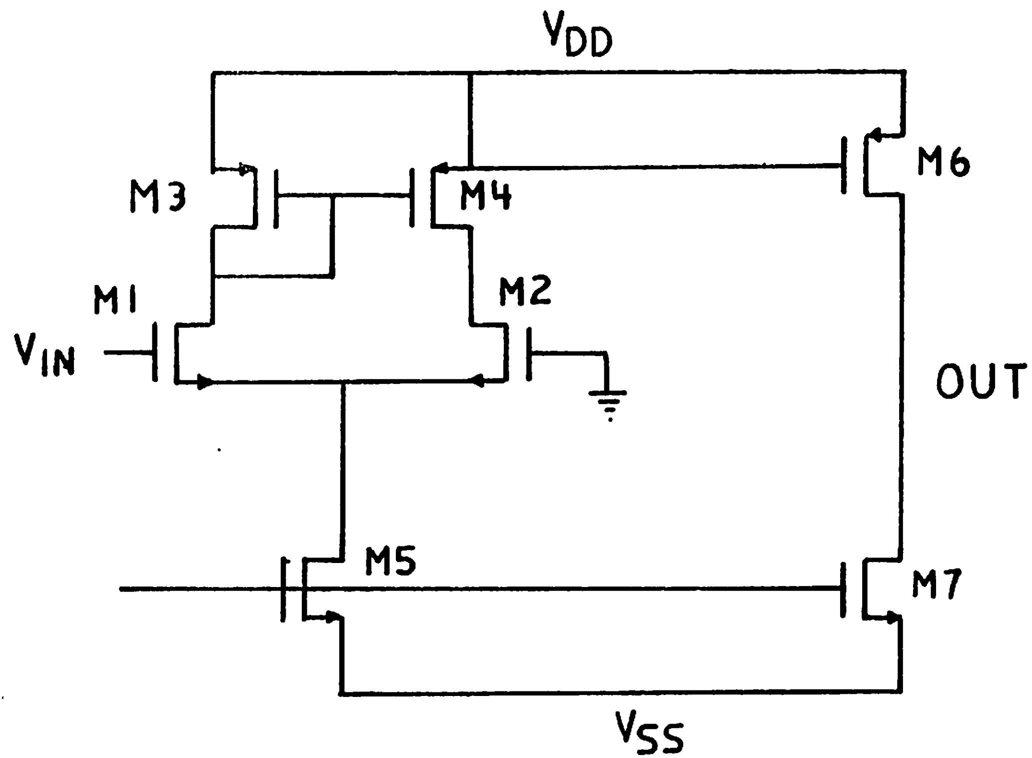


FIG. 4.1 BASIC 2-STAGE CMOS AMPLIFIER

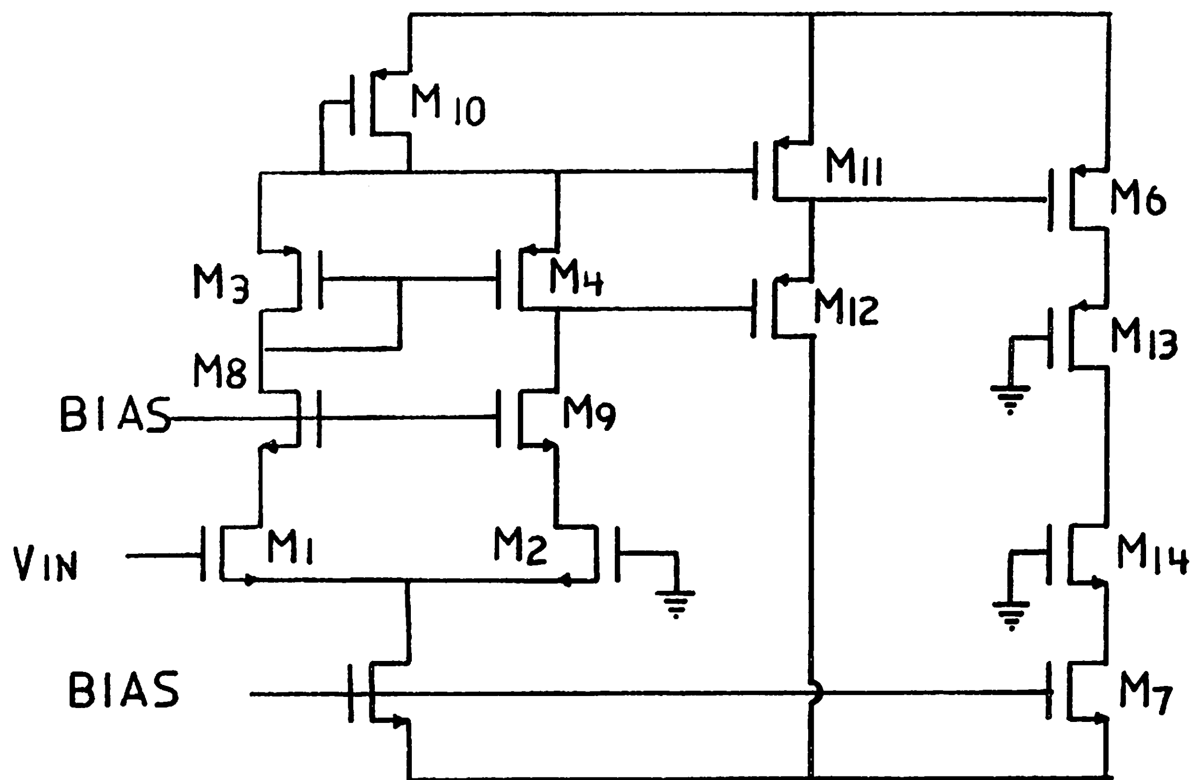
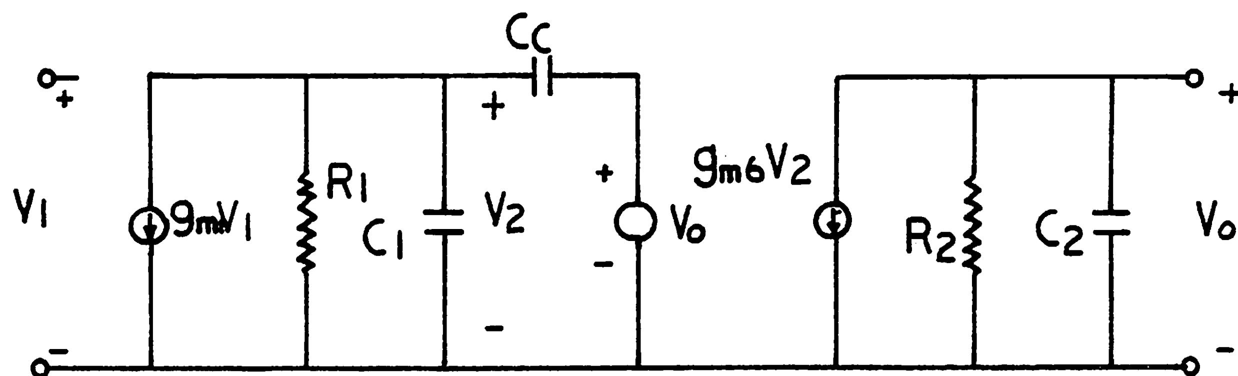
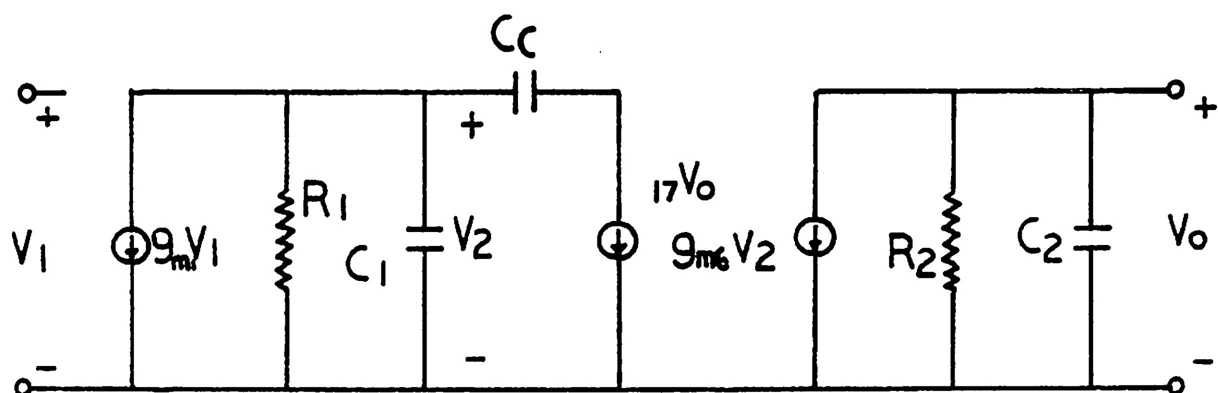


FIG.4.2 CASCODED 2-STAGE AMPLIFIER

FIG.4.3 FOLDED CASCODE AMPLIFIER

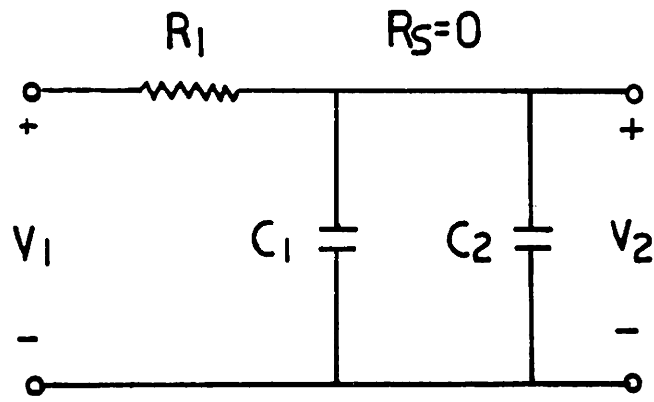


a)



b)

FIG.4.4 EQIVALENT CIRCUITS
a) WITH IDEAL BUFFER
b) WITH SOURCE FOLLOWER



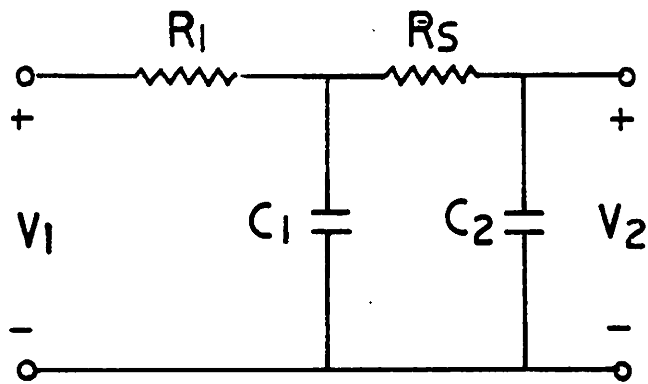


FIG.4.5 EQUIVALENT CIRCUITS
a) IDEAL SWITCH
b) NON-IDEAL SWITCH

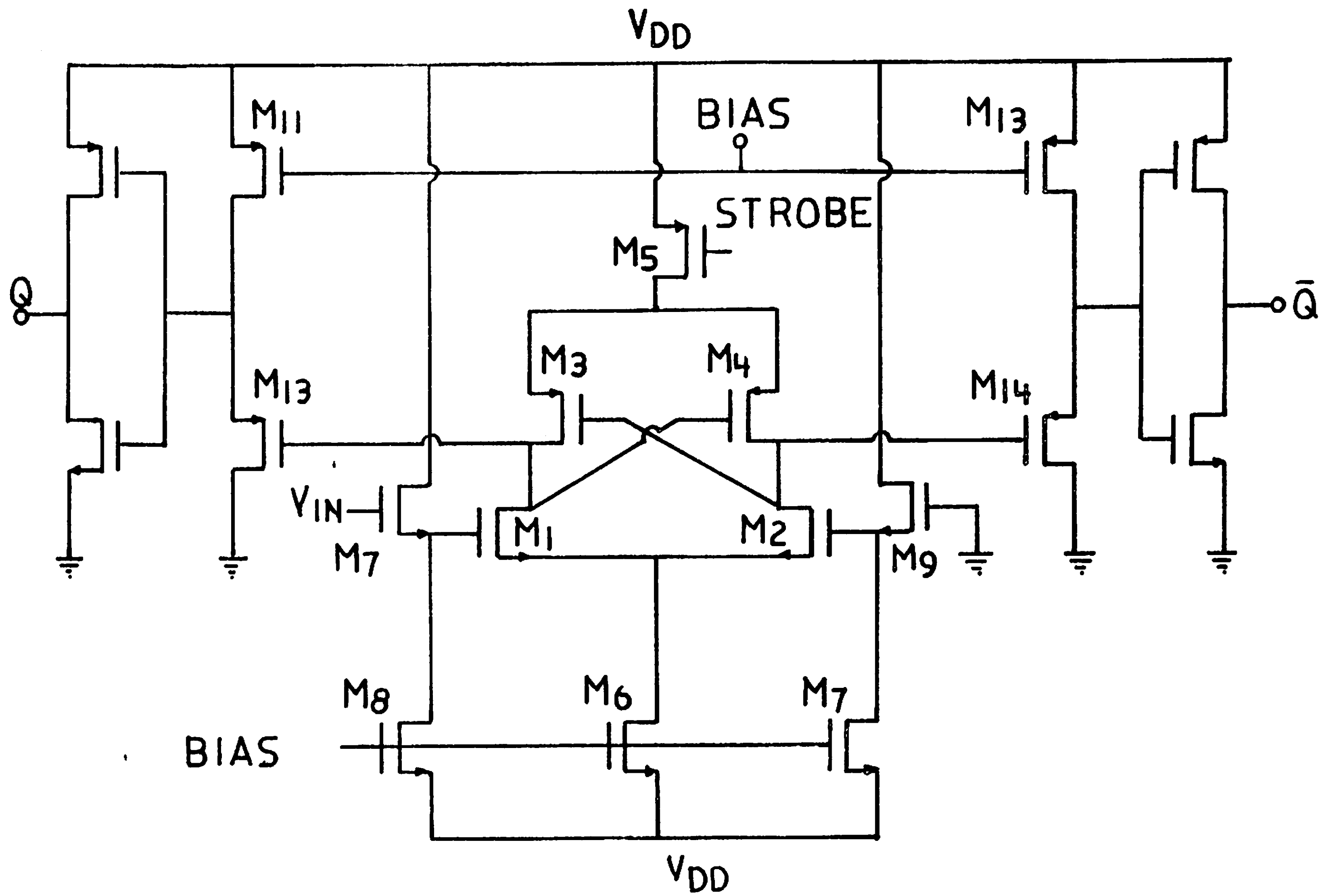


FIG. 4.6 SCHEMATIC DIAGRAM OF LATCH

Simulated Amplifier Performance		
Supply Voltage	± 5	V
Die Area	1000	mil^2
Open Loop Voltage Gain	100	dB
Power Dissipation	7	mW
CMRR	86	dB
PSRR	>80	dB
RMS Input Refered Noise	20	μV
Delay to 400 mV Output		
80 μV Input after Sat.	300	ns
20 μV Input after 2.5 mV	400	ns
Unity-gain Bnadwidth	3.9	MHz
Phase Margin	60	°
Load Capability	120	pF
Slew Rate	2	V/μs
0.1 % Settling Time, 100 mV Input	1.5	μs

Table 4.1 Simulated Amplifier Performance

	W (μm)	L (μm)	I_D (μA)		W (μm)	L (μm)	I_D (μA)
M1	500	6	100	M11	60	6	100
M2	500	6	100	M12	30	6	100
M3	60	6	100	M13	60	6	200
M4	60	6	100	M14	50	6	200
M5	120	6	200	M15	100	6	200
M6	120	6	200	M16	100	6	200
M7	100	6	200	M17	40	6	67
M8	50	6	100	M18	40	6	67
M9	50	6	100	M19	120	6	0
M10	120	6	200	M20	15	6	0

Table 4.2 Dimensions and Drain Currents of Transistors

Simulated Latch Performnace		
Supply Voltage	± 5	V
Power Dissipation	7	mW
Minimum Input Signal	< 100	mV
Delay Time		
No Load	50	ns
30 pF Load	100	ns

Table 4.3 Simulated Latch Performance

	W (μm)	L (μm)		W (μm)	L (μm)
M1	15	6	M11	60	6
M2	15	6	M12	15	6
M3	30	6	M13	15	6
M4	30	6	M14	15	6
M5	120	6	M15	15	6

Table 4.4 Dimensions of Transistors in Latch

CHAPER 5

CMOS CONTROL and SEQUENCING CIRCUITS

The CMOS control and sequencing circuits are described here, assuming the integration of a complete 16 bit converter including all the necessary logic circuits for calibration.

The schematic diagram of the entire circuit is shown in Fig. 5.1. The analog portion of the circuit is slightly different from the experimental chip that will be discussed in Chapter 8. Instead of 15 bit plus sign resolution of the experimental chip, this circuit is designed for 16 bit single polarity conversion. The reason for this is so that a single reference voltage may be used, and to avoid the need for the complementary switch associated with the double reference voltage.

Whether to use positive reference voltage or negative reference voltage should be determined considering the input voltage requirement and any process restrictions. For example, if the input voltage ranges between 0 V and assumed positive V_{ref}, it would be wise to use positive reference voltage and p-channel switches. The use of n-channel switches would restrict the input voltage range and the reference voltage to about a few volts below the positive power supply due to $V_{GS}-V_T$ requirement, limiting the dynamic range. A p-channel switch, however, can switch any positive voltage between 0V and V_{ref}. Hence, the reference voltage and the input voltage can be very close to the positive power supply voltage.

For the n-well CMOS process, it is not very efficient to use p-channel switches since they must be placed inside a well, and occupy considerably more die area than n-channel switches. In addition, p-channel transistors generally

have lower g_m constants than n-channel transistors, which in turn requires larger devices to provide same ON-resistance as n-channel transistors. Thus, if possible, it is better to use negative input and reference voltages and employ n-channel switches.

In the block diagram of Fig. 5.1, data selector switches are located between the SAR and the ROM. During the calibration cycle, these selectors are switched to the ROM. The ROM contains code for the appropriate switching of the capacitor array for the measurement of the residual voltages. For the calibration of all 10 capacitors, a 20 × 10 bit ROM is needed. Generally it will not be necessary to calibrate all 10 capacitors. If 5 MSB capacitors are to be calibrated, 10 × 5 bit ROM will be used. The content of the ROM for the calibration of all 10 capacitors is shown in Fig. 5.2. The address of the ROM should be incremented each time after the measurement of the residual voltage, allowing the measurement of the residual voltage of the succeeding bit.

The same function can be realized with two shift registers and data selectors as shown in Fig. 5.3. Whichever takes less die area should be selected, and this can be determined by die area estimation from standard logic cells.

The SAR for the lower 8 bits is shared between the sub DAC and the calibration DAC through the data selector. During the calibration cycle, the SAR is combined with the calibration DAC to digitize the residual voltages. During this time, the sub DAC is not needed. During the normal conversion, the SAR is coupled with the sub DAC for LSB conversions. Data from the accumulator is sent to the calibration DAC, and SAR is not needed for the calibration DAC during this time.

The 12 bit shift register and 12 bit full adder carry out the computation of the correction terms from the residual voltages. Since the output code from the calibration are encoded in 2's complement form, the necessary operation for computing the correction terms from the residual voltages is simple addi-

tions and shift to the right, which is realized by the shift register and the adder. 12 bit internal resolution is used to process 8 bit residual voltages to minimize truncation error.

The same shift register and the adder used to compute correction terms are used as an accumulator during the normal conversion to perform necessary operation to cancel the linearity error as was described in Chapter 3. Whether to keep the data from the RAM in the accumulator is determined by the present bit value. The RAM address is incremented after every bit decision to call the correction term corresponding to the next bit.

The sequence generator produces various signals needed for the calibration and conversion. The schematic diagram of the sequence generator is shown in Fig. 5.4.

RESET is a master reset signal which clears all the flip-flops and initiates the calibration cycle.

CAL is a status signal which determines the current status of the converter. During the calibration cycle, CAL=1, and otherwise CAL=0.

TOP signal turns the large switch on between the top plate of the capacitors and ground for the rapid discharge of the top plate charge.

SAMPLE signal turns on the small switch around the amplifier to cancel the offset voltage during the precharge cycle.

STROBE is a delayed clock which activates the latch.

START initiates the successive approximation search in both the calibration cycle and the normal conversion cycle.

QCC is a 'conversion complete' signal

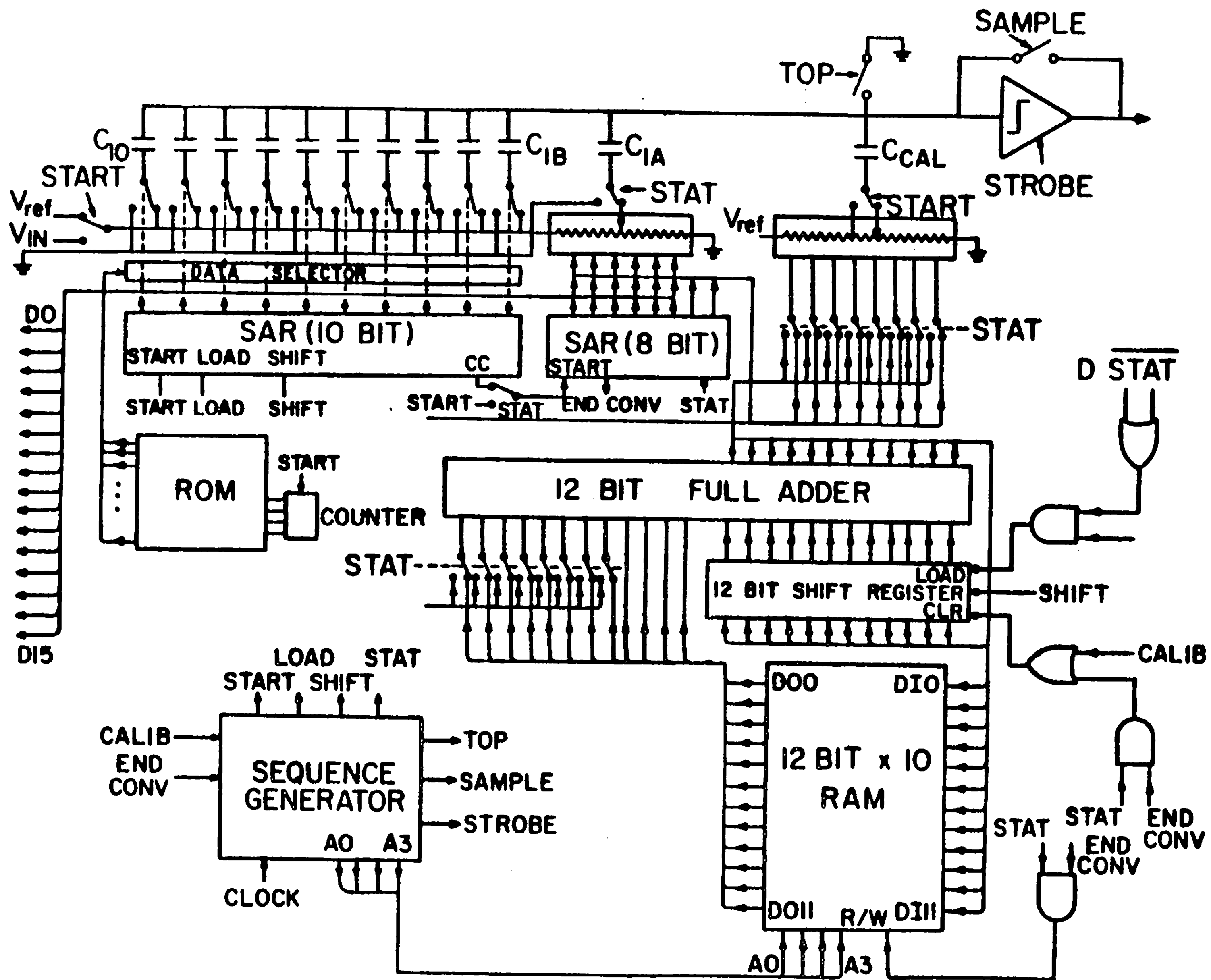


FIG 5.1 SCHEMATIC DIAGRAM OF CONVERTER

A_0	0	1	1	1	1	1	1	1	1	1	1
A_1	1	0	0	0	0	0	0	0	0	0	0
A_2	0	0	1	1	1	1	1	1	1	1	1
A_3	0	1	0	0	0	0	0	0	0	0	0
A_4	0	0	0	1	1	1	1	1	1	1	1
A_5	0	0	1	0	0	0	0	0	0	0	0
A_6	0	0	0	0	1	1	1	1	1	1	1
A_7	0	0	0	1	0	0	0	0	0	0	0
A_8	0	0	0	0	0	1	1	1	1	1	1
A_9	0	0	0	0	1	0	0	0	0	0	0
A_{10}	0	0	0	0	0	0	1	1	1	1	1
A_{11}	0	0	0	0	0	1	0	0	0	0	0
A_{12}	0	0	0	0	0	0	0	1	1	1	1
A_{13}	0	0	0	0	0	0	1	0	0	0	0
A_{14}	0	0	0	0	0	0	0	0	1	1	1
A_{15}	0	0	0	0	0	0	0	1	0	0	0
A_{16}	0	0	0	0	0	0	0	0	0	1	1
A_{17}	0	0	0	0	0	0	0	0	1	0	0
A_{18}	0	0	0	0	0	0	0	0	0	0	1
A_{19}	0	0	0	0	0	0	0	0	0	1	0

Fig. 5.2 ROM Table for 10-bit Calibration

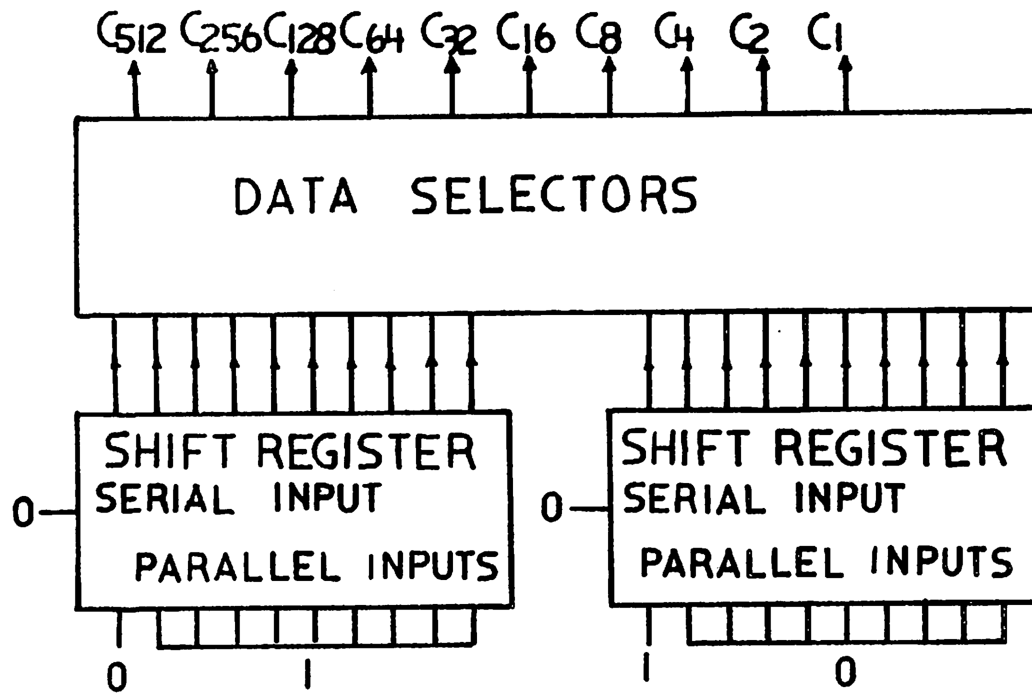


FIG. 5.3 ALTERNATIVE WAY OF CALIBRATION SWITCHING

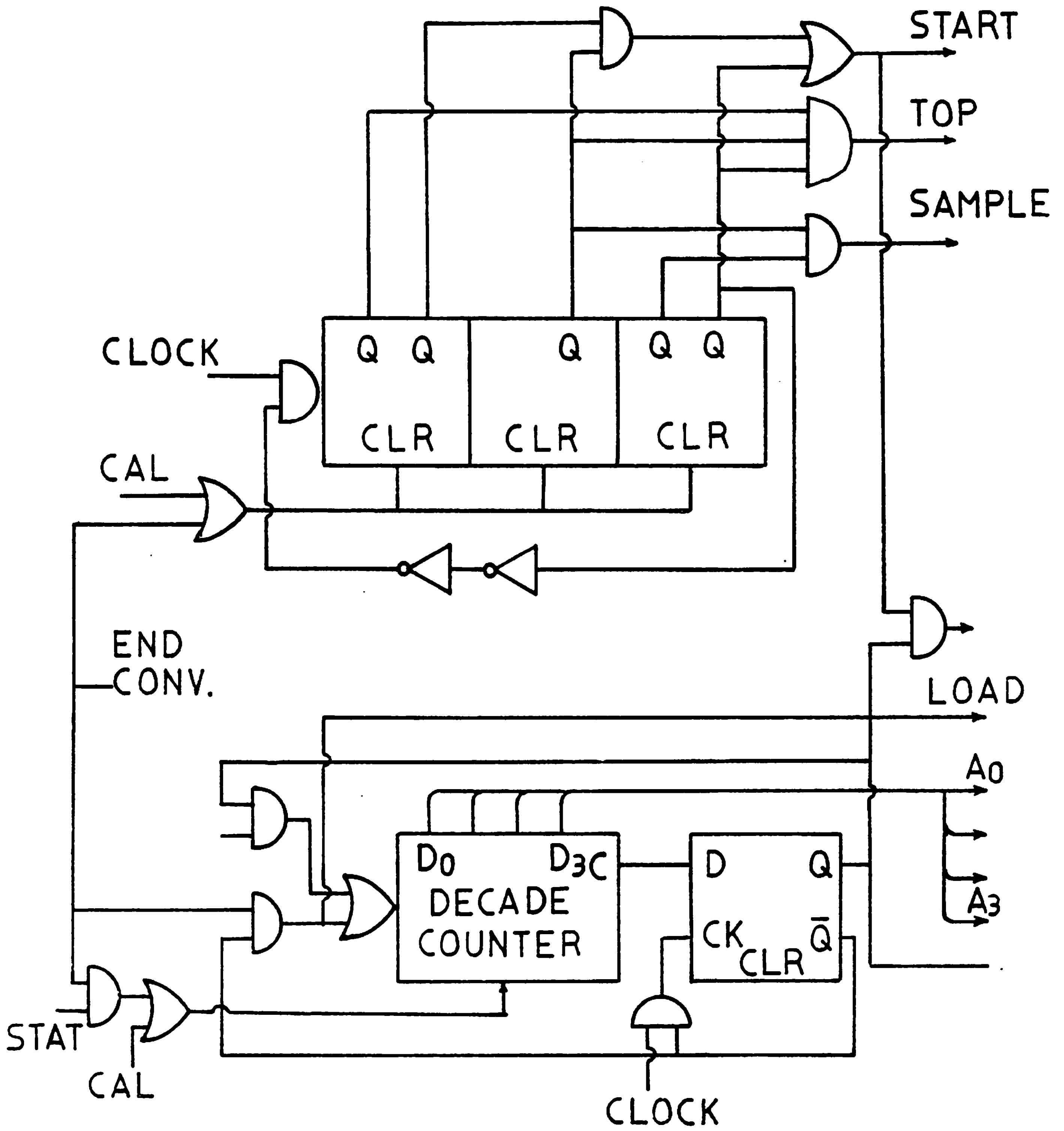


FIG. 5.4 SEQUENCE GENERATOR

CHAPTER 6

ACCURACY CONSIDERATIONS

There are various factors that can affect the performance of the self-calibrating A/D converter. In the following sections, effects of these factors and techniques to reduce problems arising from these factors are discussed [17].

6.1. Residual Offset Voltage

Although the offset voltage of the comparator is sampled in the capacitor array during the input acquisition phase, there is some residual offset voltage due to the charge injection from the feedback switch. This point is illustrated in Fig 6.1. When the switch M1 is turned on, the top plate of the capacitor array C_{TOT} is charged to the offset voltage V_{OS} of the comparator. When M1 is turned off, part of the channel charge is injected to the capacitor. This charge appears as an offset voltage of the comparator, and referred to as a ***residual offset voltage***. This residual offset voltage ΔV is a function of various parameters. The relationship between the injected charge and the slope of the clock applied to the gate is not well established. However, in the two extreme cases, fast slope (~10ns falling time) case and slow slope (~1 μs falling time) case, an approximate calculation is possible for the injected charge. In the slow slope case, all the channel charge goes to the output of the amplifier. Thus, there will be no error due to the channel charge injection. The error in sampled voltage will solely be due to the overlap capacitance.

$$\Delta V_{OL} = \frac{C_{OL}}{C_{TOT}}(V_H - V_L) \tag{6.1}$$

where C_L is the overlap capacitance of M1, V_H and V_L are logic 'high' and 'low' voltages applied to the gate of M1 respectively.

In the fast slope case, approximately half of the channel charge goes to the output of the amplifier, and the other half to the capacitor. Thus, there will be an additional error due to the channel charge injection. The channel charge Q_C in M1 is :

$$Q_C = -WLC_{OX}(V_H - V_{TH}) \tag{6.2}$$

where W and L are gate length and width of M1 respectively, and C_{OX} is unit gate capacitance, and V_{TH} is the threshold voltage. Therefore, the voltage error due to the charge injection is :

$$\Delta V_{ch} = \frac{Q_C}{2} \frac{1}{C_{TOT}} \tag{6.3}$$

Combined with the error due to the overlap capacitance, the total voltage error in the fast slope case is then :

$$\Delta V_{TOTAL} = -\frac{C_{OL}}{C_{TOT}}(V_{TH} - V_L) = \frac{WLC_{OX}}{2C_{TOT}}(V_H - V_{TH}) \tag{6.4}$$

As a numerical example assume the following numbers :

$V_H = +5V,\quad V_L = -5V,\quad V_{TH} = 1V$

$W = 15\mu m,\quad L = 6\mu m,\quad C_{OX} = .69\times10^{-15}F/\mu m^2$

$L_D = .35\mu m,\quad C_{TOT} = 120pF$

From these values, the voltage error can be calculated for the slow slope case and the fast slope case. The voltage error due to the overlap capacitance is

$180\,\mu V$, and the error due to the channel charge is $1.04\,mV$. Thus, the residual offset ranges from $180\,\mu V$ for the slow slope case, to $1.2\,mV$ for the fast slope case.

6.1.1. Effect of Residual Offset Voltage on Self-Calibration

The effect of the residual offset voltage on the ordinary A/D converter is nothing but an offset error that is equal to the residual offset voltage. However, the effect of the residual offset voltage on the self-calibrating A/D converter is a little more complicated. In short, the residual offset voltage will cause both offset error and gain error on the resulting converter. It should be noted that the residual offset voltage does not cause non-linearity.

In Chapter 3, it was shown that the correction terms $V_{\varepsilon n}$ can be expressed in terms of the residual voltages.

$$V_{\varepsilon N} = \frac{V_{XN}}{2} \tag{6.5}$$

$$V_{\varepsilon n} = \frac{1}{2}(V_{Xn} - \sum_{i=n+1}^{N} V_{\varepsilon i}), \quad n=1B,2,\ldots,N-1 \tag{6.6}$$

The last equation can be rewritten :

$$V_{\varepsilon n} = \frac{V_{Xn}}{2} - \sum_{i=1}^{N-n} \frac{V_{Xn+1}}{2^i}, \quad n=1B,2,\ldots,N-1 \tag{6.7}$$

In the presence of the residual offset voltage, the measured residual voltages are:

$$V_{Xi}^{*} = V_{Xi} - \Delta V \tag{6.8}$$

where V_{Xi}^{*} is the measured residual voltage, V_{Xi} is the actual residual voltage,

and ΔV is the residual offset voltage. The correction terms computed from these residual voltages are then :

$$
\begin{aligned}
V_{\varepsilon n}^{*} &= \frac{V_{Xn}^{*}}{2} - \sum_{i=1}^{N-n} \frac{V_{Xn+i}}{2^{i}} \\
&= \frac{V_{Xn}}{2} - \frac{\Delta V}{2} - \sum_{i=1}^{N-n} \frac{V_{Xn+i}}{2^{i}} \\
&= \frac{V_{Xn}}{2} - \sum_{i=1}^{N-n} \frac{V_{Xn+i}}{2^{i}} - \frac{\Delta V}{2^{N-n+1}} \\
&= V_{\varepsilon n} - \frac{\Delta V}{2^{N-n+1}} \qquad (6.9)
\end{aligned}
$$

Therefore, the correction terms $V_{\varepsilon n}^{*}$ computed from the measured residual voltages are different from the actual error voltages $V_{\varepsilon n}$ by $\frac{\Delta V}{2} \frac{1}{2^{N-n}}$

To see the effect of this error to the A/D conversion, consider the D/A converter model again.

$$
\begin{aligned}
V_{o,ideal} &= V_{o,actual} - \sum_{i=1}^{N} D_i V_{\varepsilon i} \\
&= \frac{V_{ref}}{2^{N}} \sum_{i=1B}^{N} 2^{i-1} D_i \qquad (6.10)
\end{aligned}
$$

with $V_{\varepsilon i}^{*}$ instead of $V_{\varepsilon i}$.

$$
\begin{aligned}
V_{o}^{*} &= V_{o,actual} - \sum_{i=1B}^{N} D_i V_{\varepsilon i}^{*} \\
&= V_{o,actual} - \sum_{i=1B}^{N} D_i V_{\varepsilon i} + \frac{\Delta V}{2} \sum_{i=1B}^{N} \frac{D_i}{2^{N-i}} \\
&= V_{o,ideal} + \frac{\Delta V}{2} \sum_{i=1B}^{N} \frac{D_i}{2^{N-i}} \\
&= \frac{V_{ref}}{2^{N}} \left(1 + \frac{\Delta V}{V_{ref}} \right) \sum_{i=1B}^{N} 2^{i-1} D_i \qquad (6.11)
\end{aligned}
$$

From the last equation, it can be seen readily that the output voltage of the DAC after the calibration using V_{ci}^{*} is different from the ideal output voltage by the factor of $\left(1+\frac{\Delta V}{V_{ref}}\right)$. Thus, the only effect of the residual offset voltage in self-calibrating DAC is the small gain error.

However, for an A/D converter, the residual offset voltage also causes an offset error of ΔV. This can be easily understood by recalling that offset voltage of the comparator gives offset error to the resulting A/D converter.

The alteration of the transfer characteristic by the residual offset voltage is indicated in Fig. 6.2. Due to the gain error and the offset error, the transfer curve is pivoted around the full scale.

6.1.2. Measurement of the Residual Offset Voltage.

The residual offset voltage can be measured by the calibration DAC. In Fig 6.3, the offset voltage of the comparator V_{OS} is sampled on the capacitor array to counterbalance the offset voltage. After the switch S1 is turned off the residual offset voltage ΔV will be added on the capacitor array. This voltage can be digitized using the sub DAC and the SAR.

6.1.3. Residual Offset Cancellation : Technique I

This technique is very simple, and requires little modification on the basic self-calibration technique. Consider the flow chart of Fig. 6.4 for the self-calibrating A/D converter in normal conversion mode. Instead of resetting the accumulator before the first bit is tested, digital equivalent of ΔV is loaded in

the accumulator. This causes an additional voltage ΔV to be added to the accumulated correction term, and in turn subtracts the ΔV from the top plate of the capacitor. Actually, the entire transfer curve is shifted by an amount of ΔV, which balances the residual offset voltage.

The gain error, however, is not corrected by this technique since nothing has been done to the offset voltage when the residual voltages are being measured during the calibration cycle. The transfer curve before and after the offset correction is shown in Fig. 6.5. In most of the applications, the gain error is of no importance, or the system gain can be adjusted elsewhere.

For the applications where accurate gain is needed, the gain error can also be corrected by another technique which is described in the following section.

6.1.4. Residual Offset Cancellation : Technique II

Due to charge injection from the MOS transistor, there is an offset of ΔV, whenever a voltage is measured by the comparator. This is also true during the measurement of V_X's. As was discussed in Section 6.1.1, this causes a gain error.

By applying $-\Delta V$ through the calibration DAC during every measurement, the residual offset can be cancelled. This operation is illustrated in Fig. 6.6. When the reference voltage is sampled on the complement capacitors of a bit, the calibration DAC code is switched to the digital equivalent of ΔV. After the top plate switch is turned off and the bottom plate voltages are exchanged, the calibration DAC code is brought back to 0. The net result is to subtract ΔV from the top plate voltage, which precisely cancels the residual offset ΔV. Thus, no offset is introduced during the measurement of the residual voltages and the gain error vanishes.

The offset error which occurs when the input voltage V_{in} is sampled is not corrected this way. A similar thing can be done when input voltage is sampled. When the top plate switch is turned on to sample the input voltage, the calibration DAC is switched to digital equivalent of ΔV just the same way it was done during residual voltage measurement. After the top plate switch is turned off, the calibration DAC code is switched back to 0 to cancel the offset.

Alternatively, technique I can be used to correct this offset error.

6.2. Coupling Capacitor Error

If the capacitor C_{1A} coupling the main DAC and the sub DAC deviates from the nominal value, non-linearity can occur. To see the effect of the non-ideal coupling capacitor, assume that every capacitors are ideal except for the coupling capacitor C_{1A}. In other words,

$$C_i = C \quad i = 1B,2,\ldots,N$$

$$C_{1A} = C(1+\varepsilon_{1A})$$

It can be readily seen that between the sub DAC code all 0's and all 1's, the step size will be different from the ideal value by a factor of $(1+\varepsilon_{1A})$. This error is non-significant because it contributes only ε_{1A} LSB differential non-linearity.

However, when the sub DAC code switches from all 1's to all 0's, the non-linearity will be much larger. The step size at this point is :

$$V_s = V_{ref}\left[\frac{C}{C_{TOT}} - \frac{2^M-1}{2^M}\frac{C_{1A}}{C_{TOT}}\right] \tag{6.12}$$

Neglecting the term $\frac{\varepsilon_{1A}}{2^{M+N}}V_{ref}$:

$$= \frac{V_{ref}}{2^N}\left(\frac{1}{2^M} - \varepsilon_{1A}\right) \qquad (6.13)$$

The differential non-linearity at this point is then :

$$V_s = V_s - \frac{V_{ref}}{2^{M+N}}$$

$$= \frac{\varepsilon_{1A}}{2^N} V_{ref} \qquad (6.14)$$

For this error to be less than ½ LSB :

$$\frac{\varepsilon_{1A}}{2^N} V_{ref} < \frac{V_{ref}}{2^{M+N+1}}$$

or

$$\varepsilon_{1A} < \frac{1}{2^{M+1}} \qquad (6.15)$$

It shows that the ratio error of the coupling capacitor C_{1A} should be less than $\frac{1}{2^{M+1}}$ to ensure the linearity of the resulting converter. For example, less than 1.5% ratio error is needed for a 15 bit plus sign experimental converter with 5 bit sub DAC (M=5). The size of the unit capacitor of the main DAC was determined by the linearity requirement of the main DAC and the matching property of the MOS capacitors [5]. 18 μm by 18 μm unit capacitors were used. With these unit capacitors, and with a careful layout, less than 1.5% ratio error in C_{1A} can be achieved. To prevent any systematic error in C_{1A} due to oxide thickness gradient or non-uniform undercut of the polysilicon top plate, C_{1A} should be located near the center of the array.

By assigning appropriate number of bits to the main DAC and the sub DAC, all the constraints on the main DAC linearity and the coupling capacitor ratio error can be satisfied. For the following analysis, assume that all the ratio errors are randomly distributed.

Define following variables :

N : *number of bits on the main DAC*

M : *number of bits on the sub DAC*

σ_{2^i} : *standard deviation of* $\frac{\Delta C_{2^i}}{C_{TOT}}$

σ_{2^i}' : *standard deviation of* $\frac{\Delta C_{2^i}}{C_{2^i}}$

For the main DAC to be accurate to ½ LSB of its own resolution, it is required that :

$$3\sigma_{2^{N-1}} < \frac{1}{2^{N+1}} \tag{6.16}$$

Here, it is assumed that the maximum ratio error occurs in the largest capacitor, and 3 σ point was taken. Then referring to the unit capacitor C_1 :

$$3\sigma_1 < \frac{1}{2^{\frac{N-1}{2}}} \frac{1}{2^{N+1}} \tag{6.17}$$

Since $C_{TOT} = 2^N C$,

$$\sigma_1 = \sigma' \frac{1}{2^N} \tag{6.18}$$

Thus :

$$3\sigma_1' < \frac{1}{2^{\frac{N-1}{2}}} \tag{6.19}$$

Then if

$$\frac{1}{2^{\frac{N-1}{2}}} < \frac{1}{2^{M+1}} \tag{6.20}$$

it is guaranteed that the linearity error due to C_{1A} is less than ½ LSB at M+N bit level. Taking the logarithm of both sides :

$$\frac{N-1}{2} < M \tag{6.21}$$

For a 15 bit plus sign converter, $M+N=15$, and the best selection will be N=10 and M=5, since it is better to assign as many bits as possible on the capacitor array main DAC which has superior linearity to the resistor string sub DAC.

If this requirement cannot be met, non-linearity can occur. However, this non-linearity can easily be corrected by the extension of the calibration to the sub DAC as well.

6.2.1. Correction of the Coupling Capacitor Error

The error in the coupling capacitor can be interpreted as a gain error in the sub DAC. If the coupling capacitor C_{1A} is off by a factor of $(1+\varepsilon_{1A})$, it is equivalent to the sub DAC having a gain error of the same factor. Thus :

$$V_{error,sub} = \left[\frac{C_{1A}}{C_{TOT}} - \frac{C}{C_{TOT}}\right] V_{o,sub} \tag{6.22}$$

where $V_{error,sub}$: sub DAC correction term $V_{o,sub}$: sub DAC output voltage

Again, assuming $C_{1A} = (1+\varepsilon_{1A})$ and from the definition $C = \frac{C_{TOT}}{2^N}$:

$$V_{error,sub} = \frac{\varepsilon_{1A}}{2^N} V_{o,sub} \tag{6.23}$$

Also, for the sub DAC :

$$V_{o,sub} = \sum_{i=1}^{M} D_{i,sub} \frac{2^{i-1}}{2^M} V_{ref} \tag{6.24}$$

where $D_{i,sub}$ is the i-th sub DAC code. Combining these two equations :

$$V_{error,sub} = \frac{\varepsilon_{1A}}{2^N} \sum_{1}^{M} \frac{2^{j-1}}{2^M} D_{j,sub} V_{ref} \tag{6.25}$$

Since $\sum_{i=1A}^{N} \frac{2^{i-1}}{2^N} \varepsilon_i = 0$:

$$\frac{\varepsilon_{1A}}{2^N} = -\sum_{i=1B}^{N} \frac{2^{i-1}}{2^N} \varepsilon_i V_{ref} \tag{6.26}$$

or

$$\begin{aligned} \frac{\varepsilon_{1A}}{2^N} V_{ref} &= -\sum_{i=1B}^{N} \frac{2^{i-1}}{2^N} \varepsilon_i V_{ref} \\ &= -\sum_{i=1B}^{N} V_{\varepsilon i} \\ &= V_{\varepsilon 1A} \end{aligned} \tag{6.27}$$

From this equation, it is shown that $V_{\varepsilon 1A}$ can be easily computed from $V_{\varepsilon 1B}$ to $V_{\varepsilon N}$. These are already computed during the basic calibration.

Defining :

$$V_{\varepsilon j,sub} = -V_{\varepsilon 1A} \frac{2^{j-1}}{2^M} \tag{6.28}$$

Then :

$$V_{error,sub} = \sum_{j=1}^{M} V_{\varepsilon j,sub} D_{j;sub} \tag{6.29}$$

This is exactly the same expression as the correction term for the main DAC except that the subscripts are those of the sub DAC. Thus, after computing the correction terms $V_{\varepsilon j,sub}$, they can be stored in the RAM in the same manner as the main DAC correction terms. During the normal conversion, the same algorithm that was used to cancel the main DAC error can be extended to the sub DAC. This requires no hardware modification but more memory locations for storing the sub DAC correction terms.

It should be noted that the sub DAC correction terms $V_{\varepsilon j,sub}$'s can be very easily computed by simply shifting digitized $-V_{\varepsilon 1A}$ progressively to the right.

$$V_{\varepsilon 1,sub} = -\frac{V_{\varepsilon 1A}}{2} \tag{6.30}$$

$$V_{\varepsilon 2,sub} = \frac{V_{\varepsilon 1,sub}}{2} \tag{6.31}$$

$$\cdot$$
$$\cdot$$
$$\cdot$$

$$V_{\varepsilon j,sub} = \frac{V_{\varepsilon j-1,sub}}{2} \tag{6.32}$$

6.3. Voltage Coefficient of Capacitors

Non-zero voltage coefficient of the capacitors results in error in the sampled charge. The overall effect of the voltage coefficient of the capacitors is a "bowed" transfer characteristic (Fig. 6.7) [18]. The maximum integral non-linearity occurs near the center of the curve. If the voltage coefficients of all the capacitors are equal, they do not contribute to differential non-linearity. However, it is possible to have a gradient in the bottom plate doping concentration. In this case, voltage coefficients of individual capacitors will be different from that of each other, and differential non-linearity will occur. In the following two sections, these effects are dealt with separately.

6.3.1. Effect of Uniform Voltage Coefficient

To see this effect, consider an ideally matched capacitor array DAC. The voltage coefficients of the capacitors are assumed to be identical.

Define following quantities :

α *: voltage coefficient of the capacitors*

C_o *: sampled charge*

C_e *: final charge*

$C_i(0)$ *: value of* C_i *at 0V bias*

$C_{TOT}(0)$ *: value of* C_{TOT} *at 0V bias*

Then :

$$Q_o = -\int_0^{V_{IN}} C_{TOT}(0)(1+\alpha V)dV = -C_{TOT}(0)\,V_{IN}(1+\alpha\frac{V_{IN}}{2}) \tag{6.33}$$

At the end of the conversion, the voltage on the top plate of the capacitor array is brought back to ground. Then the final charge in the capacitor is :

$$Q_e = -\int_0^{V_{ref}} \sum_{i=1B}^{N} C_i(0)(1+\alpha V)D_i dV$$

$$= -(1+\alpha\frac{V_{ref}}{2})V_{ref}\sum_{i=1B}^{N} C_{i(0)}D_i \tag{6.34}$$

The charge balance equation is :

$$Q_o = Q_e \tag{6.35}$$

or

$$C_{TOT}(0)\,V_{IN}(1+\alpha\frac{V_{IN}}{2}) = (1+\alpha\frac{V_{ref}}{2})V_{ref}\sum_{i=1B}^{N} C_i(0)D_i \tag{6.36}$$

Rewriting the last equation:

$$\frac{1+\alpha\frac{V_{IN}}{2}}{1+\alpha\frac{V_{ref}}{2}}C_{TOT}(0)\,V_{IN} = \sum_{i=1B}^{N} D_i C_i(0)\,V_{ref} \tag{6.37}$$

This equation is different from the ideal charge balance equation by an input dependent factor of $\frac{1+\alpha\frac{V_{ref}}{2}}{1+\alpha\frac{V_{ref}}{2}}$. In terms of voltage, the integral non-linearity is

then :

$$IN = \frac{1+\alpha\frac{V_{IN}}{2}}{1+\alpha\frac{V_{ref}}{2}}V_{IN} - V_{IN}$$

$$= \frac{\alpha\frac{V_{IN}}{2}(V_{IN}-V_{ref})}{1+\alpha\frac{V_{ref}}{2}} \qquad (6.38)$$

This quadratic error gives rise to the "bowed" characteristic. Differentiating the integral non-linearity with respect to the input voltage, maximum non-linearity can be calculated :

$$\max(IN) = \frac{\alpha\frac{V_{ref}^2}{8}}{1+\alpha\frac{V_{ref}}{2}} \qquad (6.39)$$

at $V_{IN} = \frac{V_{ref}}{2}$.

6.3.2. Effect of Differential Voltage Coefficient

Due to non-uniform doping of the top plate as well as the bottom plate of the capacitors, the voltage coefficients of each capacitor may be different. Suppose each bit capacitor has a voltage coefficient of α_i and the weighted average of the voltage coefficient of all the capacitors is zero.

$$C_i(V) = C_{i(0)}(1+\alpha_i V) \qquad (6.40)$$

$$C_{TOT}(V) = \sum_{i=1B}^{N} C_i(V)$$

$$= \sum_{i=1B}^{N} C_i(0)(1+\alpha_i V) \qquad (6.41)$$

$$= C_{TOT}(0) \qquad (6.42)$$

The last equality is true because the weighted average of the voltage coefficients is zero. Then again, sampled charge is :

$$Q_o = -\int_{V_{IN}}^{0} C_{TOT}(V)dV$$

$$= -C_{TOT}(0)\,V_{IN} \qquad (6.43)$$

And after the successive approximation search :

$$Q_e = -\int_{0}^{V_{ref}} \sum_{i=1B}^{N} D_i C_i(0)(1+\alpha_i V)dV$$

$$= \sum_{i=1B}^{N} D_i C_i(0)(1+\frac{\alpha_i}{2}V_{ref})\,V_{ref} \qquad (6.44)$$

Then the charge balance equation becomes

$$C_{TOT}(0)\,V_{IN} = \sum_{i=1B}^{N} D_i C_i(0)(1+\frac{\alpha_i}{2}V_{ref})\,V_{ref} \qquad (6.45)$$

Comparing this equation with the charge balance equation for the DAC with ratio mismatch (Equation 3.7), it can be noted that these equations are of the identical form if we set $\frac{\alpha_i}{2}V_{ref} = \varepsilon_i$. Therefore the differential voltage coefficient manifests itself as the ratio mismatch and causes differential non-linearity. Since the error factor $1+\frac{\alpha_i}{2}V_{ref}$ depends only on the V_{ref}, it is constant once the reference voltage is fixed. Hence, the differential voltage coefficient appears as ratio mismatch in calibration cycle as well since a fixed reference voltage V_{ref} or 0V is applied across the capacitors during the calibration. As a consequence, the differential voltage coefficient is automatically calibrated as a ratio mismatch by the basic calibration.

6.3.3. Measurement of the Voltage Coefficient

Measurement of the voltage coefficient of the capacitors requires a known input voltage, preferably half the reference voltage. The sequence is shown in Fig. 6.8.

The charge in the capacitor array when $\frac{V_{ref}}{2}$ is sampled is :

$$Q_o = \int_0^{\frac{V_{ref}}{2}} C_{TOT}(0)(1+\alpha V)dV \tag{6.46}$$

$$= C_{TOT}(0)(1+\alpha\frac{V_{ref}}{4})\frac{V_{ref}}{2} \tag{6.47}$$

Then, C_N is switched to the reference voltage and all the other capacitors are connected to the ground. At this time, the charge in the capacitor array is :

$$Q_{s1} = \int_0^{V_{ref}} C_N(0)(1+\alpha V)dV$$

$$= \frac{C_{TOT}(0)}{2}(1+\varepsilon_N)(1+\alpha\frac{V_{ref}}{2})V_{ref} \tag{6.48}$$

$$Q_{r1} = Q_{s1} - Q_o$$

$$= \frac{\alpha}{8}V_{ref}^2 C_{TOT}(0) + \frac{\varepsilon_N}{2}C_{TOT}(0)(1+\alpha\frac{V_{ref}}{2})V_{ref} \tag{6.49}$$

Or in terms of voltages

$$V_{r1} = \frac{\frac{\alpha}{8}V_{ref}^2 + \frac{\varepsilon_N}{2}(1+\alpha\frac{V_{ref}}{2})V_{ref}}{1+\alpha\frac{V_{ref}}{2}} \tag{6.50}$$

This residual voltage is digitized by the calibration DAC. Then the bottom plate voltages are exchanged between C_N and its complement. The residual voltage V_{r2} is:

$$V_{r2} = \frac{\frac{\alpha}{8}V_{ref}^2 - \frac{\varepsilon_N}{2}(1+\alpha\frac{V_{ref}}{2})V_{ref}}{1+\alpha\frac{V_{ref}}{2}} \tag{6.51}$$

This residual voltage is also digitized, and added to digitized V_{r1}.

$$V_{r1} + V_{r2} = \frac{\frac{\alpha}{4}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.52}$$

It should be noted that the ratio error term is cancelled by adding two residual voltages and only the term due to the voltage coefficient remains.

6.3.4. Improving Integral Linearity : Piecewise Linear Correction

Although the effect of the differential voltage coefficient is eliminated by the basic calibration, the uniform voltage coefficient still causes a bowed transfer characteristic. Intuitively, it would seem possible to compute the error and subtract it by the use of the calibration DAC. However, due to the quadratic nature of the error as shown in Equation 6.38, a digital multiplier is necessary to carry out this computation. This is not desirable because a digital multiplier will consume a large die area.

A piecewise linear correction is simpler, and only a small modification is needed on the basic hardware. A transfer characteristic with an exaggerated integral non-linearity due to the voltage coefficient and 2-section linear approximation of the curve is shown in Fig. 6.9a. The transfer characteristic after 2-section linear correction is shown in Fig. 6.9b. After the 2-section linear correction, the maximum integral non-linearity is reduced by a factor of 4 and occurs at the one and the three quarter points of the transfer curve.

To correct the piecewise linear approximated characteristic of Fig. 6.9a, the gain of the converter should be adjusted for the first half of the curve and

both the gain and offset should be adjusted for the second half. Adjusting the gain and offset of the converter can be easily performed by altering the correction terms.

By extrapolating the first half of the linear approximated curve, it is found that the gain for this half is too large and the voltage error at the end ($V_{IN} = V_{ref}$) of the curve is $\dfrac{\frac{\alpha}{4}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}}$. Since the first half of the curve corresponds to $D_N = 0$, following adjustment should be made on the correction terms to correct the gain when $D_N = 0$.

$$V'_{\varepsilon N} = V_{\varepsilon N} - \frac{\frac{\alpha}{8}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.53}$$

$$V'_{\varepsilon N-1} = V_{\varepsilon N-1} - \frac{\frac{\alpha}{16}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.54}$$

.

.

.

$$V'_{\varepsilon N-i} = V_{\varepsilon N-i} - \frac{\frac{\alpha}{2^{i+3}}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.55}$$

where $V'_{\varepsilon k}$'s are the correction terms after the adjustment and $V_{\varepsilon k}$'s are those before the adjustment.

The adjustment terms (the second terms on the right hand sides) can be computed by shifting digitized $\dfrac{\frac{\alpha}{8}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}}$ to the right successively.

For the second half of the curve, the gain adjustment is by the same amount but in the opposite direction to the first half, and an offset of

$-\frac{\frac{\alpha}{4}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}}$ should be added.

Adding the offset of the converter can be done by initially loading the accumulator with the offset voltage instead of clearing at the beginning of the conversion. Thus the adjustments for the second half ($D_N = 1$) are :

$$V_{os} = -\frac{\frac{\alpha}{4}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.56}$$

$$V'_{\epsilon N} = V_{\epsilon N} + \frac{\frac{\alpha}{8}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.57}$$

$$V'_{\epsilon N-1} = V_{\epsilon N-1} + \frac{\frac{\alpha}{16}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.58}$$

.

.

.

$$V'_{\epsilon N-i} = V_{\epsilon N-i} + \frac{\frac{\alpha}{2^{i+3}}V_{ref}^2}{1+\alpha\frac{V_{ref}}{2}} \tag{6.59}$$

Note that the adjustment made on the correction terms is in the opposite polarity to the first half.

The memory organization for this 2-section linear correction is shown in Fig. 6.10.

Although it is possible to use 4 or more section linear correction for added accuracy, it may not be worthwhile due to increased digital computation. The following section describes a technique that precisely corrects the quadratic curve without explicit multiplication.

For the verification of piecewise linear correction technique, a breadboard version of the self-calibrating A/D converter was built [19]. A large voltage coefficient was deliberately introduced by using reversed biased diodes as capacitors. Although the voltage dependence of reverse biased junction capacitance is different from that of MOS capacitance [20], a similar transfer curve was obtained. It was shown that the overall linearity was much improved after the 2-section linear correction.

6.3.5. Recursive Correction of Voltage Coefficient

A precise correction is possible by a recursive adjustment of the correction terms. In Section 6.3.1, the linearity error due to the voltage coefficient was shown to be :

$$IN = \frac{\frac{\alpha}{2} V_{IN} (V_{ref} - V_{IN})}{1 + \alpha \frac{V_{ref}}{2}} \tag{6.38}$$

Define V_n as a voltage applied by the ideally matched DAC. For example,

$$V_1 = \frac{V_{ref}}{2} \tag{6.60}$$

$$V_2 = \frac{V_{ref}}{4} \tag{6.61}$$

$$V_n = \sum_{i=1}^{n-1} D_i \frac{V_{ref}}{2^i} + \frac{V_{ref}}{2^n} \tag{6.62}$$

These are the voltages which are compared with V_{IN} during each bit test. In case of non-zero voltage coefficient, adjustment should be made to these voltages. In other words, a voltage :

$$V_{c,n} = -\frac{\alpha \frac{V_n}{2}(V_{ref} - V_{IN})}{1+\alpha \frac{V_{ref}}{2}} \tag{6.63}$$

should be added when testing the n-th bit.

Define $V_{f,n}$ as a voltage from the DAC after the bit decision is made, and $V_{cf,n}$, the correction voltage after the bit decision. Then :

$$\begin{aligned} V_{f,n} &= V_n \quad &: \text{if } D_n = 1 \\ &= V_{f,n-1} \quad &: \text{if } D_n = 0 \end{aligned} \tag{6.64}$$

Also :

$$V_{f,n} = \sum_{i=1}^{n} D_i \frac{V_{ref}}{2^i} \tag{6.65}$$

From Equation 6.62 and Equation 6.65 :

$$V_n = V_{f,n-1} + \frac{V_{ref}}{2^n} \tag{6.66}$$

Substituting Equation 6.66 into Equation 6.63 :

$$V_{c,n} = V_{cf,n-1} - \frac{\alpha \frac{V_{ref}^2}{2}}{1+\alpha \frac{V_{ref}}{2}}\left(\frac{1}{2^n} - \frac{1}{2^{2n}}\right) + \frac{\alpha \frac{V_{ref}^2}{2}}{1+\alpha \frac{V_{ref}}{2}} \sum_{i=1}^{n-1} D_i \frac{1}{2^i} \tag{6.67}$$

and

$$V_{cf,n} = V_{c,n} \quad : \text{if} D_n = 1$$
$$= V_{cf,n-1} \quad : \text{if} D_n = 0 \tag{6.68}$$

This algorithm can be implemented by full adders and registers as shown in Fig. 6.11.

6.4. Leakage Current

The leakage current from the junction connected to the top plate of the capacitor array can cause an error in A/D conversion. For the Berkeley CMOS process, the leakage current through a shallow n-channel source-drain junction at 5 V reverse bias was measured to be on the order of 1 nA/cm^2 at room temperature.

The voltage error due to the leakage current is :

$$\Delta V = \frac{I_L}{C_{TOT}} t \tag{6.69}$$

where I_L is the leakage current and t is the conversion time.

For the experimental chip, total junction area connected to the top plate of the capacitor is 3,000 μ^2. Thus at room temperature $I_L = .03pA$. Using $C_{TOT} = 120pF$, and $t = 20\mu s$,

$$\Delta V = .05\mu V$$

This is much less than ½ LSB at 16 bit level and can be neglected. By adapting widely used temperature dependence factor of $2^{\frac{T-25}{10}}$ [21], the leakage current at 125 °C is estimated to be 30 pA, and ΔV is approximately 50 μV, which is still less than ½ LSB at 16 bit level.

6.5. Dielectric Relaxation

The dielectric relaxation time for silicon dioxide is approximately 3000 s. Since the conversion time is much shorter than the dielectric relaxation time, this effect is negligible.

However, the effect of polarizable molecules in the dielectric can cause more serious problems [22-24]. This effect will cause a residual charge after the voltage is removed from the capacitor thus causing the linearity error in the converter. By a careful processing, polarizable molecules and mobile ions can be kept out. For the Berkeley CMOS process, the residual charge due to the polarization was measured to be less than 4 ppm of the original charge [25]. The precise measurement technique for the residual charge is described in Appendix II.

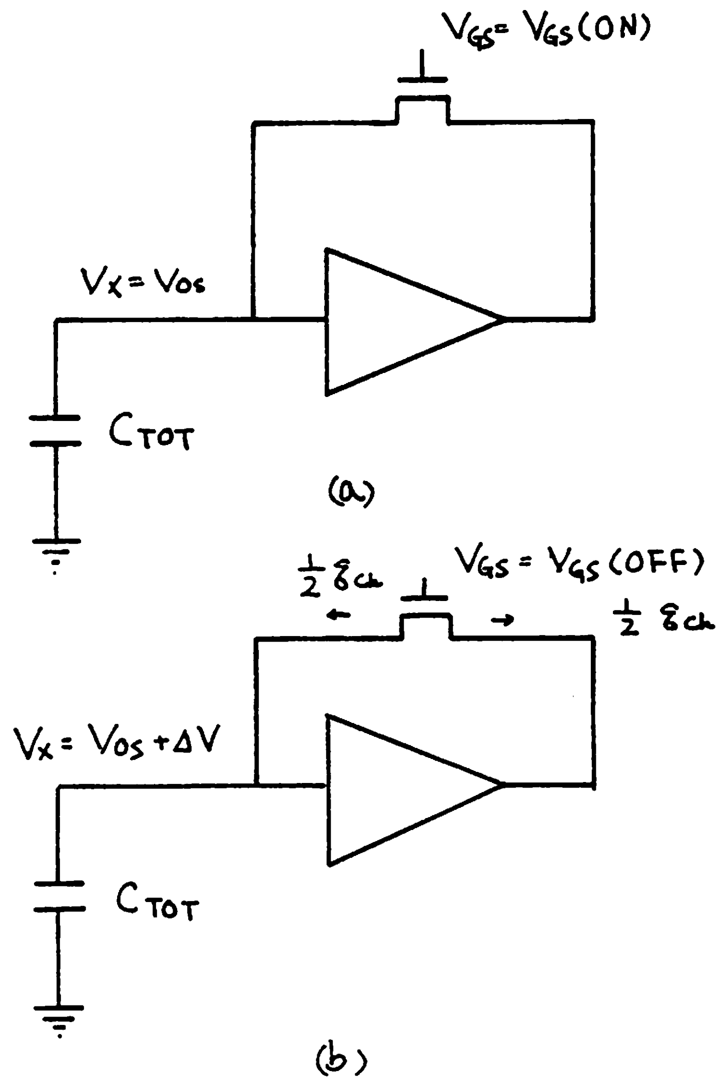


FIG. 6.1 RESIDUAL OFFSET VOLTAGE DUE TO CHARGE INJECTION

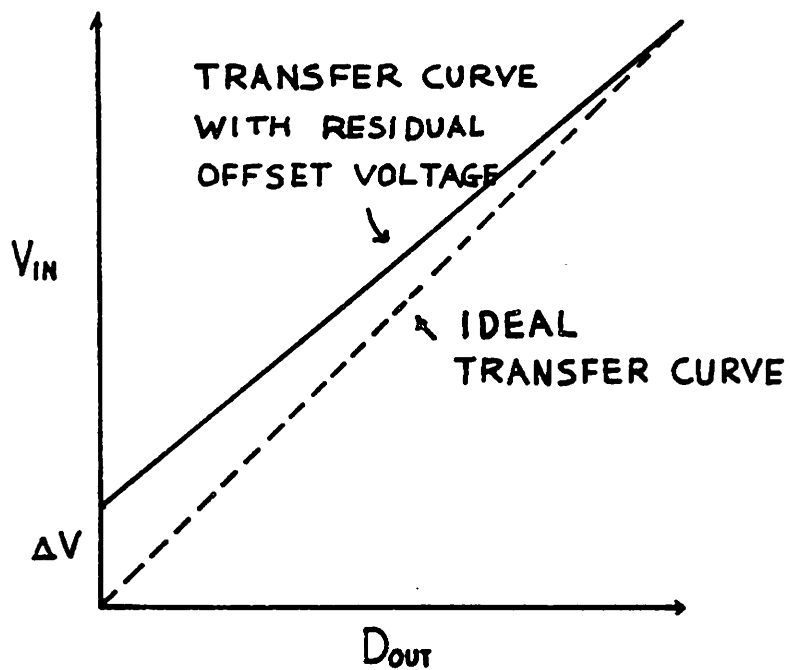


FIG. 6.2 EFFECT OF RESIDUAL OFFSET

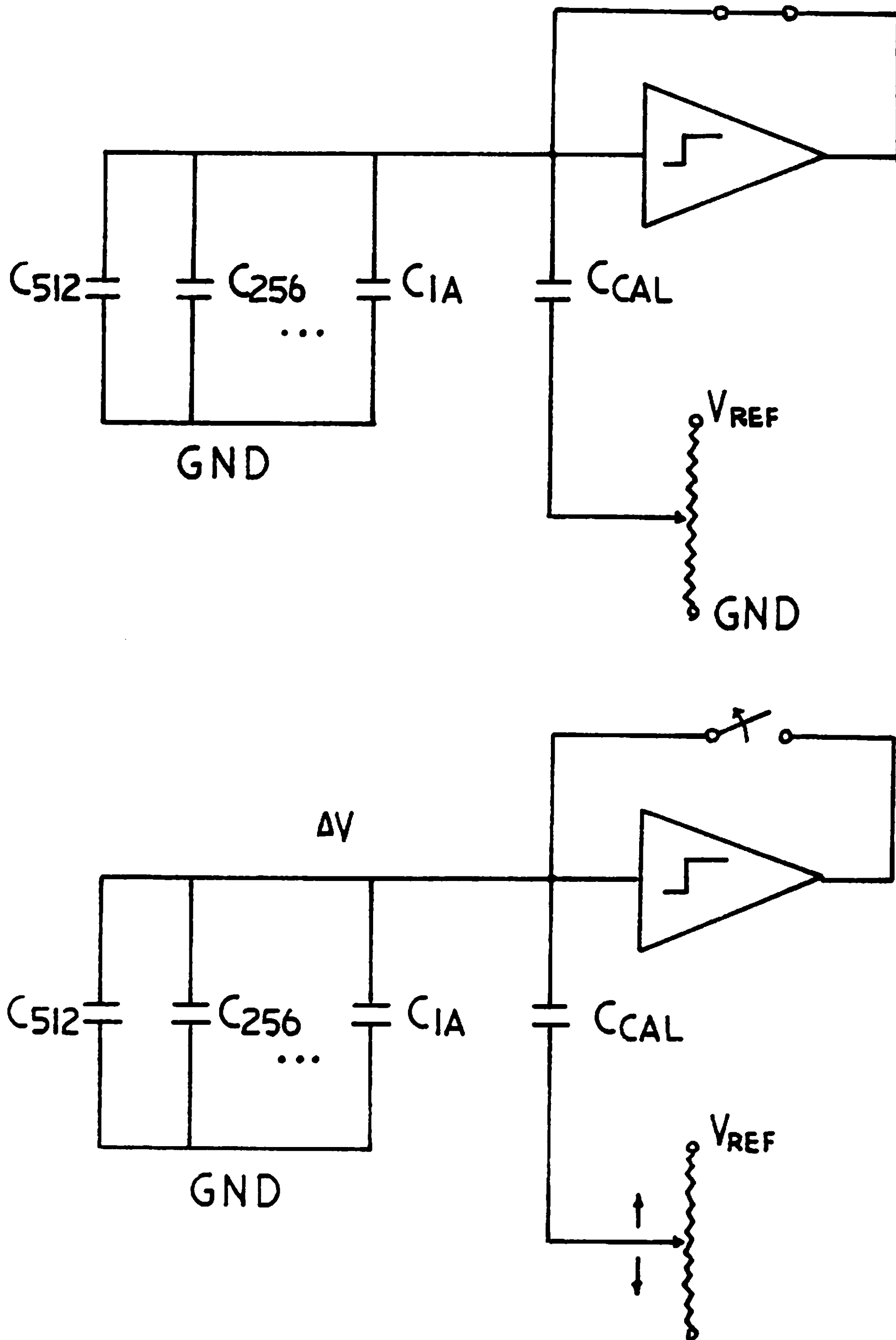


FIG. 6.3 MEASUREMENT OF RESIDUAL OFFSET VOLTAGE

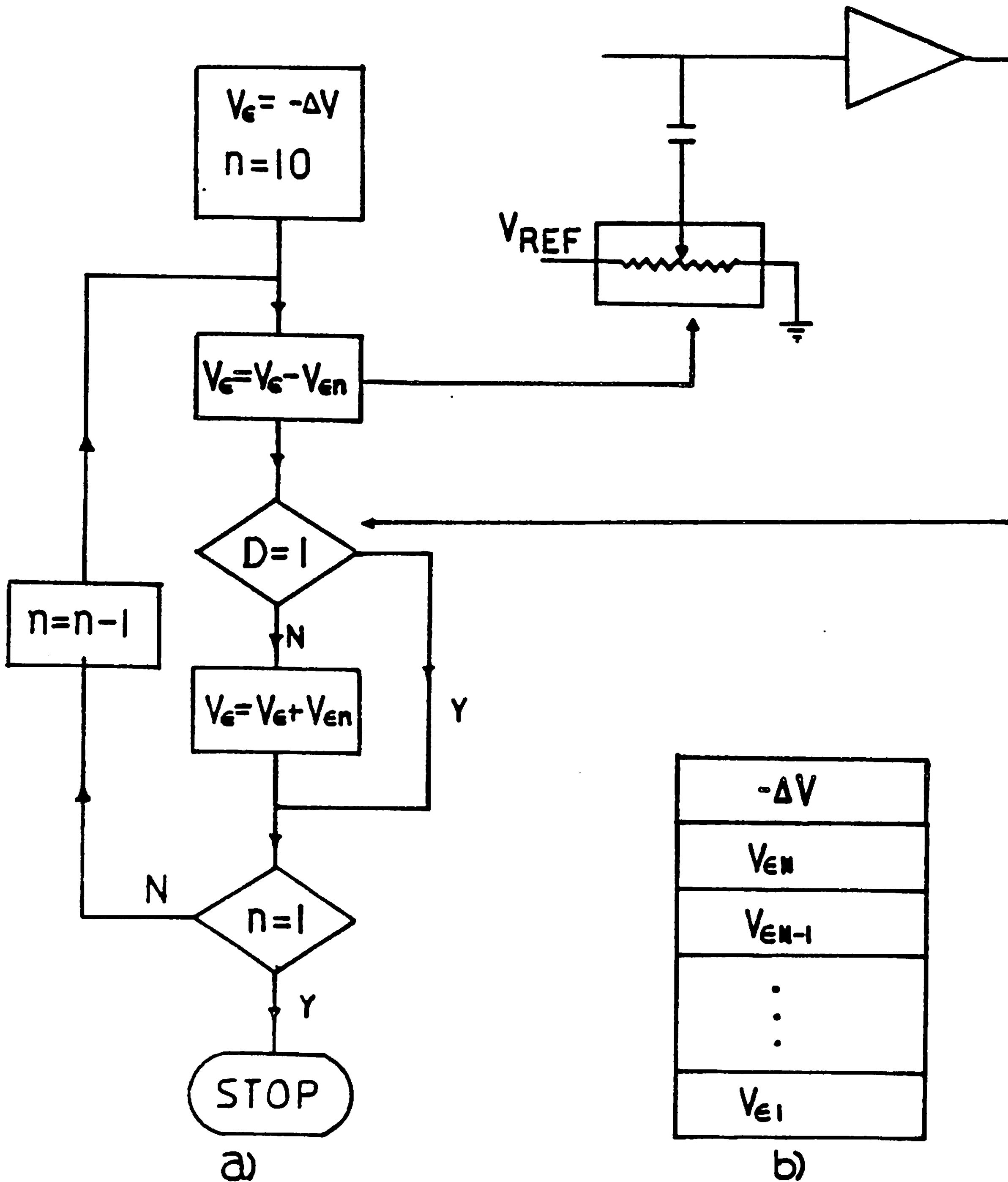


FIG. 6.4 a) CONVERSION FLOWCHART
b) MEMORY ORGANIZATION

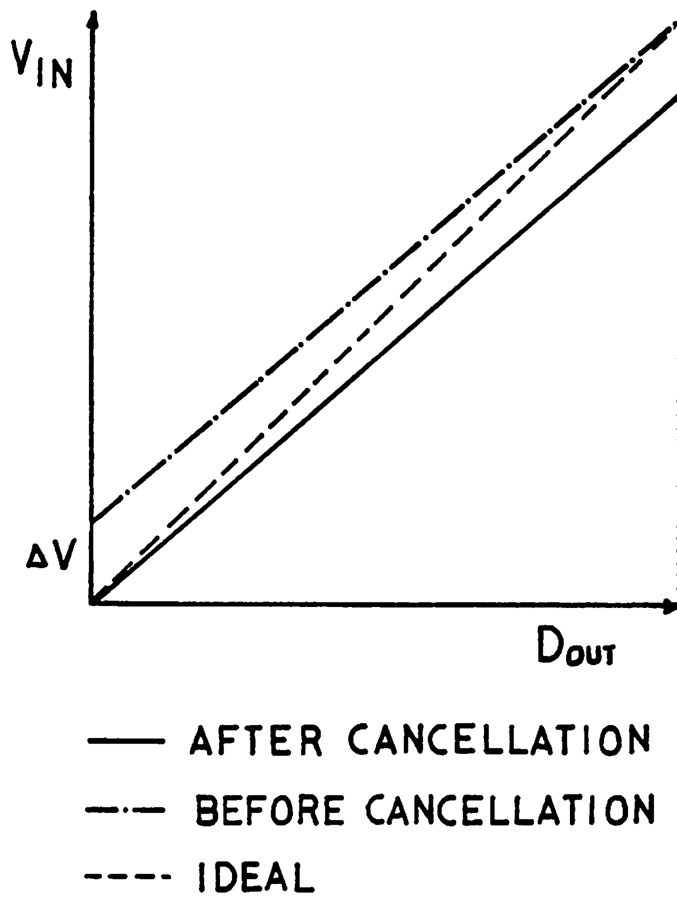
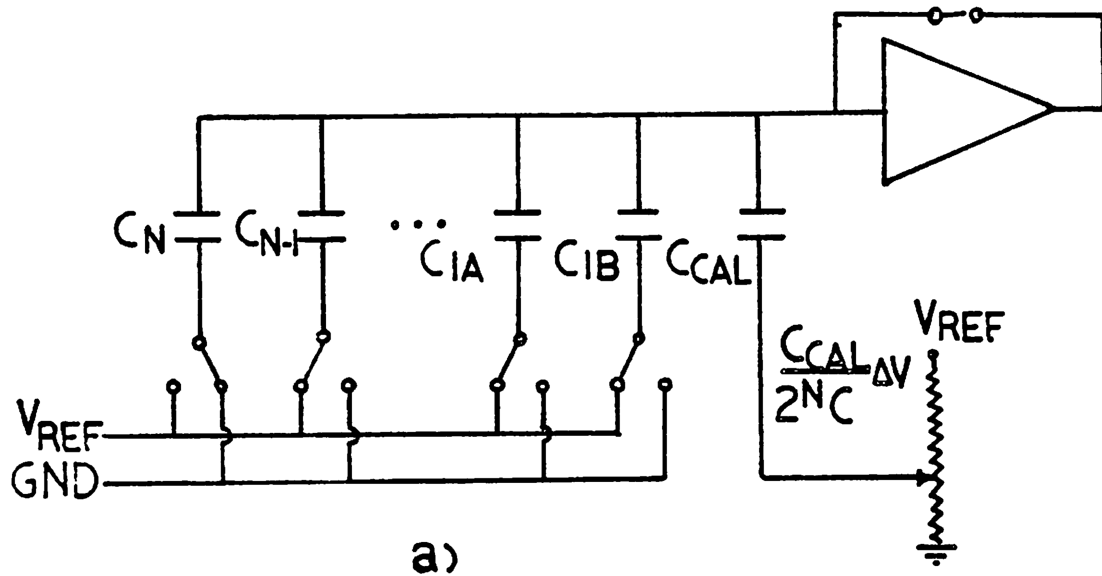


FIG. 6.5 TRANSFER CHARACTERISTIC AFTER OFFSET CANCELLATION I



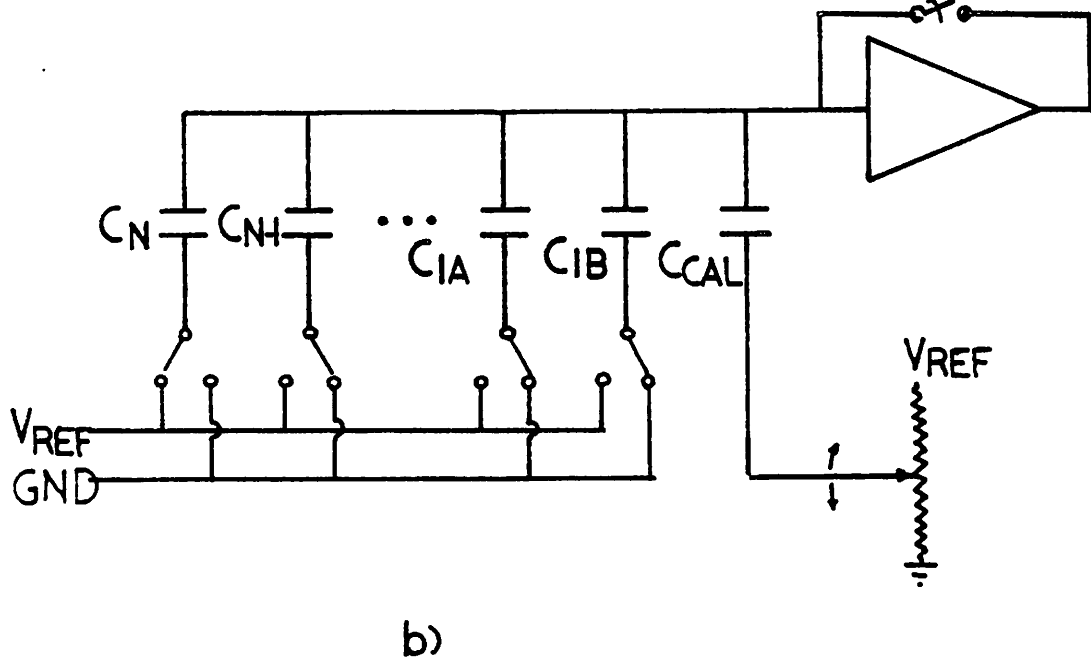


FIG. 6.6 RESIDUAL OFFSET CANCELLATION II

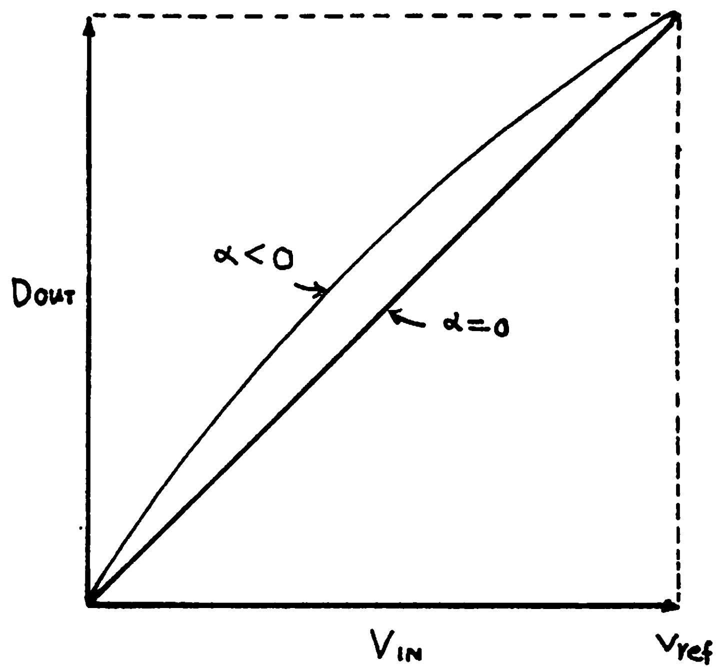


FIG. 6.7 EFFECT OF VOLTAGE COEFFICIENT

OF CAPACITORS

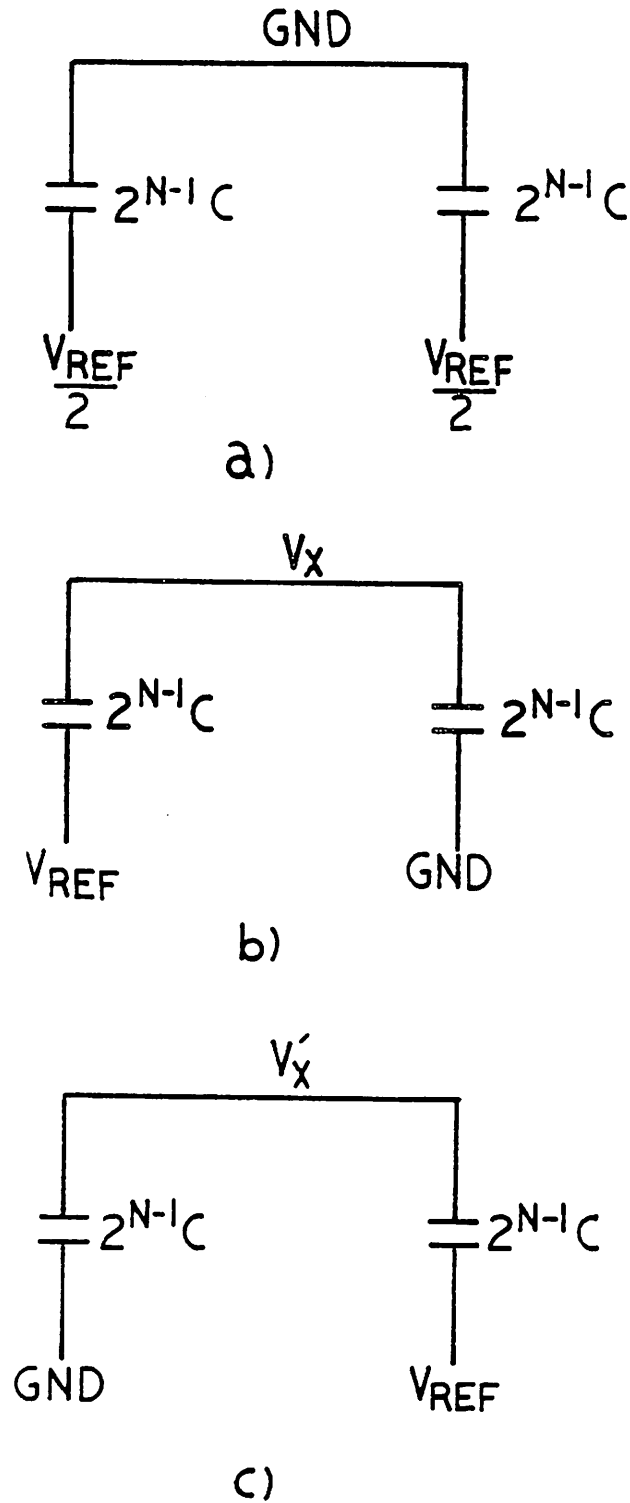
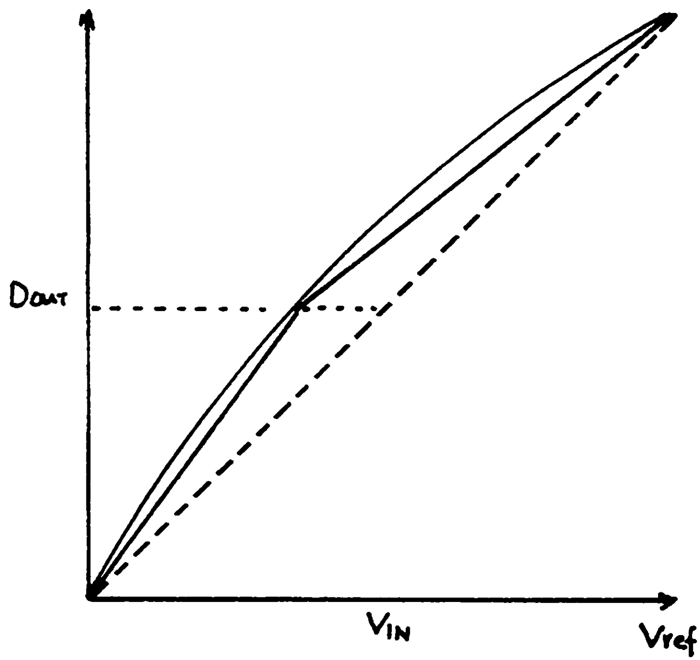
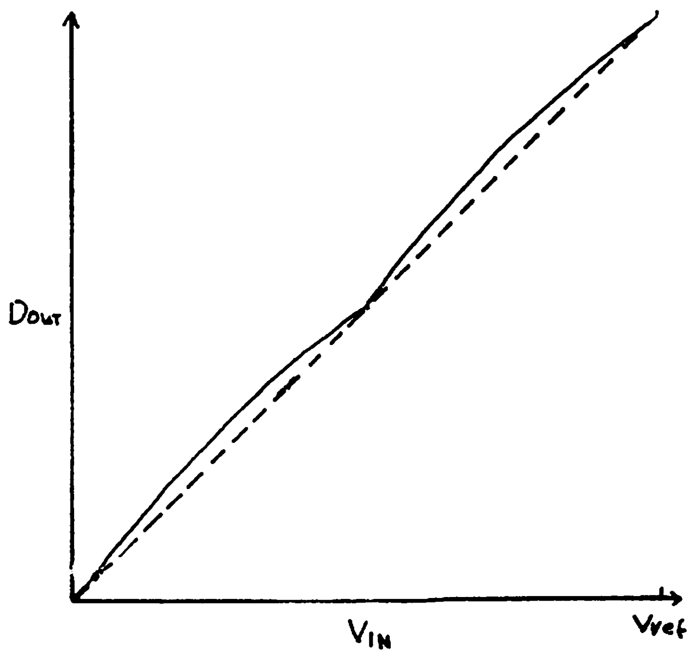


FIG. 6.8 MEASUREMENT OF VOLTAGE COEFFICIENT



(a)



(b)

FIG. 6.9 2-SECTION LINEAR CORRECTION

OF VOLTAGE COEFFICIENT

0	$-\dfrac{\frac{\alpha}{4}V_{REF}^2}{1+\alpha V_{REF}/2}$
$V_{EN} - \dfrac{\frac{\alpha}{4}V_{REF}^2}{1+\alpha V_{REF}/2}$	$V_{EN} + \dfrac{\frac{\alpha}{4}V_{REF}^2}{1+\alpha V_{REF}/2}$
$V_{EN-1} - \dfrac{\frac{\alpha}{8}V_{REF}^2}{1+\alpha V_{REF}/2}$	$V_{EN-1} + \dfrac{\frac{\alpha}{8}V_{REF}^2}{1+\alpha V_{REF}/2}$
⋮	⋮
$V_{E1} - \dfrac{\frac{\alpha}{2^{N+2}}V_{REF}^2}{1+\alpha V_{REF}/2}$	$V_{E1} + \dfrac{\frac{\alpha}{2^{N+2}}V_{REF}^2}{1+\alpha V_{REF}/2}$
↑ $\bar{D}_N$	↑ D_N

FIG. 6.10 MEMORY CONTENTS FOR 2-SECTION PIECEWISE LINEAR CORRECTION

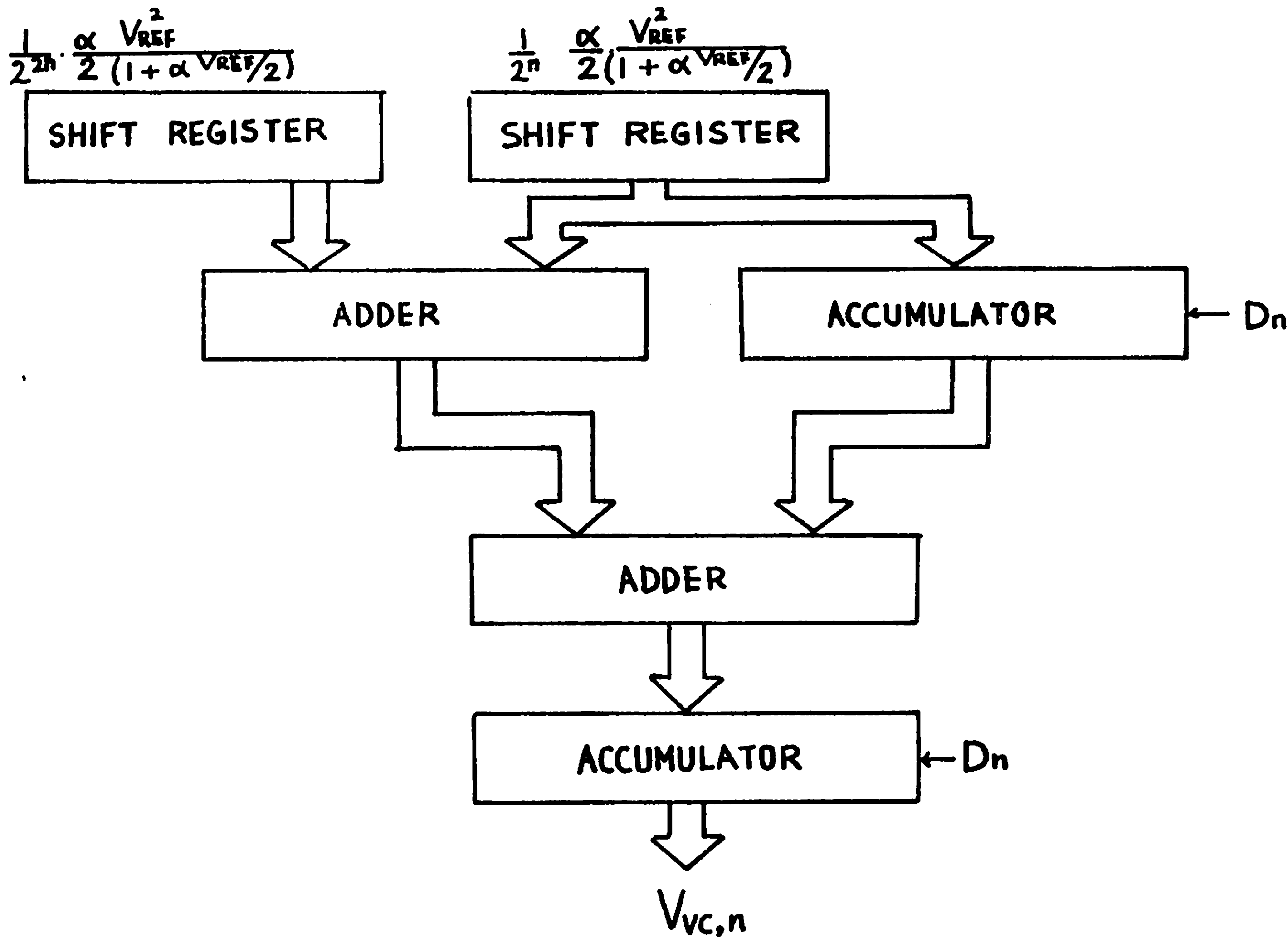


FIG. 6.11 RECURSIVE CORRECTION OF VOLTAGE COEFFICIENT

CHAPTER 7

A/D Converter Testing Techniques

7.1. Classical A/D Converter Testing Technique

A block diagram of a classical A/D converter test circuit is illustrated in Fig. 7.1 [26]. A slow ramp is fed to the A/D converter under test. The digital output of the A/D converter is then fed to a D/A converter which generally should have higher precision than the A/D converter under test. The resulting staircase output and the original ramp is compared and amplified by a differential amplifier. The amplified difference is plotted in X-Y recoder or observed on an oscilloscope.

This test can be considered as a 'DC' test because the variation of the input voltage between sampling times never exceeds 1 LSB of the converter being tested. The dynamic behavior of the converter when a fast changing signal is applied cannot be tested this way.

One of the drawbacks of this test is that a highly accurate D/A converter is needed. Testing of converters with 12 bits or more is particularly difficult. Also, this test can be fairly slow because enough time should be given for the D/A converter and X-Y plotter to settle.

This test usually measures each transition point only once, since the averaging of the transition point is very difficult. For testing high resolution converter where the difference signal is extremely small, this test is highly subject to noise, especially $\frac{1}{f}$-noise of the signal source.

7.2. Code Density Test

7.2.1. Introduction

In this test, an input with a known waveform is applied to the A/D converter under test, and the converter will sample this input randomly [27,28]. The sampling rate should be asynchronous with respect to the input frequency to assure randomness of the sampling. Generally a large number of samples are needed to obtain statistically meaningful test results. Then a histogram is constructed from the number of occurrences of each digital output code. From the histogram, the probability density of each code is computed. This probability density is compared with the expected probability density of an ideal converter, and differential and integral non-linearity can be calculated.

This is a truly dynamic test since any input waveform can be used as long as its mathematical form is known, and the converter can be operated at full speed. In addition, random noise of the system is effectively reduced by taking a large number of samples. Also, unlike the classical testing technique, the code density test never needs a highly accurate D/A converter which would restrict the precision of the test.

With the aid of a digital computer, a large amount of data can be processed very quickly. The entire testing can be completely automated, and a full characterization of a converter can be performed in a short time, even for converters with 12 bits or more resolution.

7.2.2. Selection of Input Waveform and Frequency

As was discussed in the earlier section, any waveform can be used as an input to the converter being tested if the precise mathematical form of the waveform is known. To avoid mathematical complication, the waveform should be expressed in relatively simple functions. Conceptually, it is easy to use a ramp as an input voltage. In this case, the expected probability density will be same for all codes except for codes all 0 and all 1. However, in practice, it is difficult to generate an extremely linear ramp. Also, the ramp has a large discontinuity between the end of a ramp and the beginning of the next ramp. The behavior of the waveform near the discontinuity can affect the test significantly.

As an alternative, a pure sine wave can be used instead of a ramp. Although a sine wave needs a little more complicated mathematical manipulation than a ramp, it is continuous and it is relatively easy to obtain a sine wave generator with harmonic distortion smaller than -95 dB relative to the fundamental. Also, the distortion level can be confirmed by a measurement using a spectrum analyzer, unlike the distortion in ramp [28].

The frequency of the input waveform should be determined by the performance of the converter under test. The maximum input frequency will be limited such that the sample and hold circuit can settle properly. It is important that the sampling rate and the input frequency are not harmonically related to each other. If they are harmonically related, the input voltage will be sampled at the same point repetitively, causing the statistical analysis to fail. Converter clock jitter and frequency drift of the oscillator help randomness of the sampling.

7.2.3. Code Density Test with Sine Wave Input

Assume that a sine wave of amplitude A and angular frequency ω is randomly sampled. The probability that the sampled voltage lies between V_1 and V_2 ($-A < V_1 < V_2 < A$) is :

$$P(V_1 < V < V_2) = \frac{1}{\pi}\left\{\sin^{-1}\frac{V_1}{A} - \sin^{-1}\frac{V_2}{A}\right\} \tag{7.1}$$

An ideal n bit A/D converter will convert any voltage between $\frac{2i-2^n+1}{2^n}V_{ref}$ and $\frac{2i-2^n-1}{2^n}V_{ref}$ to digital code i where i ranges from 0 for the most negative voltage to 2^n for the most positive voltage. Thus the probability of obtaining the code i by randomly sampling the sine wave is :

$$p_i = \frac{1}{\pi}\left[\sin^{-1}\left\{\left(\frac{2i-2^n+1}{2^n}\right)\frac{V_{ref}}{A}\right\} - \sin^{-1}\left\{\left(\frac{2i-2^n-1}{2^n}\right)\frac{V_{ref}}{A}\right\}\right] \tag{7.2}$$

for $i=1,2,\ldots,2^n-2$ assuming $A > V_{ref}$. Since there is no further quantization level below $-V_{ref}$ or over V_{ref}, any voltage out of these boundary will be converted into either code 0 or 2^n-1. Therefore the probabilities of obtaining code 0 and 2^n-1 are larger than those directly calculated from Equation 7.2. The computation of p_0 and p_{2^n-1} is shown in Equation 7.13 and Equation 7.15.

The shape of this probability density function is shown in Fig. 7.2. The probability is smaller in the middle since the slope of the sine wave is larger. Note that the density is discontinuous at both ends as was discussed earlier.

After the histogram is constructed from the sampled data, the estimate of each transition voltage can be computed from Equation 7.2. Taking cosine of both sides of Equation 7.2 :

$$\cos\{\pi P(V_1<V<V_2)\} = \cos\left(\sin^{-1}\frac{V_2}{A} - \sin^{-1}\frac{V_1}{A}\right)$$

$$= \cos\left(\sin^{-1}\frac{V_2}{A}\right)\cos\left(\sin^{-1}\frac{V_1}{A}\right) + \frac{V_1V_2}{A^2}$$

$$= \frac{\sqrt{A^2-V_1^2}\,\sqrt{A^2-V_2^2}}{A^2} + \frac{V_1V_2}{A^2} \quad (7.3)$$

Equation 7.3 can be rewritten :

$$V_2^2 - 2V_2V_1\cos\pi p + A^2(1-\cos^2\pi p) = 0 \quad (7.4)$$

where $p = P(V_1<V<V_2)$. Equation 7.4 can be solved for V_2 yielding :

$$V_2 = V_1\cos\pi p + \sqrt{A^2-V_1^2}\,\sin\pi p \quad (7.5)$$

Using $V_1 = -A$ and the transition level $V_2 = V_i$:

$$V_i = -A\cos\pi p \quad (7.6)$$

The estimate of each transition level can be obtained by the ***frequency substitution principle*** [29]. Substituting the observed relative frequency $\frac{ch(i)}{N_{TOT}}$:

$$\bar{V}_i = -A\cos\pi\frac{ch(i)}{N_{TOT}} \quad (7.7)$$

where $ch(i)$ is cumulative histogram to code i. The differential non-linearity for the code i is thus :

$$DN_i = \frac{2^N(V_i-V_{i-1})}{V_{ref}} - 1 \;\; LSB \quad (7.8)$$

Integral non-linearity can also be computed from Equation 7.7. Integral non-linearity is defined by the deviation of the transition level from the ideal value:

$$IN_i = \bar{V}_i - \frac{i}{2^N}V_{ref}$$

Practically, computing integral non-linearity this way will require much larger number of samples than is required for differential non-linearity computation at the same accuracy level. It would be difficult to determine integral non-linearity of A/D converters with over 10 bit resolution. The fast Fourier transform test is much sensitive to integral non-linearity than the code density test, although almost no information about differential non-linearity is obtained from FFT test.

From the histogram, the estimates the offset voltage V_{OS} and the amplitude A can also be computed.

The estimate of the offset voltage can be obtained from the difference between the number of codes over 0 and that of below 0. If the offset voltage is zero, the number of codes over 0 should be identical to that of below 0. In the presence of offset voltage V_{OS}, the effective input waveform becomes :

$$V_{IN}(t) = V_{OS} + A\sin\omega t \tag{7.9}$$

And the probability density function becomes :

$$p(V-V_{OS}) = \frac{1}{\pi\sqrt{A^2-(V-V_{OS})^2}} \tag{7.10}$$

Thus the probability p_p that any randomly sampled voltage is positive is then:

$$p_p = P(V>0) = \int_0^{A+V_{OS}} \frac{1}{\pi\sqrt{A^2-(V-V_{OS})^2}}dV \tag{7.11}$$

$$= \frac{1}{\pi}\left\{\sin^{-1}(1) - \sin^{-1}(-\frac{V_{OS}}{A})\right\} \tag{7.12}$$

$$= \frac{1}{2} + \frac{1}{\pi}\sin^{-1}\frac{V_{OS}}{A} \tag{7.13}$$

And the probability p_n that negative voltage is sampled is

$$p_n = 1 - p_p \tag{7.14}$$

Solving Equation 7.13 and Eqn 7.14 for V_{OS} :

$$V_{OS} = A\frac{\pi}{2}\sin(p_p - p_n) \qquad (7.15)$$

Again by the frequency substitution principle, an estimate of V_{OS} can be obtained by replacing the unknown population frequencies p_p and p_n by the observed sample frequencies $\frac{N_p}{N_{TOT}}$ and $\frac{N_n}{N_{TOT}}$.

$$V_{OS} = A\frac{\pi}{2}\sin\frac{N_p - N_n}{N_p + N_n} \qquad (7.16)$$

where N_p and N_n are the number of positive and negative samples respectively.

When the offset voltage is small relative to the sine amplitude, this can be approximated :

$$V_{OS} = A\frac{\pi}{2}\,\frac{N_p - N_n}{N_p + N_n} \qquad (7.17)$$

In this equation, the amplitude A is still unknown. However, an approximate value can be used since V_{OS} doesn't have to be very precisely calculated.

The amplitude A of the sine wave can now be estimated by the number of the first and the last codes. Any input greater than $(1-\frac{1}{2^{n+1}})V_{ref}$ will be coverted into the last code $(i = 2^n - 1)$, and any input smaller than $(-1+\frac{1}{2^{n+1}})V_{ref}$ will be converted into the first code $(i = 0)$.

Thus the probability of obtaining the last code by a random sampling is :

$$p_{2^n-1} = \int_{(1-\frac{1}{2^{n+1}})V_{ref}}^{A+V_{OS}} p(V-V_{OS})dV \qquad (7.18)$$

$$= \int_{V_{ref}}^{A+V_{OS}} p(V-V_{OS})dV + \int_{(1-\frac{1}{2^{n+1}})V_{ref}}^{V_{ref}} p(V-V_{OS})dV \qquad (7.19)$$

Likewise, the probability of obtaining the first code is :

$$p_0 = \int_{-A+V_{OS}}^{-V_{ref}} p(V-V_{OS})dV + \int_{-V_{ref}}^{(-1+\frac{1}{2^n+1})V_{ref}} p(V-V_{OS})dV \tag{7.20}$$

Adding Equations 7.14 and 7.15 :

$$p_{2^n-1}+p_0 = \int_{V_{ref}}^{A+V_{OS}} p(V-V_{OS})dV + \int_{-A+V_{OS}}^{-V_{ref}} p(V-V_{OS})dV \tag{7.21}$$

The second terms in the right hand sides of Equation 7.19 and Equation 7.20 cancelled each other since V_{OS} is small.

Substituting $p(V-V_{OS}) = \frac{1}{\sqrt{A^2-(V-V_{OS})^2}}$ into Equation 7.21 :

$$p_{2^n-1}+p_0 = 1 - \frac{1}{\pi}\left[\sin^{-1}\frac{V_{ref}+V_{OS}}{A} + \sin^{-1}\frac{V_{ref}-V_{OS}}{A}\right] \tag{7.22}$$

If V_{OS} is much smaller than V_{ref}, this equation can be approximated :

$$p_{2^n-1}+p_0 = 1 - \sin^{-1}\frac{V_{ref}}{A}\cdot\frac{2}{\pi} \tag{7.23}$$

Solving Equation 7.23 for A :

$$A = \frac{V_{ref}}{\sin(1-p_0-p_{2^n-1})\frac{\pi}{2}} \tag{7.24}$$

Then again by the frequency substitution principle the estimate $\hat{A}$ can be obtained:

$$\hat{A} = \frac{V_{ref}}{\sin\left[\frac{N_{TOT}-N_{2^n-1}-N_0}{N_{TOT}}\frac{\pi}{2}\right]} \tag{7.25}$$

This estimate of A can be used in Equation 7.16 or Equation 7.17 to calculate more accurate estimate of V_{OS}.

7.2.4. Total Number of Samples

There is an uncertainty in determining differential non-linerity due to the statistical nature of the test. The total number of samples to be taken should be determined by the confidence level with which the differential non-linearity of each bit is desired to be known. The uncertainty in the differential non-linearity is the uncertainty in the width of the segment. From Equation 7.7 :

$$V_i - V_{i-1} = -A\left[\cos\frac{\pi ch(i)}{N_{TOT}} - \cos\frac{\pi ch(i-1)}{N_{TOT}}\right]$$

$$= -A\left[\cos\pi\frac{ch(i-1)+N_i}{N_{TOT}} - \cos\frac{\pi ch(i-1)}{N_{TOT}}\right]$$

$$\approx -A\frac{d}{dN_i}\cos\frac{\pi ch(i-1)}{N_{TOT}}$$

$$= \frac{A\pi N_i}{N_{TOT}}\sin\frac{\pi ch(i-1)}{N_{TOT}} \qquad (7.26)$$

Although $ch(i-1)$ itself is a random variable, it only affect the integral non-linearity up to code $i-1$. Thus, $ch(i-1)$ can be considered as a constant in determining differential non-linearity for code i, and N_i is the only random variable of concern.

For a random sampling, the event that the code i appears is a Bernoulli trial with a probability of p_i. Therefore, the resulting distribution function is a binomial distribution with the mean $N_{TOT}p_i$ and the standard deviation $\sqrt{N_{TOT}p_i(1-p_i)}$.

When N_{TOT} is large, the distribution function can be approximated by the Gaussian distribution function [30]. To compute the differential non-linearity with $1-\alpha$ confidence level, from Equation 7.26, $E(N_i)$ should be known with the same confidence level. Thus :

$$P(N_i - z_{\frac{\alpha}{2}}\sigma \le E(N_i) \le N_i - z_{\frac{\alpha}{2}}\sigma) = 1-\alpha \tag{7.27}$$

To know N_i within a certain fraction k of itself with $1-\alpha$ confidence level :

$$z_{\frac{\alpha}{2}}\sigma = kE(N_i) \tag{7.28}$$

Rewriting the last equation by substituting $\sigma = \sqrt{N_{TOT}p_i}$ and $E(N_i) = N_{TOT}p_i$:

$$N_{TOT} = \frac{z_{\frac{\alpha}{2}}^2}{k^2}\frac{\sqrt{p_i(1-p_i)}}{p_i} \approx \frac{z_{\frac{\alpha}{2}}^2}{k^2 p_i} \tag{7.29}$$

since $1-p_i \approx 1$.

N_{TOT} is maximum for minimum p_i. The minimum p_i is at the middle point where the slope of the sine wave is the greatest.

$$MIN(p_i) = p_{2^{n-1}}$$

$$= \frac{2}{\pi}\sin^{-1}\left(\frac{V_{ref}}{2^n A}\right) \tag{7.30}$$

$$\approx \frac{2}{\pi}\frac{V_{ref}}{2^n A} \tag{7.31}$$

Substituting Equation 7.28 into Equation 7.25 :

$$N_{TOT} = \frac{z_{\frac{\alpha}{2}} A\pi 2^{n-1}}{k^2 V_{ref}} \tag{7.32}$$

This is the total number of samples neeeded to estimate the differential non-linearity with a precision k and at least $1-\alpha$ confidence level.

7.2.5. Summary of Code Density Test

By using a pure sine wave as an input and randomly sampling this waveform, observed sample frequency can be obtained. From this data, the amplitude of

the input sine wave can be estimated by Equation 7.20. The system offset voltage can be computed by Equation 7.11. The differential and integral non-linearity are estimated by Equation 7.21 and Equation 7.23 respectively. The total number of samples needed to determine the differential non-linearity within a certain precision and confidence level can be determined by Equation 7.29.

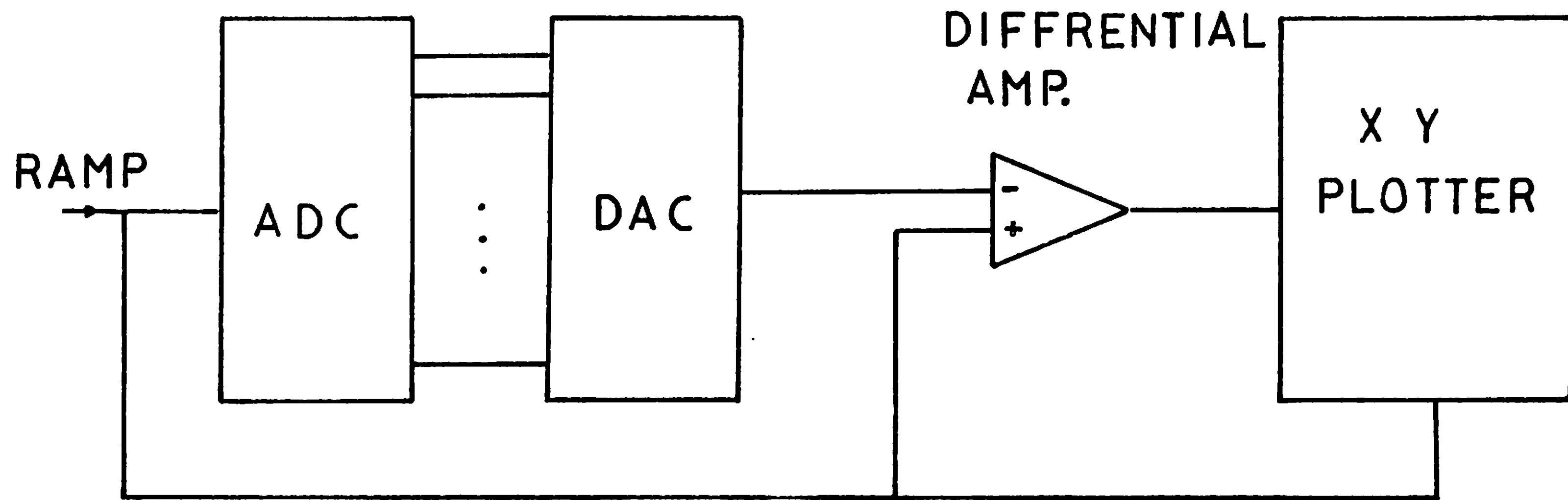


FIG. 7.1 CLASSICAL A/D CONVERTER TESTING SETUP

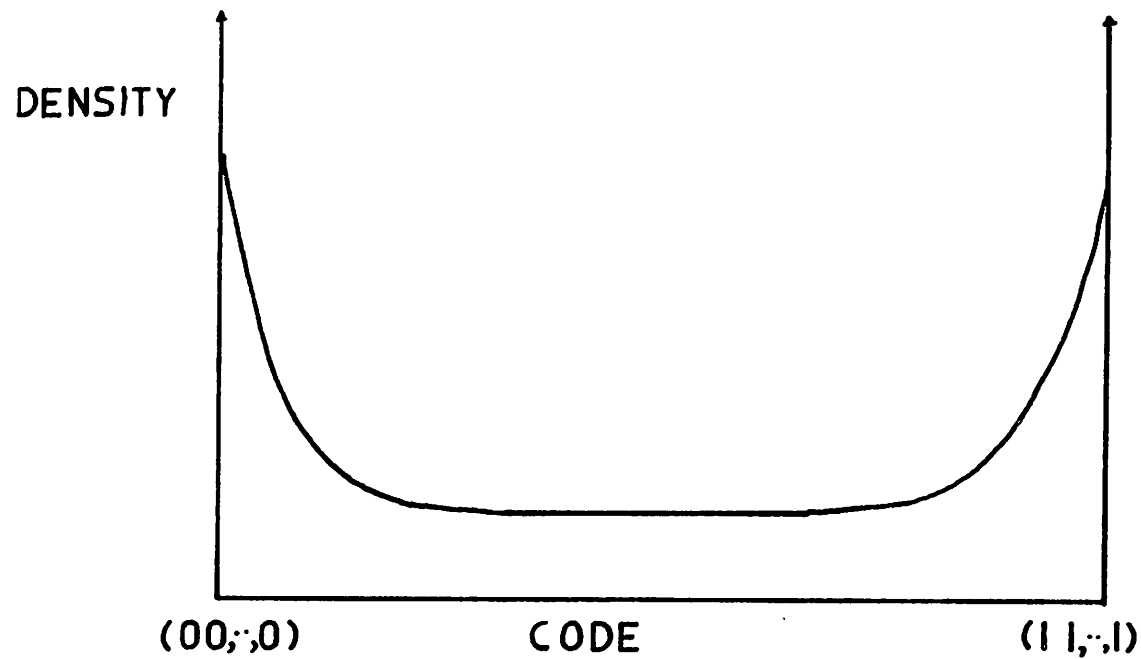


FIG. 7.2 IDEAL CODE DENSITY WITH SINEWAVE INPUT

CHAPTER 8

EXPERIMENTAL RESULTS

8.1. Description of the Experimental Chip

In order to verify the principle and techniques described in previous chapters, an experimental integrated circuit A/D converter was designed, fabricated, and fully characterized. The die photograph of the experimental chip is shown in Fig 8.1. This chip contains a 10 bit plus sign capacitor array main DAC, a 5 bit resistor string sub DAC and a 7 bit resistor string calibration DAC. The main DAC consists of 1024 unit capacitors arranged as shown in Fig 8.2. To minimize sub DAC gain error due to a systematic mismatch of the coupling capacitor, the unit capacitor connecting the sub DAC to the main DAC is located at the center of the array. The effect of the oxide thickness gradient and the non-uniform etching of the polysilicon top plate is reduced by a pseudo-common centroid layout. Only the largest capacitor C_{512} is laid out symmetrically around the center.

The capacitors are is formed by a heavily doped polysilicon top plate and ion-implanted bottom plate. The bottom plate is doped with phosphorus which tends to pile up near the surface, giving a lower voltage coefficient than an n-type plate doped with arsenic. The nominal junction depth is 0.5 μm, and surface doping level is estimated to be more than 10^{20} cm^3. The nominal oxide thickness was 1000 Å, but later reduced to 600 Å due to necessary modifications of the CMOS process [31].

The MOS transistors fabricated by the original Berkeley CMOS process [10] exhibited a very low oxide breakdown field and a large gate leakage current. The gate oxide sometimes broke down at less than 10 V. The leakage current through the gate was often more than 100 μA. The capacitor oxide, however, was of an excellent quality. In the original process schedule, the gate oxide was grown right after the n-well definition and silicon nitride was deposited on the gate oxide. This gate oxide suffered a large thermal stress during the local oxidation step, and also was subject to contamination during subsequent etching steps. The capacitor oxide, on the other hand, was grown after all the nitride etching steps and the local oxidation, and polysilicon was deposited immediately. Hence, the possibility of the thermal stress and contamination was much smaller for the capacitor oxide.

The initial purpose of using the different oxide for the transistors and capacitors was to attain a separate control over the oxide thicknesses [32]. The thinner the gate oxide, the better the performance of the circuit. In this circuit and most other applications, ratio accuracy among the capacitors is more important than the absolute value. The ratio matching is not determined by the thickness of the oxide but by the physical size of the capacitors. Thicker capacitor oxide is preferable since loading on the analog circuit is less while providing comparable matching properties.

To avoid the problems stated earlier, process modifications were necessary. The original gate oxide is removed after local oxidation, and new gate oxide is grown at the same time the capacitor oxide is grown. This improves the quality of the gate oxide at the expense of decreased capacitor oxide thickness. Under the same environment, oxide grows slightly faster on heavily doped silicon [33]. Thus the capacitor oxide thickness is only slightly thicker than the gate oxide since capacitor oxide is grown over the bottom plate heavily doped with phosphorus. Experimentally, the capacitor oxide was found to be 600 Å with a gate

oxide thickness of 500 Å [34].

To reduce the leakage current from the gate to source and drain through CVD glass passivation, a polysilicon oxidation step is added before the passivation [35].

After these modifications, the quality of the gate oxide was improved to have 55 V breakdown voltage and a negligible leakage current.

The structure of the unit capacitor is shown in Fig. 8.3.

The resistors are formed by source-drain implantation of n-channel transistors. The sheet resistance is 25 ohms/square. To minimize mismatches due to possible contact resistance variation, contacts are avoided between the unit resistors. Tree decoders are included in both the sub DAC and the calibration DAC. The interconnections between the resistors and the tree decoder switches are made in continuous n+ material [3]. A typical segment of a resistor string layout including tree decoder switches is shown in Fig. 8.4. The resistor string DACs are designed to be operated between ground and $-V_{ref}$ instead of between ground and V_{ref} to avoid the use of p-channel switches. Layout is simpler using n-channel switches than p-channel switches since p-channel switches should be placed in the well. Also, n-channel switches provide lower on-resistance.

Differential stages of the amplifier and the latch are laid out symmetrically to reduce the offset voltage. To reduce parasitic capacitances, many transistors share common sources and drains. Special care was taken near the high impedance nodes to minimize interconnection capacitances.

On-chip inverters and logic gates are used for controlling tree decoder switches and capacitor bottom plate switches to reduce the number of pinouts.

A simplified schematic diagram of the entire chip is shown in Fig. 8.5. Most of the logic circuitry was omitted from the test chip for simplicity and to permit trial of several other correction techniques.

Reference voltages are supplied externally. A CMOS band gap reference such as reported by B.S. Song *et al*, [36] can be included on the same chip. This band gap reference voltage, fabricated using the identical CMOS process to the prototype converter, exhibited average of 13 ppm/°C in commercial temperature range. Although this reference voltage can be implemented on a small area, simpler reference voltages can be used for the applications where the gain drift due to temperature variation is not important.

8.2. Test Setup

Three computer systems are interlinked for a very versatile control and characterization of the converter. A 8085 based S100 microcomputer controls the calibration, an LSI-11 is used as a buffer memory for the code density test, and DEC VAX 780 processes the data for the complete characterization. Fig. 8.6 shows the block diagram of this setup.

8.2.1. The Control Circuit

The control circuit consists of a TTL control board and a micro computer. The micro computer is S100 system with Intel 8085 CPU. The control program is written in BASIC, and compiled by a BASIC compiler.

The TTL control board contains fast switching logics such as SAR, full adders, and data registers. The grounds of the micro computer and the control board are completely separated by the opto-isolators. This is to prevent noise coupling from the microcomputer ground to the the ground of the control board which shares the same ground with noise-sensitive analog circuits.

When the control program is executed, the micro computer sends out a signal to initiate the calibration cycle. Each residual voltage is measured by the calibration DAC, and sent back to the micro computer. As an option, the residual voltages can be measured many times to reduce the effect of random noise. The average values are kept for the computation of the correction terms, and the mean square error is computed to calculate the system noise.

After all the correction terms are computed by the micro computer, they are loaded to the registers on the control board. These registers are directly accessible without going through the CPU for a fast operation. These data are read back to the micro computer to verify that correct data are written in the register.

After the data are verified to be correct, the micro computer sends out a ready signal to the control board and the converter is ready for the normal conversion.

The total calibration time is in the order of 50 ms per iteration. Therefore if the data are averaged 16 times, the calibration will take approximately 800 ms. Most of the time is taken by the micro computer. If assembly language were used for the control program, the calibration time would be much shorter. If dedicated logic circuit is used as would be the case for a product based on this technique, the calibration time is estimated to be only 600 μs per iteration.

8.2.2. The Characterization Circuit

As was discussed in Chapter 7, a code density test was used to characterize the converter. An LSI-11 is used as a buffer memory and a DEC/VAX 780 is used to process the data in the buffer memory for the complete characterization of the converter [27].

When the converter is ready for normal conversion, an extremely pure sine wave is fed to the converter. The digital output is periodically taken by the LSI-11 and stored in the buffer memory. The buffer memory is organized such that each byte corresponds to each possible output code of the converter. If the digital output code from the converter coincides a certain address of the buffer memory, the content of the memory is incremented. In this manner, each byte of the memory contains the frequency of the code corresponding to the address of the memory.

After enough data are taken, the buffer memory is mapped into a UNIX file. This file is later processed by several programs that calculates the differential nonlinearity, integral nonlinearity and offset [37].

8.3. Experimental Results :Converter Performance

Table 8.1 summarizes the performance of the comparator at room temperature [38,39]. The resolution was at least ½ LSB at 17 bit level or 30 μV. The resolution was measured by applying a small voltage through the calibration DAC after a large excursion on the other direction applied by the main DAC.

The worst case delay for 15 bit resolution was 3 μs, which is significantly slower than the designed value of 500 ns. This was due to digital switching noise coupled to the input of the comparator. The initial magnitude of the noise was about 1 mV and had a time constant of roughly 500ns. After 3 μs, the switching noise was reduced to a sufficiently small level.

The noise figure is a hand-calculated value. To reduce the parasitic capacitances from the critical nodes, probing pads were made for neither the input nor output nodes of the amplifier. Thus the actual measurement of input referred noise was not possible.

Fig. 8.7 shows a typical calibration result. The numbers are the correction terms stated in 1 LSB at 16 bit level or 125 μV. It should be noted that the correction terms are the measures of the initial ratio errors of the capacitor array. In computing the correction terms, each residual voltage is measured 16 times and average values are computed. The mean square error of the residual voltages is an approximate value of the total mean square noise [40]. The RMS noise figure of the system is therefore a square root of mean square noise, and shown to be on the average of 40 μV. The maximum observed was 50 μV, and the minimum was 28 μV. This figure includes thermal noise and $\frac{1}{f}$-noise of the comparator, $\frac{kT}{C}$-noise during offset sampling, and random component of the ground noise. Although the major portion of $\frac{1}{f}$-noise is eliminated by the offset cancellation which is in effect a double correlated sampling [41], the cancellation is not complete due to aliasing [42]. Therefore, care should be taken in processing to minimize the number of surface states.

From the correction terms , initial matching of the capacitor array can be estimated. Most of the converters tested had initial matching of 9 bits. All the converters showed a systematic error on C_{512} and C_{256}, which is believed to be due to non-uniform etching of the polysilicon top plate. The initial matching should be improved by a more careful layout of the capacitor array for more uniform etch width.

Due to the poor initial matching of the capacitor array, the range of the calibration was increased by doubling the coupling capacitor between the main DAC and the calibration DAC. By doing this, the range of the calibration is doubled at the cost of the resolution of calibration. Now the calibration is performed at 17 bit level instead of desired 18 bit level. Theoretically, maximum of 15 bit linearity can be achieved by the calibration at 17 bit resolution level [43]. It was

confirmed by the differential non-linearity test shown in Fig. 8.8. The unit is 1 LSB at 16 bit resolution level. The thick lines indicate 1 LSB at 15 bit level, where the converter showed no missing codes. Except for several larger spikes which are about 1.3 LSB at 16 bits, the non-linearity is less than ½ LSB at 15 bits. The output code of the converter was inverted offset binary. Thus, code (0,0,...,0) is the positive full scale and (1,1,...,1) is the negative full scale.

Linearity on the negative side appears to be better than that of the positive side in Fig. 8.8. This can be explained by the fact that the calibration is performed by the negative reference voltage, and the same correction terms are used for both the negative and the positive sides. Therefore, the negative side will be better fitted. The correction terms for the positive side may be slightly different due to different voltage coefficients among capacitors. The linearity of the positive side can be improved by performing another calibration against the positive reference voltage to obtain a accurate set of correction terms for the positive sides.

The integral non-linearity was measured statically by using an accurate programmable power supply and a DVM at major carries [44]. The maximum integral non-linearity observed was 1.6 LSB at 16 bits.

The integral non-linearity can also be inferred from the FFT test result shown in Fig. 8.9. An ultra pure 1 kHz sine wave was used as an input, and sampled by the converter. A 4096 point FFT was performed on the digital output codes. As can be seen in Fig. 8.9, no second or third harmonic distortion is visible. This confirms a good integral linearity.

Fig. 8.10 shows a accuracy-speed characteristic. Due to the digital switching noise, 15 bit accuracy was achieved at a slower speed than expected. At the maximum sampling speed of 80 kHz, 12 bit differential linearity was obtained.

Table 8.2 summarizes the converter performance at room temperature.

8.4. Other Experiments

The following tests can be used to identify any cause of linearity error not corrected by the calibration.

8.4.1. Switching Noise

Excessive switching noise can be coupled to the analog circuits causing an incorrect comparator decision. Since the switching noise is usually largest at the clock edge and rapidly dies away, a great deal of difference will be made in the effective switching noise when the strobe delay is varied [45]. A significant difference in differential linearity was observed when the delay was varied between 500 ns and 3 μs. No further improvement was made by introducing more than 3 μs delay. This experiment confirmed the coupling of the digital switching noise to the analog portion, and the time constant was estimated to be 500 ns.

A fast change in the control signals can cause inductive coupling between the control signals causing incorrect control. To test this, control signal edges can be slowed down by adding RC delay.

8.4.2. Leakage Current

The leakage current measured from the test device was very small as was stated in Section 6.4. The actual leakage current from the junctions connected to the top plate of the capacitor can be indirectly estimated by varying the

clock during the calibration.

Any charge loss during the successive approximation search of V_X's will appear as an added component to V_X's. Suppose $V_X(T_1)$ and $V_X(T_2)$ are residual voltages of a certain bit with different clock frequency. T_1 and T_2 are the total time needed for the successive approximation search for these two different clock frequencies.

Then the leakage current can be approximated :

$$I_L = \frac{C_{TOT}\{V_X(T_1)-V_X(T_2)\}}{T_1-T_2} \tag{8.1}$$

The leakage current was small enough to be unmeasurable this way, confirming the expectation from the test devices.

8.4.3. Minority Carrier Trapping

If any of the junctions are forward biased due to transient voltage excursions, minority carriers are injected to the substrate. These minority carriers in general have long lifetime and can travel very far [46]. If minority carriers are collected by the junction connected to the top plate of the capacitor array, a charge error can occur. Since the large grounding switch has most of the junction area at the top plate, this switch is most likely to collect the minority carrier. The converter is still operable without this switch at a slower conversion rate. The connection to this switch was scratched off the top plate to observe the difference. Also, substrate bias was applied to reduce the chance of forward biasing junctions. Neither of the modification caused difference in the converter characteristic.

8.4.4. Comparator Resolution

The resolution of the comparator was tested by applying a small voltage through the calibration DAC, and converting this voltage back by the calibration DAC and the comparator. All the calibration DAC codes were tested, and these codes were accurately reproduced by the calibration DAC and the comparator indicating a good resolution of the converter even at 18 bit level.

If resolution is not good enough, it can be improved by reducing the bias current of the comparator to increase the gain at the cost of conversion speed.

8.4.5. Hysteresis in Comparator

Due to a local heating of the input transistor during a large overdrive, a thermal hysteresis can occur [47]. Another cause of the hysteresis can be mobile ion in the gate oxide.

The presence of the hysteresis in the comparator can be detected by modifying the switching sequence. First, the input of the comparator is switched to $V_{ref}-V_{IN}$ before every decision by connecting all the bottom plates to V_{ref}. Calibration is performed with this switching waveform and the result recorded. Then the input of the comparator is brought to $-V_{IN}$ by throwing all the bottom plate switches to ground before each decision. If there is a hysteresis in the comparator, the calibration results using these two different switching waveform will be different. The average difference in the calibration results reflects the magnitude of the hysteresis.

8.4.6. Other Tests

As is discussed in Section 6.5 and Appendix 2, dielectric relaxation of the MOS capacitor was measured to be negligible.

The package lid was changed from metal to ceramic to see the effect of charge coupling between the package and the chip. Due to a difference in the field line shape, the charge coupling will be different when using metal and ceramic lids [48]. There was no observable difference in the characteristic of the converter.

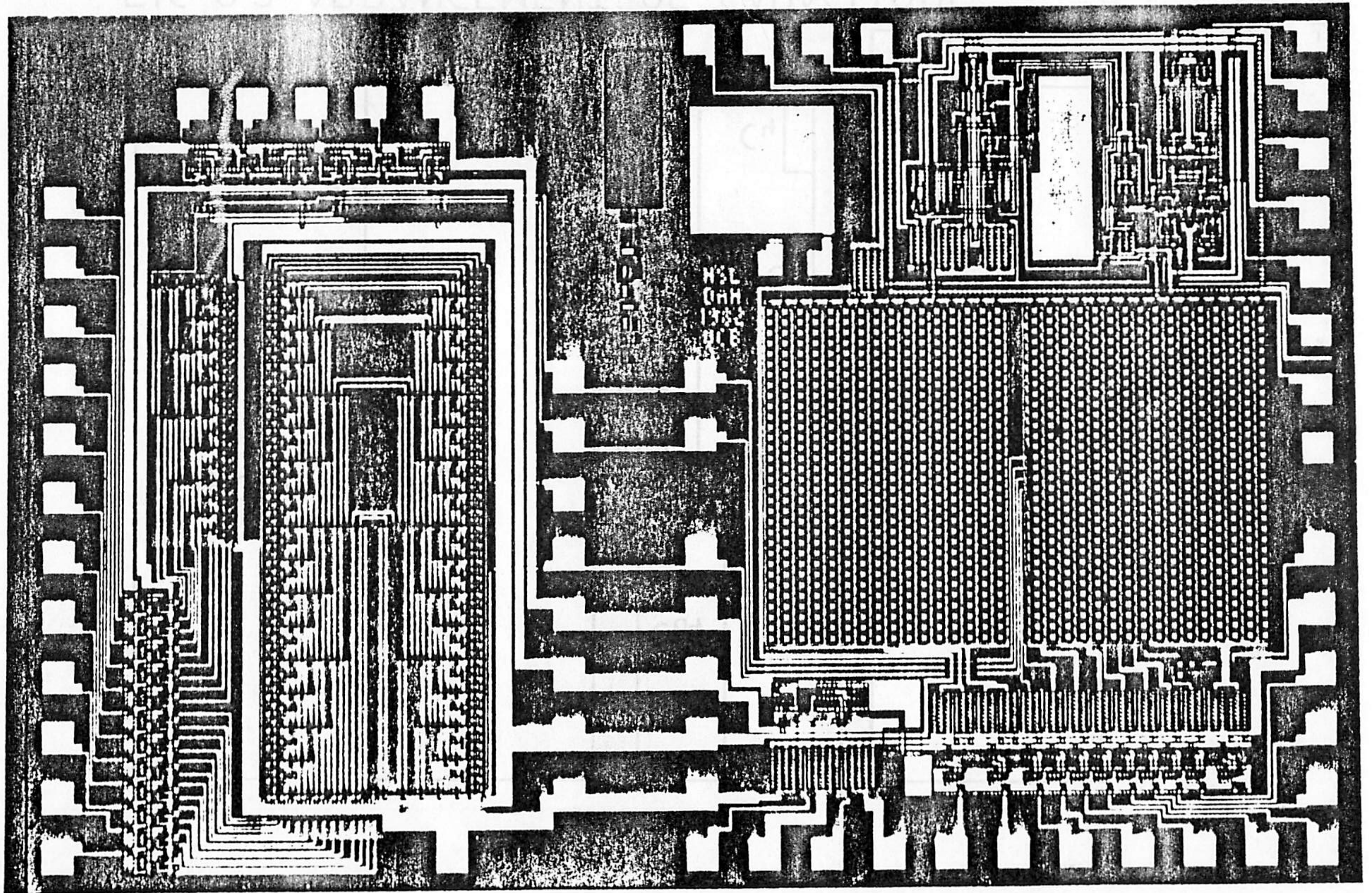


FIG. 8.1 DIE PHOTOGRAPH OF PROTOTYPE CHIP

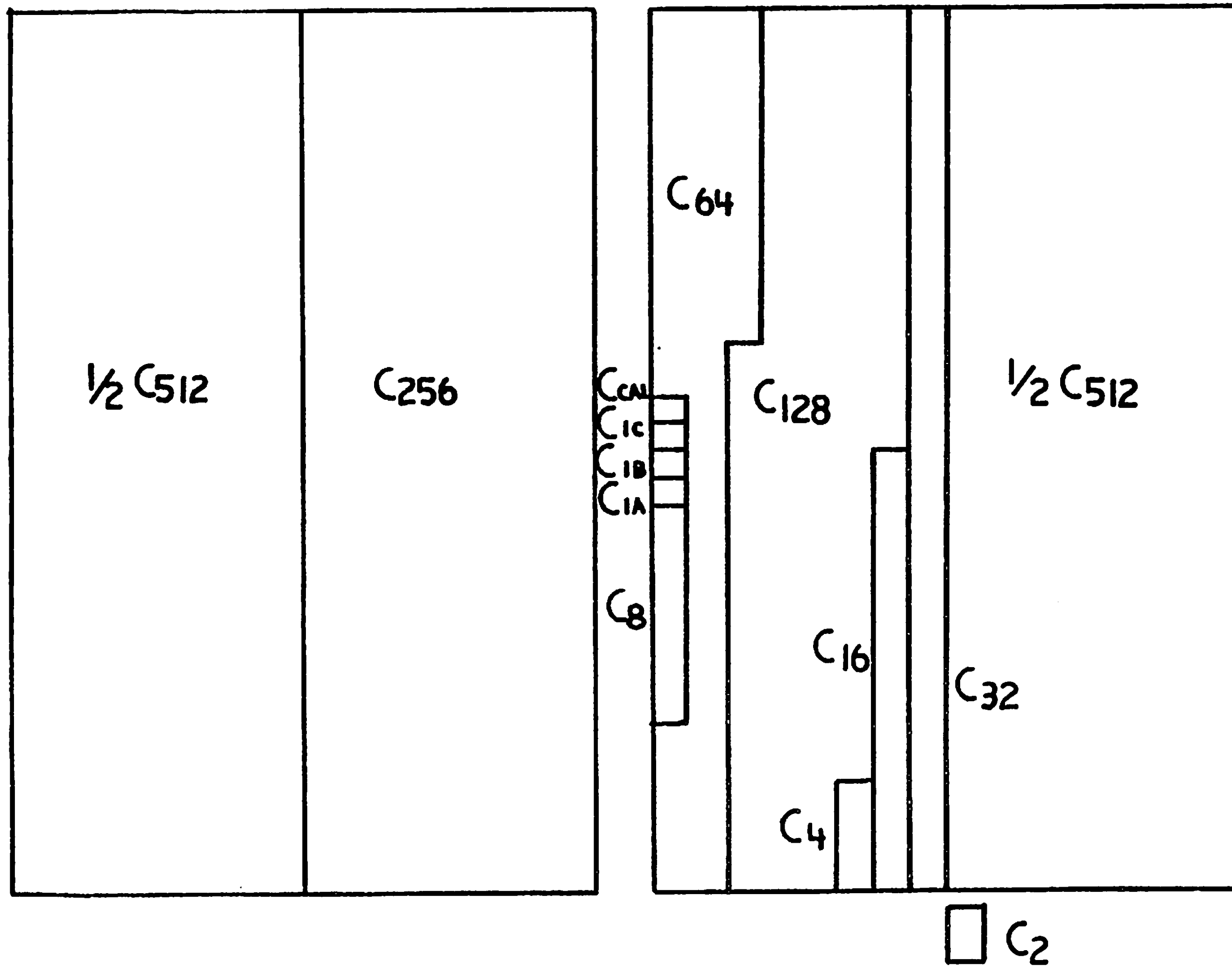


FIG. 8.2 ARRANGEMENT OF CAPACITORS

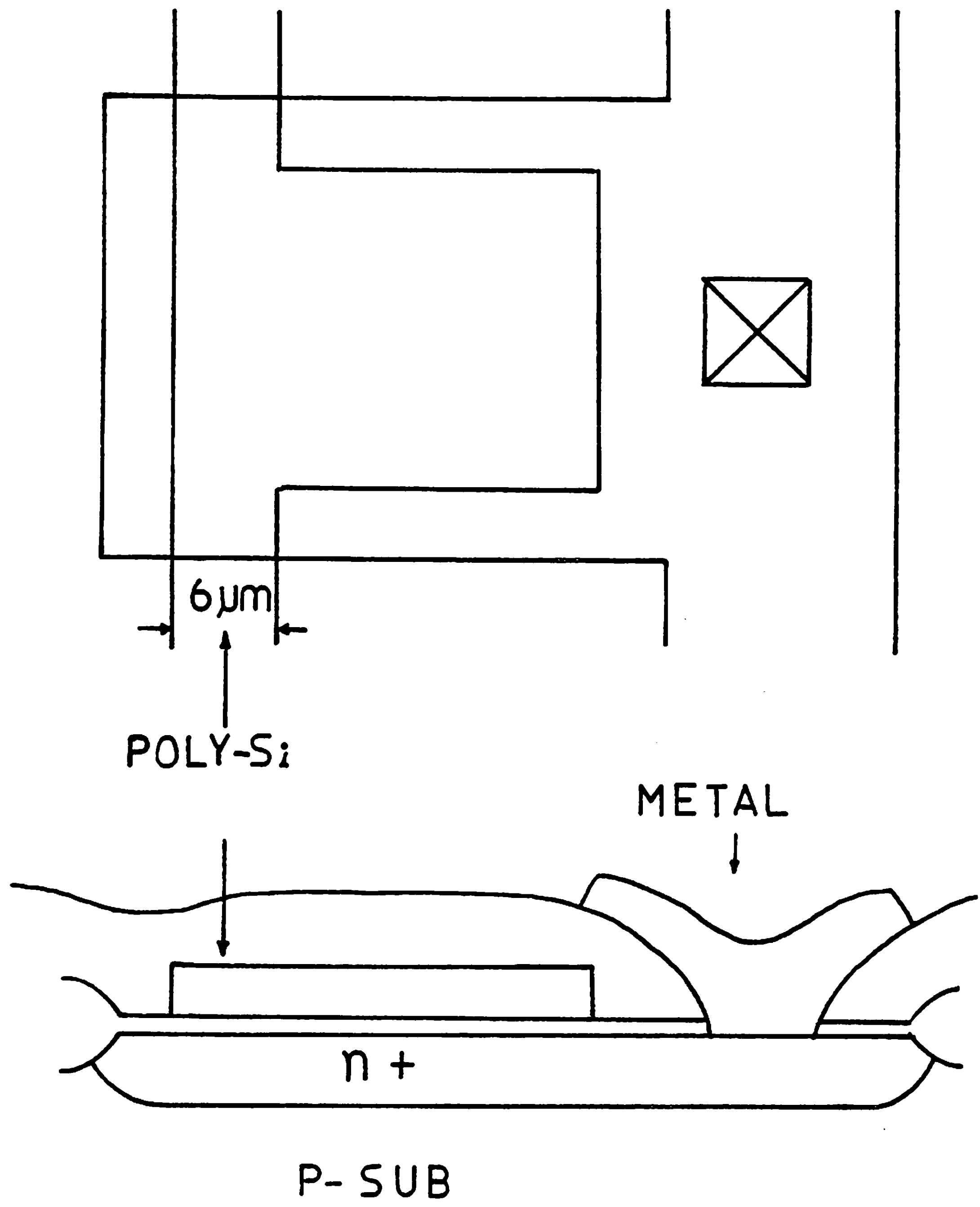


FIG.8.3 STRUCTURE OF UNIT CAPACITOR

FIG.8.4 TYPICAL SEGMENT OF R-STRING

FIG. 8.5 SCHEMATIC DIAGRAM OF PROTOTYPE IC

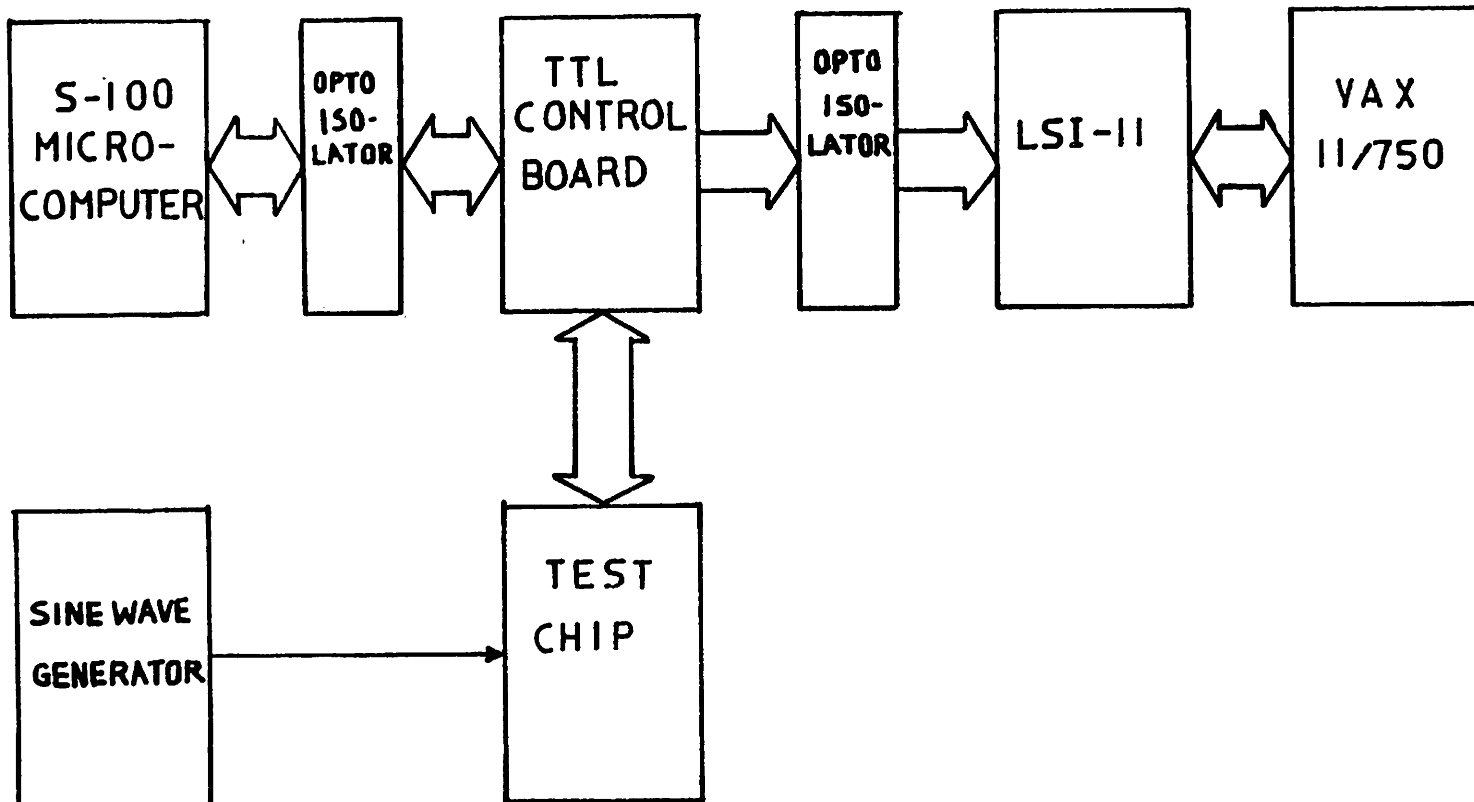


FIG. 8.6 TEST SETUP

MEASURED BY CALIBRATION

NUMBERS ARE STATED IN LSBs AT 16 BIT LEVEL

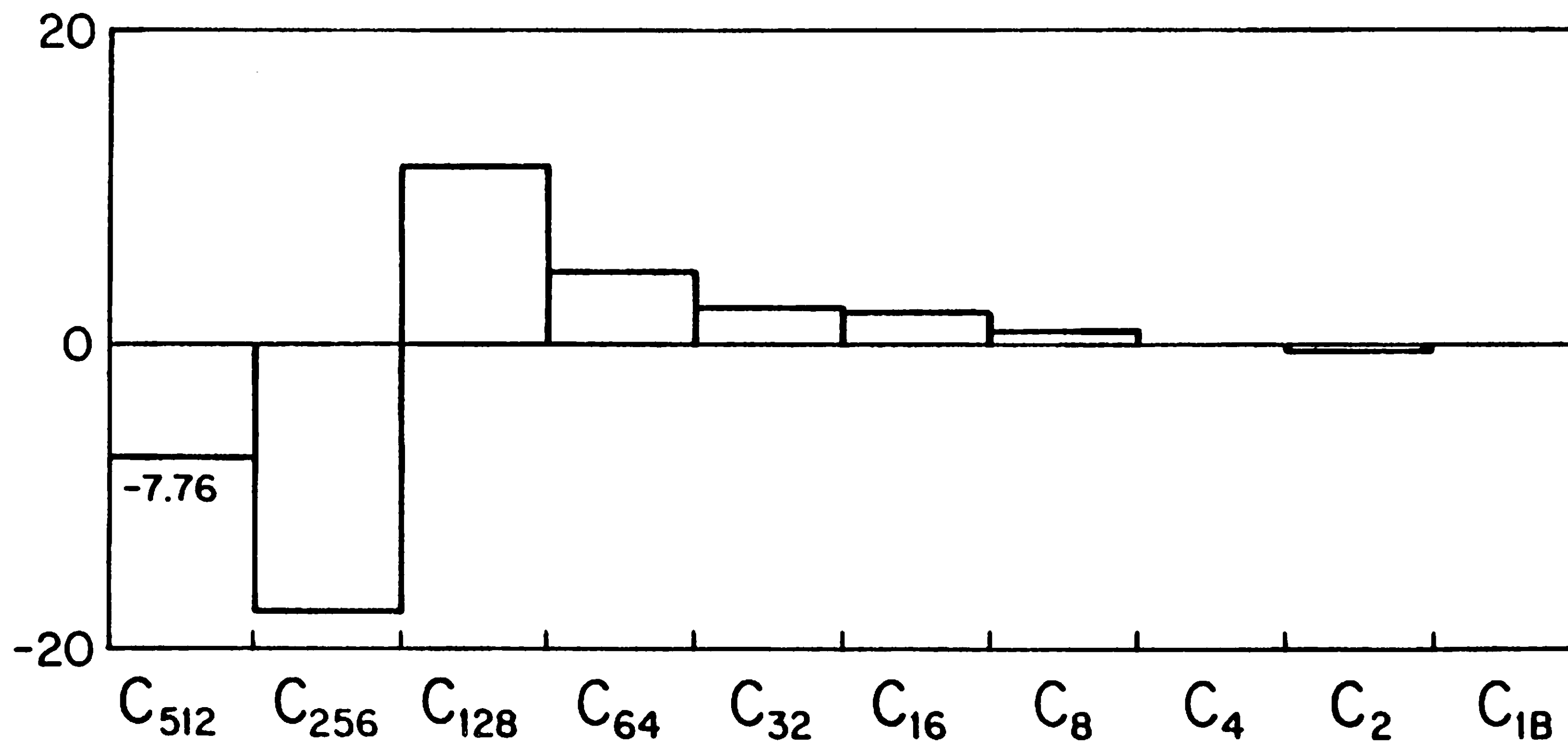


FIG.8.7 TYPICAL CORRECTION TERMS

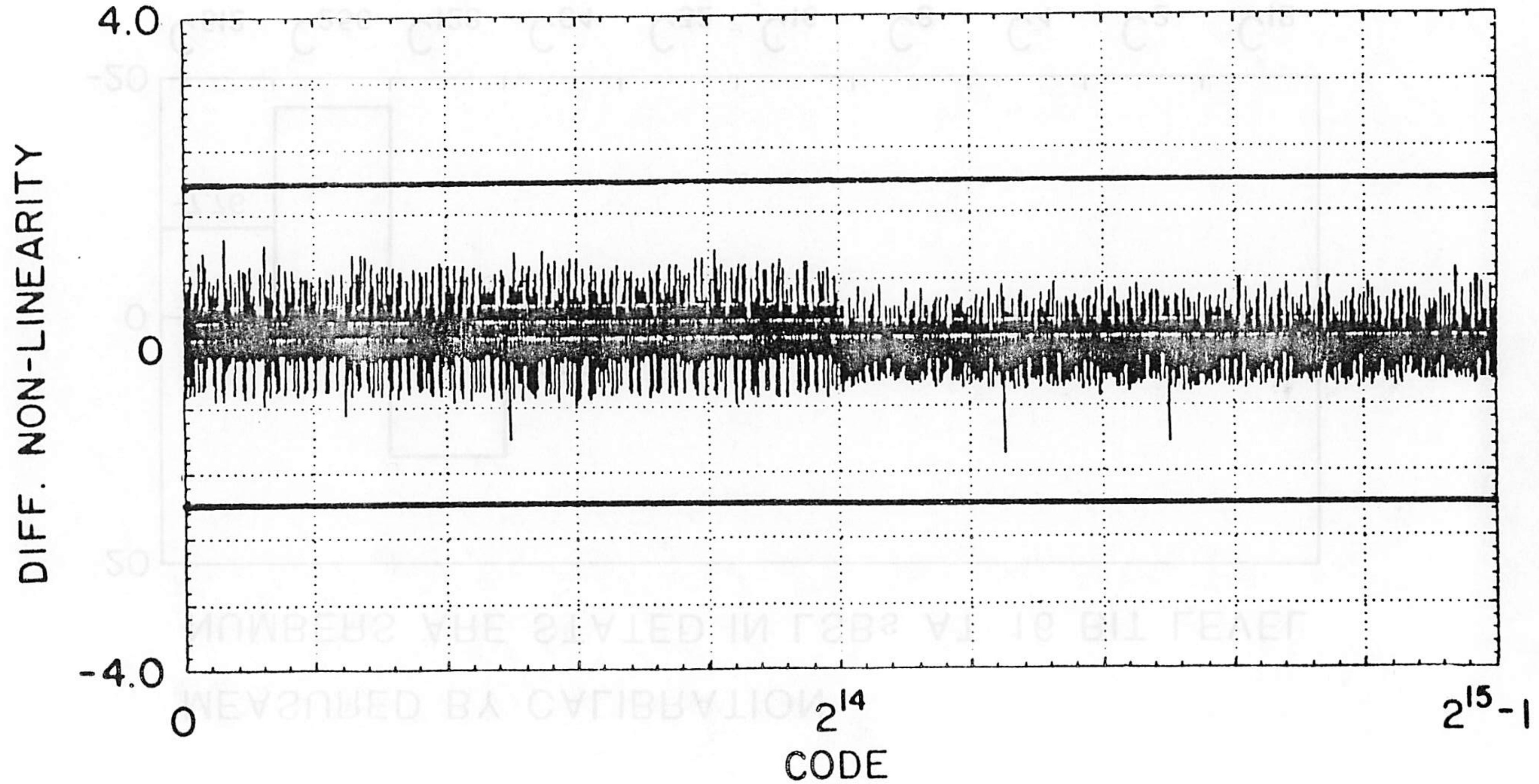


FIG. 8.8 MEASURED DIFFERENTIAL NON-LINEARITY

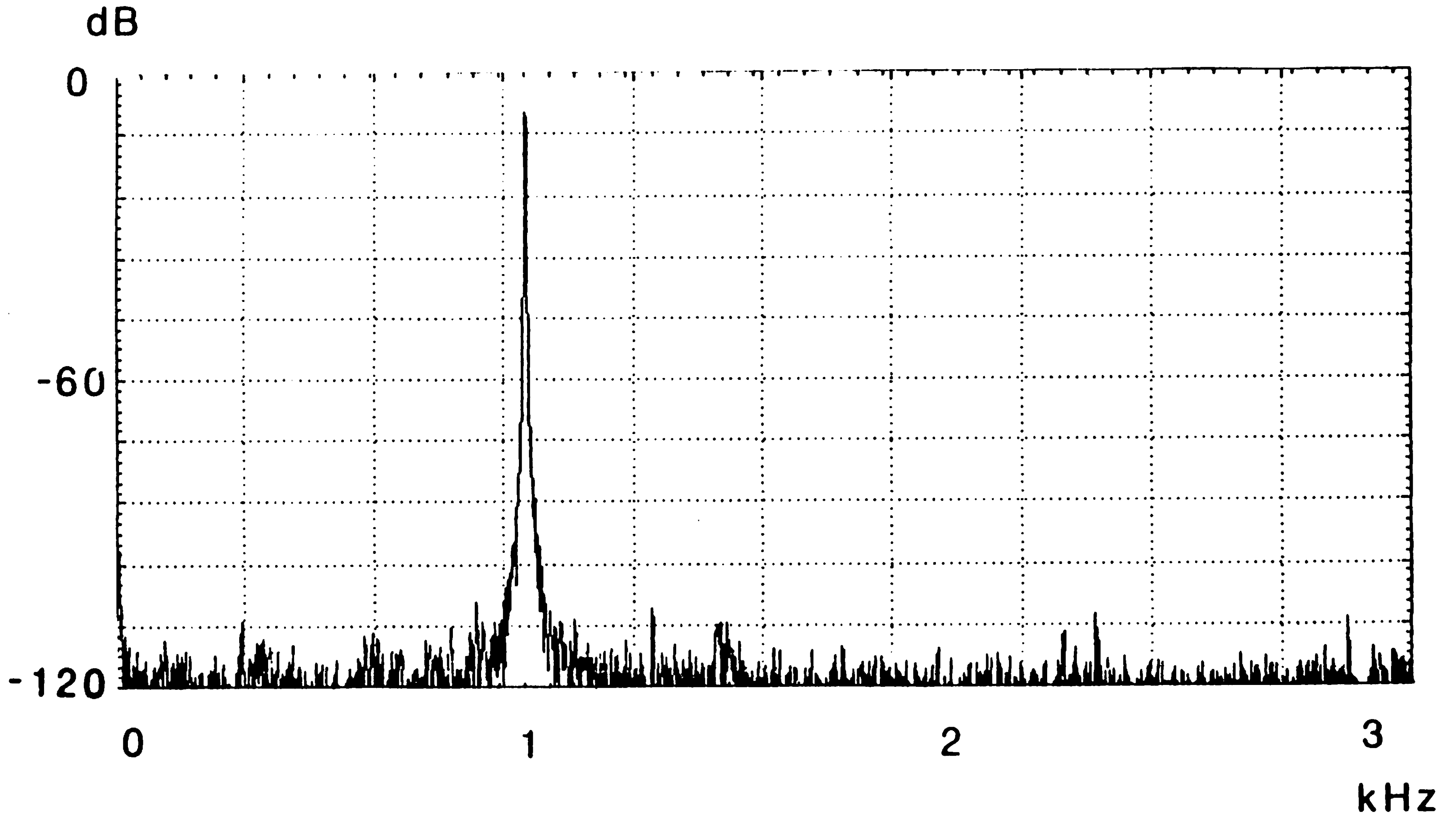


FIG. 8.9 MEASURED HARMONIC DISTORTION

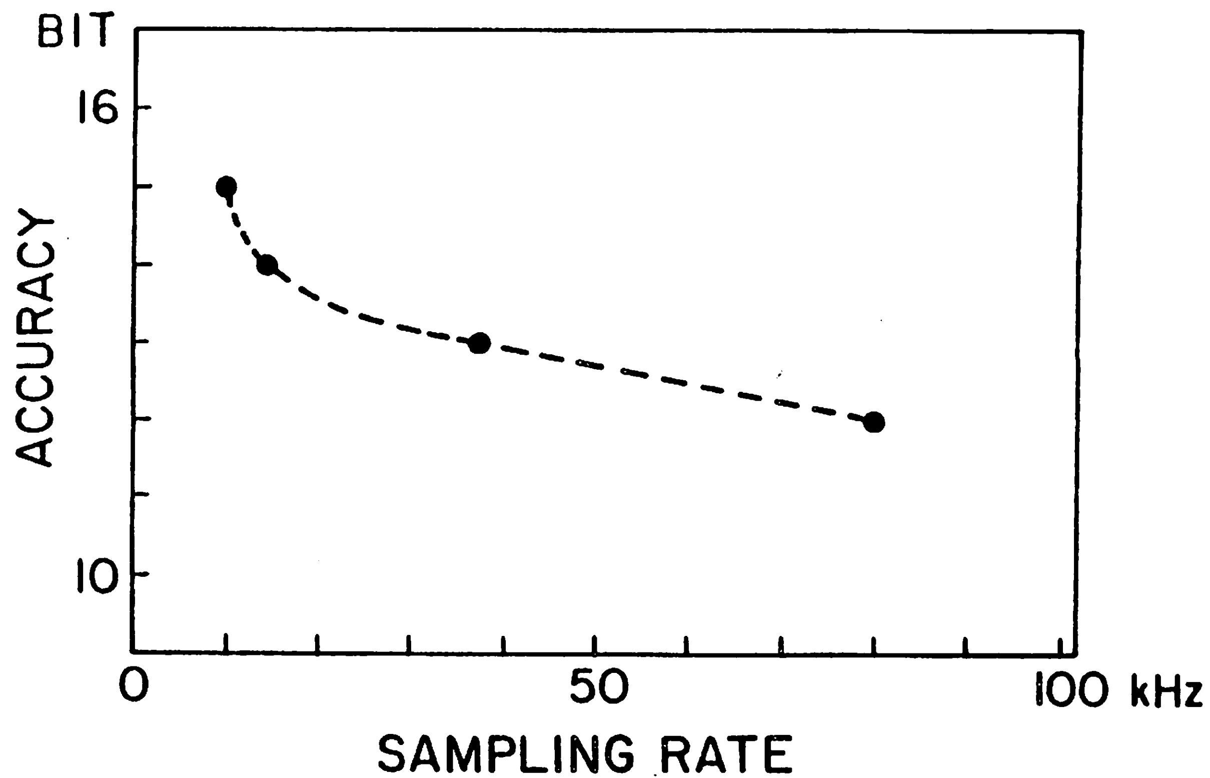


FIG 8.10 SPEED-ACCURACY CHARACTERISTIC

POWER SUPPLY	±5V
RESOLUTION	30μV
WORST CASE DELAY	3μS
INPUT REFERRED NOISE	20μV *
POWER DISSIPATION	10mW
SETTLING TIME	1.5μs
DIE AREA	0.65 mm^2

* SIMULATED VALUE

TABLE 8.1 COMPARATOR PERFORMANCE

TESTED AT ROOM TEMPERATURE	
POWER SUPPLY	±5V
RESOLUTION	15 BIT
LINEARITY	15 BIT
OFFSET	<±1/2 LSB
RMS NOISE	40μV
DIE AREA	7.5 mm^2

TABLE 8.2 CONVERTER PERFORMANCE

CHATER 9

CONCLUSIONS

The resistive - capacitive composite analog-to-digital converter technique is analyzed. This composite structure reduces DAC element ratio, and provides inherent sample and hold capability. Resistor string main DAC - weighted capacitor sub DAC structure gives an excellent monotonicity. Linearity, however, is limited by the gradient in the sheet resistivity. Weighted capacitor main DAC - resistor string sub DAC structure has potentially much better linearity because the limiting factor, the voltage coefficient of the capacitors, is usually very small.

A new method of improving the accuracy of analog-to-digital converters is discussed and analyzed. The prime application of this self-calibration technique is on the weighted capacitor main DAC - resistor string sub DAC composite structure. The inherent sample and hold capability of this structure lends itself to a convenient bit value comparison for the calibration. During the calibration cycle, linearity error of the main DAC is measured by comparing each bit and its complement. The measured linearity error is stored in RAM in a digital form to be used in A/D conversion cycles. Due to an excellent stability in the capacitor ratios, the calibration only has to be performed typically after each power-up.

The factors that can affect the accuracy of a self-calibrating A/D converter are analyzed. Factors such as residual offset voltage, voltage coefficient of capacitors, and coupling capacitor error can be corrected by simple techniques. Random noise during the calibration can be reduced by digitally averaging the correction terms. The ultimate limit would be thermal noise in the comparator

which can also be improved by a shorter channel/ thinner oxide MOS process.

A CMOS comparator capable of resolving 30 μV has been designed for the purpose of being used in the self-calibrating A/D converter. A folded cascode amplifier together with pole-zero cancellation frequency compensation technique provided a fast open loop delay as well as good closed loop performance. By the closed loop offset sampling, the offset voltage and $\frac{1}{f}$ noise is greatly reduced.

A fully dynamic testing method for testing fast, high resolution A/D converter has been developed. By the code density test, the dynamic behavior of an A/D converter can be completely characterized in a short time. FFT test can be used for integral non-linearity test.

An experimental chip fabricated using 5 μm rule standard CMOS process demonstrated initial linearity of 9 bits. After the calibration, 15 bit accuracy at 12 kHz sampling rate was achieved. 16 bit 50 kHz performance should be possible by a more careful layout to improve initial matching and to better isolate the analog signal from the digital switching noise.

Appendix I. Berkeley CMOS Process

Introduction

This high performance CMOS process was originally developed by R. Kaneshiro and T. Choi [10] and later improved by the author and P. Li [31]for better process control and reproducibility. Featuring 5μm minimum gate length and 500 Å gate oxide, this process is fully compatible with analog and digital CMOS circuits.

Unlike the original Berkeley CMOS process, gate oxide is regrown after the local oxidation. The buffer oxide under the silicon nitride undergoes a large thermal stress during the local oxidation. When used as a gate oxide, the buffer oxide exhibited low breakdown voltage and sometimes a large leakage current. Thus, in the improved process, the buffer oxide is removed after the local oxidation, and fresh oxide is regrown for the better quality oxide. Also, to prevent any leakage from the gate to source or drain through CVD glass, polysilicon regrowth step is added. These modifications resulted in much better device characteristics.

Other important modifications are the simplifications eliminating many elaborate steps for better process control. In the original process, three nitride etching steps were needed, one for n-channel active area, one for p-channel active area, and another for the capacitor area , all of which needed critical photolithography.

In the new process, nitride etching steps are combined into one giving only one critical photolithography and etching step. However, thicker nitride is needed to block the field stop implantation from the active area. Minimum of 1500 Å nitride is deposited to mask 25 keV boron implantation [49]. Also, the

local oxidation temperature is raised to 950 °C where oxide is more viscous [50].

Aluminum-silicon sputtering is used instead of complicated paladium-silicide and aluminum metalization [51].

Process Flow

1. INITIAL WAFER PREPARATION

1.1. Piranha Clean

Clean for 10 mins using glass or teflon beakers and holders. Do not use plastic beakers. Piranha will attack most plastics and leave deposits on the wafers. Never clean wafers and tweezers together.

1.2. Oxide Dip and Water Break Test

Dip the wafer in 10:1 solution of HF until the wafer becomes hydrophobic. HF solution will completely clear off the surface if the wafer has been properly cleaned.

2. INITIAL OXIDATION

Grow 3000 Å of oxide in the initial oxidation furnace. TCA clean the furnace prior to oxidation.

TEMP=1100

Push	Ox	5.0	5 min
Ox	Ox	5.0	240 min
Anneal	N_2	5.0	10 min
Pull	N_2	5.0	5 min

3. N-WELL DEFINITION

3.1. Standard Photolithography

HMDS	3 min
N_2 purge	5 min
Spin Resist	AZ1350J 6000 rpm/30 sec
Soft Bake	90 °C/15 min
Pattern	Cannon 5.6
Develop	MicroPosit Developer:DI =1:1 /60sec

3.2. Oxide Etch

BHF 2 min

prepare the BHF solution at least 24 hours prior to use to get reproducible etch rate.

3.3. Photoresist Removal

Acetone	2 min
Methanol	1 min
DI rinse	1 min
Piranha	5 min

3.4. N-Well Implantation

Phosphorus 100 keV 8 ° 1.5×10^{12}

3.5. N-Well Drive-In

Buried layer furnace - TCA clean prior to use

Piranha clean 5 min

Temp = 1100 °C

Push	N_2	15 cm	3 min
Oxidation	O_2	15 cm	280 min

Ramp temp to 1150 °C

Drive-in	$N_2 : O_2$	5.0 cm : 15 cm	720 min
Anneal	N_2	10 cm	20 min
Pull	N_2	10 cm	3 min

The drive-in is performed in 10% O_2 atmosphere

4. Buffer Oxidation

4.1. Oxide Etch Back

HF : DI = 1 : 5

Etch until wafer becomes hydrophobic (~8 min)

4.2. Oxidation

Piranha clean 3 min

N-drive furnace - TCA clean prior to use

target : 550 Å

Temp = 1000 °C

Push	N_2	10 cm	3 min
Oxidation	O_2	11 cm	50 min
Anneal	N_2	10 cm	10 min
Pull	N_2	10 cm	3 min

5. Nitride Deposition

Load 2 wafers at a time, facing outward. Better uniformity can be obtained by loading the wafer facing inside, which takes a considerably longer time and gives more particular contamination. Use 4 dummy slats (half wafers) to smooth out the gas flow.

To prevent contamination, nitride should be deposited immediately after the oxidation.

Target : 1500 Å

NH_3 600 mT

SiH_4 100 mT

Determine the deposition time by a dummy run. deposition rate varies significantly at times.

6. Active Area Definition

6.1. Standard Photolithography

6.2. Nitride Etch

Descum is necessary to remove photo resist residue. Use barrel reactor. 5 mins. of 10W O_2 plasma at 65 °C is enough.

Etch Plasma-Therm SF_6O_2 60°C 100 W

Determine the etch rate by a dummy run. Approximately 10 min is needed.

7. P-Field Definition

7.1. Standard Photoresist Removal

7.2. Standard Photolithography

7.3. P-Field Implantation

Boron 100 keV 8 ° 1.5×10^{13}

8. Backside Implantation

8.1. Standard Photoresist Removal

8.2. Spin on Protective Photoresist

Prebake	IR or 115°C Oven	
HMDS	3 min/5 min Purge	
AZ-1350J	5000 rpm	30 sec
Hard bake	115 °C	10 min

8.3. Backside Oxide Etch

Etch in BHF until wafer becomes hydrophobic.

8.4. Implantation

BF_2 200keV 8 ° 2×10^{15}

9. LOCOS

9.1. Standard Photoresist Removal

9.2. Oxidation

P-Drive Furnace. Target : 8500 Å

Temp = 950 °C

Push	N_2	5 cm	3 min
Oxidation	Wet O_2	2 cm	255 min
Anneal	N_2	10 cm	20 min
Pull	N_2	10 cm	3 min

Set the bubbler heater to 110 V. 2 refills of the bubbler are needed at this setting. Switch the gas to nitrogen during refills and subtract this time from the oxidation time.

10. Nitride Removal

Oxide Dip: HF : DI 1 : 10 40 sec

This HF dip removes thin oxide grown over nitride during LOCOS.

Phosphoric Acid 155 °C 30 min

Use reflux to maintain the temperature at 155 °C.

11. Threshold Implantation

Boron 50 keV 8 ° 7×10^{11}

Compensate for noise

12. Capacitor Area Definition

12.1. Standard Photolithography

12.2. Pre-implantation Bake

N_2 1 Torr 60 W 30 min

12.3. Capacitor Implantation

Phosphorus 80 keV 8 ° 2.5×10^{15}

Allow minimum of 20 mins per wafer to avoid damage to the photoresist

13. Gate Oxidation

13.1. Photoresist Removal

Plasma Ash O_2 1 Torr 30 min

Piranha 5 min

13.2. Buffer Oxide Removal

HF : DI 1 : 10 80 sec

13.3. Oxidation

N Drive-in Furnace : TCA Clean prior to use

Target : 500 Å

Temp = 1000 °

Push	N_2	10 cm	5 min
Oxidation	O_2	11 cm	45 min
Anneal	N_2	10 cm	10 min
Pull	N_2	10 cm	5 min

14. Polysilicon Deposition/Doping

14.1. Piranha Clean

Clean for 10 mins. Use teflon tweezer only. Metal tweezer will create a nucleation center to cause a milky polysilicon.

14.2. Polysilicon Deposition

Polysilicon should be deposited right after the oxidation to prevent contamination. Place wafers with the active side facing each other. Dummy slats are not necessary.

Target : 3500 Å

SiH_4 600 mT

Determine the deposition rate by a dummy run.

14.3. Polysilicon Doping

N-predep Furnace

Temp = 950 °C			
Push	N_2	4 cm	5 min
Oxidation	$O_2 : N_2$	2.5 cm : 5 cm	10 min
Doping	$O_2 : N_2 : POCl_3$	2.5 cm : 5 cm : 3 cm	30 min
Anneal	N_2	4 cm	5 min
pull	N_2	4 cm	5 min

Turn on the source cooler 30 mins. prior to doping.

15. NMOS Definition

15.1. Deglaze

HF : DI 1 : 10 10 sec

The phosphorus rich glass should be removed on which photoresist will not adhere.

15.2. Standard Photolithography

15.3. Standard Plasma Etch

Descum - Etch in Plasma Term

Polysilicon etches much faster than nitride. The etch rate should be determined by a dummy run.

15.4. Standard Photoresist Removal

15.5. NMOS S/D Implantation

As 180 keV 8 ° 3×10^{15}

16. PMOS Definition

16.1. Piranha Clean

16.2. Standard Photolithography

16.3. Standard Plasma Etch

Due to the implantation damage, polysilicon etches faster at this time. Be careful not to over-etch.

16.4. Pre-implantation Bake

N_2 1 Torr 60 W 45 min

16.5. PMOS S/D Implantation

Boron 60 keV 8 ° 2×10^{15}

Allow at least 20 mins per wafer.

16.6. Photoresist Removal

Plasma Asher O_2 1 Torr 120 W 40 min

Piranha Clean 5 min

16.7. Polysilicon Re-oxidation

P-drive Furnace

Temp = 1000 °C

Push	N_2	10 cm	5 min
Oxidation	O_2	11 cm	30 min
Anneal	N_2	10 cm	10 min
Pull	N_2	10 cm	5 min

17. CVD Passivation

17.1. Piranha Clean

17.2. CVD Glass Deposition

3500 Å	Undoped CVD Glass
6500 Å	7 % PSG

Due to high reflow temperature, a sandwich layer of undoped CVD glass is needed to prevent counter doping of p+ regions.

17.3. Reflow

N Drive-in Furnace

Temp = 1050 °C

Push	N_2	5 cm	5 min
Reflow	N_2	5 cm	20 min
Push	N_2	5 cm	5 min

18. Contact Definition

18.1. Standard Photolithography

Increase the light dose to 5.9

18.2. Contact Hole Etch

Etch in BHF

Bake 130 °C 10 min

Repeat etch-bake cycles as many times as required to prevent contact cut blooming. Recommended etching times are 15 sec., 30 sec., 45 sec., 60 sec., 90 sec. and then repeat 120 sec. etch until all the contact hole monitors are clear of oxide. Then over etch for 1 min to assure a complete etch.

18.3. Standard Photoresist Removal

19. Metalization

19.1. Oxide Dip HF : DI 1 : 10 5 sec

This oxide dip removes a thin oxide grown over the vials during the piranha clean. Be careful not to over etch the CVD glass. PSG etches extremely fast.

19.2. Pre-metalization Bake

Throughly dry the wafer under IR lamp or 110 °C oven.

19.3. Aluminum Sputtering

Target : 0.75 μm

20. Metal Run Definition

20.1. Standard Photolithography

Due to a high reflectivity of aluminum, the exposure should be reduced to 5.5.

20.2. Aluminum Etch

Aluminum Etchant Type A 40 °C

Approximately 90 sec. is needed. Allow 10 sec. over etch after all the aluminum is gone over the unmasked area.

21. Backside Metalization

21.1. Protective Photoresist Spin-on

IR Bake 20 min

AZ-1350J 5000 rpm 30 sec

Hard Bake 120 °C 20 min

21.2. Backside Polysilicon Etch

Polysilicon on the backside of the wafer is not removed if Plasma-Therm is used for the polysilicon etch. It should be removed before the backside metalization.

Standard Plasma Etch

21.3. Backside Oxide Etch

Etch in BHF until the wafer becomes hydrophobic.

21.4. Aluminum Sputtering

Target : 1 μm

21.5. Photoresist Removal

Acetone 3 min - Methanol Rinse - DI Rinse

22. Sintering

Sintering Furnace

Temp = 375 °C

Forming Gas   15 cm   20 min

Appendix II

A Precision Measurement Technique for Residual Polarization

Introduction

Non-ideal characteristics of MOS integrated circuit capacitors can affect the performance of data converters, switched-capacitor filters, and many other circuits. Voltage and temperature coefficients of capacitance have been analyzed and measured by McCreary. [18]

Ionic contamination of silicon dioxide, typically with sodium, results in hysteresis in capacitor charge-voltage (Q-V) characteristics as well as shifts in MOS transistor threshold voltage. These effects occur on a time scale measured in seconds to hours, and are more important to long-term transistor characteristics than to data converters and filters which are normally re-initialized on a microsecond time scale. Intensive efforts have drastically reduced ionic contamination in MOS integrated circuit processes.

Fast mechanisms for dielectric polarization or hysteresis, such as the ferroelectric effect, are known to exist for some materials [23]. Similar effects have been observed in phosphorus-rich SiO_2. [24,52] Any residual polarization in the capacitors of a weighted-capacitor data converter will impose a limitation on linearity which is difficult or impossible to overcome at the circuit or system level. In the course of work on very high resolution data converters employing MOS capacitors with phosphorus-doped single-crystal and polysilicon plates, we were motivated to find a direct method of measuring possible dielectric polarization in MOS capacitors with resolution far better than is achievable by

conventional MOS capacitance-voltage (C-V) measurements.

Measurement of residual polarization is especially difficult for integrated circuit capacitors of small values (10 - 100 pF). The need to cycle capacitor voltages in 1 to 10 μs (corresponding to normal operating speed for a data converter) further increases measurement problems. We have overcome the noise and speed problems through use of a high-resolution CMOS voltage comparator on the same chip as the integrated capacitors. Further reduction of the noise is achieved through off-chip digital signal averaging.

Details of Measurement

Fig. A1 illustrates a possible (exaggerated) polarization curve of a capacitor [23]. The residual polarization appears as residual charge Q_r. This residual charge can be measured by the test circuit shown in Fig. A2. A pair of nominally-identical capacitors C_1 and C_2 and a much smaller coupling capacitor C_C are needed. A high-resolution voltage comparator and a digital-to-analog converter (DAC) are used to digitize the residual charge. In this experiment, two 60 pF capacitors, a 0.12 pF capacitor and an on-chip 7 bit resistor string DAC were used [39].

Consider the switching sequence shown in Fig. A2. Here, the two larger capacitors are assumed to be identical in value. First, both capacitors are charged to a fixed voltage $-V_1$. This ensures both capacitors are polarized in the same direction, and have identical residual polarization in the beginning. Next, C_1 is charged to $+V_1$ and C_2 is discharged to ground. The initial charge in C_1 and C_2 at this point is:

$$Q_{1i} = -Q_r$$

$$Q_{2i} = \int_0^{V_1} C_{1\to 2}(V)dV$$

Thus the total initial charge is:

$$Q_i = Q_1+Q_2 = \int_0^{V_1} C_{1\to2}(V)dV - Q_r$$

Then, the switch S_1 is turned off, and the voltages on the capacitors are exchanged. The final charges on the capacitors are:

$$Q_{1f} = \int_0^{V_1-V_X} C_{1\to2}(V)dV \approx Q_i+Q_r-C_{1\to2}(V_1)V_X$$

$$Q_{2f} = Q_r + \int_0^{-V_X} C_{2\to1}(V)dV \approx Q_r-C_{2\to1}(0)V_X$$

If the hysteresis loop is small:

$$C_{1\to2}(V_1) \approx C_{2\to1}(0) \approx C$$

Thus the total charge after the redistribution of charge is :

$$Q_f = Q_{1f}+Q_{2f}$$
$$= Q_i+2Q_r-2CV_X$$

Using $Q_f = Q_i$ from the charge balance equation and solving for V_X :

$$V_X = \frac{Q_r}{C} \tag{A2.1}$$

This voltage can be digitized using the DAC and the voltage comparator by a successive-approximation search. The resolution of this measurement is given by:

$$\Delta V = \frac{V_{ref}\, C_C}{2^N(\, 2C+C_C\,)} \tag{A2.2}$$

Since V_X is known to this resolution, from equation A2.1 the resolution level for Q_r is :

$$\Delta Q = C\Delta V$$

The relative resolution $\frac{\Delta Q}{Q_{TOT}}$ is therefore :

$$\frac{\Delta Q}{Q_{TOT}} = \frac{\Delta Q}{CV_1}$$

$$= \frac{V_{ref}}{2^N V_1} \cdot \frac{C_C}{(2C+C_C)} \quad (3)$$

where V_{ref} is the full scale voltage of the DAC and N is the resolution of the DAC. In the actual measurement setup of Fig. 2, $V_1 = V_{ref} = 4V$. Therefore, from (3) the resolution corresponding to this setup is 8 parts per million (ppm) with 4V across the capacitor.

In reality, there are several problems associated with this basic switching sequence. The offset voltage of the comparator, charge injection from MOS switch S_1 and capacitor ratio mismatch would be indiscernible from the residual polarization. However, these factors can be separated using the improved switching sequence of Fig. A3 and Fig. A4. Here, the two larger capacitors are assumed to be slightly different:

$$C_1 = C+\Delta C$$

$$C_2 = C-\Delta C$$

In Fig. A3, the offset voltage of the comparator and the charge injection from the MOS switch are lumped together as V_{OS} since both of them cause an offset error in the measurement. This offset error V_{OS} can be measured using the DAC by a successive approximation search. Two measurements in opposite sequence are needed to eliminate the measurement error due to capacitor mismatch. In the precharge mode of Fig. A3a and Fig. A3c, the DAC is switched to digitize V_{OS}. It should be noted that these precharge cycles are preceded by charging both capacitors to $-V_1$. In the redistribution mode of Fig. A3b and Fig.

A3d, the DAC is switched back to all 0's. This operation will precisely cancel the effect of both the comparator offset voltage and the charge injection.

In Fig. A3a and A3b, V_1 is sampled on C_1 and then redistributed. The voltage at node (a) is :

$$V_{X1} = \frac{\Delta C}{C} V_1 + \frac{Q_r}{C} \tag{A2.4}$$

In the opposite sequence of Fig. A3c and Fig. A3d, V_1 is sampled on C_2 :

$$V_{X2} = -\frac{\Delta C}{C} V_1 + \frac{Q_r}{C} \tag{A2.5}$$

In these equations, the cross-product terms are neglected. By adding equation A2.4 and equation A2.5 :

$$\frac{2Q_r}{C} = V_{X1} + V_{X2} \tag{A2.6}$$

Thus the residual polarization at V_1 is

$$\frac{Q_r}{CV_1} = \frac{V_{X1} + V_{X2}}{2V_1}$$

The resolution is doubled compared to that of equation A2.3, and is therefore 4 ppm.

To prevent the DAC from overflowing, the range of the DAC and the value of the coupling capacitor should be properly chosen. The general rule of thumb is:

$$\max(|V_{OS}|, |V_{X1}|, |V_{X2}|) \leq \frac{V_{ref} C_C}{4C} \tag{A2.7}$$

The residual polarization of MOS capacitors with polysilicon top plate and phosphorus doped bottom plate was measured using the technique described above. Signal voltage was 60 μV, and the system noise was 40 μV. Each meas-

urement was taken 16 times and digitally averaged reducing effective noise to 10 μV. The residual polarization measured this way was unmeasurably small at 4 ppm resolution level.

Also under investigation are techniques to measure slow surface state density and hot electron trapping with slightly modified test structures [53].

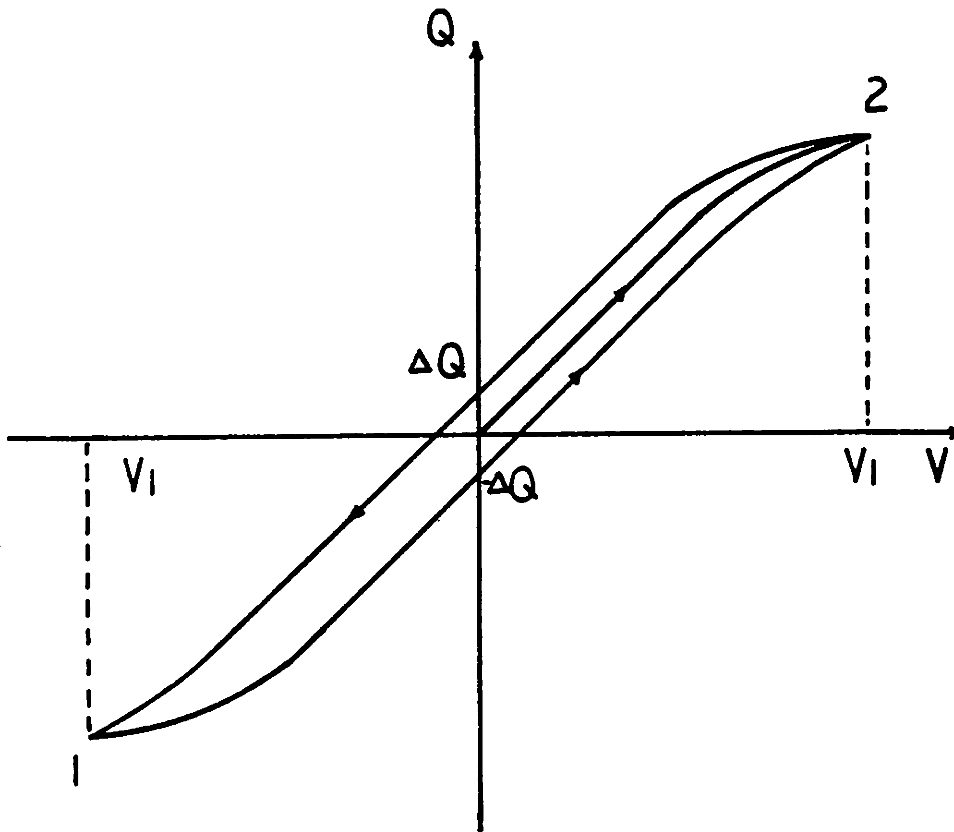


FIG. A1 POLARIZATION CURVE

OF A CAPACITOR

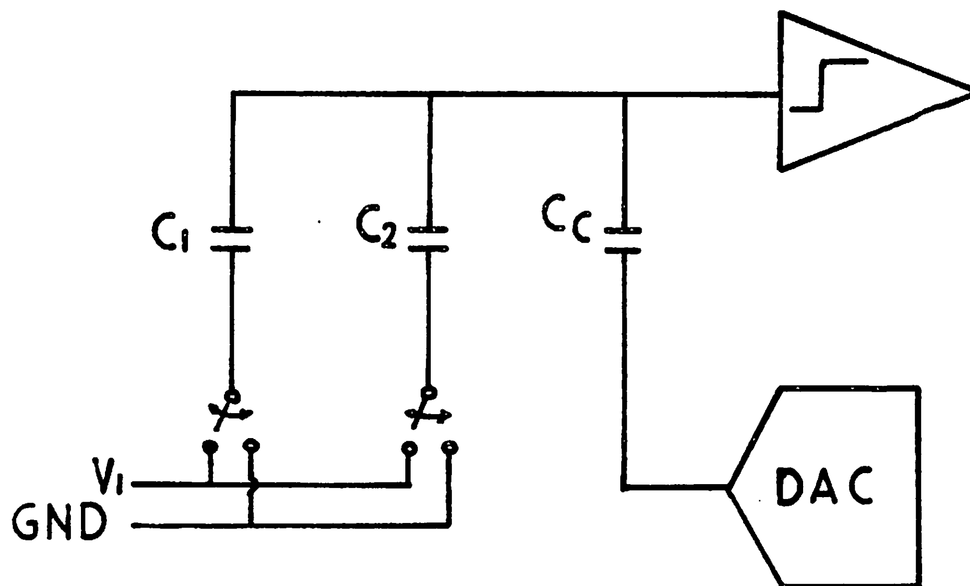


FIG.A2 MEASUREMENT SETUP FOR RESIDUAL POLARARIZATION

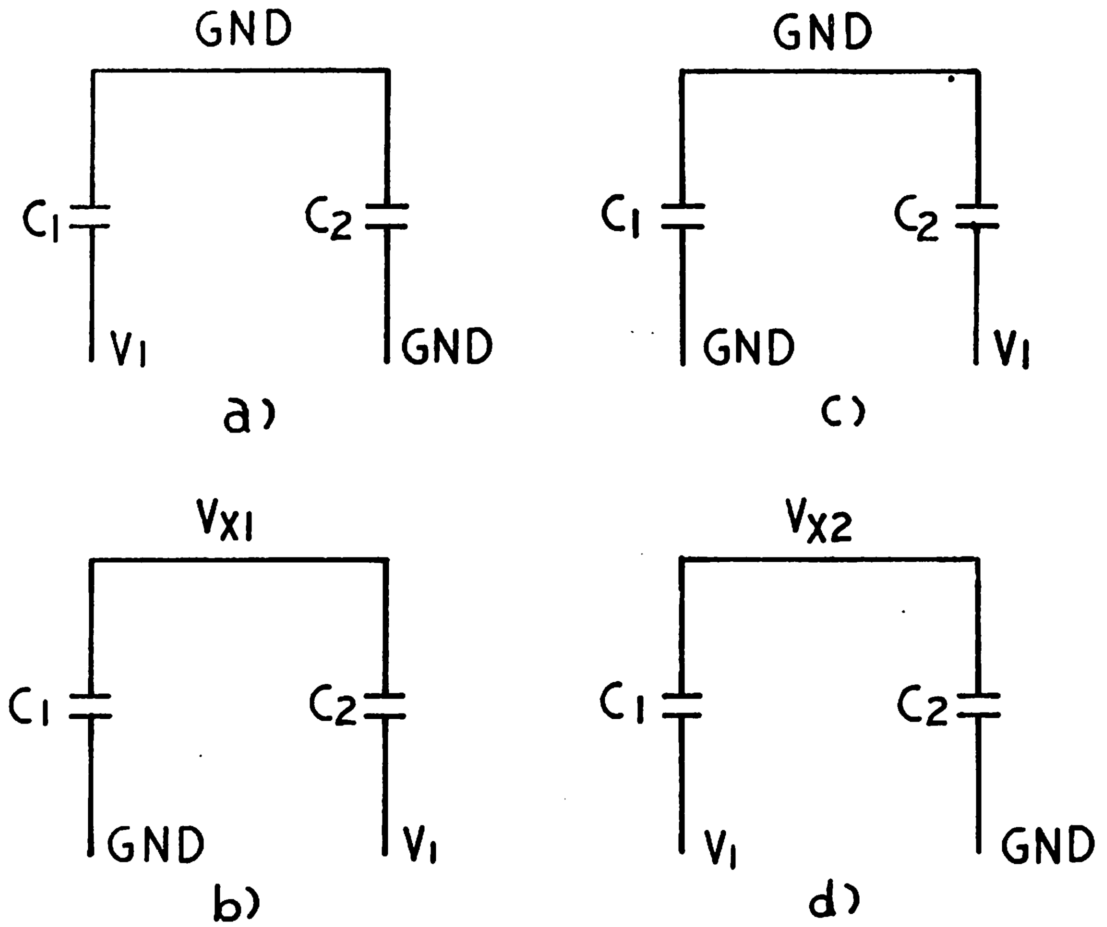


FIG. A3 IMPROVED SWITCHING SEQUENCE

Appendix III

Effect of Drift in Offset Voltage, Input Amplitude and Reference Voltages on Integral Linearity Test

Introduction

When the code density test described in Chapter 7 is used for the integral linearity test, the drift in the offset voltage, amplitude variation of the input sine wave, and decay of the reference voltages can cause incorrect results. This effect is particularly significant at high resolution level over 14 bits.

Effect of each factor on the integral linearity test is analyzed here.

Drift in Input Amplitude or Symmetrical Drift in Reference Voltages

A drift in the amplitude of input sine wave has the same effect on the integral linearity test as a symmetrical drift in the reference voltages. In a relative sense, a variation in the amplitude can be interpreted as a variation in the reference voltages in the opposite direction.

When the drift is slow compared to the input signal, the probability density function including the drift term can be approximated:

$$P(v<V) = \frac{1}{2}+\frac{1}{\pi}\sin^{-1}\frac{V}{A}(1+\alpha t)$$

The expected cumulative number of codes from the negative full scale to the code i is then:

$$E[ch(i)] = \frac{N_{TOT}}{2}+ N_{TOT}\left\{\frac{F(x+\Delta x)-F(x)}{\Delta x}\right\}$$

where

$$F(x) = \int \sin^{-1}x\,dx$$
$$= \sin^{-1}x - \sqrt{1-x^2}$$

and

$$\Delta x = \frac{aTV}{A}$$

Here, x is the normalized voltage $\frac{V}{A}$. The transition points can now be computed using Equation 7.21.

$$x_i = -\cos\pi\left[\frac{1}{2} + \frac{F(x+\Delta x)-F(x)}{\Delta x}\right]$$
$$= \sin\frac{F(x+\Delta x)-F(x)}{\Delta x}$$

From the Taylor's series expansion:

$$\frac{F(x+\Delta x)-F(x)}{\Delta x} \cong F'(x) + \frac{\Delta x}{2}F''(x) + \frac{(\Delta x)^2}{6}F'''(x)$$
$$= \sin^{-1}x + \frac{\Delta x}{2}\frac{1}{\sqrt{1-x^2}} - \frac{(\Delta x)^2}{6}\frac{x}{\sqrt{1-x^2}^{\frac{3}{2}}}$$

Let $\Delta = \frac{\Delta x}{2}\frac{1}{\sqrt{1-x^2}} - \frac{(\Delta x)^2}{6}\frac{x}{\sqrt{1-x^2}^{\frac{3}{2}}}$.

Then:

$$x_i = \sin(\sin^{-1}+\Delta)$$
$$= x(1-\frac{\Delta^2}{2})-\Delta\cos x$$

Neglecting the third and the fourth order terms of Δx,

$$x_i = x - \frac{7}{24}\frac{x}{1-x^2}(\Delta x)^2$$

$$= x - \frac{7}{24}\frac{x^3}{1-x^2}(\alpha T)^2$$

The maximum deviation of x_i from linearity is thus:

$$IN = \frac{7}{24}(\alpha T)^2\left[\frac{x_m^2 x}{1-x_m^2} - \frac{x^3}{1-x^2}\right]$$

where $x_m = \frac{V_{ref}}{A}$. By differentiating the last equation, the maximum integral non-linearity can be found:

$$IN_{max} = \frac{1}{2}\frac{\sqrt{2x_m^2-1}}{1-x_m^2}$$

at

$$x = \pm\sqrt{2x_m^2-1}$$

From this equation, the maximum error in the test is proportional to the square of the total drift αT, and decreases with smaller $\frac{V_{ref}}{A}$. Thus, to reduce the sensitivity of the test to the amplitude or reference drift, larger amplitude should be selected for the input sine wave. A plot of the error for testing a 15 bit converter is shown in Fig. A4 and Fig. A5. Total drift αT is 12.5 LSB. In Fig. A4, two curves with $\frac{V_{ref}}{A} = 0.999$ and $\frac{V_{ref}}{A} = 0.99$ are plotted together. Fig. A5 is for $\frac{V_{ref}}{A} = 0.99$ at an expanded scale. Note that the curve is more spread out for larger $\frac{V_{ref}}{A}$.

Drift in Offset Voltage

In the similar way, the effect of drift in the offset voltage can be analyzed. The error in integral linearity test is:

$$IN = \frac{7}{24}(aT)^2\left[\frac{x}{1-x_m^2} - \frac{x}{1-x^2}\right]$$

This error is plotted in Fig. A6 and Fig. A7. Note the similarity to Fig. A4 and Fig. A5. Again, the sensitivity decreases with smaller $\frac{V_{ref}}{A}$. Total drift of 25 LSB is assumed in these plots.

Mismatch and Asymmetrical Drift in Reference Voltages

The effect of mismatch and asymmetrical drift in the reference voltages is more salient as can be seen in Fig. A8 and Fig. A9. Fig. A8 shows the error due to 12.5 LSB mismatch between the positive and the negative reference voltages. In Fig. A9, the positive reference voltage stayed unchanged, but the negative reference voltage drifted by 12.5 LSB. It can be concluded that accurate matching between the reference voltage should be maintained during the entire test for the accuracy in the test.

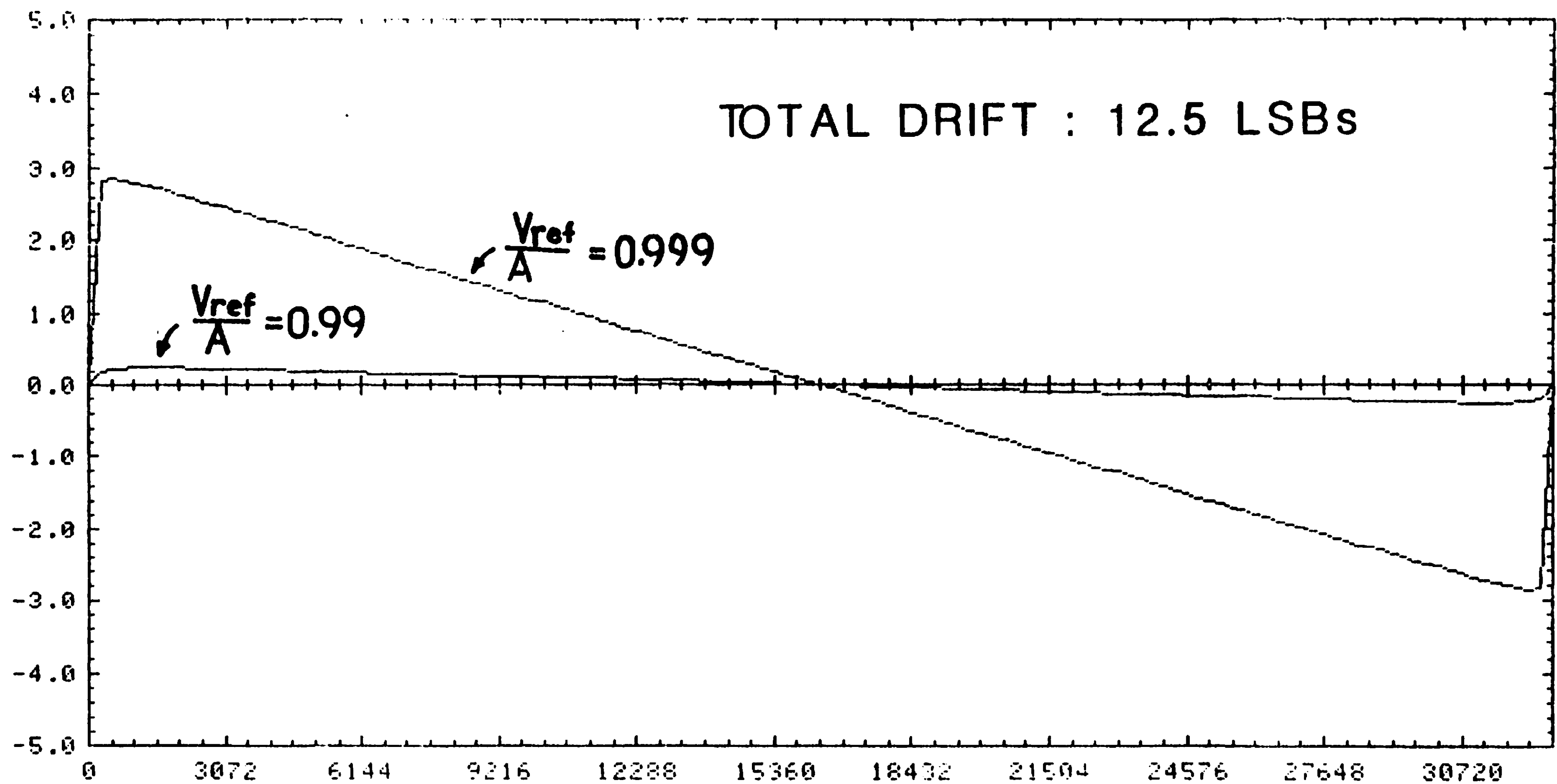


FIG. A4 EFFECT OF DRIFT IN AMPLITUDE OR REFERENCE VOLTAGES

LSB

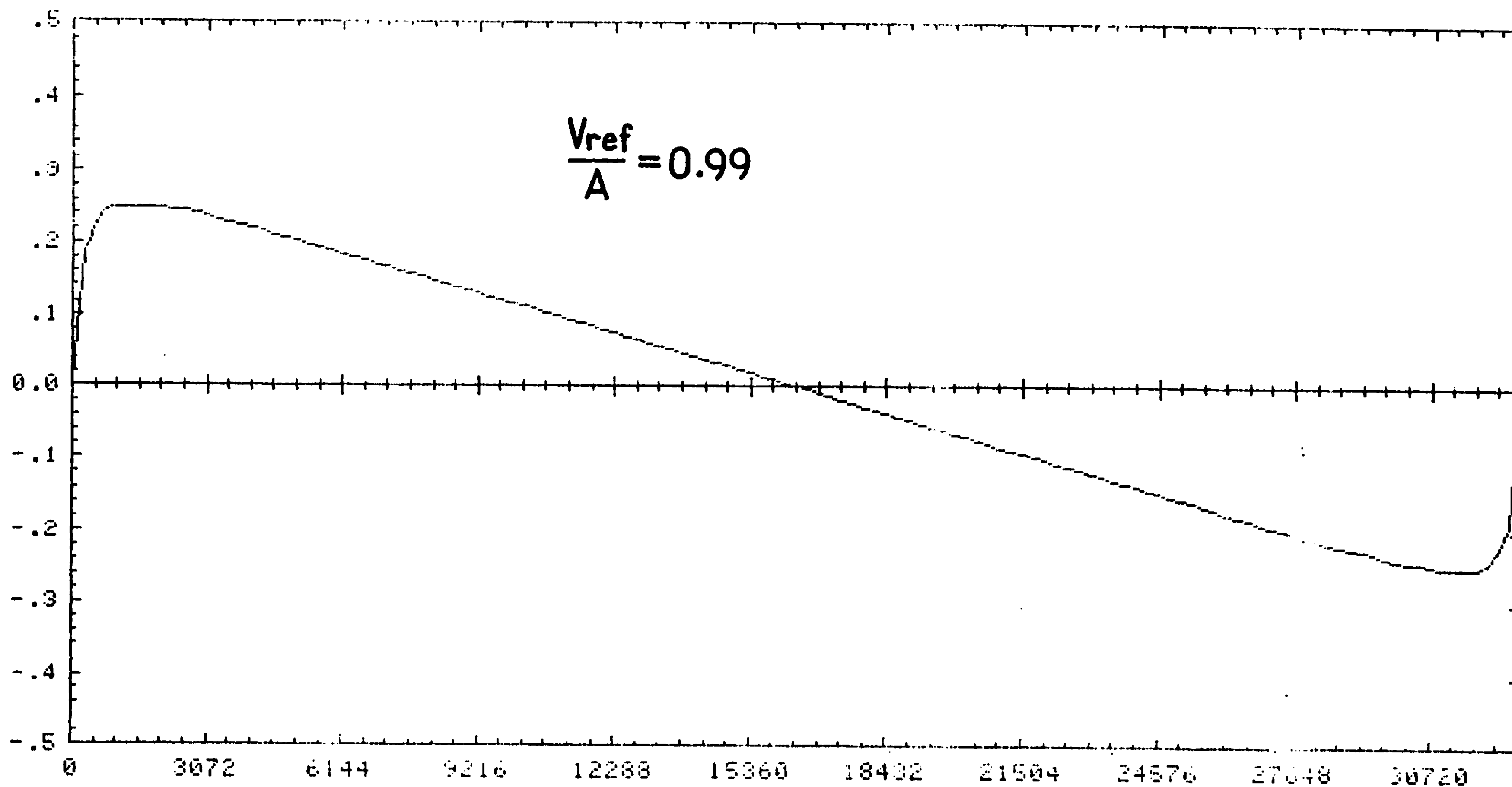


FIG. A5 EFFECT OF DRIFT (CONTINUED)

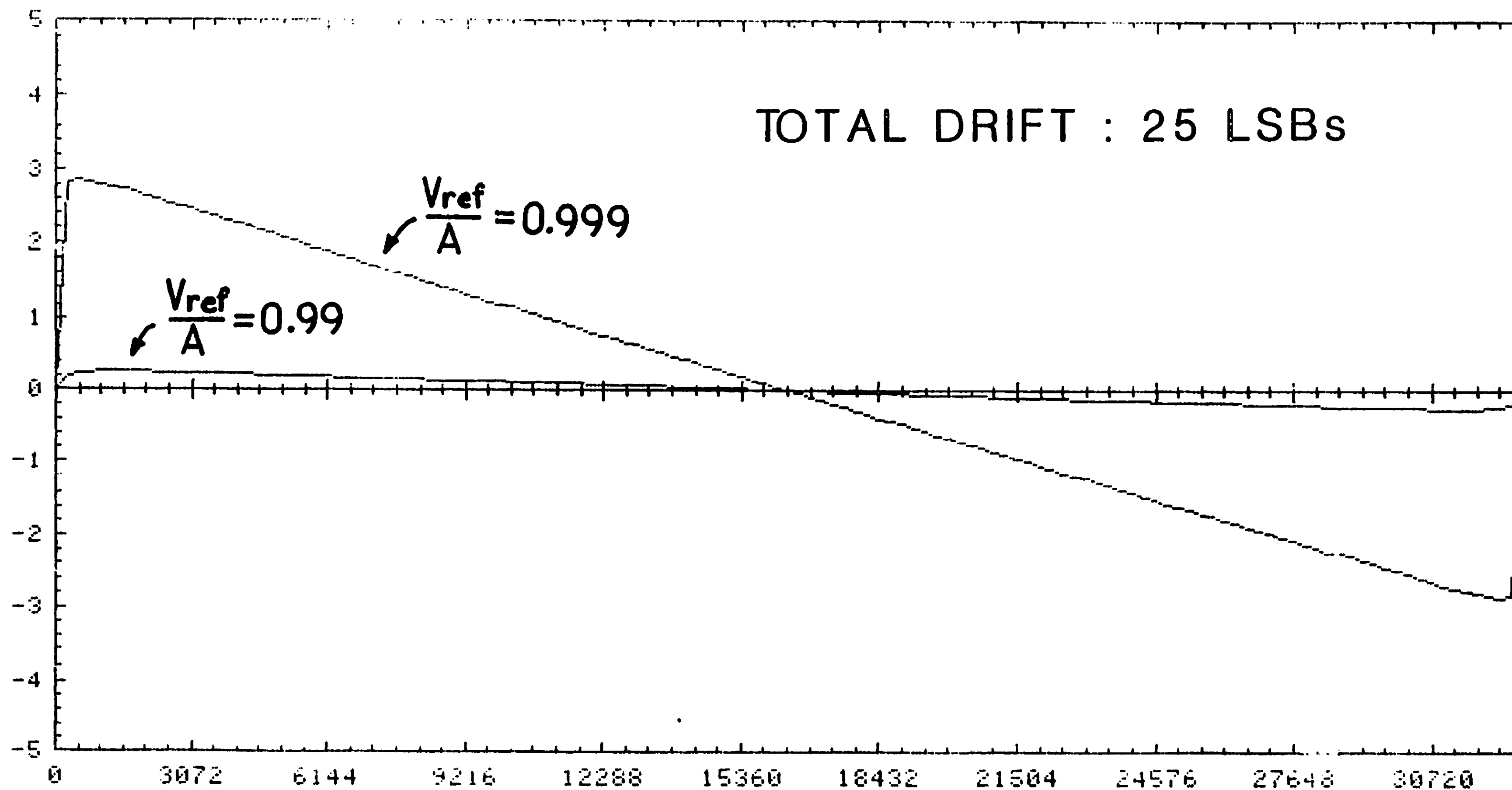
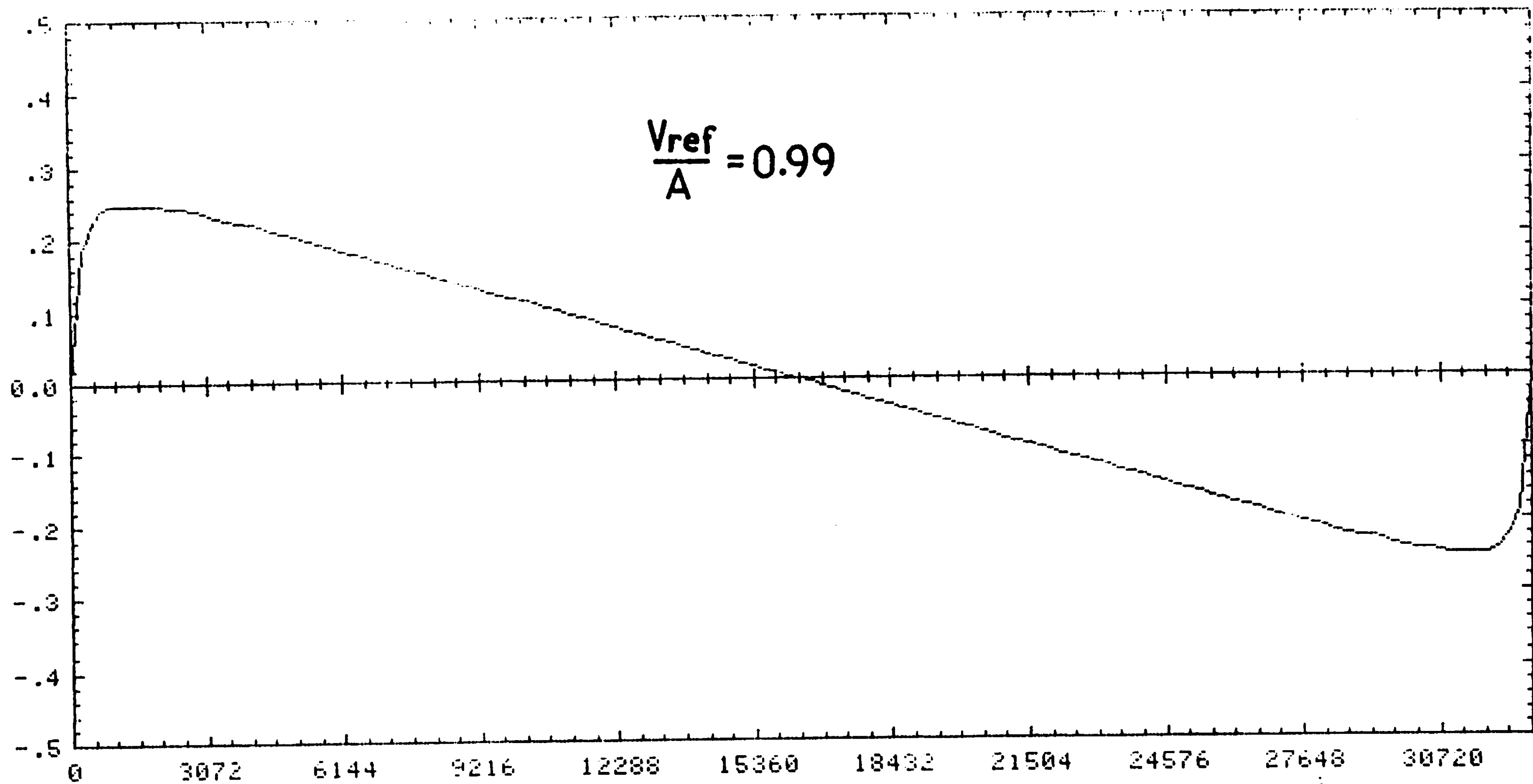


FIG. A6 EFFECT OF OFFSET DRIFT



RG. A7 EFFECT OF OFFSET DRIFT (CONTINUED)

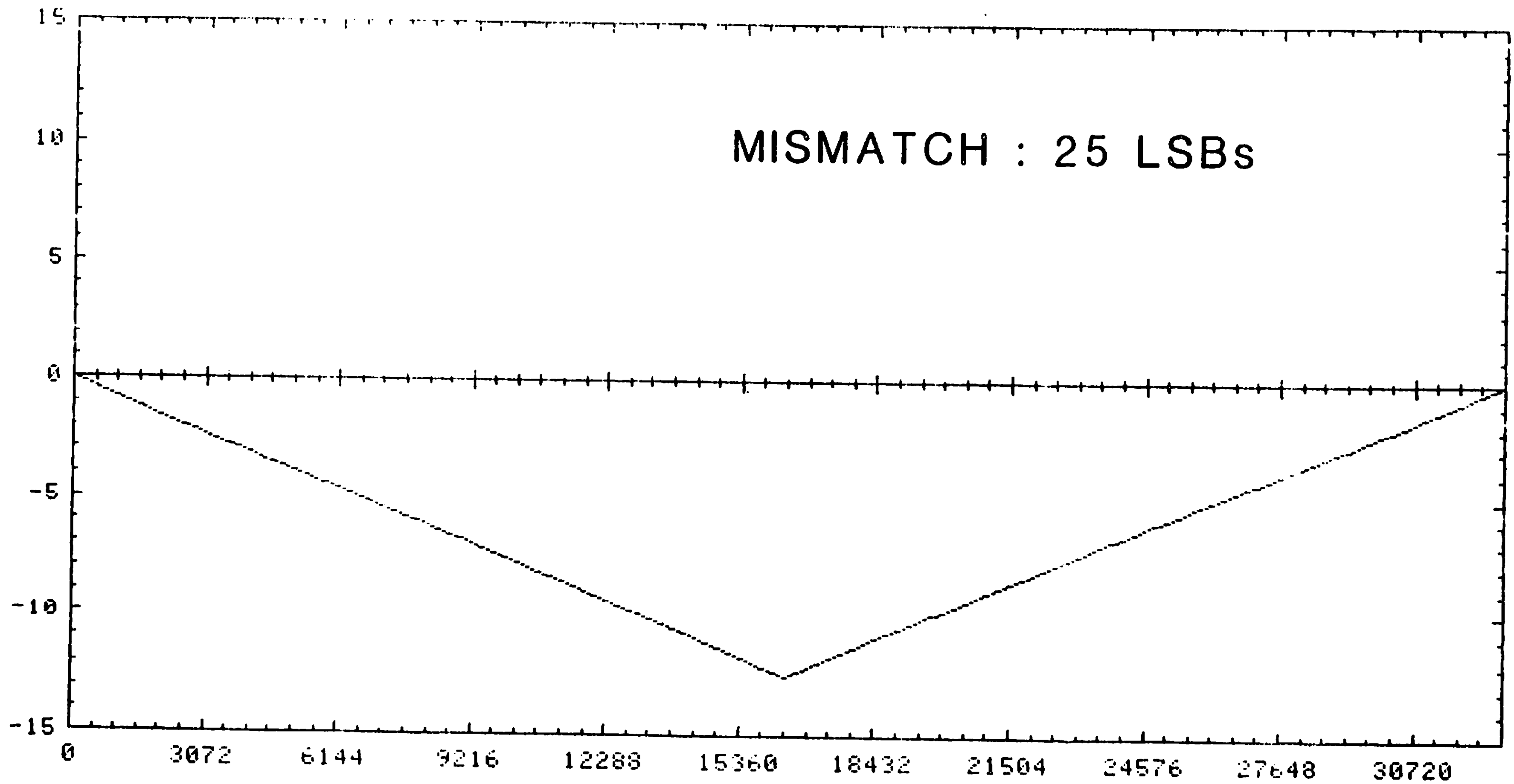


FIG. A8 EFFECT OF MISMATCHED REFERENCE VOLTAGES

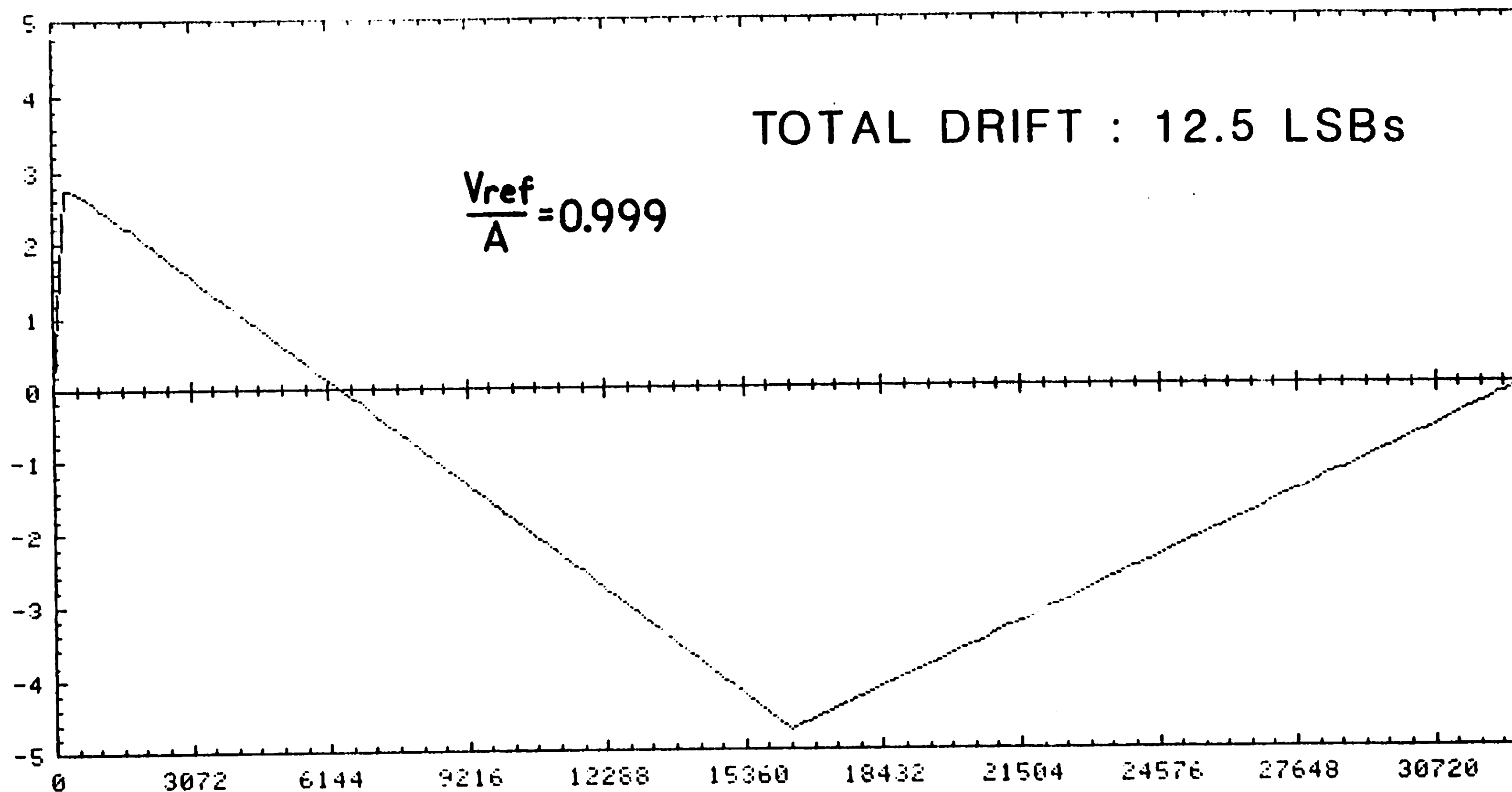


FIG. A9 EFFECT OF ASYMMETRICAL DRIFT

IN REFERENCE VOLTAGES

REFERENCES

(1) B Fotouhi and D.A. Hodges, "High-Resolution A/D Conversion in MOS/LSI," *IEEE J. Solid-State Circuits*, vol. SC-14, pp 920-926, Dec. 1979

(2) H-S Lee and D.A Hodges, "Self-Calibration Technique for A/D COnverters," *IEEE Trans. Circuits and Systems*, vol CAS-30, pp 188-190, Mar. 1983

(3) A.R. Hamade, "A Single Chip All-MOS 8-bit A/D Converter," *IEEE J. Solid-State Circuits* vol. SC-13, pp 785-791, Dec. 1978

(4) J.L. McCreary and P.R. Gray, "All-MOS Charge-Redistribution Analog-to-Digital Conversion Techniques," *IEEE J. Solid-State Circuits*, vol. SC-10, pp 371-379, Dec. 1975.

(5) J.L. McCreary and D.A. Sealer, "Precision Capacitor Ratio Measurement Technique for Integrated Circuit Capacitor Arrays," *IEEE Trans. Instrum. Meas.*, vol. IM-28, Mar. 1979.

(6) Z.G. Boyacigiller, B. Weir, and P.D. Bradshaw, "An Error-Correcting 14b/20μs CMOS A/D Converter," 1981 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers, vol. XXIV, pp 62-63

(7) K. Maio, M. Hotta, N. Yokozawa, M. Nagata, K. Kaneko, and T. Iwasaki, "An Untrimmed D/A Converter with 14-bit Resolution," *IEEE J. Solid-State Circuits*, vol. SC-16, Dec. 1981.

(8) T. Choi and R. Kaneshiro, "Berkeley CMOS Process," unpublished, Univ. of California, Berkeley, 1980.

(9) R.J. Van de Plassche and D. Goedhart, "A Monolithic 14-bit D/A Converter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp 552-556, June 1979.

(10) P.W. Li, M.Chin, P.R. Gray, and R. Castello, "A Ratio Independent Algorithmic A/D Conversion Technique," 1984 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers, vol. XXVII, pp 62-63.

(11) P.R. Gray, "Class Notes for EECS 249," University of Califronia, Berkeley, California, 1981.

(12) P.R. Gray, D.A. Hodges and R.W. Brodersen, Analog MOS Integrated Circuits, IEEE Press, pp 28-49, 1980.

(13) Ibid.

(14) T. Choi and R. Kaneshiro, "SPICE Parameters for Berkeley CMOS Process," unpublished, University of California, Berkeley, California 1980.

(15) B.Y. Kamath, R.G. Meyer and P.R. Gray, "Relationship between Frequency Response and Settling Time of Operational Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-9, pp 347-352, Dec. 1974.

(16) D.A. Hodges, University of California, Berekely, California, Private Communication.

(17) H-S Lee and D.A. Hodges, "Accuracy Considerations on Self-Calibrating A/D Converters," submitted to *Trans. Circuits and Systems*.

(18) J.L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitor," *IEEE J. Solid-State Circuits*, vol. SC-16, pp 608-616, Dec. 1981.

(19) Y.C. Lau, "Error Correction of Capacitor Voltage Non-linearity for a Charge-Redistribution Analog-to-Digital Converter," M.S. Thesis, University of California, Berkeley, California, 1983.

(20) R.S. Muller and T.I. Kamins, "Device Electronics for Integrated Circuits". New York: J. Wiley and Sons Inc.1977.

(21) J.L. McCreary, "Successive Approximation Analog-to-Digital Conversion Techniques in MOS Integrated Circuits," Ph. D. Dissertation, University of California, Berkeley, California, 1975.

(22) D.A. Hodges, op. cit., [16]

(23) C, Kittel, "Introduction to Solid State Physics," New York: J. Wiley and Sons Inc. 1956, pp 182-206

(24) A.S Grove, Physics and Technology of Semiconductor Devices. New York: J. Wiley and Sons Inc. 1967, pp 334-355.

(25) H-S Lee and D.A. Hodges, "A Precision Measurement Technique for Residual Polarization in Integrated Circuit Capacitors," submitted to the *IEEE Trans. Electron Devices*.

(26) J.L. McCreary, op. cit., [21]

(27) J. Doernberg, "Computer Aided Analog-to-Digital Converter Testing," M.S. Report, University of California, Berkeley, California, 1983.

(28) J. Doernberg, H-S Lee and D.A. Hodges, "Full-Speed Testing Technique of A/D Converters," submitted to the *IEEE J. Solid-State Circuits*.

(29) Bickel and Duksum, "Mathematical Statistics : Basic Ideas and Selected Topics," San Fransisco : Holden-Day Inc., 1977.

(30) Ibid.

(31) H-S Lee and P.W. Li, "Improved Berkeley CMOS Process," unpublished, University of California, Berkeley, California, 1983.

(32) R. Kaneshiro, University of California, Berkeley, California, Private Communication.

(33) "Semiconductor Technology Handbook," Technology Associates, 1978.

(34) H-S Lee, "CMOS Process Notes," unpublished, University of California, Berkeley, California, 1983.

(35) S. Tam, University of California, Berkeley, California, Private Communication.

(36) B.S. Song and P.R. Gray, "A Precision Curvature Compensated CMOS Bandgap Reference," 1983 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers, vol. XXVI, pp 240-241.

(37) J. Doernberg, University of California, Berkeley, California, Private Communication.

(38) H-S Lee, D.A. Hodges and P.R. Gray, "A Self-Calibrating 12 bit 12 Ms CMOS ADC," 1984 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers, vol. XXVII, pp 64-65.

(39) H-S Lee, D.A. Hodges and P.R. Gray, "Self-Calibrating 15 bit CMOS A/D Converter," submitted to the *IEEE J. Solid-State Circuits*.

(40) D.A. Hodges, op. cit., [16]

(41) R.J. Kansy, "Response of Correlated Double Sampling Circuit to 1/f Noise," *IEEE J. Solid-State Circuits*, vol. sc-15, pp 373-375, June, 1980.

(42) B.S. Song, "Precision Voltage Reference Techniques in MOS Technology," Ph. D. Dissertation, University of California, Berkeley, California, 1983.

(43) H-S Lee, "Feasibility Study on Self-Calibration Techniques for A/D Converters," unpublished, University of California, Berkeley, California, 1981.

(44) P.R. Gray, University of California, Berkeley, California, Private Communication.

(45) D.A. Hodges, op. cit., [16]

(46) S. Tam, op. cit., [19]

(47) W.J. Sitkewich, Semiconductor Production Division, Harris Corp. Melbourne, Florida, Private Communication.

(48) P.R. Gray, op. cit., [44]

(49) P.W. Li, University of California, Berkeley, California, Private Communication.

(50) R.T. Howe, University of California, Berkeley, California, Private Communication.

(51) P.W. Li, op. cit., [49]

(52) W.G. Oldham, University of California, Berkeley, California, Private Communication.

(53) D.A. Hodges, op. cit., [16]