# EXPLOITING THE OP AMP NONLINEARITY
# IN CIRCUIT DESIGN

by

L. O. Chua and F. Ayrom

Memorandum No. UCB/ERL M84/50

23 April 1984

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

# EXPLOITING THE OP AMP NONLINEARITY IN CIRCUIT DESIGN†

L. O. Chua and F. Ayrom

Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
University of California, Berkeley, CA 94720

## Abstract

The inherent saturation nonlinearity of the op amp is used to design circuits having a wide variety of useful nonlinear v-i characteristics. These circuits are made of one op amp and 3 or 4 linear resistors which are passive under a rather mild assumption derived from the 3-port paramouncy condition. Explicit design formulas are given for each prototype circuit and numerous examples are given and validated by actual measurements.

†Research supported by Semiconductor Research Corporation Grant SRC 82-11-008.

## 1. Introduction

Operational amplifiers (op amps) have been used almost exclusively as a linear element in circuit design [1-3]. Even in nonlinear circuit applications, such as synthesis of precision nonlinear driving-point characteristics [4] the op amp is operated only in the linear region, and the circuit's nonlinear behavior is provided by other nonlinear elements such as pn-junction diodes. Consequently, the dynamic range of the input signal in most op amp circuits must be restricted to avoid driving the op amp into saturation.

In this paper we will exploit, rather than avoid, the inherent nonlinearity of the op amp in designing practical circuits. In particular, we will show that any one-port made of one op amp and linear positive resistors (Fig. 1(a)) is characterized by one of the ten odd-symmetric driving-point characteristics shown in Fig. 1(b), assuming the op amp has a symmetric saturation characteristic. Moreover, we will show that under a rather mild inequality assumption, any of these v-i characteristics can be realized by the canonical circuit shown in Fig. 2.

Each v-i characteristic in Fig. 1(b) has numerous applications [5-7]: characteristic (i)-(iv) in Fig. 1(b) can be used for wave shaping applications; characteristic (v)-(vi) can be used for designing oscillators and multivibrators, whereas characteristics (vii)-(x) can be used for designing flip-flops. Moreover, since these characteristics can be realized with high precision, they can be used as building blocks for synthesizing more complicated v-i characteristics. Since the origin in each v-i characteristic in Fig. 1(b) can be translated to any other point in the v-i plane by adding one or two batteries, we have an unusually large repertoire of accurate v-i characteristic building blocks made of only op amps, linear positive resistors, and batteries.

Because of its widespread applications, Section 2 is written in a "cookbook" style for users interested only in building the canonical op amp circuits to have any one the v-i characteristics in Fig. 1(b) with prescribed breakpoints and slopes. Although the canonical circuit in Fig. 2 contains 7 resistors, no more than 4 are needed in each case. Consequently, the simplified circuits in Section 2 are all special cases of the canonical circuit. Explicit formulas for calculating the resistances and battery voltages are given for each simplified canonical circuit. To demonstrate the accuracy of these circuits in realizing a prescribed v-i characteristic, examples with experimentally measured v-i characteristics are given for comparison purposes.

Some practical aspects of the circuits presented in Section 2 are discussed in Section 3.

Section 4 is devoted to the design of several practical circuits using the simplified canonical circuits from Section 2 as building blocks.

The canonical circuit in Fig. 2 is derived via a circuit - theoretic approach in Section 5. The concept of a paramount matrix [8] plays a crucial role in the conception of this circuit. Indeed, our approach represents one of the very few instances in electronic circuit design where a circuit configuration is derived systematically rather than through an *ad hoc* or intuitive approach.

## 2. Design Formulas and Examples

Each v-i characteristic in Fig. 1 can be synthesized by a simplified version of the canonical circuit in Fig. 2. In the following we consider one v-i characteristic at a time (in the order listed) and give the corresponding circuit along with the formulas for calculating the element values. Note that since we retain the resistor label in the canonical circuit, the resistors in the following circuits are not numbered consecutively since only 3 or 4 (out of 7) resistors are needed in each case. Except for $E_{s+}$ and $E_{s-}$ which denote the positive and negative saturation voltages of the op amp being used,[†] all other parameters are labelled in the associated v-i characteristics. In order to guarantee that all resistors are positive, it is both necessary and sufficient that these parameters must satisfy the following standing assumptions:

Slope-breakpoint inequality

$$\left|\frac{m_0-m_1}{m_0}\right| < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} \qquad (1a)$$

$$\frac{E_{B2}-E_{B1}}{E_{s+}+|E_{s-}|} < 1 \qquad (1b)$$

for all cases except (iv) and (viii) where (1a) and (1b) are replaced by

$$m_0 > \frac{I_{B2}-I_{B1}}{E_{s+}+|E_{s-}|} \qquad (2)$$

[†] For improved accuracy in our design we do not assume the op amp saturation voltages to be equal in magnitude. Of course, if an odd-symmetric v-i characteristic is required, then an op amp with $|E_{s+}| = |E_{s-}|$ must be chosen.

The standing assumption will be derived in Section 4. It is a weak assumption that is satisfied by most v-i characteristics of practical interest.

Two design examples will be given for each simplified canonical circuit. The first example is an odd-symmetric characteristic taken directly from Fig. 1. The second example is a translated version of the corresponding characteristic from Fig. 1. For comparison purposes we have used the same op amp (national/ 8035 741 CN) in all these examples. This op amp was measured to have a positive saturation voltage $E_{s+} = 15$ V and a negative saturation voltage $E_{s-} = -13$ V. Had another op amp with an identical saturation voltages been chosen, then no batteries will be needed in realizing each odd-symmetric characteristic in the following examples: 1.1, 2.1, 3.1, 4.1, 5.1, 6.1, 7.1, 8.1, 9.1 and 10.1.

$\boxed{\text{v-i characteristic (i)}}$

Consider the v-i characteristic in Fig. 3(a). This is identical to the v-i characteristic (i) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 3(b).

Example 1.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 4(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -1$ V, $E_{B2} = 1$ V and $I_{B1} = -1$ mA. Substituting these parameters into (1), we found

$$\left|\frac{2-1}{1}\right| < \frac{15+13}{1+1}$$

$$\left|\frac{1+1}{15+13}\right| < 1$$

Hence, the slope-breakpoint condition is satisfied and we know only positive resistors are needed. The element values calculated from the design algorithm in Fig. 3(b) are:

$$R_3 = 1\ \text{K}\Omega,\ R_4 = 13\ \text{K}\Omega,\ R_6 = 518.5\ \Omega$$

$$R_7 = 14\ \text{K}\Omega,\ E_1 = -.77\ \text{V},\ E_2 = -.37\ \text{V}$$

The v-i characteristic measured from the resulting circuit is shown in Fig. 4(b).†

†All v-i curves in this paper are traced with a specially designed negative-resistance curve tracer [9].

Example 1.2

Synthesize the v-i characteristic shown in Fig. 5(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 3$, $m_1 = 1$, $E_{B1} = -3$ V, $E_{B2} = 1$ V and $I_{B1} = -2$ mA. The slope-breakpoint condition is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 3(b) are:

$R_3 = 1\ K\Omega$, $R_4 = 6\ K\Omega$, $R_6 = 368\ \Omega$

$R_7 = 3.5\ K\Omega$, $E_1 = -1.33$ V, $E_2 = -1.21$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 5(b).

v-i characteristic (ii)

Consider the v-i characteristic in Fig. 6(a). This is identical to the v-i characteristic (ii) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 6(b).

Example 2.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 7(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = -4$ mA. It is easily verified that condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 6(b) are:

$R_1 = 500\ \Omega$, $R_3 = 583\ \Omega$, $R_4 = 3.5\ K\ \Omega$

$E_1 = -.17$ V, $E_2 = 0$

The v-i characteristic measured from the resulting circuit is shown in Fig. 7(b).

Example 2.2

Synthesize the v-i characteristic shown in Fig. 8(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = -2$ V, $E_{B2} = 4$ V and $I_{B1} = 1$ mA. Since condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Fig. 6(b) are:

$R_1 = 500\ \Omega$, $R_3 = 633\ \Omega$, $R_4 = 2.33\ K\Omega$

$E_1 = -7.91$ V, $E_2 = -2.5$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 8(b).

v-i characteristic (iii)

Consider the v-i characteristic in Fig. 9(a). This is identical to the v-i characteristic (iii) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 9(b).

Example 3.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 10(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = 0$. Condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 9(b) are:

$R_3 = 1\ \mathrm{K\Omega}$, $R_4 = 6\ \mathrm{K\Omega}$, $R_6 = 583\ \Omega$

$R_7 = 3.5\ \mathrm{K\Omega}$, $E_1 = -.17$ mV, $E_2 = -.17$ mV

The v-i characteristic measured from the resulting circuit is shown in Fig. 10(b).

Example 3.2

Synthesize the v-i characteristic shown in Fig. 11(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 0$, $E_{B1} = -1$ V, $E_{B2} = 3$ V and $I_{B1} = 4$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 9(b) are:

$R_3 = 1\ \mathrm{K\Omega}$, $R_4 = 6\ \mathrm{K\Omega}$, $R_6 = 583\ \Omega$

$R_7 = 3.5\ \mathrm{K\Omega}$, $E_1 = 1$V, $E_2 = -1.33$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 11(b).

v-i characteristic (iv)

Consider the v-i characteristic in Fig. 12(a). This is identical to the v-i characteristic (iv) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 12(b).

Example 4.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 13(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = \frac{1}{4}$, $m_1 = \infty$, $I_{B1} = -3$ mA, $I_{B2} = 3$ mA and

$E_{B1} = 0$. Substituting these parameters into (2), we found:

$$\frac{1}{4} > \frac{3+3}{15+13}$$

Hence, the slope-breakpoint inequality is satisfied and we know only positive resistors are needed. The element values calculated from the design algorithm in Fig. 12(b) are:

$R_4 = 4.7\ K\Omega$, $R_5 = 18\ K\Omega$, $R_6 = 10\ K\Omega$

$E_2 = 0$, $E_3 = -1$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 13(b).

Example 4.2

Synthesize the v-i characteristic shown in Fig. 14(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = \frac{1}{4}$, $m_1 = \infty$, $I_{B1} = -1$ mA, $I_{B2} = 3$ mA and $E_{B1} = 4$ V. The slope-breakpoint condition (2) is satisfied. The element values calculated from the design algorithm in Fig. 12(b) are:

$R_4 = 7\ K\Omega$, $R_5 = 1\ K\Omega$, $R_6 = 8.33\ k\Omega$

$E_2 = 4$ V, $E_3 = -2$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 14(b).

## v-i characteristic (v)

Consider the v-i characteristic in Fig. 15(a). This is identical to the v-i characteristic (v) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 15(b).

Example 5.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 16(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = -\frac{1}{2}$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = 1$ mA. Since the slope-breakpoint condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Fig. 15(b) are:

$R_3 = 1\ K\Omega$, $R_4 = 6\ K\Omega$, $R_6 = 608.7\ \Omega$

$R_7 = 2.8\ K\Omega$, $E_1 = -.167$ V, $E_2 = -.217$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 16(b).

Example 5.2

Synthesize the v-i characteristic shown in Fig. 17(a) using an op amp with $E_{S+} = 15$ V and $E_{S-} = -13$ V. Here $m_0 = 1$, $m_1 = -\frac{1}{2}$, $E_{B1} = 1$ V, $E_{B2} = 2$ V and $I_{B1} = 1$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 15(b) are:

$R_3 = 1$ K , $R_4 = 26$ K , $R_6 = 1.06$ K

$R_7 = 18$ K , $E_1 = 1.54$ V, $E_2 = .765$ V

The v-i characteristic measured from the resulting circuitis shown in Fig. 17(b).

v-i characteristic (vi)

Consider the v-i characteristic in Fig. 18(a). This is identical to the v-i characteristic (vi) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 18(b).

Example 6.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 19(a) using an op amp with $E_{S+} = 15$ V and $E_{S-} = -13$ V. Here $m_0 = 1$, $m_1 = -2$, $E_{B1} = -3$V, $E_{B2} = 3$ V and $I_{B1} = 6$ mA. Since the slope-breakpoint condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Fig. 18(b) are:

$R_3 = 2.8$ KΩ, $R_4 = 1.56$ KΩ, $R_6 = 3$ KΩ

$R_7 = 11$ KΩ, $E_1 = -1.8$ V, $E_2 = -.273$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 19(b).

Example 6.2

Synthesize the v-i characteristic shown in Fig. 20(a) using an op amp with $E_{S+} = 15$ V and $E_{S-} = -13$ V. Here $m_0 = 1$, $m_1 = -\frac{1}{2}$, $E_{B1} = 1$ V, $E_{B2} = 3$ V and $I_{B1} = 4$ mA. Condition (1) is satisfied and we know only positive resistors are needed. The element values calculated from the design algorithm, in Fig. 18(b) are:

$R_3 = 1.12\ K\Omega,\ R_4 = 9\ K\Omega,\ R_6 = 2\ K\Omega$

$R_7 = 25\ K\Omega,\ E_1 = -1.75\ V,\ E_2 = 2.12\ V$

The v-i characteristic measurement from the resulting circuit is shown in Fig. 20(b).

v-i characteristic (vii)

Consider the v-i characteristic in Fig. 21(a). This is identical to the v-i characteristic (vii) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 21(b).

Example 7.1 (Odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 22(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = 0$. The slope-breakpoint condition (1) is satisfied and only posiqive resistors are needed. The element values calculated from the design algorithm in Fig. 21(b) are:

$R_3 = 1.17\ K\Omega,\ R_4 = 7\ K\Omega,\ R_6 = 1\ K\Omega$

$R_7 = 6\ K\Omega,\ E_1 = -.17\ V,\ E_2 = -.17\ V$

The v-i characteristic measured from the resulting circuit is shown in Fig. 22(b). Note that since this characteristic is multivalued (i.e. neither voltage-controlled nor current-controlled), we were able to trace only two segments of the v-i characteristic.

Example 7.2

Synthesize the v-i characteristic shown in Fig. 23(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 4$ V and $I_{B1} = 4$ mA. The slope-breakpoint condition is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 21(b) are:

$R_3 = 1.27\ K\Omega,\ R_4 = 4.67\ K\Omega,\ R_6 = 3\ K\Omega$

$R_7 = 11\ K\Omega,\ E_1 = -4.09\ V,\ E_2 = 1\ V$

The v-i characteristic measured from the resulting circuit is shown in Fig. 23(b). Again only two segments are shown because the characteristic is multi-valued.

v-i characteristic (viii)

Consider the v-i characteristic in Fig. 24(a). This is identical to the v-i characteristic (viii) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 24(b).

Example 8.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 25(a) using an op amp with $E_{s+} = +15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = \infty$, $I_{B1} = -2$ mA, $I_{B2} = 2$ mA and $E_{B1} = 0$. The slope-breakpoint inequality (2) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 24(b) are:

$R_3 = 167\ \Omega$, $R_5 = 1\ \mathrm{K}\Omega$, $R_7 = 7\ \mathrm{K}\Omega$

$E_2 = 0$, $E_3 = -1$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 25(b). Note that since this characteristic is multivalued only two segments of the v-i characteristic are shown.

Example 8.2

Synthesize the v-i characteristic shown in Fig. 26(a) using an op amp with $E_{s+} = 15$ V, $E_{s-} = -13$ V. Here $m_0 = 1$, $I_{B1} = -1$ mA, $I_{B2} = 3$ mA and $E_{B1} = 6$ V. Since condition (2) is satisfied only positive resistors are needed. The element values calculated from the design algorithm in Fig. 24(b) are:

$R_3 = 167\ \Omega$, $R_5 = 1\ \mathrm{K}\Omega$, $R_7 = 7\ \mathrm{K}\Omega$

$E_2 = 6$ V, $E_3 = -2$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 26(b). Again only two segments are shown because the characteristic is multi-valued.

v-i characteristic (ix)

Consider the v-i characteristic in Fig. 27(a). This is identical to the v-i characteristic (ix) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 27(b).

Example 9.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 28(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = -3$ V, $E_{B2} = 3$ V and $I_{B1} = -6$ mA. Condition (1) is therefore satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 27(b) are:

$R_2 = 500\ \Omega$, $R_4 = 2.33\ \text{K}\Omega$, $R_6 = 636.4\ \Omega$

$E_1 = -.273$ V, $E_2 = 0$

The v-i characteristic measured from the resulting circuit is shown in Fig. 28(b). Note that since this characteristic is multivalued only two segments are shown.

Example 9.2

Synthesize the v-i characteristic shown in Fig. 29(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = 2$ V, $E_{B2} = 4$ V and $I_{B1} = -3$ mA. Since condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Fig. 27(b) are:

$R_2 = 500\ \Omega$, $R_4 = 7\ \text{K}\Omega$, $R_6 = 588.5\ \Omega$

$E_2 = 4.23$ V, $E_3 = 3.5$ V

The v-i characteristic measured from the resulting circuit is shown in Fig. 29(b). Again only two segments are shown because the characteristic is multi-valued.

v-i characteristic (x)

Consider the v-i characteristic in Fig. 30(a). This is identical to the v-i characteristic (x) in Fig. 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Fig. 30(b).

Example 10.1 (odd-symmetric characteristic)

Synthesize the v-i characteristic shown in Fig. 31(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -4$ V, $E_{B2} = 4$ V and $I_{B1} = -4$ mA. Condition (1) is therefore satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 30(b) are:

$R_3 = 583\ \Omega$, $R_4 = 3.5\ K\Omega$, $R_6 = 2\ K\Omega$

$R_7 = 5\ K$ , $E_1 = -\ .17\ V$, $E_2 = -\ .4\ V$

The v-i characteristic measured fromthe resulting circuit is shown in Fig. 31(b). Since this characteristic is multivalued, only two segments are shown.

Example 10.2

Synthesize the v-i characteristic shown in Fig. 32(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -\ 13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -\ 4$ V, $E_{B2} = -\ 2$ V and $I_{B1} = -\ 4$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Fig. 3(b) are:

$R_3 = 518.5\ \Omega$, $R_4 = 14\ K\Omega$, $R_6 = 1\ K\Omega$

$R_7 = 13\ K\Omega$, $E_1 = -\ 1.59\ V$, $E_2 = -\ 3.31\ V$

The v-i characteristic measured from the resulting circuit is shown in Fig. 32(b). Since this characteristic is multivalued, only two segments are shown.

## 3. Practical Considerations

In this section we discuss two practical aspects of the circuits presented in Section 2. First, we show that by using an op amp with identical saturation voltages no batteries will be needed in realizing any odd-symmetric characteristic in Fig. 1(b). Next, we present alternative circuits, for cases where batteries are needed, in which the needed batteries are realized using the power supply voltage.

### A. Realization of odd-symmetric characteristic with circuits containing no batteries

Using an op amp with identical saturation voltages any odd-symmetric characteristic in Fig. 1(b) can be realized with circuits containing no batteries. This is easily verified by substituting $E_{s+} = |E_{s-}|$ and $E_{B2} = -\ E_{B1}$ in design formulas of Section 2.

In general the saturation voltages of any op amp depend on the power supply voltages $v_{cc+}$ and $v_{cc-}$ required for the op amp operation. In the case of the 741 op amp the positive saturation voltage $E_{s+} = v_{cc+}$ but the negative saturation voltage is considerably lower (up to 2 volts) than $v_{cc-}$ [10]. However, by adjusting $v_{cc+}$ the two saturation voltages can be made identical. Recall all the examples in Section 2 were obtained by using $v_{cc+} = 15$ V, $v_{cc-} = -15$ V which correspond to $E_{s+} = 15$ V and $E_{s-} = -13$ V. However, using $v_{cc+} = 13$ V and $v_{cc-} = -15$ V we were able to obtain $E_{s+} = |E_{s-}| = 13$ V. This op amp was then used to realize the same odd-symmetric characteristics presented as examples in Section 2. These measured characteristics along with the resistor values are exhibited in Fig. 33 through Fig. 42.

B. Alternative circuits

In order to measure the v-i characteristic of any circuit shown in Section 2, four power supplies are needed. Two power supplies $v_{cc+}$, $v_{cc-}$ for op amp operation and the other two as batteries. From a practical point of view this is sometimes undesirable. Hence, in what follows alternative circuits are presented in which the two batteries are realized by direct use of the op amp power supplies. The only restriction is that the battery voltages $|E_1|$ and $|E_2|$ must be less than the power supply voltages.

First, consider the circuit in Fig. 43. This circuit can be used to realize any battery $E_1$ less than the supply voltage $E_s$ by choosing appropriate values for $R_A$ and $R_B$.

Figure 44 shows the circuit modification needed to realize a series combination of a resistor and a battery, as in the circuits from Section 2, using the power supply.

The circuit modification needed to realize a battery which is directly connected to input terminals of an op amp using the power supply is shown in Fig. 45.

## 4. Applications

This section is devoted to the design of several practical circuits using the simplified canonical circuits from Section 2 as building blocks.

(a) A soft oscillator

Consider the circuit in Fig. 46(a) where the non-linear resistor has a voltage controlled v-i characteristic as in Fig. 46(b). The dynamic route in Fig. 46(b) shows that regardless of the initial flux on the inductor the circuit exhibits oscillations. The measured v-i characteristic and the measured oscillations are shown in Fig. 47.

(b) A hard oscillator

Consider the circuit in Fig. 48(a) where the parallel combination of $R_1$ and $R_2$ has a v-i characteristic as shown in Fig. 48(b). The dynamic route in Fig. 48(b) reveals that the origin is a stable equilibrium point. Therefore, in order to obtain oscillations an initial current of $i_L(0) > \frac{1}{2}$ mA must be imposed on the inductor. The measured characteristic for $R_1$ and $R_2$ are shown in Fig. 49(a)-(b), the parallel combination of these two is shown in Fig. 49(c) and the measured oscillation is exhibited in Fig. 49(d).

(c) A 3-state circuit

Consider the circuit in Fig. 50(a) where the parallel combination of the two non-linear resistors results in a v-i characteristic as shown in Fig. 50(b). From the associated dynamic route we see that $Q_1$, $Q_2$ and $Q_3$ are all stable equilibrium points. Therefore, depending on the initial charge on the capacitor one of three states will be reached. The measured v-i characteristic along with the circuit used in the realization is shown in Fig. 51.

(d) A chaotic circuit

Roughly speaking, a circuit is chaotic iff its solution is neither a periodic (possibly constant) nor an almost periodic function. It is now widely believed that a large class of practical nonlinear circuits can become chaotic if the circuit parameters are appropriately chosen.

The circuit in Fig. 52(a) has recently been shown to exhibit chaotic behavior [11]. The non-linear resistor in this circuit must have a v-i characteristic as in Fig. 52(b). In the following we present the design procedure for obtaining such a characteristic. A parallel combination of two odd-symmetric voltage-controlled characteristics is needed in the synthesis. Consider the characteristics in Fig. 53; in order for the parallel combination of these two characteristics to result in a characteristic as in Fig. 52(b) we need:

$$m_{01} + m_{02} = m_0 \tag{3}$$

$$m_{02} + m_{11} = m_1 \tag{4}$$

$$m_{11} + m_{12} = m_2 \tag{5}$$

To solve these equations choose $m_{12} > m_{11}$ such that (5) is satisfied. Then,

$$m_{02} = m_1 - m_{11}$$

$$m_{01} = m_0 - m_1 + m_{11}$$

Hence, to realize the characteristic in Fig. 52(b) we have to realize $R_1$ with parameters $(m_{01}, m_{11}, E_{B1})$ and $R_2$ with parameters $(m_{02}, m_{12}, E_{B2})$ using the design algorithms from Section 2.

Remark

We choose $m_{12} > m_{11}$ in order to satisfy condition (1) of Section 2. This is due to the fact that $E_{B1}$ is quite large and we need a small $m_{11}$ in order to satisfy the slope-breakpoint inequality.

Example

Realize the characteristic shown in Fig. 52(b) with $m_0 = 5$, $m_1 = -.1$, $m_2 = -4$, $E_{B1} = 11$ and $E_{B2} = +1$. Substituting these parameters into equations (3)-(5) we get

$$m_{01} + m_{02} = 5$$

$$m_{01} + m_{12} = -.1$$

$$m_{11} + m_{12} = -4$$

Choose $m_{11} = -.5$, $m_{12} = -3.5$. Then,

$$m_{01} = 3.4,\ m_{02} = 1.6$$

Therefore, we have to realize $R_1$ with $(m_{01} = 3.4,\ m_{11} = -.5,\ E_{B1} = 11)$ and $R_2$ with $(m_{02} = 1.6,\ m_{11} = -3.5,\ E_{B2} = 1)$. This was done using op amps with identical saturation voltages $E_{s+} = |E_{s-}| = 13$. The measured characteristic for $R_1$ and $R_2$ is shown in Fig. 54(a)-(b). The measured characteristic resulting from the parallel combination of these two is shown in Fig. 54(c). Fig. 54(d) is the circuit used in these realizations.

Connecting the one-port in Fig. 54(d) in place of R in Fig. 52(a), and using appropriate values of R, L, $C_1$, and $C_2$, an interesting chaotic attractor is observed and will be reported in detail in a future paper. This is one example where a prescribed piecewise-linear negative differential resistance characteristic must be precisely synthesized. The methods developed in this paper could not have been more timely.

## 5. Theory

In this section we present the circuit-theoretic approach from which the canonocal circuit in Fig. 2 is derived. First, the problem of synthesizing op amp circuits is reduced to that of synthesizing a 3 x 3 conductance matrix. Next, the concept of a paramount matrix is introduced. Finally, the fact that a 3 x 3 conductance matrix is realizable using linear positive resistors iff it is paramount, is used to derive the canonical circuit.

### A. Circuit Formulation

Consider a general circuit containing one op amp, linear positive resistors and independent voltage sources as shown in Fig. 55. Next, replace the op amp by its piecewise-linear model as in Fig. 56(a), where the 2-terminal nonlinear resistor is characterized by Fig. 56(b). The resulting circuit is shown in Fig. 57. Note that for simplicity we use an op amp model with saturation voltages $E_{s+}$ and $E_{s-}$ of equal magnitude. The following results apply equally well, mutatis mutandis, when $E_{s+} \neq |E_{s-}|$. Since the 3-port N in Fig. 57 contains only 2-terminal resistors and independent sources, it is reciprocal. Let N be described by the following voltage-controlled representation.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{12} & g_{22} & g_{23} \\ g_{13} & g_{23} & g_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{6}$$

where $g_{ij} = g_{ji}$ because N is reciprocal. Next, consider the circuit in Fig. 58 which is obtained from Fig. 57 by pulling out the only nonlinear element. Comparing the circuits in Fig. 57 and Fig. 58 and using (6) we obtain the following transmission (chain) representation for the 2-port N' (assuming $g_{12} \neq 0$).

$$\left.\begin{aligned} i &= (g_{13} - \frac{g_{11}g_{23}}{g_{12}}) i_d + (\frac{g_{11}g_{22}}{g_{12}} - g_{12}) v_d + (I_1 - \frac{g_{11}}{g_{12}} I_2) \\ V &= - \frac{g_{23}}{g_{12}} i_d + \frac{g_{22}}{g_{12}} v_d - \frac{1}{g_{12}} I_2 \end{aligned}\right\} \tag{7}$$

We are now ready to present explicit equations describing the driving point characteristic of any circuit containing one op amp, linear positive resistors and independent voltage sources.

Theorem 1

Hypotheses:

1. $A \to \infty$ in Fig. 56(b), i.e., assume an ideal op amp model.
2. The 3-port N in Fig. 55 has a short-circuit conductance matrix $\underset{\sim}{G}$.

Conclusion:

The driving-point characteristic of the one op amp circuit in Fig. 55 consists of 3 connected piecewise-linear segments. If we label these segments consecutively by 1, 2, and 3, then segments 1 and 3 are parallel to each other. Each segment is described by the following linear equation and interval of validity:

Segment 1

$$\boxed{i = \left(\frac{g_{11}g_{22} - g_{12}^2}{g_{22}}\right) v + E_s \left(\frac{g_{12}g_{23} - g_{13}g_{22}}{g_{22}}\right) + I_1 - \frac{g_{12}}{g_{22}} I_2} \tag{8a}$$

where,

$$\left.\begin{array}{ll} -\infty < i < E_s\left(\frac{g_{11}g_{23} - g_{12}g_{13}}{g_{12}}\right) & , \text{ if } \frac{g_{11}g_{22} - g_{12}^2}{g_{12}} > 0 \\ E_s\left(\frac{g_{11}g_{23} - g_{12}g_{13}}{g_{12}}\right) \leq i < \infty & , \text{ if } \frac{g_{11}g_{22} - g_{12}^2}{g_{12}} < 0 \\ -\infty < v < E_s \frac{g_{23}}{g_{12}} & , \text{ if } g_{12} > 0 \\ E_s \frac{g_{23}}{g_{12}} < v < \infty & , \text{ if } g_{12} < 0 \end{array}\right\} \tag{8b}$$

Segment 2

$$\boxed{i = \left(\frac{g_{11}g_{23} - g_{12}g_{13}}{g_{23}}\right) v + I_1 - \frac{g_{13}}{g_{23}} I_2} \tag{9a}$$

where,

$$
\left.
\begin{array}{ll}
-E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) \le i \le E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) & , \text{ if } \dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}} > 0 \\
E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) \le i \le -E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) & , \text{ if } \dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}} < 0 \\
-E_s\dfrac{g_{23}}{g_{12}} \le v \le E_s\dfrac{g_{23}}{g_{12}} & , \text{ if } \dfrac{g_{23}}{g_{12}} > 0 \\
E_s\dfrac{g_{23}}{g_{12}} \le v \le -E_s\dfrac{g_{23}}{g_{12}} & , \text{ if } \dfrac{g_{23}}{g_{12}} < 0
\end{array}
\right\} \tag{9b}
$$

Segment 3

$$
\boxed{i = \left(\frac{g_{11}g_{22}-g_{12}^2}{g_{22}}\right)v - E_s\left(\frac{g_{12}g_{23}-g_{13}g_{22}}{g_{22}}\right) + I_1 - \frac{g_{12}}{g_{22}} I_2} \tag{10a}
$$

where,

$$
\left.
\begin{array}{ll}
E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) \le i < \infty & , \text{ if } \dfrac{g_{11}g_{22}-g_{12}^2}{g_{12}} > 0 \\
-\infty < i \le E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right) & , \text{ if } \dfrac{g_{11}g_{22}-g_{12}}{g_{12}} < 0 \\
-E_s\dfrac{g_{23}}{g_{12}} \le v < \infty & , \text{ if } g_{12} > 0 \\
-\infty < v \le -E_s\dfrac{g_{23}}{g_{12}} & , \text{ if } g_{12} < 0
\end{array}
\right\} \tag{10b}
$$

Proof

For $-\infty < v_d \le -\frac{E_s}{A}$ we have $i_d = -E_s$. Substituting for $i_d$ in (7) and solving for $v_d$ we get

$$
\left.
\begin{array}{l}
V_d = \dfrac{i - I + E_s k_{11}}{k_{12}} \\
\qquad\qquad\qquad , \quad -\infty < v_d \le -\dfrac{E_s}{A} \\
V_d = \dfrac{v - V + E_s k_{21}}{k_{22}}
\end{array}
\right\} \tag{11}
$$

where,

$$k_{11} = \frac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}, \quad k_{12}\ \frac{g_{11}g_{22}-g_{12}^2}{g_{12}}, \quad I = I_1 - \frac{g_{11}}{g_{12}} I_2$$

$$k_{21} = -\frac{g_{23}}{g_{12}}, \qquad k_{22} = \frac{g_{22}}{g_{12}}, \qquad V = \frac{-1}{g_{12}} I_2$$

Solving for i in terms of v in (11) and letting $A \to \infty$ we obtain equations (8). A similar procedure yields equations (9) and (10). □

Our next result characterizes the properties of the driving-point characteristics of the piecewise-linear resistive one port shown in Fig. 59. First, we state the general case. The special case for op amp circuits will follow as a Corollary.

Theorem 2

Consider the nonlinear resistor terminated one-port shown in Fig. 59. Let R be an n-segment piecewise-linear voltage-controlled resistor described by the canonical equation [4]:

$$i_2 = a_0 + a_1v_2 + c_1|v_2-b_1| + \dots + c_n|v_2-b_n| \tag{12}$$

Let N be the two-port containing linear resistors, independent sources and linear controlled sources. Let N be described by the following transmission representation:

$$i = k_{11}i_2 + k_{12}v_2 + I$$

$$v = k_{21}i_2 + k_{22}v_2 + V$$

Then, the v-i driving-point characteristic is

(a) Strictly monotone-increasing if and only if

$$k_{12}k_{22}+(k_{11}k_{22}+K_{12}k_{21})(a_1+\sum_{\ell=1}^{k}c_\ell-\sum_{\ell=k+1}^{n}c_\ell)+k_{11}k_{21}(a_1+\sum_{=1}^{k}c_\ell-\sum_{\ell=k+1}^{n}c_\ell) > 0 \tag{13}$$

for all $k = 0, 1,, \dots, n$

(b) Current-controlled if and only if

$$k_{12}+k_{11}(a_1+\sum_{\ell=1}^{k}c_\ell-\sum_{\ell=k+1}^{n}c_\ell) > 0 \text{ (or } < 0\text{) for all } k = 0, 1, 2, \dots, n \tag{14}$$

(c) Voltage-controlled if and only if

$$k_{22} + k_{21}(a_1 + \sum_{\ell=1}^{k} c_\ell - \sum_{\ell=k+1}^{n} c_\ell) > 0 \text{ (or } < 0) \text{ for all } k = 0, 1, 2, \ldots, n \quad (15)$$

Furthermore, the driving-point characteristic is multivalued (i.e., neither voltage-controlled nor current-controlled) if neither one of (13), (14) nor (15) is satisfied.

Proof

An outline of the proof is as follows. First, using a similar procedure as in the proof of Theorem 1 we derive the driving-point characteristic which consists of n different segments. Then, using the fact that for a characteristic to be, for example, current-controlled, the range of the current for each segment should not overlap, we obtain conditions (13)-(15).

Corollary 2

The driving-point characteristic of a single op amp circuit (i.e., (8)-(10)) is

(a) Strictly monotone-increasing if and only if

$$\left.\begin{array}{l} g_{23} < 0 \\ g_{11}g_{23} - g_{12}g_{13} < 0 \end{array}\right\} \quad (16)$$

(b) Current-controlled if and only if

$$\left.\begin{array}{l} g_{23} > 0 \\ g_{11}g_{23} - g_{12}g_{13} < 0 \end{array}\right\} \quad (17)$$

(c) Voltage-controlled if and only if

$$\left.\begin{array}{l} g_{23} < 0 \\ g_{11}g_{23} - g_{12}g_{13} > 0 \end{array}\right\} \quad (18)$$

(d) Multivalued if and only if

$$\left.\begin{array}{l} g_{23} > 0 \\ g_{11}g_{23} - g_{12}g_{13} > 0 \end{array}\right\} \quad (19)$$

Proof

The proof is a special case of the proof of Theorem 2.

### B. Paramouncy

An nxn symmetric matrix $\underset{\sim}{G}$ is said to be Paramount iff each principle minor of order m is not less than the absolute value of any mth order minor built from the same rows (or columns), where m = 1, 2, ..., n-1 [8]. In particular for a 3x3 matrix we have the following conditions:

$$\underset{\sim}{G} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{12} & g_{22} & g_{23} \\ g_{13} & g_{23} & g_{33} \end{bmatrix}$$

$$\text{conditions involving first-order minors} \left\{ \begin{array}{l} g_{11} \geq |g_{12}|, \; g_{11} \geq |g_{13}| \\ g_{22} \geq |g_{12}|, \; g_{22} \geq |g_{23}| \\ g_{33} \geq |g_{13}|, \; g_{33} \geq |g_{23}| \end{array} \right.$$

$$\text{conditions involving second-order minors} \left\{ \begin{array}{l} \Delta_{11} \geq |\Delta_{13}|, \; \Delta_{11} \geq |\Delta_{12}| \\ \Delta_{22} \geq |\Delta_{21}|, \; \Delta_{22} \geq |\Delta_{23}| \\ \Delta_{33} \geq |\Delta_{31}|, \; \Delta_{33} \geq |\Delta_{32}| \end{array} \right.$$

where,

$\Delta_{ij}$ = determinant of the submatrix obtained by deleting row i and column j.

An example of a paramount matrix is shown below.

$$\underset{\sim}{G} = \begin{bmatrix} 3 & 2 & -2 \\ 2 & 2 & -1 \\ -2 & -1 & 2 \end{bmatrix} \quad \begin{array}{ll} \Delta_{11} = 3 & |\Delta_{12}| = |\Delta_{21}| = 2 \\ \Delta_{22} = 2 & |\Delta_{13}| = |\Delta_{31}| = 2 \\ \Delta_{33} = 2 & |\Delta_{23}| = |\Delta_{32}| = 1 \end{array}$$

The inverse of a non-singular paramount matrix is also paramount. Paramouncy is a weaker condition than diagonal dominancy but a stronger condition than positive definitness.

### C. Canonical Circuit

It has been shown [8] that a necessary and sufficient condition for a 3x3 matrix to be realizable as a short-circuit admittance of a 3-port resisitve network made of positive linear resistances is that it be a paramount matrix. In this subsection we use this fact to systematically derive the canonical circuit in Fig. 2.

Consider any of the odd-symmetric driving-point characteristics in Fig. 1(b). Comparing equations (8)-(10) with any of these characteristics we obtain the following equations. (Note that we are assuming no batteries, i.e., $I_1 = I_2 = 0$ in (8)-(10)).

$$m_0 = m_2 = \frac{g_{11}g_{22}-g_{12}^2}{g_{22}} \tag{20}$$

$$m_1 = \frac{g_{11}g_{23}-g_{12}g_{13}}{g_{23}} \tag{21}$$

$$E_B = E_s\left(\frac{g_{23}}{g_{12}}\right) \tag{22}$$

we are now ready to present the algorithm for synthesizing any of the characteristics in Fig. 1(b).

Step 1

Using (20)-(22) find a paramount $\underset{\sim}{G}$ matrix. Two parameters can be chosen arbitrarily. However, the above Corollary must also be taken into account, i.e., $\underset{\sim}{G}$ must satisfy the appropriate inequalities (16), (17), (18) or (19).

Step 2

Realize the $\underset{\sim}{G}$ matrix from Step 1. An algorithm for accomplishing this task is given in [8]. We need at most six positive linear resistors. The 3-port shown in Fig. 60 can be used to realize any 3x3 paramount conductance matrix.

Step 3

Connect the 3-port obtained in Step 2 to an op amp and complete the synthesis procedure.

Example

For the characteristic shown in Fig. 61 we have

$m_0 = 2$, $m_1 = -1$, $E_B = -5$

Assume, $E_s = 10$ volts.

Step 1. Choose $g_{22} = g_{12} = 2$, then (20)-(22) yield

$g_{23} = -1$, $g_{11} = 4$, $g_{13} = -\frac{5}{2}$

Hence,

$$G = \begin{bmatrix} 4 & 2 & -5/2 \\ 2 & 2 & -1 \\ -5/2 & -1 & 5/2 \end{bmatrix}$$

which is paramount. Also

$$g_{23} = -1 < 0$$

$$g_{11}g_{23} - g_{12}g_{13} = -4 + 5 = 1 > 0$$

i.e., condition (18) of the above Corollary is also satisfied.

Step 2. Using the algorithm in [8], we find the 3-port in Fig. 62 realizing the $\underset{\sim}{G}$ matrix from Step 1.

Step 3. Connecting the 3-port in Step 2 to an op amp we get the circuit in Fig. 63 which realizes the characteristic shown in Fig. 61.

The canonical circuit in Fig. 2 is then obtained by finding the "union" of all the circuits which realize the characteristics in Fig. 1(b).

Let us now derive the slope-breakpoint inequality from Section 2. The sufficiency of these inequalities follow directly from the design formulas given in Section 2. We prove the necessity of these inequalities one case at a time. Consider the design algorithm in Fig. 3(b), substituting for $E_1$ in $R_4$ we have:

$$\frac{R_4}{R_3} = \frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{E_{B2}|E_{s-}|-E_{B1}|E_{s-}|-E_{B1}^2+E_{B1}E_{B2}} \tag{23}$$

$$= \frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{|E_{s-}|(E_{B2}-E_{B1})+E_{B1}(E_{B2}-E_{B1})}$$

$$= \frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{(E_{B1}+|E_{s-}|)(E_{B2}-E_{B1})}$$

$$\therefore \frac{R_4}{R_3} = \frac{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{E_{B2}-E_{B1}} \tag{24}$$

To get $\frac{R_4}{R_3} > 0$ we need

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1 \tag{25}$$

which is part of the slope-breakpoint inequality (1). Next, substitute for $R_7$ into $R_6$ to get:

$$R_6 = \frac{1+\frac{R_4}{R_3}}{m_1+m_0\frac{R_4}{R_3}} \tag{26}$$

substiting (24) into (26) we have:

$$R_6 = \frac{E_{B2}-E_{B1}+E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{m_1(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}$$

$$= \frac{E_{s+}+|E_{s-}|}{(m_1-m_0)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{27}$$

For $R_6$ to be positive the demoninator in (27) must be positive, i.e.,

$$(m_1-m_0)(E_{B2}-E_{B1}) > -\,m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_0-m_1}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} \tag{28}$$

which is the second part of the slope-breakpoint inequality (1).

To derive the necessity of (2) consider the design algorithm of Fig. 12 (b). Substituting for $R_4$ into $R_5+R_6$ we have:

$$R_5+R_6 = \frac{E_{s+}+|E_{s-}|}{m_0(E_{s+}+|E_{s-}|)-I_{B2}+I_{B1}} \tag{29}$$

For $R_5 + R_6$ to be positive we need the denominator in (29) to be positive, i.e.,

$$m_0(E_{s+}+|E_{s-}|) > I_{B2} - I_{B1}$$

or

$$m_0 > \frac{I_{B2}-I_{B1}}{E_{s+}+|E_{s-}|} \tag{30}$$

which is condition (2) of Section 2.

A similar procedure can be used to derive these inequalities for all other cases. These are presented in the Appendix.

## 6. Conclusions

In this paper the inherent saturation nonlinearity of the op amp was used to design circuits with a wide variety of useful nonlinear v-i characteristics. We have shown that under a rather mild assumption, these circuits are made of one op amp and 3 or 4 linear positive resistors. Explicit design formulas have been presented for each prototype circuit and numerous examples have been given and validated by actual measurements. Several useful applications have also been presented. In particular, formulas for the design of a chaotic circuit have been given. It should be noted that an interactive software package for the design of these circuits has been developed.

## Appendix

### Proof for Fig. 6(b)

Consider the design algorithm in Fig. 6(b). Substituting for $R_4$ into $R_3$ we have:

$$R_3 = \frac{(m_1-m_0)\frac{(E_{s+}+|E_{s-}|)}{m_1(E_{B2}-E_{B1})}}{(m_0-m_1)+\frac{m_0(E_{s+}+|E_{s-}|)}{E_{B2}-E_{B1}}}$$

$$= \frac{\frac{(m_1-m_0)}{m_1}(E_{s+}+|E_{s-}|)}{(m_0-m_1)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{31}$$

For $R_3$ to be positive the denominator in (31) must be positive, i.e.,

$$(m_0-m_1)(E_{B2}-E_{B1}) > -\, m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_1-m_0}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}$$

which is the slope-breakpoint inequality of Section 2.

### Proof for Fig. 9(b)

Next, consider the design algorithm in Fig. 9(b). Substituting for $E_1$ into $R_4$ we have:

$$\frac{R_4}{R_3} = \frac{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{E_{B2}-E_{B1}} \tag{32}$$

Since $E_{B2} - E_{B1} > 0$, for $\frac{R_4}{R_3}$ to be positive we need

$$E_{s+}+|E_{s-}|+E_{B1}-E_{B2} > 0$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is part of the slope-breakpoint inequality. Substituting for $R_7$ into

$R_6$ we have:

$$R_6 = \frac{1+R_4/R_3}{m_0 \frac{R_4}{R_3}} \tag{33}$$

Substituting from (32) into (33) we get:

$$R_6 = \frac{E_{B2}-E_{B1}+E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{m_0(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}$$

$$= \frac{E_{s+}+|E_{s-}|}{m_0(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}$$

Since $m_0 > 0$, for $R_6$ to be positive we need

$$E_{s+}+|E_{s-}|+E_{B1}-E_{B2} > 0$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is again the slope-breakpoint equality. Note that since $m_1 = 0$ for this case, conditions (1a) and (1b) are identical.

Proof for Fig. 15(b)

Next, consider the design algorithm in Fig. 15(b). Substituting for $E_1$ into $R_4$ we have

$$\frac{R_4}{R_3} = \frac{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{E_{B2}-E_{B1}} \tag{34}$$

since the demoninator in (34) is always positive, for $\frac{R_4}{R_3}$ to be positive we need:

$$E_{s+}+|E_{s-}| > E_{B2} - E_{B1}$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is condition (1b). To derive (1a), substitute for $R_7$ into $R_6$ to get

$$R_6 = \frac{1+\frac{R_4}{R_3}}{m_1+m_0\,\frac{R_4}{R_3}} \tag{35}$$

substituting from (34) into (35) we have:

$$R_6 = \frac{E_{s+}+|E_{s-}|}{(m_1-m_0)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{36}$$

For $R_6$ to be positive, the denominator in (36) must be positive, i.e.,

$$(m_1-m_0)(E_{B2}-E_{B1}) > -m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_0-m_1}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}$$

which is condition (1a).

<u>Proof for Fig. 18(b)</u>

Consider the design algorithm in Fig. 18(b). Substituting for $E_2$ into $R_6$ we have:

$$\frac{R_6}{R_7} = \frac{E_{B2}-E_{B1}}{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}} \tag{37}$$

For $\frac{R_6}{R_7} > 0$ we need the denominator in (37) to be positive, i.e.,

$$E_{s+}+|E_{s-}| > E_{B2} - E_{B1}$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is condition (1b). To derive (1a), substitute for $R_4$ into $R_3$ to get

$$R_3 = \frac{1+\frac{R_6}{R_7}}{m_0+m_1\,\frac{R_6}{R_7}} \tag{38}$$

substituting from (37) into (38) we have

$$R_3 = \frac{E_{B2}-E_{B1}}{m_0(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})+m_1(E_{B2}-E_{B1})}$$

$$= \frac{E_{B2}-E_{B1}}{(m_1-m_0)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{39}$$

since the numerator in (39) is always positive for $R_3$ to be positive we need:

$$(m_1-m_0)(E_{B2}-E_{B1}) > - m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_0-m_1}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}$$

which is condition (1a).

Proof for Fig. 21(b)

Consider the design algorithm in Fig. 21(b). Substituting for $E_2$ into $R_6$ we have:

$$\frac{R_6}{R_7} = \frac{E_{B2}-E_{B1}}{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}} \tag{40}$$

For $\frac{R_6}{R_7}$ to be positive, the denominator in (40) must be positive, i.e.,

$$E_{s+}+|E_{s-}| > E_{B2} - E_{B1}$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is condition (1b). Note that since $m_1 = 0$ in this case, conditions (1a) and (1b) are identical.

Proof for Fig. 24(b)

Consider the design algorithm in Fig. 24(b). Substituting for $R_7$ into $R_3 + R_5$ we have

$$R_3 + R_5 = \frac{E_{s+}+|E_{s-}|}{m_0(E_{s+}+|E_{s-}|)-I_{B2}+I_{B1}} \tag{41}$$

For $R_3 + R_5$ to be positive, the demoninator in (41) must be positive, i.e.,

$$m_0(E_{s+}+|E_{s-}|) > I_{B2} - I_{B1}$$

or

$$m_0 > \frac{I_{B2}-I_{B1}}{E_{s+}+|E_{s-}|}$$

which is condition (2).

Proof for Fig. 27(b)

Consider the circuit in Fig. 27(b). Substituting for $R_4$ into $R_6$ we have:

$$\frac{R_6}{R_4} = \frac{\frac{(m_1-m_0)}{m_1}(E_{s+}+|E_{s-}|)}{(m_0-m_1)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{42}$$

since $m_1 > m_0 > 0$ the numerator in (42) is positive. Therefore, for $\frac{R_6}{R_4}$ to be positive we need

$$(m_0-m_1)(E_{B2}-E_{B1}) > - m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_1-m_0}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}$$

which is condition (1a).

Proof for Fig. 30(b)

Consider the circuit in Fig. 30(b). Substituting for $E_2$ into $R_6$ we have

$$\frac{R_6}{R_7} = \frac{E_{B2}-E_{B1}}{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}} \tag{43}$$

since $E_{B2} - E_{B1}$ is always positive, for $\frac{R_6}{R_7}$ to be positive we need the demomina-tor to be positive, i.e.,

$$E_{s+}+|E_{s-}| > E_{B2} - E_{B1}$$

or

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}} > 1$$

which is condition (1b). To derive condition (1a), substitute for $R_4$ into $R_3$ to get:

$$R_3 = \frac{1+R_6/R_7}{m_0+m_1 \frac{R_6}{R_7}} \tag{44}$$

Substituting from (43) into (44) we have:

$$R_3 = \frac{E_{B2}-E_{B1}}{(m_1-m_0)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)} \tag{45}$$

Since the numerator in (45) is always positive, for $R_3$ to be positive we need

$$(m_1-m_0)(E_{B2}-E_{B1}) > -m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_0-m_1}{m_0} < \frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}$$

which is condition (1a).

## References


[1] J. G. Graeme, G. E. Tobey and L. P. Huelsman, Operational Amplifiers: Design and Applications, McGraw-Hill Book Company, New York, 1971.

[2] J. G. Graeme, Applications of Operational Amplifiers, McGraw-Hill Book Company, New York, 1973.

[3] Y. J. Wong and W. E. Ott, Function Circuits: Design and Applications, McGraw-Hill Book Company, New York, 1976.

[4] L. O. Chua and S. Wong, "Synthesis of piecewise-linear networks," IEEE J. Electronic Circuits and Systems, Vol. 2, No. 4, pp. 102-108, July 1978.

[5] L. O. Chua, Introduction to Nonlinear Network Theory, McGraw-Hill Book Company, New York, 1969.

[6] H. J. Reich, Functional Circuits and Oscillators, Van Nostrand Company, Princeton, Jew Jersey, 1961.

[7] J. Millman and H. Taub, Pulse, Digital and Switching Waveforms, McGraw-Hill Book Company, New York, 1965

[8] L. Weinberg, Network Analysis and Synthesis, McGraw-Hill Book Company, New York, 1962.

[9] L. O. Chua and Q. Q. Zhong, "Negative resistance curve tracer," Memorandum No. UCB/ERL M84/29, University of California, Berkeley, March 25, 1984.

[10] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, Chapters 5-6, John Wiley & Sons, Inc., 1977.

[11] T. Matsumoto, "A chaotic attractor from Chua's circuit," Memorandum No. UCB/ERL M84/36, University of California, Berkeley, April 17, 1984.

Figure Captions

Fig. 1. (a) Circuit configuration under study. (b) Possible v-i characteristics for the one-port in (a).

Fig. 2. Canonical circuit.

Fig. 3. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 4. (a) Odd-symmetric characteristic for example 1.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2v/div.

Fig. 5. (a) v-i characteristic for example 1.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div. v : 2v/div.

Fig. 6. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 7. (a) Odd-symmetric characteristic for example 2.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2v/div.

Fig. 8. (a) v-i characteristic for example 2.2. (b) Measured v-i characteristic. Scale, i : 5ma/div, v : 4 v/div.

Fig. 9. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 10. (a) Odd-symmetric characteristic for example 3.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 11. (a) v-i characteristic for example 3.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 12. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 13. (a) Odd-symmetric characteristic for example 4.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 14. (a) v-i characteristic for example 4.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 15. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 16. (a) Odd-symmetric characteristic for example 5.1. (b) Measured v-i characteristic. Scale, i : 1 ma/div, v : 1 v/div.

Fig. 17. (a) v-i characteristic for example 5.2. (b) Measured v-i characteristic. Scale, i : 1 ma/div, v : 1/div.

Fig. 18. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 19. (a) Odd-symmetric characteristic for example 6.1. (b) Measured v-i characteristic. Scale, i : 4 ma/div, v : 2 v/div.

Fig. 20. (a) v-i characteristic for example 6.2. (b) Measured v-i characteristic. Scale, i : 4 ma/div, v : 2 v/div.

Fig. 21. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 22. (a) Odd-symmetric characteristic for example 7.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 23. (a) v-i characteristic for example 7.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2v/div.

Fig. 24. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 25. (a) Odd-symmetric characteristic for example 8.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 26. (a) v-i characteristic for example 8.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 27. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 28. (a) Odd-symmetric characteristic for example 9.1. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 29. (a) v-i characteristic for example 9.2. (b) Measured v-i characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 30. (a) v-i characteristic to be synthesized. (b) Circuit configuration and element values.

Fig. 31. Odd-symmetric characteristic for example 10.1. (b) Measured i-v characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 32. (a) v-i characteristic for example 10.2. (b) Measured i-v characteristic. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 33. Odd-symmetric characteristic from Example 1.1 realized using an op amp with identical saturation voltage in Fig. 3(b) with $R_3$ = 1 kΩ, $R_4$ = 12 kΩ, $R_6$ = 520 Ω, and $R_7$ = 13 kΩ. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 34. Odd-symmetric characteristic from example 2.1 realized using an op amp with identical saturation voltages in Fig. 6(b) with $R_1$ = 500 Ω, $R_3$ = 590.9 Ω, $R_4$ = 3.25 kΩ. Scale, i : 4 ma/div, v : 4 v/div.

Fig. 35. Odd-symmetric characteristic from example 3.1 realized using an op amp with identical saturation voltages in Fig. 9(b) with $R_3$ = 1 kΩ,

$R_4$ = 2.5 kΩ, $R_6$ = 590.9 Ω, and $R_7$ = 3.25 kΩ. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 36. Odd-symmetric characteristic from example 4.1 realized using an op amp with identical saturation voltages in Fig. 12(b) with $R_4$ = 4.33 kΩ, $R_5$ = 26 kΩ, and $R_6$ = 26 kΩ. Scale, i : 2 ma/div, v : 2 v/div.

Fig. 37. Odd-symmetric characteristic from example 5.1 realized using an op amp with identical saturation voltages in Fig. 15(b) with $R_3$ = 1 kΩ, $R_4$ = 5.5 kΩ, $R_6$ = 619 Ω, and $R_7$ = 2.6 kΩ. Scale i : 2 ma/div, v : 2v/div.

Fig. 38. Odd-symmetric characteristic from example 6.1 realized using an op amp with identical saturation voltages in Fig. 18(b) with $R_3$ = 3.25 k , $R_4$ = 1.44 k , $R_6$ = 1 k , and $R_7$ = 3.33 k . Scale, i : 5 ma/div, v : 2 v/div.

Fig. 39. Odd-symmetric characteristic from example 7.1 realized using an op amp with identical saturation voltages in Fig. 21(b) with $R_3$ = 1.18 kΩ, $R_4$ = 6.5 kΩ, $R_6$ = 1 kΩ, and $R_7$ = 5.5 kΩ. Scale, i : 2 ma/div, v : 2v/div.

Fig. 40. Odd-smmetric characteristic from example 8.1 realized using an op amp with identical saturation voltages in Fig. 24(b) with $R_3$ = 1 kΩ, $R_5$ = 154 Ω, and $R_7$ = 6.5 kΩ. Scale, i : 2 ma/div, v : 2v/div.

Fig. 41. Odd-symmetric characteristic from example 9.1 realized using an op amp with identical saturation voltages in Fig. 27(b) with $R_1$ = 500 Ω, $R_3$ = 650 Ω, and $R_4$ = 2.167 kΩ. Scale, i : 4 ma/div, v : 2 v/div.

Fig. 42. Odd-symmetric characteristic from example 10.1 realized using an op amp with identical saturation voltages in Fig. 30(b) with $R_3$ = 590.9 Ω, $R_4$ = 3.25 kΩ, $R_6$ = 1 kΩ, and $R_7$ = 2.25 kΩ. Scale i : 4 ma/div, v : 4v/div.

Fig. 43. Circuit for realizing a battery using the power supply voltages.

Fig. 44. Circuit transformation to realize a series combination of a resistor and a battery using the power supply voltage.

Fig. 45. Circuit transformation to realize a battery directly connected to the op amp input terminal using the power supply voltage.

Fig. 46. (a) The circuit for a soft oscillator. (b) v-i characteristic for R.

Fig. 47. (a) Measured v-i characteristic for R realized using Fig. 15(b) with $R_3$ = 1 kΩ, $R_4$ = 5.5 kΩ, $R_6$ = 619 Ω and $R_7$ = 2.6 kΩ. Scale i : 2 ma/div, v : 2 v/div. (b) Measured voltage oscillations. Scale v : 2v/div, t : 200 μs/div.

Fig. 48. (a) Circuit for a hard oscillator. (b) v-i characteristic for the parallel combination of $R_1$ and $R_2$.

Fig. 49. (a) Measured v-i characteristic for $R_1$ using Fig. 15(b) with $R_3$ = 1 kΩ, $R_4$ = 13 k , $R_6$ = 6.22 k , $R_7$ = 11.2 k , $E_1$ = - 2.23 V, and $E_2$ = - 8.33 V. Scale i : 1 ma/div, v : 2 v/div. (b) Measured v-i characteristic for $R_2$ using Fig. 15(b) with $R_3$ = 1 kΩ, $R_4$ = 13 kΩ, $R_6$ = 6.22 kΩ, $R_7$ = 11. 2 kΩ, $E_1$ = 2.07 v, and $E_2$ = 7.22 v. Scale i : 1 ma/div, v : 2 v/div. (c) Measured v-i characteristic for the parallel combinationof $R_1$ and $R_2$. Scale i : 1 ma/div, v : 2 v/div. (d) Measured oscillations. Scale v : 5 v/div, t : 500 μs/div.

Fig. 50. (a) A three-state circuit. (b) v-i characteristic for the parallel combination of $R_1$ and $R_2$.

Fig. 51. (a) Measured v-i characteristic for the parallel combination of $R_1$ and $R_2$. (b) Cricuit used to measure v-i characteristic in (a).

Fig. 52. (a) A chaotic cirucit (b) v-i characteristic for R.

Fig. 53. Two v-i characteristics needed to realize R in Fig. 52.

Fig. 54. (a), (b) Measured v-i characteristics for $R_1$ and $R_2$ in the chaotic circuit example. Scale i : 2 ma/div, v : 4v/div. (c) Measured v-i characteristic for parallel combination of (a) and (b) representing R in the chaotic circuit. (d) Circuit used in these measurements.

Fig. 55. General circuit containing one op amp resistors and batteries.

Fig. 56. Piecewise-linear circuit model for an op amp.

Fig. 57. 3-port obtained by replacing the op amp in Fig. 55 with the model in Fig. 56.

Fig. 58. 2-port obtained by pulling out the only nonlinear element in Fig. 57.

Fig. 59. Circuit for Theorem 2.

Fig. 60. This 3-port can be used to realize any 3x3 paramount conductance matrix with positive resistors.

Fig. 61. v-i characteristic to be realized using the algorithm in Section 5.

Fig. 62. A realizationof the $\tilde{G}$ matrix in the above example.

Fig. 63. A circuit to realize the v-i characteristic in Fig. 61.

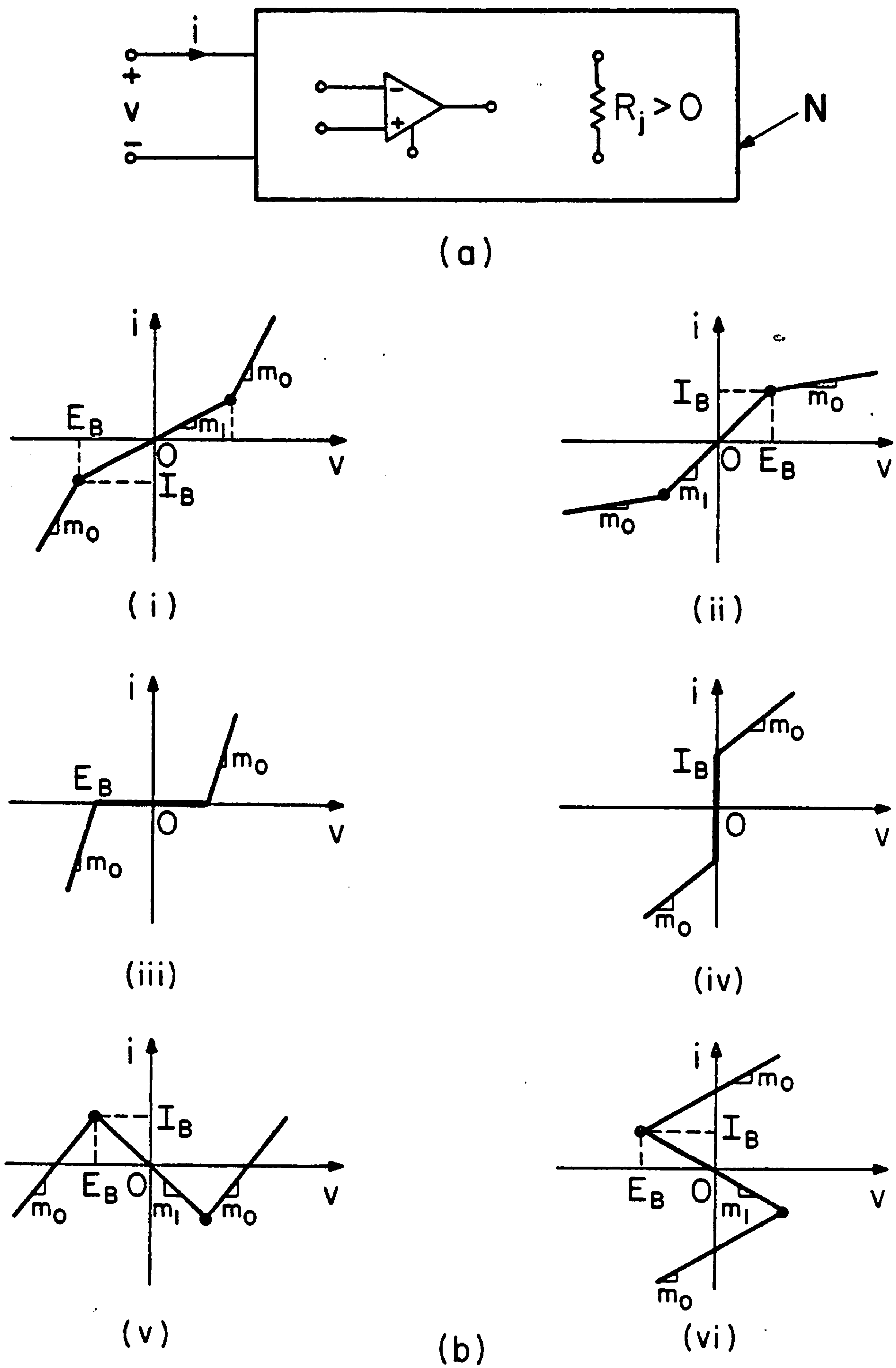
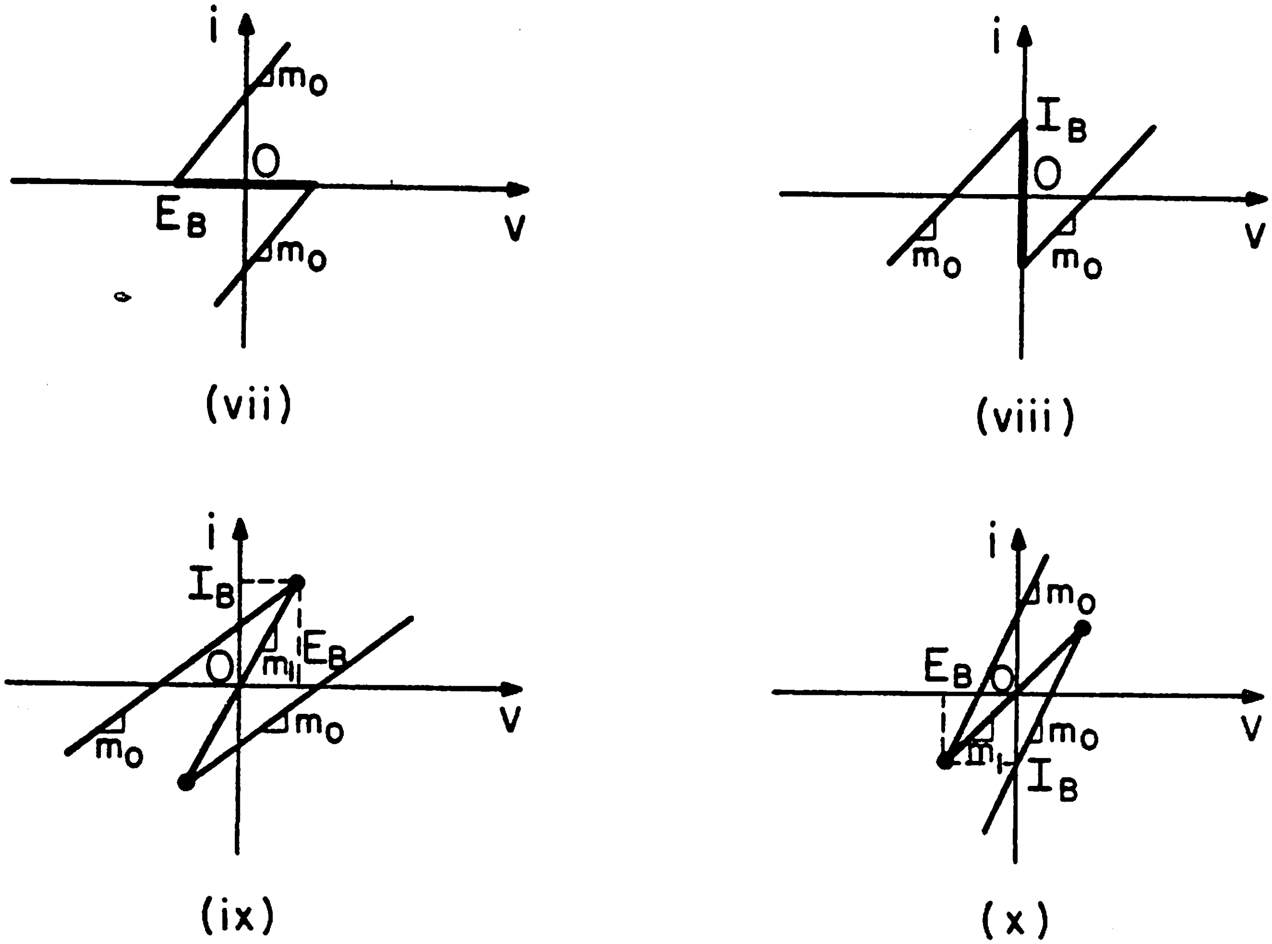



Fig. 1


i
v
O
$E_B$
$m_o$
$m_o$
(vii)
i
v
O
$I_B$
$m_o$
$m_o$
(viii)
i
v
O
$I_B$
$E_B$
$m_1$
$m_o$
$m_o$
(ix)
i
v
O
$E_B$
$I_B$
$m_1$
$m_o$
$m_o$
(x)

(b)

Fig. 1 (Cont'd)

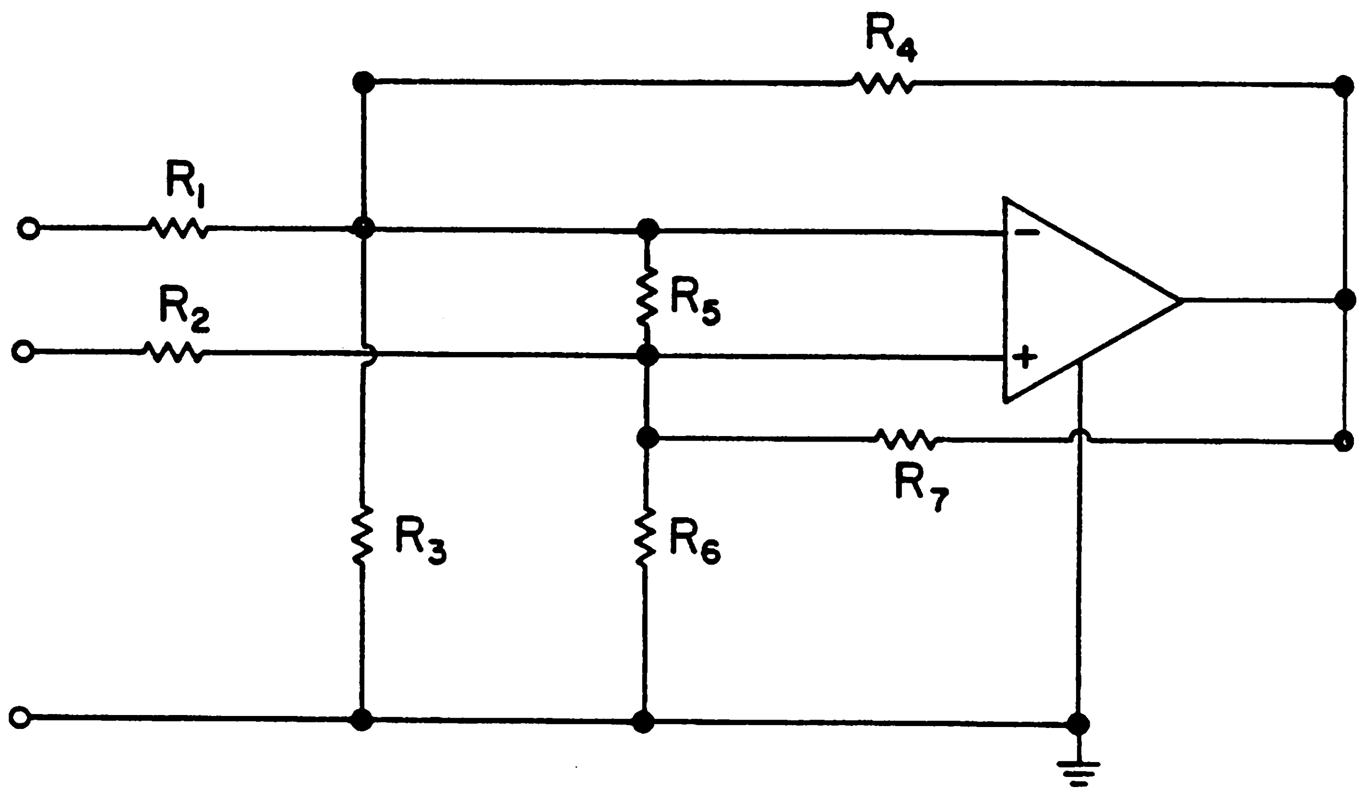
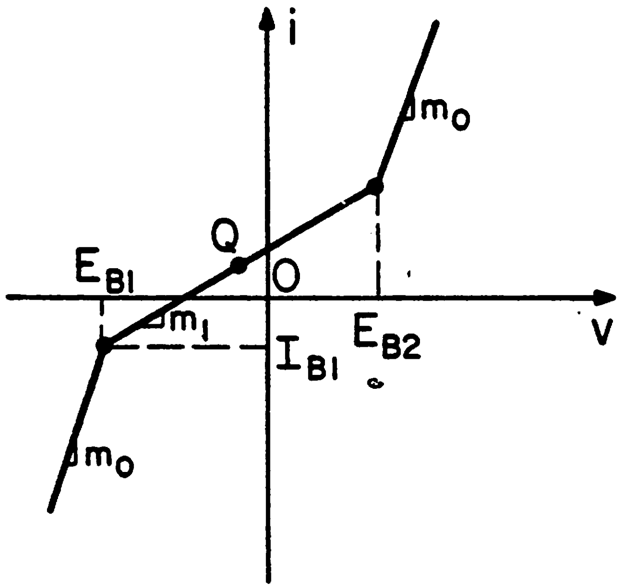



Fig. 2



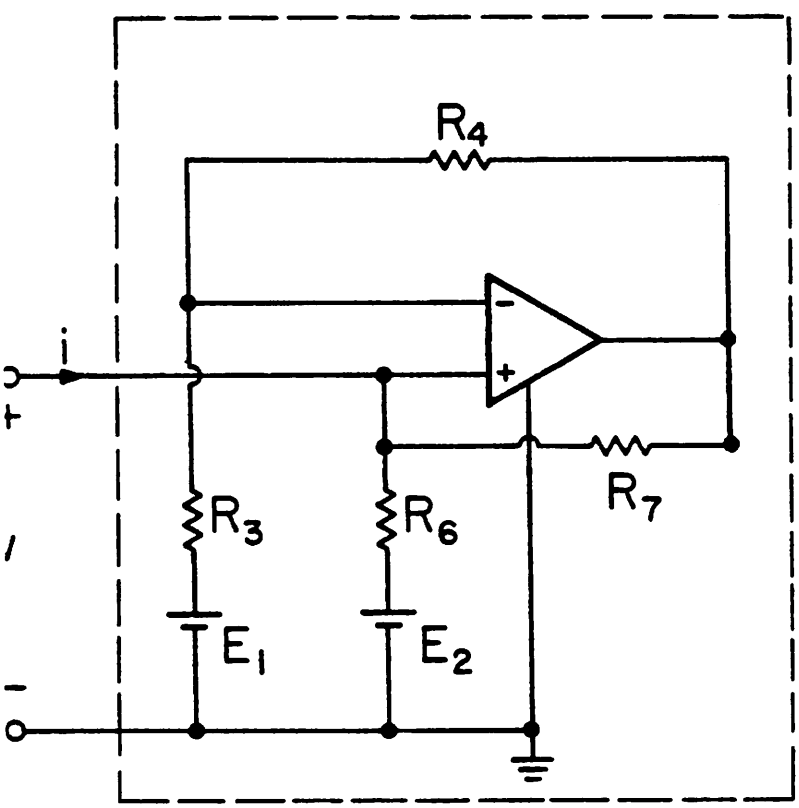

(a)

## Assumptions:

$0 < m_0 < \infty$

$0 \le m_1 < \infty$

$m_1 < m_0$




## Design Algorithm:

Choose any convenient value $R_3 > 0$ calculate:

$$E_1 = \frac{E_{B1}E_{S+} + E_{B2}|E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_4 = \left[\frac{E_{B1} + |E_{S-}|}{E_1 - E_{B1}}\right] R_3$$

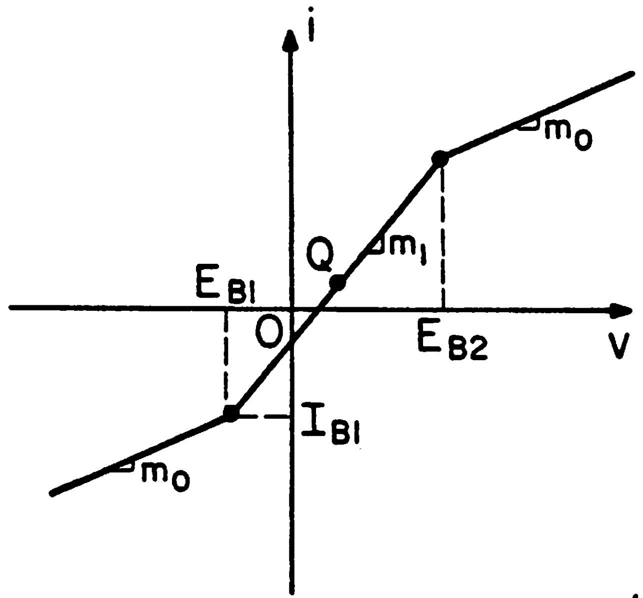
$$R_7 = \frac{R_3 + R_4}{(m_0 - m_1)R_3}$$

$$R_6 = \frac{R_7}{m_0 R_7 - 1}$$

$$E_2 = R_6\left[m_0 E_{B1} + \frac{|E_{S-}|}{R_7} - I_{B1}\right]$$

(b)

Fig. 3



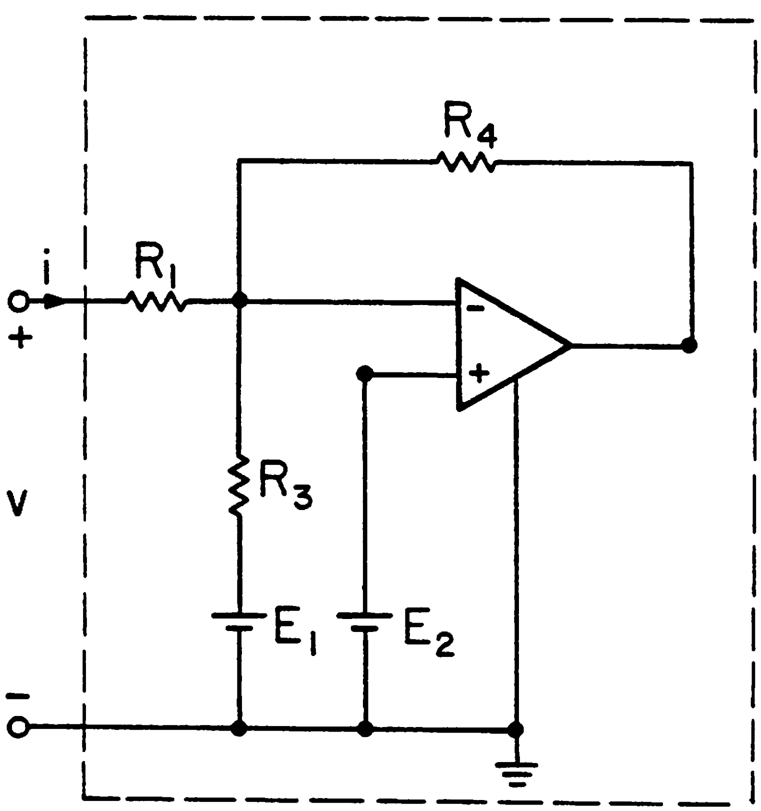

**Assumptions:**

$0 < m_0 < \infty$

$0 < m_1 < \infty$

$m_1 > m_0$

(a)




**Design Algorithm:**

Calculate:

$$R_1 = \frac{1}{m_1}$$

$$R_4 = \frac{(E_{S+} + |E_{S-}|)R_1}{E_{B2} - E_{B1}}$$

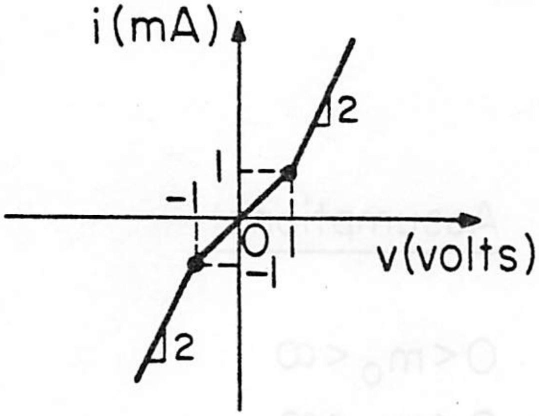
$$R_3 = \frac{(m_1 - m_0)R_4}{(m_0 - m_1) + m_0 m_1 R_4}$$

$$E_2 = E_{B1} - R_1 I_{B1}$$

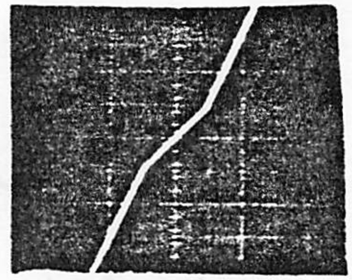
$$E_1 = R_3\left[E_2\left(\frac{R_3 + R_4}{R_3 R_4}\right) - \frac{E_{S+}}{R_4} - I_{B1}\right]$$

(b)

Fig. 6

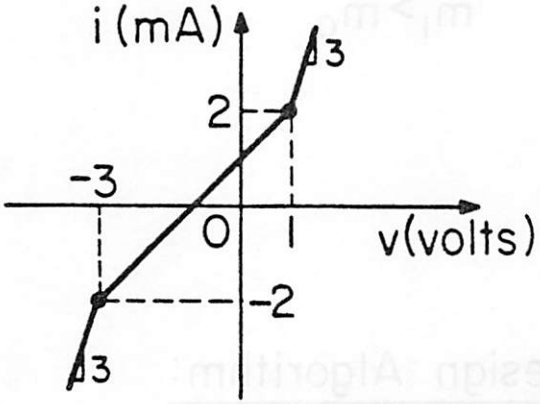



(a)

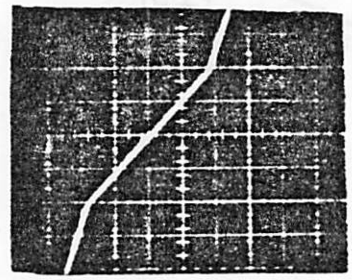


(b)

Fig. 4

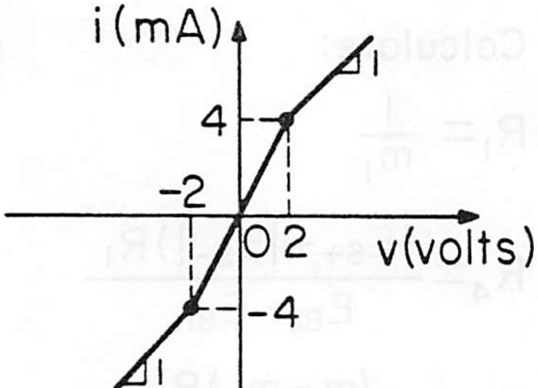



(a)

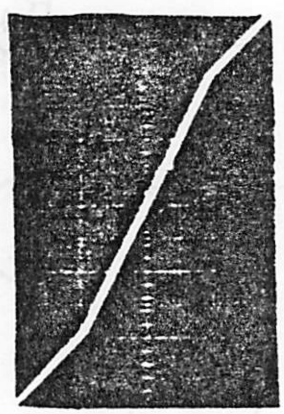


(b)

Fig. 5

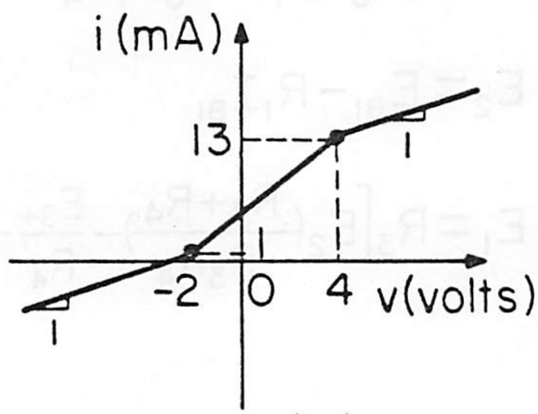



(a)

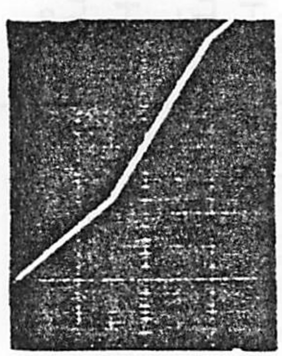


(b)

Fig. 7

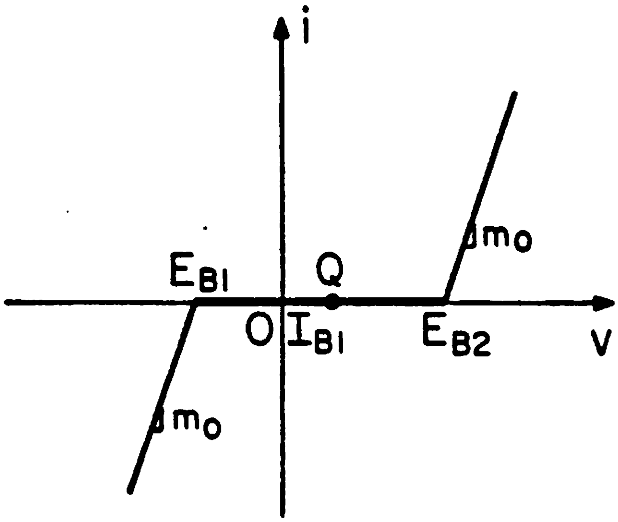



(a)



(b)

Fig. 8

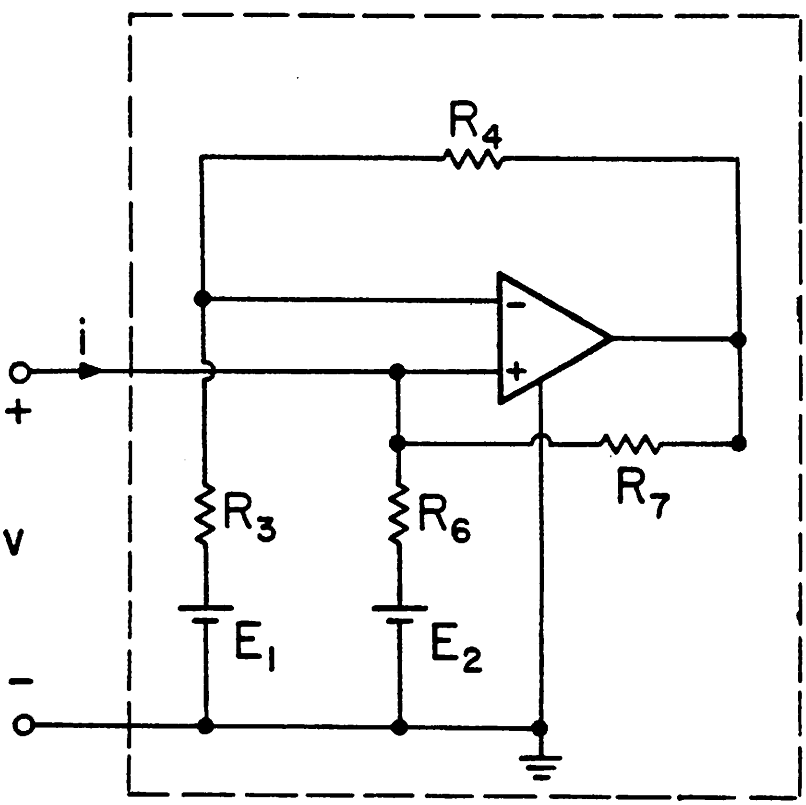



### Assumptions:

$0 < m_0 < \infty$

$m_1 = 0$

(a)




### Design Algorithm:

Choose any convenient value $R_3 > 0$, calculate:

$$E_1 = \frac{E_{B1}E_{S+} + E_{B2}|E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_4 = \left[\frac{E_{B1} + |E_{S-}|}{E_1 - E_{B1}}\right] R_3$$

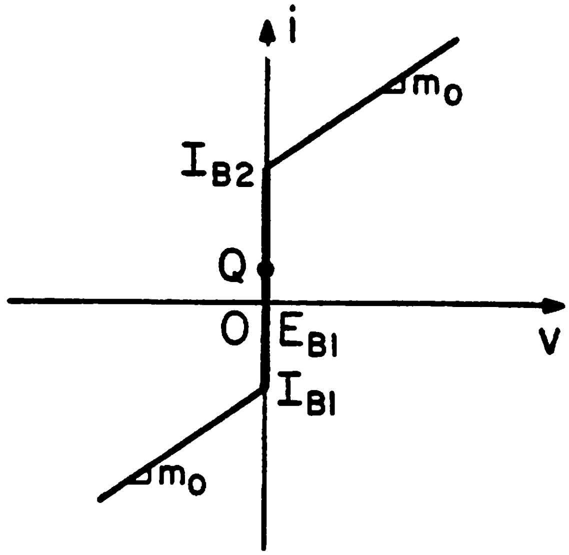
$$R_7 = \frac{R_3 + R_4}{m_0 R_3}$$

$$R_6 = \frac{R_7}{m_0 R_7 - 1}$$

$$E_2 = R_6\left[m_0 E_{B1} + \frac{|E_{S-}|}{R_7} - I_{B1}\right]$$

(b)

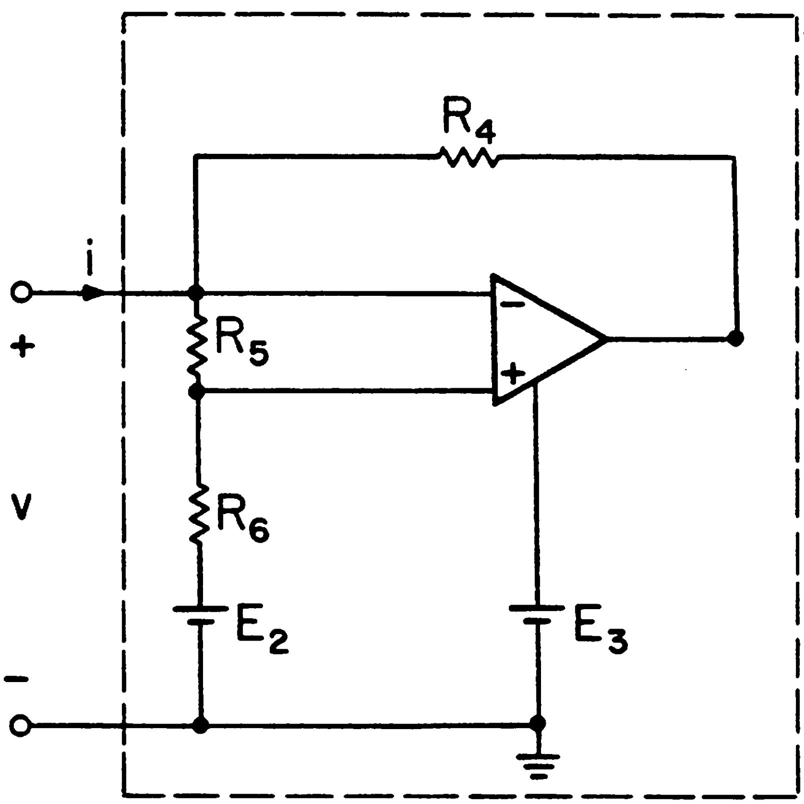
Fig. 9




**Assumptions:**

$$0 < m_0 < \infty$$
$$m_1 = \infty$$

(a)




**Design Algorithm:**

Choose $R_5 > 0$, $R_6 > 0$ s.t.

$$R_4 = \frac{E_{S+} + |E_{S-}|}{I_{B2} - I_{B1}}$$

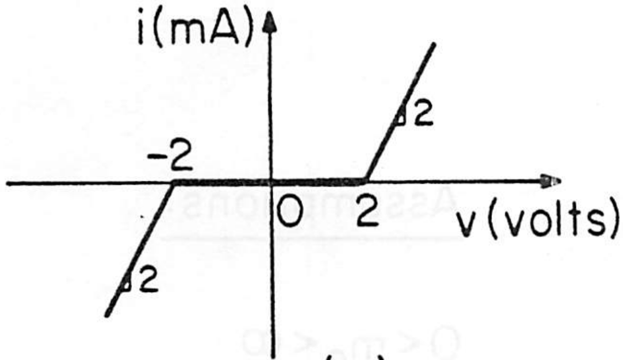
$$R_5 + R_6 = \frac{R_4}{m_0 R_4 - 1}$$

$$E_2 = E_B$$

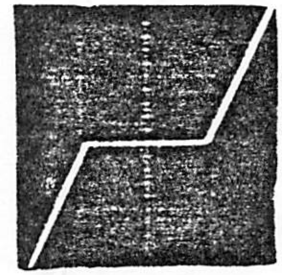
$$E_3 = E_2 - |E_{S-}| - R_4 I_{B1}$$

(b)

Fig. 12

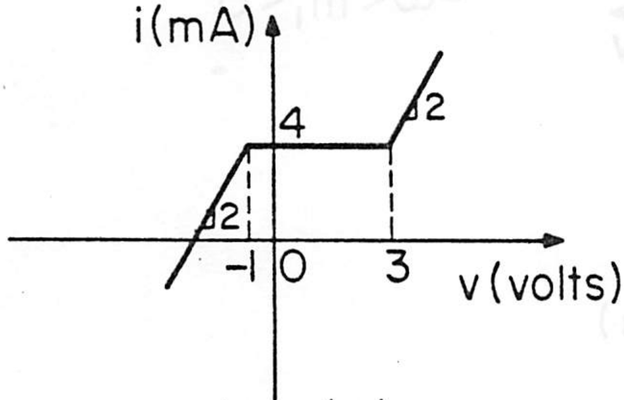



(a)

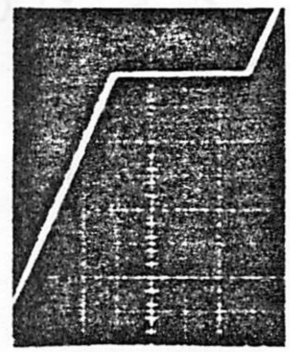


(b)

Fig. 10

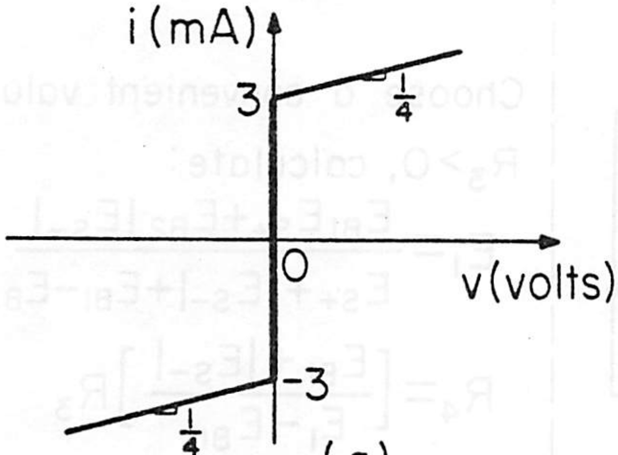



(a)

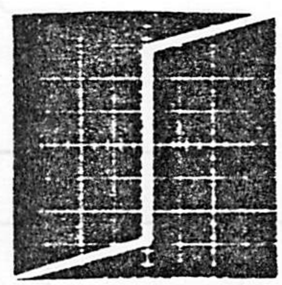


(b)

Fig. 11

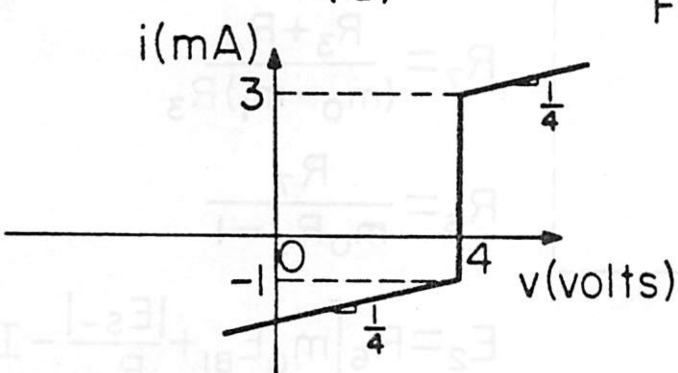



(a)

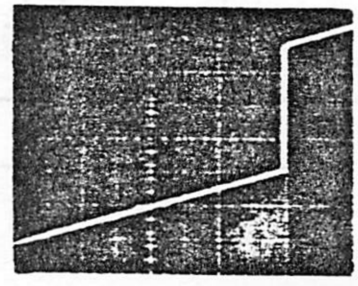


(b)

Fig. 13

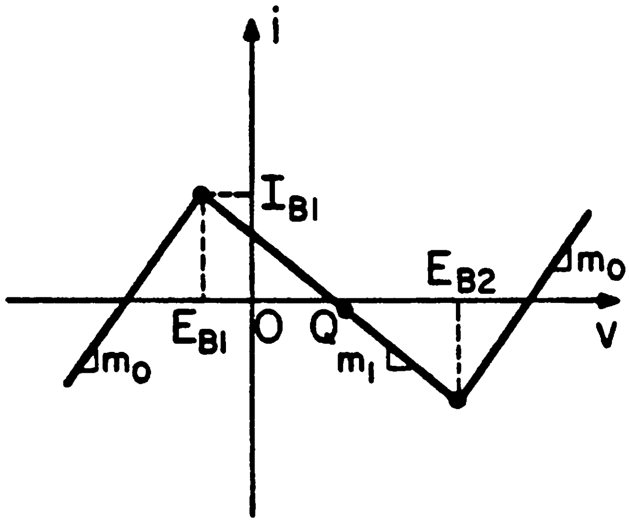



(a)



(b)

Fig. 14

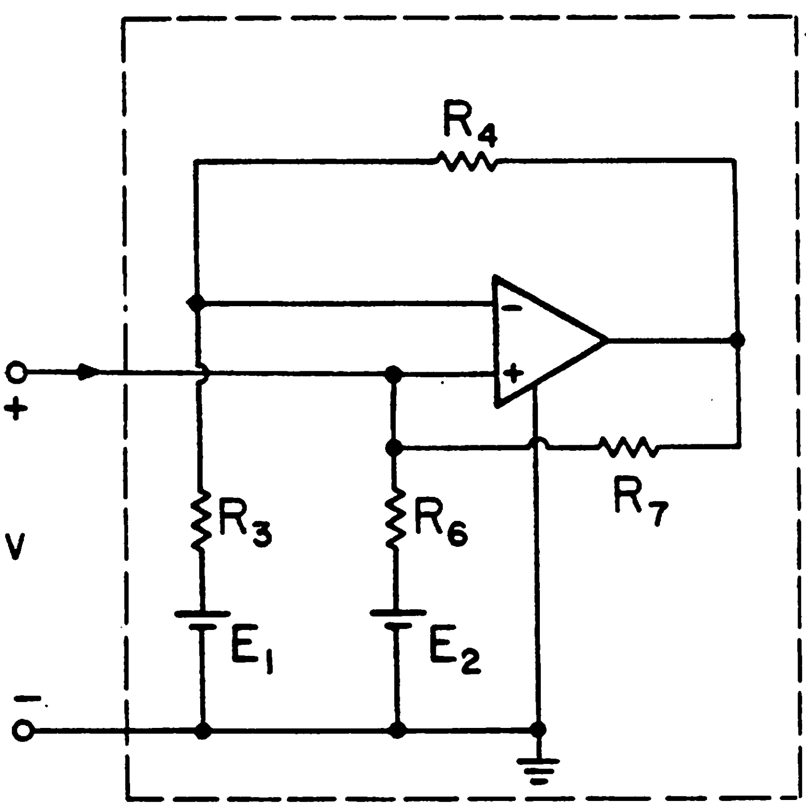



### Assumptions:

$0 < m_0 < \infty$

$-\infty < m_1 < 0$

(a)




### Design Algorithm:

Choose a convenient value $R_3 > 0$, calculate:

$$E_1 = \frac{E_{B1}E_{S+} + E_{B2}|E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_4 = \left[\frac{E_{B1} + |E_{S-}|}{E_1 - E_{B1}}\right]R_3$$

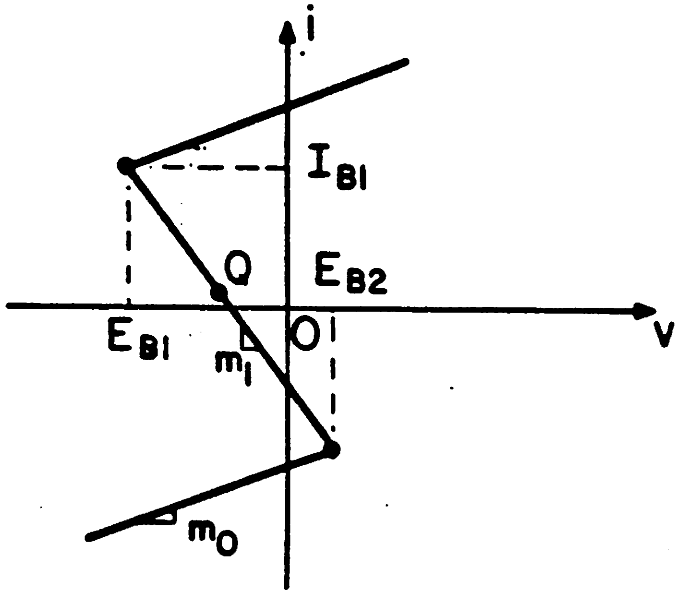
$$R_7 = \frac{R_3 + R_4}{(m_0 - m_1)R_3}$$

$$R_6 = \frac{R_7}{m_0 R_7 - 1}$$

$$E_2 = R_6\left[m_0 E_{B1} + \frac{|E_{S-}|}{R_7} - I_{B1}\right]$$

(b)

Fig. 15

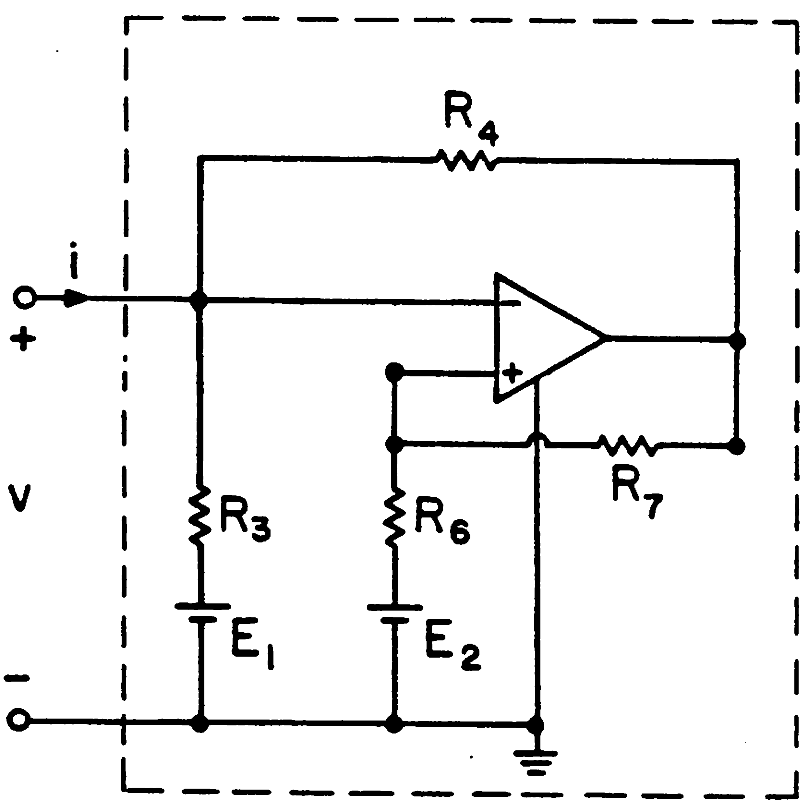



**Assumptions:**

$0 < m_0 < \infty$

$-\infty < m_1 < 0$

(a)




**Design Algorithm**

Choose convenient value for $R_7 > 0$, calculate:

$$E_2 = \frac{E_{B1}E_{S+} + E_{B2}|E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_6 = \left[\frac{E_2 - E_{B1}}{E_{B1} + |E_{S-}|}\right] R_7$$

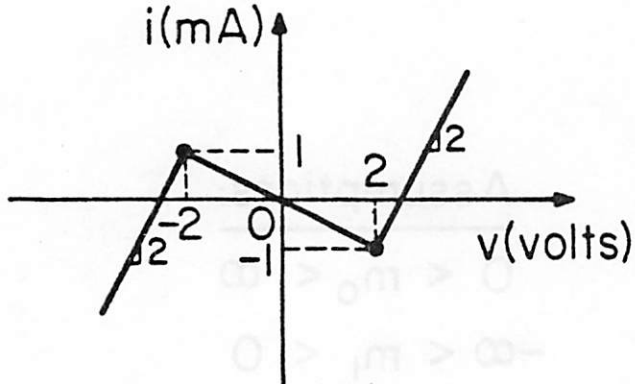
$$R_4 = \frac{R_6 + R_7}{(m_0 - m_1)R_6}$$

$$R_3 = \frac{R_4}{m_0 R_4 - 1}$$

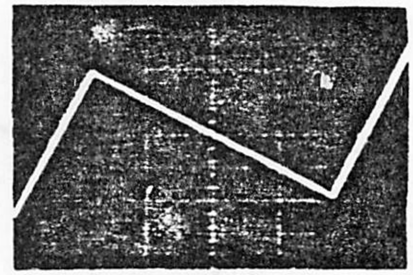
$$E_1 = R_3\left[m_0 E_{B1} + \frac{|E_{S-}|}{R_4} - I_{B1}\right]$$

(b)

Fig. 18

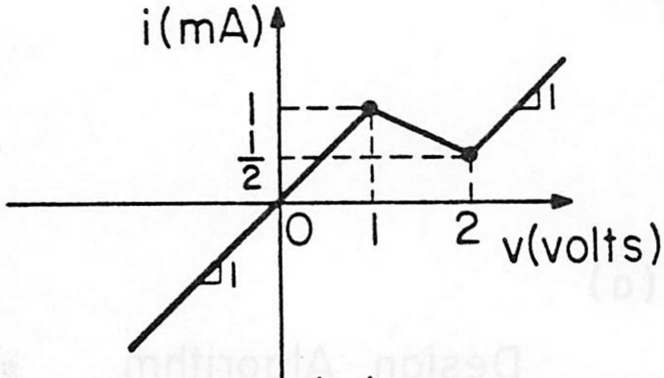



(a)

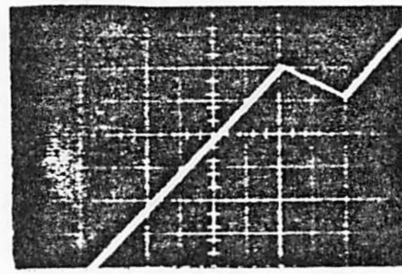


(b)

Fig. 16

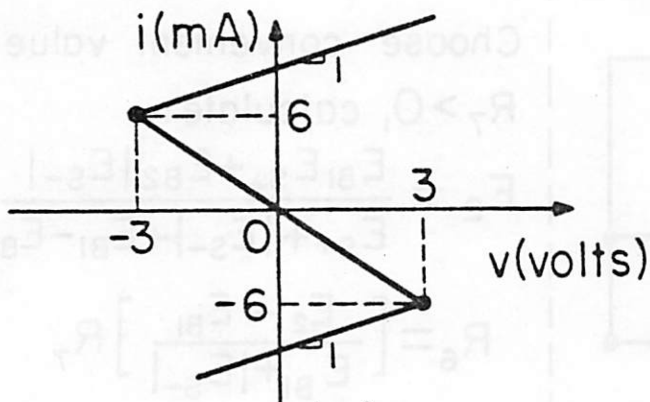



(a)

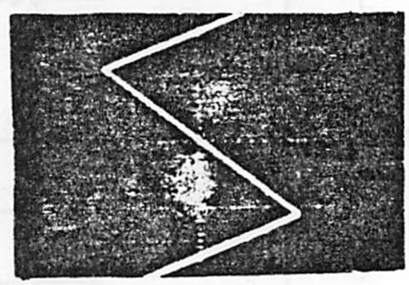


(b)

Fig. 17

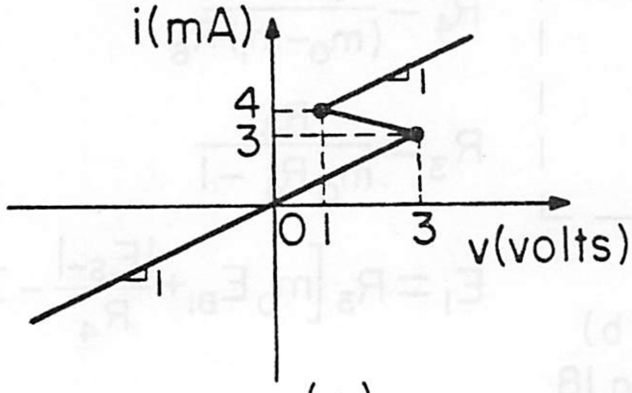



(a)

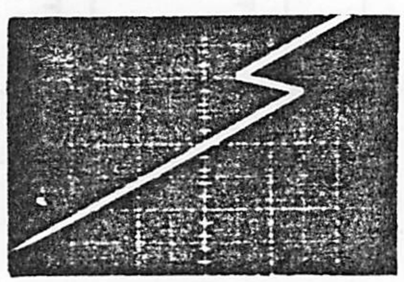


(b)

Fig. 19

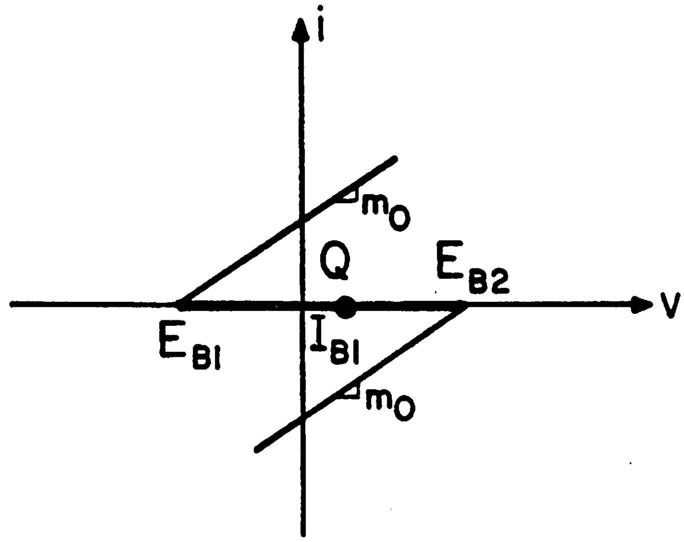



(a)



(b)

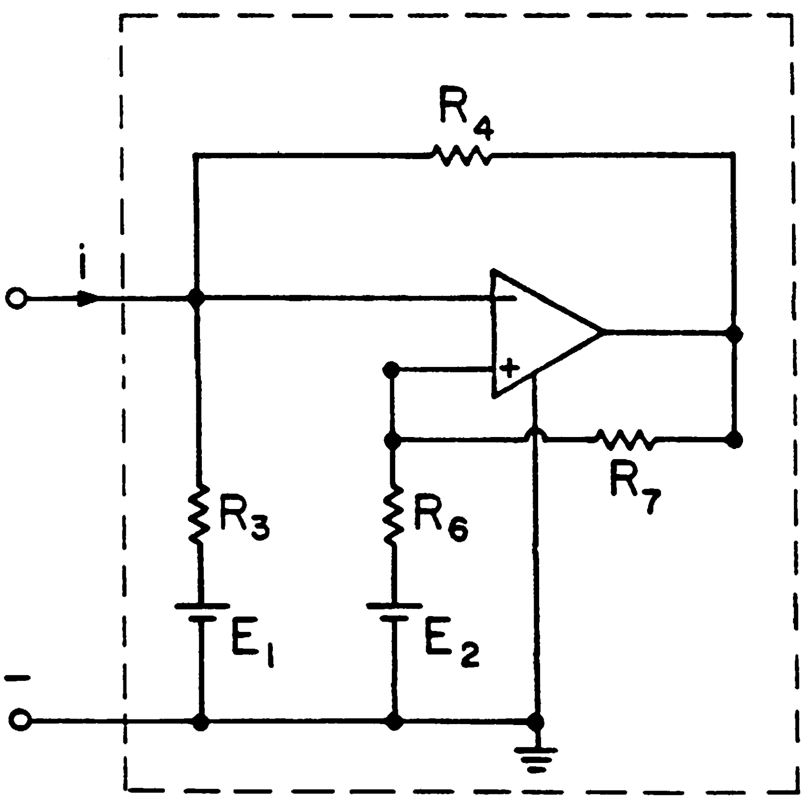
Fig. 20




## Assumptions:

$$0 < m_0 < \infty$$
$$m_1 = 0$$

(a)




## Design Algorithm

Choose convenient value for $R_7 > 0$, calculate:

$$E_2 = \frac{E_{B1} E_{S+} + E_{B2} |E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_6 = \left[ \frac{E_2 - E_{B1}}{E_{B1} + |E_{S-}|} \right] R_7$$

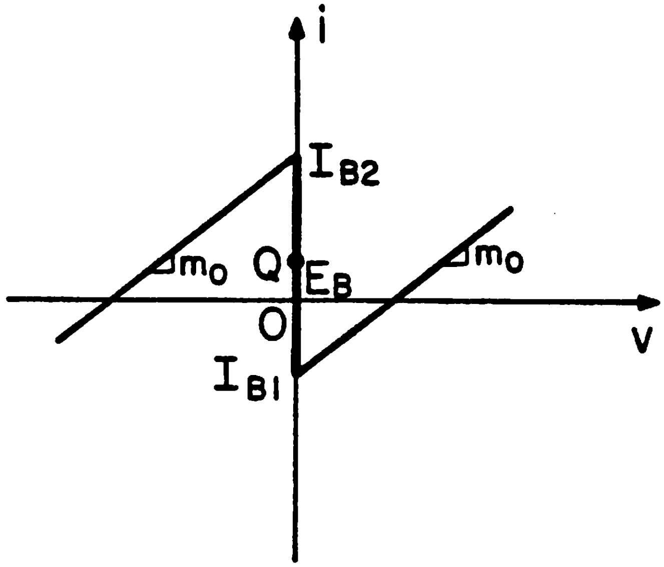
$$R_4 = \frac{R_6 + R_7}{m_0 R_6}$$

$$R_3 = \frac{R_4}{m_0 R_4 - 1}$$

$$E_1 = R_3 \left[ m_0 E_{B1} + \frac{|E_{S-}|}{R_4} - I_{B1} \right]$$

(b)

Fig. 21

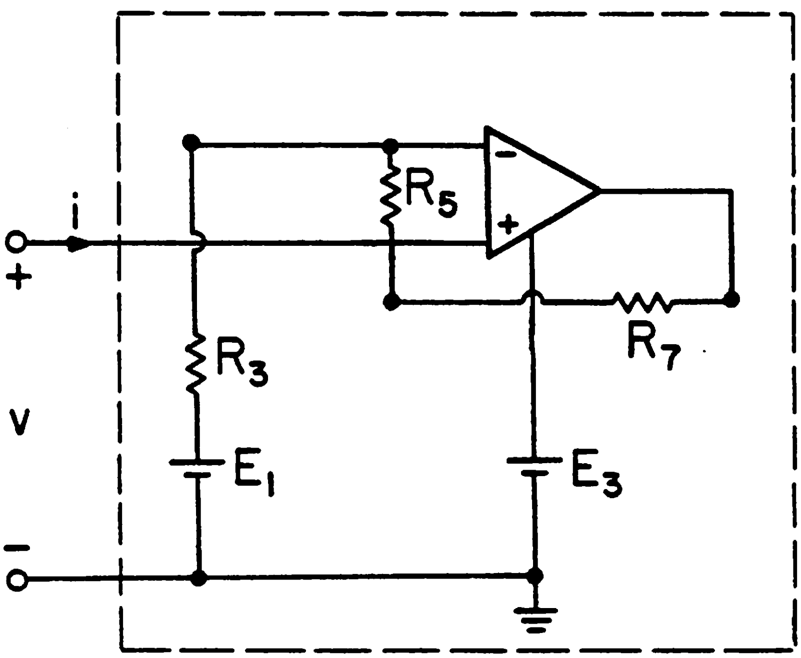



## Assumptions:

$$0 < m_0 < \infty$$

$$m_1 = \infty$$

(a)




## Design Algorithm:

Choose any $R_3 > 0$, $R_5 > 0$ s.t.

$$R_7 = \frac{E_{S+} + |E_{S-}|}{I_{B2} - I_{B1}}$$

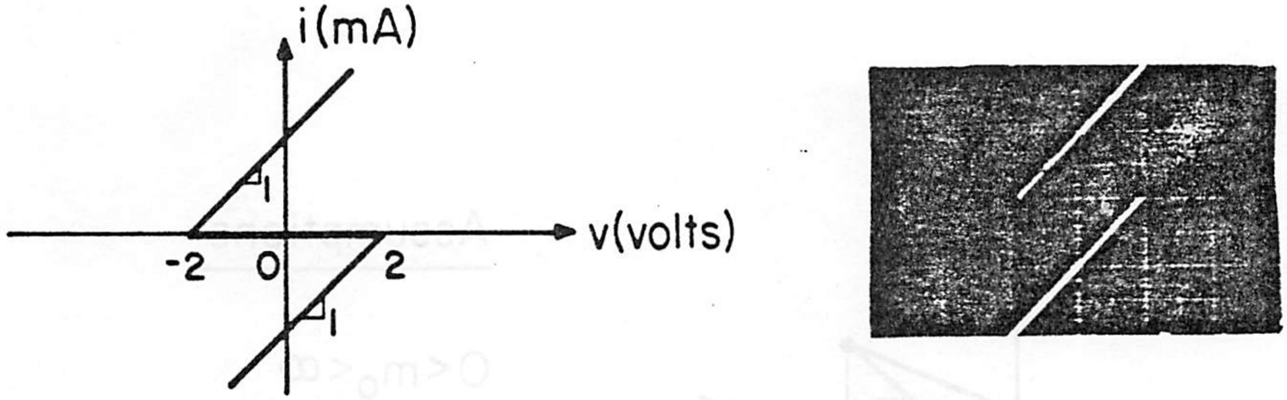
$$R_3 + R_5 = \frac{R_7}{m_0 R_7 - 1}$$

$$E_1 = E_B$$

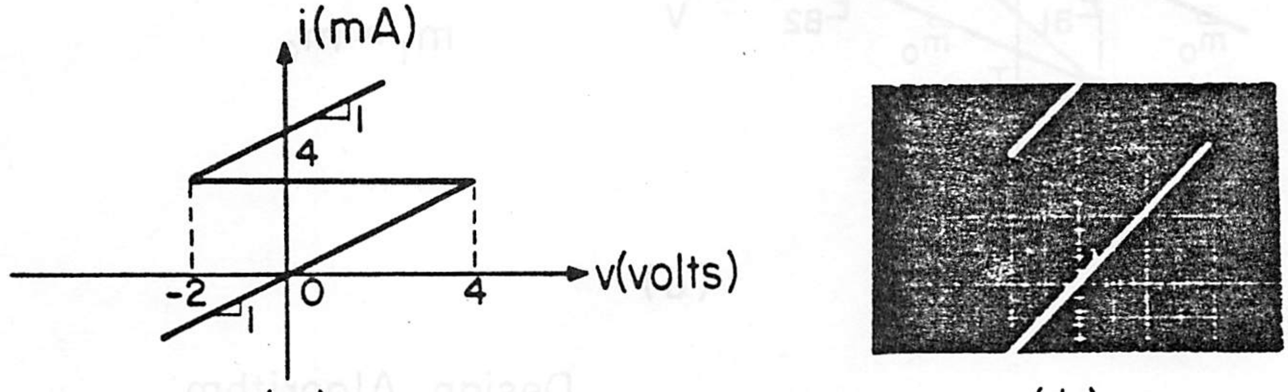
$$E_3 = E_1 - E_{S+} - R_7 I_{B1}$$

(b)

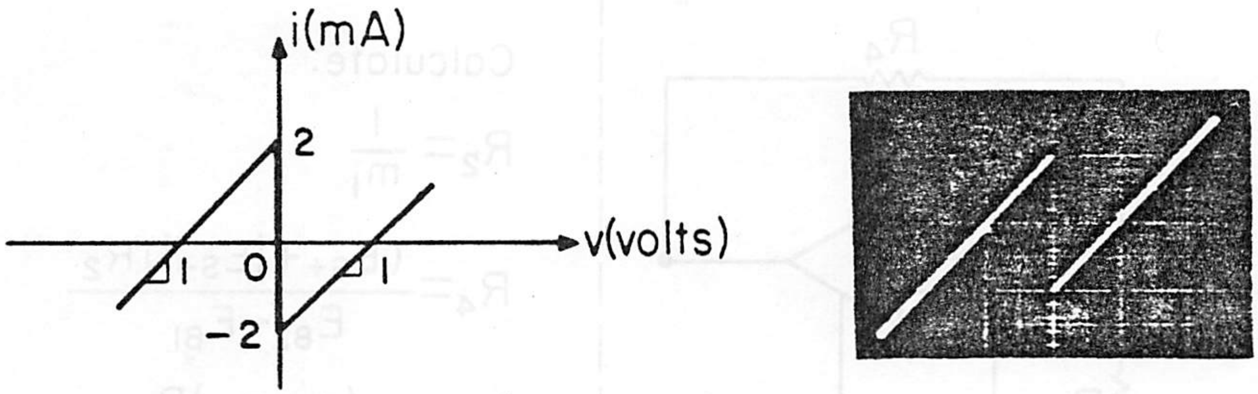
Fig. 24



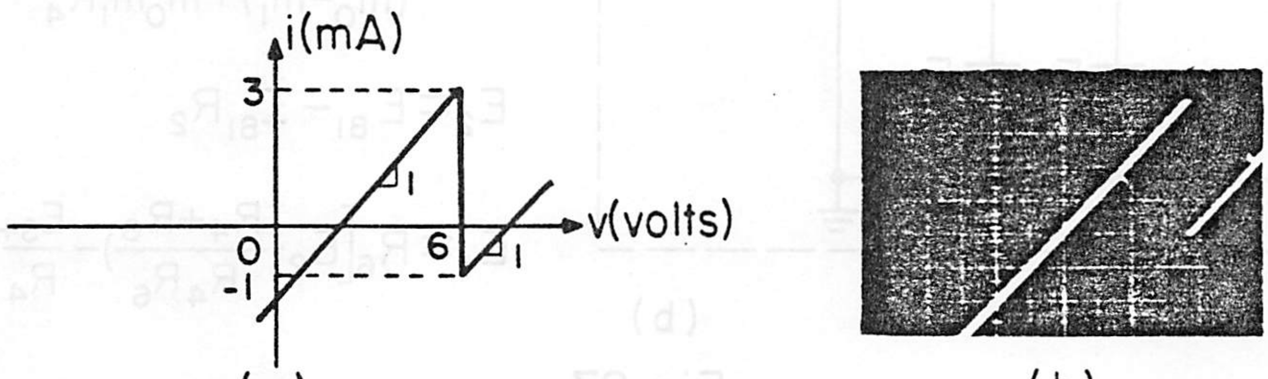

(a) Fig.22 (b)



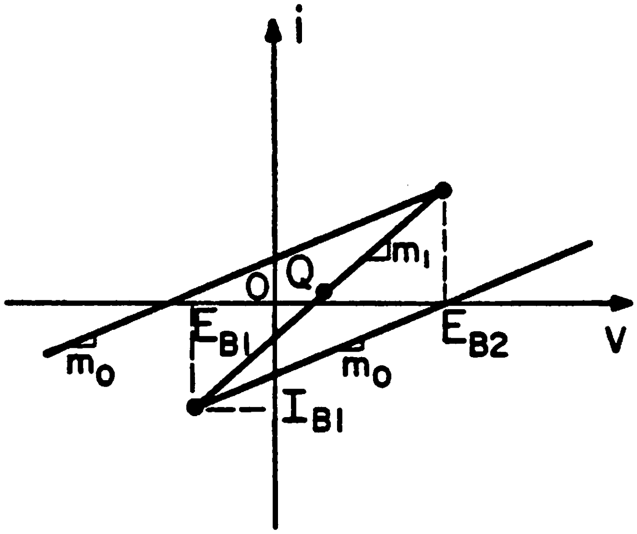

(a) Fig.23 (b)




(a) Fig.25 (b)




(a) Fig.26 (b)



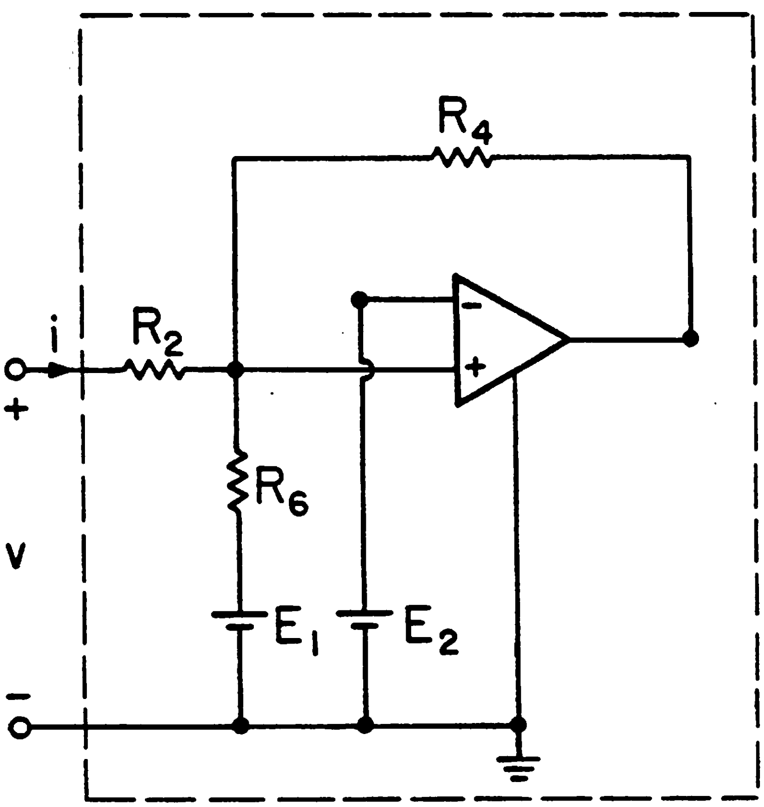

(a)

**Assumptions:**

$0 < m_0 < \infty$

$0 < m_1 < \infty$

$m_1 > m_0$




(b)

**Design Algorithm:**

Calculate:

$$R_2 = \frac{1}{m_1}$$

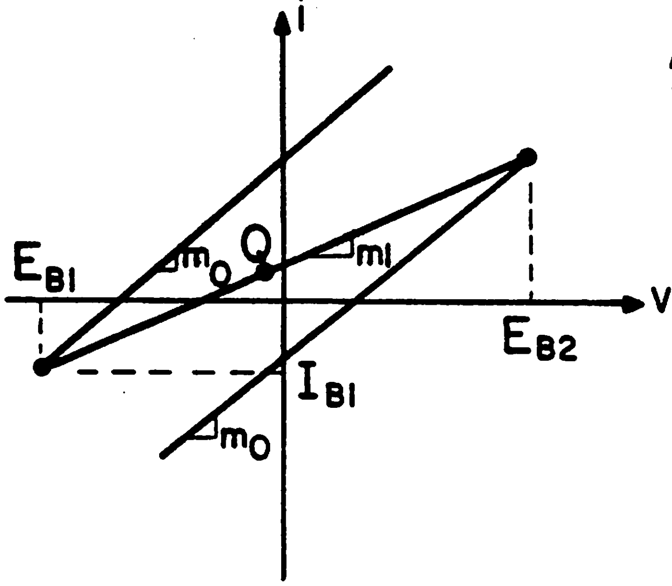
$$R_4 = \frac{(E_{S+} + |E_{S-}|)R_2}{E_{B2} - E_{B1}}$$

$$R_6 = \frac{(m_1 - m_0)R_4}{(m_0 - m_1) + m_0 m_1 R_4}$$

$$E_2 = E_{B1} - I_{B1}R_2$$

$$E_1 = R_6\left[E_2\left(\frac{R_4 + R_6}{R_4 R_6}\right) - \frac{E_{S+}}{R_4} - I_{B1}\right]$$

Fig. 27



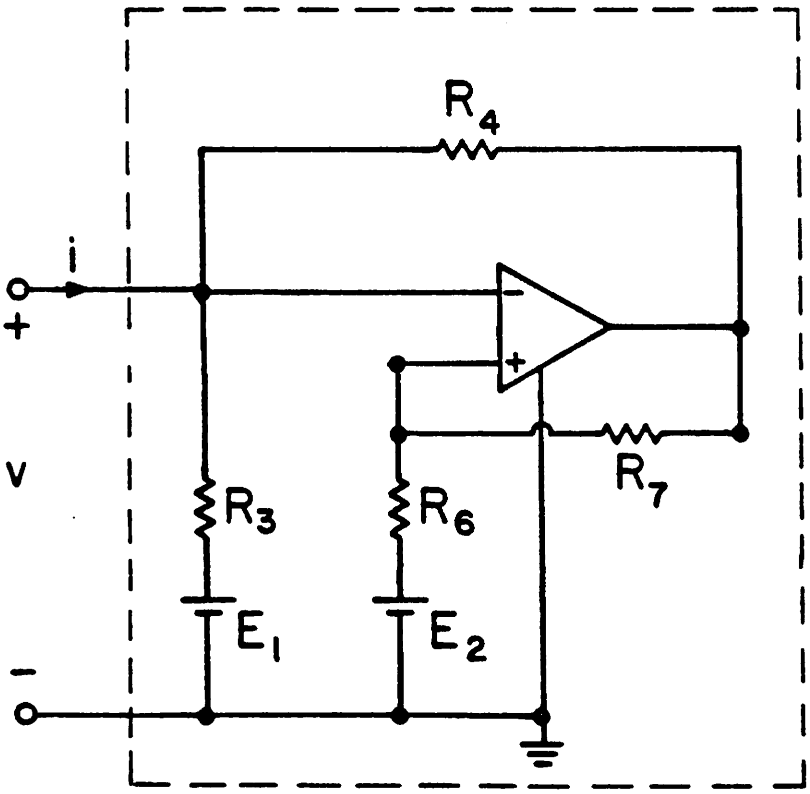

## Assumptions

$0 < m_0 < \infty$

$0 < m_1 < \infty$

$m_1 < m_0$

(a)




## Design Algorithm

Choose convenient value for $R_7 > 0$, calculate:

$$E_2 = \frac{E_{B1} E_{S+} + E_{B2} |E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_6 = \left[ \frac{E_2 - E_{B1}}{E_{B1} + |E_{S-}|} \right] R_7$$

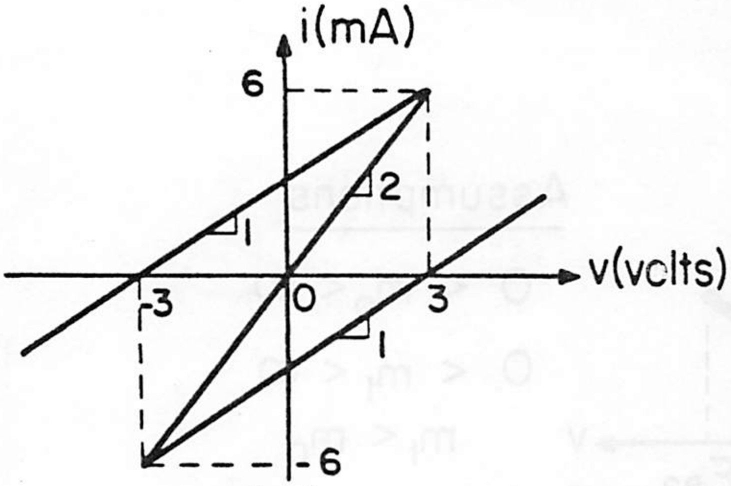
$$R_4 = \frac{R_6 + R_7}{(m_0 - m_1) R_6}$$

$$R_3 = \frac{R_4}{m_0 R_4 - 1}$$

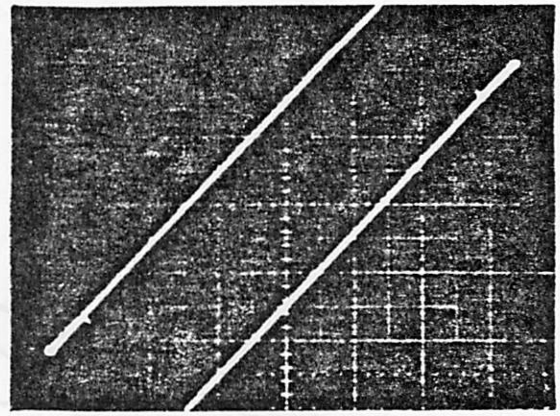
$$E_1 = R_3 \left[ m_0 E_{B1} + \frac{|E_{S-}|}{R_4} - I_{B1} \right]$$

(b)

Fig. 30

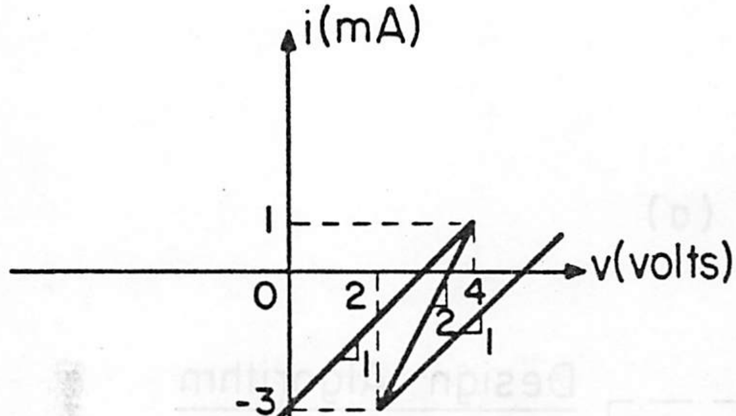



(a)

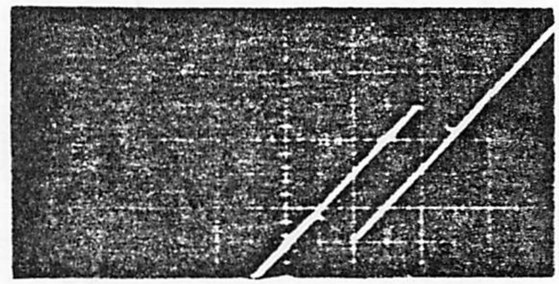


(b)

Fig. 28

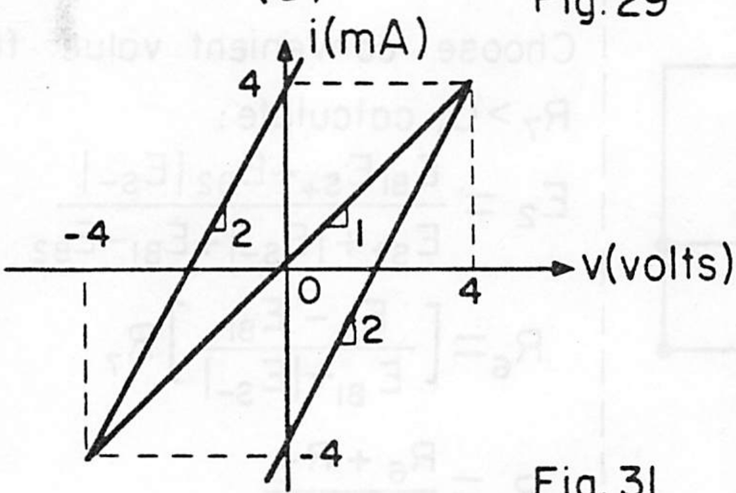



(a)

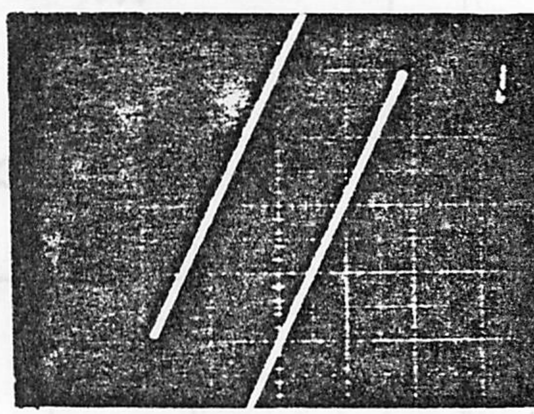


(b)

Fig. 29

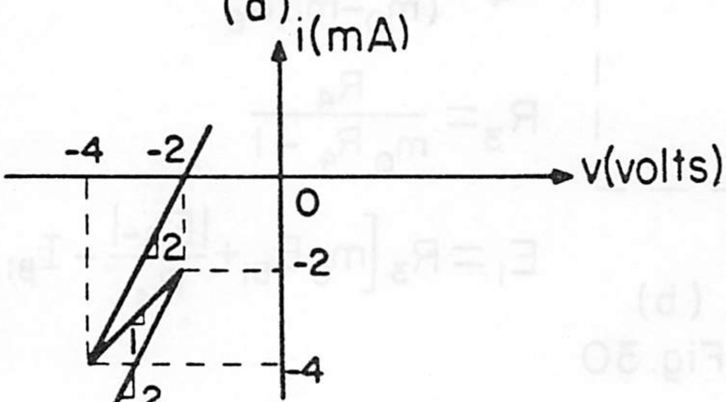



(a)

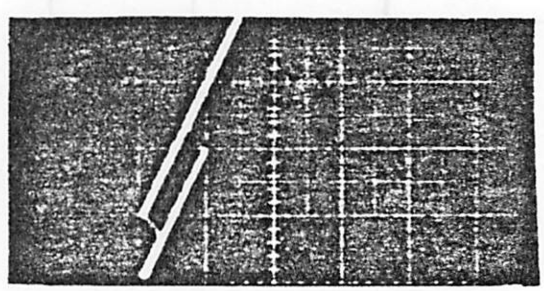


(b)

Fig. 31




(a)



(b)

Fig. 32

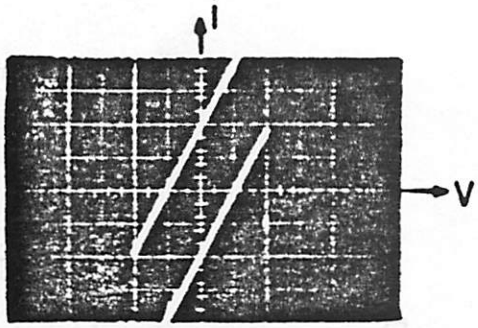


Fig.33

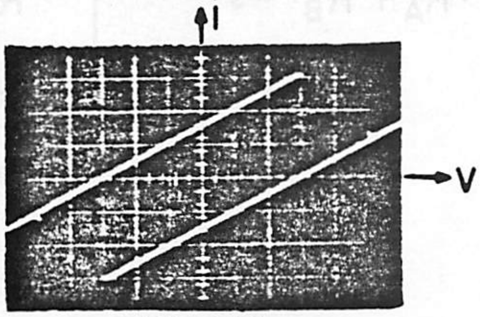


Fig.34

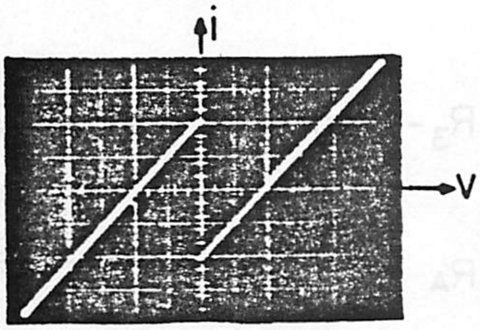


Fig.35

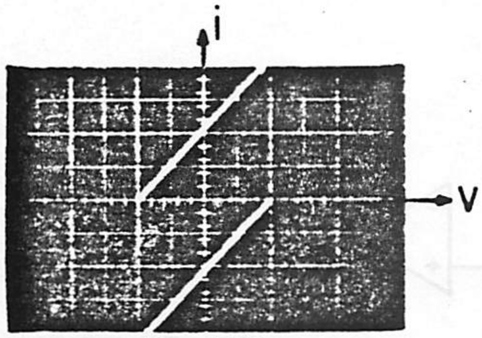


Fig.36

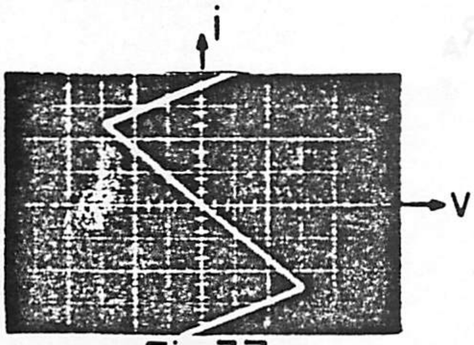


Fig.37

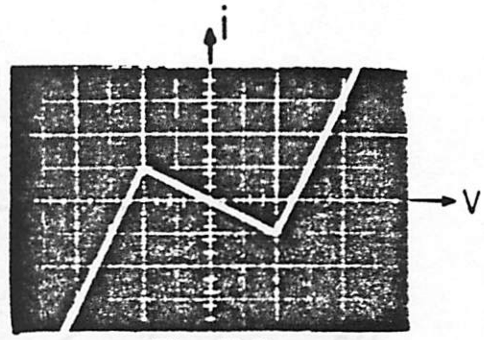


Fig.38

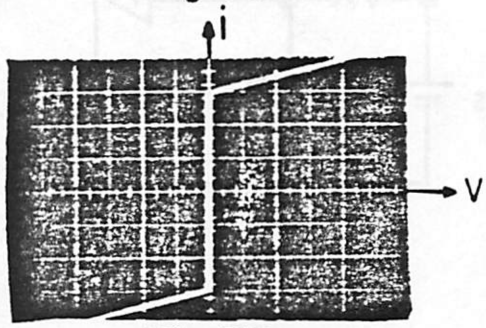


Fig.39

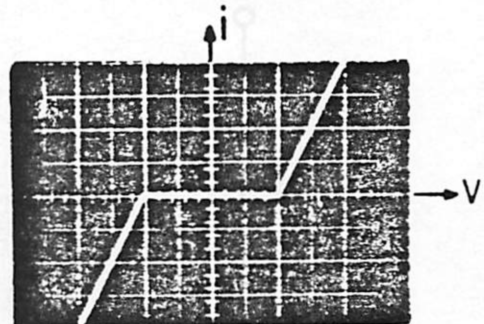


Fig.40

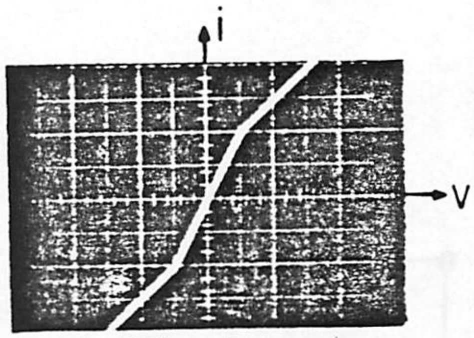


Fig.41

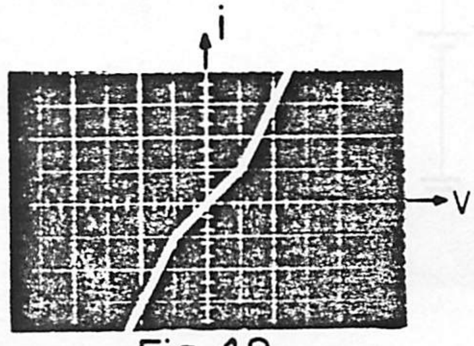


Fig.42

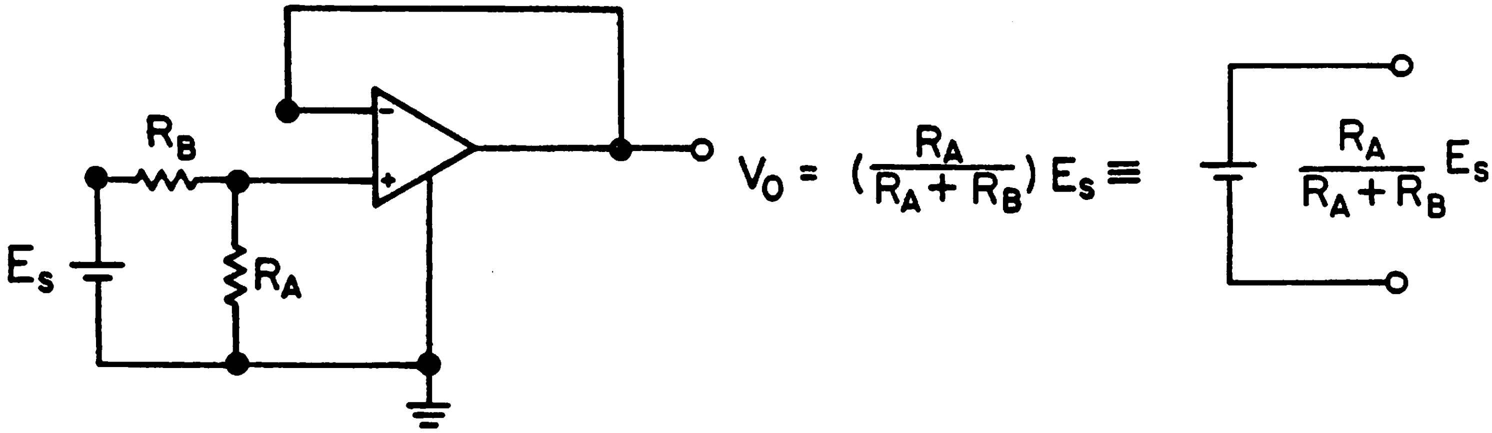



Fig. 43

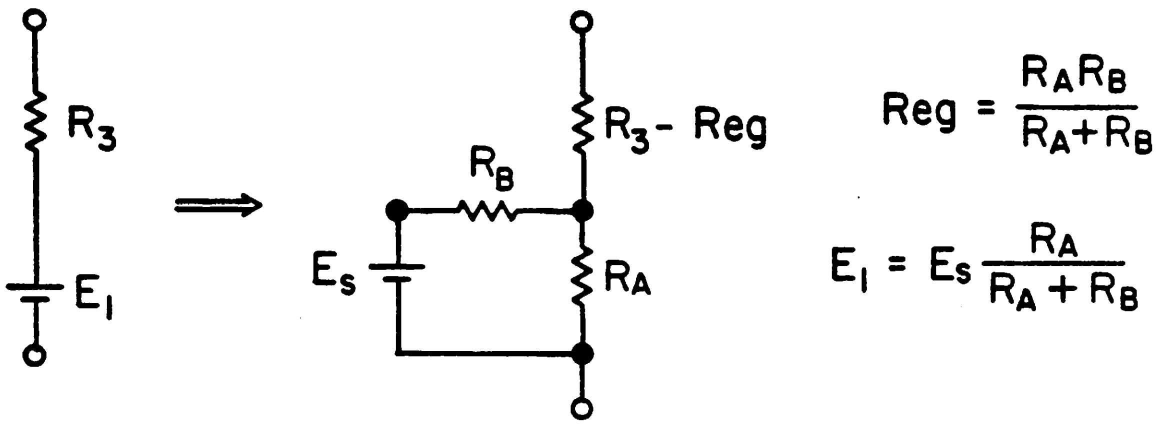



Fig. 44

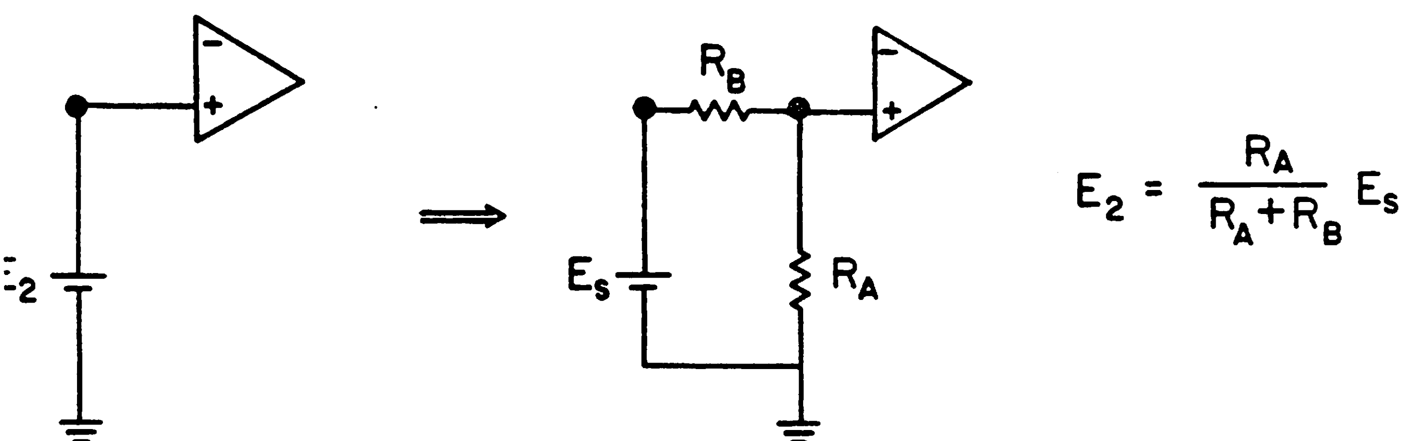
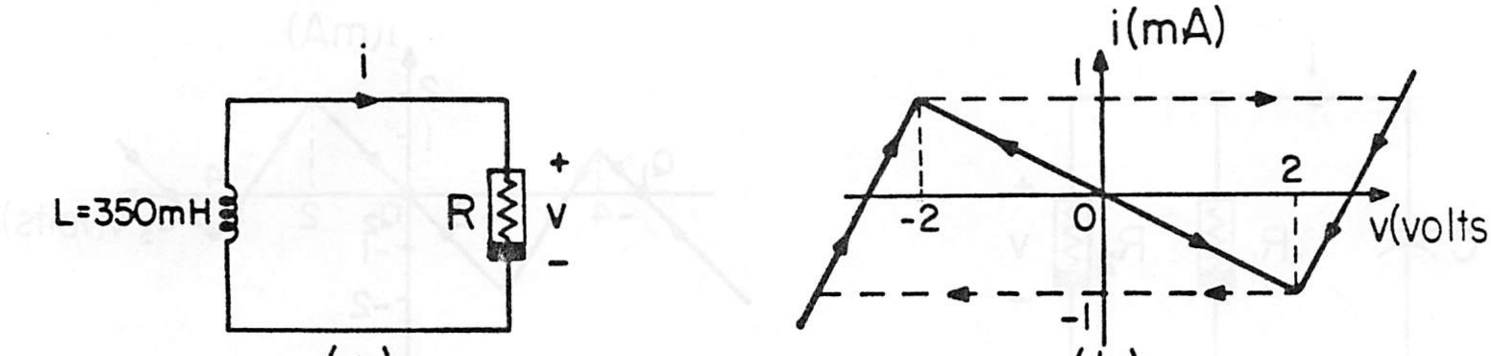
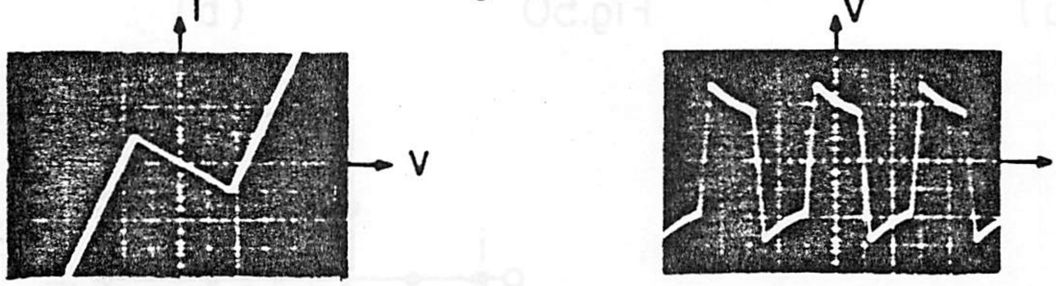



Fig. 45



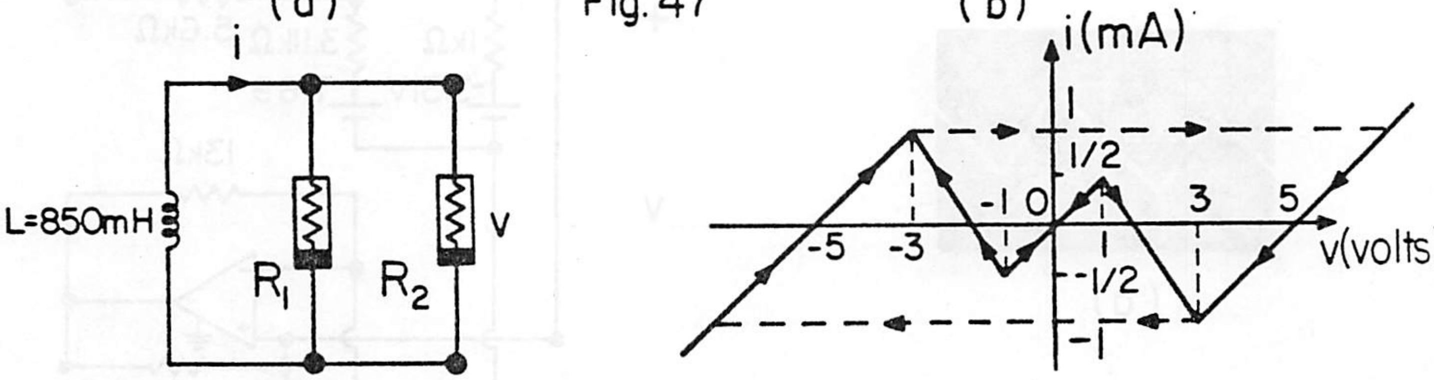

(a) (b)

Fig. 46




(a) (b)

Fig. 47




(a) (b)

Fig. 48

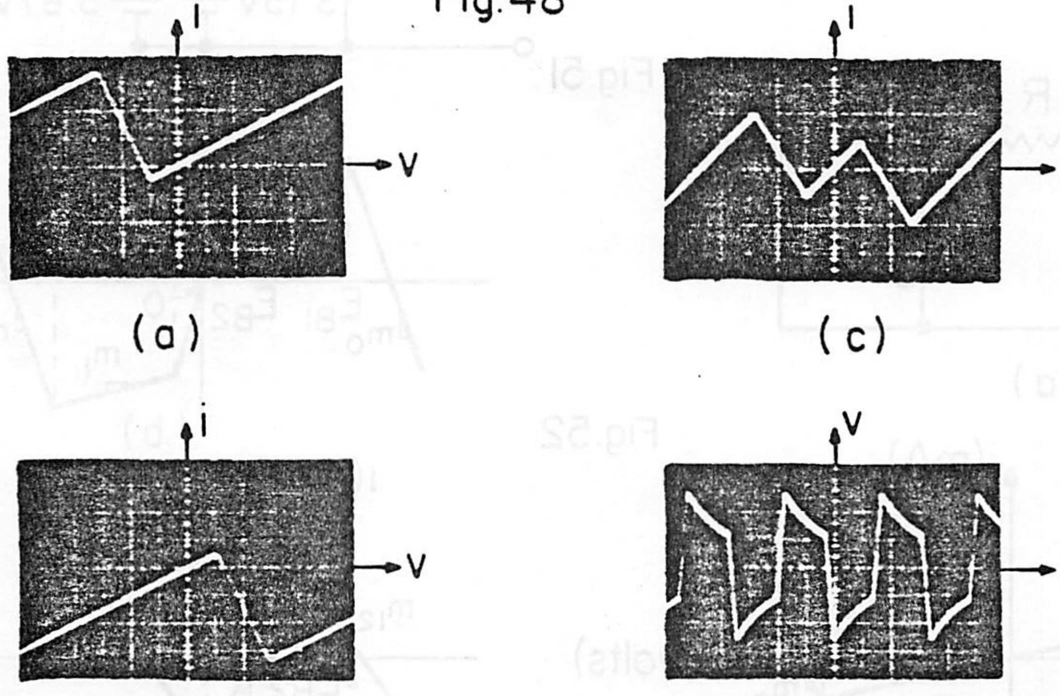
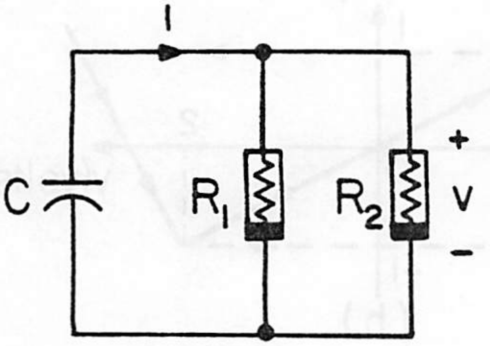
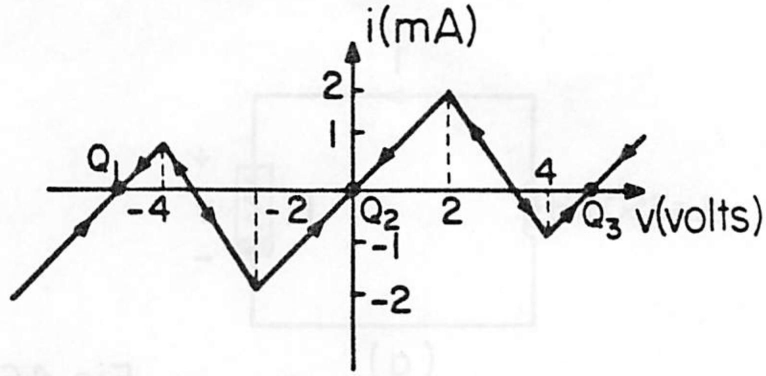



Fig. 49

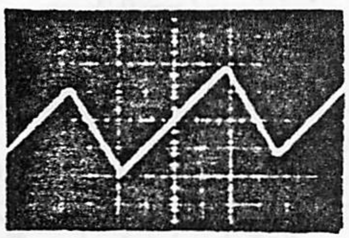



(a)

Fig.50




(b)



(a)

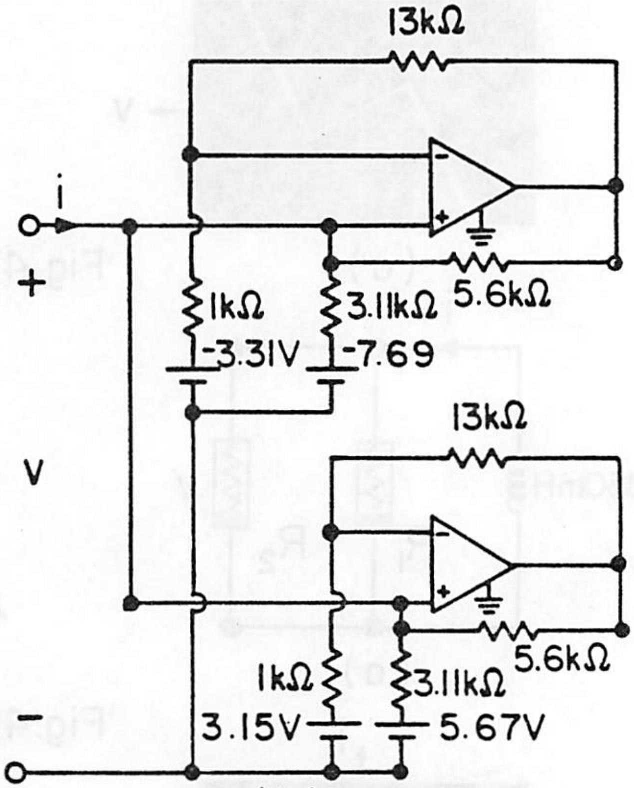
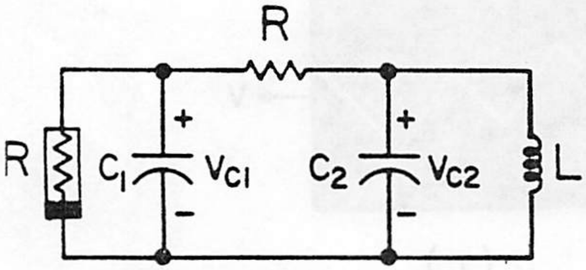


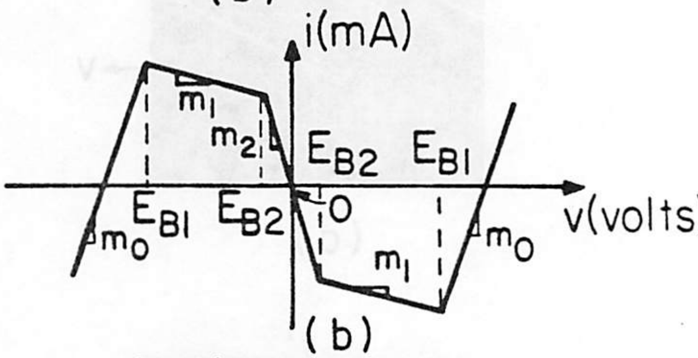

Fig.51

(b)

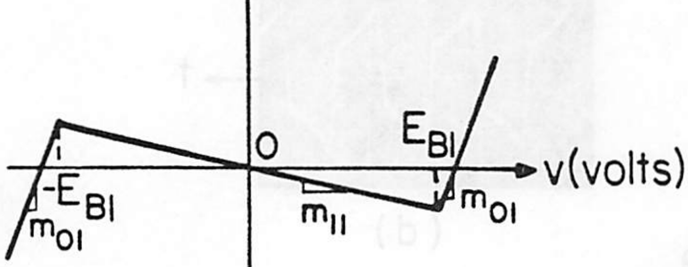



(a)

Fig.52

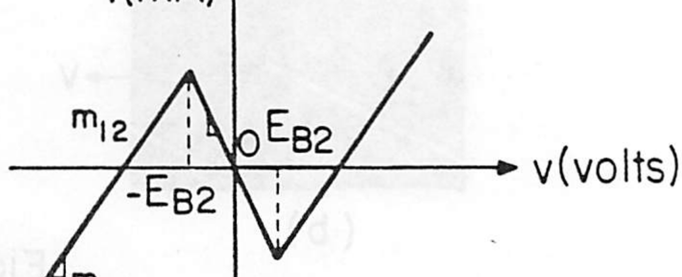



(b)




(a)

Fig. 53




(b)

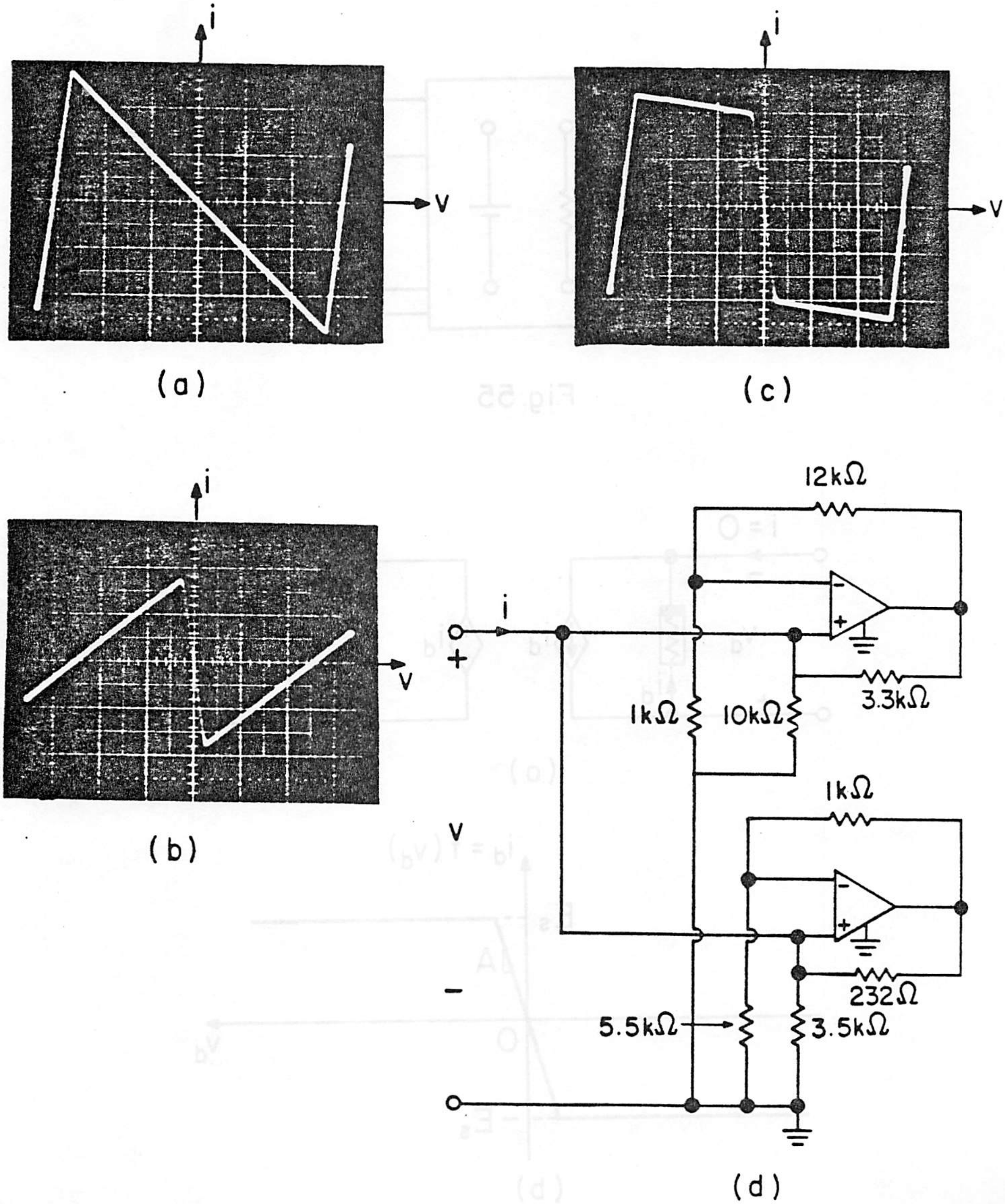



Fig. 54

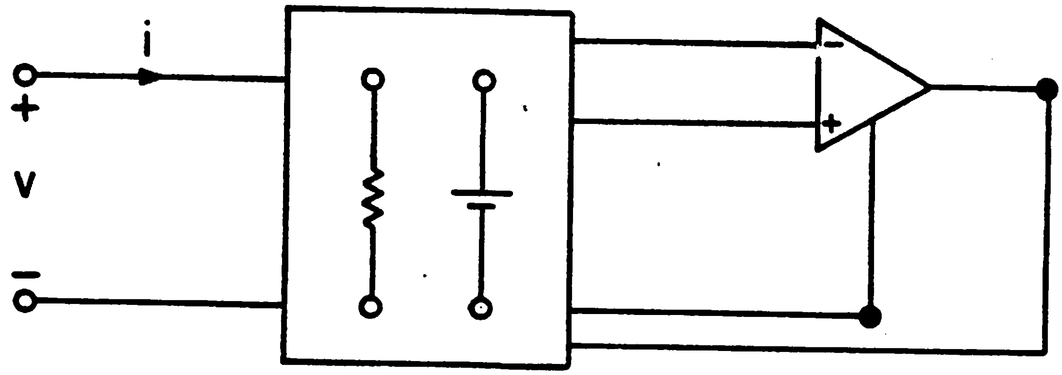



Fig. 55

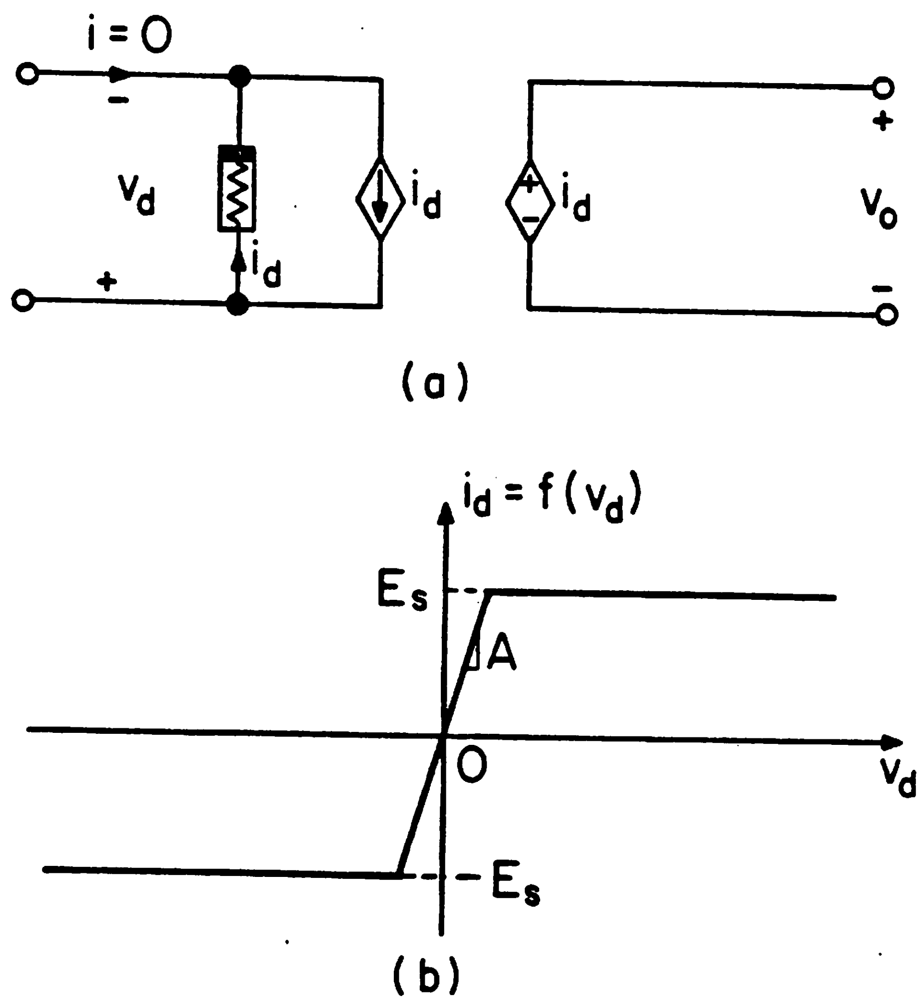



Fig. 56

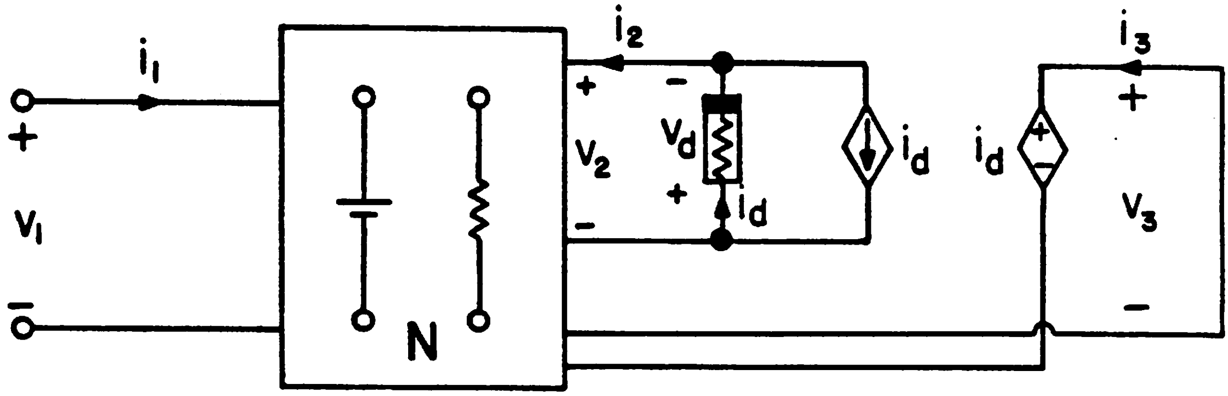



Fig. 57

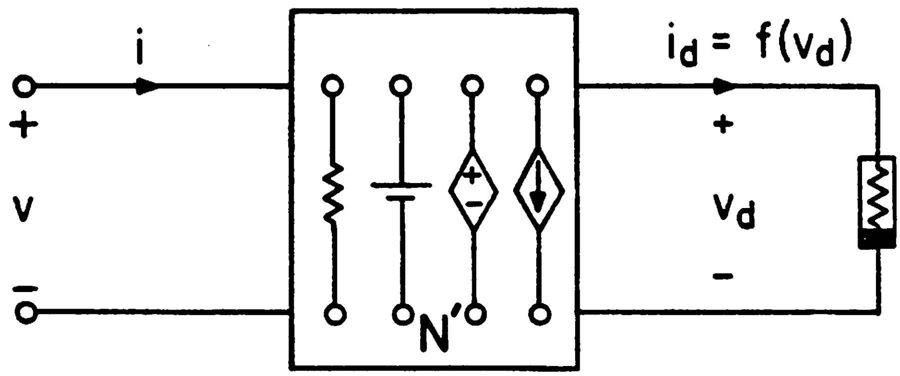



Fig. 58

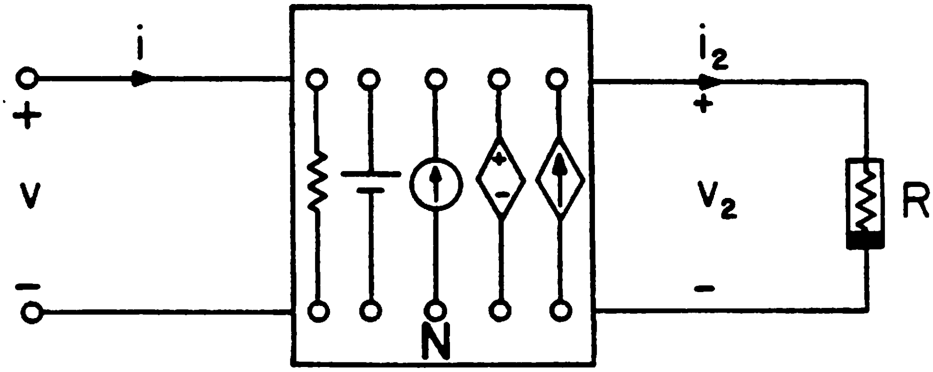



Fig. 59

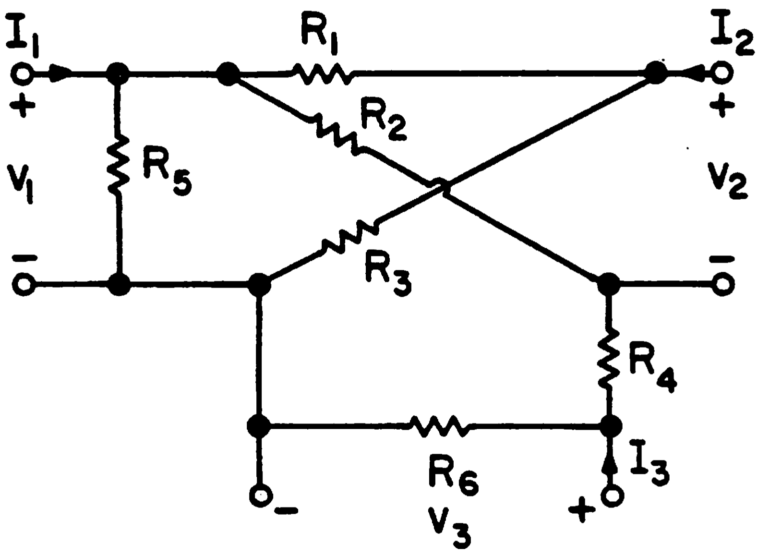


Fig. 60

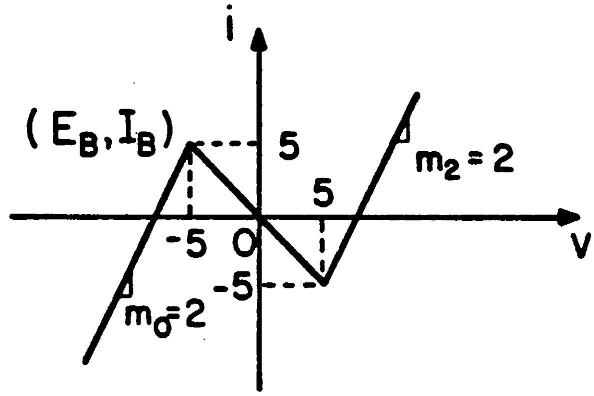


Fig. 61

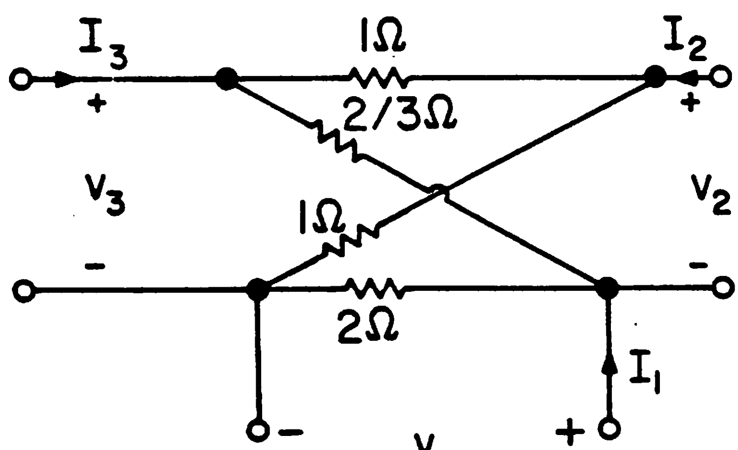


Fig. 62

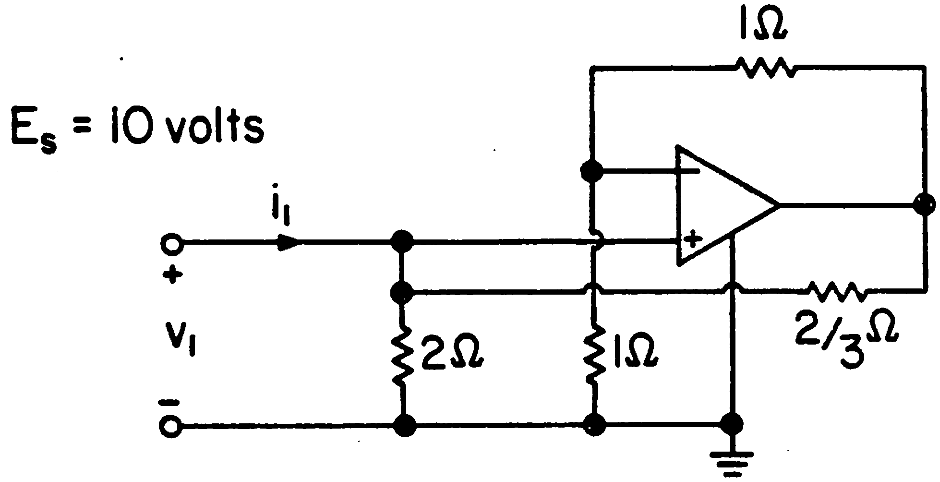



Fig. 63