PERFORMANCE LIMITATIONS IN SWITCHED-CAPACITOR FILTERS

by

Rinaldo Castello and Paul R. Gray

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1. INTRODUCTION

Despite their relatively short history, switched capacitor (S.C.) circuits are already fairly mature. Most of their specifications have improved substantially since the first monolithic S.C. filters using S.C. integrators were designed and fabricated in 1977 [1],[2].

In particular the power dissipation per pole has been reduced from about 10 to 20 mW in the first NMOS prototypes to less than 1 mW in the CMOS filters in production today [3]. These figures refer to general purpose systems working from a $\pm$ 5 Volts supply and with clock rates of 128 kHz or more. For special purpose applications, on the other hand, much smaller values have been achieved [4]-[7].

Another aspect that has been extensively investigated is the improvement of the dynamic range of the filter. To this end techniques like fully differential circuit design and noise frequency translation via chopper stabilization have been proposed. This has produced a filter with a dynamic range of 102 db [8]. To achieve such a result, however, a large increase in the chip area occupied by the filter was necessary.

Finally the total die area occupied by the filter has been substantially reduced. This has allowed the integration on a single chip of many S.C. filters together with other components [9]-[12].

Almost all of these results have been achieved by improving the performance of the operational amplifiers (op amps) in the filter [3], [13]-[15]. It is likely that better and better op. amps. will be designed in the future allowing this trend to continue. Eventually, however, some fundamental limitations other than those coming from the op. amps. will come into play. Such limitations cannot be overcome by circuit or process improvements; therefore they determine the ultimate performance limit of the filter. This paper analyzes these fundamental limitations with reference to low pass filters.

Section 2 focuses on the S.C. integrator which is the building block of most S.C. filters. Under certain assumptions, the minimum area and power requirements, and the maximum achievable dynamic range are obtained as a function of relatively few parameters that are

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

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Rinaldo Castello and Paul R. Gray

Department of Electrical Engineering and Computer Science
University of California, Berkeley
Berkeley, California 94720

Switched-Capacitor (S.C.) filters continue to improve in performance mainly through progress in the design of MOS operational-amplifiers (op amps). Ultimate limits to achievable filter performance, however, stem from factors more fundamental than op amp nonidealities, factors independent of process and circuit improvements. This paper develops, from certain basic assumptions, ultimate limits on dynamic range, chip area, and power consumption in S.C. integrators and low pass filters. For integrators, minimum area and power requirements are shown to vary as the square of desired dynamic range. Some physically realistic approximations lead to expressions relating filter area, power consumption, and dynamic range which involve only fundamental process parameters, supply voltage and filter cut-off frequency. Comparison with actual performance in typical commercially manufactured S.C. filters suggests that there is still a strong motivation in improving op amp specifications. A typical commercial 5^{th} order voiceband filter operating from a $\pm 5\ V$ supply with a dynamic range of 95 db consumes approximately 5 mW and requires an area of approximately 5000 mil^2 compared with the theoretical minima of 8.5 μW and 11.2 mil^2 respectively.

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Section 2 focuses on the S.C. integrator which is the building block of most S.C. filters. Under certain assumptions, the minimum area and power requirements, and the maximum achievable dynamic range are obtained as a function of relatively few parameters that are

dependent on both the technology and the circuit used. It is shown that both the minimum power and area requirement vary proportionally to the square of the achievable dynamic range.

Section 3 analyzes the performance limitations of a low-pass S.C. filter. The theory of section 2 is extended to any low-pass ladder structure without introducing further approximations. The obtained results, while intuitively interesting, are function of the particular filter under consideration and cannot be related to each other in a general way.

By introducing additional approximations, which in most practical cases cause only a small error, and normalizing the results to the order of the filter, several simple relationship are obtained. Logarithmic plots showing the dependence of the minimum area and power requirement versus the achievable dynamic range are also provided.

On the basis of such plots state-of-the-art filters can be compared with the theoretical minima. As an example, for a 5^{th} order voiceband filter with 95 db of dynamic range assuming a $\pm 5Volts$ supply the minimum area required is approximately $7300\mu m^2$ and the minimum power $8.5\mu W$. This is about two to three orders of magnitude smaller than the typical actual values for both power and area.

Finally in Section 4 the effect of the op amp non-idealities which were ignored in the derivation of the previous sections are considered. The op amp fundamental limitations are very difficult to exactly quantize and this is part of the reason why they were first ignored, nonetheless some upper bounds for the absolute minimum power, area, and noise can be obtained with reference to a particularly simple but relistic op amp configuration. This shows how the op amp limitations should not affect the ultimate filter performance in most practical cases.

2. PERFORMANCE LIMIT FOR THE IDEAL INTEGRATOR

In this section the S.C. integrator is analyzed to obtain limits for the minimum power consumption and chip area requirement and for the maximum dynamic range achievable

together with their interrelations. All of the following calculations refer to the so called differential bottom plate integrator shown in Fig.1. Such a circuit was chosen for sake of concreteness, since it is insensitive to parasitic capacitance and has been used extensively in the literature [3],[8],[16]. However the extension of the theory to other S.C. integrator configurations is very straightforward and yields similar results.

The following basic assumptions will be used throughout the paper.

1. The op. amp. in the integrator is assumed to be ideal in the sense that it does not contribute any noise to the filter, it does not use any D.C. power, and it occupies no chip area. The reason for such drastic assumptions is that there are no fundamental limits, identifiable a priori, for the minimum value that can be achieved, via process and/or circuit design improvements, for any of the op. amp. non idealities mentioned above.

The only potential exception to this comes from the op. amp. white noise. It has however been shown [17] that its contribution, when is not negligible, can be added to that of the $\frac{k\,T}{C}$ noise since both can be represented in the same way. In this paper the op amp white noise is neglected for the sake of simplicity; however, because of the above considerations, the following analysis can be easily extended to include it, if a specific op. amp. configuration is given. In section 4 the validity of these assumptions will be discussed in more detail.

2. The integrator capacitor is assumed to be much larger than the sampling capacitor i.e.

$$\frac{C_i}{C_s} \gg 1 \tag{2.1}$$

where C_s and C_i are the sampling and integration capacitors as shown in Fig.1. Making use of the following basic equation for the S.C. integrator [19]:

$$\frac{C_s}{C_i} = \frac{2\,\pi\, f_{unity}}{f_{clock}} \tag{2.2}$$

where f_{unity} is the unity gain frequency of the integrator and f_{clock} is the clock frequency, condition (2.1) becomes:

$$\frac{f_{clock}}{f_{unity}} \gg 2\pi \tag{2.3}$$

Assumption (2.3) is almost always valid if the integrator is part of a low-pass vioceband S.C. filter. In such a case, in fact, each integrator has a unity-gain frequency which is comparable in value with the band edge of the filter, while the clock frequency is typically many times larger than the filter band edge to avoid warping effects in the transformation from the z to the s domain [18] and to ease anti-aliasing requirements.

On the basis of the above assumptions, the absolute minimum integrator area is approximately equal to the area of C_i. Assuming to have a symmetrical power supply equal to $\pm V_s\ Volts$ and that the capacitor dielectric has a maximum electric field before break-down equal to E_{max} and a dielectric constant equal to ϵ_{diel}, the minimum thickness of the capacitor is:

$$t_{min} = 2\,\frac{V_s}{E_{max}} \tag{2.4}$$

The minimum area required to realize a capacitor of value C_i is therefore:

$$AREA_{min} = \frac{t_{min} C_i}{\epsilon_{diel}} = \frac{2\,V_s\,C_i}{E_{max}\,\epsilon_{diel}} \tag{2.5}$$

The maximum amount of energy that can be stored in the integrator ϵ_{max} is given by

$$\epsilon_{max} = \frac{1}{2}\,(2\,V_s)^2\,C_i = 2\,V_s^2\,C_i \tag{2.6}$$

Substituting Eq. 2.6 into Eq. 2.5 gives the minimum area as a function of the maximum stored energy:

$$AREA_{min} = \frac{\epsilon_{max}}{V_s\ E_{max}\,\epsilon_{diel}} \tag{2.7}$$

Next, the absolute minimum power consumption is computed. To this end the integrator of Fig. 1 can be represented as in Fig. 2. Furthermore the left hand side of the circuit of Fig. 2 can be modified as shown in Fig. 3. The only potential source of error in such a substitution is the phase difference existing between the two input of the integrator. Such a difference,

however, does not effect power dissipation. The two current sources I_1 and I_2 are used to model an ideal class B Op. Amp. To guarantee zero quiescent power dissipation, as it was assumed, I_1 must be equal to zero when $I_2 \neq 0$ and vice versa. The same is valid for I_1' and I_2'.

The total power dissipation is given by the amount of energy per unity of time drown from the supplies by the two portions of the circuit i.e.

1. The amount of energy that C_s draws from one supply and than damps into the amplifier virtual ground.

2. The amount of energy that C_I draws from the other supply, through the action of the Op. Amp., to be damped again into the virtual ground. Assuming that the input signal v_i is a pure sinusoid with frequency f and peak amplitude V_i, the energy dissipated during one period of the signal can be computed as in Appendix A and is equal to:

$$\epsilon_{cycle} = \frac{4}{\pi} V_i \; V_s \; C_s \; \frac{f_{clock}}{f} \tag{2.8}$$

The average power dissipated is obtained multiplying the energy per cycle by the frequency of the signal i.e.

$$P = \frac{4}{\pi} V_i \; V_s \; C_s \; f_{clock} \tag{2.9}$$

The input to output transfer function of the integrator is given by the following equation [19]

$$V_i = \frac{f}{f_{unity}} = \frac{2\pi f \; C_i}{f_{clock} \; C_s} V_o \tag{2.10}$$

From Eq. 2.10 it can be seen that for a in-band signal, i.e. $f \leq f_{unity}$, the maximum amplitude of the input signal that does not cause any clipping at the output is a function of the input frequency. For this reason it is convenient to express the power consumption as a function of the output signal. This can be done by substituting Eq. 2.10 into Eq. 2.9 obtaining

$$P = 8 V_s V_o f C_i \tag{2.11}$$

For a maximum amplitude sinusoid at the output, i.e. $V_o = V_s$ the power dissipation becomes

$$P = 8 f C_i V_s^2 \tag{2.12}$$

Using Eq. 2.6 into Eq. 2.12 gives

$$P = 4 \epsilon_{max} f \tag{2.13}$$

the minimum power consumption for a full swing sinusoidal output is therefore proportional to the maximum energy stored in the integrator times the frequency of the signal.

Last, the dynamic range is considered. While the power consumption and the area requirement can be uniquely defined for a stand-alone S.C. integrator, the dynamic range is a function of the particular circuitry that surrounds it. In any practical case the integrator must be part of a feedback loop in order to guarantee a stable DC operating point. This is shown schematically in fig. 4 together with the input-to-output transfer function with and without feedback. Both the total output noise, and the dynamic range, must be expressed as a function of the particular feedback configuration.

Having assumed an ideal op. amp., the only sources of noise are the MOS switches. The noise contributed by the left hand side switch is sampled by C_s every clock cycle. The signal appearing across capacitor C_s is therefore a sampled first order low-pass filtered white noise. It has been shown that for a properly operating S. C. circuit, i.e. the time constants associated with the switches and the capacitors are much smaller than the clock period, such a discrete random process has a white spectral distribution and a total noise power (variance) equal to $\frac{k T}{C_s}$[24]. Discrete time linear system theory can therefore be used to determine the output noise variance n_i^2 obtaining the following result [22]

$$n_i^2 = \frac{kT}{C_s} \sum_{m=0}^{\infty} h^2(m) \tag{2.14}$$

where $h(m)$ is the impulse response from the noise source to the output. Using Parseval's theorem [22] in Eq. (2.14) gives the final result

$$n_i^2 = \frac{kT}{C_s} \frac{1}{2\pi} \int_{-\pi}^{\pi} H\ (e^{j\omega})\, H\ (e^{-j\omega})\, d\omega \tag{2.15}$$

where $H\ (e^{j\omega})$ is the z transform of $h\ (m\ )$ evaluated on the unit circle. By introducing the the following definition

$$B_o = \frac{f_{clock}}{2\pi} \int_{-\pi}^{\pi} H\ (e^{j\omega})\, H\ (e^{-j\omega})\, d\omega \tag{2.16}$$

and making use of Eq. (2.2), Eq. (2.15) can be written as

$$n_i^2 = \frac{1}{2\pi} \frac{kT}{C_i} \frac{B_o}{f_{unity}} \tag{2.16b}$$

The quantity B_o is the effective noise bandwidth from the input of the switched capacitor integrator to the integrator output for the particular feedback configuration considered. It is the integral of the magnitude squared of the frequency response of the sampled data feedback circuit from the integrator input to the output, taken around the unit circle. For lowpass filters where the clock rate is far above the passband, this is equivalent to the integral over the passband of the transfer function from the integrator input to the output for the continuous equivalent circuit. In the following B_o will be called the noise bandwidth to the output.

The noise contributed by the right hand side switch is also sampled by C_s. However, in this case, the resulting signal cannot rigorously be considered as a first order low pass filtered noise. The reason is that the circuit through which the white noise of the switch is sampled does not have a single pole roll-off since it contains also the op. amp. The amount of noise transferred to the output is, to first order, proportional to the ratio between the op. amp. unity gain bandwidth and the bandwidth of the circuit formed by the switch resistance and the sampling capacitor[23]. For simplicity it is assumed to have an ideal op. amp. (infinite bandwidth). In such case the two switches behave in the same way and the total output noise, n^2, becomes

$$n^2 = \frac{1}{\pi} \frac{kT}{C_i} \frac{B_o}{f_{unity}} \tag{2.17}$$

Assuming that the maximum undistorted output signal is approximately equal to the supply voltage V_s, i.e. $2\sqrt{2}V_s$ rms, the dynamic range of the integrator,(DR), becomes:

$$(DR)^2 = \frac{s^2}{n^2} = \frac{\pi}{2}\frac{V_s^2 C_i}{kT}\frac{f_{unity}}{B_o} \tag{2.18}$$

Eq. (2.18) can be rewritten as follows by making use of Eq.(2.6)

$$(DR)^2 = \frac{\pi}{4}\frac{\epsilon_{max}}{kT}\frac{f_{unity}}{B_o} \tag{2.19}$$

Eq. (2.19) suggests that the square of the dynamic range is given by the ratio between the maximum energy stored in the integrator and the unity of thermal energy kT, modified by the ratio between the noise bandwidth to the output and the unity gain bandwidth of the integrator.

As an example consider the unity gain feedback circuit shown in Fig. 5. This is the simplest configuration in which the S.C. integrator can be operated. It corresponds to a first order low pass filter whose z domain transfer function from C_s to the output is given by

$$H(z) = \frac{\frac{C_s}{C_i}}{1 - z^{-1} + \frac{C_s}{C_i}} \tag{2.20}$$

$H(e^{j\omega T})$ is approximately shown in Fig. 5b. In this simple case B_o can be easily computed by making use of Cauchy residue theorem with the following result

$$B_o = f_{clock}\frac{C_s}{C_s + 2C_i} \tag{2.21}$$

Assuming condition (2.1) to be valid and using Eq. (2.2) in Eq. (2.21) gives the following result

$$B_o = \frac{f_{clock}}{2}\frac{C_s}{C_i} = \pi f_{unity} \tag{2.22}$$

As expected, for this simple case, B_o is just the effective noise bandwidth of the single-time constant low-pass filter whose transfer function is shown in Fig. 5. Using the above result

the circuit dynamic range becomes.

$$(DR)^2 = \frac{V_s^2 C_i}{2 kT} \tag{2.23}$$

which is a particularly simple result. Note that this ratio is simply the maximum energy stored on the integrating capacitor divided by kT. This result has strong implications for the ultimate limit on the ability to scale switched capacitor filters with technological feature size. In effect, silicon dioxide can only store a certain amount of energy per unit volume as dictated by the maximum field strength of silicon. For a given oxide thickness and power supply voltage this dictates a maximum energy storage per unit area, which dictates a minimum area for a given dynamic range and power supply voltage. Such a minimum value can be computed in the more general case by combining Eq. (2.19) and Eq. (2.7) with the following result

$$(DR)^2 = \frac{\pi}{4} \frac{V_s \epsilon_{diel} E_{max} AREA}{kT} \frac{f_{unity}}{B_o} \tag{2.24}$$

This indicates that the ultimately achievable dynamic range is proportional to the square root of the product of the power supply voltage and the area.

Since the absolute minimum achievable level of power dissipation is proportional to ϵ_{max}, as it was shown in Eq. (2.13), a relationship similar to Eq. (2.24) between dynamic range and power consumption must exist. Mathematically such a relationship can be obtained by combining Eq. (2.13) and Eq. (2.19) to obtain te following result

$$(DR)^2 = \frac{\pi}{16} \frac{P}{kT B_o} \frac{f_{unity}}{f} \tag{2.25}$$

Thus the dynamic range is proportional to the square root of the minimum power dissipation necessary to charge and discharge the sampling and integrating capacitors from the power supply.

Notice that Eq. (2.25) is only valid for $f \leq f_{unity}$ since outside this range the gain of the integrator is less than 1 and therefore it is not possible to have $V_o = V_s$ for an input signal v_i smaller than the supply voltage. It is easy to see that the absolute maximum for P (

P_{max}), when both V_i and V_o are not allowed to exceed the supply voltage, corresponds to $f = f_{unity}$. In this case Eq. (2.24) becomes

$$(DR)^2 = \frac{\pi}{16} \frac{P_{max}}{kT\ B_o} \tag{2.26}$$

It can be shown that Eqs. (2.24)-(2.26) are valid for both single ended and fully differential integrators[17].

3. APPLICATION OF THE THEORY TO A LOW PASS S. C. FILTER

In this Section the previous analysis is extended to the case of low-pass ladder S. C. filters.

It is known that for a ladder active filter the basic building block is the integrator which, if the filter is implemented via S. C. techniques, can be realized by the circuit of Fig. 1 or by some other similar structure.

To apply the results of the previous section to te entire filter, it is first shown that there is a-one to-one correspondence between the order of the filter (number of poles) and the number of integrators required to realize it. This is easily done with the help of a simple example.

Fig. 6 shows the passive ladder prototype for a 3^{rd} order low-pass filter. This circuit can be represented in terms of integrator summers and multiplyers as in Fig. 7 [20]. The flow diagram of Fig. 7 shows that each integrator output corresponds to one of the state variables of the filter, i.e. a voltage across a capacitor or a current through an inductor. Therefore the number of integrators will be equal to the number of state variables, which also coincides with the order of the filter.

The above situation can be immediately generalized to an n^{th} order structure as long as the number of state variables coincides with the number of reactive elements. Even when this is not the case (due to the presence of loops of capacitors or cut-sets of inductors), however, it is still possible to modify the passive prototype so that the number of integrators will

coincide with the order of the filter by introducing some voltage-controlled voltage sources in the circuit [19]. In a S.C. implementation such controlled generators can be realized by simply substituting the basic integrator of Fig. 1 with the integrator-summer of Fig. 8 [19]. All the results of Section 2 can be extended with no changes to the structure of Fig. 8 if the extra area due to capacitor C_3 is neglected.

From the above considerations and from the results of Section 2 follows immediately that the minimum amount of area required for a n^{th} order S.C. filter is:

$$AREA_{tot} = 2 \frac{V_s}{E_{\max} \epsilon_{diel}} \sum_{i=1}^{n} C_i = \frac{\sum_{i=1}^{n} \epsilon_{\max_i}}{V_s E_{\max} \epsilon_{diel}} \tag{3.1}$$

Where $\epsilon_{\max_i}$ is the maximum amount of energy that can be stored in the i^{th} integrator.

To compute the total power dissipated in the filter for a sinusoidal input of frequency f and peak amplitude equal to the supply voltage V_s, use can be made of Eq. (2.11) provided that the gain from the input of the filter to the output of the i^{th} integrators, $G_i(f)$, is known for each integrator. This gives:

$$P_{tot} = 8 f V_s^2 \sum_{i=1}^{n} G_i(f) C_i = 4 f \sum_{i=1}^{n} G_i(f) \epsilon_{\max_i} \tag{3.2}$$

where f_i^{unity} is the unity gain frequency if the i^{th} integrator. Notice that in Eq. (3.2) it is implicitly assumed that $G_i(f) \leq 1$ for every i. This condition must be verified to be able to process a full swing (supply to supply) input signal without unacceptably large distortion. Such an assumption will be discussed further later in the paper.

Finally the total output noise contribution can be computed from Eq. (2.17) provided that the value of the noise bandwidth from the input of integrator i to the output of the filter, B_i, is known for all the n integrators.

$$n_{tot}^2 = \frac{1}{\pi} kT \sum_{i=1}^{n} \frac{B_i}{f_i^{unity} C_i} \tag{3.3}$$

This gives for the filter dynamic range

$$(DR_{tot})^2 = \frac{\pi V_s^2}{2kT \sum_{i=1}^{n} \frac{B_i}{f_i^{unity} C_i}} = \frac{\frac{\pi}{4}}{\sum_{i=1}^{n} \frac{kT}{\epsilon_{max_i}} \frac{B_i}{f_i^{unity}}} \tag{3.6}$$

where the in-band input-to-output gain of the filter has been assumed to be equal to one and the maximum output swing to be equal to the supply voltage(° ~~2~~V_s rms).

This is generally true in a S. C. low-pass filter since the 6 db in-band loss of the passive prototype can be easily eliminated by making the capacitor that samples the input voltage twice as big as the other sampling capacitor in the first integrator.

An alternative way to express the dynamic range in term of the sampling capacitors which will be useful later is shown in Eq. (3.5)

$$(DR_{tot})^2 = \frac{V_s^2 f_{clock}}{4kT \sum_{i=1}^{n} \frac{B_i}{C_{s_i}}} \tag{3.5}$$

where C_{s_i} is the sampling capacitor in the i^{th} integrator.

The above equations involve almost no approximations and can be used if all of the required parameters are known. The results, however, are a function of the particular filter design adopted and are in a form that does not show any particular relationship between the various performances. More insight on the problem can be gained by introducing some approximations.

First, it is assumed that the sampling capacitors are identical for all the integrators, with the exception of the one that samples the input voltage, which was assumed to be twice as big as the others.

Next the following approximation is introduced:

$$\sum_{i=1}^{n} \frac{1}{f_i^{unity}} \approx \frac{n}{f_{max}} \tag{3.6}$$

where f_{max} is the band edge of the filter. Physically this means that the average value of the time constants of all the integrators in the filter coincide with the time constant associated

with the band edge of the filter. In a typical low-pass ladder filter the error introduced by Eq. (3.6) rarely exceed $\pm 30\%$.

Table 1, for example, shows the values of the integrators unity gain frequency together with f_{max} for a commercial PCM low-pass filter (INTEL 2912). In this case the approximation introduces only about 2% error.

From Eqs. (3.1), (2.2), and (3.6) it follows that:

$$AREA_{tot} = \frac{2 V_s \, n}{E_{max} \epsilon_{diel}} \frac{f_{clock} \, C_s}{2 \pi f_{max}} = \frac{2 V_s \, n}{E_{max} \epsilon_{diel}} C_I = \frac{n \, \epsilon^I_{max}}{E_{max} \epsilon_{diel} \, V_s} \tag{3.7}$$

where the following two definitions have been introduced

$$C_I = \frac{f_{clock} \, C_s}{2 \pi f_{max}} \tag{3.8}$$

$$\epsilon^I_{max} = 2 V_s^2 \, C_I \tag{3.9}$$

From Eq. (2.2) C_I can be interpreted as the integration capacitance necessary to obtain an integrator whose unity gain frequency is f_{max}. ϵ^I_{max} is the maximum amount of energy that can be stored in C_I.

In order to obtain a single numerical value for the power dissipated in the filter Eq. (3.2) is evaluated for $f = f_{max}$; therefore obtaining an upper bound for the minimum power requirement. At that frequency, for a properly designed filter, the gain from the input to each intermediate node can be assumed, with good approximation, to be equal to 1 i.e. $G_i (f_{max}) = 1$ for $i = 1 \cdots n$ [20].

To understand why this is in most cases a good approximation notice that to avoid saturation, which will reduce the maximum usable amplitude of the input signal, the gain from the input to each internal node must be less or equal to one for all frequency. On the other hand the value of the gain from all the intermediate nodes to the output should be minimum, to minimize the total output noise contribution. A good compromise between these two requirements is to set the peak value of each intermediate gain to one. Since peaking typically occurs in the proximity of the band edge the above assumption is justified.

Eq. (3.6) can be substituted in Eq. (3.2) to give:

$$P_{tot}\ (f_{\max}) = 8\,n\ V_s^2\ f_{\max} C_I = 4\,n\ \epsilon^I_{\max}\ f_{\max} \tag{3.10}$$

The total output noise is obtained by using Eq. (3.5), with the condition that all the sampling capacitors are equal:

$$n_{tot}^2 = \frac{4\,kT}{C_s\ f_{clock}} \sum_{i=1}^{n} B_i = \frac{2}{\pi} \frac{kT}{C_I\ f_{\max}} \sum_{i=1}^{n} B_i \tag{3.11}$$

this implies a dynamic range for the filter (DR_{tot}) of:

$$(DR_{tot})^2 = \frac{\pi V_s^2 C_I\ f_{\max}}{2\,kT \sum_{i=1}^{n} B_i} = \frac{\pi}{4} \frac{\epsilon^I_{\max}}{kT} \frac{f_{\max}}{\sum_{i=1}^{n} B_i} \tag{3.12}$$

Eqs. (3.7), (3.10), and (3.12) can be normalized to obtain the equivalent area, power, and dynamic range per pole as follows:

$$AREA_{pole} = \frac{AREA_{tot}}{n} = \frac{\epsilon^I_{\max}}{E_{\max}\,\epsilon_{diel}\,V_s} \tag{3.13}$$

$$P_{pole} = \frac{P_{tot}}{n} = 4\,\epsilon^I_{\max}\ f_{\max} \tag{3.14}$$

$$(DR_{pole})^2 = n\ (DR_{tot})^2 = \frac{\pi}{4} \frac{\epsilon^I_{\max}}{kT} \frac{f_{\max}}{\frac{1}{n} \sum_{i=1}^{n} B_i} \tag{3.15}$$

Eqs. (3.13), (3.14), and (3.15) can be related to each other in the same way as it was done for Eqs. (2.7), (2.13), and (2.19) to obtain:

$$(DR_{pole})^2 = \frac{\pi}{16} \frac{P_{pole}}{kT \frac{1}{n} \sum_{i=1}^{n} B_i} \tag{3.16}$$

$$(DR_{pole})^2 = \frac{\pi}{4} \frac{V_s\,\epsilon_{diel}\,E_{\max}\,AREA_{pole}}{kT} \frac{f_{\max}}{\frac{1}{n} \sum_{i=1}^{n} B_i} \tag{3.17}$$

Comparing Eqs. (3.16) and (3.17) with Eqs. (2.24) and (2.25) it can be seen that they have the same physical interpretation with $f_{\max}$ and $\frac{1}{n} \sum_{i=1}^{n} B_i$ playing the role of f_{unity} and B_o

respectively.

In Eq. (3.16) and (3.17) $\frac{1}{n}\sum_{i=1}^{n} B_i$ is the only term that depends on the particular circuit architecture used. It turns out, however, that in practical cases its value is relatively constant. In fact the following approximation can be introduced

$$\frac{1}{n}\sum_{i=1}^{n} B_i = \delta\, 2\, f_{\max} \tag{3.18}$$

where δ is a parameter that depends on the particular filter implementation whose average value is can be assumed to be equal to .75 with a worst case inaccuracy of about ±40%. For the filter of Table 1, for instance, δ is equal to .9.

Using (3.18) with $\delta = .75$ in (3.16) and (3.17) gives:

$$(DR_{pole})^2 = \frac{\pi}{24}\,\frac{P_{pole}}{kT\, f_{\max}} \tag{3.19}$$

$$(DR_{pole})^2 = \frac{\pi}{6}\,\frac{V_s\, \epsilon_{diel}\, E_{\max}\, AREA_{pole}}{kT} \tag{3.20}$$

From Eqs. (3.19) and (3.20) the logarithm of P_{pole} and A_{pole} can be plotted versus the achievable dynamic range, DR_{pole}, expressed in db with $f_{\max}$ or V_s used as a parameter respectively. This is shown in Fig. 9 and 10 in the case that the capacitor dielectric is silicon dioxide with $E_{\max} = 5\ 10^6 \frac{V}{cm}$.

The plots of Figs. 9 and 10 can be used for both single ended and fully differential filter configurations.

On the base of the above results the power consumed and the area occupied by any low pass S.C. filter can easily be compared with the theoretical minima.

As an example consider a PCM 5^{th} order low-pass elliptic filter with a cut-off frequency of 3.4 kHz, a supply voltage of $\pm 5\ Volts$ and a signal-to-noise ratio of 95 db. Typical values for such a filter are a power per pole of about 1 mW, and an area per pole of about $6.25\ 10^5\ \mu^2$ ($1000\ mils^2$). Using Eq. (3.15) the dynamic range per pole can be determined

from the overall dynamic range of the filter as follows:

$$(DR_{pole}) = 95db + 10 \log 5 = 102\, db \tag{3.21}$$

The plots of Fig. 9 and 10 for a $\pm 5\ Volts$ supply and a dynamic range of 102 db give a minimum area requirement of approximately 1400 μ^2 and a minimum power requirement of approximately 1.7 μW .

The actual values are approximately 2 to 3 orders of magnitude larger than the theoretical minima showing that there is a strong motivation to further reduce the area occupied and the power consumed by the core amplifier. Finally from the above results it immediately follows that to achieve a dynamic range of 95 db in a 5^{th} order voiceband filter operating from a $\pm 5 Volts$ supply the minimum area required is approximately $7300 \mu m^2$ and the minimum power $8.5 \mu W$. On the other hand the absolute maximum dynamic range that can be achieved for the same filter as above assuming a total area of $5000 mil^2$ and a total power dissipation of $5mW$ is approximately 121 db.

4. EFFECT OF AMPLIFIER NONIDEALITIES

As stated in Section 2 all of the above results were based on the assumption of having an op amp with ideal characteristics, i.e. zero power consumption, zero area, zero noise contribution. Such an ideal situation was to be achieved by continuously scaling the feature size, provided that the $\frac{1}{f}$ noise could be eliminated by some technique like chopper stabilization. In actuality practical constraint will result in other limitations on the level of op amp performance achievable. The ultimate minimum value for the above op amp characteristics is very difficult to define. It is however possible, based on a simple model, to obtain upper bounds for the limit values of the above quantities. This is done in this section. The obtained results show that the op amp fundamental limitations should not substantially effect the the ultimate performance of the filter in all practical cases.

4.1. Power Dissipation

In the following the minimum amount of power requested by the op amp for a given clock frequency is compared with the result of Eq. (2.12). The minimum op amp power consumption is obtained under the following assumptions:

1) The limiting factor in the op amp settling time (T_{set}) is given by the linear portion of the step response as opposed to the slewing portion. As a consequence the following equation is valid

$$T_{set} = \delta \tau \tag{4.1}$$

where δ is a number (typically between 5 and 10) that depends on the accuracy required in the step response, and τ is the time constant of the closed loop step response of the op amp (a single pole step response is assumed). If $C_I \gg C_s$ and no large capacitance is attached at the integrator summing node it follows that

$$\tau \approx \frac{1}{\omega_u} \tag{4.2}$$

where ω_u is the unity gain frequency of the amplifier. The above assumption is quite reasonable since class A/B amplifiers that do not exhibit any slewing behaviour and have a power dissipation which is only a few percent higher than their stand by values can be emploied.

2) The devices are operated in the subthreshold region. This corresponds to the maximum possible transconductance for a certain current level I i.e.

$$\frac{gm}{I} = \frac{q}{n\ kT} \tag{4.3}$$

where n is the subthreshold slope factor whose value is typically between 1 and 2.

3) The time allowed for the op amp to settle is assumed to be $\frac{1}{2\ f_{clock}}$ i.e. 50% duty cycle is assumed

4) The most simple inverter like structure of Fig. 11 is assumed for the op amp with the possibility of using cascode devices to enhance the voltage gain.

5) The load capacitance of the integrator is assumed to be equal to $2\,C_s$ i.e. the sampling capacitor of the next stage plus the effective capacitive load at the output due to the feedback circuit which is the series of C_I and C_s.

From assumptions 4) and 5) follows that

$$\omega_u = \frac{gm_I}{2\,C_s} \tag{4.4}$$

where gm_I is the transconductance of the driver device M1. Using assumption 3) in Eq. (4.4) gives

$$\frac{gm_I}{2\,C_s} \geqslant 2\,\delta\ f_{clock} \tag{4.5}$$

The absolute minimum value of gm_I (gm_{min}) is

$$gm_{min} = 4\,\delta\,C_s\ f_{clock} \tag{4.6}$$

using assumption 2) the absolute minimum stand-by current level I_{min} becomes

$$I_{min} = 4\,n\ \delta\,C_s\ f_{clock}\ \frac{kT}{q} \tag{4.7}$$

which gives a minimum power consumption P_{min} of

$$P_{min} = 8\,n\ \delta\,V_s\ C_s\ f_{clock}\ \frac{kT}{q} \tag{4.8}$$

Using Eq. (2.2) in Eq. (4.8) gives

$$P_{min} = 16\,\pi\,n\ \delta\,V_s\ C_i\ f_{unity}\ \frac{kT}{q} \tag{4.9}$$

Comparing the above result with the result of Eq. (2.12) in which the signal frequency is assumed to be f_{unity} gives the following result

$$\frac{P}{P_{min}} = \frac{8\,f_{unity}\ C_I\ V_s^2}{16\,\pi\,n\ \delta\,V_s\ C_i\ f_{unity}\ \frac{kT}{q}} = \frac{V_s}{2\,\pi\,\delta\,n\ \frac{kT}{q}} \tag{4.10}$$

for $n = 1.5$ and $\delta = 7$ Eq. (4.10) gives

$$\frac{P}{P_{\min}} = \frac{V_s}{21\,\pi\,\frac{kT}{q}} = \frac{V_s}{1.7\,V} \tag{4.11}$$

From Eq. (4.11) follows that, for a $\pm 5\ Volt$ supply, the error introduced in the calculation of the absolute minimum power required by an S.C. integrator (Eq. (2.12)) by assuming that the op amp does not consume any power is smaller or equal than about 35%. Ideally, at least, such an error should be much less the the above value since from a fundamental stand point the absolute minimum power required by the op amp is considerably less than the value given by Eq. (4.9). The reason is that the unity gain bandwidth of the simple structure of Fig. 11 does not approach the fundamental speed limit of MOS transistor M1 which is given be the inherent f_T of the device for the particular bias condition used. This is because the parasitic capacitance of M1 is typically much smaller than the load capacitance C_s, as it will be shown in the next section. It is, at least conceptually, possible to increase the value of the unity gain bandwidth of an op amp up to a more close fraction of the f_T of the devices used. One possible way to reach such a goal for the simple structure of Fig. 11 is to use positive feedback around M1 in order to obtain a larger transconductance for the same value of the current level and device size.

All of the above considerations suggests that the ultimate limit in the power dissipation of an S.C. integrator does not come from the op amp consistently with the assumption of section 2.

4.2. Amplifier Noise and Finite Bandwidth

The only fundamental noise associated with the op amp is the white portion. As it was said in Section 2 this noise component can be expressed in the same form as the $\frac{kT}{C}$ one. The relative importance of the amplifier noise with respect to the noise of the MOS switches is considered in this section. The total noise of an S.C. integrator (both MOS switches and op amp contribution) depends on the relative value of the op amp unity gain bandwidth, ω_u, and the cut-off frequency of the low pass filter formed by the switch resistance and the sampling

capacitor ω_{on} whose value is given by $\omega_{on} = \frac{1}{R_{oni}\ C_s}$ where R_{oni} is the on resistance of the i^{th} MOS switch. With reference to Fig. 12 two extreme cases exist. The first case is the one considered in Section 2 where an infinite op amp bandwidth has been assumed. This gives the same noise contribution for both the left and right hand side switches and a negligible contribution from the op amp assuming a finite total noise energy in the amplifier. On the other extreme case the op amp bandwidth is assumed to be much smaller than ω_{on}. By performing a simplified analysis as it was done by Gobet and Knob [25] both the noise contributed by the right hand side switches (n_R^2) and by the op amp (n_{OP}^2) can be expressed as a fraction of the noise contributed by the left hand side switches (n_L^2), which was calculated in Section 2, as follows.

$$\frac{n_R^2}{n_L^2} \approx \frac{\omega_u}{\omega_{on}} = \frac{gm_1}{2\,C_s}\,R_{on\,1}\,C_S = \frac{gm_1\ R_{on\,1}}{2} \tag{4.12a}$$

$$\frac{n_{OP}^2}{n_L^2} \approx \frac{\frac{R_{eq}}{R_{on\,2}}}{2\,\frac{\omega_{on}}{\omega_u}} = \frac{gm_1\ R_{eq}}{2} \tag{4.12b}$$

in the derivation of both Eqs. (4.12a) and (4.12b) Eq. (4.4) was used and R_{eq} is the equivalent input noise resistance of the op amp. From Eq. (4.12a) making use of the assumption that $\omega_{on} \gg \omega_u$ it can be concluded that the contribution of the right hand switches is negligible. On the other hand assuming that the op amp noise is contribute primarily by the input device M1 and that no high frequency second stage noise contribution occurs it follows that $R_{eq} = \frac{2}{3}\,\frac{1}{gm_1}$ and Eq. (4.12b) gives $\frac{n_{OP}^2}{n_L^2} \approx \frac{1}{3}$. Between the two extreme case there is only about 30% change in the total output noise contribution, furthermore if a source coupled pair is assumed at the op amp input such a change is reduce to only about 15%. From the above results it seems reasonable to conclude that in any practical situation Eq. (2.17) will be reasonably accurate.

In reality one more potential source of noise degradation exist when the output of the S.C. integrator is sampled by another circuit of the same kind, which is the case in any S.C. filter configuration. This is due to the continuous time noise that is transmitted to the output by the amplifier independently of which phase of the clock is high. Such a wide band component can be aliased into the baseband by the next stage sampling operation. Fortunately it can be shown that for the case of a single stage transconductance amplifier the above nose contribution combines with the thermal noise of the MOS switches of the following stage in such a way that the variance of the total noise sampled is unchanged.

4.3. Amplifier Area

In this section the minimum amount of area required for the op amp is compared with the result of Section 2. The simple structure of Fig. 11 is again assumed. The area of the amplifier is assumed to be approximately equal to the area of M1 i.e. the load device is assumed to be much smaller than M1 and therefore neglected in the area calculation. The total area of the transistor is assumed to be equal to β times the area of its gate. Typical values for β can be taken to be between 2 and 5. In the following to obtain numerical results $\beta = 3$ is used. Such a value can be achieved in practice by folding the transistor many times in order to have sources and drains sharing the same diffusion area. M1 is assumed to be operating in subthreshold. This is done to be consistent with the assumption used in the section dealing with the op amp power and also to insure a reasonable amount of gain in the amplifier.

The maximum current level in weak inversion for a given aspect ratio is roughly given by[25]

$$I = \mu C_{ox} \frac{Z}{L} \left(\frac{kT}{q} \right)^2 \tag{4.13}$$

Eq. (4.13) defines the minimum value of the aspect ratio $\frac{Z}{L}$ of an MOS transistor for which the devices is still operating in weak inversion for any given current level. Minimum aspect ratio corresponds to minimum gate area for a given technology therefore the above condition is used in the following calculation. Combining Eq. (4.3) with Eq. (4.13) an expression for the

device transconductance is obtained.

$$gm = \mu C_{ox} \frac{Z}{L} \frac{kT}{q\ n} \tag{4.14}$$

Substituting in Eq. (4.6) for gm_{min} the expression of Eq. (4.14) and making use of Eq. (2.2) gives

$$\mu C_{ox} \frac{Z}{L} \frac{kT}{q\ n} = 4\ \delta\ C_s\ f_{clock} = 8\ \pi\ \delta\ C_I\ f_{unity} \tag{4.15}$$

Multipling both sides of Eq. (4.15) by L^2 and solving for the gate area of M1 i.e. $Z\ x\ L$ gives

$$Z\ x\ L = \frac{8\ \pi\ \delta\ q\ n\ f_{unity}\ L^2}{kT\ \mu} \frac{C_I}{C_{ox}} \tag{4.16}$$

Noticing that $\frac{C_I}{C_{ox}}$ is nothing but the area of C_I follows that

$$\frac{Z\ x\ L}{Area\ of\ C_I} = \frac{8\ \pi\ \delta\ q\ n\ f_{unity}\ L^2}{kT\ \mu} \tag{4.17}$$

The op amp area was assumed to be equal to β times the area of the gate of M1 therefore

$$\frac{Area\ of\ Op\ Amp}{Area\ of\ C_I} = \frac{\beta\ 8\ \pi\ \delta\ q\ n\ f_{unity}\ L^2}{kT\ \mu} \tag{4.18}$$

Using $\mu = 800\ \frac{cm^2}{V\ sec}$ $n = 1.5$ $\delta = 7$ $\beta = 3$ in Eq. (4.18) gives

$$\frac{Area\ of\ Op\ Amp}{Area\ of\ C_I} = 38\ L^2\ f_{unity} \tag{4.19}$$

Assuming a 1 μm minimum channel length technology it follows from Eq.(4.19) that $\frac{Area\ of\ Op\ Amp}{Area\ of\ C_I} = 1$ for $f_{unity} \approx 2.6\ MHz$. These results show that for future scaled technologies i.e. 1 μm or less minimum channel length, the dominant factor in determining the ultimate limits in the minimum achievable area of an S.C. integrator is given by the size of the integration capacitor and not by the op amp area up to filter bandwidths well into the MHz range. This again is consistent with the assumptions of Section 2.

5. CONCLUSIONS

In this paper the fundamental limitations which determine the ultimate achievable performance for an S.C. low pass filter have been analyzed. Such limitations are fundamental in the sense that they cannot be eliminated by process, circuit or system improvement.

Making use of certain assumptions these limitations are first obtained for the S.C. integrator. The results show that both the power and the area requirement vary as the square of the dynamic range. The analysis is also extended to a ladder low-pass filter structure.

By introducing approximations that, in most practical cases, cause only a small error, some simple relationship between the dynamic range and the minimum area and power necessary to achieve it are obtained. By plotting such relationship on a log-log scale with the supply voltage and the cut-off frequency of the filter as parameters, a very easy way to compare the actual filter performance with the theoretical limit values is provided.

The potential for a large improvement on the overall performance of today's state of the art filters by further improving the characteristics of the op. amps. used to realize the integrators is shown.

Finally the absolute minim area and power consumption for a 5^{th} order voiceband filter with 95 db of dynamic range assuming a $\pm 5Volts$ supply are shown to be approximately $7300\mu m^2$ and $8.5\mu W$ respectively. the ultimate performance of the filter in all practical cases.

APPENDIX 1

With reference to Fig. 3 the energy drawn from the supplies during one clock is first computed.

Assuming a positive input signal $v_i\ (t)$ (the result is dual for a negative one) and calling $i_i\ (t)$ the current in C_s and $i_o\ (t)$ the current in C_i, as shown in Fig. 3, than $I_i\ (t) = I_1$ and $I_o\ (t) = -I_2$. The amount of energy drawn from the supplies during one clock period, ϵ_{clock}, is given by

$$\epsilon_{clock} = V_{CC} \int_{nT}^{(n+1)T} I_1\ (t)\, dt - V_{EE} \int_{nT}^{(n+1)T} I_2\ (t)\, dt = \tag{A.1}$$

$$= V_{CC} \left\{ Q_S \left[(n+1)T \right] - Q_S \left[nT \right] \right\} = V_{EE} \left\{ Q_i \left[(n+1)T \right] - Q_i \left[nT \right] \right\}$$

where $Q_S\ (nT)$ ($Q_i\ (nT)$) is the charge on C_S (C_i) at $t = nT$. Assuming that ϕ_2 is on for $nT \leqslant t < (n + \frac{1}{2})T$ that ϕ_1 is on for $(n + \frac{1}{2})T \leqslant t < nT$ than

$$Q_S\ (nT) = 0 \tag{A.2}$$

$$Q_S \left[(n+1)T \right] = C_S\ V_i \left[(n+1)T \right]$$

From charge conservation at the amplifier summing node follows that

$$Q_i \left[(n+1)T \right] - Q_i \left[nT \right] = -C_S\ V_i \left[nT \right] \tag{A.3}$$

The total energy drown from the two supplies during one clock cycle is therefore

$$\epsilon_{clock} = V_{CC}\ C_S\ v_i \left[(n+1)T \right] + V_{EE}\ C_S\ v_i \left[nT \right] \tag{A.4}$$

For a sinusoidal input signal of peak amplitude V_i and frequency f the total amount of energy drawn during a full cycle of the input signal, ϵ_{cycle}, is

$$\epsilon_{cycle} = 2\, C_S\ V_i\ (V_{CC} + V_{EE}) \sum_{n=0}^{M} \sin\left(\frac{\pi}{n}\ M\right) \tag{A.5}$$

where $M = \frac{f_{clock}}{2\, f}$. For simplicity in the following M is suppose to be an integer number.

The summation appearing in Eq. (A.4) is evaluated below. Noticing that $\sin x = \mathrm{Im}[\, e^{jx} \,]$ follows that

$$\sum_{n=0}^{M} \sin\left(n \frac{\pi}{M}\right) = \mathrm{Im}\left[\sum_{n=0}^{M} e^{j n \frac{\pi}{M}}\right] = \tag{A.6}$$

$$= \mathrm{Im}\left[\frac{1 - e^{j \frac{\pi}{M}(M+1)}}{1 - e^{j \frac{\pi}{M}}}\right] = \mathrm{Im}\left[\frac{1 + e^{j \frac{\pi}{M}}}{1 - e^{j \frac{\pi}{M}}}\right]$$

$$= \frac{\sin\left(\frac{\pi}{M}\right)}{\left(1 - \cos\left(\frac{\pi}{M}\right)\right)} = Cotg\left(\frac{\pi}{2M}\right)$$

Since $cotg(x) \approx \frac{1}{x}$ if $x \ll 1$ by making use of Eq. (2.2) in the above result it follows that

$$\sum_{n=0}^{M} \sin\left(n \frac{\pi}{M}\right) \approx \frac{f_{clock}}{\pi f} \tag{A.7}$$

Substituting Eq.(A.7) in Eq. (A.5) gives

$$\epsilon_{cycle} = \frac{2}{\pi} C_S V_i \left(V_{CC} + V_{EE}\right) \frac{f_{clock}}{f} \tag{A.8}$$

Assuming to use symmetrical supplies i.e. $V_{CC} = V_{EE} = V_s$ the final result is obtained

$$\epsilon_{cycle} = \frac{4}{\pi} C_S V_i V_s \frac{f_{clock}}{f} \tag{A.9}$$

FIGURE CAPTIONS

Fig. 1 Bottom plate S.C. integrator

Fig. 2 Circuit used to compute the power drown from the supplies

Fig. 3 Equivalent circuit of Fig. 2

Fig. 4 Closed-loop S.C. integrator

Fig. 5 One pole S.C. filter

Fig. 6 Passive ladder prototype for a 3^{rd} order low-pass filter

Fig. 7 Block diagram for the circuit of Fig. 6

Fig. 8 Bottom plate integrator/summer

Fig. 9 Minimum power dissipation vs. dynamic range for different values of f_{max}

Fig.10 Minimum chip area vs. dynamic range for different values of V_s

Table1 Parameter values for the Intel 2912 PCM low-pass filter ($f_{max} = 3.4kHz$, $\frac{1}{f_{max}} = 294\ \mu\text{sec}$, $n = 5$)

REFERENCES

[1] B.J. Hosticka, R.W. Brodersen, and P.R. Gray, "MOS Sampled Data Recursive Filter Using Switched Capacitor Integrator", *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600-608, Dec. 1977.

[2] J.T. Caves, M.A. Copland, C.F. Rahim, S.D. Rosenbaum, "Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalent" *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 592-599, Dec. 1977.

[3] W.C. Black , Jr., D.J. Allstot, R.A. Reed, "A High Performance Low Power CMOS Channel Filter," *IEEE J. Solid-State Circuits*,

[4] F. Krummenacher, "Micropower Switched Capacitor Biquadratic Cell," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 507-512, June 1982.

[5] B.J. Hosticka, D. Herbst, B. Hoefflinger, U. Kleine, J. Pandel, R. Schweer, "Real-Time Programmable SC Bandpass Filter," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 499-506, June 1982.

[6] B.J. Hosticka, "Dynamic CMOS Amplifiers" *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 887-894, Oct. 1980.

[7] M.G. Degrauwe, J. Rijmenants, E.A. Vittoz, and H.J. De Man, "Adaptive Biasing CMOS Amplifiers" *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 522-528, June 1982.

[8] K.C. Hsieh, and P.R. Gray, D. Senderowicz, D. Messerschmitt "A Low-Noise Chopper-Stabilized Differential Switched Capacitor Filtering Technique," *IEEE J. Solid-State Circuits*, vol. SC-16 pp.708-715, Dec. 1981.

[9] L.T. Lin, H.F. Tseung, D.B. Cox, S.S. Viglione, D.P. Conrad, and R.G. Runge, "A Monolithic Audio Spectrum Analyzer" *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 40-45, Feb. 1983.

[10] Y.Kuraishi, T. Makabe, and K. Nakayama, "A Single-Chip Analog Front-End LSI for Modems" *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1039-1044, Dec. 1982.

[11] Y.A. Haque, R. Gregortan, D. Blasco, R. Mao, and W. Nicholson, "A Two-Chip PCM Codec with Filters" *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 961-969, Dec. 1979.

[12] D.Senderowicz, S.F. Dreyer, J.H. Huggins, C.F. Rahim, and C.A. Laber, "A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip" *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1014-1023, Dec. 1982.

[13] D.Senderowicz, D.A. Hodges, and P.R. Gray, "A High-Performance NMOS Opera tional amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 760-768, Dec. 1978.

[14] Y.P. Tsividis and, P.R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 748-753, Dec. 1976.

[15] D.Senderowicz, J.H. Huggins, "A Low-Noise NMOS Operational Amplifier" *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 999-1008, Dec. 1982.

[16] R. Gregorian, and W. A. Nicholson JR., "CMOS Switched-Capacitor Filters for a PCM Voice CODEC," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 970-980, Dec. 1979.

[17] K.C. Hsieh, "Noise Limitations in Switched-Capacitor Filters," *Ph. D. Dissertation*, University of California, Berkeley;

[18] T.C. Choi, and R.W. Brodersen, "Considerations for High-Frequency Switched- Capacitor Ladder Filters" *IEEE Trans. Circuits and Syst.* vol. CAS-27, pp. 545-552, June 1980.

[19] R.W. Brodersen, P.R. Gray, D.A. Hodges, "MOS Switched-Capacitor Filters," *Proc. IEEE*, pp. 61-71 Jan. 1979.

[20] D.J. Allstot,"MOS Switched Capacitor Ladder Filter", *Ph. D. Dissertation*, University of California, Berkeley; May 1979.

[21] P.R. Gray, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: Wiley, 1977.

[22] L.R. Rabiner, and B. Gold, *Theory and Application of Digital Signal Processing*, Englewood Cliff: Prentice-Hall, 1975.

[23] C.A. Gobet, and A. Knob, "Noise Analysis of Switched Capacitor Networks," *IEEE Trans. Circuits and Syst.* vol. CAS-30, pp. 37-43, Jen. 1983.

[24] C.A Gobet, "Spectral Distribution of a Sampled 1st-Order Lowpass Filtered White Noise," *Electronics Letters*. vol. 17 No 19, pp. 720-721, Sept. 1981.
[25] E. Vittoz, and F.Krummenacher, "Micropower SC Filters in Si-Gate CMOS Technology," in *Proceedings*ECCTD'80, Warsaw, vol. 1, pp.61-72, Sept. 1980.

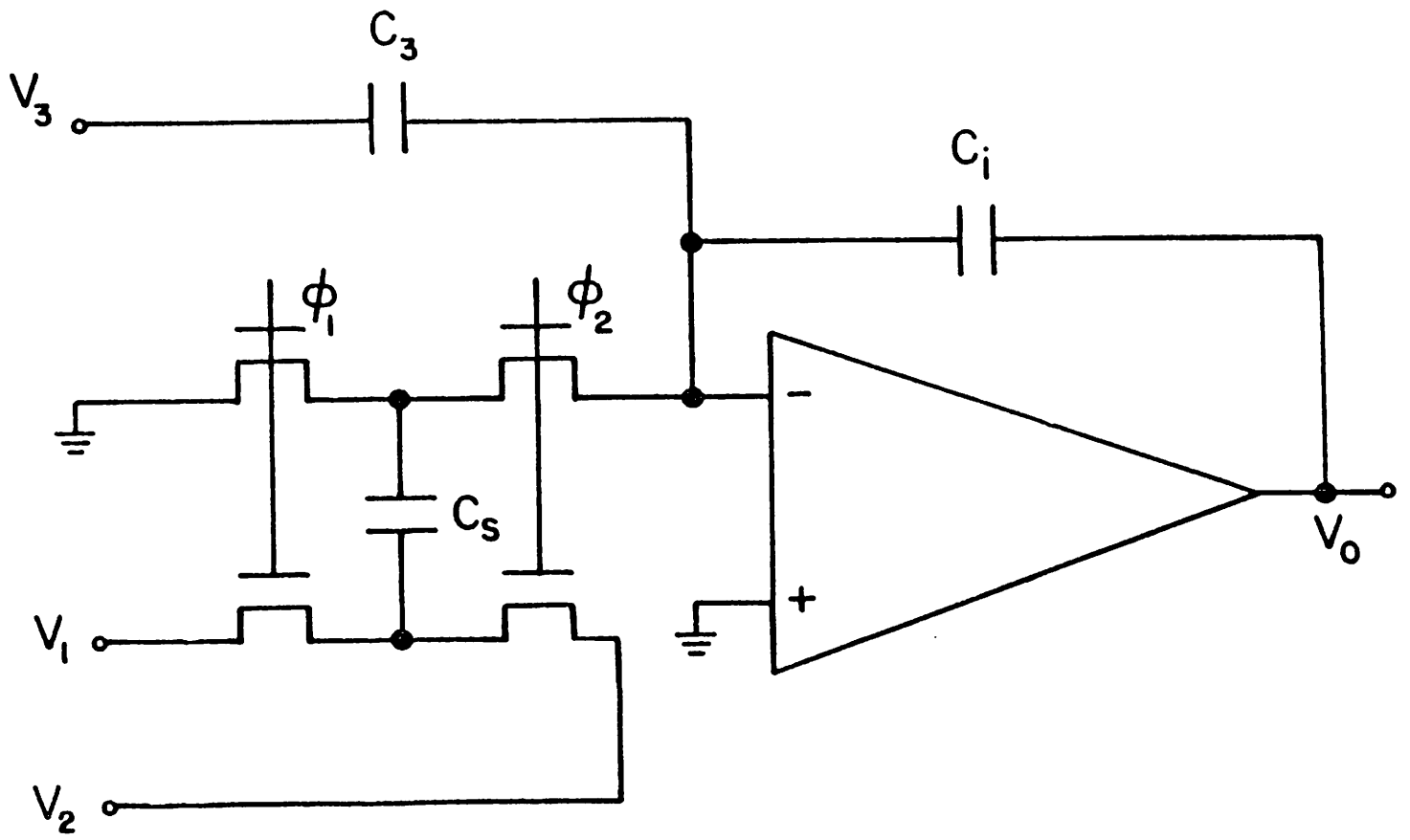


Fig. 1

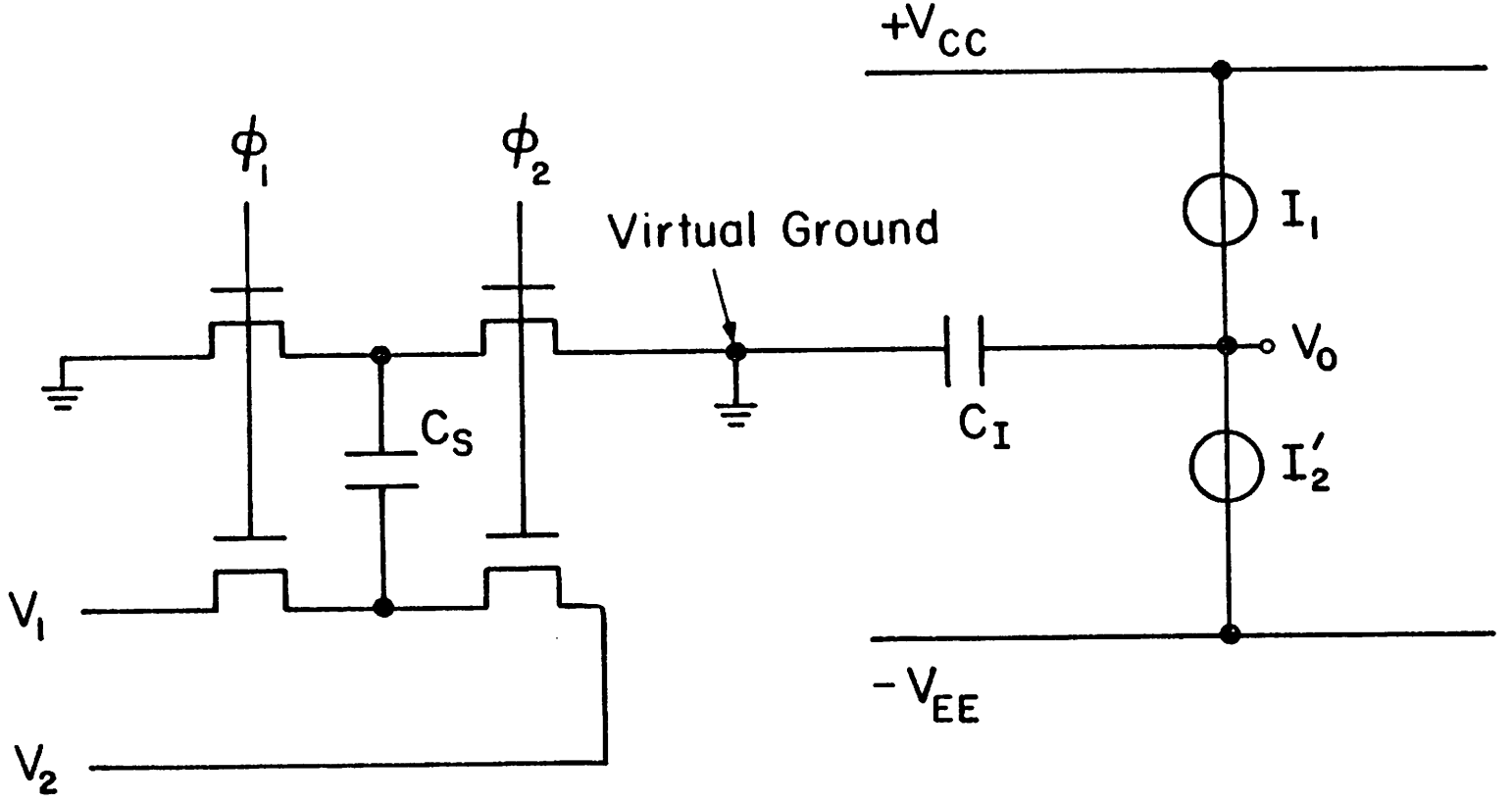


Fig. 2

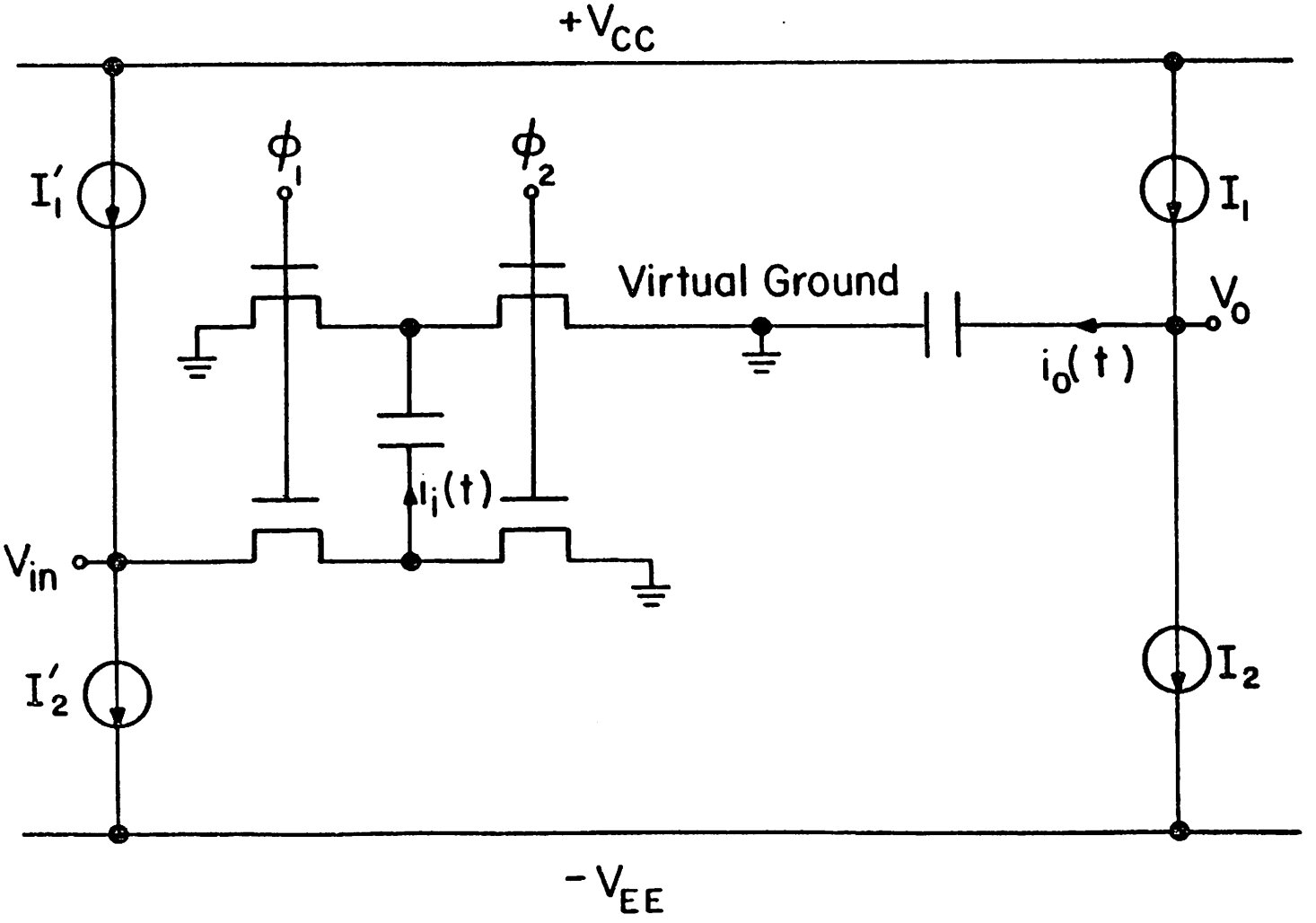
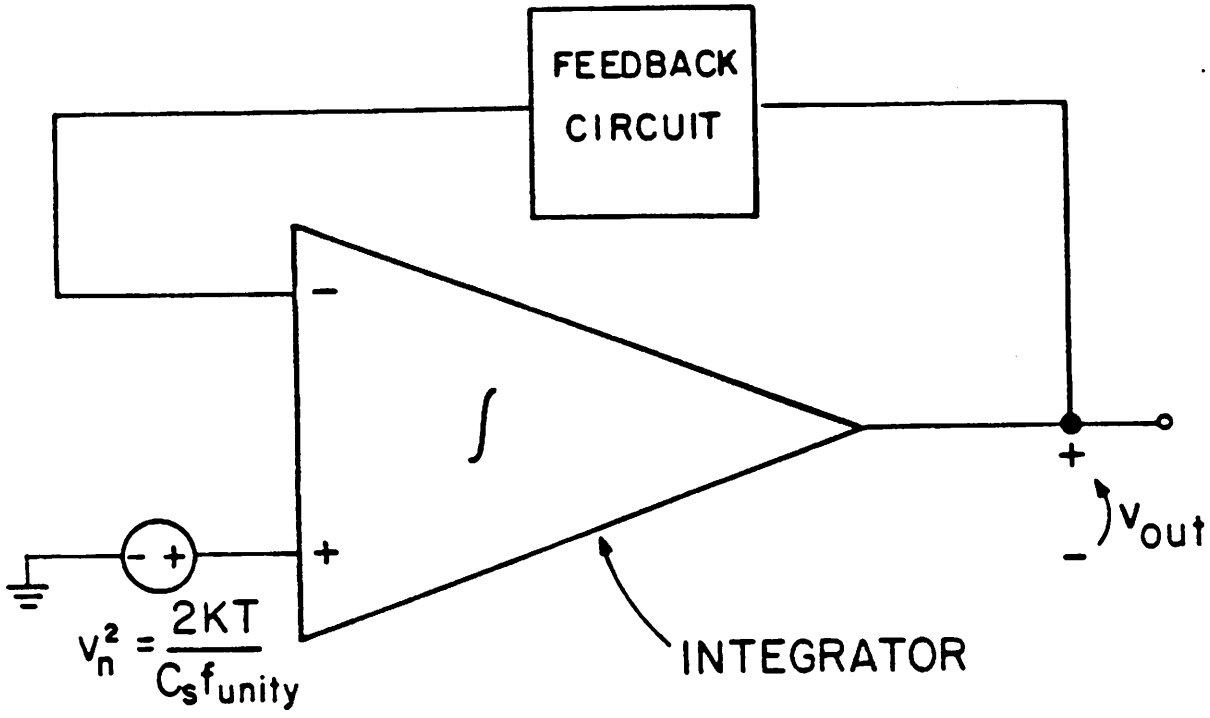


Fig. 3


FEEDBACK
CIRCUIT
−
+
∫
+
v_{out}
−
$v_n^2 = \frac{2KT}{C_s f_{unity}}$
INTEGRATOR

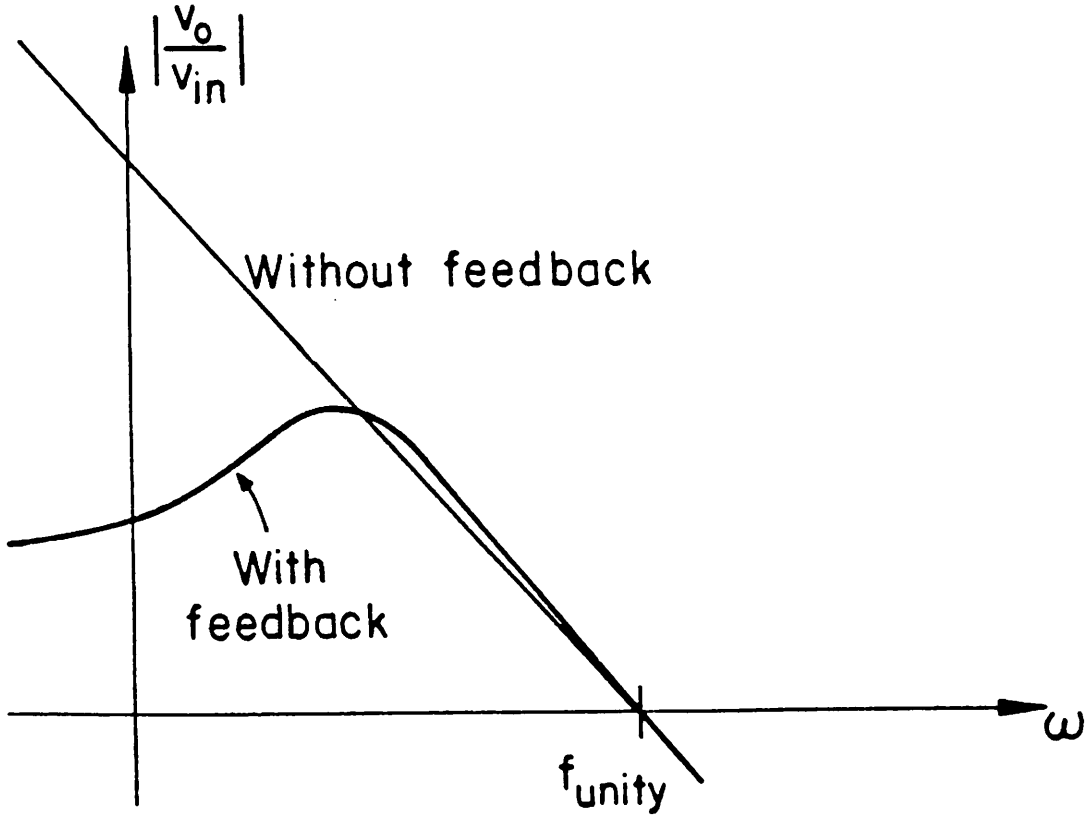
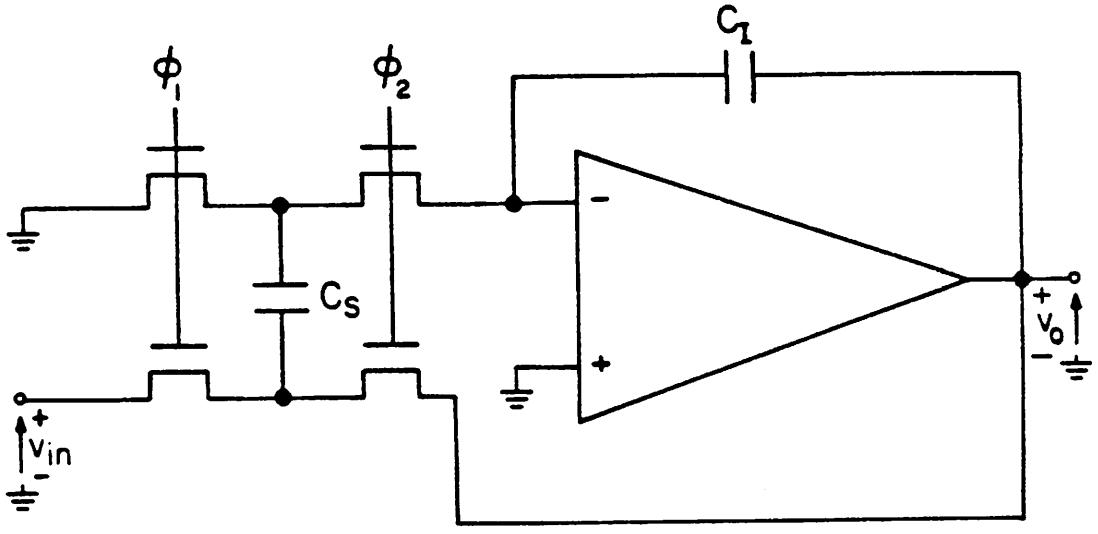

$\left|\frac{V_o}{V_{in}}\right|$
Without feedback
With
feedback
ω
f_{unity}

Fig. 4



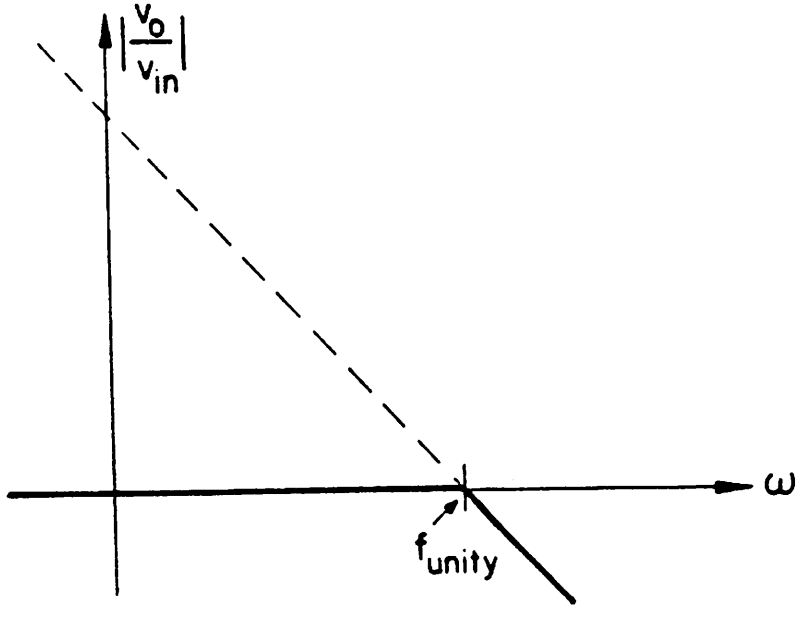


Fig. 5

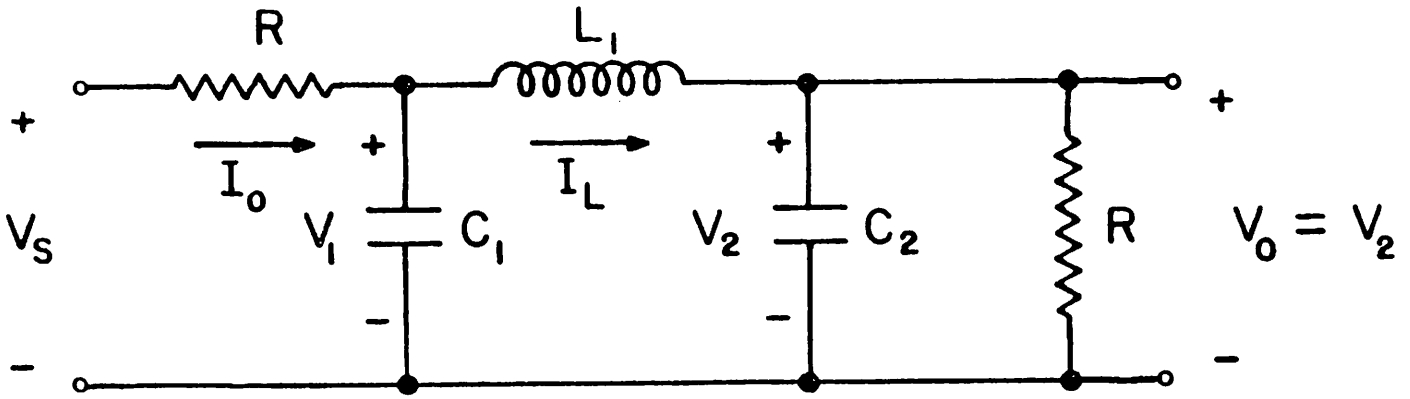


Fig. 6

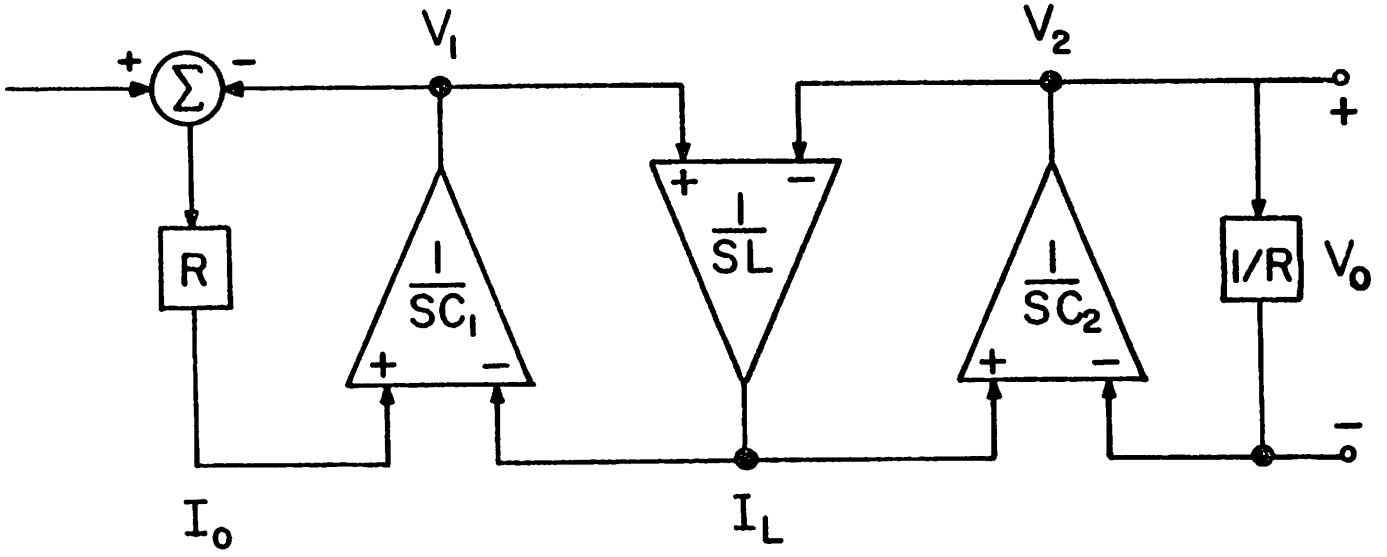


Fig. 7

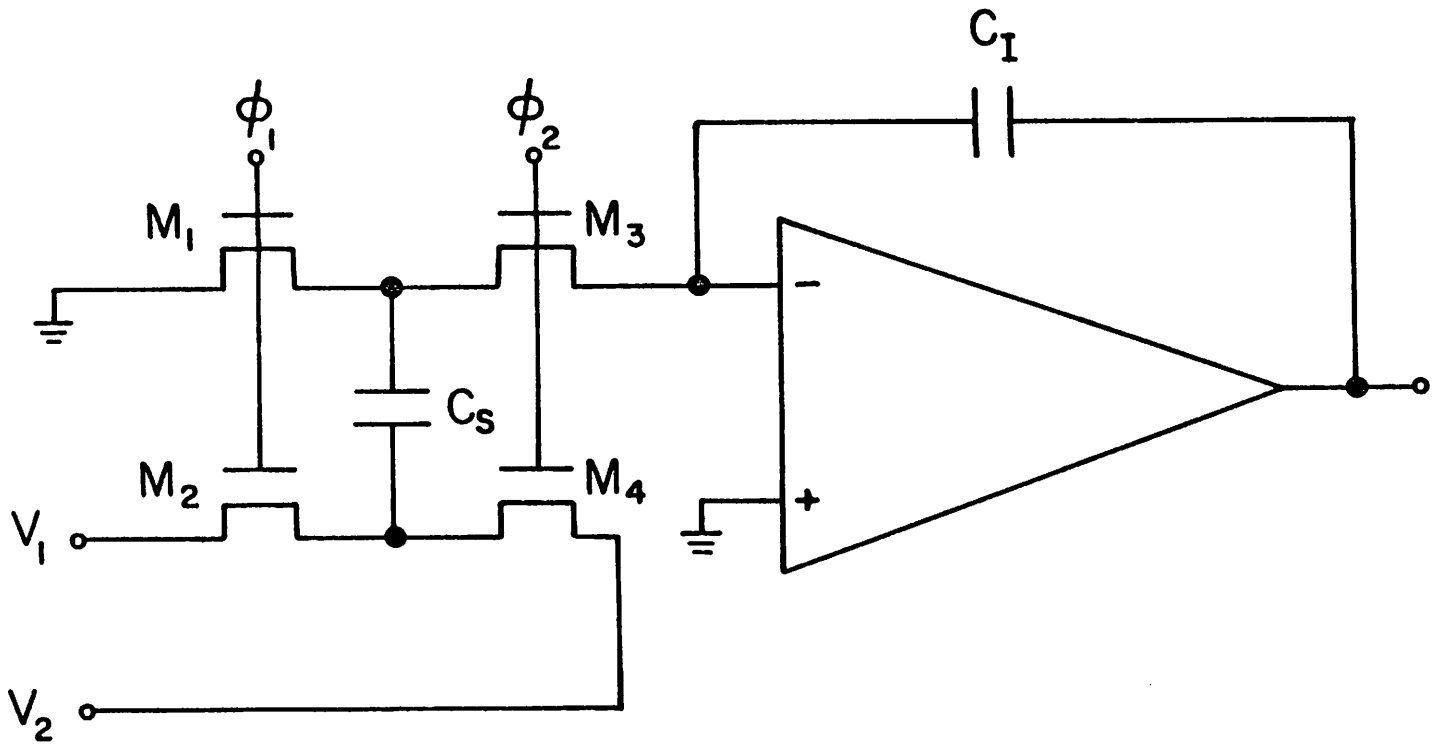


Fig.8

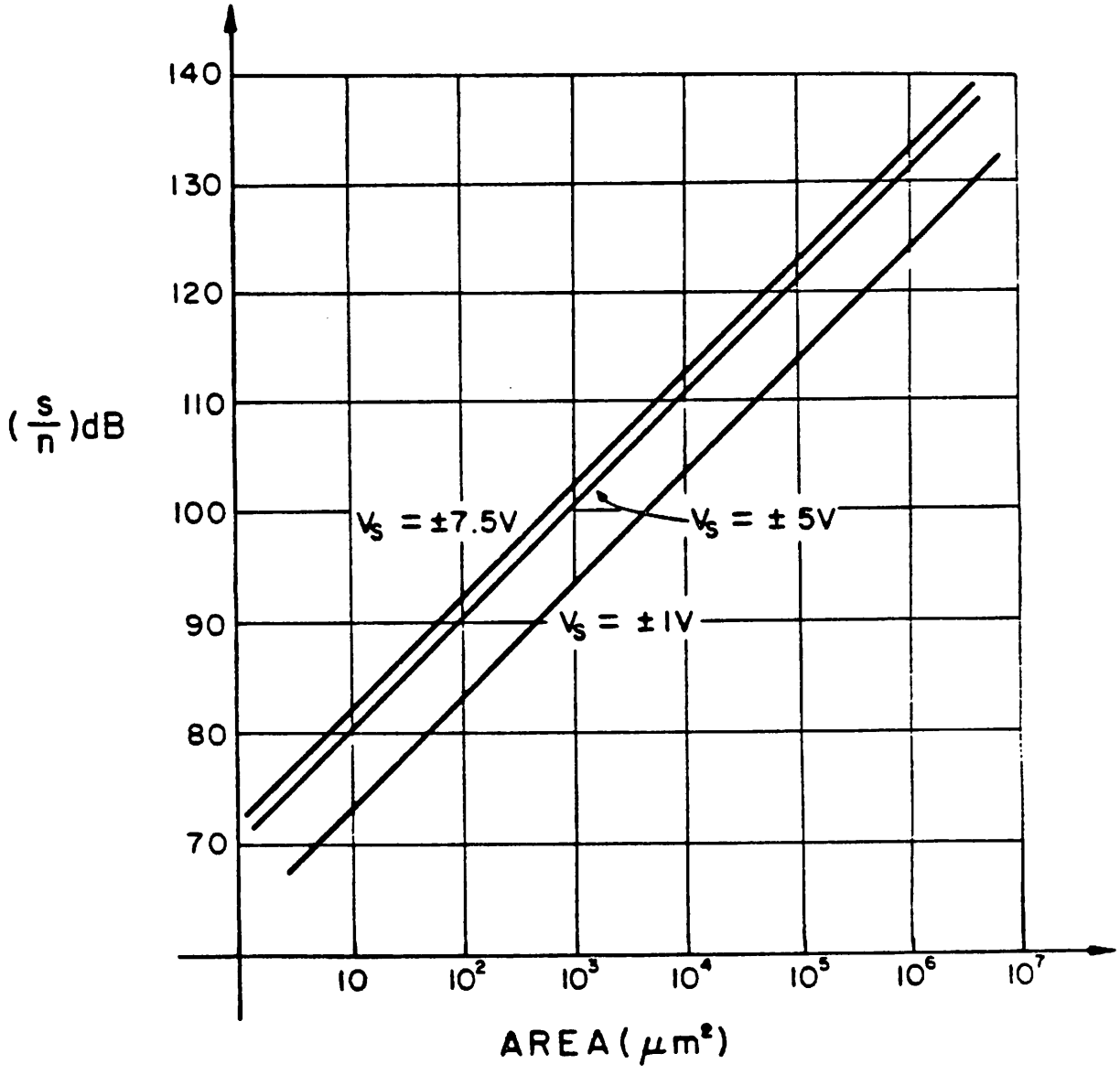

140
130
120
110
100
90
80
70
$(\frac{S}{n})dB$
$V_S = \pm 7.5V$
$V_S = \pm 5V$
$V_S = \pm 1V$
10
10^2
10^3
10^4
10^5
10^6
10^7
AREA (μm^2)

Fig. 9

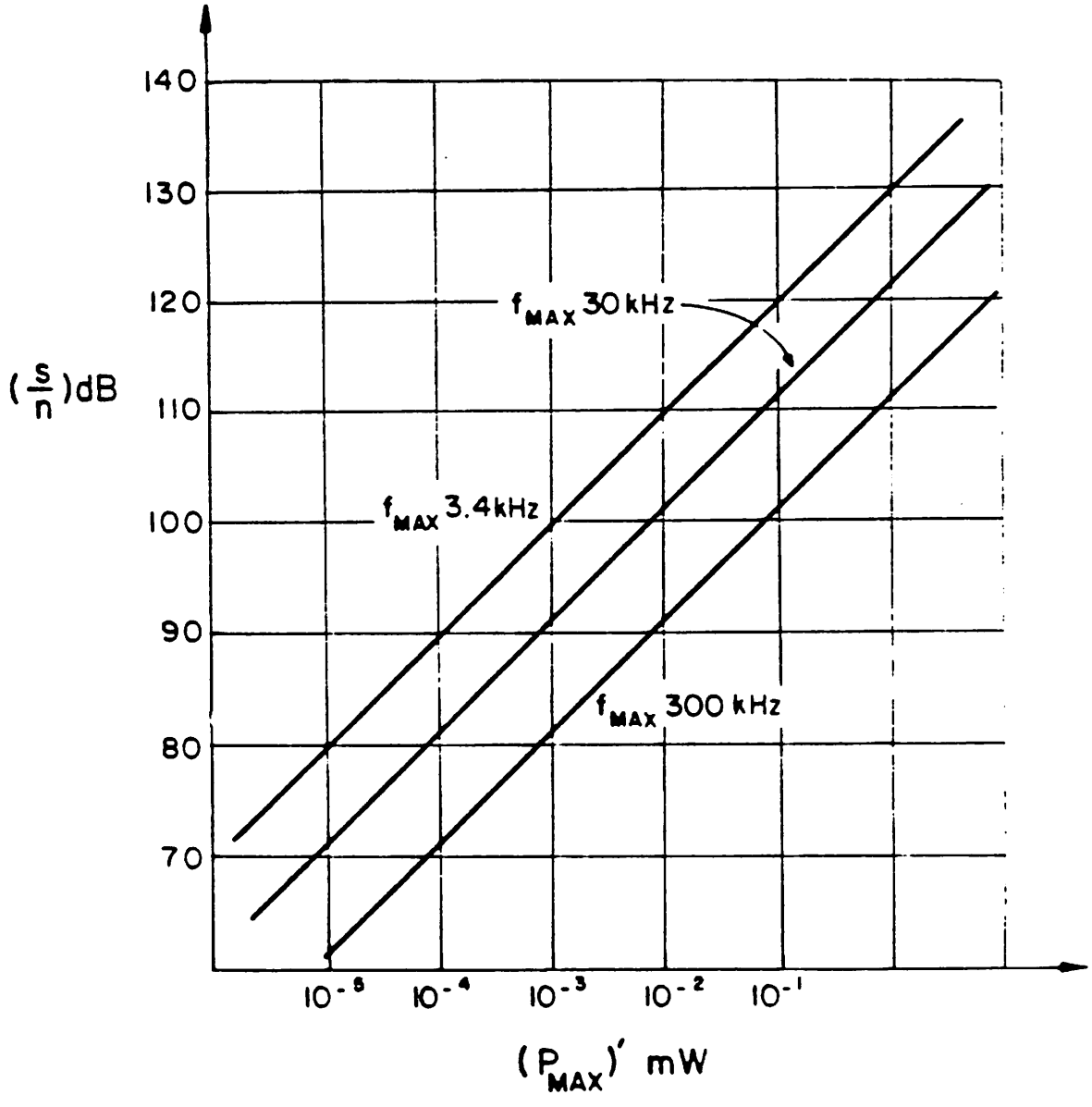

140
130
120
110
100
90
80
70
$(\frac{S}{n})$dB
f_{MAX} 30 kHz
f_{MAX} 3.4 kHz
f_{MAX} 300 kHz
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
$(P_{MAX})'$ mW

Fig. 10

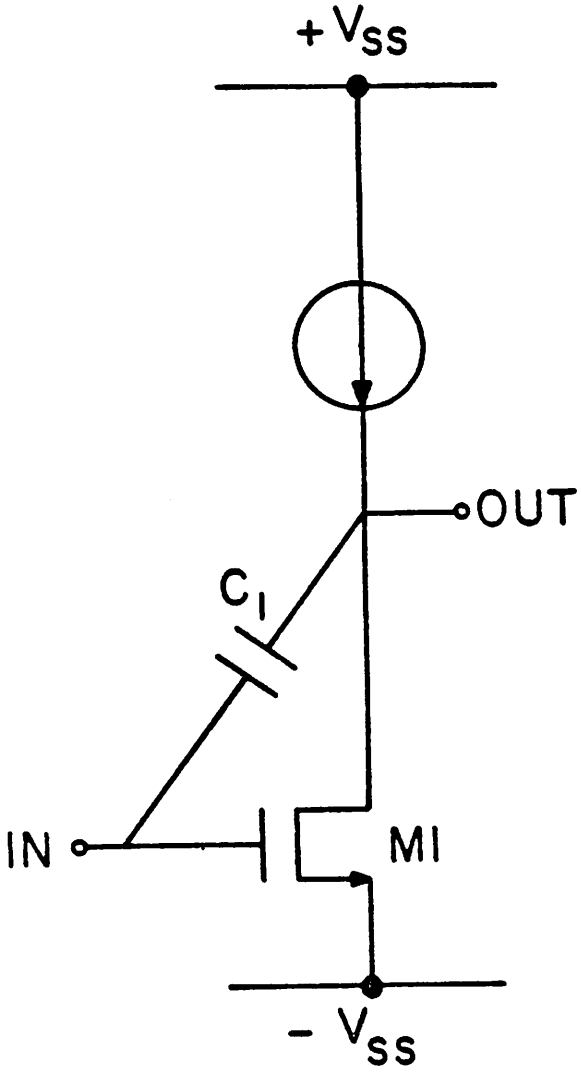


Fig. 11

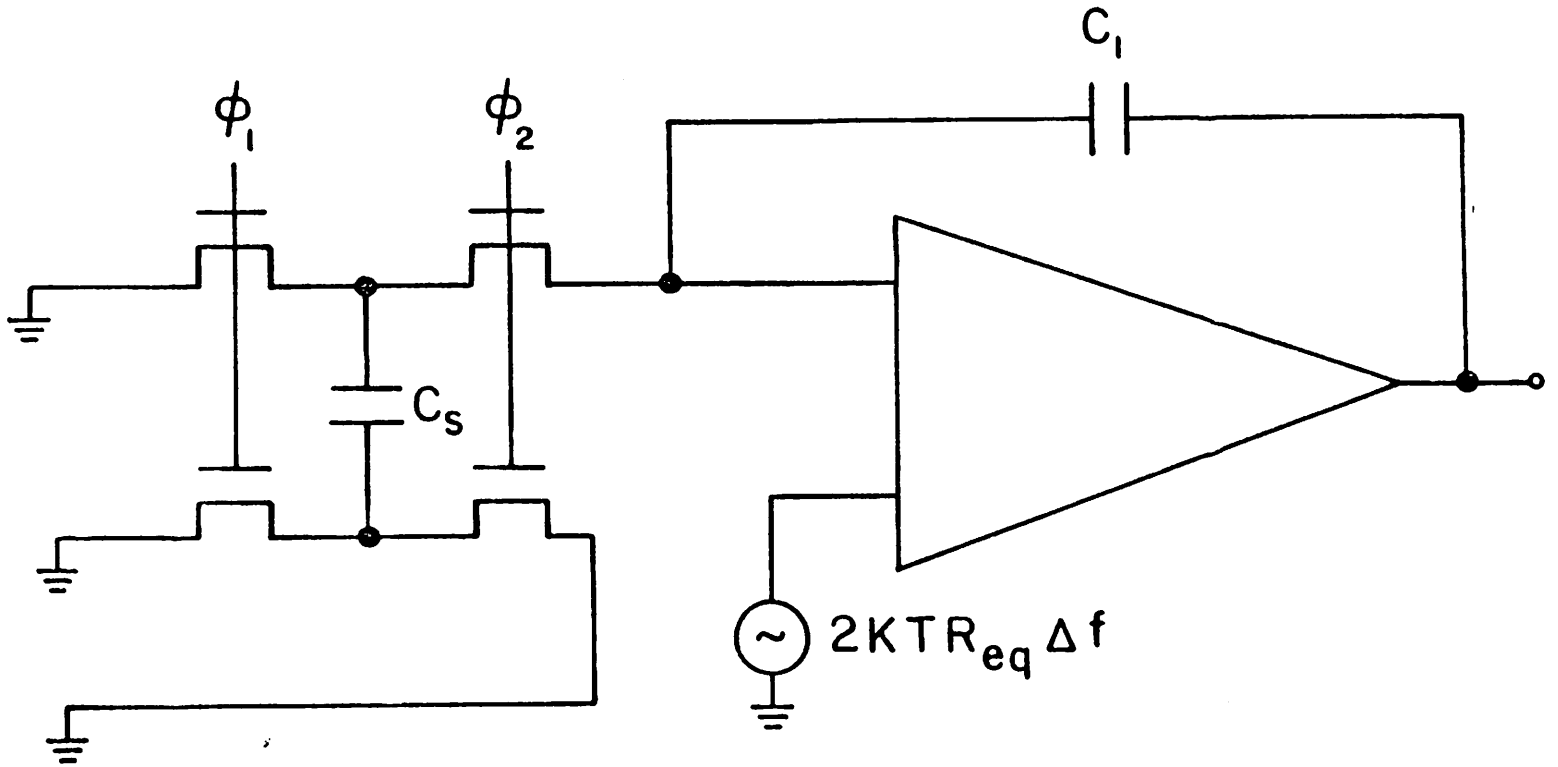


Fig. 12

TABLE I

	f_i (kHz)	$1/f_i$ (μs)	$\Delta C_i/C_I$	$(\Delta C_i/C_I)^2$
i = 1	4.715	212.1	-.2789	.077
i = 2	2.227	449	.527	.277
i = 3	5.186	192.8	-.344	.118
i = 4	4.0415	247.4	.159	.025
i = 5	2.965	337.3	-.147	.0216
Σ / 5	3.826	287.5	-.021	.1037