LOW-POWER LOW-VOLTAGE HIGH PERFORMANCE SWITCHED-CAPACITOR FILTER

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ELECTRONICS RESEARCH LABORATORY

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MOS technology scaling requires the use of lower supply voltages. Analog circuits operating from a low supply and achieving a sufficiently large dynamic range must be designed if analog/digital interfaces are to be implemented in scaled technologies. This paper describes a high performance 5th order low-pass S.C. filter operating from a single 5 Volts supply. The filter uses a fully-differential topology combined with input-to-output class A/B amplifier design, dynamic biasing, and S.C. common mode feedback. An experimental prototype fabricated in a $5\mu m$ CMOS technology requires only $350\mu W$ of power to meet the PCM channel filter requirements. Typical measured results are: a dynamic range of 92 dB, a supply rejection (PSRR) of more than 50dB and a total harmonic distortion (THD) of -73 dB for a 2 V rms differential output signal. The chip active area is about 3900 $mils^2$.

1. INTRODUCTION

Switched-Capacitor (S.C.) filters performance has been steadily improving in the last several years and many prototypes satisfying the stringent PCM channel filter requirement have been reported [1-6]. However, in the most recent commercial implementation the required power-per-pole is in the neighborhood of 1 mW and a relatively high double polarity ($\pm 5 V$) supply voltages is needed.

From a fundamental stand point, the absolute minimum achievable power dissipation in a voiceband filter with a dynamic range of 90 db in a 3-micron technology operated from a $\pm 5 V$ supply is less than one microwatt per pole [23]. A very large margin for improvement is therefore available. A reduction in the power consumption is important in the realization of battery operated analog/digital interfaces and could prove to be even more important in the future as larger and more complex systems are integrated on the same chip [7].

At the same time, as a consequence of the continuous scaling of MOS technology, supply voltages will have to be reduced if analog interfaces are to take advantage of this scaling [8]. This fact, and the desire of having an analog/digital compatible technology, create a strong motivation for developing new approaches in the design of analog circuits to make them more suitable for low voltage operation.

Recently many low power MOS circuits suitable for S.C. applications have been presented [9-15]. Of these, some are also intended to be used from a low voltage supply [10-13,15]. All of them, however, are for special purpose applications, use a low frequency clock (with the exception of [12]), and have relatively low performance. In fact no low-voltage, low-power filter meeting the PCM channel filter requirement have been reported to date.

In this paper a 5th order CMOS PCM channel filter operating from a single 5 Volts supply and dissipating about 70 $\mu Watt$ per pole is described. The device utilizes a combination of circuit techniques including input-to-output class A/B amplifier design, fully differential topology, dynamic biasing, switched capacitor common mode feedback, etc, which provide performance comparable or improved with respect to past 10 Volts commercial realizations.

2. FILTER ARCHITECTURES FOR LOW-POWER, LOW VOLTAGE, HIGH DYNAMIC RANGE OPERATION

The filter reported in this paper uses the standard active ladder architecture, for its low sensitivity to parameter variations, [16] and utilizes parasitic-free bottom plate S.C. integrators [4]. Some of the main design choices and their motivations are outlined below.

The 6-db loss inherent in the ladder structure is compensated by introducing an extra sampling capacitor at the input of the filter. A gain close to 0 db in the passband is therefore achieved. Such a solution causes a certain amount of peaking (less than 6 db) at some internal nodes for frequencies close to the band edge which degrade the filter linearity for large input signals. On the other hand, by doing this no extra amplification block is needed at the output and the noise level is reduced.

In order to obtain the highest possible performance from a low voltage supply, a fully differential architecture was chosen. The advantages of such a topology, i.e. increased dynamic range, reduced clock feed-through, improved power supply rejection and linearity, have been discussed before [3,17]. These considerations assume a particular significance in low voltage applications. Furthermore the capability, intrinsic in a fully differential approach, to independently choose the value of the input and output common-mode voltage, becomes very important in the design reported here, as will be explained in detail in section 3.

The desired common-mode voltage at the input of each integrator V_{cmi} is established as shown in Fig. 1, while the details of how the common mode output voltage V_{cmo} is defined are given in the next section. Both V_{cmi} and V_{cmo} can be easily generated on chip. For optimum performance (maximum swing) V_{cmo} should be equal to half of the total supply voltage (a single supply is assumed); this is however not the case for V_{cmi} . In the present design V_{cmi} is higher than V_{cmo} by an amount approximately equal to the threshold voltage of the n-channel transistors. A final advantage of a fully differential structure is that it does not require on-chip clock regulation, which results in a substantial saving in area and power.

The main disadvantage of such an approach is an increase in the complexity of both the filter and the amplifier structure with respect to a corresponding single-ended realization. In this design a very efficient common-mode feedback circuit design limits the power consumption increase to approximately 40%, while the total area required increases by as much as 60 to 70 %.

As will be shown in section 3, the voltage at the output of each amplifier can swing to within .5 volts from either supply before any performance degradation starts to occur. Since the values of both p and n thresholds are typically larger than .5 Volts (even in the absence of body effects), it is necessary to use complementary CMOS switches (transmission gates) at all the amplifiers output nodes.

To achieve the maximum possible speed, a class A/B amplifier design has been adopted. In general the use of a class A/B structure should be considered if, by using a class A solution, the portion of the settling time that the amplifier spends in a slewing mode, Δt_1, is comparable to or larger than the portion spent in the linear (small signal) mode Δt_2. For a class A MOS amplifier the relative importance of Δt_1 and Δt_2 depends on both the size of the output voltage step, ΔV_o and on the $V_{GS} - V_T$ of the input devices. The maximum of $\dfrac{\Delta t_1}{\Delta t_2}$ for a given ΔV_o occurs when the input devices are biased in the subthreshold region (which is the case for the present design). For a unity gain feedback configuration it can be shown that [18]:

$$\frac{\Delta t_1}{\Delta t_2} = \frac{\dfrac{\Delta V_o \; q \; \xi^2}{n \; kT}}{\ln \dfrac{1000 \; 2 \; n \; kT}{q \; \Delta V_o}} \tag{1}$$

In EQ. (1) the factor 1000 comes from the fact that a settling accuracy equal to .1% of the voltage step has been assumed, ξ is the damping factor of the closed loop step response and n is the subthreshold coefficient whose value is typically between one and two [25].

To explain the decision of using a class A/B structure for the core amplifier the maximum value of $\dfrac{\Delta t_1}{\Delta t_2}$ for the present design is computed from Eq.1. In order to do this the

maximum value of the output step ΔV_o is first determined with the help of Fig. 2 where a typical S.C. integrator output waveform is shown. The total voltage step that the amplifier must follow, ΔV_o, is given by the sum of the signal excursion over a clock cycle, ΔV_2, plus the value of the initial voltage spike, ΔV_1, which is due to feed-forward effects through the integrator capacitance. For the filter reported here ΔV_1 and ΔV_2 have comparable amplitude. Taking the considerations above into account and assuming $f_{clock} = 128\ kHz$, $\xi = \frac{\sqrt{3}}{2}$, and $n = 1.5$ Eq. 1 gives $\frac{\Delta t_1}{\Delta t_2} > 2$ for a full swing input signal (4.6 Volts peak-to-peak) at 2 kHz frequency.

This suggests that if the slewing portion of the response can be eliminated, without degrading the linear response, the total settling time can be reduced by more than three times. Such a result motivates the choice of using a class A/B structure. Other advantages of the class A/B topology will be discussed in the next section.

3. OPERATIONAL AMPLIFIER DESIGN

The filter performance depends for the most part on the characteristics of the operational amplifier (op. amp.) used to realize the S.C. integrator. For this reason particular care has been taken in the design of such a circuit. This has resulted in a fully differential class A/B amplifier using a single- stage topology. The reasons for choosing a fully differential topology have already been discussed. The only extra advantage not yet mentioned is the absence of any systematic offset at the op. amp. input.

As shown before, the use of a class A/B structure has the potential for achieving the required speed with far less current than is required in a class A solution. Lower current level not only means less power consumption, but, in MOS technology, implies larger gain. Furthermore some of the extra gain obtained can be traded-off for bandwidth by reducing the channel length of some of the output devices; this could allow further reduction of the current level, while still achieving the desired speed.

Low current in the output stage also implies low V_{DSAT} on the output devices and therefore large swing, while low current in the input stage corresponds to a large value of the ratio $\frac{gm}{I}$ which reduces the input random offset voltage [19] caused by the random mismatch in all the devices other than the input ones. On the other hand, class A/B structures are generally more complicated than class A. This increases their area and input offset for a given current level.

A single stage configuration was chosen primarily because it is particularly suitable for class A/B operation; however some of its other positive characteristics are also important. In particular, the power supply rejection at high frequency (beyond the dominant pole) is far better than in the multi-stage case. Furthermore, no high frequency, second stage noise contribution is present, which can be severely damaging in a sample data system due to aliasing effects. Finally in the present design the amount of capacitance present at the output of each amplifier is enough to guarantee proper closed-loop response, so that no extra compensation is required.

The main draw-back of the single stage topology is the need for cascode devices at the output to ensure a sufficient gain with consequent reduction of the allowable swing. This can be particularly damaging in low voltage circuits. However by careful design the problem can be greatly reduced as it is shown below. The details of the particular amplifier used in this project are discussed next.

3.1. Forward Amplifier

A simplified schematic of the main amplifier without common-mode circuitry is shown in Fig. 3. Such a circuit is a modified version of a previously proposed but never realized structure [20]. The common-mode feedback circuit will be considered later. The entire structure is perfectly symmetric about the axes A-A; therefore all of the considerations that can be made about one of the two halves apply totally unchanged to the other one. In this section, for the sake of simplicity, we will always refer to the right hand side of the circuit, unless otherwise

specified.

Transistors M1-M4 are the input cross-coupled devices that split the signal into two paths and provide class A/B operation. Devices M5-M8 perform a level-shift operation and provide the proper voltage at the gates of M3 and M4. Since they are forced to carry a constant current I, independently of the input signal, they essentially behave as batteries.

With zero differential voltage applied assuming that $(\frac{Z}{L})_2 = (\frac{Z}{L})_6$ $((\frac{Z}{L})_1 = (\frac{Z}{L})_5)$ and $(\frac{Z}{L})_4 = (\frac{Z}{L})_8$ $((\frac{Z}{L})_3 = (\frac{Z}{L})_7)$, it follows that $I_1 = I_2 = I$ (neglecting output resistance effects). Since both M11,M14 and M9,M13 are 1:1 current mirrors, the output current is also equal to I. The amplifier power consumption is therefore controlled by the value of the current in the two matched current sources.

3.1.1. Maximum current driving

Next the maximum current driving of the amplifier for a large input signal, ΔV_i, is computed. This is a very important parameter in determining the speed of a class A/B circuit. The limiting factors on the amount of current that the amplifier can deliver to the load are the value of the supply voltage and the size of the largest possible input signal. For a low-voltage, micropower circuit the former is the dominant one as it will be shown below. In all the following, unless otherwise stated, it is assumed that ΔV_i has a positive polarity i.e. the non inverting input (Inp^+) is positive with respect to the inverting one (Inp^-) (the results are dual for a negative polarity). As a consequence of the applied input the combined gate-to-source voltage drop across M1 and M4 increases by ΔV_i, while the drop across M2 and M5 decreases by the same amount which forces I_2 to increase by ΔI_2 and I_1 to decrease by ΔI_1. Such a variation is mirrored to the output with a gain of 1 via M11,M14 and M9,M13 giving a total output current (I_L) available to charge the load capacitance equal to:

$$I_L = \Delta I_1 + \Delta I_2 = I_2(\Delta V_i) - I_1(\Delta V_i) \qquad (2)$$

The maximum differential signal that can be expected at the input of the amplifier is close to 1 Volt. Since any input signal in excess of approximately 150 mV gives $I_1(\Delta V_i) \approx 0$ it

follows that the maximum load current I_L^{MAX} is

$$I_L^{MAX} \approx I_2 (\Delta V_i)_{MAX} \qquad (3)$$

The value of $I_2(\Delta V_i)_{MAX}$ is a strong function of the common mode input voltage V_{cmi} and is very difficult to obtain analytically; therefore its exact evaluation should be left to computer simulation. $I_2(\Delta V_i)_{MAX}$ can, however, be approximated by the value of $I_2(\Delta V_i)$ at which the first one between M4 and M1 (depending on the value of V_{cmi}) is entering the linear region of operation. From this point on, in fact, I_2 can only increase by a relatively small amount. The largest value of $I_2(\Delta V_i)_{MAX}$ for a certain supply voltage V_{SS} is obtained when M4 and M1 enter the linear regin of operation simultaneusly. It can be shown that the value of V_{cmi} that corresponds to such an optimum situation (V_{cmi_0}) is approximately equal to $\dfrac{V_{SS}}{2} + V_{T1}$, where V_{T1} is the threshold voltage of transistor M1 (M2), and give rise to a maximum driving current of approximately

$$I_2(\Delta V_i)_{MAX} \approx \frac{1}{2} k' \left(\frac{Z}{L}\right)_9 (V_S - V_{TN})^2 \qquad (6)$$

where k' is the n -type transconductance parameter and V_{TN} is the n -type threshold voltage.

In the design reported here the above optimum bias condition was chosen. The corresponding peak current can be calculated from Eq. 6 for $V_{SS} = 5V$ and using the actual values of the device size together with the process parameters. This gives $I_2(\Delta V_i)_{MAX} = 90 \mu A$, which is approximately 45 times larger than the nominal stand-by current value. Such a current level corresponds to an input differential signal of approxilimately 800 mV which is smaller than the actual maximum value; this confirms that the limiting factor in achieving the largest possible driving is the value of the supply voltage. Notice that by chosing V_{cmi} to be equal to V_{cmo} i.e. $\dfrac{V_{SS}}{2}$, as it would be necessary the case if a single ended configuration was used, the maximum current becomes only about $25 \mu A$ which is almost 4 times smaller than in the previous case. These results agree fairly well with the simulation.

3.1.2. Dynamic Biasing

The calculation above has given the value of the peak input current. In order to have a fast step response, however, the amplifier must be able to deliver all of the this current to the output load. For this to occur the bottom current mirror, M9,M13, (or the top one for an input signal of the opposite sign) should maintain a gain of 1 up to $I_2(\Delta V_i)_{MAX}$ or, equivalently, M13 should stay in the saturation region up to such a current level. If this is not the case the output current limits before it reaches its peak value and the full advantage of class A/B operation is not exploited. The voltage level at the gate of M15 (V_{BIAS}) necessary for the above condition to be verified is much higher than the level required for proper operation at the quiescent current level.

This can be seen clearly from the plot of Fig. 4 where the output characteristics of transistor M13 are shown together with the load lines for two different values of V_{BIAS}; $(V_{GS} - V_T)_Q$ and $(V_{GS} - V_T)_{MAX}$ represent the quiescent and the maximum transient value of $(V_{GS} - V_T)$ of transistor M13. For a fixed voltage bias there is a trade-off between swing and current driving capability. In fact, as it is shown by curve a), to achieve maximum swing, M13 has to be biased at the edge of the linear region, i.e. $V_{DS} = V_{DS}^a$, in such a case, however, the maximum value of the output current, I_{MAX}^a, is only a few times the quiescent value, I_Q even for a very large value of $(V_{GS} - V_T)_{MAX}$. On the other hand, to obtain a very large value of the output current the bias condition shown by curve b) has to be chosen. In this case, however, the output swing is greatly reduced since $V_{DS}^b \gg V_{DS}^a$.

In a low voltage environment a large output swing is a primary goal in order to keep the dynamic range as high as possible. On the other hand for micropower application a large current driving capability is equally important to keep speed as high as possible.

An optimum load line for transistor M13 during transient condition is shown in Fig. 4 as curve c). In this case the peak driving current of curve b) (I_{MAX}^b) together with the drain-to-source voltage of curve a) (V_{DS}^a) is achieved. The bias voltage at the gate of device M15 that corresponds to curve c) is given in Eq. 7.

$$V_{BIAS} = V_{T\,15} + (V_{GS} - V_T)_{13} + (V_{GS} - V_T)_{15} = V_{T\,15} + \frac{8\,I\,(\Delta V_i)}{\mu\,C_o}(\frac{L}{Z})_{13} \quad (7)$$

where for simplicity it is assumed that M13 and M15 have the same aspect ratio and that the output voltage is such that M13 is in saturation

From Eq. 7 it is evident that, if body effects are neglected, V_{BIAS} can be generated by the simple circuit of Fig 5 , where M30 has an aspect ratio $(\frac{Z}{L})_{30} = \frac{1}{4}\,(\frac{Z}{L})_{13}$ provided that the current in M30 tracks the output current $I(V_i)$ during all transient. Since V_{BIAS} changes in response to variation of the current level the above scheme is called "dynamic biasing".

Fig. 6 is a detailed schematic of the main amplifier. On it is shown how the tracking current is generated. The current in each one of the two branches of the input structure is mirrored both from the top and from the bottom, therefore giving two perfectly matching currents one of which is sent directly to the output while the other is used to generate V_{BIAS}.

In the actual circuit the aspect ratio of the bias devices (M30,M40) is chosen to be smaller than the theoretical minimum given by Eq.7 The output devices (M15,M16) are therefore biased deeper into the saturation region than the theoretical minimum represented by curve c). This is done to guarantee a sufficiently large voltage gain even for relatively short channel devices and to compensate for the fact that, due to body effect, $(V_T)_{15} > (V_T)_{30}$. As a consequence, the output swing is slightly reduced, nevertheless the amplifier can swing to within .5 V from the supply rails while still maintaining a gain of over 83 db according to SPICE simulation. As a last point, notice that the frequency behavior of a dynamically biased cascode structure is practically identical to that of a fixed bias one.

The same kind of load line as curve c) could be obtained by using the high swing, high impedance current mirror shown in Fig 7 [21]. Such an approach requires less power and silicon area but is not feasible in a low-voltage environment.

3.2. Dynamic Behavior

The circuit considered here, like all the class A/B circuits, performs in a very non-linear fashion for large input signals due to the big excursion on the current level during transient. A closed form analysis is therefore very difficult, if not impossible, and will not be attempted here. Computer simulation can be used if a very accurate estimation of the time domain response of the circuit is required.

An approximate analysis is instead performed, where the non-linear circuit is simulated by a succession of linear ones whose operating conditions corresponds to those of the amplifier during the transient. Such an approach provides some interesting conclusion which are in qualitative agreement with the computer simulation.

During the transient the amplifier can be in one of two different regions of operation. In region 1 the input voltage is very small so that both signal paths are active while, in region 2 the input is large enough that one of the two paths is completely shut-off and the current level in the other one is equal to $I_1 \gg I_Q$.

The open-loop voltage gain in both regions of operations is given by:

$$A_v = gm_{eff} \, R_o \tag{8}$$

where gm_{eff} is the effective input to output transconductance of the amplifier and R_o is the output resistance. The exact value of gm_{eff} is quite complicated [18] however, to a good approximation:

$$gm_{eff} \approx \frac{gm_1 \, gm_4}{gm_1 + gm_4} + \frac{gm_2 \, gm_3}{gm_2 + gm_3} \quad in \ region \ 1 \tag{9}$$

$$gm_{eff} \approx \frac{gm_1 \, gm_4}{gm_1 + gm_4} \quad in \ region \ 2 \tag{10}$$

The output resistance R_o can be computed with the help of Fig. 8 where the voltages $V_{BIAS\,1}$ - $V_{BIAS\,4}$ are constant since in computing R_o the input is kept to a fixed voltage. $R_o = R_1 \, / \, / \, R_2$ in region 1 and $R_o = R_1$ in region 2 with

$$R_1 \approx gm_{16} \, r_{o\,14} \, r_{o\,16} \tag{11}$$

$$R_2 \approx gm_{15} \, r_{o\,13} \, r_{o\,15} \tag{12}$$

where r_{oi} is the output impedance of transistor i.

The operational amplifier dominant pole is

$$p_1 = \frac{1}{R_o \, C_L} \tag{13}$$

where C_L the total capacitance at the output node. For a single-pole roll-off, this gives a unity gain frequency ω_{unity}

$$\omega_{unity} = \frac{gm_{eff}}{C_L} \tag{14}$$

For a properly designed circuit, the second pole is associated with the current mirror (either the top or the bottom one) while the third one is associated with the cascode devices (M15 or M16).

Both the second and third pole can be expressed as follow;

$$\omega_{nd} \approx \frac{gm_i}{C_{paras}} \tag{15}$$

where gm_i is the transconductance of either the diode-connected device in the active current mirror (M9) or the cascode device (M15), and C_{paras} is the total parasitic capacitance at node B or C respectively which can, with good approximation, be considered independent of the current level since its main contribution comes from a gate capacitances.

The variation of the above quantities (gain, unity gain bandwidth, non-dominant pole frequency) during the transient can be represented by plotting their values as a function of the larger of the two input currents. This is done in Fig. 9 under the following basic assumptions.

All transistors are assumed to be in the strong inversion region, with the only possible exception of the input devices (M1-M8). The output impedance and the transconductance of an MOS device are assumed to vary with the current as follows [15,19];

$$g_m \propto \sqrt{I} \quad \text{in strong inversion}$$

$$g_m \propto I \quad \text{in weak inversion}$$

$$R_o \propto \frac{1}{I} \quad \text{in strong iversion}$$

Assuming a fix value of the quiescent current I_Q there are two possible situation that can occur depending on the size of the input devices. They are shown in Figs. 9 a and b. In the following I_{st} represents the value of the current level above which the input devices are operating in strong inversion.

Fig. 9a corresponds to the case of using very large input devices so that $I_{st} > 4 I_Q$. In Fig. 9b the input devices are assumed to be small enough to guarantee that they are biased in strong inversion for $I = I_Q$. In both cases during the transient the current level goes from its quiescent value to its peak value I_{MAX} and back again to I_Q due to the action of the feedback loop. As a consequence the value of ω_{unity} during transient is always larger than in stand-by while A_V is always smaller. Such a behavior is particularly favorable for S.C. applications; in fact during the transient the speed is enhanced, while the temporary loss of gain is of no consequence since a large gain is only important at the end of the clock cycle. On the other hand the relative position of ω_{unity} and ω_{nd} during the transient behave differently for the two cases considered. For the case of Fig. 9a ω_{unity} and ω_{nd} are changing in such a way that the margin of stability present at the stand by current level is not preserved during the transient. As a consequence, to avoid instability or excessive ringing, the amplifier may need to be overcompensated with a consequent overall speed loss.

For the case of Fig. 9b the relative position of ω_{unity} and ω_{nd} is now changing in the opposite direction, therefore no stability problems occur if stability is guaranteed at the quiescent current level. The maximum input device size for which the stability margin does not degrade during the transient corresponds to the condition $I_Q = \frac{1}{4} I_{st}$.

As a consequence of the behavior outlined above the size of the input devices cannot exceed some maximum value or the amplifier speed will be compromised and eventually ins-

tability can occur. On the other hand most of the ac characteristics of the op. amp. improve by increasing the size of the input devices. This can be seen with the help of Fig. 10, which shows the qualitative behavior of the gain, the unity gain frequency, and of both the $\frac{1}{f}$ and white noise as a function of the input device size for a fixed value of I_Q. From this plot, it is clear that an optimum performance is achieved when the input devices are in the subthreshold region. Furthermore, to reduce the $\frac{1}{f}$ noise the input device size should be increased as much as possible [22].

The size of the input devices(M1,M8) also affects the frequency behavior of the input cross coupled structure. It can be shown, in fact, that such a structure contributes a pole zero doublet with about 50% separation located in the proximity of the f_T of the devices comprising it. In the subthreshold region for an MOS transistor of length L and width W with constant current level, f_T is proportional to $\frac{1}{W\,L}$. Therefore by increasing W the frequency of the doublet is rapidly reduced until it becomes smaller than ω_{unity}. From this point on the settling time of the amplifier begins to be degraded. If speed is a primary concern the value of W should be constrained in order to guarantee that the doublet is outside of the passband. Such a limit can be more or less stringent than the one related to the transient behavior of the op. amp. depending on the size of the load capacitor.

The combination of all the above constraints give rise to an optimum size for the input devices that depends on both the size of the load capacitance and the value of I_Q; their exact value can, however, be found only by computer simulation. In practice when the current level is fairly high and/or C_L is fairly small, it is impossible to sufficiently increase W to bring the input devices into subthreshold while still guaranteeing stability; therefore the optimum condition cannot be reached. In the design reported here the current level necessary to fulfill the speed requirement is low enough that the optimum condition can be closely approached, in fact the input devices are biased just below threshold, i.e. $I_Q \approx \frac{1}{2} I_{st}$.

3.2.1. Noise

The noise performance of the amplifier is of particular concern for two reason. First, low voltage supply implies a small voltage swing and therefore a lower dynamic range for a given noise level. Second, low power consumption implies larger noise since the white noise is inversely proportional to the input devices transconductance; this again degrades the dynamic range of the amplifier all else being constant.

As was pointed out before, increasing the size of the input devices reduces both the $\frac{1}{f}$ and the wide band noise. However, two more factors are to be considered if an optimum noise performances is sought.

First, the input structure has to be as simple as possible; second the input referred noise due to all the devices other than the input ones should be made as small as possible (ideally negligible).

In this design the input structure (M1-M8) is much more complicated than the classical source-coupled pair (8 devices instead of 2). However, it can be easily shown that the noise power associated with each of the 8 input devices should be divided by 4 when referred back to the input node. The intuitive reason for this is that the noise generated by each one of M1-M8 propagates only through one of the two signal paths while the input signal propagates through both.

The overall input referred noise produced by M1-M8 is therefore equivalent to that of one n plus one p device which is comparable to that of an source-coupled pair.

To analyze the noise contributed by the rest of the circuit the entire fully differential structure must be considered (Fig. 6). The only devices that contribute appreciable noise, besides M1-M8, are M19, M24, M20, M23, M9, M11, M10, M12, M60a, M60b and those associated with common mode feed-back structure which will be, however, considered later.

It can easily be shown that the contribution of M60a,b can be made negligibly small by sufficiently increasing their channel length with respect to that of M1-M8 [22]. The situation

is not quite as simple for the other 8 transistors and will be analyzed in more detail.

First notice that, similar to the input devices, they only affect one signal path and therefore their noise power contribution should be divided by 4 when referred back to the input. This is not the case if the amplifier is operated single ended. Furthermore the ratio of the noise power contributed by one of these devices and that of an input transistor is inversely proportional to the ratio of their transconductances for the white component and inversely proportional to the ratio of their channel lengths to the square for the $\frac{1}{f}$ component [22].

In order to simultaneously reduce both kinds of noise the channel length of the current mirror devices should be made as long as possible. This also has a beneficial effect on the voltage gain. On the other hand the frequency of the first non dominant pole is proportional to $L^{-\frac{3}{2}}$ where L is the channel length of the current mirror transistors. As a consequence there is a trade-off between noise and gain, on one side, and speed on the other.

Fortunately for the designer, while p-type transistors, are slower than their n counterpart, given the same size, they also contribute less noise to the system both because they are intrinsically less noisy [15] and because they have a smaller transconductance. As a consequence their channel lengths can be chosen to be much shorter than that of the n ones. Taking advantage of such a favorable situation the noise contributed by all current mirror devices can be reduced to a smaller fraction of the total (about 15% for both $\frac{1}{f}$ and white noise), while at the same time keeping the frequency of the second pole within 40% of the maximum achievable value (all minimum length devices) with the maximum output swing kept as a constant. It is interesting to note that, in order to achieve such a result the device length has to be chosen in such a way that the n type current mirrors are slower than the p ones.

As a final point notice that since the cascode devices, M15,M16, give a totally negligible noise contribution to the system their channel length can be made very short (consistently with the gain requirement) thereby improving the frequency response.

3.3. Common Mode Feedback Circuit

In a fully differential configuration no common-mode feedback path capable of stabilizing the common-mode value of the internal nodes exists at the system level. As a consequence each op. amp. has to be surrounded by a specialized circuit which performs the above function. The need for a common-mode feedback circuit (CMFBC) is by far the most important draw-back inherent in a fully differential approach. Besides requiring extra area and power, the CMFBC typically limits the output swing, increases the noise, and slows down the op. amp. All of the above negative effects become particularly undesirable in a low-voltage, low-power system.

For all of the different CMFBC configurations proposed to date a large power consumption is almost an intrinsic necessity due to the need of having devices that behave linearly over large voltage excursions. An alternative approach suitable for sampled data systems was proposed by Senderowicz et al [3] and is adopted in this design.

The conceptual schematic representation of the circuit is shown in Fig. 11. M4, M5, and M6, are identical devices and therefore they carry the same current I; M1, M2, and M3, are also identical. At the beginning let us suppose that switches Ma, Mb, Mc, and Md are open. To analyze the behavior of the circuit the feedback loop is broken by assuming that the drains of M1 and M2 are disconnected from the output nodes and the loop gain is computed. The ac voltage at node A (V_A) as a function of the two output voltages V_{o1} and V_{o2} is given by

$$V_A = V_{o1} \frac{C_1}{C_1 + C_2 + C_p} + V_{o2} \frac{C_2}{C_1 + C_2 + C_p} \tag{16}$$

where C_1 and C_2 are the two common-mode feedback capacitances and C_p is the total parasitic at node A. From Eq. 16 it follows that if C_1 and C_2 are perfectly matched and $C_p \ll C_1 + C_2$ the common-mode portion of the output signal is transmitted to node A unchanged while the differential portion has no effect on V_A. From node V_A to the common mode output there is a negative gain whose amplitude is comparable to the forward gain of the amplifier. On the other hand the gain from node V_A to the differential output is

ideally zero. The loop gain is therefore very large and negative for any common mode signal while is extremely small (zero for perfectly matched devices) for any differential signal. This implies that the common-mode output voltage is kept at an almost constant value even in the presence of some common-mode output signal and at the same time the op. amp. differential gain is totally uneffected. The DC value of the common-mode output voltage is, however, not well defined depending only (if no leakage on the capacitor is assumed) on the initial voltage across C_1 and C_2. The purpose of C_{1a} and C_{2a} is to establish the voltage drop across C_1 and C_2 that gives the desired common-mode output and to periodically restore it to compensate for leakages. In a S.C. application C_{1a} and C_{2a} are switched in opposition of phase with the input signal therefore not interfering with the normal operation of the filter. This CMFBC is particularly suited for low voltage low power applications for two main reasons. First it does not require any extra power consumption, with the exception of the replica circuit that defines the proper value of V_A (M3, I, and M6) which can, however, be shared among all of the op. amps. in the system. Second, it does not degrade the differential output swing since the level shift operation performed by the capacitor C_1 and C_2 is not limited by the voltage supplies.

There is, however, a trade-off between the minimum noise and the maximum speed achievable. In fact, in order to increase the unity gain frequency of the CMFBC the transconductance of M1 and M2 should be increased which, in turn, introduces more noise (particularly white noise). As a consequence a compromise between noise and speed must be reached.

As shown in Fig. 11 the top current sources (M4 and M5) are realized with p -type transistors, while the feedback devices M1 and M2 are n types. This gives a slightly higher noise contribution than the dual configuration, but has another advantage which is very important in micropower applications as explained below.

Due to the very small value of the current supplied by M4 and M5, if no precaution is taken, the output common-mode voltage may enter a slewing mode during the transient and the speed of the CMFBC can be severely degraded. The reason for this is that, due to the

different delay associated with the p and n section of the circuit during the transient some common-mode signal is appearing at the output even for a purely differential input. The CMFBC must be able to restore the proper common-mode output value within one clock phase. While the maximum current that the CMFBC can supply is quite large for a positive signal, is limited to 2I (about $2\mu A$ in this design) in the opposite direction. This implies that the speed of response may be inadequate for the case of a negative common mode output transient. One solution to this problem is to guarantee that the polarity of the transient common-mode output signal is always positive which can by done by ensuring that the p type current mirror is faster than its n type counterpart. It turns out that, as explained before, due to noise considerations the sizes of the devices are chosen in such a way that the above condition is verified. A second solution, probably more efficient, which however is more complicated, is to operate the CMFBC in class A/B [18].

4. EXPERIMENTAL RESULTS

The feasibility of the techniques discussed above for low-voltage S.C. applications was tested via a classic PCM transmit filter. Such a filter realizes a five-pole, four-zero transfer function which has been shown to satisfy the stringent D-3 channel filter specification. Two experimental prototype chips where fabricated using two different CMOS technologies. Similar performance for both the amplifier and the filter were obtained in the two cases. For the sake of simplicity only one set of results will be reported here.

A microphotograph of the entire chip is shown in Fig. 12. In a $5\mu m$ technology the active area occupied by the filter is approximately 54 X 72 mils. Some of the measured op. amp. characteristics are listed in Table 1 for a nominal supply voltage of 5 V and for a power dissipation of $90\mu W$. The amplifier layout is almost perfectly symmetrical in order to guarantee exact cancellation of the spurious signals coupled into the system. Some small asymmetries were impossible to avoid (cross-coupled devices), but they were all limited to the metal layer. The power level in both the filter and the amplifier can be externally controlled. Fig 13 shows a detailed plot of the filter passband for different values of the total power dissi-

...pation. For very-low current level the amplifier speed is reduced and peaking occurs at the band edge, on the other hand when the current becomes too high the gain is reduced and drooping occurs. Nevertheless the filter meets the channel filter requirements over a 25 to 1 change in the current level. The absolute minimum power required to stay within specs is about $350\mu W$ which corresponds to about $70\mu W$ per op amp. At the nominal value of $0.5mW$ total power dissipation the pass-band ripple is approximately 0.12 db. A coarse filter response is shown in Fig 13. The transmission zeros are at 4.5 kHz and 6.7 kHz respectively and the stop band attenuation is always more than 34 db. All of the above data agree well with the simulated results obtained from the program DIANA [24]. The behavior of both the passband and the overall response corresponding to a variation of $\pm 10\%$ in the supply voltage is shown in Fig 14. As it can be seen the largest variation occurs at the bandedge peak, which is typically the most sensitive point, and is about ± 0.01 db. Notice that on the coarse plot of Fig. 14b no appreciable variation can be detected even in correspondence of the transmission zeros.

The power supply rejection as a function of frequency in the range from zero to 6 kHz for both positive and negative supply is illustrated by Fig. 15a. As can be seen better than 50 db rejection at 1 kHz is achieved in both cases. Furthermore, as it can be seen from Fig 15b, the rejection is always more than 30 db up to very high frequency. In Fig. 16 the negative power supply rejection ratios for both single ended and fully differential output are shown simultaneusly for purpose of comparison. Fig. 16 shows that an improvement of 15 to 30 db is obtained by using a fully differential configuration (similar results are obtained for the positive supply).

The input referred noise spectrum is shown in Fig. 17 together with the filter frequency response. The total C-message weighted integrated noise is $65\mu V$. Such a moderately low value, particularly considering the low power consumption, was achieved because of the careful choice of the devices sizes as was explained in the previous section.

· The total harmonic distortion for a 2 Volt rms differential output at 1 kHz is about -73 db. The good linearity of the filter is further shown in Fig. 18 where the total harmonic distortion (THD) for the nominal supply voltage of 5 Volts and a 1 kHz input signal is plotted versus the output signal amplitude. From Fig. 18 it can be seen that the THD stays below -40 db up to a differential output of approximately 4.6 Volts peak (3.3 V rms) i.e. 200 mV from both supply rails. The above result combined with above value of the C-message weighted noise gives a dynamic range of approximately 93 db which is comparable with the value achieved by typical commercially manufactured filters operated from ±5 *Volts* supplies and consuming 10 to 15 times more power.

The large output swing is primarely due to the use of dynamic biasing for the cascode devices and to the fact that the CMFB circuit behave linearly even for signals which are larger than the supplies. The very linear CMFB circuit also partially explains the low distortion value achieved in the filter. Other factors are, however, also important in improving the filter linearity. In particular, for relatively small signals (more than 1 V from the supplies), the fully differential structure has a primary effect in reducing the THD. This is shown quantitatively in Fig. 19 where the harmonic content present at the output for a relatively small signal (4.4 V p-p differential output) of frequency equal to 1 kHz is shown for both the single ended and the fully differential configuration. Notice that for ease of comparison the signals in the two cases have been scaled to give the same peak value for the fondamentals. As expected in going from single ended to fully differential the even harmonics cancel out while the odd ones are slightly increased (ideally by 6 db). However, if for the single ended output the second harmonic is dominant, as it is the case for a relatively small signal, then the fully differential configuration will give a lower THD. For the case of Fig. 19 the THD is reduced by approximately 12 db (from -68 db to -80 db) by using fully differential topology. The above effect, however, is not as substantial when the amplitude of the signal approaches the supply voltage. This is shown in Fig. 20 where the same situation as in Fig. 19 is shown with the difference that now a 8.4 p-p differential output voltage is used. In this case for the single ended topology the second and third harmonics are comparable in amplitude therefore

the improvement associated with the fully differential topology is less than 6 db. Nonetheless it is interesting to notice how the second harmonic is reduced by more than 20 db which demonstrates the good matching of the two signal paths. The clock feed-through for the single ended and fully differential case was also measured for comparison. For grounded inputs, which give perfectly matched signal paths the fully-differential case shows an improvement (reduction) of more than 30 db. All of the above results are summarized in Table 2.

Since lower and lower supply voltages are expected to be used in future scaled technologies it is important to reduce the minimum value of the total supply voltage required for proper operation. For the filter reported in this paper which was fabricated in a conventional (not scaled) process featuring approximately $\pm .8\ V$ thresholds such a minimum value was approximately 3 V i.e. either a single 3 V buttery or a $\pm 1.6\ V$ supply. Notice that a smaller value could be obtained if a low threshold process had been used since the limiting factor in this case is given by the voltage drop across the two diode connected devices present in each of the input bias branches (transistors M5,M7 and M2,M4). Finally to test the op. amp. speed at different current levels the clock rate was increased from its nominal value (128 kHz) and the current required to achieve a proper filter response was recorded. The results of such test are depicted in Fig. 21. Notice that, as expected, for low values of the current level the input devices are operated in subthreshold and the op amp unit gain bandwidth (and therefore its speed for small input signals) is proportional to the current level. On the other hand for larger current the input devices are in strong inversion and the speed becomes proportional to the square root of the current. Notice also that, although the op amp was not intended for high speed applications, by simply increasing its current level it can properly function up to clock rates in the 2 MHz range. At such speed the available time for settling is as low as 200 nSec and the required power consumption becomes approximately 17 mW per op amp.

FIGURE CAPTIONS

Fig. 1 Fully Differential S.C. Integrator

Fig. 2 Output Voltage Waveform for the Circuit of Fig. 1

Fig. 3 Simplified Schematic of the Forward Core Amplifier

Fig. 4 Different Load Lines for the Cascode Devices

Fig. 5 Circuit to Generate the Dynamic Bias Voltage

Fig. 6 Detailed Schematic od the Forward Core Amplifier

Fig. 7 High Swing Current Mirror

Fig. 8 Circuit to Compute the Output Impedence of the Amplifier

Fig. 9 Variation of the Op. Amp. Gain, Unity Gain Frequency, and Non Dominant Pole Position as a Function of the Current Level for Different Input devices Size.

Fig. 10 Variation of the Op. Amp. Gain, Unity Gain Frequency, White Noise, and $\frac{1}{f}$ Noise as a Function of the Input Devices Size.

Fig 11 Simplified Dynamic Common Mode Feedback Circuit

Fig 12 Chip Microphotograph

Fig 13 a) Detailed Passband response for Different Current Levels b) Coarse Frequency Response of the Filter.

Fig. 14 Changes in the a) Passband Response and b) in the overall Filter Response for ± 10% variation in the Supply Voltage.

Fig. 15 Positive and Negative PSRR a) in the 0-6 KHz range and b) in the 1-100 kHz range.

Fig. 16 Single-Ended and Fully-Differential PSRR a) in the 0-6 kHz and b) 1-100 kHz Frequency range.

Fig. 17 Filter output Noise.

Fig. 18 Total Harmonic Distortion as a Function of the Output Voltage

Fig. 19 Comparison Between the Harmonic Distortion for a Fully- Differential and a Single-Ended Output for a differential output voltage of 4.4 p-p V.

Fig. 20 Comparison Between the Harmonic Distortion for a Fully- Differential and a Single-Ended Output for a differential output voltage for a 8.4 p-p V.

Fig. 21 Maximum Clock Frequency Versus Required Supply Current.

Table 1 Amplifier Specifications.

Table 2 Summary of the Filter Performance.

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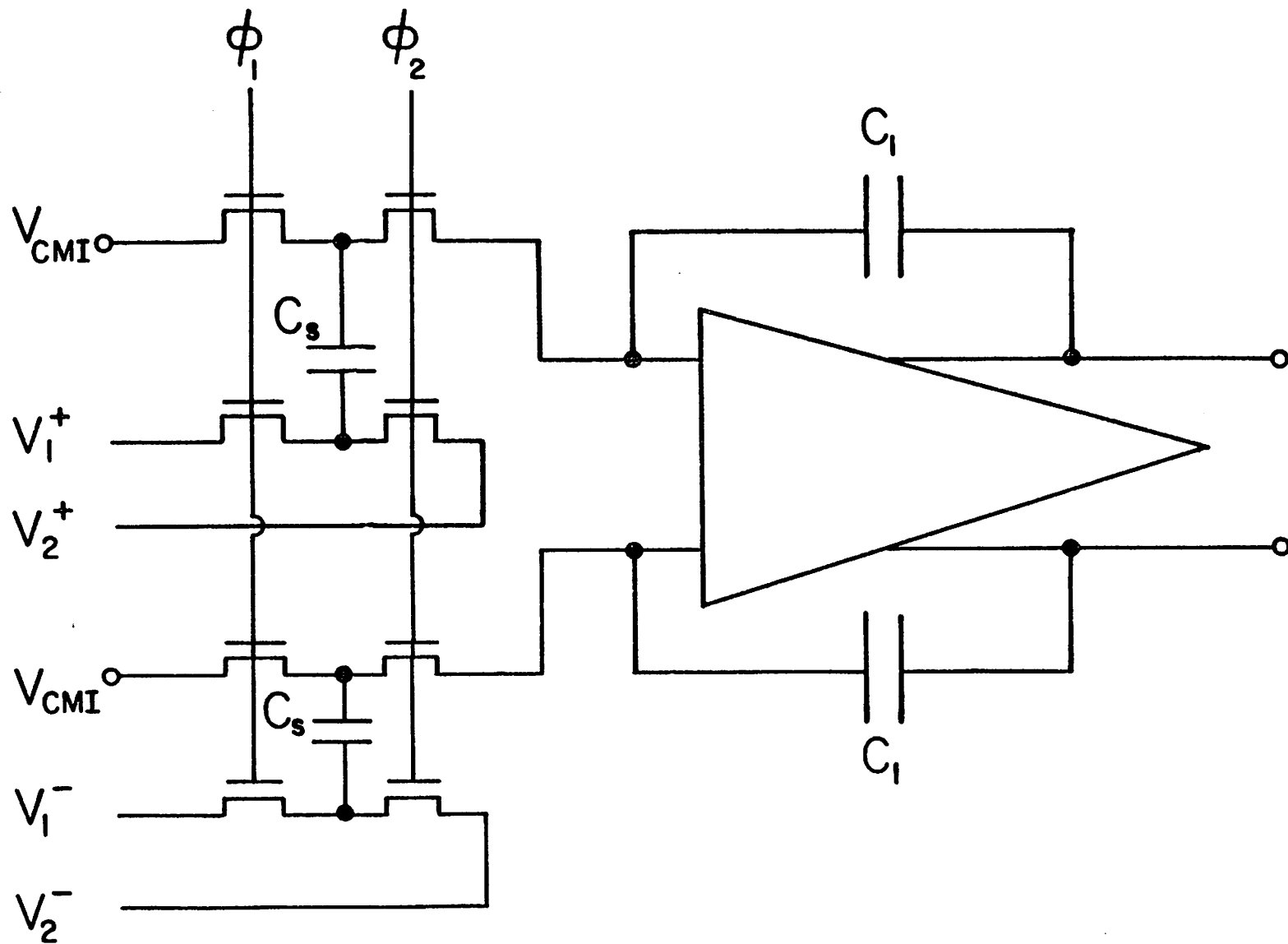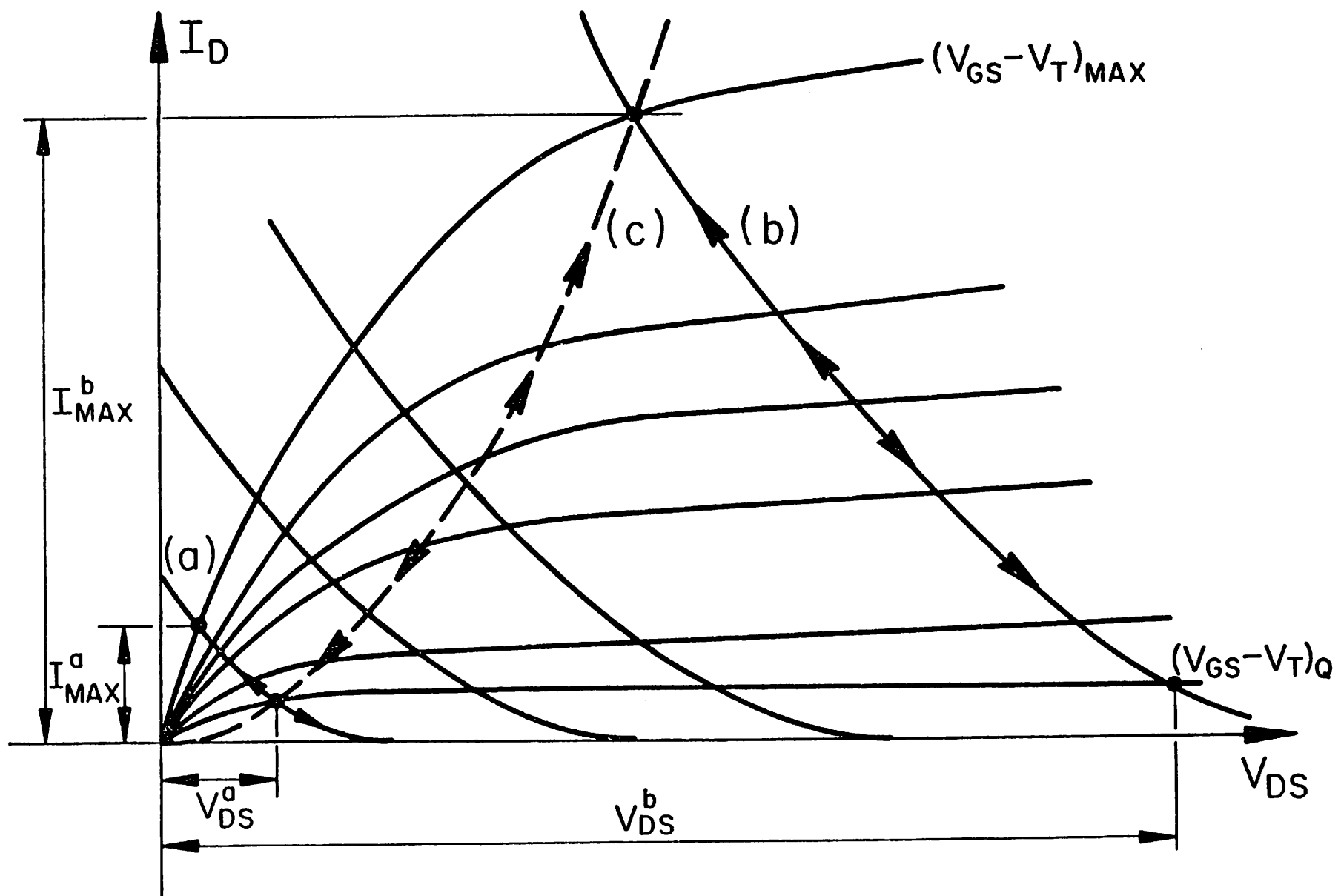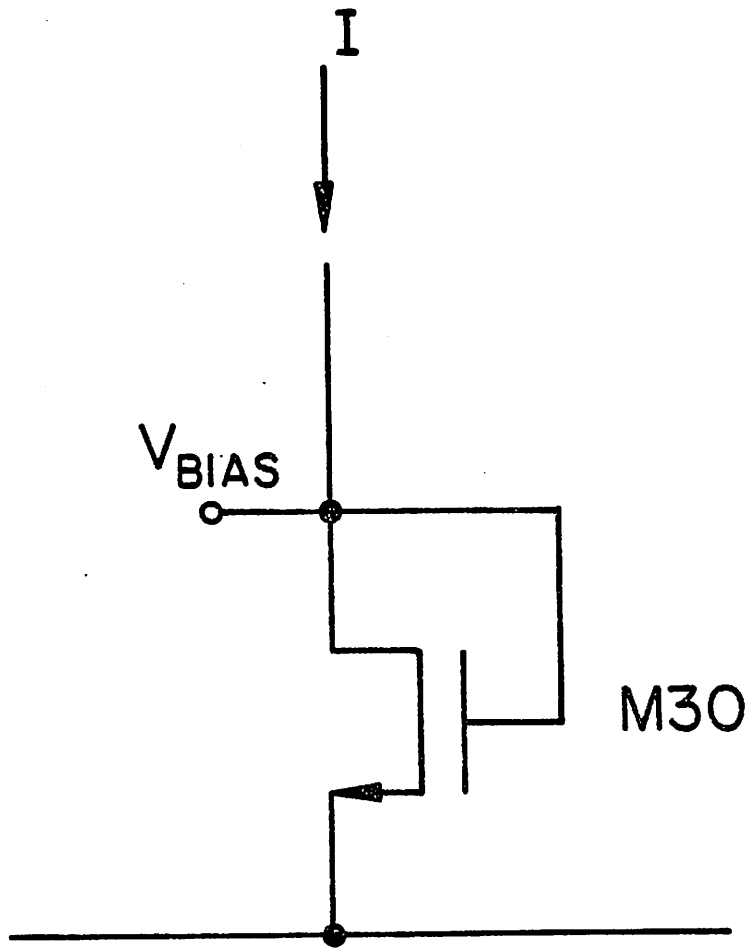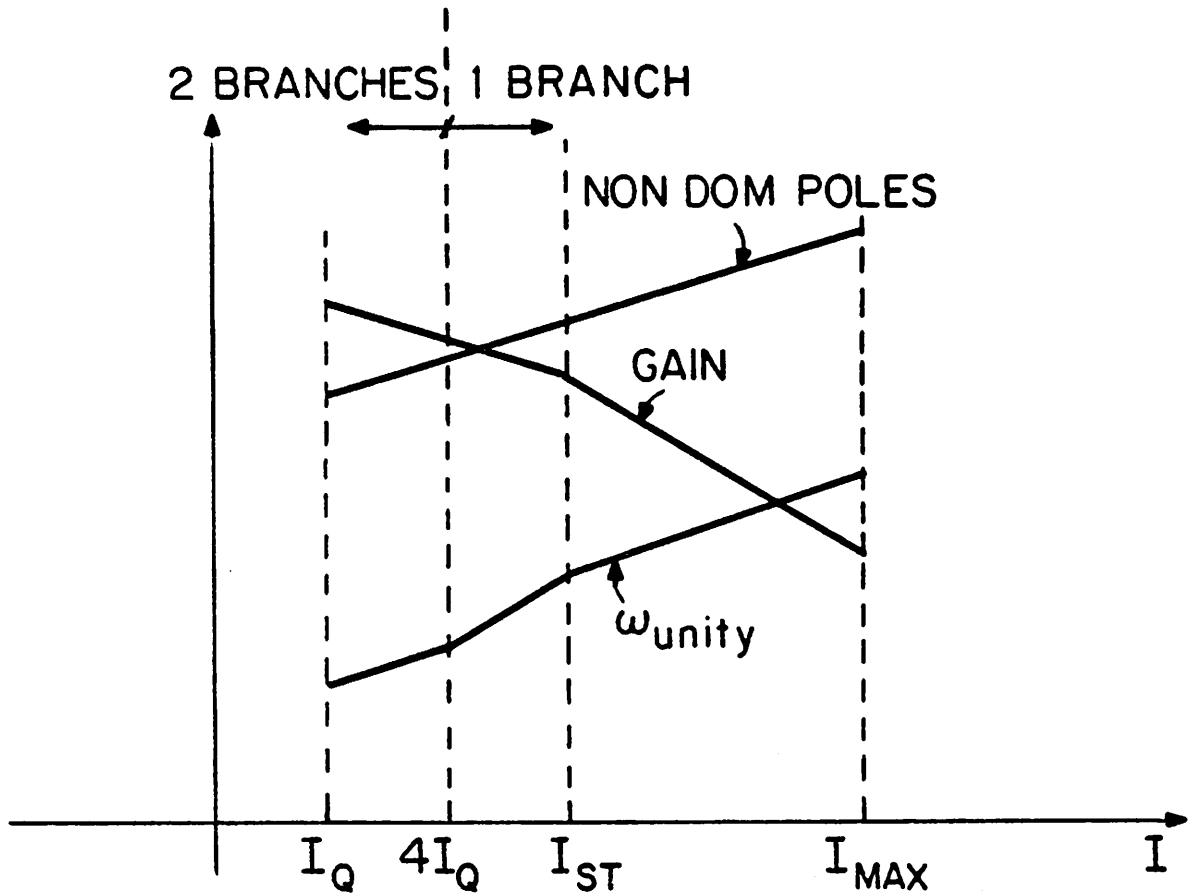
Fig. 1

Fig. 2

Fig. 3

Fig. 4

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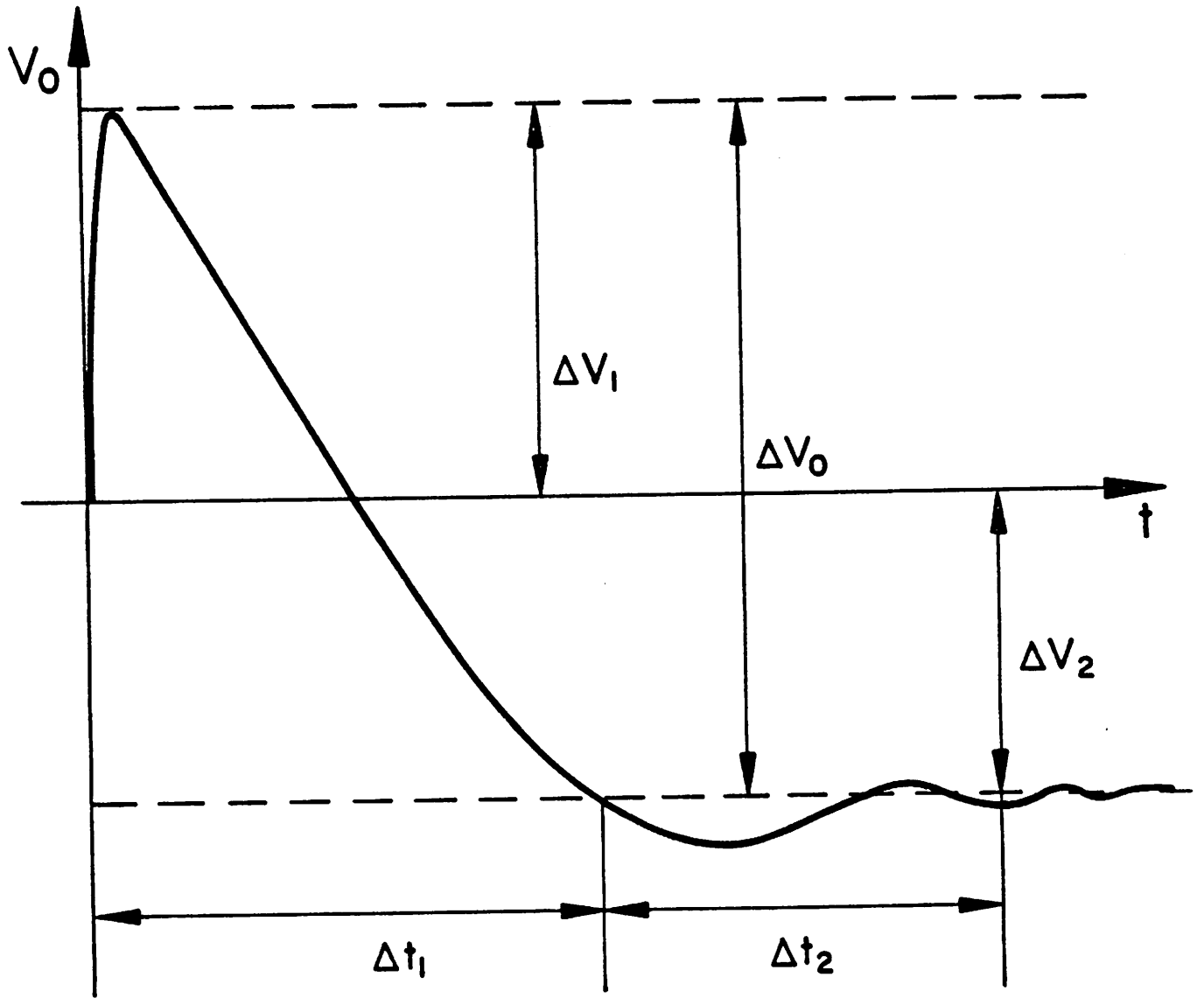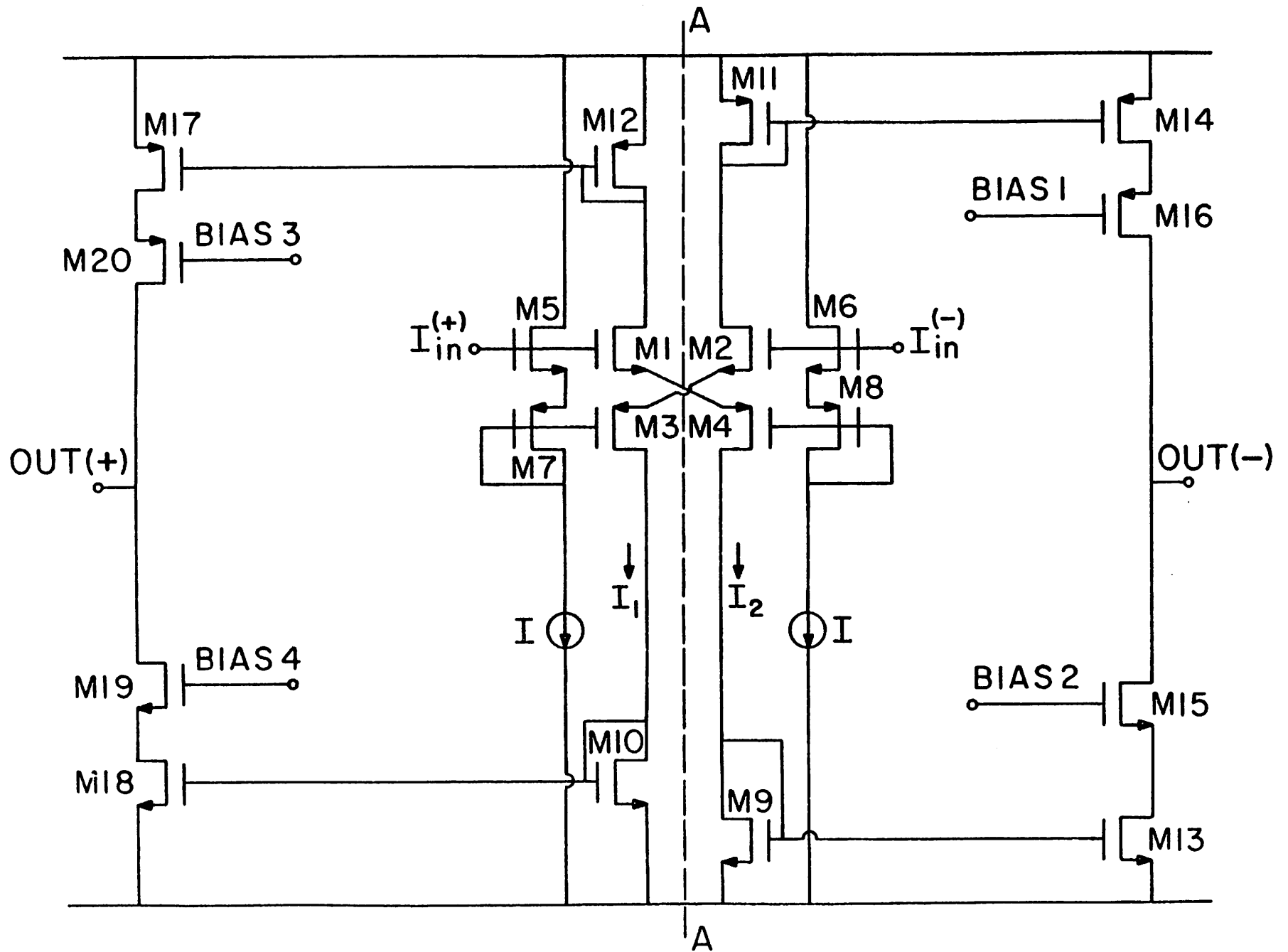
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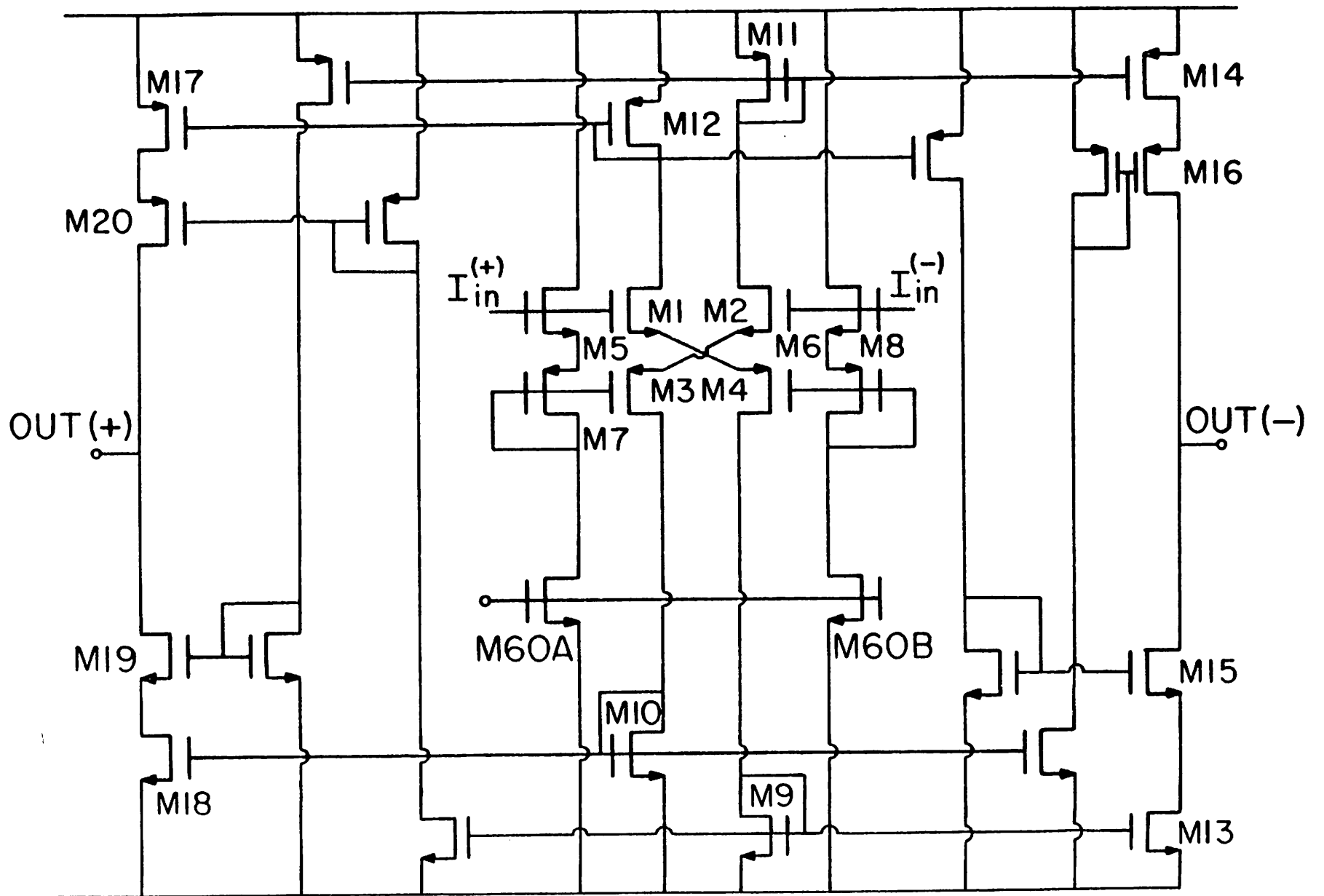
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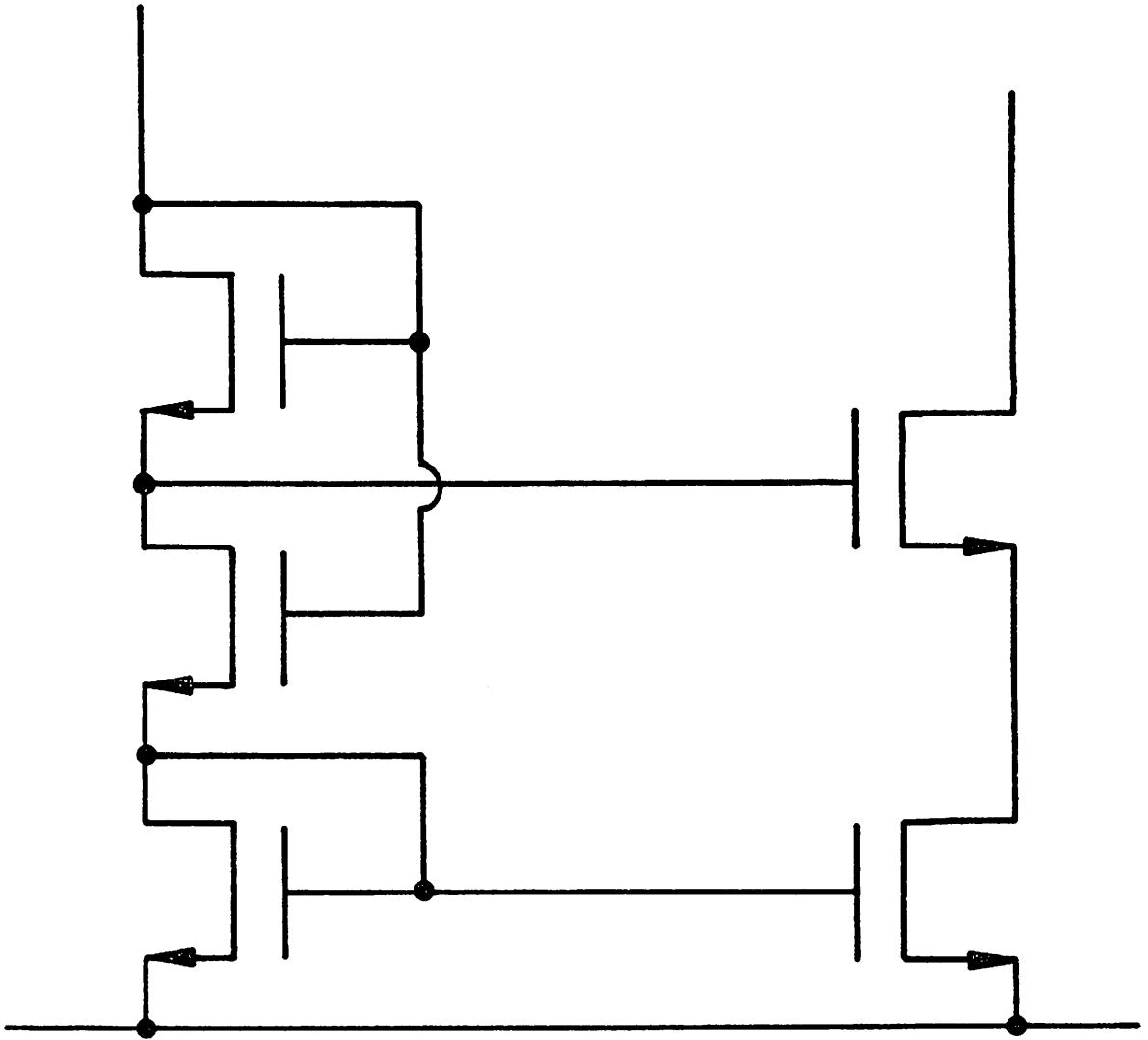
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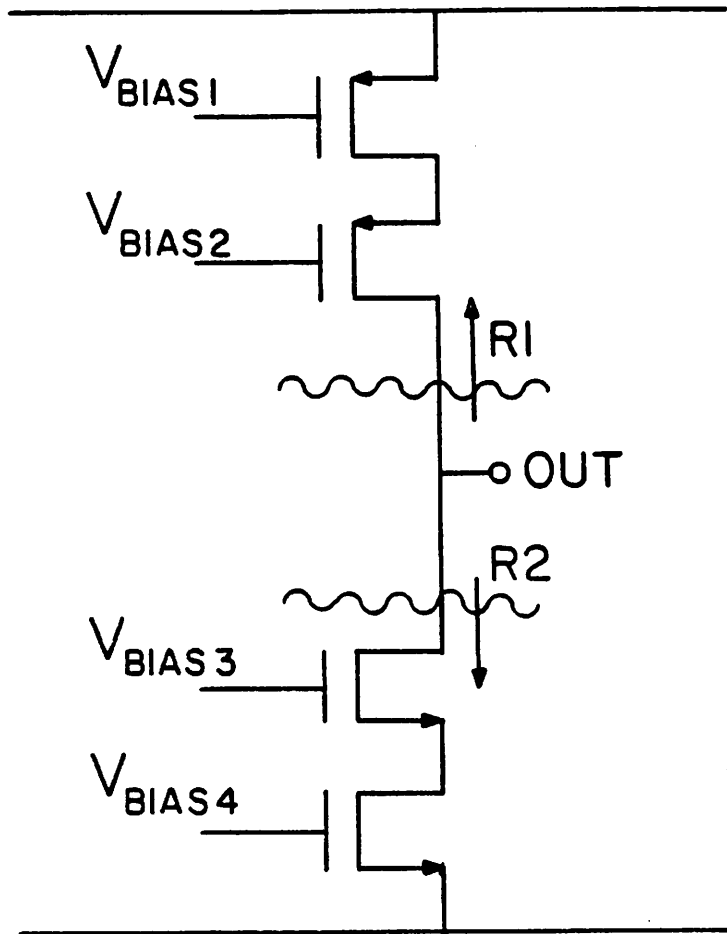
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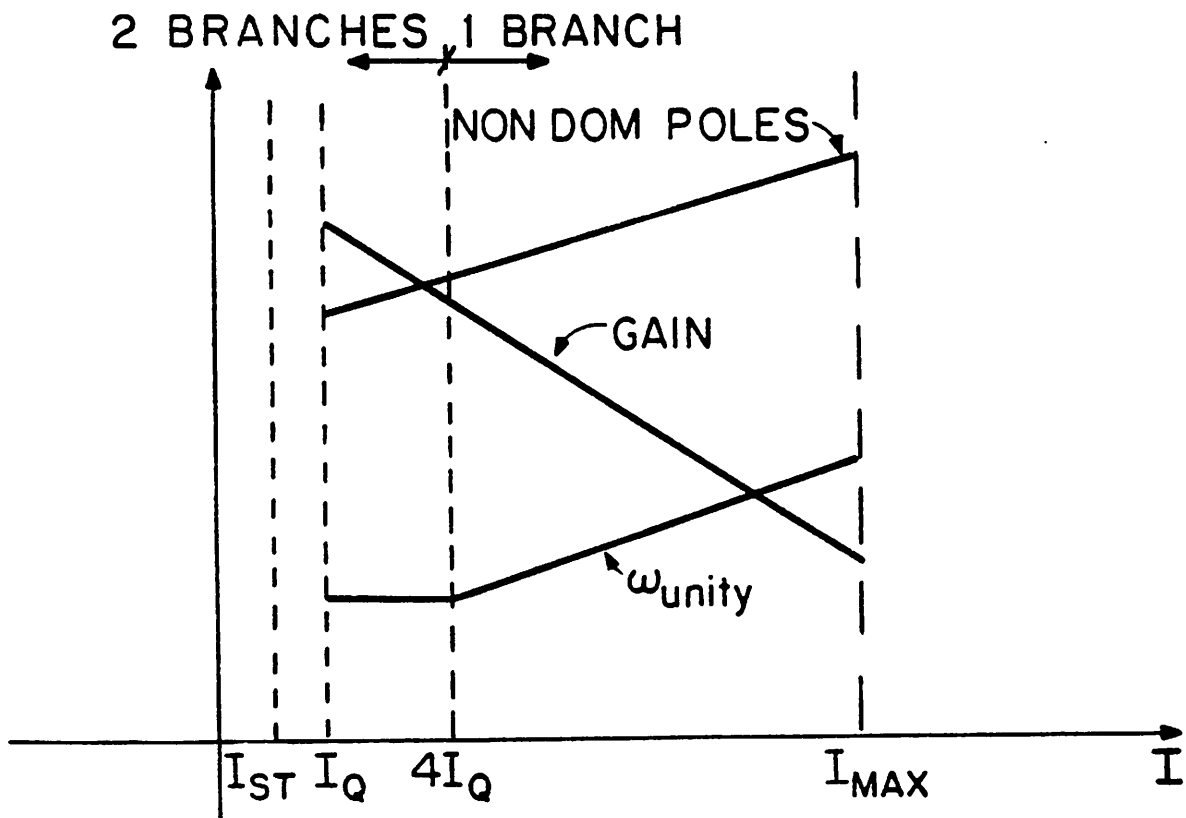
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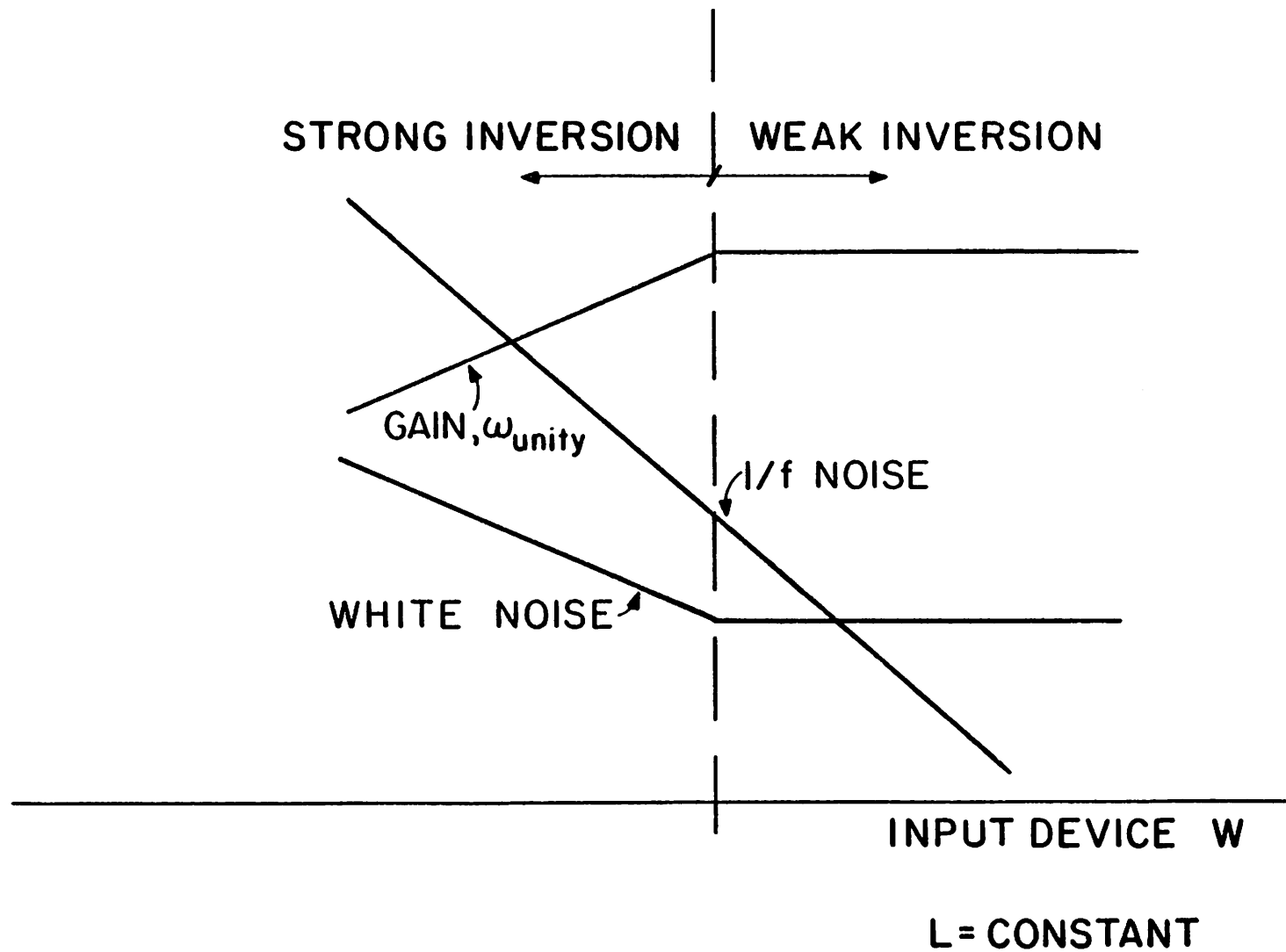
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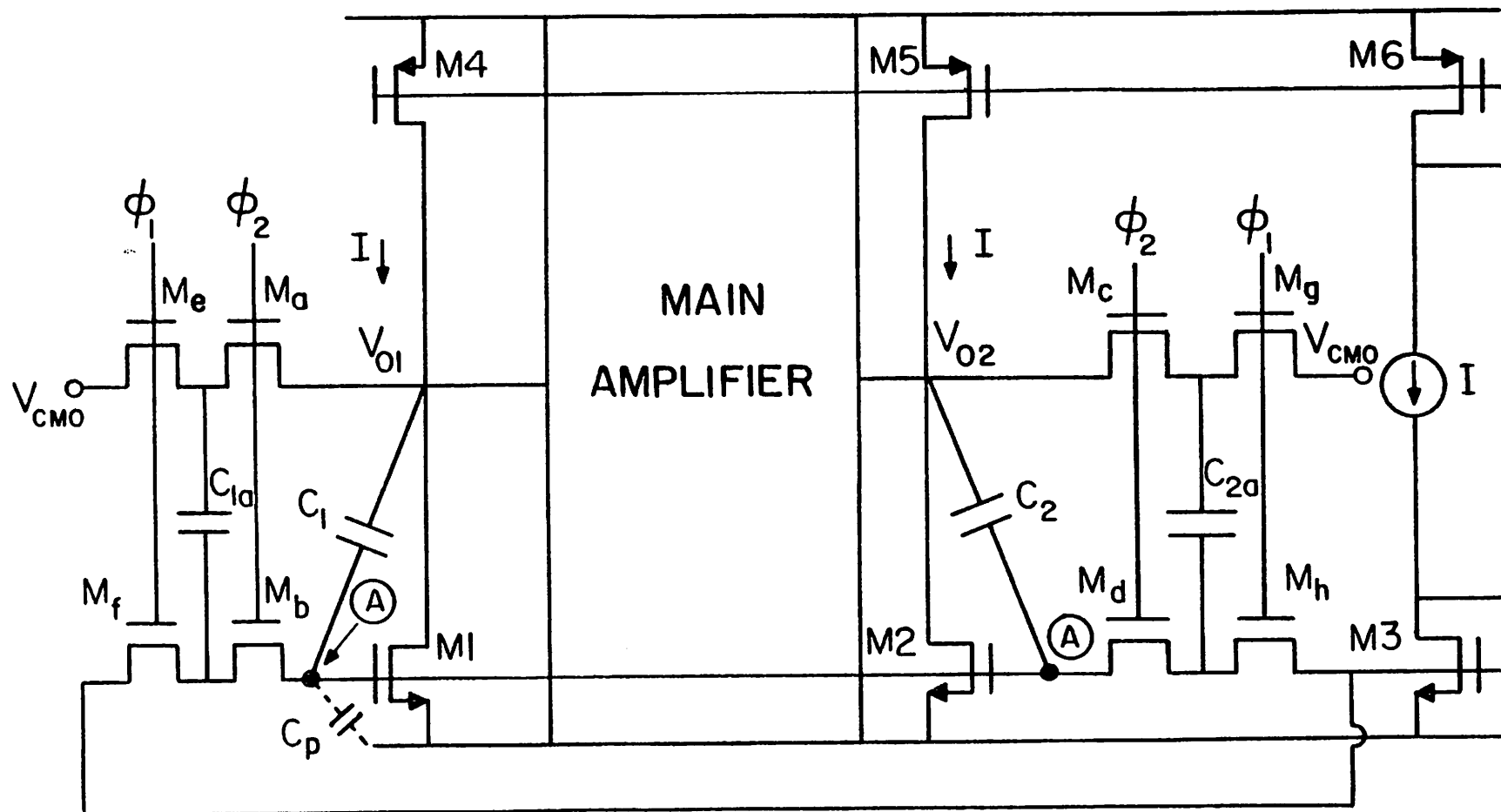
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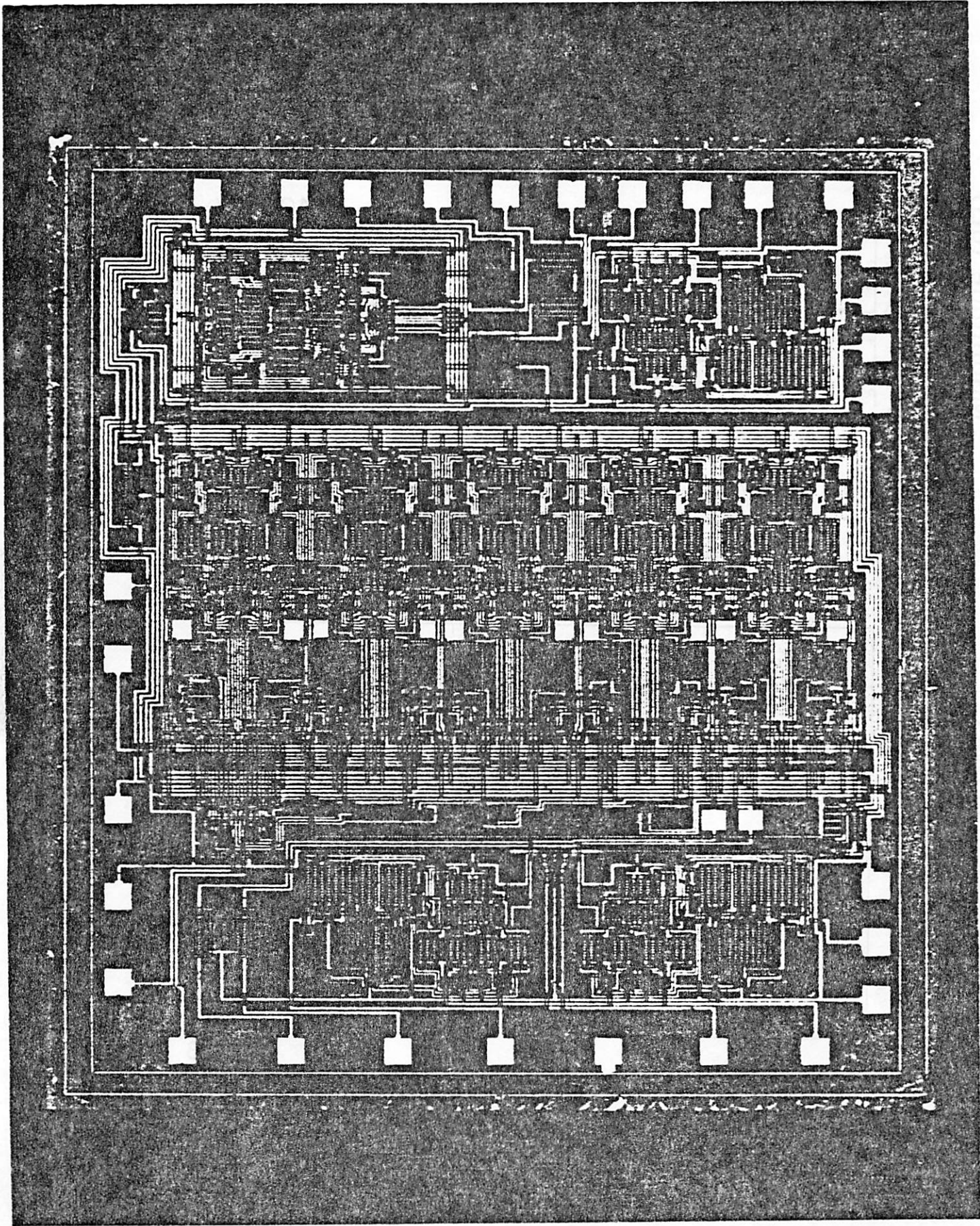
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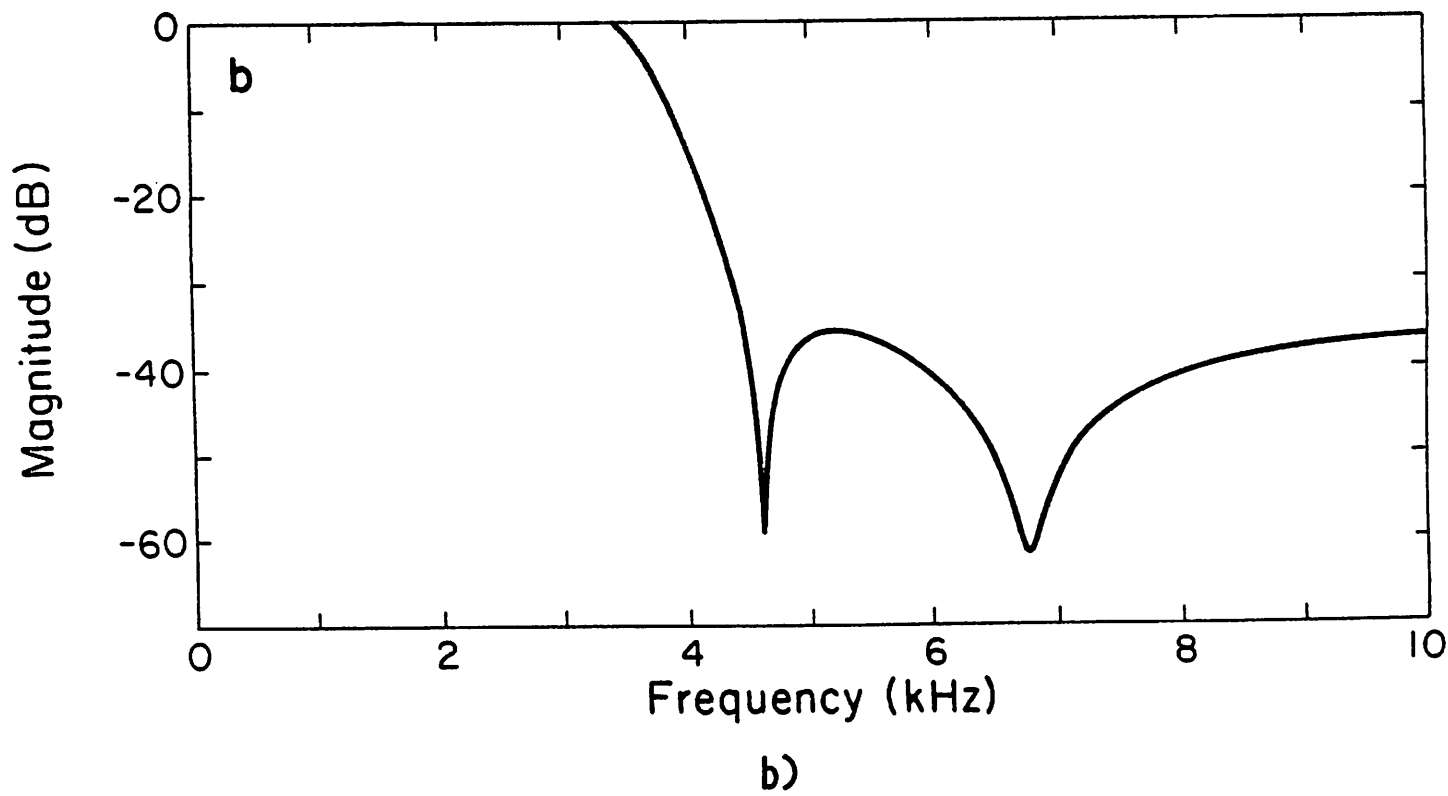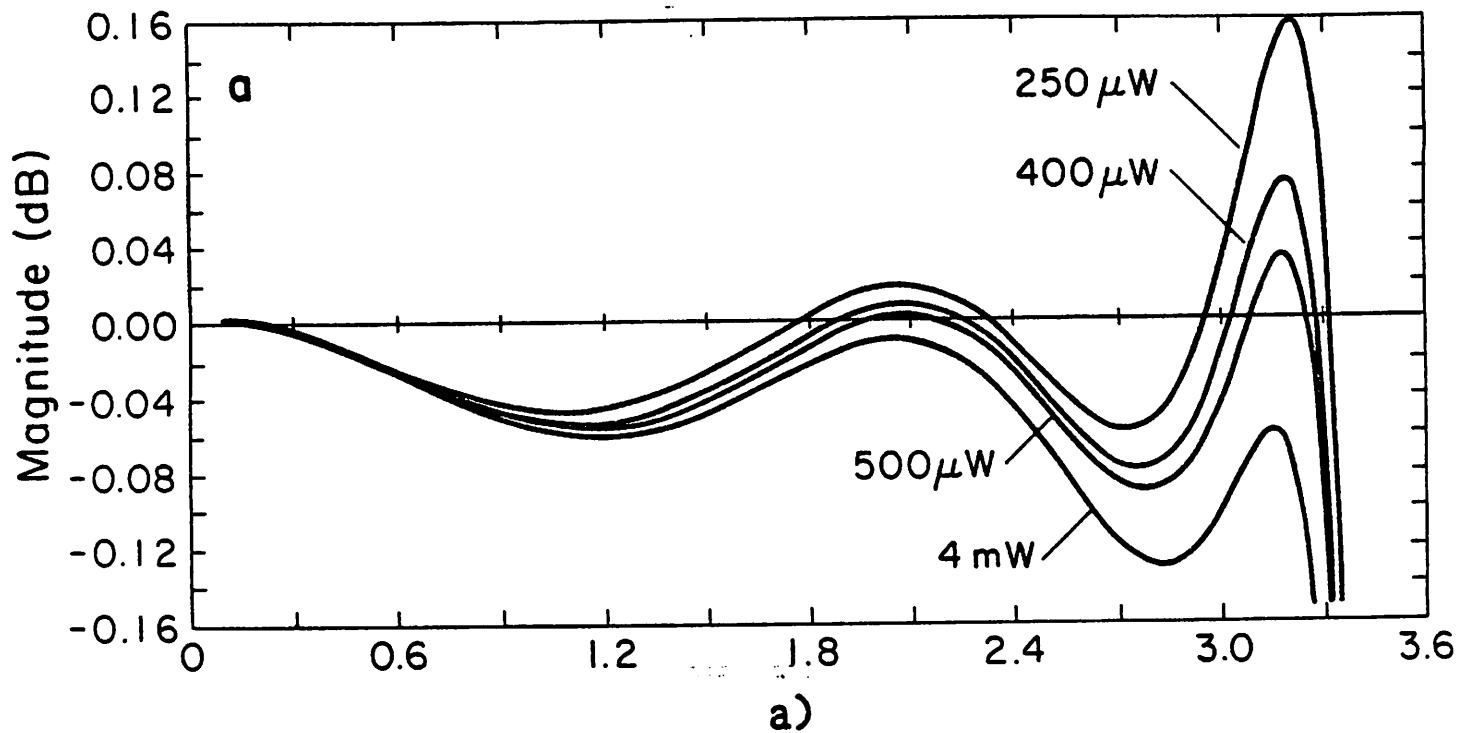
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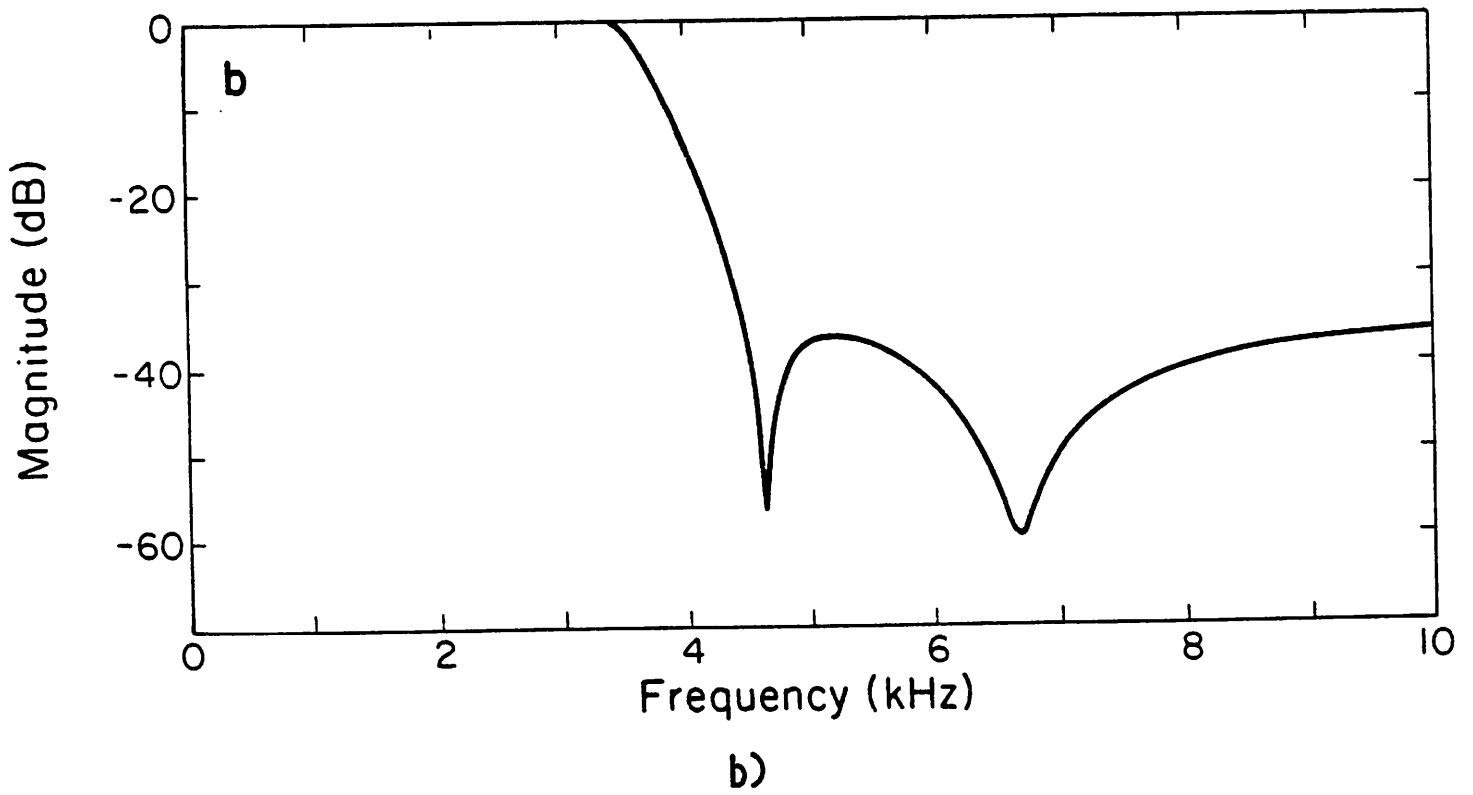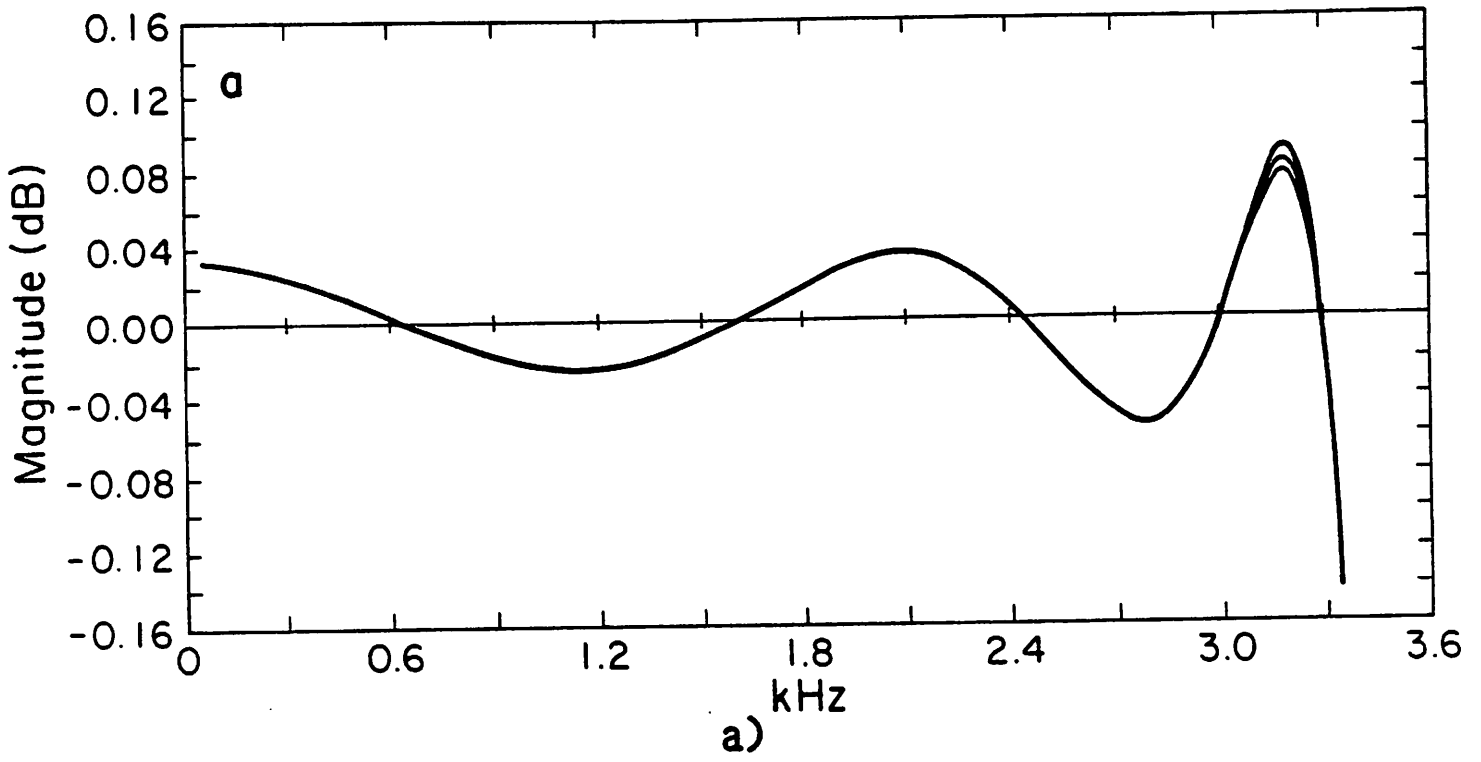
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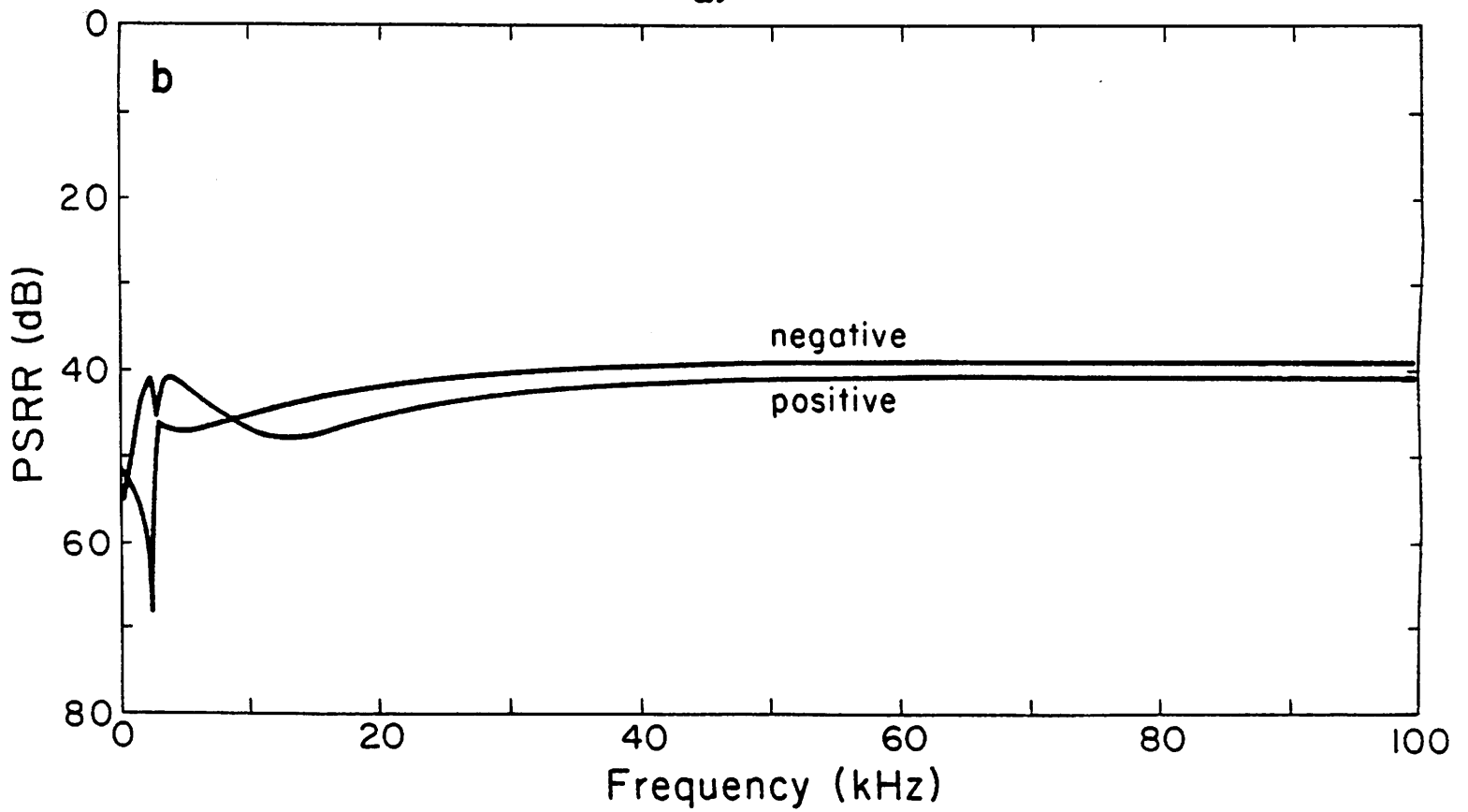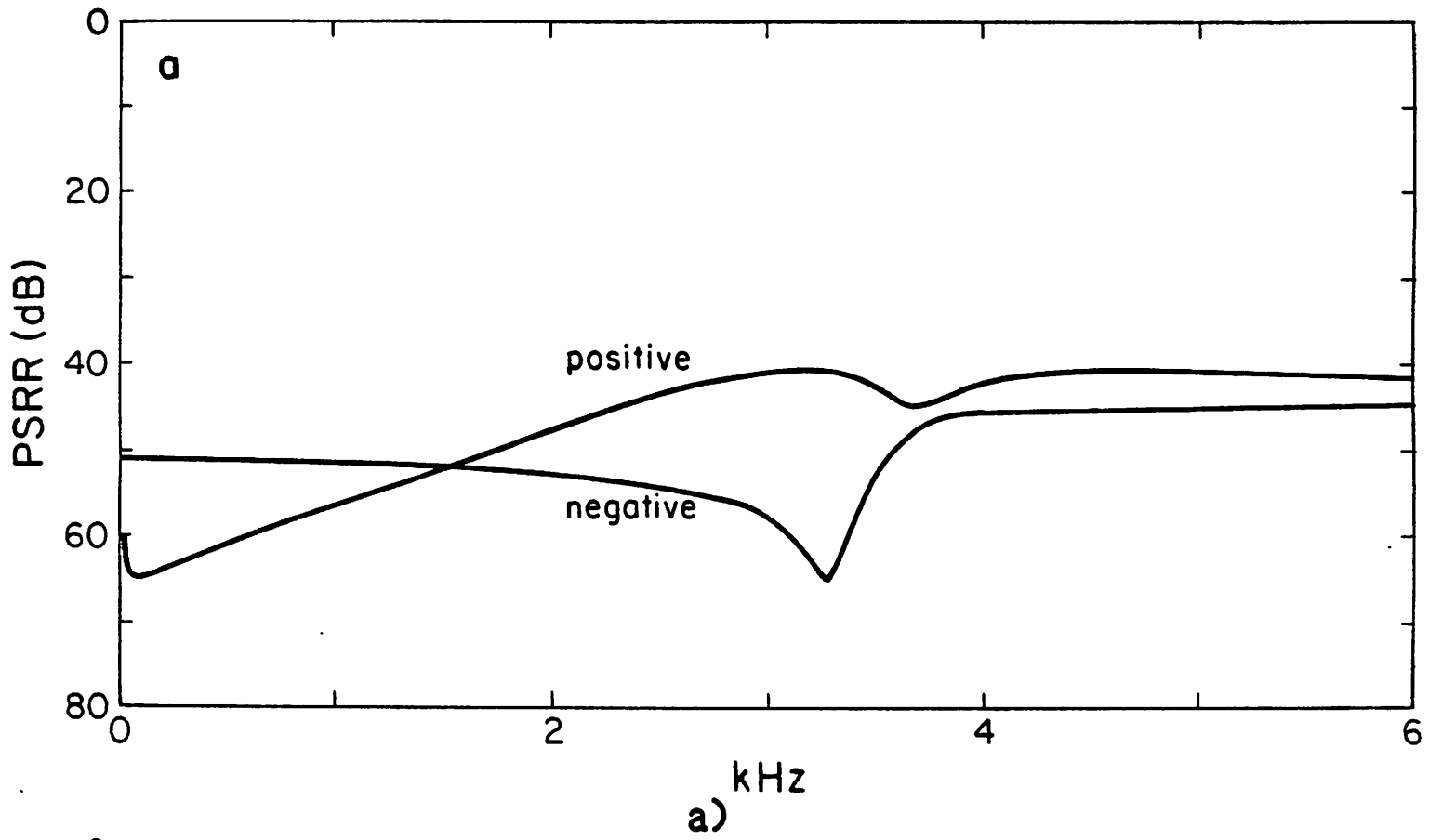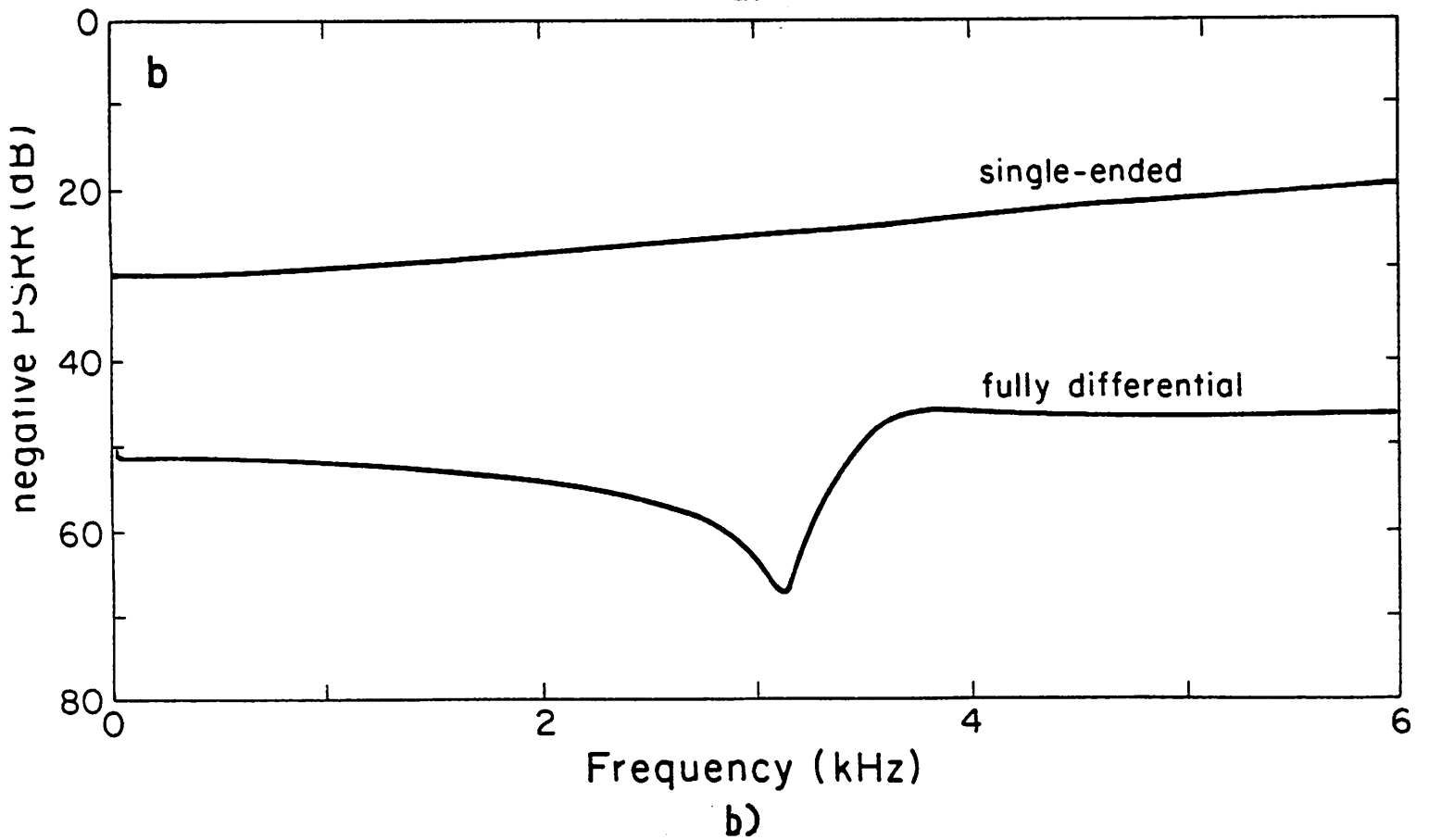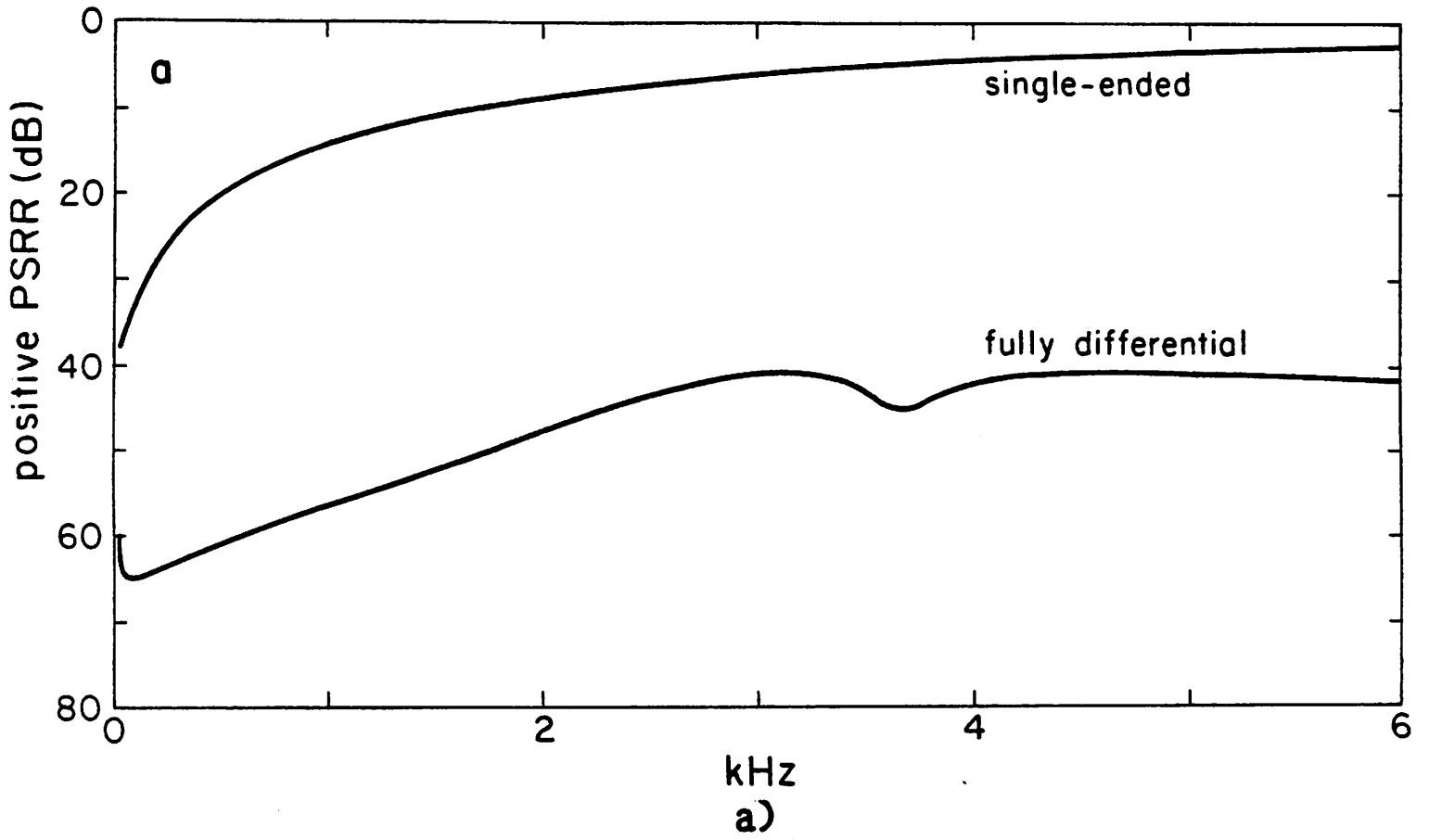
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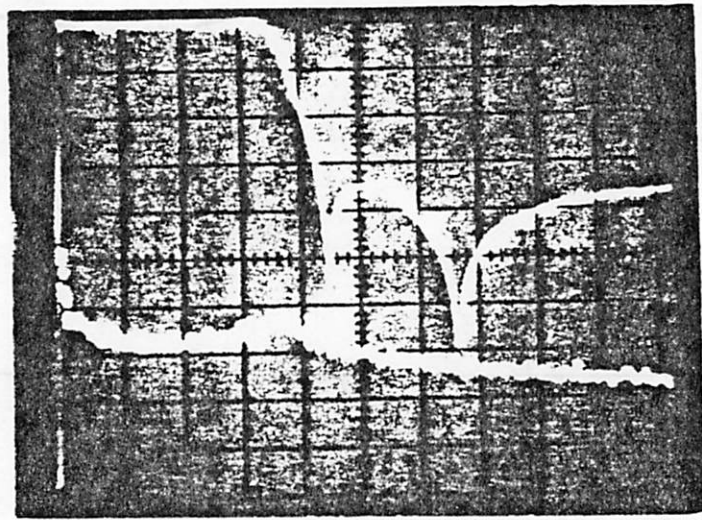
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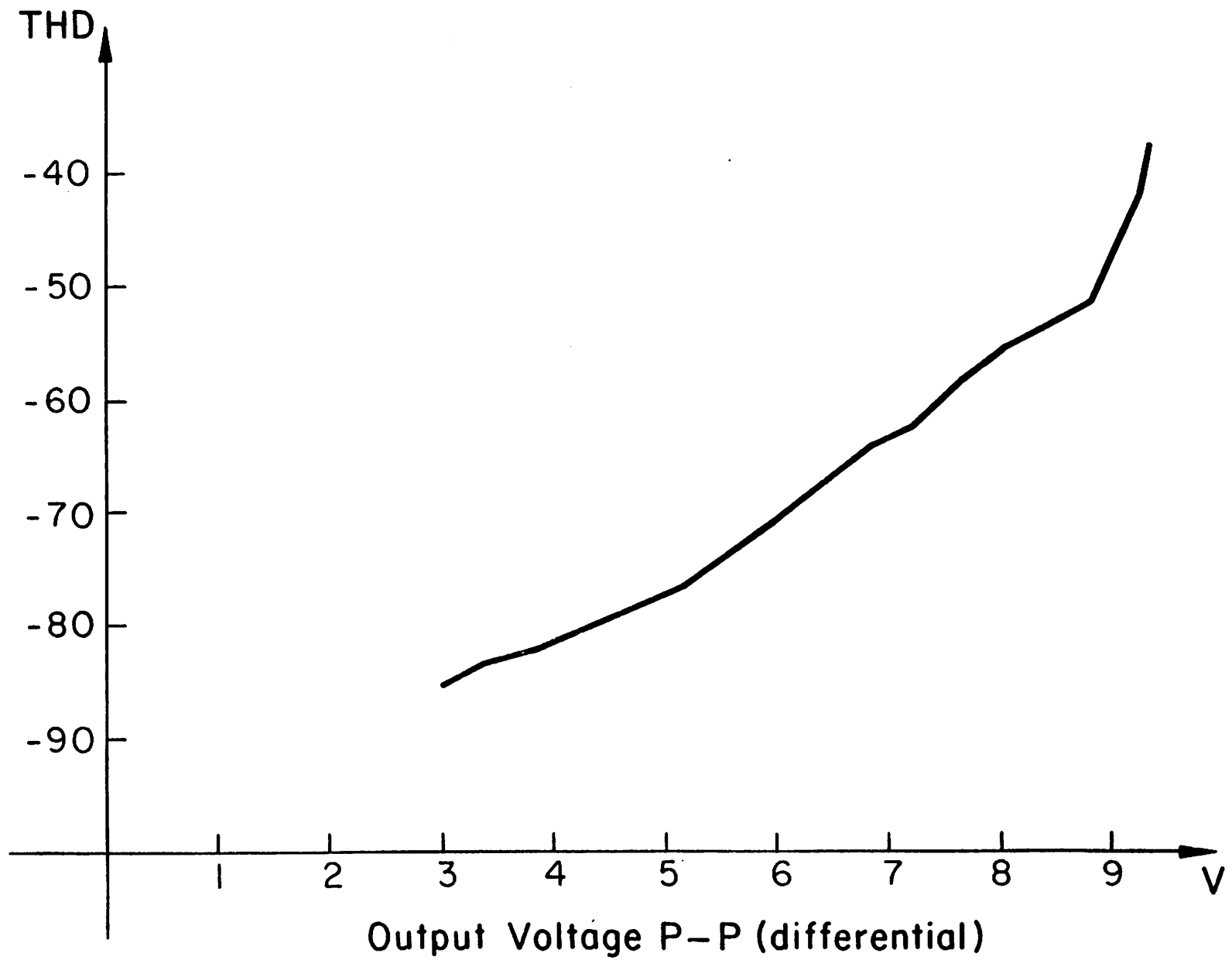
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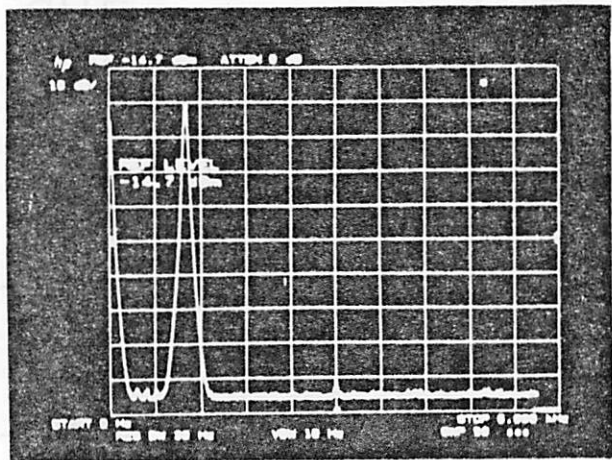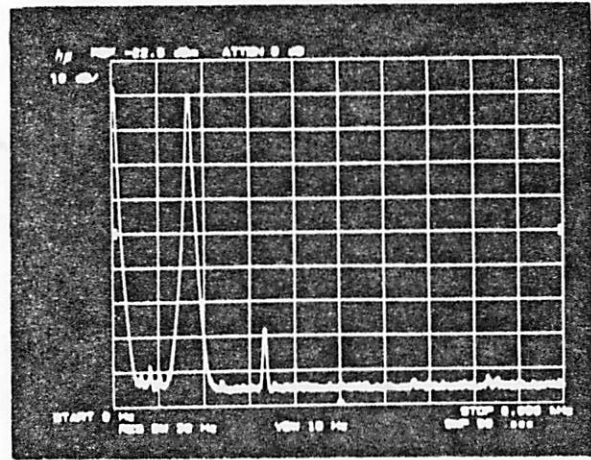
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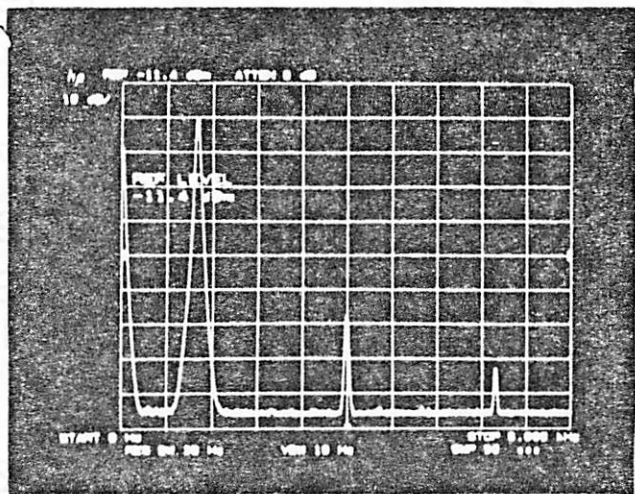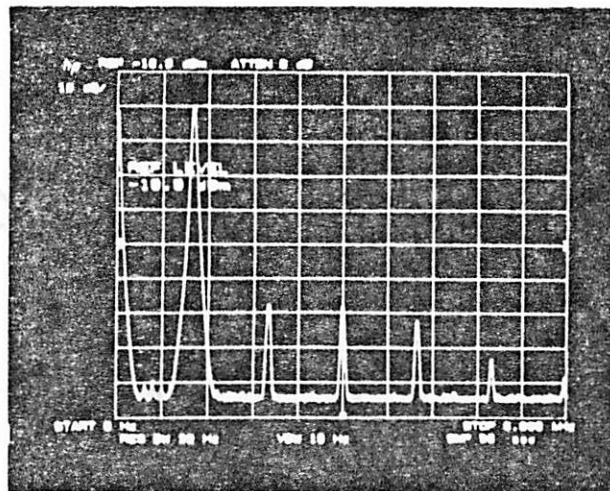
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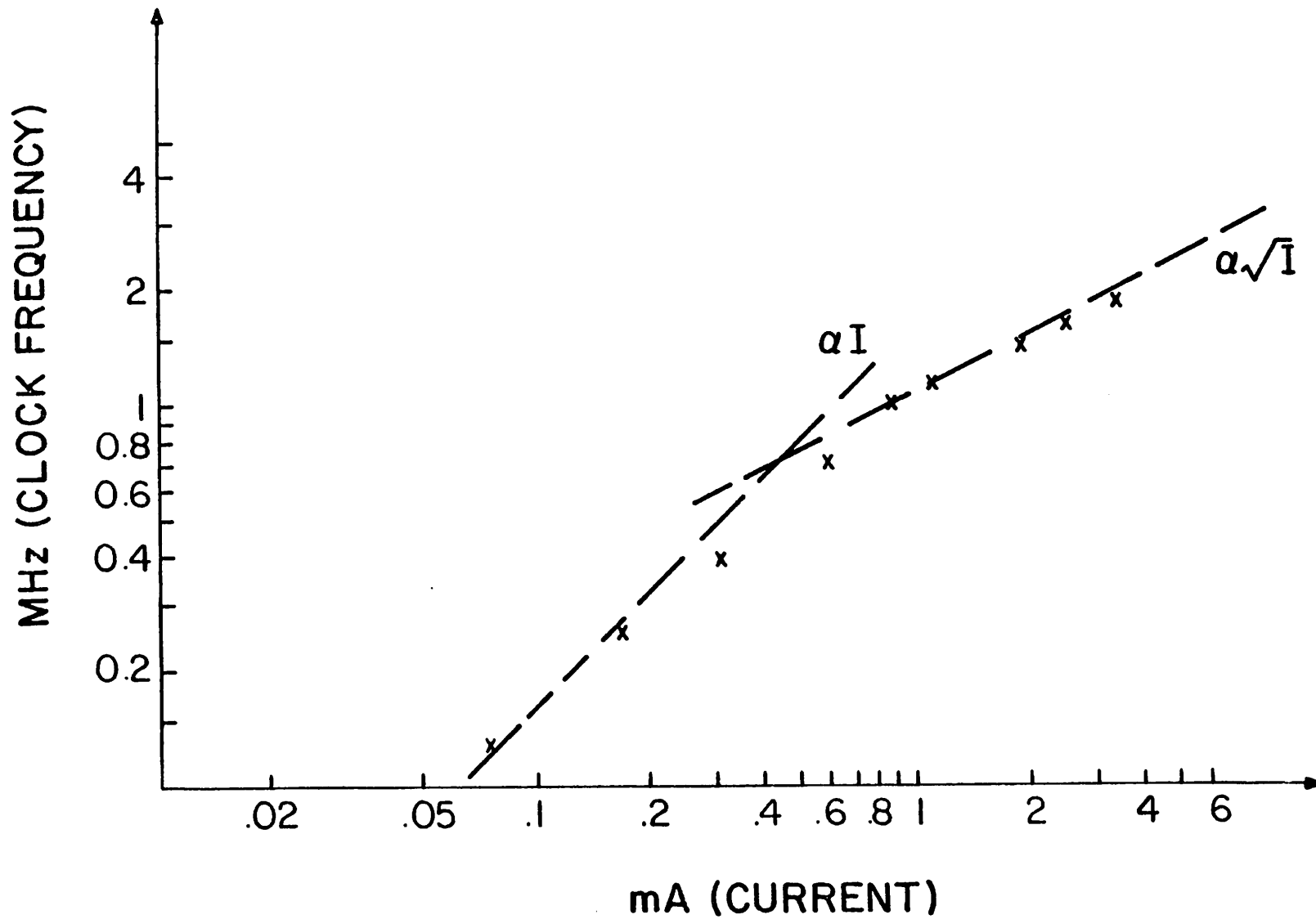
Fig. 21

CORE AMPLIFIER SPECIFICATIONS (0-5 Volts Supply)	
DIFFERENTIAL GAIN	> 10,000
POWER DISSIPATION	$90\mu W$
UNITY GAIN FREQUENCY	2 MHz
NOISE	140 nV/$\sqrt{Hz}$ 1KHz 50 nV/$\sqrt{Hz}$ white
OUTPUT SWING	0.5 Volts from Supply
AREA	300 mils^2

Table I

PARAMETER	CONDITION	VALUE
MINIMUM POWER DISSIPATION	5 VOLTS ONLY	350μW
P.S.R.R.	1KHz +SUPPLY 1KHz −SUPPLY	56 dB 52 dB
TOTAL HARMONIC DISTORTION	2V rms differential output 1KHz	73 dB
IDLE NOISE	CMESSAGE WEIGHTED	70 μV
OUTPUT SWING DIFFERENTIAL	<1% THD	3.1(RMS)V
DYNAMIC RANGE	—	93.dB

Table 2