PRECISION CMOS OPERATIONAL AMPLIFIER

by

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ABSTRACT

The modelling of a lateral biploar npn transistor in a standard p-well CMOS process is described. This model can be structured in the form of a 'sub-circuit' in simulator such as SPICE. The design of a precision operational amplifier using this npn lateral device is discussed. This amplifier has input bias current of 10nA and dc gain greater than 100dB. It also features an input offset self-calibrating scheme which can bring dc offset voltage down to $50\mu V$ range.

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CHAPTER 1

INTRODUCTION

The development of precision analog components in MOS technology has been accelerated in order to meet the growing integration trend of analog and digital LSI functions. An essential building block of the analog function is a precision operational amplifier. Low offset, noise and bias currents improve system accuracy when used in applications such as long-term integrators and high-accuracy amplifiers for very low-level signals. Therefore, the availability of precision amplifiers in standard MOS technologies is of great interest. This report explores the techniques for designing precision CMOS operational amplifiers.

MOS transistors are well known to be inferior to bipolar transistors in certain analog application aspects. In particular, for a given device size (area), MOS transistor pair exhibits much higher mismatch offset as well as higher 1/f noise when compared to their bipolar counterparts. These limitations of MOS devices have in the past prevented the existence of precision operational amplifier in standard CMOS technologies. Hence, by using the 5-terminal lateral bipolar transistors available in standard CMOS technologies as the amplifier input devices, both the offset and noise performance of the circuit can be improved.

Chapter 2 describes the characterization, modelling and optimization of the 5-terminal lateral bipolar device. In chapter 3, the design of a 3-stage precision CMOS operational amplifier using the lateral bipolar transistors is discussed.

To achieve low offset, circuit trimming is required. In the past decade, serveral trimming techniques for monolithic devices have been developed for the adjustment and improvement of a critical variable. The most common ones are: laser trimming, fusible links trimming and Zener-zap trimming[1]. In many cases, trimmings are performed at the wafer probe stage. The required instrumentation and the lengthy testing time sacrifice some of the cost advantages of the monolithic process. Cost considerations therefore provide a strong incentive to go for "self-calibration". Chapter 4 introduces an input offset self-calibration technique. The self-calibration process used in the amplifier discribed here will be initiated every time the circuit is powered up. It requires a clock signal which is readily available in most systems and a power-up strobe signal. The information obtained through the calibration will be stored in a 7-bit static RAM. Since the circuit is recalibrated everytime it is powered up, it does not suffers from long term drift problem.

Miscellaneous considerations and conclusions are presented in Chapter 5 and Chapter 6 respectively.

CHAPTER 2

MODELLING OF THE 5-TERMINAL LATERAL BIPOLAR TRANSISTOR

2.1. Introduction

The lateral bipolar device available in standard CMOS technologies has attracted the attention of analog designers in recent years [2] [3]. The devices were mostly fabricated in deep well CMOS process and effects of the vertical substrate bipolar transistor that is permanantly connected in parallel to the lateral device is therefore not significant. However, with the advances of processing techniques, shallow-junction technologies are now readily available. The commonly used well depth to date (Aug. 1984) is around 3-4 micron in standard single well VLSI CMOS technologies. Hence the effects of the vertical devices fabricated in these VLSI technologies become much more important than those fabricated in technologies with well depth of 10 microns or higher. It is therefore important to have a proper model for this 5-terminal device available to circuit designers to allow them to have better predictions on circuit performance. Fig.(1a) and Fig.(1b) show the top and cross-sectional views respectively of a 5-terminal lateral npn transistor in standard p-well CMOS technology. The passive and active elements involved in the model are explicitly shown in the diagram.

This section of the report describes an accurate model for this 5-terminal device. The model consists of 3 bipolar transistors, a few resistors and control sources. It can be configured in the form of a 'sub-circuit' in simulator such as SPICE [4]. Device characterization will first be presented which is then followed by model parameter extraction. Simulation results based on this model will be compared with measured characteristics at the end of this section.

2.2. Device Characterization

2.2.1. Device Operation Principle

This 5-terminal device is basically an MOS transistor operating in bipolar mode. The I-V transfer characteristics [log(IC) vs Vbe] under various gate bias is shown in Fig.(2). The transition from MOS operation mode to bipolar mode is apparent as Vg varies from +1.0 V to -0.4 V. The p-Si under the gate region starts to accumulate as Vg becomes negative. When strong accumulation is reached, only bipolar action is involved. From Fig.(2), it can be seen that the 1/slope [1/GRAD] of the log(IC) vs Vbe curve is approximately 60 mV, which is the typical characteristic of a silicon bipolar transistor.

2.2.2. Characterization and Modelling Approach

From Fig(1b), it is important to note that the 3 transistors share a common base and will therefore interact with one another. As a result, they cannot be "individually" modelled. But at the same time, 3 "separate" transistors are required to generate a complete SPICE model that is suitable for any biasing conditions (including situations when the transistor is operating under reverse mode). The following definitions and observations are made to allow the elimination of this dilemma :

A) Definition [refer to Fig.(3)] :

$$\beta_C = \frac{I_C}{I_{B(total)}} \tag{1}$$

$$\beta_{SUB} = \frac{I_{SUB}}{I_{B(total)}} \tag{2}$$

The conditions when both Q_c and Q_{SUB} are biased up in the forward active mode will be consider.

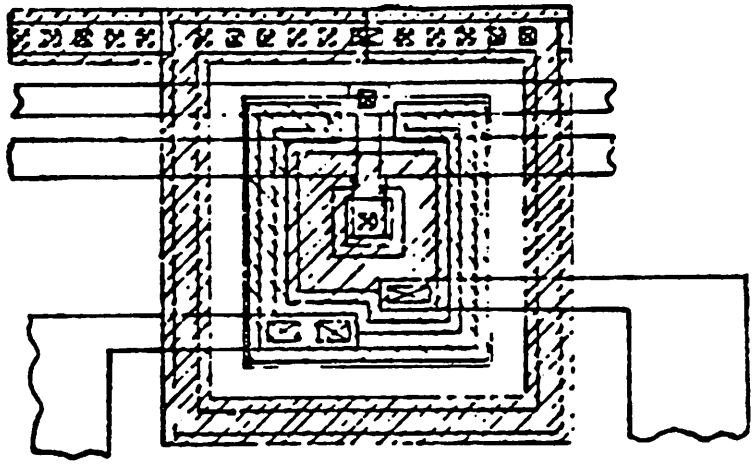


Fig.(1a) Top view of a 5-terminal lateral bipolar device.

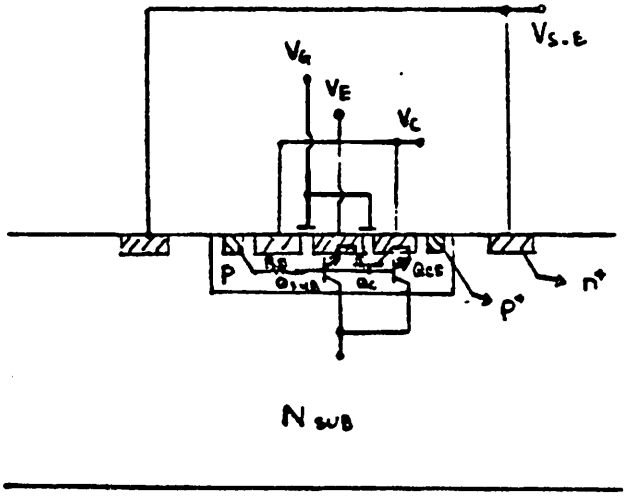


Fig.(1b) Cross-sectional view of the device in Fig.(1a).

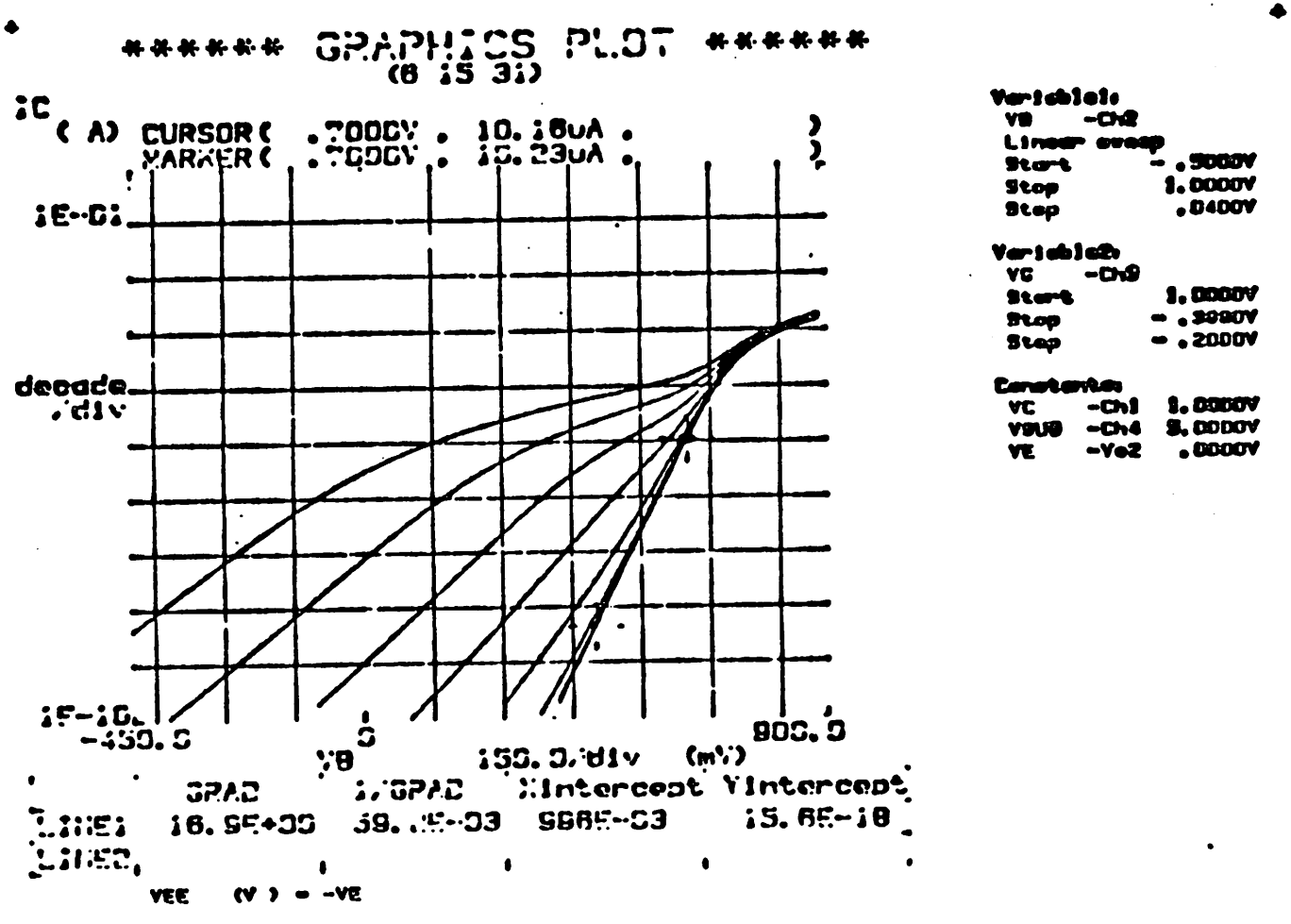


Fig.(2) I - V transfer characteristics of the lateral bipolar device.

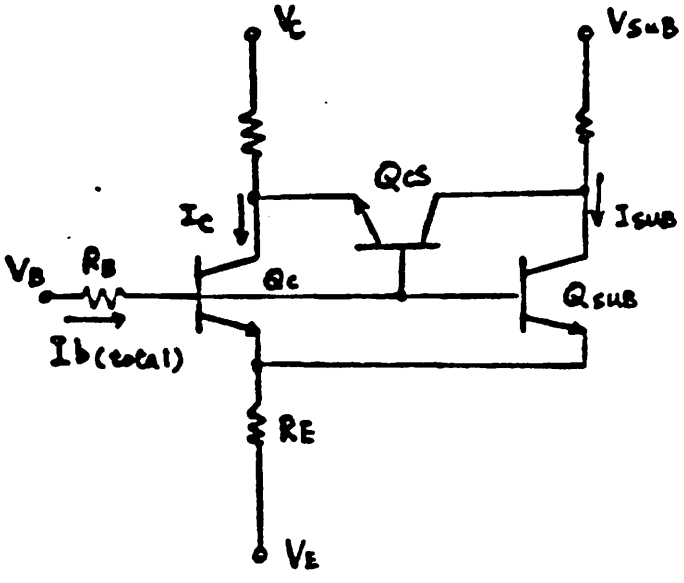


Fig.(3) Schematic of device in Fig.(1b).

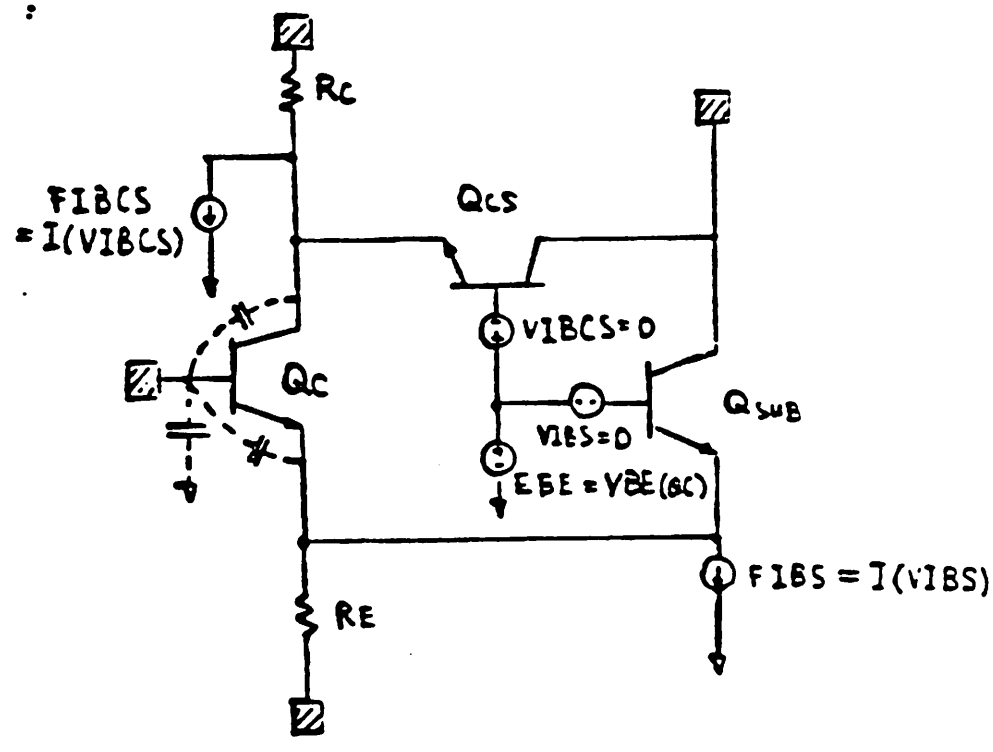


Fig.(4) Complete SPICE model of the lateral bipolar device.

B) Observations [refer to Fig.(3)] :

i) Q_{cs} is off.

ii) Since Q_c and Q_{SJB} share a common emitter and a common base, we can think of them as a "single" device with split-collectors.

iii) R_B is a "lumped" base resistance and R_E is the common emitter resistance of this split-collector device.

iv) For a given V_{BE}, a certain value of $I_{b(total)}$ will flow into the base terminal and the total collector current will be $I_c + I_{SJB}$.

v) If I_c, I_{SJB} and $I_{b(total)}$ are plotted (semi-log) against V_{BE}, the lumped R_B can be extracted from this "common" $I_{b(total)}$ curve.

vi) Using the definitions in (A), it is obvious that for a given value of I_c, we can determine the corresponding value of $I_{b(total)}$ uniquely.

vii) Since R_B is extracted from the $I_{b(total)}$ curve, the value of this base-current dependent resistor can be determined uniquely for any given value of $I_{b(total)}$.

With the above observations, the following claims can be made :

(1) The sum of all different base current components [$I_{b(total)}$] are sufficiently modelled by the parameter β_c [since for a given V_{BE} I_c and $I_{b(total)}$ are fixed].

(2) The effects of the total base current [$I_{b(total)}$] on the effective base resistance can be sufficiently modelled by the parameter R_B [recall that R_B is the "common" lumped base resistance].

The complete model as shown in Fig.(4) is proposed. Each transistor in this model is represented by the BJT model used in SPICE [i.e. either the

Gummel-Poon model or the Ebers-Moll model]. From Fig.(4), it is important to note that :

(I) Base on observations (iii), (iv), (vi) and (vii), the transistor Q_c models the complete characteristics of the 5-terminal device but the additional current due to the minority-carrier injection from the common emitter to the substrate [I_{SUB}]. That is, the current-dependent base resistance [R_B], the total base current [$I_{b(total)}$], the lateral collector current [I_c], shot noise due to I_c, shot noise due to $I_{b(total)}$, noise due to R_B and various capacitances have all been modelled. The shot noise due to I_{SUB} is not modelled by Q_c does not present any problem. This is because the substrate is always connected to supply and the collector current shot noise of the substrate device will not appear in the signal path.

(II) Since I_{SUB} is not modelled by Q_c, we therefore need to find a way to generate this I_{SUB} and to introduce it at the node right before the common emitter resistance. The transistor Q_{SUB} is used to perform this function in the complete model. The introduction of Q_{SUB} should, however, satisfies the following requirements :

a) For a given V_{BE} of Q_{SUB}, a unique value of I_{SUB} is to be generated.

b) The effect of the $I_b R_{base}$ voltage drop of Q_{SUB} on the value of the collector current must be taken into account.

c) The noise contributions of I_b and R_{base} mentioned in (b) should not appear in the signal path [i.e. the collector of Q_c in the model] based on statement (I) above. Otherwise non-existing noise sources are introduced in the model.

d) Since we only want to introduce the current, I_{SUB}, into the node just before the common emitter resistance, the base current of the device

used to generate $I_{S/B}$ must therefore be removed from this node.

e) The signal path should not be capacitively loaded by this $I_{S/B}$ generating device.

The model configuration shown in Fig.(4) is almost self-explanatory once the above requirements are noted. i.e. :

(1) (a) implies that the V_{BE} applied to $Q_{S/B}$ should be identical to that applied to Q_c. The base terminal of $Q_{S/B}$ must be isolated from the signal path in order to satisfy (c). The voltage-controlled voltage source, EBE, is used to realize these two requirements.

(2) From (b), the $I_{S/B}$ and R_{base} of concern must obviously be the same as $I_{b\,(total)}$ and R_B described earlier. This is realized by choosing the values of the SPICE parameters RB and BF for $Q_{S/B}$ to be equal to R_B and $\beta_{S/B}$ [defined earlier] respectively.

(3) To meet the requirement of (d), voltage source VIBS (with d.c. value equal to zero) is used to monitor the base current of $Q_{S/B}$ and the current-controlled current source FIBS (controlled by current flowing through VIBS) is introduced to remove this base current from the summing node.

(4) To satisfy the requirement stated in (e), $Q_{S/B}$ and is assumed to be capacitance free.

Similar modelling approach is applied to Q_{cs}, and the functions of the controlled sources VIBCS and FIBCS are apparent.

The degree of matching between adjacent devices was also accessed. It was found that the Vbe mismatch is less than 2 mV for devices with the geometry as shown in Fig.(1a).

2.2.3. Device Characteristics

Measured transfer characteristics are presented in this section. Measurements are performed based on the assumptions stated in section 2.2.1 . Fig.(5a) to Fig.(5h) show the transfer characteristics of a typical device in both forward and reverse modes of operation.

2.2.4. Parameter Extraction

The model for the bipolar junction transistor is based on the integral charge model of Gummel and Poon [5]. The parameter extraction techniques are well documented in other literature [6] and will not be repeated here.

2.3. Simulation Results

The DC parameters extracted for the different transistors in the model are as shown below:

Parameter	Q_c	$Q_{S'JB}$	Q_{cs}
β_F	32	140	150
I_s	1.7e-17	0.9e-16	5.3e-16
NF	0.98	0.98	0.96
VAF	11	90	55
IKF	1.0e-3	1.0e-3	0.4e-3
ISE	4.0e-18	4.0e-18	2.0e-15
NE	1.18	1.16	1.325
RB	1.5e3	1.5e3	1.5e3
IRB	2.5e-4	1.0e-3	5.0e-3
RBM	200	200	200
RC	500	500	-
β_R	5	-	-
NR	0.98	-	-
VAR	11	-	-
IKR	2.5e-3	-	-
ISC	2.0e-15	-	-
NC	1.325	-	-

Fig.(6a) to Fig.(6h) are the simulated results based on the proposed model in Fig.(4). It can be seen that they agree very well with the measured data. In particular, notice the close resemblance between Fig.(5d) and Fig.(6d), and between Fig.(5h) and Fig.(6h).

2.4. Device Structure Optimization

From the measured results, $\beta c(max)$ is only around 30. However, the device structure in Fig.(1a) is by no means optimized.

To improve βc, the following steps can be taken :

(1) Reduce the lateral base width, x_b (i.e. the MOS channel length). This well reduced the Gummel number of the transistor and hence improve βc. In additional, reducing x_b will also improve the frequency performance of the device since

$$f_T \alpha \frac{1}{x_b^2} \tag{3}$$

(2) Increase the periphery to area ratio of the emitter so that the relative amount of carriers injected down into the substrate will be reduced. This can be achieved by using a "fingered" emitter structure as shown in Fig.(7), where 2 μm design rule is assummed. This layout has improved the periphery to area ratio by approximately a factor of 4 while the required area is kept to be about the same when compared to the layout in Fig.(1a) (3 μm design rule).

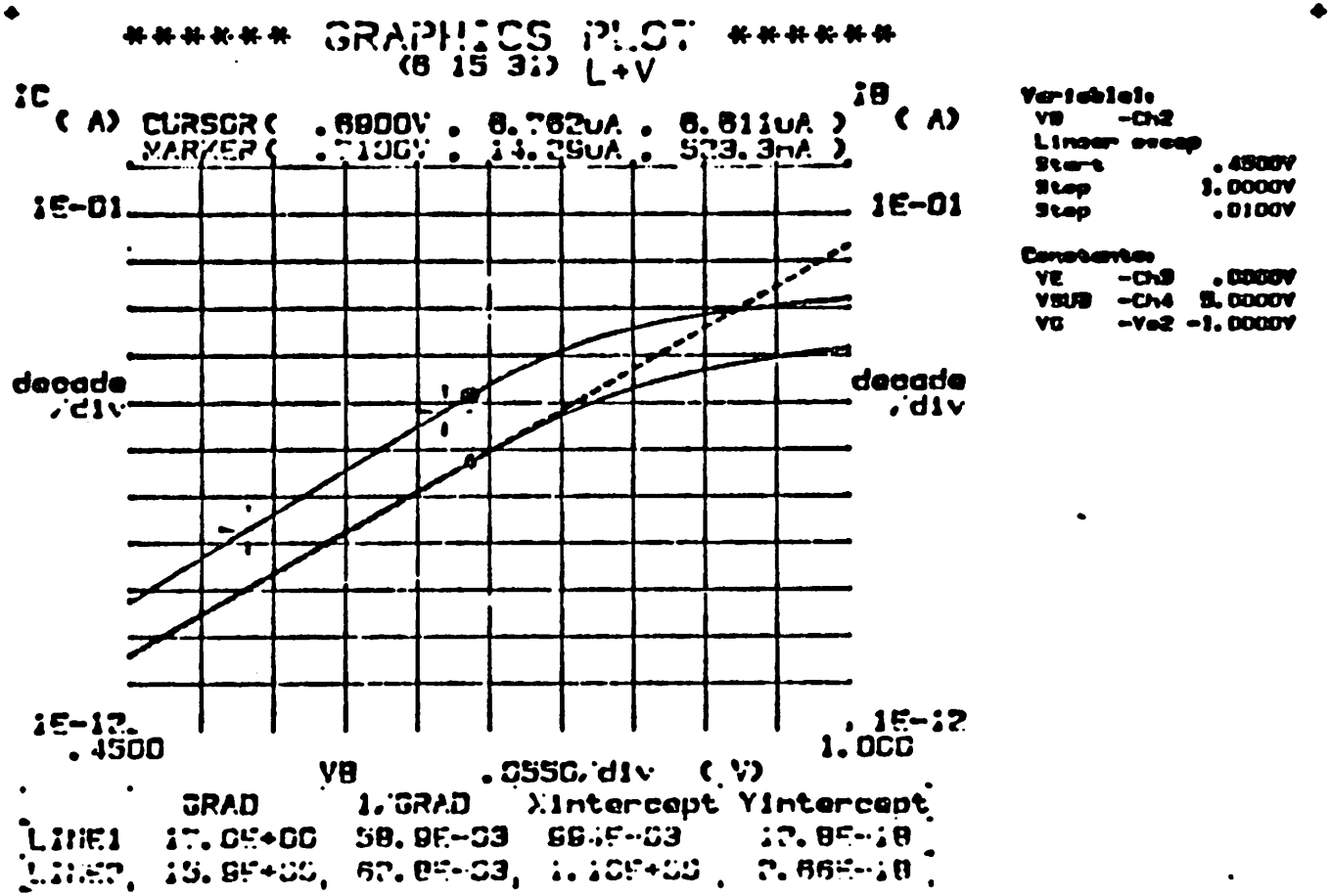


Fig.(5a) Ic and Ib Vs Vbe

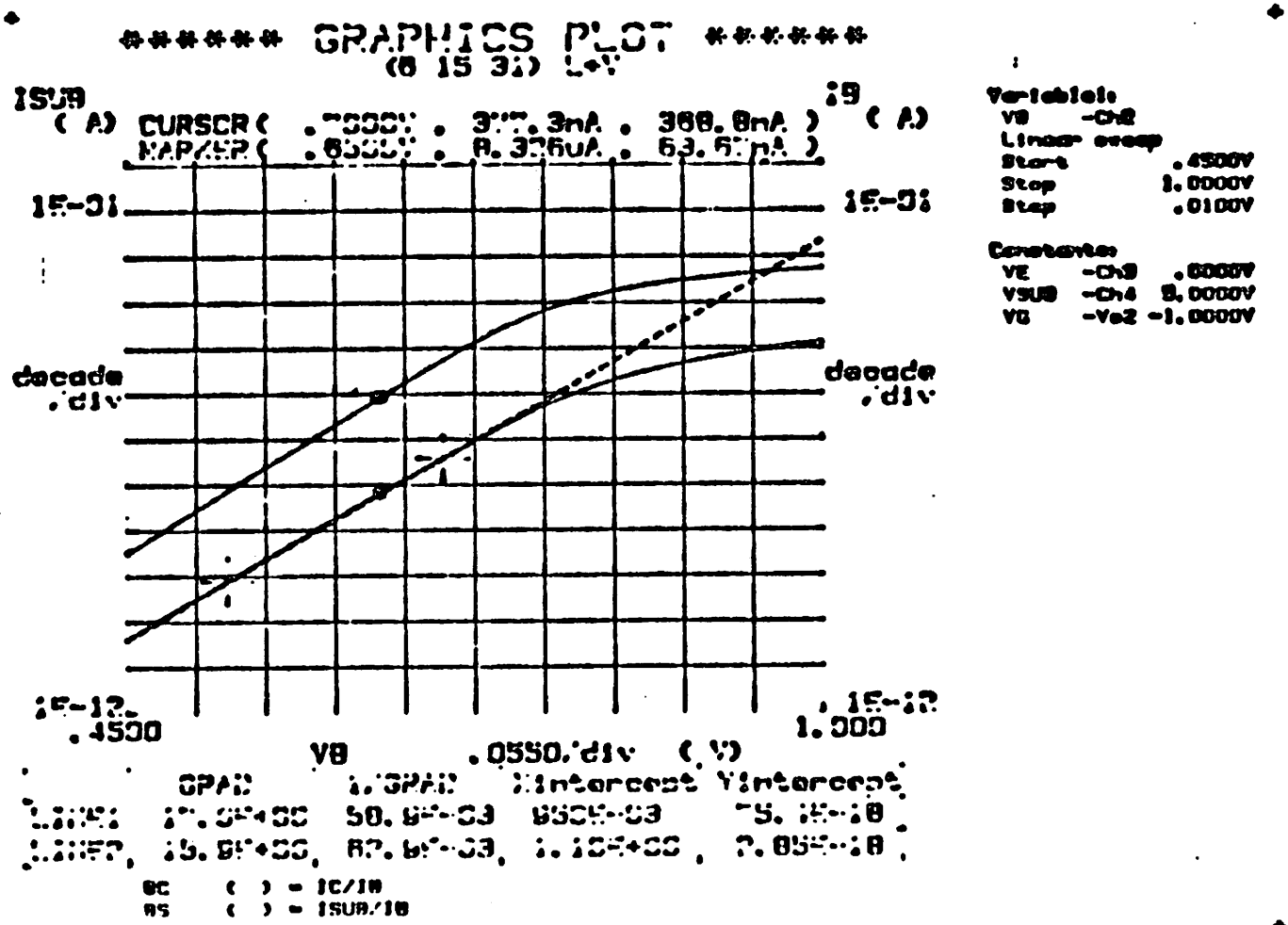
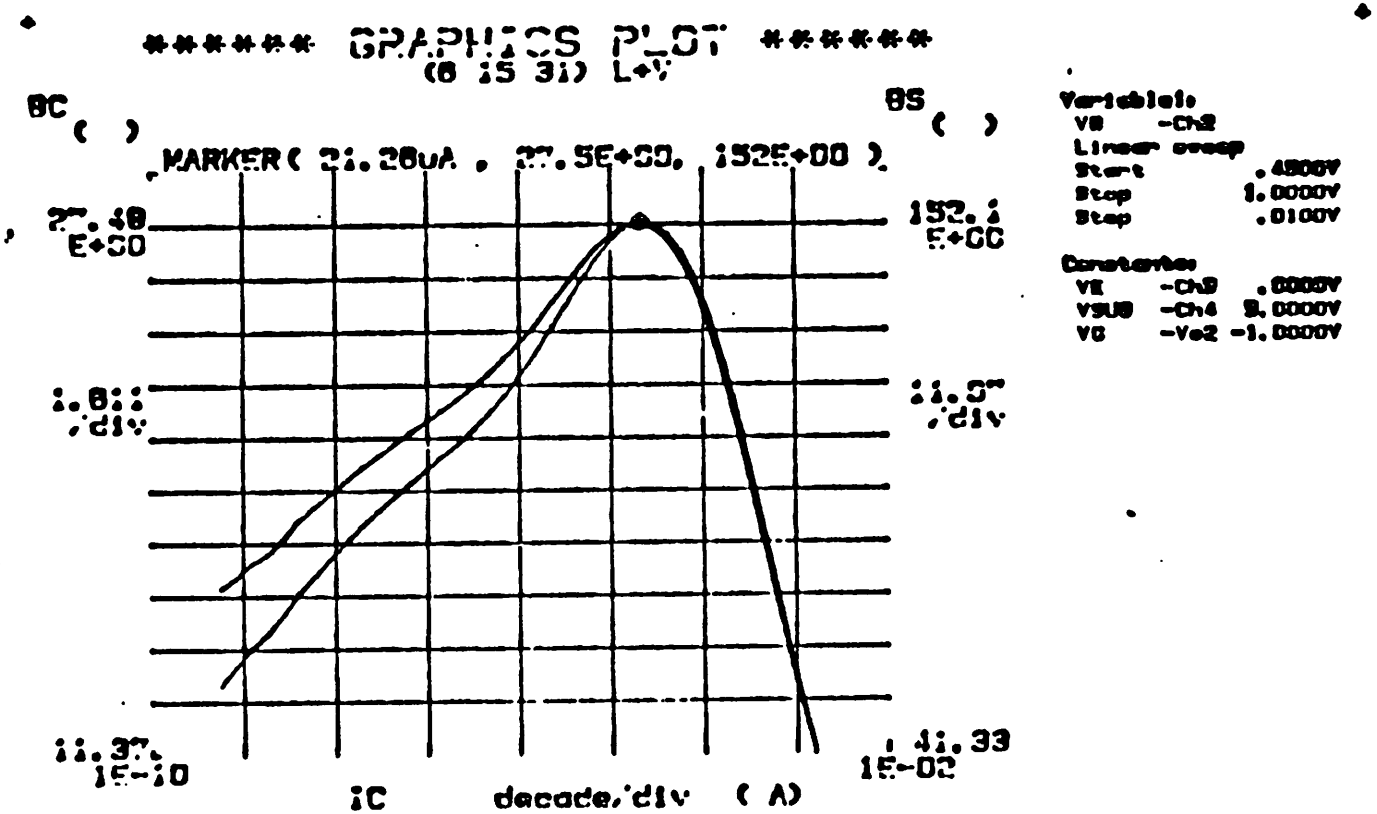


Fig.(5b) Isub and Ib Vs Vbe

Fig.(5c) β_c and β_{sub} Vs I_c.



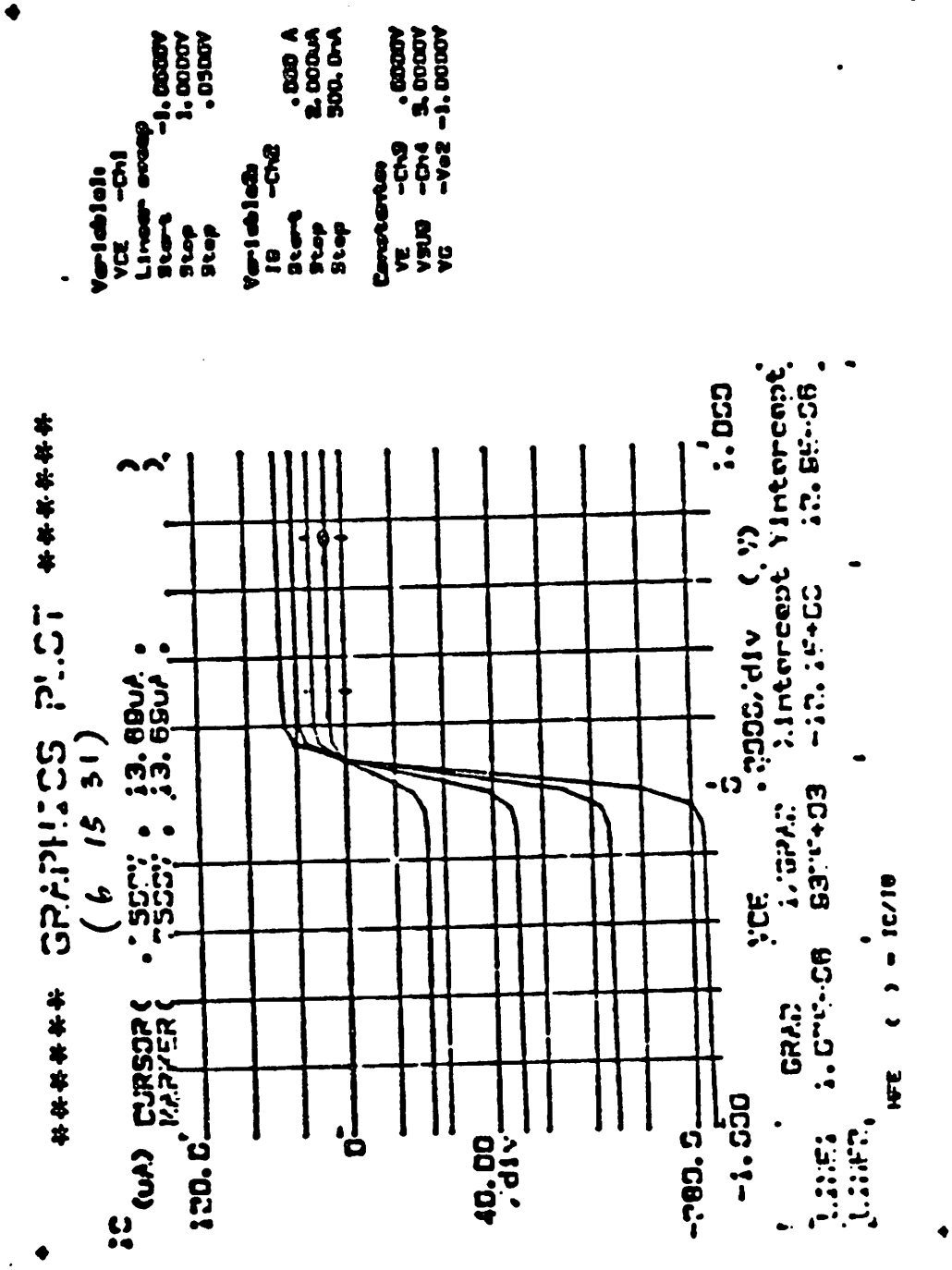


Fig.(5d) I_c Vs V_{ce} characteristics.

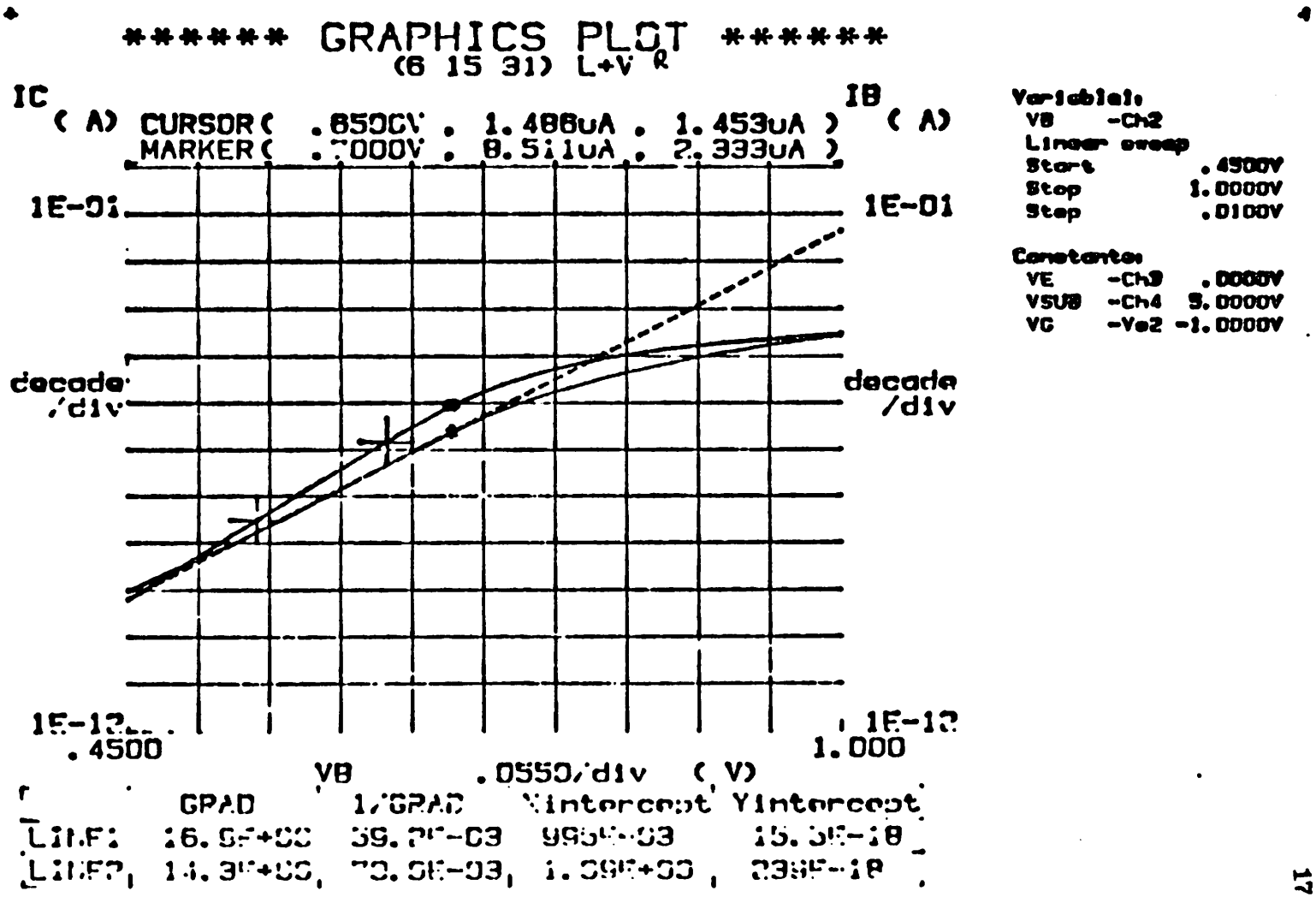


Fig.(5c) I_{SUB} and I_C Vs V_{BE} (Reverse mode).

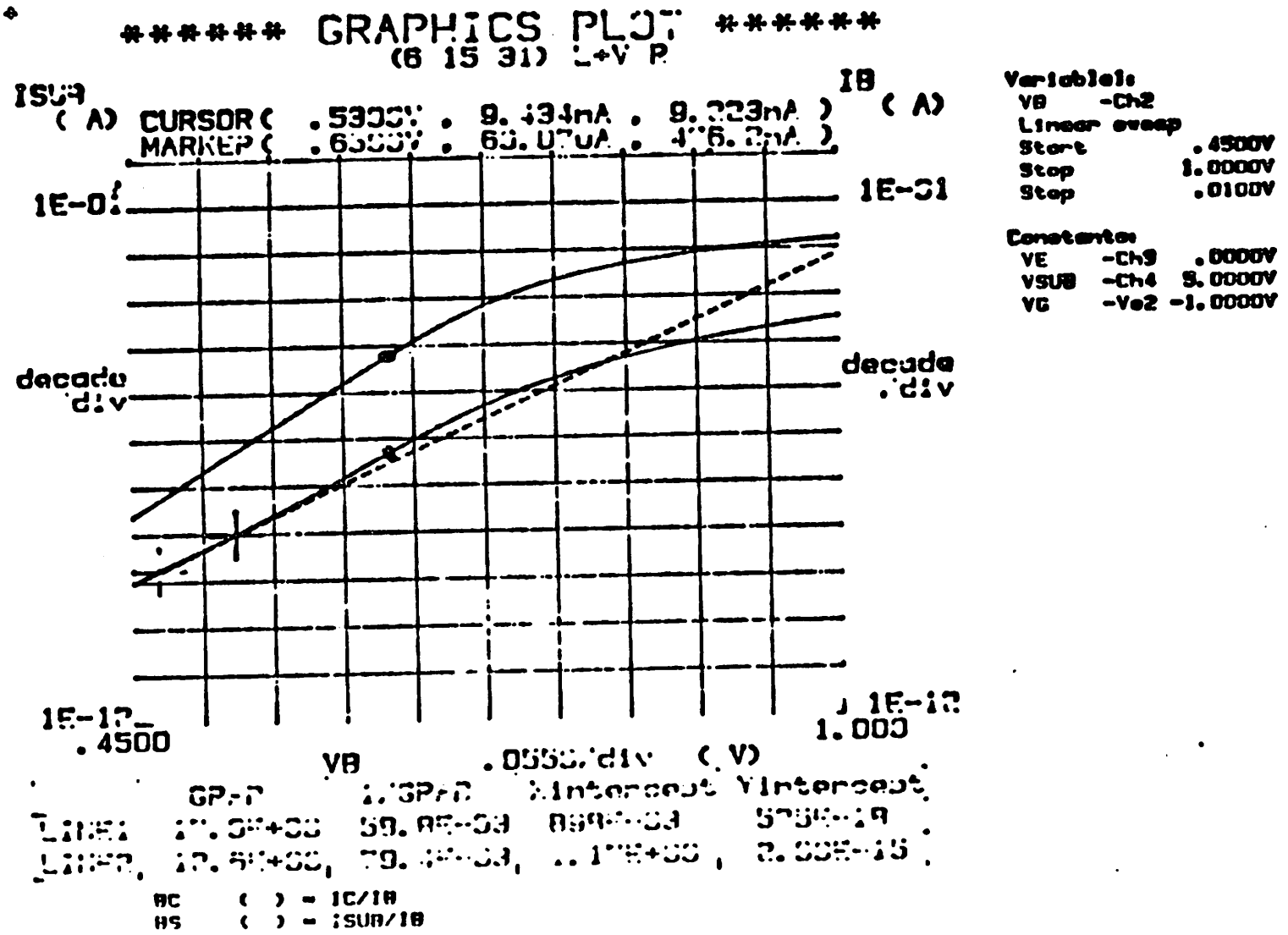
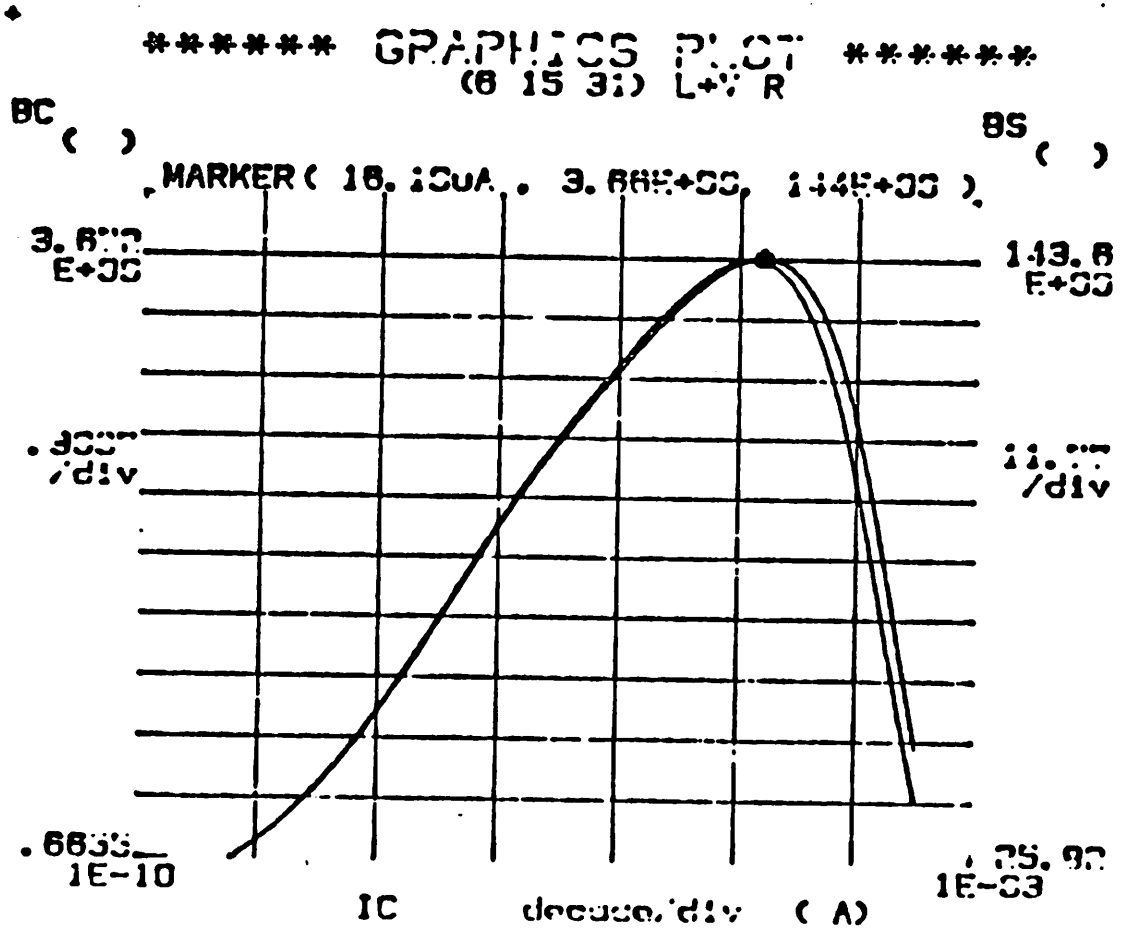


Fig.(5f) β_i and β_{sub} Vs I_c (Reverse mode).



Variables
VB -Ch2
Linear sweep
Start .4500V
Stop 1.0000V
Step .0100V

Constants
VE -Ch3 .0000V
VSUB -Ch4 5.0000V
VC -Ve2 -1.0000V

BC ( ) = IC/IB
BS ( ) = ISUB/IB

Fig.(5g) I_C and I_B Vs V_{BE} (Reverse mode).

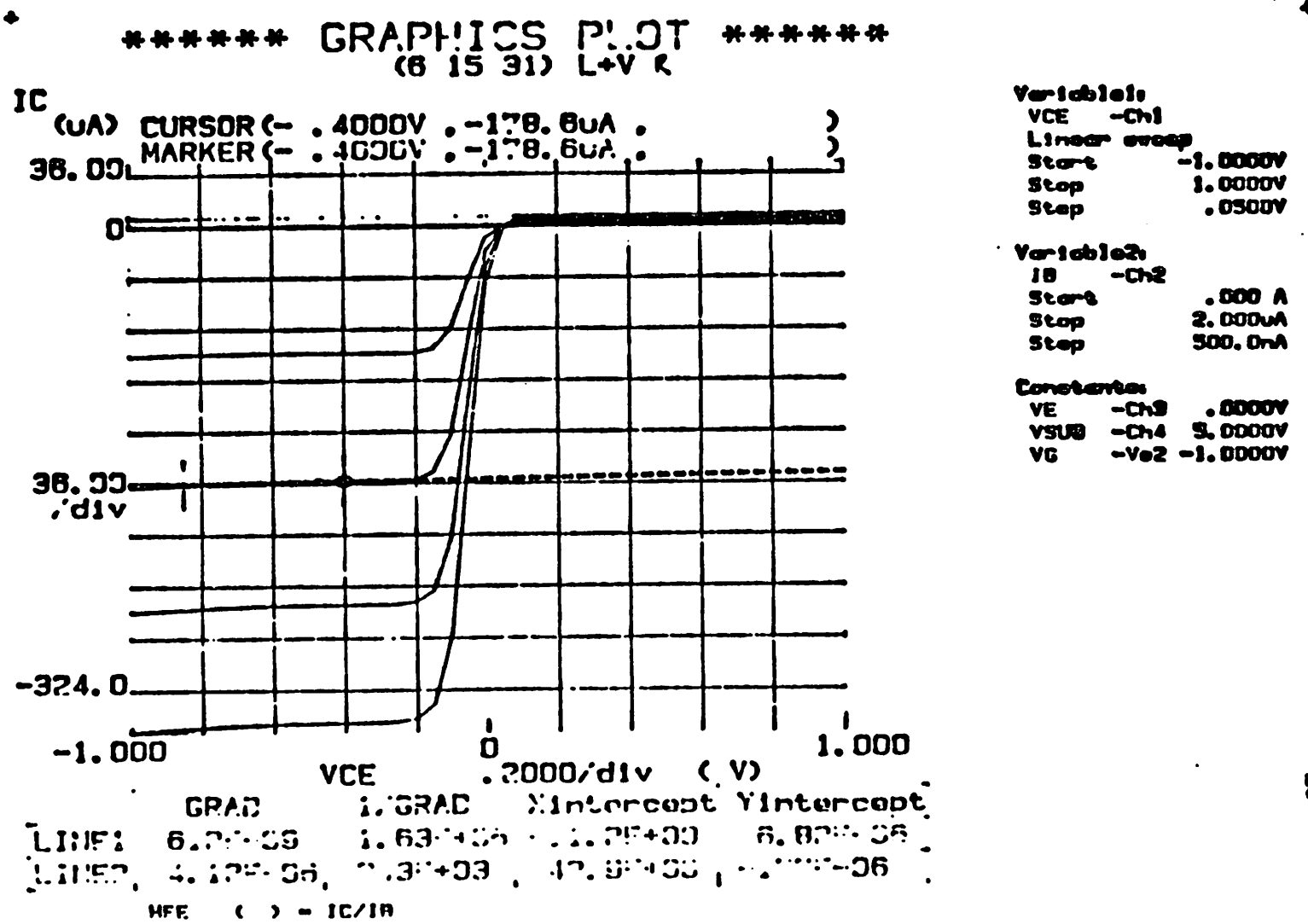


Fig.(5h) I_c Vs V_{ce} characteristics (Reverse mode).

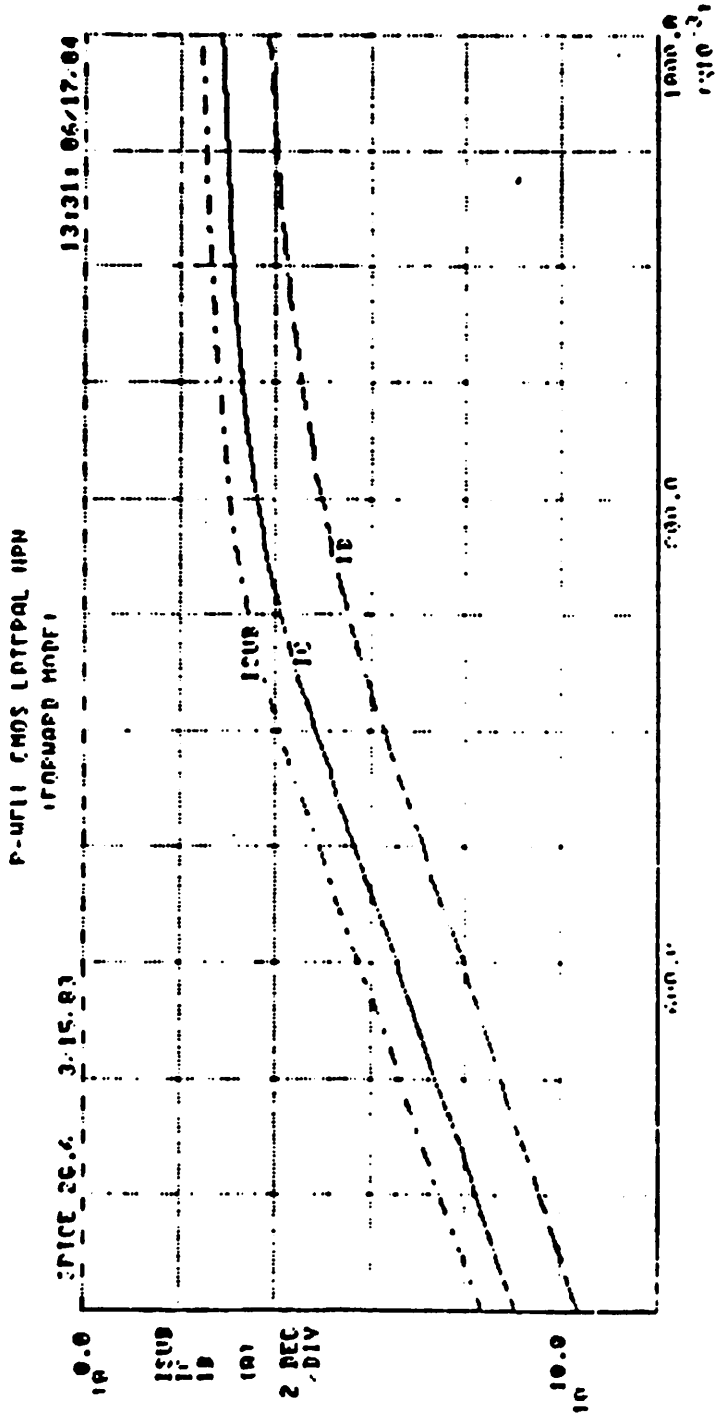


Fig.(6a) I_c, I_{SUB} and I_b Vs V_{BE}.

Fig.(6b) β_c Vs I_c.

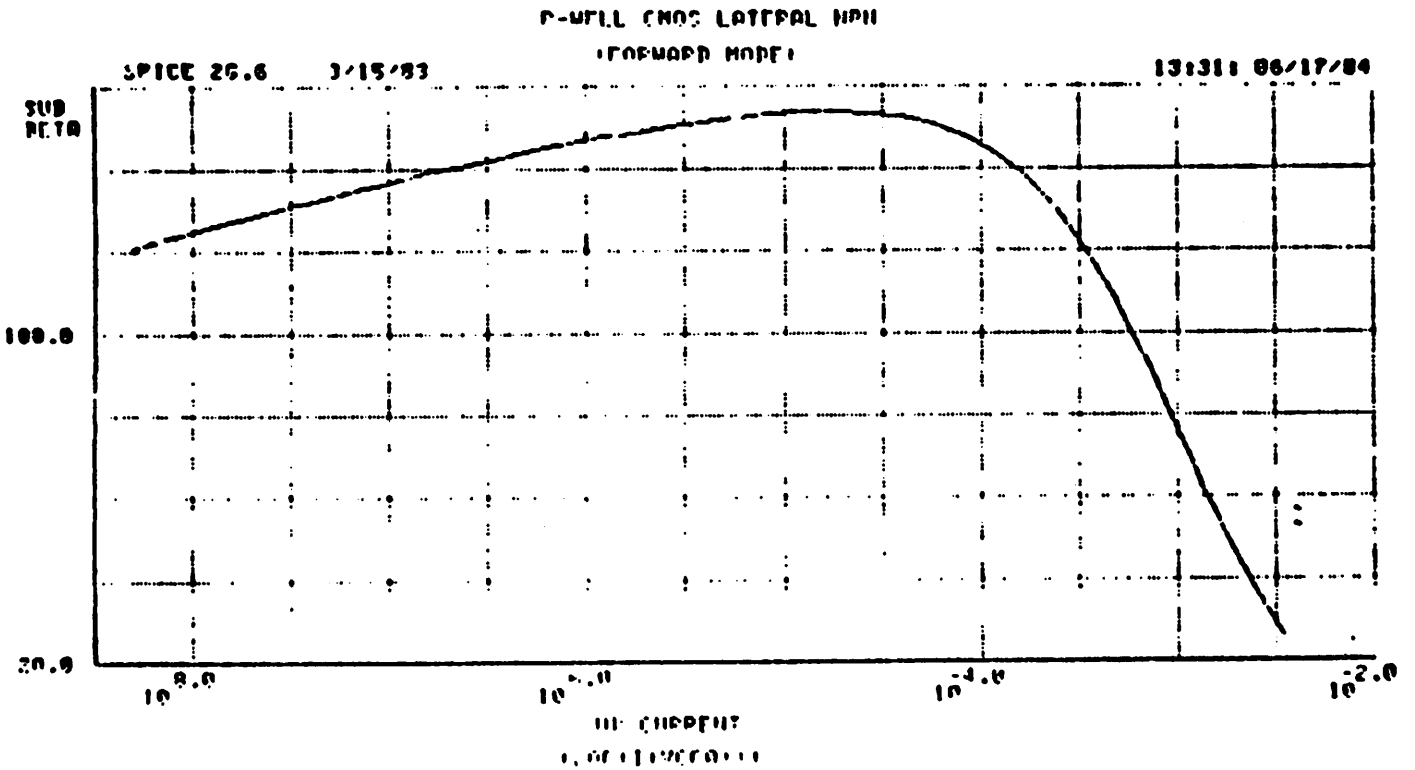


Fig.(6c) β_{sub} Vs I_{sub}.

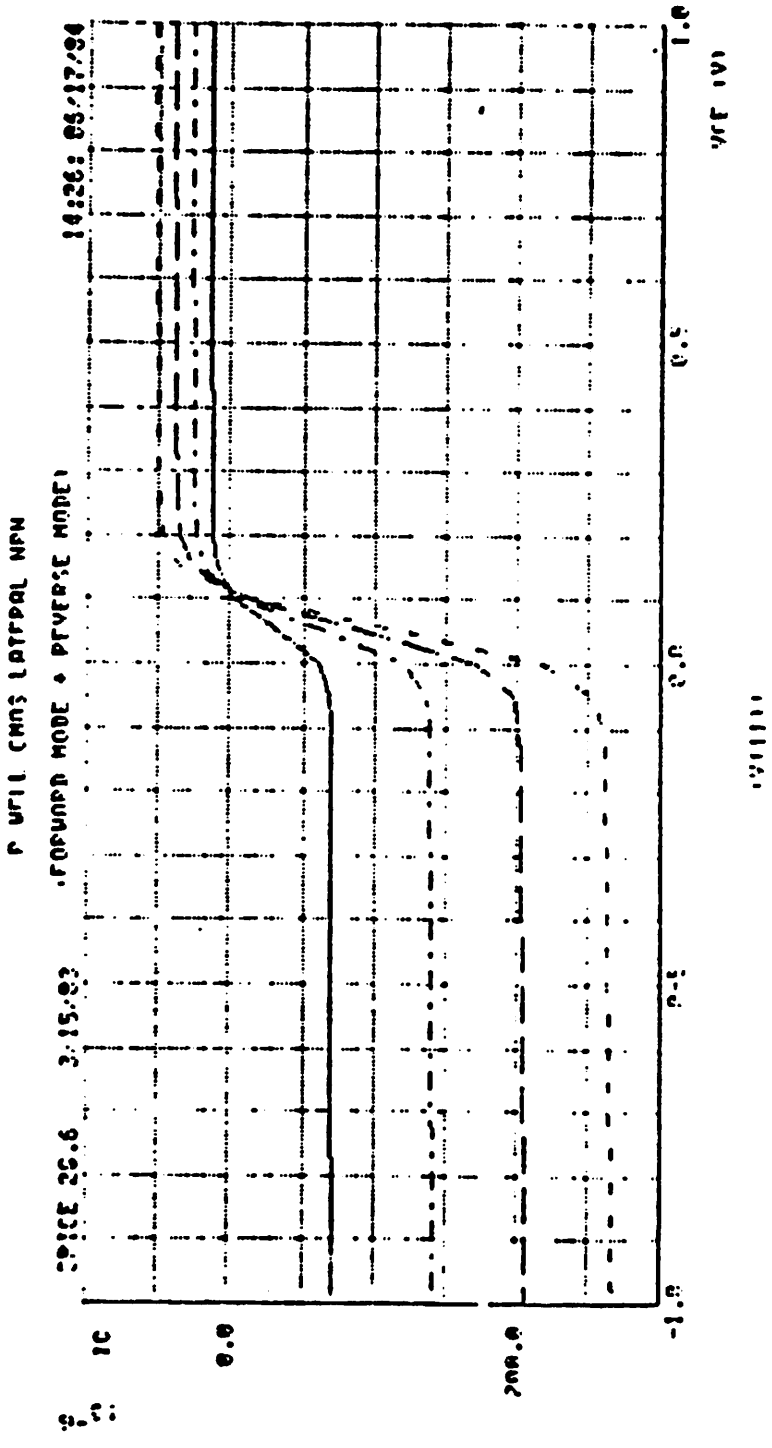


Fig.(6d) I_c Vs V_{bc} characteristics.

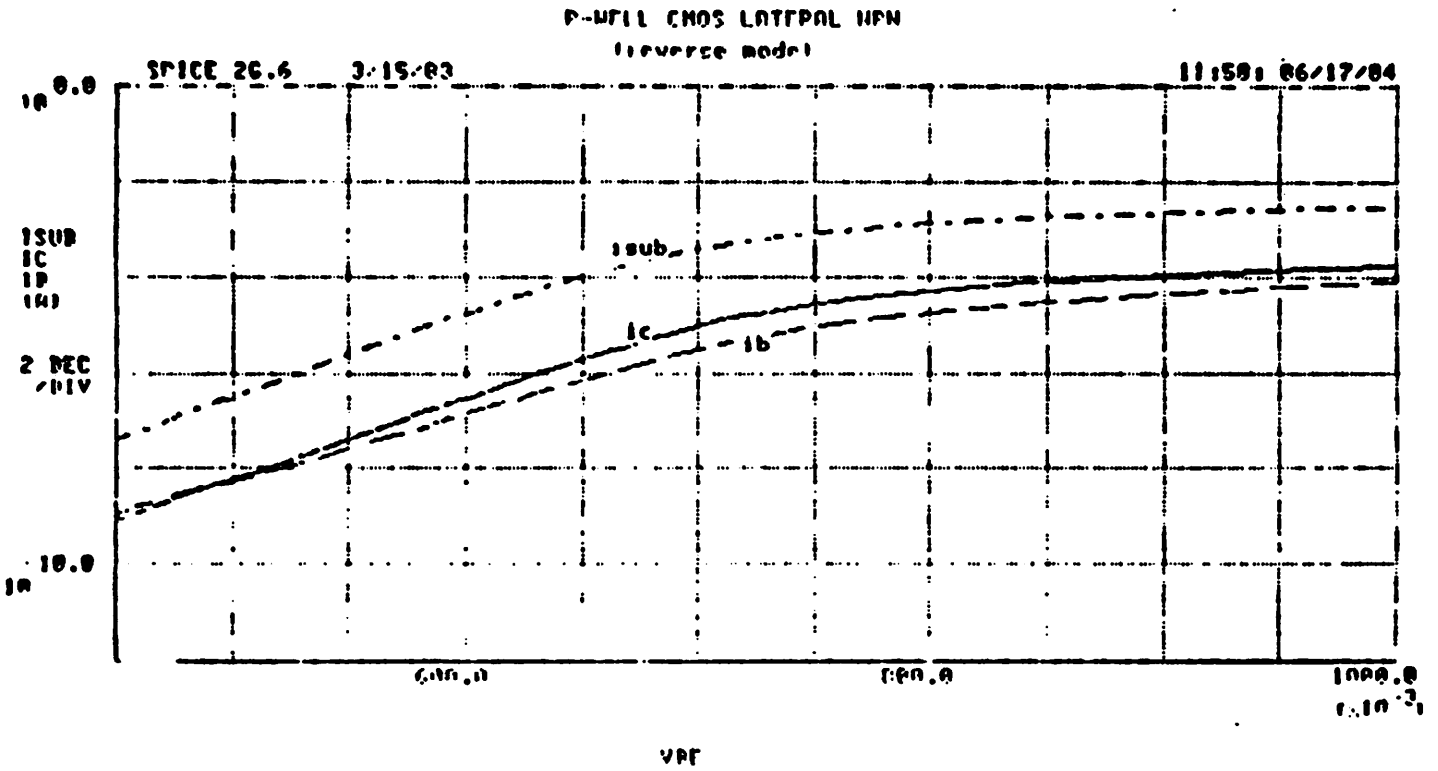


Fig.(6c) I_c, I_{sub} and I_b Vs V_{BE} (Reverse mode).

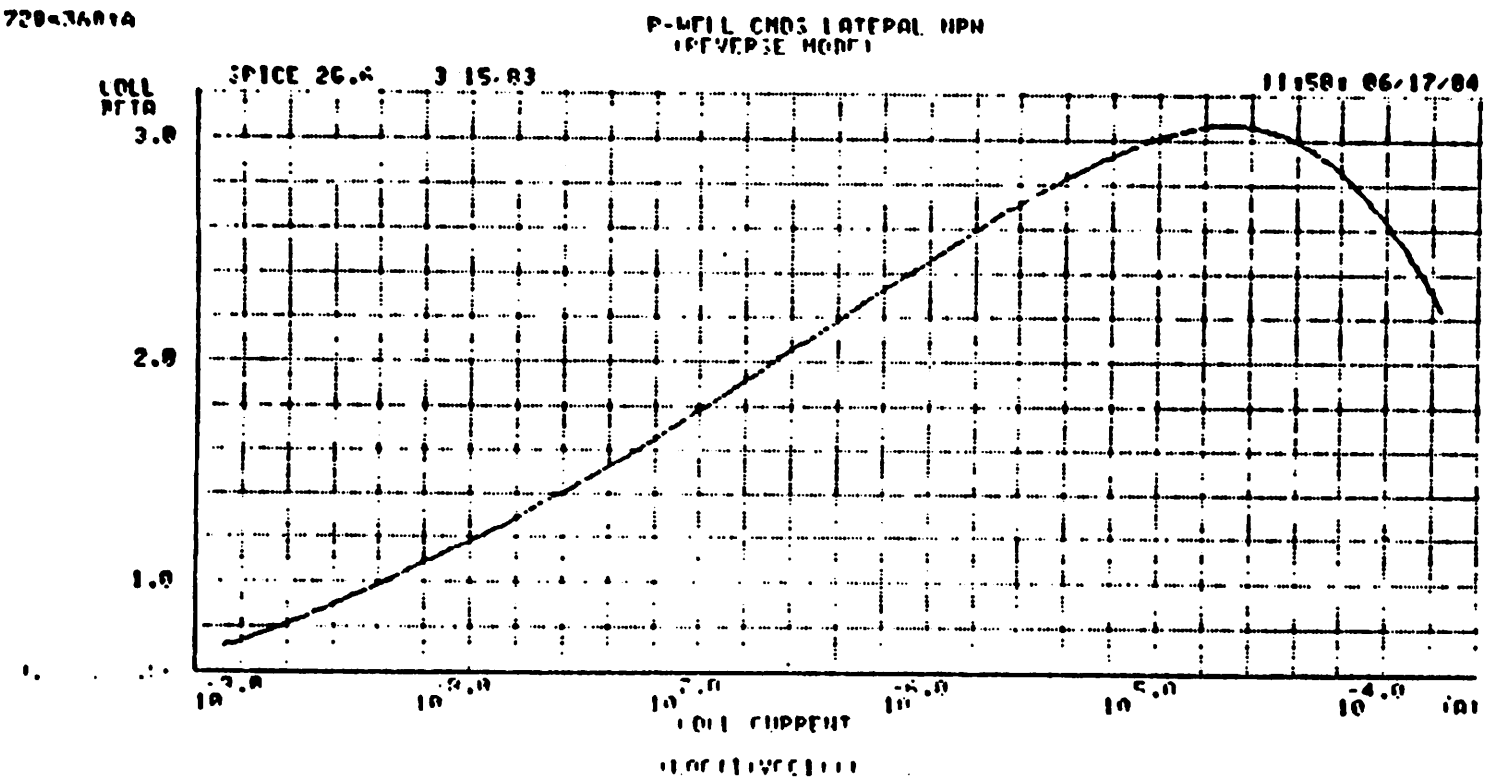


Fig.(6f) β_r Vs I_c (Reverse mode).

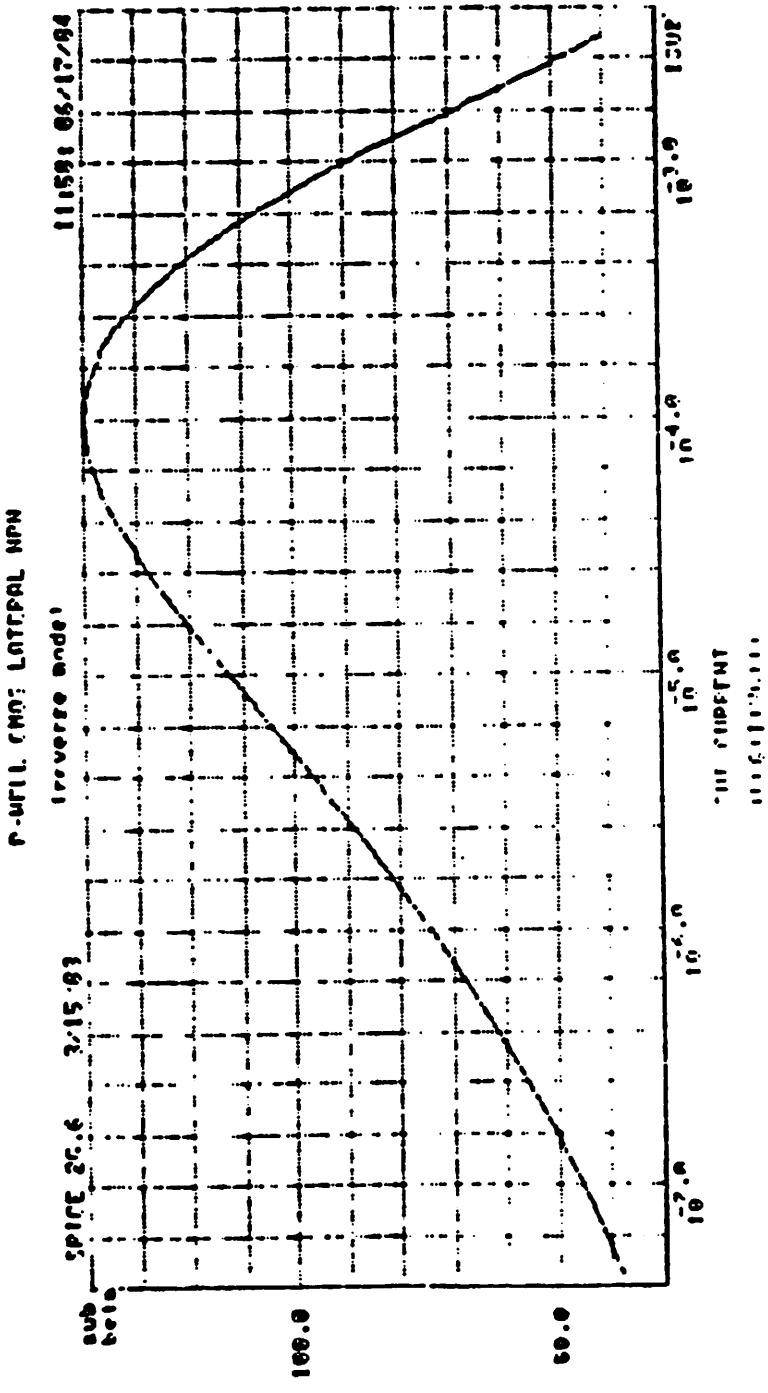


Fig.(6g) β_{SUB} Vs I_{SUB} (Reverse mode).

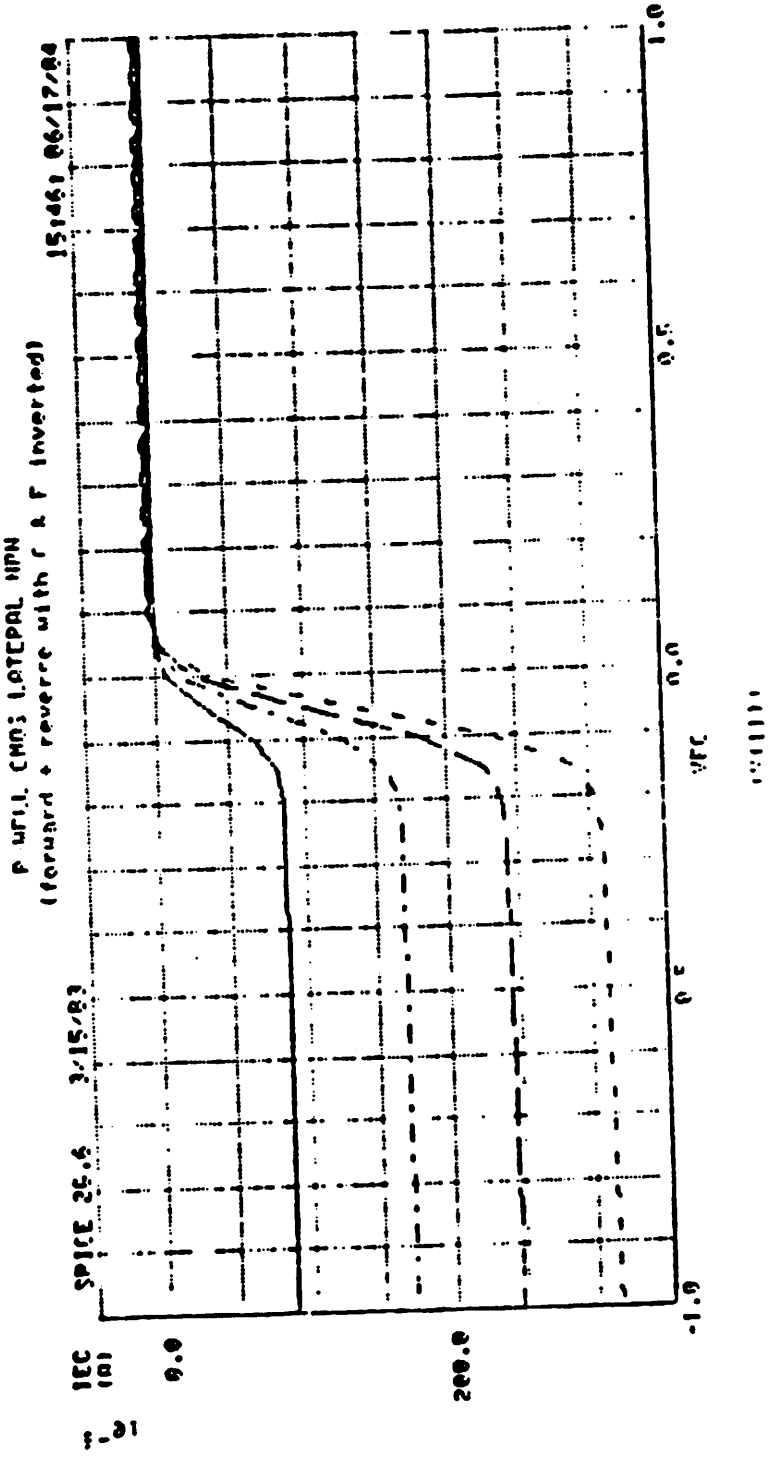


Fig.(6h) I_c Vs V_{ce} characteristics (Reverse mode).

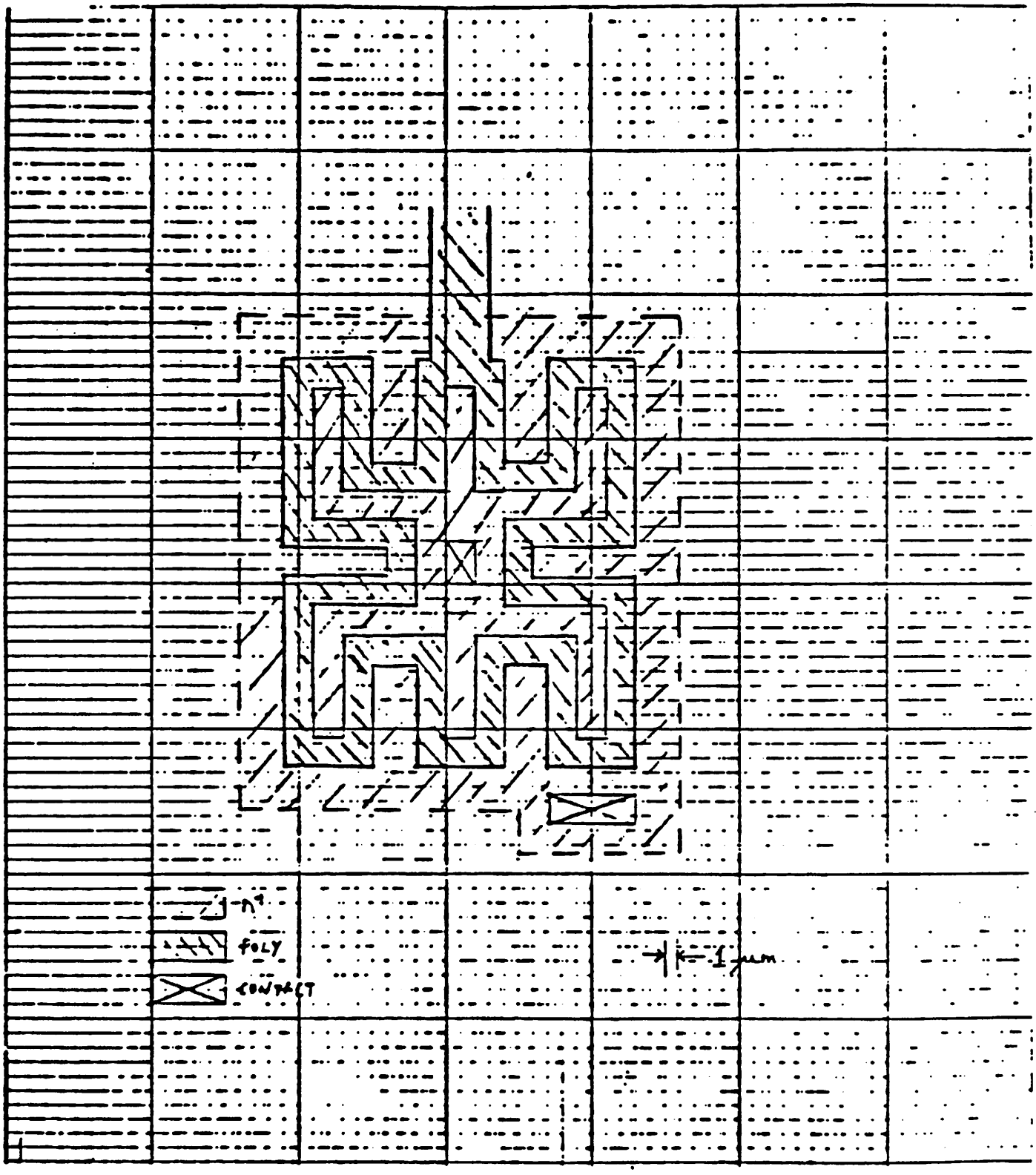


Fig.(7) Improved lateral bipolar transistor structure.

CHAPTER 3

PRECISION OPERATIONAL AMPLIFIER

3.1. Introduction

The inherent capability of very large scale integration of the MOS technologies has resulted in their seemingly ever increasing importance in the IC industry. Although much effort has been put into the investigation of the potential of MOS technologies for analog integrated circuits in the past decade [7], existing monolithic precision operational amplifiers which have high gain, low offset, low offset drift and good noise performance are fabricated using bipolar technologies. To realize the ultra-low offset property, active trimming at wafer probe stage is generally employed in these amplifiers [8]. Tremendous cost advantage can be achieved if :

1) Amplifiers with comparable performance can be fabricated using MOS technologies. This capability thus allows large-scale integrated circuits for high-performance analog-digital circuit functions be realized on the same chip.

2) Circuits with self-calibrating capability on a critical parameter can be realized in standard MOS technology. This would eliminate the need for the special instrumentation as well as the extra testing time required to perform active trimming.

3.2. Basic Circuit Configuration

Fig.(8) shows the block diagram of the amplifier. In order to make best use of the low 1/f noise and well-match properties of the lateral bipolar transistors available in standard CMOS process, they are used as the input devices of the differential operational

amplifier.

In general, the simpler the input stage of any amplifier, the better its noise and offset performance. The simplest input stage is an emitter coupled pair with resistive loads. This is then followed by a high gain stage and a low gain output stage.

3.3. Detailed Circuit Description

3.3.1. Input Stage

The schematic of the input stage is shown in Fig.(9). Since the base width of the input devices are made to be very narrow, to avoid punch-through between the collector and emitter, Vcb is kept small and constant by the boot-strapping circuit (M4I - M8I).

In order to have good common-mode rejection, a current source must be used as the "tail" of the emitter coupled pair. This current source defines the biasing current of the input stage. However, not all the current from this current source will run through the resistive loads. This is due to the presence of the substrate collectors. Therefore, M1I - M3I and Q1I are needed to generate the proper biasing for the input stage. Q1I is used to simulate the required amount of emitter current that would provide the desired lateral collector currents to the input transistor pair.

The gain (A_1) of the input stage is given by :

$$A_1 = g_{m(Q1)} R \qquad (4)$$

and A_1 is arranged to be approximately 17 in the circuit described here.

3.3.2. Second Stage

Fig.(10) shows the second stage schematic. Q1D and Q1E serve as level shifter. While the rest of the second stage is a folded tripple cascode high gain stage. The only

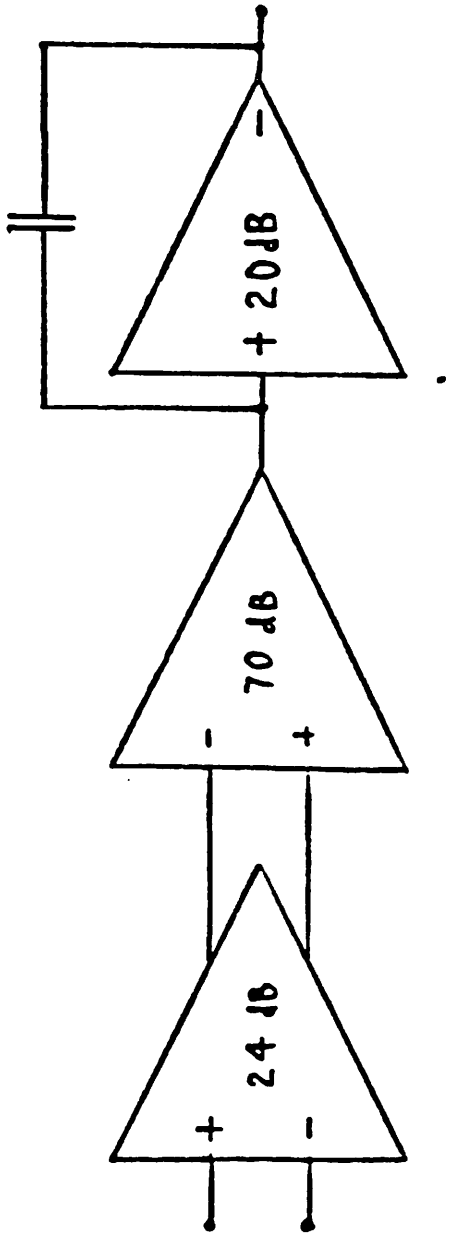


Fig.(8) Amplifier block diagram.

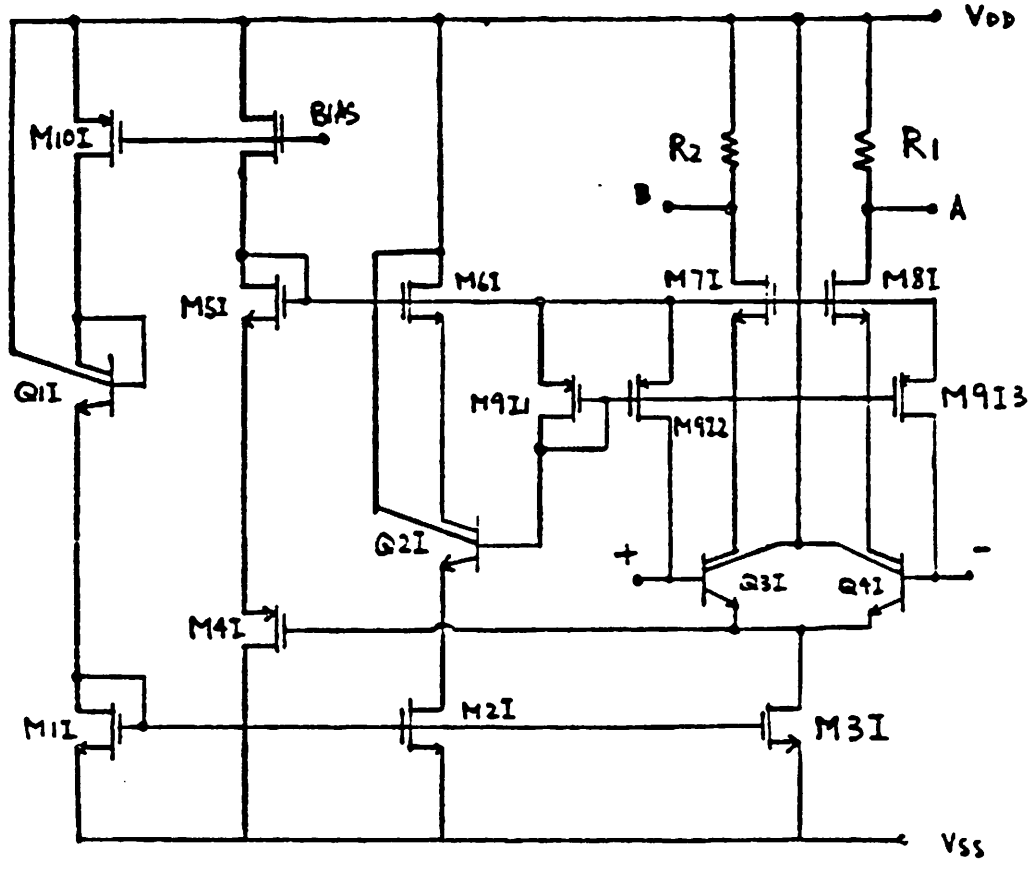


Fig.(9) Input stage schematic.

difference from the standard cascode gain stage is that transconductance reduction is also performed at the same time. Transconductance reduction is applied here instead of at the input stage because we cannot afford to lose any voltage gain at the input stage for noise and offset performance reasons.

The effectivre Gm from the first stage inputs to the second stage output is given by :

$$Gm = (g_{m(Q11)} R_1 X g_{m(M1D)}) \frac{1}{n} \tag{5}$$

and the gain (A_2) of the second stage is given by :

$$A_2 \approx [g_{m(M4D)} (r_{o(M1D)} // r_{o(M3D)}) g_{m(M5D)} r_{o(M4D)} r_{o(M5D)}] \frac{g_{m(M1D)}}{2n} \tag{6}$$

3.3.3. Output Stage

Fig.(11) shows the schematic of the low gain output stage. A pole-split capacitor Ccom is connected between the input and output of this stage. The gain of this stage (A_3) is given by :

$$A_3 = \frac{g_{m(M5B)}}{g_{m(M11B)}} g_{m(M23B)} RL \tag{7}$$

under quiescent conditions.

Although the gain of this stage is load and signal dependent, the pole split action of Ccom will retain stability of the circuit. Two small capacitors (Ccom1 and Ccom2) are also included to smooth out the response of the output stage.

3.4. Frequency and Transient Response

Standard single-pole compensation is used for this amplifier. The unity gain frequency is given by :

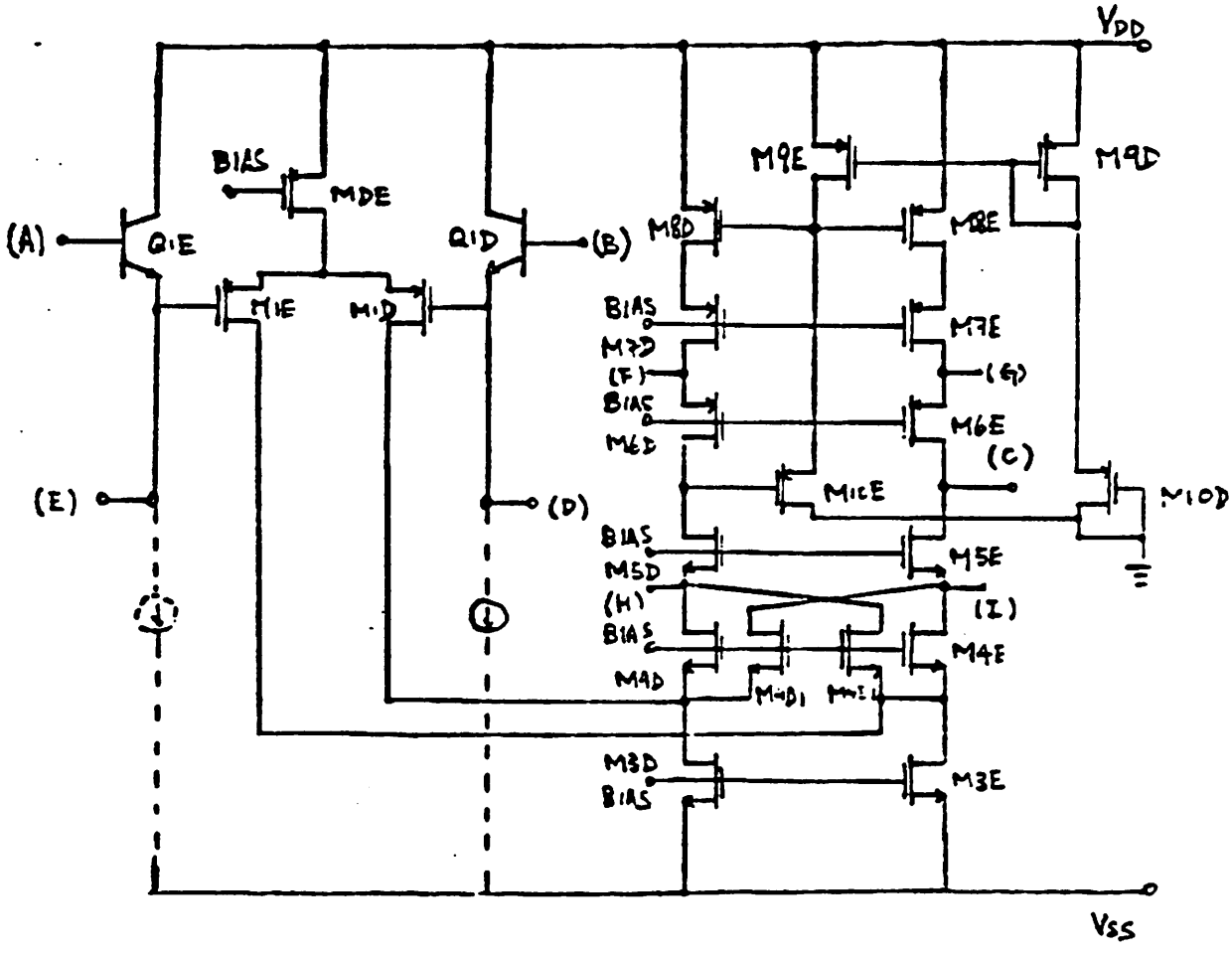


Fig.(10) Second stage schematic.

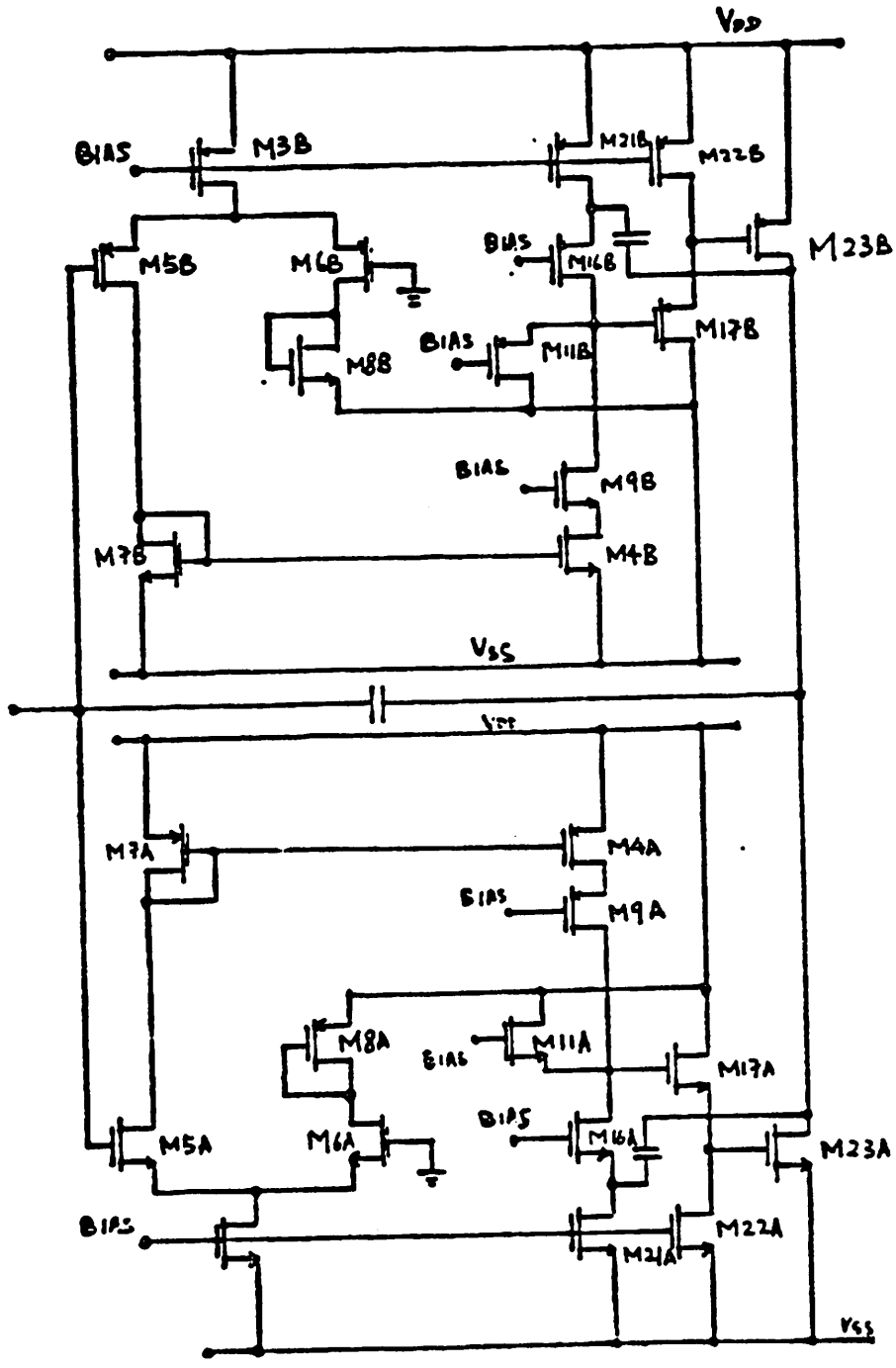


Fig.(11) Output stage schematic.

$$\omega u = \frac{Gm}{Ccom} \tag{8}$$

and the Gain-Bandwidth Product (GBP) is therefore given by :

$$GBP = A_1 A_2 A_3 \left(\frac{Gm}{Ccom}\right) \tag{9}$$

SPICE simulation of the open-loop frequency response of the complete amplifier with RL = 2 k Ω and CL = 100 pF loading is shown in Fig.(12a). Fig(12b) shows the amplifier frequency response with CL = 100 pF and no RL. As expected, stability is maintained due to the pole-split action of the compensation capacitor.

For ± 2.5 V supplies, common mode range at the input is limited by the bootstrapping ciucuitry. Hence an input voltage of 0.5 V is used for the transient response analysis. The amplifier is connected in a gain of two configuration with CL =100 pF and RL = 2 k Ω This transient response is shown in Fig.(13).

3.5. Input Bias Current Compensation Circuit

Many different techniques can be used for bias current compensation. A commonly used method is shown in Fig.(14a). This compensation scheme increases input current noise by a factor of $\sqrt{2}$ because the cancelling current noise is uncorrelated to the input transistor current noise. This is the case of the bias current cancellation network used on the OP-07 amplifier [9], where the noise currents of Q1 and Q3 [Fig.(14a)] are uncorrelated. The circuit shown in Fig.(14b) does not suffer from this problem. Since the noise currents of both M912 and M913 originate from the same source, the base current of Q21, and thus are correlated. With balanced source resistors the cancellation noise currents represent a common-mode component, and therefore do not add to the input current noise [10]. Another advantage offered by this circuit is that the Vce of Q21, Q31 and Q41 are forced to be the same which would allow close to perfect base current simulation by Q21 (

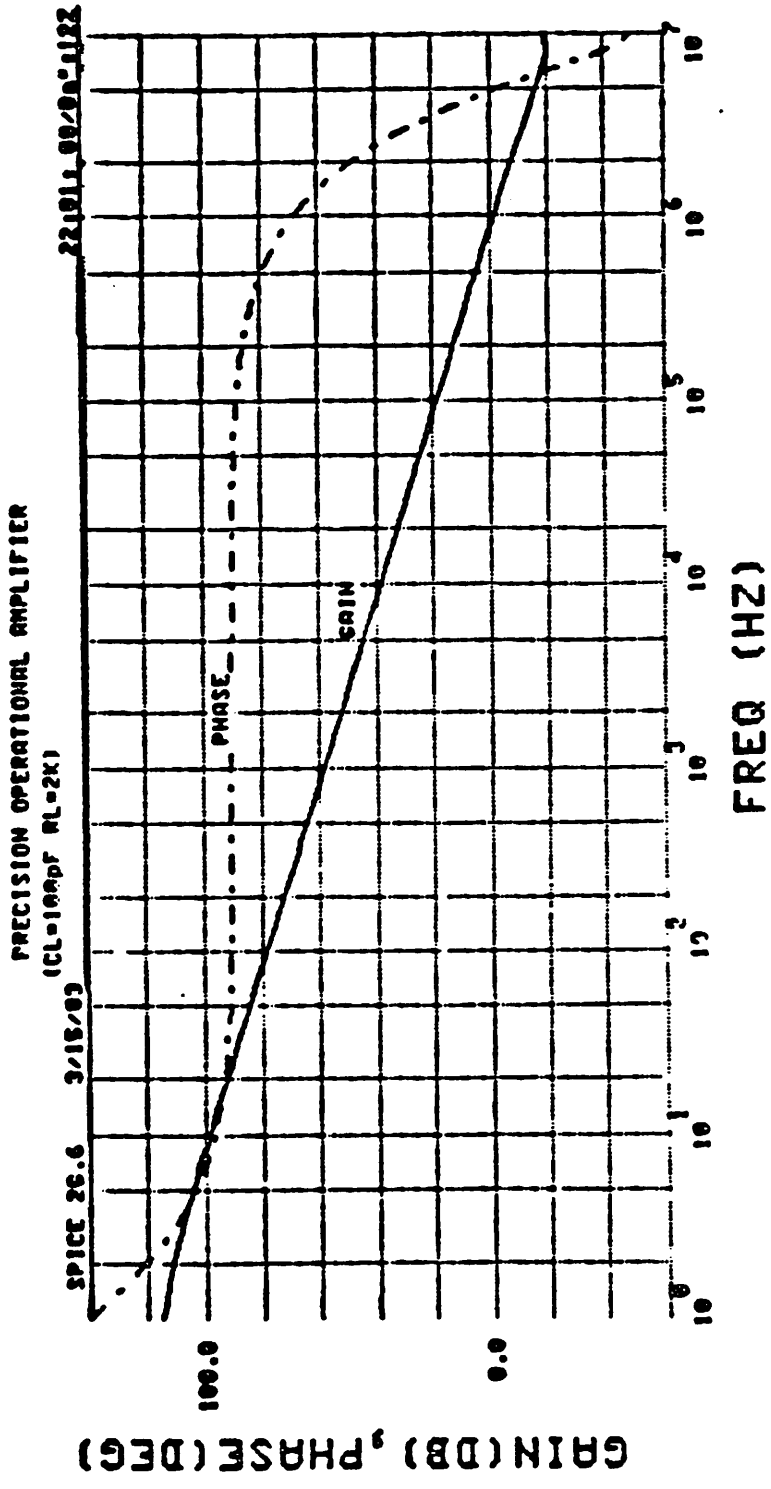


Fig.(12a) Frequency response (RI. = 2 kΩ and CL = 100 pF).

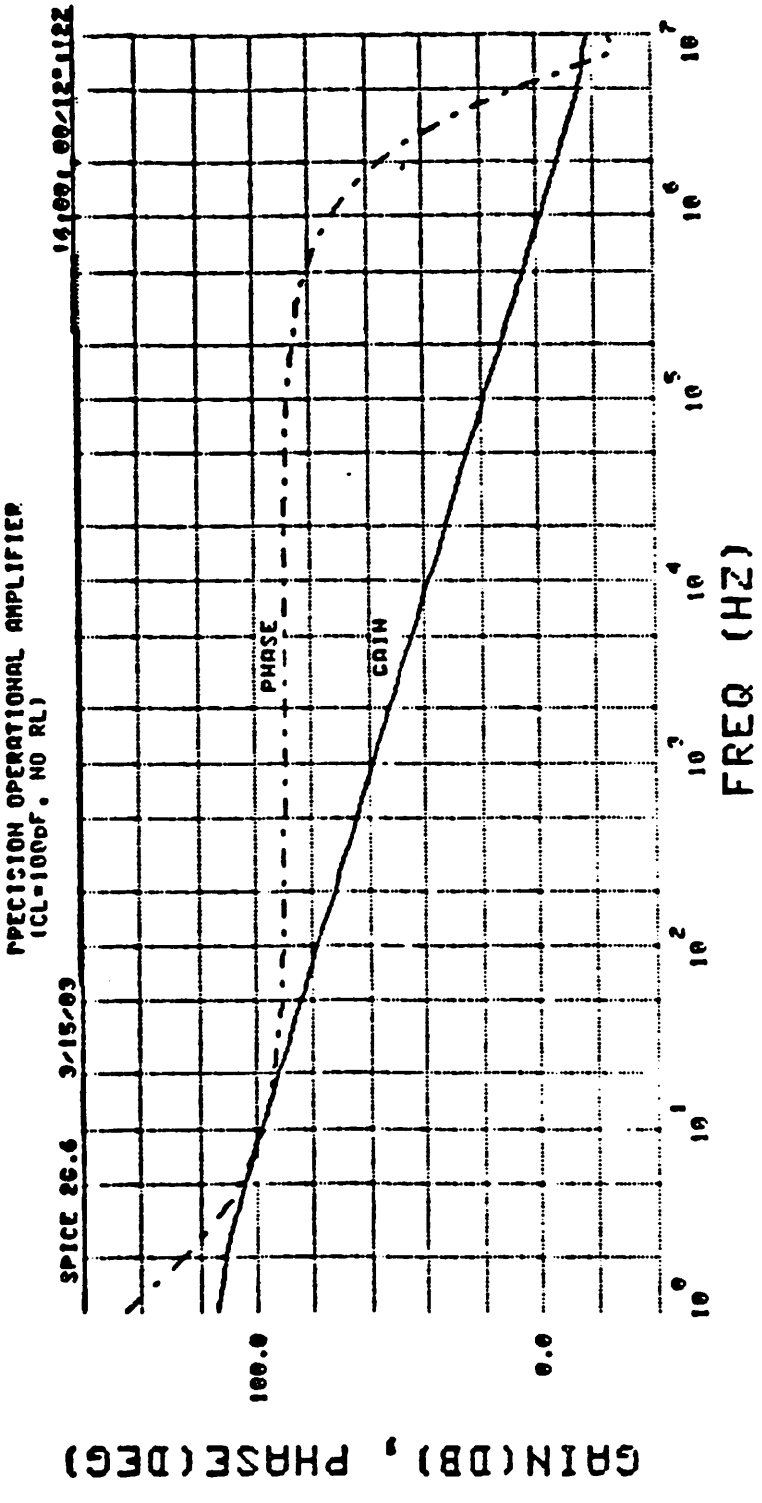


Fig.(12b) Frequency response (no RL and CL = 100 pF).

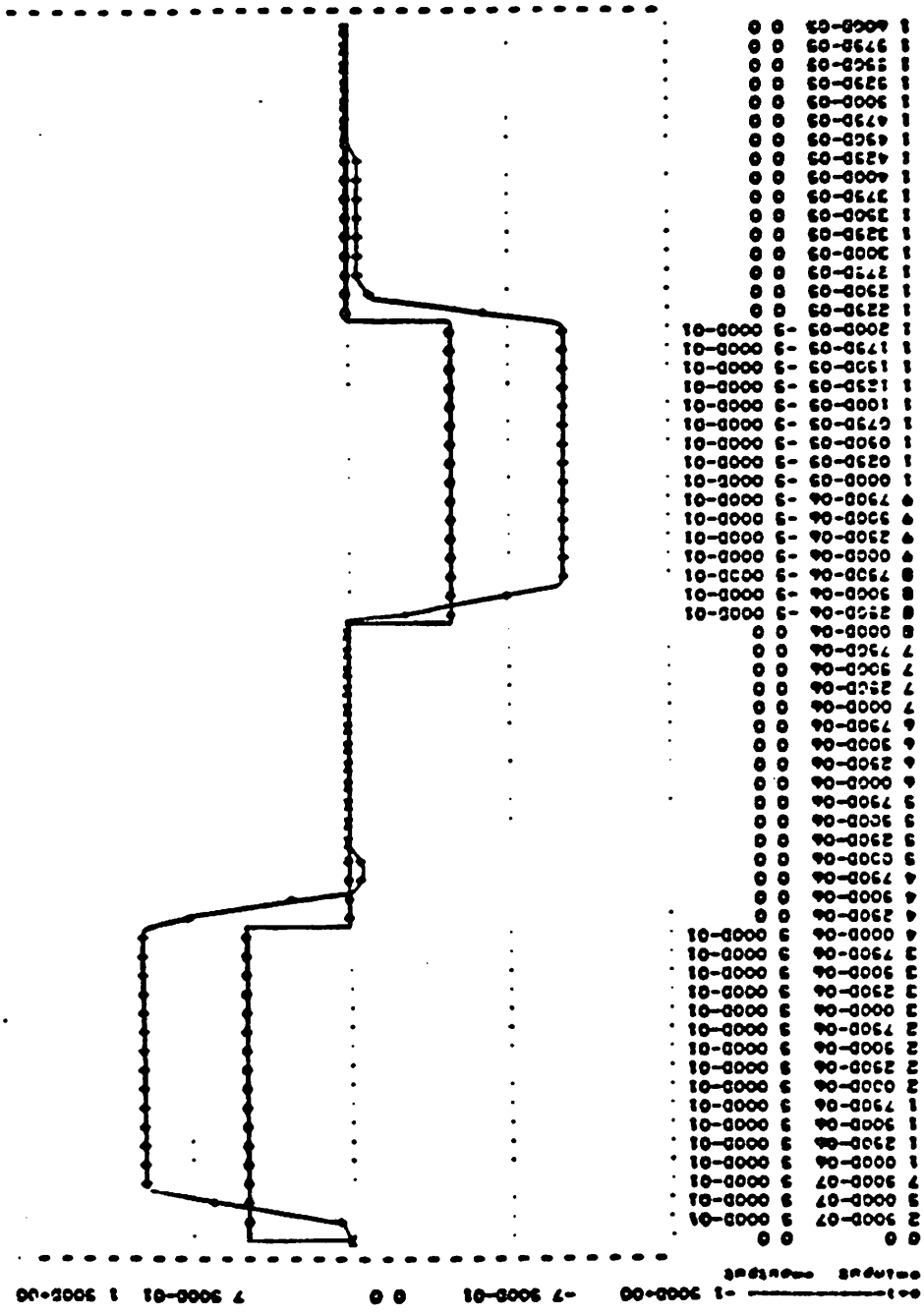


Fig.(13) Transient response (RL = 2 k Ω and CL = 100 pF).

i.e. there would not be any Early effect involved). Unfortunately, the circuit cannot be easily realized using the 5-terminal lateral device for the following reasons :

(a) For a PNP version of the 5-terminal device (available in standard N-well CMOS process), β value as low as 50 is expected.

(b) The existence of the substrate device in parallel with the lateral transistor.

Both (a) and (b) generate uncertainties in the value of Is3 [refer to Fig.(14b) : since Is1 $\neq$ 3(Is3)] required to give proper biasing conditions.

(c) The presence of any parasitic capacitance (say in the range of 0.05 pF) at the base of Q2I will create tremendous problem. This can be explained as follows :

Suppose a negative swinging common mode signal is applied to the differential inputs, the emitter of Q2I will swing downward. The presence of the parasitic capacitanc will, however, prevent the base of Q2I to follow. As $V_{be(Q2I)}$ increases, Q2I will go into saturation and a large amount of current will be injected through the substrate to both the collector and emitter terminals. This phenomenon is demonstrated clearly in Fig.(5d). Therefore, we cannot afford to allow any of the 5-terminal device in the amplifier to go into saturation under normal operating conditions.

Several configurations can be used to improve on the problems described above, they are shown in Fig.(14c), Fig.(14d) and Fig.(14e) respectively.

The circuit in Fig.(14c) provides a solution to problems (a) and (b), but it still suffers from the third problem. In order to solve problem (c), the circuit must be configured in such a way that Q2I will not go into saturation. Both Fig.(14d) and Fig.(14e) satisfy this

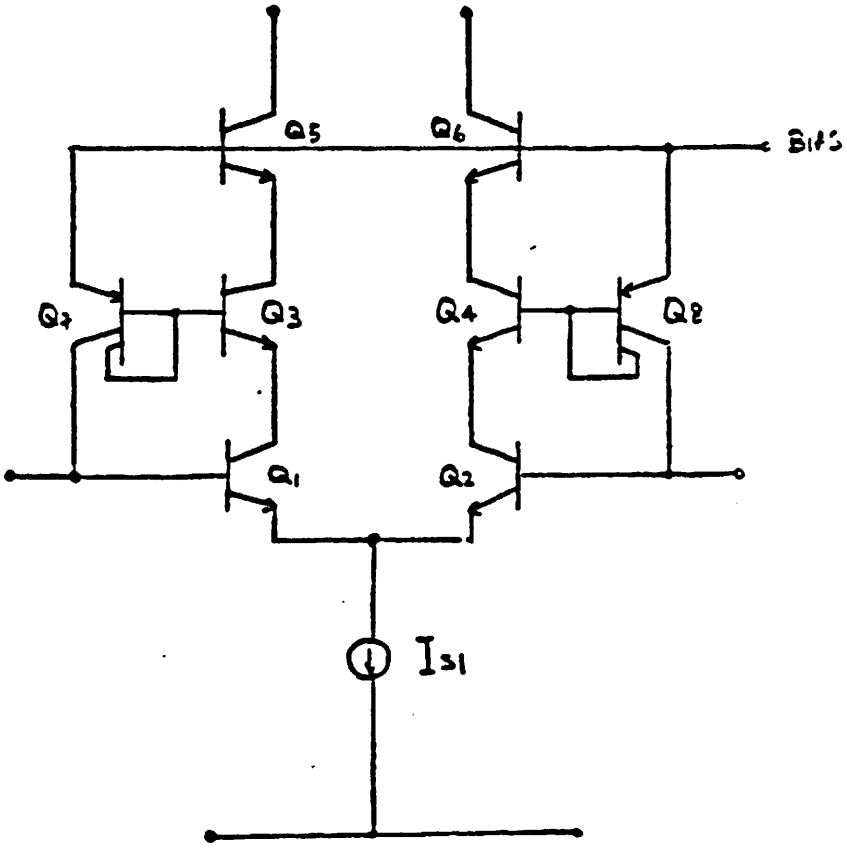


Fig.(14a) Base current compensation scheme used in OP-07.

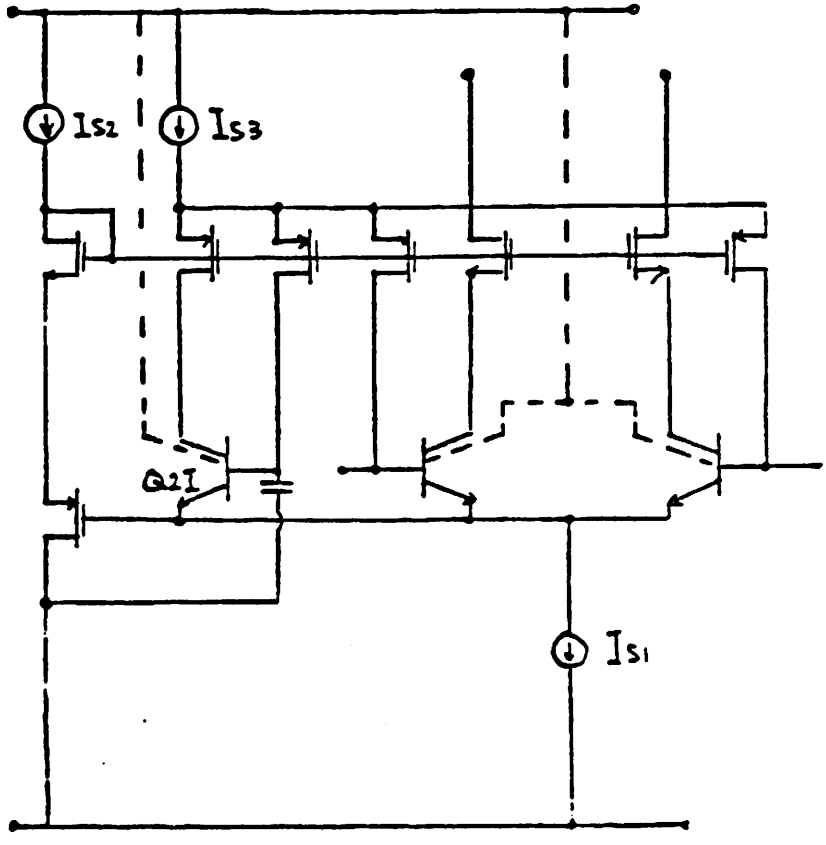


Fig.(14b) Improved base current compensation scheme.

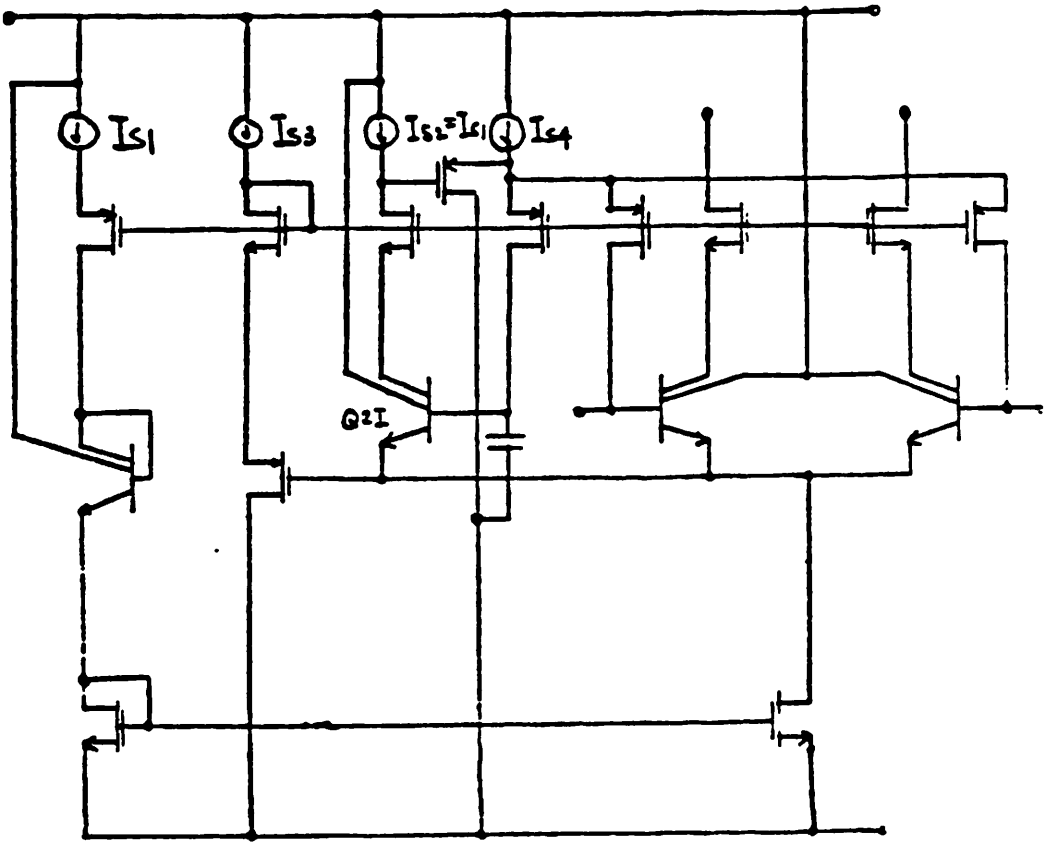


Fig.(14c) Base current compensation scheme [improvement on Fig.(14b)]

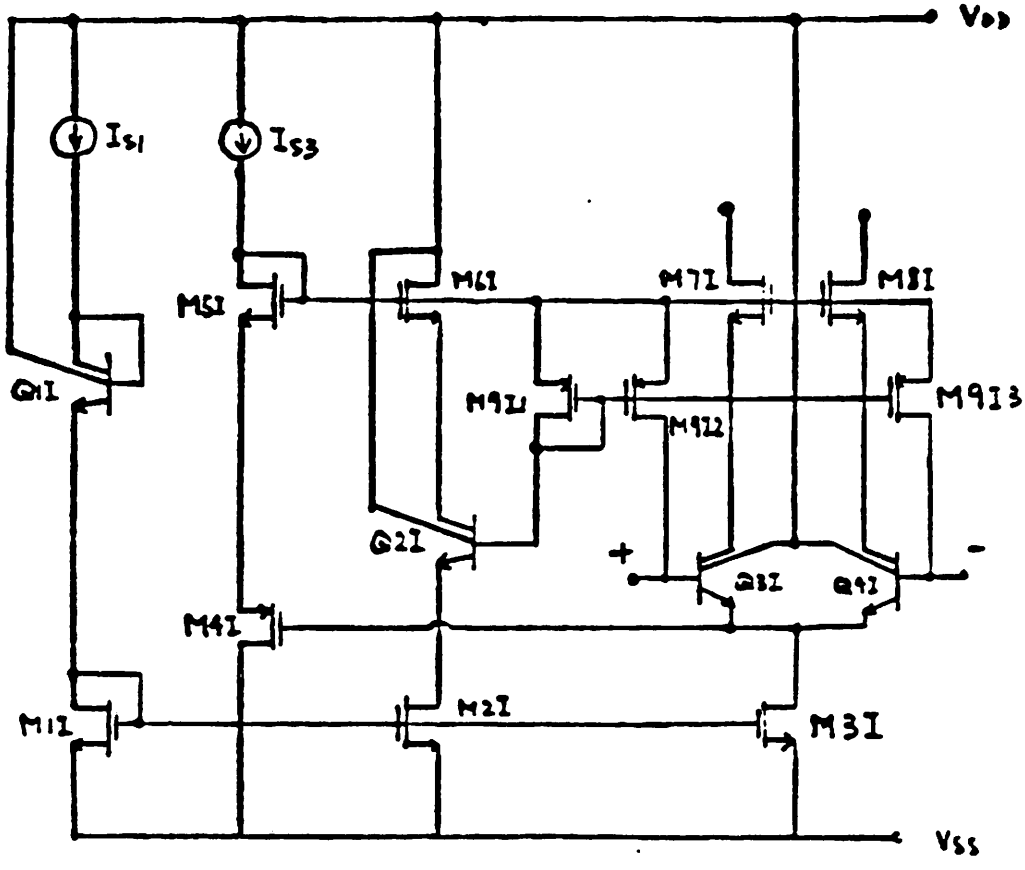


Fig.(14d, Base current compensation scheme-A [improvement on Fig.(14c)]

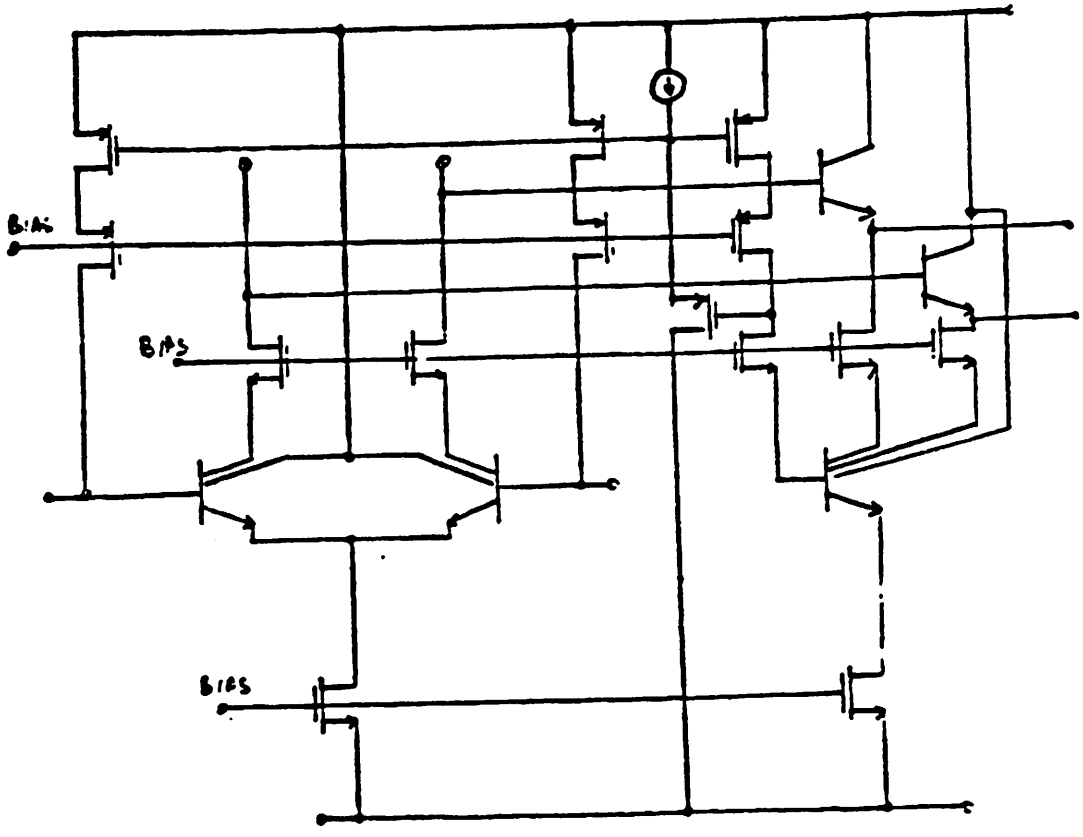


Fig.(14e) Base current compensation scheme-B [improvement on Fig.(14c)]

requirement. Note that in both cases :

1) The emitter of Q2I is removed from the emitters of the input pair.

2) Emitter of Q2I is sitting on top of a current source so that it can move "freely" and no slewing problem is expected.

3) The collector current of Q2I is defined from the emitter rather than by forcing a current into the collector directly.

It can easily be shown that Q2I will not go into saturation at all time.

The circuit in Fig.(14d) is chosen as the input stage in the present design because it is simpler than the one in Fig.(14e).

In general, ~ 95% compensation in base current is achieved in practice. Hence, for βc = 50 and Ic = 10 μA, Ib = 200 nA. For 95% compensation, we would expect input bias current to be 10 nA.

3.6. Slew Rate Enhancement Circuit

3.6.1. Transfer Characteristics

Fig.(15) shows the slew rate enhancement circuit. The two bipolar transistors Q15D and Q15E are normally off, they turn on only when the circuit is under large signal transient. Therefore, this enhancement circuit does not affect small signal, noise and offset performace of the amplifier.

From Fig.(15),

$$V_{in} = V_d - V_e \qquad (10)$$

$$V_o = V_a - V_{BE(N1D)} - V_{GS(N12D)} + V_{GS(N13D)} + V_{BE(N1E)} \tag{11}$$

$$V_{BE1D} = V_T \ln\left[\frac{I_{(N12D)} + I_{(N18E)}}{I_{s1}}\right] \tag{12}$$

$$V_{BE1E} = V_T \ln\left[\frac{I_{(N12E)} + I_{(N18D)}}{I_{s2}}\right] \tag{13}$$

$$V_{GS(N12D)} = V_{th} + \sqrt{\frac{2I_{(N12D)}}{\mu C_{ox} W/L}} \tag{14}$$

$$V_{GS(N13D)} = V_{th} + \sqrt{\frac{2I_{(N13D)}}{\mu C_{ox} W/L}} = Va = constant \tag{15}$$

$$I_{(N13D)} = I_{(N13E)} = I_a = constant \tag{16}$$

Combining equations (10) to (16), i.e.

$$V_{in} = V_T\left[\ln\left(\frac{I_{(N12D)} + I_{(N13E)}}{I_s}\right) - \ln\left(\frac{I_{(N12E)} + I_{(N13D)}}{I_s}\right)\right] - V_a + V_{th} + \sqrt{\frac{2I_{(N12D)}}{\mu C_{ox} W/L}} \tag{17}$$

For large positive Vi, $I_{(N12E)}$ will go to zero and equation (17) becomes :

$$V_{th} - V_{in} - V_a = V_T \ln\left[\frac{I_a}{I_a + I_{(N12D)}}\right] - \sqrt{2\frac{I_{(N12D)}}{\mu C_{ox} W/L}} \tag{18}$$

The value of $I_{(N12D)}$ can be solved iteratively as a function of Vi, and $I_{(N15D)}$ is then given by :

$$I_{s(N15D)} = I_{s(N15)} exp\left[\frac{I_{(N12D)} R_{1D} + I_{(N5f)} R_{1D}}{V_T}\right] = I_{s(N15)} C_1 exp\left[\frac{I_{(N12D)} R_{1D}}{V_T}\right] \tag{19}$$

where $C_1 = exp\left[\frac{I_{(N5f)} R1D}{V_T}\right]$

The transfer characteristics of the enhancement circuit is shown in Fig.(16).

3.6.2. Enhancement Circuit Threshold Temperature Tracking

It is important for the circuit threshold to have a similar temperature coefficient to that of a base-emitter voltage. The current $I_{(M5_E)}$ is given by :

$$I_{(M5_E)}=C_2[\frac{V_{BE1G}}{R_{1G}}] \tag{20}$$

Therefore, the base voltage of Q_{15D} is :

$$V_{BE15D}=(I_{(M12D)}+I_{(M5_E)})R_{1D} \qquad =C_2V_{BE1G}+C_3V_T \tag{21}$$

Where C_2 and C_3 are constants. Hence, if we make C_2V_{BE1G} as the dominant term, the base voltage of $Q15D$ will track with the base voltage of V_{BE1G}.

3.7. Noise Performance

In general, MOS devices are considered to be noisier than their bipolar counterparts. Hence, in order to improve the noise performance of amplifiers to be fabricated in standard CMOS process, lateral bipolar transistors are used as the differential input pair. Also, it is important to have passive 1st stage loading, and to allocate reasonable amount of 1st stage gain. This 1st stage gain is require to reduce the noise contribution from the subsequence stages. The use of cascoded configuration is encouraged, because the common-gate devices do not contribute a significant amount of noise.

The 1/f noise equations from the BDM model for MOS devices in SPICE2 has been shown to be incapable to describe the true nature of noise behavior, and it can only be used as a noise fitting equation for already known values of mean square noise voltage [11]. Therefore, 1/f noise is assummed to be zero when noise analysis was performed using

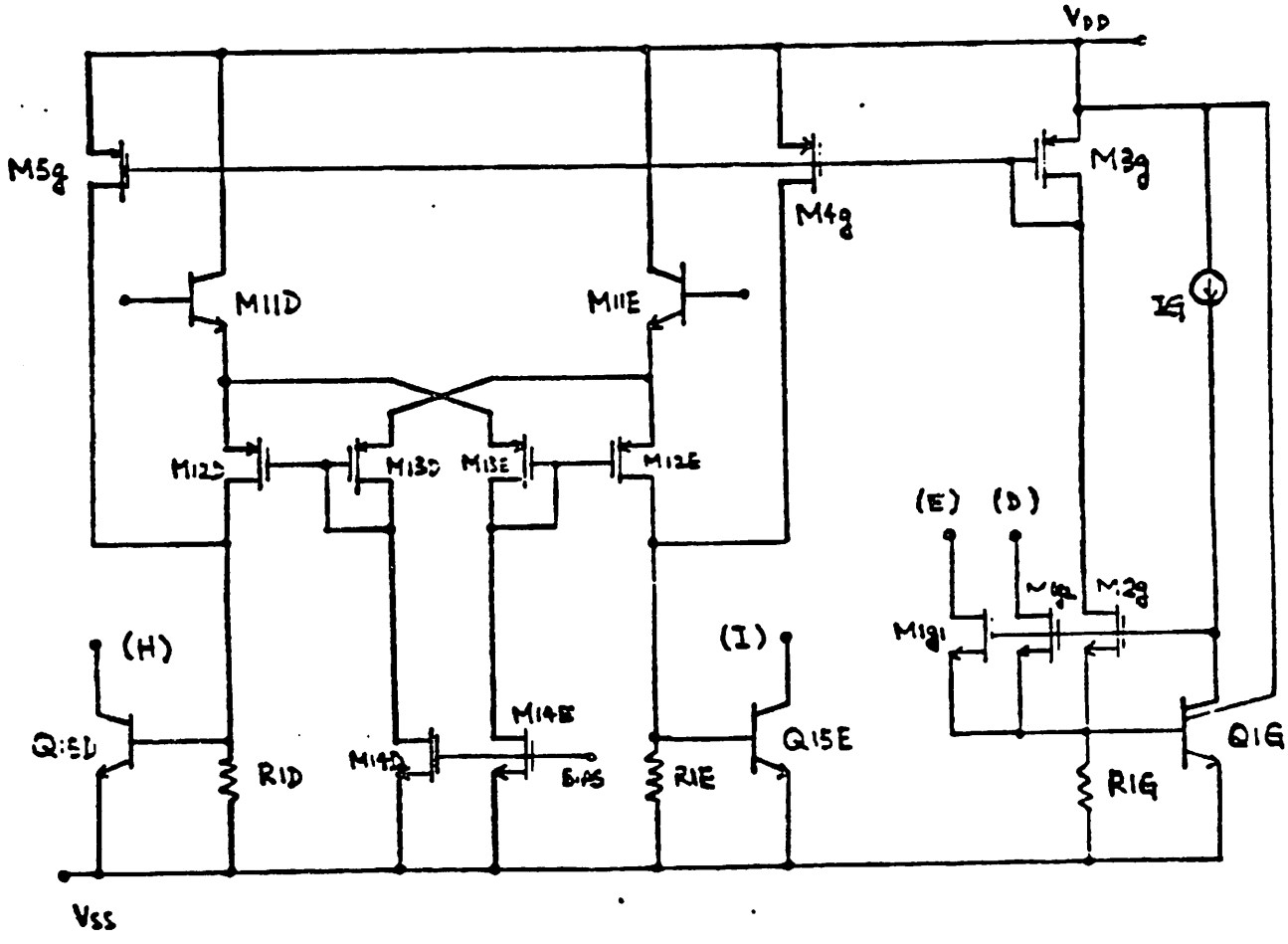


Fig.(15) Slew rate enhancement circuit.

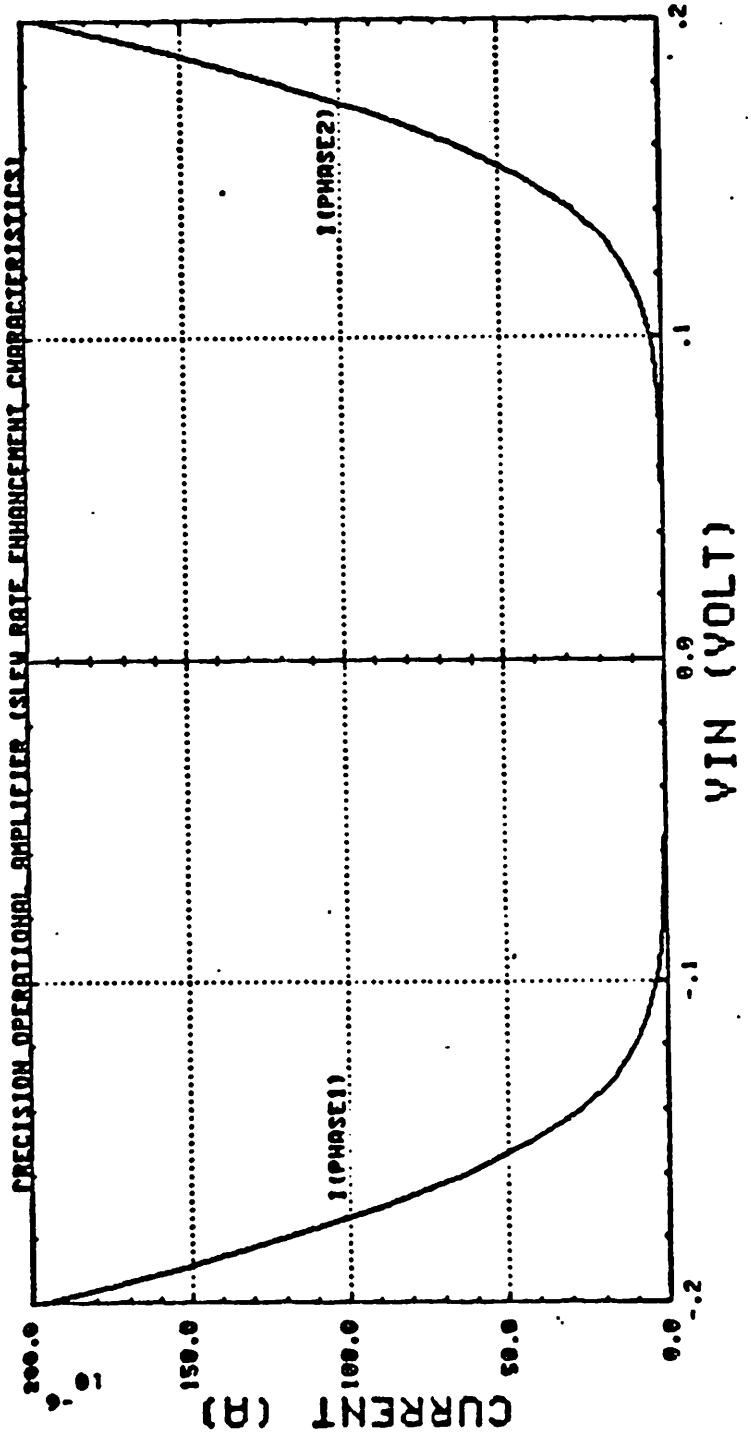


Fig.(16) Slew rate enhancement transfer characteristics.

SPICE.

3.7.1. Noise Performance (1/f Noise Excluded)

Excluding the noise contributions of the two external feedback resistors, the noise denisity at 1 kHz is 8.5 nV/$\sqrt{Hz}$. This is comparable to the noise performance of most bipolar operational amplifiers with similar general characteristics.

3.7.2. 1/f Noise Performance Considerations

Normal lateral bipolar transistors are surface devices and therefore in general have higher 1/f noise than vertical transistors. The lateral bipolar transistors used in this amplifier, however, do not suffer from this problem. This is because when a negative voltage is applied to the gate of the devices, the surface is accumulated. The gate essentially becomes a field plate and will push the minority carriers travelling across the base away from the surface. As a result, the 1/f noise of the device is therefore minimized. We will neglect the 1/f noise of the bipolar devices and will concentrate only on that of the MOS devices.

As mentioned earlier, cascoded devices in common gate configuration do not have significant noise contribution. Therefore, the dominant noise sources will be originated from M1D, M1E, M3D, M3E, M8D and M8E. The 1/f noise voltage of a MOS device is approximately independent of bias and can be estimated by :

$$\overline{V}_{i/f}^2 = \frac{K_{n,p}}{WLC_{ox}f}\Delta f \qquad (22)$$

Therefore, to minimize 1/f noise of the amplifier :

(1) Use large gate area for M1D and M1E

(2) Use long channel length for M8D and M8E

The W and L values of M3D and M3E are determined by the biasing circuit and cannot be altered easily. It is obvious that the noise contributions of the transistors mentioned above are equally important. The input-referred noise voltage is given by :

$$\overline{V}_{1/f(in)}^2=\frac{1}{A_1^2}[2\overline{V}_{1/f(M1D)}^2+2\overline{V}_{1/f(M3D)}^2+2\overline{V}_{1/f(M8D)}^2]\Delta f \qquad (23)$$

With M1 : W = 100 μm, L = 3 μm

M3 : W = 40 μm, L = 6 μm

M8 : W = 80 μm, L = 15 μm

and assume : $K_p=3\times10^{-24}V^2\text{-F}$ $K_n=6\times10^{-24}V^2\text{-F}$

At 1 kHz, i.e., $\overline{V}_{1/f(in)}=17.3\frac{nV}{\sqrt{Hz}}$

Hence, the total amplifier noise density is given by :

$$\overline{V}_n=\sqrt{\overline{V}_{1/f}^2+\overline{V}_{other}^2} \qquad (24)$$

and the total amplifier noise density at 1 kHz is approximately 20 nV/$\sqrt{Hz}$.

3.8. Untrimmed Offset Performance

With the advances of instrumentation, photolithographic and processing techniques, well matched component can be fabricated on the same chip with special precautions. For the same collector current, the V_{BE} matching of a pair of properly structured bipolar transistors can be better than 1 mV. If cross-coupled quadrature structure is used, the V_{BE} mismatch can be further reduced down to less than 0.5 mV. In this section, the untrimmed offset of the amplifier is estimated.

The input offset introduced by the input stage is first estimated [Fig.(9)]. As in the case of noise analysis, the common-gate cascoded devices do not contribute significant amount of offset, and the input stage can be simplified to simple emitter-coupled pair with resistive loads. The 1st stage offset (V_{os1}) is given by :

$$V_{os1}=V_T[\frac{\Delta Is}{Is}+\frac{\Delta R}{R}] \tag{25}$$

If special precautions have been taken during layout, less than 1% of resistor mismatch can be achieved [12]. For conservative estimation, assume 4% mistach in Is and 2% mismatch in resistors,

i.e. V_{os1} = 1.56 mV

The offset introduced by the bipolar pair at input of the second stage is given by :

$$V_{os2}=\frac{V_T}{A_1}[\frac{\Delta Is}{Is}+\frac{\Delta Ic}{Ic}] \tag{26}$$

where $\frac{\Delta Ic}{Ic}$ is the mismatch of the MOS current sources at the emitter of this level-shifting bipolar transistor pair.

Assumming 5% mismatch in both $\frac{\Delta Is}{Is}$ and $\frac{\Delta Ic}{Ic}$,

i.e. V_{os2} = 0.15 mV

If the rest of the second stage is assummed to introduce $\frac{5mV}{A_1}$, then $V_{os3}=0.29mV$. V_{os3} is mainly caused by mismatch in MOS transistors. Therefore,

$$V_{os}=V_{os1}+V_{os2}+V_{os3}=2mV \tag{27}$$

If trimming is performed and if the offset nulling voltage (V_{osn}) is proportional to T (temperature), then it is important to have the offset voltage (V_{os}) being also proportional to T. From the above results, both V_{os1} and V_{os2} are proportional to T while V_{os}

tends to stay constant with temperature. However, ($V_{os1}+V_{os2}$) >> V_{os3}, therefore, V_{os} is approximately proportional to T and offset drift is minimized.

CHAPTER 4

OFFSET SELF-CALIBRATING TECHNIQUE

4.1. Introduction

The concept of "self-calibration" has captured much attention recently. "Self-calibration" eliminates the "external" trimming required to adjust a certain critical parameter of the circuit. Hence, with proper implementation of this concept, tremendous cost saving in producing high-performance precision circuitry is possible.

4.2. Trimming Procedure

From section 3.8, the estimated V_{os} is 2 mV, which sets the minimum requirement of the upper limit of the trimming range. Noise, on the other hand, sets the lower limit of the achievable trimming range. It can be shown that the lower limit is approximately 45 μV (noise band = 1 MHz assummed). Hence, a minimum of 6-bit trimming accuracy is required to provide the above trimming range.

4.2.1. Trimming Approach Considerations

4.2.1.1. Voltage Controlled Offset Trimming - Approach A

The basic concept of this approach is to use a pass transistor to connect the input of the second stage to the proper tapping point along the resistor string of the first gain-stage. Fig.(17) shows one of the possible configurations required to implement this approach. It is

important to note that since no "mathematical addition" of voltages is available, in order to achieve 6-bit accuracy, 64 tapping points and 64 pass transistors will be required.

Advantage :

The introduced offset nulling voltage V_{osn} is proportional to T when referred back to the input. Hence V_{os} drift after trimming is minimized.

Disadvantage :

(1) The total value of resistors required is large. In other words, large area required.

(2) To maintain good overall balance at the differential input stage, the same resistor strings will have to be implemented on both sides of this differential gain stage and therefore takes even larger area than stated in (1) alone.

(3) As mentioned earlier, many tapping points and pass transistors are required.

4.2.1.2. Current-Controlled Offset Trimming - Approach B

A much more efficient trimming technique is shown in Fig.(18). This approach used binary weighted currents to generate the desired offset nulling voltage. But for 6-bit plus sign (i.e. 7-bit) accuracy, the required current ratio is relatively large and undesirable. To eliminate this problem, the trimming resistor is tapped into different sections of unequalled values. Hence, by connecting the binary weighted current sources to these different tapping points, a current ratio of only 4 is sufficient. Each of these current sources is either switched in or swithced out by a minimum size series pass transistor. The control signals for the switches are stored in a 7-bit×1 static RAM when the self-calibration is completed.

Advantages :

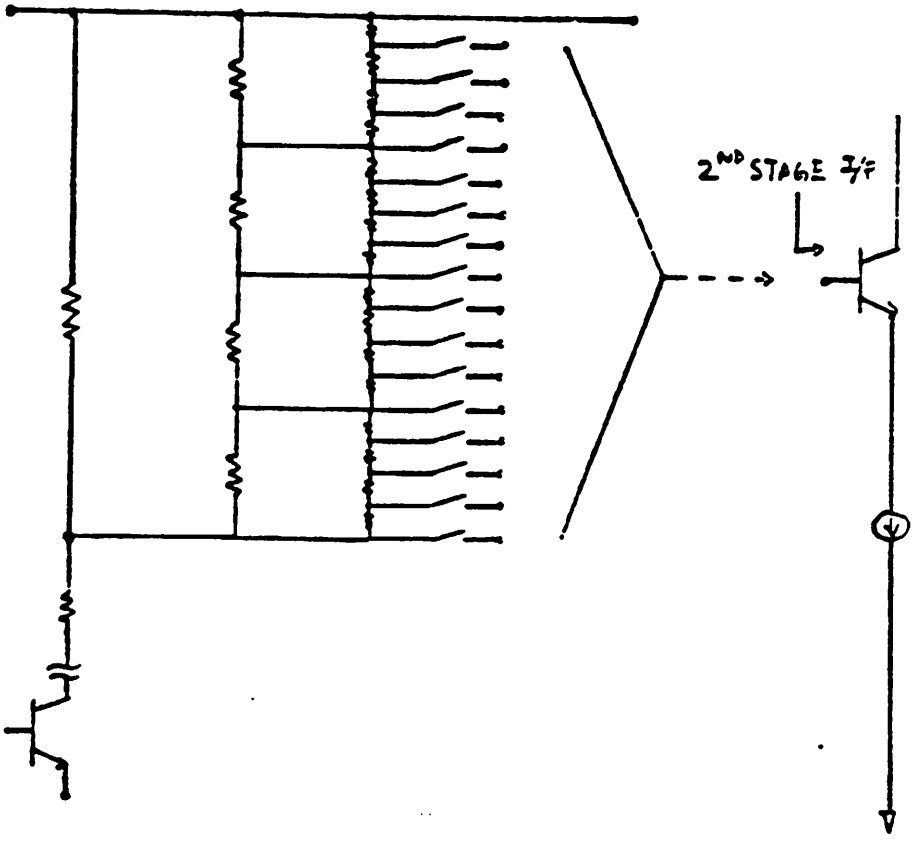


Fig.(17) Voltage controlled offset trimming.

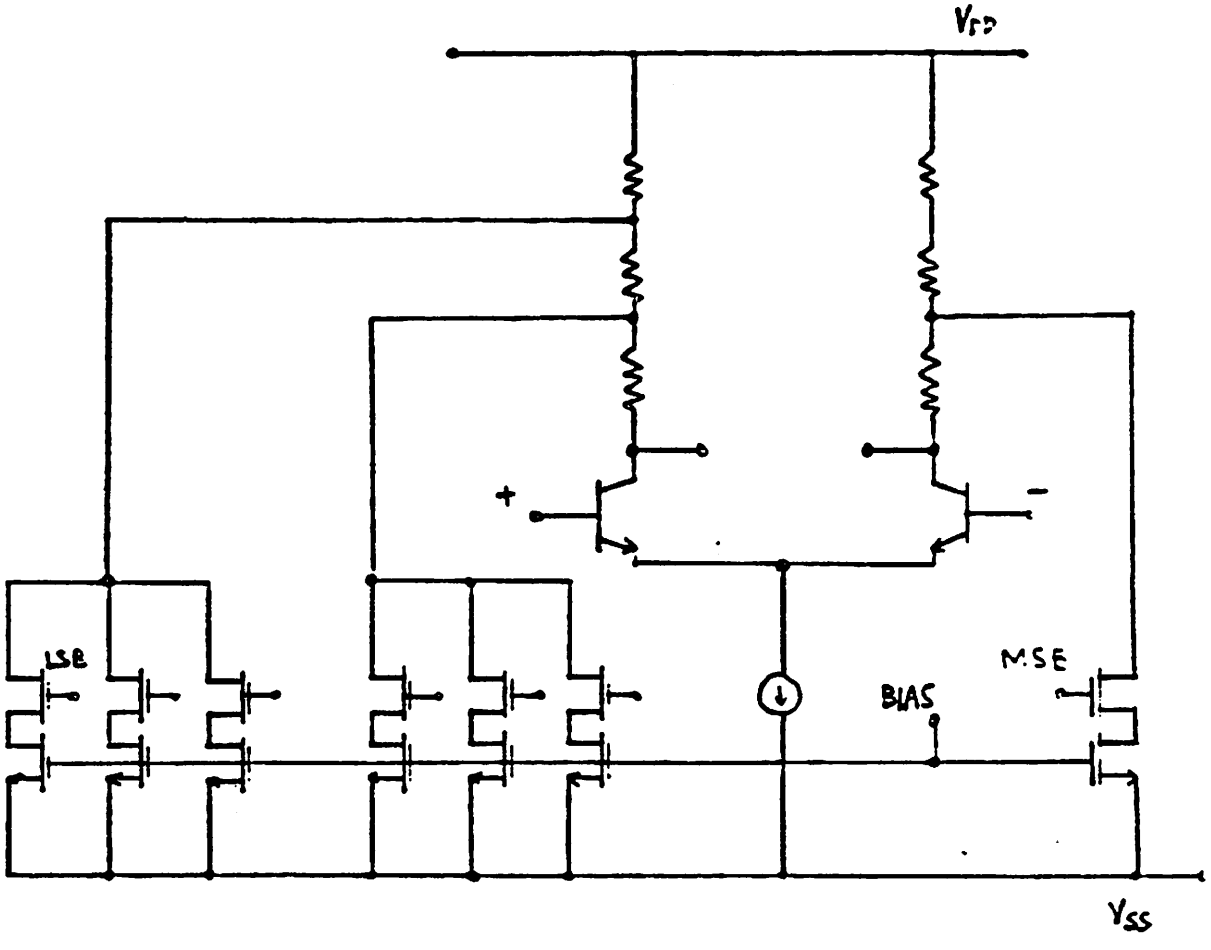


Fig.(18) Current controlled offset trimming.

(1) Relatively simple, only 15 transistors are required (excluding control circuit).

(2) Does not alter AC gain after trimming.

(3) Simple trimming algorithm.

(4) Only requires simple control logic circuit.

(5) The generated offset nulling voltage V_{osn} is proportional to temperature and offset drift is therefore minimized.

Disadvantages :

(1) Trimming is not inherently monotonic.

(2) Will introduce some noise into the amplifier. But this can be minimized to a negligible level by using long channel devices as current sources.

The proof of advantage (5) is given below :

Assume :

(a) The bias current of the 1st stage to be : $I = C_a \frac{V_T}{R_1}$

(b) The trimming currents : $I_T = C_b \frac{V_T}{R_2}$

Therefore, the input referred offset nulling voltage is given by :

$$V_{osn} = \frac{I_T R_T}{A_1} = C_c V_T \qquad (28)$$

where C_a, C_b and C_c are constants.

Hence, V_{osn} is proportional to T.

4.3. Trimming Procedure

In most applications, the opperational amplifier will be connected closed-loop by external feedback elements. In order to perform self-calibration, this external feedback loop must be opened "internally".

An externally applied START-UP (SU) pulse will initiate the self-calibration process. SU will reset the 7-bitX1 static RAM where the required trimming bit pattern will be stored. It will also set all the bits of a 4-bit down-counter at which the RAM address will be successively generated. The control signal CAL generated on chip will determine the time period required for the calibration, it also serves as a flag indicating that self-calibration is in progress.

Fig.(19) shows the required switching pattern to break the external feedback loop. Transistors MT5 and MT6 are OFF while MT1, MT2, MT3, MT4, MT7, MT8 and MT9 are ON. The output stage will be forced into a tri-state condition. Therefore, only the offset from the first two gain stages are trimmed. This does not create any problem because the dc gain of these two stages is approximately 30000, any offset introduced by the output stage will be negligible when referred back to the input. It is important to note that the 1st and 2nd stage of the amplifier are connected closed-loop during the calibration process. This is to guarantea the voltage which appears at the second stage output will be relatively small and the trimming speed will not be severely limited by the slewing time of the amplifier.

The algorithm for the self-calibration technique is shown in Fig.(20). The trimming procedue is apparent by combining the information indicated Fig.(18), Fig.(19) and Fig.(20).

4.4. Control Circuits

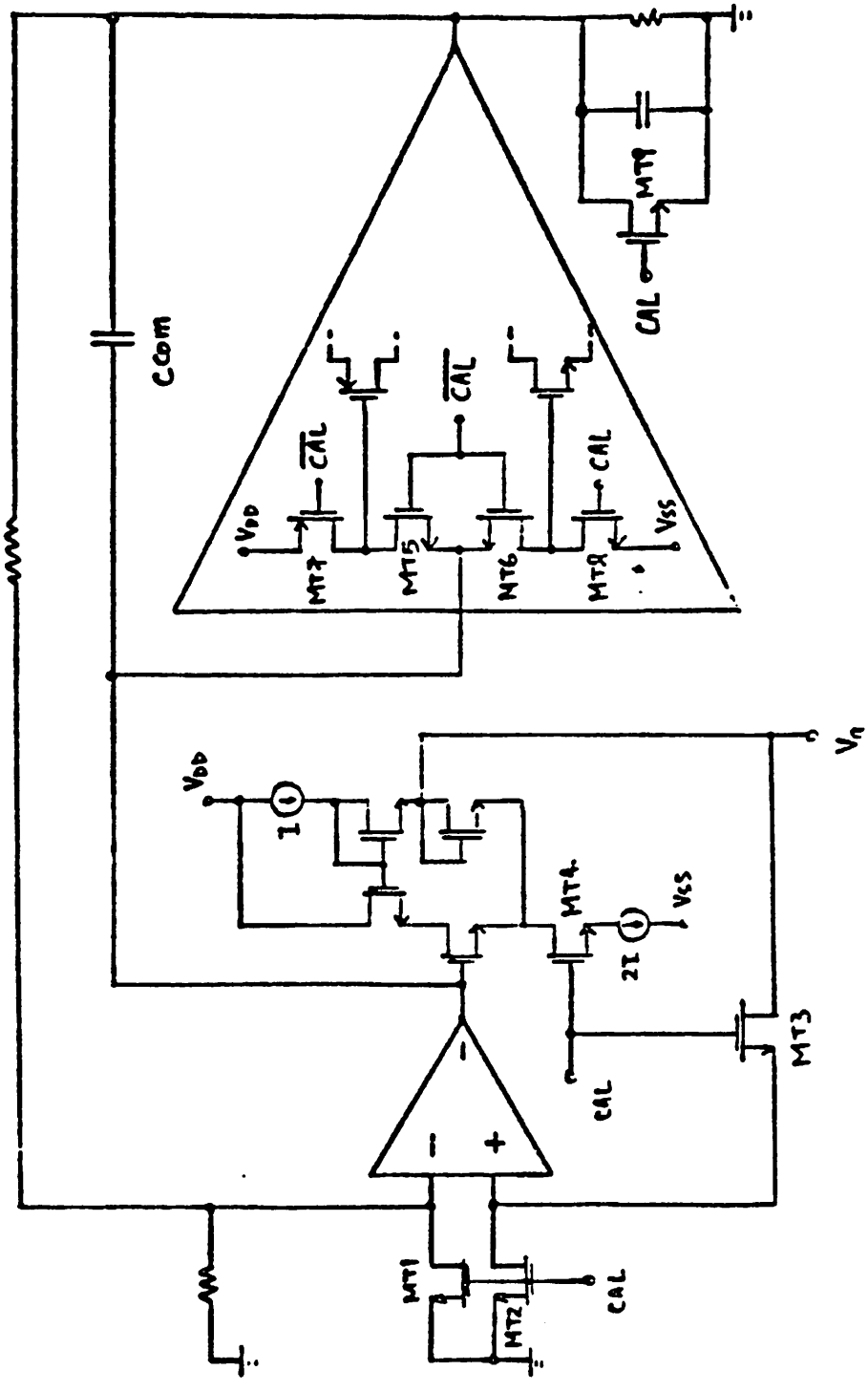


Fig.(19) Required switching pattern to break the external feedback loop.

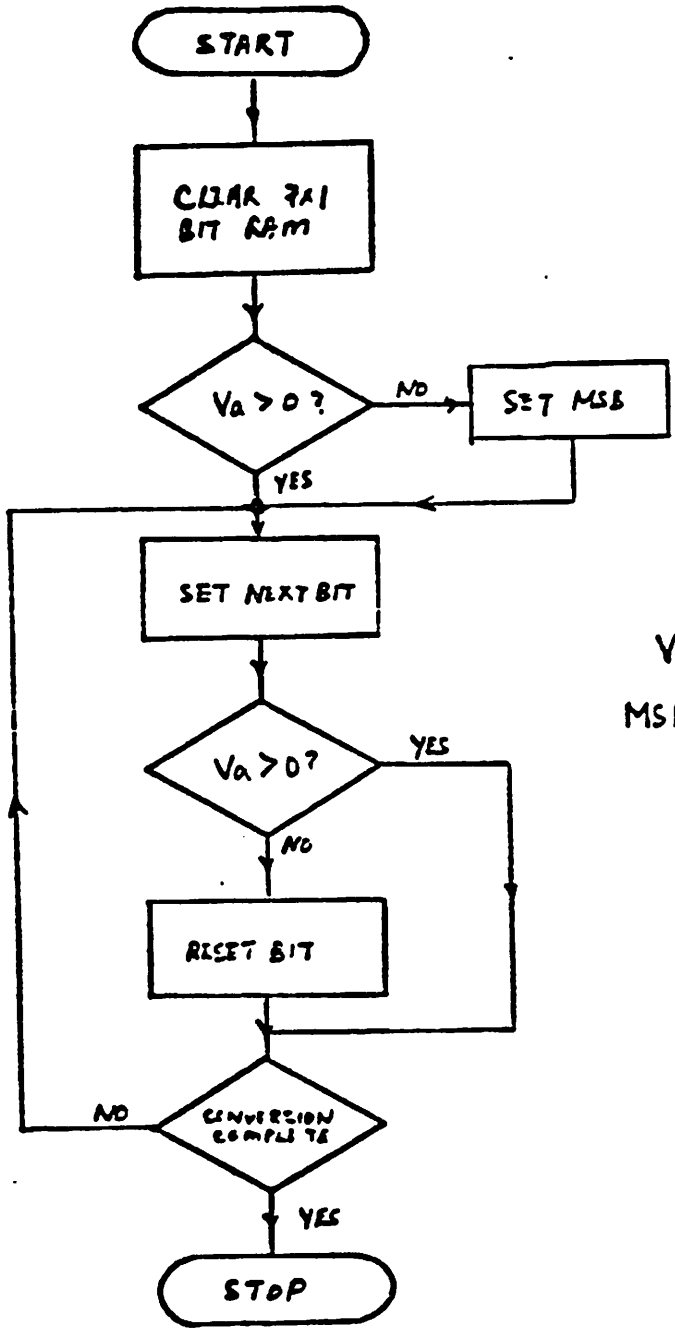


Fig.(20) Self-calibration algorithm.

A block diagram of the complete self-calibration scheme is shown in Fig.(21). The control circuitry consists of a clock-divider (clock rate divide-by-2), 2 two-phase non over-lapping clock generators, a 4-bit counter, a sense amplifier, a latch, a tree decoder, some static storage cells and control switches.

4.4.1. Detail Operation

As mentioned earlier, the SU signal will clear the RAM and will set the counter to the 1111 state. From the external clock, non-overlapping clocks Φa and Φb are generated. The clock-divider will generate a clock signal which has a period twice as long as that of the external clock. Based on this signal, non-overlapping clocks Φ1 and Φ2 are generated. Φ1, Φ2, Φa and Φb provide all the clocking signals required to sequence the entire control circuitry.

As mentioned before, the SU signal will clear the RAM and set the counter to 1111. The 4-bit down-counter is clocked by Φa. Based on the outputs of the counter (Q_A - Q_D) a control signal CAL is generated.

$$CAL = \overline{\bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{Q}_D} \tag{29}$$

Hence, during the period when the counter is counting down from 1111 to 0000, CAL = 1. CAL and $\overline{CAL}$ are used to control the swithces that are required to open the external feedback loop to allow self-calibration. Although there are only 7 storage RAM cells (7-bit trimming) and only 7 addresses are needed, a 4-bit counter is used to generate the address. The purposes of choosing a 4-bit counter are:

(1) The state 0000 is reserved as a flag for " end of calibration ".

(2) Although there are only 7 RAM cells needed to be set, 8-cycles are needed.

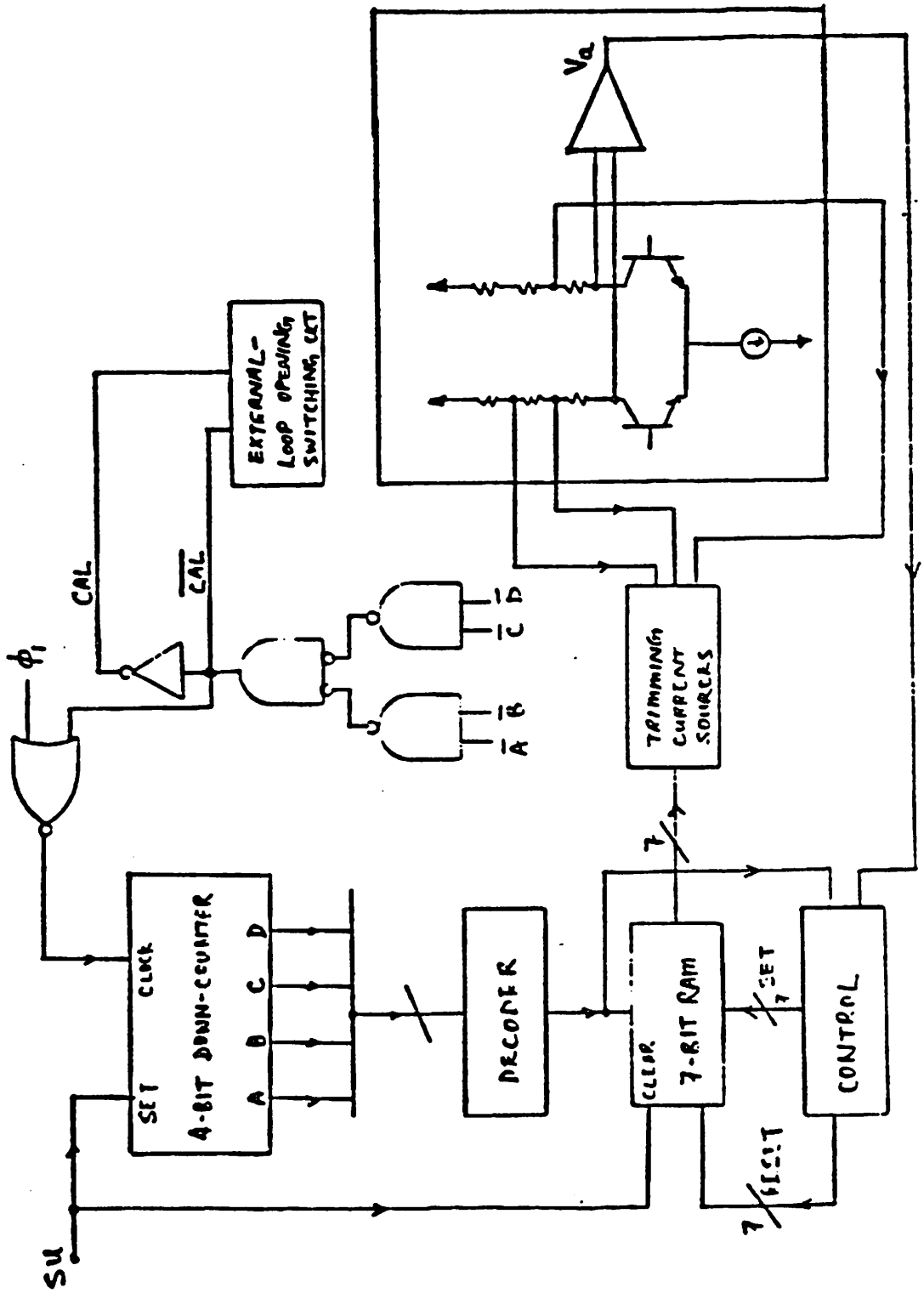


Fig.(21) Block diagram of the complete self-calibration scheme.

(3) The rest of the cycles (from 1111 to 1001) are needed to allow sufficient time for the amplifier to settle when it is first powered up.

Fig.(22) shows the timing diagram of the clocks and the counter outputs. Detailed circuit schematics for the trailing edge triggered D-flip flop, 4-bit down counter, sense amplifier, the latch, the tree decoder, the control circuits to set and reset the RAM cells are shown in Fig.(23a - 23e).

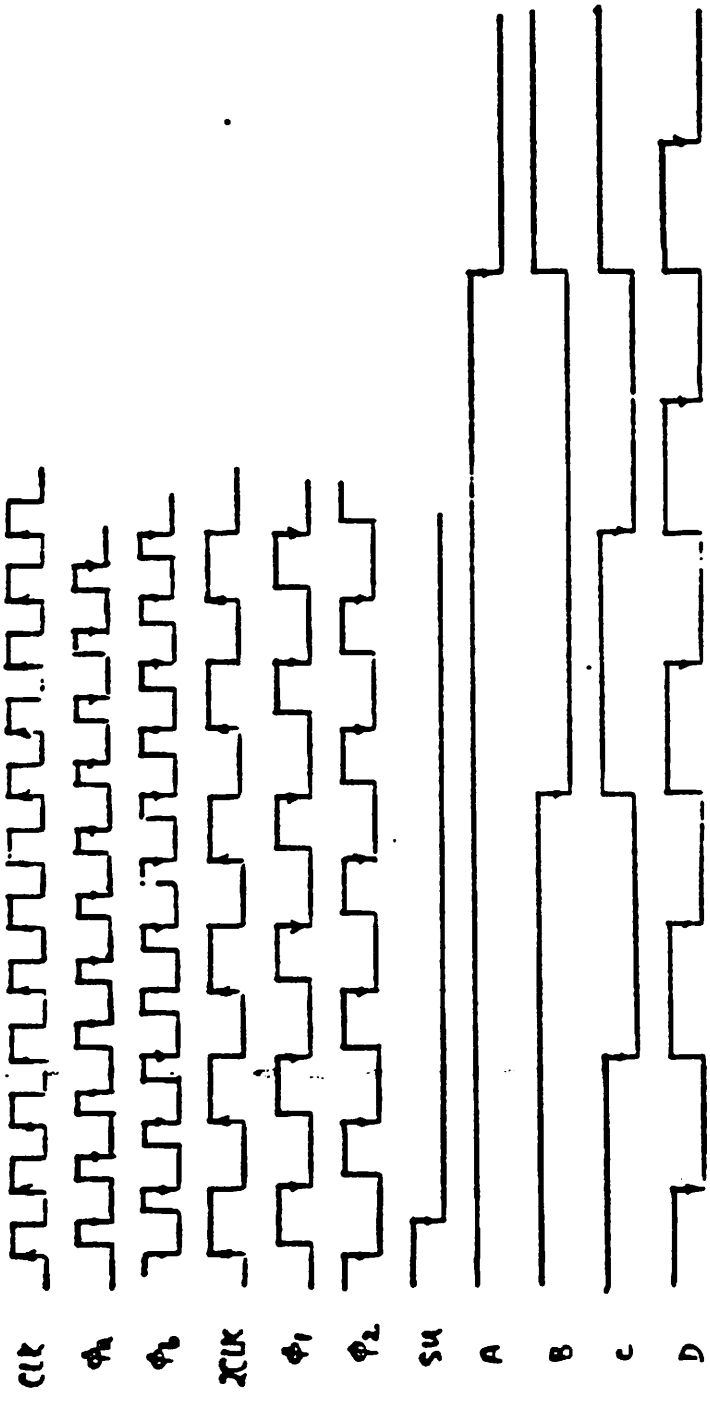


Fig.(22) Timing diagram of the clocks and the counter outputs.

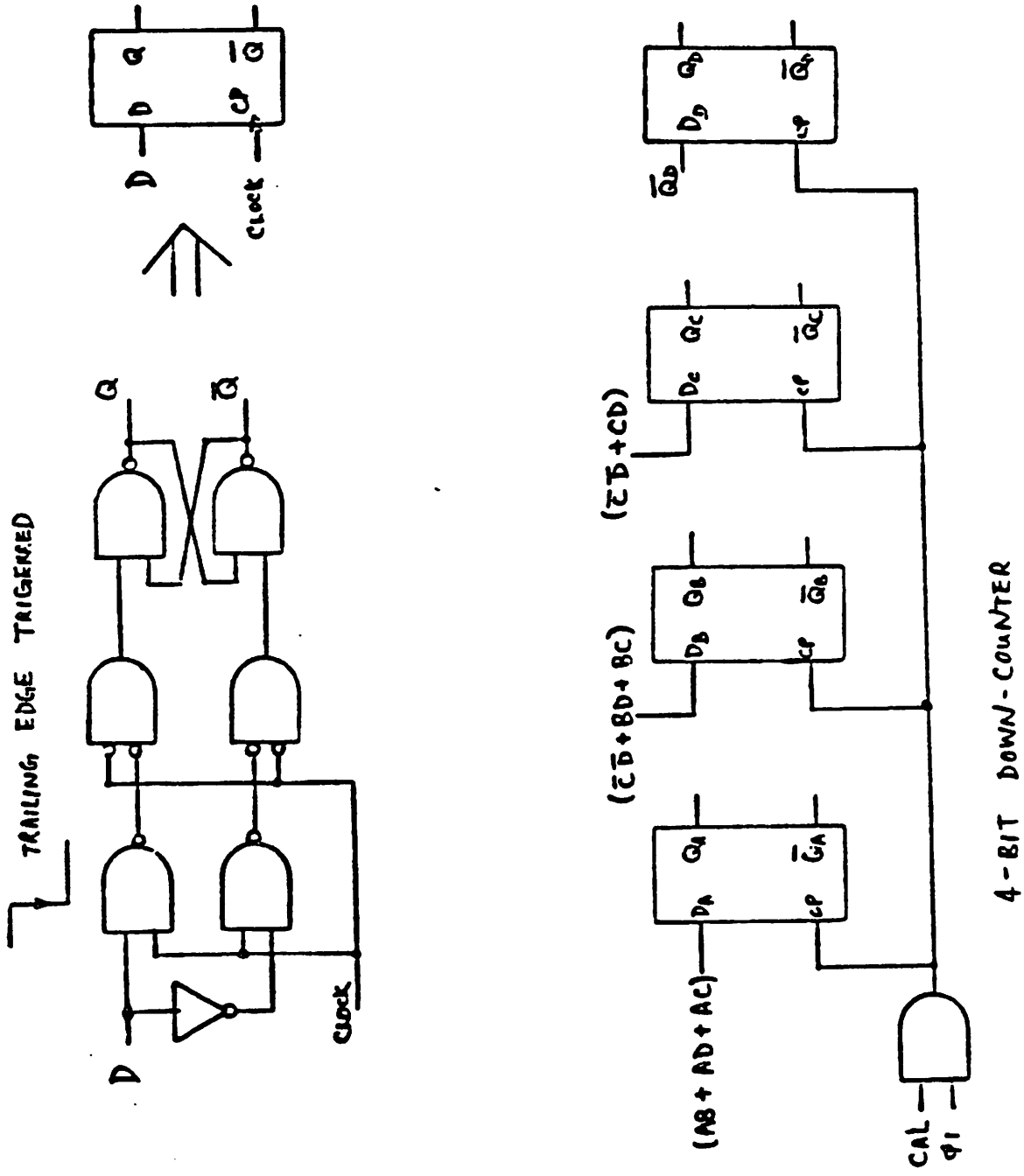


Fig.(23a) Implementation of the 4-Bit down-counter.

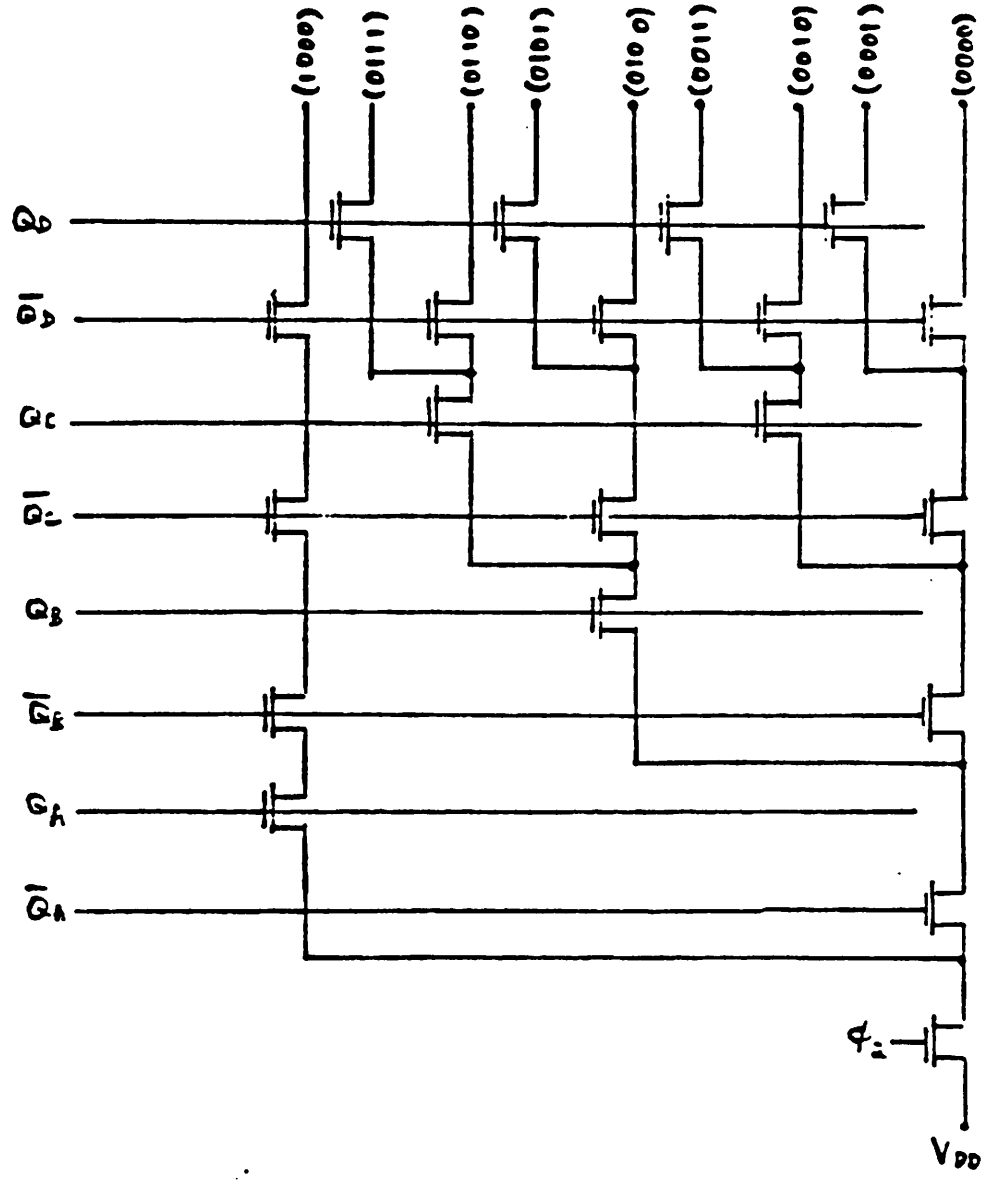


Fig.(23b) Decoder Implementation.

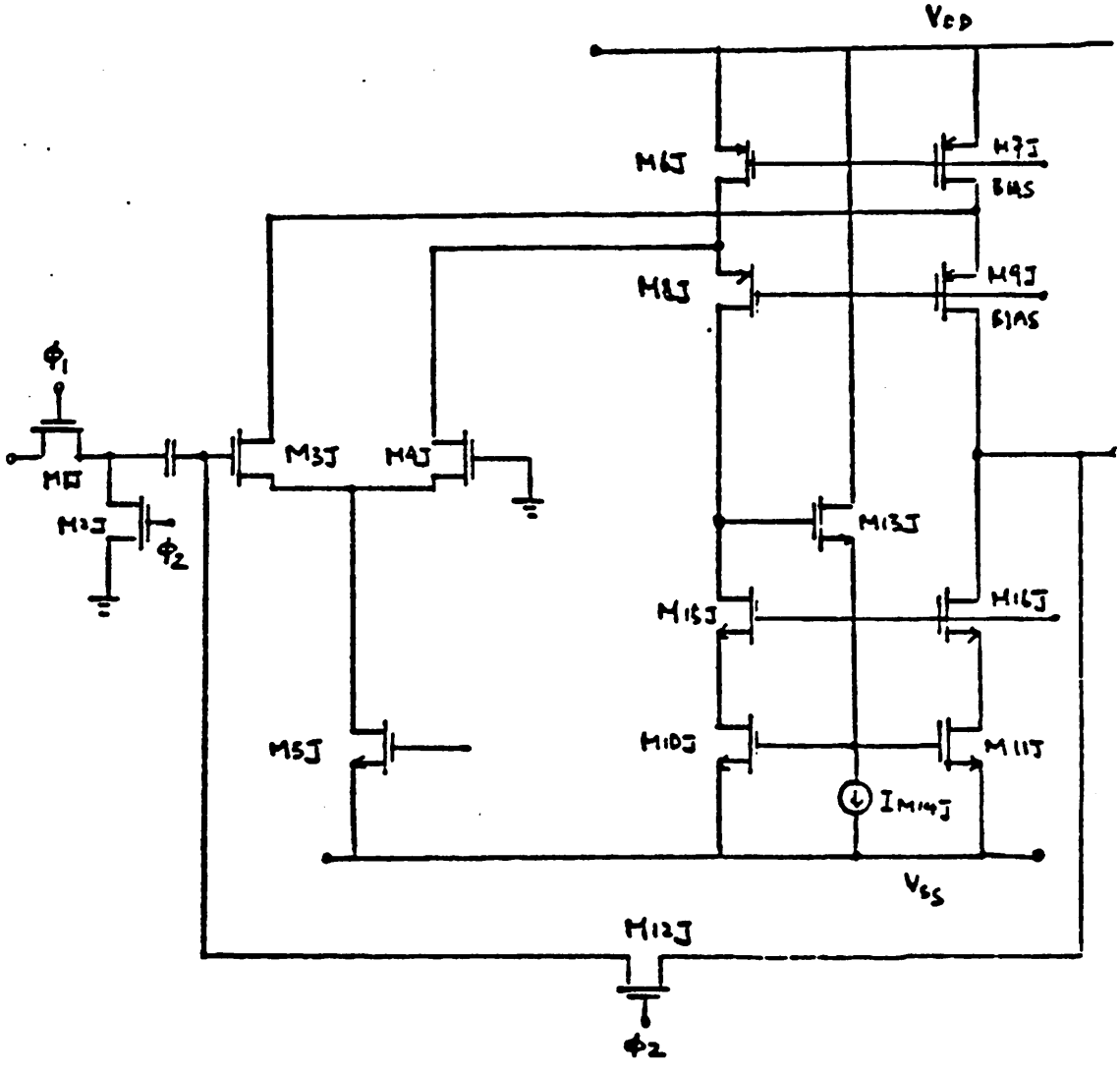


Fig.(23c) Sense amplifier for the self-calibration circuitry.

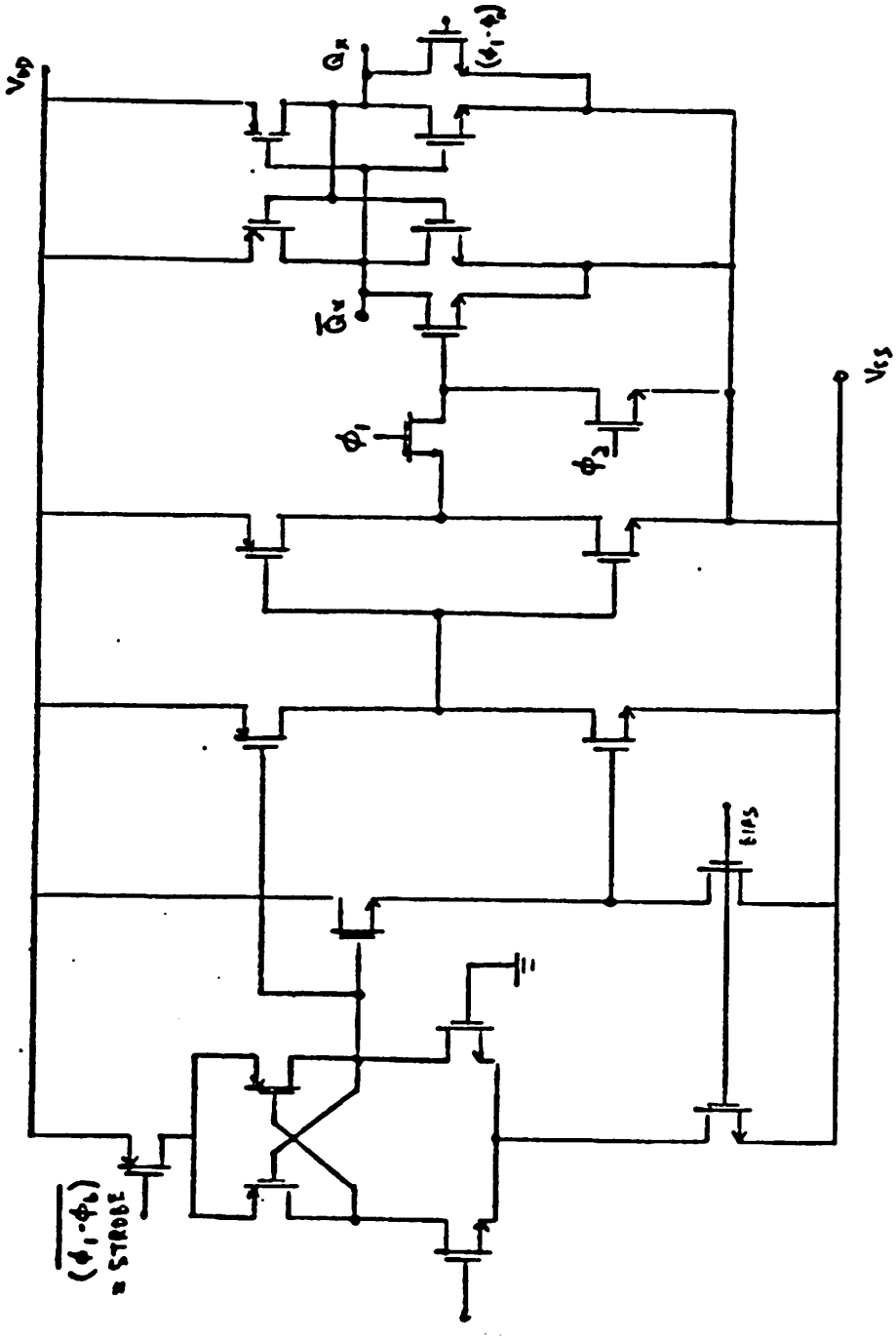


Fig.(23d) Latch for the self-calibration circuitry.

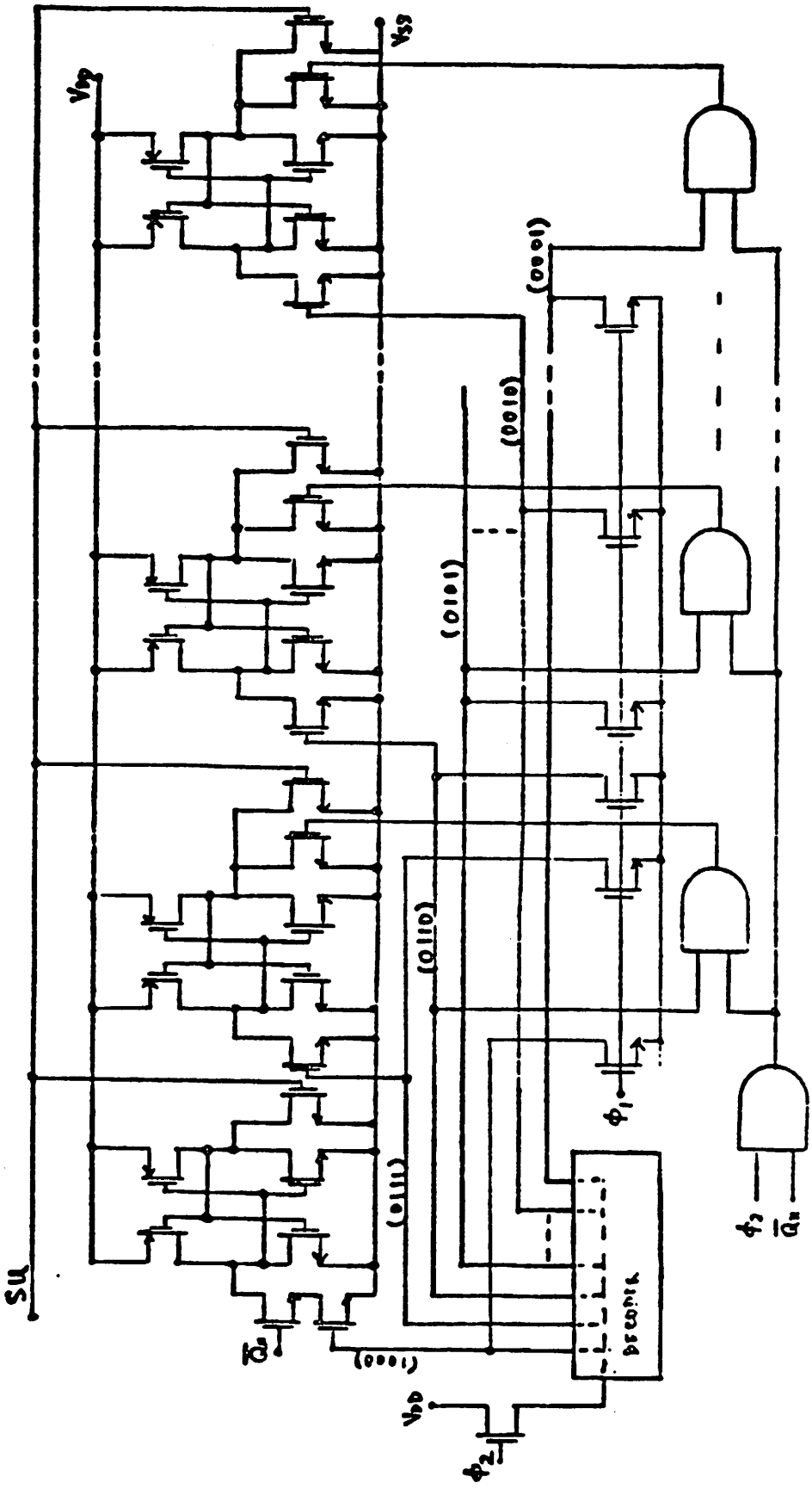


Fig.(23e) 7-bit RAM and Set-Reset control circuitry.

CHAPTER 5

OTHER CONSIDERATIONS

5.1. Layout Considerations

Layout has always played a critical role in the production of high-performance integrated circuits. For the circuit described in this report, the following should be noted :

(1) To achieve high gain, the effects of thermal feedback should be minimized. This implies the importance of symmetric layout as well as isothermal layout-considerations.

(2) To achieve low untrimmed offset, the input pair must be in cross-coupled structure. The matching of the 2 resistive loads is also very important, they should be arranged to have the same number of tapping points even though some of them will not be used on one of the resistors.

(3) Various substrate connections should be made available in order to minimize the effects of any substrate currents on the circuit performance including latch-up.

(4) The digital part of the circuit should be "separated" from the analog part of the circuit for the compactness of the analog circuit, for the easiness of trouble shooting and for the minimization of clock noise during the self-calibration process.

5.2. Miscellaneous

(1) Substrate current should be minimized [Isub $< 500\ \mu A$].

(2) The availability of 2 μ channel length design rule is essential to allow short base-width for the lateral bipolar devices.

(3) Minimum contact size should be used for the emitter of the lateral bipolar transistors in order to allow the maximization of β_c.

CHAPTER 6

CONCLUSIONS

In summary, the lateral bipolar transistors available in standard CMOS process can be of great usefulness in certain analog applications. In particular, they can be used to provide the "low-offset" and "low-1/f noise" features which are not readily realizable by using standard MOS transistors. However, the main limitations of these lateral bipolar devices are expected to be their poor frequency response (i.e. low f_T) and the presence of the large substrate current due to the parasitic vertical bipolar transistors.

An input offset self calibration technique is introduced. This technique makes possible the fabrication of low input offset (less than 100μV) operational amplifiers in standard CMOS technologies. The limitation of the technique is that the lower trimming limit is set by the noise performance of the amplifier.

A precision operational amplifier in standard CMOS technology is designed by incorporating the advantages that are provided by the lateral bipolar devices and the input offset self- calibration scheme. This amplifier out-performs any existing MOS amplifier (that have similar gain characteristics) in terms of its input offset and noise performance.

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