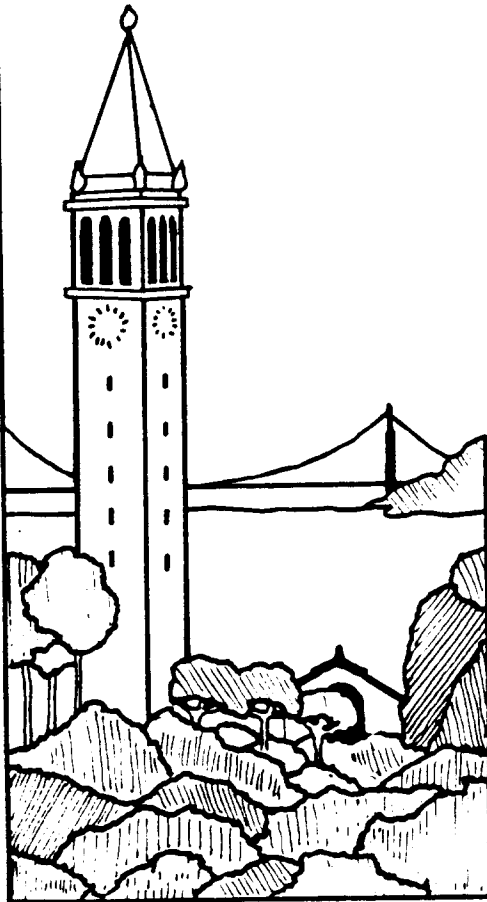


Signal Delay in RC Trees with Charge Sharing or Leakage

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ABSTRACT

A single value for delay, based upon the delay of Elmore, is derived for two types of RC tree networks. In one type of network, there is no driving source: this undriven situation causes static charge sharing among nodes. An expression for delay is obtained by straightforward analysis of this network.

In our second case, an RC tree which is driven by at least one source has leaky capacitors. We show how to calculate delays for such trees by a linear time algorithm.

Simple MOS circuits undergoing charge sharing and with leakage paths to ground are analyzed using the methods presented in this paper. The results are compared with those of SPICE.

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1. Introduction

Modeling digital MOS circuits by RC networks for the purpose of estimating delay has become a well accepted practice [9, 11, 12, 5, 8]. One approach pioneered by Rubinstein, Penfield and Horowitz (R-P-H) is to model a circuit as an RC network driven by a single source [9, 11, 12, 5]. Crystal [8] takes a more restrictive approach, calculating the delay at a node by considering only a single resistive path to the source.

The result of a delay calculation may be a single value [8], a “best fit” exponential [5], or a pair of bounding waveforms [9, 11, 12]. We choose the intermediate course of supplying a “best fit” exponential.

The RC model of R-P-H [9] depends on two basic approximations. Transistor inputs are approximated by step waveforms, and conducting transistors are approximated by linear resistors. A simulation program like SPICE [6], on the other hand, makes no such approximations and is hence computationally much slower, though more accurate. The R-P-H approach is conceptually simple and computationally efficient, and has been incorporated into several timing-analysis programs [4, 10]. In this paper, we employ this basic R-P-H model.

Most analyses of RC networks introduce several additional assumptions. One is that all RC networks need to be driven by exactly one source. However, many MOS circuits used in practice have no driving source: this undriven situation may cause static charge sharing among nodes [1], a situation we have addressed in this paper. Secondly, there are instances where more than one source drives a network. For example, consider an nMOS inverter driving two loads with its input set to logic value ‘1’, as shown in Fig. 1. The load capacitors are driven by two sources, VDD and GND. To the best of our knowledge, ours is the only analysis to allow multiple sources. A third additional assumption of analyses of RC networks is that all capacitors are ideal, having no leakage path to ground. Under this assumption, a previously charged capacitor that is isolated from the rest of the circuit would retain its charge for an infinite duration of time. Yu and Wyatt [12] relax this assumption, allowing one leaky capacitor. Our analysis permits any number of leaky capacitors.

A fourth additional assumption that many models make is that the RC network is a tree, meaning that no resistor meshes are allowed. Lin and Mead (L-M) [5] have provided a “best fit” exponential for an RC mesh. Wyatt [11] extends this, providing a pair of bounding waveforms for an RC mesh. In this paper, we analyze the restricted case of an RC tree.

A most general RC model would allow floating capacitors in the network. No floating capacitors are permitted in this paper. There exists no known analysis for such a model, and it remains an important open problem for future research.

In this paper, an expression for delay in an RC tree network undergoing charge sharing is provided. The analysis of this network is based on two simple principles of circuit theory, namely, charge and energy conservation.

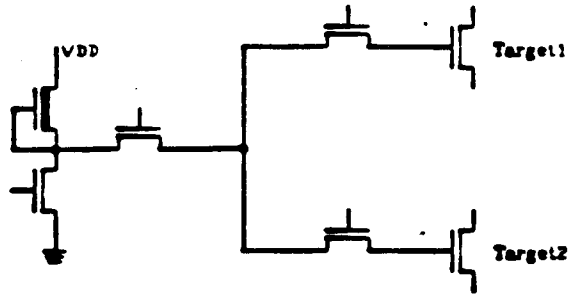


Figure 1. An nMOS inverter.

The analysis of RC tree networks driven by more than one source is not as straightforward as the analysis of charge sharing networks. Our analytic approach is to use RC trees with leakage. An RC tree with leakage is defined as a loopless resistor network where there is a resistor and capacitor between every node and GND, driven by any number of sources. Fortunately, as far as delay is concerned, only one network needs to be analyzed: an RC tree with leakage driven by one and only one source, namely VDD. It will be shown in later sections how this can be used to take care of all other cases.

Based upon the switch level simulation model proposed by Bryant [1], a timing model for MOS transistor circuits is presented in Section 2. The transient behavior of a transistor circuit is approximated by a linear RC network for estimating delays. The delay used in our model is based upon L-M's definition [5], modified to correctly treat the effects of charge sharing and leakage resistors (Section 3). The L-M definition of delay is the same as Elmore's delay [3] for an RC network with no initial charge [5].

In Section 3, our definition of delay is also shown to be the same as Elmore's for the case of no initial charge. An interpretation for delay is provided. On this basis, we estimate a waveform as an exponential with a single time constant. RC networks driven by GND and by multiple sources are simple extensions of the case where RC networks are driven by a single source, namely VDD (Section 3).

In Section 4, an expression for delay at a node in an RC tree undergoing charge sharing is derived. In Section 5, an expression for delay at any node in an RC tree with leakage is derived, in terms of the delay values at all other nodes in the network. This leads to a linear system of equations, with the delay values at all nodes as the unknowns. This system may be solved by standard techniques, for example matrix inversion.

Section 6 provides a more efficient method for delay calculation. A constructive definition for RC trees with leakage is provided. A set of parameters is defined for any RC network, including a primitive network, which is the basic building block of an RC tree with leakage. These parameters are updated at each stage of tree-construction, until the whole tree is constructed.

In Section 7, two different networks, one undergoing charge sharing, and another driven by a voltage source with a leakage path to ground are analyzed using the methods presented in this paper and the results are compared with those of SPICE. Section 8 concludes the paper.

The proofs of all theorems and corollaries in this paper can be found in the Appendix.

2. The Timing Model

The timing model for MOS transistor circuits is based on the switch model proposed by Bryant [1]. In this model, a circuit is represented by a set of transistors $\{t_1, \dots, t_m\}$ and a set of nodes $\{p_1, \dots, p_n\}$. With each node p_i are associated a resistance, a capacitance, a charge and a voltage source. Also associated with a node is a state, which is a function of its charge. With each

transistor are associated a set of resistances. The value of a transistor's resistance depends on the the state of the node controlling its gate and on the states of its other two nodes, the source and the drain. Although the capacitance and resistance at a node and the resistance of a transistor are voltage dependent, they are assumed as constants here.

The evolution of an MOS circuit is approximated by a sequence of RC networks. Various node capacitors are charged and discharged through the network. This charging-discharging process may change the state of a node which in turn changes the topology of the RC network. The process continues until the topology of the network changes no longer.

Definition 1. An RC network is a loopless connected graph on n nodes. With each edge i is associated a nonnegative resistance r_i . With each node k are associated a positive resistance R_k , a positive capacitance C_k , a nonnegative charge Q_k and a voltage source $v_k \in \{VDD, GND, \phi\}$, where ϕ indicates no connection.

The electrical interpretation of this definition is that the nodes of the graph correspond to the connection points. Circuit elements associated with a node in the definition are elements that exist between the node and GND in the network. Note that this definition does not allow for floating capacitors (capacitors associated with the edges of the graph) in the network.

When the edges and nodes are all labeled with numbers, these parameters can be grouped together as vectors. An RC network is then denoted by $N(n, r, R, C, Q, V)$, where n is the number of nodes, r is a vector of edge resistances, R is a vector of leakage resistances, C is a vector of node capacitances, Q is a vector of capacitance charges, and V is a vector of node voltage sources. In Fig. 2, below, the nodes are labeled by circled indices. Edges are the series resistors r_i . A single leakage resistor, R_3 , is shown. All other leakage resistors are (by default) infinite.

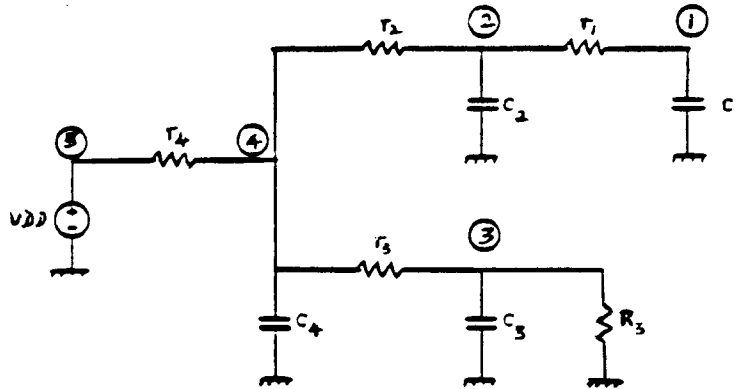


Figure 2. A standard RC network.

With the approximations introduced above, the problem of estimating the delay of an MOS circuit reduces to that of estimating the delay of an RC network. Certain special cases of RC networks, which occur in this paper, are denoted below:

- 1) $N(n, r, R, C, Q, VDD_n)$: An RC network with n nodes, driven by a single source, namely VDD, which is connected to node n . This network will be referred to as the standard network, or N_n , in the rest of the paper.
- 2) $N(n, r, R, C, Q, GND_n)$: The same network as in 1) with node n connected to GND.
- 3) $N(n, r, \infty, C, Q, \phi)$: An RC network on n nodes with only ideal capacitances and no sources. This network will be referred to as the charge sharing network, or $N_n(\phi)$ in the rest of the paper.

Example. Consider the standard RC network N_5 shown in Fig. 2. There is a single driving source, VDD, which is a step function of magnitude VDD, and connected to node 5. Since our RC networks are loopless, we may assign the label $\min(a, b)$ to the edge (a, b) .

Define a path nk to be the (unique) list of edges joining node n to node k . Let $R_{k,i}$ denote the sum of the resistances of the edges common to the unique paths nk and ni [9]. For example, in Fig. 2, $R_{2,2} = r_4 + r_2$ and $R_{2,3} = r_4$. Note that a doubly subscripted $R_{k,i}$ is distinct from a leakage resistance R_k .

In general, we might need to evaluate the delay at a node in any RC network. Thus, it is sufficient to derive an expression for delay in N_n and $N_n(\phi)$ only. As shown in the next section, delay computation in any network with one or more sources is a simple extension of the method for the standard network.

3. Definition of Delay

Prior to analysis, it is necessary to have a consistent and unambiguous definition of delay. Although there are a number of such definitions in practical use, most of these are awkward for theoretical investigation. Elmore's delay [3], on the other hand, is very efficient in this respect, and is defined as

$$\tau^0 = \int_0^{\infty} t v'(t) dt. \quad (1)$$

where $v'(t)$ is the derivative of the transient voltage $v(t)$ of some node of a network whose delay is τ^0 . This definition of delay is based upon the observation that, if $v(t)$ is monotonic in time, τ^0 is the centroid of $v'(t)$ and is very close to what is commonly conceived as delay.

In an RC network with no input or only step inputs, the voltage at node i can be obtained from

$$V_i(s) = \frac{v_i(\infty) (1 + a_{1,i}s + \dots + a_{m,i}s^m)}{s (1 + b_{1,i}s + \dots + b_{n,i}s^n)}. \quad (2)$$

In a network with no floating capacitors and no initial stored charge [3],

$$\tau^0 = b_{1,i} - a_{1,i} \quad (3)$$

Before we go into a discussion on delay, we need a well known result in network theory [2]:

In any passive RC network, $V_i(s)$, the Laplace transform of the voltage $v_i(t)$ at node i can be written as

$$V_i(s) = \frac{1}{s} \left[v_i(0) + \frac{c_{1,i}}{1 + t_{1,i}s} + \dots + \frac{c_{n,i}}{1 + t_{n,i}s} \right]. \quad (4)$$

when the input waveform is a step function.

We now state a theorem that is a direct consequence of the definition of Elmore's delay.

Theorem 1. In an RC network, Elmore's delay at node i can be expressed as

$$\tau_i^0 = \frac{c_{1,i} t_{1,i} + \dots + c_{n,i} t_{n,i}}{v_i(\infty)} \quad (5)$$

where the $c_{k,i}$ and $t_{k,i}$ are defined by (4). Theorem 1 tells us that τ_i^0 is the weighted average of the individual time constants and hence gives us a "best fit" exponential waveform.

$$v_i(t) \approx v_i(\infty)(1 - \exp(-t/\tau_i^0)) \quad (6)$$

Lin and Mead (L-M) [5] have given a modified definition of delay, which is the same as Elmore's delay for zero initial charge. Here, it is assumed that all networks are driven by $VDD=1$, so that $v(\infty)$ is always 1. The L-M definition of delay is valid only for type 1 networks with no leakage paths to GND.

$$T_D^{L-M} = \int_0^{\infty} [1 - v(t)] dt. \quad (7)$$

This expression is just the area above the response $v(t)$, but below 1.

A "best fit" time constant, τ^{L-M} is easily obtained from T_D^{L-M} as follows.

$$\tau^{L-M} = \frac{T_D^{L-M}}{1 - v(0)} \quad (8)$$

The L-M definition is not suitable for RC networks as dealt with in this paper, because $v(\infty)$ is not always 1. Accordingly, we redefine delay as

$$\tau = \frac{\int_0^{\infty} [v(\infty) - v(t)] dt}{v(\infty) - v(0)}. \quad (9)$$

From our definition of delay, and from (2), we have

$$\tau_i = \frac{\lim_{s \rightarrow 0} s \left[\frac{v_i(\infty)}{s} - V_i(s) \right]}{v_i(\infty) - v_i(0)} = (b_{1,i} - a_{1,i}) \left[\frac{v_i(\infty)}{v_i(\infty) - v_i(0)} \right] \quad (10)$$

Therefore, our τ is equal to Elmore's delay τ^0 for RC networks with no initial charge.

Corollary 1. In an RC network, delay at node i can be expressed as

$$\tau_i = \frac{c_{1,i} t_{1,i} + \dots + c_{n,i} t_{n,i}}{v_i(\infty) - v_i(0)} \quad (11)$$

An immediate consequence of Corollary 1 is that we now have a "best fit" exponential waveform with time constant τ_i .

$$v_i(t) \approx v_i(0) + (v_i(\infty) - v_i(0))(1 - \exp(-t/\tau_i)) \quad (12)$$

Definition 2. The parameter D_i is defined as the product of $(v_i(\infty) - v_i(0))$ and the delay τ_i .

$$D_i = (v_i(\infty) - v_i(0)) \cdot \tau_i \quad (13)$$

D_i in a network $N(n, r, R, C, Q, V)$ will also be referred to as $D_i(n, r, R, C, Q, V)$ when the context is not obvious. As the next few theorems show, most of our results on delay are expressed through the parameter D_i .

We need another important result from network theory, the **Superposition Theorem** [2], which can be stated as below for the purpose of this paper:

Theorem 2. $D_i(n, r, R, C, Q, V)$ is obtained as the sum of the D_i in each network obtained from $N(n, r, R, C, Q, V)$ by setting all but one source to GND.

$$\begin{aligned} D_i(n, r, R, C, Q, V) = & D_i(n, r, R, C, Q, [v_{1,\text{GND}}, \dots, \text{GND}]) \\ & + D_i(n, r, R, C, Q, [\text{GND}, v_2, \dots, \text{GND}]) \\ & + \dots \\ & + D_i(n, r, R, C, Q, [\text{GND}, \text{GND}, \dots, v_n]). \end{aligned} \quad (14)$$

Theorem 3. $D_i(n, r, R, C, Q, \text{GND}_n)$ is obtained as the difference between the D_i in the networks N_n (the same network, but driven by VDD at node n), and $N_n(0)$ (the standard network with no initial charge).

$$\begin{aligned} D_i(n, r, R, C, Q, \text{GND}_n) = & D_i(n, r, R, C, Q, \text{VDD}_n) \\ & - D_i(n, r, R, C, 0, \text{VDD}_n) \end{aligned} \quad (15)$$

where the network $N(n, r, R, C, 0, \text{VDD}_n)$ represents the standard network N_n with the capacitances having no initial charge.

Corollary 2. (The discharging theorem.) Let Q represent the final charge attained by $N(n, r, R, C, 0, \text{VDD}_n)$. The delay at node i in network $N(n, r, R, C, Q, \text{GND}_n)$, is the same as the delay at node i in the network $N(n, r, R, C, 0, \text{VDD}_n)$.

A consequence of theorems 2 & 3 is that we need an expression for delay only in the charge sharing and standard networks. In Section 4, we derive an expression for delay in the charge sharing network, $N_n(\phi)$, and in Sections 5 & 6, we provide methods to evaluate delay in the standard network, N_n . We also show that the cases of networks with no initial charge and with ideal capacitors are special cases of the standard network, and do not require special treatment.

4. An Expression for Delay in the Charge Sharing Network

Consider a charge sharing network with n nodes, $N_n(\phi)$. We need to derive an expression for delay at some node in the network. Renumber the nodes as follows: the node for which we need to solve is numbered n , and the other nodes are numbered by a depth first traversal of the tree. The voltage waveform at any node i in this network can be obtained from

$$V_i(s) = \frac{v_f (1 + a_{1,i}s + \dots + a_{n,i}s)}{s (1 + b_{1,i}s + \dots + b_{n,i}s)} \quad (16)$$

where $v_f = v_i(\infty)$ is the final voltage of the network, and is obtained as follows:

$$v_f = \frac{\sum_{i=1}^n Q_i}{\sum_{i=1}^n C_i} \quad (17)$$

Here, the Q_i stand for the charge in C_i at time $t=0$.

From (9), we have

$$\tau_i = \frac{\int_0^{\infty} [v_f - v_i(t)] dt}{v_f - v_i(0)} \quad (18)$$

The current into a node k at time t is

$$i_k = C_k \frac{dv_k(t)}{dt} \quad (19)$$

The voltage drop from node n to node i due to all node currents is

$$v_{n,i}(t) = \sum_{k=1}^{n-1} R_{k,i} C_k \frac{dv_k(t)}{dt} \quad (20)$$

From (20), we get

$$v_i(t) = v_n(t) - \sum_{k=1}^{n-1} R_{k,i} C_k \frac{dv_k(t)}{dt} \quad (21)$$

Subtracting both sides from v_f , we get

$$v_f - v_i(t) = v_f - v_n(t) + \sum_{k=1}^{n-1} R_{k,i} C_k \frac{dv_k(t)}{dt} \quad (22)$$

and by integrating both sides, we have

$$D_i = D_n + \sum_{k=1}^{n-1} R_{k,i} C_k (v_f - v_k(0)) \quad (23)$$

Since there are no leakage paths to ground, no charge is lost from the network. Therefore, at any time t , the total charge in the network must equal the final charge (at $t = \infty$).

$$C_n v_n(t) + \sum_{i=1}^{n-1} C_i v_i(t) = v_f C_n + \sum_{i=1}^{n-1} C_i v_f \quad (24)$$

By rearranging terms in (24), we get

$$C_n (v_f - v_n(t)) = - \sum_{i=1}^{n-1} C_i (v_f - v_i(t)) \quad (25)$$

and hence, by integrating

$$C_n D_n = - \sum_{i=1}^{n-1} C_i D_i \quad (26)$$

Substituting for D_i in (26) from (23)

$$C_n D_n = - \sum_{k=1}^{n-1} C_k D_k - \sum_{i=1}^{n-1} C_i \sum_{k=1}^{n-1} R_{k,i} C_k (v_f - v_k(0)) \quad (27)$$

Thus, the expression for D_n is

$$D_n = - \frac{\sum_{i=1}^{n-1} C_i \sum_{k=1}^{n-1} R_{k,i} C_k (v_f - v_k(0))}{\sum_{k=1}^n C_k} \quad (28)$$

and the expression for delay at node n is

$$\tau_n = - \frac{\sum_{i=1}^{n-1} C_i \sum_{k=1}^{n-1} R_{k,i} C_k (v_f - v_k(0))}{(v_f - v_n(0)) \sum_{k=1}^n C_k} \quad (29)$$

5. An Expression for Delay in the Standard Network

We now give an expression for delay in the standard network.

Consider the standard RC network as shown in Fig. 2. The current at time t into R_k and C_k together is

$$i_k = C_k \frac{dv_k(t)}{dt} + \frac{v_k(t)}{R_k}. \quad (30)$$

The voltage drop along the path from n to node i due to i_k is

$$v_{n,i}(t, i_k) = R_{k,i} \left[C_k \frac{dv_k(t)}{dt} + \frac{v_k(t)}{R_k} \right] \quad (31)$$

and, due to all i_k , $k=1,2,\dots,n-1$ is

$$v_{n,i}(t) = \text{VDD} - v_i(t) = \sum_{k=1}^{n-1} R_{k,i} \left[C_k \frac{dv_k(t)}{dt} + \frac{v_k(t)}{R_k} \right]. \quad (32)$$

Eqn. (32) is similar to (9) of [9] except for the additional term due to the leakage currents.

At steady state, the circuit is purely resistive. Therefore,

$$\text{VDD} - v_i(\infty) = \sum_{k=1}^{n-1} \frac{R_{k,i}}{R_k} v_k(\infty). \quad (33)$$

From (32) and (33), we have

$$v_i(\infty) - v_i(t) = \sum_{k=1}^{n-1} R_{k,i} \left(C_k \frac{dv_k(t)}{dt} + \frac{v_k(t)}{R_k} \right) - \sum_{k=1}^{n-1} \frac{R_{k,i}}{R_k} v_k(\infty). \quad (34)$$

Using (9) and (34), we get an expression for τ_i as given by (35).

$$D_i = \int_0^{\infty} \left[\sum_{k=1}^{n-1} R_{k,i} \left(C_k \frac{dv_k(t)}{dt} + \frac{v_k(t)}{R_k} \right) - \sum_{k=1}^{n-1} \frac{R_{k,i}}{R_k} v_k(\infty) \right] dt. \quad (35)$$

We now have the following theorem.

Theorem 4. For $i = 1, 2, \dots, n-1$, the D_i satisfy the following system of linear simultaneous equations:

$$\left(1 + \frac{R_{i,i}}{R_i} \right) D_i + \sum_{k \neq i} \frac{R_{k,i}}{R_k} D_k = \sum_{k=1}^{n-1} R_{k,i} C_k (v_k(\infty) - v_k(0)). \quad (36)$$

Eqn. (36) can be put in matrix form as follows:

$$\begin{bmatrix} \left(1 + \frac{R_{1,1}}{R_1} \right) & \frac{R_{1,2}}{R_2} & \dots & \frac{R_{1,n}}{R_n} \\ \frac{R_{2,1}}{R_1} & \left(1 + \frac{R_{2,2}}{R_2} \right) & \dots & \frac{R_{2,n}}{R_n} \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \frac{R_{n,1}}{R_1} & \frac{R_{n,2}}{R_2} & \dots & \left(1 + \frac{R_{n,n}}{R_n} \right) \end{bmatrix} \begin{bmatrix} D_1 \\ D_2 \\ \cdot \\ \cdot \\ D_n \end{bmatrix} = \begin{bmatrix} \sum_{k=1}^n R_{k,1} C_k (v_k(\infty) - v_k(0)) \\ \sum_{k=1}^n R_{k,2} C_k (v_k(\infty) - v_k(0)) \\ \cdot \\ \cdot \\ \sum_{k=1}^n R_{k,n} C_k (v_k(\infty) - v_k(0)) \end{bmatrix}$$

$$\mathbf{R} \cdot \mathbf{D} = \mathbf{T}$$

$$\mathbf{D} = \mathbf{R}^{-1} \cdot \mathbf{T} \quad (37)$$

Solving this linear system of equations would in general involve $O(n^3)$ arithmetic operations, but will provide the delay values for all the nodes in the network. However, most of the time, we need to solve for only a few nodes. In the next section, we provide an $O(n)$ algorithm for delay computation at a node in a standard RC network.

6. Hierarchical Approach for Delay Computation

Prior to any further discussion, a more constructive definition of standard RC networks than the one provided in Sections 1 & 2 is given. A standard RC network is recursively defined to be one of the following:

- a) A resistor in series with a nonideal capacitor. The free end of the resistor is the input, labeled 2, and its other end is the output, labeled 1. The other end of the capacitor is grounded. This is shown in Fig. 3(a). This network will also be referred to as the primitive element or N_2 in the rest of the paper.
- b) A series connection of the primitive element and an RC network with n nodes, N_n , to give N_{n+1} . The input of N_{n+1} is the input of N_2 , with the input of N_n connected to the output of N_2 . The nodes in N_{n+1} are renumbered as follows: The node numbers in N_n remain unchanged. Node 2 of N_2 is relabeled $n+1$. This is shown in Fig. 3(b).
- c) A parallel composition of an n -node network N_n with an m -node network N_m , forming a network N_{n+m-1} . The input of N_{n+m-1} is the input of N_n , as shown in Fig. 3(c). The nodes in N_{n+m-1} are renumbered as follows: The node numbers in one of them, say N_n , remain the same except for the input node, while the node numbers in N_m get incremented by $n-1$. The input node of N_{n+m-1} gets the label $n+m-1$.

In all three cases, the input node is connected to VDD.

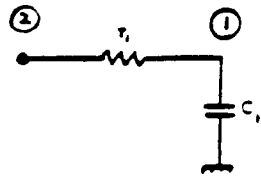


Figure 3(a). The primitive network N_2 .

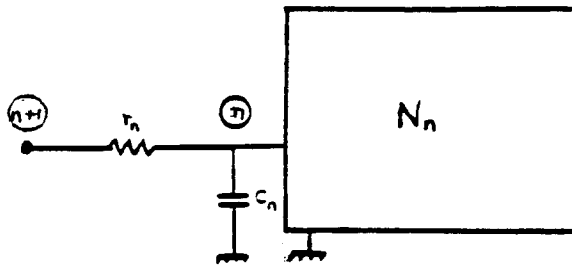


Figure 3(b). Series composition.

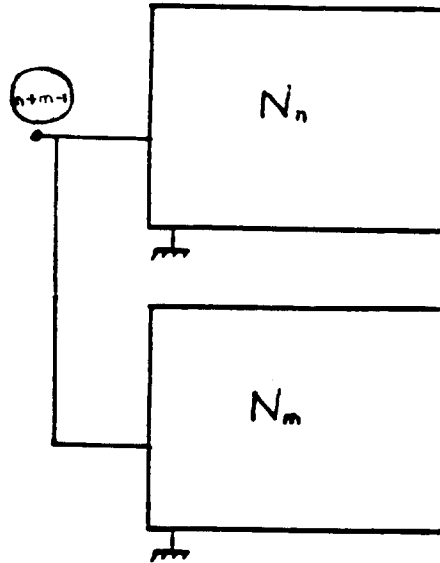


Figure 3(c). Parallel composition.

Having defined standard RC networks as dealt with in this paper, we define certain parameters associated with such a network. All parameters defined below are for N_n , a standard RC network with n nodes.

Definition 3. $\rho^{(n)}$ (*dimension : resistance*) is the effective resistance between the input node and GND.

Definition 4. $v_k^{(n)}(\infty)$ (*dim : voltage*) is the final voltage reached at node k in N_n .

Definition 5. $\tau_k^{(n)}$ (*dim : time*) is the delay at node k in N_n .

Definition 6. $\tau O_k^{(n)}$ (*dim : time*) is the delay at node k in $N(n, r, R, C, 0, \text{VDD}_n)$.

Definition 7. $D_k^{(n)}$ (*dim : time · voltage*) is defined as $v_k^{(n)}(\infty) \cdot \tau_k^{(n)}$.

Definition 8. $DO_k^{(n)}$ (*dim : time · voltage*) is defined as $v_k^{(n)}(\infty) \cdot \tau O_k^{(n)}$.

Definition 9. $(R_k^r)^{(n)}$ (*dimensionless*) is defined as the sum of all elements in row k of matrix \mathbf{R}^{-1} , as defined in eqn. (37).

Definition 10. $\bar{C}^{(n)}$ (*dim : charge*) is defined as

$$\bar{C}^{(n)} = \sum_{k=1}^n C_k v_k^{(n)}(\infty) \quad (38)$$

Definition 11. $\Delta^{(n)}$ (*dim : charge*) is defined as

$$\Delta^{(n)} = \sum_{k=1}^n \frac{D_k^{(n)}}{R_k} \quad (39a)$$

Definition 12. $\Delta_0^{(n)}$ (*dim : charge*) is defined as

$$\Delta_0^{(n)} = \sum_{k=1}^n \frac{DO_k^{(n)}}{R_k} \quad (39b)$$

Definition 13. $\sigma^{(n)}$ (*dim : conductance*) is defined as

$$\sigma^{(n)} = \sum_{k=1}^n \frac{(R_k^r)^{(n)}}{R_k} \quad (40)$$

Definition 14. $Q^{(n)}$ (*dim : charge*) is the total stored charge in N_n , at time $t = 0$:

$$Q^{(n)} = \sum_{k=1}^n Q_k \quad (41)$$

We are now in a position to state a theorem, based on which we present an $O(n)$ algorithm for delay calculation at a node.

Theorem 5(a). For the primitive element N_2 (see Fig. 3(a)), the various parameters are given by

$$\rho^{(2)} = r_1 + R_1$$

$$v_1^{(2)}(\infty) = \text{VDD} \cdot \left(\frac{R_1}{r_1 + R_1} \right)$$

$$\bar{C}^{(2)} = \text{VDD} \cdot \left(\frac{R_1}{r_1 + R_1} \right) \cdot C_1$$

$$Q^{(2)} = v_1(0) \cdot C_1$$

$$(R_1^r)^{(2)} = \frac{R_1}{r_1 + R_1}$$

$$\sigma^{(2)} = \frac{1}{r_1 + R_1}$$

$$D_1^{(2)} = C_1 \cdot \frac{r_1 R_1}{r_1 + R_1} \left(\text{VDD} \cdot \left(\frac{R_1}{r_1 + R_1} \right) - v_1(0) \right)$$

$$\begin{aligned}
 D\theta_1^{(2)} &= \text{VDD} \cdot C_1 r_1 \left(\frac{R_1}{r_1 + R_1} \right)^2 \\
 \Delta_0^{(2)} &= \text{VDD} \cdot C_1 \frac{r_1 R_1}{(r_1 + R_1)^2} \\
 \Delta^{(2)} &= \frac{C_1 r_1}{r_1 + R_1} \left(\text{VDD} \cdot \frac{R_1}{r_1 + R_1} - v_1(0) \right) \tag{42}
 \end{aligned}$$

Theorem 5(b). Given the parameters for network N_n , the parameters for the network N_{n+1} (see Fig. 3(b)) are given by

$$\begin{aligned}
 \rho^{(n+1)} &= r_n + \frac{R_n \rho^{(n)}}{R_n + \rho^{(n)}} \\
 v_n^{(n+1)}(\infty) &= \text{VDD} \left[1 - \frac{r_n}{\rho^{(n+1)}} \right] \\
 v_i^{(n+1)}(\infty) &= \left[\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right] v_i^{(n)}(\infty) \\
 \bar{C}^{(n+1)} &= v_n^{(n+1)}(\infty) \left[C_n + \frac{\bar{C}^{(n)}}{\text{VDD}} \right] \\
 Q^{(n+1)} &= v_n(0) C_n + Q^{(n)} \\
 (R_n^r)^{(n+1)} &= \frac{1}{1 + \frac{r_n}{R_n} + r_n \sigma^{(n)}} \\
 (R_i^r)^{(n+1)} &= (R_i^r)^{(n)} \cdot (R_n^r)^{(n)} \\
 \sigma^{(n+1)} &= (R_n^r)^{(n+1)} \cdot \left[\sigma^{(n)} + \frac{1}{R_n} \right] \\
 D_n^{(n+1)} &= r_n (R_n^r)^{(n+1)} \cdot \left[\bar{C}^{(n+1)} - Q^{(n+1)} - \Delta^{(n)} - \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right) \Delta_0^{(n)} \right] \\
 D\theta_n^{(n+1)} &= r_n (R_n^r)^{(n+1)} \cdot \left[\bar{C}^{(n+1)} - \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right) \Delta_0^{(n)} \right] \\
 D\theta_i^{(n+1)} &= D\theta_n^{(n+1)} + \left[\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right] D\theta_i^{(n)} \\
 D_i^{(n+1)} &= D_i^{(n)} + D\theta_i^{(n+1)} - D\theta_i^{(n)} - r_n (R_i^r)^{(n+1)} \cdot (Q^{(n+1)} + \Delta^{(n)} - \Delta_0^{(n)}) \\
 \Delta_0^{(n+1)} &= \frac{\sigma^{(n+1)} \cdot D\theta_n^{(n+1)}}{(R_n^r)^{(n+1)}} + \left[\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right] \Delta_0^{(n)}
 \end{aligned}$$

$$\Delta^{(n+1)} = \Delta^{(n)} + \Delta_0^{(n+1)} - \Delta_0^{(n)} - r_n (R_n^r)^{(n+1)} \cdot \sigma^{(n)} \left[Q^{(n+1)} + \Delta^{(n)} - \Delta_0^{(n)} \right] \quad (43)$$

Theorem 5(c). Given the parameters for networks N_n and N_m , the parameters for the network N_{n+m} (see Fig. 3(c)) are given by

$$\rho^{(n+m-1)} = \frac{\rho^{(n)} \rho^{(m)}}{\rho^{(n)} + \rho^{(m)}}$$

$$v_i^{(n+m-1)}(\infty) = \begin{cases} v_i^{(n)}(\infty), & \text{if } i = 1, 2, \dots, n-1 \\ v_{i-n+1}^{(m)}(\infty), & \text{if } i = n, n+1, \dots, n+m-2 \end{cases}$$

$$\bar{C}^{(n+m-1)} = \bar{C}^{(n)} + \bar{C}^{(m)}$$

$$Q^{(n+m-1)} = Q^{(n)} + Q^{(m)}$$

$$(R_i^r)^{(n+m-1)} = \begin{cases} (R_i^r)^{(n)} & i = 1, 2, \dots, n-1 \\ (R_{i-n+1}^r)^{(m)} & i = n, n+1, \dots, n+m-2 \end{cases}$$

$$\sigma^{(n+m-1)} = \sigma^{(n)} + \sigma^{(m)}$$

$$D_i^{(n+m-1)} = \begin{cases} D_i^{(n)} & i = 1, 2, \dots, n-1 \\ D_{i-n+1}^{(m)} & i = n, n+1, \dots, n+m-2 \end{cases}$$

$$D\theta_i^{(n+m-1)} = \begin{cases} D\theta_i^{(n)} & i = 1, 2, \dots, n-1 \\ D\theta_{i-n+1}^{(m)} & i = n, n+1, \dots, n+m-2 \end{cases}$$

$$\Delta_0^{(n+m-1)} = \Delta_0^{(n)} + \Delta_0^{(m)}$$

$$\Delta^{(n+m-1)} = \Delta^{(n)} + \Delta^{(m)} \quad (44)$$

The algorithm for delay computation at a node in an RC network follows immediately from Theorems 5a-c. Starting from all the leaves, build the tree using steps a, b & c as given earlier in this section, until the entire tree has been built. At each stage of construction, update the relevant parameters as given by Theorem 5. τ_i , the delay at node i is then obtained as

$$\tau_i = \frac{D_i}{v_i(\infty) - v_i(0)} \quad (45)$$

It turns out that when all leakage resistances, R_k , are set to infinity, and VDD is set to 1, the following happen:

- 1) $\rho^{(n)}$ is infinite for all n .
- 2) $v_i^{(n)}(\infty) = 1$, for all i and n .
- 3) $\bar{C}^{(n)}$ is the sum of all capacitances in N_n .
- 4) $\sigma^{(n)}$, $\Delta^{(n)}$, $\Delta_0^{(n)}$ go to 0 for all n .
- 5) $(R_k^r)^{(n)} = 1$, for all n .

Based on these five observations, the theorems can be appropriately simplified.

In the case of no initial charge ($Q^{(n)} = 0$, for all n) the following happen:

- 1) $D_i^{(n)} = D\theta_i^{(n)}$, for all i and n .
- 2) $\Delta^{(n)} = \Delta\theta^{(n)}$, for all i and n .

In the next section, an application for RC trees with leakage is provided.

7. Some Examples

Two examples are presented in this section: one is a charge sharing network and the other is a standard network with a leakage path to ground. The results obtained using the methods presented in this paper are compared with those of SPICE. In the case of the standard network, we also compare our result with that obtained by the Lin-Mead model.

Example 1. A charge sharing network. Consider the nMOS dynamic-RAM cell shown in Fig. 4(a). The RC network derived from this is shown in Fig. 4(b).



Figure 4(a). An nMOS dynamic-RAM cell.

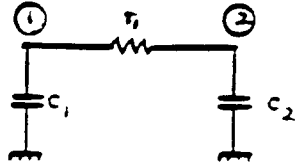


Figure 4(b). The RC network derived from Figure 4(a).

The network parameters are given below:

$$n = 2$$

$$r_1 = 5 \text{ K}\Omega$$

$$C_1 = 1.6 \times 10^{-2} \text{ pF}$$

$$C_2 = 1.2 \times 10^{-1} \text{ pF}$$

$$Q_1 = 8 \times 10^{-14} \text{ C}$$

$$Q_2 = 0 \text{ C}$$

v_f , the final voltage reached by the network is

$$v_f = \frac{8 \times 10^{-14}}{1.2 \times 10^{-13} + 1.6 \times 10^{-14}} = 0.588 \text{ V}$$

From (29), we get the values of delay at nodes 1 & 2.

$$\tau_2 = -\frac{5 \times 10^3 \times (1.6 \times 10^{-14})^2 \times (0.588 - 5)}{0.588 \times (1.6 \times 10^{-14} + 1.2 \times 10^{-13})} = 7.06 \times 10^{-11} \text{ sec}$$

$$\tau_1 = -\frac{5 \times 10^3 \times (1.2 \times 10^{-13})^2 \times 0.588}{(0.588 - 5) \times (1.6 \times 10^{-14} + 1.2 \times 10^{-13})} = 7.06 \times 10^{-11} \text{ sec}$$

From (12), we get an estimate of the waveforms at the two nodes.

$$v_2(t) = 0.588(1 - \exp(-t/7.06 \times 10^{-11}))$$

$$v_1(t) = 0.588 + 4.412 \exp(-t/7.06 \times 10^{-11})$$

Exactly this waveform is obtained by a SPICE simulation of the charge sharing network.

In fact, the time constants τ_1 and τ_2 obtained by algebraically solving for the voltages in this network are

$$\tau_1 = \tau_2 = r_1 \frac{C_1 C_2}{C_1 + C_2} = 7.06 \times 10^{-11} \text{ sec}$$

Example 2. A standard network.

Consider the NAND gate shown in Fig. 5(a), with both gate transistors in the 'ON' state. The RC network derived from this is shown in Fig. 5(b).

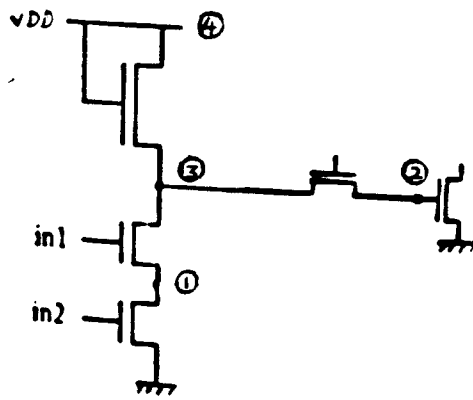


Figure 5(a). A nMOS NAND gate.

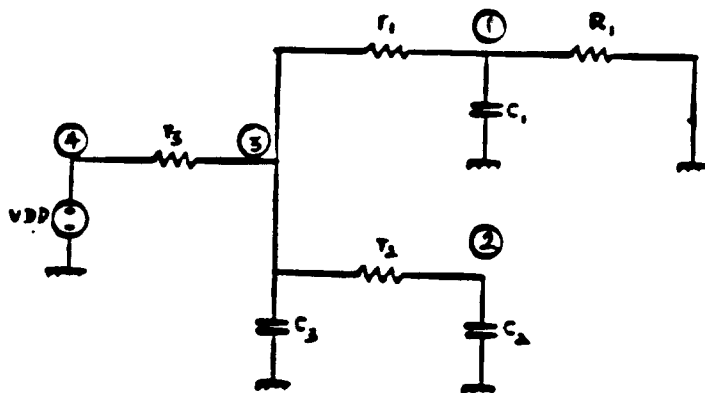


Figure 5(b). An RC network for the circuit of Figure 5(a).

The network parameters for our NAND gate are given below:

$$\begin{aligned}
 n &= 4 \\
 r_1 &= 5 \text{ K } \Omega \\
 r_2 &= 2.5 \text{ K } \Omega \\
 r_3 &= 40 \text{ K } \Omega \\
 R_1 &= 5 \text{ K } \Omega \\
 C_1 &= 1.6 \times 10^{-2} \text{ pF} \\
 C_2 &= 0.8 \times 10^{-2} \text{ pF} \\
 C_3 &= 1.6 \times 10^{-2} \text{ pF} \\
 Q_1 &= 8 \times 10^{-14} \text{ C} \\
 Q_2 &= 4 \times 10^{-14} \text{ C} \\
 Q_3 &= 8 \times 10^{-14} \text{ C} \\
 v_4 &= \text{VDD}
 \end{aligned}$$

The nMOS circuit is clearly in the discharging state: to change the logic state of node 2 from logic '1' to logic '0'.

Solving for the delay at node 2, we obtain:

$$\begin{aligned}
 v_2^{(4)} &= 0.2\text{VDD} \\
 D_2^{(4)} &= -2.272 \times 10^{-10} \text{ VDD} \\
 \tau_2 &= \frac{-2.272 \times 10^{-10} \text{VDD}}{0.2\text{VDD} - \text{VDD}} = 2.79 \times 10^{-10} \text{ sec}
 \end{aligned}$$

Thus the voltage waveform is estimated to be

$$v_2(t) = 0.2\text{VDD} + 0.8\text{VDD} \exp(-t/2.79 \times 10^{-10})$$

Solving for node 1, we get

$$\begin{aligned}
 v_1^{(4)}(\infty) &= 0.1\text{VDD} \\
 D_1^{(4)} &= -1.212 \times 10^{-11} \text{VDD} \\
 \tau_1 &= 1.3467 \times 10^{-11} \text{ sec}
 \end{aligned}$$

The voltage waveform at node 1 is

$$v_1(t) = 0.1\text{VDD} + 0.9\text{VDD} \exp(-t/1.3467 \times 10^{-11})$$

Solving for node 3, we get

$$\begin{aligned}
 v_3^{(4)}(\infty) &= 0.2\text{VDD} \\
 D_3^{(4)} &= -2.112 \times 10^{-10} \text{VDD} \\
 \tau_3 &= 2.64 \times 10^{-10} \text{ sec}
 \end{aligned}$$

The voltage waveform at node 3 is

$$v_3(t) = 0.2\text{VDD} + 0.8\text{VDD} \exp(-t/2.64 \times 10^{-10})$$

Fig. 6(a) - (c) shows plots of the "best fit" waveforms of $v_2(t)$, $v_1(t)$ and $v_3(t)$ respectively for the case where $\text{VDD} = 5 \text{ V}$. Also plotted in the same figures are the waveforms obtained by a SPICE simulation of the RC circuit.

The waveform obtained by our analysis follows the SPICE waveform very closely, although it is a single time constant approximation.

On the other hand, the Lin-Mead model for discharging ignores the path to VDD and gives waveforms that go from VDD to 0.

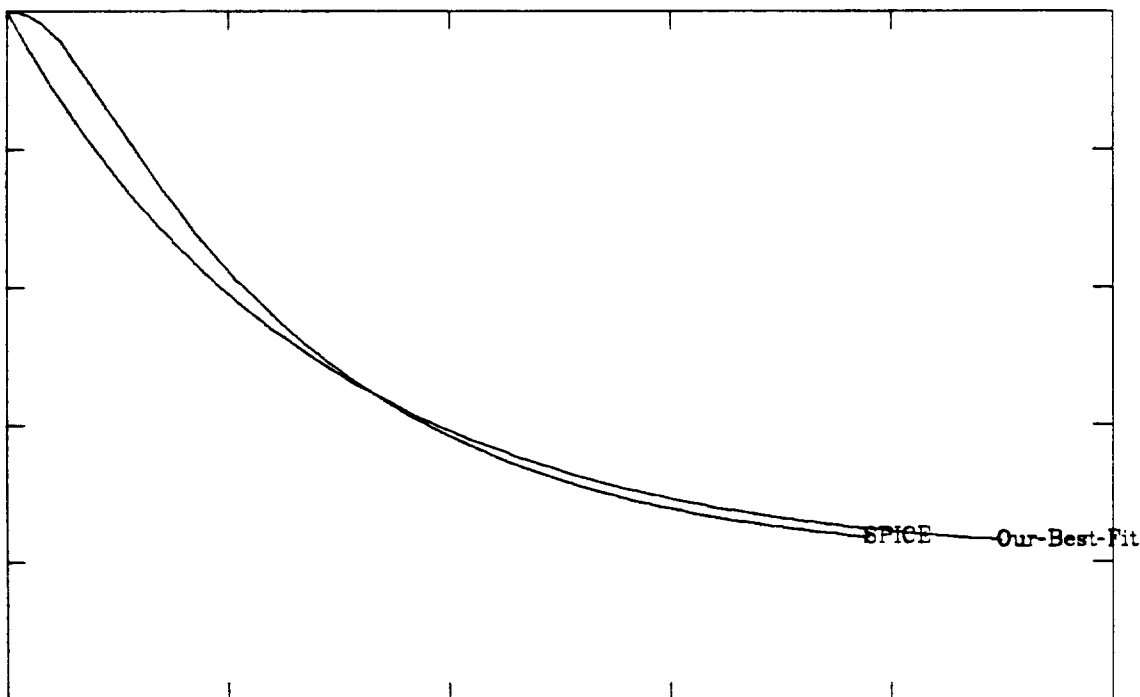


Figure 6(a). The waveform $v_2(t)$ for the circuit of Figure 5.

8. Conclusions

An expression for delay, based upon the delay of Elmore, has been derived for RC trees with charge sharing or leaky capacitors. Our definition of delay provides a "best fit" exponential waveform in networks with charge sharing, with more than one source and with nonideal capacitors. The analysis of the charge sharing and standard networks is a first step towards a uniform characterization of gates, switches, wires and dynamic RAM cells in any current VLSI technology. We are currently examining the use of these networks in ELOGIC [7].

An important fact to keep in mind when using our results is that we have provided a "best fit" single exponential for the linear RC model. A simulation program like SPICE can handle nonlinear circuits, although much more slowly. Thus, an interesting topic for future research is to study the effects of linearization and the speed vs. accuracy tradeoffs in simulation programs.

We also need to study the usefulness of bounding the waveforms of a nonlinear circuit by waveforms derived from a linear circuit, and, if found useful, derive tight lower and upper bounds on the waveform. One important step in this direction is the derivation of bounding waveforms for linear circuits [9, 11, 12].

Another important problem requiring attention is the characterization of wires as transmission lines. Two questions arise: 1) what linear model do we adopt that is both accurate and easy to analyze, and 2) can the ideas used in this paper be adapted to analyze these linear circuits.

We believe it will be possible to extend our results from RC trees to more general classes of RC networks. In particular, it should not be difficult to analyse RC meshes with charge sharing and leakage, since the underlying mathematical structure is still a system of linear differential equations with constant coefficients. Our current research effort is to extend our results to RC networks with floating capacitances, in order to model the important "Miller effect".

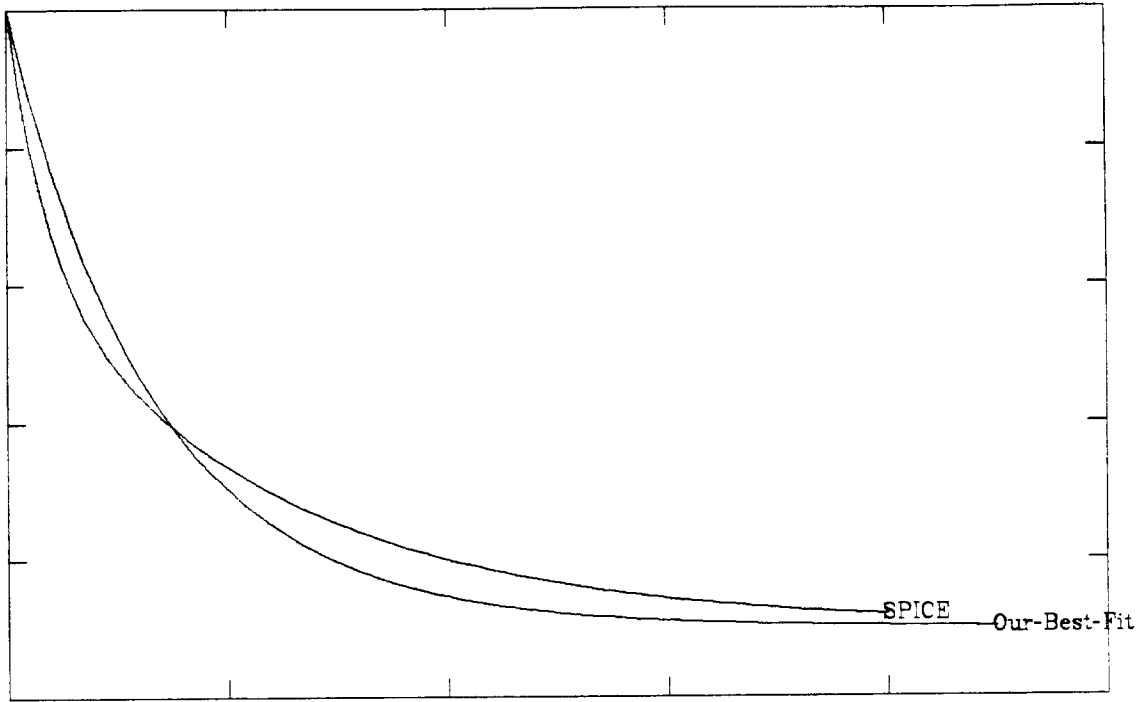


Figure 6(b). The waveform $v_1(t)$ for the circuit of Figure 5.

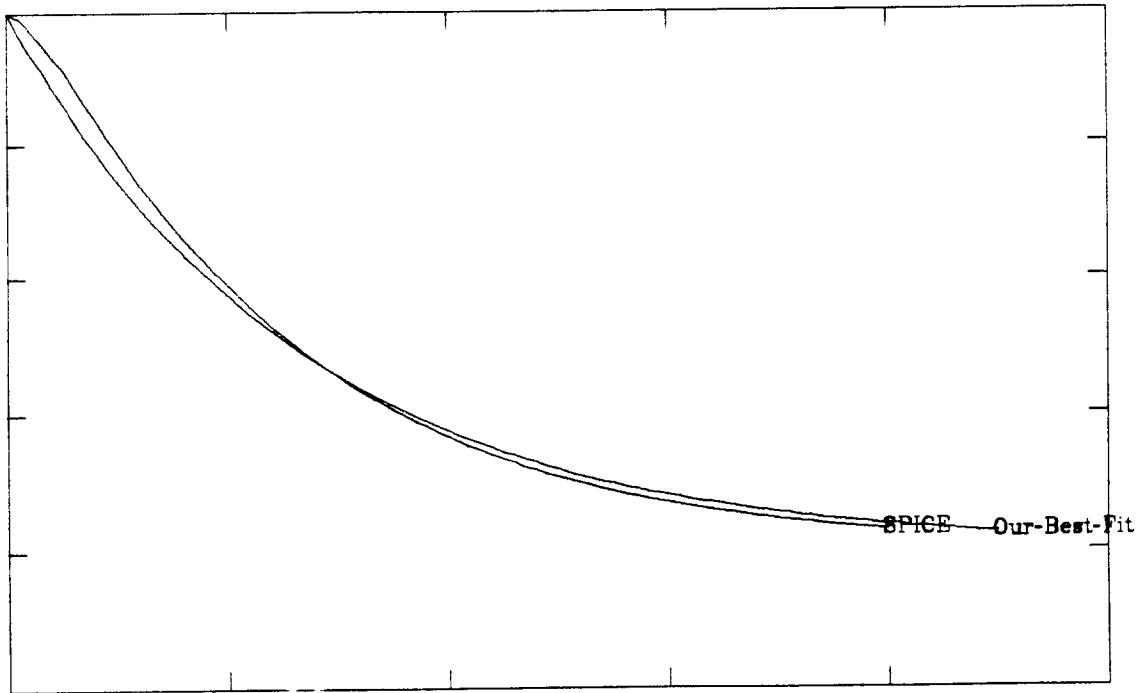


Figure 6(c). The waveform $v_3(t)$ for the circuit of Figure 5.

Appendix.

Proof of Theorem 1. From (4), it follows that

$$v_i(\infty) = v_i(0) + c_{i,1} + \dots + c_{i,n}$$

and

$$V_i(s) = \frac{1}{s} \left[\frac{v_i(0) \prod_{k=1}^n (1 + t_{i,k} s) + c_{i,1} \prod_{k \neq 1}^n (1 + t_{i,k} s) + \dots + c_{i,n} \prod_{k=1}^{n-1} (1 + t_{i,k} s)}{\prod_{k=1}^n (1 + t_{i,k} s)} \right]$$

It follows that

$$b_{i,1} = t_{i,1} + \dots + t_{i,n}$$

and

$$a_{i,1} = \frac{v_i(0)(t_{i,1} + \dots + t_{i,n}) + c_{i,1}(t_{i,2} + \dots + t_{i,n}) + \dots + c_{i,n}(t_{i,1} + \dots + t_{i,n-1})}{v_i(0) + c_{i,1} + \dots + c_{i,n}}$$

Thus,

$$\tau_1^0 = b_{i,1} - a_{i,1} = \frac{c_{i,1}t_{i,1} + \dots + c_{i,n}t_{i,n}}{v_i(\infty)}$$

Proof of Theorem 2. The Superposition Theorem [2] states that, at any time t ,

$$\begin{aligned} v_i(n, r, R, C, Q, V) &= v_i(n, r, R, C, Q, [v_1, \text{GND}, \dots, \text{GND}]) \\ &\quad + v_i(n, r, R, C, Q, [\text{GND}, v_2, \dots, \text{GND}]) \\ &\quad + \dots \\ &\quad + v_i(n, r, R, C, Q, [\text{GND}, \text{GND}, \dots, v_n]) \end{aligned}$$

Since integration is a linear operation, Theorem 2 follows immediately from this and the definition of D_i .

Proof of Theorem 3. Again, from the Superposition Theorem, we have, at any time t ,

$$v_i(n, r, R, C, Q, \text{VDD}_n) = v_i(n, r, R, C, Q, \text{GND}_n) + v_i(n, r, R, C, 0, \text{VDD}_n)$$

Theorem 3 follows immediately from this and the definition of D_i .

Proof of Theorem 4. Instead of directly evaluating the various integrals in (35), we consider the expression for D_i in the Laplace transform domain.

$$D_i = \lim_{s \rightarrow 0} \left[\sum_{k=1}^{n-1} R_{k,i} \left\{ C_k (s V_k(s) - v_k(0)) + \frac{V_k(s)}{R_k} \right\} - \frac{R_{k,i}}{R_k} \frac{v_k(\infty)}{s} \right] \quad (1')$$

From (2) and (1'), we have

$$D_i = \lim_{s \rightarrow 0} \sum_{k=1}^{n-1} R_{k,i} C_k v_k(\infty) \frac{(1 + a_{k,1}s + \dots + a_{k,n}s)}{(1 + b_{k,1}s + \dots + b_{k,n}s)} - \frac{R_{k,i}}{R_k} \frac{v_k(\infty)}{s} \left[1 - \frac{(1 + a_{k,1}s + \dots + a_{k,n}s)}{(1 + b_{k,1}s + \dots + b_{k,n}s)} \right]$$

On taking limits, we get

$$D_i = \sum_{k=1}^{n-1} R_{k,i} C_k (v_k(\infty) - v_k(0)) - \frac{R_{k,i}}{R_k} v_k(\infty) (b_{k,1} - a_{k,1})$$

From (10) and (13), we know that D_k is the same as $v_k(\infty) \cdot b_{k,1} - a_{k,1}$.

Theorem 4 follows from a rearrangement of terms.

Proof of Theorem 5(a). From Fig. 3(a) and the definitions, the expressions for $\rho^{(2)}$, $v_1^{(2)}(\infty)$, $\bar{C}^{(2)}$ and $Q^{(2)}$ follow.

By simple analysis of the circuit using Kirchoff's laws, we have

$$V_1^{(2)}(s) = \frac{\text{VDD} \left\{ \frac{R_1}{r_1 + R_1} \right\} \left\{ 1 + s \frac{v_1(0)}{\text{VDD}} C_1 r_1 \right\}}{s \left\{ 1 + s C_1 \frac{r_1 R_1}{r_1 + R_1} \right\}}$$

Hence, we have

$$\tau_1^{(2)} = (b_{1,1} - a_{1,1}) \frac{v_1(\infty)}{v_1(\infty) - v_1(0)} = \left\{ \frac{C_1 r_1 R_1}{r_1 + R_1} - \frac{v_1(0)}{\text{VDD}} C_1 r_1 \right\} \frac{v_1(\infty)}{v_1(\infty) - v_1(0)}$$

By simple algebraic manipulation, we can show that

$$\tau_1 = C_1 \frac{r_1 R_1}{r_1 + R_1}$$

Therefore, the expressions for $D_1^{(2)}$ and $DO_1^{(2)}$ follow.

Now, the expressions for $(R_1^{(2)})$, $\sigma^{(2)}$, $\Delta^{(2)}$ and $\Delta_0^{(2)}$ follow.

Proof of Theorem 5(b). The expressions for $\rho^{(n+1)}$, $v_n^{(n+1)}(\infty)$, $v_i^{(n+1)}(\infty)$ and $Q^{(n+1)}$ follow from their definitions and Fig. 3(b).

The expression for $\bar{C}^{(n+1)}$ now follows from its definition and the expression for $v_i^{(n+1)}(\infty)$.

In the subsequent discussion, all primed parameters stand for quantities in N_{n+1} and unprimed parameters for quantities in N_n . In N_{n+1} , the system of equations represented by (36) becomes

$$\begin{aligned} \frac{r_n}{R_n} D_n^{(n+1)} + \left\{ 1 + \frac{R'_{i,i}}{R_i} \right\} D_i^{(n+1)} + \sum_{k \neq i}^{n-1} \frac{R'_{k,i}}{R_k} D_k^{(n+1)} \\ = \sum_{k=1}^{n-1} R'_{k,i} C_k (v_k^{(n+1)}(\infty) - v_k(0)) + r_n C_n (v_n^{(n+1)}(\infty) - v_n(0)) \end{aligned} \quad i=1,2,\dots,n-1 \quad (2')$$

and,

$$\begin{aligned} \left\{ 1 + \frac{r_n}{R_n} \right\} D_n^{(n+1)} + \sum_{k=1}^{n-1} \frac{r_n}{R_k} D_k^{(n+1)} \\ = \sum_{k=1}^{n-1} r_n C_k (v_k^{(n+1)}(\infty) - v_k(0)) + r_n C_n (v_n^{(n+1)}(\infty) - v_n(0)) \end{aligned} \quad (3')$$

Let

$$D_i^{(n+1)} = D_i^{(n)} + \Delta D_i^{(n)}$$

Subtracting (36) from (2'), we get

$$\begin{aligned} \left\{ 1 + \frac{R'_{i,i}}{R_i} \right\} \Delta D_i^{(n)} + \sum_{k \neq i}^{n-1} \frac{R'_{k,i}}{R_k} \Delta D_k^{(n)} + \frac{r_n}{R_n} D_n^{(n+1)} \\ = \sum_{k=1}^{n-1} R'_{k,i} C_k (v_k^{(n+1)}(\infty) - v_k^{(n)}(\infty)) + \sum_{k=1}^{n-1} r_n C_k (v_k^{(n+1)}(\infty) - v_k(0)) \\ + r_n C_n (v_n^{(n+1)}(\infty) - v_n(0)) \\ - \sum_{k=1}^{n-1} \frac{r_n}{R_k} D_k^{(n)} \end{aligned} \quad (4')$$

Rewriting (3'), we have

$$\begin{aligned} & \sum_{k=1}^{n-1} \frac{r_n}{R_k} \Delta D_k^{(n)} + \left(1 + \frac{r_n}{R_n}\right) D_n^{(n+1)} \\ &= \sum_{k=1}^{n-1} r_n C_k (v_k^{(n+1)}(\infty) - v_k(0)) + r_n C_n (v_n^{(n+1)}(\infty) - v_n(0)) - \sum_{k=1}^{n-1} \frac{r_n}{R_k} D_k^{(n)} \end{aligned} \quad (5')$$

From eqns. (4') and (5'), and using the expression for $v_k^{(n+1)}(\infty)$, we get

$$\begin{aligned} & (1 + R_{i,i}) \Delta D_i^{(n)} + \sum_{k \neq i}^n \frac{R_{k,i}}{R_k} \Delta D_k^{(n)} \\ &= D_n^{(n+1)} + \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right) \sum_{k=1}^{n-1} R_{k,i} C_k v_k^{(n)}(\infty) \quad i=1,2,\dots,n-1 \end{aligned} \quad (6')$$

We can now put the system of equations represented by (6') into matrix form as follows.

$$\mathbf{R} \cdot \Delta \mathbf{D} = \mathbf{D}_n^{(n+1)} + \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right) \cdot \mathbf{T}_0 \quad (7')$$

where

$$\Delta \mathbf{D} = \begin{bmatrix} \Delta D_1^{(n)} \\ \Delta D_2^{(n)} \\ \vdots \\ \Delta D_{n-1}^{(n)} \end{bmatrix} \quad \mathbf{D}_n^{(n+1)} = \begin{bmatrix} D_n^{(n+1)} \\ D_n^{(n+1)} \\ \vdots \\ D_n^{n+1} \end{bmatrix}$$

and

$$\mathbf{T}_0 = \begin{bmatrix} \sum_{k=1}^{n-1} R_{k,1} C_k v_k(\infty) \\ \sum_{k=1}^{n-1} R_{k,2} C_k v_k(\infty) \\ \vdots \\ \sum_{k=1}^{n-1} R_{k,n-1} C_k v_k(\infty) \end{bmatrix}$$

From (7'), it follows that

$$\Delta D_i^{(n)} = (R_i^r)^{(n)} D_n^{(n+1)} + D \theta_i^{(n)} \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right) \quad (8')$$

Going through a similar analysis for $\Delta D \theta_i^{(n)}$, we get

$$\Delta D \theta_i^{(n)} = (R_i^r)^{(n)} D \theta_n^{(n+1)} + D \theta_i^{(n)} \left(\frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right) \quad (9')$$

Substituting (8') in (5') and using the definitions, we get

$$D_n^{(n+1)} = \frac{\bar{C}^{(n+1)} - Q^{(n+1)} - \Delta^{(n)} - \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} - 1 \right\} \Delta_0^{(n)}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} \quad (10')$$

It follows that

$$D\theta_n^{(n+1)} = \frac{\bar{C}^{(n+1)} - \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \Delta_0^{(n)}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} \quad (11')$$

From (9') and (11'), we get an expression for $D\theta_i^{(n+1)}$.

$$D\theta_i^{(n+1)} = (R_i^r)^{(n)} \left[\frac{\bar{C}^{(n+1)} - \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \Delta_0^{(n)}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} \right] + \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} D\theta_i^{(n)} \quad (12')$$

and from (8') and (12')

$$D_i^{(n+1)} = D_i^{(n)} + D\theta_i^{(n+1)} - D\theta_i^{(n)} - \frac{(R_i^r)^{(n)}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} \cdot (Q^{(n)} + \Delta^{(n)} - \Delta_0^{(n)}) \quad (13')$$

From the definitions of $\Delta_0^{(n+1)}$ and $\Delta^{(n+1)}$, and from (12') and (13') we get

$$\Delta_0^{(n+1)} = \frac{\left\{ \frac{1}{R_n} + \sigma^{(n)} \right\}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} \left\{ \bar{C}^{(n+1)} - \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \Delta_0^{(n)} \right\} + \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \Delta_0^{(n)} \quad (14')$$

and

$$\Delta^{(n+1)} = \Delta^{(n)} + \Delta_0^{(n+1)} - \Delta_0^{(n)} - \frac{\sigma^{(n)}}{\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n}} (Q^{(n+1)} + \Delta^{(n)} - \Delta_0^{(n)}) \quad (15')$$

To prove the rest of the theorem, we rewrite (11') as follows:

$$\left(\sigma^{(n)} + \frac{1}{R_n} + \frac{1}{r_n} \right) D\theta_n^{(n+1)} = \bar{C}^{(n+1)} - \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \Delta_0^{(n)}$$

Using the definitions, we expand the terms to get

$$\begin{aligned} & \left(1 + \frac{r_n}{R_n} + r_n \sigma^{(n)} \right) D\theta_n^{(n+1)} \\ &= r_n \left(v_n^{(n+1)}(\infty) C_n + \sum_{k=1}^{n-1} C_k v_k^{(n+1)}(\infty) \right) - r_n \left\{ \frac{v_n^{(n+1)}(\infty)}{\text{VDD}} \right\} \sum_{k=1}^{n-1} \frac{D\theta_k^{(n)}}{R_k} \end{aligned}$$

Again, expanding for $D\theta_k$, we get

$$\begin{aligned} \left(1 + \frac{r_n}{R_n} + r_n \sigma^{(n)}\right) D\theta_n^{(n+1)} &= r_n \left[v_n^{(n+1)}(\infty) C_n + \sum_{k=1}^{n-1} C_k v_k^{(n+1)}(\infty) \right] \\ &- \frac{r_n}{\text{VDD}} \left[\sum_{j=1}^{n-1} \frac{1}{R_j} \right] \sum_{k=1}^{n-1} (R_k^c)^{(n)} \left[\sum_{i=1}^n R_{i,k} C_i v_i^{(n+1)}(\infty) \right] \\ &+ \frac{r_n^2}{\text{VDD}} \left[\sum_{j=1}^{n-1} \frac{1}{R_j} \right] \left[\sum_{i=1}^{n-1} (R_i^c)^{(n)} \right] \left[C_n v_n^{(n+1)}(\infty) + \sum_{k=1}^{n-1} C_k v_k^{(n+1)}(\infty) \right] \end{aligned} \quad (16')$$

where $(R_i^c)^{(n)}$ denotes the sum of all elements in column i of the $n-1 \times n-1$ matrix \mathbf{R}^{-1} .

By rearranging terms in (16'), we get

$$\begin{aligned} \left(1 + \frac{r_n}{R_n} + r_n \sigma^{(n)}\right) D\theta_n^{(n+1)} &= \left[1 + \frac{r_n}{\text{VDD}} \left[\sum_{j=1}^{n-1} \frac{1}{R_j} \right] \left[\sum_{i=1}^{n-1} (R_i^c)^{(n)} \right] \right] \sum_{k=1}^n R_{k,n} C_k v_k^{(n+1)}(\infty) \\ &- \sum_{i=1}^{n-1} \left[\frac{r_n}{\text{VDD}} \left[\sum_{j=1}^{n-1} \frac{1}{R_j} \right] (R_i^c)^{(n)} \right] \sum_{k=1}^{n-1} R_{k,i} C_k v_k^{(n+1)}(\infty) \end{aligned}$$

Now, from the definition of $(R_n^r)^{(n+1)}$, it follows that

$$(R_n^r)^{(n+1)} = \frac{1}{1 + \frac{r_n}{R_n} + r_n \sigma^{(n)}} \quad (17')$$

and from (9') and (17'), we get

$$(R_n^r)^{(n+1)} = (R_i^c)^{(n)} (R_n^r)^{(n+1)} \quad (18')$$

The expression for $\sigma^{(n+1)}$ now follows from its definition and eqns. (17') and (18').

The final forms of the expressions for $D_n^{(n+1)}$, $D\theta_n^{(n+1)}$, $D\theta_i^{(n+1)}$, $D_i^{(n+1)}$, $\Delta_0^{(n+1)}$ and $\Delta^{(n+1)}$ can now be obtained from (10'), (11'), (12'), (13'), (14'), (15') respectively by simple algebraic manipulation.

Proof of Theorem 5(c). From Fig. 3(c), it is clear that $\rho^{(n+m-1)}$ is the parallel combination of $\rho^{(n)}$ and $\rho^{(m)}$.

Again, from Fig. 3(c), we note that the final voltage reached at any node in N_{n+m} is the same as the final voltage reached in N_n or N_m , since these two networks are connected only at the source node. Hence, it follows that

$$\bar{C}^{(n+m-1)} = \bar{C}^{(n)} + \bar{C}^{(m)}$$

The expressions for $D_i^{(n+m-1)}$ and $D\theta_i^{(n+m-1)}$ hold for the same reason.

The expression for $Q^{(n+m-1)}$ follows from its definition.

To see why the expression for $(R_i^r)^{(n+m-1)}$ holds, note that the system of equations represented by (37) now has $n+m-2$ variables and $n+m-2$ equations. Entries in the matrix \mathbf{R} corresponding to rows i , $i=1,2,\dots,n-1$ and columns j , $j=n,n+1,\dots,n+m-2$ are all zero, as are the entries corresponding to rows i , $i=n,n+1,\dots,n+m-2$ and columns j , $j=1,2,\dots,n-1$. The other entries are the same as in the \mathbf{R} matrices for N_n or N_m .

The expressions for $\sigma^{(n+m-1)}$, $\Delta_0^{(n+m-1)}$ and $\Delta^{(n+m-1)}$ follow from their definitions and the discussion above.

Proof of Corollary 1. From the proof of Theorem 1 and from (10), the corollary follows.

Proof of Corollary 2. Since Q represents the final charge attained by $N(n, r, R, C, 0, \text{VDD}_n)$, $D_i(n, r, R, C, Q, \text{VDD}_n)$ is 0. Now, the corollary follows from Theorem 3.

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