SHALLOW DIFFUSION OF GeSe IN GaAs USING RAPID THERMAL ANNEALING TO FORM NON-ALLOYED OHMIC CONTACTS

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ABSTRACT

We have formed non-alloyed, ohmic contacts to GaAs by contacting heavily-doped n+ regions. These n+ regions are formed by using rapid thermal annealing (RTA) with a high-intensity tungsten-halogen lamp to diffuse germanium and selenium from a deposited GeSe thin-film. RTA reduces surface degradation and improves crystal reparation compared to lengthy furnace cycles, although furnace annealing produces identical electrical characteristics. RTA also permits better control of the diffusion profile than conventional furnace annealing. Ion-beam mixing prior to RTA has only a small effect on the diffusion of a deposited GeSe film, because the damage created by implantation is repaired during RTA before significant diffusion occurs. We define a threshold temperature representing the onset of significant diffusion and/or electrical activation, and propose a model relating the annealing, activation, and diffusion temperatures for the GeSe/GaAs system. Optimal 20-second RTA occurs above a diffusion threshold at 950^{o}C but below the failure of the sputtered SiO_2 encapsulant at 1100^{o}C.

The n+ regions created have peak impurity concentrations over $10^{20}/cm^3$ at depths under 750 Å with sheet resistances less than 60 Ω/□. Non-alloyed ohmic contacts exhibit specific contact resistivities of $2.2 \times 10^{-4}\ \Omega \cdot cm^2$. This technique has application to the formation of ohmic contacts for GaAs integrated circuits.

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Yao-Hwa Wu provided invaluable help during several laboratory experiments, and now has me considerably in his debt. The MBE and quantum electronics groups in general answered hundereds of naive questions about GaAs processing. Steve Lester designed the test pattern used in the contact resistivity measurements. Paul Chu performed all the SIMS analysis. John van Lueewen provided the furnace annealing, and Wingyu Leung designed the GeSe evaporation system. The U. C. Berkeley microlab staff gave considerable assistance in keeping the troublesome RTA system on its feet. Finally, many thanks to everyone in 373 Cory, who kept things interesting and put up with frequently bizarre behavior.

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1. INTRODUCTION

Gallium arsenide (GaAs) is gaining prominence as an alternative material for high-speed digital and microwave integrated circuits. The primary advantages of GaAs include extremely high speed due to high electron mobility, radiation hardness, and high resistivity when compensated by a deep-level acceptor.[1] There is potential to integrate GaAs devices on-chip with opto-electronic devices, and the improving GaAs technology is impacting microwave and digital circuits. As in silicon technology, high yield and reproducible fabrication are primary concerns in GaAs device manufacture.

Low-resistance ohmic contacts are essential for the fabrication of high-speed GaAs devices. The ability to form these contacts reliably is one of the limits of GaAs technology at this time. Most contacts are currently formed by alloying on the GaAs surface a thin-film consisting of the contact metal (gold) and a dopant (germanium). During alloying at 450°C a portion of the GaAs is dissolved in the alloy while the dopant diffuses into the GaAs. Upon cooling the dopant is incorporated into the epitaxially regrown GaAs.[2] A tunneling ohmic contact results from the formation of a heavily-doped semiconductor layer at the metal-GaAs interface. Since this conventional alloying process involves a heat treatment above the Au-GaAs eutectic temperature, a liquid phase occurs that can result in an uneven contact interface and a poorly controlled junction depth. A thin layer of nickel deposited on top of the AuGe film prior to alloying reduces but does not completely alleviate these problems. The poor interface morphology can lead to significant yield problems

for small devices with shallow junctions and high current densities.

An alternative technique for making ohmic contacts to GaAs devices is to form non-alloyed contacts to heavily-doped regions. An alloying step is unnecessary if a heavily-doped region is present at the semiconductor surface before the metal is deposited. These contacts produce ohmic characteristics after only a low-temperature sinter. Because the metal is not melted, non-alloyed contacts result in a more even and reproducible interface. Furthermore, refractory metals can be used to contact the GaAs. The creation of a shallow, heavily-doped region is the first step in forming a non-alloyed, ohmic contact. A shallow region allows control of the contact depth and the lateral diffusion, and thereby permits smaller device geometries.

Non-alloyed ohmic contacts to n-type GaAs are most frequently formed to heavily-doped regions prepared by ion implantation[3,4,5,6] and molecular-beam epitaxy (MBE).[7,8] Both of these techniques have disadvantages, however. Ion implantation into a crystalline substrate leaves a channeling tail that can make the heavily-doped region deeper than desired. Implantation in GaAs is further limited by the low activation efficiency of the implanted impurity. MBE has the disadvantage of requiring mesa isolation to separate individual ohmic regions, resulting in a non-planar structure that is not suited to large integration levels.

Another method for forming these heavily-doped contact regions in GaAs is the diffusion of impurities from a deposited thin-film source. This method is attractive because it creates a shallow layer of high impurity concentration while avoiding the activation problems and deep impurity profiles associated with doping by ion implantation. In particular, diffusion of impurities with small diffusivities allows good control of shallow junction depths and short gate lengths. Previous work in forming shallow n+ regions by diffusion includes the thermal diffusion of tin from a SnO_2/SiO_2 thin-film with[9] and without[10] the assistance of continuous-wave laser irradiation, and the pulse-annealed diffusion of selenium from a As_2Se_3 source.[11]

Our approach to the formation of non-alloyed ohmic contacts to GaAs involves codiffusants, ion-beam mixing, and rapid thermal annealing (RTA). In this study, we report on the codiffusion of germanium and selenium from a thin-film source using ion-beam mixing followed by RTA with a high-intensity tungsten-halogen lamp. Ohmic contacts are then formed by depositing metal and performing a low-temperature sinter. Codiffusants appear to take advantage of the slow diffusion of germanium and selenium on different sublattices to form shallow n+ layers. Ion-beam mixing disperses interfacial contaminants, causes atomic mixing of the GeSe thin-film and the GaAs surface, and creates mobile defects such as vacancies and interstitials. All of these effects can enhance the substitutional diffusion of impurities.[12] Using rapid thermal annealing (RTA) to diffuse and activate the GeSe thin-film prior to metal deposition involves higher annealing temperatures with shorter cycle times than furnace annealing, thereby leading to shallower junctions, better surface morphology, and simpler processing.

The diffused layers formed by RTA after deposition of a GeSe layer have peak concentrations over $10^{20}/cm^3$ at depths under 750 Å. The ohmic contacts formed to this layer have a specific contact resistance of 55 $\Omega/\square$ and a sheet resistance of $2.2 \times 10^{-4} \Omega \cdot cm^2$. The results of this study have previously been reported at the Spring and Fall Symposiums of the Materials Research Society.[13, 14] This report is centered around those two publications, but includes a background section as well as details that were not included in the previous papers.

2. BACKGROUND

The intent of this project is to form non-alloyed ohmic contacts to GaAs. Our technique begins with the diffusion of a GeSe thin-film into GaAs to form shallow, heavily-doped regions. We use ion-beam mixing and rapid thermal annealing to enhance and control the diffusion, respectively. We then form ohmic contacts to these diffused regions, and use contact resistivity measurements to determine the quality of the contacts.

While the third and fourth sections of this report refer to the practical aspects of these subjects, this second section describes the theory behind each subject. In addition, the subject of post-etching films on GaAs is also treated.

2.1. Diffusion of Germanium Selenide

Diffusion is an alternative to ion implantation and molecular beam epitaxy for forming doped regions in semiconductors. We use germanium and selenium as the doping impurities due to their slow diffusivities and mutual interaction.

2.1.1. Doping Techniques

Ion implantation has become the most prevalent doping technique due to considerations of cleanliness and high volume. Unfortunately, the formation of shallow contact regions by ion implantation is impeded by channeling tails that can extend the doped region several thousand angstroms into the crystal. Shallow, heavily-doped regions are desirable in forming ohmic contacts because they reduce the barrier height for tunneling currents. Shallow regions also give better control over device dimensions, such as the gate length, and thereby allow greater circuit density.

Beyond the problem of channeling tails, which are inherent to implantation into a semiconductor crystal, there are several problems specific to implanting into GaAs. While a high percentage of implanted ions are routinely activated in silicon, implantation into GaAs generally results in less efficiency. GaAs implantation also pushes the capabilities of

most existing implantation systems by requiring energies in the 200-500 keV range, while silicon technology requires only 50-150 keV for most applications. Finally, the damage created by implantation, which is discussed in section 2.2, must be annealed at high temperatures that cause dissociation problems in the GaAs crystal.

Molecular beam epitaxy (MBE), on the other hand, has the disadvantage of requiring mesa isolation between contact regions, and is therefore not compatible with large scale integration.[4] The low volume and high cost of MBE systems also detract from this technique. Diffusion is a promising alternative for contact region doping, especially if dopants are chosen that have small diffusion constants. Both of the dopants used in this project diffuse slowly in GaAs so that shallow, heavily-doped regions may be reproducibly formed. Germanium and selenium also exhibit several specific properties that make their use advantageous.

2.1.2. Germanium-Selenide Glass

We use germanium selenide as an n+ diffusion source in this project. Its primary use in microelectronics has been as part of a high-contrast, multi-level resist system. Multi-level resists aid patterning of non-planar topologies and increase packing density by giving good control over critical dimensions. The resist system based on silver-doped GeSe is especially beneficial because it combines the advantages of multi-level resists with unique material characteristics.[15] This system has demonstrated the highest resolution of any resist material to date[16] and shows potential for pushing the limits of optical lithography.

As described by Leung, et al.[17] the silver-doped Ge_xSe_{1-x} (x=.10) system begins with a thick, organic planarizing layer (1.3 microns) that is rendered light-insensitive by a 45 minute hard-bake at 180 °C. A film of Ge_xSe_{1-x} glass (approximately 2,000 Å) is then deposited by electron-beam evaporation. Finally, a Ag_2Se layer (approximately 90 Å) is formed by immersing the wafer in an aqueous solution of silver nitrate and potassium cyanide for 60 seconds. During optical exposure (λ = 4360 Å) the silver in the lighted

areas receives energy and migrates vertically from the Ag_2Se layer into the Ge_xSe_{1-x} layer. This photodoping process creates an silver concentration gradient in the Ag_2Se layer that causes silver to diffuse laterally from dark to lighted areas.[18] Since the exposing UV light is attenuated by the silver atoms as it passes vertically through the Ag_2Se layer, the removal of silver by photodoping from this upper layer effectively "bleaches" the Ag_2Se. The lateral and vertical silver transport mechanisms are responsible for both photobleaching and photodoping, which in turn contribute in this resist system to the phenomena of contrast enhancement, edge sharpening, feature-dependent amplification and feature-dependent photodoping suppression.

This bi-level resist system was developed by Tai, et al at Bell Laboratories[19] and further studied at U. C. Berkeley by Leung.[17, 20, 21] The present research evolved during this latter period due to the ability of both germanium and selenium to act as n-type dopants in GaAs. Selenium, a group VI element, will be substitutionally incorporated on the arsenic sublattice.[22] Germanium, a group IV element, can be incorporated into either the gallium or arsenic sublattice and will act as an n- or p-type dopant, respectively. This dual doping behavior is common in compound semiconductors such as GaAs, and the dopant is described as amphoteric. Which sublattice the germanium is incorporated on depends on the relative vacancy concentration. Since the selenium diffusion reduces the number of arsenic vacancies, the germanium is expected to be incorporated largely on the gallium lattice as an n-type dopant.

Compensation is one side effect of using an amphoteric dopant such as germanium. Even though most of the germanium is incorporated onto the gallium sublattice, some will take sites on the arsenic sublattice. Because both ionized donors and acceptors are present, the net free-carrier concentration will be less than the impurity concentration. This compensation effect lowers the mobility compared to that of uncompensated material with an equal concentration of electrically active dopants.[23] The decrease in mobility results from Coulombic scattering off the ionized impurities, which are present in larger numbers in

compensated material than in uncompensated material of the same net doping. In addition, selenium can form inactive compounds with gallium at high concentrations (Ga_2Se_3) that further reduce the free-carrier concentration for a given impurity doping.[24]

In summary, codiffusants appear to take advantage of the slow diffusion of selenium and germanium on different sublattices to form shallow n+ layers. To enhance this diffusion, we use ion-beam mixing and rapid thermal annealing, which are discussed in the following two sections.

2.2. Ion-Beam Mixing

Ion-beam mixing uses ion implantation to mix a solid-state interface by nuclear stopping. Conventional ion implantation forces energetic ions into a sample. These ions are slowed by electronic and nuclear collisions. During nuclear collisions the penetrating ion physically collides with the lattice atoms and can displace atoms from regular lattice sites. This mixing effect enhances diffusion and allows interfacial reactions to occur at a lower temperature than otherwise possible.

Ion-beam mixing has been applied to the formation of contacts, silicides and nonequilibrium phases.[25, 26, 27, 12] In our particular application ion-beam mixing is expected to enhance diffusion by three mechanisms. Firstly, the ions disperse impurities at the GeSe/GaAs interface. Regardless of how carefully the substrate is cleaned, a residual surface layer of approximately 20 Å remains. This surface layer is discussed in section 2.4. Other impurity layers can also form beneath the GeSe source film and hinder diffusion. The knock-on effect of ion implantation effectively removes this barrier to atomic diffusion. Secondly, the knock-on effects of implantation atomically mix the interface and create a shallow GeSe donor layer in the GaAs before annealing begins. Thirdly, nuclear collisions create defects, probably including vacancies, interstitials and defect clusters, which enhance diffusion of the source impurities into the substrate by providing sites for substitutional diffusion. The result of these mechanisms is enhanced diffusion at lower

temperatures with more lateral uniformity.

Efficient ion-beam mixing requires that the majority of the energy lost by the incoming ion be transferred into lattice displacements. Figure 1 is instructive in understanding how the energy dissipated during ion implantation is divided between nuclear and electronic stopping. Electronic stopping will initially dominate for a high-energy ion, and the energy lost will be deposited as heat. As the ion continues into the material and loses energy, the amount of electronic stopping decreases while the amount of nuclear stopping increases. When the ion's energy has decreased to E_c the energy dissipated in electronic and nuclear stopping are equal. At energies below E_c nuclear stopping dominates, and the energy is converted into both heat and lattice displacements. The lattice displacements constitute the crystal damage, and result in dislocation loops or even amorphization that must be repaired by annealing.

The proportion of nuclear stopping that contributes to lattice displacements is discussed elsewhere.[26, 28] In the simplest case, the incoming ion is traveling slowly enough that a hard-sphere model for its interaction with the lattice atom is valid. The number of lattice atoms displaced is then

$$N_d = \frac{E_n}{2E_d} \tag{1}$$

where N_d is the number of displaced lattice atoms, E_n is the amount of energy lost in nuclear stopping, and E_d is the energy necessary to displace a lattice atom far enough that spontaneous recombination does not occur. The hard-sphere model becomes invalid if the incoming ion is traveling fast enough that it approaches the lattice atom closer than the Thomas-Fermi screening radius. The threshold energy corresponding to this velocity is given by

$$E_h = 2E_R Z_1 Z_2 (Z_1^{2/3} + Z_2^{2/3})^{1/2} \frac{(M_1 + M_2)}{M_2} \tag{2}$$

where E_R is 13.6 eV and Z and M are the atomic number and mass of the incoming ion and lattice atom, respectively. Above this energy the number of lattice atoms displaced is no longer a simple function of the energy lost in nuclear stopping. Furthermore, the efficiency of producing displacements decreases above this energy as only some of the nuclear collisions result in displacement of the target atom.

The E_h for arsenic implanted into GaAs is 250 keV, so we may assume that all the energy from our 120 keV implants is transferred into lattice displacements. For silicon implanted into GaAs, E_h = 70 keV, rendering the simple hard-sphere model invalid for 120 keV implants. However, Kinchin and Pease[29] define another threshold energy at which approximately half of the energy lost in nuclear collisions results only in lattice vibrations as opposed to actual atomic displacements. This critical energy is

$$E_b = \frac{M_1 M_2}{(M_1 + M_2)^2} \frac{E_h^2}{E_d} \tag{3}$$

where E_d is approximately 15 eV for GaAs.[30] In this project the incident energy is significantly less than E_b for both silicon and arsenic implants, so we may assume that all the energy lost in nuclear stopping leads to the displacement of target atoms.

This discussion simplifies the actual situation by ignoring the effects of ion recoil, in which the displaced atom can in turn displace other atoms in a cascading effect. Nuclear stopping may also cause several types of damage depending on the ion energy and mass. Simple vacancies unfortunately do not form all the defects in a disordered crystal. One fallacy of this simple model is that electrical activation of impurities does not occur until approximately 1000 ^{o}C, while the vacancy impurity pairs are annealed at 600 ^{o}C. Apparently there are other complexes formed that are more stable and require higher annealing temperatures to remove.

Even with these simplifications our approximations of nuclear stopping are adequate to calculate ion-beam mixing effects. In general, nuclear stopping is maximized by using

low incident energies and heavy ions. The energy density dissipated in nuclear stopping is a function of the depth below the surface of the sample, but generally peaks at a shallower depth than the range distribution, as illustrated in Figure 2. Hence the ion mass, ion energy, and the thickness of the encapsulation must be tailored to maximize the nuclear stopping at the point where mixing is required. In this project we tailored the implant energy and encapsulation thickness using a computer generated LSS approach such that the nuclear stopping distribution would peak at the GaAs/GeSe interface to maximize atomic mixing and knock-on effects.

2.3. Rapid Thermal Processing

Rapid thermal processing (RTP) uses high-intensity radiation to heat a sample to a precisely controlled temperature in a very few seconds. Heating and cooling rates typically range from 30-300 ^{o}C/second, and peak times range from a few seconds to several minutes. These fast ramps and short durations give RTP several advantages over standard furnace processing, including short furnace cycles and minimal dopant redistribution.

RTP with graphite-strip sources, which are a form of infra-red radiation, generally require that the sample be placed in a vacuum. A shutter controls exposure to the black-body source, which heats the sample by optical absorption initially and by free carrier acceleration above 300 ^{o}C. This type of source presents a danger of contamination from the graphite heater itself.[31] Near-ultraviolet sources, such as our Heatpulse system, use high-intensity lamps to heat the sample. Exposure is controlled by the lamp current, and no vacuum system is necessary. Heating is primarily by band-to-band transitions in near-ultraviolet systems.

Rapid thermal processing has applications in post-implantation annealing, diffusion, silicide formation, glass reflow, gate nitridation and oxidation, alloying, dopant activation, polysilicon resistivity reduction, and interface state reduction.[32] Applications of rapid thermal annealing (RTA) to GaAs processing have been especially notable[33, 34] due to the

following advantages of RTA over furnace processing for GaAs devices:

(1) Higher electrical activation of implants.

(2) More complete lattice reparation of implantation damage.

(3) Less GaAs dissociation and the ability to do capless anneals.

RTA in this project must diffuse and activate the dopant, repair the implantation damage, and leave a smooth surface morphology for contact formation. Conventional furnace annealing does not provide acceptable activation or post-implantation crystal reparation for GaAs, and tends to leave a rough surface from dissociation. This topic is discussed in detail elsewhere.[31, 35] Pulsed laser annealing, an alternative approach that removes implantation damage well, unfortunately allows too much dopant distribution in the molten layer to form shallow contacts. Rapid thermal processing with tungsten-halogen lamps is a compromise between complete removal of implantation damage and negligible dopant profile broadening.[35]

The Heatpulse 210T annealing furnace[36] used in this project is a near-ultraviolet system. It includes 13 high-intensity tungsten-halogen lamps that are arranged in upper and lower banks (6 and 7 bulbs, respectively) and housed in water-cooled, reflective walls. A quartz annealing tube is positioned between the banks, and is hermetically sealed to the door with an o-ring. A flat piece of quartz attached to the door holds the wafer and allows sample loading into the isolated annealing chamber. The visible light from the continuous-wave lamps passes through the quartz annealing tube and wafer tray and is absorbed by the sample.

Each of the thirteen bulbs produces 1.5 kW lamps, and at 100% intensity the microcontroller limits the input power to 18 kW lamps. The high-intensity of the lamps heats the sample quickly to as high as 1200 ^{o}C for times limited to 300 seconds. The anneal profile can be controlled by either sample temperature or lamp intensity. For accurate

control and monitoring of the sample temperature, a thermocouple located inside the annealing chamber is connected via a feedback loop to the microcontroller. Since the Heatpulse 210T is a cold-wall system, where only the sample and the filaments reach an elevated temperature, the thermocouple must be attached to a test wafer. A distinct advantage of a cold-wall system is that no unwanted impurities on the furnace tube or sample tray will diffuse into the sample. This problem is one of the limitations of diffusion technology when conventional furnaces are used. Unfortunately, this arrangement gives inaccurate temperature measurements since the thermocouple in not attached to the test sample itself. An optical pyrometer is an improvement over the current method.

2.4. Contact Resistance

The decrease in the size of contact openings as semiconductor device sizes approach sub-micron geometries leads to an increase in the contact resistance encountered by a current flowing across the metal-semiconductor interface. High resistance between the source-drain contacts and the channel of GaAs FETs is especially debilitating to the high-frequency operation of these devices. The theoretical aspects of contact resistance, as well as the details of several measurement techniques, are reviewed elsewhere.[26] This section will briefly review that discussion and describe our own measurement techniques and the problems encountered therein.

2.4.1. Theory of Contact Resistance

Ohmic contacts are defined as metal-semiconductor contacts that have a negligible contact resistance relative to the bulk semiconductor resistance.[37] For conventional ohmic contacts with low semiconductor doping concentrations, the thermionic-emission current dominates current transport. Tunneling ohmic contacts result when the semiconductor doping is higher (above approximately $10^{19}cm^{-3}$),[38] and involve the quantum-mechanical tunneling of carriers through the potential barrier between the contact metal and the

heavily-doped semiconductor. In this field-emission regime the effective barrier height is greatly reduced by the tunneling process, and nearly linear I-V characteristics are therefore possible.

The quality of an ohmic contact can be characterized by its specific contact resistivity, ρ_C ($\Omega \cdot cm^2$), which is defined as the average resistance per unit area of the metal-semiconductor interface. The specific contact resistivity is related by Equation 4 to the area of the contact, A, and the contact resistance, R_C ($\Omega/\square$), where contact resistance is a non-precise term for a variety of resistances that affect current flow at the metal-semiconductor interface.

$$R_C = \frac{\rho_C}{A} \tag{4}$$

Theoretically, ρ_C can be determined in the field emission regime from physical parameters such as barrier height, doping, and the effective mass of electrons in the semiconductor. In practice, however, processing conditions, interfacial impurities, and surface states all effect the electrical properties of the contact. Frequently the actual contact resistance is substantially different from the theoretical value. Measurement of ρ_C is further complicated by effects such as current crowding, diffusion resistance, and contact geometry. Consequently, contact resistance is very difficult to deduce in an accurate and reproducible manner.

2.4.2. Measurement of Contact Resistance by the Transmission Line Method

Several methods are used for estimating contact resistivity from the measured contact resistance by using Equation 4. The transmission line model proposed by Shockley[39] and refined by Berger[40, 41] is the most common method of analyzing the electrical behavior of a planar contact. As shown in Figure 3, the transmission line model compares a planar metal-semiconductor contact with a transmission line section. The method compares the

resistance of the doped semiconductor layer to the incremental series resistance of the transmission line, r_s, the interfacial resistance to the incremental shunt resistance, r_i, and the contact metal resistance to the series resistance, r_m.

The TLM allows calculation of both the contact front resistance and the contact end resistance. The contact front resistance, R_F, is taken at the leading edge of the contact assuming zero i_2, and is given by

$$R_F = Z \coth(\alpha L) \tag{5}$$

where

$$Z = \frac{1}{w}(R_{SH}\,\rho_C)^{\frac{1}{2}} \tag{5.1}$$

and

$$\alpha = (\frac{R_{SH}}{\rho_C})^{1/2} \tag{5.2}$$

Z is the characteristic impedance, α is the attenuation constant, L is the contact length, w is the diffusion width, and R_{SH} is the sheet resistance of the channel. R_F includes the interfacial and bulk contributions to the contact resistance at the leading edge of the contact (x=0), and is therefore a measure of the contact resistance at the point of largest current density. Current density varies due to vertical current crowding, as pictured in Figure 4. The effect of current crowding is modeled by the coth(αL) term, which approaches 1 for large values of αL. For large values of L the contact resistance has a negligible dependence on the contact length.

The contact end resistance, R_E, can also be calculated from the transmission line model, and is the resistance at the back edge of the contact.

$$R_E = \frac{Z}{\sinh(\alpha L)} \tag{6}$$

The contact end resistance is a measure of the contact resistance at the point of smallest current density. Since the dependence on L is exponential for long contacts, an independent measurement of both Z and α is possible.

As in any analytical model, there are several key assumptions made in the transmission line model:

(1) The contact width equals the width of the doped area (w=W).

(2) The sheet resistance directly below the contacts equals the channel R_{SH}.

(3) The resistor channel is infinitely thin.

The first assumption relates to lateral current crowding, and has been addressed by Hall,[42] Ting et al,[43] and Finetti et al.[44] This assumption, which is frequently incorrect for standard contact geometries, is quite proper for the test structure used in this project. The second and third assumptions relate to the semiconductor layer directly beneath the contact, and has been addressed by Chang.[45] Since in an alloyed contact the resistance of the layer directly below the contact will not necessarily equal the sheet resistance of the channel, we must modify the transmission line model by defining the incremental sheet resistance of the alloyed layer as $r_{sc} \neq r_s$. Neglecting lateral current crowding, Equations 5 and 6 become:

$$R_F = Z' \coth(\alpha' L) \tag{7}$$

and

$$R_E = \frac{Z'}{\sinh(\alpha' L)} \tag{8}$$

where the primed variables now contain R_{sc} rather than R_{SH}. Combining equations 7 and 8 gives

$$\alpha' = \left(\frac{R_{sc}}{\rho_C}\right)^{1/2} = \frac{1}{d}\cosh^{-1}\left(\frac{R_F}{R_E}\right) \tag{9}$$

We can thus determine α' by measuring R_F and R_E. Substituting α' into Equation 7 and using the measured front resistance gives Z', which may then be used to determine the contact resistivity ρ_C and the sheet resistance in the alloyed region

$$\rho_C = \frac{Z' w}{\alpha'} \tag{10}$$

and

$$R_{sc} = \alpha' Z' w \tag{11}$$

This alteration to the original equation should not be necessary in our case since we are working with non-alloyed as opposed to alloyed contacts.

2.4.3. Test Structure for Contact Resistance Measurement

Figure 5 shows the pattern used in this project for making TLM measurements. Contact resistance measurements to GaAs are most frequently made using this structure.[4, 5, 8, 46] A long n+ channel is crossed every 20 μm's by metal fingers that are each 20 μm's wide. This structure, which does not require oxide isolation between the metal and the undoped semiconductor since the substrate is semi-insulating, also removes the need for contact-hole definition. The intersection of the metal and the n+ diffusion defines the contact areas. Fabrication details are discussed in section 3. The resistance of the structure is given by

$$R = \frac{R_{SH}}{W}\left(d + 2L_T \coth \frac{L}{L_T}\right) \tag{12}$$

where R_{SH} is the sheet resistance, d is the contact spacing, L and W are the length and width of the contacts, respectively, and L_T is defined as the transfer length.

By ignoring lateral current crowding effects we can define $R_F = R_C$. Consequently, a simple measure of the contact front resistance can be made by forcing current through the two end pads and measuring the resulting voltage between one end pad and each of the fingers in succession. The resulting plot of R_{total} vs. L should be a straight line of slope R_{SH}/W and y-intercept $2R_F$. This technique is discussed further in section 5.1.

The contact end resistance may be determined on the same test pattern. As illustrated in Figure 6, end resistance is measured as a ratio of voltage v_2 to current i_1. As mentioned elsewhere,[26] accurate determination of contact resistivity from the TLM measurements requires measurement of both R_F and R_E. If both values are not measured it is necessary to assume an approximate value for the sheet resistance of the diffused layer beneath the contact. The common assumption that this resistance, R_{sc}, is equal to that of the doped channel, R_{SH}, is frequently incorrect for alloyed contacts.

We have found in the course of this project that the test structure described above is not sufficient for measuring small specific contact resistivities; i.e., in the range of $10^{-6}\ \Omega \cdot cm^2$. The sheet resistance measured is an average of that under the contact pads and that of the diffused region. The error in determining L_T is also large for small contact resistivities, as L_T becomes less than 5 μm. At the very least, the contact pads should be spaced at unequal distances to allow a reasonable measure of ρ_C. With this test structure our measured values are only estimates, but do give approximations of the actual contact resistance.

2.5. Surface Films After Chemical Cleaning

Regardless of the care taken in cleaning bare GaAs, a residual surface layer is always present. This layer, a combination of native oxide and a post-etching film, can interfere with diffusion from the GeSe thin-film. Consequently, it is important to minimize the thickness of this layer even if it cannot be removed entirely.

The native oxide forms at the rate of approximately 2 Å/minute as the sample is left in atmosphere after initial cleaning and etching, and stabilizes at 30 Å to 40 Å. A quick HCl dip immediately before loading the wafer into the deposition chamber removes this oxide, and does not seem to degrade the resist used in the lift-off process. This dip is not needed if the sample is loaded soon after the initial degrease and etch. If photoresist is used to pattern the diffusion source, a quick NH_4OH dip removes the carbon film left behind by the resist.[47] Since NH_4OH also removes the native oxide, this procedure can replace the HCl dip when a lift-off process is used.

The surface film left by the initial etchant is a more serious problem. Our substrate cleaning procedure is designed to etch away approximately 5 microns of the substrate to remove polish damage. The etching solutions that we used are based on sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). These types of etchants have been investigated by etching patterns with various etchant compositions.[48, 49, 50] The characteristics of the etching process depend on the concentration of H_2SO_4 and H_2O_2 in the etching solution. An etchant low in H_2SO_4 gives a flat-bottomed etch profile because the GaAs etching is surface-reaction limited. For this type of slow etchant, such as the second listed in Appendix A, the etching rate is regulated by the H_2O_2-GaAs reaction.[48] However, this process will leave a surface layer of at least 40 Å due to H_2O_2 diffusion effects. The surface layer, by forming a diffusion barrier between the etchant and the substrate, may be responsible for the flat profiles obtained. Unfortunately, it is also very difficult to remove. While native oxides are soluble in the etchant solutions and can be removed after etching by dipping in HCl, the surface layer is not reduced by more than 20% in either HCl or HF after a slow H_2O_2 etch. The origin of the surface layer is not well understood, but it appears to form by a preferential reaction with the acidic part of the solution.

On the other hand, if the etchant is high in H_2SO_4 content, such as the first etchant in Appendix A, H_2O_2 diffusion is still present but the surface film does not seem to be as thick. It is possible that the surface layer is simply etched away faster in the stronger

solution, or the GaAs could be oxidized by the H_2O_2 to form a native oxide which is then etched by the solution. The resulting etch profile is non-planar, however, because the faster etching reaction is diffusion-limited. This nonuniform profile is caused by surface diffusion of the etchant molecules that are absorbed by the protective mask.[49, 50]

Obviously, no etching solution is optimal for all uses. A weak H_2SO_4 solution leaves a surface layer while a stronger solution produces a nonuniform etch. The border between the two seems to be at approximately 33% H_2SO_4.[50]

We tested the surface film left by various cleaning procedures before choosing the first two recipes in Appendix A for our research. The surface film left by each etchant was measured on an ellipsometer using a HeNe laser (λ = 6328 Å). Details of this measurement technique are described by Runyan.[51] Briefly, the thickness (d) and/or refractive index (N_f) of an unknown thin film on a thick substrate of known absorption coefficient (K_s) and refractive index (N_s) can be determined by analyzing reflections of elliptically polarized light. The optical constants for the GaAs substrate are N_s = 3.85 and K_s = -.16, while the native oxide film has a refractive index N_f = 1.82. These constants for the GaAs-anodic oxide system have been determined by several methods.[52, 53, 54, 55] We used the values of Lyashenko, et al. because they were determined using a HeNe laser and would therefore seem to be most consistent with our equipment. Although we were never able to generate a layer-free surface according to our measurements, we instead took the smallest value obtained (approximately 20 Å) as evidence of the "best" cleaning procedure.

We chose to use the strong H_2SO_4 solution listed in Appendix A for the initial cleaning etch where the uniformity around edges was not relevant. We needed, however, a minimal surface layer after this step so that the GeSe diffusion would not be retarded. For the etch of alignment marks we used the etchant weaker in H_2SO_4 listed in Appendix A to give flat-bottomed profiles since we were not concerned with the surface layer.

3. EXPERIMENTAL PROCEDURE

Our first experiments were designed to characterize the heavily-doped layer formed by diffusion of the GeSe thin-film. The GeSe was deposited across the entire sample; therefore, masking lithography was not necessary for the initial process. Once we determined the optimal method for forming the n+ region, a more complex process was necessary to determine the quality of contacts to the doped region.

3.1. Initial Process for Diffusion Studies

The initial process is illustrated in Figure 7. Semi-insulating, undoped, LEC-grown GaAs wafers with a <100> orientation were used as substrates. Sample preparation began with a thorough degrease and an etch in H_2SO_4:H_2O_2:H_2O (5:1:1) for one minute at 65°C to remove polish damage. We tried several different cleaning procedures, as described in section 2.5 and Appendix A, and ultimately settled on the first listed there. We used an etchant solution high in H_2SO_4 content to minimize the thickness of the post-etching surface film,[56] which would interfere with subsequent diffusion of the GeSe thin-film. A dilute HCl dip performed immediately before loading the sample into the evaporation chamber removed native oxide that would further interfere with diffusion of the thin-film source.

A $Ge_{0.1}Se_{0.9}$ film 100 Å thick (nominal) was then deposited using an electron-beam evaporation system at a base pressure of approximately 6×10^{-7} Torr. After sputtered deposition of an SiO_2 encapsulating layer, the samples were implanted with 120 keV ^{29}Si and ^{75}As at doses ranging from 2×10^{14} cm^{-2} to 4×10^{15} cm^{-2}. The SiO_2 encapsulants were 1000 Å and 300 Å thick (nominal) for the silicon and arsenic implants, respectively. These thicknesses were chosen so that the nuclear stopping damage caused by the ion implantation would peak at GeSe/GaAs interface for each implanted species, thus causing maximum ion-beam mixing at the interface. This topic is discussed in more detail in section 2.2.

An additional 700 Å of SiO_2 was then sputtered onto the arsenic-implanted samples to give a 1000 Å encapsulant on all samples during annealing. A layer of SiO_2 thicker than 1000 Å can cause stress or peeling during RTA, while a thinner layer allows outdiffusion of arsenic. Encapsulation is necessary during annealing of GaAs samples to prevent dissociation unless an arsenic overpressure is used. Possible methods of encapsulation include deposition of SiO_2 or Si_3N_4 and proximity capping using a silicon or GaAs wafer. We initially attempted to sputter Si_3N_4, but were unsuccessful in obtaining a good film. Details of this procedure are in Appendix B.

The samples were annealed face down on a silicon substrate in an argon ambient using a high-intensity tungsten-halogen lamp. We found that a slow ramp (35 °C per second) is necessary to prevent surface degradation. The surface degradation is probably due to dissociation of the GaAs following evaporation of selenium through the encapsulant, as discussed in section 4.4. The SiO_2 encapsulant was removed using buffered HF before subsequent analysis once we had determined that there was no appreciable diffusion of GeSe into the encapsulant.

The resulting sheet resistivity, Hall mobility, and sheet carrier concentration were determined by a Van der Pauw technique. Indium dots were sintered to the samples for 1 minute at 450°C in forming gas to form ohmic contacts prior to measurements. Crystal damage was analyzed by examining channeling spectra for Rutherford backscattering (RBS) with 2.275 MeV $^{4+}$He ions at a detector angle of 102°. SIMS analysis determined the dopant profile before and after annealing.

3.2. Test Chip for Ohmic Contact Analysis

The second process is pictured in Figure 8. This four-mask process strives to determine the practicality of using GeSe diffusion for forming devices. The emphasis of the process is to measure contact resistance. The techniques described above were duplicated with the addition of steps necessary to define the contact patterns.

Layout of the test vehicle was done on the Berkeley graphics editor, KIC. The output from KIC was used to generate a tape that served as the input for a GCA Mann optical pattern generator. The masks were 4-times enlargements printed on 2.5 inch emulsion plates and were used with a Canon 4-to-1 projection aligner. The process flow for fabricating the test devices is as follows:

(1) Clean and etch wafer using recipe 1 in Appendix A.

(2) Mask I, alignment marks.

(3) Etch alignment using recipe 2 in Appendix A.

(4) Remove resist in acetone

(5) Mask II, diffusion stripes.

(6) Quick dip in HCl to remove native oxide.

(7) GeSe evaporation.

(8) Acetone lift-off.

(9) Sputtered SiO_2 encapsulation.

(10) Scribe 2" wafer into 9 die.

(11) Rapid thermal anneal.

(12) Remove oxide in buffered HF.

(13) Mask III, contact metal.

(14) Quick dip in NH_4OH to remove oxide and resist scum.

(15) Metal deposition.

(16) Acetone lift-off.

(17) Contact sinter.

Using the same wafers and cleaning procedures as described in section 3.1, we began the process by etching alignment marks in the bare GaAs wafer. Shipley 1400-31 photoresist was spun on at 6000 rpm for 30 seconds, baked at 90°C for 15 minutes, exposed on the

Canon at 5.6 intensity, and developed in 1:1 developer:water. The GaAs was then etched with a 4°C 1:8:8 solution as described in reference 2 of Appendix A. This step was later found to be unnecessary since the GeSe diffusion can be seen following RTA. We made the alignment marks in case the shallow diffusion was not visible, which would make it impossible to align the contact mask.

We then used lift-off to deposit the GeSe diffusion stripes. Patterning followed the same cleaning procedure used above. The lithography recipe again began with a 30 second, 6000 rpm spin of Shipley 1400-31 resist. Shipley 1350J was not used as previously because it is no longer manufactured: 1450J replaces it with the inclusion of a leveling agent, and 1400-31 is the same resist with tighter parameter control. The resist was soft-baked at 70°C for 20 minutes followed by a 10 minute immersion in chlorobenzene. The chlorobenzene hardens the top of the resist causing it to develop more slowly than the bottom portions. The resulting trench profile ensures that GeSe will not deposit on the vertical resist walls and make lift-off unsuccessful. Following the chlorobenzene immersion the wafers were baked at 70°C for 10 more minutes to drive off solvents. The resist was then underexposed (4.8 intensity) and overdeveloped (70 seconds in undiluted Microposit developer). A dilute NH_4OH dip performed immediately before loading the sample into the evaporation chamber removed native oxide and photoresist residue[47] that would interfere with diffusion of the thin-film source, as discussed in section 2.5.

GeSe was evaporated in the bell-jar, and the wafers were immersed in acetone and placed in an ultrasonic cleaner to dissolve the resist. Dimensions of the GeSe patterns were measured on the Vickers image shearing microscope, and showed the diffusion stripes were within 1 μm of the 100 μm, 200 μm, and 400 μm width intended. Following encapsulation with sputtered SiO_2, the samples were annealed at 1050°C for 20 seconds in the RTA furnace.

After scribing the wafer into 1 cm die and removing the SiO_2 encapsulant in buffered HF, we patterned the metal contacts using the same lift-off technique. Gold and Au-Ge

were evaporated from a tungsten boat in the Veeco 401 evaporation system at a base pressure of 2×10^{-7} Torr. Approximately 1500 Å to 2000 Å was deposited. We used a shutter for some of the samples to keep the temperature low during evaporation, but even without this precaution lift-off proceeded easily. Aluminum was evaporated from a base pressure of 1×10^{-5} using a tungsten filament. Both of these procedures required less than a minute of deposition. Tungsten was sputtered at 100 W for 30 minutes, giving a 2300 Å layer. Lift-off required a long ultrasonic treatment, as the substrate temperature during sputtering apparently baked the photoresist. Post-metallization sintering was performed in both the RTA furnace and a small sintering chamber. The temperature ramp was approximately $5^{o}C$ per second in both systems, but forming gas purged the sintering furnace while argon purged the RTA furnace. We concentrated most of the work in the simpler RTA furnace, but both it and the graphite strip in the sintering chamber gave identical results. The resulting specific contact resistivity and sheet resistance were measured using the test structure discussed in section 2.4.3.

4. DIFFUSION STUDIES

The formation of a heavily-doped n+ region occurs by diffusion of the GeSe source film during a 20 second RTA cycle, except where indicated. To determine the effects of ion-beam mixing on this diffusion, we use an experimental matrix consisting of five series of samples. Within each series the annealing temperatures range from 500°C to 1100°C. We implant both silicon and arsenic ions at two different doses, while the fifth series is prepared without ion-beam mixing. The electrical properties of the diffused region are monitored by a conventional van der Pauw technique, and the chemical profiles are provided by secondary ion mass spectroscopy (SIMS) and Rutherford backscattering spectroscopy (RBS).

4.1. Doping Threshold for Samples without Ion-Beam Mixing

Figure 9 shows the dependence of free-carrier concentration and average Hall mobility on the annealing temperature for the series of samples prepared without ion-beam mixing. A threshold occurs at approximately 950°C, above which the samples have measurably high carrier concentrations and mobilities. Below the threshold the samples have high sheet resistivity, but above the threshold there is a sudden and substantial lowering of the resistivity, R_{SH}. Above the threshold the carrier concentration increases slightly and the sheet resistivity decreases as the diffusion profile broadens and more dopant atoms are present in the n+ layer. This change in the electrical characteristics is minimal, however, indicating that diffusion to greater depths is not necessary for a low-resistivity layer. In contrast to the increase in the free-carrier concentration, the mobility decreases beyond the threshold. This decrease is probably due to increased Coulombic scattering from substitutional impurities on the gallium and arsenic lattices. Because of the compensation effect in GaAs of amphoteric dopants such as germanium, the increase in impurity concentration, and hence in scattering, is greater than the change in the net free-carrier concentration, N_S,[23] as discussed in section 2.1.2.

The threshold at 950°C is apparently related to diffusion of the GeSe thin-film rather than activation of the impurities. The SIMS data in Figure 10 shows that significant diffusion occurs during annealing above the threshold. Further evidence that the threshold is related to diffusion and not temperature is that samples annealed for 30 minutes at 850°C. as discussed in section 4.3. show profiles and electrical measurements similar to samples annealed in the RTA system at approximately 1000°C.

4.2. Effects of Ion-Beam Mixing

To determine the effects of ion-beam mixing. we first compared the samples processed without implantation to samples mixed with arsenic ions at doses of 2×10^{15} cm^{-2} and 4×10^{15} cm^{-2}. Electrical measurements show only small differences in the resulting layers. as illustrated in Figures 11-13. The sheet resistance curves in Figure 13 are identical for the two arsenic doses and similar for the unimplanted samples.

While the unimplanted samples have a threshold between 950°C and 1000°C. the samples mixed by arsenic implantation have a threshold about 50°C lower. Again the threshold is diffusion-limited. as illustrated in Figure 14. Little change from the profile created by ion-beam mixing is noticeable after a 900°C RTA; however. after an 1100°C RTA there is significant diffusion of germanium and selenium from the thin-film source. The small difference in threshold could be due to the dispersion of interfacial contaminants by ion-beam mixing. It is also possible that the implantation causes enough atomic mixing to form an interfacial quaternary Ga-As-Ge-Se layer. but the SIMS resolution is not sufficient to confirm this hypothesis. Either effect would allow the diffusion of a significant concentration of impurities at a lower anneal temperature.

We also compared mixing with silicon ions. which. in addition to providing ion-beam mixing. should also serve as a dopant in GaAs. While silicon. like germanium. is amphoteric in GaAs. it tends to act as an n-type impurity. This tendency should be heightened by the presence of selenium on the arsenic lattice. The silicon doses were

2×10^{14} cm^{-2} and 1×10^{15} cm^{-2}. Mixing by high-dose silicon implantation alters the electrical characteristics significantly, as shown in Figures 11-13. While the curves have a shape similar to those for arsenic mixing and no mixing, the threshold temperature has been reduced by 200°C and the electrical characteristics have been improved significantly for the higher-dose samples.

The threshold temperature is lower because the formation of an n+ layer is no longer limited by the supply of germanium and selenium atoms. Instead, ion-beam mixing supplies enough silicon donors to form a low-resistivity layer, as pictured in Figure 15. Lowered sheet resistivities are observed as soon as the implanted silicon is electrically activated. This activation occurs at approximately 700°C, in agreement with the results of other workers.[57, 58] The sharp increase in the free-carrier concentration shown in Figure 11 near 700°C confirms that this temperature is the activation threshold for implanted silicon. The continued increase in N_S above the 700°C threshold suggests that the free-carrier concentration at the threshold is limited by the solid solubility of the dopant species. At higher anneal temperatures the diffusion profile broadens and more carriers are activated, as discussed earlier. Similarly, the mobility in Figure 12 decreases beyond the activation threshold due to increased Coulombic scattering.

At the threshold, the silicon-implanted samples have a lower sheet resistivity, a higher free-carrier concentration, and a higher average mobility than the arsenic-implanted samples. These electrical characteristics are improved because the presence of silicon donors in addition to germanium and selenium creates a more heavily-doped layer. However, the depth of the implantation profile makes it difficult to form layers as shallow as those formed by diffusion of all dopant impurities.

While ion-beam mixing does not seem to improve source diffusion, it does successfully mix the interface and create defects. Figure 16 illustrates typical RBS channeling spectra for samples before and after annealing. Samples mixed with arsenic ions are presented because the higher dose creates more crystal damage, but the behavior is similar

for silicon implants at a lower order of magnitude. The high background yield for the implanted but unannealed sample shows that ion-beam mixing successfully causes crystal disorder. The spectra for annealed samples show that RTA restores the crystalline structure. The crystalline recovery is more effective at higher temperature. In Figure 17 we show the channeling minimum yield, χ_{min}, which is taken from 350 Å to 1400 Å below the surface. χ_{min} is the ratio of the channeling yield to the yield of the random orientation, and gives a measure of the crystal quality. Samples mixed with arsenic ions show 300% more damage before annealing than the samples mixed with silicon ions due to the larger dose and higher nuclear stopping power of arsenic. Samples implanted with each ion show similar restoration after annealing, and both closely approach the crystalline quality of the virgin GaAs.

Given that ion-beam mixing alters the interface and creates crystalline damage as intended, we propose a model to explain the ineffectiveness of ion-beam mixing by either arsenic or silicon implantation in aiding the diffusion of a thin-film dopant. We have shown that the diffusion of the GeSe thin-film is not significant until over 900°C during RTA, while the electrical activation of silicon occurs at 700°C. However, other workers have found that annealing of implanted damage occurs in two phases, one phase occurring near 250°C and the other occurring between 400°C and 500°C.[57, 59, 60, 61] Consequently, the defects created by ion-beam mixing are repaired before the thin-film impurities diffuse into the substrate. Ion-beam mixing thus aids the diffusion mechanism only moderately by dispersing interfacial contaminants and causing atomic mixing.

4.3. Effects of Rapid Thermal Annealing

The use of RTA as compared to furnace annealing, however, causes a more significant improvement in the formation of shallow n+ layers. We compared the RTA technique to conventional furnace processing by furnace-annealing some samples with a 7000 Å SiO_2 encapsulant. These samples were mixed with silicon or arsenic ions at doses of

1×10^{15} cm^{-2} and capped with 2000 Å of sputtered SiO_2 and then 5000 Å of CVD SiO_2. Samples furnace-annealed at 850°C for 30 minutes display similar electrical characteristics to samples processed with an RTA cycle of 1000°C for 20 seconds. SIMS analysis of the furnace-annealed samples show selenium profiles between those of the 900°C and 1100°C RTA samples. This result is expected based on the diffusivity of the dopants in GaAs as shown in Table 1. Whether we use our own calculated values of D_0 and Q or those reported elsewhere,[62] the diffusion model given in section 4.5 indicates that this furnace anneal should produce the same diffusion profile as a 20 second RTA at between 1000°C and 1050°C. The confirmation of this prediction suggests that the simple diffusion equation is accurate for our RTA experiments. In many instances, imperfect temperature control during the ramps and at the start of the plateau can cause deviations from this approximation for RTA. Our temperature control is precise enough, however, that we were not forced to calculate an effective diffusion time to overcome these errors.[63] Since the furnace samples were annealed at only 850°C, the threshold noted above at 950°C for the RTA samples is apparently related to diffusion rather than activation of the dopants.

While the electrical characteristics are similar, furnace annealing results in significantly more crystalline disorder and surface degradation than RTA. The χ_{min} curve shows that the crystalline disorder caused by ion-beam mixing is not repaired as fully by furnace annealing as by RTA. The silicon-implanted sample retains twice as much disorder after furnace annealing than after RTA, and the arsenic-implanted sample exhibits slightly more disorder even though the arsenic dose is less than for the sample processed with RTA. Since the quality of the GaAs crystal is paramount to the quality of any device formed on it, this ability to repair the damaged GaAs crystal is a significant advantage for RTA in any GaAs process that involves ion implantation. The reduction of surface degradation by RTA is discussed in the following section.

4.4. Encapsulant Failure

The SIMS profiles in Figure 10 indicate that the selenium peak occurs 750 Å below the surface of the sample after an 1100 °C RTA for samples that have been processed without ion-beam mixing. Normally, a thin-film source thicker than a few monolayers will result in an impurity profile that peaks at the surface after diffusion. The depth of the peak suggests that the supply of selenium is depleted by the end of the annealing cycle. We suspect that this depletion results from selenium's high vapor pressure, which reaches one atmosphere well below the annealing temperatures used in this study.[64] At 1100°C the selenium apparently vaporizes through the encapsulant.

Selenium evaporation is further suggested by the surface of the annealed samples. While the low-temperature RTA samples exhibit a smooth surface, the surface of the encapsulant on the 1100 °C RTA samples shows signs of blistering. Furthermore, the furnace-annealed samples show significant blistering of the encapsulant even though we used a substantially thicker SiO_2 encapsulant. The blistering occurs only over areas covered by the GeSe film, indicating that the evaporation of the thin-film is causing the encapsulant failure. As the encapsulant fails the GaAs begins to dissociate. The resulting degradation of the sample surface can be seen once the encapsulant is removed, as shown in Figure 18. The use of RTA cycles below 1100°C controls the selenium evaporation and successfully eliminates degradation of the GaAs surface. This high-temperature RTA limit combined with the threshold noted earlier infers that optimal 20-second RTA occurs between 950°C and 1100°C. In this region the RTA samples demonstrate the same electrical and chemical properties as furnace-annealed samples, but show a smoother surface morphology because the encapsulant integrity is maintained.

Another result of the encapsulant failure is the presence of silicon in the GaAs crystal, as shown in Figure 19. The silicon is diffusing from the SiO_2 encapsulant during annealing. As the encapsulant begins to fail at 1100 °C, a substantial amount of silicon enters the sample. This silicon concentration could be contributing to the measured

electrical characteristics; however, the silicon profile is at both a shallower depth and a lower concentration than either the germanium or selenium, and its contribution to the impurity profile can probably be neglected. Nevertheless, our sputtered SiO_2 layer apparently does not provide sufficient encapsulation for high-temperature or long-time annealing cycles.

4.5. Diffusivities of Impurities

Table 1 presents the diffusivities of germanium and selenium in GaAs for our experimental conditions. Diffusivity calculations were made at the tail of the diffusion for the 900°C and 1100°C RTA profiles shown in Figure 10. We assumed Gaussian diffusion due to the Gaussian-like shape of the SIMS profiles. A simple diffusion model allows calculation of the diffusivity by

$$C(x,t) = C_S \exp\left(\frac{-x^2}{4Dt}\right) \tag{13}$$

where C is the concentration as a function of depth (x) and time (t), C_S is the surface concentration, and D is the diffusivity at the appropriate temperature. The calculated values of D are used to find D_0 and the activation energy, Q, by extrapolation. These latter values do not agree with those published elsewhere[62] for single-element diffusion studies on selenium. Our results show a lower activation energy than earlier reported, which may be due to the use of rapid thermal annealing techniques in this project. Germanium demonstrates a greater activation energy than selenium, and diffuses to a greater depth in our samples, but still has a small diffusivity in GaAs at the annealing temperatures used. The slow diffusion of germanium and selenium in our system makes these impurities well-suited to forming shallow junctions.

5. OHMIC CONTACT FORMATION

These heavily-doped n+ layers were then applied to non-alloyed ohmic contact formation. Contact resistivity was measured from a standard transmission line structure,[65] illustrated in Figure 5, on samples that were subjected to diffusion at 1050°C. Various metals were deposited using the same lift-off procedure as described earlier for the GeSe thin-film. Primary consideration focused on samples made with gold layers approximately 1500 Å thick. The gold was evaporated at a base pressure of 2×10^{-7} Torr, and the sample temperature was minimized during evaporation to prevent self-alloying and to facilitate lift-off.

5.1. Measurement Technique

Specific contact resistivity was measured using the extrapolation method[40] between 20 μm spaced, 200 μm wide pads. This method provides plots of resistance vs. contact spacing, as shown in Figure 20. The overall resistance of the structure is given by

$$R = \frac{R_{SH}}{W}\left(d + 2L_T \coth \frac{L}{L_T}\right) \qquad (14)$$

where R_{SH} is the sheet resistance, d and L are the contact spacing and length, respectively, W is the width of the diffusion, and L_T is defined as the transfer length. The sheet resistance is equal to the slope of the linear plot in Figure 20 multiplied by the contact width, W. The X-intercept in Figure 20 equals $2L_T$, since in our case $L \gg L_T$. The specific contact resistivity, ρ_C, is then calculated by

$$\rho_C = R_{SH} L_T^2 \qquad (15)$$

5.2. Results

Low-temperature sintering was necessary to produce ohmic contacts. Figure 21 presents the relationship between the sintering temperature and the contact resistivity for gold contacts. The samples were sintered in an argon ambient using the same RTA furnace as earlier. The ramp-rate was reduced to $5^{o}C$ per second and the peak temperature was held for 2 minutes. Temperature was again monitored using the chrome-alumel thermocouple included with the RTA system.[36] The pattern of the results is similar to that found by Werthen[66] for Au-Ge contacts to n-type GaAs, and is presumably due to the penetration of a thin impurity layer at the metal-semiconductor interface.

The gold contacts in Figure 20 display a specific contact resistivity of $2.2 \times 10^{-4}\ \Omega \cdot cm^2$ with a sheet resistance of 55 $\Omega/\square$. Samples made with Au-Ge contacts exhibit similar characteristics, while aluminum and tungsten contacts display higher contact resistivities, as shown in Table 2. These contacts are both reproducible and ohmic over several decades of current, but the contact resistivity is higher than we anticipated. Given the low sheet resistance of the samples, one explanation for the large contact resistance is that the GeSe forms an interfacial layer. GeSe is a chalcogenide glass that crystallizes under $600^{o}C$ with a large bandgap (the $GeSe_2$ compound has a bandgap of 2.2 eV).[67] However, neither alloying the Au-Ge contacts at $450^{o}C$ nor etching the sample surface before metallization with a 1:1:60 H_2O:H_2SO_4:H_2O_2 solution as described in reference 3 of Appendix A significantly reduces the contact resistivity. Either technique should allow the contact to penetrate an interfacial layer. However, the germanium and selenium may be segregating to the contact interface after alloying to form a glassy layer, or the etching solution may not be removing enough of the semiconductor surface before metal deposition.

6. CONCLUSIONS

We have developed a new method for forming non-alloyed ohmic contacts to GaAs devices. We found that shallow, heavily-doped layers can be formed by diffusion from a GeSe thin-film. We determined that rapid thermal annealing (RTA) improves the diffusion of shallow n+ layers while ion-beam mixing has a moderate effect for the GeSe/GaAs system. Rapid thermal annealing (RTA) allows control of the diffusion profile and prevents degradation of the GaAs surface. Optimal 20-second RTA occurs above the diffusion threshold at 950°C but below 1100°C where the SiO_2 encapsulant begins to fail. A further study of different annealing times is being prepared.[68] RTA reduces surface and crystalline damage while producing the same electrical characteristics as furnace annealing. Ion-beam mixing is less significant because the damage created to enhance diffusion is repaired at a lower temperature (400°C) than is necessary for diffusion (900°C). Furthermore, simple diffusion equations can be used to calculate RTA cycles provided that the temperature profile is controlled precisely.

We are able to form reproducible, non-alloyed ohmic contacts to these n+ regions with a low-temperature sinter. The low sheet resistance (55 Ω/□) and high specific contact resistivity (2.2×10^{-4} $\Omega \cdot cm^2$) suggest that an impurity layer is present at the contact interface. For this contact technique to be useful, this impurity layer must be removed from the surface. Any further work using the GeSe film to form non-alloyed ohmic contacts to GaAs devices must first overcome this remaining problem.

APPENDIX A: GaAs Cleaning Procedures

We experimented with various GaAs cleaning procedures developed by different people for their own particular application. Our procedure is an amalgamation that we found to be most effective. The process begins by thoroughly degreasing the wafer. We then used the first etch to remove polish damage during the initial wafer preparation, and the second etch to etch alignment marks in the GaAs substrate before diffusion. The third etching solution was used prior to evaporation to etch slightly and leave a surface free of native oxide and photoresist deposits. This subject is discussed in more detail in section 2.5.

1. Reference: Nick Kepler, 373 Cory, 642-1010.

Degrease:

1. Rinse in TCA, and then leave in boiling TCA for 5 minutes.
2. Rinse twice in acetone, then leave in boiling acetone for 5 minutes.
3. Rinse twice in methanol, then leave in boiling methanol for 1 minute.
4. Rinse thoroughly in DI H_2O.
5. Blow dry with N_2.

Etch:

1. Mix 5:1:1 H_2SO_4:H_2O_2:H_2O and let cool to 65 ^oC +/- 3 ^oC. Add H_2O_2 to water and H_2SO_4 last in case of splashes.
2. Etch at approximately 5 microns per minute. Stir mixture in uniform, reproducible pattern.
3. Rinse in DI H_2O by diluting acid mixture for several minutes until runoff is pure water. By not exposing the wafer to air until rinse is complete, you prevent formation of As oxide, which forms in the presence of water vapor.
4. Immediately blow dry with N_2.
5. If wafer is left for more than 1 hour before use, remove surface oxide with pure HCl for 1 minute. Blow dry after (optional) DI H_2O rinse.

Comments

We used this procedure for the initial cleaning of our sample wafers Our choice was based on the simplicity of the procedure, the uniformity of the surface, the lack of etch pits, and the minimal surface film.

2. Reference: Berkeley MBE Group, 173 Cory, 642-8136.

Degrease:

1. Rinse in TCA, and then leave in boiling TCA for 5 minutes.
2. Rinse twice in acetone, then leave in boiling acetone for 5 minutes.
3. Rinse twice in methanol, then leave in boiling methanol for 5 minutes.
4. Rinse thoroughly in DI H_2O.
5. Blow dry with N_2.

Etch:

1. Mix 1:8:8 H_2SO_4:H_2O_2:H_2O and cool for 30 minutes in ice bath to 4^oC.
2. Etch at 1.5 micron per minute.
3. Rinse in DI H_2O.
4. Remove surface oxide with 1:1 HCl:H_2O for 2 minutes.

Comments:

We used this procedure for etching alignment marks on our sample wafers. Our choice was based on the slow (and therefore controllable) etch rate and the flat-bottomed profile for small etch patterns.

3. Reference: T. H. Miers, JECS, vol. 129, p. 1795, August, 1982.

Contact preparation:

1. After developing lift-off resist, clean 5 seconds in 10:1 H_2O:NH_4OH to remove carbon scum from resist.
2. Etch 15 seconds in 60:1:1 H_2O:H_2SO_4:H_2O_2 to remove about 300 Å of GaAs surface.
3. Clean 5 seconds in 10:1 H_2O:H_2SO_4 to remove carbon scum from resist and oxide.

Comments:

We used this technique to give a clean GaAs surface for ohmic contact formation. Photoresist can leave a carbon film, which the ammonium hydroxide removes (along with any native oxide), while the sulfuric acid etch removes the top layer of the semiconductor, which we believe is a Ge-Se-Ga-As alloy of some sort.

APPENDIX B: Sputtering of Silicon Nitride Onto GeSe

Sputtering of Si_3N_4 is perhaps the best method of encapsulating GaAs samples prior to annealing. While some workers have found problems with bubbling and loss of adhesion during annealing,[69] generally Si_3N_4 is a superior encapsulant to SiO_2 because it does not allow as much diffusion of gallium and arsenic out of the substrate.[70] The initial parameters we used for sputtering originated in a paper by Mogab, et. al.,[71] and were calculated for the Randex system at U. C. Berkeley by Dr. David Haas. The optimum power is 350 W and the partial pressures are 3 mT of nitrogen and 3 mT of argon. 15 mT of argon is necessary to start the plasma. Our initial sputtering run left an extremely poor surface, and we did several more tests at lower power. In each run we sputtered onto a GaAs substrate with a GeSe film covering most of the surface. We also sputtered onto GeSe on glass and onto a silicon substrate during some of these tests.

The Si_3N_4 apparently bubbles on the surface of the sample, as previously reported by Harris, et. al.[69] However, this bubbling is far more evident on top of a GeSe film than above plain GaAs, silicon, or a glass slide. Apparently a reaction occurs between the nitride and GeSe films. While the high vapor pressure of selenium could cause it to bubble through the nitride, the problem seems to require a more involved explanation since oxide films deposited at the same power (and presumably, therefore, the same temperature) do not show such bubbling.

The nitride sputtering works best at low power, although pinholes exist even at 60 W. The possibility that the improvement at low power is due at least partially to thinner films (600 Å instead of 1000 Å) should not be overlooked. However, we suspect instead that the lower temperature resulting from low-power sputtering reduces whatever reaction is taking place. It is also possible that sputter-cleaning the GaAs substrate before sputtering on the nitride would improve the adhesion, but this technique could also remove the

thin GeSe layer. More investigation is in order since some of the results are contradictory. Further studies should concentrate on films of different thicknesses deposited at low power. It would be especially interesting to try Donnelly's method of pyrolytic nitride deposition,[72] which was designed to avoid the loss of adhesion found by Harris, et al.

Table 1

Diffusion coefficients in GaAs for codiffusion of germanium and selenium during rapid thermal annealing. Values for selenium single-element diffusion (a) are also included.[62]

Impurity	Temperature (°C)	D (cm^2/ sec)	Q (eV)	D_0 (cm^2/ sec)
Ge	900	1.6×10^{-13}	2.16	2.9×10^{-4}
	1100	3.5×10^{-12}		
Se	900	2.5×10^{-13}	1.29	8.6×10^{-8}
	1100	1.6×10^{-12}		
Se (a)			4.16	3×10^{3}

Table 2

Specific contact resistance and sheet resistance for several contact metals. The contacts are made to heavily-doped, n-type regions in GaAs.

Contact Metal	Sintering Temperature (°C)	ρ_c ($\Omega \cdot cm^2$)	R_S ($\Omega/\square$)
Au	340	2×10^{-4}	55
Au-Ge	340	3×10^{-4}	65
Al	450	6×10^{-4}	90
W	450	11×10^{-4}	80

Figure 1

Comparison of electronic and nuclear stopping during ion implantation

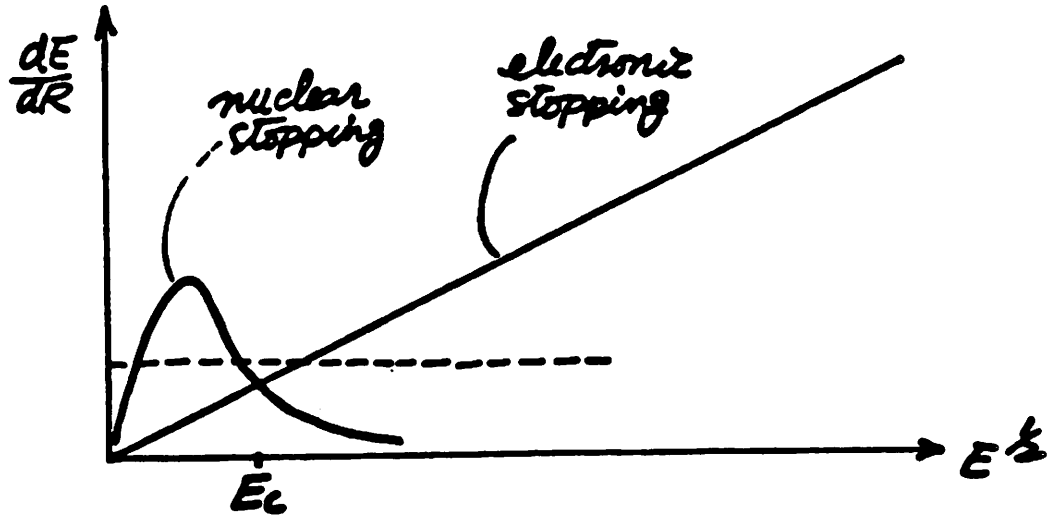


Figure 2

Comparison of range and damage profiles

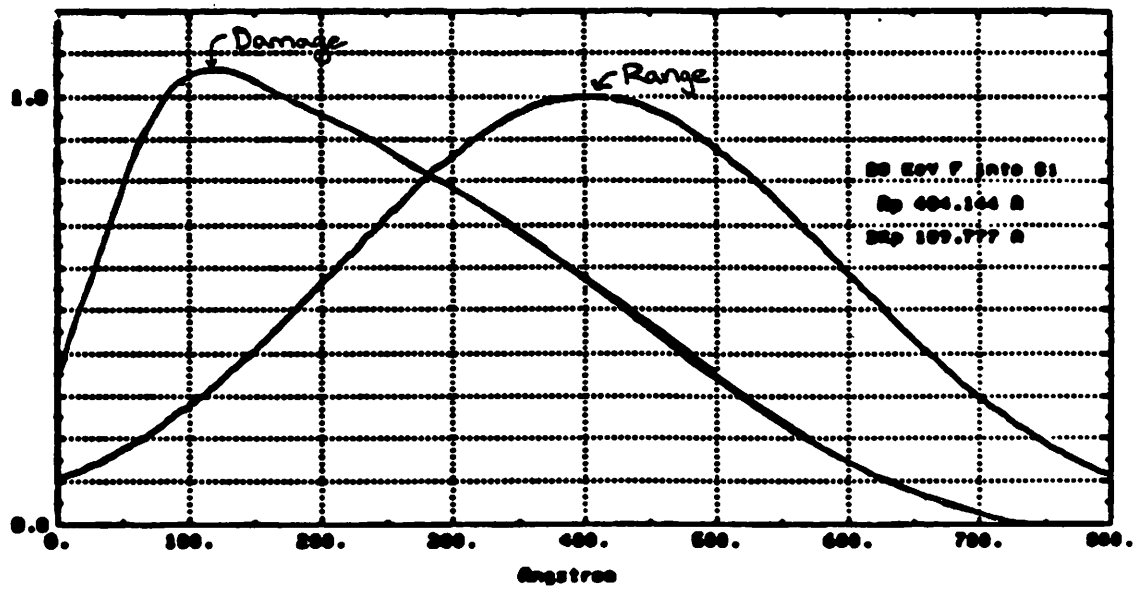


Figure 3

Schematic diagram of an ideal metal-semiconductor contact and the equivalent circuit diagram using the Transmission Line Model[26]

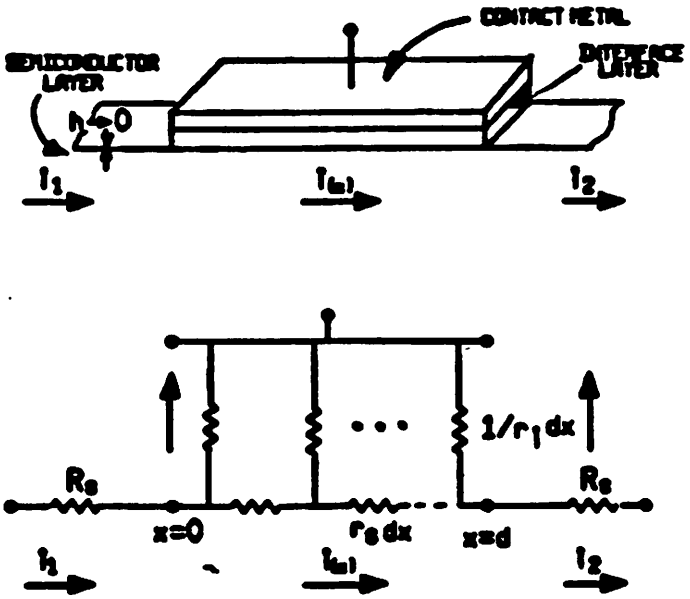


Figure 4

Cross-section of a planar resistor showing vertical current crowding[26]

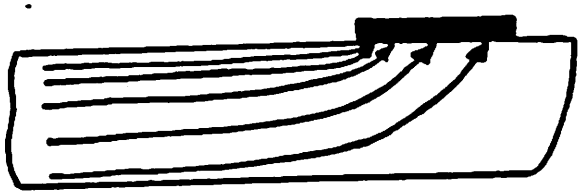


Figure 5

Test pattern used to measure contact resistivity

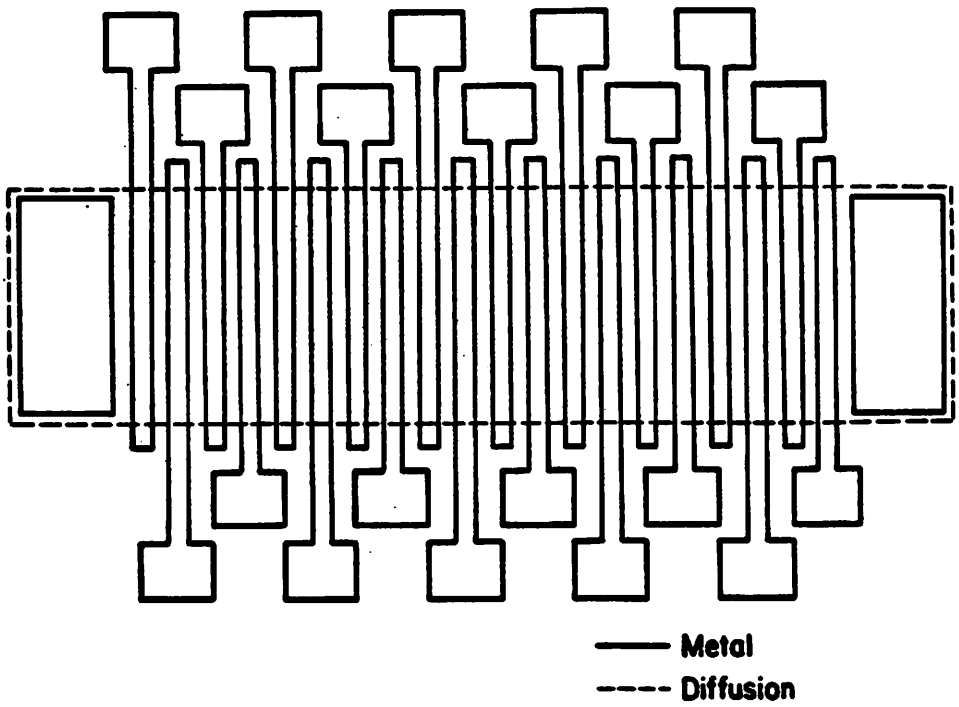


Figure 6

Measurement technique for determining contact end resistance, R_E, as a ratio of v_2 to i_1[26]

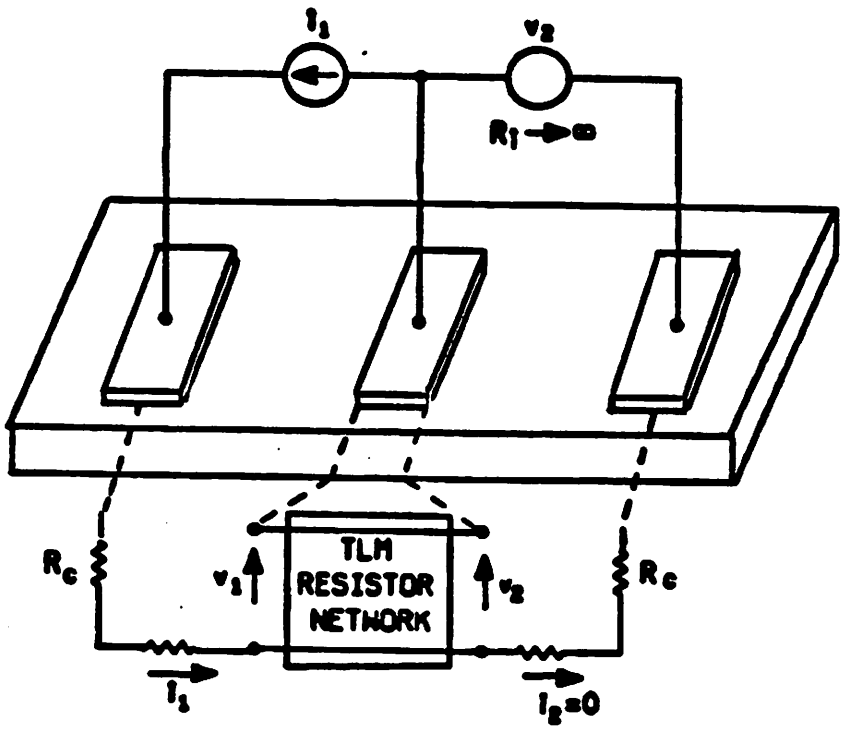


Figure 7

Schematic diagram showing the effects of ion-beam mixing and rapid thermal annealing on the diffusion process

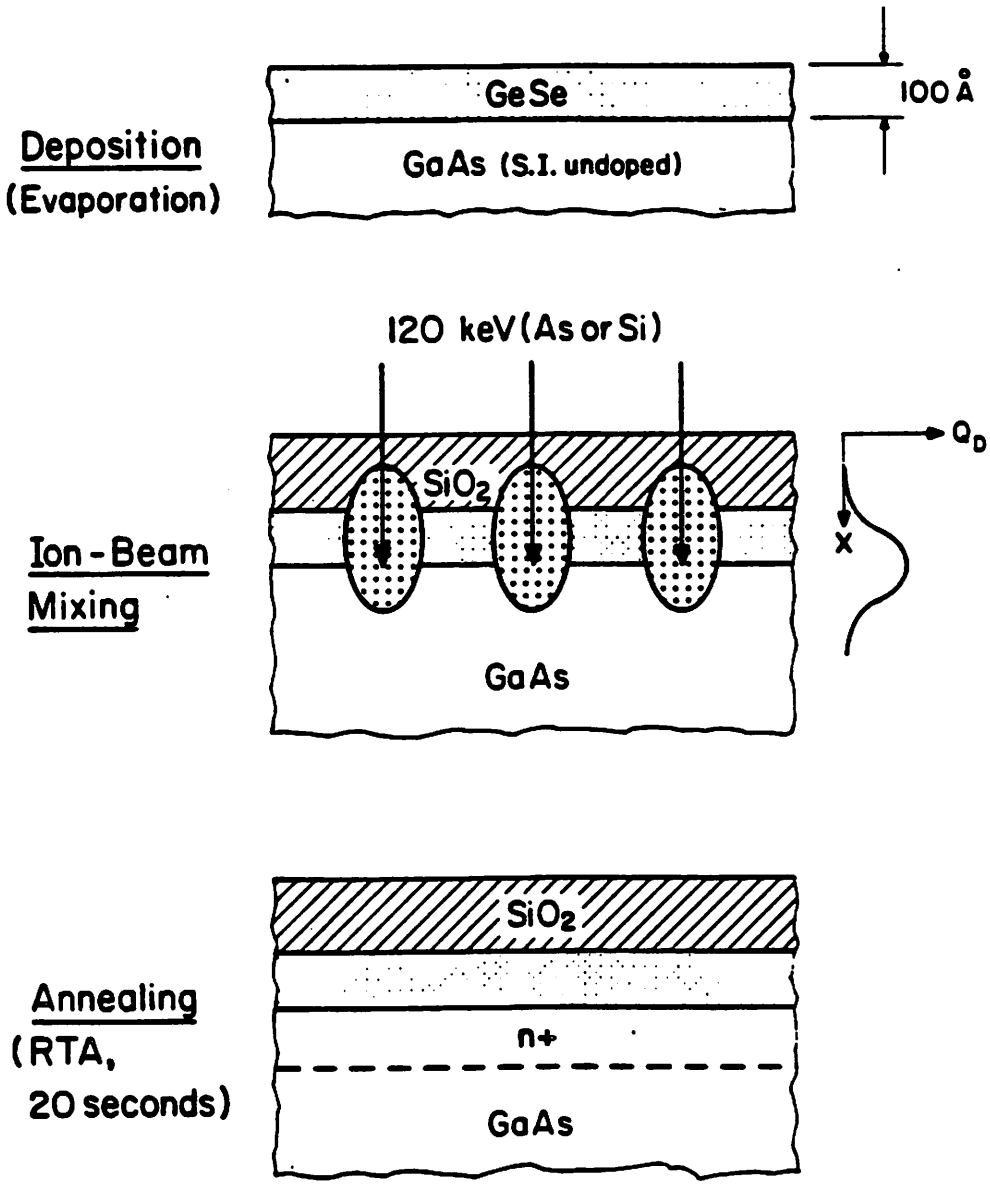


Figure 8

Schematic diagram showing the effects of rapid thermal annealing on diffusion. Contact metallization uses a conventional lift-off technique

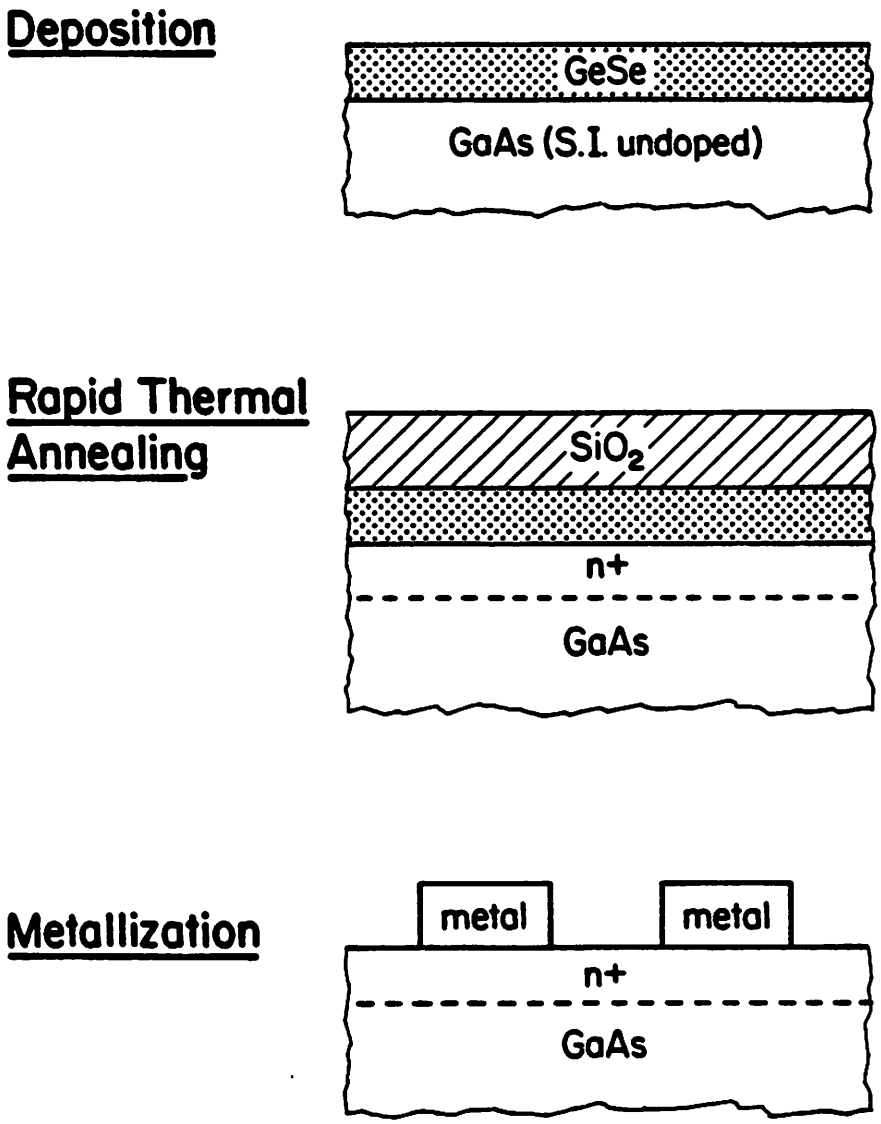


Figure 9

Dependence of the free-carrier concentration, N_S, and the average Hall mobility, μ_H, on the annealing temperature for samples prepared without ion-beam mixing

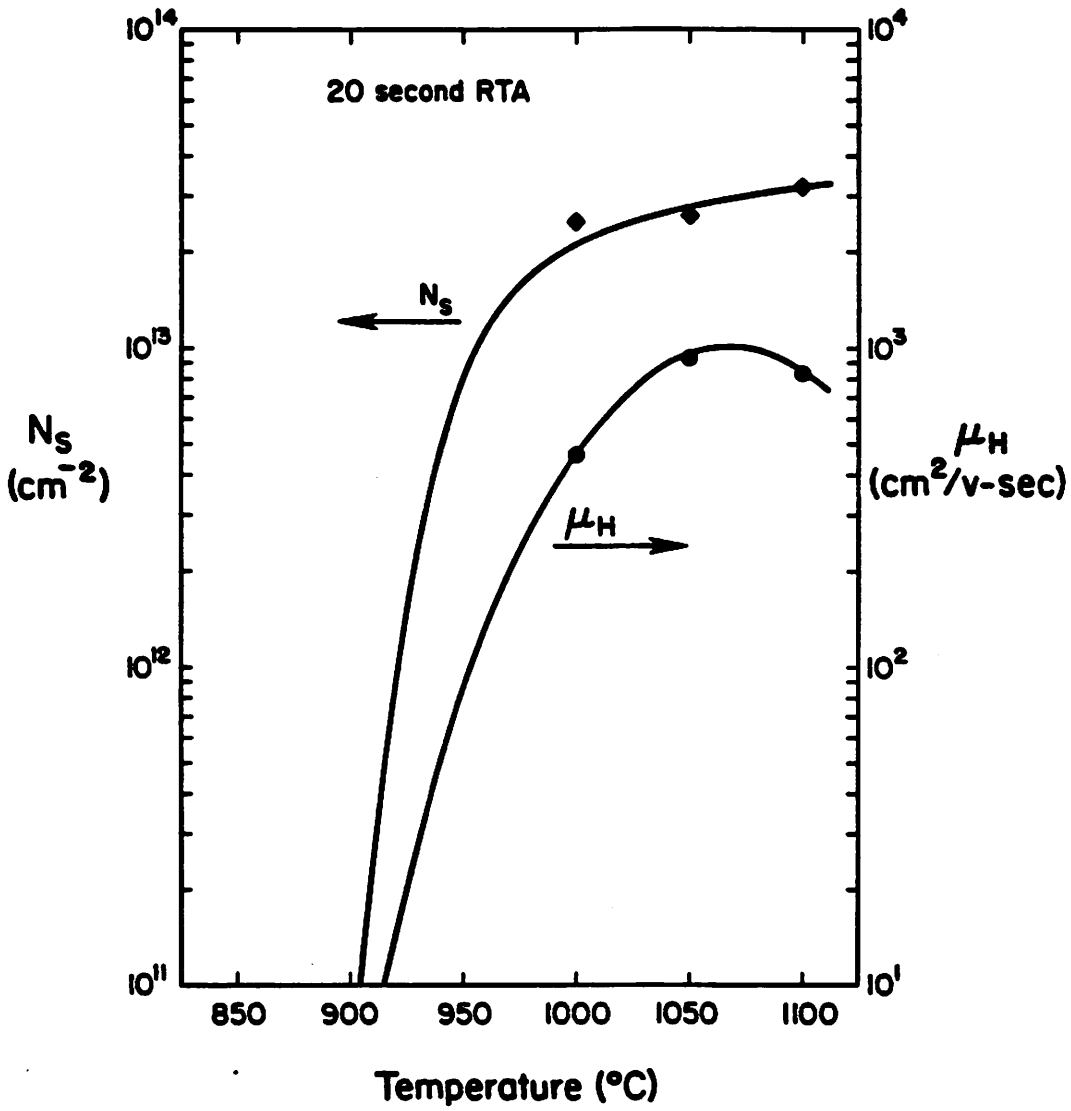


Figure 10

SIMS profiles of germanium and selenium diffusion in GaAs after a 20 second RTA without ion-beam mixing

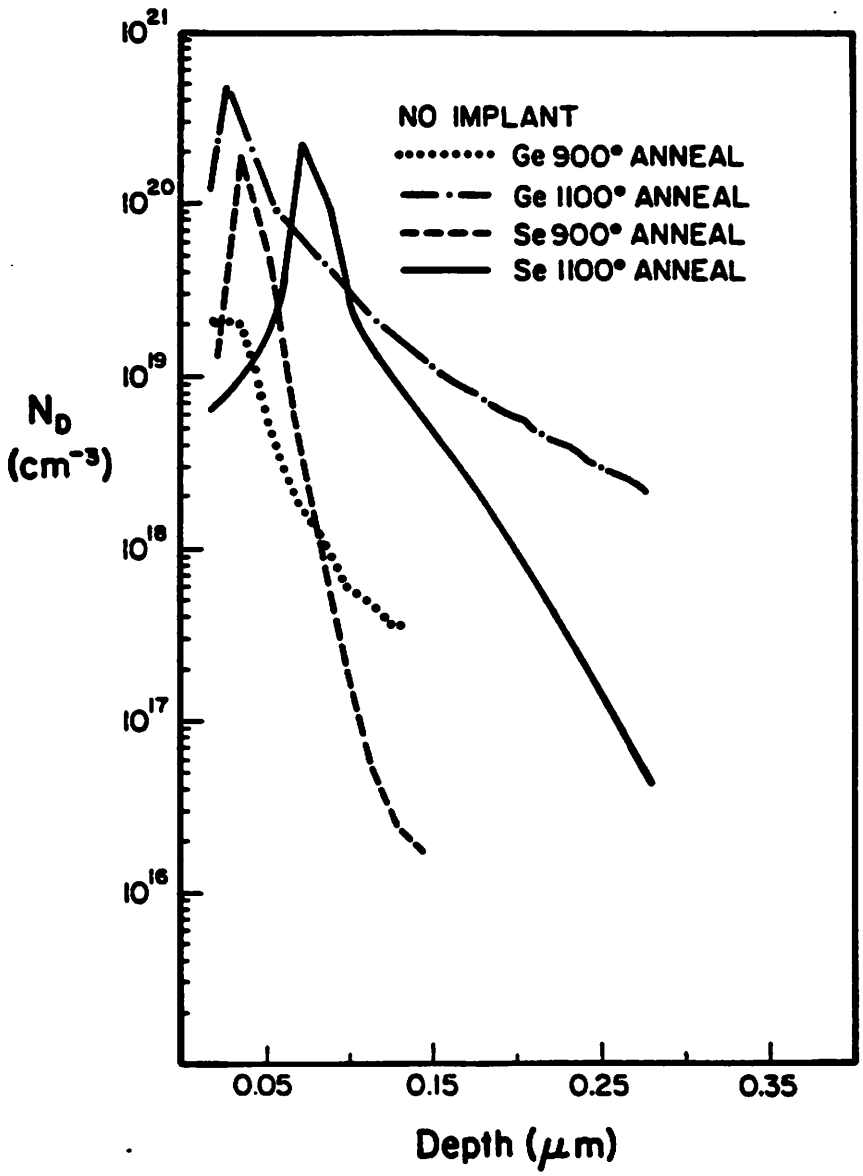


Figure 11

Dependence of the free-carrier concentration, N_S, on the annealing temperature for ion-beam mixing with silicon and arsenic ions

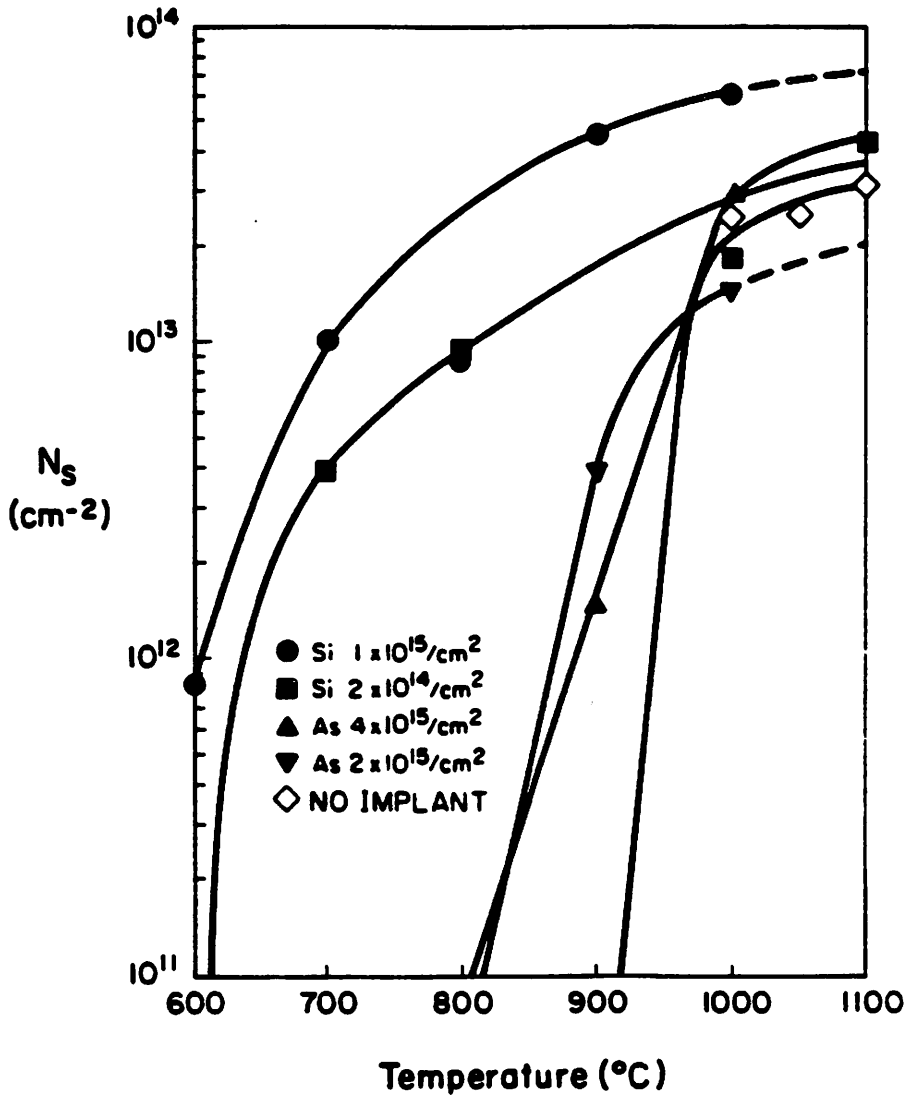


Figure 12

Dependence of the average Hall mobility, μ_H, on the annealing temperature for ion-beam mixing with silicon and arsenic ions

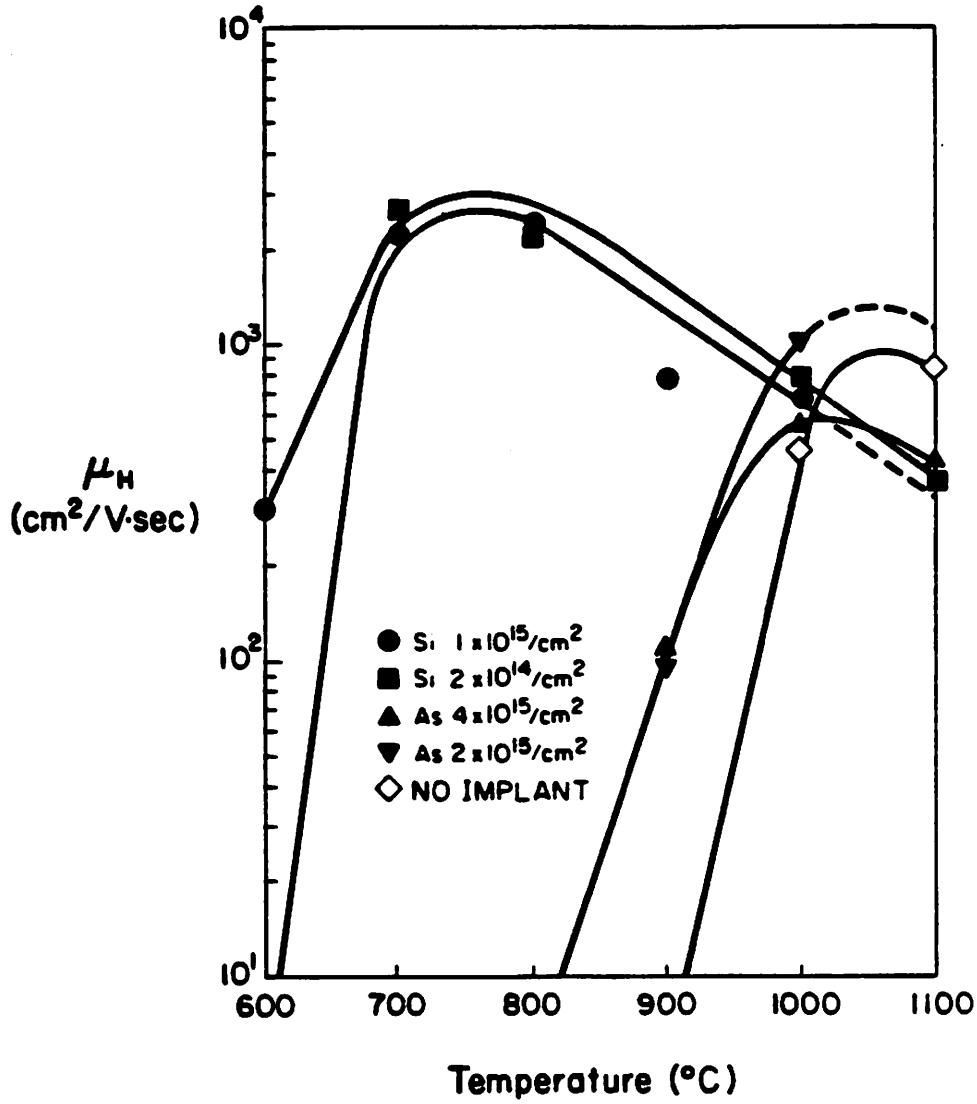


Figure 13

Dependence of the sheet resistance, R_{SH},
on the annealing temperature
for ion-beam mixing with silicon and arsenic ions

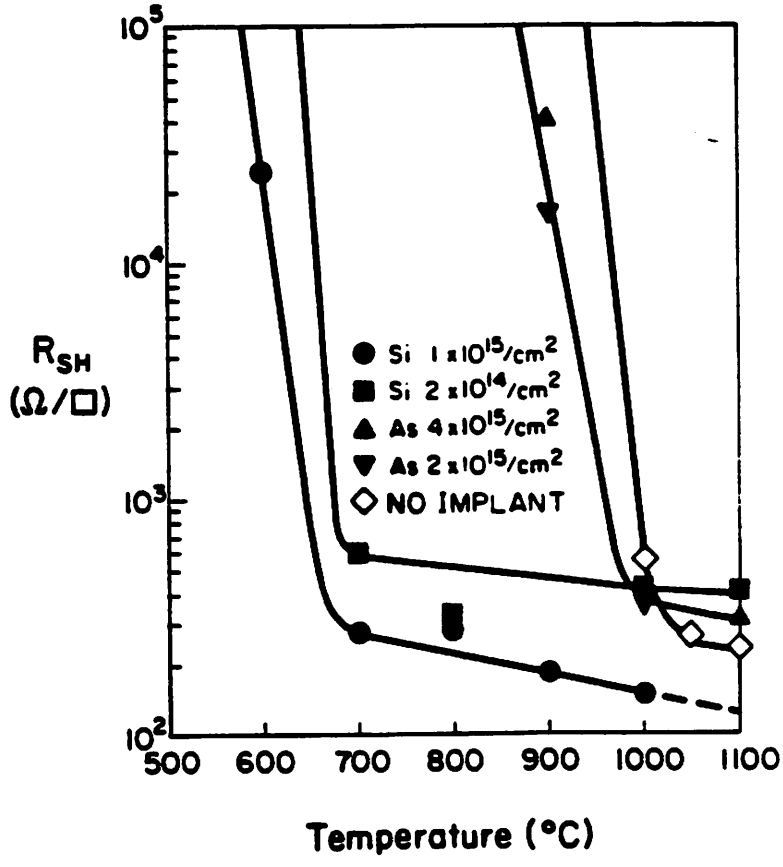


Figure 14

SIMS profiles of germanium and selenium diffusion in GaAs
after ion-beam mixing with silicon and arsenic and a 20 second RTA

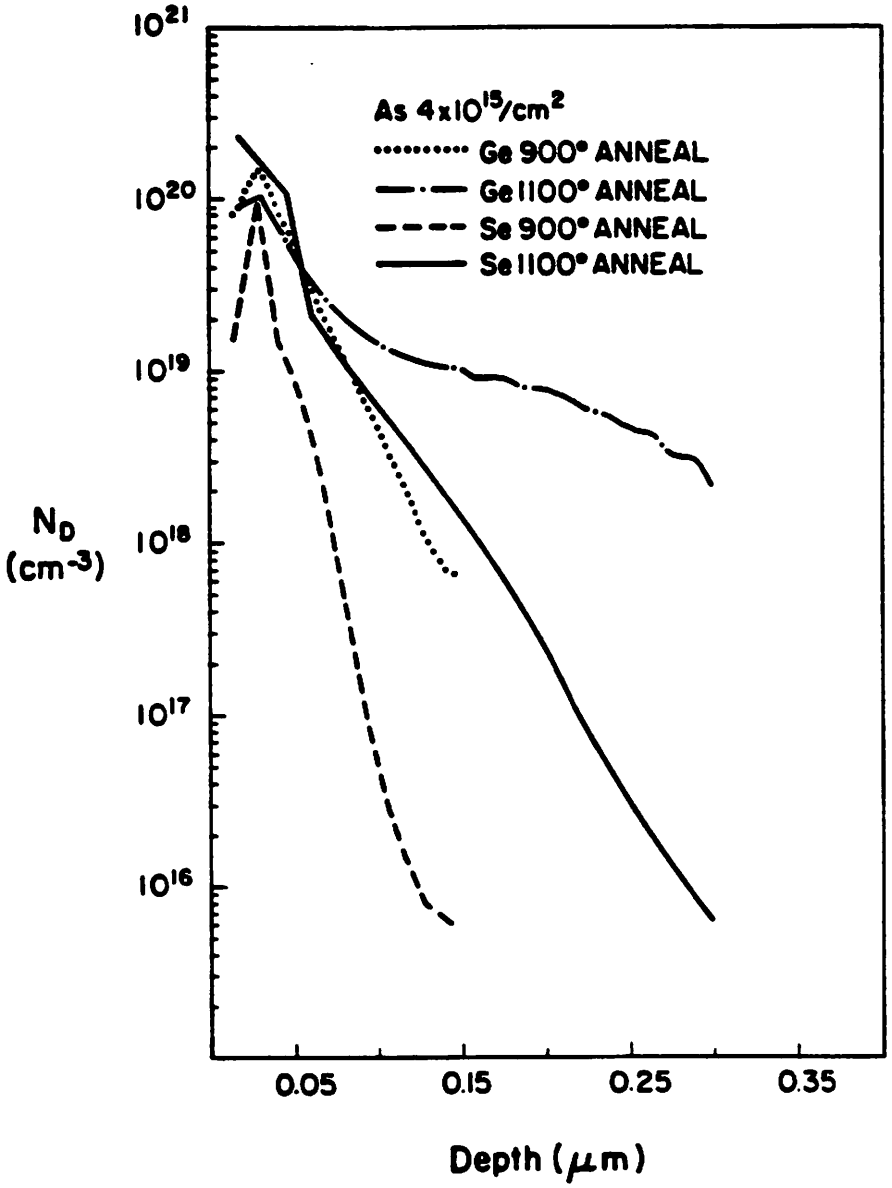


Figure 15

SIMS profiles of impurities in GaAs after ion-beam mixing with silicon and a 20 second RTA shows that the silicon contributes significantly to the doping.

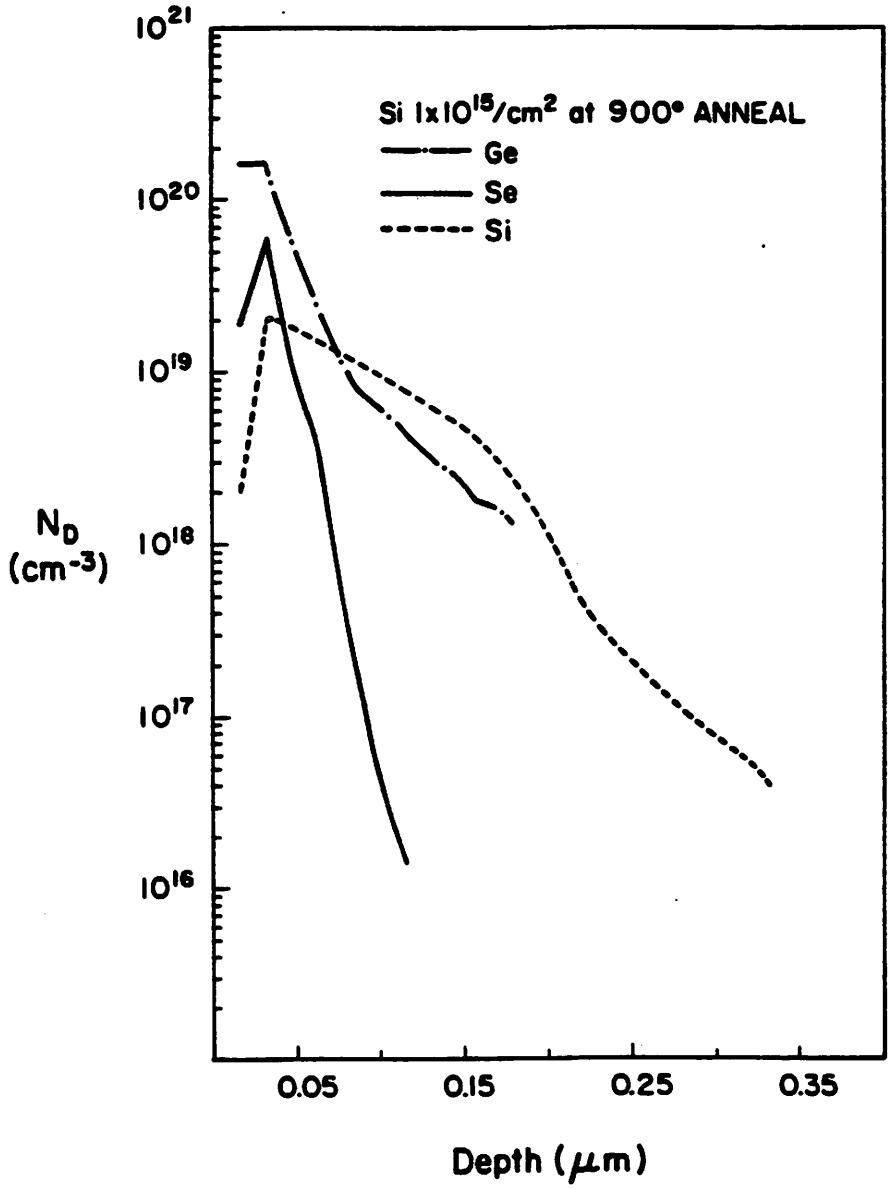


Figure 16

Backscattering spectra showing the annealing behavior of GaAs after ion-beam mixing and RTA. The crystalline disorder is repaired more effectively at higher temperatures

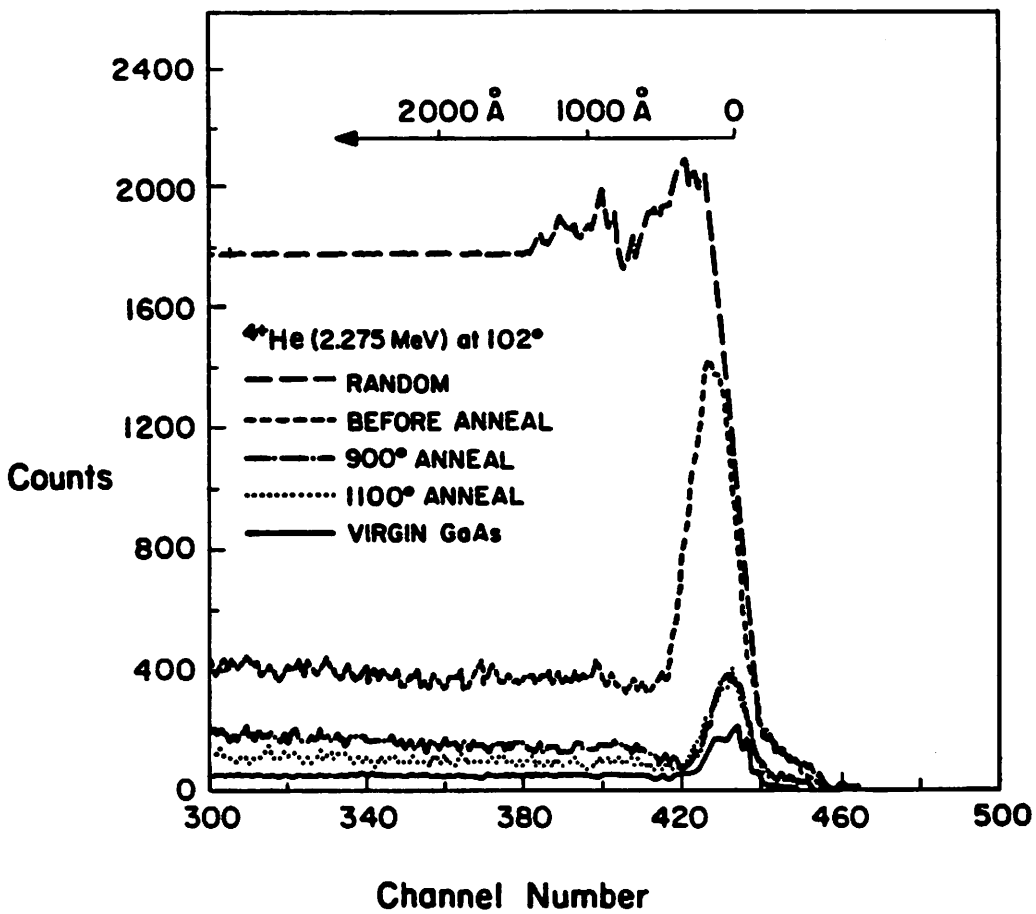


Figure 17

Variation of minimum channeling yield with annealing temperature. Samples implanted with silicon and arsenic are restroed to comparable levels by RTA, but furnace annealing does not restore the crystal as effectively. The furnace samples were annealed at 850°C for 30 minutes; this cycle corresponds to the same $\sqrt{Dt}$ as a 1000°C RTA for 20 seconds[14]

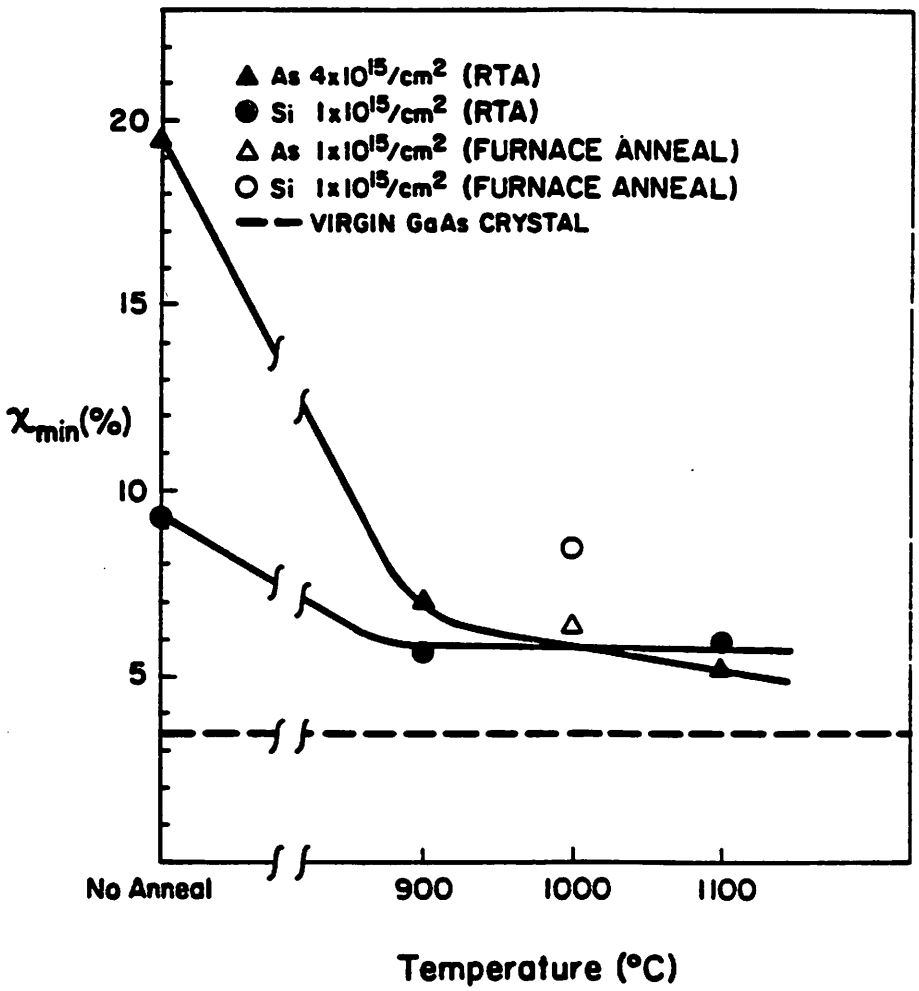


Figure 18

SEM micrographs from representative samples after (a) furnace annealing, and (b) RTA, illustrate the severe surface degradation caused by furnace annealing

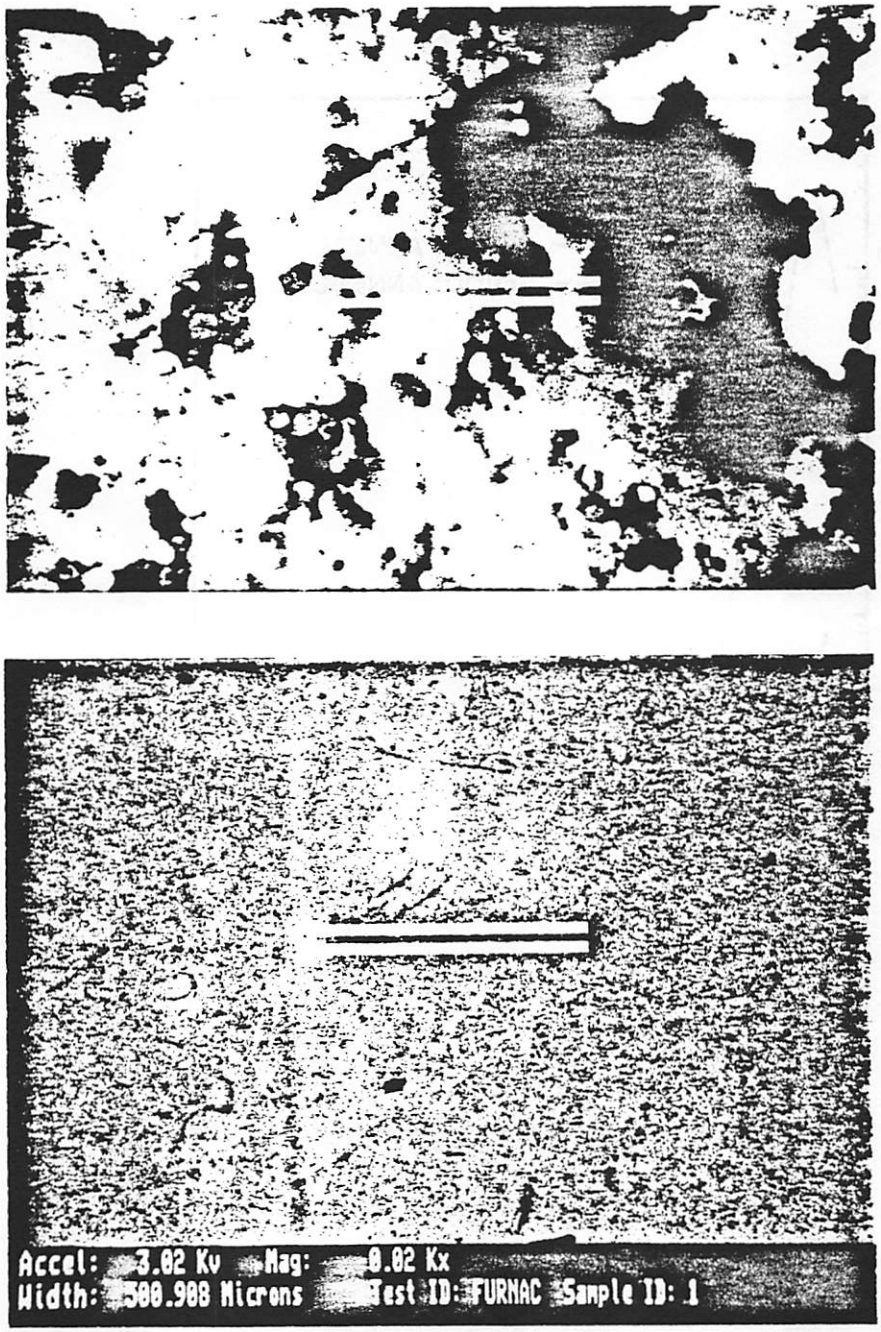


Figure 19

SIMS profile showing significant silicon diffusion into the GaAs from the sputtered SiO_2 encapsulant after an 1100 degress RTA

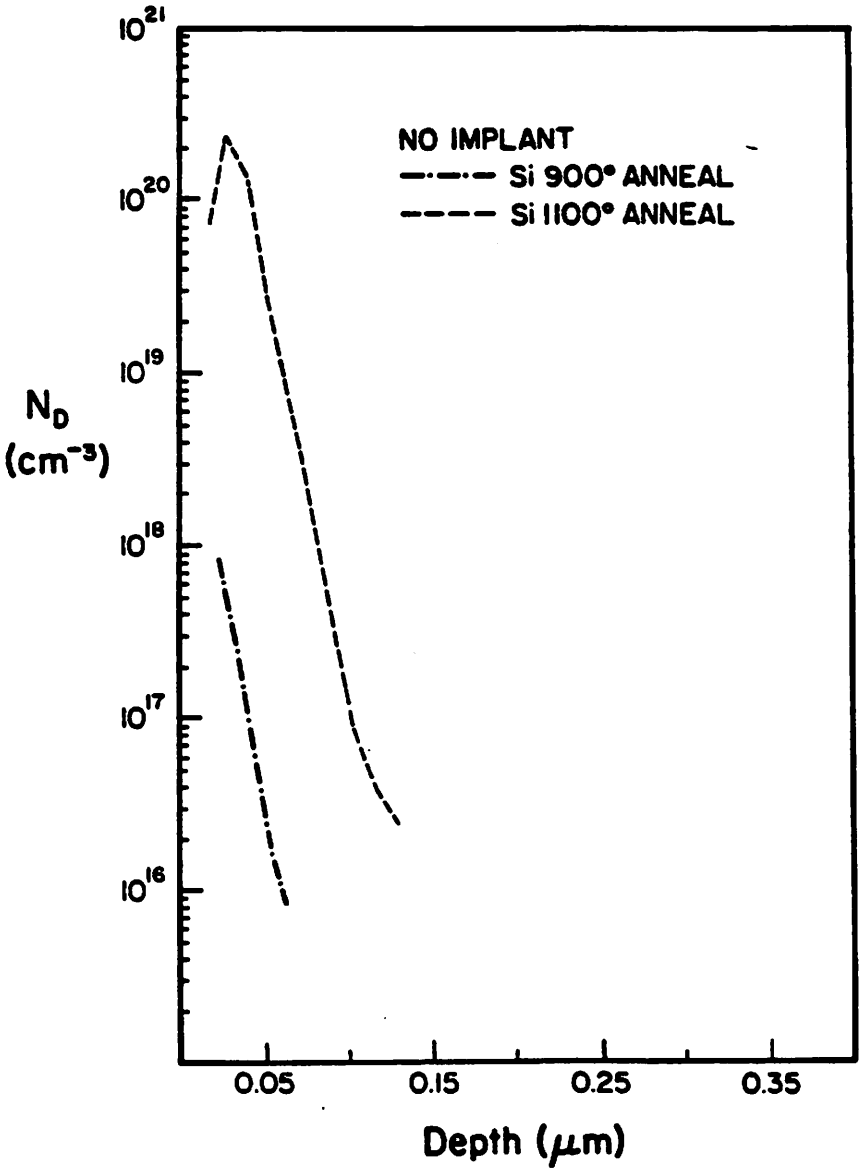


Figure 20

Specific contact resistivity is calculated by the extrapolation method from plots of resistance vs. contact spacing This plot represents gold contacts sintered at 340°C, and gives R_{SH}=56 Ω/□ and ρ_c=2.2 x 10^{-4} Ω · cm^2

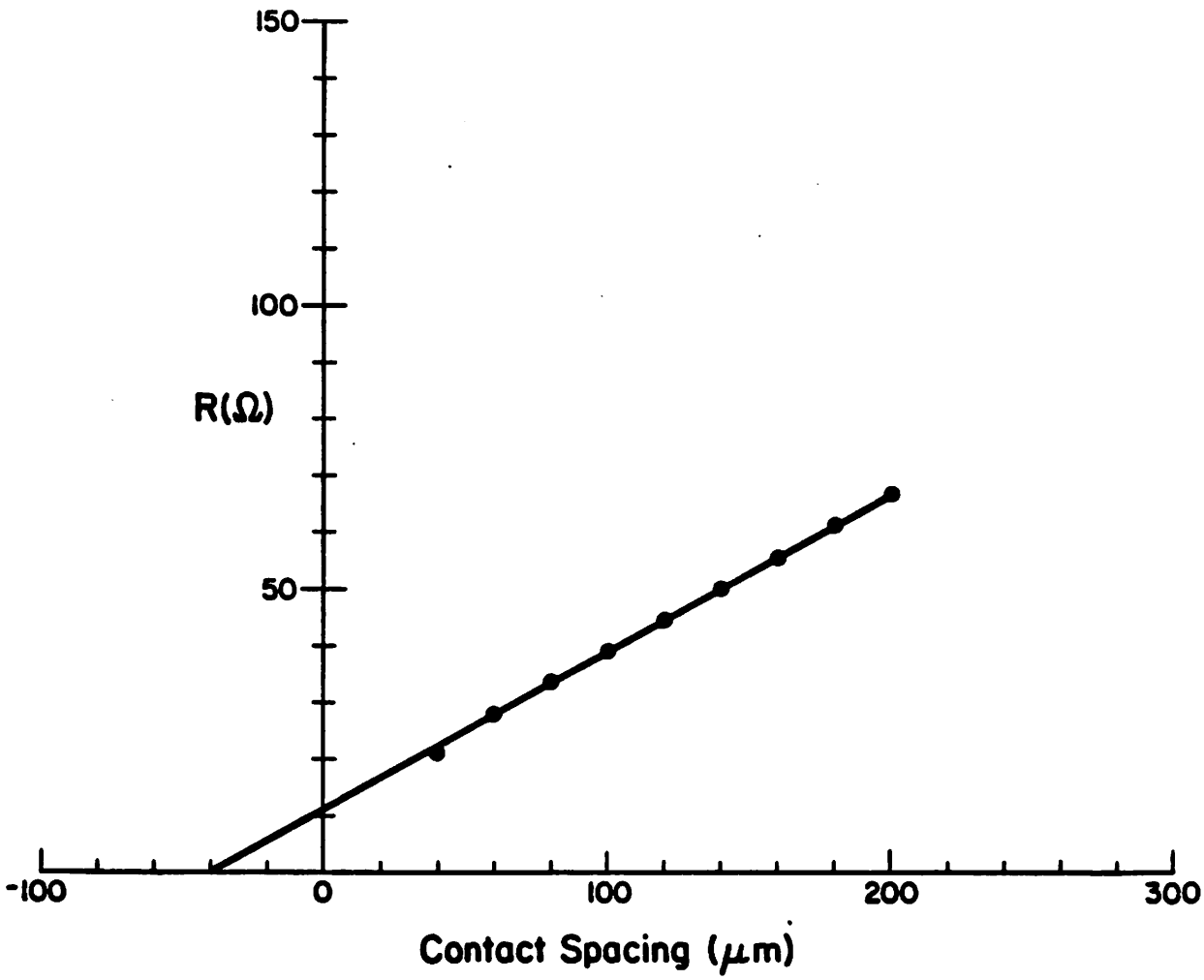
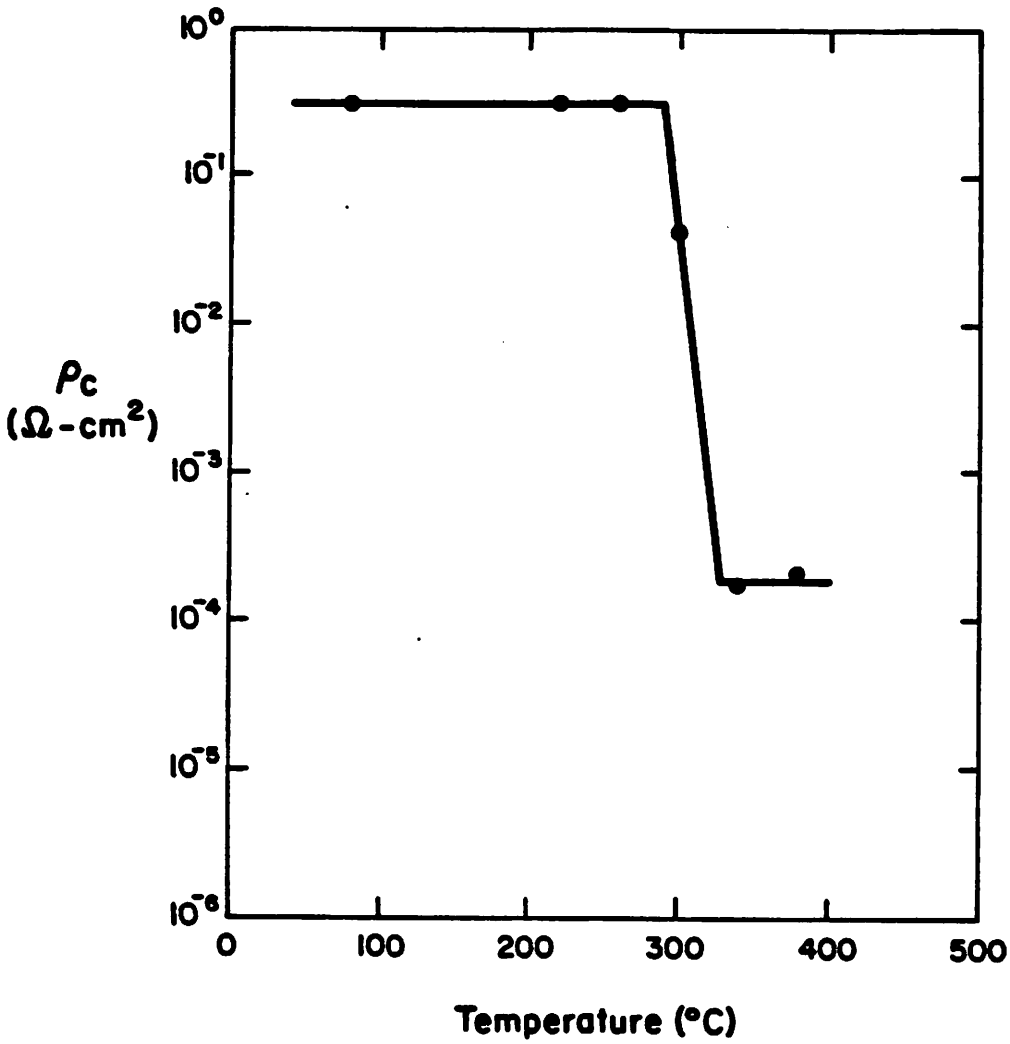


Figure 21

The dependence of specific contact resistivity on sintering temperature for gold contacts.



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