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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

SPICE2 Implementation of BSIM

Bing J. Sheu, Don L. Scharfetter, and Ping K. Ko

Department of Electrical Engineering and Computer Sciences
and Electronics Research Laboratory
University of California, Berkeley CA 94720

ABSTRACT

This ERL memorandum is composed of three parts. The first part is a collection of BSIM model equations. It includes dc models for both strong-inversion conduction and weak-inversion conduction, charge-based capacitance model, and extrinsic-component model. The second part is a supplement to the original "PROGRAM REFERENCE FOR SPICE". It is intended for CAD personnels who have to maintain SPICE2 with the BSIM option. The third part is a supplement to the original "SPICE Version 2G User's Guide". It is intended for SPICE users who have access to BSIM.

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I. Introduction

II. The Model

III. BSIM Program Reference

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I. INTRODUCTION

BSIM (Berkeley Short-channel IGFET Model) is composed of a simple and accurate short-channel MOSFET model and associated facility for IC process-oriented circuit design. BSIM has several important features. First, it is computation-efficient because the model formulation is simple. Second, the model can be easily extended to include new effects. Third, the model parameters for a family of devices can be obtained by automated characterization. The auto-characterization system generates a process file which describes process and model parameters for the circuit simulator. Designers need only describe the layouted geometries of devices and parasitic elements to execute circuit simulation. Use of a process file in a simulation is illustration in Fig. 1.

BSIM has been implemented in a special version of SPICE2G.6. The model equations used in BSIM are described in section II. Section III is the "BSIM Program Reference" which is a supplement to the original "PROGRAM REFERENCE FOR SPICE" by Cohen [1]. Section IV is the "BSIM User's Guide" which is a supplement to the original "SPICE Version 2G User's Guide" by Vladimirescu et al. [2]. The previously published ERL memoranda on the BSIM subject are listed in the reference [3-7].

II. THE MODEL

The formulation of the model is based on device physics of small-geometry MOS transistors. The special effects included are:

- vertical-field dependence of carrier mobility
- carrier-velocity saturation
- drain-induced barrier lowering
- depletion-charge sharing by the source and the drain
- non-uniform doping profile for ion-implanted devices
- channel length modulation
- subthreshold conduction
- geometric dependence of electrical parameters

II.1 The Process File

The process-file format is shown in Fig. 2. The process file is configurated into two parts: the keywords at the first line and the data at the other lines. Certain lines of data are grouped together and identified by the corresponding keyword at the first line. For example, the data at the third and fourth lines are associated with the first keyword DU1 specified at the first line. At present, there are 9 keywords for interconnect types (DU1 to DU3, PY1 to PY3, ML1 to ML3) and 10 keywords for transistor types (NM1 to NM5, PM1 to PM5). In a process file, there will be two lines of data associated with each interconnect keyword and 23 lines of data associated with each transistor keyword. The line with "*" as the first character is treated as a comment line and can be used as a reminder. Section IV describes the content of the process file in detail.

II.2 The DC Model – Strong-inversion Component

The characteristics of each device is modeled by 17 process-oriented parameters. At a particular bias voltage, the 17 process-oriented parameters are mapped into 8 model parameters through the following equations:

V_{FB} , ϕ_S , K_1 , K_2 are bias-independent.

$$U_0 = U_{0Z} + U_{0B} V_{BS} \tag{1}$$

$$U_1 = U_{1Z} + U_{1B}\, V_{BS} + U_{1D}\,(\, V_{DS} - V_{DD}\,) \tag{2}$$

$$\eta = \eta_Z + \eta_B\, V_{BS} + \eta_D\,(\, V_{DS} - V_{DD}\,) \tag{3}$$

μ_0 is obtained by quadratic interpolation through three data, μ_0 at $V_{DS} = 0$, μ_0 at $V_{DS} = V_{DD}$, and the sensitivity of μ_0 to V_{DS} at $V_{DS} = V_{DD}$, where

$$\mu_0\,(\text{ at } V_{DS} = 0\,) = \mu_Z + \mu_{ZB}\, V_{BS} \tag{4}$$

$$\mu_0\,(\text{ at } V_{DS} = V_{DD}\,) = \mu_S + \mu_{SB}\, V_{BS} \tag{5}$$

The eight model parameters are:

V_{FB}, the flat-band voltage,

ϕ_S, the surface-inversion potential,

K_1, the body-effect coefficient,

K_2, the source/drain depletion-charge-sharing-effect coefficient,

η, the drain-induced barrier lowering coefficient,

U_0, the mobility-degradation coefficient,

U_1, the velocity-saturation coefficient, and

μ_0, the carrier mobility.

The first 5 parameters model the threshold voltage :

$$V_{th} = V_{FB} + \phi_S + K_1\sqrt{\phi_S - V_{BS}} - K_2(\phi_S - V_{BS}) - \eta V_{DS} \tag{6}$$

The other 3 parameters model the drain current. In order to speed up the execution time for the circuit simulations, the 3/2 power dependence of the drain current on substrate bias has been replaced by the numerical approximation proposed by Poon [8-9]. The drain current in the triode region is expressed as:

$$I_{DS} = \frac{\mu\, C_o \dfrac{W}{L}}{(\, 1 + U_1\, V_{DS}\,)} \left[(\, V_{GS} - V_{th}\,)\, V_{DS} - \frac{a}{2}\, V_{DS}^2 \right] \tag{7}$$

$$\text{where} \quad \mu = \frac{\mu_0}{1 + U_0\,(\, V_{GS} - V_{th}\,)} \tag{8}$$

$$a = 1 + \frac{g\, K_1}{2\sqrt{\phi_S - V_{BS}}} \tag{9}$$

$$g = 1 - \frac{1}{1.744 + 0.8364\,(\phi_S - V_{BS})} \tag{10}$$

The body effect coefficient "a" makes BSIM a close numerical approximation of the standard text-book model over a reasonable range of V_{DB} and V_{DS} [9].

The drain current in the saturation region is expressed as:

$$I_{DS} = \frac{\mu C_o \frac{W}{L} (V_{GS} - V_{th})^2}{2 a K} \tag{11}$$

$$\text{where} \quad K = \frac{1 + v_c + \sqrt{1 + 2 v_c}}{2} \tag{12}$$

$$v_c = \frac{U_1 (V_{GS} - V_{th})}{a} \tag{13}$$

II.3 The DC Model – Including the Weak-inversion Component

The complete drain-current expression is

$$I_{DS_{complete}} = I_{DS_{si}} + I_{DS_{wi}} \tag{14}$$

where $I_{DS_{si}}$ is the strong-inversion component as described in sub-section II.2. The weak-inversion component $I_{DS_{wi}}$ can be expressed as

$$I_{DS_{wi}} = \frac{I_{exp} \cdot I_{limit}}{I_{exp} + I_{limit}} \tag{15}$$

$$\text{where} \quad I_{exp} = \mu_0 C_o \frac{W}{L} (\frac{kT}{q})^2 e^{1.8} e^{\frac{V_{GS}-V_{th}}{n} (\frac{q}{kT})} [1 - e^{-V_{DS} (\frac{q}{kT})}] \tag{16}$$

$$I_{limit} = \frac{\mu_0 C_o}{2} \frac{W}{L} (3 \frac{kT}{q})^2 \tag{17}$$

II.4 The Charge-based Capacitance Model

A new and simple capacitance model for BSIM has been derived. This new model conserves charge and has non-reciprocal property. Charge conservation is guaranteed by using charge as the state variable. The total stored charge in each of the gate, bulk, and channel regions is obtained by integrating the distributed charge densities over the area of the active region. Two physically meaningful channel-charge-partitioning method are used to partition the channel charge into drain

and source components. In BSIM, the drain/source partitioning of the channel charge changes from 40/60 (or 0/100) in the saturation region smoothly to 50/50 in the triode region.

The charge expressions in different regions are given below.

1) accumulation region:

$$Q_G = W\,L\,C_o\,(\,V_{GS} - V_{FB} - V_{BS}\,) \tag{18}$$

$$Q_B = -\,Q_G \tag{19}$$

$$Q_S = 0 \tag{20}$$

$$Q_D = 0 \tag{21}$$

2) subthreshold region:

$$Q_G = W\,L\,C_o\,\frac{K_1^2}{2}\left[-1 + \left[1 + \frac{4\,(\,V_{GS} - V_{FB} - V_{BS}\,)}{K_1^2}\right]^{1/2}\right] \tag{22}$$

$$Q_B = -\,Q_G \tag{23}$$

$$Q_S = 0 \tag{24}$$

$$Q_D = 0 \tag{25}$$

(A) 40/60 Channel-charge Partitioning Scheme

3) triode region:

$$Q_G = WLC_o\left[V_{GS} - V_{FB} - \phi_S - \frac{V_{DS}}{2} + \frac{V_{DS}}{12}\,\frac{\alpha_x\,V_{DS}}{(\,V_{GS} - V_{th} - \frac{\alpha_x}{2}\,V_{DS}\,)}\right] \tag{26}$$

$$Q_B = WLC_o\left[-V_{th} + V_{FB} + \phi_S + \frac{(1-\alpha_x)}{2}\,V_{DS} - \frac{(1-\alpha_x)\,V_{DS}}{12}\cdot\frac{\alpha_x\,V_{DS}}{(\,V_{GS} - V_{th} - \frac{\alpha_x}{2}\,V_{DS})}\right] \tag{27}$$

$$Q_S = -\,WLC_o\left[\frac{V_{GS} - V_{th}}{2} + \frac{\alpha_x\,V_{DS}}{12}\cdot\frac{\alpha_x\,V_{DS}}{(\,V_{GS} - V_{th} - \frac{\alpha_x}{2}\,V_{DS})}\right.$$

$$- \frac{\alpha_x V_{DS}}{\left(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS} \right)^2} \left[\frac{(V_{GS} - V_{th})^2}{6} - \frac{\alpha_x V_{DS} (V_{GS} - V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40} \right] \Bigg] \tag{28}$$

$$Q_D = - WLC_o \left[\frac{V_{GS} - V_{th}}{2} - \frac{\alpha_x V_{DS}}{2} + \frac{\alpha_x V_{DS}}{\left(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS} \right)^2} \left[\frac{(V_{GS} - V_{th})^2}{6} - \frac{\alpha_x V_{DS} (V_{GS} - V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40} \right] \right] \tag{29}$$

4) saturation region:

$$Q_G = W L C_o \left(V_{GS} - V_{FB} - \phi_S - \frac{V_{GS} - V_{th}}{3 \alpha_x} \right) \tag{30}$$

$$Q_B = W L C_o \left(V_{FB} + \phi_S - V_{th} + \frac{(1 - \alpha_x)(V_{GS} - V_{th})}{3 \alpha_x} \right) \tag{31}$$

$$Q_C = - \frac{2}{3} W L C_o (V_{GS} - V_{th}) \tag{32}$$

$$Q_S = - \frac{2}{5} W L C_o (V_{GS} - V_{th}) \tag{33}$$

$$Q_D = - \frac{4}{15} W L C_o (V_{GS} - V_{th}) \tag{34}$$

(B) 0/100 Channel-charge Partitioning Scheme

3') triode region:

$$Q_G = W L C_o \left[V_{GS} - V_{FB} - \phi_S - \frac{V_{DS}}{2} + \frac{V_{DS}}{12} \frac{\alpha_x V_{DS}}{\left(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS} \right)} \right] \tag{35}$$

$$Q_B = W L C_o \left[- V_{th} + V_{FB} + \phi_S + \frac{(1 - \alpha_x)}{2} V_{DS} - \frac{(1 - \alpha_x) V_{DS}}{12} \cdot \frac{\alpha_x V_{DS}}{\left(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS} \right)} \right] \tag{36}$$

$$Q_S = -WLC_o\left[\frac{V_{GS}-V_{th}}{2}+\frac{\alpha_x}{4}V_{DS}-\frac{\alpha_x V_{DS}}{24}\cdot\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right] \quad (37)$$

$$Q_D = -WLC_o\left[\frac{V_{GS}-V_{th}}{2}-\frac{3}{4}\alpha_x V_{DS}+\frac{\alpha_x V_{DS}}{8}\cdot\frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right] \quad (38)$$

4') saturation region:

$$Q_G = W\,L\,C_o\,(\,V_{GS}-V_{FB}-\phi_S-\frac{V_{GS}-V_{th}}{3\,\alpha_x}\,) \quad (39)$$

$$Q_B = W\,L\,C_o\,(\,V_{FB}+\phi_S-V_{th}+\frac{(\,1-\alpha_x\,)\,(\,V_{GS}-V_{th}\,)}{3\,\alpha_x}\,) \quad (40)$$

$$Q_C = -\frac{2}{3}\,W\,L\,C_o\,(\,V_{GS}-V_{th}) \quad (41)$$

$$Q_S = -\frac{2}{3}\,W\,L\,C_o\,(\,V_{GS}-V_{th}) \quad (42)$$

$$Q_D = 0 \quad (43)$$

II.5 The Extrinsic Components

(A) Transistor Parasitic Components

1) overlap capacitances:

$$C_{ovlgd} = C_{gdo}\cdot W_{eff} \quad (44)$$

$$C_{ovlgs} = C_{gso}\cdot W_{eff} \quad (45)$$

$$C_{ovlgb} = C_{gbo}\cdot L_{MK} \quad (46)$$

2) drain and source resistances:

$$R_D = R_{SH}\cdot N_{RD} \quad (47)$$

$$R_S = R_{SH}\cdot N_{RS} \quad (48)$$

3) drain and source junction conductances

$$I_{dt} = I_{JS} \cdot A_D \tag{49}$$

$$I_{st} = I_{JS} \cdot A_S \tag{50}$$

If not specified, I_{st} and I_{dt} will default to 1.0E-14.

4) Source/Drain Junction Capacitances

$$C_{bda} = C_J \cdot A_D \tag{51}$$

$$C_{bsa} = C_J \cdot A_S \tag{52}$$

$$C_{bdw} = C_{JW} \cdot P_D \tag{53}$$

$$C_{bsw} = C_{JW} \cdot P_S \tag{54}$$

4.1) drain junction:

For $V_{DS} < 0$:

$$Q_{BD} = P_J \cdot C_{bsa} \cdot \frac{[\,1-(\,1-\frac{V_{BD}}{P_J}\,)^{\,1-M_J}\,]}{1-M_J} + P_{JW} \cdot C_{bsw} \cdot \frac{[\,1-(\,1-\frac{V_{BD}}{P_{JW}}\,)^{\,1-M_{JW}}\,]}{1-M_{JW}} \tag{55}$$

$$C_{BD} = \frac{C_{bsa}}{(\,1-\frac{V_{BD}}{P_J}\,)^{M_J}} + \frac{C_{bsw}}{(\,1-\frac{V_{BD}}{P_{JW}}\,)^{M_{JW}}} \tag{56}$$

For $V_{BD} > 0$:

$$Q_{BD} = \frac{P_J \cdot C_{bsa}}{1-M_J} + \frac{P_{JW} \cdot C_{bsw}}{1-M_{JW}} + V_{BD} \cdot (\,C_{bsa} + C_{bsw}\,) + V_{SB}^{\,2} \cdot \left(\frac{C_{bsa} \cdot M_J}{2 \cdot P_J} + \frac{C_{bsw} \cdot M_{JW}}{2 \cdot P_{JW}} \right) \tag{57}$$

$$C_{BD} = C_{bsa} + C_{bsw} + V_{BD} \cdot \left(\frac{C_{bsa} \cdot M_J}{P_J} + \frac{C_{bsw} \cdot M_{JW}}{P_{JW}} \right) \tag{58}$$

4.2) source junction:

For $V_{BS} < 0$:

$$Q_{BS} = P_J \cdot C_{bsa} \cdot \frac{[\,1-(\,1-\frac{V_{BS}}{P_J}\,)^{\,1-M_J}\,]}{1-M_J} + P_{JW} \cdot C_{bsw} \cdot \frac{[\,1-(\,1-\frac{V_{BS}}{P_{JW}}\,)^{\,1-M_{JW}}\,]}{1-M_{JW}}$$

(59)

$$C_{BS} = \frac{C_{bsa}}{\left(1 - \frac{V_{BS}}{P_J}\right)^{M_J}} + \frac{C_{bsw}}{\left(1 - \frac{V_{BS}}{P_{JW}}\right)^{M_{JW}}} \tag{60}$$

For $V_{BS} > 0$:

$$Q_{BS} = \frac{P_J \cdot C_{bsa}}{1 - M_J} + \frac{P_{JW} \cdot C_{bsw}}{1 - M_{JW}} + V_{BS} \cdot (C_{bsa} + C_{bsw}) + V_{SB}^2 \cdot \left(\frac{C_{bsa} \cdot M_J}{2 \cdot P_J} + \frac{C_{bsw} \cdot M_{JW}}{2 \cdot P_{JW}} \right) \tag{61}$$

$$C_{BS} = C_{bsa} + C_{bsw} + V_{BS} \cdot \left(\frac{C_{bsa} \cdot M_J}{P_J} + \frac{C_{bsw} \cdot M_{JW}}{P_{JW}} \right) \tag{62}$$

(B) Resistors and Capacitors Generated with Interconnects

1) resistance:

$$R = R_{SH} \cdot \frac{L}{W} \tag{63}$$

2) capacitance:

$$C = C_J \cdot L \cdot W + 2 \cdot C_{JW} \cdot (L + W) \tag{64}$$

III. BSIM PROGRAM REFERENCE

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This is a supplement to the original "PROGRAM REFERENCE FOR SPICE." and is intended for CAD personnels who have to maintain SPICE with the BSIM (Berkeley Short-channel Igfet Model) option. It describes the functions of the newly added subroutines and the modifications to the original subroutines. The related linked list specifications are also included. To be complete, it should be used together with the original program reference.

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III.1 Implementation Consideration

The implementation of the BSIM model and the process-oriented simulator structure involves a large number of changes in the source code of SPICE 2G.6. These changes are described in terms of the subroutines and the data structure. New linked lists are created for the BSIM MOS device with internal ID=15, device process information with internal ID=25, and interconnect process information with internal ID=26.

Compared to the regular MOS device linked list in SPICE, there are more entries reserved for the BSIM MOS device to store the electrical parameters of each individual device. There are two model pointers in the BSIM MOS device linked list (ID=15) while one model pointer is reserved in regular MOS device linked list (ID=14). One of these two pointers points to the parameters for the active gate region and the other points to the parameters for source/drain junctions.

A new linked list with ID=25 is created to store the 57 extracted BSIM process parameters and one flag pararmeter to choose the channel charge partitioning method. The model pointer 1 in the BSIM MOS Device linked list (ID=15) points to the BSIM Model linked list (ID=25) for intrinsic gate region information. The model pointer 2 in the BSIM MOS Device linked list (ID=15) points to the Interconnect Model linked list (ID=26) for source/drain junction information. The model pointer in the Resistor linked list (ID=1) or the Capacitor linked list (ID=2) points to the Interconnect Model linked list (ID=26) for resistance or capacitance information.

The resistor and capacitor elements used to have no models, hence no pointers; now they have. For such an element two more entries are added to the original linked list, one for the interconnect type and the other for the model pointer. During the read-in stage, the simulation program stores the corresponding integer for different key words (PY1, ML1 and DU1 etc) appearing on the line specifying the element. Later the integer code of the element is used in searching for the appropriate model to which the pointer entry of the element can point. The same strategy is used for BSIM MOS devices. Section II contains the configuration of the linked lists described above.

The geometries of resistors, capacitors and MOS transistors are stored in their own linked lists as before. The pre-calculation takes place during the error-check stage. The electrical parameters of each BSIM MOS device are calculated from the BSIM process parameters together with the length and width of the device and are stored in the linked list of each device. The resistor and capacitor values are calculated from the process information of the various interconnects and the sizes of the elements. The source/drain junction capacitances of the BSIM MOS device are voltage dependent. Therefore, they have to be determined during each iteration cycle.

III.2 Functions of the Newly Added Subroutines

There are 5 new subroutines written for this implementation. Their names and functions are described in the following:

1) subroutine PROCHK.f:

This subroutine does a one-time pre-processing of device model parameters as described above. It prints out a list of the electrical parameters of the MOS devices as an optional. Its role is similar to that of MODCHK.f for the SPICE2 MOS Level-1, 2 and 3 models.

2) subroutine BSIMEQ.f:

The BSIM DC and charge/capacitance equations are implemented in this subroutine. Given all the electrical parameters and the specific terminal voltages of a MOS device, this routine evaluates the drain current & self-/trans- conductances and the charges & capacitances associated with the gate, bulk, and drain terminals. Its role is equivalent to a combination of subroutines MOSEQ2.f and MOSQ2.f.

3) subroutine BSIM.f:

This subroutine processes the MOS devices using the BSIM model for DC and transient analysis. It is similar to subroutine MOSFET.f in the original SPICE code. Only the companion BSIM charge/capacitance model is used for the charge storage effect associated with the thin oxide.

4) subroutine BSMCAP.f:

Given the calculated intrinsic charge and capacitances from subroutine BSIMQ.f and the overlap capacitances, this subroutine computes the equivalent conductances and terminal charges for the BSIM devices. It is like subroutine MOSCAP.f.

5) subroutine FNDTYP.f:

This subroutine changes the pointers from resistors, capacitors and BSIM devices to the linked lists for their own models. It uses two keys to search for a match, the process name and the model type. It is similar to subroutine FNDNAM.f in the original SPICE2 code.

III.3 Modification to the Original Subroutines

Seventeen subroutines in the original SPICE2 code are partially modified in implementing the BSIM model. Their names and modifications are described in the following:

ACLOAD.f	DCTRAN.f	LOAD.f	TOPCHK.f
ADDELT.f	ERRCHK.f	MATLOC.f	TRUNC.f
ALTER.f	FIND.f	MATPTR.f	
CARD.f	GETLIN.f	NXTCHR.f	
DCOP.f	LNKREF.f	READIN.f	

1) subroutine ACLOAD.f:

Blocks of code are added to zero out and load the complex coefficient matrix for BSIM MOS devices (ID=15).

2) subroutines ADDELT.f, ALTER.f and FIND.f:

The major changes in these subroutines are made to create linked lists with ID=15, 25 and 26, and to expand the sizes of the linked lists with ID=1 and 2. Sub-section III.4 describes the linked list specifications.

3) subroutines CARD.f, GETLIN.f:

Changes are made to handle the BSIM process file.

4) subroutine DCTRAN.f:

Subroutine BSIM.f is called by this subroutine. The line "1 +JELCNT(14)", which is near the beginning of source code for transient analysis, is changed to "1 +JELCNT(14)+JELCNT(15)".

5) subroutine DCOP.f:

Pieces of code are added to handle the printing of operating-point information of BSIM MOS devices.

6) subroutine ERRCHK.f:

The changes made include to translate node initial conditions to device initial conditions when UIC is specified on the .TRAN card for devices with ID=15, and to assign default values of length, width and areas to those devices. The added subroutine PROCHK.f is called by this subroutine.

7) subroutine LNKREF.f:

Pieces of code are inserted to resolve unsatisfied name references for the BSIM MOS devices. Subroutine FNDTYP.f is called by LNKREF.f twice for such device to fix both model pointers. This subroutine calls FNDTYP.f, instead of FNDNAM.f, to handle resistors and capacitors.

8) subroutine LOAD.f:

Subroutine BSIM.f is called by this subroutine.

9) subroutines MATPTR.f, MATLOC.f and TRUNC.f:

Pieces of code are inserted in these subroutines to take care of the BSIM MOS devices.

10) subroutine NXTCHR.f:

Change is made to treat "_" as a delimiter.

11) subroutine READIN.f:

There are more changes made in this subroutine than the previous ones. Variable strings BIDM(19), JPOLAR(19), NPROID(19), JPAR(3) and BMPAR(69) are created and initialized to handle the read-in of the BSIM MOS device and INTERCONNECT parameters. One more entry is added to the string AIDC to recognize the keyword "PROCESS". Changes are made take care of the new input syntax for resistors, capacitors, BSIM MOS devices, and INTERCONNECTs. The keyword "PROCESS" is treated like the keyword "MODEL" except it is used with ID=25 and 26. The process file is opened and the parameters in it are read by calling the subroutine CARD.f.

12) subroutine TOPCHK.f:

The line "1 1HQ,1HJ,1HM,0.0D0,0.0D0,1HT,0.0D0,0.0D0,0.0D0 /" is changed to "1 1HQ,1HJ,1HM,1HS,0.0D0,1HT,0.0D0,0.0D0,0.0D0 /" for the inclusion of BSIM MOS devices.

III.4 Linked List Specifications

(a). Resistor (ID=1)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: element name
	+1: LOCV		+1: g (TEMP)
	+2: n1		+2: r (TNOM)
	+3: n2		+3: temp.coef. 1
	+4: (n1,n2)		+4: temp.coef. 2
	+5: (n2,n1)		+5: length
	+6: (n1,n1)		+6: width
	+7: (n2,n2)		
	+8: model type		
	+9: model pointer		
	+10: cycle number		

(b). Capacitor (ID=2)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: element name
	+1: LOCV		+1: computed element value
	+2: n1		+2: initial condition
	+3: n2		+3: argument vector
	+4: function code		+4: length
	+5: (n1,n2)		+5: width
	+6: (n2,n1)		
	+7: tp (function coefficients)		
	+8: LXi offset	LXi	+0: q(capacitor)
	+9: exponent vector		+1: i(capacitor)
	+10: (n1,n1)		
	+11: (n2,n2)		
	+12: model type		
	+13: model pointer		
	+14: cycle number		

(c). BSIM MOS Device (ID=15)

	-1: subckt info			
LOC	+0: next pointer	LOCV	+0: element name	
	+1: LOCV		+1: mask channel length	
	+2: nd		+2: mask channel width	
	+3: ng		+3: drain diffusion area	
	+4: ns		+4: source diffusion area	
	+5: nb		+5: IC: vds	
	+6: nd'		+6: IC: vgs	
	+7: ns'		+7: IC: vbs	
	+8: model pointer 1		+8: device mode	
	+9: off		+9: von	
	+10: (nd,nd')		+10: vdsat	
	+11: (ng,nb)		+11: drain perimeter	
	+12: (ng,nd')		+12: source perimeter	
	+13: (ng,ns')		+13: # square of drain diff.	
	+14: (ns,ns')		+14: # square of source diff.	
	+15: (nb,ng)		+15: vto	
	+16: (nb,nd')		+16: XPART	
	+17: (nb,ns')		+17: VFB	
	+18: (nd',nd)		+18: PHI	
	+19: (nd',ng)		+19: K1	
	+20: (nd',nb)		+20: K2	
	+21: (nd',ns')		+21: ETA	
	+22: (ns',ng)		+22: BETAZ	
	+23: (ns',ns)		+23: U0	
	+24: (ns',nb)		+24: U1	
	+25: (ns',nd')		+25: X2BZ	
	+26: LXi offset		+26: X2E	
	+27: (nd,nd)		+27: X3E	
	+28: (ng,ng)		+28: X2U0	
	+29: (ns,ns)		+29: X2U1	
	+30: (nb,nb)		+30: BETAS	
	+31: (nd',nd')		+31: X2BS	
	+32: (ns',ns')		+32: X3BS	
	+33: model type 1		+33: X3U1	
	+34: model pointer 2		+34: COVLGD	+37: N0
	+35: model type 2		+35: COVLGS	+38: NB
	+36: cycle number		+36: COVLGB	+39: ND

Lxi	+0: VBDO	+16: QD
	+1: VBSO	+17: iQD
	+2: VGSO	+18: CGGBO
	+3: VDSO	+19: CGDBO
	+4: id	+20: CGSBO
	+5: ibs	+21: CBGBO
	+6: ibd	+22: CBDBO
	+7: gm	+23: CBSBO
	+8: gds	+24: QBD
	+9: gmbs	+25: iQBD
	+10: gbd	+26: QBS
	+11: gbs	+27: iQBS
	+12: QB	+28: CDGBO
	+13: iQB	+29: CDDBO
	+14: QG	+30: CDSBO
	+15: iQG	

Comments :

(1) vto=VFB+PHI+K1* $\sqrt{PHI}$ -K2*PHI

(2) device mode: +1(-1) for normal(inverse).

(3) If RSH $\neq$ 0.0D0, and NRD $\neq$ 0.0D0
then at LOCV+13: GDPR=1.0D0/(RSH*NRD)
If RSH $\neq$ 0.0D0, and NRS $\neq$ 0.0D0
then at LOCV+14: GDPR=1.0D0/(RSH*NRS)

(d). BSIM Model (ID=25)

	-1: subckt info
LOC	+0: next pointer
	+1: LOCV
	+2: device type

LOCV	+0: process name			
	+1: VFB	+22: U1	+43: X2MS	+64: NB
	+2: LVFB	+23: LU1	+44: LX2MS	+65: LNB
	+3: WVFB	+24: WU1	+45: WX2MS	+66: WNB
	+4: PHI	+25: X2MZ	+46: X3MS	+67: ND
	+5: LPHI	+26: LX2MZ	+47: LX3MS	+68: LND
	+6: WPHI	+27: WX2MZ	+48: WX3MS	+69: WND
	+7: K1	+28: X2E	+49: X3U1	
	+8: LK1	+29: LX2E	+50: LX3U1	
	+9: WK1	+30: WX2E	+51: WX3U1	
	+10: K2	+31: X3E	+52: TOX	
	+11: LK2	+32: LX3E	+53: TEMP	
	+12: WK2	+33: WX3E	+54: VDD	
	+13: ETA	+34: X2U0	+55: CGDO	
	+14: LETA	+35: LX2U0	+56: CGSO	
	+15: WETA	+36: WX2U0	+57: CGBO	
	+16: MUZ	+37: X2U1	+58: XPART	
	+17: DL	+38: LX2U1	+59: DUM1	
	+18: DW	+39: WX2U1	+60: DUM2	
	+19: U0	+40: MUS	+61: N0	
	+20: LU0	+41: LMS	+62: LN0	
	+21: WU0	+42: WMS	+63: WN0	

Comments :

(1) device type:

1 for NMOS

-1 for PMOS

(2) XPART:

1 for 0/100 drain/source charge partitioning at the saturation region.

0 for 40/60 drain/source charge partitioning at the saturation region.

(e). Interconnect Model (ID=26)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: process name
	+1: LOCV		+1: RSH
	+2: interconnect type		+2: CJ
			+3: CJW
			+4: IJS
			+5: PJ
			+6: PJW
			+7: MJ
			+8: MJW
			+9: WDF
			+10: DL

Comments :

(1) interconnect type:

1 for DU1

2 for DU2

3 for DU3

4 for PY1

5 for PY2

6 for PY3

7 for ML1

8 for ML2

9 for ML3

IV. BSIM USER'S GUIDE

****

This is a supplement to the original "SPICE Version 2G User's Guide," and is intended for SPICE users who have access to BSIM(Berkeley Short-channel Igfet Model). It contains descriptions of the various additional device features supported by BSIM and how to activate them. To be complete, it should be used together with the original user's guide.

****

In addition to the regular resistor and capacitor formats, BSIM also supports resistors and capacitors generated with interconnects.

IV.1 Resistors

General form:

RXXXXXXX N1 N2 PNAME_LT L=VAL <W=VAL> <TC=TC1<,TC2>>

Examples:

R1 1 2 PC1_DU1 L=10U

RC1 12 17 PC1_DU1 L=20U W=4U TC=0.001, 0.015

N1 and N2 are the two element nodes. PNAME is the process name.

LT is the interconnect type. At present, there are nine interconnect types available (DU1 to DU3, PY1 to PY3, and ML1 to ML3).

L and W are the resistor length and width, in meters. W should be specified if the default value in the process file is not used.

TC1 and TC2 are the (optional) temperature coefficients; if not specified, zero is assumed for both. The value of the resistor as a function of temperature is given by: value(TEMP) = value(TNOM)*(1+TC1*(TEMP-TNOM)+TC2*(TEMP-TNOM)**2))

IV.2 Capacitors

General form:

CXXXXXXX N1 N2 PNAME_LT L=VAL <W=VAL>

Examples:

CBYP 13 0 PC1_PY1 L=20U

COSC 17 23 PC1_ML2 L=30U W=30U IC=3V

N1 and N2 are the two element nodes. PNAME is the process name.

LT is the interconnect type. At present, there are nine interconnect types available (DU1 to DU3, PY1 to PY3, and ML1 to ML3).

L and W are the capacitor length and width, in meters. W should be specified if the default value in the process file is not used.

The (optional) initial condition is the initial (time-zero) value of capacitor voltage (in volts). [Note that the initial conditions (if any) apply 'only' if the UIC option is specified on the .TRAN card.]

IV.3 BSIM MOSFET's

General form:

SXXXXXXX ND NG NS NB PNAME_MT_DT<_STHD> <L=VAL> <W=VAL> <AD=VAL>

+ <AS=VAL> <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF>

+ <IC=VDS,VGS,VBS>

Examples:

S1 24 2 0 20 PC1_NM1

S31 2 17 6 10 PC2_NM2_DU2_STHD L=5U W=2U

S31 2 16 6 10 PC2_PM1_DU3 5U 2U

S1 2 9 3 0 PC2_PM2_DU3 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

S1 2 9 3 0 PC1_NM1_STHD 10U 5U 2P 2P

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively.

PNAME is the process name.

MT is the mos type. At present, there are five mos types for both NMOS and PMOS (NM1 to NM5, and PM1 to PM5).

DT is the diffusion type to be used for the source/drain junctions. The three three diffusion types available (DU1, DU2, and DU3). The default is DU1.

L and W are the channel length and width, in meters.

AD and AS are the areas of the drain and source diffusions, in sq-meters.

[Note that the suffix U specifies microns (1E-6 m) and P sq-microns (1E-12 sq-m). If any of L,

W, AD, or AS are not specified, default values are used. The user may specify the values to be used for these default parameters on the .OPTIONS card. The use of defaults simplifies input deck preparation, as well as the editing required if device geometries are to be changed.]

PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .process card for an accurate representation of the parasitic series drain and source resistance of each transistor.

[PD, PS, NRD, and NRS all default to 0.0. OFF indicates an (optional) initial condition on the device for dc analysis. The (optional) initial condition specification using IC=VDS,VGS,VBS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. See the .IC card for a better and more convenient way to specify transient initial conditions.]

IV.4 .PROCESS Card

General form:

.PROCESS PNAME FILENAME=fname

Examples:

.PROCESS PC1 FILENAME=PNMED

.PROCESS PD2 FILENAME=FAST

The .PROCESS card specifies process parameter values that will be used by one or more devices.

PNAME is the process name, and fname is the name of the file containing the process parameter values. The process card is used together with resistors, capacitors, as well as mosfets.

IV.5 Process File

This file is generated by the automated characterization program, and it contains the process information for the transistors as well as for the interconnects. For transistors, the L (channel-length) and W (channel-width) sensitivity factors of a basic electrical parameter are denoted by appending the italic characters 'l' and 'w' to the name of the parameter. For the example of the basic parameter V_{FB} (flat-band voltage), there are two corresponding sensitivity factors, V_{FBl}, V_{FBw}. If P_0 is the basic parameter and P_L and P_W are the corresponding L and W sensitivity

factors. The formula

$$P = P_0 + \frac{P_L}{L_{eff}} + \frac{P_W}{W_{eff}}$$

is used to obtained the value for each transistor size with both L_{eff} (= L_{MK} - ΔL) and W_{eff} (= W_{MK} - ΔW) in μm.

(a) The format of the process parameters is listed below:

TRANSISTORS

	name	L sens. factor	W sens. factor	units of basic parameter
1	V_{FB} (VFB)	V_{FBl} (LVFB)	V_{FBw} (WVFB)	V
2	ϕ_S (PHI)	ϕ_{Sl} (LPHI)	ϕ_{Sw} (WPHI)	V
3	K_1 (K1)	K_{1l} (LK1)	K_{1w} (WK1)	$V^{1/2}$
4	K_2 (K2)	K_{2l} (LK2)	K_{2w} (WK2)	-
5	η_0 (ETA)	η_{0l} (LETA)	η_{0w} (WETA)	-
6	μ_Z (MUZ)	δ_l (DL)	δ_w (DW)	$cm^2/V-s(\ \mu m\ ,\ \mu m\ )$
7	U_{0Z} (U0)	U_{0Zl} (LU0)	U_{0Zw} (WU0)	V^{-1}
8	U_{1Z} (U1)	U_{1Zl} (LU1)	U_{1Zw} (WU1)	$\mu m\ V^{-1}$
9	μ_{ZB} (X2MZ)	μ_{ZBl} (LX2MZ)	μ_{ZBw} (WX2MZ)	cm^2/V^2-s
10	η_B (X2E)	η_{Bl} (LX2E)	η_{Bw} (WX2E)	V^{-1}
11	η_D (X3E)	η_{Dl} (LX3E)	η_{Dw} (WX3E)	V^{-1}
12	U_{0B} (X2U0)	U_{0Bl} (LX2U0)	U_{0Bw} (WX2U0)	V^{-2}
13	U_{1B} (X2U1)	U_{1Bl} (LX2U1)	U_{1Bw} (WX2U1)	$\mu m\ V^{-2}$
14	μ_S (MUS)	μ_{Sl} (LMS)	μ_{Sw} (WMS)	cm^2/V^2-s
15	μ_{SB} (X2MS)	μ_{SBl} (LX2MS)	μ_{SBw} (WX2MS)	cm^2/V^2-s
16	μ_{SD} (X3MS)	μ_{SDl} (LX3MS)	μ_{SDw} (WX3MS)	cm^2/V^2-s
17	U_{1D} (X3U1)	U_{1Dl} (LX3U1)	U_{1Dw} (WX3U1)	$\mu m\ V^{-2}$
18	T_{ox} (TOX)	T_{emp} (TEMP)	V_{dd} (VDD)	$\mu m\ (^0C\ .\ V)$
19	CGDO	CGSO	CGBO	F/m
20	XPART	DUM1	DUM2	-
21	N0	LN0	WN0	
22	NB	LNB	WNB	

23	ND	LND	WND

INTERCONNECTS

1	Rsh (RSH)	Cj (CJ)	Cjw (CJW)	Ijs (IJS)	Pj (PJ)
2	P_{jw} (PJW)	Mj (MJ)	Mjw (MJW)	Wdf (WDF)	δ_l (DL)

(b) The names of the process parameters of transistors are listed below:

V_{FB}	flat-band voltage
ϕ_S	surface inversion potential
K_1	body effect coefficient
K_2	drain/source depletion charge sharing coefficient
η_0	zero-bias drain-induced barrier lowering coefficient
μ_Z	zero-bias mobility
U_{0Z}	zero-bias transverse-field mobility degradation coefficient
U_{1Z}	zero-bias velocity saturation coefficient
μ_{ZB}	sensitivity of mobility to substrate bias at $V_{ds} = 0$
η_B	sensitivity of drain-induced barrier lowering effect to substrate bias
η_D	sensitivity of drain-induced barrier lowering effect to drain bias, at $V_{ds}= V_{dd}$
U_{0B}	sensitivity of transverse-field mobility degradation effect to substrate bias
U_{1B}	sensitivity of velocity saturation effect to substrate bias
μ_S	mobility at zero substrate bias and at $V_{ds}=V_{dd}$
μ_{SB}	sensitivity of mobility to substrate bias at $V_{ds} = V_{dd}$
μ_{SD}	sensitivity of mobility to drain bias at $V_{ds} = V_{dd}$
U_{1D}	sensitivity of velocity saturation effect to drain bias, at $V_{ds}= V_{dd}$
T_{ox}	gate-oxide thickness
T_{emp}	temperature at which the process parameters are measured
V_{dd}	measurement bias range
N0	zero-bias subthreshold slope coefficient

NB	sensitivity of subthrehold slope to substrate bias
ND	sensitivity of subthrehold slope to drain bias
CGDO	gate-drain overlap capacitance per meter channel width
CGSO	gate-source overlap capacitance per meter channel width
CGBO	gate-bulk overlap capacitance per meter channel length
XPART	gate-oxide capacitance model flag

Note: XPART=0 selects 40/60 drain/souorce charge-partitioning at the saturation region. while XPART=1 selects 0/100 drain/source charge-partitioning at the saturation region. XPART=1 is recommended.

The names of the process parameters of diffusion layers are listed below:

sheet resistance/square	Rsh	Ω/square
zero-bias bulk junction bottom capacitance/unit area	Cj	F/m^2
zero-bias bulk junction sidewall capacitance/unit length	Cjw	F/m
bulk junction saturation current/unit area	Ijs	A/m^2
bulk junction bottom potential	Pj	V
bulk junction sidewall potential	Pjw	V
bulk junction bottom grading coefficient	Mj	-
bulk junction sidewall grading coefficient	Mjw	-
default width of the layer	Wdf	m
average variation of size due to side etching or mask compensation	δ_l	m

---

The names of the process parameters of poly and metal layers are listed as following:

sheet resistance/square	Rsh	Ω/square

capacitance/unit area	Cj	F/m^2
edge capacitance/unit length	Cjw	F/m
default width of the layer	Wdf	m
average variation of size due to side etching or mask compensation	δ_l	m

IV.6 EXAMPLE DATA DECKS

(a) The following is an example of a process file. The lines starting with "*" are used as comments.

```
NM1 DU1 PY1 ML1
*PROCESS=PC1
*RUN=12 medium-size devices
*OPERATOR=Ralph
*DATE=11/3/84
*n-channel mosfet
-1.0641E+000    1.71979E-001    1.11454E-001
7.95392E-001    0.00000E+000    0.00000E+000
1.10425E+000    -4.3371E-001    -9.8518E-002
1.93126E-001    4.14269E-004    -6.0274E-002
-4.7124E-003    -1.0565E-002    1.08645E-002
6.00853E+002    6.24380E-001    1.03840E+000
5.11222E-002    1.73108E-001    -5.9804E-002
-2.3954E-001    2.91101E+000    -5.3638E-002
4.66158E+000    -8.0305E+000    5.54267E+000
-9.1420E-004    1.23113E-002    2.43260E-003
1.05704E-004    1.04115E-002    -2.5834E-003
2.68363E-004    -1.5668E-003    -8.5052E-004
-7.2567E-002    1.10182E-001    5.66859E-002
5.49834E+002    1.77273E+003    -9.0196E+001
-1.6724E+001    8.98504E+000    2.82340E+001
4.86164E+000    1.56629E+001    -6.5700E+000
7.76925E-003    -1.0940E-001    -8.3353E-003
2.50000E-002    2.50000E+001    5.00000E+000
1.50000E-009    1.50000E-009    2.00000E-010
1.0             0.0             0.0
1.50000E+000    0.00000E+000    0.00000E+000
```

```
1.00000E-001    0.00000E+000    0.00000E+000
0.00000E+000    0.00000E+000    0.00000E+000
*n+ diffusion layer
50.0            4.5e-5          0.0             1.0e-4  0.8
0.6             0.5             0.33            2.0e-6  0.5
*polysilicon layer
20.0            7.0e-5          3.6e-11         0.0     0.0
0.0             0.0             0.0             2.0e-6  0.5
*metal layer
0.04            0.26e-4         0.36e-10        0.0     0.0
0.0             0.0             0.0             3.0e-6  0.4
```

(b) The following deck determines the transient characteristics of a resistive load inverter with a capacitor connected at the output node.

```
SAMPLE CMOS INVERTER
VCC  1  0  5
SMN1  2  3  0  0  PC1_NM1      W=50U L=10U
SMP1  2  3  1  1  PC1_PM1_DU2  W=50U L=10U
VIN  4  0  PWL (0 0  5N 5  10N 5  20N 0)
RIN  4  3  PC1_PY1   L=20U  W=60U
C1   2  0  50FF
.OPTIONS  NOMOD  RELTOL=1E-5  CHGTOL=1E-15
.TRAN  0.5N  20N
.PRINT TRAN  V(3)  V(2)
.PLOT TRAN  V(3)  V(2)
.PROCESS PC1 FILENAME=PNMED
.WIDTH OUT=80
.END
```

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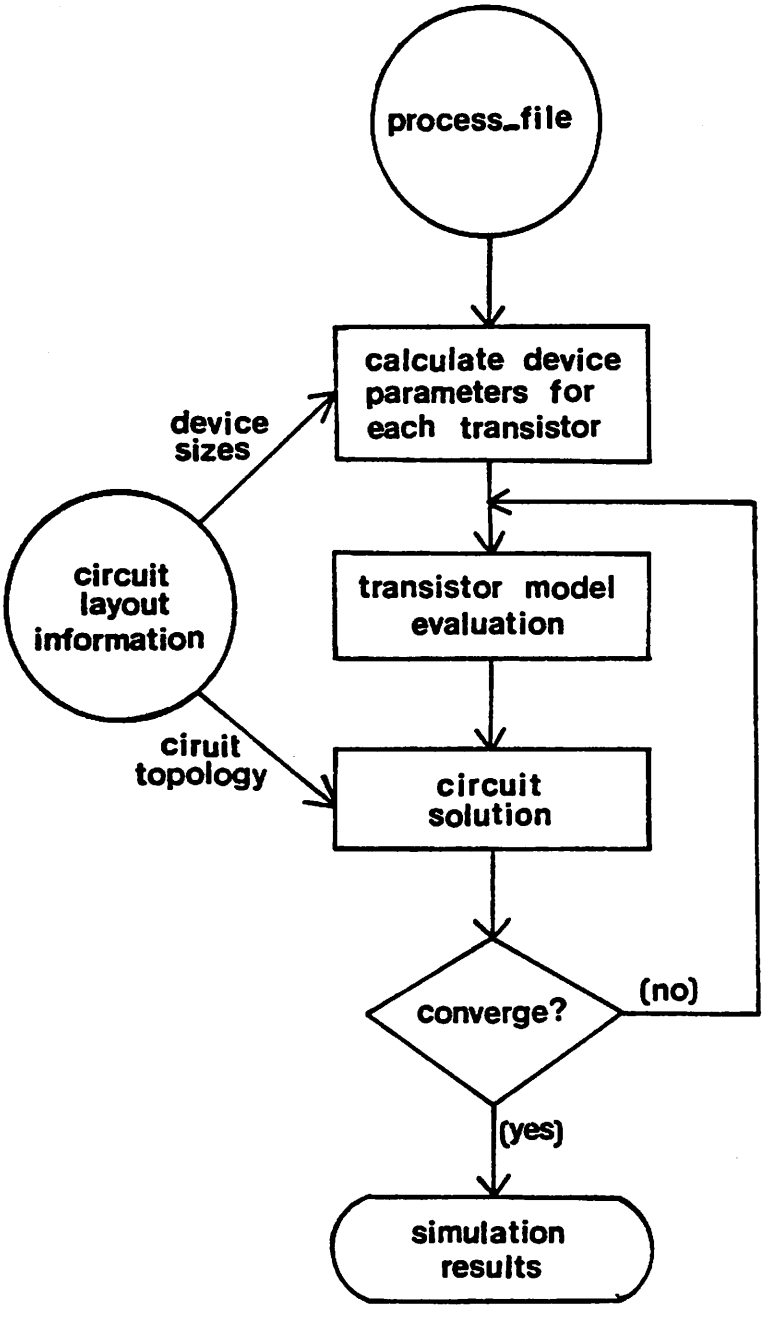

Fig. 1 Process-oriented circuit simulation

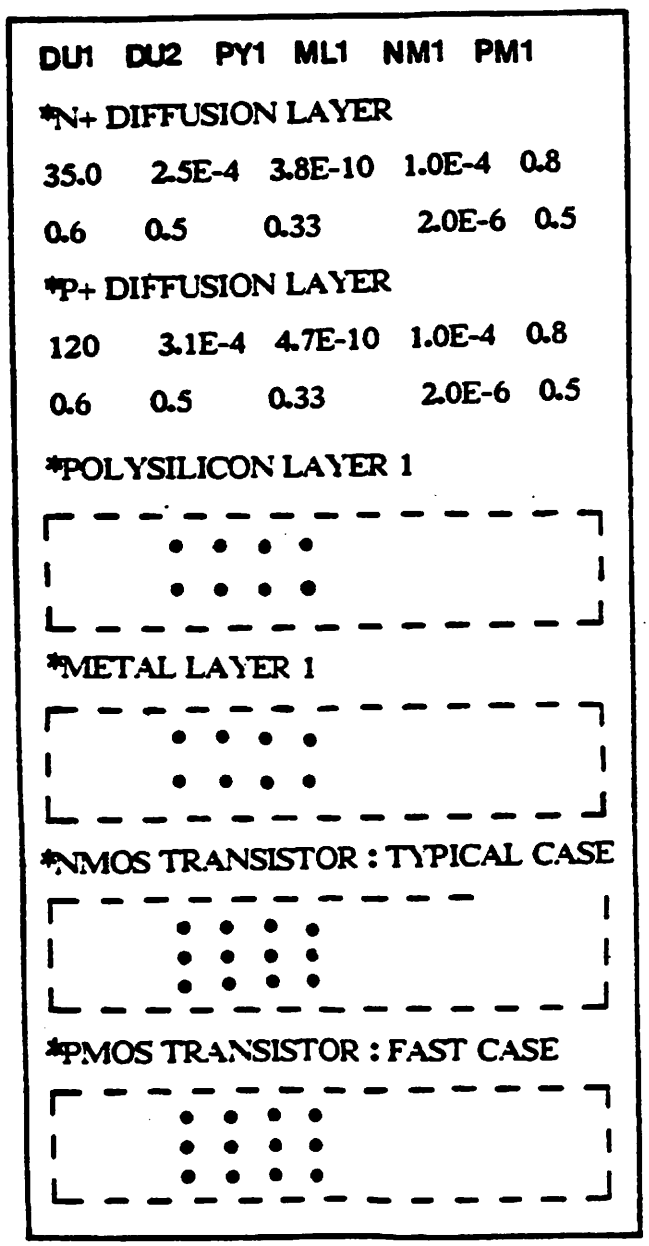

Fig. 2 Process-file configuration