# CHAOS IN A SWITCHED CAPACITOR CIRCUIT

by

A. Rodriguez-Vazquez, J. J. Huertas and L. O. Chua

Memorandum No. UCB/ERL M85/44

24 May 1985

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

# Chaos in a Switched Capacitor Circuit[1]

A. Rodriguez-Vazquez, J. J. Huertas and L.O. Chua[2]

*Abstract*

We report chaotic phenomena observed from a simple nonlinear switched capacitor circuit. The experimentally measured *bifurcation tree* diagram reveals a *period-doubling route* to chaos. This circuit is described by a first-order discrete equation which can be transformed into the *logistic map* whose chaotic dynamics is well known.

[1]This research is supported in part by the Office of Naval Research under Contract NOOO14-76-C-0572, the National Science Foundation Grant ECS-8542885, and by the Spain CAICYT under Contract 0245/81.

[2]Rodriguez-Vazquez and Huertas are with the University of Seville, Spain. L.O. Chua is with the University of California, Berkeley.

Several nonlinear circuits which exhibit various types of chaotic phenomena have been reported recently [1-5]. Our objective in this letter is to report an experimental result showing the ubiquitous *chaotic* phenomena can also occur in a switched-capacitor circuit. Since switched-capacitor circuits are important in VLSI technology, any potential anomaly or failure mechanisms due to the onset of chaos should be fully analyzed. This chaotic circuit is also of circuit-theoretic interest because its dynamic equation is equivalent to the well-known *logistic* map [6] whose chaotic dynamics have been extensively studied and is now well-understood. Since the logistic map is the simplest *chaotic* polynomial discrete map, the chaotic circuit to be described below is the *simplest* chaotic circuit described by a *first-order discrete* map.

Consider the switched capacitor circuit in Fig. 1(a): it is made of a battery $V_S$, a linear capacitor $C_S$, a *nonlinear* switched capacitor component [7-8], and three analog switches. The state (on or off) of the switches is controlled by a standard two-phase clock defined by the timing diagram shown in Fig. 1(b). The switches labeled $S^{\phi}$ (resp., $S^{\phi}$) turn *on* in synchronization with the rising edge of the clock signal $\phi^{\phi}$ (resp., $\phi^{\phi}$).

The nonlinear switched capacitor component —henceforth called an FESC (forward Euler switched-capacitor) resistor— is defined by

$$Q_n - Q_{n-1} = K V_{n-1}^2 \triangleq \Delta Q_n \qquad (1)$$

where $\Delta Q_n$ is the net charge flowing into the FESC resistor during the n *th* clock period, $V_{n-1}$ is the voltage sampled across the FESC resistor during the (n-1) *th* period, and K is an arbitrary positive constant.

We have built the circuit in Fig. 1(a) with $C_S = 1\,nF$ and $K = .5\,nF/V$ using off-the-shelf components and observed the steady-state voltage waveform samples V for different values of the battery voltage $V_S$. Contrary to our intuitive expectation for a single-valued relationship between V and $V_S$, we found the relationship to be *multiple* -valued over some ranges of the "parameter" $V_S$, and undefined i.e., *chaotic*, for other

ranges. This observation is summarized by the *bifurcation tree* measured experimentally from this circuit. The familiar cascades preceding the chaotic region implies a *period-doubling route* to chaos [6].

To derive a recursive relationship for $V_n$, we note that the net charge $\Delta Q_{net}$ flowing into the FESC resistor during the (n+1) *th* clock period must be equal to the net charge flowing out of the *linear* capacitor $C_s$ (charge conservation principle), and hence:

$$V_{n+1} = V_s - \frac{K}{C_s} V_n^2 \qquad (2)$$

We can transform (2) into several more familiar equivalent forms by defining

$$X_{n+1} = a V_{n+1} + b \qquad (3)$$

If we choose $a = 1/V_s$ and b=0, we would obtain

$$X_{n+1} = 1 - \lambda X_n^2 \qquad (4)$$

where

$$\lambda = K V_s / C_s$$

If we choose

$$a = \frac{1}{4V_s}\left(-1 \pm \sqrt{1 + 4K\frac{V_s}{C_s}}\right)$$

and b=½, we would obtain the well known *logistic map*

$$X_{n+1} = 4\lambda X_n (1 - X_n) \qquad (5)$$

where

$$\lambda \triangleq \frac{K}{4aC_s}$$

Both equations, (3) and (5) have been intensively studied [6] and their global qualitative behaviors are now well classified and understood. Consequently, Fig. 1(a) represents the *first* real physical circuit whose chaotic dynamics can be *completely* analyzed.

For readers interested in repeating our experiments, the FESC resistor in Fig. 1(a) can be realized by the circuit shown in Fig. 3.

*Acknowledgement:*

The authors would like to thank Greg Bernstein for stimulating discussions which led to this letter.

*Figure Captions*

Fig. 1 A nonlinear switched capacitor circuit and its associated timing diagram.

Fig. 2 Bifurcation tree

Fig. 3 Off-the-shelf realization of the FESC resistor in Fig. 1(a).

*References*


1. Tang, Y.S., A.I. Mees and L.O. Chua, "Synchronization and Chaos", *IEEE Trans. on Circuits and Systems*, vol. CAS-30, pp. 620-626, September 1983.
2. A. Azzouz, R. Duhr and M. Hasler, "Transition to Chaos in a Simple Nonlinear Circuit Driven by a Simusoidal Voltage Source," *IEEE Trans. Circuits and Systems*, vol. CAS-30, pp. 913-914, December 1983.
3. T. Matsumoto, L.O. Chua and S. Tanaka, "Simplest Chaotic Nonautonomous Circuit," *Physical Review A*, vol. 30, pp. 1155-1157, August 1984.
4. T. Matsumoto, "A Chaotic Attractor from Chua's Circuit," *IEEE Trans. on Circuits and Systems*, vol. CAS-31, pp. 1055-1058, December 1984.
5. G-Q Zhong and F. Ayrom, "Experimental Confirmation of Chaos from Chua's Circuit," *International Journal of Circuit Theory and Applications*, vol. 13, pp. 93-98, 1985.
6. P. Cvitanovich (Ed.), *Universality in Chaos: A Report Selection*, Adam Hilger, Bristol, 1984.
7. J.L. Huertas, L.O. Chua, A.B. Rodriguez-Vazquez and A. Rueda, "Nonlinear Switched-Capacitor Networks: Basic Principles and Piecewise-linear Design," *IEEE Trans. Circuits Systems*, vol. CAS-32, pp. 305-319, April 1985.
8 A. Rodriguez-Vazquez, J.L. Huertas and L.O. Chua, "On a Class of SC Resistors and its Application to the Synthesis of Nonlinear Driving-Point and Transfer-Characteristic Plots", *Int. Journal Circuit Theory and Applications*, to appear.
9 A. Rodriguez-Vazquez, J.L. Huertas, L.O. Chua: "Rational SC Networks", in preparation.

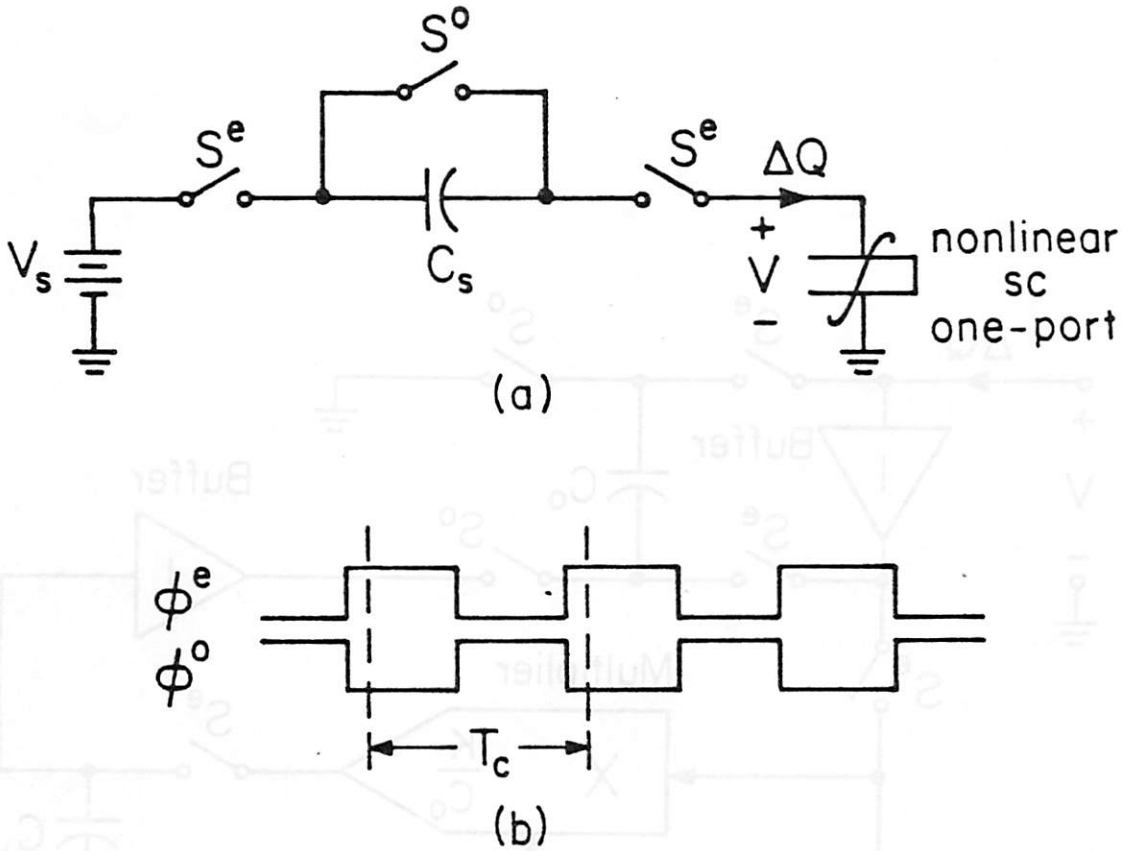


Figure 1

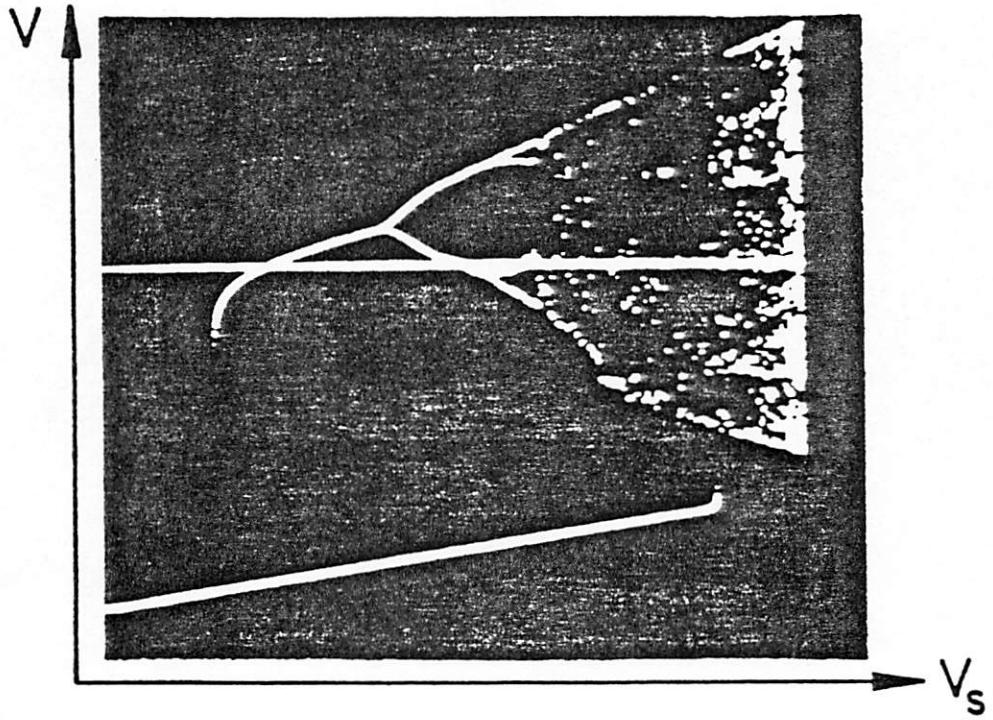


Figure 2

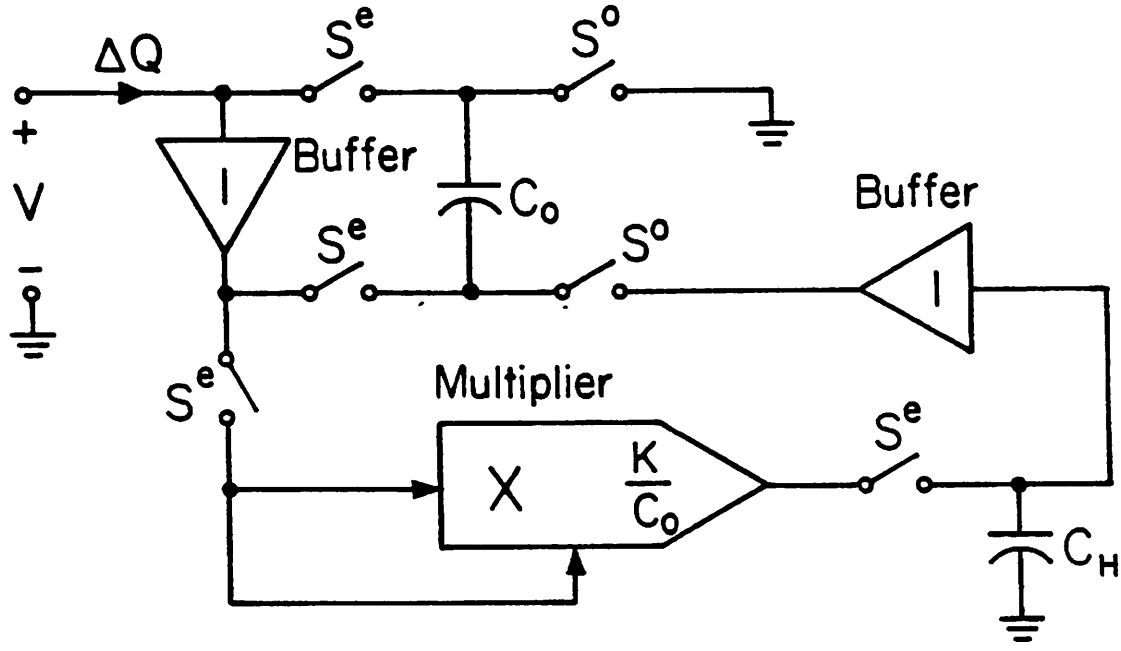
ΔQ
$S^e$
$S^o$
+
V
−
Buffer
1
$C_o$
$S^e$
$S^o$
Buffer
1
$S^e$
Multiplier
X
$\frac{K}{C_o}$
$S^e$
$C_H$

Figure 3