PRECISION ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERSION USING REFERENCE RECIRCULATING ALGORITHMIC ARCHITECHTURES

by

Cheng-Chung Shih

Memorandum No. UCB/ERL M85/60

25 July 1985

PRECISION ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERSION USING REFERENCE RECIRCULATING ALGORITHMIC ARCHITECHTURES

by

Cheng-Chung Shih

Memorandum No. UCB/ERL M85/60

25 July 1985

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

PRECISION ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERSION USING REFERENCE RECIRCULATING ALGORITHMIC ARCHITECHTURES

by

Cheng-Chung Shih

Memorandum No. UCB/ERL M85/60

25 July 1985

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Precision Analog to Digital and Digital to Analog Conversion Using Reference Recirculating Algorithmic Architechtures

Ph. D. Cheng-Chung Shih Department of EECS

Paul Russell Gray

Chairman of Committee

Abstract

In recent years, complicated and powerful digital signal processors have been implemented as a single integrated circuit. Because of the advantage of noise immunity and process insensitivity in digital processing, there is a trend toward having more signal processing done in digital form instead of in analog form. However, a major obstacle in the transition to digital processing is the expensive high resolution analog to digital converter and the digital to analog converter required before and after the digital processing.

In this thesis, a new method of cyclic analog to digital (A/D) and digital to analog (D/A) conversion using switched capacitor techniques is described. By periodically modifying the reference voltage to compensate for the non-ideal signal transfer loop gain in alogorithmic converters, it is possible to realize analog-digital and digital-analog converters whose linearity is independent of component ratios and which occupy only a small die area. These converters require only two moderate-gain MOS operational amplifiers , one comparator, and a few capacitors. Two test chips for A/D and D/A conversion were built. The test data shows that the experimental A/D performs as a monotonic 13 bit converter with maximum 1 LSB differential and 2 LSB integral nonlinearity.

ACKNOWLEDGEMENTS

I like to express my deepest thanks to Professor Paul. R. Gray for his thoughtful guidance and support throughout the course of my research work. Without his encouragement, the success of this work would have never been possible.

I am also very grateful to Professors David G. Messerschmitt, Robert W. Brodersen and David A. Hodges for the helpful advice they each gave me.

Discussions with many of the fellow students in the Department of EECS are greatly appreciated.

Special thanks to Stuart Siu for constructing the control board for the D/A and testing the D/A and to Steve Lewis for his careful correcting of the draft of this dissertation.

This work was supported by the National Science Foundation under Grant ECS-8023872, State of California MICRO program, Racal-Vadic Corporation, Fairchild Semiconductor, and GTE-Lenkurt Corporation.

DEDICATIONS

My wife, Jill De-Kuang constantly gave me her love and understanding throughout the duration of my graduate study. Without her support and encouragement, this Ph.D. work would not have been possible.

I also want to express my deepest thanks to my parents, Mon-Wang and Fu-Chu Shih for their patient guidance, sacrificed and support throughout my life time.

This dissertation is dedicated to my wife and my parents.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

Integrated circuit technology has changed dramatically in the past few years. One result of this change is that more and more transistors can be put into a single integrated circuit. In fact, about half a million transistors have been successfully fabricated into a commercial product[Beye81]. Although advances in process technology have made both digital and analog integrated circuits more compact and faster than ten years ago, digital IC's have shown especially significant improvement. This fact encourages the use of more digital and less analog circuits.

However, since real signals of interest exist in the form of continuous analog waveforms, in order to perform any digital signal processing(DSP), every analog signal sample must be transformed into a digital word before any digital manipulation can occur. Likewise after digital processing, every digital word has to be transformed back into an analog signal sample in order to interface with the analog world. It is therefore clear that in the more and more popular digital signal processing environment, analog to digital converters (A/D) and digital to analog (D/A) converters are two essential parts of the DSP system.

In the past, one of the major deterrents of using digital processing is that the overhead of the transformation between analog and digital waveforms is large. No matter what the digital processor's function is, this transformation is a necessary step before any discrete processing. The overall process accuracy is directly limited by the front end conversion accuracy, especially when high precision is needed in the processing. On the other hand, using direct analog signal processing, infinite precision is ideally possible; furthermore, no complex, high precision analog/digital conversion is needed. Of

course, many benefits are derived by changing to digital systems. For example, the deterioration of the signal during the processing is minimized and the storage of information is simplified. From an IC implementation point of view, the digital circuit needs a reduced accuracy requirement and is able to take full advantage of the process shrinking which in the future may be translated into less chip area and less process dependence and higher yield than is now possible.

When a digital processor is used to handle a great deal of complicated jobs, the overhead of the A/D and D/A converters becomes less significant. During the past few years, the digital signal processing of speech waveforms has been carefully studied. However, due to differing technology requirements for analog and digital circuits and to projected area requirements for one combined analog and digital circuit, most of these systems have used 2 chips, one for the A/D and D/A, the other for the DSP circuits. In the few reported cases for which an on chip analog/digital converter have been used, the converter took almost the same amount of die area as the main digital system.

The objective of this research is to study a low cost converter technique for speech signal band processing which is process insensitive and amenable to CMOS technology. CMOS technology is presently, the most pervasive digital process because of its low power consumption and high density. Such a converter will reduce the overhead of the digital system and lower the cost of the digital signal processing chip dramatically. Another objective of this research is to design the converter so that its area can scale down along with the area of the digital circuits as the process technology improves. Since the algorithmic converter using the reference refreshing approach investigated in this research only needs two operational amplifiers, one comparator and a few picrofarads of capacitance, the die area can be relatively small compared with other type of converters. When this converter is integrated along with a digital system, it only occupies a small part of the chip. Most importantly, it can shrink along with the

digital system as the technology improves without degrading the performance of the converter.

The second chapter covers some important terminologies used in describing a converter and some basic implementation methods of A/D and D/A conversion methods, and discusses the tradeoffs between speed and chip area and some inherent characteristics of each converter type. A cyclic conversion method which is used in this study is explored in detail and a new technique which modifies the cyclic conversion method by refreshing the reference voltage each cycle along with the signal is investigated in the third chapter. Using the reference refreshing technique, all the first order gain errors including capacitor mismatch and error due to the finite gain of the operational amplifier can be corrected. Chapter 4 deals with the other nonideal errors in the integrated circuit and points out a solution for each one of them. In the fifth chapter, the detailed circuit implementation and design considerations of the operational amplifier and comparator are discussed. The external logic design of the control system is described in chapter six. The seventh chapter presents the experimental results of the new reference refreshing A/D and D/A. Conclusions are presented in Chapter 8.

CHAPTER 2

MONOLITHIC CONVERSION TECHNIQUES

In this chapter, the characterization of monolithic A/D conversion techniques is discussed in depth. In section 2.1, the fundamentals of the A/D conversion process are explained. In section 2.2, many kinds of errors and terminologies associated with A/D converters are summarized. Section 2.3 presents the most popular A/D techniques used in present IC design and shows the characteristics and some examples applications of each method.

2.1. Fundamental of A/D Conversion

Basically, a A/D converter composes a sampler which samples and holds the input signal for further processing and a quantizer which encodes a continuous analog signal into a digital representation with a finite number of bits. The digital output of the converter is N binary bits where $b_1, b_2, \cdots, b_N$ are the binary bit coefficients having a value of either a 1 or a 0. Unavoidably, there is a difference (ϵ) between the finite digital approximation and the actual infinite resolution input signal V_{in}.

$$V_{in} = V_{fs}\left(\frac{b_1}{2^1}+\frac{b_2}{2^2}+\ldots+\frac{b_N}{2^N}\right)+\epsilon \qquad (2.1)$$

The digitized bit coefficients of the analog input signal are obtained from the A/D output, either simultaneously in the parallel form or serially with one bit at a time.

Since there are infinitely many possible analog inputs and only a finite number of possible digital outputs, it is clear that there is not a one to one correspondence between analog inputs and digital outputs. Instead, the output is a quantized version of the analog input. As a result, each output code corresponds to a small range of analog input value; therefore, the analog input suffers an error in the conversion process (ϵ in Eq 2.1

) . The smallest quantization step, Δ between the discrete output levels corresponds the one least significant bit (LSB). The maximum resolution of the A/D is limited by this step size because all inputs falling between adjacent analog transition points will be represented by the same output code. The converter's *dynamic range* is the ratio of the largest to the smallest analog signals that it can handle. Since the largest signal is equal to full scale input V_{fs}, the dynamic range can be expressed as

$$Dynamic\ range = \frac{V_{fs}}{\Delta} \tag{2.2}$$

For a linear A/D, the dynamic range can be easily determined by the bit number of the converter. From equation 2.2, the dynamic range in dB for a N-bit A/D is 20*N*log2. But in the case of companded codec, it is primarily determined by the smallest and largest resolvable input signal. The 8 bit μ-law coder has the dynamic range about 80dB in stead of 50dB.

For illustrative purposes, two possible idea transfer characteristics of a simple 3 bit A/D converter are shown in figure 2.1. Both transfer characteristics resemble stair cases with steps at the analog transition points. Also, both curves are drawn so that they are symmetric about the x and y axes. The difference between the two depends on whether the origin intersects the curve on a rise between steps or on the tread of a step. In figure 2.1a, the intersection occurs in the middle of a vertical segment rising between 2 output codes; hence this is called a mid-riser transfer curve. For it, zero is a transition voltage, and half of the 2^N digital output codes are on each side of the zero transition . On the other hand, shown in figure 2.1b is an example of a mid-tread transfer curve, so named because it intersects the origin in the middle of the tread representing the digital code for zero volts input. For a mid-tread case, only 2^N-1 digital codes are used. Note that all the definitions and characteristics discussed above apply to any A/D converter, irrespective of the bit count.

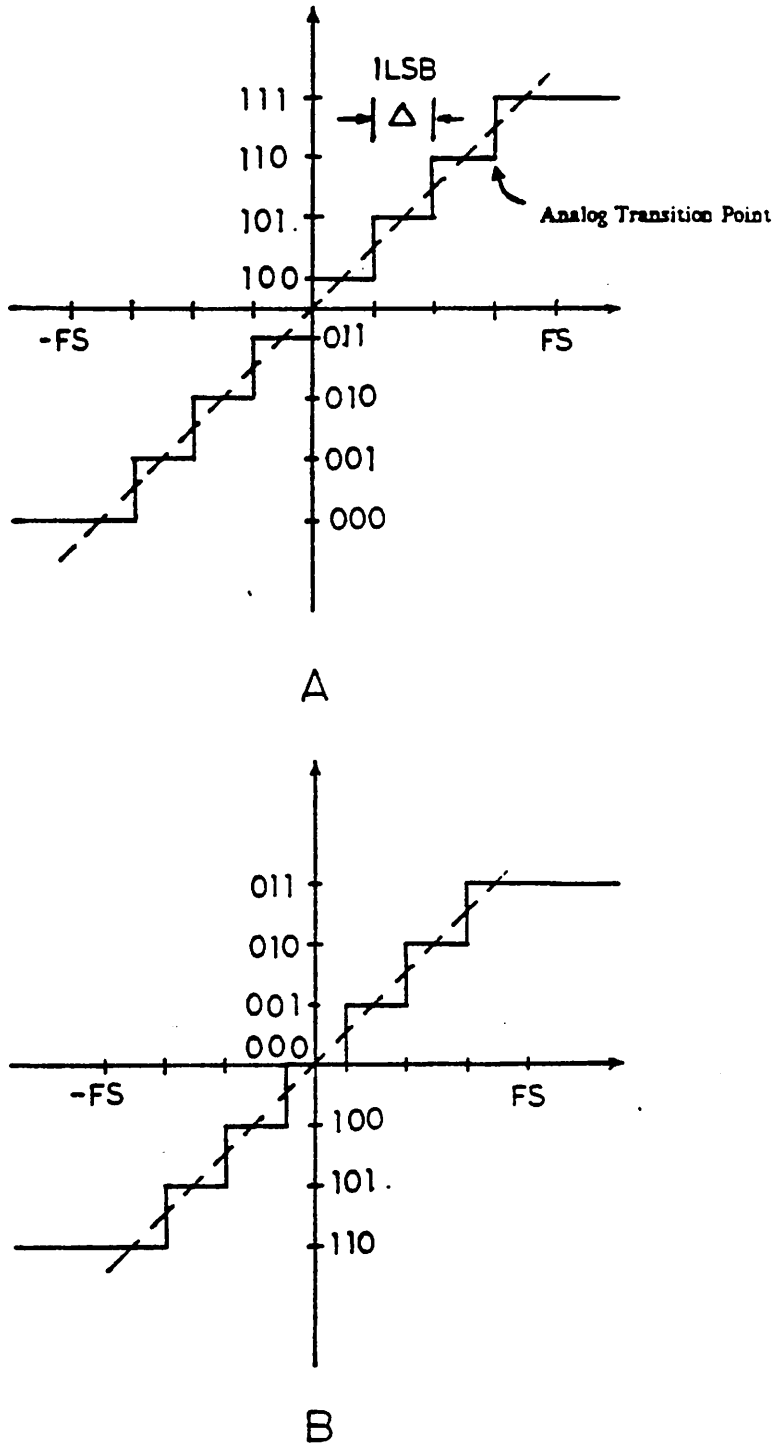


Fig 2.1 The ideal 3 bit A/D transfer curve (a) mid-rise case and (b) mid-tread case

2.2. Characterization of Converters

A/D converter's characterization is best described by referring to the converter's transfer curve. The transfer function clearly describes each transition point of the input signal corresponding to each output code change. The analog transition is usually called the quantization bandedge which assuming 50% probability for input signal to be represented by either adjacent digital code.

2.2.1. Quantization error

Quantization error is the fundamental, irreducible error associated with the effect of encoding a continuous(analog) signal into a finite number of digital bits. A 12 bit A/D, for example, can represent an input voltage to a minimum uncertainty of 1 part of 2^{12}. In order to analyze the quantization effect, it is convenient and useful to assume a simple statistical model for the quantization noise. Assume the input to be a sinusoid with peak amplitude adjusted so that the largest level is just excited. The signal to quantizing noise in dB units for a N bit converter[Mess].

$$SNR(dB) = 6N + 1.8 \tag{2.3}$$

For a random input with normal distribution $(0,\sigma)$ $.4\sigma$ as the overload for the converter, the signal to quantization noise ration in dB,

$$SNR(dB) = 6N - 7.2 \tag{2.4}$$

Both equation 2.3 and 2.4, which state that each bit in the code word contributes 6 dB to the signal to noise ratio, are valid subject to the following assumptions. The input signal has to change in a complicated manner so that the noise sequence behaves like a statistical model[Rabi78]. The quantization step size is small enough with respect to the signal to ensure that there is no correlation between each quantization error. Generally both assumptions are true when the signal is sampled above the Nyquist rate and a 6-bit or higher converter is used.

2.2.2. Differential Nonlinearity

The definition of differential nonlinearity is how much the actual quantization step width varies from the ideal step width of 1 LSB. Fig 2.2 shows a differential nonlinearity of X-1 LSB where the actual step width is X LSB. Although some small and localized differential nonlinearities may be insignificant for large signal, differential nonlinearity is important in many applications, since it gives the resolution of a converter. Because, if a small signal superimposes on an large signal and happens to fall into that region with this differential nonlinearity error, then the accuracy of the A/D conversion of the small signal is bad. On the other hand, there are some applications where the differential nonlinearity for large signal is of no importance. For example, the companded coding method.[Mess] intentionally distorts the transfer function in order to reduce the number of bit required in the digital representation.

2.2.3. Missing Codes

In some nonideal A/D transfer curve, some of the digital codes never appear at the output no metter what is the input signal. Fig 2.2 points out two missed codes in the transfer function. Missing codes represent a special kind of differential nonlinearity. For the missing code, the effective quantization step width is 0 LSB, which results in a differential nonlinearity of -1 LSB. The problem of missing codes generally caused by a non-monotonic conversion relationship on the part of the internal D/A converter. When the internal D/A is nonmonotonic, some digital codes will never be used as the decode output because they probably generate the same analog output to the internal comparator. In some control systems, a missing code error is not tolerable because it will sometimes cause system instability.

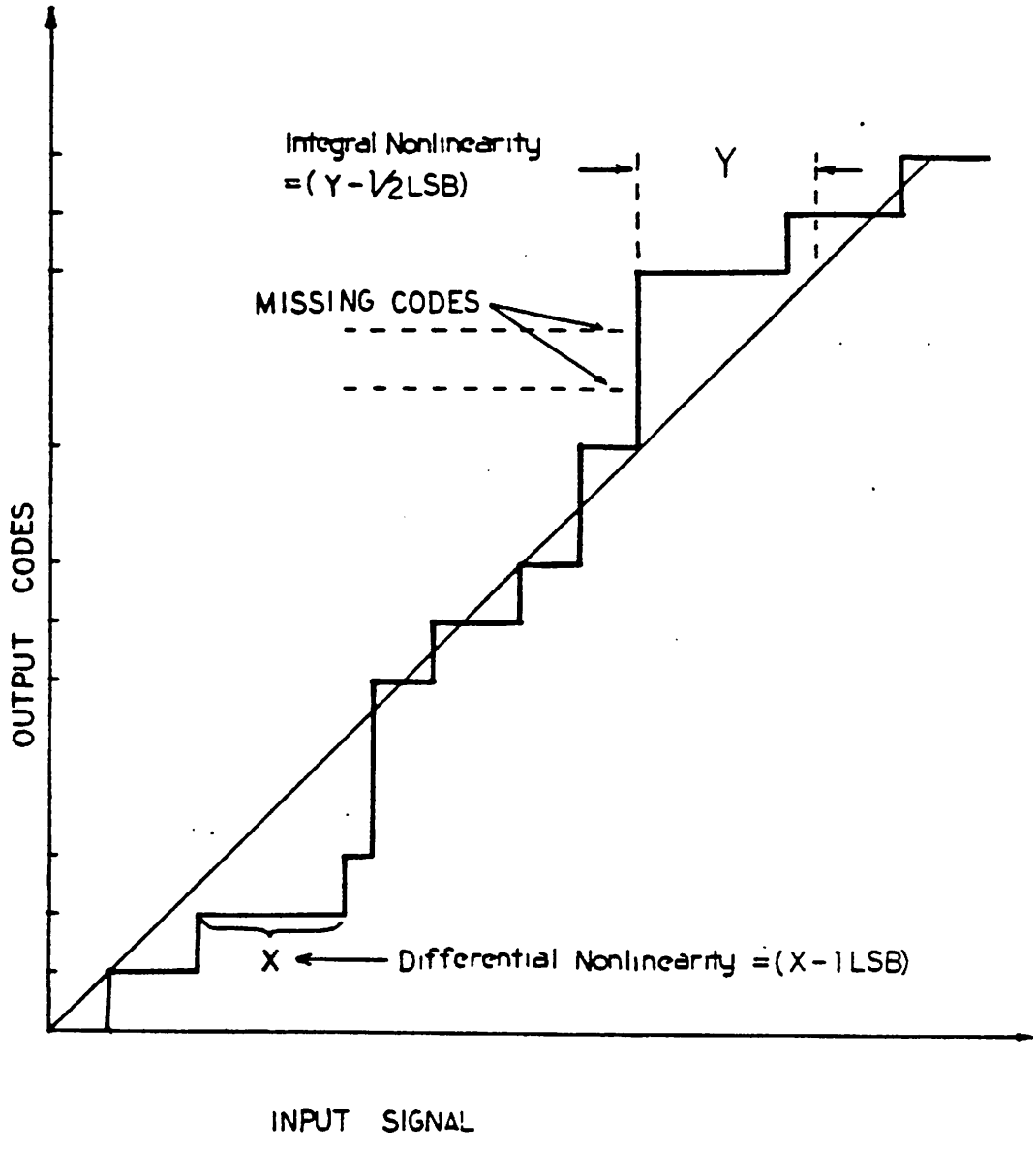


Fig 2.2 A nonideal transfer curve demonstrated differential. integral nonlinearity and missing codes error.

2.2.4. Offset Error

The offset error is defined as the amount by which the actual code center line missed the origin of the transfer characteristics. The code center line is a hypothetical line which connects the center points of each of the code transitions. The offset error affects all codes by the same additive amount(Fig 2.3a) and thus can be modeled as an offset preceding an ideal converter.

2.2.5. Gain Error

The gain error sometime called scale factor is defined as the slope difference of the actual and the ideal code center lines(Fig 2.3b). It affects all codes by the same percentage amount so that the input signal gets amplified be a factor not exactly one and thus can be modeled as a gain preceding an ideal converter.

2.2.6. Integral Nonlinearity

Integral nonlinearity is the maximum deviation of the actual A/D transfer function from a best fit straight line. Before the evaluation of the integral nonlinearity of the A/D, the gain and offset errors have to be excluded. Integral nonlinearity in an A/D is generally worse when digitizing full scale signals or signal level in the middle range of the transfer function than low level signals where the transfer function is relative linear. Figure 2.2 shows an integral nonlinearity error of $Y-\frac{1}{2}$ LSB. In many communication systems, the integral nonlinearity is less important than the differential nonlinearity.

2.2.7. Monotonicity

Monotonicity by definition requires that the internal D/A of an A/D converter always generates an increasing (magnitude) analog output value for increasing digital code. Non-monotonicity can only occur if the differential nonlinearity is equal or larger

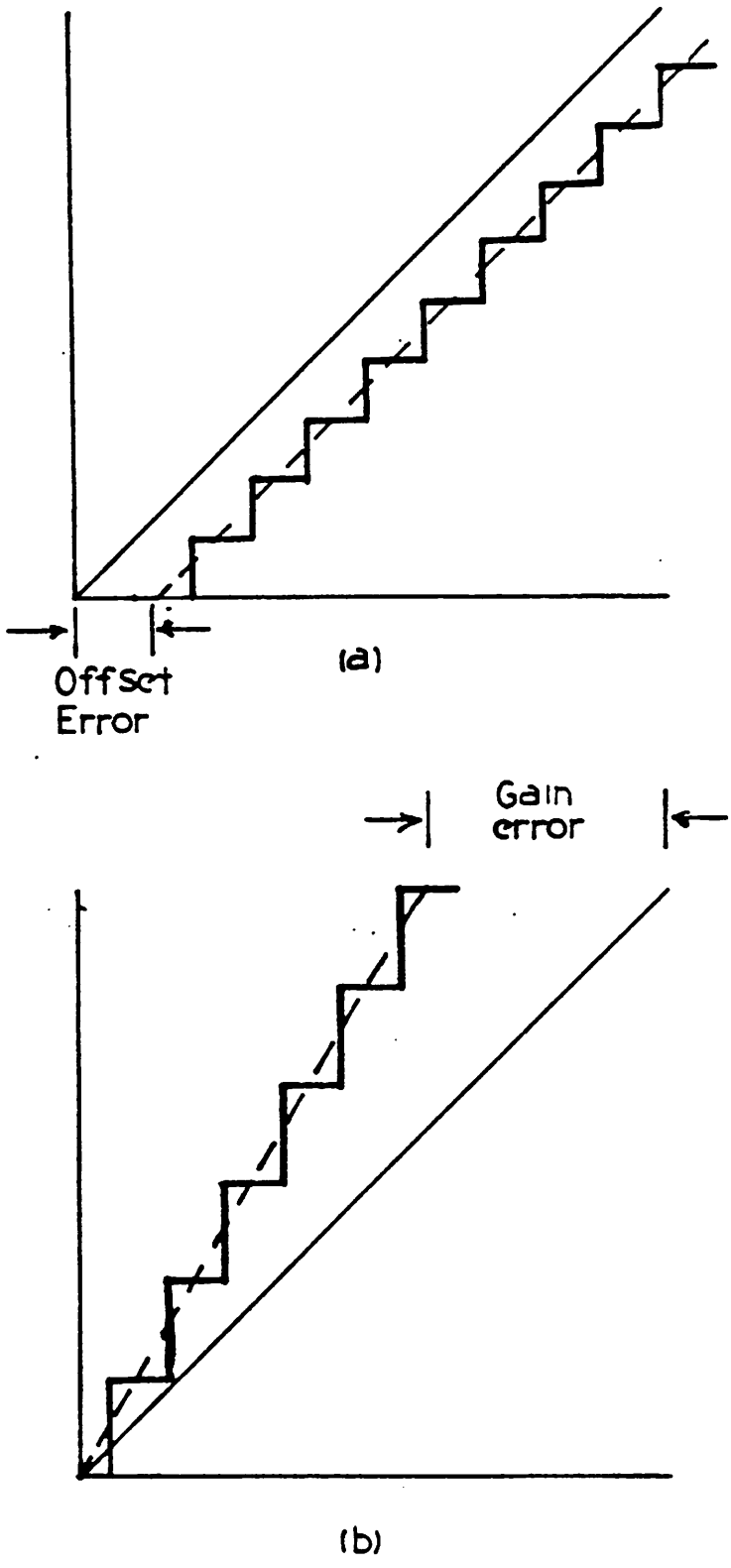


Fig 2.3 Quantization characteristics of linear A/D converter (a) Offset error (b) Gain error

than 1 LSB. Notice that a converter which has a differential nonlinearity specification of ±1/2 LSB maximum is always more tightly specified than one which is only guaranteed to be monotonic. In some control systems application, however, the differential nonlinearity is not a major concern as long as the converter is monotonic. When the terminology of monotonicity is used in the specification of an A/D, it usually means the A/D is without any missing code or any dip in the transfer function.

2.2.8. Signal to Noise Ratio

One important measurement for communication system performance is the signal to noise ratio(SNR). Although it is not always the most accurate standard by which to compare one system's performance with that of another system, the SNR is the most objective and reproducible way of measurement. The A/D converter can be tested by a distortion analyzer with the set up as Fig 2.4. For an ideal 13-bit A/D, the SNR versus input signal level is shown in Fig 2.5. Since the quantization noise is determined by the step size of the converter, the signal to quantization noise ratio improves linearly with the input signal level. When the signal is smaller than the smallest step size of the converter or when the signal overloads the converter, the quantization noise statistical model will break down. Instead of following the straight line, the SNR drops quickly in those regions. Furthermore, any nonlinearity or distortion of the ADC will cause the SNR vs. input to not follow the ideal straight line. In speech systems, the requirements for an coder-decoder is different from those for a general linear converter. Although speech systems need high dynamic range converters because of the large speech level variation, the resolution for large input signals does not have to be as good as that for small input signal. For example, a μ-law converter needs the equivalent SNR of a 13-bit A/D when the input magnitude is small but only that of a 7 bit A/D for large signals. The ideal μ-law and A-law SNR versus input signal level is also shown in Fig 2.5. The speech quality after the conversion of these kinds of codec is well acceptable

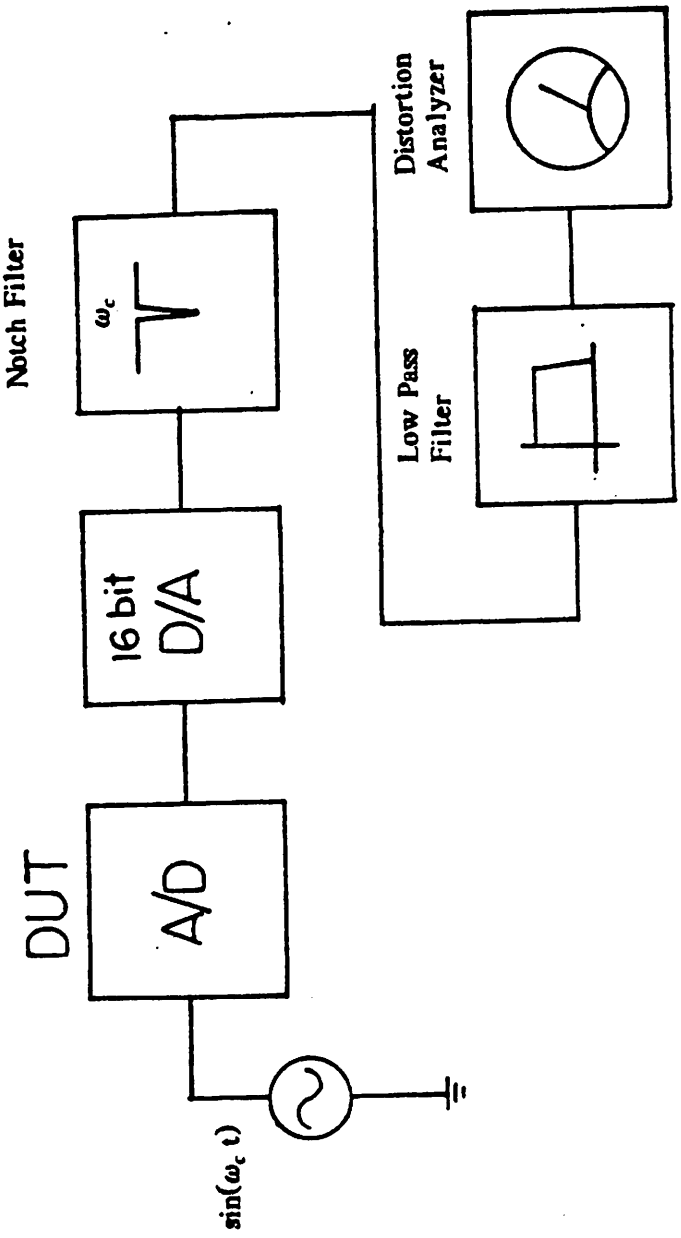


Fig 2.4 The test setup for SNR measurement with sinusoid input

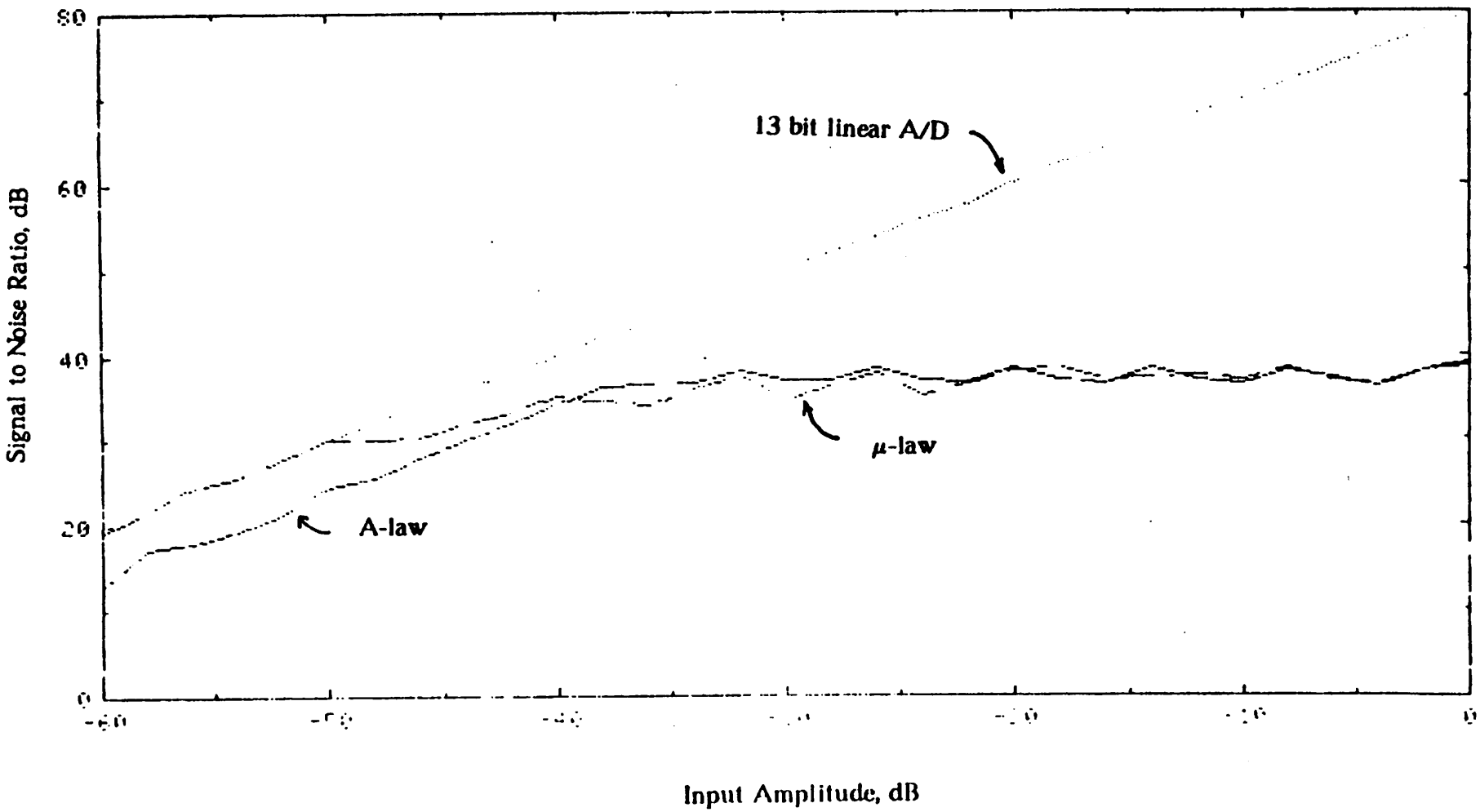


Fig 2.5 The SNR versus input signal level diagram with 13-bit linear A/D, μ-law converter, A-law converter

by the human's ear.

2.3. A/D Conversion Techniques' Characteristic and Applications

2.3.1. Integrating-type A/D Converters

Integrating A/D converters first generate a pulse whose width is propositional to the input signal voltage(V_{in}). The duration of the timing pulse is then measured by the combination of a stable reference clock and a counter by counting the number of input cycles from the beginning to the end of the pulse. From the above processes, the counter transforms the input signal amplitude into digital output.

In practice, the two most popular circuit techniques used are the single-slope and the dual-slope integration methods. The functional block diagram and the timing waveform of a single slope converter is shown in Fig 2.6. Before the start of the conversion cycle, the switch SW_1 across the integrating operational amplifier A_1 is closed, and the integrator output is clamped to zero. At the beginning of the conversion cycle, the counter starts to count the clock pulses, while at the same time, SW_1 is opened, and the integrator output ramps in the positive direction with a slope equal to $\frac{1}{R_1C_1}$. The counting of clocks continues until the integrator output level reaches the analog input level V_{in}. At this point, the comparator changes state and via an AND gate cuts off the clock signal going into the counter. The resulting count, n, in the counter is the digital approximation of the analog signal V_{in}. For an N bit A/D conversion

$$n = \frac{2^N}{V_{fs}} V_{in} \tag{2.5}$$

There are two basic drawbacks with the single ramp converter. First, the system accuracy relies strongly on the absolute value of the R_1C_1 product, which is difficult to control accurately. Second, the initial ramp startup point also affects the transfer curve

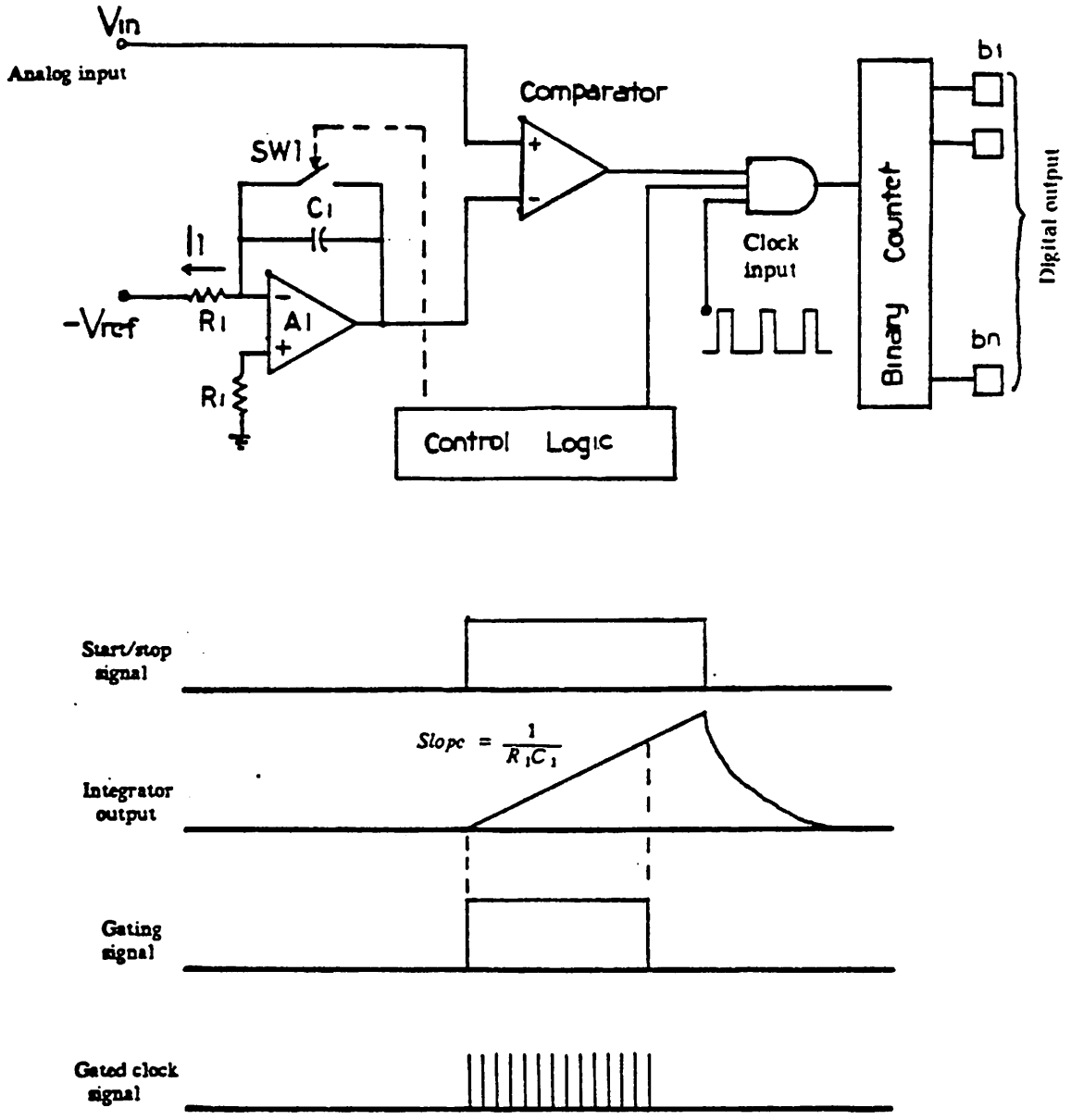


Fig 2.6 The block diagram of single slope integrated converter with some of the timing waveforms shown below.

of the actual single-slope converter. These problems are inherent in any single slope type converters; however, the dual slope conversion technique avoids these problems.

The dual-slope type converter is one of the most popular types of integrating A/D converters. Figure 2.7 shows the functional block diagram of a typical dual-slope converter. During the first phase, the system operates by integrating the unknown analog signal V_{in} for a fixed period of time, generally for 2^N clock cycles. The integrator output voltage V_x ramps up with the slope.

$$(\frac{dV_x}{dt})_I = \frac{+V_{in}}{R_1C_1} \tag{2.6}$$

During the second phase, the resulting integrator output level is then returned to zero, by integrating a known reference voltage of opposite polarity. The integrator output ramps down with the slope.

$$(\frac{dV_x}{dt})_{II} = \frac{-V_{ref}}{R_1C_1} \tag{2.7}$$

The length of time required for the integrator output to return to zero, as measured by the number of clock cycles gated into a counter, is proportional to the value of the input signal, averaged over the integration period. The dual-slope conversion accuracy is independent of both the value of the integrator time constant and the reference clock frequency accuracy, since these parameters affect the ramp up and down times equally. As long as their values remain stable during the integration cycle, these parameters' accuracy is of no importance. In this manner, long-term drifts due to time or temperature effects also are largely avoided.

Characteristics and Applications

From the above discussions, the basic characteristics of integrating A/D converters can be summarized as follows:

1. *Low Conversion Speed*. For different input voltage, the conversion time is not the same but the longest conversion time takes a total of 2^N clock cycles. Generally,

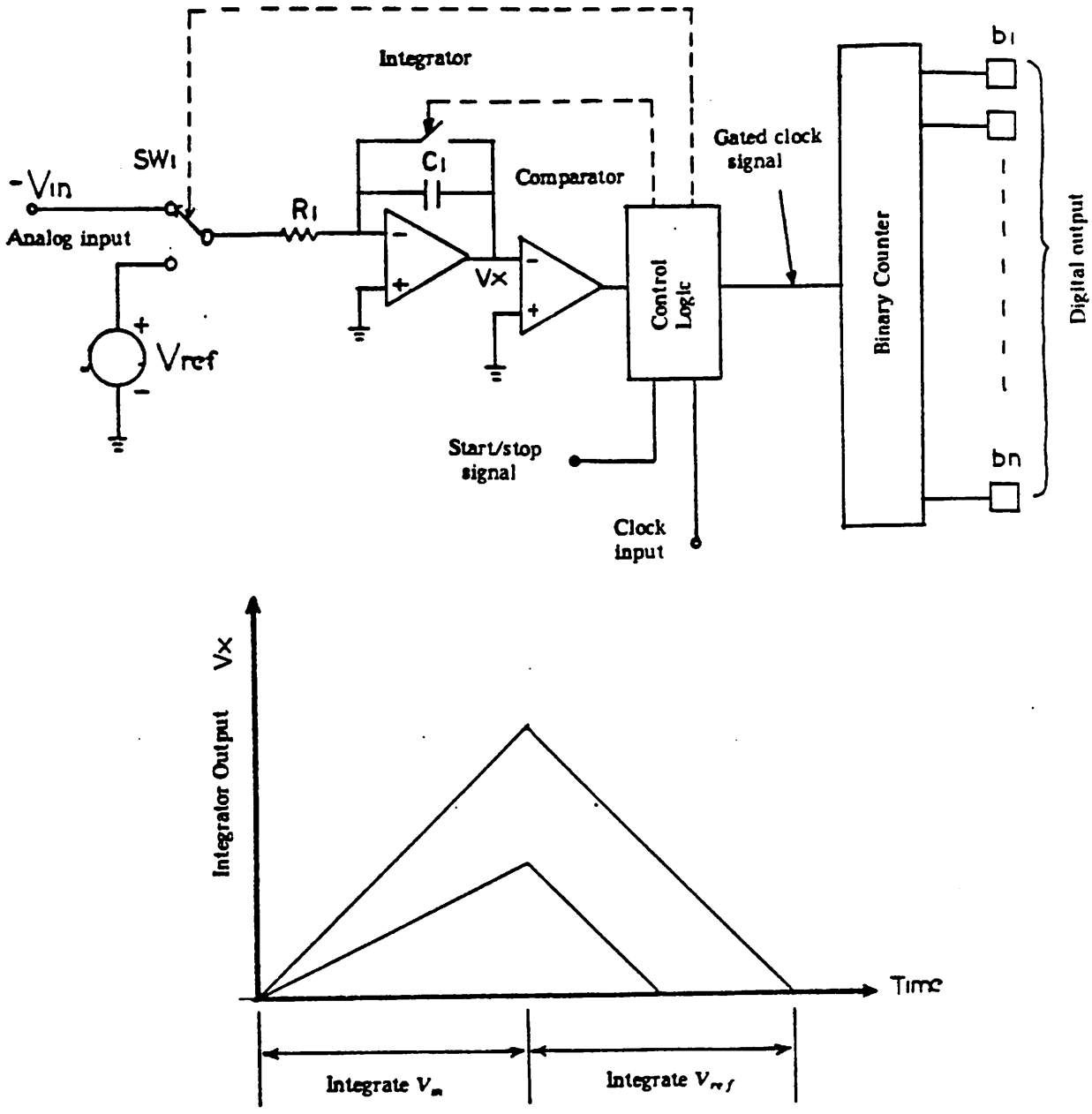


Fig 2.7 The block diagram of dual slope integrated converter and the waveform of V, for different input signal.

the conversion speed of the converter is limited by this critical time. For an 13 bit A/D with 2MHz internal clock, the conversion time will be approximately 4 msec.

2. *Intrinsically Produces No Missing Codes*. The digital output code is determined by the number of clock cycles accumulated in the counter during the timing pulse width. All digital codes between zero and full scale are possible to be present at the output.

3. *High Accuracy*. The offset voltage of operational amplifier and comparator circuits only affect the offset of the converter transfer curve not the differential nonlinearity. The linearity, determined primarily by the quality of the integrator ramp waveform, is excellent. Differential nonlinearity is virtually none existent since the analog function and the ramp waveform always remain continuous during the conversion process. If the ramp linearity and the resolution of the comparator are not the limiting factors, the accuracy of the integrating A/D can be improved by increasing the total number of clock cycles used per conversion. The comparator response time and the speed of the control logic give the upper limit for the maximum clock frequency that is allowed in the system. Beyond this point, in order to increase the total counts per conversion cycle, the ramp time must be increased which in turn sacrifices the conversion rate. Thus, in general, there is a trade off between the conversion rate and the resolution.

Integrating A/D converters are primarily suited for low cost, high accuracy and low speed measurements of slowly varying signals. Their prime areas of application are in digital panel meters and multimeters for which the accuracy is the major concern.

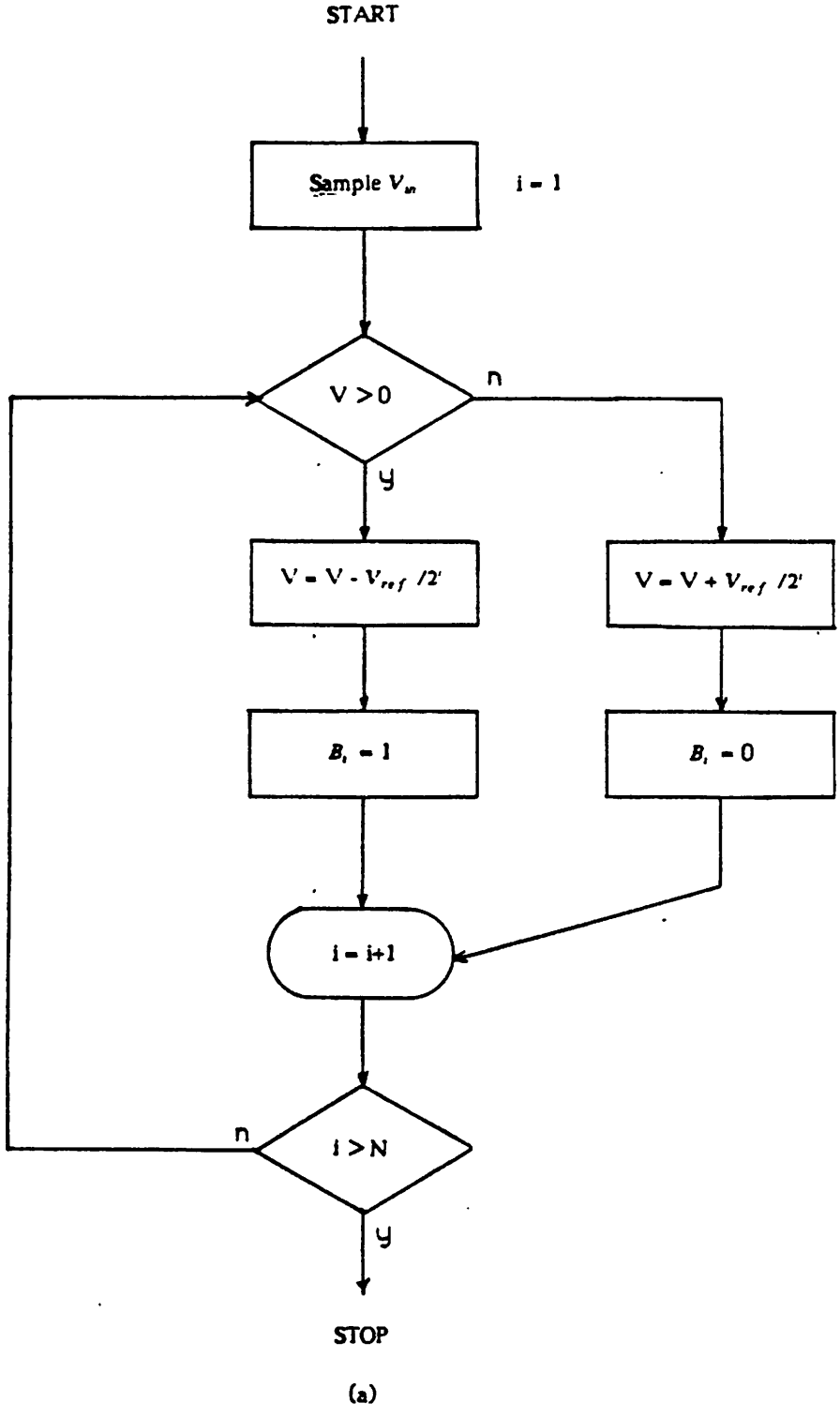
2.3.2. Successive Approximation A/D Converters

The N-step successive approximation technique is perhaps the most popular A/D conversion algorithm. The N-bit successive approximation converter encodes the input signal using N cycle times. Usually, the conversion starts with the most significant bit.

Each cycle, the converter divides the possible region, where the input signal might locate, into half and eliminate one of the regions after the decision. The converter gets about a factor of two closer to the real position of the input signal after each bit decision. Finally, after N cycles, the converter has decided which one of the possible 2^N slots contains the input. In general, there are two approachs to realize the algorithm. Figure 2.8a,b show the flow charts for both methods. The first algorithm compares the input with a successively divided reference and is used in most successive approximation converters. It requires the use of N-stages of binary weighted components for an N-bit conversion. The second algorithm employs a multiplied remainder scheme and is used in circuits which only need a few precision components. It, however, requires the use of an amplifier[McCh77].

A successive approximation A/D converter technique that has been used successfully is the weighted capacitor charge redistribution method. This technique, first introduced by McCreary and Gray[McCr75], typically uses binary-weighted capacitors to carry out a divided reference algorithm. An implementation of a MOS circuit of this type is shown in figure 2.9. Converter sampling is performed by connecting all of the capacitor bottom's plates to the input voltage and shorting the top plate to a fixed voltage, which is usually the comparator offset point in order to eliminate the comparator offset. Converter operation progresses by sequentially changing each capacitor's bottom plate to either V_{ref} or $-V_{ref}$ (starting with the largest capacitor) depending upon the sign of V_x. This sequence continues until all N capacitors have been tested, at the rate of one capacitor per internal cycle, for an N-bit plus sign conversion.

In order to achieve the resolution that is required, the matching of the capacitor array is very important. For an average maximum error of 1 LSB in the 7 bit case, $\frac{\sigma_c}{C}$ is approximately 4% [Blac80]. For even higher resolution, the matching requirement is more tight. The matching accuracy that can be achieved between two capacitors is



(a)

Fig 2.8 (a) The flow chart for successively divided reference algorithm

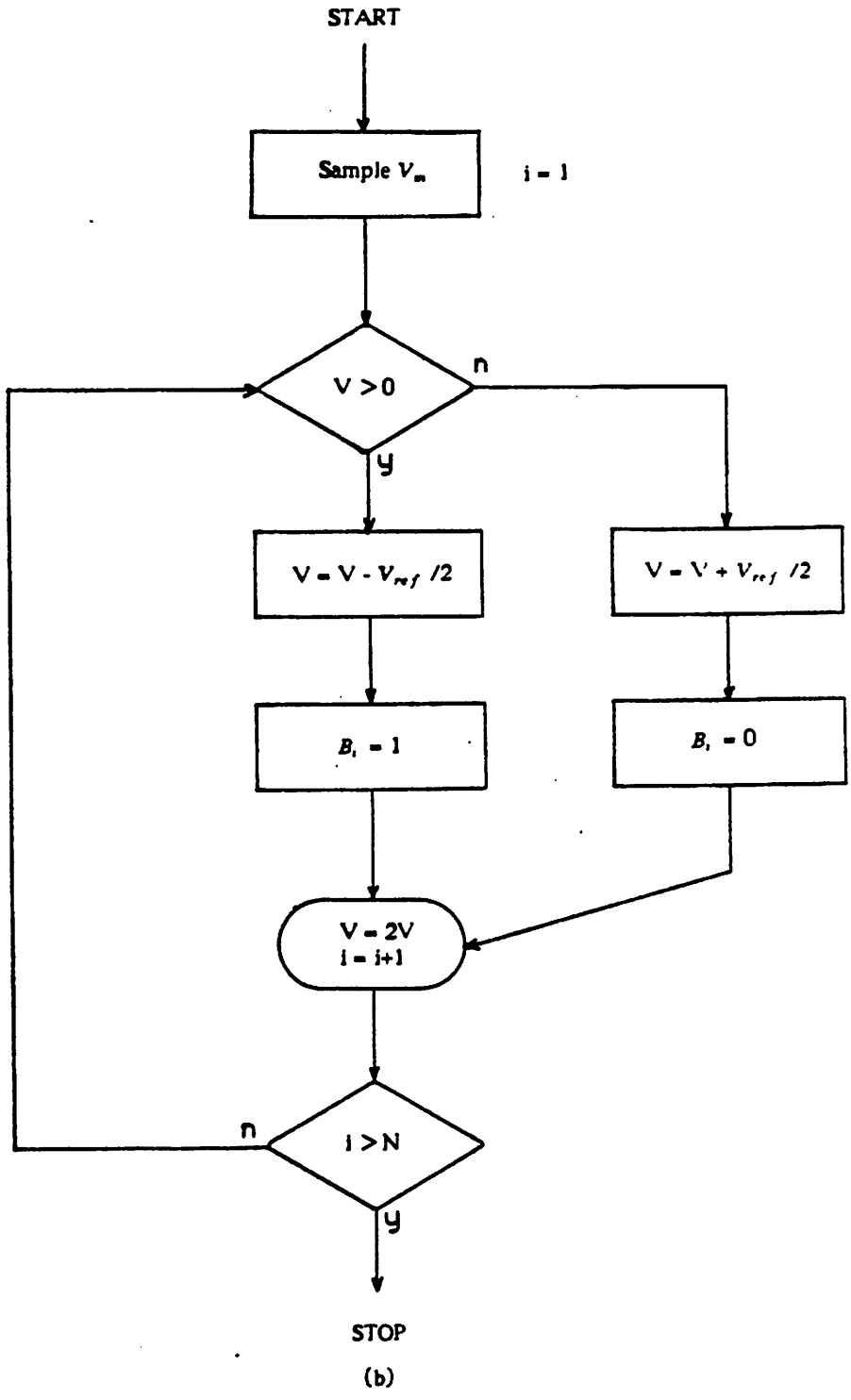


Fig 2.8 (b) The flow chart for multiplied remainder algorithm

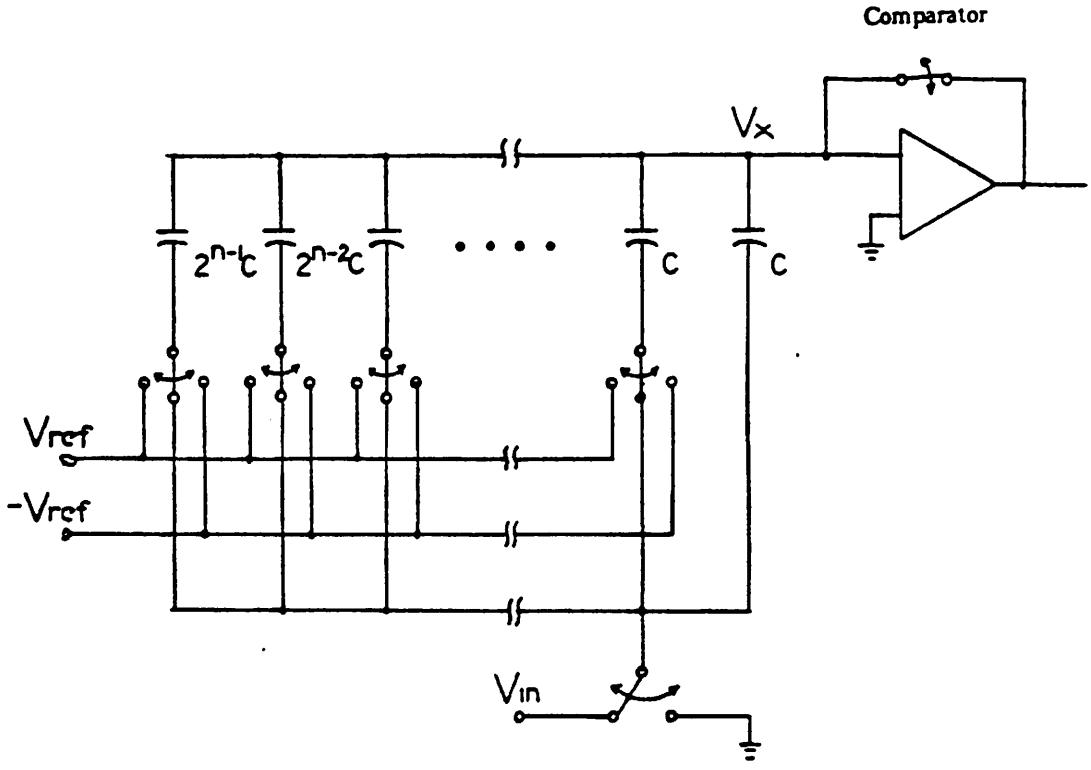


Fig 2.9 A complete circuit for weight-capacitor charge redistribution method

determined by the geometries of the capacitors. The matching between two capacitors is improved when larger geometry capacitors are used. This property sets the smallest capacitor unit that can be used when high matching accuracy is required in the converter. The speed limitation of real binary-weighted capacitor circuits, tends to be dominated by simple R-C time constants associated with the largest capacitors and the on resistance of the sampling transistor. Because of large capacitor array required, there is also an aperture uncertainty error when the input is not a DC signal. One way to reduce the main capacitor array size, which is quite effective in high resolution converters, is to use two sets of capacitor array as shown in figure 2.10[Tsiv76]. The main capacitor array is reduced from 2^{m+n} to 2^m, a factor of 2^n reduction. But the matching accuracy in the main capacitor array still must meet a N-bit requirement (not just m-bit), in order to produce a N-bit A/D.

The cyclic or algorithmic converter, which uses the multiplied remainder scheme, is shown in Figure 2.11. The input signal is compared to the half scale voltage each time. When the input is above half scale, the remainder after the subtraction of the half scale voltage is multiplied. Otherwise, the signal is multiplied without the subtraction. This converter only needs a few capacitors, two operational amplifier and a comparator. Because of the simplicity of this implementation, the die area is considerably smaller. The speed of this technique is limited by the speed of the operational amplifier. More detailed analysis of the algorithmic converter will be given in the next chapter.

Generally, the successive approximation A/D conversion speed goes down linearly with increasing resolution and not exponentially as for the serial technique. For high resolution converters, the successive approximation converter will be much faster than the integral converter.

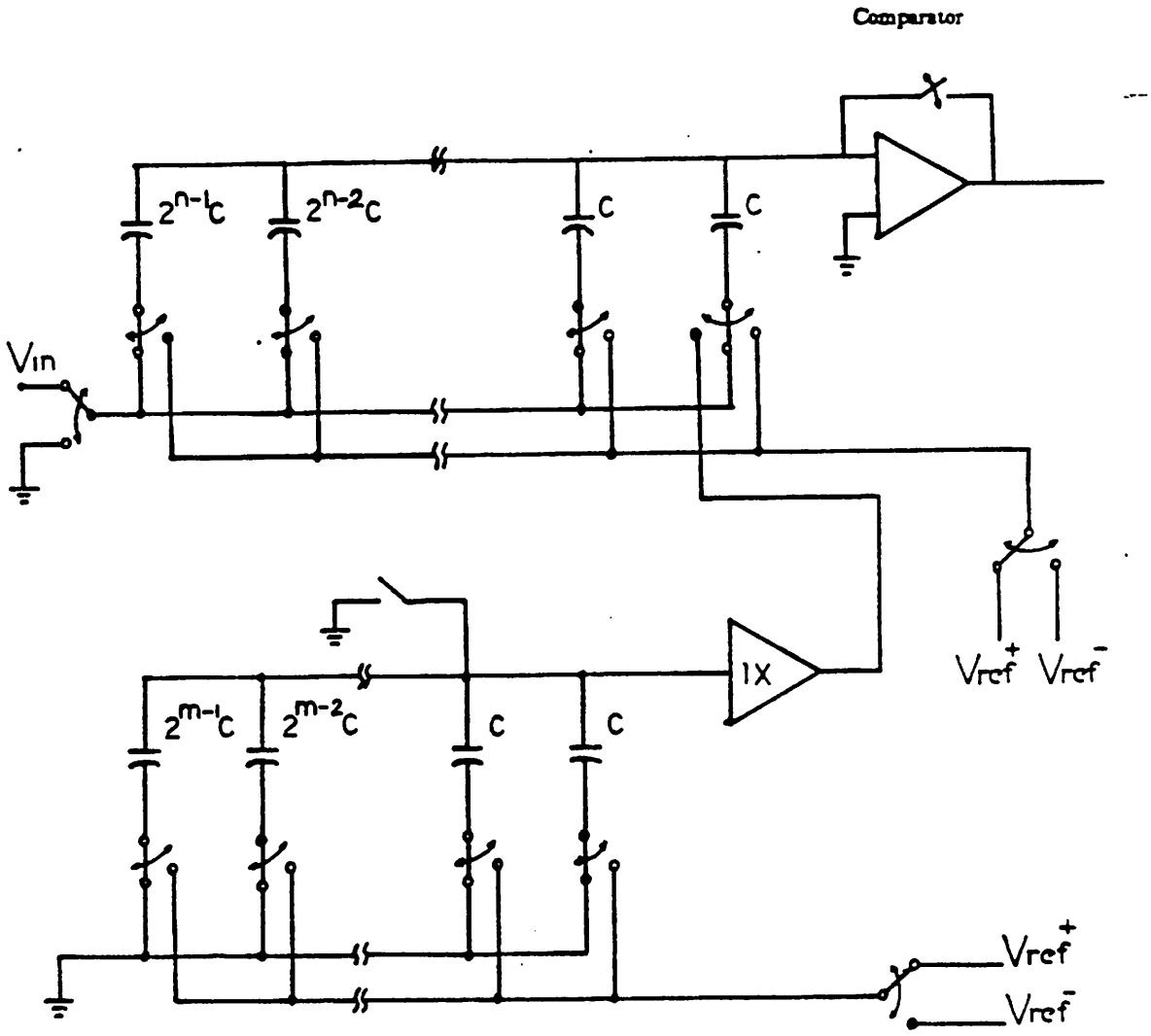


Fig 2.10 A two capacitor arrays implementation of the successive approximation algorithm

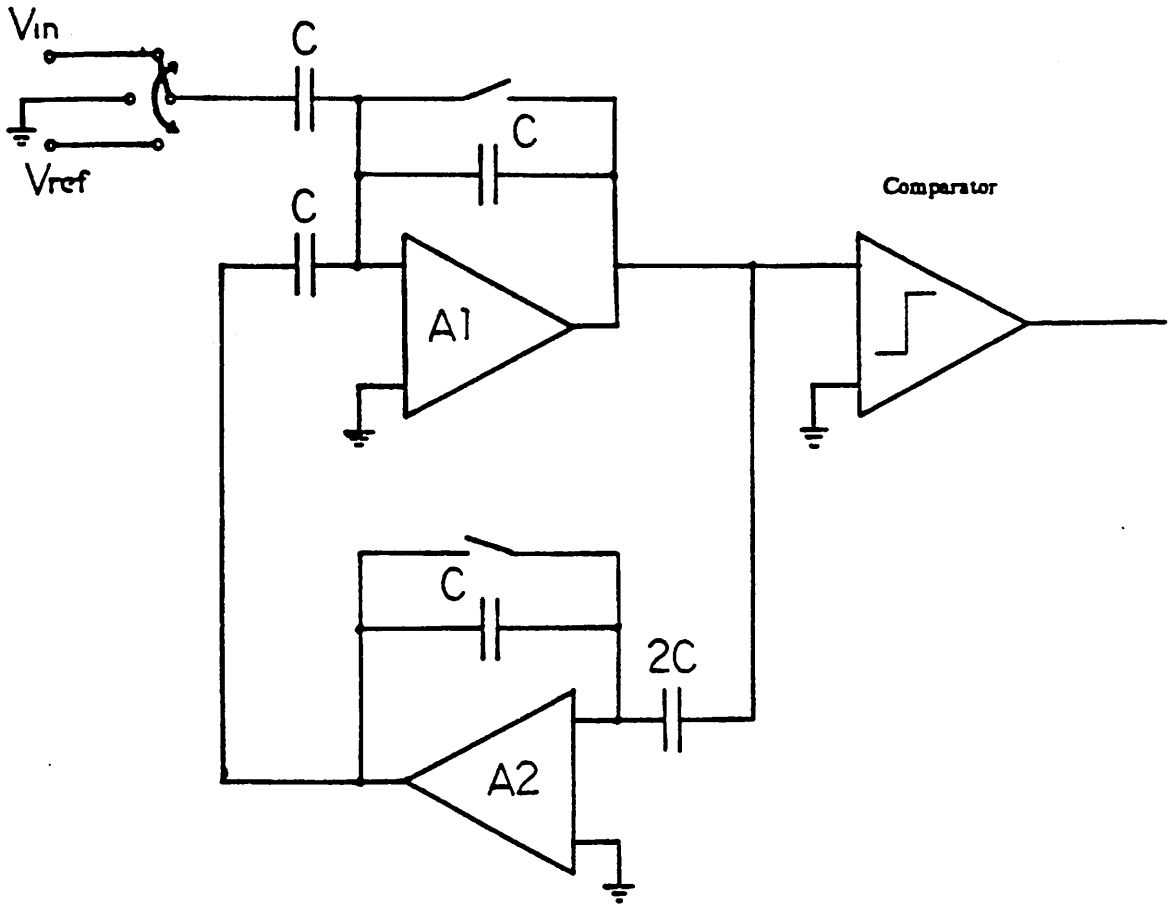


Fig 2.11 A simple switched capacitor cyclic conversion schematic

2.3.3. Pipeline A/D Converter

A common characteristic of the converter types previously presented, is that only a small part of the circuitry is "active" at any given time. A conversion algorithm which has a high utilization rate of its circuitry is desired. The idea of pipelined processing falls into this category. Generally, the pipeline process makes all of the circuitry work at the same time with all but the input process continuing the unfinished work from the previous processer. One approach is to modify the cyclic algorithm into the form presented in Figure 2.12. In this method distinct circuitry exists for each bit of the conversion process, but no bit cell is idle during any time cycle. This is accomplished by having each bit cell make the decision on a specific bit on a different portion of each clock period and synchronously passing the conversion remainder onto subsequent stages. For an N-bit converter, this results in an effective throughput of one conversion per clock cycle, but with a typically N period of decode time delay for each input sample. The comparator for each cell can be saved by properly opening the feedback loop of the operational amplifier and using it as the gain stage[Yiu].

Generally speaking, pipeline approach increases the conversion speed at the expense of added complexity. But with proper design, in order to speed up the conversion rate by a factor of N, the complexity is increased by a factor of less than N. There is a difficulty with this approach, however, particularly in high resolution converters, and that is the problem of achieving good isolation between bit cells without introducing too much distortion. Pipelined converters using switched capacitor implementation do not have this kind of coupling problem.

The throughput of the pipeline converter is N times faster than that of successive approximation converters, while the complexity increases at most linearly with the resolution unlike the case of parallel converters which will be discussed in the next section.

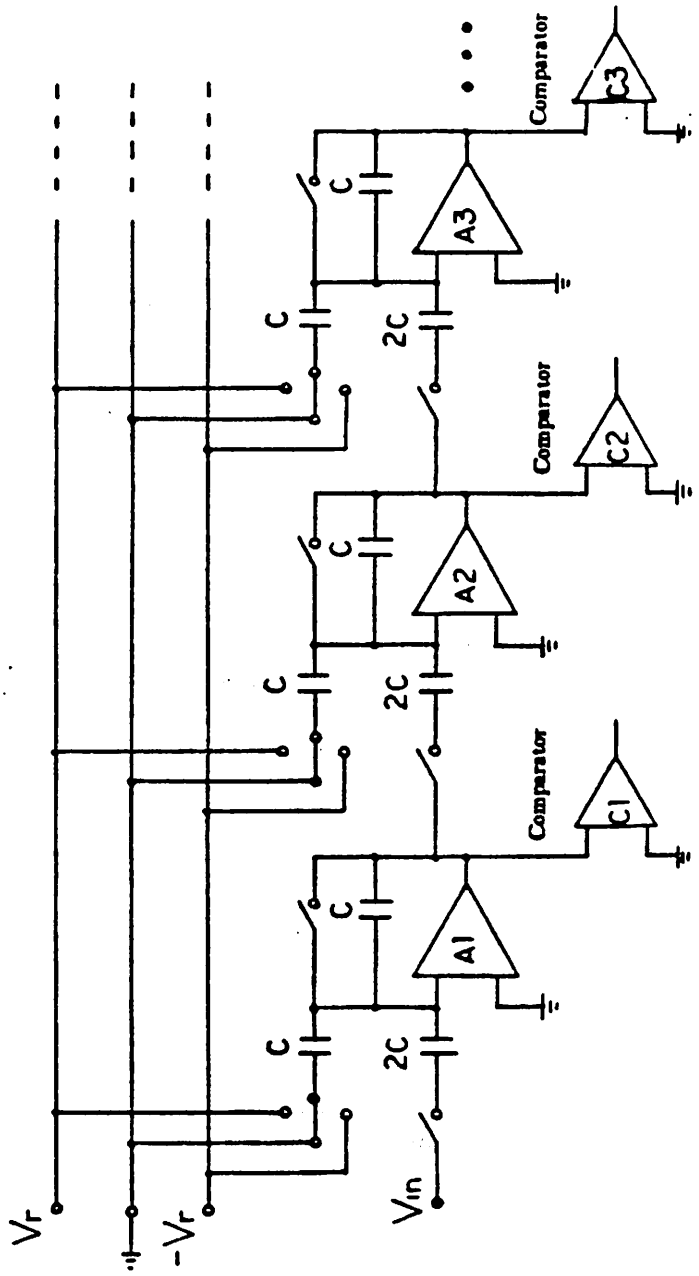


Fig 2.12 The cyclic pipeline schematic using multiplied remaider algorithm

2.3.4. Parallel A/D Converter

Parallel A/D conversion is inherently the fastest and conceptually the simplest conversion. The most straight forward way to implement the N bit parallel converter is to use 2^N-1 comparators and 2^N reference levels where the input signal is compared simultaneously with these reference levels. To figure out the exact level where the signal resides does not require any complicated clock sequence but only to perform 2^N-1 comparisons at the same time. Therefore, the entire encoding operation can be performed within one clock cycle. Because of this property, such converter systems are also called *flash encoders*. The digital code is generated by examining the output of the 2^N comparators. Figure 2.13 shows a block diagram of a parallel A/D converter system.

The system complexity increases very rapidly as the resolution of the parallel converter is increased. The chip area and the power dissipation requirements also grow exponentially with the increasing number of bits of the converter. The design and the layout of parallel converter circuits create problems when the resolution reach 6 bits or more. Recently, for high resolution converters, two-stage flash conversion is considered[Doer]. This sacrifices the speed by factor of two but prevents the exponential growth of the complexity.

When a resistor array is used for the generation of the reference, the resistor matching has to be better than 5% to make sure the converter differential nonlinearity no more than 1 LSB in an 7-bit resolution[Blac80]. The other practical error source is the comparator intrinsic offset whose requirement is actually coupled together with the matching requirement for the resistor array. Note in parallel conversion if the differential nonlinearity is greater than 1 LSB, a situation potentially much worse than a simple missing code may develop. A disallowed internal logic state will occur which may deadlock the conversion unless proper precautions have been made. This indicates

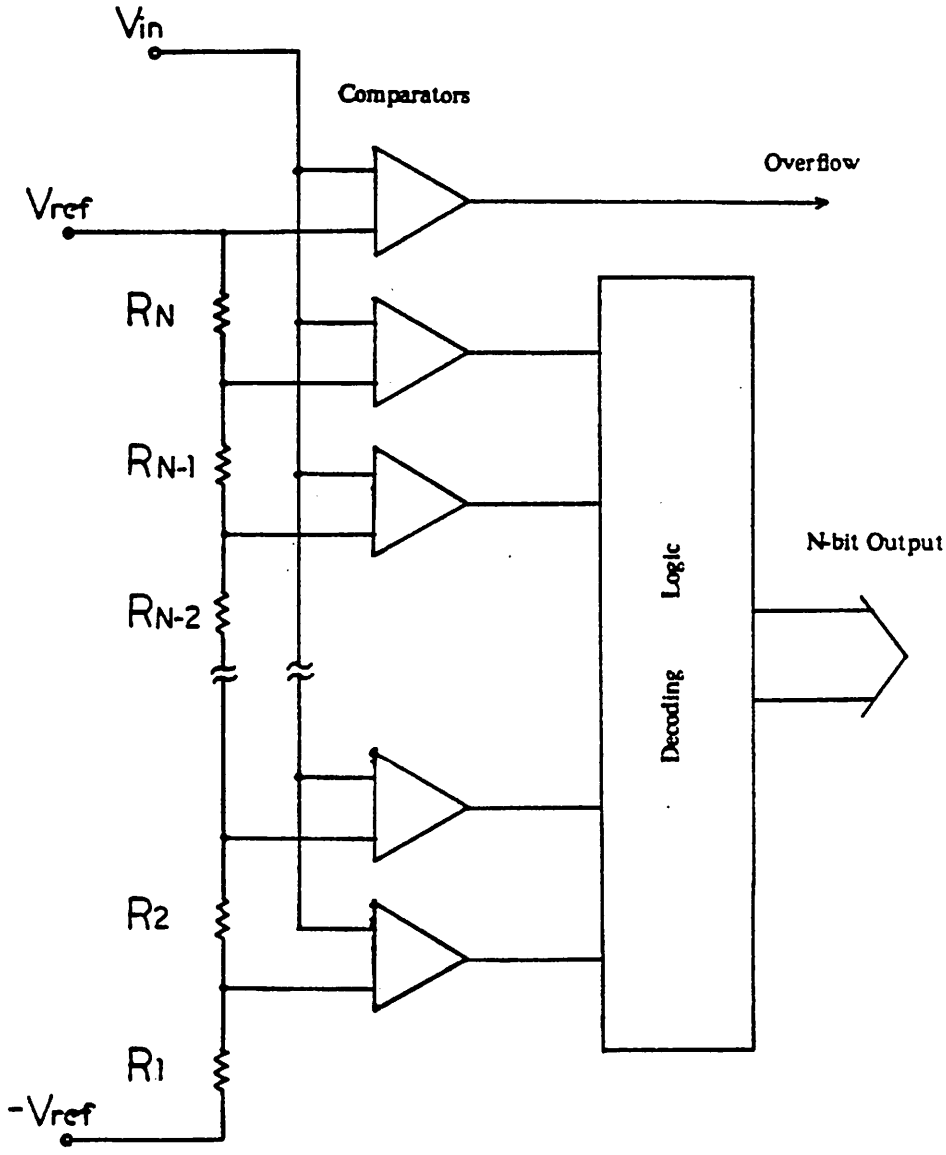


Fig 2.13 The parallel converter schematic

that tight control of the comparator offsets is necessary if good linearity is to be obtained with good yield.

The conversion rate of a flash converter is determined by the comparator speed which is usually faster than the operational amplifier settling time, which decides the cycle time of an algorithmic pipeline A/D.

2.3.5. Oversampled A/D converters

All the previous techniques perform an analog to digital conversion by first sampling the analog input signal then trying to find out which one of 2^N possible slots contains the input signal. Generally the previous approaches produce one digital output code per input sample. The analysis of these kind of converters can be separated into the sampling phase and the conversion phase. The input signal's distribution function has no effect on the converter's characteristic. Normally these converters should have the same performance, independent of the input signal characteristic, except for possible imperfections caused by the sample and hold circuit. By testing the converter with an DC signal and finding out all the nonlinearities of the converter, the static performance of these converters has been well defined.

The basic operation of an oversampled A/D converter is totally different from that of the other converters. For a band limited signal, the minimum sampling rate of the signal is two times the input signal bandwidth by Nyquist theory. The quantization noise of an PCM , shown in Fig 2.14, is represented as the following.

$$N(f) = (\frac{\sigma^2}{12})\frac{1}{f_s} \quad where\ \sigma = step-size \tag{2.8}$$

The total inband noise can be derived by integrating the noise which fall into the signal band which is usually half of the sampling frequency.

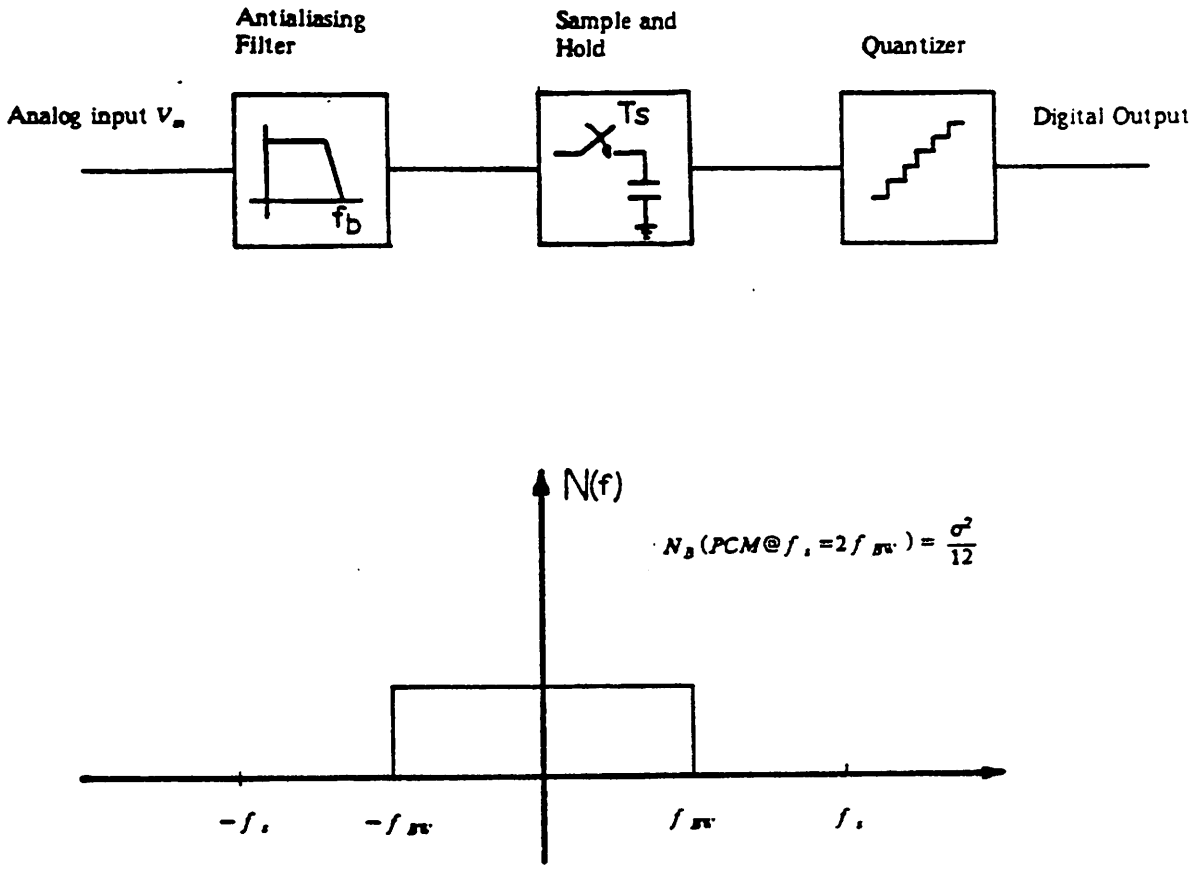


Fig 2.14 The block diagram of a normal PCM coder and the corresponding noise power spectrum

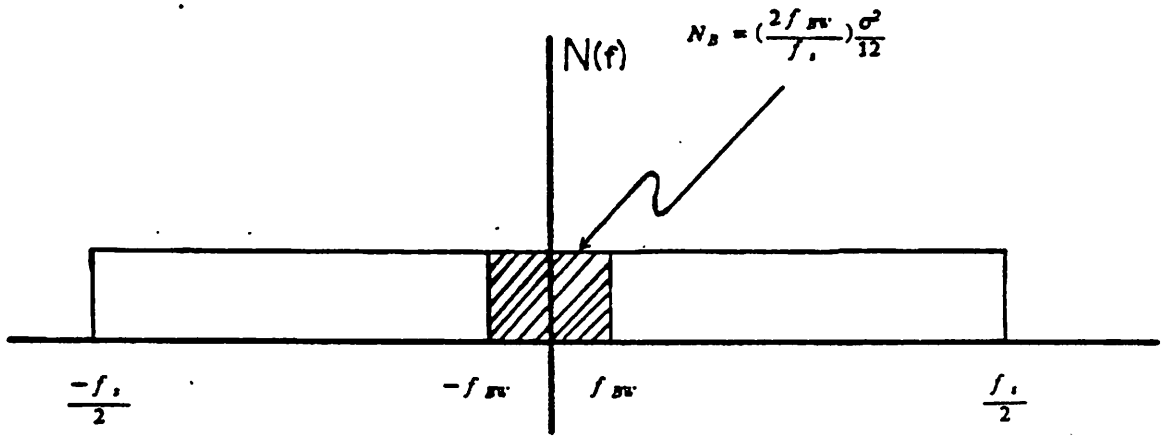
$$N_o = \int_{-f_s/2}^{f_s/2} N(f)df = \frac{\sigma^2}{12} \tag{2.9}$$

Sampling the input signal at an higher rate does not increase the total quantization noise but instead spreads the quantization noise over an wider bandwidth. The out of band noise can be eliminated by an low pass filter with the bandwidth equal to f_{BW}. Figure 2.15a shows the noise power spectrum in the signal band after the low pass filter.

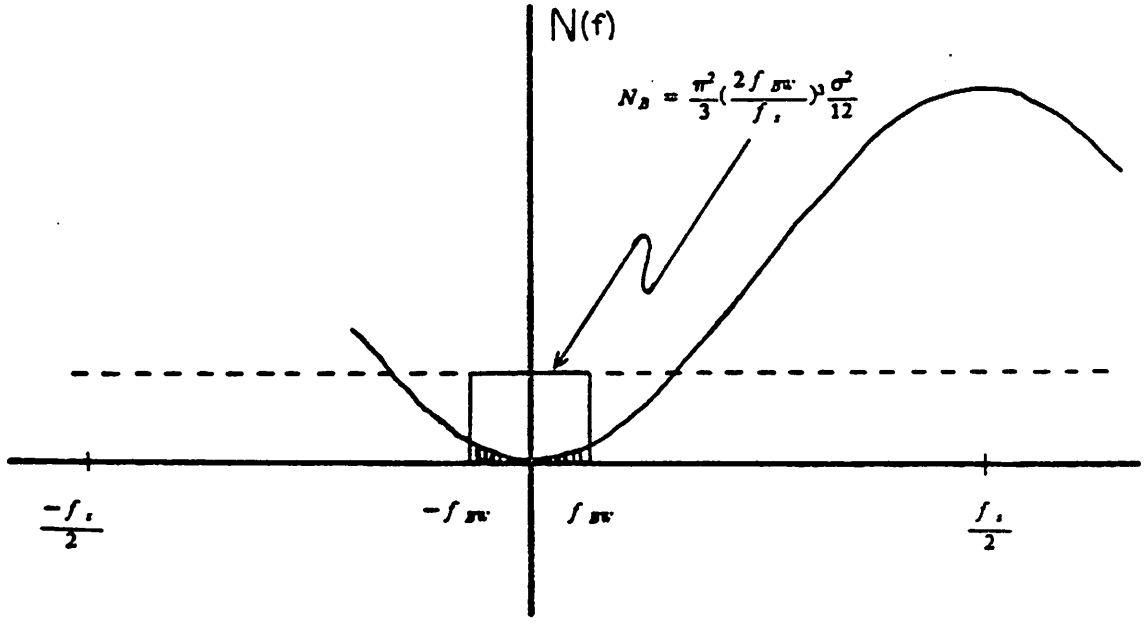
$$N_B = \int_{-f_B/2}^{f_B/2} N(f)df = (\frac{\sigma^2}{12})\frac{2f_{BW}}{f_s} \tag{2.10}$$

The gain from oversampling is in the $(\frac{2f_{BW}}{f_s})$ term. Every quadrupling of the sampling frequency reduces the effective quantization noise power by four times, corresponding to about 6 dB gain of the signal to noise ratio. From another point of view, making the sampling rate four times higher actually yields one extra bit of resolution for the A/D. For a 4kHz band limited signal, the inband quantization noise for 13 bits resolution @ f_s = 8 kHz is equal to that for 4 bits of resolution with pulse code modulation (PCM) oversampled at 2 GHz. By enhancing the resolution in time, a high resolution A/D conversion can be made by low precision circuits.

Oversampled Δ-modulation and the oversampled Σ−Δ modulation are two popular methods that utilize this idea. The basic functional block of the Δ-modulation is shown in Fig 2.16a. The sampling switch samples the input signal at an very high frequency (>> Nyquist frequency). Then the difference of y(t) and $\tilde{x}(t)$ is quantized by an comparator. In the feedback loop, the previously quantized difference is integrated by the integrator and produces a signal, $\tilde{x}$, which is a prediction of the new input signal. In this approach, instead of a 4-bit A/D converter, a single bit comparator is used therefore, in equation (2.10), the sampling rate needs to be 128GHz to achieve an 13 bit resolution. With this kind requirement, the implementation of the digital filter will be either impossible or will consume a tremendous amounts of power. Furthermore, the



(a)



(b)

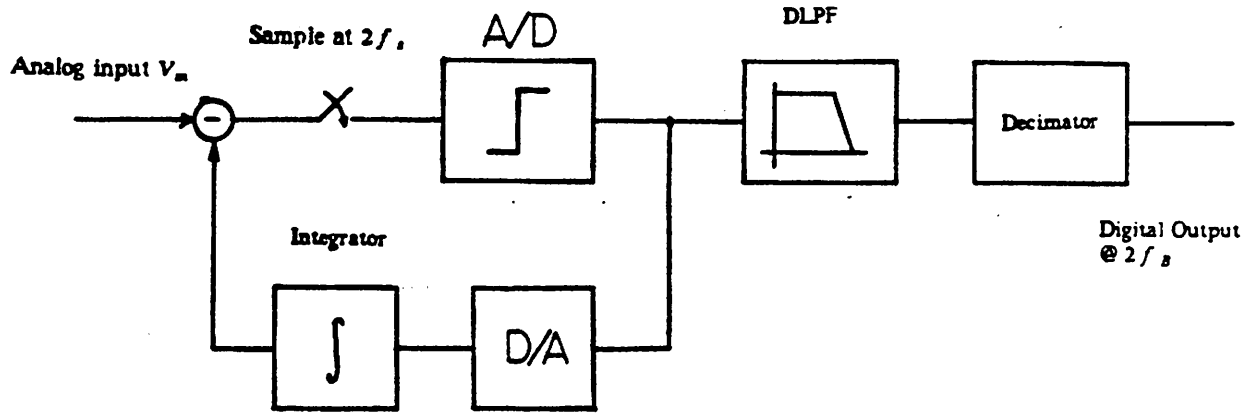
Fig 2.15 The noise spectrum with the hatched area shown the effective inband noise after the filtering

(a) Oversampled PCM

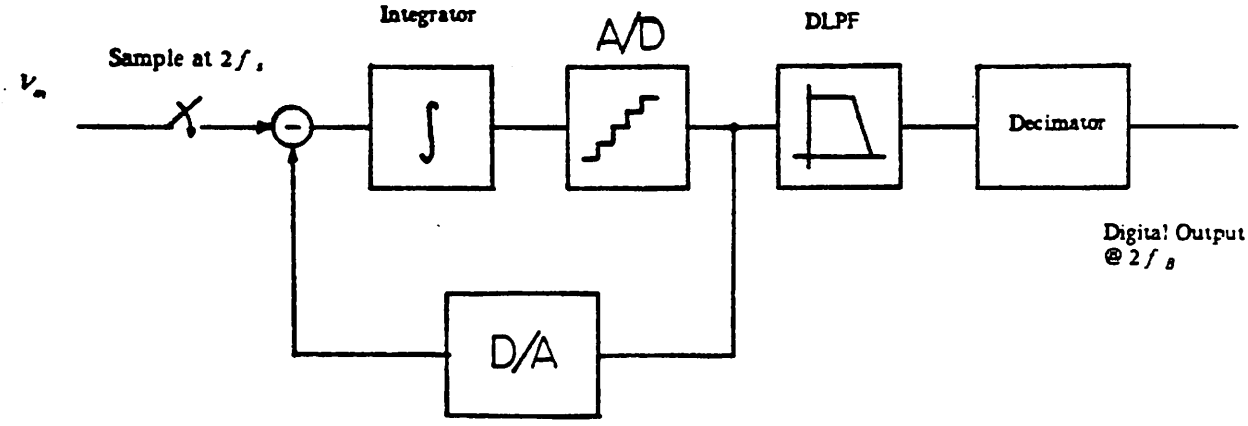
(b) Σ−Δ modulation

assumptions for equation (2.3) break down when 1-bit converter is used. When the input signal is oversampled, there is a lot of correlation between two sampled signals. In order to get the most benefit from this characteristic, a delta modulator is used instead of a simple 1-bit converter. Basically, the delta modulator encodes the difference of the input signal and the prediction value. Because of the correlation between two successive input signals is high, the difference amplitude has much smaller variance than the original signal. One bit is often sufficient resolution to represent such a small variance signal. After this modification, the oversampled converter becomes much more difficult to be analyze. The sampling rate not only spreads out the in band quantization noise but also affects the correlation between signals, which in turn determines the performance of the delta modulator. The oversampled Δ-modulation is very dependent on the input signal's distribution function. Using sinusoidal or triangular input as a test signal will produce different SNR measurements. In Fig. 2.16a, a block diagram of a oversampled Δ-modulation converter is shown. The digital lowpass filter (DLPF) after the comparator can be easily implemented by averaging the one bit output from the comparator.

The Σ—Δ interpolated converter is another type of oversampled converter. It modifies the shape of the quantization noise power spectral and drives most of the quantization noise out of band. The block diagram of an interpolated converter is shown in Fig 2.16b. The circuit uses a negative feedback loop containing an integrator and a coarse quantizer that spans the signal range. A digital representation of the quantized signal increments the contents of an accumulator. After signals have cycled around the feedback loop a set number of times, an output is taken from the accumulator and its content set to zero before cycling for the next sample begins. The average of the quantized signals represents the average input with a quantization error that is N times less than the error associated with the coarse quantizer[Cand74]. The noise $E(\cdot)$ introduced by the converter is the first difference of uniform quantization noise $\epsilon(\cdot)$.



(a)



(b)

Fig 2.16 The block digrams for (a) Δ modulation (b) Σ−Δ modulation

$$E(n) = \epsilon(n) - \epsilon(n-1) \tag{2.11}$$

$$\Phi_E(n) = 2\Phi_\epsilon(0) \text{ when } n = 0$$

$$= \Phi_\epsilon(0) \text{ when } n = 1$$

$$= -\Phi_\epsilon(0) \text{ when } n \ -1$$

It has a triangular probability density function spanning magnitudes up to that of the step size. The noise spectral density has a shape like the one shown in Fig 2.15b. Although the total quantization noise power of the Σ−Δ converter is twice as much as the uniform quantizer, only a small portion of the noise falls inside the signal band. The benefit by oversampling is proportion to the third power of the oversample ratio ($\frac{f_s}{2f_{BW}}$). The improvement is greater than that for Δ-modulation.

For an oversampled system, the output signal is representative of the average input signal over the entire sample interval, not just over a small aperture within the sample interval, as is the case with most ordinary PCM coders. Such averaging is equivalent to a low-pass filter with spectral response[sin(ωT/2)/(ωT/2)]. Using an appropriately weighted averaging of the oversampled output can provide an even better low-pass filter than a straight forward summation [Cand76].

In some areas, the oversampled converter is the best alternative to avoid high precision circuits. But there are some practical problems and limitations of this approach. First, because of the oversampling requirement, it is only good for low frequency applications. For example, speech processing already requires a sampling rate in the MHz range. Second, there is an increased level of low frequency noise components when the input signal is very small[Cand76], and under some combinations of low input signal level and high input frequency the converter ceases to encode the input signal. Third, as is discussed in the previous paragraph, the oversampled converter performance not only depends on the input signal level but also depends on the input signal frequency. It is hard to analyze the conversion process and pinpoint any problem. By small DC

shifts[Cand76] or spectral redistribution [Ever79] or double integration of the input signal[Cand85], some of the problems can be solved. The input·dc bias just moves the problem to place where signal level is large but to solve the problem. The spectral redistribution in some way is similar to the input bias but it also change the correlation between the sampled input signals which affects the whole characteristic of the converter. The performance of the converter after spectral redistribution will not only depend on the input signal but also the frequency and amplitude of the dither signal. One optimal frequency of the dither signal for sinusoid input might not be the best choice for the speech signal. The double integration seems to be the most promising solution. Finally, the averaging of the input signal during a period of time, also limits this kind of converter to some special application instead of a general purpose A/D converter.

CHAPTER 3

CYCLIC CONVERTERS USING THE REFERENCE REFRESHING METHOD

As we have seen, there are many different conversion techniques and applications, and each one of them has a unique characteristic. For speech signal processing and voice band digital signals, dynamic range around 75-80 dB and 125 μsec conversion time are necessary requirements. In order to be able to integrate converters for such applications within a signal processing chip, the converter should take up as little die area as possible. Because both pipeline and flash converters are too complicated in high resolution implementation to have small enough area, only three types of converters are capable of meeting the area requirement. They are (1) integrating converters, (2) oversampled converters and (3) successive approximation converters. Consider these techniques one at a time. First, the integrating converter is not a proper choice because of its inherently low conversion speed. Using CMOS circuit design techniques, for example, a 12 bit integrating conversion can only operate at less than a few hundreds herz range. Second, The characteristics of oversampled $\Sigma-\Delta$ converters depend strongly on the input signal distribution function. The output code word from the $\Sigma-\Delta$ is the result of averaging a number of input samples over a period of time. Before the minimum feature size of the technology goes below 1.5 μ, the complexity of the digital filter will make this approach uneconomical to implement. Finally, cyclic successive approximation converters seem to be a good choice for this application because of their reasonably low area (constant with increasing resolution) and reasonably high conversion rate (decreasing only linearly with increasing resolution).

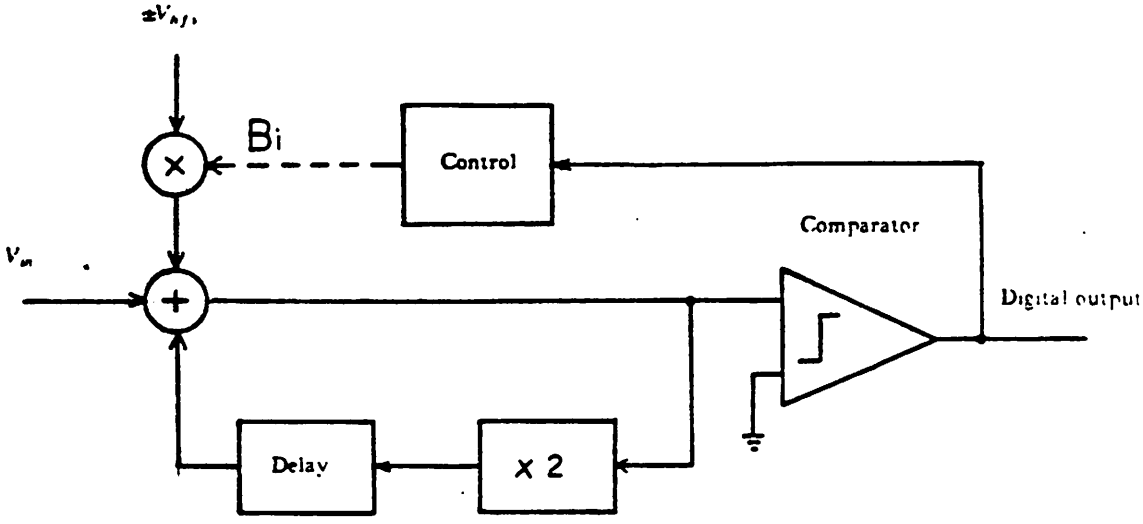
In this chapter, first the basic operations of the cyclic A/D and D/A conversion techniques will be explained. In the second section, the CMOS implementation of this

technique is explored. The effect of the nonideal situations such as the capacitor mismatch and finite operational amplifier gain effect are discussed in the third section. A new technique that modifies the cyclic conversion by refreshing the reference signal along with the sampled signal is investigated in section 4. This method removes the sensitivity of the converter to capacitor matching and finite op-amp gain. In section 5, the zero order error of the loop is discussed and offset sampling technique is proposed to solve this problem. The detail operation procedures of the new improved conversion technique is described in section 6. Section 7 gives the computer simulation results for the cyclic conversion before and after using the reference refreshing approach. This new technique compared with some other ratio independent techniques in section 8. In the last section of this chapter, another comparison is made between the reference refreshing cyclic converter and the oversampled sigma-delta converter. The tradeoffs between these two converters are explored.

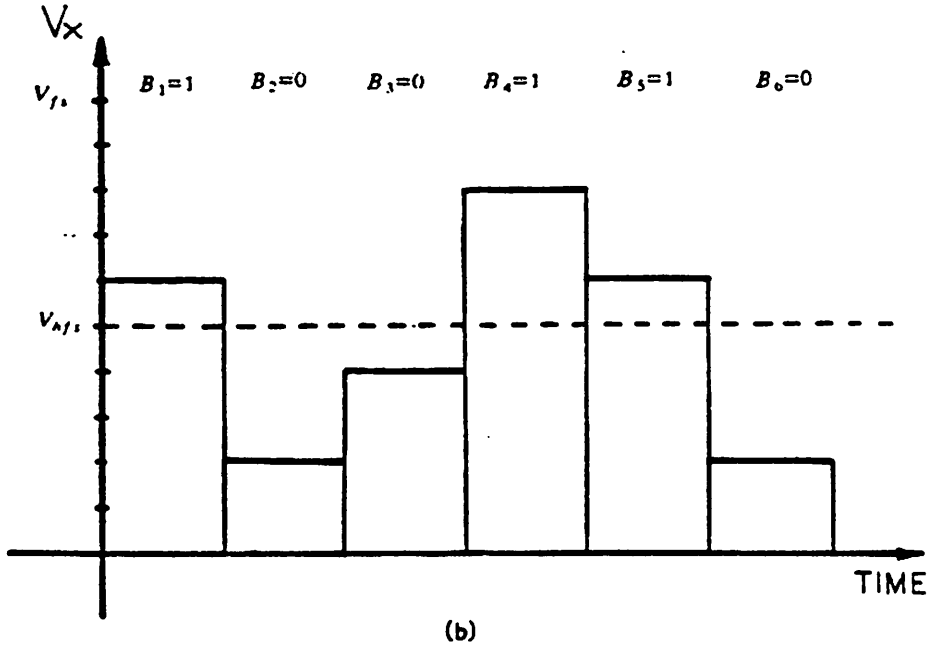
3.1. Cyclic Conversion Techniques

Cyclic Analog to Digital Conversion

The technique described in this chapter is a modification of the "cyclic" or "algorithmic" conversion technique[McCh78]. Traditional cyclic or algorithmic conversion involves comparison, reference subtraction if applicable, and multiplication of the result by a factor of two. The block diagram of the cyclic converter and example of the internal voltage variation versus time are shown in Fig 3.1. With a dual polarity input signal, an extra cycle is needed to determine the input signal polarity before further processing. The sign bit also determines the polarity of the reference that is used in the following cycles. The second step in the process is to decide whether the signal is in the upper or lower half of the full range. If the signal is in the upper range, the reference (half of full scale voltage) is subtracted from the signal and the difference is doubled. At the same time, the most significant bit of the digital output is set to one. If the



(a)



(b)

Fig 3.1 (a) The block diagram of a cyclic A/D converter
(b) an example of internal voltage variation vs. time

signal is in the lower half, the signal is simply doubled without subtraction and the most significant bit is set to zero. In the next cycle, the remainder from the previous cycle is used as the input and the process is repeated. After each additional cycle, one extra digital bit is generated. Following the procedure, the signal can be encoded into a 13-bit digital output in 13 iterations including the sign detection cycle. The mathematical description of the conversion is as follows:

$$A_0 = V_{in}$$
$$A_i = T(A_{i-1} - B_{i-1}V_{hfs}) \tag{3.1}$$

where

$$T(x) = 2x$$
$$B_{i-1} = 0 \text{ if } A_{i-1} \textit{ in the lower-half}$$
$$B_{i-1} = 1 \text{ if } \textit{otherwise}$$

The dual polarity algorithmic A/D conversion flow diagram is shown in Fig 3.2.

The decision as to whether the signal is in the upper or lower range is made by subtracting the half range voltage from the signal and comparing the remainder with zero. If the remainder is below zero, the signal must be in the lower half region. The reference is then restored back to the signal before doubling. If the remainder is above zero, the remainder is multiplied by two directly. Sometimes, this approach is called the *restoring* cyclic conversion. An alternate way to implement the cyclic conversion (which does not require the restoration of the reference voltage) is called a *non-restoring* cyclic algorithm. The choice of whether to add the reference voltage to the signal or to subtract the reference from the signal is determined by the polarity of the previous outcome. If the previous outcome is positive, the reference voltage is subtracted from the signal. On the other hand, if the previous signal is negative the reference is added to the signal. After the addition or subtraction, the polarity of the new signal determines the next output bit. If the signal is positive, the corresponding digital

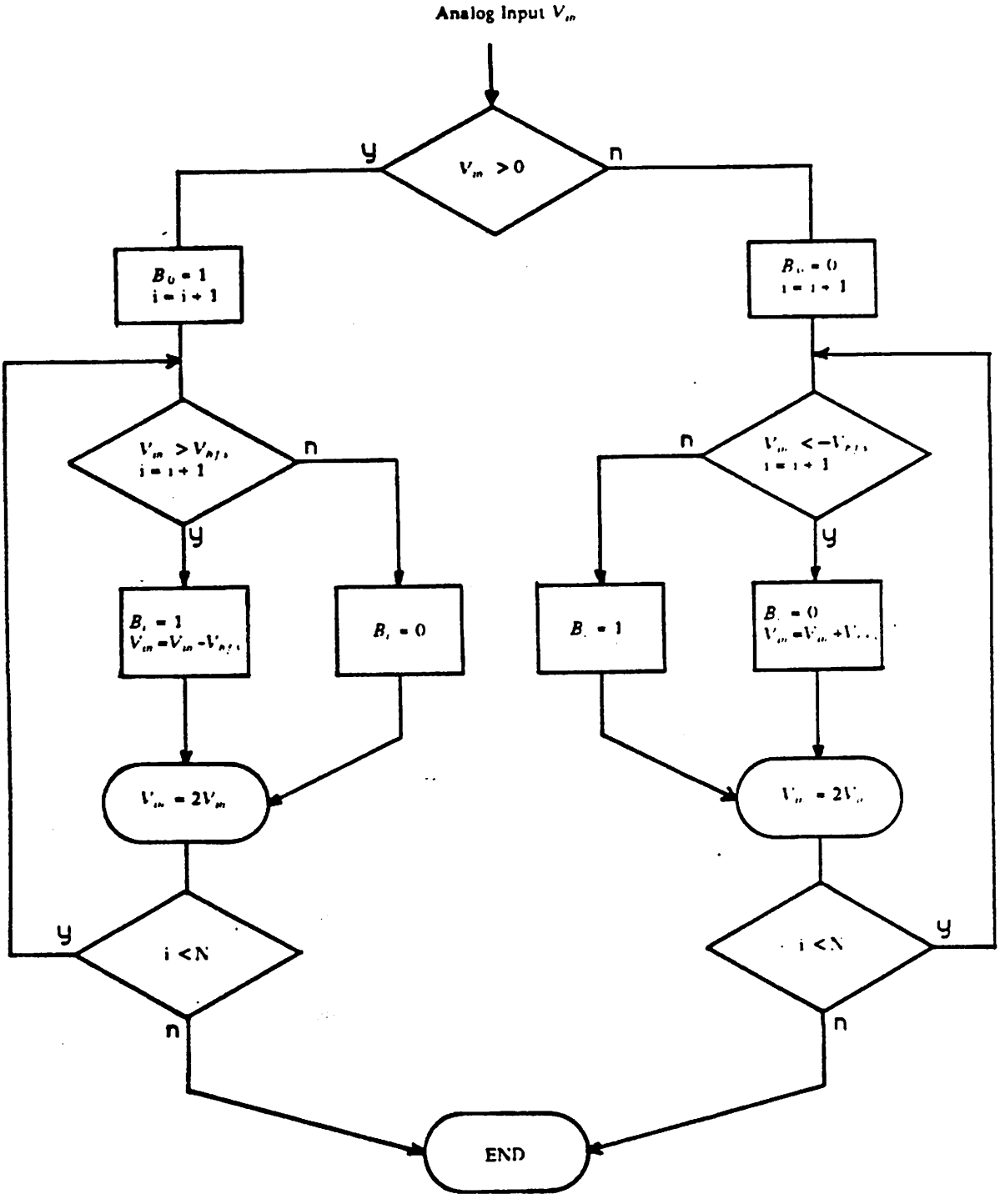


Fig 3.2 The flow chart of a dual polarity algorithmic A/D conversion

output is set to one. Otherwise, the digital output is set to zero. By iterating the above procedure, the analog signal can be again converted into a digital form. Using the nonrestoring algorithm, no reference restoration needs to be performed after the comparisons because whether addition or subtraction operation is determined by the bit output of the previous cycle. Thus, the non-restoring algorithm is more straightforward and often takes less time for the conversion than the restoring algorithm; however, since either an addition or a subtraction is performed every cycle, regardless of the signal magnitude, the nonresoring method might introduce excessive noise to small signals. Because of the special concern about small signal performance in this research project, a modified restoring algorithm is chosen, which avoids the the subtraction before the comparisons. Since the comparator designed in this research can compare the input signal with the reference directly, the signal location can be resolved without the subtraction at the beginning of the comparison. This special operation is desirable for small input signals, because no unnecessary operations are performed on a signal until the signal is amplified to exceed half full scale. Details of this implementation will be discussed in the next section.

Cyclic Digital to Analog Conversion

The D/A cyclic converter block diagram is shown in figure 3.3(a). For a D/A conversion, no comparator or multiplier is needed. Instead, a divide by 2 function is necessary for the D/A converter. In the D/A operation, the least significant bit is decoded first. The polarity of the reference is determined by the sign bit of the digital input code. The decision as to whether to add the reference voltage or not in each cycle depends on the digital input code. The analog output is built up from sums of voltages represented by each bit starting with the LSB and ending at the MSB. Thus the sum from the previous conversions is divided by two before it is added to the current conversion. At the end of 13 cycles, the analog output is derived from the digital code.

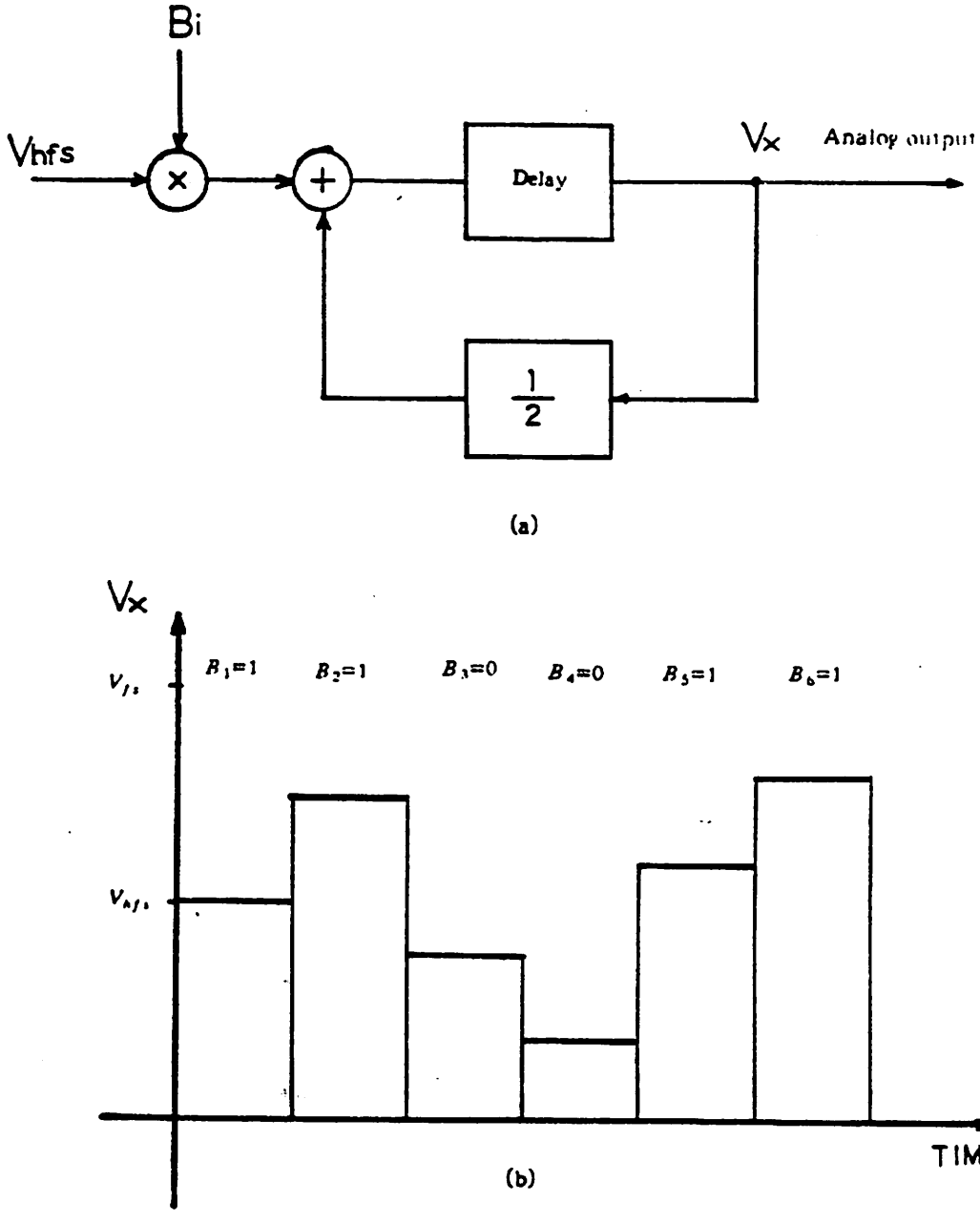


Fig 3.3 (a) The block diagram of a cyclic D/A converter
(b) an example of internal voltage variation vs. time

The mathematical description of the D/A conversion is as follows:

$$A_i = T(A_{i-1} + B_{N-i+1} V_{hfs}) \qquad (3.2)$$

$$A_N = V_{out}$$

where

$$T(x) = x / 2$$

B_N *is the least significant bit*

A simple 5-bit example of the conversion is illustrated in Fig 3.3(b). As usual, the D/A operation is much easier than the A/D conversion mostly because no comparison is needed in the D/A conversion and every step is predetermined after the input digital code is received. The flow chart of a N-bit sign magnitude D/A is explained in Fig.3.4.

3.2. CMOS Implementation of the Cyclic Converters

In order to have a single chip digital signal processor, the A/D and D/A converters have to be on the same chip as the processor. When a very large scale integrated circuit is designed , yield and power consumption of the chip are the two most important concerns. Typically MOS technology can provide higher density than bipolar. Higher circuit density can be translated into higher yield in production. With complementary MOS, the power is basically utilized while charging the next stage input capacitance. There is no static current and thus no wasted power during stand by. Because of the increasing popularity of CMOS technology in VLSI circuits and in order to have these converters fabricated on the same chip as the digital circuits, CMOS is chosen as the technology for these converters.

A/D Circuit Implementation

In order to construct a cyclic A/D converter, several functional blocks are required; i.e. a sample and hold (S/H), a multiplier and a comparator. Each will be discussed below.

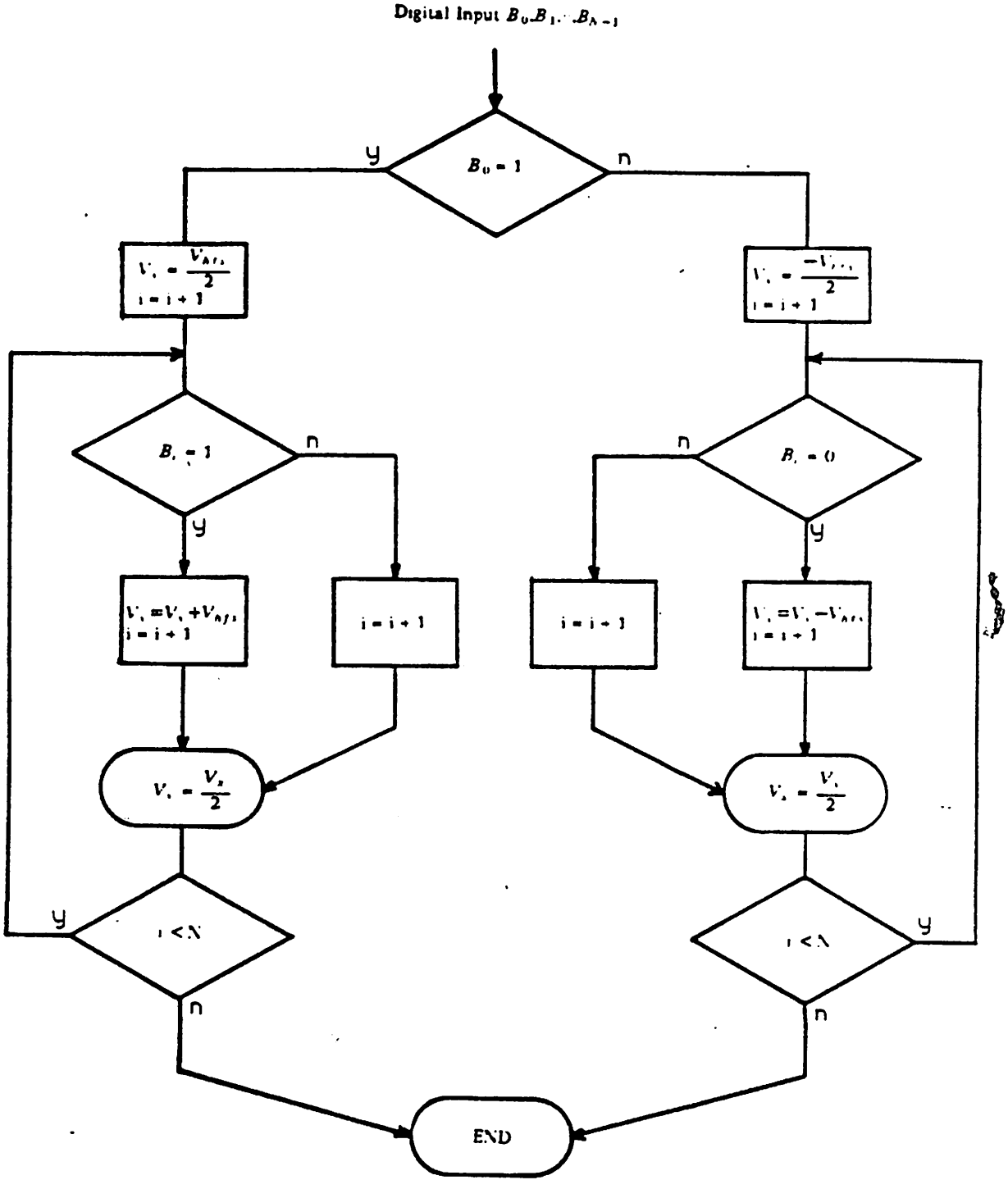


Fig 3.4 The flow chart of a dual polarity algorithmic D/A conversion

A sample and hold function can be realized by two equal sized capacitors C_1 and C_2, an operational amplifier, and several switches. (see Fig 3.5) The operation of the S/H is as follows. With switch SW1 closed to V_{in} and switches SW2, SW3 closed, the input is connected across capacitor C_1 and capacitor C_2 is discharged. Next, switches SW2 and SW3 are opened and switches SW1 is closed to ground. As a result, because the op-amp holds the summing node voltage to virtual ground, the charge on C_1 which has the magnitude of $C_1 V_{in}$ is transferred to C_2 . If C_1 and C_2 have the same capacitance, the input signal voltage is effectively sampled and held at the output of the operational amplifier.

The S/H circuit described above can be transformed into a a multiplication by two block just by changing the secondary position of SW1. By throwing switch SW1 to the opposite polarity of the input voltage instead of returning it to ground, the amount of charge driven to capacitor C_2 is doubled. Thus, at the end of the operation, the voltage appearing at the output of the operational amplifier is twice of the value of the sampled input voltage. So instead of two clock cycles integration method, the multiplication by two function can be done in one clock cycle and at the same time eliminates any possible distortion from double integrations.

Another major block in the converter is the comparator. The comparator determines whether the signal of interest is above or below half full scale. First, the half full scale voltage (V_{ref}) is subtracted from the signal of interest by changing the position of SW4 from ground to V_{ref} . After the subtraction, the remainder is connected to the comparator to compare the remainder with ground. Whether or not the original signal level is above V_{ref} is easily determined by examining the remaider's polarity. After the comparison, the reference voltage can be restored by returning switch SW4 to ground in a restoring algorithm.

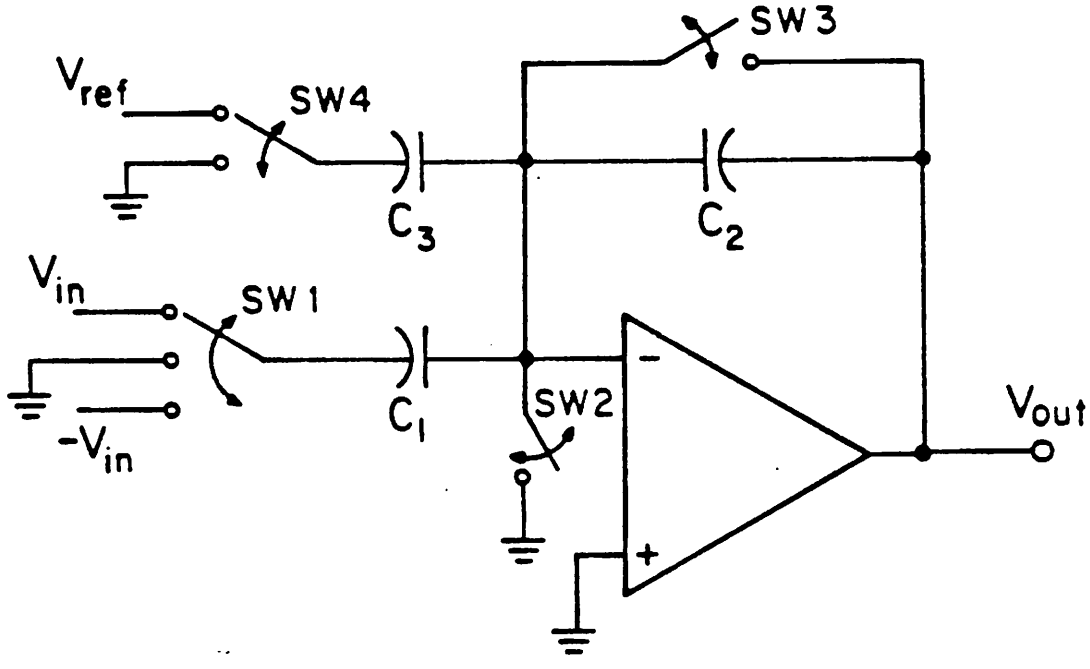


Fig 3.5 A basic circuit for sample and hold and subtraction

Another way of comparing the signal with the reference is by having an extra capacitor in front of the comparator as in Fig 3.6. Before connecting the input signal to the comparator, the reference voltage can be stored on this capacitor by connecting SW1 to V_{ref} and closing SW2. Then the input signal is introduced to the comparator by changing the position of SW1 to V_{in}. Now V_{in} is compared with the reference level instead of with ground. With this kind of comparison, no unnecessary subtraction before the comparison or possible addition after the comparison is needed to located the input signal. This is important because every addition and subtraction is a possible error source and can be especially harmful for small input signals. Here, no subtractions are performed on small signals until they are amplified up to half full scale.

An A/D circuit diagram with two fully differential operational amplifiers and a comparator is shown in Fig 3.7. All the capacitors in the figure have the same value (2 pF). The fully differential operational amplifier makes both the positive and negative output signal available for the multiplication scheme just mentioned. Some other benefits of using the fully differential operational amplifier will be obvious in the coming sections.

D/A Circuit Implementation

As previously mentioned, there are two major differences between the D/A and the A/D converter. First, in the D/A converter, the comparator is not required. Second, a cyclic D/A needs a divider by two instead of a multiplier. This is easily built by changing the ratio of the C_1 and C_2 capacitors in the S/H (Fig 3.5) from one to one half. A D/A converter circuit consisting two fully differential operational amplifiers is shown in Fig 3.8. All capacitors used in the converter are 2 pF except C_4, which is 4 pF in order to get the division function needed in the D/A.

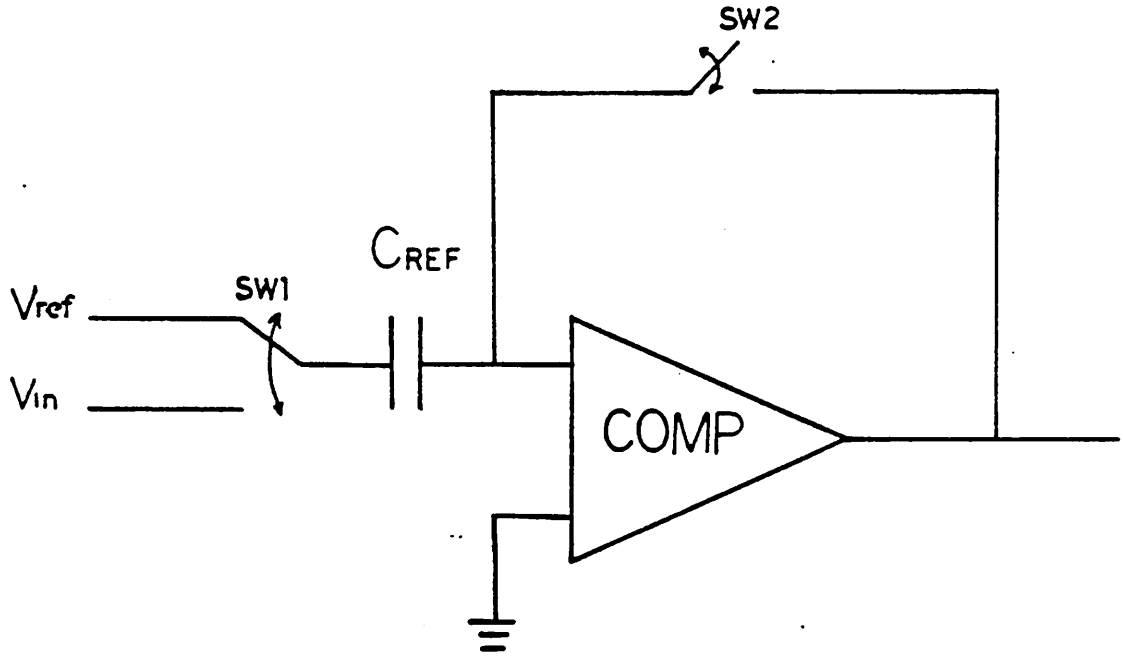


Fig 3.6 With one extra capacitor, the comparator circuit can directly compare with a fix voltage

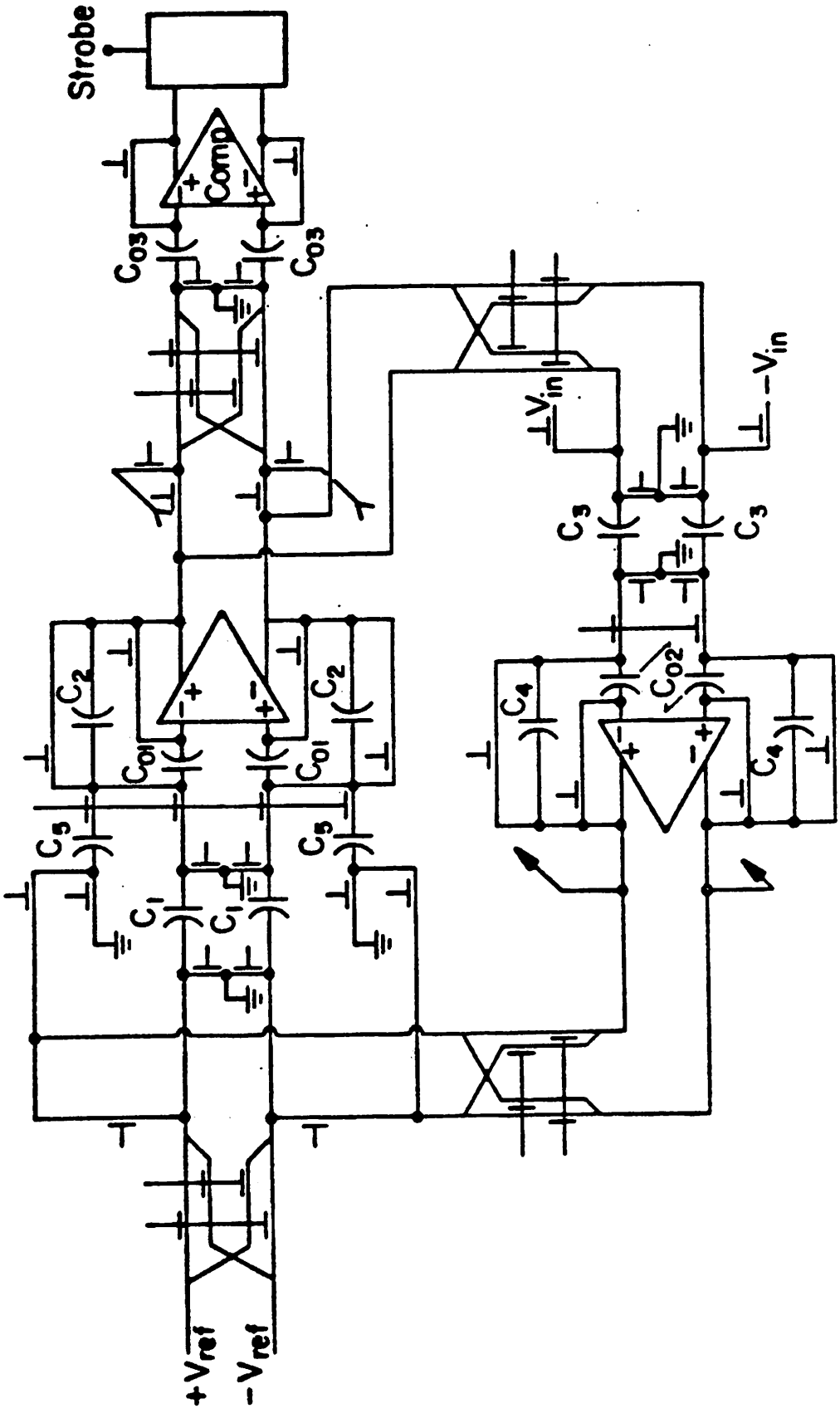
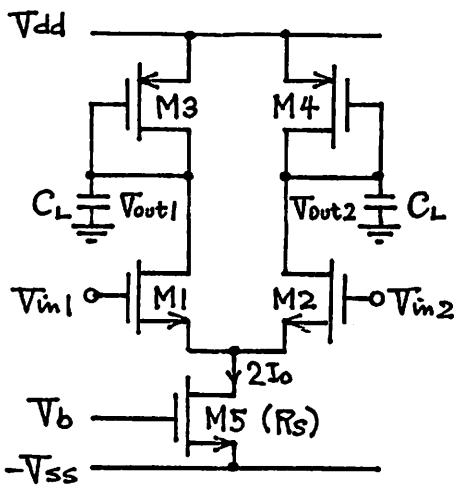
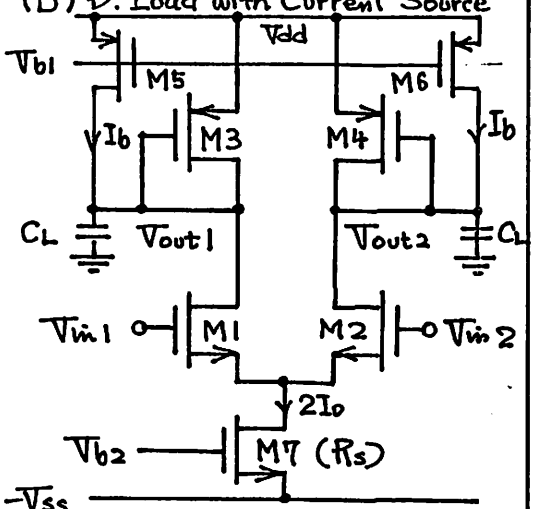
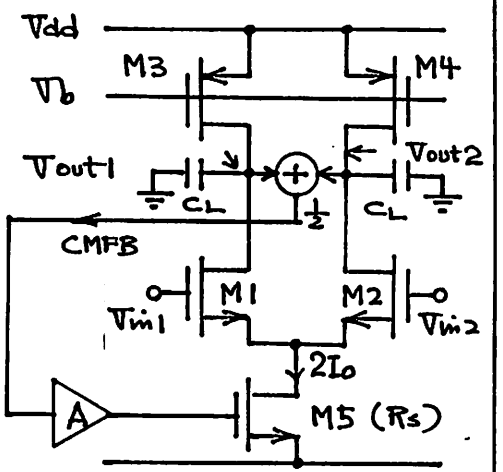


Fig 3.7 A detail system circuit diagram for the A/D converter with two fully differential amplifiers, one comparator, and a few capacitors.

Basic Circuit Configuration	(A) Diode Load	(B) D. Load with Current Source	(C) Current Source Loads & CMFB
			
diff. mode gain Ad	$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\beta_1}{\beta_3}}$	$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\beta_1 I_{d1}}{\beta_3 I_{d3}}}$	$g_{m1}(r_{o1} // r_{o3})$
cut off frequency ω_c	$\frac{g_{m3}}{C_L}$	$\frac{g_{m3}}{C_L}$	$\frac{1}{C_L(r_{o1} // r_{o3})}$
gain band width GBW	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$
common mode gain Ac	$\frac{g_{m1}}{g_{m3}} \frac{1}{2R_s g_{m1}+1}$	$\frac{g_{m1}}{g_{m3}} \frac{1}{2R_s g_{m1}+1}$	$\frac{1}{A g_{m5} \cdot R_s}$
gains for AC power supply: Add	1 (diode connection)	1 (diode connection)	$1/A g_{m5} \cdot r_{o3}$
gains for AC power supply: Ass	$1/2R_s g_{m3}$	$1/2R_s g_{m3}$	$1/A$
Reset Time Const.: non-linear	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/(g_{m1}+g_{m3})$	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/(g_{m1}+g_{m3})$	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/g_{m1}$
Reset Time Const.: linear	$(1/R_f \cdot C_{in} + g_{m3}/C_L)^{-1}$	$(1/R_f \cdot C_{in} + g_{m3}/C_L)^{-1}$	$(1/R_f \cdot C_{in} + 1/(r_{o1} // r_{o3}) \cdot C_L)^{-1}$
Dynamic Range (out)	$V_{dd}-\lvert V_{thp}\rvert - 2\sqrt{I_o/\beta_3} < V_{out} < V_{dd}-\lvert V_{thp}\rvert$	$V_{dd}-\lvert V_{thp}\rvert - 2\sqrt{(I_o-I_b/2)/\beta_3} < V_{out} < V_{dd}$	$-V_{ss}+V_{thN}+2\sqrt{\frac{I_o}{\beta_5}}+\lvert V_{thp}\rvert+2\sqrt{\frac{I_b}{\beta_7}} < V_{out} < V_{dd}$
Size [1]	554 μm² (273 Mrad/s)	296 μm² (1570 Mrad/s)	
Power Dissipation [1]	32 μW (〃)	760 μW (〃)	
GBW_{max}.	267 Mrad/s	1661 Mrad/sec ※ C_{in} = 0.14pF	

[1] Size and Power for an Optimum Design ($GBW \geq 0.9 GBW_{max}$, $G_{effective}=10$, $W_{min}=2\mu m$, V_{out} level considered at $V_{dm}=0$)

Fig.3.6-2 Basic Characteristics of Fully Differential Amplifiers (1)

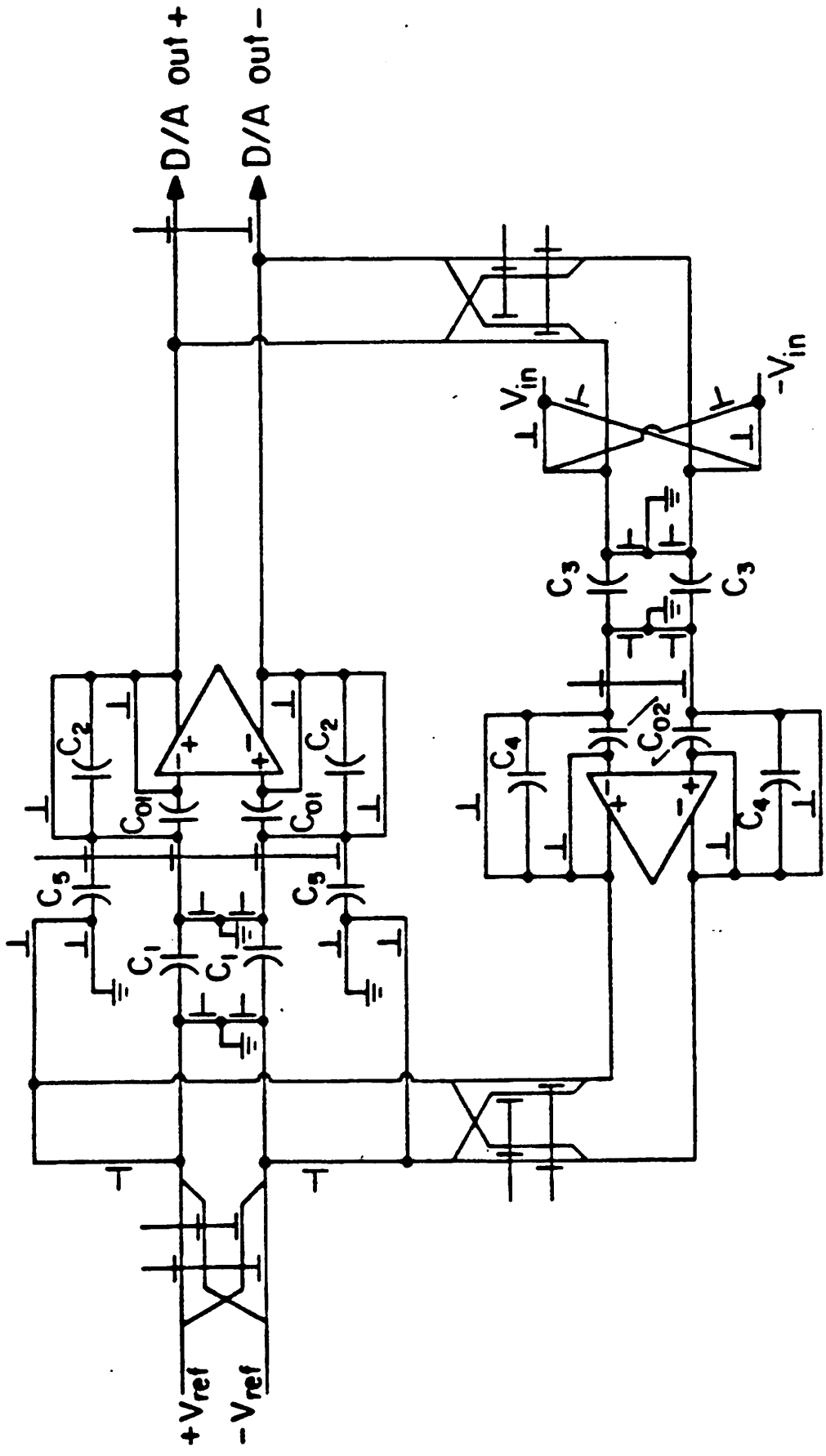


Fig 3.8 A detail system circuit diagram for the D/A converter with two fully differential amplifiers and a few capacitors.

3.3. Effects of Capacitor Mismatch and Finite Op-Amp Gain on Cyclic Conversion

With switched capacitor implementation of the algorithmic converter, the accuracy of sample and hold and the multiplication function both depend on the matching between two capacitors. In spite of laying out the capacitors to have exactly the same area ratio as the desired capacitor ratio, errors in edge location due to tolerances associated with mask generation, and the etching process as well as uneven oxide thickness across the wafer, contribute to the matching inaccuracy between capacitors. By extravagant the experimental data from a recent paper[Shyu84], in order to achieve about 50% yield to .012% matching between two capacitors, the size of the capacitor will have to be larger than 300x300 μ^2(38pF).

Additionally, the finite open loop gain associated with a real op-amp also deteriorates the accuracy of the close loop gain in the S/H circuit (Fig 3.5). Finite gain is especially a problem for MOS amplifiers because the transconductance for a given current of the MOS transistor is much lower than the bipolar transistor. This finite gain amplifier will reduce the accuracy of the charge transfer operation between two capacitors. When the input voltage is sampled on the C_1 capacitor, the charge stored on the capacitor is $C_1 V_{in}$. When the bottom plate of the capacitor is connected to ground and the top plate is connected to the amplifier input node, with infinite amplifier gain, all the charge on the capacitor C_1 will be transferred to C_2. However when the gain is finite (A), C_1 is discharged to $\frac{V_{out}}{A}$ instead of all the way to 0 volt. This effect contributes first order gain error in the transfer function of the algorithmic conversion. In equation (3.3), the two major factors that cause the nonideal loop gain of the algorithmic converter in the charge transfer operation are summarized.

$$\frac{V_{out}}{V_{in}} = (\frac{C_1}{C_2})\frac{1}{(1+\frac{C_1}{C_2}A)} \qquad \textit{where A is the op-amp gain} \tag{3.3}$$

By taking into account of the capacitor ratio inaccuracy, finite operational amplifier's gain and other errors existing in the loop, the loop transfer equation will be different from the ideal case presented in equation 3.1. The real transfer function T(x) will have some nonideal terms:

$$T(x) = 2x + \sum_{i=0}^{N} E_i x^i \tag{3.4}$$

where

E_0: DC offset

E_1: Loop gain error due to capacitor mismatch etc.

E_2 , E_3: Other high order distortions

These deviations result in both integral and differential nonlinearity in algorithmic converter. First, consider the loop gain error term, E_1. When a dual polarity N bit algorithmic A/D converter is used, a large differential nonlinearity or missing code can be the result from a positive or negative gain error respectively. And the problem will be most apparent at the major carrier. For a normalized converter with ± 1 maximum input range, let Δ be the step size between 011...1 and 100...0 (the major carrier). For an input magnitude of (1/2 - Δ), the signal should be encoded as 011...1. In order to satisfy the above requirement, except the decision of the most significant bit (cycle 1), at the rest of the decision instant the remainder need to exceed 1/2 to encode the signal correctly. So at the end of the cycle N-1, the following equation need to be satisfied,

$$1-2^{N-1}\Delta+E_1\frac{1}{2}(1+2+\cdots+2^{N-1}) \geq \frac{1}{2} \tag{3.5}$$

To achieve a N bit converter with differential nonlinearity less than half LSB, equation 4 should be valid for Δ value between 1/2 LSB and 3/2 LSB. Substituting this range of Δ into equation 3.4, it turns out that the absolute maximum gain error should be less

than $\frac{1}{2^N}$. In a 12 bit case, the maximum allowable loop gain error should be less than .025%. Since there are two amplifiers in the loop, each of them needs to be accuracy to .0125%. The only reasonable way to obtain this high capacitor matching accuracy is by laser trimming the capacitors which increases the cost of the converter. Also, in order to obtain such a small loop gain error, the minimum open loop gain of the amplifiers must be at least 84dB.

3.4. Reference Refresh Principle

The technique described in this paper is a modification of the "cyclic" or "algorithmic" conversion technique[McCh78] that removes the dependency of the conversion on the loop gain accuracy by refreshing the reference. The basic principle is that a precise gain of 2 is not necessary if the reference is modified on each cycle by a factor that is the same as the factor by which the loop gain is different from two. In other words, the loop gain error, E_1, can algorithmically corrected by modifying the reference voltage (V_{ref}) at each cycle based on the loop error. The reference voltage of the circuit is not fixed during the conversion but is updated once each cycle. The reference voltage source is only sampled at the first cycle for each conversion. The effective reference voltage($V_{ref}^{[k]}$) at the k-th cycle will be $V_{ref}(1+\frac{E_1}{2})^k$. The following example explicitly shows the correction effect for an 3 bit A/D conversion .

$$K\left\{K[K(V_{in}-B_0V_{ref}^{[0]})-B_1V_{ref}^{[1]}]-B_2V_{ref}^{[2]}\right\} \tag{3.6}$$

$$= K^3[V_{in}-B_0V_{ref}^{[0]}-B_1\frac{V_{ref}^{[1]}}{K}-B_2\frac{V_{ref}^{[2]}}{K^2}]$$

$$= K^3\left|V_{in}-B_0V_{ref}-B_1\frac{V_{ref}}{2}-B_2\frac{V_{ref}}{2^2}\right|$$

where

$$K = 2\,(1+\frac{E_1}{2})$$

$$V_{ref}^{[k]} = V_{ref}\,(1+\frac{E_1}{2})^k$$

After the reference refreshing, the A/D or D/A is not affected by the first order error in the loop. In Fig 3.9, it shows that the refreshed reference will always points at the midpoint of the full possible input range each cycle even with 10% first order error. In Fig 3.10, a simulation result of a 3 bit A/D transfer curve shows that the loop gain error is corrected by the reference refreshing technique. One other advantage of this technique is that by passing the reference and the signal through the same loop, all the errors that are partly related to the first order error term (such as charge injection) are automatically eliminated at the same time. The reference refreshing approach also reduces the effects that are generated from all the other high order errors such as E_2, E_3 in equation (3.4). This fact greatly simplifies the implementation of a high-resolution converter.

The reference recirculation method can be used not only for analog-to-digital conversion but also on digital-to-analog conversion. For digital to analog conversion, the least significant bit is processed first. If the input bit is one, the reference is added to the temporary result and the sum is divided by two. Next, the reference is refreshed by passing it through the same loop that the signal goes through. Unlike the A/D, the loop gain of the D/A is one half instead of one. Therefore, in order to achieve the unity loop gain for the reference voltage in the D/A conversion, the reference voltage will adopt the change path procedure to have a effective gain of one. For the same reason as for the A/D converter, reference refreshing must be interleaved during the construction of the analog output. By implementing the above correction method, the D/A's transfer curve can also be independent of capacitor mismatch and op-amp gain. A comparison of a 3 bit D/A transfer curve which has first order error of 10% with and without the reference refresh technique is shown in Fig. 3.11.

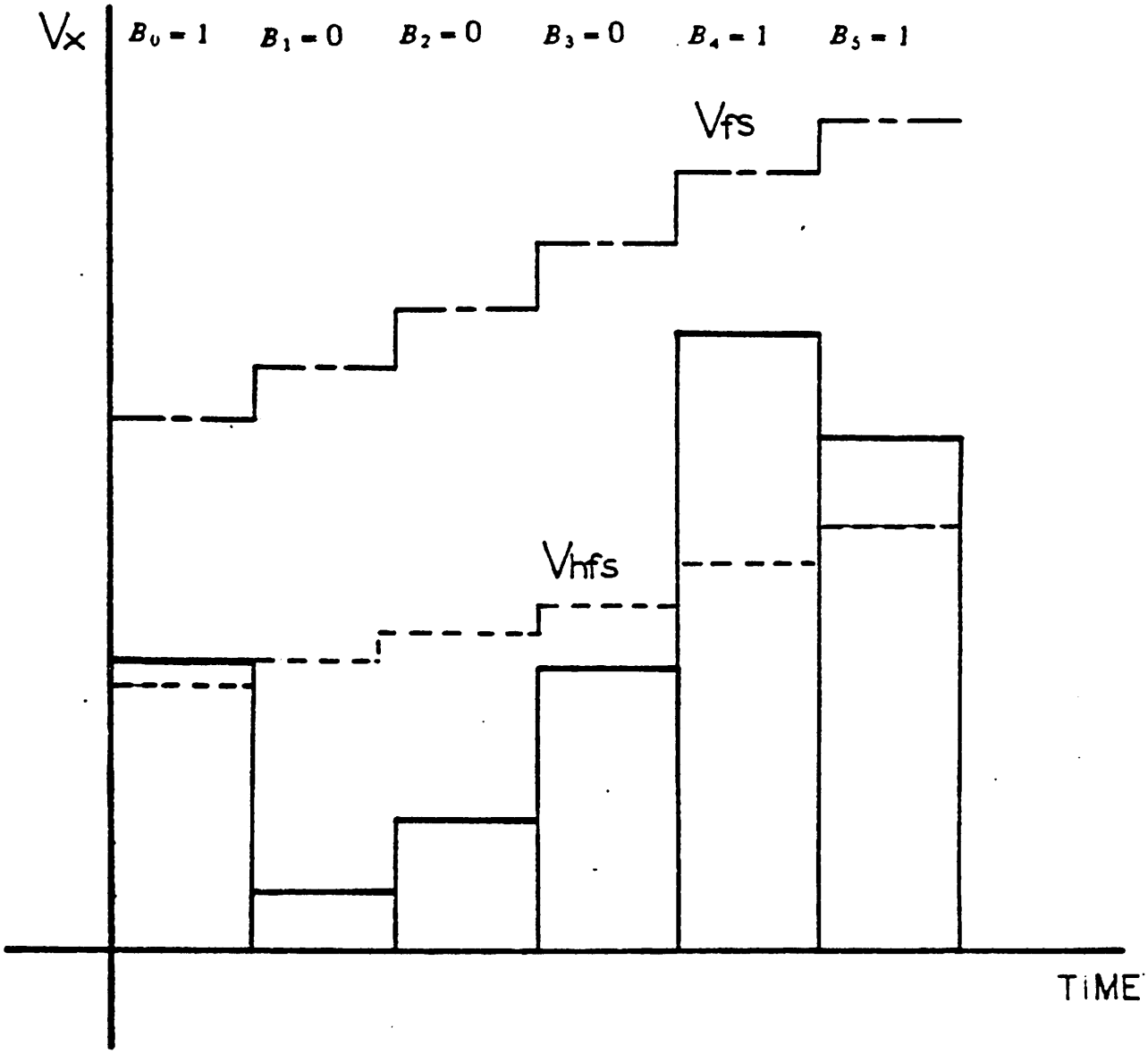


Fig 3.9 An example of internal voltage variation of a 6 bit converter with $E_1 = .1$ after the reference recirculation technique.

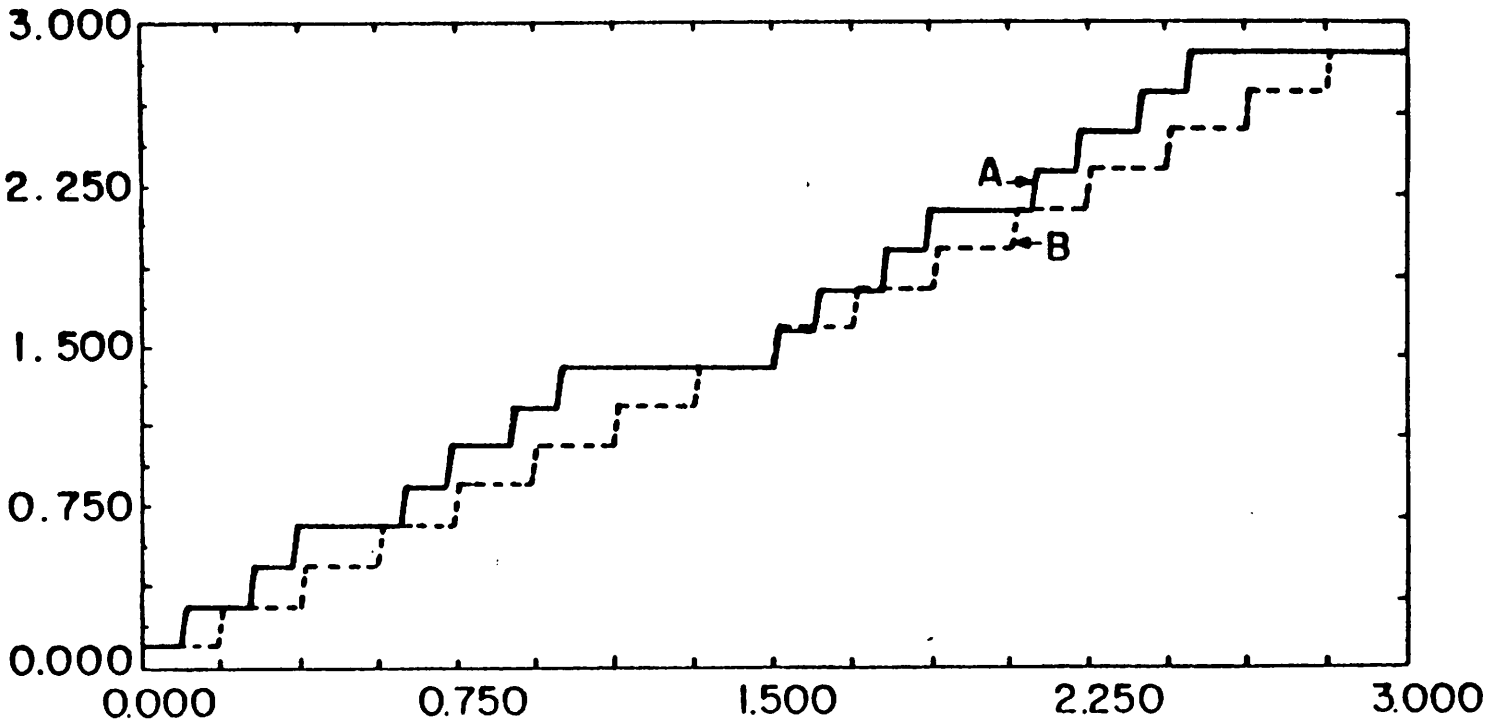


Fig 3.10 A simulation result of a 3 bit A/D transfer curve
(a) before reference refreshing
(b) after reference refreshing

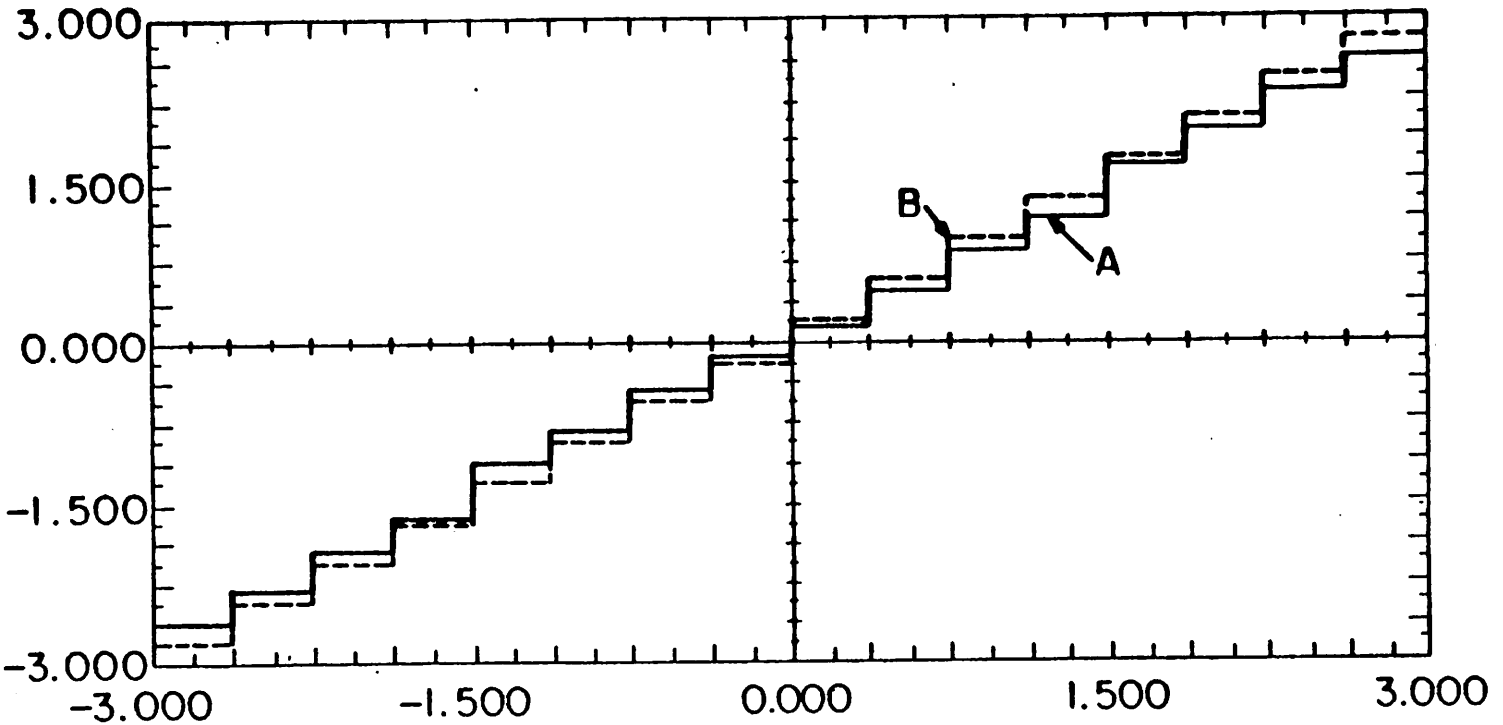


Fig 3.11 A simulation result of a 3 bit D/A transfer curve using the reference refreshing approach

(a) before reference adjustment

(b) after reference adjustment

One side effect of the D/A conversion by using the reference recirculation method is that the analog output of the D/A converter will display a constant D/A transfer curve gain error. This occurs because the effective reference voltage at the end of the digital-analog conversion is the original reference multiplied by the ratio error raised to the N power where N is the number of bits. This voltage sets the full-scale voltage for the DAC. However, this error can be easily corrected by adjusting the voltage reference according to the loop gain error.

3.5. Offset Voltage Storage Technique

The E_0 term in eq. 3.4 is majorly coming from offset voltage of the amplifiers in the loop. Basically, the offset voltage of an operational amplifier (op-amp) composes of two component, the *systematic offset* and the random offset. The systematic offset results from the circuit design and occurs even when every supposedly matched devices in the circuit are identical. On the other hand, the *random offset* is caused by the mismatch between those supposedly matched pairs of devices.

Systematic Offset Voltage

In bipolar technology, the comparatively high voltage gain per stage makes the input referred dc offset voltage of an op-amp only depend on the design of the first stage. But generally in MOS op-amps, because of the relative low gain per stage, the offset of the differential to signal ended converter and second stage can play a important role. Assuming a two stages MOS amplifier with perfectly matched devices, if the inputs of the first stage are grounded, the quiescent voltage at the output of the first stage may be different from the quiescent voltage that is required to force the amplifier output voltage to zero. For a first stage gain of 50, for example, each 100 mV difference in these voltage results in 2 mV of input referred systematic offset.

Random Input Offset Voltage

Source-coupled pair of in MOS technology normally exhibits higher offset voltage than an emitter coupled differential pair in bipolar technology with the same level of geometric mismatch or process gradient. Any kind of differential input stage load devices mismatch requires an input offset voltage to force the output to have zero output. Suppose the load devise mismatch percentage is Δ, the offset voltage V_{os} will have to be

$$V_{os} = \frac{I}{g_m}\Delta$$

The input offset voltage actually depends on the $\frac{I}{g_m}$ ratio of the input device and the fraction of mismatch between matched devices. For MOS transistor, the $\frac{I}{g_m}$ ratio is $\frac{(V_{gs}-V_T)}{2}$ which normally has the value around 100-500 mV. Although minimizing the V_{gs} can improve the offset voltage, the $\frac{I}{g_m}$ value also determines the slew rate of the op-amp which sets the lower limit for the improving of the offset voltage.

On the other hand, the threshold voltage of a MOS devise is determined by the threshold adjustment implantation instead of determined by the energy gap between P-N junction. This adding another factor of mismatch component into the MOS amplifier which is the threshold voltage difference between two matched devises. Normally a large geometry and common centroid structure can minimize the threshold voltage standard deviation to the order of 2mV.

Offset Sampling Technique

The operational amplifier chosen in this design is a fully differential single stage folded cascade structure. There is no systematic offset for this kind of amplifier. By adding up the possible effects from the matched devices and different threshold voltage, the calculated input offset voltage for the amplifier used in this project is in the range of 10mV. Because a LSB for a 13 bit A/D with 10 V full scale input is only 1.22 mV. This offset value is corresponding to 9 LSB and will limit the accuracy of the A/D to

approximately 10 bits. In order to eliminate offset, an extra pair of capacitors is used in front of the op-amp. Proper switch sequencing stores and maintains the offset value on these capacitors. In effect, they can be viewed as voltage sources that cancel out the inherent offset voltage of the op-amp. The procedure that implements the offset cancellation is shown in Fig 3.12. Because of the periodic sampling of the offset voltage, this method also behaves as a double correlated noise reduction technique[Hsie81, Brod76]. Noise with power spectrum below half of the offset sampling rate is eliminated by the offset sampling technique. Consequently, 1/f noise, significant in MOS amplifiers, is also mostly eliminated.

3.6. Description of Operation

The interleaved signal and reference for the A/D conversion are shown in Fig 3.13a-i. In the initial cycle of the conversion, all the op-amp offsets are sampled on the offset sampling capacitors by closing the loop around the op-amp and grounding the top plates of the offset sampling capacitors (Fig 3.13a). In Fig 3.13b, The input signal is sampled on C_3 and the C_4 is cleared at the same time. Then by closing the SW 11, the charge on C_3 is transferred to C_4. The sign of the signal is determined at this stage (Fig 3.13c). After the sign bit is determined, the proper polarity of the reference voltage is sampled onto C_1 and the C_2 is cleared at the same time (Fig 3.13d). Fig 3.13e shows the reference has been transferred to C_2 by closing SW 7. In the next cycle (Fig 3.13f), both the signal and the reference are separately sampled on C_1 and C_3 and transferred to C_2 and C_4. The subtraction function is performed by changing the voltage on the bottom plate of C_5 voltage from ground to reference (Fig 3.13g). Then the remainder is compared with ground to determine the most significant bit. In Fig 3.13h, the remainder and the reference are again sampled onto the next stage. Since the remainder needs to be multiplied by two, instead of connecting the bottom plate of C_3 to ground, the bottom plate of C_3 is tied to the opposite polarity of the signal (Fig

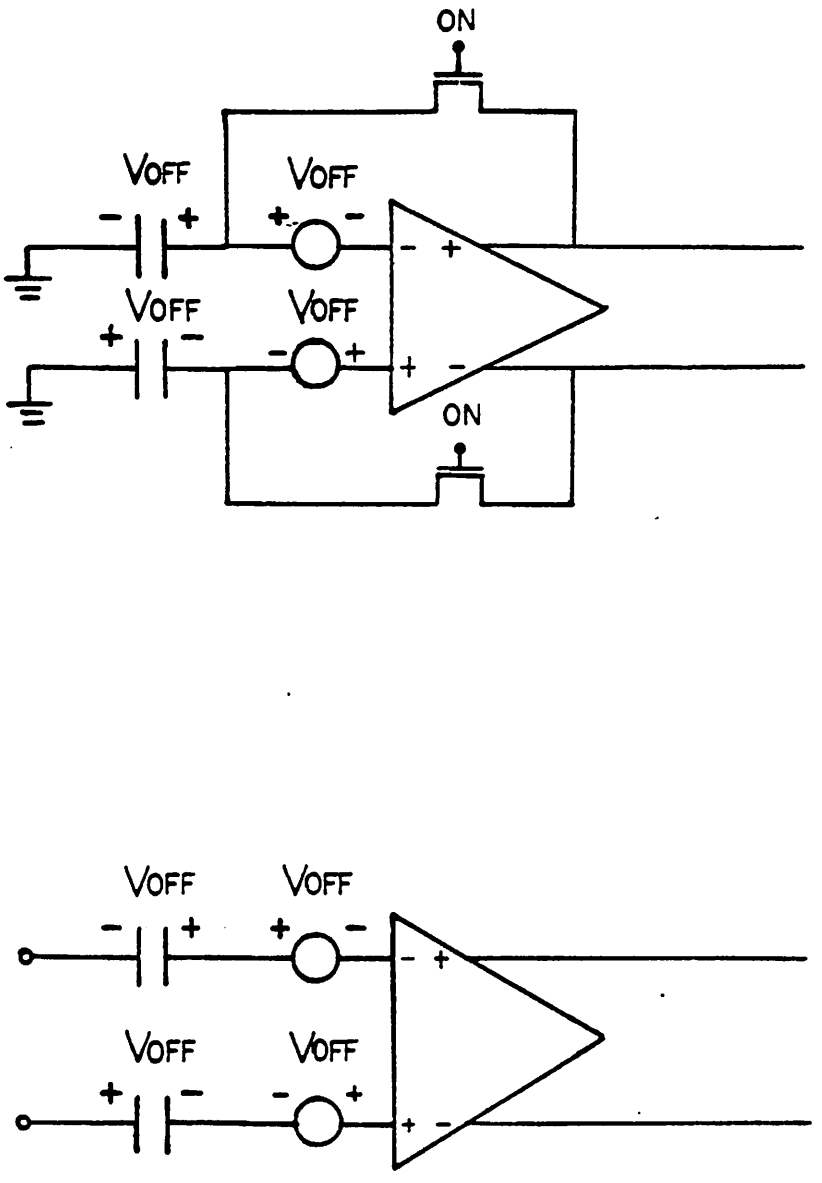
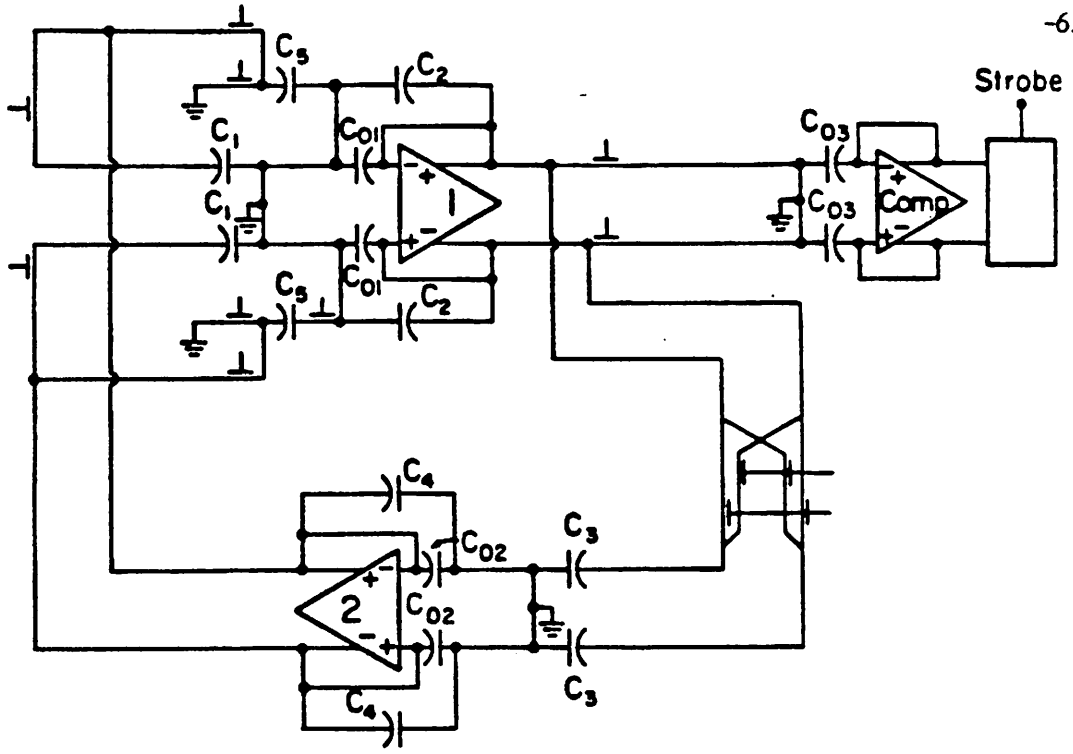
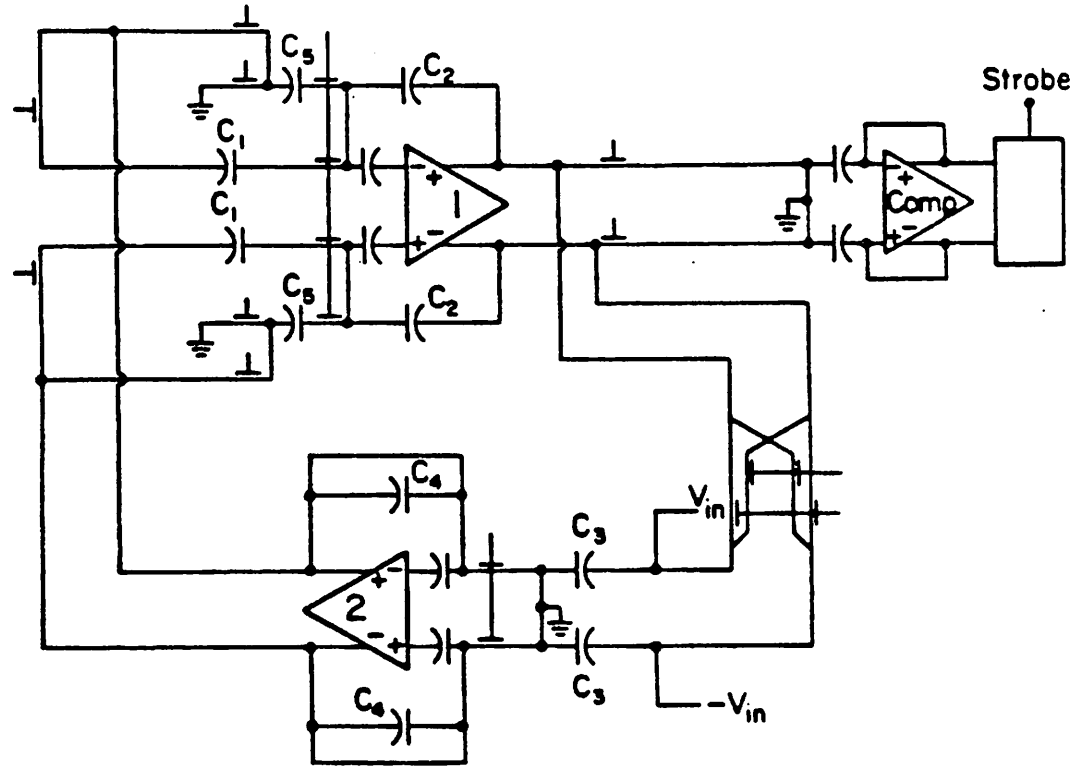


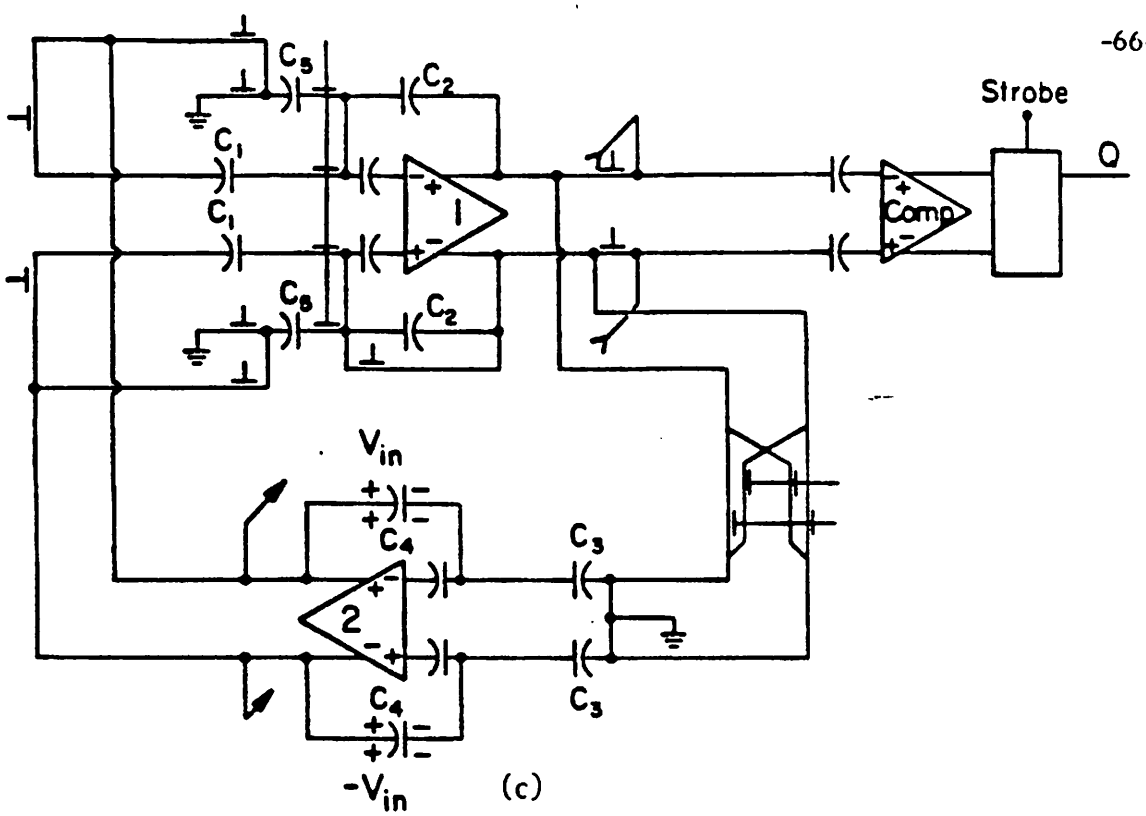
Fig 3.12 A demonstration of offset sampling technique with offset sampling capacitor.
(a) The offset is sampled on the offset sampling capacitor(C_{off})
(b) After turning off the switches, the offset voltage stored on C_{off} removes the op-amp's offset



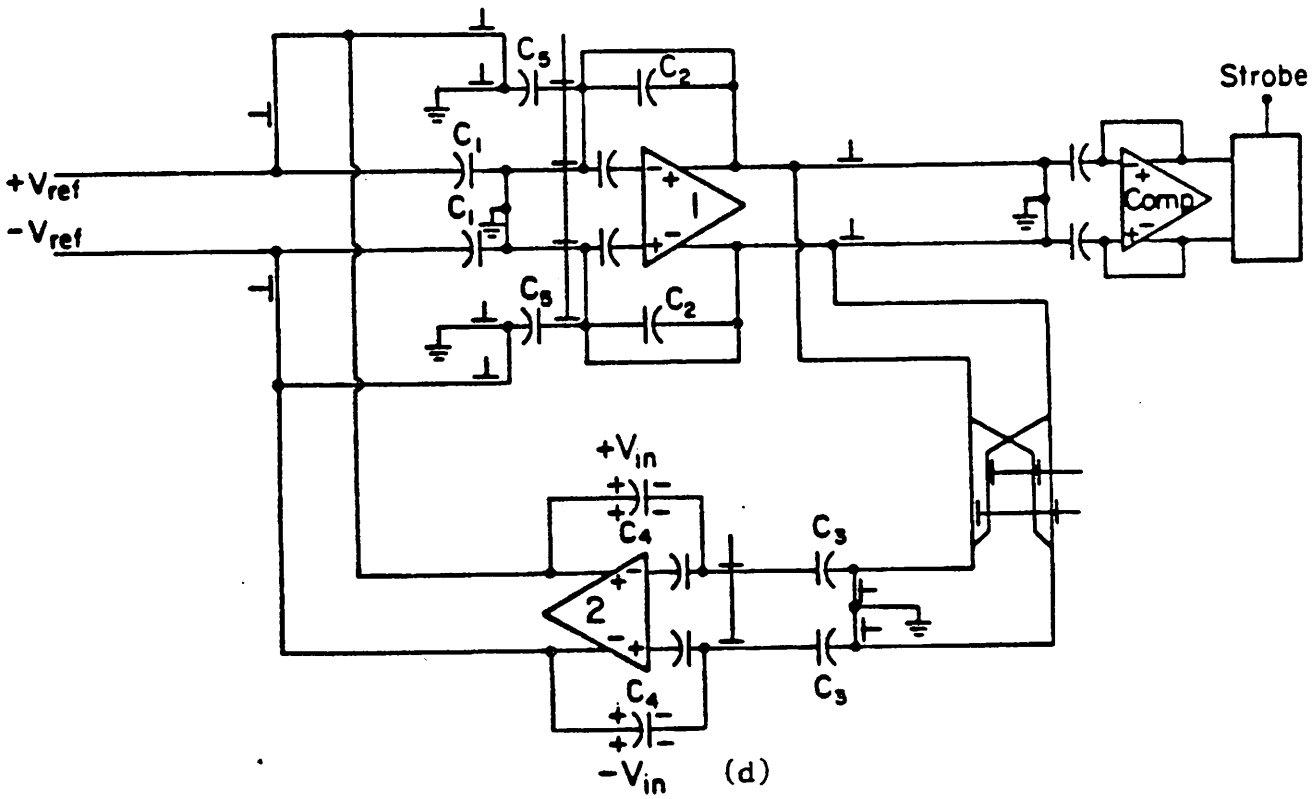
(a)



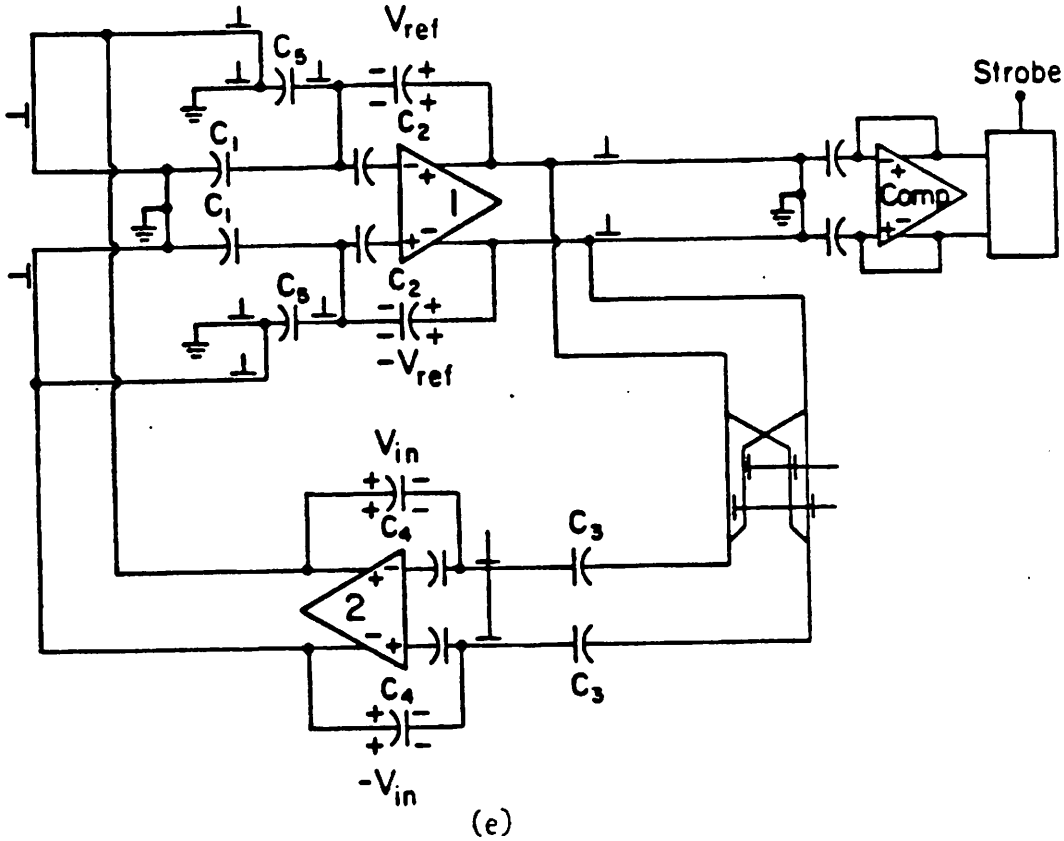
(b)


C5
C2
C1
C1
1
Comp
Strobe
Q
C5
C2
Vin
C4
C3
2
C4
C3
-Vin

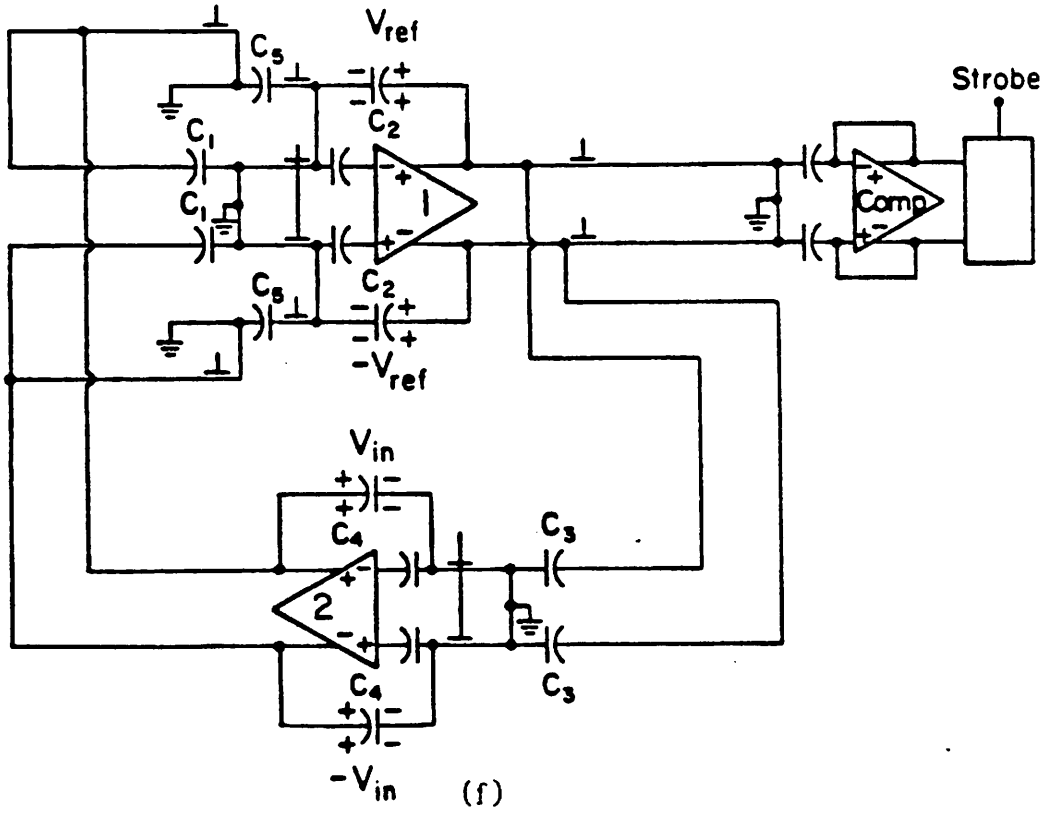
(c)


C5
C2
Strobe
C1
+Vref
C1
-Vref
1
Comp
C5
C2
+Vin
C4
C3
2
C4
C3
-Vin

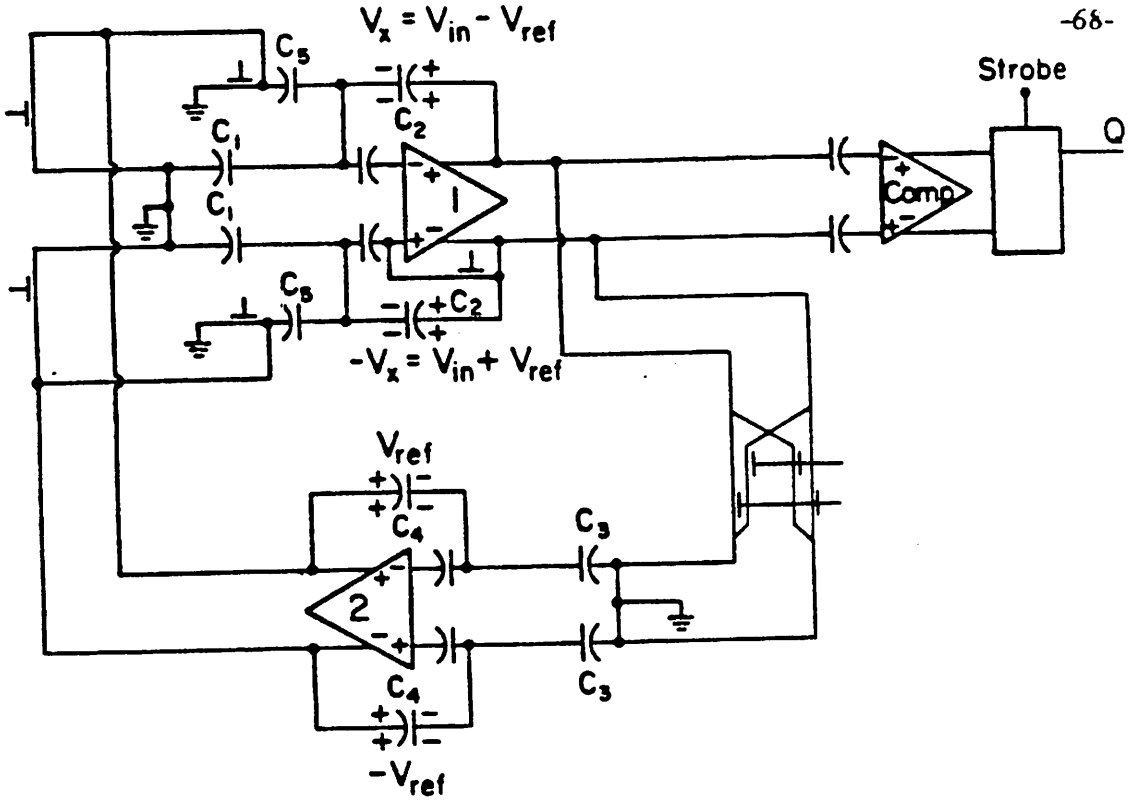
(d)


Vref
C5
C1
C2
Strobe
Comp
1
-Vref
Vin
C4
C3
2
-Vin

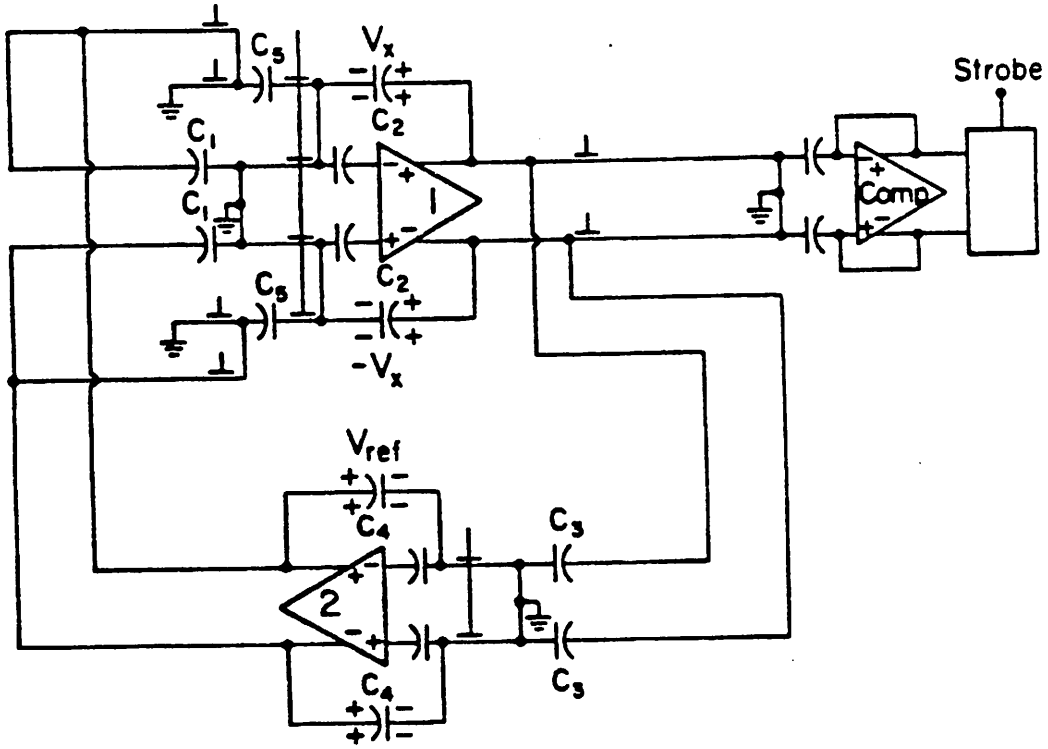
(e)


Vref
C5
C1
C2
Strobe
Comp
1
-Vref
Vin
C4
C3
2
-Vin

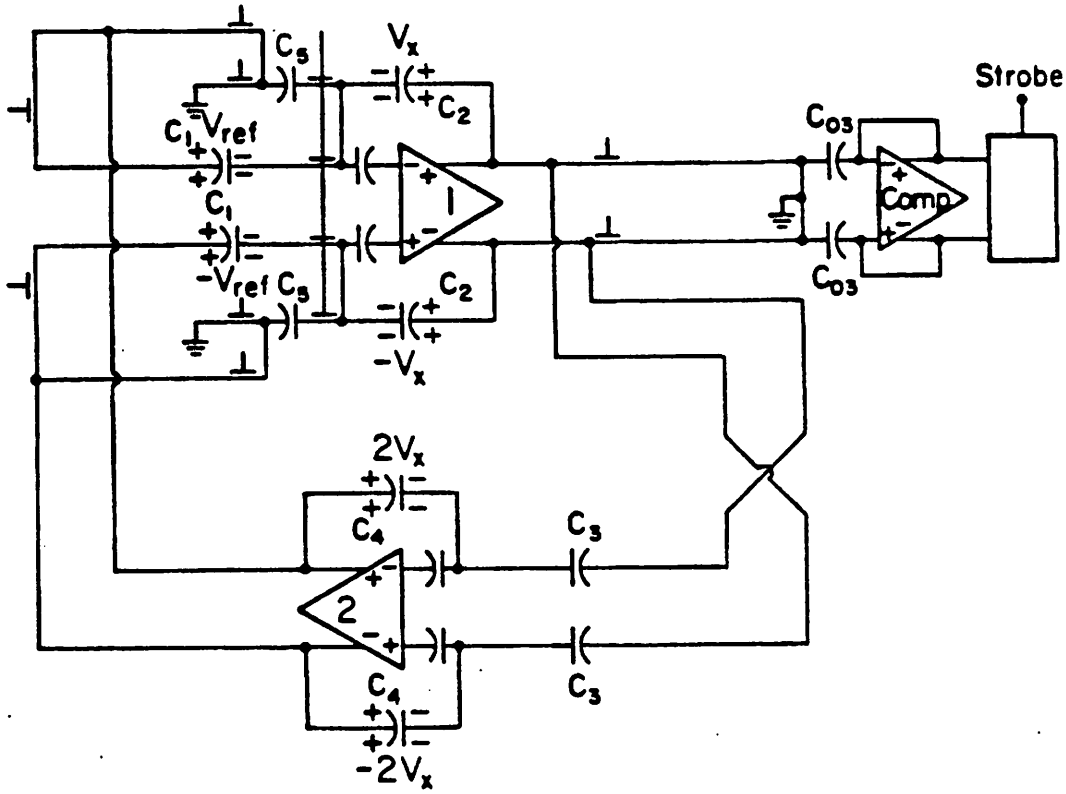
(f)


$V_x = V_{in} - V_{ref}$
C_5
C_1
C_1
C_2
1
C_5
C_2
$-V_x = V_{in} + V_{ref}$
Strobe
Q
Comp
V_{ref}
C_4
C_3
2
C_4
C_3
$-V_{ref}$

(g)


C_5
V_x
C_1
C_2
1
C_1
C_5
C_2
$-V_x$
Strobe
Comp
V_{ref}
C_4
C_3
2
C_4
C_3
$-V_{ref}$

(h)



(i)

Fig 3.13 The signal and reference flowing sequence for the A/D conversion

(a) Offset sampled on C_{o1}, C_{o2} and C_{o3}

(b) The input is sampled on C_3

(c) The input is transferred to C_4 and the sign bit decision is made

(d) According to the sign bit outcome, the proper polarity of the reference is sampled on C_1

(e) The reference is transferred to C_2

(f) Both the signal and the reference are sampled and then transferred to the next stages

(g) If necessary, the reference is subtracted through C_5

(h) Again the reference and the remainder are transferred to the next stage

(i) The remainder is multiplied by two

3.13i). Repeatly following the procedures in Fig 3.13f-i, a 13 bit A/D completes its conversion in 13 cycles. Thus the reference refreshing procedure is interleaved in between the normal cyclic conversion. Both the input signal and the reference have to pass through the loop same number of times. Each time the most recently refreshed reference is used to generate the correct decision level.

Basically, D/A conversion follows the same general rules as for A/D conversion.

3.7. Computer Simulation Results

Computer simulations of the absolute error of the circuit with loop gain error of 5% are shown with solid line (i) in Fig 3.14. It can be seen that the largest error occurs at the major carry. The effect of the loop gain error is reduced by two at with the second carry and by four at the third carry. In Fig 3.15, the enlarged transfer curve around the major carry is plotted to magnify the effect of positive and negative loop error which produces large differential nonlinearity or a missing code respectively. The simulation also shows the voltage difference between the real input and the output from the A/D converter assuming an ideal D/A is used. The absolute error curve after implementing the reference recirculation method on a 13 bit A/D with loop gain error of 5% is shown by the doted line (ii) in Fig 3.14. The reference refreshing approach does remove the problem caused by the capacitor mismatch and low amplifier gain . Furthermore, figures 3.16 and 3.17 show that even the high order errors in the transfer equation 3.4 are improved by using the reference refreshing method.

3.8. Comparison with other ratio independent techniques

Ratio-independent multiplication-by-two method

Ratio-independent multiplication-by-two[Li84] is also a modified version of the algorithmic converter. By interchanging the sampling and integrating capacitors during the second integration and having the charge redistributed among these capacitors, the

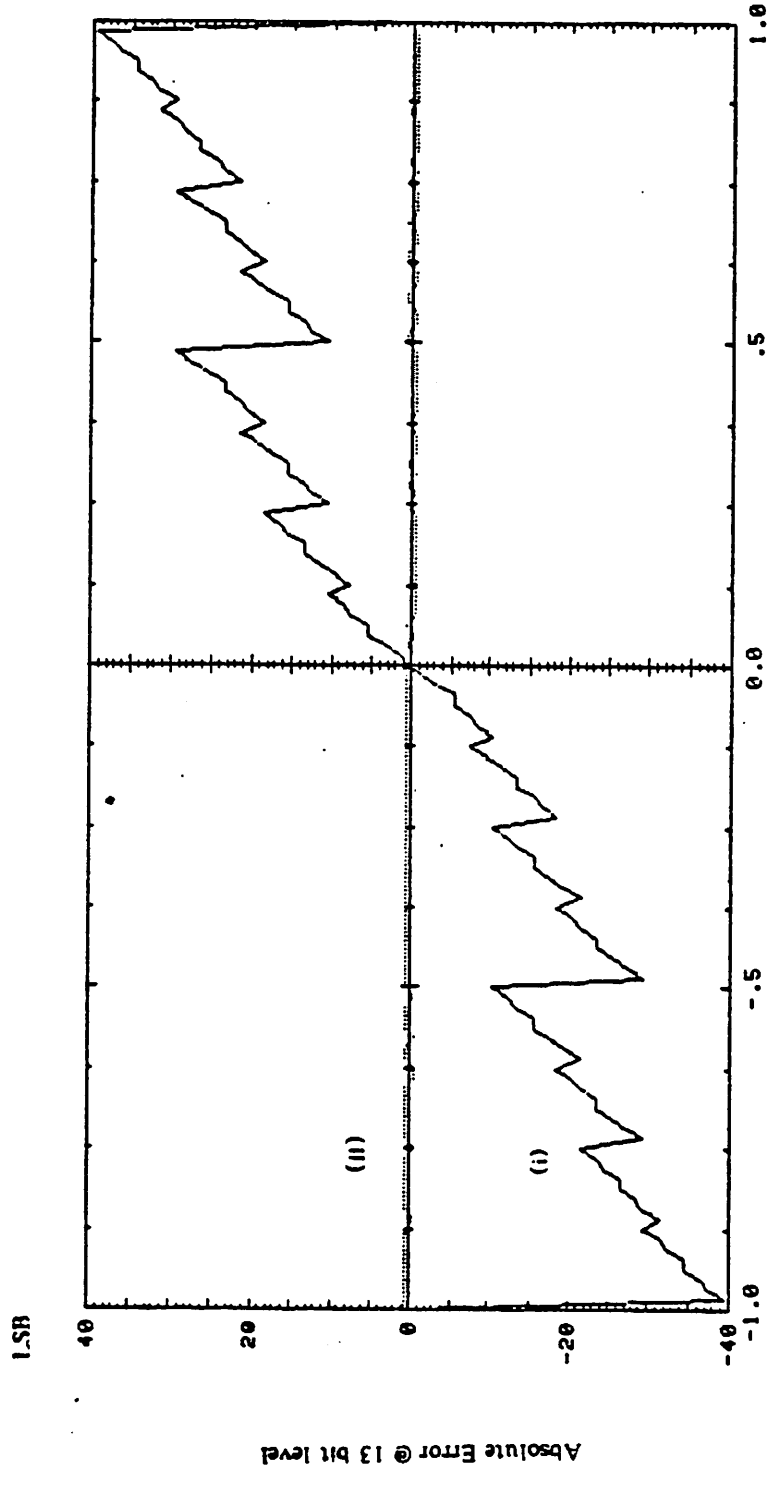


Fig 3.14 Absolute error of a 13 bit cyclic conversion with E_1 = .005
(i) before reference refreshing
(ii) after reference refreshing

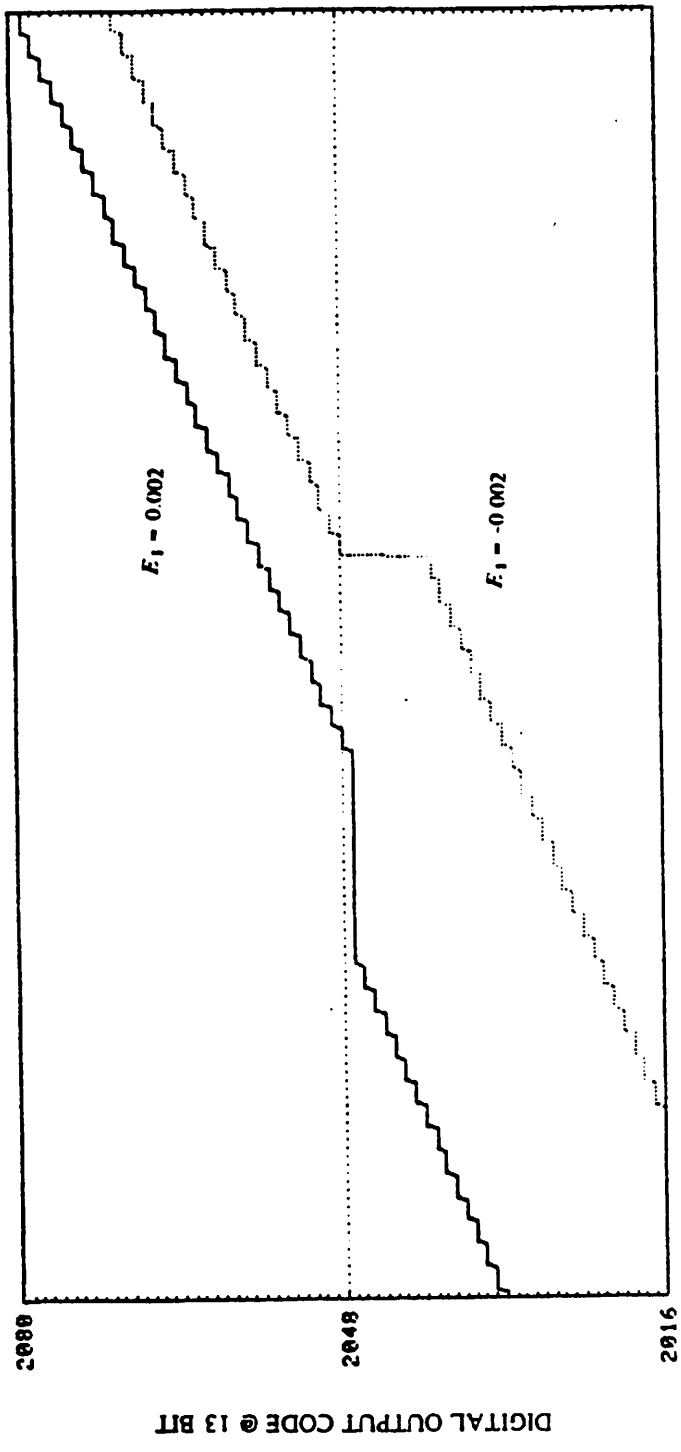


Fig 3.15 The enlarged transfer curve around the major carrier with positive and negative loop gain respectively

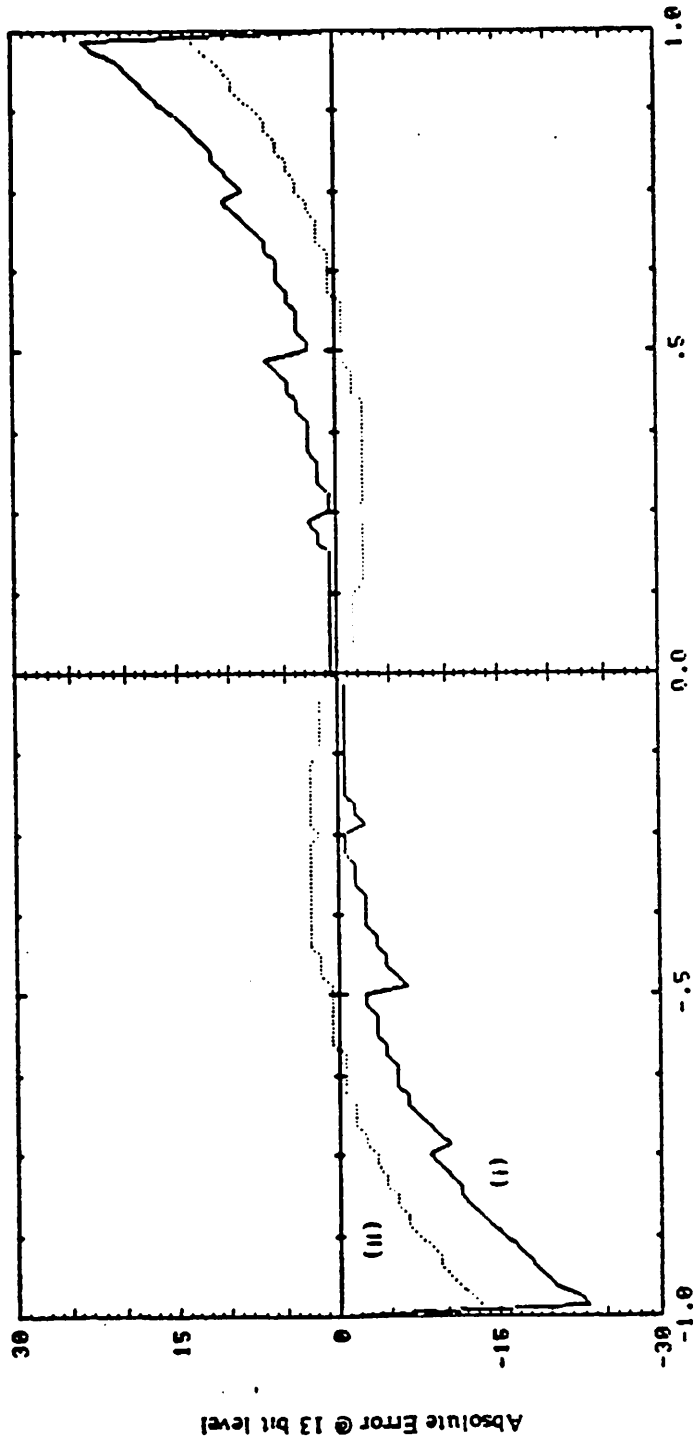


Fig 3.16 Absolute error of a 13 bit cyclic conversion with $E_2 = .01$
(i) before reference refreshing
(ii) after reference refreshing

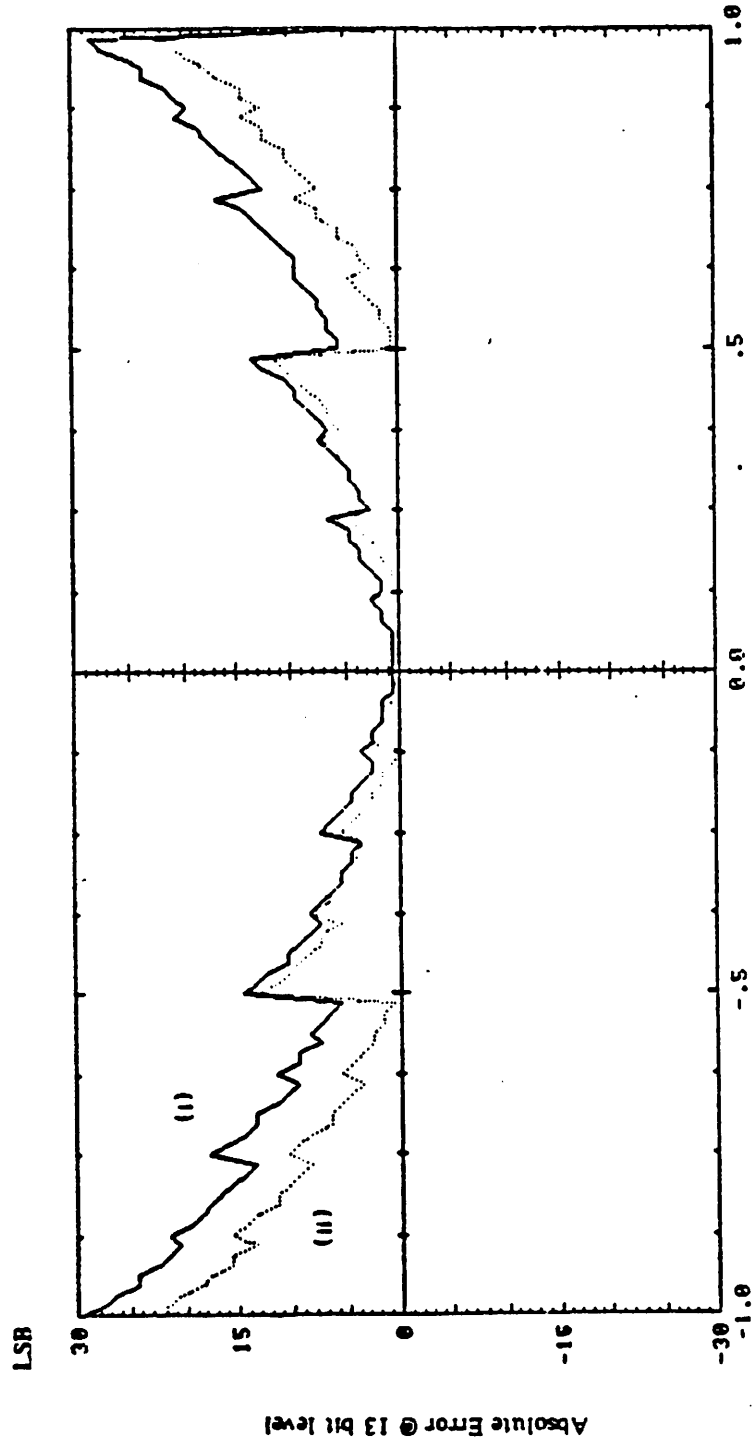


Fig 3.17 Absolute error of a 13 bit cyclic conversion with $E_3 = .01$
(i) before reference refreshing
(ii) after reference refreshing

ratio of these capacitors will not affect the accuracy of the multiplication. For the sample and hold, by using the same capacitor for both sampling and feedback, there does not exist the matching problem. Both of these approachs based on the assumption that the operational amplifier have an infinite gain.

So comparing the reference refreshing approach with ratio independent multiplication by two method, the former approach has three major benefits:

(1) There is no high gain requirement for the reference refreshing technique. With any reasonable gain op-amp, the reference refreshing converter can still eliminate the loop gain error.

(2) The ratio-independent multiplication-by-two method can only work for the A/D but not for D/A. Therefore in many cases when both converters are needed, the reference refreshing technique is a better choice.

(3) The ratio independent multiplication by 2 modification only improves the problem that is generated by the capacitors matching. The reference refreshing converter not only corrects the first order errors but also partially cancels some high order error in the loop.

Although the reference recirculation conversion method seems more complicated than normal cyclic conversion, generally the reference recirculation method requires little extra circuit complexity and cause little loss of speed in the conversion. It does not take any extra time to refresh the reference because that it is parallelly processed with the signal.

Self calibration A/D converter

A method to correct the linearity error of a monolithic successive approximation A/D converter through the use of digital algorithm and an extra calibration DAC was recently introduced by Harry Lee and David Hodges[Lee84]. At each power up period, this converter goes through a calibration cycle using its calibration DAC to measure the

linearity error in the capacitor array and store the results into a memory. After the calibration cycle, the converter starts to perform the conversion, and during the conversion process the error information is used to correct the nonlinearity of the capacitor array. With this digital correction, the performance of the A/D has been improved to 15 bit resolution. In order to achieve high accuracy, the capacitor array still must have reasonable matching because the range over which the correction can occur is limited. The reference refreshing technique can be viewed as an analog self calibration method for which no initial calibration cycle is performed. Instead, the converter interleaves the conversion and calibration operation. The chip area needed for reference refreshing A/D is also much smaller than that of the self calibration A/D converter.

3.9. Comparison with oversampled A/D converter

The oversampled A/D converter samples the input signal at a much higher rate than the Nyquist rate and then uses simple analog circuitry to convert the analog signal to digital code. A sophisticated digital filter is used to remove the quantization noise of the digital code so that the code after the filtering has a much higher resolution. The detailed operation has been explained in the previous chapter.

Although few precision analog components are needed in oversampled converter[Haus], the digital filter takes up so much area that it is not practical to implement with 3u technology. With less than 1 μ technology, however, the chip size will probably be comparable with that of a cyclic converter. Using the double integration $\Sigma-\Delta$ approach, the study concluded that the loop gain should be carefully controlled. In another words, precision capacitor matching still has to be mentioned in this $\Sigma-\Delta$ converter. Furthermore, the oversampled converter performance depends heavily on the input signal characteristic. Use of this converter would require a careful study of the compatibility of this conversion with the whole system.

CHAPTER 4

OTHER ACCURACY CONSIDERATIONS

In the previous chapter, the two most important problems in the realization of the high resolution converter using switched capacitor techniques have been pointed out and solutions have also been described. In this chapter, some second order error sources that exist in the circuit will be described. Possible solutions to reduce magnitude of the effects are also given for some of the problems. This subject is important because, after implementing the reference refreshing technique described in the previous chapter, the second order errors limit the highest achievable accuracy of the converter.

The effect of clock feedthrough is described in the first section. In the second section, the effects of residual offset errors and some methods to reduce the distortion are examined separately for both the comparator and the amplifier offset. In section 3, all noise sources in the converter and their influence on the conversion process are discussed. In the last three sections, the effects on the conversion of stray capacitance on the summing nodes, voltage dependent capacitors and capacitor dielectric relaxation are explored.

4.1. Unbalanced Charge Injection and Clock Feedthrough

A sample and hold circuit is considered difficult to design in bipolar technology but can be implemented in MOS technology with only a MOS switch and a capacitor. Because of the inherent high input impedance of a MOS transistor gate, the charge on a capacitor can be nondestructively sensed. One possible error source in this sampling process comes from the sampling switch. While turning off the sampling switch, some of the channel charge under the switch is injected onto the capacitor. Furthermore, the

gate voltage variation is also coupled through the overlap capacitance to the sampling capacitor. Both of these phenomena will distort the sampled signal. In the following paragraphs, these distortions are analyzed.

4.1.1. The Modeling of the Unbalance Charge Injection and Clock Feedthrough

Consider the circuit shown in Fig 4.1. The sampling transistor will go through two different operation regions while the gate voltage of the switch is changed from high to low. First, when $V_g \geq V_{in} + V_t$, the switch is in linear region and there is a resistive channel between the drain and source. An equation relating the variation of the drain voltage to other circuit parameters is as follows:

$$C_S \frac{dv_d}{dt} = -i_d + (C_{ol} + \frac{C_{gate}}{2}) \frac{d(V_g - V_{in} - v_d)}{dt} \tag{4.1}$$

Substituting the Shichman-Hodges channel model (Fig 4.2), then the above equation can be replaced by

$$C \frac{dv_d}{dt} = -\beta(V_H - V_{in} - V_t - St)v_d + (C_{ol} + \frac{C_{gate}}{2})S \tag{4.2}$$

where

S : gate voltage ramp rate (dV sub g over dt)

$\beta : \mu_n C_{ox}' \frac{W}{L}$

C_{gate} : gate capacitance (WL C_{ox}')

C_S : sampling capacitor

C_{ol} : overlap capacitor

$C : C_S + C_{ol} + \frac{C_{gate}}{2}$

V_t : threshold voltage which is a function of V_{bulk} and v_d

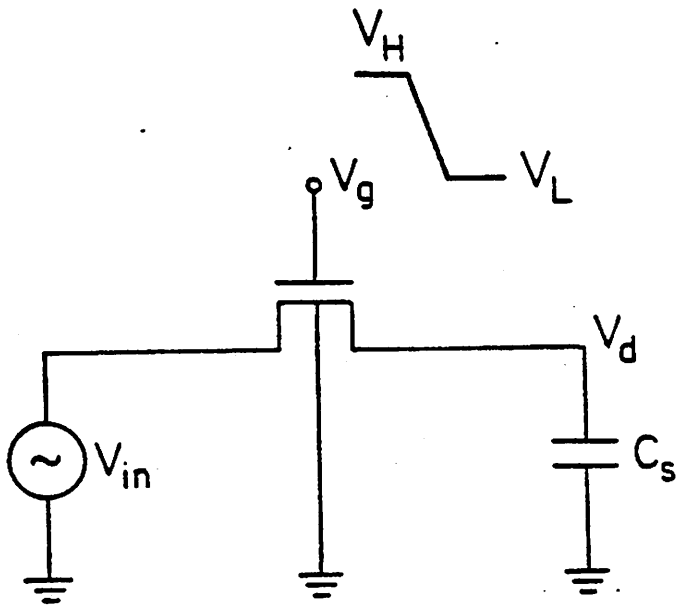


Fig 4.1 An example of only one switch and one capacitor sample and hold circuit

By assuming the initial condition $v_d(0) = 0$, the closed form of the above differential equation is as follows.

$v_d(t) =$

$$(C_{ol}+\frac{C_{gate}}{2})\sqrt{\frac{\pi S}{2\beta C}}e^{(\frac{\beta S}{2C})(t-\frac{V_H-V_{in}-V_t}{S})^2}[erf(\sqrt{\frac{\beta}{2SC}}(V_H-V_{in}-V_t))-$$

$$erf(\sqrt{\frac{\beta}{2SC}}(V_H-V_{in}-V_t-St))] \quad (4.3)$$

At the time $t' = \frac{V_H-V_{in}-V_t}{S}$, $V_g = V_{in} + V_t$, the sampling transistor goes to cutoff region and the above equation will no longer be valid. The error voltage at this time is

$$v_{d-on} = v_d(t') = (C_{ol}+\frac{C_{gate}}{2})\sqrt{\frac{\pi S}{2\beta C}}erf(\sqrt{\frac{\beta}{2SC}}(V_H-V_{in}-V_t)) \quad (4.4)$$

For $V_g \leqslant V_{in}+V_t$, the equivalent circuit is shown in Fig 4.3. The error voltage generated in this period is simply the overlap capacitor coupling error.

$$v_{d-off} = \frac{C_{ol}}{C_S}(V_{in}+V_t-V_L) \quad (4.5)$$

Combining the errors from these two regions, the total error voltage from the sampling switch at the end of the sampling process is.

$$v_d = (C_{ol}+\frac{C_{gate}}{2})\sqrt{\frac{\pi S}{2\beta C}}erf(\sqrt{\frac{\beta}{2SC}}(V_H-V_{in}-V_t))+\frac{C_{ol}}{C_S}(V_{in}+V_t-V_L) \quad (4.6)$$

The error function erf(x) can be approximated by 1 when x >> 1, or by $\frac{2x}{\sqrt{\pi}}(1-x^2)$ when x << 1. When the technology is given, it can be seen from Eq (4.6), that a free variable is the gate voltage ramp rate (S).

With a slow ramp, $S \ll \frac{\beta(V_H-V_{in}-V_t)^2}{2}C$, replace the erf(x) by 1. Eq (4.6) can be simplified to:

$$v_d \approx (C_{ol}+\frac{C_{gate}}{2})\sqrt{\frac{\pi S}{2\beta C}}+\frac{C_{ol}}{C_S}(V_{in}+V_t-V_L)$$

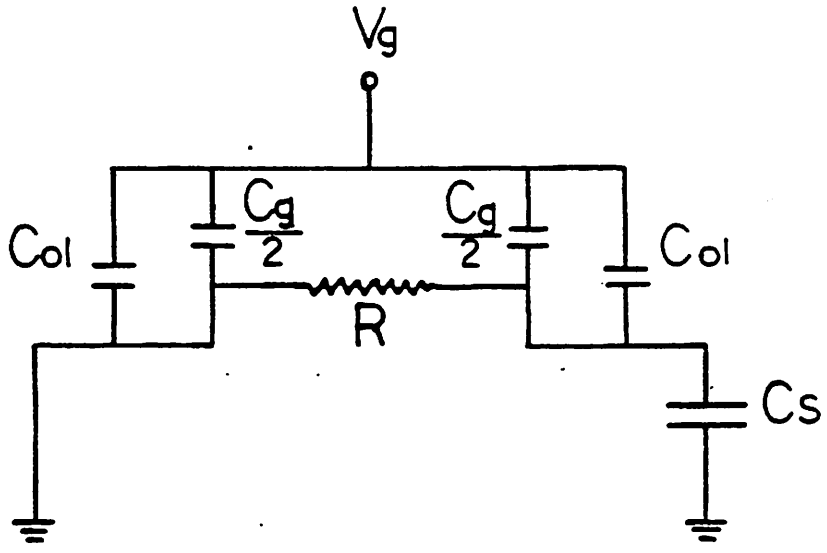


Fig 4.2 Replace the switch with Shichman-Hodges channel model. when $V_g \geq V_{in} + V_t$

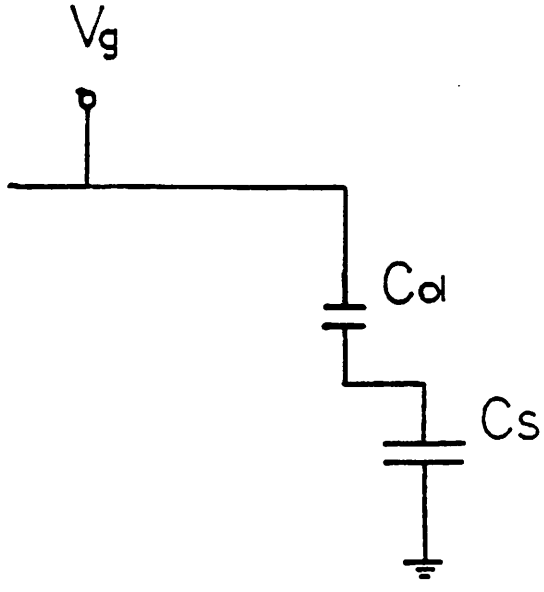


Fig 4.3 Replace the switch with the overlap capacitor only. when $V_g < V_{in} + V_t$

$$\approx[(C_{ol}+\frac{C_{gate}}{2})\sqrt{\frac{\overline{\pi S}}{2\beta C}}+\frac{C_{ol}}{C_S}(V_t-V_L)]+[\frac{C_{ol}}{C_S}]V_{in} \qquad (4.7)$$

With a fast ramp, $S \gg \frac{\beta(V_H-V_{in}-V_t)^2}{2}C$, replace erf(x) by $\frac{2x}{\sqrt{\pi}}(1-x^2)$, Eq (4.6) can be simplified to:

$$v_d \approx \frac{(C_{ol}+\frac{C_{gate}}{2})}{C}[(V_H-V_{in}-V_t)-\frac{\beta}{6SC}(V_H-V_{in}-V_t)^3]+\frac{C_{ol}}{C_S}(V_{in}+V_t-V_L)$$

$$\approx[\frac{(C_{ol}+\frac{C_{gate}}{2})}{C}(V_H-V_t)+\frac{C_{ol}}{C_S}(V_t-V_L)]+[-\frac{(C_{ol}+\frac{C_{gate}}{2})}{C}+\frac{C_{ol}}{C_S}]V_{in} \qquad (4.8)$$

In the above equations, the V_t term also depends on the drain voltage. However, with small v_d, the threshold voltage can be considered as a constant voltage during the process.

By going through the analysis of this simple sampling circuit, there are a few facts that are concluded.

(1) In order to get some meaningful insights into this phenomena, the extreme cases of the gate clocking are considered. In equations (4.7) and (4.8), the error can be separated into two parts. The first part is independent of the sampled input magnitude. Therefore, this term acts like an extra offset from the sampling process. The second part is a signal dependent error that in most cases is linearly related to the input signal. With these characteristics, the second term acts as a gain error to the signal being sampled.

(2) The sampling error is proportional to the sizes of both the sampling capacitor and the sampling switch. Thus, the absolute sampling error can be reduced by either increasing the sampling capacitor or decreasing the switch size.

4.1.2. Corrections for Charge Injection Error

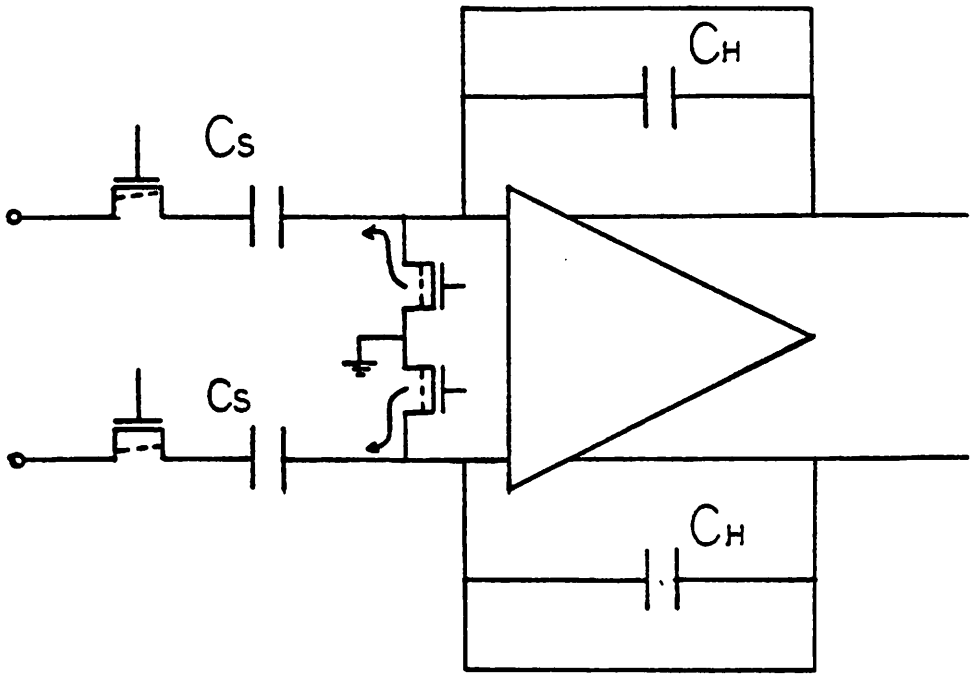
As the sampling capacitor is reduced to save the die area , the charge injection and clock feedthrough error becomes more and more significant in terms of voltage error. In this project, the sampling capacitor is chosen to be only 2 pF and the clock feedthrough is expected to be in the 10 mV range which corresponds to several LSB's level at 13 bit resolution. So several steps are taken to eliminate this distortion.

(1) By using a fully differential circuit , any signal independent offset error caused by the symmetrical switch pair appears as a common mode input signal and is rejected by the differential input stage.

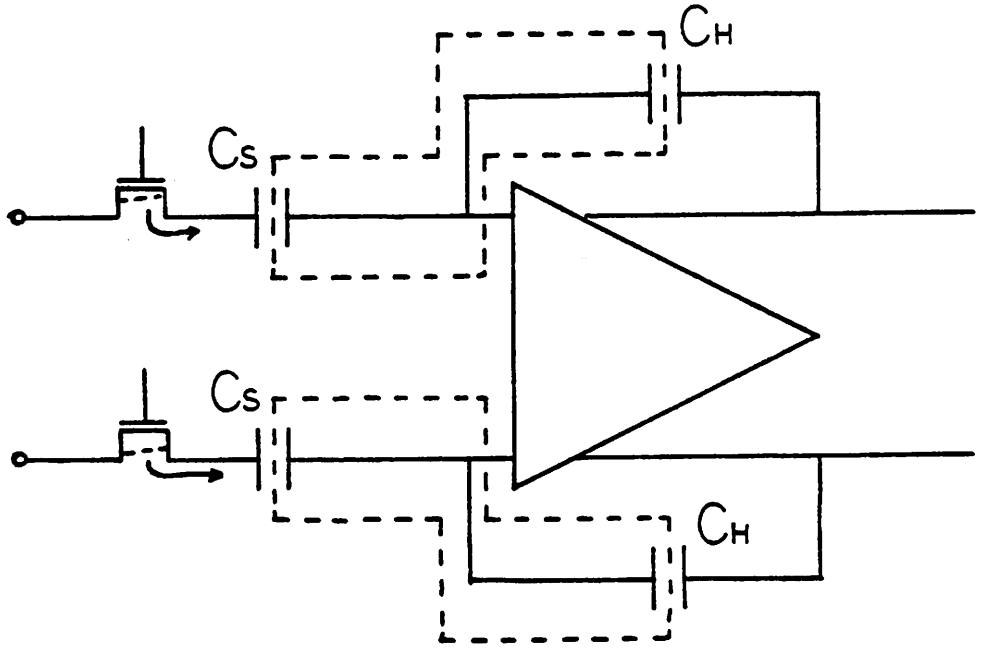
(2) The reference refreshing approach theoretically eliminates all gain error in the cyclic loop. By examining Eq (7) and (8), it can be seen that a part of the clock feedthrough is linearly related to the input signal and can be corrected by the reference refreshing approach.

(3) By modifying the sampling process clocking sequence, high order input dependent distortion can also be corrected. Now in Fig 4.4, instead of turning switch SW1 and SW2 at the same time, switch SW2 is turned off first. After SW2 is opened, the input nodes of the amplifier are totally isolated from external input. Because the sources of the SW2 pair are both tied to ground, the clock feedthrough from both transistors in the SW2 pair is the same and behaves as common mode signal to the differential amplifier. When SW1 pair is turned off at the next instant, all the clock error can only distort the charge on the bottom plate of C_1. It can not affect the charge that has been stored between C_1 and C_2.

(4) The magnitude of the charge injection effect also depends on the impedance looking back from the drain and source. Because both positive and negative voltages can appear at the drain of SW1 , a complementary switch is required to assure approximately constant on resistance of the SW1 pair. Then, the clock feedthrough of



(a)



(b)

Fig 4.4 By modifying the clocking sequence, SW1 will cause the signal independent charge injection onto the top plate of C_1 and C_2.

(a) First, the grounding switches are turned off which only introduces common mode error

(b) Second, the charge injection later introduced by the input switches will not affect the charge within the dotted lines.

SW2 pair will indeed behave as a common mode signal.

All of the above solutions are based on the assumption that transistors in switch pairs are identical. The effectiveness of the above procedures is limited by the matching capability of the technology.

4.2. Residual Offset Voltage

In the previous chapter, the cause of amplifier offset and an offset sampling technique are described. The effectiveness of the offset sampling methods depends heavily on the matching accuracy of the switch pairs. With 20% mismatch between supposedly matched switches, there is about 2 mV residual offset after the offset cancellation scheme. In the following sections, the effect of residual offset of the comparator or the amplifiers are discussed individually and some techniques that lessen the the severity of these problems are also investigated.

4.2.1. Effect of Residual Comparator Offset

With residual offset (σ) on the comparator, the decision position for each bit is shifted by $\frac{\sigma}{2^n}$. Since the signal is amplified by a factor of two each cycle, the significance of the comparator offset is decreased by a factor of two every cycle. The comparator offset only changes the decision level but the signal itself is left unaffected. When the comparator input is close to ground, the offset can cause the comparator to make an incorrect decision in determining the sign bit causing a conversion error. For example, with a positive comparator offset (σ), any positive input which is smaller than σ will be considered as a negative input. After the wrong sign decision, the converter will try to find out whether or not the signal exceeds the negative half full scale. Since the signal was positive, a mistake occurs. So there is no way to resolve any positive input that is less than σ. In Fig 4.5a, the enlarged simulated transfer curve around zero

shows the dead zone as a result of the comparator offset. This can also be a problem at the major carry. Another simulation output, Fig 4.6, demonstrates the effect of comparator offset to the transfer curve near the first major carry.

Now, it is clear that the effect of the comparator offset in the cyclic conversion is not similar to that for some other approaches[McCr75, Smar76] where the offset voltage only creates a DC shift of the transfer curve and can be easily removed by a DC feedback loop[Coop81, Yama81] or passing through a band pass filter. In the cyclic conversion, the offset actually affects the whole transfer curve and is especially important at the first few major carries.

4.2.2. Effect of Residual Operational Amplifier offset

The consequence of residual offset of the amplifiers is different from that of the comparator. Any offset of the operational amplifiers will directly add onto the signal or the reference as they pass through the loop. Any offset added onto the signal is also amplified along with the signal. So the gain of two of the signal that helps reduce the effect of the comparator residual offset does not lessen the effect of the operational amplifier's offset. At the same time, this offset also accumulates on the reference that is circulated along with the signal with unity gain. The enlarged simulated transfer curves around the first major carry of a 13 bit converter with positive or negative amplifier's offset are shown in Fig. 4.7.

4.2.3. Dead Zone Cancellation Technique

In many applications, especially in the telecommunication area, the performance of the converter near zero input is critical to the system performance. A large dead zone around zero generated by the comparator offset is intolerable in many systems. In this section, a technique that can eliminate the dead zone is introduced.

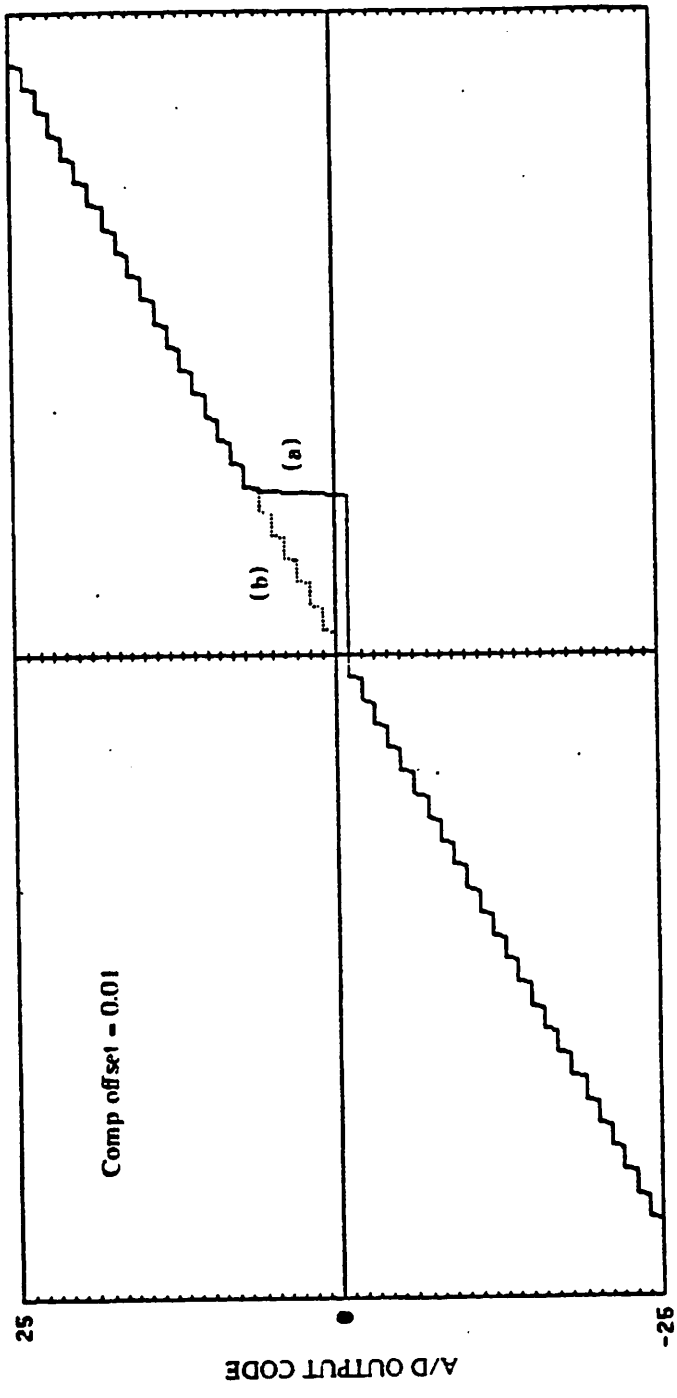


Fig 4.5 The transfer curve around zero of a 13 bit A/D
(a) With comparator offset
(b) With the same comparator offset and the dead zone cancellation technique

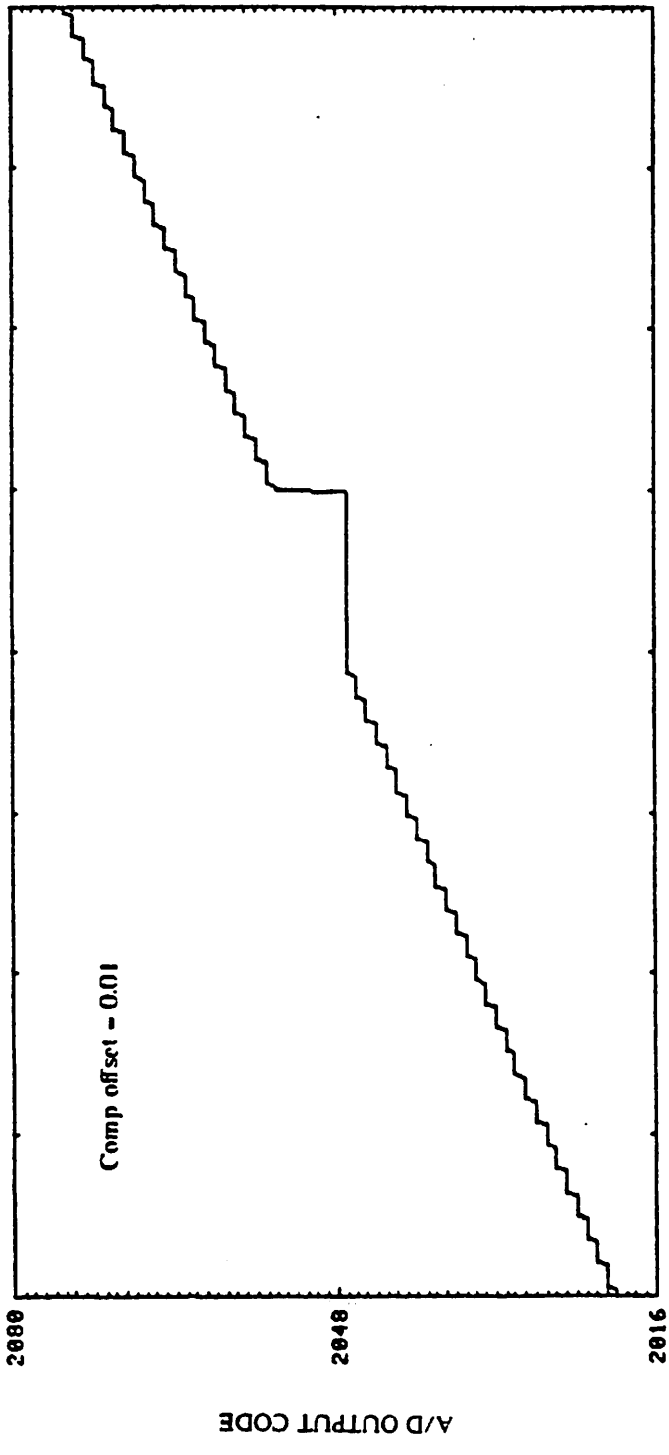


Fig 4.6 The transfer curve around the first major carry of a 13 bit A/D with comparator offset

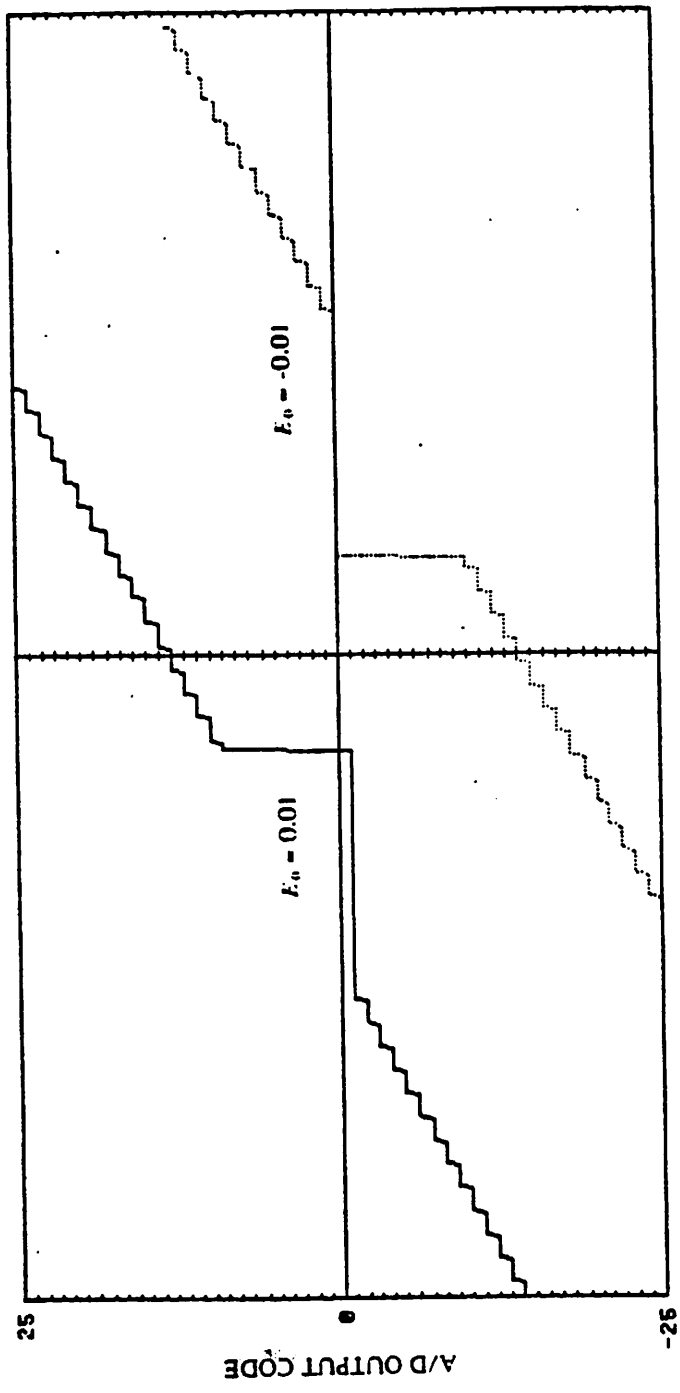


Fig 4.7 The transfer curve around zero of a 13 bit A/D
(a) With positive amplifier offset
(b) With negative amplifier offset

By using the restoring algorithm, a small input will be magnified by two on each cycle without subtraction until it reaches half full scale. An incorrect sign bit decision caused by the residual offset of the comparator can be detected by implementing an additional comparison each cycle which rechecks the input signal polarity even after sign bit decision has been made. Because the signal will keep growing by a factor of two each cycle, a wrong sign bit decision will eventually be detected by the extra comparisons (Fig 4.8). Whenever the converter discovers that an incorrect sign detection has been made during the sign bit decision cycle, it just corrects the sign bit and uses the opposite polarity reference in the following cycles. Because interchange path switches are implemented at the output of each operational amplifier, the polarity of the reference can be easily changed. This occasional correction of reference polarity does not add any cycles to the conversion. If the extra comparison is done when the signal is sampled and held on amplifier #2 , only one extra comparison time is required. The simulation output without and with dead zero cancellation is shown in Fig 4.5a & 4.5b respectively. This technique reduces the dead zone around zero by a factor of 2^{N-1} for a N bit converter.

4.2.4. Op-Amp Offset Reduction Technique

Op-amp offsets in the loop are represented as the E_0 term in equation 3.3. The offset value is assumed to be a constant within one conversion period. In order to avoid the accumulation of the offset error on successive cycles, two different methods are used to reduce the effect of the offset on the signal and the reference individually. With proper procedures, both of these methods can be implemented at the same time without affects each other.

Offset Holding Technique

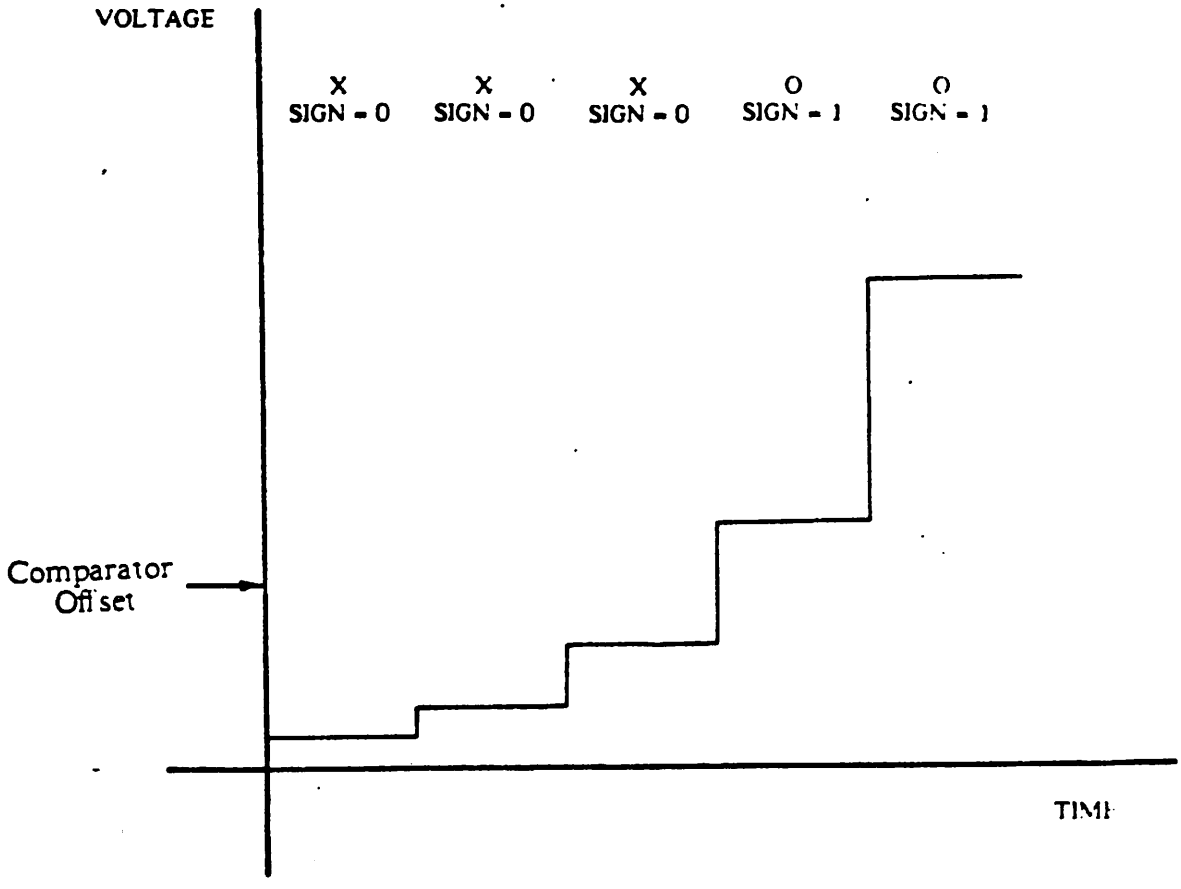


Fig 4.8 An example of the dead zone cancellation technique.

A way to keep the offset error from growing is to interchange the signal path after the first cycle. Now, the first offset error has a polarity opposite to the rest of the offset error that is going to add onto the signal in the following cycles. Because the present offset and the signal are amplified by two each cycle before the next offset adds onto the signal, the offset value stays constant as the real signal portion is magnified. Examing the first three cycles of the conversion should explain the technique more clearly: Notice the V_{off} term in the following three cycles stays constant as V_{in} becomes $2V_{in}$ and $4V_{in}$.

$$V_1 = V_{in} - V_{off} - B_1 V_{hfs}$$

$$\begin{aligned} V_2 &= 2V_1 + V_{off} - B_2 V_{hfs} \\ &= 2(V_{in} - V_{off} - B_1 V_{hfs}) + V_{off} - B_2 V_{hfs} \\ &= 2V_{in} - V_{off} - 2B_1 V_{hfs} - B_2 V_{hfs} \end{aligned}$$

$$\begin{aligned} V_3 &= 2V_2 + V_{off} - B_3 V_{hfs} \\ &= 4V_{in} - V_{off} - 4B_1 V_{hfs} - 2B_2 V_{hfs} - B_3 V_{hfs} \end{aligned}$$

With the offset holding technique, the offset on the signal can be kept constant throughout the conversion of one sample. Thus, the offset becomes relatively smaller and smaller as the encoding process goes on. Although the offset holding technique does not eliminate the problem, it does reduce the offset distortion on small signals. This characteristic is useful for some of the telecommunication systems where tight requirements are imposed on small input signals. Detailed transfer curves (Fig 4.9) at different major carry location illustrate the effect of the offset holding technique.

Reference Offset Cancellation

Because the recirculating reference does not go through the gain of two loop, the previously described method is no good for offset imposed on the reference signal. To prevent the accumulation of the offset on the reference, the reference is toggled between

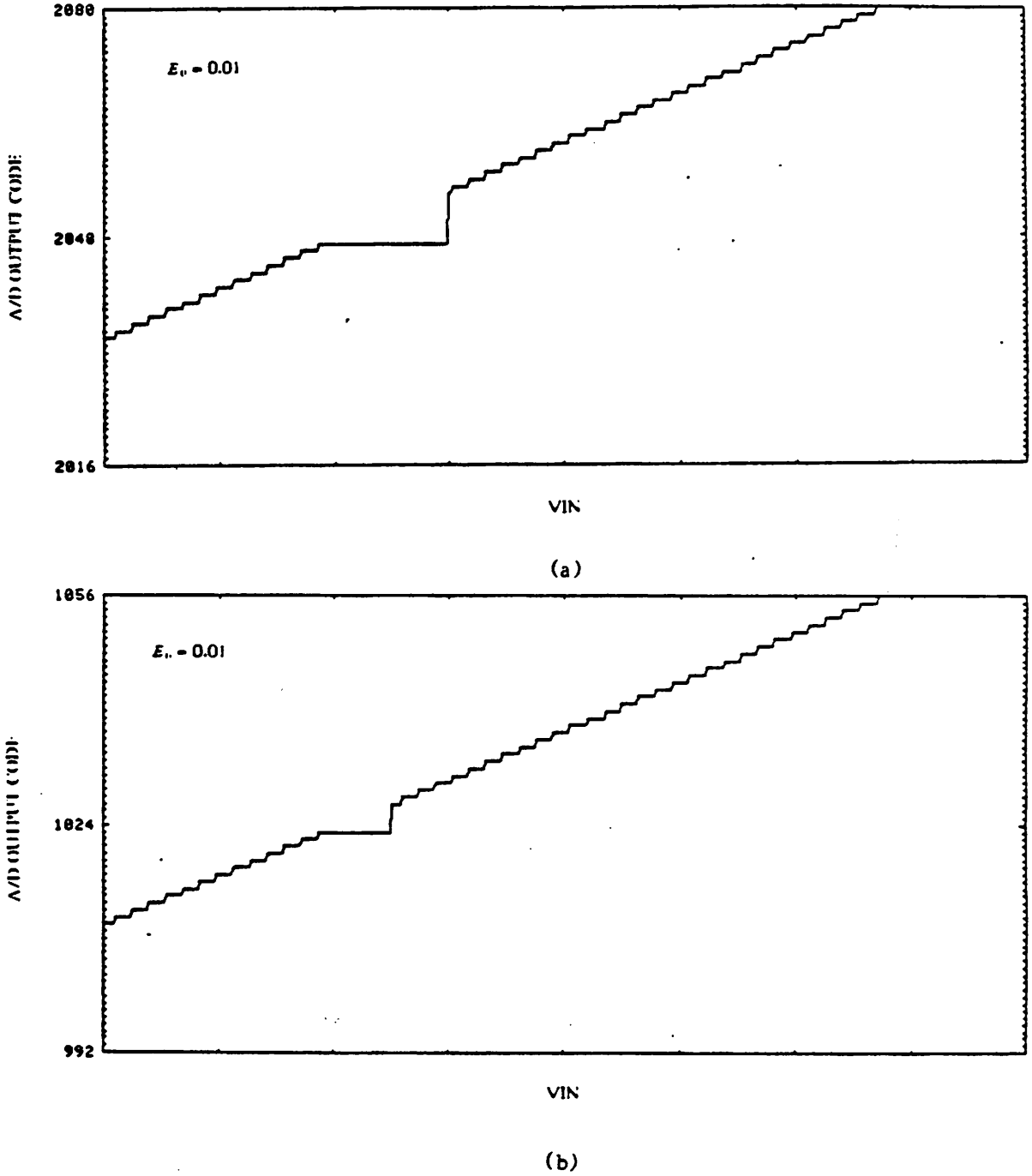


Fig 4.9 The loop offset effect on different major carry locations.
(a) The first major carry
(b) On the second major carry, the effect is reduced by two

each cycle. Then the reference only changes between V_{ref} and $V_{ref} + V_{off}$.

4.3. Noise Consideration

Before this section, all the error sources considered are deterministic; nondeterministic noise is another important error source. Noise varies from sample to sample with little or no correlation between samples. It can only be analyzed by statistical methods and is described by the mean and variance of a particular distribution. There is almost no way to eliminate noise through a systematically method once it is generated. So the focus here is to minimize the amount generated. Noise in the converter creates uncertainty in the decision process and puts another limitation on the minimum resolution of the converter.

4.3.1. Noise Sources in Switched-Capacitor Circuit

The two major noise sources in the switched-capacitor converter are thermal noise from the channel resistance of the switches and the amplifiers' noise. In the next few subsections, the noise analysis is performed by examining the basic function blocks of the converter and the sample and hold circuit shown in Fig 4.10. A single ended circuit is used for simplicity, and the results can be easily converted so that they apply to fully differential case. In the switched capacitor conversion process, two major procedures that are continuously performed are the sampling and transferring process of the signal. Fig 4.11a,b illustrates the noise source in each of these two steps.

Switch Thermal Noise ($\frac{KT}{C}$ Noise)

At the sampling step, the finite on resistance of the sampling switch generates a thermal noise source which is sampled by the sampling capacitor through a $R_{ON}{}_{13}C_1$ filter inherent in the switch and capacitor combination[Hsie81]. Also, the channel resis-

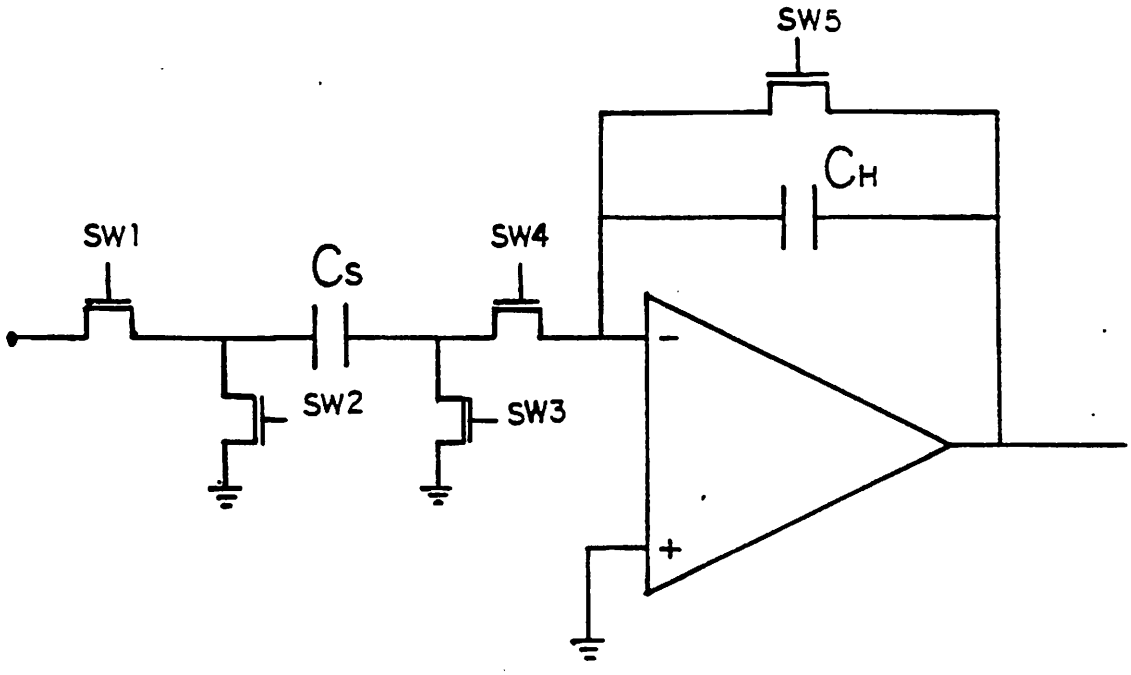


Fig 4.10 A sample and hold circuit diagram

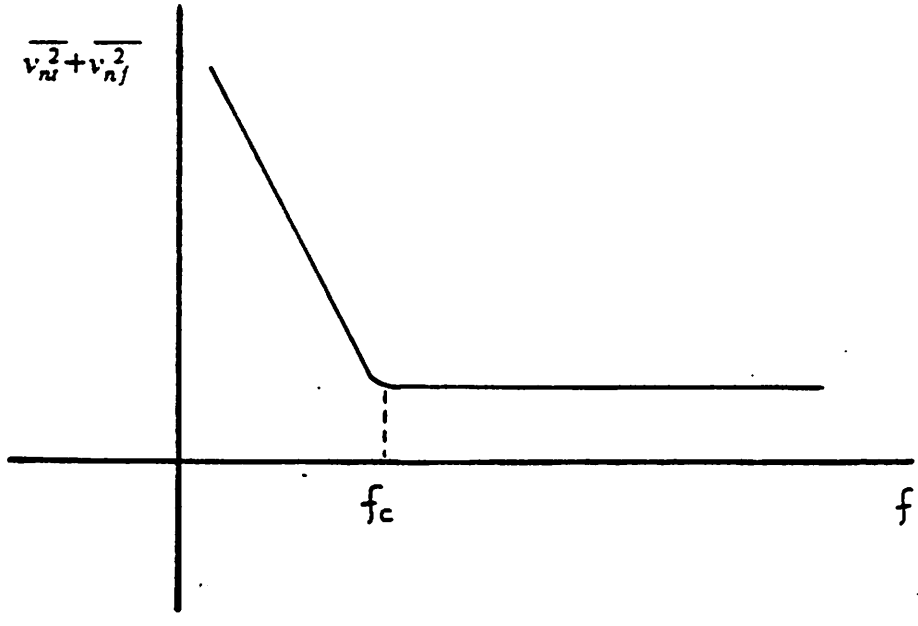


Fig 4.12 A typical noise power spectrum of a MOS transistor

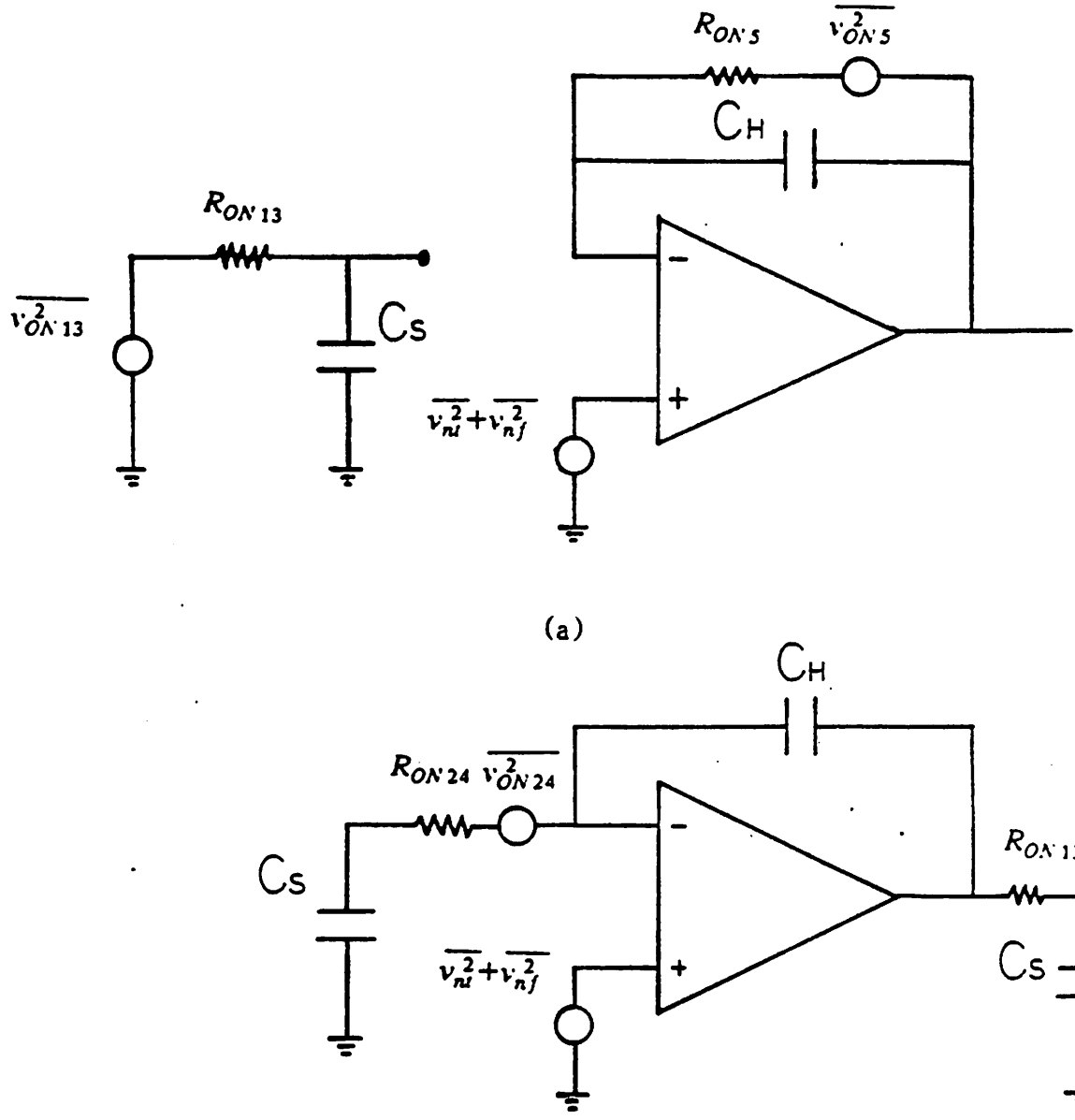


Fig 4.11 The circuit configurations at different condition
(a) The sampling cycle
(b) The transferring cycle

tance R_{ON5} of SW5, used for clearing the holding capacitor C_h, is another noise source to the system. The total on resistance from SW1 and SW3 has a thermal noise power density, $\overline{v_{R13}^2}$, which is equal to $2kT(R_{ON1} + R_{ON3})$. Due to the band-limited characteristic of the sample circuit, the expect noise variance on the sampling capacitor C_s is

$$E(v_{Cs}^2(t,\omega)) = \int_{\infty}^{-\infty} 2kTR_{ON13} \left| \frac{1}{1+j\omega R_{ON13}C_s} \right|^2 d\omega$$

$$= \frac{kT}{C_s} \quad . (4.9)$$

By assuming infinite input impedance of the operational amplifier, The noise variance on C_s from the thermal noise source R_{ON5} is similar to the previous result.

$$v_{Cs}(s) = v_{ON5}(s) - v_{Cs}(s)sR_{ON5}C_h \quad (4.10)$$

The noise on C_h from v_{on5} has variance of $\frac{kT}{C_h}$ at the end of discharge.

In the charge transfer step, the sample and hold circuit changes to another configuration (Fig 4.11b). If the amplifier has large enough gain and the time constant $(R_{ON24}C_h)$ is smaller than the transfer period, the noise sample stored in C_s is transferred completely and held on C_h with the variance of $(\frac{C_h}{C_s})^2\frac{kT}{C_s}$. On the other hand, the thermal noise generated by the channel resistance of SW2 and SW4, $\overline{v_{ON24}^2}$, is sampled on C_h through a network of amplifier, the sampling and holding capacitors, and the switches. The voltage transfer function from the noise source $\overline{v_{ON24}^2}$ to v_{C_h} is

$$H(s) = \frac{v_{C_h}(s)}{v_{R24}(s)}$$

$$= \frac{-c[s+(1+A_o)P_o]}{c(s+P_o)+(1+sR_{ON24}C_h)[s+(1+A_o)P_o]} \quad (4.11)$$

where $c = \frac{C_s}{C_h}$ is the capacitor ratio which is normally equal to unity in the S/H circuit and $R_{ON24} = R_{ON2}+R_{ON4}$. The operational amplifier in this analysis is assumed to be a single pole amplifier with A_o as the DC voltage gain and the P_o as the pole frequency.

The expected noise variance of $\overline{v_{Ch}^2}$ on the holding capacitor C_h from the noise source $\overline{v_{R24}^2}$ is

$$E(v_{Ch}^2(t,\omega)) = \int_{\infty}^{-\infty} 2kTR_{on\,24}|H(j\omega)|^2 d\omega$$

$$= c^2\frac{kT}{C_s}\left|\frac{1+\frac{(1+A_o)^2P_oR_{ON\,24}C_s}{(1+c+A_o)}}{1+c+(1+A_o)P_oR_{ON\,24}C_s}\right| \qquad (4.12)$$

Since c = 1 in the sample and hold circuit and $A_o \gg 1$, then Eq (4.12) can be simplified to,

$$E(v_{Ch}^2(t,\omega)) = c^2\frac{kT}{C_s}\left|\frac{1+P_oR_{ON\,24}C_s}{2+(1+A_o)P_oR_{ON\,24}C_s}\right| \qquad (4.13)$$

The sampled noise shown in Eq. 4.13 is less than $c^2\frac{kT}{C_s}$ which is the thermal noise resulting from SW1 and SW2 in the sampling cycle and transferred to C_h. Depending on the operational amplifier's unity gain frequency and the time constant $R_{ON\,24}C_s$, the noise of Eq. (4.13) can range in between 1/2 to 1 of $c^2\frac{kT}{C_s}$.

In summary, the channel resistance of the switches in the converter introduces a band limited noise to the signal with variance proportional to $\frac{kT}{C}$. Assuming that the noise from the two sources are independent with each other, the noise variance of each source can be summed together to evaluate the total effect.

Operational Amplifier Noise

In the MOS operational amplifier, there exist two major noise sources, the thermal noise ($\overline{v_{nf}^2}$) and the flicker noise ($\overline{v_{nt}^2}$). The channel resistance of the MOS transistor is the source of the thermal noise in the circuit. Flicker noise (1/f noise) is particularly important in MOS transistor. In these devices, surface states tends to cause an input referred noise component which is higher than the thermal noise component for fre-

quencies below 1 to 10 kHz. A typical noise power spectrum for a MOS transistor is shown in Fig 4.12. The corner frequency (f_n) of the flicker noise is very much dependent on the fabrication process. In most cases, the magnitude of the input referred flicker noise is approximately independent of the bias current and voltage, and is inversely proportional to the active gate area of the transistor. For a MOS transistor, the input referred noise voltage, including both the thermal and flicker noise, can be written as:

$$\frac{v_i^2}{\delta f} = 4kT\frac{2}{3}\frac{1}{g_m} + \frac{K_f}{ZLC_{ox}f} \tag{4.14}$$

where

K_f is the flicker noise coefficient determined from experimental result.

Using the amplifier shown in Fig 4.13 as an example, the input referred noise of a amplifier is:

$$\overline{v_{eqT}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + (\frac{g_{m3}}{g_{m1}})^2(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}) + (\frac{g_{m9}}{g_{m1}})^2(\overline{v_{eq5}^2} + \overline{v_{eq6}^2}) \tag{4.15}$$

where it has assumed that $g_{m1}=g_{m2}$, $g_{m3}=g_{m4}$ and $g_{m9}=g_{m10}$. By carefully designing the op-amp according of the above information, the input referred noise of a amplifier will be dominated by the noise from the input devices.

Most of the flicker noise energy is concentrated below the the corner frequency f_n. So the offset sampling technique can actually eliminate the flicker noise if sampling is performed at more than twice the flick noise corner frequency; therefore, with sampling , the input referred amplifier noise is almost entirely thermal noise and can be modeled as an equivalent noise resistance. The equivalent input noise resistance of the operational amplifier is,

$$R_{eq} = \frac{4}{3}\frac{1}{g_m} \tag{4.16}$$

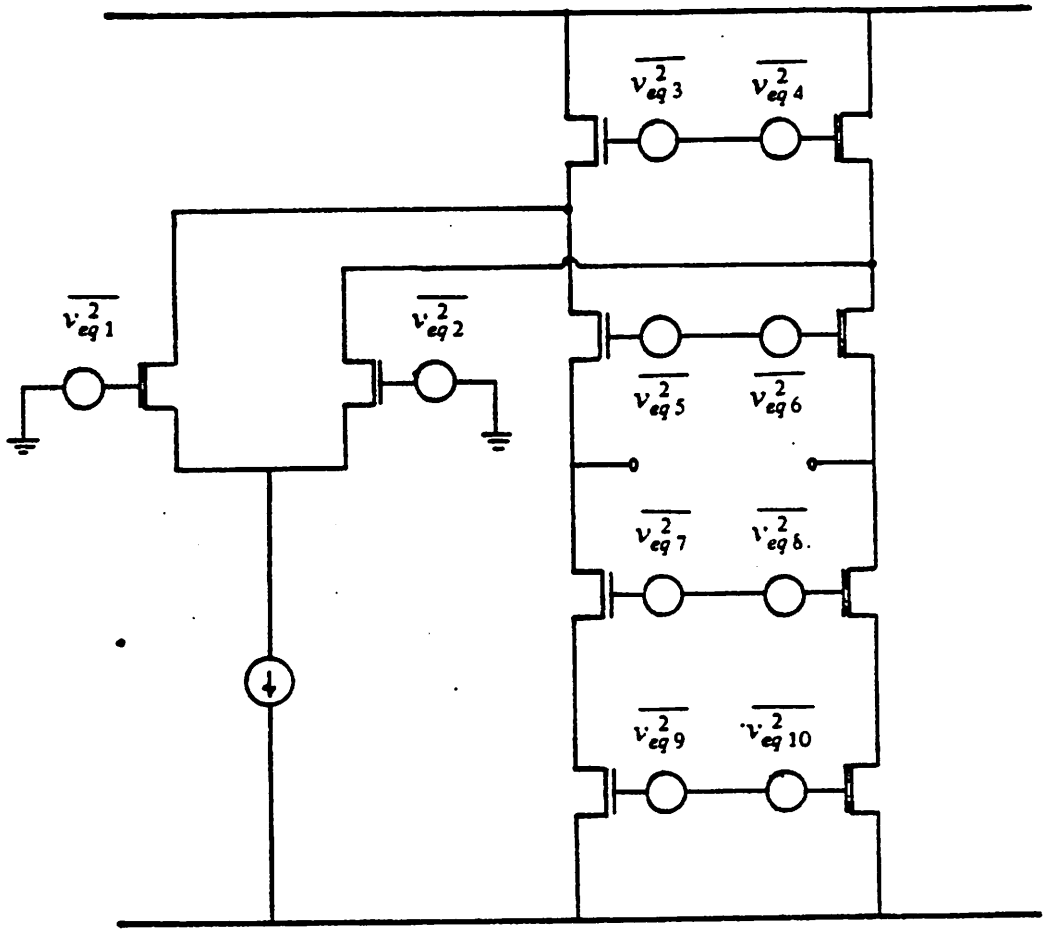


Fig 4.13 The possible noises source in a single stage fold cascode amplifier

Now, refer back to Fig 4.11a,b. when during the sampling cycle, the op-amp noise does not introduce any noise to C_s or C_h if the input impedance of the amplifier is infinite. During the transfer cycle, the op-amp can be modeled as a voltage dependent voltage source in series with the op-amp output resistance ($R_{out} = \frac{1}{gm}$), and the expected noise variance sampled by C_{s2} from $\overline{v_{nt}^2}$ is

$$E(v_{Cs2}^2(t,\omega)) = \frac{kT}{C_{s2}} \frac{(R_{ON13}+R_{eq})}{(R_{ON13}+R_{out})} \tag{4.17}$$

where R_{eq} is the equivalent input noise resistance of the operational amplifier. From eq. 4.17, it can be seen that the thermal noise from the op-amp only adds a little noise to the sampling capacitor in addition to the $\frac{kT}{C}$ noise that is generated by the sampling process.

4.3.2. Effect of Noise on A/D and D/A Converter

In a data conversion system, any noise added directly influences the accuracy of the converter. An incorrect decision caused by the noise will not be corrected or affected by the overall bandwidth of the whole system. In the previous sections, the major noise sources and the effects of noise for different configurations have been discussed throughly. Now, the performance of the converter with all of these noise sources is examined.

Both the signal and the reference voltage are affected by the noise while they go through the sampling and transferring process around the loop in a reference refreshing cyclic converter. Any noise that is imposed on the recirculating reference is also going to corrupt the signal itself during the addition or subtraction operation. The variance of the noise is increased by a factor of two because of the fully differential architecture. By counting the number of sampling and transferring operations performed on the signal and the reference during each cycle and adding the noise associated with each

together independently, the expected noise standard deviation of the signal after the first cycle is calculated to be about $4\sqrt{2}\sqrt{\frac{\overline{kT}}{C_h}}$. Since the residual signal magnitude increases by a factor of two after every cycle in the A/D conversion, the corresponding input referred noise power term at the n-th cycle is reduced by a factor of $4^{(n-1)}$. By adding up all the noise from the rest of the cycles, the expected standard deviation of the total input referred noise is only about $6.6\sqrt{\frac{\overline{kT}}{C_h}}$ (0.3 mV) , where the 13 bit LSB level in this design is 1.2 mV.

For the D/A conversion, the input code and the noise that accumulates on the refreshed reference determine the amount of noise that appears on the final analog output. Because the signal is divided by two each time, any distortion that is generated at the beginning of conversion is not as important as the noise that comes in at the last few steps. So codes that require addition of the reference during the last few cycles will have the maximum noise level. Supposed that the variance of the noise that is added onto the reference and the signal every cycle is $\overline{v_n^2}$. Then the maximum expected noise variance of the output signal is,

$$\overline{v_{tot}^2} = \left\{ (N+1) + \frac{((N-1)+1)}{4^1} + \frac{((N-2)+1)}{4^2} + \frac{((N-3)+1)}{4^3} + \ldots + \frac{2}{4^{N-1}} \right\} \overline{v_n^2} \qquad (4.18)$$

The final expected noise standard deviation for a 13 bit D/A converter is about $17\sqrt{\frac{\overline{kT}}{C_h}}$. So the D/A has about 3 times worse noise performance than the A/D converter.

4.4. Stray Capacitor Effect

In Fig 4.14, a single ended sample hold circuit is drawn with all of the possible stray capacitors illustrated using dotted lines. By following the clocking sequence used in this conversion, the input signal is sampled on the bottom plate and then transferred

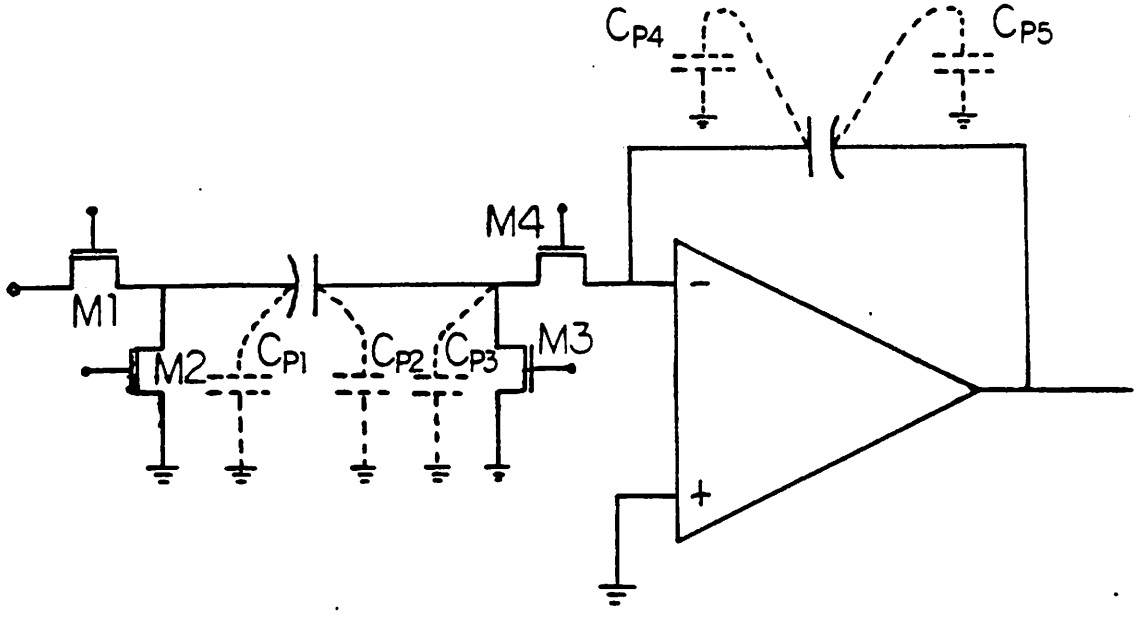


Fig 4.14 The stray capacitors in a bottom plate sample and hold circuit.

to the integrating capacitor. Stray capacitance around the input node (C_{p1}) does not generate any error in the process because the input node is voltage driven. The bottom plate stray capacitors (C_{p2} and C_{p3}) are charged to zero by SW3 and held at zero by the op-amp. The voltage across C_{p4} is also kept at zero volts by the op-amp. So C_{p2}, C_{p3} and C_{p4} experience no change in voltage or charge and thus cause no error. C_{p5} is a load to the op-amp and does not affect its final value: therefore C_{p5} causes no error if the op-amp is allowed sufficient time to settle properly.

4.5. Capacitor Voltage Coefficient

The capacitance of a MOS capacitor varies with the voltage that it drops . This voltage dependent capacitance [McCr81] can be expressed as,

$$C(v) = C_o(1+\alpha_1 v+....) \tag{4.19}$$

The total charge that is sampled on the capacitor is

$$Q_{tot} = \int_0^{V_{in}} C(v)v dv$$

$$= C_o(V_{in} + \frac{1}{2}\alpha_1 V_{in}^2+....) \tag{4.20}$$

Because of the usage of the fully differential architecture, all of the odd order terms in eq 4.21 are canceled. The even order terms have the similar effect as the odd error terms in the loop. So by using the reference refreshing approach, these kind of errors are also been suppressed.

4.6. Capacitor Hysteristic Effect

Due to the possible contamination of the capacitor dielectric during the process and an extra thin nitride layer existed in most of the double polysilicons capacitor, there may be space charges presented in between the capacitor plates. This mobile impurity ions or the effect of polarizable molecules in the dielectric can cause a residual

charge after the voltage is removed from the capacitor.[Gray, Hodg, Grov67] One simple way to model a capacitor with this effect is by considering that as a ideal capacitor in parallel with a serial resistor and capacitor which has a large time constant.[Gray] After putting a voltage across the capacitor long enough, even the capacitor is shorted later, there will be some residual charges left on the capacitor because of the large time constant.

The time period that a voltage stays across a capacitor in a cyclic conversion is much smaller than the time constant of the capacitor hysteristic. So, the hysteristic effect is not going to affect the converter's performance.

CHAPTER 5

HIGH SPEED CMOS AMPLIFIER AND COMPARATOR

Some special requirements for the amplifier used in the cyclic data acquisition system are discussed in the first section. In the second section, a high speed fully differential operational amplifier is presented. At the end of the chapter, a CMOS comparator is discussed.

5.1. Special Considerations of an Amplifier used in Cyclic Converters

The basic requirement for an amplifier used in an A/D or D/A is that its output be accurate within one LSB after some specified time for any possible input. In another words, the settling time is measure by the time required for the output to reach its absolute ideal value ± 1/2 LSB instead of the relative percentage of the input signal. For small signals, the settling time of the op-amp is mainly dependent on the bandwidth of the operational amplifier. On the other hand, for large signal levels, the slew rate of the amplifier becomes a major contributor to the settling time. An operational amplifier in an A/D or D/A must be capable of driving large output swing in one clock period. In contrast, an op-amp in a switched capacitor filter usually only has to cope with small changes in the output during any particular clock cycle because the sampling frequency is usually much greater than the signal bandwidth. So both high slew rate and wide bandwidth are important factors in choosing the right architecture for the amplifier in an A/D or D/A.

Since the reference refreshing algorithm can cancel first order gain errors, the voltage gain of the amplifier is not critical from this point of view. However, the linearity of the op-amp's close loop input to output transfer curve is important. Any architec-

ture of an amplifier which has better linearity is preferred in this project. Since the amplifier is used in the feedback configuration, the linearity improvement is proportional to the open loop gain. Therefore, in this respect, an operational amplifier with an open loop gain of one thousand is desirable.

Since the capacitor matching does not affect the performance of the converter, the sampling and integrating capacitors are chosen to be as small as possible. This reduces the charging capability requirement for the op-amp but increases both clock feedthrough and switches thermal noise errors. These two error sources instead set up the limit on how small the capacitors can be besides the matching requirement. Any minor clock feedthrough error is amplified if the capacitor used in the circuit is small. Also, the thermal noise from all of the switches is linearly proportional to the capacitor size. Therefore, a speed vs. accuracy tradeoff exists in determining the optimum capacitor value. For this project, the capacitor value of 2 pF was selected for both the sampling and holding capacitors.

Because both the slew rate and bandwidth requirement, a single stage cascode class A op-amp is chosen to have reasonable slew rate and fast settling time. On the other hand, in order to reduce the effect on the conversion of the charge transfer errors mentioned last chapter and to increase the power supply rejection ratio, a fully differential architecture is selected for the amplifier. Because of the symmetry associated with this configuration, the charge injection, clock feedthrough and power supply variation are all seen by the op-amp as common mode signals and are thus greatly diminished in importance.

5.2. A High Speed Fully Differential Operational Amplifier

The operational amplifier is a fully differential amplifier. Basically it is a single stage class A op-amp with folded cascode output stage. The individual parts of the

operational amplifier is described in the following subsections.

5.2.1. Bias circuit

The bias circuit is shown in Fig 5.1a. The voltage dropped on MBN2's gate is V_t plus δV. By making the W/L ratio of MBN1 1/4 of the W/L ratio of MBN2, the output swing of the op-amp can swing up to Vss - 2 δV independent of the threshold voltage of the transistor[Choi83]. Practically, a ratio of 1/5 or 1/6 is used because some safety margin is put in to ensure that all of the transistors are biased in the saturation region.

5.2.2. Description of Gain Stage

Voltage Gain Aspect

The differential amplifier is a single stage amplifier with a folded cascode output branch. See Fig 5.1b. The output impedance of the double cascode branch is $\frac{(G_m * R_{out}) * R_{out}}{2}$, where R_{out} is inversely proportional to the drain current and increases with the device channel length while G_m is propositional to the square root of the current. The voltage gain of the op-amp is:

$$Voltage\ gain = GM_{in} GM_{p3} Rout_{p3} Rout_{p1} \qquad (5.1)$$

Therefore, the voltage gain of the op-amp is inversely proportional to the quiescent current. However, the maximum charging current that the output branch can supply also depends on the quiescent input and output branch current. Using minimum bias current and long channel output devices will increase the voltage gain of the amplifier. On the other hand, using higher bias current can give better slew rate.

Frequency Response Aspect

The high impedance node of this op-amp is at the output node; therefore, the load capacitance is used as the compensation. Normally, no special compensation capacitance is needed to retain the op-amp stability. The unity bandwidth of the op-amp is pro-

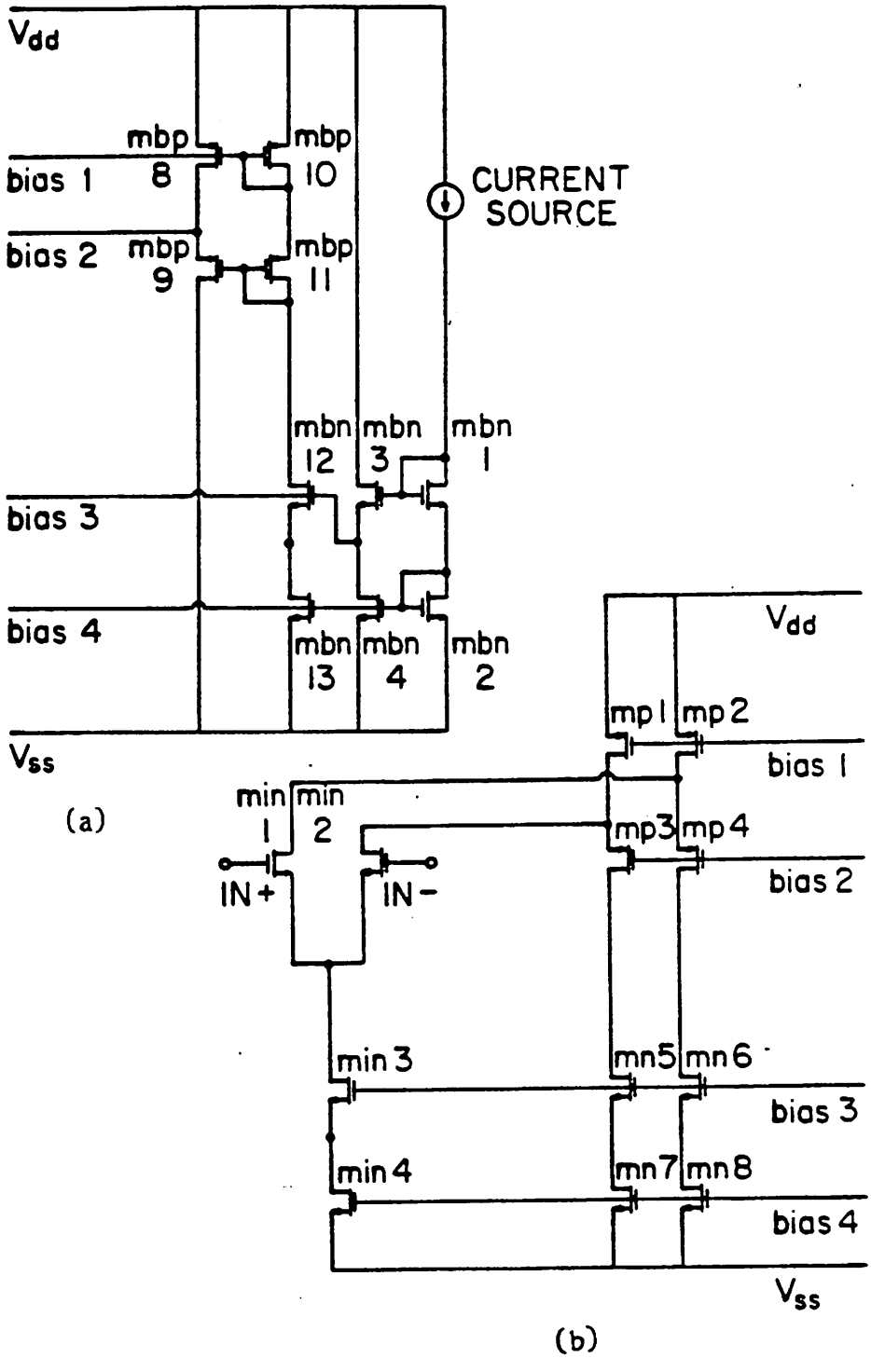


Fig 5.1 The circuit diagram of the differential amplifier
(a) The bias circuit
(b) The gain stage

portional to the transconductance of the input device divided by the load capacitance at the output ($\frac{G_m}{C_L}$). The nondominant pole in the circuit is caused by the time constant associated with the cascode node on the PMOS side. In order to push the second pole away from the dominant pole, the capacitance at that node has to be minimized. The major contributions of the capacitance are the gate capacitance of MP3 and MP4 and the overlap capacitance of the input devices. The nondominant pole have magnitude on the order of the f_T of this device[Gray84]. For an MOS transistor, the f_T is approximately equal to $\frac{g_m}{C_{gs}}$, or proportional to. $\frac{(V_{gs}-V_t)}{L^2}$. So decreasing L increases the f_T and pushes out the nondominant pole. Unfortunately, to achieve high gain, long channel devices are preferred. So there is a trade off between high gain and high speed for class A single stage amplifier. Also, by maximizing $(V_{gs}-V_t)$ is another way to achieve better f_T. However, it limits the swing of the op-amp.

5.2.3. Description of Differential Pairs Common Mode Feedback Circuit

In fully differential amplifier, the common mode component of the output voltage must be maintained near the midpoint of the power supply voltages to keep the whole circuit operating properly and to utilize the full dynamic range. A common mode feedback circuit is used to force the common mode output voltage to a predetermined voltage (usually the supply midpoint).

Two differential pairs are used to form the common mode feedback circuit. See Fig 5.2. The gates of both MCP5 and MCP6 are tied to ground in order to make the common mode signal stay close to this reference. When a positive common mode signal appears at the output nodes, it decreases the total current that flows through MCP9 and MCP10 and at the same time it increases the total current in MCN13 and MCN14. By the mirror circuits of MCN13, MCN15 and MCN16, MCN14 , the current that flows through MCN15 and MCN16 also increases. The extra current needed for MCN15 and

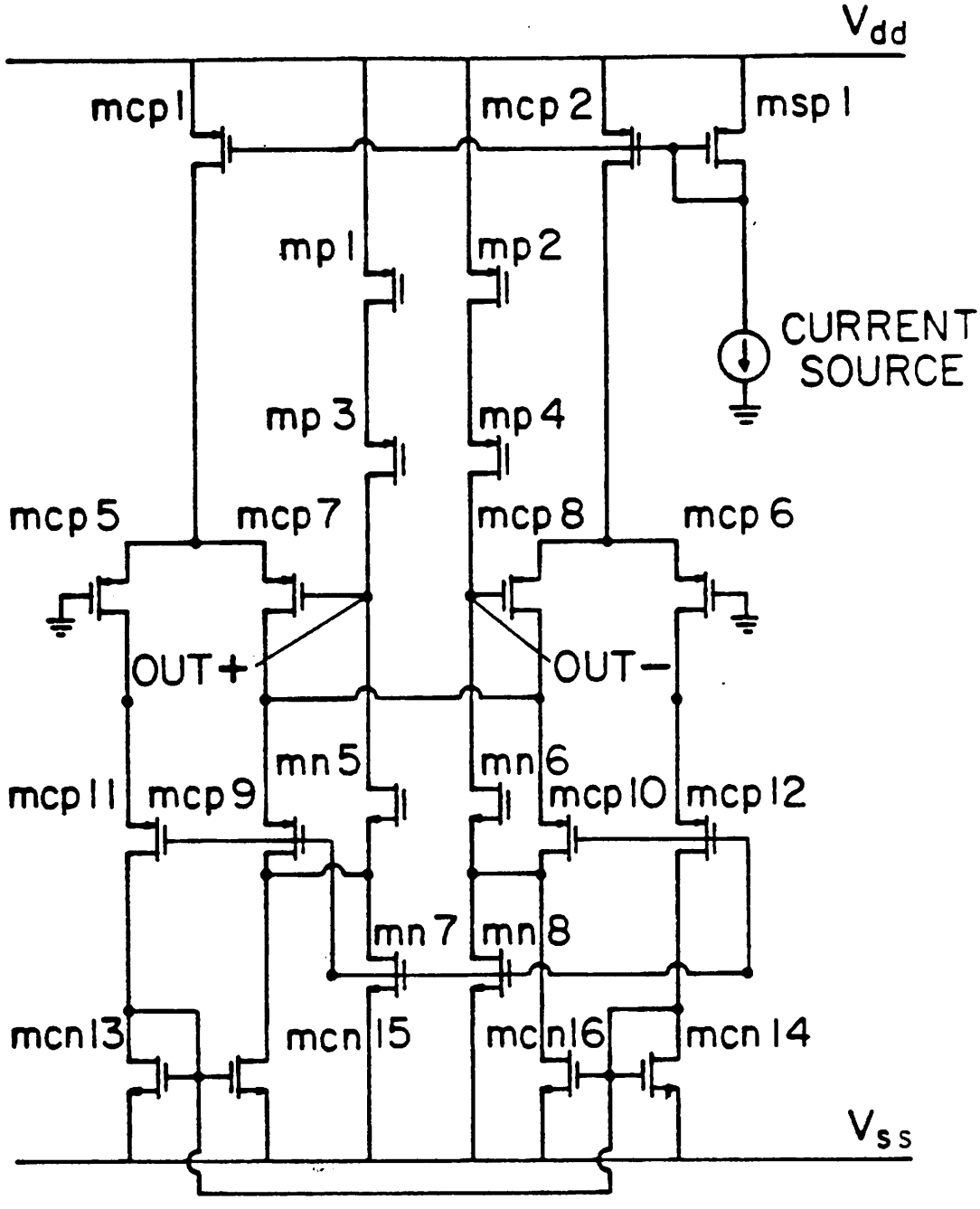


Fig 5.2 The common mode feedback circuit diagram

MCN16 is supplied by MN7 and MN8 which causes the common mode output voltage to drop back down. Since the source of the MCP9 and MCP10 are tied together and they have the same gate bias, the sum of the drain currents of MCP9 and MCP10 stays the same when a differential signal appears at the output. The total current that flows through MCN15 and MCN16 is also independent of a differential output. One important note of using this circuit is that any resistance that appears in between the drains of MCN13 and MCN14 or the drains of MCP7 and MCP8 will act as a negative feedback resistance and drastically reduce the operational amplifier's differential gain.

For fast common mode settling, a large G_m for MCP7 and MCP8 is required because the bandwidth of the common mode feedback circuit is directly proportional to the input device G_{m-cm} value. However, a large transconductance will make the common mode feedback differential pair more likely to leave the linear region of operation when a large negative swing occurs. Because the current that flows through MCP7 or MCP8 is equal to $G_{m-cm}\delta V_{out}$ and with large negative δV_{out} , all the bias current will flow through the MCP7 or MCP8 which forces one of the common mode feedback differential pair get out of the linear operation region. Without proper common mode feedback from these differential pairs, the fully differential amplifier will have unproper biasing and seize to function. Thus, the transconductance of common mode feedback differential pairs causes a trade off between the maximum output swing and the speed. On the other hand, large positive output swing will easily squeeze the input transistors of the common mode feedback differential pairs into triode region. Again, disable the normal operation of the common mode feedback circuit and limit the positive output swing of the differential output. In order to have large swing in the positive direction, the V_{DS} of MCP1 and MCP2 should be as small as possible.

5.2.4. Impact Ionization Effect

With large positive output swing , the electric field from drain to gate for the output devices is much larger than normal. When the electric field in a semiconductor is increased above a certain value, many carriers gain enough energy so that they can start to excite electron-hole pairs by impact ionization[Kama76]. With the hole-electron pairs generated by impact ionization, the majority of the carriers will be collected by the substrate. Because of this effect, the subtract current jumps to a much larger value than normal. It looks effectively like a resistor directly connected between the cascode output node to the signal ground. Even though the cascode output branch is designed to have high output impedance, the actual output resistance is shunted by the effect of impact ionization. Since, this resistance value is about ten times the normal MOS output resistance, the benefit of using the cascode output branch is destroyed by this nonideal effect and the gain of the operational amplifier is reduced after the impact ionization effect occurs. Normally the NMOS transistors impact ionization effect starts earily than for PMOS transistor because of basic mobility difference between holes and electrons.

There are two circuit ways to prevent the impact ionization problem from happening. First, inserting an extra transistor in between the output node and the NMOS output transistor and tying the gate of the extra transistor to ground makes sure none of the NMOS transistors have large enough drain to gate voltage to cause impact ionization. However, this extra transistor introduces nonlinearity in the transfer curve of the operational amplifier because that extra transistor is operated in different region depending on its drain voltage. Second, if a P-Well process is used, then simply tying a separate well to each source solves the problem because the carriers generated by impact ionization go to the source instead of to signal ground. With this method, no distortion of the transfer curve is expected.

5.2.5. Simulation Results

The simulated DC transfer characteristic for the amplifier is shown in Fig 5.3a. The common mode variation with the differential output is shown in Fig. 5.3b. The frequency response of the amplifier with 2 pF capacitor load is shown in Fig 5.4. The transient response of the amplifier with ± 3 volt input is shown in Fig 5.5. The summary of the performance of this fully differential amplifier is shown in Table 5.1.

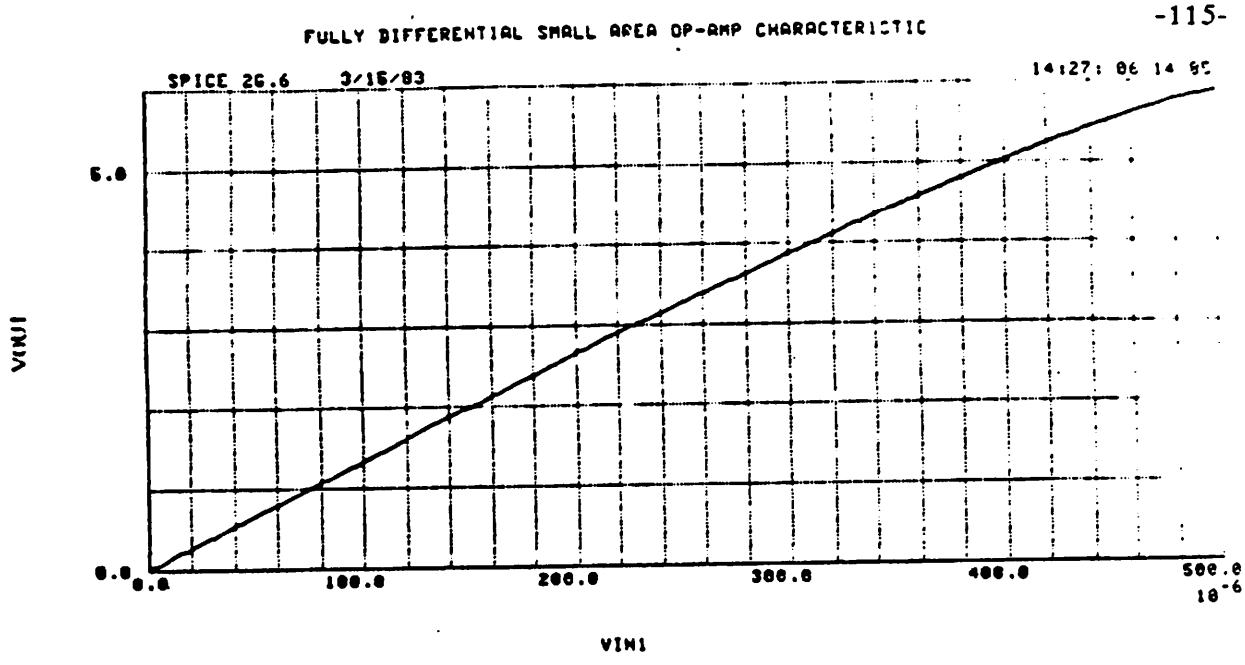
5.3. Comparator Circuit

The basic function of a comparator is to compare an unknown signal with a reference and to determine which is larger. The resolution of the comparator determines the minimum detectable difference between the signal and the reference. A comparator is usually composed of two parts, a differential high gain stage and a latch circuit. The differential high gain stage is used to enlarge the difference between the input voltage and the reference so that the latch can make the correct decision.

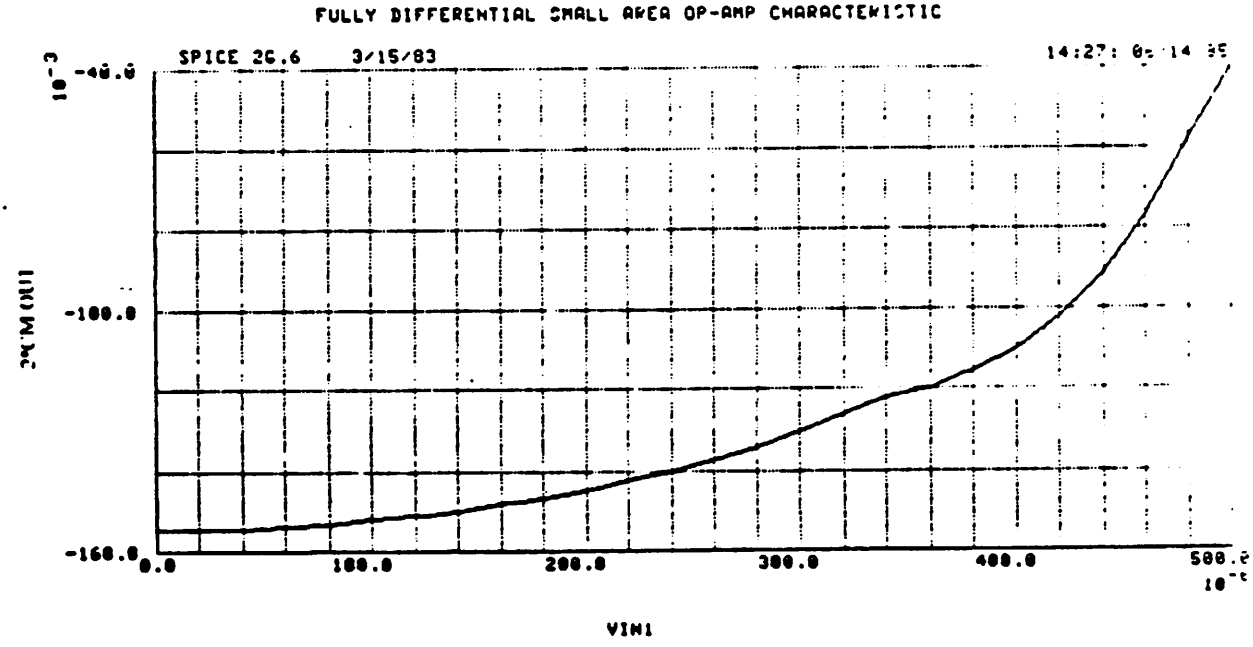
The differential gain stage used in this project is similar to the differential amplifier previously described. There are, however, some minor changes that make it more suitable to be used as a gain stage in a comparator. First, the bias current is only half of that in the original operational amplifier design. Since there is no slew problem in a comparator, the high bias current is not necessary. With lower cascode output stage bias current, the open loop voltage gain is higher. Instead of having high swing capability as a op-amp required, in fact, two CMOS drain gate connected transistors are used to clamp the output swing so that excessive reset time is prevented. Because output branch of a class A operational amplifier has only limited amount of current, the clamping transistors

will not be burned out by the amplifier.

For a class A amplifier with small differential input voltage, the output current is equal to the input transistors transconductance times the input voltage($G_m * v_{in}$). In



(a)



(b)

Fig 5.3 SPICE simulated DC transfer curve of the amplifier
(a) The differential output variation with respect to input variation
(b) The common mode output variation with respect to input variation

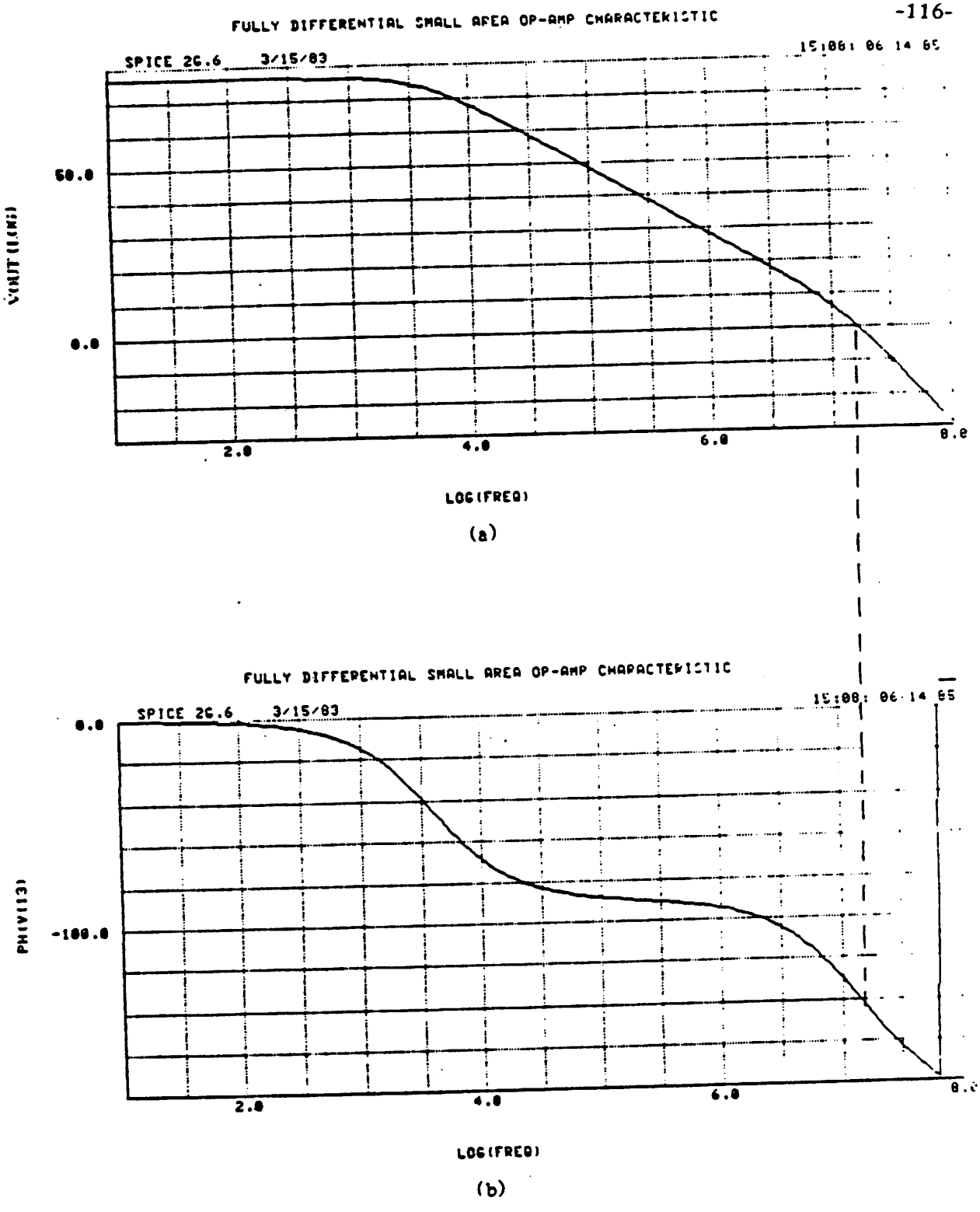
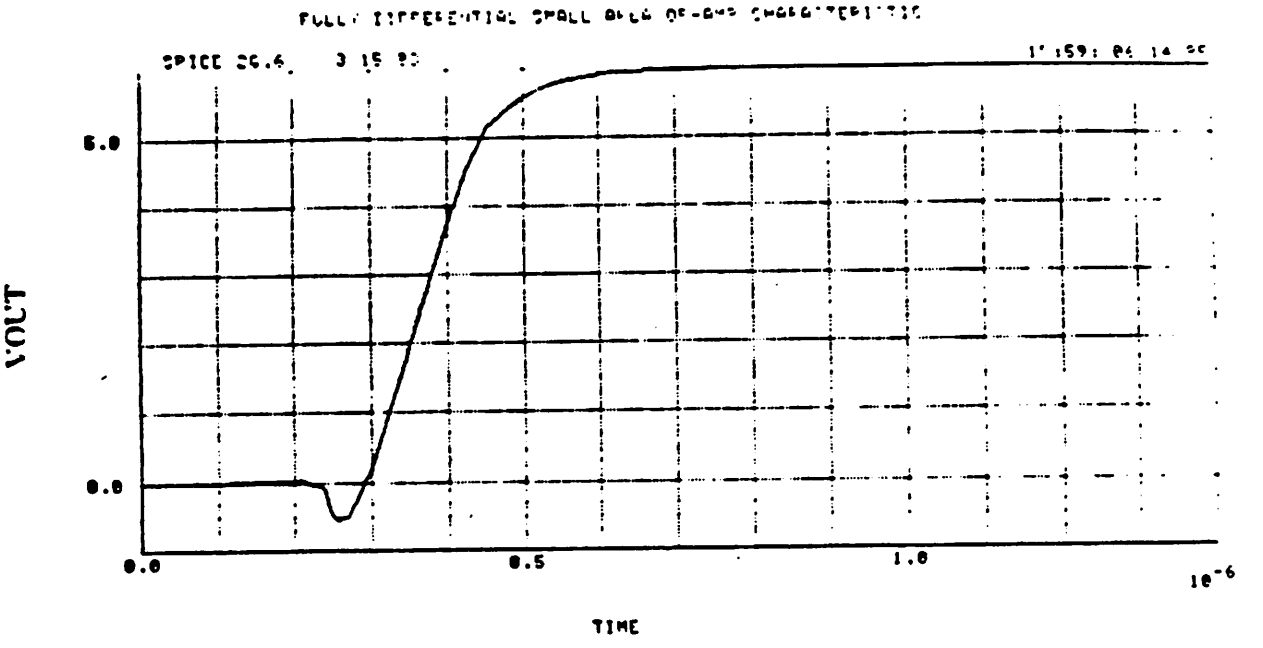


Fig 5.4 The frequency and phase response of the amplifier with 2 pF load



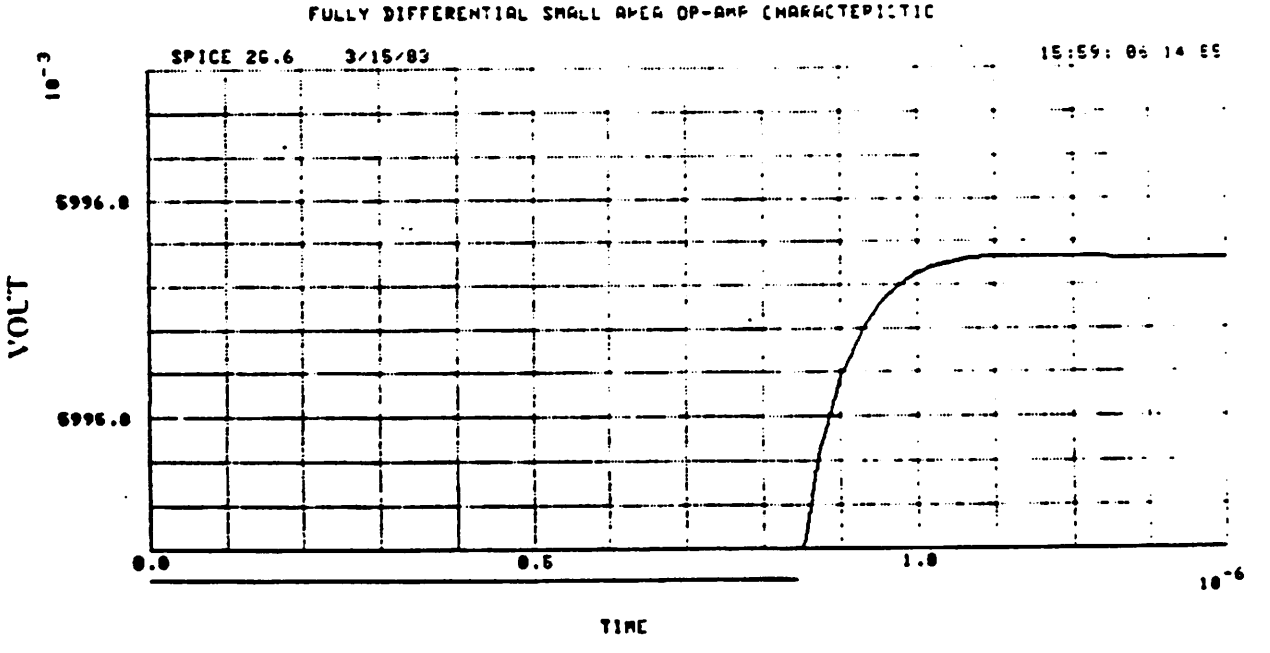


Fig 5.5 The transient response of the amplifier to 6 volt differential output

SIMULATED AMPLIFIER PERFORMANCE		
Supply voltage	±5	V
Open loop voltage gain	78	dB
Power dissipation	5.5	mW
CMRR with ± 3 V output	>90	dB
PSRR with ± 3 V output	>90	dB
RMS input-referred noise	48	μV
Unity-gain bandwidth	19	MHz
Phase margin	42	degree
Load capability	2	pF
Slew rate	50	$V/\mu s$
±3 V output settle to within 0.5mV	700	ns

Table 5.1 The summary of the differential amplifier performance

this case, the comparator has a limited output current to charge the input capacitance of the next stage i.e. the latch. In order to charge the latch input to a reasonable voltage in a short time, the input devices must have a fairly large transconductance. So the input devices of the comparator gain stage have a larger W/L ratio than the same devices in the differential amplifiers.

The latch circuit is shown in Fig 5.6. The output of the gain stage is directly tied to the latch. The input source follower is used to prevent the output voltage of the gain stage from being affected by a sudden change in the latch output. Without the source followers, this could be a serious problem because the operational amplifier has a large output impedance; therefore, noise can easily couple to these nodes.

In the idle period, the strobe signal is high and transistor MLP1 is in cutoff region. Transistor HLP1 turns off the current flow in the latch, so every transistors in the latch circuit are operated at the edge of the triode region and both of the latch outputs stay at logic low.

When the input is ready, the strobe signal is pulled down. The latch is activated when bias current starts to flow. At this instant, the latch senses the input and uses positive feedback loop to amplify the input and store the decision at the latch outputs. After the data has been latched, even though the input of the latch changes and the strobe is still low, the output of the latch will not change because the latch circuit has already reach a unreversible stable state. In order to have the output to drive the output pad, two inverters are used to increase the current capability.

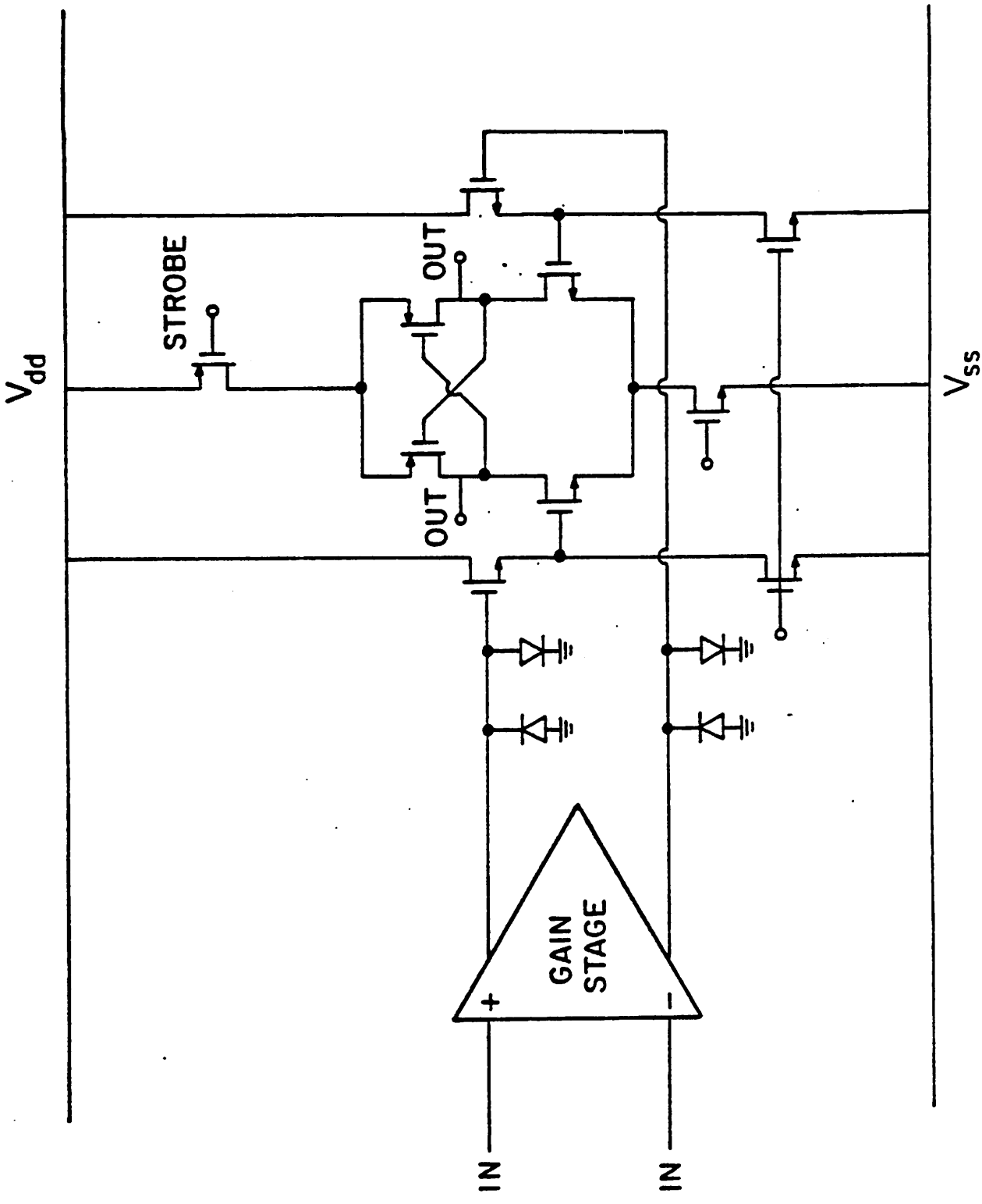


Fig 5.6 The detail latch circuit diagram

CHAPTER 6

LOGIC CONTROL CIRCUIT AND TESTING SETUP

In this research project, only the analog portion of the A/D and the D/A are integrated. The control circuit is implemented externally of the chip with standard TTL and CMOS logic chips. The reason for this approach is to make the testing setup of the converter more flexible. Different algorithms can be tested by changing the external clocking sequence without refabricating the chip itself. Also, to further increase the testability, some additional testing nodes and optional switches are added on chip.

In the first section of this chapter, the structure of the external logic is described, which includes the TTL finite state machine and the implementation of the interface between the TTL logic and the CMOS analog chip . Then in section 2, two different testing methods for the A/D converter, the code density test and the exact transfer curve test, are described individually. The exact transfer curve test method for the D/A converter is explored in section 3.

6.1. The Basic Structure of the Controller for the A/D and D/A

The idea of having an external controller is to offer the opportunity to examine the performance of the chip with several kinds of different clocking algorithms. So the most suitable structure for the controller is the one which can try out different clocking without any rewiring of the control board. Using microcomputer as a controller, the control sequence can be programmed by software. However, the microprocessor is too slow for this application. So, instead, a special finite state machine is designed.

6.1.1. TTL Finite State Machine Controller

The block diagram of the finite state controller for A/D is shown in Fig 6.1. Based on the present state and the previous two bits from the A/D digital output, the controller will select the proper jump address for the program counter. These jump addresses are stored in an Erasable Read Only Memory (EPROM). When the jump signal appears, the program counter then loads in the new address and generates the proper clock signal. The flow sequence of the controller can be easily modified by changing the jump address in the EPROM. The actual control pattern that turns on and off the switches is programmed in a set of high speed programmable read only memorys. This controller structure makes the user perform a hardware programming by changing either the jump addresses or the actual control patterns. In order to remove the glitches at the output of the PROM's, a synchronized buffer is used for each PROM. The control logic is running at 10 MHz. The control clocking delay needed in between the sampling switch and the grounding switch for the charge injection prevention clocking scheme is realized by separating them with one controller clock period (100ns) instead of a asynchronize logic delay. The controller for the D/A is similar to that of the A/D and is shown in Fig 6.2.

6.1.2. Interface Circuit with Analog Chip

The entire TTL circuit is operated with a single 5 volt supply; however, the analog circuit control signals need ± 5 volt swing. Furthermore, the output waveform generated by the latch from the test chip varies between ± 5 volt and must be brought back to the TTL level to feed the signal back to the control circuit to determine the proper clocking for the next cycle. Especially, the CMOS to TTL level conversion, the conversions have to be done in approximately 20 ns. For the TTL to CMOS level conversion, an open collector pull-up inverter is chosen (See Fig 6.3). Internally, The TTL circuit operates between 0 and -5 volts. The open collector output is pulled up to 5

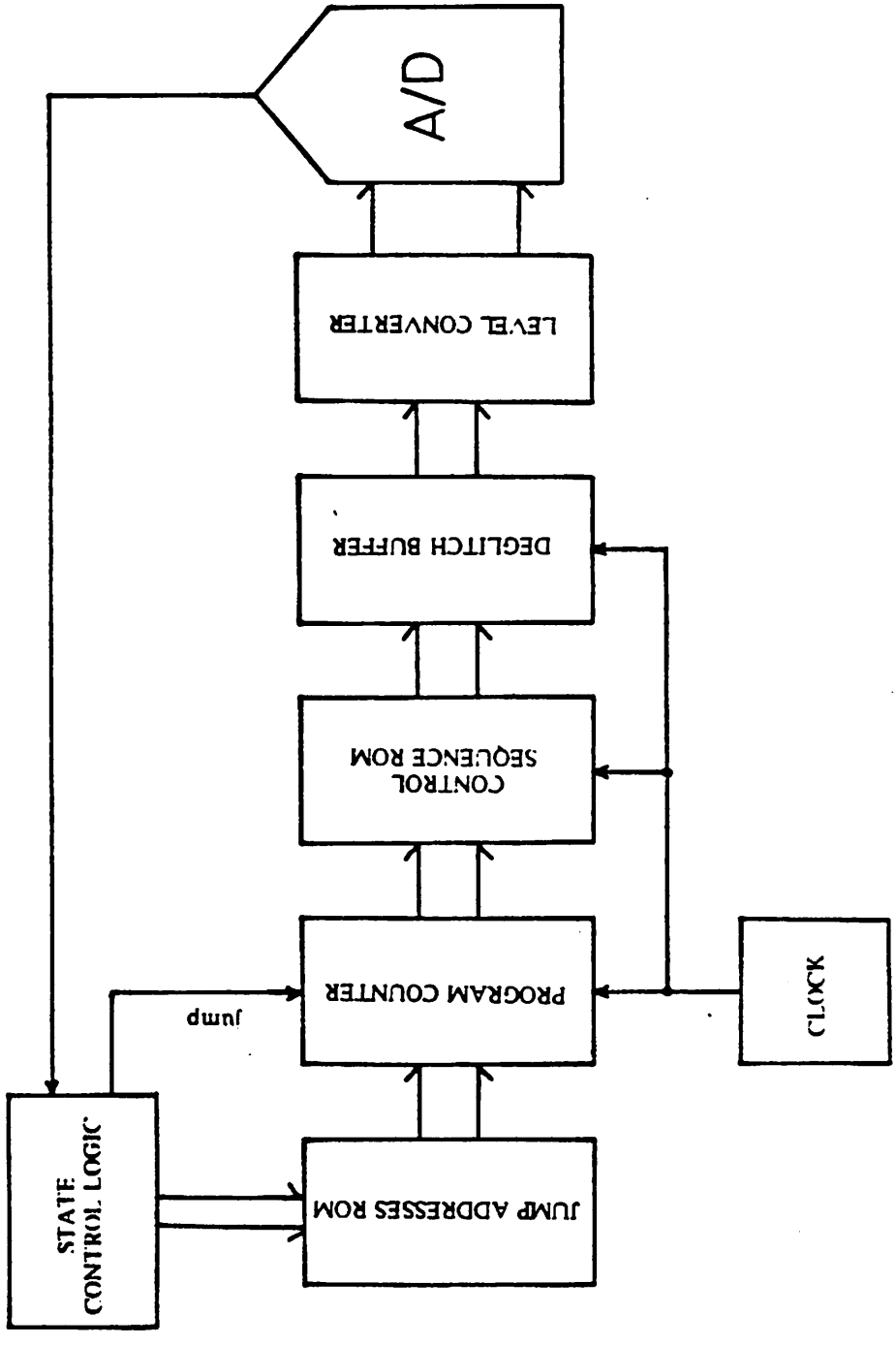


Fig 6.1 The block diagram of the finite state machine for the A/D

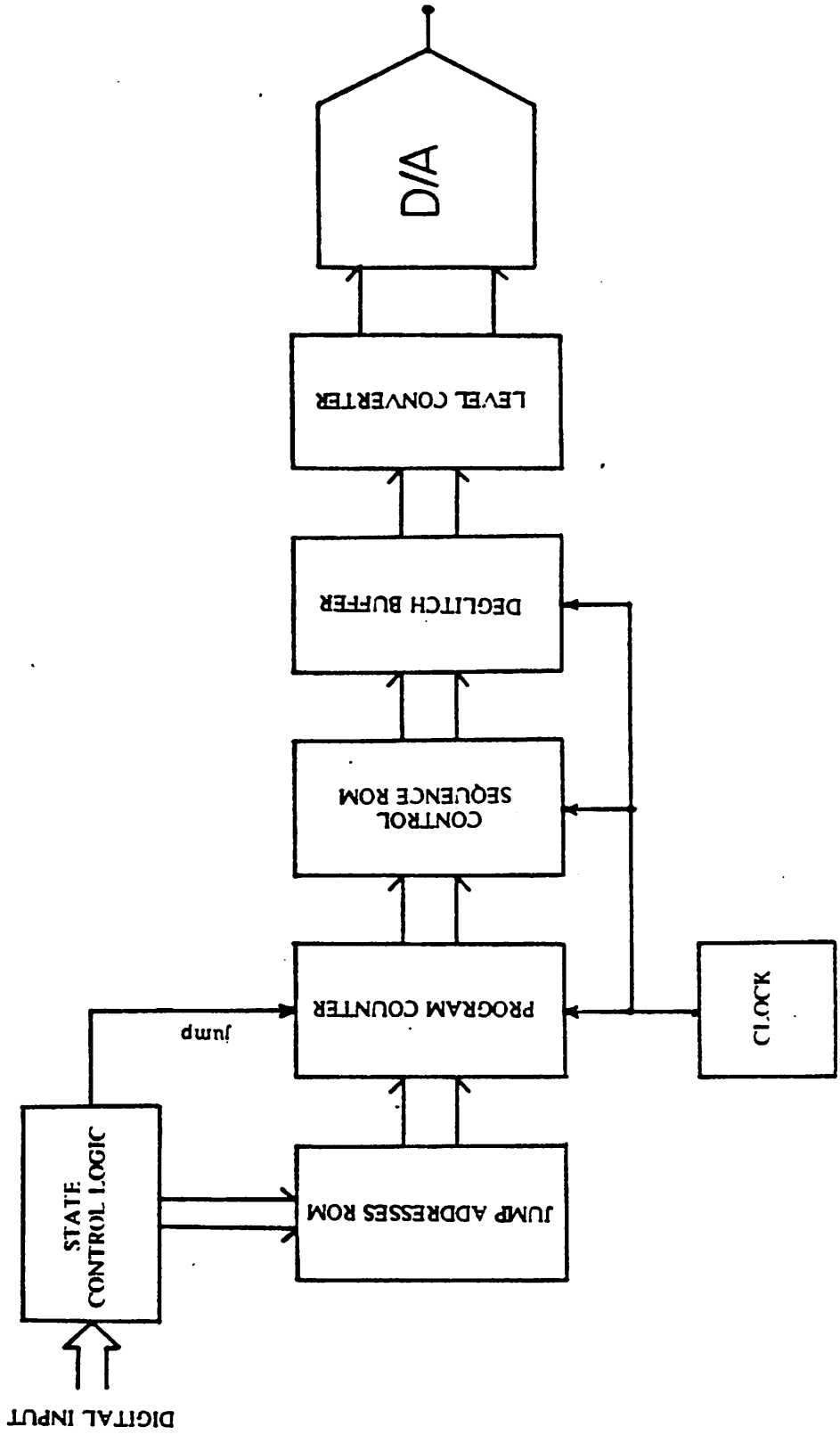


Fig 6.2 The block diagram of the finite state machine for the D/A

volt by a 1K ohm pull-up resistor. To convert a CMOS level signal back to TTL signal in a short time is more complicated than the TTL to CMOS level conversion. In Fig. 6.4, a CMOS analog switch (CD4066) and a TTL inverter together are used to achieve the transformation. The gate of the analog switch is connected to the CMOS output from the analog chip and the TTL logic low is connected to the input of the switch. A pull up resistor with one end tied to TTL logic high is used at the output node of the analog switch. When the gate signal is high, the analog switch is turned on and a TTL logic low appears at the output of the switch. On the other hand, when the analog switch is turned off, the output is at the TTL high level. Using this scheme, the transformation speed is as fast as the switching speed of the analog switch.

If all the control circuits for the converters are fabricated on one chip, the level conversion can be easily incorporated into the circuit design. In the actual implementation, the control circuit is straightforward and the estimated silicon area for the control portion is only around 600 mil^2.

6.2. Test Setup for A/D Converter

With the above described controller on one board, the analog chip is located on a separate vector board. The two external current sources required are built with two ten turns variable resistors. Two rechargeable batteries each with 1.2 voltage output are connected in series and applied as the external voltage reference.

A code density test method[Doer84] is adopted to perform the linearity testing of the A/D. The theory of code density test is based on the fact that the cumulative density of each digital output code after a long period of asynchronous sampling is closely related to the characteristic of the input signal and the transfer characteristic of the A/D converter. When a triangular wave which exercises the full range of the converter is applied to the input of a ideal converter, the frequency of appearance of every possi-

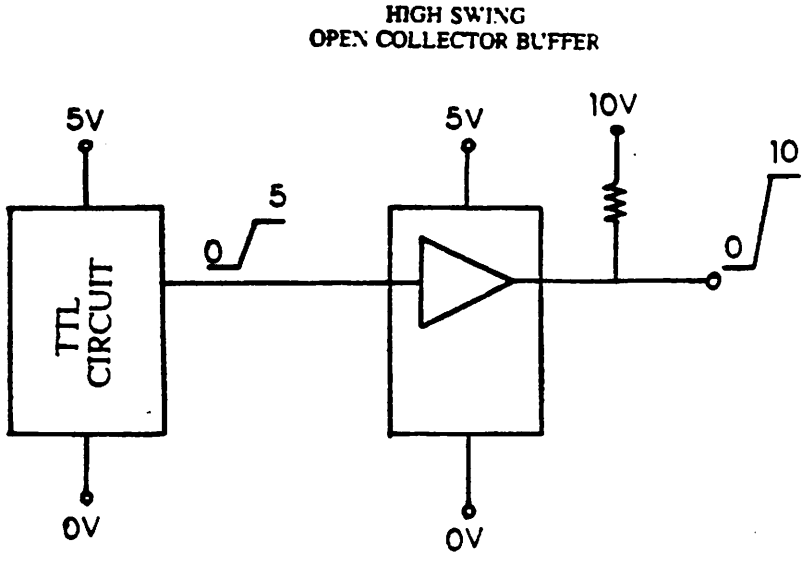


Fig 6.3 The TTL to CMOS level converter

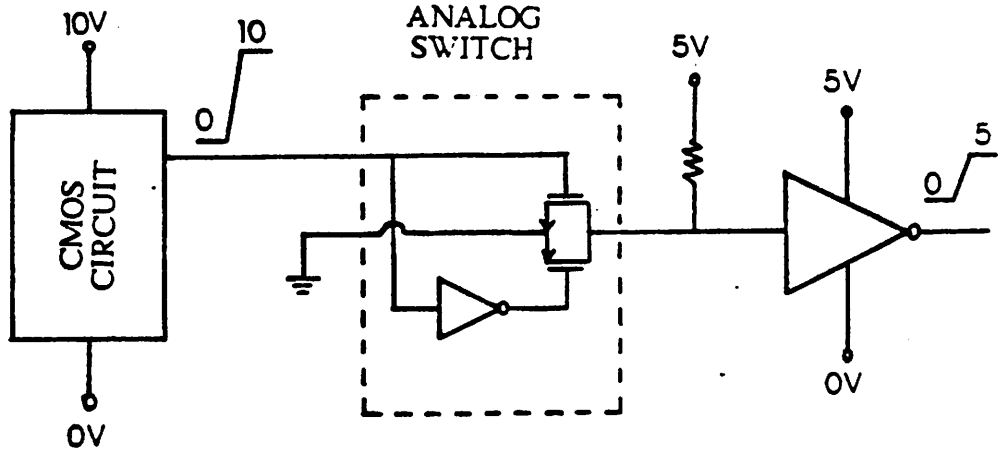


Fig 6.4 The CMOS to TTL level converter

ble digital output code is equally likely. By examining the code density output after a large number of samples, one should be able to see the results of converter imperfections . If any particular output code has not been detected even after the collection of a large number of samples, a missing code error has occurred. Furthermore, if too many or too few occurrence of specific code are detected, that code must have a abnormal stepsize and large differential nonlinearity is confirmed.

Since a low distortion triangular waveform is hard to acquire, a ultra low distortion sinusoid wave generator is used instead. Although the probability distribution of sinusoid wave at different magnitude is not uniform, it can be corrected by a deterministic function which compensates for the different slope at different input level.

The confidence of the result from the code density test is proportional to the number of samples that have been taken. With code density test, an inband sinusoid AC signal instead of a DC signal is used as the input to the converter . So the characteristics of the dynamic performance of the A/D, such as the sample and hold circuit and the timing jitter, are also evaluated by this test. The test setup is shown in Fig 6.5.

Another possible testing method for the A/D converter is the exact transfer curve testing. Just by stepping the input voltage by small increments across the whole input range of the A/D and collecting the corresponding digital outputs from the A/D converter, the detail transfer curve of a A/D converter can be plotted. With a programmable digital controlled precision voltage generator and a microcomputer such as HP9836, the whole testing procedure can be done automatically. Setup see Fig 6.6. The advantage of this testing method is that it gives the exact location of each analog transition point, which reveals more about the conversion characteristic than the code density test. However, in order to achieve the accuracy within 0.1 LSB for a high resolution N bit converter, the tester has to examine at least 10×2^N points to determine the differential or integral nonlinearity. And the time to complete one curve will be at least (the setup

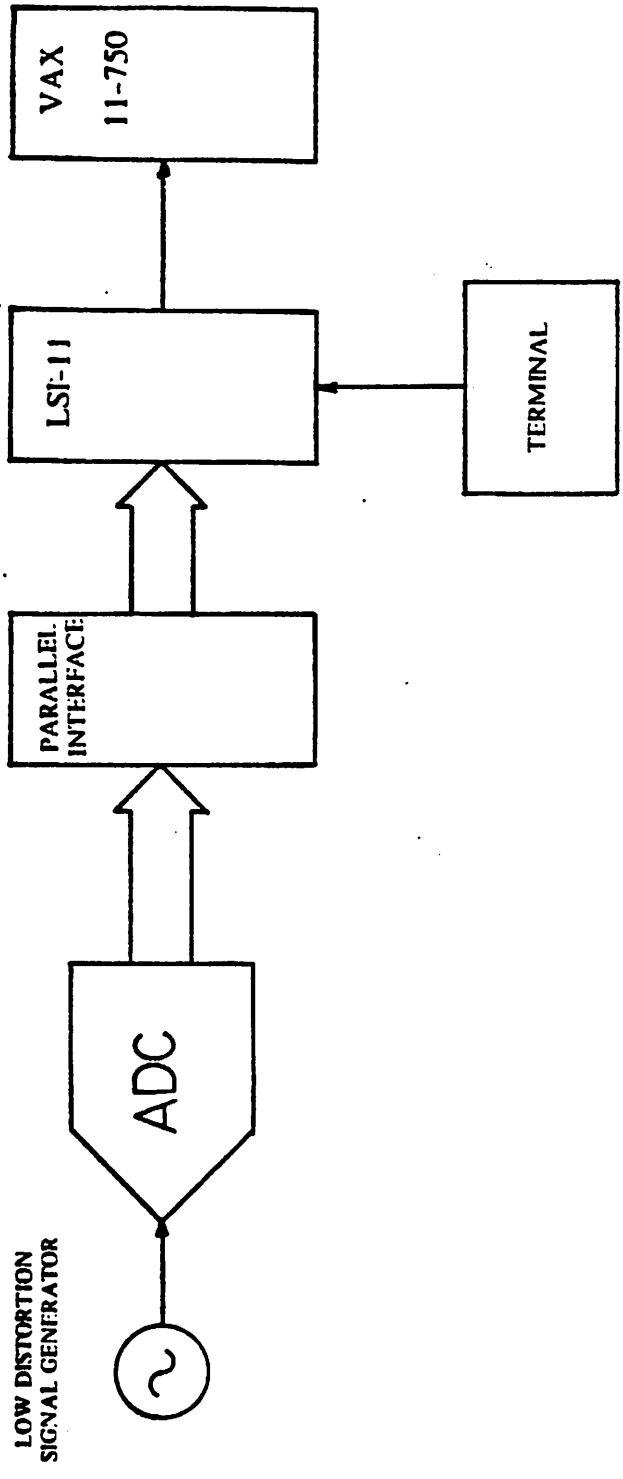


Fig 6.5 The test setup for the code density test

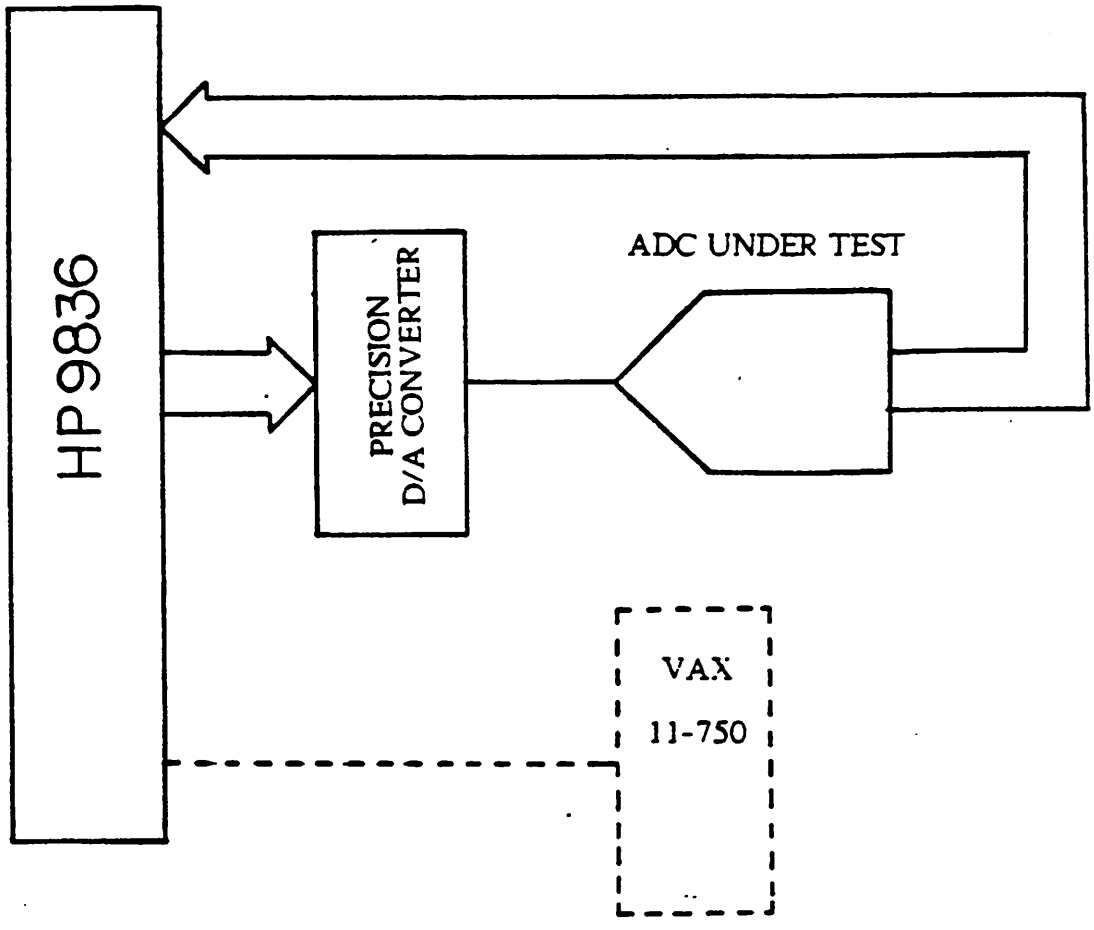


Fig 6.6 The automatic microcomputer controlled test setup for the A/D exact transfer curve test

time for the precision voltage source + the A/D conversion time) x 10 x 2^N . Normally, it is a very time consuming process for high resolution converter. Fortunately, the inherent characteristic of the cyclic conversion simplifies the testing of the A/D because the most significant nonlinearity will always happen at the major carries. A detail check up at those regions can determine the performance of the converter. One disadvantage of this testing process is that the dynamic performance of the converter is not tested because the input signal is always a DC signal.

The converter described in this paper was tested by the above two methods. Because the computer controlled automatic testing setup is still under development, the exact transfer curve testing performed in this research is done manually.

6.3. Testing Setup for D/A Converter

Exact transfer curve testing is also designed for the testing of the D/A converter. With a computer controlled setup, each digital code is applied to the D/A converter and the corresponding analog output is sampled and measured by a programmable precision digital voltage meter. The test setup is shown in Fig 6.7. For each digital code under test, more than one analog sample is taken per code and the average of these samples is used. After examining all of the possible input codes, the transfer curve of the D/A under test is generated. It is also true that the worst nonlinearity of the cyclic D/A converter will appear at the major carries. Just by looking into the performance of the converter around the major carry, the nonlinearity of the converter can be determined. This automatic testing setup for the D/A is also under construction.

This special testing characteristic of cyclic converters makes both the A/D and D/A cyclic converter attractive for commercial production because only the region around the major carries instead of the whole conversion range must be tested during the quality control stage. In another words, a lot of testing time and money is saved by choosing cyclic conversion.

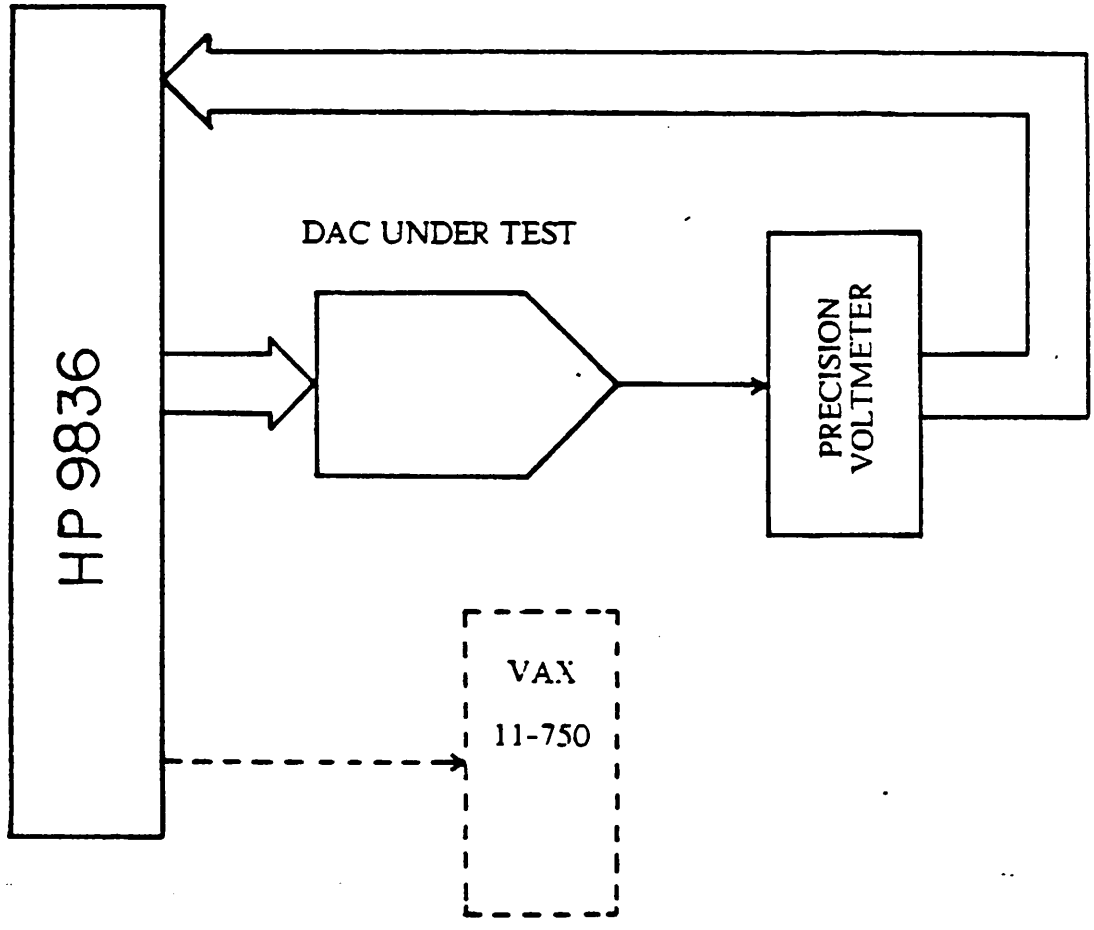


Fig 6.7 The automatic microcomputer controlled test setup for the D/A exact transfer curve test

CHAPTER 7

EXPERIMENTAL RESULTS

This project was fabricated through MOS Implementation Service (MOSIS) [1] which provides double polysilicon capacitor CMOS P-Well 5 μ process[2] and in Berkeley MICRO laboratory.[3] Both the analog portions of A/D and D/A converter have been transformed into silicon. A test operational amplifier and a test comparator that have the same design as the one used in the converter were fabricated at the same time to investigate the converter performance. The experimental results from these test chips are studied in this chapter.

7.1. Performance of the Operational Amplifier

The class. A single stage folded cascode amplifier is tested with the test setup shown in Fig 7.1. The output vs. input transfer curve of amplifier is shown in Picture 7.1. The maximum output swing of the amplifier before saturation is $\pm$ 5V, which is less than the SPICE simulation result. The reason is that the actual process γ value of 1.6 is much higher than expected. The common mode output variation with the maximum differential output swing is shown in Picture 7.2. The maximum common mode output deviation is less than 100 mV. The common mode output peaks at large output swing and the performance is sensitive to the bias current, as expected. The step response of the amplifier buffered with a source follower is displayed in Picture 7.3.

---

[1]MOSIS is a division under the University of Southern California sponsored by Defense Advance Research Projects Agency (DARPA).

[2]The MOSIS CMOS process normally is a 5 volt 3μ process but it is used in this project under 10 volt power supply. To compensate for increased supply voltage, the smallest channel length used in this project is 5μ instead of 3.5μ and many other design rules are also modified to make sure it can operated under 10 volt power supply.

[3]In Appendix, the detail Berkeley N-Well CMOS process procedures are shown. Because of the instability of the MICRO laboratory at those time, the chip was not very successful.

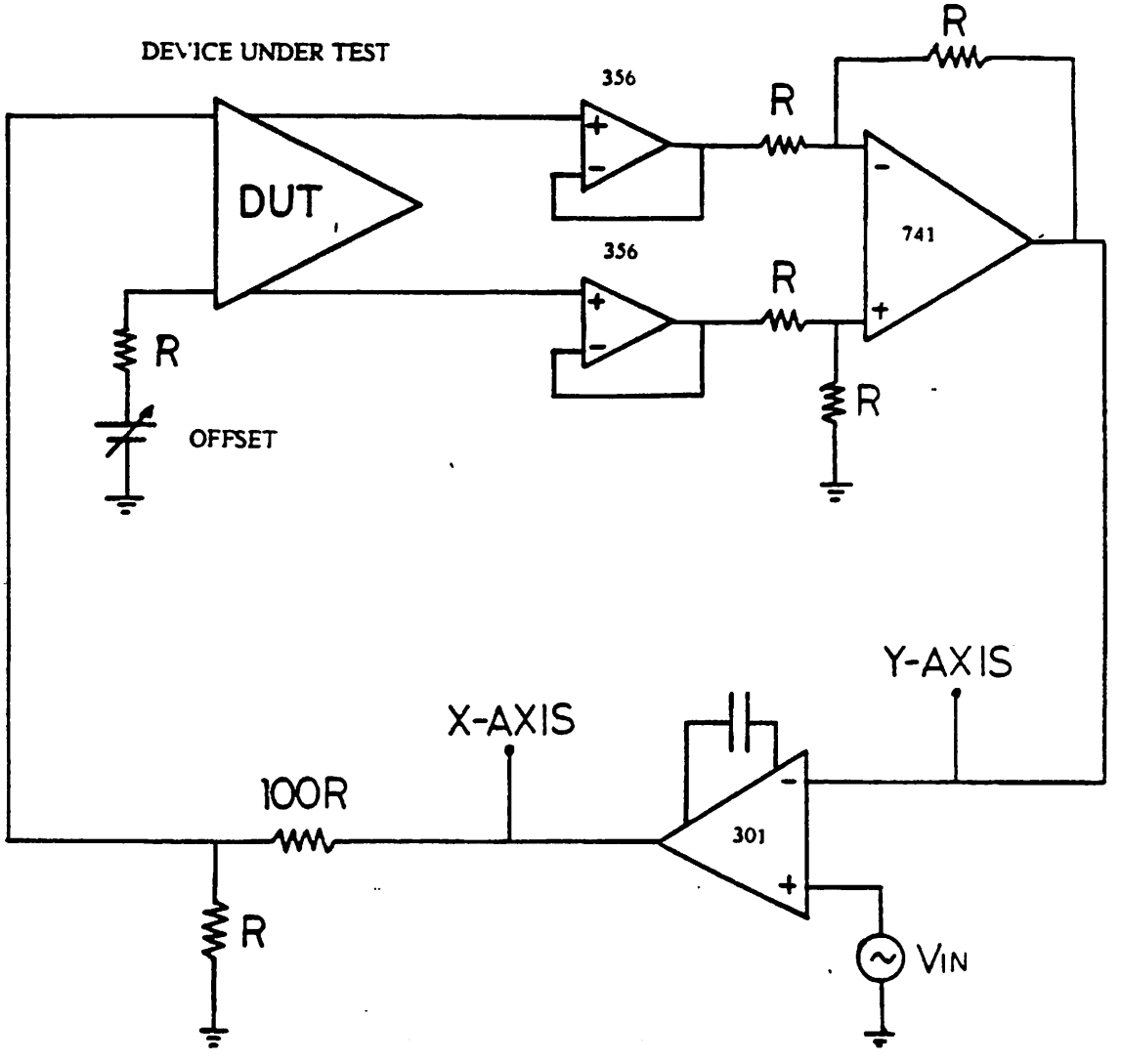
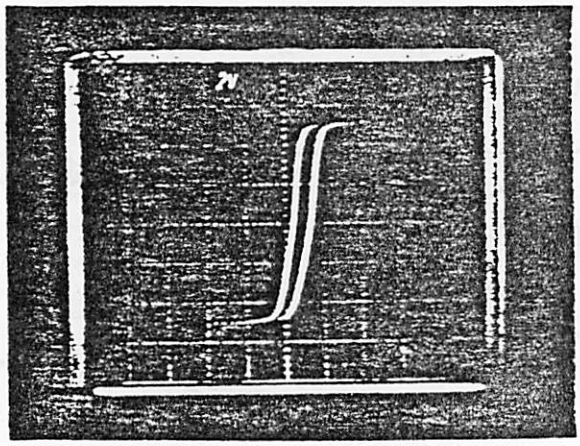
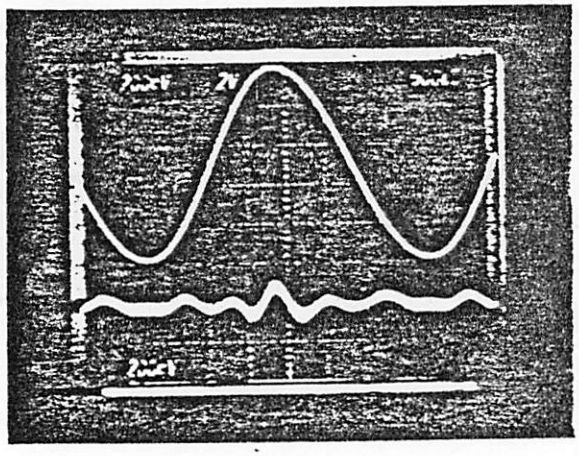


Fig 7.1 The test setup for a fully differential amplifier



Picture 7.1 The input vs. output transfer curve of the CMOS amplifier operated under ± 5V power supply



Picture 7.2 The common mode output variation vs the differential output

Because of the large capacitance load, the step response is much slower than internal transient response. The summary of the operational amplifier test performance is in Table 7.1.

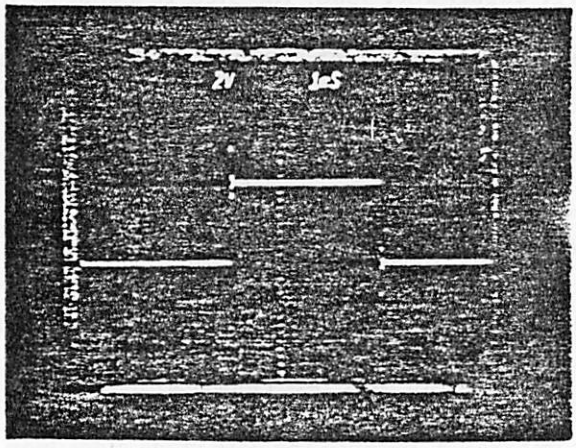
7.2. Performance of the Comparator

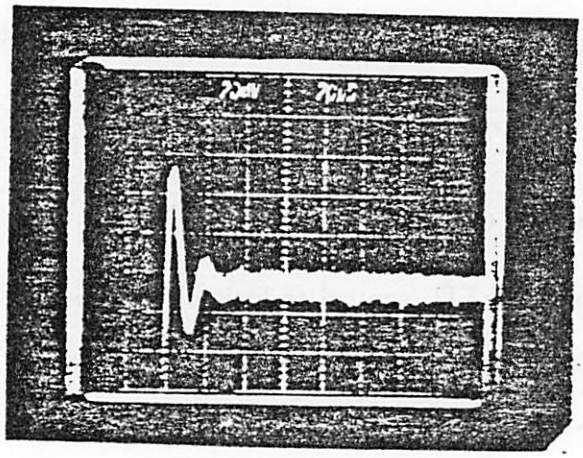
When connected as shown in Fig 7.2, the test comparator can resolve a 0.2mV input. Because of the design of this test comparator, there is no way to really measure the speed of this comparator. Because the gain stage close loop clear switchs are not provided in the test comparator, it needs a much longer time to change the output node voltage than normal. By examining the decision swing voltage level of the comparator, the offset of the comparator is measured. Even though the amplifier in the comparator is fully differential amplifier, some of the tested chips have the offset value as large as 30 mV.

7.3. Analog to Digital Converter

Using the external TTL controller logic circuit described in the previous chapter with the analog portion of A/D converter, this converter can perform as a restoring or nonrestoring converter. The die photograph of the A/D converter is shown in Picture 7.4. The internal voltage variations vs. time at the output of the operational amplifier #2 are examined in the following pictures. Because of the large capacitance of the output pad and the finite driving capability of a class A amplifier, the clock is slowed down to make this possible. In Picture 7.5, the restoring algorithm is shown and in Picture 7.6, the nonrestoring algorithm is shown. In both cases, the reference is toggled between positive and negative polarity to avoid the loop offset accumulation.

In Picture 7.7, an incorrect sign bit decision is caused by the comparator offset and the signal is saturated after a few cycles because the conversion can not recover the





Picture 7.3 The step response of the amplifier

EXPERIMENTAL AMPLIFIER PERFORMANCE		
Supply voltage	±5	V
Approximate die area	458	mil^2
Open loop voltage gain	76	dB
Power dissipation	5.5	mW
Load capability	2	pF
Slew rate	50	$V/\mu s$
±2.5 V output settle to within 0.5mV	1000	ns

Table 7.1 The summary of the test amplifier performance

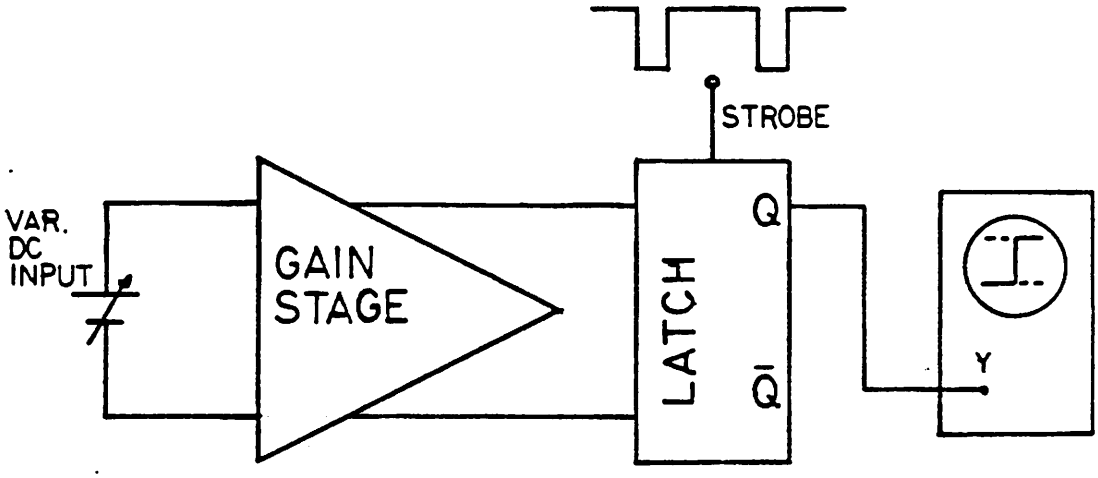
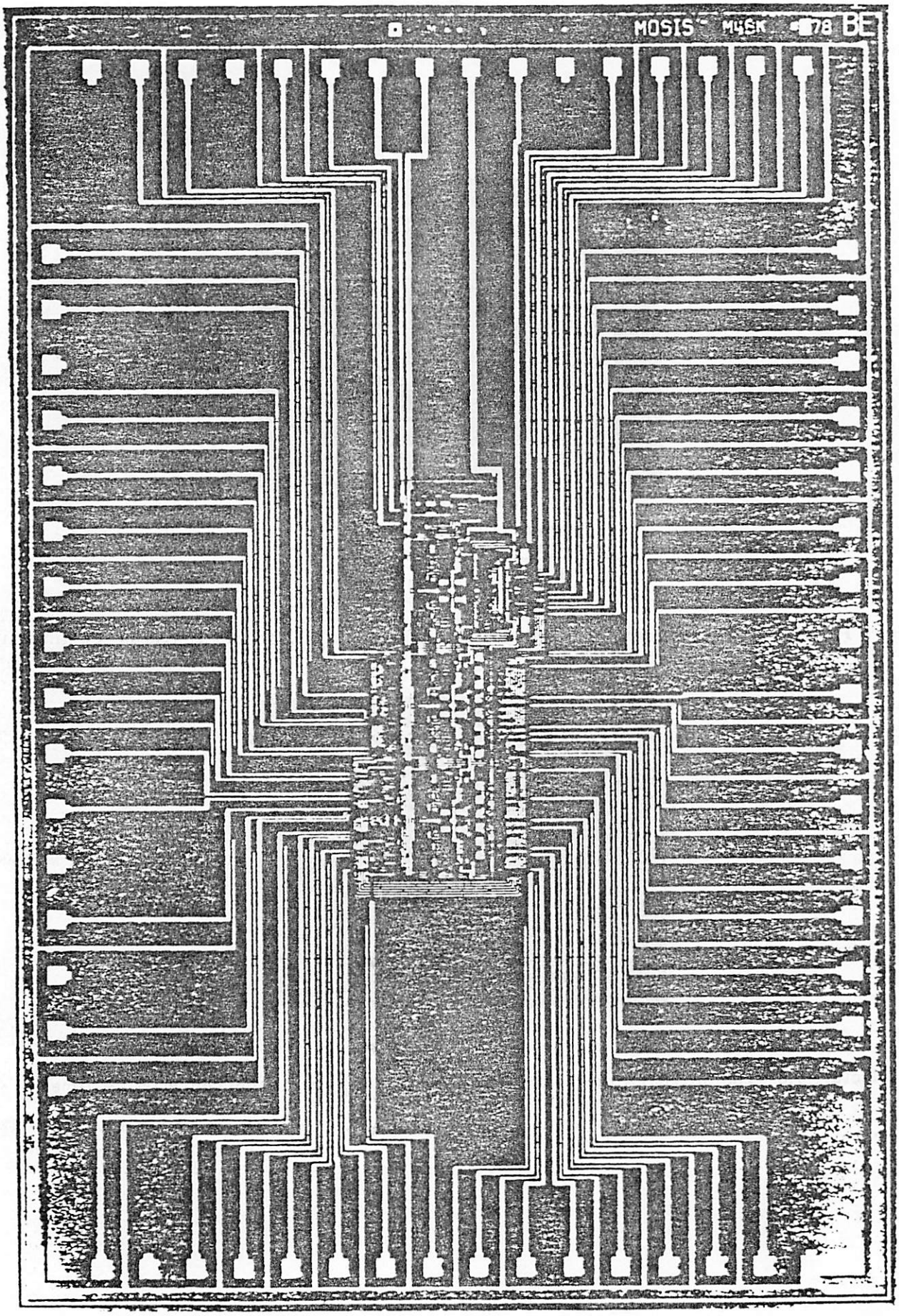
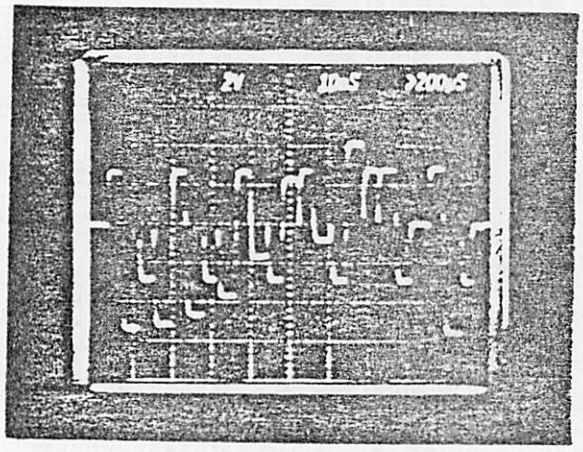


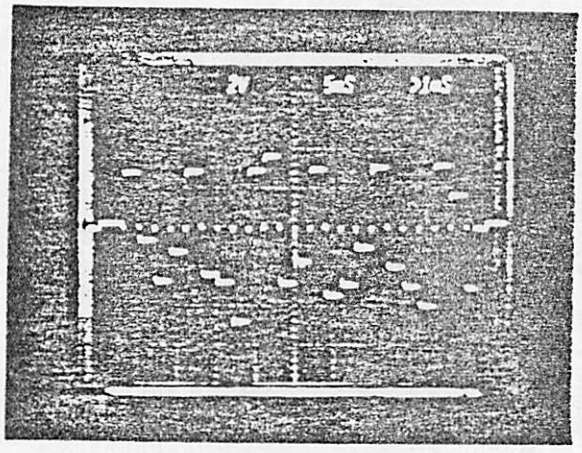
Fig 7.2 The test setup for a fully differential comparator



Picture 7.4 The die photo of the A/D converter



Picture 7.5 The internal voltage variation of restoring algorithm converter vs. time at amplifier #2 output



Picture 7.6 The internal voltage variation of nonrestoring algorithm converter vs. time at amplifier #2 output

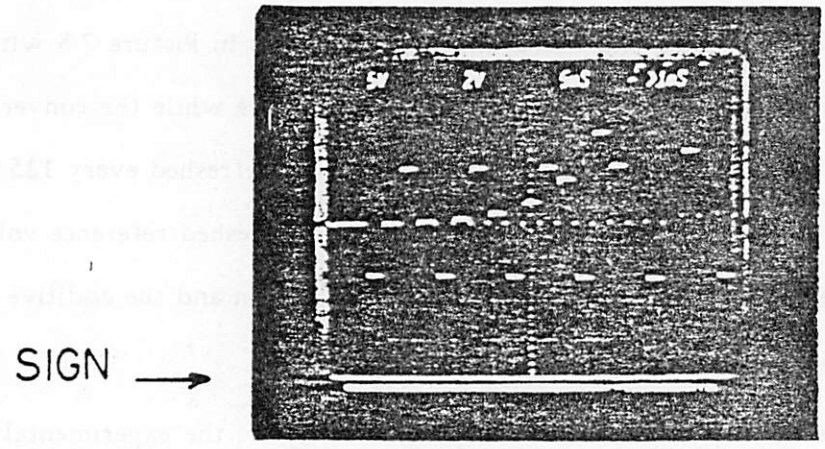
incorrect sign bit. In contrast, after the dead zone cancellation technique is implemented, the sign bit is corrected and no saturation is observed in Picture 7.8 with the same input level as Picture 7.7. The offset sampling is effective while the converter is running under full speed (8kHz) where the sampled offset is refreshed every 125 μsec. The residual offset is less than 1 LSB at 13 bit level. The refreshed reference voltages are examined on the oscilloscope and both the nonideal loop gain and the additive noise from the circuit is observed in Picture 7.9.

Using the code density test described in previous chapter, the experimental A/D converter performs only as an 8 bit converter with the reference refreshing technique disabled. After incorporating the reference refreshing technique, the A/D converter functions as a monotonic 13 bit converter with maximum of 1 LSB differential nonlinearity and $\pm$ 2 LSB integral nonlinearity. The differential nonlinearity curves of the converter, both before and after the reference refreshing technique, are shown in Fig. 7.3a,b.

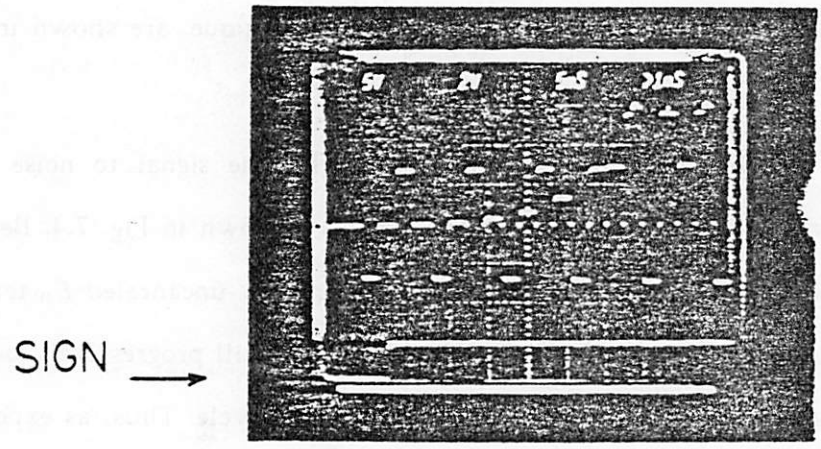
Evaluated by the Discrete Fourier Transform (DFT), the signal to noise ratio (S/N) of the converter with different input signal levels is shown in Fig. 7.4. Because as the reference is inverted on each pass through the loop, any uncanceled E_0 term is not accumulated on the reference. Any fixed zero order error will progressively be less significant as the signal itself gets amplified by two on each cycle. Thus, as expected, from the S/N ratio diagram, it is apparent that the A/D performs better for small signals than for large signals. The performance of the A/D is summarized in Table 7.2.

7.4. Digital to Analog Converter

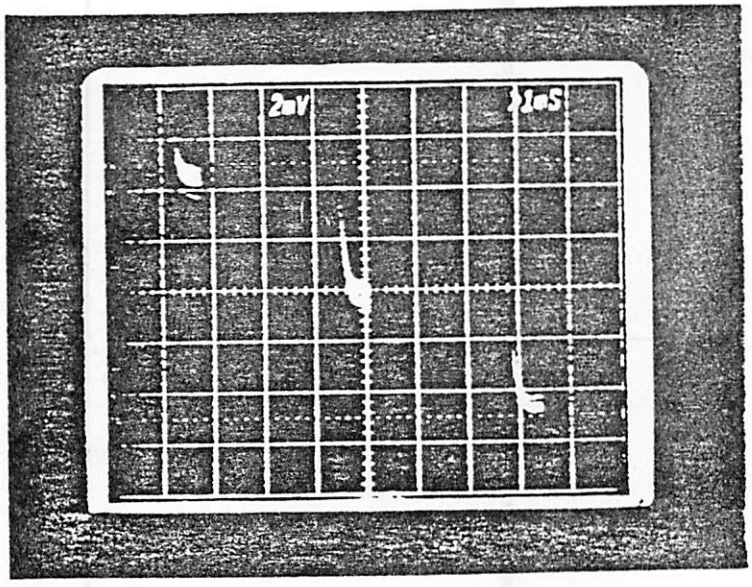
The die photograph of the analog portion of the D/A converter is shown in Picture. 7.10. Also using the external TTL controller, one example of the internal voltage variation at the output of #2 amplifier is shown in Picture. 7.11.



Picture 7.7 Because of comparator offset, the internal voltage becomes saturated after the 9th cycle.



Picture 7.8 After dead zone cancellation technique, the sign bit is corrected and signal has been decoded properly.



Picture 7.9 The effect of noise and nonideal loop gain on the refreshed references at different cycles

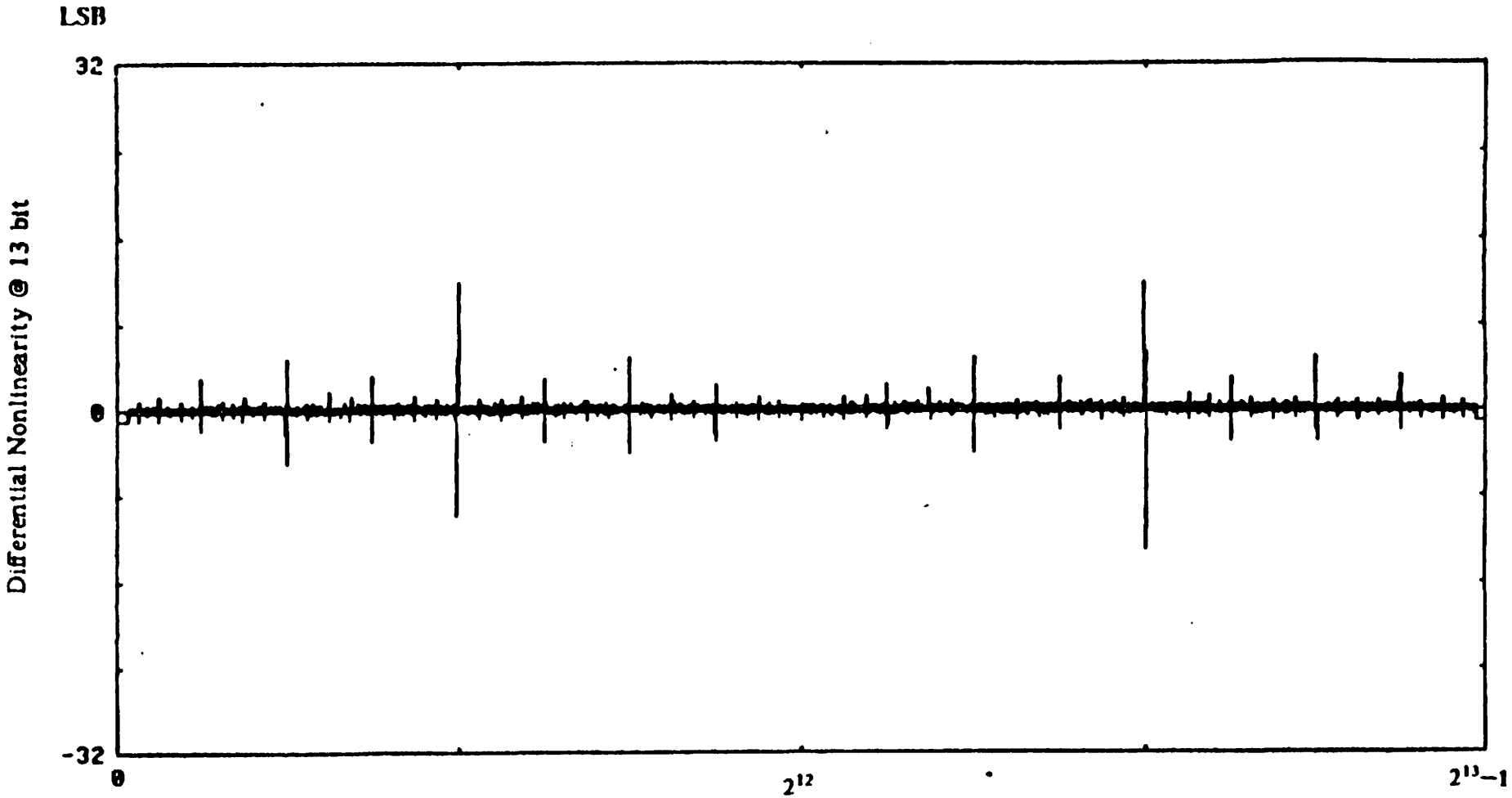
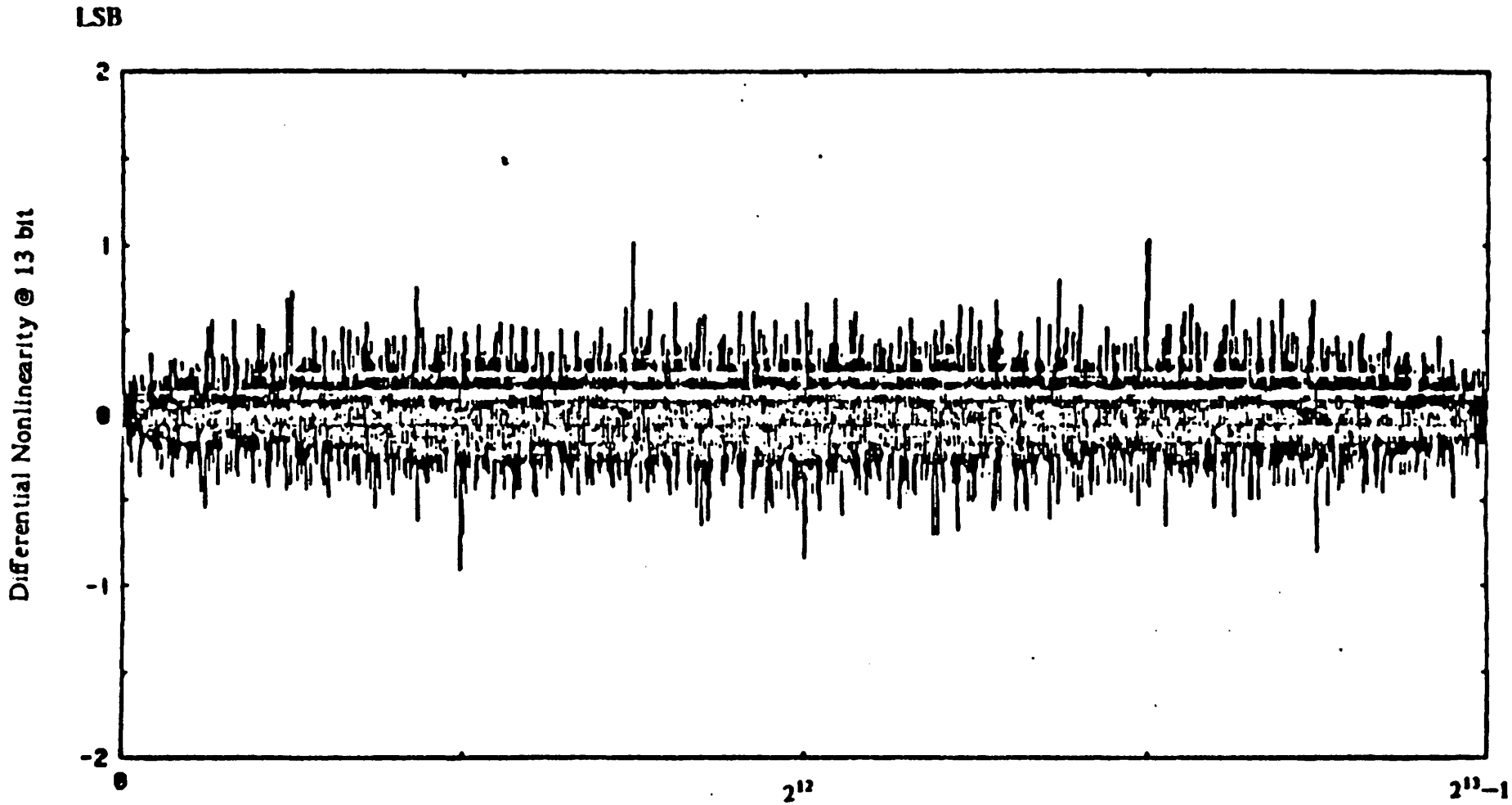


Fig 7.3 The differential nonlinearity (DN) of the converter tested under 13 bit level
(a) The converter experience maximum 15 LSB level DN converter when reference refreshing algorithm disabled



(b) The converter achieve 1 LSB DN with reference refreshing algorithm

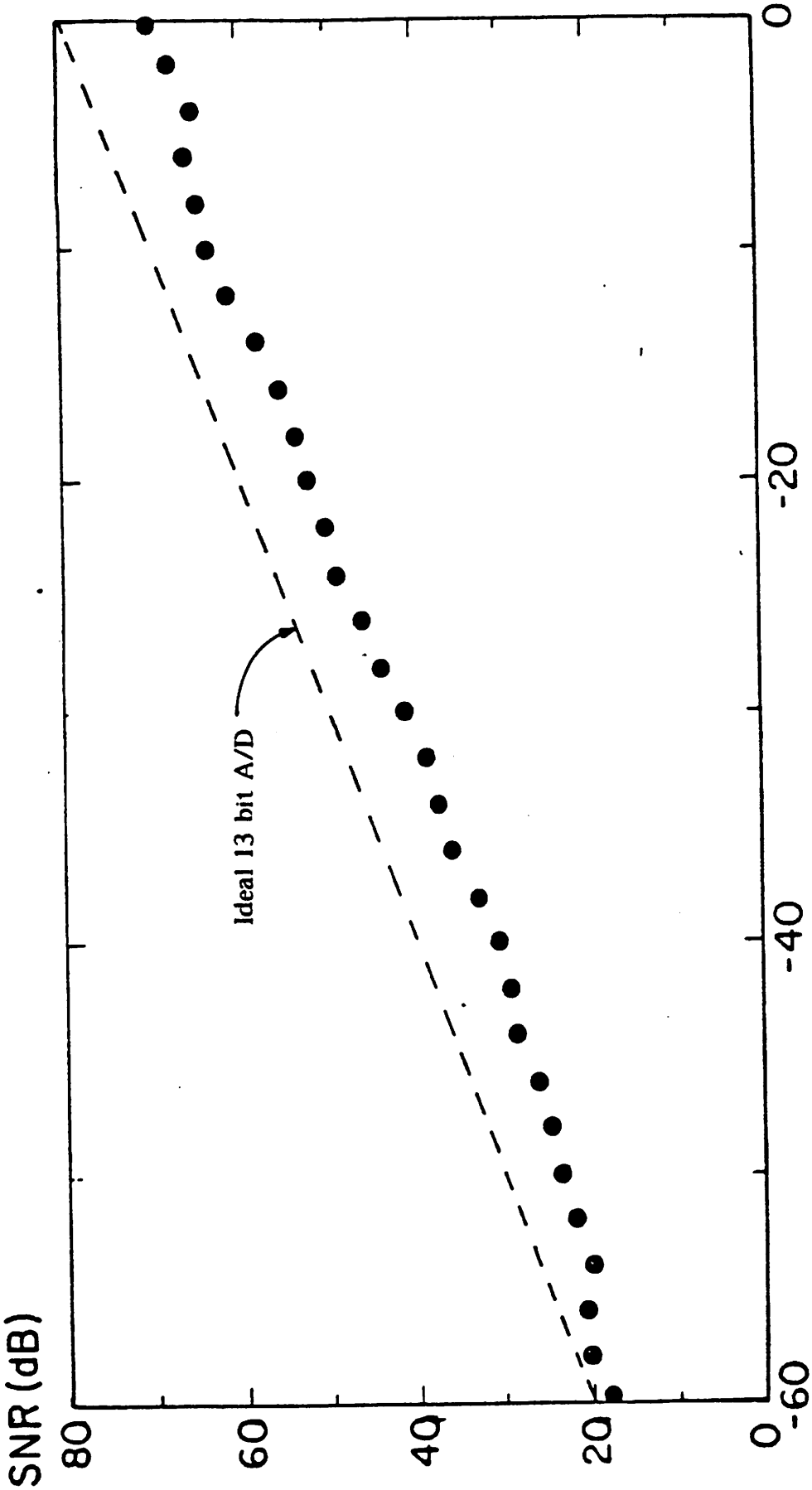
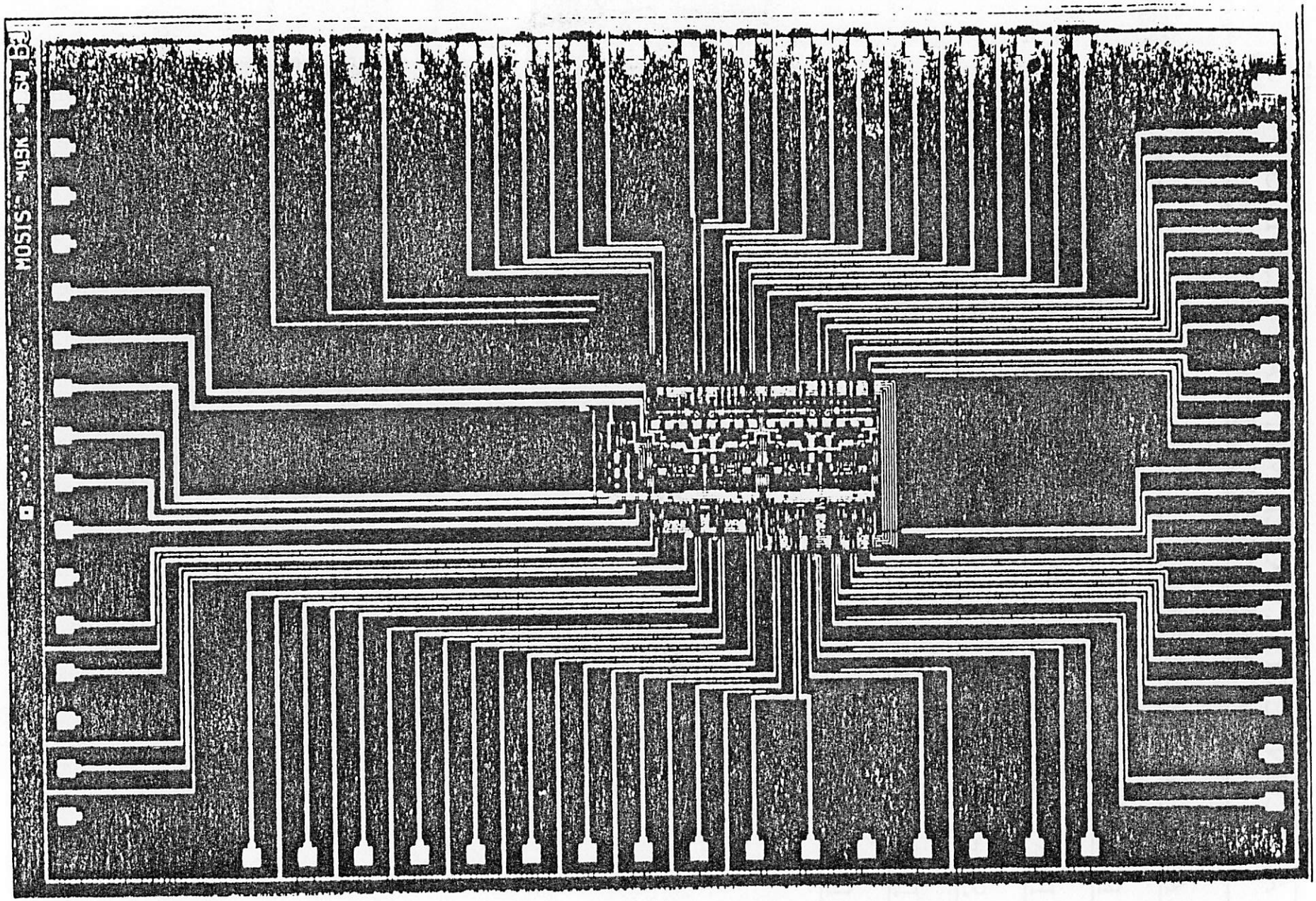


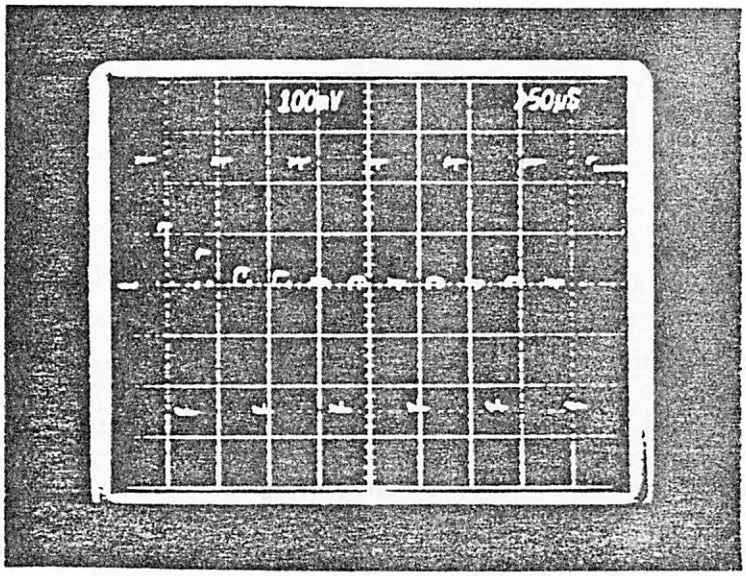
Fig 7.4 The SNR vs input signal level of the converter

A/D CONVERTER EXPERIMENTAL RESULTS (5 μ CMOS P-Well Technology)		
Approximate die area	1900	mil^2
Estimated control area	600	mil^2
Power dissipation	15	mW
Sampling Rate	8	KHz
Differential Nonlinearity	±1.0	LSB(13bit)
Integral Nonlinearity	±2.0	LSB(13bit)

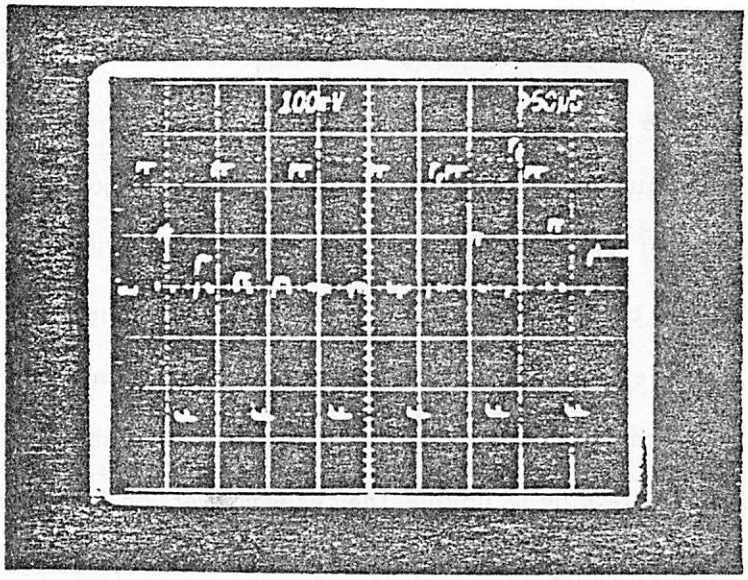
Table 7.2 The summary of the A/D performance



Picture 7.10 The die photo of the D/A converter



INPUT CODE =
010000000000



INPUT CODE =
000101000000

Picture 7.11 The internal voltage variation of D/A converter vs. time at the #1 amplifier output

CHAPTER 8

CONCLUSION

Switched capacitor cyclic A/D and D/A converters have been studied. With only two sample and hold amplifiers, one comparator, a few capacitors and several switches, a N bit conversion can be achieved by circulating the signal around one loop N times. Using the reversing polarity method on the sample and hold circuit, the multiplication by two function required by the A/D conversion is achieved. On the other hand, the divide by two function required by the D/A conversion is accomplished by changing the capacitor ratio from one to one half in the S/H circuit. The accuracy of the converter relys directly on the quality of the the S/H circuit and thus requires precisely matched capacitors and large open loop op-amp gain.

A new approach to algorithmic A/D and D/A conversion has been described that combines the techniques of switched capacitor cyclic conversion and reference voltage refreshing. Instead of having a fixed reference for the conversion, the reference used in this new technique is calibrated each cycle as it goes through the same path as the signal itself. Only a little extra circuit area and conversion time is needed to implement this analog calibration technique, and it works for both the A/D and D/A conversions. By using the reference refreshing technique, the cyclic conversion algorithm is made almost independent of the matching of the capacitor pairs and the operational amplifiers' open loop gain. Furthermore, with the offset sampling technique previously described, the algorithm is even independent of operational amplifier offset voltage. As a result, small component values and simple low gain operational amplifiers can be used; therefore, the die area required for this circuitry can be scaled as technological feature sizes are reduced. Instead of taking up half of the area of a complicated chip as most present

converters do. a high resolution reference refreshing converter only needs a small fraction of a processor chip. Moreover. at the cost of only one extra pair of capacitors. the D/A can time share most of the same circuits used for the A/D. resulting in a net area similar to that for the A/D converter along. Some other second order problems in the converter are solved with proper clocking and the fully differential architecture of the converter. By further decreasing the capacitors used in the converter. the performance of the converter will eventually be limited by the thermal noise (kT/C noise) existing in the converter. Another important benefit of the reference refreshing algorithmic converter is that the required testing procedures are simple. In mass production. the time required in testing makes many algorithms impractical to be used in commercial products.

A experimental chip fabricated using 5 μm rule P-Well CMOS process demonstrated initial linearity of only 8 bit. After the use of reference refreshing. a monolithic 13 bit 8KHz A/D converter with maximum 1 LSB differential nonlinearity is achieved in a 1900 mil^2 area. With more compact layout. the die area of the converter should be no larger than 1500 mil^2 .

APPENDIX

THE BERKELEY CMOS PROCESS (May 14, 1984)

1. INITIAL WAFER PREPARATION

A. Wafer Cleaning

a. Spin the wafer on the wafer spinner and carefully slide a Q-tip soaked with TCA across the wafer several times.

b. With the wafer still spinning, direct a jet of acetone onto the wafer to remove any trace of TCA.

c. Using a squirt bottle, spray the wafer with methanol. Wait 20 seconds and the stop the spinner.

d. Inspect under collimated light.

e. Repeat (a) through (d) if the wafers are spotted.

B. Piranha Clean 5 min

C. Water Break Test HF:DI/1:10

Immerse the cleaned wafer into the dilute HF solution for approximately 10 seconds. Slowly pull out the wafer. If the wafer has been properly cleaned, the HF solution will sheet off from the surface.

2. INITIAL OXIDATION

Initial Ox Furnace
TCA clean prior to use.
1100 °C target: 315nm

Push	N_2	10.0	5 min
Ox	O_2	11.0	240 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	5 min

3. N-WELL DEFINITION

A. Standard Photolithography

HMDS	3 min on/5 min N2 purge
	(only enough bubbles to surround the tube)
AZ-1350J	6000 rpm/30 sec
Softbake	90 °C /15 min
Pattern	6.3
Develop	Micro-Dev:DI/1:1 30 sec
Hardbake	115 °C /20 min

The nominal exposure is 5.6. However, it is advised that you perform an exposure test to ascertain the optimal exposure setting. The exposed pattern under optimal condition should develop in 60 to 70 seconds.

B. Oxide Etch BHF/until well area becomes hydrophobic (2 min)

C. N-Well Implantation

Phos/100 Kev/8 ° /1.5 x 10^{12}

D. Photoresist Removal

Acetone 1 min/MeOH & DI rinse /Piranha 5 min

E. N-Well Drive In

Buried Layer Furnace
TCA clean prior to use
Piranha Clean 5 min

1100 °C

Push	N_2	15	3 min
Ox	O_2	15	280 min

Ramp furnace to 1150 °C

Drive	N_2:O_2	5.0:15	720 min
Anneal	N_2	10.0	20 min
Pull	N_2	10.0	3 min

The N-Well drive in is performed in a 10% O_2 atmosphere.

4. BUFFER OX OXIDATION

A. Oxide Etch Back

HF:DI 1:5 Etch until wafer becomes hydrophobic (~ 8 mins)

B. Piranha Clean5 min

C. Oxidation

Dry throughly
N-Drive Furnace
TCA Clean prior to use

1000 °C target: 55 nm

Push	N_2	10.0	3 min
Ox	O_2	11.0	50 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	3 min

5. NITRIDE DEPOSITION

Use dummy slats to smooth out the gas flow.
Place the wafers on the boat with the active faces of wafers facing each other.
Nitride should be deposited right after gate oxidation. This will prevent the gate from becoming contaminated. Nitride is an excellent barrier to contaminants.
The nitride deposition rate is higher at the outer surface than at the inner surface. Furthermore, the uniformity is better on the latter.

Gas flows are to be set to:

NH3	600mT	
SiH4	100mT	Determine the time by the dummy run

Deposit 150 nm (at the thinest area) of Nitride
2 hours and 15 mins facing outward.

6. ACTIVE DEFINITION

A. Standard Photolithography (Dry it thoughly double the dring time)

B. Nitride Etch

Preheat	N_2/1 Torr/60 W/70 oC
Descum	O_2/.76 Torr/10 W/5 min
Use parallel plate	SF_6–O_2/60 °C /100 W/ 15min

7. P-Field Definition

A Photoresist Removal

Acetone-Methonal-DI-Piranha 5 min

B Bake 115 °C/5 min

C Standard Photolithography

D P-Field Implantation

Boron/100 Kev/ $1.5x\ 10^{13}$

E. Backside Implantation

15. NMOS DEFINITION

A. Deglaze

The phosphorous glass must be removed prior to photolithography. Photoresist will not adhere to phosphorous-rich glass.

HF:DI/1:10 10~ 20 sec
Do the water break test to determine the time.
Do not dipe over 1 min.
Piranha Clean 5 min. (Grow a thin layer of oxide to get better adhesion)

B. IR Bake 30 min (Lower the IR lamp and Dry it very thoughly)

C. Standard Photolithography

D. Standard Polysilicon Etch

Preheat N2/1 Torr/60 W/70 oC
Descum O2/.76 Torr/10 W/5 min
Use parallel plate SF_6-O_2/60 °C/50W/~ 3min
Flow rate for SF_6 is 20 and O_2 is 2

* Polysilicon etches faster than nitride. We
* advise that you etch one wafer at a time.
* The parallel plate plasma etcher etch faster toward
* the center. Put the wafer's flat side outward.
* Use the end-point detecter to prevent over etch.

E. Photoresist Removal

Acetone 1 min/MeOH & DI Rinse/Piranha 5 min

F. Implantation

As/180 Kev/$3x\ 10^{15}$

16. PMOS DEFINITION

A. Piranha Clean 5 min

B. Standard Photolithography

C. Standard Polysilicon Etch

Be very careful when defining the PMOS poly gate. Visual detection of end-point is next to impossible. Therefore, etch in SF6-O2 for 50% of the time required during NMOS gate definition. Inspect the wafers under the microscope, and etch again if necessary. Be very careful not to over-etch. Averagely it takes less time than the NMOS etching time.

D. Pre-implantation Bake

N2/1 Torr/60 W/45 min

E. Implantation

Boron/60 KeV/ $2x\ 10^{15}$

F. Photoresist Removal

Ash off photoresist
O2/1 Torr/120 W/40 min

G Poly Reoxidation

Piranha clean 5 min
P Drive-in furnace
1000 °C

Push	N_2	10.0	5 min
Ox	O_2	11.0	30 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	5 min

17. PASSIVATION

A. Piranha Clean 5 min

B. CVD Deposition

350 nm undoped CVD oxide
650 nm 7% PSG oxide
* Due to high reflow temperature, a sandwich
* layer of CVD oxide is necessary in order to
* prevent the counter-doping of the p+ diffusions.

C. Reflow and Densification

N-Drive Furnace
1050 °C

Push	N_2	5.0	3 min
Densify	N_2	5.0	20 min
Pull	N_2	5.0	3 min

18. CONTACT DEFINITION

A. Standard Photolithography (Increase the light dose to 6.0~6.2, use dummy wafer to test the best exposer time)

B. Oxide Etch

Determine the PSG etch rate from the blank dummy wafers. Use this etch rate to gauge your etch-bake time cycle.
(1. 15sec 2. 30sec 3. 30sec 4. 45sec 5. 60sec...
after 6 min increase every two mins)

Etch/Bake/Etch to prevent contact cuts from blooming.

Etch BHF
Bake 130 °C /10 min

Repeat as many times as required.

C. Remove Photoresist

Acetone 1 min /Rinse with Methanel & DI/Piranha 5 min

19. METALLIZATION

A. Oxide Dip

HF:DI/1:10 5 sec

This oxide dip removes the thin oxide which
was grown over the vias during piranha cleaning.

B. IR Bake 20 min

C. Aluminum Sputtering target: 500~ 1000A

Set the sputtering machine 470V/1.5A/10mT
Open the shutter for 15 sec then cool down for 4 min
Repeat as many time as needed.
Growth rate is about 0.35u min at center. 0.25 at edge

20. METAL RUN DEFINITION

A. Standard Photolithography

Use 5.5 for exposer time
Reduce exposure time by 25%
Canon each nobe is 6%

B. Metal Etch

Aluminum Etchant Type A 45 °C

C. Photoresist Removal

Acetone 5 min

21. BACKSIDE PREPARATION

A. IR Bake 10 min

B. Spin on protective photoresist

C Etch the back poly either in barrel reactor or parallel plate

D. Oxide etch (Etch till hydrophobic)

E. Aluminum sputter on the backside target: 1 um

F. Photo Resist Removal Acetone 5 min

22. SINTERING

Forming gas N_2:H_2 10:1	15 cm	20 min	350 °C

REFERENCES

Beye81. J.W. Beyers, L.J. Dohse, J.P. Fucetola, R.L. Kochis, C.G. Lob, G.L. Taylor, and E.R. Zeller, "A 32b VLSI CPU Chip," *1981 IEEE International Solid-State Circuits Conference*, pp. 104-105 (Feberary, 1981).

Blac80. W.C. Black, "High Speed COMS A/D CONVERSION TECHNIQUES," pp. 53 in *Ph.D. Dissertation*, University of California , Berkeley, California (1980).

Brod76. R.W. Brodersen and S.P. Emmons, "Noise in Buried Channel Charge-Coupled Devices," *IEEE Journal of Solid-State Circuits* **SC-11**(Feb. 1976).

Cand74. J.C. Candy, "A Use of Limit Cycle Oscillations to Obtain Robust Analog to Digital Converters," *IEEE Trans. on Communicaitons* **COM-22** pp. 298-305 (March 1974).

Cand85. J.C. Candy, "A Use of Double Integration in Sigma Delta Modulation," *IEEE Trans. on Communicaitons* **COM-33** pp. 249-258 (March 1985).

Cand76. J.C. Candy, Y.C. Ching, and D.S. Alexander, "Using Triangularly Weighted Interpolation to Get 13-Bit PCM from a Sigma-Delta Modulator," *IEEE Trans. on Communicaitons*, pp. 1268-1275 (Nov. 1976).

Choi83. T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, and P. R. Gray, "High-Frequency CMOS Switched-Capacitor Filters for Communications Application ," *IEEE Journal of Solid-State Circuits* **SC-18** pp. 652-664 (December 1983).

Coop81. M. Cooperman and R. Zahora, "Charge Redistribution Codec," *IEEE Journal of Solid-State Circuits* **SC-16** pp. 155-163 (June, 1981).

Doer. J. Doernberg, *Private Communication*, University of California, Berkeley, California

Doer84. J. Doernberg, H-S Lee, and D. A. Hodges, "Fully Speed Testing of A/D Converters ," *IEEE Journal of Solid-State Circuits* **SC-19** pp. 820-827 (December 1984).

Ever79. J.D. Everard, "A Single-Channel PCM Codecs," *IEEE Journal of Solid-State Circuits* **SC-14** pp. 25-37 (February, 1979).

Gray. P.R. Gray, *Private Communication*, University of California, Berkeley, California

Gray84. P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons Inc., New York, NY (1984).

Grov67. A.S Grove, *Physics and Technology of Semiconductor Devices*, J. Wiley and Sons Inc. , New York (1967).

Haus. M. Hauser, *Private Communication*, University of California, Berekely, California

Hodg. D.A. Hodges, *Private Communication*, University of California, Berekely, California

Hsie81. K. C. Hsieh, "Noise limitations in switched-capacitor filters," *Ph.D. dissertation, Univ. Califonia, Berkeley* , (December 1981).

Kama76. T. Kamata, K. Tanabashi, and K. Kobayashi, "Substrate Current Due to Impact Ionization in MOSFET," *Jpn. Journal Applied Physics* **14** p. 1127 (1976).

Lee84. H-S Lee, D. A. Hodges, and P. R. Gray, "A Self-Calibration 15 Bit CMOS A/D Converters ," *IEEE Journal of Solid-State Circuits* **SC-19** pp. 813-819 (December 1984).

Li84. P. W. Li, M. J. Chin, P. R. Gray, and R Castello, "A Ratio-Independent Algorithmic Analog-to-Digital Conversion Technique ," *IEEE Journal of Solid-*

State Circuits **SC-19** pp. 828-836 (December 1984).

McCh78. R. H. McCharles, "Charge Circuits for Analog LSI ," *IEEE Transactions on Circuits and Systems* **CAS-25** pp. 490-497 (July 1978).

McCh77. R. M. McCharles, V.A. Saletore, W.C. Black, and D.A. Hodges, "An algorithmic analog to digital converter," *ISSCC Dig. of Technical Papers*, pp. 96-97 (February 1977).

McCr81. J.L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitor," *IEEE J. Solid-State Circuits*, **SC-16** pp. 608-616 (Dec. 1981).

McCr75. J.L. McCreary and P.R. Gray, "All-MOS Charge-Redistribution Analog-to-Digital Conversion Techniques," *IEEE J. Solid-State Circuits* **SC-10** pp. 371-379 (Dec. 1975).

Mess. Messerschmitt, *Class Notes for EECS 2901*, University of California, Berkeley, California

Rabi78. L. R. Rabiner and R. W. Schafer, *Digital Processing of Speech Signals*, Prentice-Hall Inc., Englewood Cliffs, NJ (1978).

Shih83. C.-C. Shih, "Charge Injection and Clock Feedthrough in MOS Circuit ," Report on Class Project for Solid-State Devises, Univ. Califonia, Berkeley (March 1983).

Shyu84. J.-B. Shyu, G. C. Temes, and F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources ," *IEEE Journal of Solid-State Circuits* **SC-19** pp. 948-955 (December 1984).

Smar76. G. Smarandoiu, K. Fukahori, P.R. Gray, and D.A. Hodges, "An All-MOS Analog-to-Digital Converter Using a Constant Slope Approach," *IEEE Journal of Solid-State Circuits* **SC-11** pp. 408-410 (June, 1976).

Tsiv76. Y.P. Tsividis, P.R. Gray, D.A. Hodges, and J. Chacko, Jr., "A Segmented μ-255 Law PCM Voice Encoder Utilizing NMOS Technology." *IEEE Journal of Solid-State Circuits* **SC-11** pp. 740-747 (Dec. 1976).

Yama81. K. Yamakido, T. Suzuki, H. Shirasu , M. Tanaka , K. Yasunari, J. Sakaguchi, and S. Hagiwara, "A Single-Chip CMOS Filter/Codec." *IEEE Journal of Solid-State Circuits* **SC-16** pp. 302-307 (Auguest, 1981).

Yiu. L.-C. Yiu, *Private Communication*, University of California, Berkeley, California