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MOS TRANSISTOR MODELING AND CHARACTERIZATION FOR CIRCUIT SIMULATION

by

Bing Jay Sheu

Memorandum No. UCB/ERL M85/85

26 October 1985

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

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Ph. D. Bing Jay Sheu Department of EECS

Chairman of Committee

Abstract

This thesis describes the development of an accurate and computationally efficient metal-oxide-semiconductor transistor model and its associated characterization facility for advanced integrated-circuit design. Both the strong-inversion and weak-inversion components of the drain current are included. In order to speed up the circuit-simulation execution time, the dependence of the drain current on the substrate bias has been modeled with a numerical approximation. This approximation also simplifies the expressions for the transistor terminal charges. The charge model was derived from its drain-current counterpart to preserve consistency of the device physics. Charge conservation is guaranteed in this model.

The transistor parameters are extracted by an automated parameter extraction program. Circuit designers need only describe the layout geometries of the transistors and parasitic elements to execute circuit simulation. Use of the model to analyze device characteristics from several fabrication processes has resulted in good agreement between measured and calculated results for transistors with effective channel lengths as small as one micron. It is anticipated that only minor enhancements are necessary to extend this model for submicron devices.

DEDICATION

I dedicate this dissertation to my parents, brother, and sisters.

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CHAPTER 1

INTRODUCTION

Increases in the level of integration of very large-scale integrated (VLSI) circuits are realized mainly through the shrinkage of device dimensions. With the current rapid development of high performance metal-oxide-semiconductor integrated-circuit (MOS IC) technologies, the minimum-feature sizes for production processes have shrunk from 10 μm in production in 1971 to 2.5 μm in 1981 [1.1]. VLSI circuits with transistor effective channel lengths of 1.2 μm are in volume production in 1985. Further scale down to 0.5 μm is expected to be realized in 1990. With the present speed of technology improvement continues, the level of integration will increase from 10^6 transistors per chip in the year 1985 to 10^7 transistors per chip in 1990. Such marvelous technological advances have made possible the implementation of a whole system in a single chip.

For efficient integrated-circuit design, computer-aided tools have become indispensable. Currently such tools in simulation, layout, and automatic synthesis are being heavily used. In Fig. 1.1, a selection of some of these tools available in the public domain are shown.

The SPICE1 and SPICE2 (Simulation Program with Integrated Circuit Emphasis) programs [1.2,1.3] has been widely accepted for circuit analysis since its introduction a decade ago. Circuit simulation has been speeded up substantially through algorithm improvement and hardware enhancements in the past few years. Novel circuit-simulation algorithms, such as the iterated-timing-analysis method [1.4] and the waveform-relaxation method [1.5], promise to offer more than an order of magnitude speed-up as compared with the conventional circuit simulator SPICE2. The dedicated-

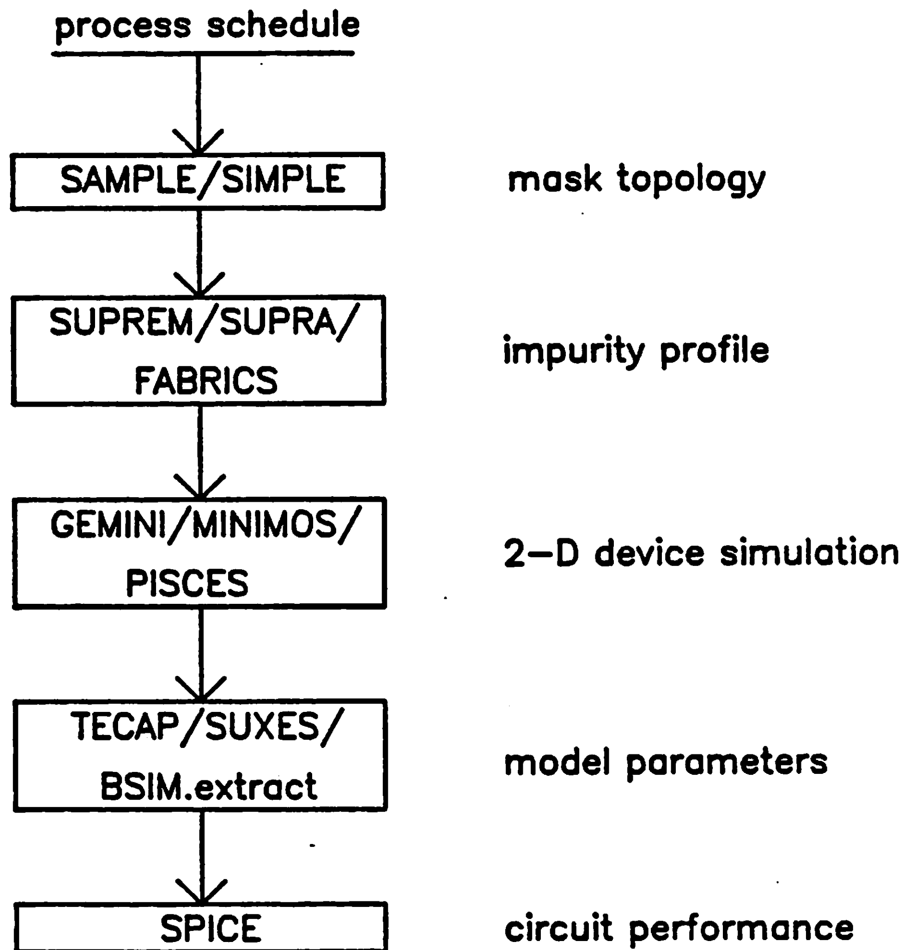


Fig. 1.1 A selection of some of the computer-aided tools available in the public domain.

hardware approach, such as multi-processor based simulation schemes [1.6,1.7], also drastically reduces the circuit-simulation time.

Device modeling plays a important role in VLSI circuit design because computer-aided circuit analysis results are only as accurate as the models used. It is therefore essential to develop device models which meet the preset accuracy and computational efficiency requirements. The SPICE2 program provides three MOS transistor models [1.8]. The LEVEL-1 model, which contains fairly simple expressions, is most suitable for preliminary analysis. The LEVEL-2 model, which contains expressions from detailed device physics, does not work well for small-geometry transistors. The LEVEL-3 model represents an attempt at pursuing the semi-empirical modeling approach, which only approximates device physics and relies on the proper choice of the empirical parameters to accurately reproduce device characteristics.

In this dissertation, the development of a simple and accurate short-channel MOS transistor model, the Berkeley Short-Channel IGFET Model (BSIM) [1.9], and its associated characterization facility for IC process-oriented circuit designs are described. The BSIM builds upon AT&T Bell Labs' CSIM with substantial enhancements [1.10]-[1.12]. The characterization facility includes a fully automated parameter-extraction program and implementation of the complete model, which includes expressions for dc and capacitance characteristics and extrinsic components, in SPICE2. Since the fully device-physics-oriented approach usually makes parameter extraction particularly difficult, the semi-empirical approach was adopted in developing BSIM to cope with the rapid advance of technology and to make automated parameter extraction possible. An analytical representation with 17 electrical parameters per device size was found to be adequate for modeling the dc characteristics. The parameter-extraction program generates a process file which contains a set of parameter values for circuit analysis. Circuit designers need only describe the layout geometries of transistors and parasitic ele-

ments to execute circuit simulation. Use of BSIM to analyze device characteristics from several NMOS and CMOS processes has resulted in good agreement between measured and modeled results with effective channel lengths down to 1 μm. Only minor enhancements are necessary to extend BSIM for submicron devices.

The BSIM is simulator-independent. Implementation of BSIM in SPICE2 and SPICE3 has been finished.

CHAPTER 2

BERKELEY SHORT-CHANNEL IGFET MODEL

LIST OF SYMBOLS

a	conductance degradation coefficient.
C_o	gate capacitance per unit area.
ΔL	channel-length reduction.
ΔW	channel-width change.
E_c	critical field for carrier velocity saturation.
g	coefficient of average body effect on drain current.
I_{DS}	drain current.
I_{DSAT}	drain current in the saturation region.
K_1	body-effect coefficient including short- and narrow- channel effects.
K_2	source and drain depletion charge sharing effect coefficient.
L_{eff}	effective channel length.
L_{MK}	masked-level channel length.
N_A	substrate doping concentration.
N_{ss}	surface state density.
n_i	intrinsic carrier concentration.
T_{ox}	gate-oxide thickness.
U_0	vertical field mobility degradation coefficient.
U_{0B}	sensitivity of U_0 to the substrate bias.
U_{0Z}	U_0 at zero substrate bias.
U_1	carrier velocity saturation coefficient.

U_{1B}	sensitivity of U_1 to the substrate bias.
U_{1D}	sensitivity of U_1 to the drain bias at V_{DS}=V_{DD}.
U_{1Z}	U_1 at zero substrate bias.
V_{BS}	substrate-to-source voltage.
V_{DS}	drain-to-source voltage.
V_{DSAT}	saturation drain voltage.
V_{FB}	flat-band voltage.
V_{GB}	gate-to-substrate voltage.
V_{GS}	gate-to-source voltage.
V_{th}	threshold voltage.
V_{t0}	threshold voltage for zero drain and substrate biases.
W_{eff}	effective channel width.
W_{MK}	masked-level channel width.
μ_0	intrinsic surface mobility.
μ_Z	μ_0 at zero substrate and drain biases.
μ_{ZB}	sensitivity of μ_0 to the substrate bias at $V_{DS} = 0$.
μ_S	μ_0 at zero substrate bias and $V_{DS} = V_{DD}$.
μ_{SB}	sensitivity of μ_0 to the substrate bias at $V_{DS} = V_{DD}$.
μ_{SD}	sensitivity of μ_0 to the drain bias at $V_{DS} = V_{DD}$.
ϕ_S	surface potential at strong inversion.
ϕ_{ms}	gate-to-semiconductor work function difference.
η	drain-induced barrier lowering coefficient.
η_Z	η at zero substrate bias and $V_{DS} = V_{DD}$.
η_B	sensitivity of η to the substrate bias.
η_D	sensitivity of η to the drain voltage.

2.1. MOS Transistor Modeling for Circuit Simulation - An Overview

Many articles on MOS transistor modeling have appeared in the literature [2.1]-[2.10] and efforts to model ever smaller and more complex MOS transistors continue at a rapid pace.

2.1.1. Long-Channel Devices

We begin by discussing the first-order model, used in the early P-channel MOS transistor analysis, where

$$I_{DS} = \beta_0 \left(V_{GS} - V_t - \frac{V_{DS}}{2} \right) V_{DS} \tag{2.1}$$

below saturation and

$$I_{DS} = \frac{\beta_0}{2} \left(V_{GS} - V_t \right)^2 \tag{2.2}$$

above saturation, and here the threshold voltage (V_t) is a constant. Saturation occurs when sufficient drain voltage (V_{PF}) is applied to deplete the channel at the drain, and $V_{PF} = V_{GS} - V_t$.

The first-order model neglects a fundamental effect, which is the consequence of finite resistivity of the substrate. This bulk-doping or body effect acts as a back gate. That is, after the channel (in an N-channel transistor) is established, an "n-p" junction is formed at the back side of the channel. The p value is, of course, the substrate doping.

As the current flows in the channel, the "I-R" drop in effect induces a reverse bias across this n-p junction. The depletion-region charge associated with this back gate must be accounted for according to Gauss' law. By using the gradual-channel approximation, a charge term can be derived that varies as the square root of potential. When the expression is integrated along the channel from the source to the drain, with potential as the running variable, it leads to the following improved first-order model [1]:

$$I_{DS} = \beta_0 \left[(V_{GS} - \phi_S - V_{FB}) V_{DS} - \frac{V_{DS}^2}{2} - \frac{2 \sqrt{2 q \epsilon_{si} N_A}}{3 C_o} \right.$$

$$\left. * \left[(V_{DS} + \phi_S - V_{BS})^{3/2} - (\phi_S - V_{BS})^{3/2} \right] \right] . \tag{2.3}$$

The 3/2 power terms result from the integration of the square-root dependent bulk-doping effect evaluated at the two integration limits. Furthermore, the threshold voltage, i.e., the gate bias at which the above expression starts to apply, is

$$V_t = V_{t0} + \frac{\sqrt{2 q \epsilon_{si} N_A}}{C_o} \left[\sqrt{\phi_S - V_{BS}} - \sqrt{\phi_S} \right] \tag{2.4}$$

where V_{t0} is the threshold voltage for zero substrate bias.

Similar to the first-order derivation, saturation occurs when the channel at the drain is depleted. Hence, the saturation voltage, V_{DSAT}, equals to the gate-to-source voltage minus the threshold voltage at the drain terminal. For values of V_{DS} greater than V_{DSAT}, I_{DS} is constant (saturated) at the value I_{DSAT}.

For many years this improved first-order theory was quite adequate for accurate integrated-circuit design. Problems began to appear as more and more two-dimensional effects become prominent in small-size transistors.

2.1.2. The Semi-Empirical Modeling Approach

Fully physics-oriented models completely derived from device physics are either mathematically too complicated or do not compare well with measured results. If all the governing physical effects are incorporated, expensive numerical solutions are required [2.11,2.12]. An MOS transistor model has to be evaluated thousands of times during circuit simulation. This renders direct applications of the computationally inefficient fully physics-oriented models impractical for circuit simulation. In addition, fully physics-oriented models evolve behind the integrated-circuit process.

Another plausible solution is the table look-up approach [2.13] which directly stores measured drain-current data for circuit simulation. While this approach may

sound attractive, it suffers from several fundamental problems. First, it is highly desirable to be able to evolve the proper device sizes while evolving the design. The direct table look-up approach assumes the number of device sizes to be employed in a design is known and small and the I-V characteristics are available. Second, interpolation between points assumes noise-free and glitch-free data, neither of which can be guaranteed. Third, no simple way to include effects of process variations in the simulation. In addition, enormous memory space has to be dedicated to the storage of the multi-dimensional arrays needed to model the characteristic dependence of various biasing conditions.

MOS transistor models widely used in circuit analysis are essentially semi-empirical in nature. Terms with strong physical meaning are employed to model the fundamental physical effects while parameters are judiciously introduced to embrace subtle device characteristics. This approach serves best for circuit-analysis purposes especially as two- and three-dimensional small-geometry effects become more important.

2.2. BSIM Formulation

The Berkeley Short-Channel IGFET Model (BSIM) [1.9], a simple and accurate short-channel MOS transistor model, has four important features. First, it is based on solid understanding of device physics. Second, the model formulation is very simple, which makes it suitable for the simulation of both digital and analog circuits. Third, the model can be easily enhanced to include new effects. Fourth, the model parameters for a family of devices can be obtained automatically by a dedicated parameter-extraction program which generates a process file. In a circuit simulator, the electrical parameters for each device can be calculated from size-independent parameters, which are contained in a process file, and the dimensions of the devices.

The formulation of BSIM is based on the device physics of small-geometry MOS transistors. Special effects included are:

- vertical field dependence of carrier mobility
- carrier velocity saturation
- drain-induced barrier lowering
- depletion charge sharing by the source and drain
- non-uniform doping for ion-implanted devices
- channel-length modulation
- subthreshold conduction
- geometric dependencies

The eight drain-current parameters which directly appear in the threshold-voltage and drain-current expressions are:

V_{FB}, the flat-band voltage,

ϕ_S, the surface-inversion potential,

K_1, the body-effect coefficient,

K_2, the source and drain depletion charge sharing coefficient,

η, the drain-induced barrier lowering coefficient,

U_0, the vertical field mobility degradation coefficient,

U_1, the velocity saturation coefficient, and

μ_0, the carrier mobility.

2.2.1. Strong-Inversion Component

(A) Threshold Voltage

The first five drain-current parameters, V_{FB}, ϕ_S, K_1, K_2, and η, model the threshold voltage:

$$V_{th} = V_{FB} + \phi_S + K_1 \sqrt{\phi_S - V_{BS}} - K_2(\phi_S - V_{BS}) - \eta V_{DS} \tag{2.5}$$

Parameter K_1 is equivalent to parameter γ in textbook models [2.14,2.15]. The K_1 and K_2 terms together model the non-uniform doping effect. In addition to the drain-induced barrier lowering effect, η also partially accounts for the channel-length modulation effect.

(B) Drain Current

Another three drain-current parameters, U_0, U_1 and μ_0, appear in the drain-current expression. In order to speed up circuit-simulation execution time, the 3/2 power dependence of the drain current on the substrate bias has been replaced by the numerical approximation proposed by Poon [1.10]-[1.12]. The drain-current expressions in various operation regions are summarized below.

(1) Cut-Off Region [$V_{GS} < V_{th}$]:

$$I_{DS} = 0. \tag{2.6}$$

(2) Triode Region [$V_{GS} \geqslant V_{th}$ and $0 < V_{DS} < V_{DSAT}$]:

$$I_{DS} = \frac{\mu_0}{[1 + U_0(V_{GS} - V_{th})]} \cdot \frac{C_o \frac{W}{L}}{(1 + \frac{U_1}{L} V_{DS})} \left[(V_{GS} - V_{th}) V_{DS} - \frac{a}{2} V_{DS}^2 \right]. \tag{2.7}$$

where

$$a = 1 + \frac{g K_1}{2 \sqrt{\phi_S - V_{BS}}}. \tag{2.8}$$

and

$$g = 1 - \frac{1}{1.744 + 0.8364 (\phi_S - V_{BS})}. \tag{2.9}$$

(3) Saturation Region [$V_{GS} \geqslant V_{th}$ and $V_{DS} \geqslant V_{DSAT}$]:

$$I_{DS} = \frac{\mu_0}{[\,1 + U_0 (V_{GS} - V_{th})\,]} \cdot \frac{C_o \frac{W}{L} (V_{GS} - V_{th})^2}{2\,a\,K} , \tag{2.10}$$

where

$$K = \frac{1 + v_c + \sqrt{1 + 2\,v_c}}{2} , \quad V_{DSAT} = \frac{V_{GS} - V_{th}}{a \sqrt{K}} , \tag{2.11}$$

and

$$v_c = \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{a} . \tag{2.12}$$

The body-effect coefficient "a" makes BSIM a close numerical approximation of the standard textbook model over a reasonable range of V_{DB} and V_{DS}. Detailed derivation of the expression for "a" can be found in Section 2.3.3.

2.2.2. Including the Weak-Inversion Component

When the gate voltage is below the threshold voltage, the semiconductor surface is in weak inversion and the corresponding drain current is called the subthreshold current. It is particularly important to include the subthreshold conduction model in the analysis and designs of low-voltage, low-power circuits.

The diffusion-dominated drain current diminishes exponentially with decreasing gate voltage when the transistor is biased in the weak-inversion region. Previous SPICE2 MOS transistor models include subthreshold conduction by matching the strong-inversion component with the weak-inversion component at a transition point close to the threshold voltage [1.8]. Discontinuity of drain-current derivatives exists, as has been pointed out by Antognetti [2.16], which jeopardizes the convergence of the simulation. Proper matching of the strong-inversion component and the weak-inversion component is not a trivial task because it has to be done on a multi-dimensional basis with respect to the gate, drain, and substrate biases. In BSIM, a simple and accurate approach is employed [2.16]. The total drain current is modeled as the linear sum of a strong-inversion component and a weak-inversion component, given by

$$I_{DS_{total}} = I_{DS_{si}} + I_{DS_{wi}} . \tag{2.13}$$

$I_{DS_{si}}$ is the strong-inversion component as described before. The weak-inversion component $I_{DS_{wi}}$ can be expressed as

$$I_{DS_{wi}} = \frac{I_{exp} \cdot I_{limit}}{I_{exp} + I_{limit}} , \tag{2.14}$$

where

$$I_{exp} = \mu_0 C_o \frac{W}{L} (\frac{kT}{q})^2 e^{1.8} e^{\frac{V_{GS}-V_{th}}{n} (\frac{q}{kT})} [1- e^{-V_{DS} (\frac{q}{kT})}] , \tag{2.15}$$

and

$$I_{limit} = \frac{\mu_0 C_o}{2} \cdot \frac{W}{L} \cdot (3 \frac{kT}{q})^2 . \tag{2.16}$$

The factor $e^{1.8}$ is chosen to achieve best fits in the subthreshold characteristics with minimum effect on the strong-inversion characteristics [2.17]. Three subthreshold parameters, n_0, n_B, and n_D, are used to model the subthreshold-slope coefficient,

$$n = n_0 + n_B V_{BS} + n_D V_{DS} . \tag{2.17}$$

This approach does not introduce any discontinuity in the drain current and first derivatives, and thus does not hamper convergence in circuit simulation.

2.2.3. Parameter Pre-Processing

(A) Conversion from Size-Independent Parameters to Electrical Parameters

Figure 2.1 shows the data flow in the process-oriented circuit simulation. In a process file, for each device type, there are 54 size-independent parameters used to find the 17 size-dependent electrical parameters. At the data structure set-up stage, the simulation program stores 17 electrical parameters for each transistor according to the formula:

$$P = P_0 + \frac{P_L}{L_{MK} - \Delta L} + \frac{P_W}{W_{MK} - \Delta W} . \tag{2.18}$$

This data-processing step only needs to be done once. L_{MK} and W_{MK} are masked-level

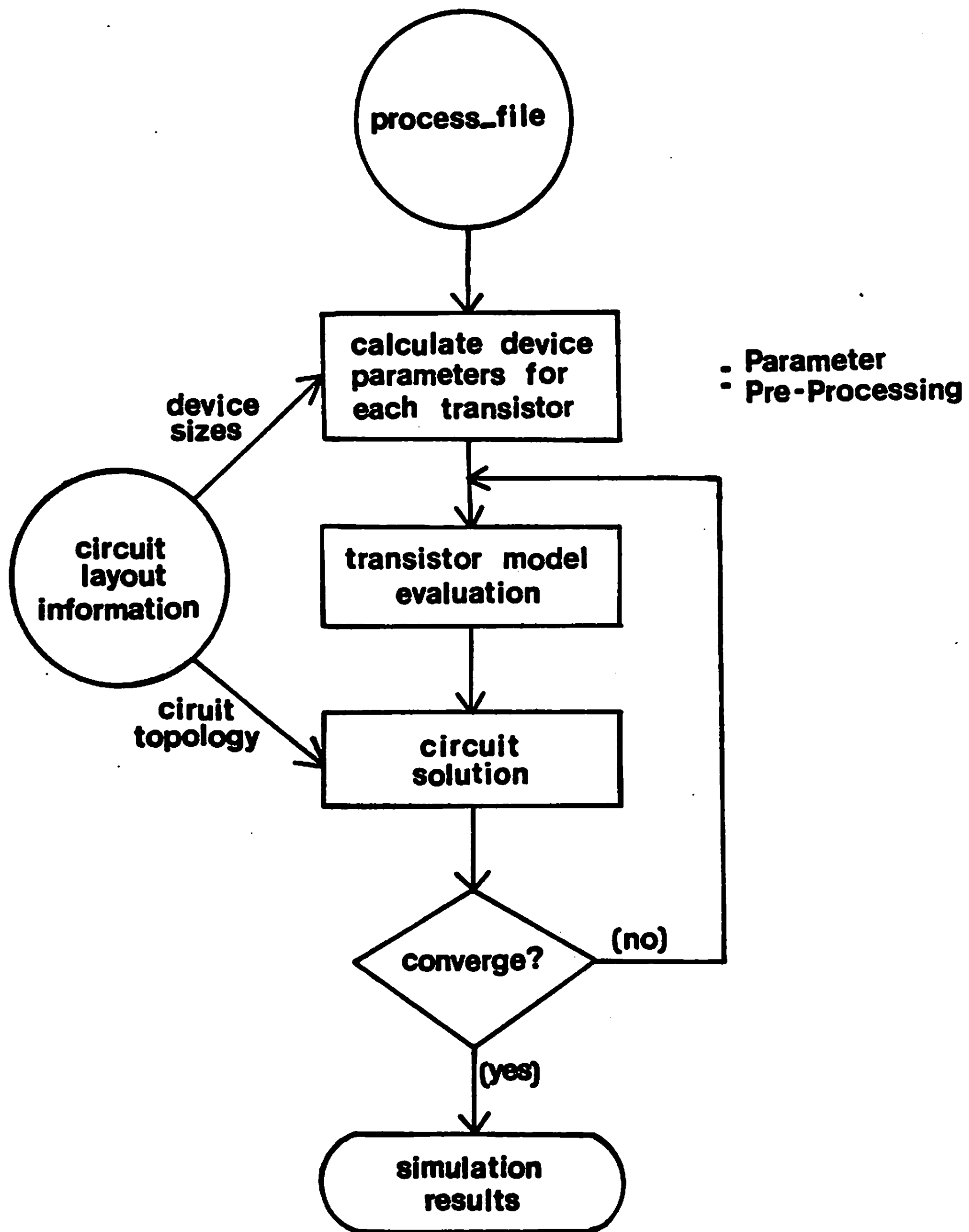


Fig. 2.1 Data flow in the process-oriented circuit simulation.

channel length and width, while ΔL and ΔW are net size changes due to various fabrication steps. The three components, P_0, P_L and P_W, of each electrical parameter P represent respectively its offset value, channel-length sensitivity, and channel-width sensitivity. For the subthreshold conduction, there are nine additional size-independent parameters in the process file from which three subthreshold parameters per transistor can be obtained. Subthreshold parameters are also processed using Eq. (2.18).

(B) Reduction from Bias-Independent Parameters to Drain-Current Parameters

At the model-evaluation stage, for each transistor the 17 electrical parameters are mapped to 8 drain-current parameters. V_{FB}, ϕ_S, K_1, K_2 are kept intact. The rules to map U_0, U_1, η, and μ_0 are listed below:

$$U_0 = U_{0Z} + U_{0B} V_{BS} . \tag{2.19}$$

$$U_1 = U_{1Z} + U_{1B} V_{BS} + U_{1D} (V_{DS} - V_{DD}) . \tag{2.20}$$

$$\eta = \eta_Z + \eta_B V_{BS} + \eta_D (V_{DS} - V_{DD}) . \tag{2.21}$$

Parameter μ_0 is obtained by quadratic interpolation through three data points, μ_0 at $V_{DS} = 0$, μ_0 at $V_{DS} = V_{DD}$, and the sensitivity of μ_0 to V_{DS} at $V_{DS} = V_{DD}$, with

$$\mu_0 |_{(\text{at } V_{DS} = 0)} = \mu_Z + \mu_{ZB} V_{BS} , \tag{2.22}$$

and

$$\mu_0 |_{(\text{at } V_{DS} = V_{DD})} = \mu_S + \mu_{SB} V_{BS} . \tag{2.23}$$

A second-order polynomial function is used.

2.3. Model Derivation

The BSIM builds upon AT&T Bell Labs' CSIM [1.11,1.12]. An idealized N-channel MOS transistor is illustrated in Fig. 2.2. The relationship between the electric field (E_{ox}) in the oxide, the gate voltage with respect to the substrate potential (V_{GB}), and the electrostatic potential at the oxide-semiconductor interface (V_{sur}) can be understood by considering the energy band diagram in Fig. 2.3. Summing up the voltages on both

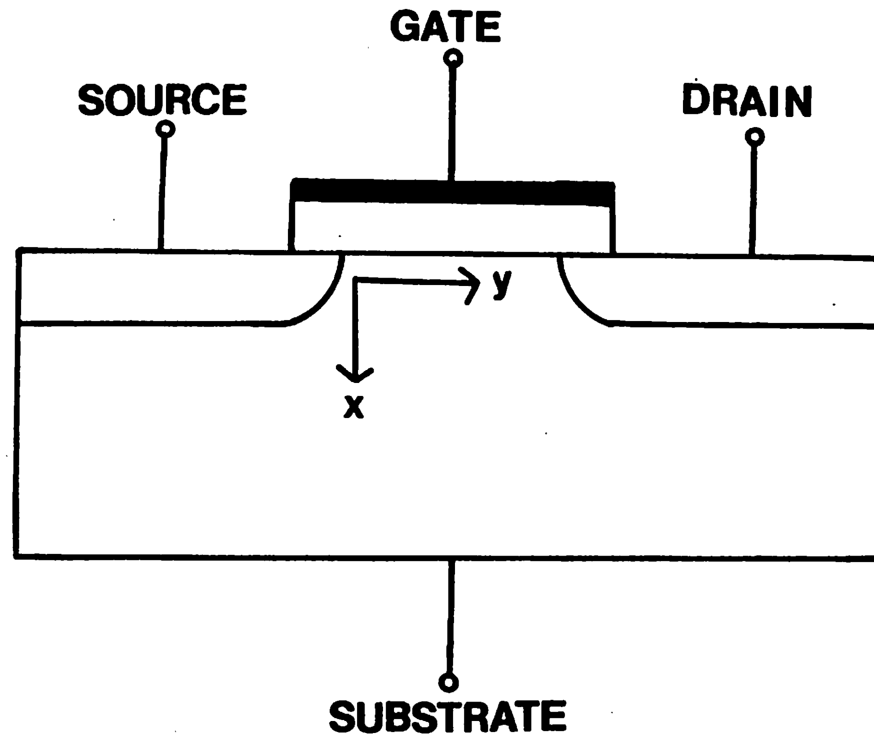


Fig. 2.2 An idealized N-Channel MOS transistor.

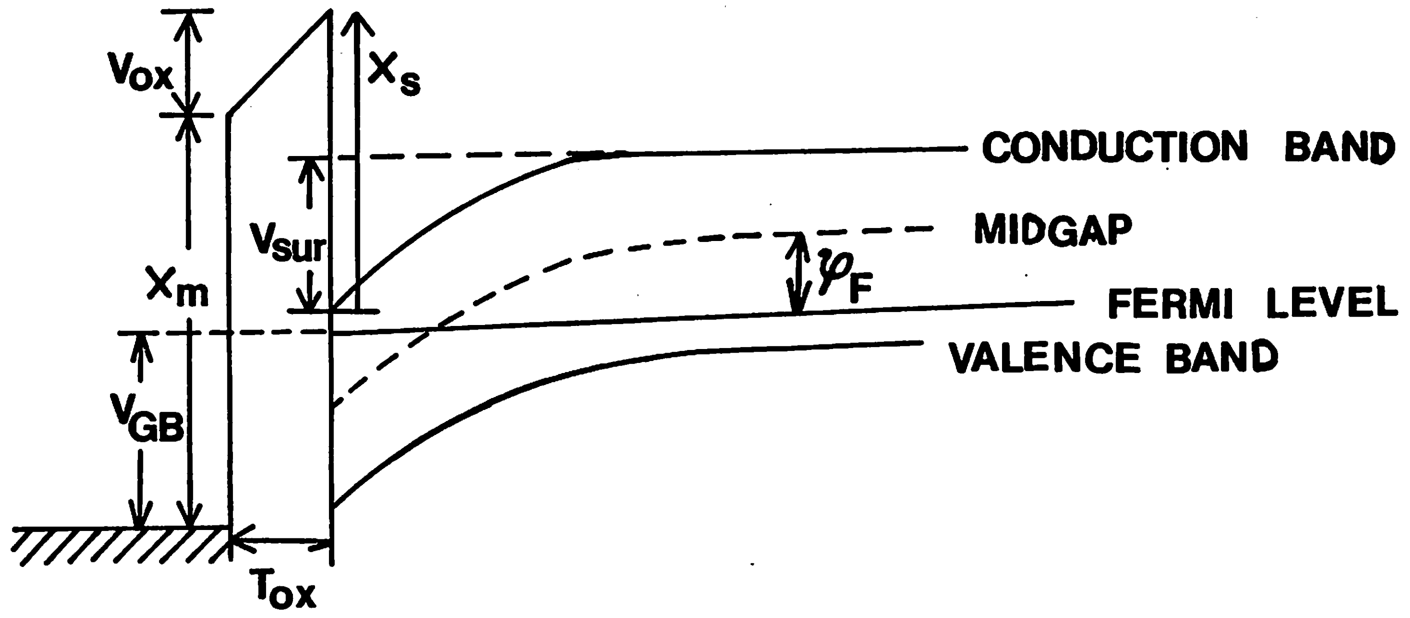


Fig. 2.3 An energy band diagram.

the gate and the semiconductor side gives

$$V_{ox} + X_m = V_{GB} + \phi_f + \frac{E_g}{2} - V_{sur} + X_s \, , \tag{2.24}$$

where X_m and X_s are, respectively, the gate and semiconductor work functions. V_{ox} is the voltage across the oxide, and E_g is the bandgap energy. The gate-to-semiconductor work function difference (ϕ_{ms}) is defined as

$$\phi_{ms} = X_m - X_s - \phi_f - \frac{E_g}{2} \, . \tag{2.25}$$

Combining Equations (2.24) and (2.25), we obtain

$$V_{ox} = T_{ox} \, E_{ox} = V_{GB} - V_{sur} - \phi_{ms} \, , \tag{2.26}$$

where T_{ox} is the gate oxide thickness. To determine the relationship between E_{ox} and the charge in the semiconductor, let us assume:

(1) The gate-oxide thickness is much smaller than the channel length. This assumption implies that E_{ox} is perpendicular to the gate plane.

(2) The horizontal component E_y of the electric field in the semiconductor at the oxide-semiconductor interface is much smaller than the vertical component E_s. This assumption is reasonable in the region where the channel charge Q_c is substantial, but it is incorrect in the velocity-saturation region where Q_c is small. Our main interest is to compute the drain current which is proportional to the integral of Q_c along the channel. In the velocity-saturation region, where the above assumption is invalid, the contribution to the integral is small. Hence, this assumption is reasonable for drain current computation.

By Gauss' law and Assumptions 1 and 2, one obtains

$$\epsilon_s \, E_s = \epsilon_{ox} \, E_{ox} + Q_{ss} \, , \tag{2.27}$$

where ϵ_{ox} and ϵ_s are the dielectric constants of the oxide and the semiconductor, and Q_{ss} is the surface charge. The vertical electric field E_s consists of three components,

$$\epsilon_s \, E_s = Q_c + Q_b + \epsilon_s \, E_1 \, . \tag{2.28}$$

where Q_b is the depletion charge in the semiconductor and, using the abrupt junction approximation, is given by

$$Q_b = \sqrt{2\, q\, \epsilon_s N_A V_{sur}}\ . \tag{2.29}$$

For short-channel devices, this expression is modified due to the influence of the source and drain junction fields. The vertical electric field E_s in Eq. (2.28) contains a third component E_1 which originates from the drain and will be discussed in detail later.

A qualitative expression for the bulk charge can be derived by considering an MOS structure where alternatively the source and drain, and the gate are ignored (Fig. 2.4(a) and (b)). These diagrams illustrate the influence of source and drain junction fields on the bulk charge. According to Gauss' law (Fig. 2.4(a)), the electric field E_{ox} at the oxide-semiconductor interface will be balanced by the surface charge Q_{ss}, the channel charge Q_c, and the negative charge Q_b in the depletion region (A) of the substrate. In the absence of the gate (Fig. 2.4(b)), the electric field E_j at the junction will be balanced by the charge in the depletion layer (B) near the junction. Now consider the complete structure where the drain, source, and substrate are at the same potential and a positive voltage is applied to the gate as shown in Fig. 2.4(c). The depletion charge shown in area (C) have to balance both the electric field E_{ox} coming in from the oxide-semiconductor interface and E_j due to the source or drain to the substrate junction. Let a fraction, t, of the charge (C) be used to balance E_j. Since this fraction of the charge will not be available to balance E_{ox}, one could say that the doping of the substrate is effectively lowered. This fraction t will depend on the position along the channel. As an approximation, t should be proportional to the ratio of the charge in area (C) to the total depletion charge of $2X_j/L$. Since X_j is proportional to $1/\sqrt{N_A}$, t must be proportional to $1/(L\sqrt{N_A})$. Therefore, the effective fraction of the charge $f(L,N_A)$ available to balance E_{ox} can be expressed by

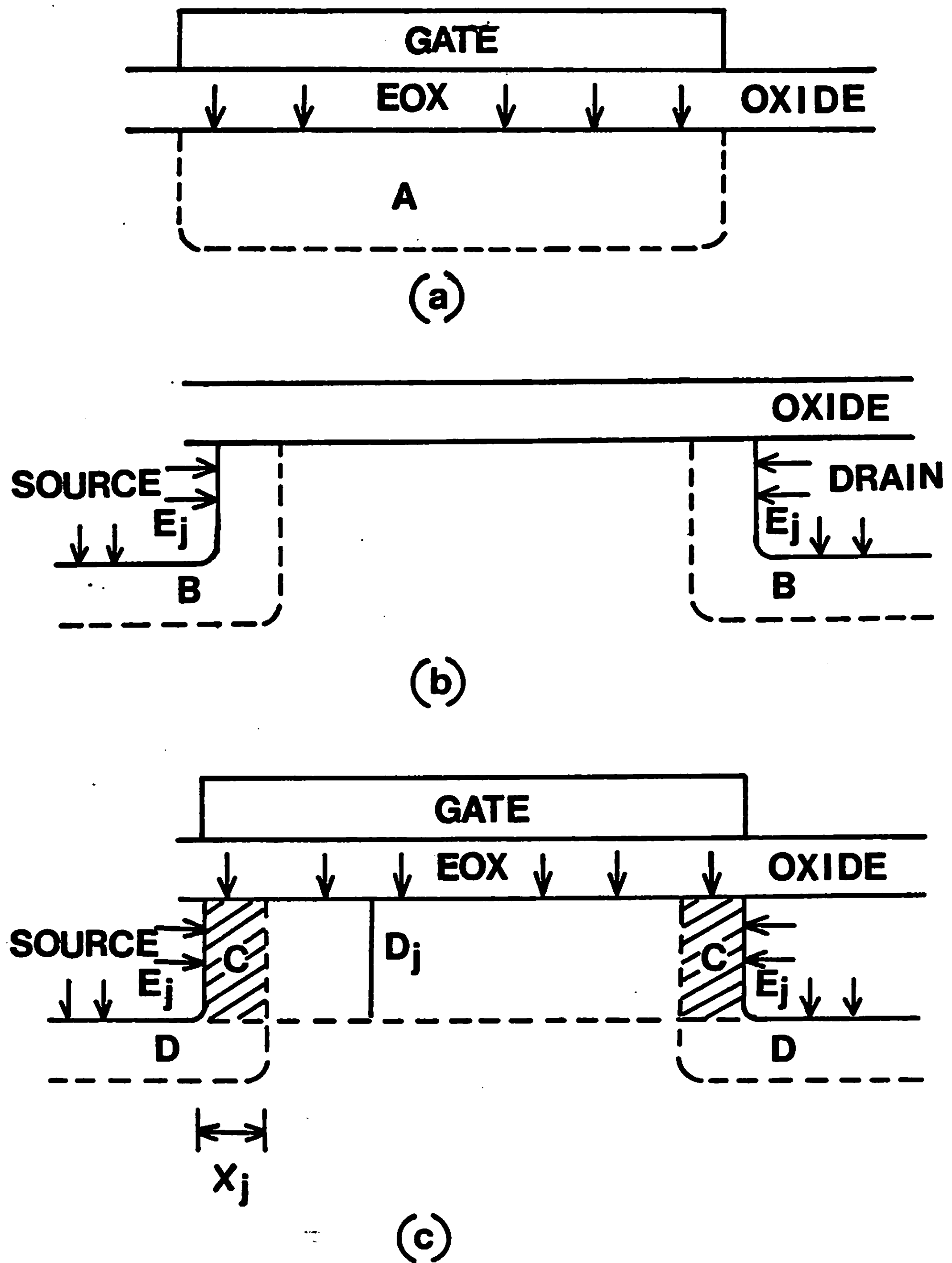


Fig. 2.4 Diagrams illustrating the effect of drain and source junction fields.
(a) The drain and source being ignored.
(b) The gate being ignored.
(c) The complete structure with the drain, source, and substrate at the same potential.

$$f(L,N_A) = 1 - \frac{K_{vt}}{L\sqrt{N_A}}, \tag{2.30}$$

where K_{vt} is a constant. A more elaborate function for $f(L,N_A)$ and a more rigorous derivation can be found in [2.18] and [2.19] which show that $f(L,N_A)$ is also a function of V_{BS}. However, we found that the additional V_{BS} dependence tends to complicate the formulation and does not add much accuracy to the model. With the modified charge, Eq. (2.28) becomes

$$\epsilon_s E_s = Q_c + f(L,N)\ \sqrt{2\,q\,\epsilon_s N_A V_{sur}}. \tag{2.31}$$

To derive the third component E_l of the electric field E_s, let us consider the case where V_{DS} is zero but V_{GB} and V_{BS} are non-zero. The substrate is depleted according to the solution of the Poisson equation. When V_{DS} is non-zero, an additional potential will be imposed in the region already depleted. Since no additional charge appears in the Poisson-equation solution for zero drain bias, this additional potential will satisfy the Laplace equation. This Laplace equation can be solved under certain simplifying assumptions and the solution gives the additional electric fields as shown in Fig. 2.5. These electric fields terminate at the channel and induce additional channel charge which enhances the drain current and results in a finite output conductance in the saturation region.

The following approximations are made to derive a simple expression for E_l.

(1) The source and drain junction depths are small compared to the channel length.

(2) Approximate boundary conditions for the Laplace equation, with solution denoted by V_l, are $V_l = 0$ at the oxide-semiconductor interface and $V_l = V_{DS}$ at the drain region. This approximation is illustrated in Fig. 2.6.

By substitution, it can be shown that

$$V_l = V_{DS}\,\frac{\Theta}{\pi} \tag{2.32}$$

satisfies the Laplace equation in cylindrical coordinates.

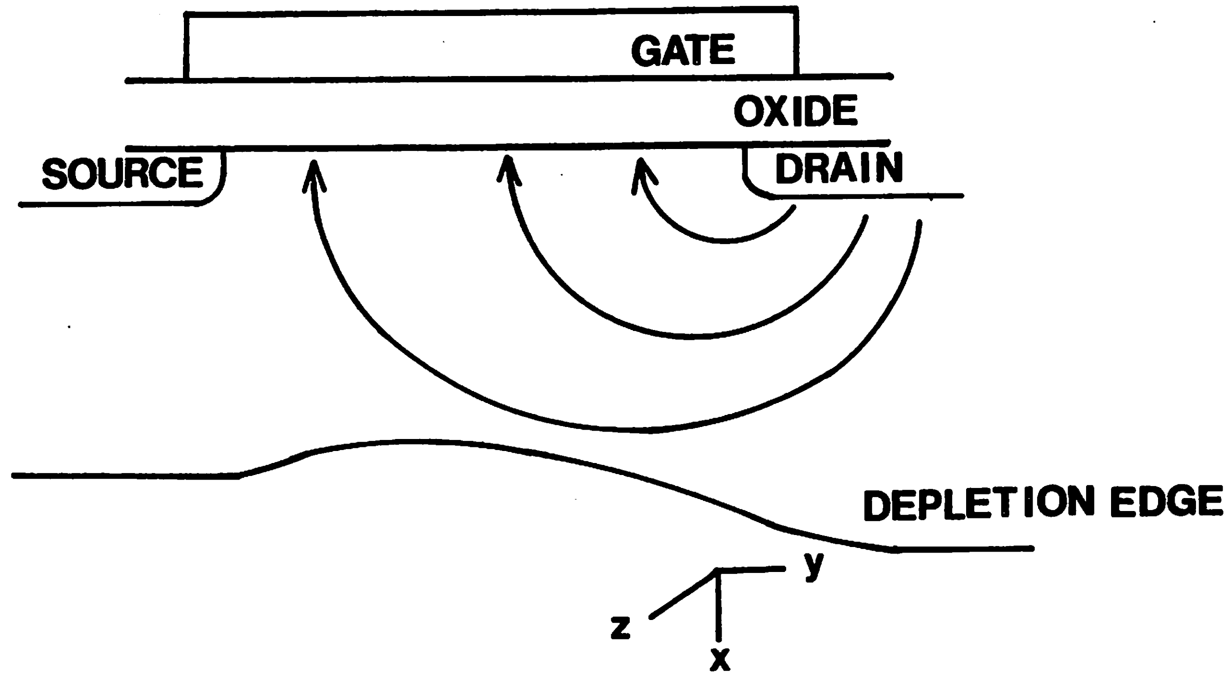


Fig. 2.5 A diagram illustrating the drain modulation effect.

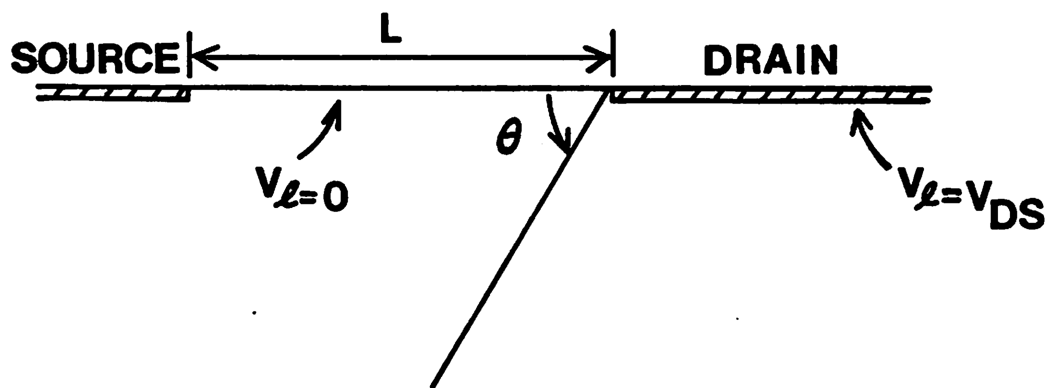


Fig. 2.6 A diagram illustrating the simplified boundary condition for the Laplace equation.

$$\left[\frac{d^2 V_1}{d r^2}\right] + \left[\frac{1}{r}\right]\left[\frac{d V_1}{d r}\right] + \left[\frac{1}{r^2}\right]\left[\frac{d^2 V_1}{d \Theta^2}\right] = 0 , \tag{2.33}$$

and the boundary conditions. Differentiating V_1 with respect to y at the source, one obtains

$$E_1 = -\frac{V_{DS}}{\pi L} . \tag{2.34}$$

With the addition of E_1, Eq. (2.31) becomes

$$\epsilon_s E_s = Q_c + f(L,N) \sqrt{2 q N_A V_{sur}} + \epsilon_s E_1 . \tag{2.35}$$

Combining Eqs. (2.26), (2.27), and (2.35), one can express Q_c in terms of V_{GB} and V_{sur} as

$$Q_c = C_o \left[V_{GB} - V_{sur} - V_{FB} - K_1 \sqrt{V_{sur}}\right] - \epsilon_s E_1 , \tag{2.36}$$

where

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_o} , \tag{2.37}$$

and

$$K_1 = f(L,N) \cdot \frac{\sqrt{2 q \epsilon_{si} N_A}}{C_o} . \tag{2.38}$$

When the surface is inverted, the surface potential V_{sur} is approximately given by

$$V_{sur} = \phi_n + \phi_S - V_{BS} , \tag{2.39}$$

where ϕ_n is the electron quasi-Fermi level. Then Eq. (2.36) becomes

$$Q_c = C_o \left[(V_{GS} - \phi_n - \phi_S - V_{FB}) - K_1 \sqrt{\phi_n - V_{BS} + \phi_S}\right] - \epsilon_s E_1 , \tag{2.40}$$

where

$$V_{GS} = V_{GB} + V_{BS} . \tag{2.41}$$

To derive an expression for the drain current, the current flow is assumed to be parallel to the y-axis such that

$$\frac{d \phi_n}{d x} = 0 , \tag{2.42}$$

and

$$J = q\,\mu_0\, n \left(\frac{d\,\phi_n}{d\,y} \right). \tag{2.43}$$

where μ_0 is the electron mobility and n is the electron density. When Eq. (2.43) is integrated with respect to x and z, one obtains

$$I_{DS} = \mu_0\, W\, Q_c \left(\frac{d\,\phi_n}{d\,y} \right). \tag{2.44}$$

Integrating Eq. (2.44) with respect to y and ϕ_n,

$$I_{DS} \int_0^L dy = \mu_0\, W \int_0^{V_{DS}} Q_c\, d\phi_n\,. \tag{2.45}$$

Note that if channel shortening due to the finite extent of the drain depletion region is included, the upper limit is accordingly reduced.

By combining Eqs. (2.40) and (2.45), the drain current is given by

$$I_{DS} = \beta \int_0^{V_{DS}} [(V_{GS} - \phi_n - \phi_S - V_{FB}) - K_1 \sqrt{\phi_n + \phi_S - V_{BS}} + \eta\, V_{DS}]\, d\phi_n\,. \tag{2.46}$$

where β is the conductance coefficient and η is the drain-induced barrier lowering coefficient.

When Eq. (2.46) is integrated with respect to ϕ_n in the triode region, one obtains

$$I_{DS} = \beta \left((V_{GS} - \phi_S - V_{FB})\, V_{DS} + (\eta - \frac{1}{2})\, V_{DS}^2 - \frac{2}{3} K_1 [(V_{DS} + \phi_S - V_{BS})^{3/2} - (\phi_S - V_{BS})^{3/2}] \right) \tag{2.47}$$

Note that Eq. (2.47) is exactly the Ihantola-Moll model [2.1] if $\eta = 0$ and $K_1 = \sqrt{2q\epsilon_{si} N_A}/C_o$, i.e., $f(L,N_A) = 1$.

2.3.1. Expansion of the Bulk-Doping Term

The function

$$F(V_{DS}\,, \phi_S - V_{BS}) = \frac{2}{3} \left[(V_{DS} + \phi_S - V_{BS})^{3/2} - (\phi_S - V_{BS})^{3/2} \right] \tag{2.48}$$

can be approximated numerically in the range $0\,V < V_{DS} < 10\,V$ and

$0.7\ V < \phi_S - V_{BS} < 20.7\ V$ by

$$F(V_{DS}, \phi_S - V_{BS}) = \sqrt{\phi_S - V_{BS}}\, V_{DS} + \frac{0.25\, g \cdot V_{DS}^2}{\sqrt{\phi_S - V_{BS}}} . \tag{2.49}$$

where

$$g = 1 - \frac{1}{1.744 + 0.8364\,(\phi_S - V_{BS})} \tag{2.50}$$

The details of this approximation are discussed in Section 2.3.3. The drain current in the triode region can be expressed as

$$I_{DS} = \beta\,[\,(V_{GS} - V_{th})\,V_{DS} - \frac{a}{2} V_{DS}^2\,] \tag{2.51}$$

where

$$V_{th} = V_{FB} + \phi_S + K_1 \sqrt{\phi_S - V_{BS}} - K_2\,(\phi_S - V_{BS}) - \eta\, V_{DS} , \tag{2.52}$$

and

$$a = 1 + \frac{g\, K_1}{2\sqrt{\phi_S - V_{BS}}} . \tag{2.53}$$

The factor "a" given by Eq. (2.53) represents the bulk-doping effect. The origin of the K_2 term has already been explained.

2.3.2. Channel-Charge Modeling

After inserting Eqs. (2.52) and (2.53) into Eq. (2.40), the channel-charge expression has the simplified form

$$Q_c = -C_o\,(V_{GS} - V_{th} - a\,\phi_n) . \tag{2.54}$$

If the continuos velocity-saturation characteristic (see Fig. 2.7) [2.20],

$$v = \frac{\mu_0 E_y}{\left|1 + \frac{E_y}{E_c}\right|} , \quad \text{with } v \longrightarrow v_{sat} \equiv \mu_0 E_c \text{ when } E_y \longrightarrow \text{infinte} , \tag{2.55}$$

is used in the integration of Q_c, one finds the drain-current expression in the triode region to be

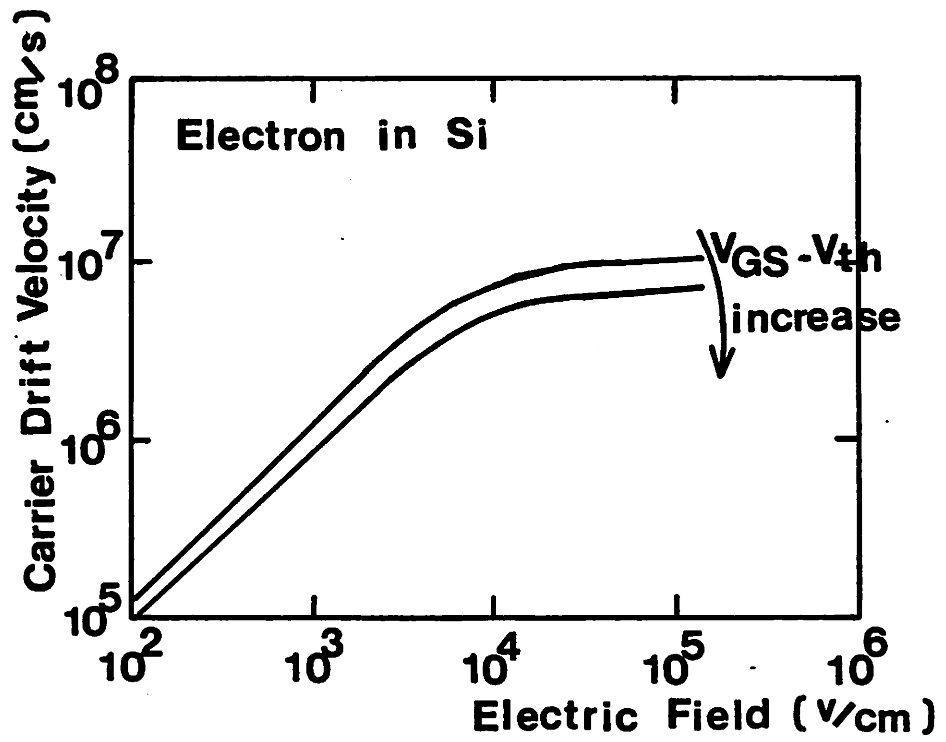


Fig. 2.7 Carrier velocity versus electric field [2.20].

$$I_{DS} = \beta \left[(V_{GS} - V_{th} - I_{DS} R_{sat}) V_{DS} - \frac{a}{2} V_{DS}^2 \right] . \quad (2.56)$$

where

$$R_{sat} = \frac{1}{W v_{sat} C_o} . \quad (2.57)$$

Eq. (2.56) can be rearranged as

$$I_{DS} = \frac{\beta}{(1 + \frac{U_1}{L} V_{DS})} \left[(V_{GS} - V_{th}) V_{DS} - \frac{a}{2} V_{DS}^2 \right] . \quad (2.58)$$

where

$$\frac{U_1}{L} = \beta R_{sat} . \quad (2.59)$$

The conventional definition of saturation voltage, V_{DSAT}, is obtained as from Eq. (2.54) with $Q_c = 0$. This condition is not realistic for modern short-channel devices. A more realistic assumption is that at the point in the channel where ϕ_n goes to V_{DSAT} the channel current is limited by velocity saturation, i.e.,

$$Q_c = - \frac{I_{DSAT}}{W v_{sat}} = - C_o (V_{GS} - V_{th} - a V_{DSAT}) . \quad (2.60)$$

Substitution of the above expression into Eq. (2.54) yields an upper limit for the integral in Eq. (2.46) as

$$\phi_n \longrightarrow V_{DSAT} = \frac{1}{a} [(V_{GS} - V_{th}) - I_{DSAT} R_{sat}] \quad (2.61)$$

By carrying out the integration in Eq. (2.46) with the new upper limit, the following expression for the drain current in the saturation region can be obtained,

$$I_{DSAT} = \beta [(V_{GS} - V_{th} - I_{DSAT} R_{sat}) V_{DSAT} - \frac{a V_{DSAT}^2}{2}] . \quad (2.62)$$

Eq. (2.62) can be rearranged as

$$I_{DSAT} = \frac{\beta}{2 a} (V_{GS} - V_{th} - I_{DSAT} R_{sat})^2 , \quad (2.63)$$

which is a quadratic equation for I_{DSAT}. To facilitate comparison with the usual expression, we define

$$I_{DSAT} = \frac{\beta (V_{GS} - V_{th})^2}{2 a K} . \tag{2.64}$$

where K is obtained by equating Eqs. (2.63) and (2.64), i.e.,

$$K^2 - K [1 + \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{a}] + \left| \frac{U_1}{L} \right|^2 \cdot \frac{(V_{GS} - V_{th})^2}{(2 a)^2} = 0 , \tag{2.65}$$

or

$$K = \frac{1 + v_c + \sqrt{1 + 2 v_c}}{2} . \tag{2.66}$$

where

$$v_c = \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{a} . \tag{2.67}$$

If $v_c \ll 1$, then

$$K \longrightarrow 1 + \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{a} . \tag{2.68}$$

If $v_c \gg 1$, then

$$K \longrightarrow \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{2 a} . \tag{2.69}$$

and

$$I_{DSAT} \longrightarrow C_o v_{sat} W (V_{GS} - V_{th}) . \tag{2.70}$$

The above expression is well-known, and states that in the limit of carrier velocity being fully saturated at v_{sat}, the saturation current is linear instead of squared with respect to ($V_{GS} - V_{th}$), and that its value is independent of the channel length.

One can obtain the saturation drain voltage from Eqs. (2.61) and (2.64),

$$V_{DSAT} = \frac{(V_{GS} - V_{th})}{a \sqrt{K}} . \tag{2.71}$$

In the case of $\frac{U_1}{L} \cdot (V_{GS} - V_{th}) \ll 1$,

$$V_{DSAT} \longrightarrow \frac{V_{GS} - V_{th}}{a} . \tag{2.72}$$

In the case of $\frac{U_1}{L} \cdot (V_{GS} - V_{th}) \gg 1$,

$$V_{DSAT} \longrightarrow \left[\frac{2\,(V_{GS} - V_{th})}{a} \cdot \frac{L}{U_1} \right]^{1/2} . \tag{2.73}$$

2.3.3. Numerical Approximation of the Substrate-Bias Effect

The aim here is to find an accurate approximation of $F(V_{DS}, \phi_S - V_{BS})$ over a reasonable voltage range of V_{DS} and $(\phi_S - V_{BS})$ [1.10]-[1.12]. For convenience, let $V_A = \phi_S - V_{BS}$. The function

$$F(V_{DS}, V_A) = \frac{2}{3} \left[(V_{DS} + V_A)^{3/2} - (V_A)^{3/2} \right] \tag{2.74}$$

can be expanded as

$$F(V_{DS}, V_A) = \sqrt{V_A}\, V_{DS} + \frac{0.25\, V_{DS}^2}{\sqrt{V_A}} + \dots \tag{2.75}$$

The above expansion is invalid when V_A is much greater than V_{DS}. To alleviate this problem, the expansion is changed to

$$F(V_{DS}, V_A) = \sqrt{V_A}\, V_{DS} + \frac{0.25\, g\, V_{DS}^2}{\sqrt{V_A}} \tag{2.76}$$

where $g(V_A)$ is determined by requiring the expansion in Eq. (2.76) to give the best fit to $F(V_{DS}, V_A)$ in the desired voltage range.

The value of V_A are considered in the range 0.7 V to 20.7 V at 2-V increments. For each fixed V_A, a parameter g is determined such that the expansion

$$\sqrt{V_A}\, V_{DS} + \frac{0.25\, g\, V_{DS}^2}{\sqrt{V_A}}$$

will give the best fit to $F(V_{DS}, V_A)$ in a least-square sense, over a range of V_{DS} from 0 to 10 V at 0.5-V increments. It is found that g can be accurately expressed as a function of V_A in the following form.

$$\frac{1}{1-g} = P_1 + P_2 \cdot V_A \tag{2.77}$$

where P_1 and P_2 are determined by a least-square fitting over the range of V_A from 0.7 to 20.7 volts. The results are

$$P_1 = 1.744 \tag{2.78}$$

and

$$P_2 = 0.8364 \tag{2.79}$$

The root-mean-square error of the approximation in Eq. (2.76) using the above value of P_1 and P_2 is 2% and is illustrated by Fig. 2.8.

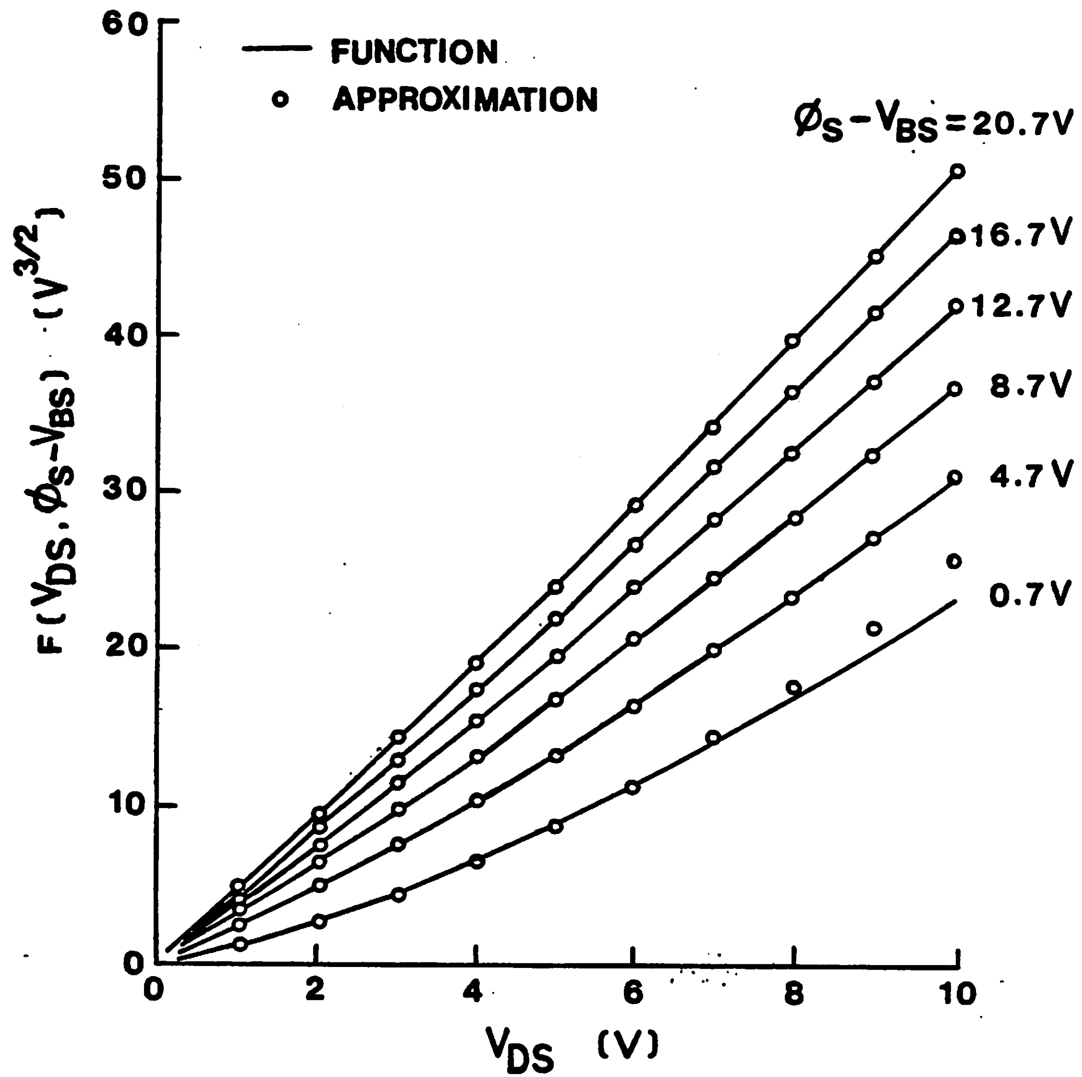


Fig. 2.8 Approximating the function $F(V_{DS}, \phi_S - V_{BS})$.

CHAPTER 3

PARAMETER EXTRACTION

A fully integrated computer-aided-design approach is essential for efficient design of complex VLSI circuits. Historically, the interface between process characterization and circuit simulation has been one of the weakest links. To the end, an integrated system for automated extraction of BSIM parameters has been developed that serves efficiently as this interface. With test devices available on wafers, the extraction program extracts parameter values and forms a process file for circuit analysis. Figure 3.1 shows the role of such an integrated system in the advanced integrated-circuit design.

3.1. Automated Parameter-Extraction System Hardware

A schematic diagram of the parameter-extraction system hardware is shown in Fig. 3.2 [3.1]. The system consists of three major elements: an H-P 9836 desktop computer, an H-P 4145A semiconductor parameter analyzer, and an Electro-glass 2001X fully-automated probe station. The H-P 9836 computer acts as the system controller through an IEEE-488 interface bus. Data transfer between the H-P 9836 and a host computer is via a RS-232 bus. The system also includes an option of using a manual probe station. This alternative is particularly useful in developing new software features. An H-P ThinkJet graphics printer supplies hard copies of measured and extracted results.

3.2. Parameter-Extraction Program

Global optimization techniques have been widely used in conventional MOS transistor parameter-extraction programs [3.2]-[3.5]. In general, the quantity to be

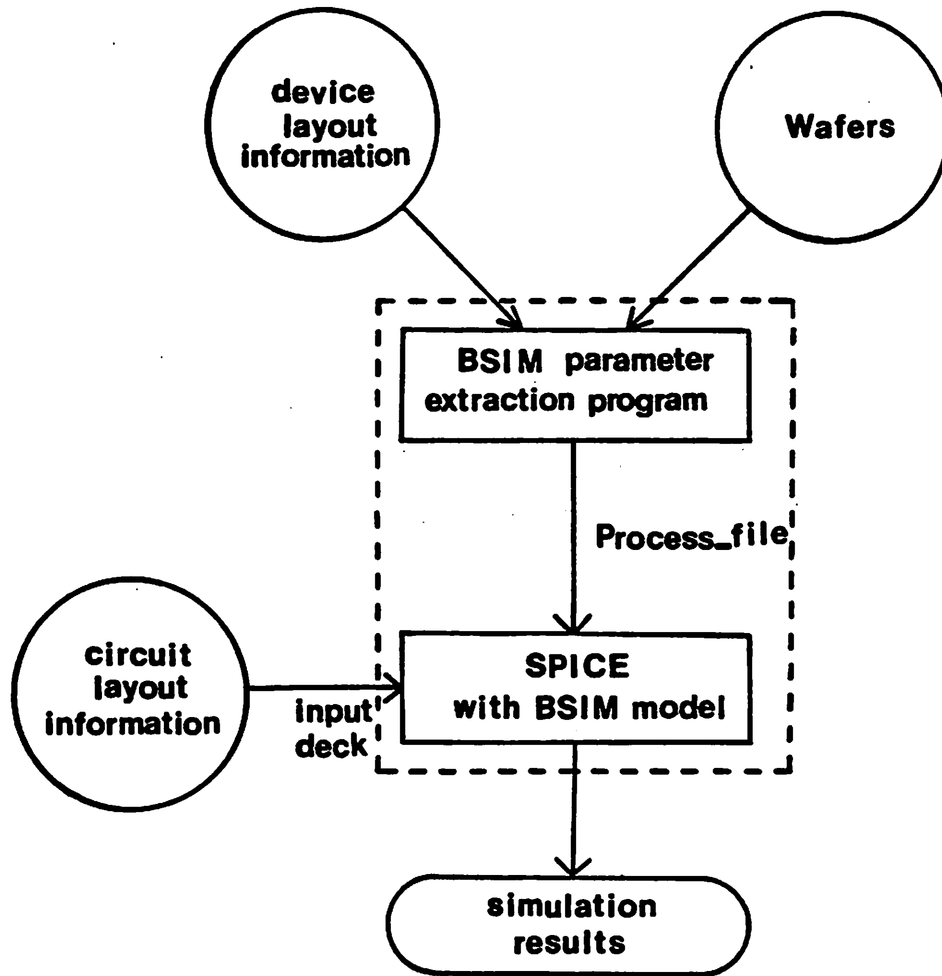


Fig. 3.1 A fully integrated approach for computer-aided parameter extraction and circuit design.

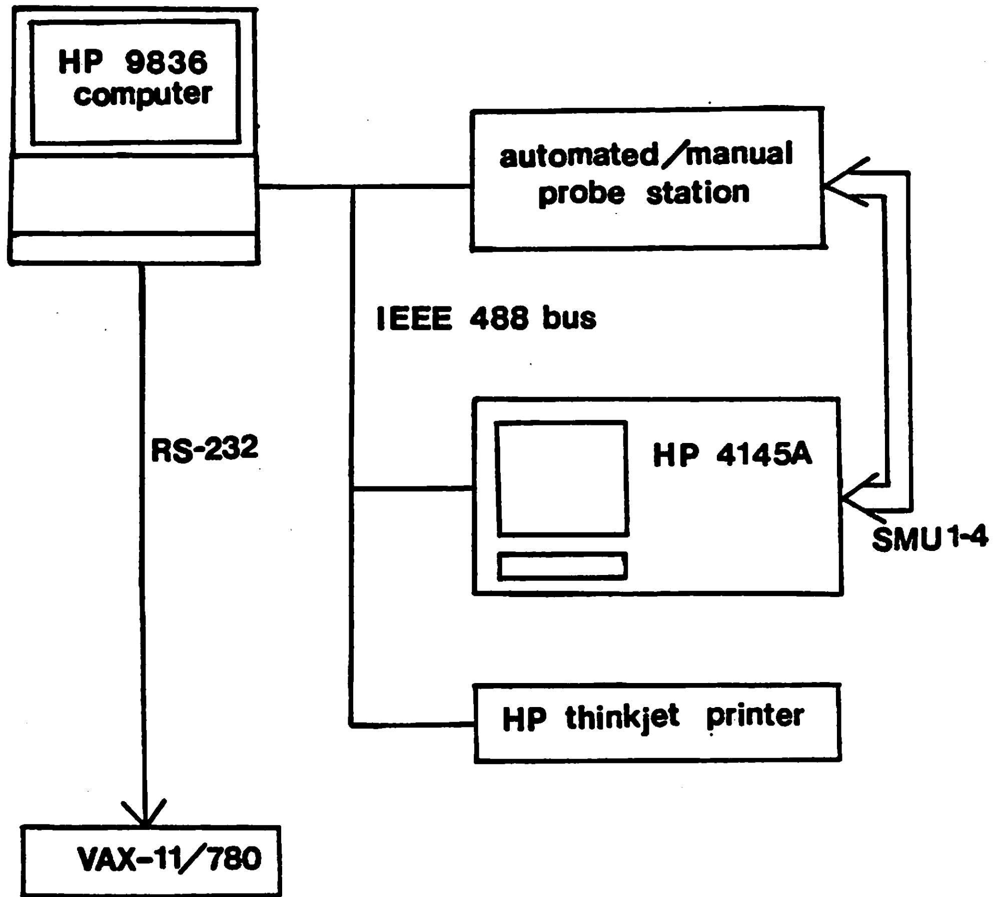


Fig. 3.2 Schematic diagram of the fully automated parameter-extraction system.

minimized is the norm of the error vector which can be written in the form [3.2]

$$||\mathbf{f}(\mathbf{p})||^2 = \sum_i f_i(\mathbf{p})^2 \equiv \sum_i \left(\frac{I_i(\mathbf{p}) - I_i^*}{\max(I_i^*, I_0)} \right)^2 . \tag{3.1}$$

Here $\mathbf{p}$ is the parameter vector to be optimized and $f(\mathbf{p})$ is the error vector between the measured drain current, I_i^*, and the calculated value, I_i, at the ith data point. User input I_0 determines whether a relative or absolute error is used.

The solution obtained by a global optimization technique is just a combination of parameter values that minimize the norm of the error vector, with no regard to the physical meaning. While the global optimization approach applies to single transistor characteristics well, it possess some difficulties in the extraction of size-independent parameters. The BSIM extraction program employs a different approach. The local extraction technique is used. Only related parameters are extracted together, instead of letting all the parameter values change on the fly as is done in the global fitting approach. Therefore, development of a process file which contains size-independent parameter values is simple and straightforward.

3.2.1. Program Features

The extraction software is written in H-P Pascal on the H-P 9836 computer, and is partitioned into six major modules [3.1]:

- automatic prober control
- device measurement control
- parameter extraction
- process file development
- interactive graphics
- menu and display handling.

Measurements are fully program-controlled. The only inputs from the user are the probe file, which contains device-layout information, and the extraction voltage range.

Parameter extraction does not depend on any initial guesses nor parameter bounds. The capability to develop a process file is also included in the parameter-extraction program. After devices of different sizes are measured and characterized, a process file is formed. The process file can then be transferred to a host computer for circuit simulation.

Salient features of the extraction program are summarized below:

(1) modular: This makes maintenance and updating simple.

(2) efficient: It only takes three minutes to extract strong-inversion parameters per transistor.

(3) accurate: Errors less than 4% for different transistor sizes and bias conditions have been achieved.

(4) user-friendly: It is menu-driven. Jobs can run interactively or in the batch mode.

(5) flexible: Four different operation modes are available. These include the fully automatic mode, semi-automatic mode, manual probe-station mode, and single-device mode.

(6) physical: Related parameters are extracted together. Extracted parameter values reflect their original physical meanings. This makes BSIM and the associated parameter-extraction program an excellent tool for statistical studies of transistor characteristics [3.6]-[3.8].

3.2.2. Highlights of Extraction Procedures

Figure 3.3 shows the flowchart of the whole program. Prior to the real parameter extraction, a series of functionality tests are performed to identify any defect devices or connection problems. Then, measurements of drain current corresponding to various bias conditions are carried out. Measured results are stored for the next step which extracts parameter values from the data. When the above procedures have been done for all devices on the same die, a process file is formed. Once the process file is created,

BSIM EXTRACTION PROGRAM FLOWCHART

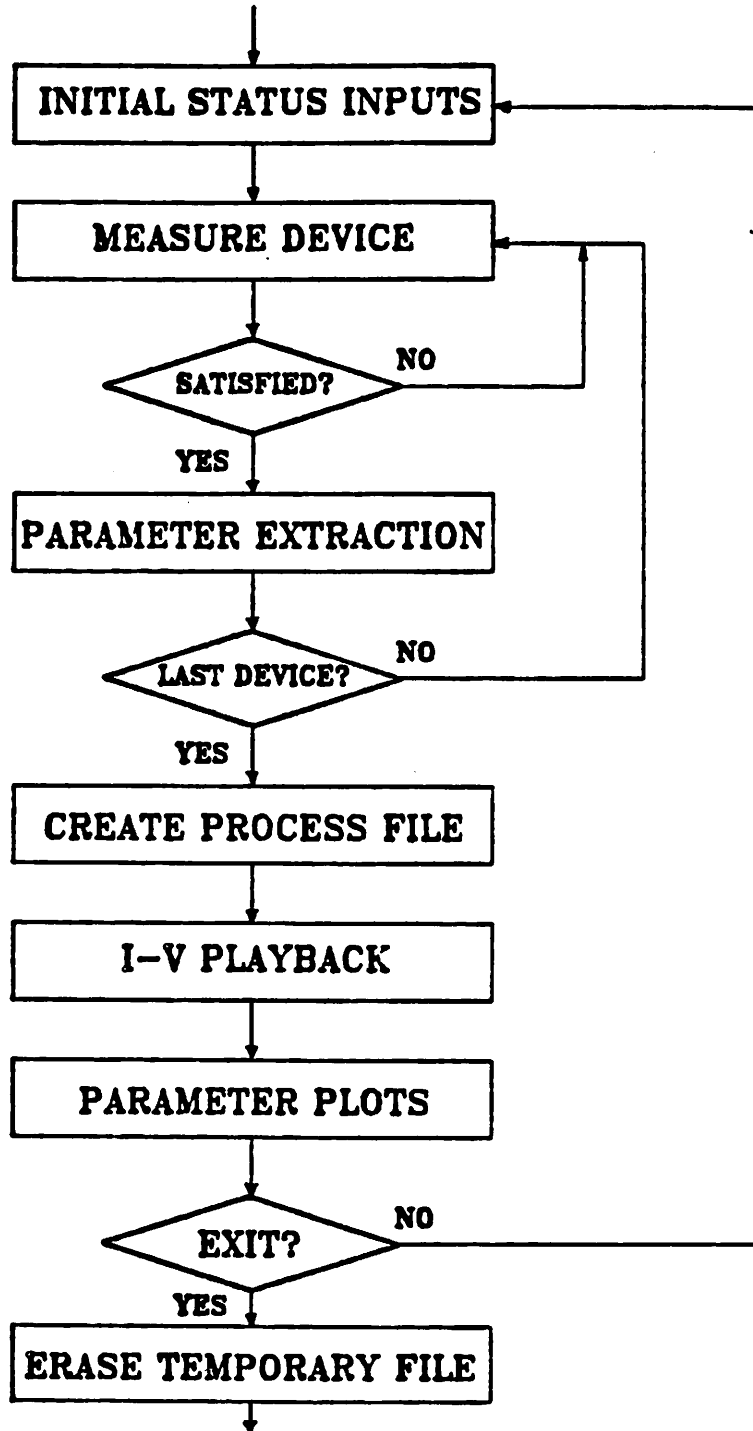


Fig. 3.3 Flowchart of the whole program.

the user can select on-line comparisons of measured and modeled results. Plots of extracted parameter values versus transistor channel lengths and widths can also be generated [3.9].

The flowchart for the parameter-extraction subroutine is shown in Fig. 3.4. Threshold voltage related parameters, together with low field parameters, are first extracted when small drain biases are applied to the transistor. The rest of the parameters are extracted when large drain biases are applied to the transistor. Additional information corresponding to a medium drain bias is used to refine the extracted parameter values, which makes the set of parameter values a good representation of the transistor characteristics over the whole bias range. Extraction of subthreshold parameters is implemented as an option. It can be activated after the extraction of strong-inversion parameters is finished.

A detailed description of the theory and algorithms used in the parameter-extraction program and a complete user's guide can be found in [3.10].

3.2.3. Subthreshold Parameter Extraction

To extract subthreshold parameters, transistor subthreshold swings are characterized under different drain and substrate biases. Then, three subthreshold parameters, n_0, n_B, and n_D, are fitted to the measured results with the linear-least-squares method. The fact that the subthreshold swing does not change too much makes the extraction task simple. Additional results of subthreshold parameter extraction can be found in [2.17].

Since the threshold voltage appears in the exponential term of the subthreshold conduction expression, the success of the subthreshold conduction model highly depends on the accurate determination of transistor threshold voltage.

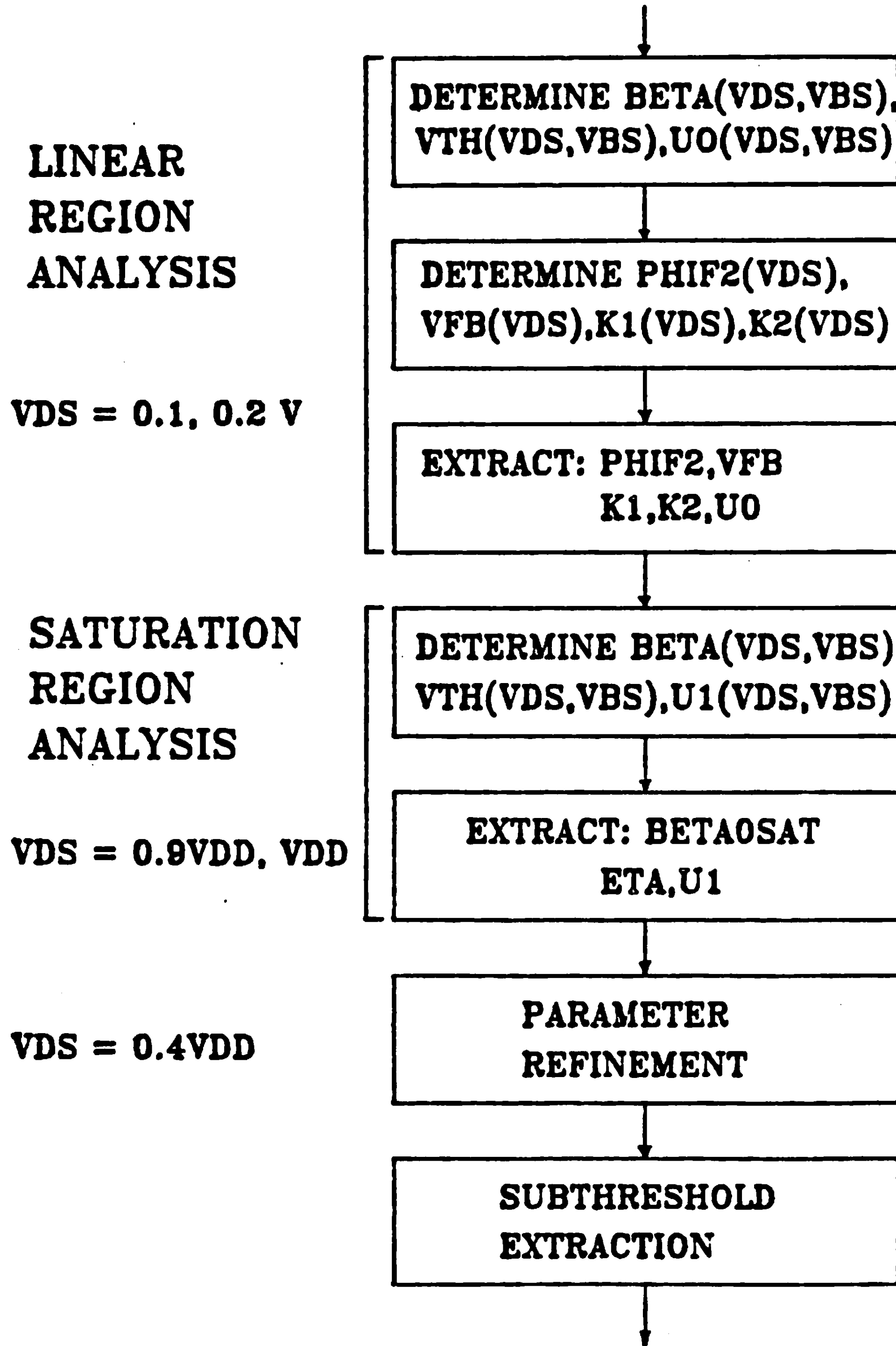


Fig. 3.4 Flowchart of the parameter-extraction subroutine.

3.3. Comparison of Measured and Modeled Results

Experiments were carried out using devices fabricated at various industrial sites. Figure 3.5 shows a comparison of measured and modeled output characteristics of a $W_{MK} = 20\ \mu m$ and $L_{MK} = 3.5\ \mu m$ N-channel transistor. Modeled results are plotted with solid lines while measured data are displayed with cross marks. Figure 3.6 shows a similar comparison for a $W_{MK} = 20\ \mu m$ and $L_{MK} = 2\ \mu m$ P-channel transistor. The comparison of long-channel N-channel and P-channel transistors are shown in Fig. 3.7 and 3.8, respectively. The gate-oxide thickness of the transistors is 30.0 nm. Figure 3.9 shows the results of a N-channel transistor with the gate-oxide thickness of 70.0 nm which was fabricated from a different process.

Comparison of measured and modeled total drain current for a $W_{MK} = 3\ \mu m$ and $L_{MK} = 4\ \mu m$ N-channel transistor is shown in Fig. 3.10. A similar comparison is shown in Fig. 3.11 for a $W_{MK} = 2\ \mu m$ and $L_{MK} = 4\ \mu m$ P-channel transistor. With threshold voltages properly characterized, agreement between measured and modeled results in the subthreshold region is excellent.

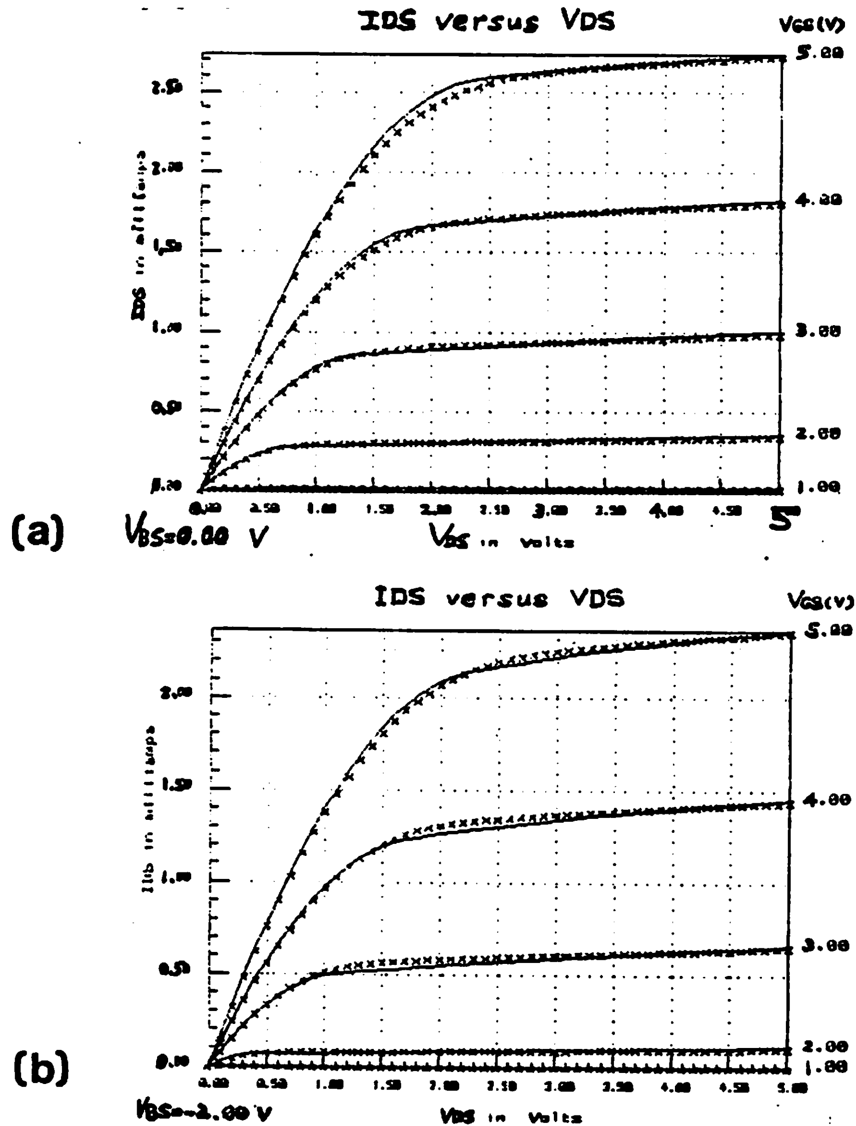
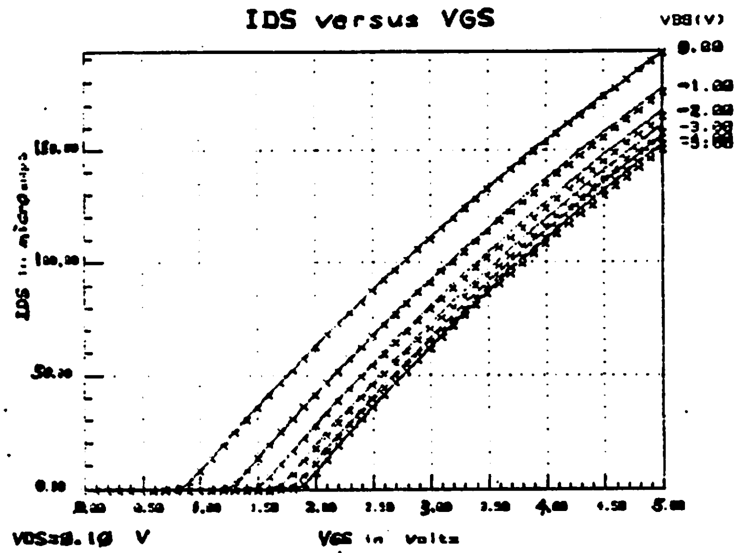
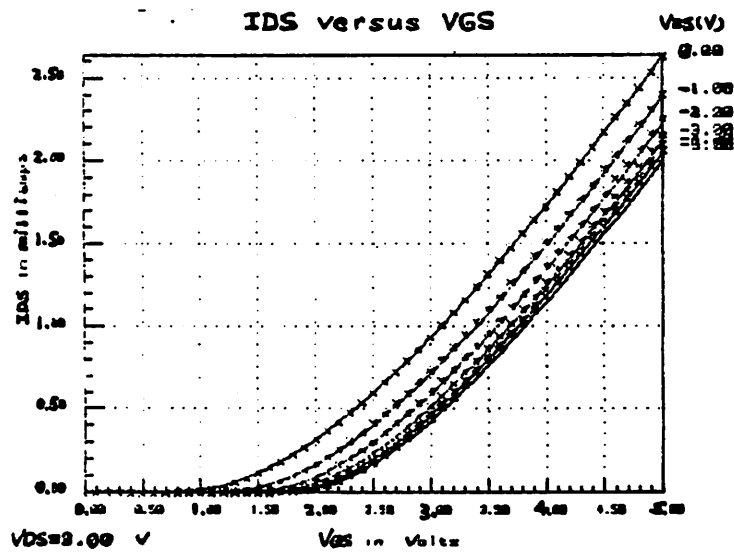


Fig. 3.5 Measured and modeled output characteristics of a W_{MK} = 20 μm and L_{MK} = 3.5 μm N-channel transistor. T_{ox} = 30.0 nm. (a) I_{DS} versus V_{DS} at V_{BS} = 0.0 V. (b) I_{DS} versus V_{DS} at V_{BS} = -2.0 V. (c) I_{DS} versus V_{GS} at V_{DS} = 0.1 V. (d) I_{DS} versus V_{GS} at V_{DS} = 3.0 V.



(c)



(d)

Fig. 3.5

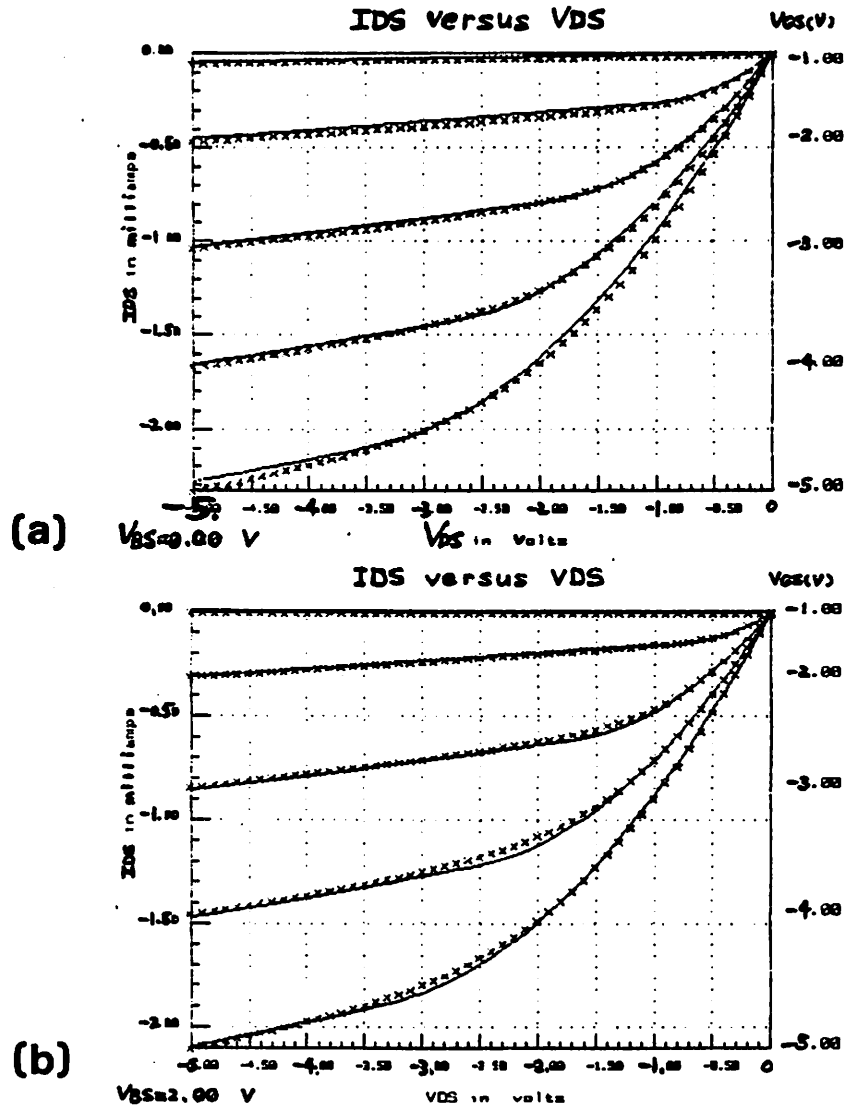
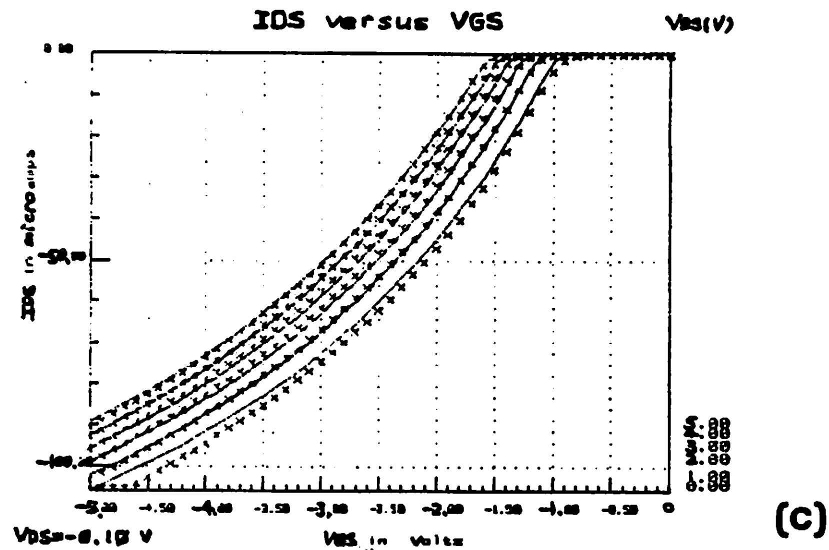


Fig. 3.6 Measured and modeled output characteristics of a $W_{MK} = 20\ \mu m$ and $L_{MK} = 2\ \mu m$ P-channel transistor. $T_{ox} = 30.0$ nm. (a) I_{DS} versus V_{DS} at $V_{BS} = 0.0$ V, (b) I_{DS} versus V_{DS} at $V_{BS} = 2.0$ V, (c) I_{DS} versus V_{GS} at $V_{DS} = -0.1$ V, (d) I_{DS} versus V_{GS} at $V_{DS} = -3.0$ V.



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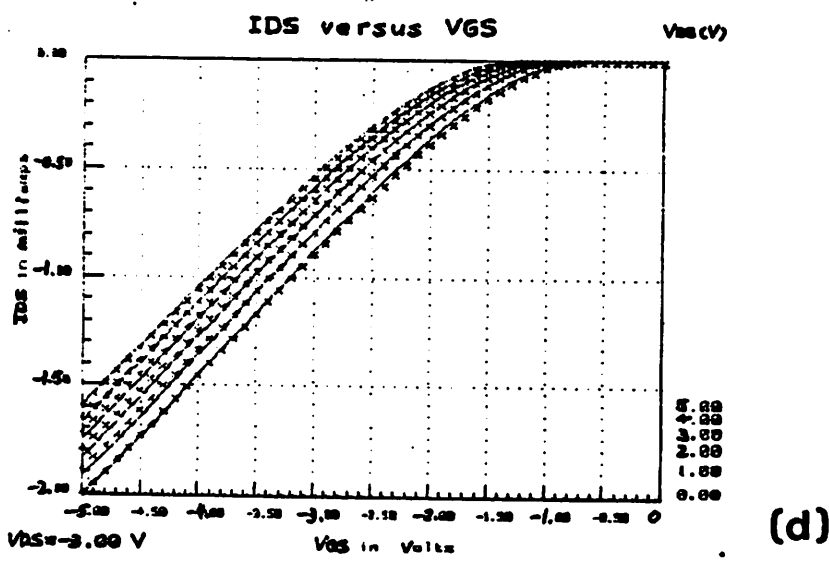

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Fig. 3.6

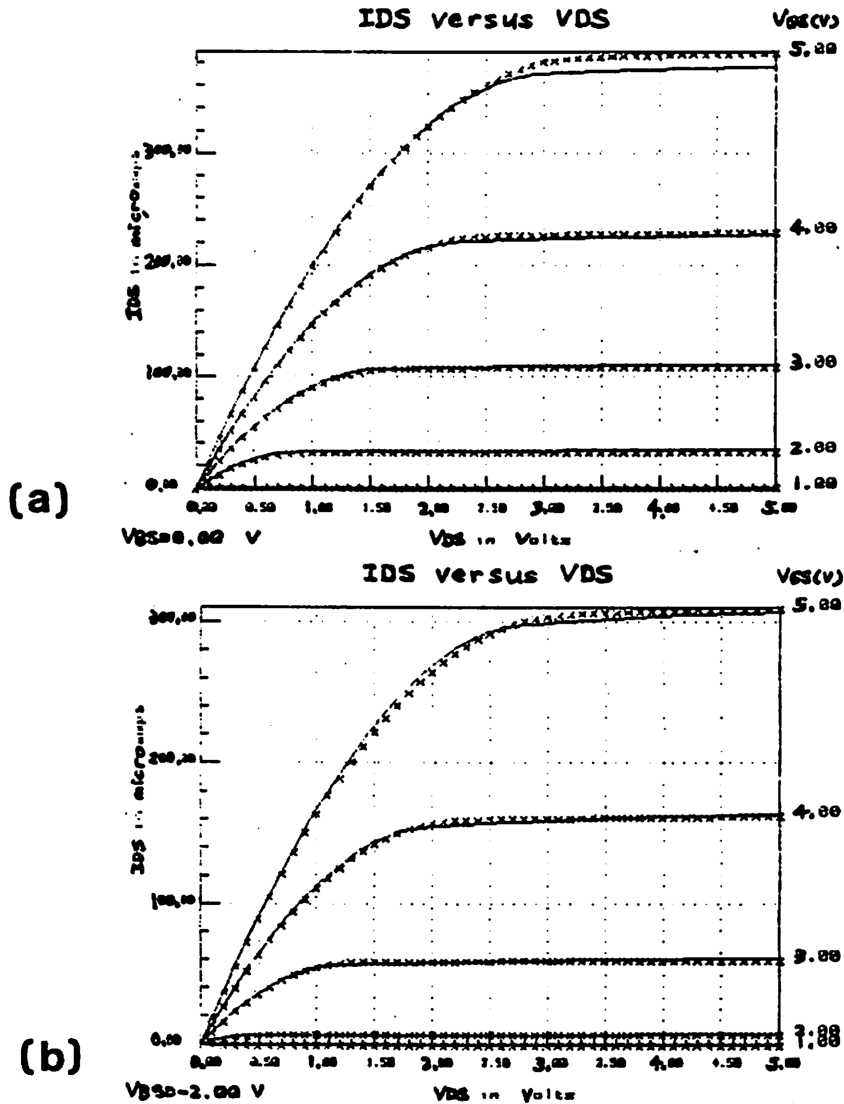
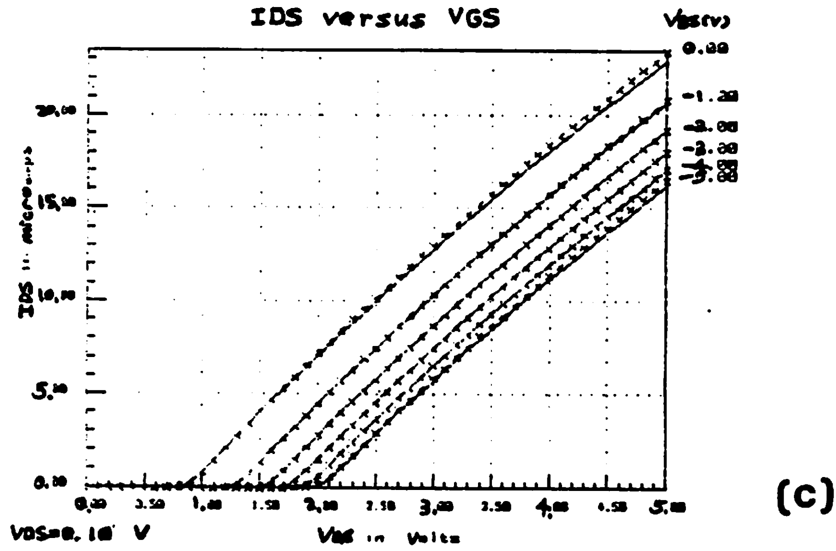


Fig. 3.7 Output characteristics of a W_{MK} = 20 μm and L_{MK} = 20 μm N-channel transistor. T_{ox} = 30.0 nm. (a) I_{DS} versus V_{DS} at V_{BS} = 0.0 V. (b) I_{DS} versus V_{DS} at V_{BS} = -2.0 V. (c) I_{DS} versus V_{GS} at V_{DS} = 0.1 V. (d) I_{DS} versus V_{GS} at V_{DS} = 3.0 V.



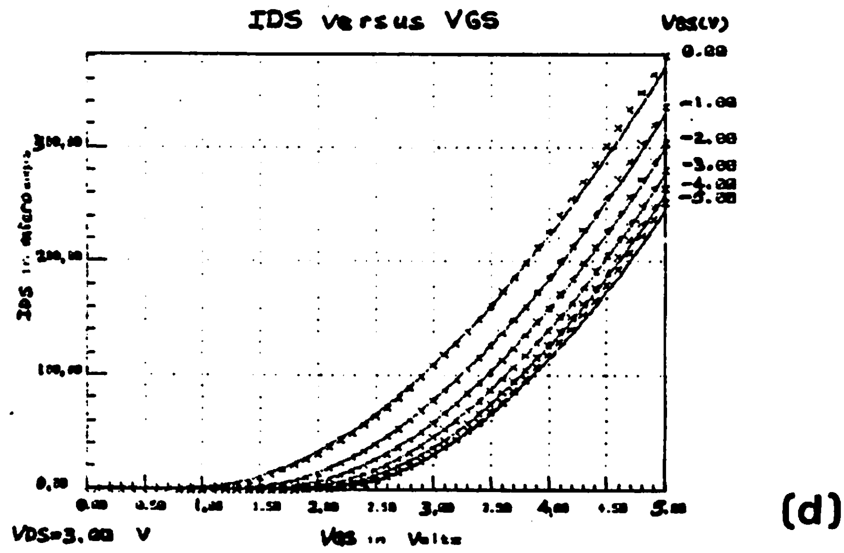


Fig. 3.7

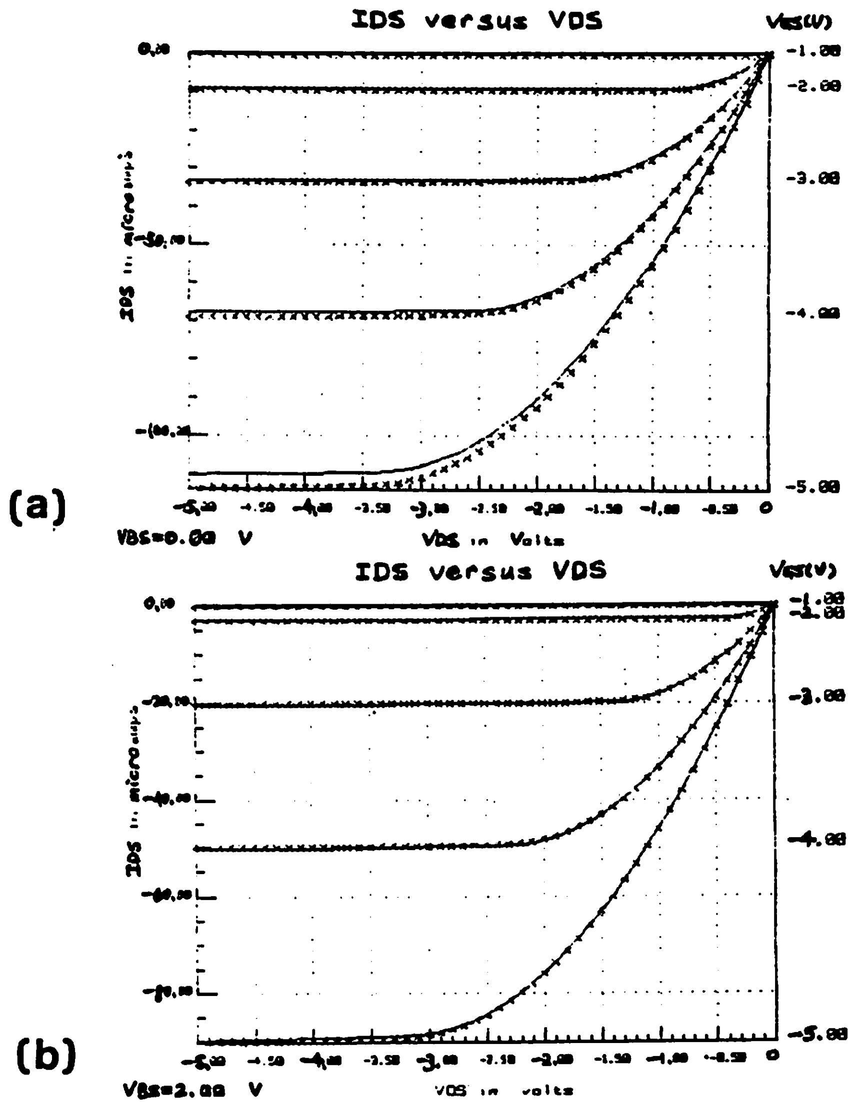
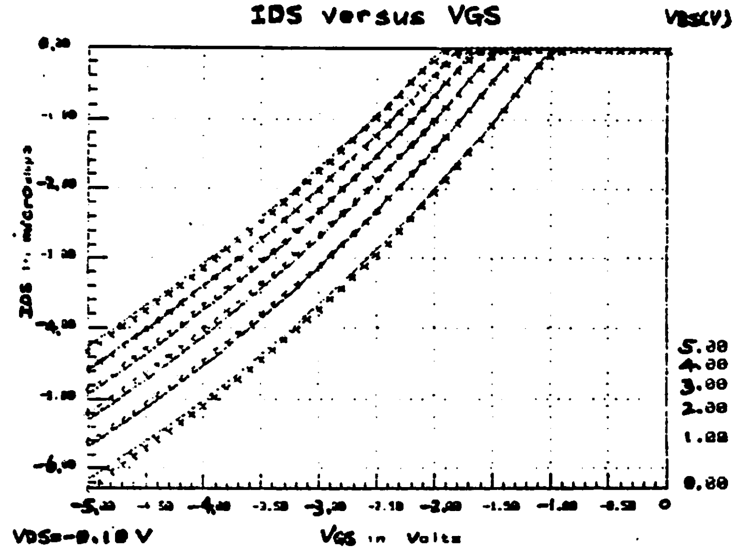


Fig. 3.8 Output characteristics of a $W_{MK} = 20$ μm and $L_{MK} = 20$ μm P-channel transistor. $T_{ox} = 30.0$ nm. (a) I_{DS} versus V_{DS} at $V_{BS} = 0.0$ V, (b) I_{DS} versus V_{DS} at $V_{BS} = 2.0$ V, (c) I_{DS} versus V_{GS} at $V_{DS} = -0.1$ V, (d) I_{DS} versus V_{GS} at $V_{DS} = -3.0$ V.



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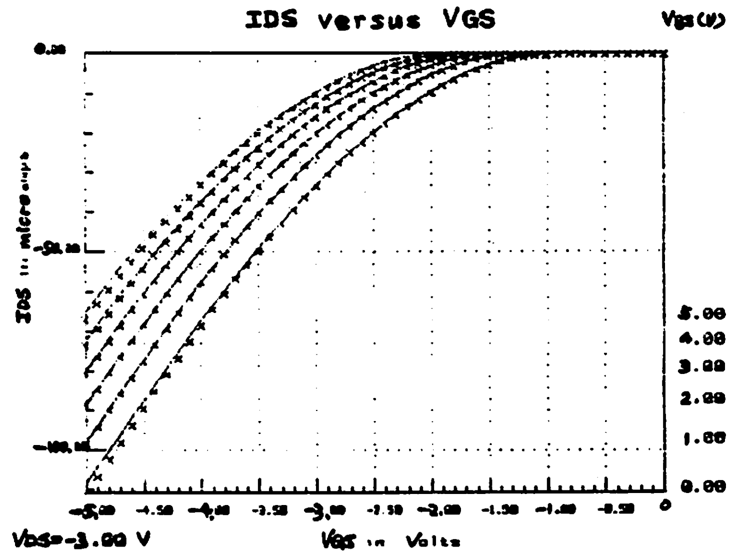


(d)

Fig. 3.8

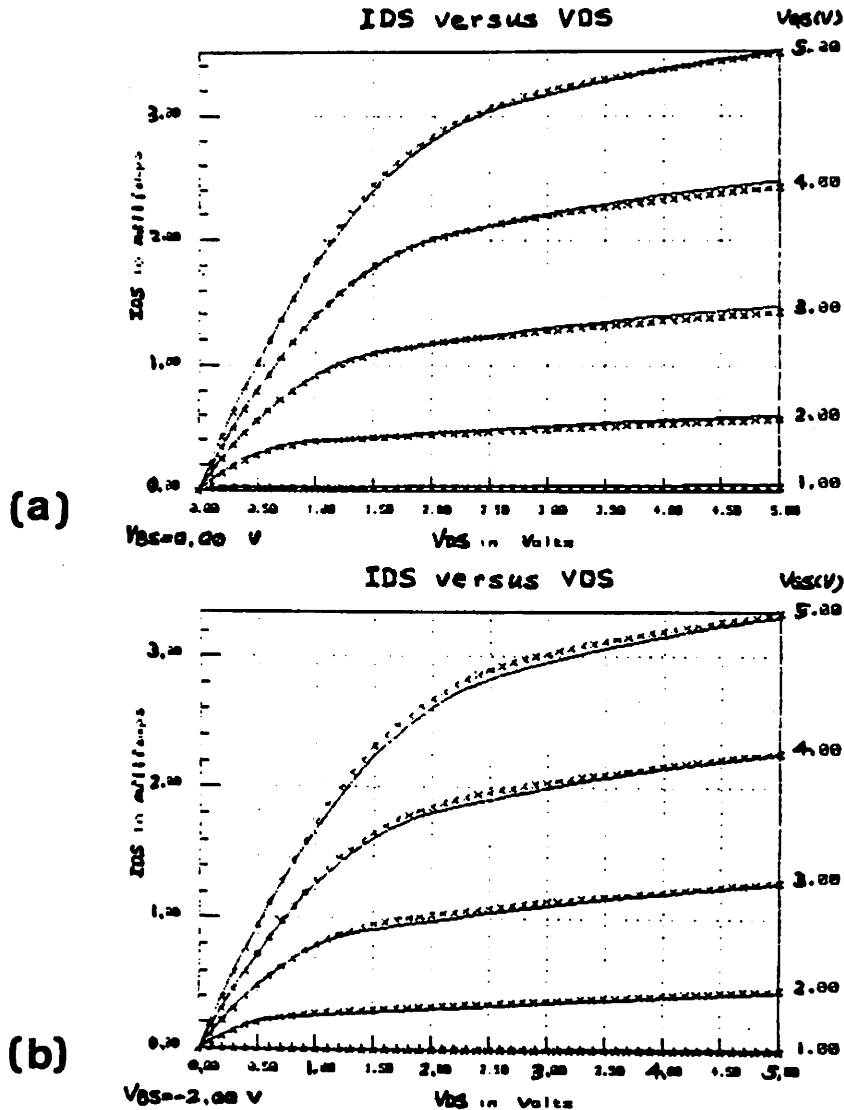
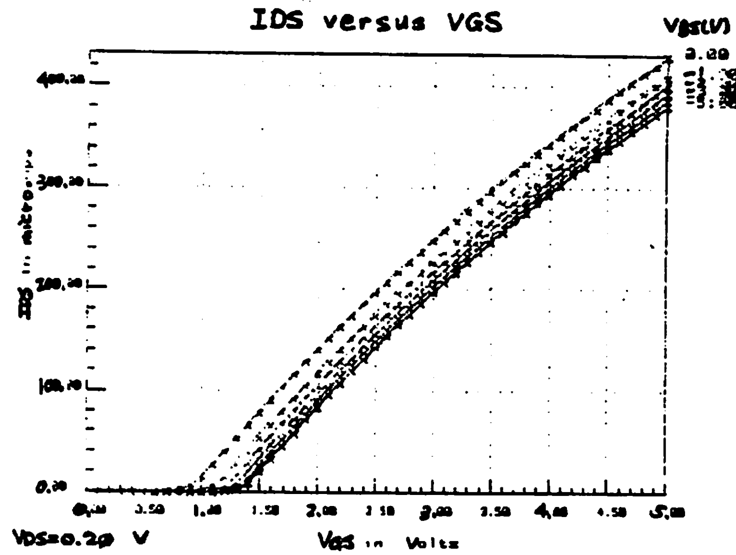


Fig. 3.9 Output characteristics of a W_{MK} = 50 μm and L_{MK} = 3.5 μm N-channel transistor. T_{ox} = 70.0 nm. (a) I_{DS} versus V_{DS} at V_{BS} = 0.0 V, (b) I_{DS} versus V_{DS} at V_{BS} = -2.0 V, (c) I_{DS} versus V_{GS} at V_{DS} = 0.2 V, (d) I_{DS} versus V_{GS} at V_{DS} = 3.0 V.



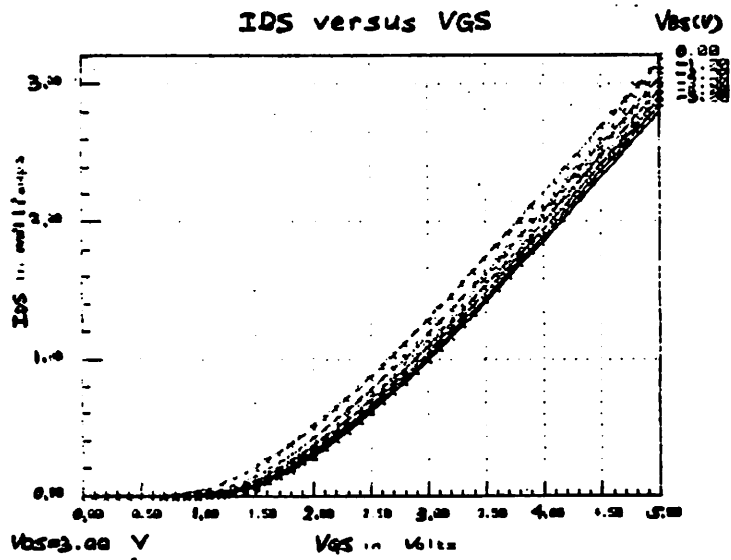


Fig. 3.9

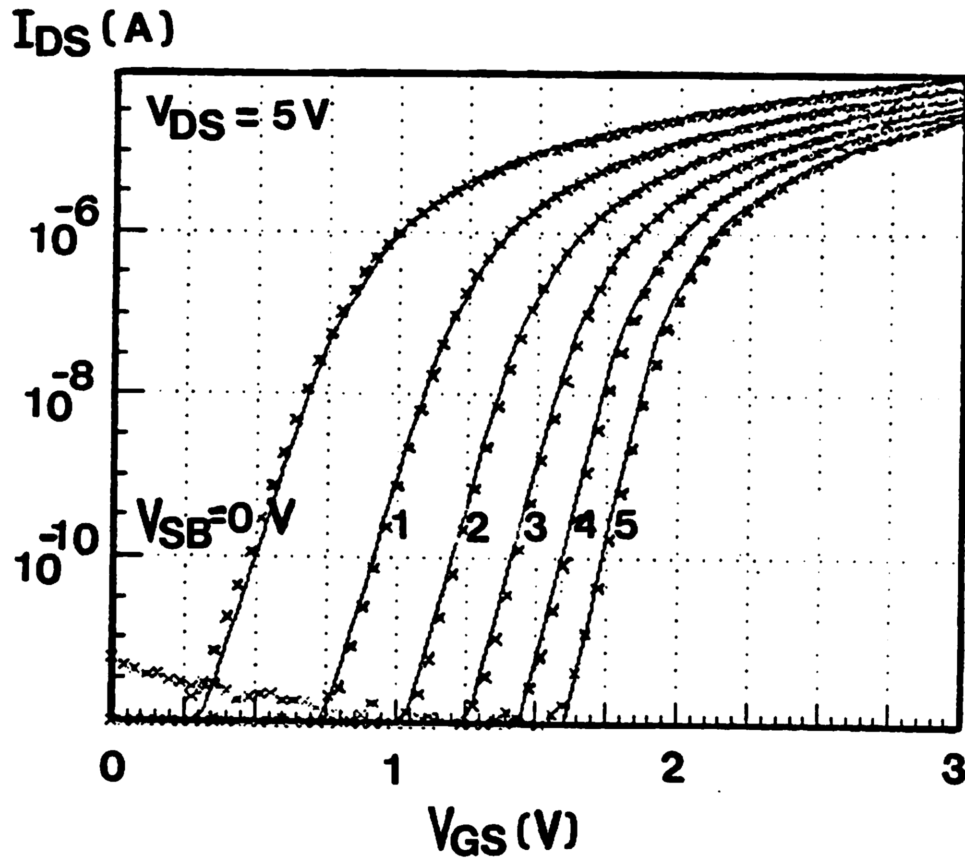


Fig. 3.10 Comparison of measured and modeled total drain current for a W_{MK} = 3 μm and L_{MK} = 4 μm N-channel transistor with Tox= 30.0 nm.

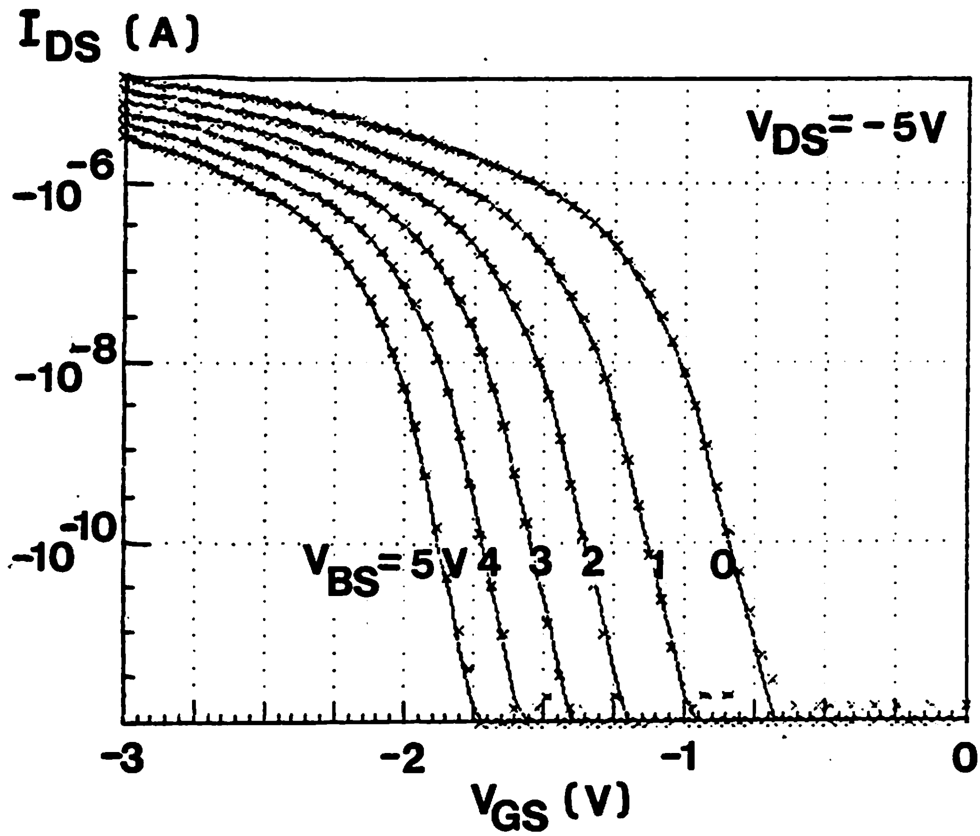


Fig. 3.11 Comparison of measured and modeled total drain current for a W_{MK} = 2 μm and L_{MK} = 4 μm P-channel transistor with Tox= 30.0 nm.

CHAPTER 4

THE BSIM CHARGE AND CAPACITANCE MODEL

Less effort has been devoted to obtaining satisfactory charge models than the dc models.

Both conductive and capacitive current components exist due to the same charge storage in an MOS transistor. The charge and capacitance model presented here was intimately derived with its associated dc model. The partitioning of the channel charge into drain and source components is given significant attention. Body-bias effects are properly incorporated and the device physics are explained and properly modeled.

4.1. Capacitance Modeling for Circuit Simulation - The Theory

In 1971, Meyer [4.1] proposed a capacitance model for circuit analysis which has become the basis for most existing MOS transistor models used in circuit simulators. In the Meyer model, the expressions for intrinsic gate capacitances are obtained from the derivatives of the gate-charge expression with respect to the gate-source and gate-drain voltages,

$$C_{gs} = \frac{\partial Q_G}{\partial V_{GS}} \quad \text{and} \quad C_{gd} = \frac{\partial Q_G}{\partial V_{GD}} . \tag{4.1}$$

It asserts that transistor capacitances are reciprocal and no ac coupling exists between the source and the drain, i.e., C_{sd} and C_{ds} are zero. The Meyer model, as was noted by Ward [4.2], fails to model the bulk charge. The effect of the bulk doping and body bias are indirectly included in the threshold voltage. However, the threshold voltage is treated as constant when taking integrals or derivatives.

To derive a complete and accurate MOS transistor capacitance model for circuit analysis, the following issues need to be properly addressed: charge conservation, channel-charge partitioning, small-geometry effects, and distributed-channel effect.

4.1.1. Choice of State Variables

The issue of modeling MOS transistor charge storage [4.2,4.3] has attracted integrated-circuit designers' attention since Ward and Dutton [4.4] pointed out that charge nonconservation is a particular problem for the Meyer model in simulating circuits containing high impedance nodes as are typical in dynamic and charge-storage circuits. Either inaccuracies or failures will occur in the simulation results of some switched-capacitor, DRAM, and silicon-on-sapphire circuits that are sensitive to the capacitive components of the MOS transistor currents.

Although there have been various solutions proposed in the literature, there is unanimous agreement that the solution to the charge non-conservation problem is to use the terminal charges instead of the terminal voltages as state variables. The terminal charges, Q_G, Q_B, Q_S, and Q_D are the charges associated with the gate, bulk (body), source, and drain, and the capacitive current components of I_G, I_B, I_S, and I_D, are respectively the derivatives of Q_G, Q_B, Q_S, and Q_D with respect to time.

Yang et al. [4.5] demonstrated the importance of choosing charge as the state variable by using a nonlinear capacitor which is controlled by a remote voltage other than its terminal voltages. A discontinuous relationship of the capacitor versus controlling voltage is contrived in their network.

In general, a simple example can be constructed to illustrate the fundamental nature of charge non-conservation problem [4.6]. First, one may write a capacitance branch relation in terms of charge.

$$Q = f(v1, v2, \ldots, t) \tag{4.2}$$

$$i = \frac{d}{dt} f(\, v1, v2, \ldots, t) = \frac{\partial f}{\partial v1}\frac{dv1}{dt} + \frac{\partial f}{\partial v2}\frac{dv2}{dt} + \ldots + \frac{\partial f}{\partial vn}\frac{dvn}{dt} + \frac{\partial f}{\partial t} \, . \quad (4.3)$$

Fortunately, we can use the simple case of the stored charge being a function of a single voltage as follows:

$$Q = f(v) \, . \quad (4.4)$$

$$i = \frac{d}{dt} f(v) = \frac{\partial f}{\partial v} \cdot \frac{dv}{dt} \, . \quad (4.5)$$

We recognize $\partial f / \partial v$ as the definition of capacitance and call it $C(v)$. Then,

$$i = C(v) \frac{dv}{dt} \, . \quad (4.6)$$

By integrating from the present time point, t_0, to the next time point, t_1, Eq. (4.6) becomes

$$\int_{t_0}^{t_1} i(t)\, dt = \int_{t_0}^{t_1} C(v)\, dv \, . \quad (4.7)$$

Here comes the problem. If $C(v)$ is treated as a constant and pulled out, Eq. (4.7) simplifies to

$$\int_{t_0}^{t_1} i(t)\, dt = C(v) \left[\, v(t_1) - v(t_0) \,\right] . \quad (4.8)$$

The function $C(v)$ is not known over the interval t_0 to t_1. The Meyer model implemented in SPICE2 evaluates $C(v)$ at t_0. This rules out charge conservation. The problem can not be totally eliminated even by careful choices of step sizes and error tolerances. Evaluation of $C(v)$ at t_1 has been suggested as an alternative. Since t_1 is the new time, it must be picked up during the iteration. Still, it will not conserve charge.

Now, if the charge formulation is used instead, all problems are avoided. Note that

$$i = \frac{dQ}{dt} \quad (4.9)$$

By integrating from t_0 to t_1, Eq. (4.9) becomes

$$\int_{t_0}^{t_1} i(t)dt = Q(t_1) - Q(t_0) = f(v(t_1)) - f(v(t_0)) . \tag{4.10}$$

In view of $f(v(t_1))$ being evaluated at the new time point, one can simply perform the Taylor-series expansion about the voltage at the last iteration to obtain the companion model. Either the trapezoidal or Gear integration formula [1.3] can be applied to the left-hand side of Eq. (4.10) to carry out the complete integration.

4.1.2. Channel-Charge Partition

For the bulk charge, an approximate expression is more suitable for the circuit-simulation purpose than an "exact" expression which is very complicated. The nonuniform bulk-doping profile of implanted-channel devices introduces additional complexity.

The expressions for the gate and bulk charges are relatively easy to derive compared to the source and drain charge expressions because both the source and drain terminals are in intimate contact with the channel region. The channel charge can not be associated only with the drain or only with the source. Partitioning of the channel charge into source and drain components must be done carefully.

A number of channel-charge partitioning methods have been attempted. The point of partition is somewhat arbitrary, usually based on physical arguments without substantial theoretical or experimental supports [4.2]. The partition may imply that the gate-to-drain and gate-to-source capacitances are reciprocal [4.7],[4.8], that C_{dg} must be zero in saturation [4.9], or that the drain-source capacitances must be zero [4.10].

Ward [4.2] has developed a physically meaningful partitioning method. The formulas are shown below,

$$Q_S = W \int_0^L \left(1 - \frac{y}{L} \right) q_c(y)\, dy \tag{4.11}$$

$$Q_D = W \int_0^L \frac{y}{L} q_c(y)\, dy \tag{4.12}$$

The point of partition, according to this method, is at 3/5 of the channel from the source end. This partitioning method leads to an admittance matrix for the device whose capacitance terms are all nonzero and non-reciprocal, and the capacitances between the source and the drain (C_{sd} and C_{ds}) are negative. The non-reciprocal gate capacitances produce gate-to-source and gate-to-drain feedthrough which are not present in the Meyer model. The universally accepted non-reciprocal capacitance is similar to a voltage-controlled current source which produces current in proportion to the time derivative of the controlling voltage. The gate-drain capacitances C_{gd} and C_{dg} differ both in value and in physical interpretation. Capacitance C_{gd} describes the gate current produced by a change in the drain voltage, while C_{dg} gives the drain current which results from a change in the gate voltage. Capacitance C_{gd} is zero in the saturation region due to the channel being isolated from the drain terminal, but C_{dg} has a finite value.

Although non-reciprocity has been proven with measurements [4.2,4.11] and device analysis, the term "non-reciprocal capacitance" is a misnomer. A more appropriate name should be "trans-capacitive coefficient".

4.1.3. Small-Geometry Effects

So far, capacitance models used in circuit simulators are mainly for long-channel devices. Small-geometry effects haven't been included yet. The important effects in modeling the dc characteristics of small-geometry transistors are essential in modeling the ac characteristics. These effects are:

- vertical field mobility degradation effect,
- carrier velocity saturation effect,
- channel-length modulation effect,

- source-drain series resistance effect.

The channel-side bias-dependent fringing-field effect is uniquely associated with the ac characteristics. A detailed description of modeling the small-geometry transistor capacitances can be found in Appendix H.

4.1.4. Distributed-Channel Effect

When a transistor is turned on, it takes a certain amount of time to build up the channel charge. When the transistor is turned off, another amount of time is needed to dissipate the channel charge. The time constant of the channel is inversely proportional to the amount of channel charge and is thus non-negligible at low gate bias, especially for long-channel transistors [4.12]. An empirical expression for the channel transit time constant, assuming no velocity saturation effect, is [4.13,4.14]

$$\tau_0 = \frac{L_{eff}}{\mu_n \left(\frac{q_c}{C_o} \right)} \tag{4.13}$$

where q_c is per unit-area channel charge density.

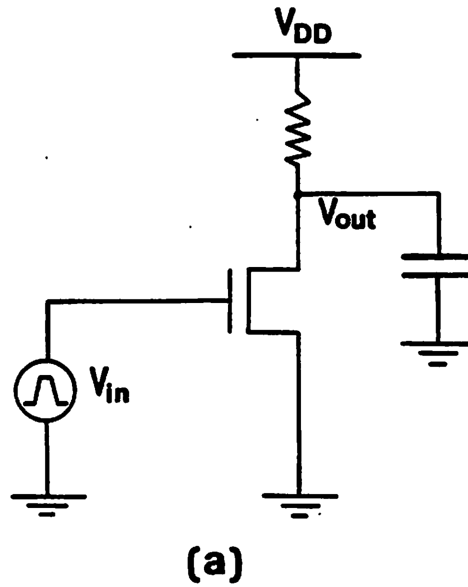
The quasi-static approximation (QSA), which is widely used in deriving circuit-simulation device models, assumes that the terminal charges found under steady-state conditions are valid during all transient conditions. By neglecting the distributed nature of the channel, it allows the stored charges to be evaluated from the instantaneous terminal voltages. This assumption becomes incorrect when circuit transient time is comparable to the transistor channel transit time. Fortunately, fast circuits are usually built with fast devices. There can be errors when a few slow (long-channel) transistors are used in a very fast circuit.

Previous approaches to high-speed transient circuit analysis [4.14,4.15] have several limitations. The non-linear transmission line approach, while valid at high speeds, is generally limited to simplified conditions. Lack of bulk-charge effects and

step inputs are typical restrictions. Paulos et al. [4.16] obtained an analytical solution to the non-linear transmission line analysis in the small-signal domain by truncating the Bessel functions. However, their results are not readily applicable to the large-signal transient analysis.

In using the conventional lumped MOS transistor model, special attention has to be paid to the channel-charge partitioning method. Although the 40/60 channel-charge partitioning scheme [4.17] has a sound physical foundation for quasi-static applications, large current spikes appear due to the gate-to-drain capacitive feedthrough when the transistor is biased in the saturation region. This feedthrough capacitance introduces a low-frequency pole in the small-signal analysis and greatly affects simulation results. Figure 4.1 shows a schematic diagram of a resistive-load inverter with a linear ramp waveform applied to the gate. Output characteristics for the 40/60 and 0/100 channel-charge partitioning methods are shown in Fig. 4.2(a), and (b), respectively. The feedthrough-induced current spikes are a function of the gate-voltage ramping speed.

A lumped MOS transistor model does not offer the exponential-type increase or decrease of drain and source currents to the final value. Instead, it predicts sharp changes when the gate voltage goes across the threshold voltage. This is because the distributed nature of the channel is not included in the model. The multi-sectional approach is suitable for modeling the distributed channel effect [4.13]. The number of sections per transistor should be judiciously chosen to obtain accurate simulation results with reasonable execution time. Preliminary results show that no more than four sections per transistor are needed. A schematic diagram of the high-frequency device models for advanced MOS VLSI circuit analysis is shown in Fig. 4.3. In addition to the distributed-channel effect of the intrinsic transistor region, the long-distance interconnect effect, wide-gate effect, and local interconnect effect are all essential for



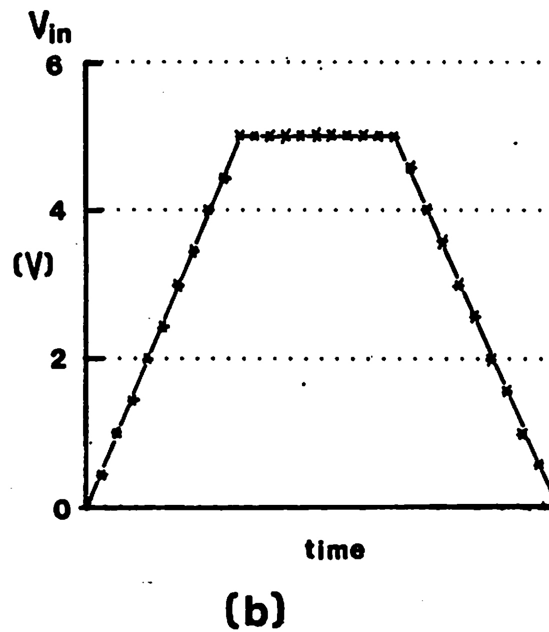
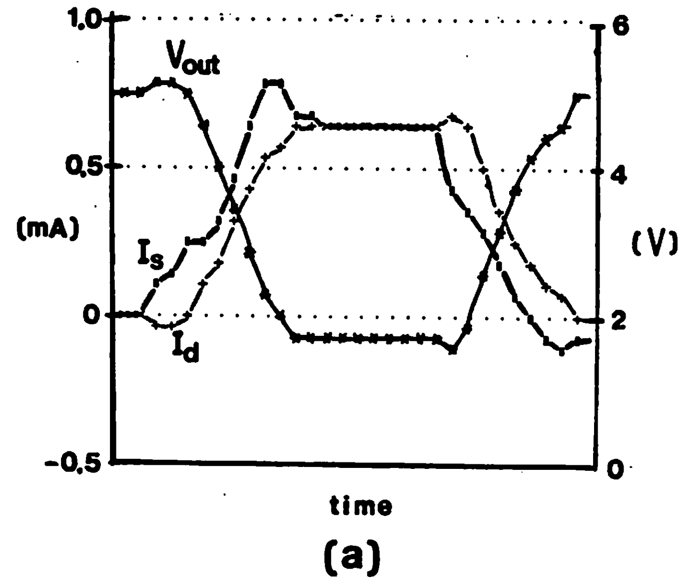


Fig. 4.1 (a) Schematic diagram of a simple resistive-load inverter and the (b) input waveform.



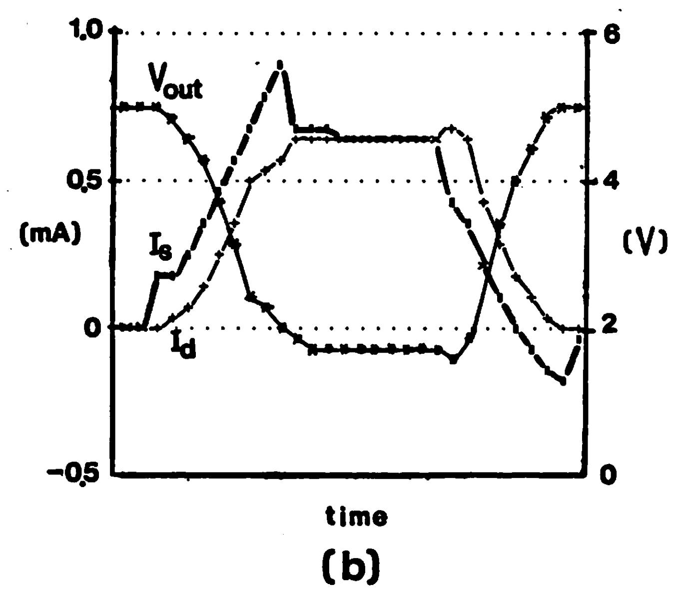


Fig. 4.2 Output voltages and currents for the (a) 40/60. and (b) 0/100 channel-charge partitioning methods.

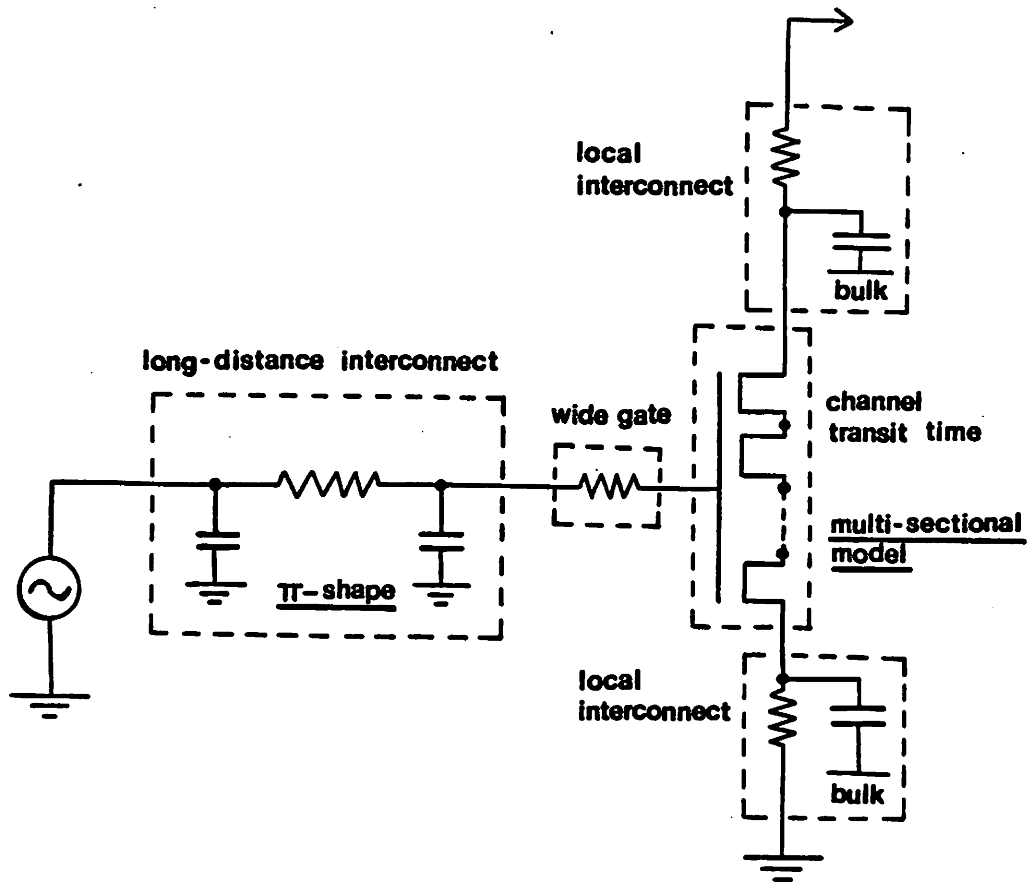


Fig. 4.3 A schematic diagram of high-frequency device models. Long-distance interconnect effect, wide-gate effect, local interconnect effect, as well as distributed channel effect are important for advanced circuit simulation.

advanced MOS VLSI circuit simulation.

4.2. The BSIM Charge Model

A new and simple charge model for BSIM has been derived. This new model conserves charge and has the non-reciprocal property. The expressions for the charge densities are similar in form to those of [4.5]. However, due to different ways of treating the physics behind transistor operation, the functional dependence of α_x is quite different. The charge equations in the different operation regions are given below.

(A) Accumulation region:

$$Q_G = W\,L\,C_o\,(V_{GS} - V_{FB} - V_{BS})\,. \tag{4.14}$$

$$Q_B = -Q_G\,. \tag{4.15}$$

$$Q_S = 0\,. \tag{4.16}$$

$$Q_D = 0\,. \tag{4.17}$$

(B) Subthreshold region:

$$Q_G = W\,L\,C_o\,\frac{K_1^2}{2}\left[-1 + \left[1 + \frac{4\,(V_{GS} - V_{FB} - V_{BS})}{K_1^2}\right]^{1/2}\right]. \tag{4.18}$$

$$Q_B = -Q_G\,. \tag{4.19}$$

$$Q_S = 0\,. \tag{4.20}$$

$$Q_D = 0\,. \tag{4.21}$$

When an MOS transistor is biased in the triode region, the distributed charge densities of the gate, channel, and bulk can be expressed as:

$$q_g(y) = C_o\,(V_{GS} - V_{FB} - \phi_S - V_y)\,. \tag{4.22}$$

$$q_c(y) = -C_o\,(V_{GS} - V_{th} - \alpha_x V_y)\,. \tag{4.23}$$

$$q_b(y) = -C_o\,[V_{th} - V_{FB} - \phi_S - (1 - \alpha_x)\,V_y\,]\,. \tag{4.24}$$

where

$$\alpha_x = a\left[1 + \frac{U_1}{L}(V_{GS} - V_{th})\right]. \tag{4.25}$$

Here, V_y is the electron quasi-Fermi potential with respect to the source. Observe that

$$q_g + q_c + q_b = 0. \tag{4.26}$$

This relationship follows the constraint of charge neutrality in a one-dimensional MOS capacitor structure.

Expressions for the total charge stored in the gate, bulk, and channel regions can be obtained by integrating the distributed charge densities over the area of the active gate region (from $y = 0$ to $y = L$ and $z = 0$ to $z = W$). That is,

$$Q_G = W\int_0^L q_g(y)\,dy, \tag{4.27}$$

$$Q_B = W\int_0^L q_b(y)\,dy, \tag{4.28}$$

$$Q_C = W\int_0^L q_c(y)\,dy. \tag{4.29}$$

Here, $q_c(y)$ is the mobile channel charge per unit length along the channel, and y is the position along the channel from 0 to L.

Combining Eqs. (4.22)-(4.24) with Eqs. (4.27)-(4.29) and replacing the differential channel length "dy" with the corresponding differential potential drop "dV", we obtain the following expressions for total gate, channel, and bulk charges in static equilibrium.

$$Q_G = W\int_0^L C_o(V_{GS} - V_{FB} - \phi_S - V_y)\,dy$$

$$= WL\,C_o\left|V_{GS} - V_{FB} - \phi_S - \frac{V_{DS}}{2} + \frac{V_{DS}}{12}\,\frac{\alpha_x V_{DS}}{(V_{GS} - V_{th} - \frac{\alpha_x}{2}V_{DS})}\right|\cdot \tag{4.30}$$

$$Q_B = -W\int_0^L C_o[V_{th} - V_{FB} - \phi_S - (1-\alpha_x)V_y]\,dy$$

$$= W L C_o \left[- V_{th} + V_{FB} + \phi_S + \frac{(1-\alpha_x)}{2} V_{DS} - \frac{(1-\alpha_x) V_{DS}}{12} \cdot \frac{\alpha_x V_{DS}}{(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS})} \right] . \quad (4.31)$$

$$Q_C = - W \int_0^L C_o (V_{GS} - V_{th} - \alpha_x V_y) \, dy$$

$$= -WLC_o \left[V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS} + \frac{\alpha_x V_{DS}}{12} \cdot \frac{\alpha_x V_{DS}}{(V_{GS} - V_{th} - \frac{\alpha_x}{2} V_{DS})} \right] . \quad (4.32)$$

It is clear that the total stored charge components of an MOS transistor, Eqs. (4.30)-(4.32), also exhibit charge-neutrality relationship,

$$Q_G + Q_C + Q_B = 0 . \quad (4.33)$$

It is necessary to partition the channel charge into the drain component (Q_D) and the source component (Q_S). The issue of channel-charge partition has so far been dealt with by gross approximation or use of an arbitrary factor. Ward et al. [4.4] already noted this difficulty. They describe many possibilities and chose the 50/50 partition between Q_D and Q_S, although their device simulation had indicated a 40/60 partition in the saturation region. Yang, et al [4.5] proposed to make the partition so as to satisfy the condition that Q_D and Q_S and their derivatives be continuous throughout the triode and saturation regions. They failed to note, however, that there are infinite ways to partition the channel charge to satisfy that requirement.

Taylor, et al. [4.18] adopted the 50/50 partition for mathematical simplicity while noting that the correct partition of the capacitive current is 0/100 whenever dV_G/dt is positive (assuming an N-channel transistor) and 100/0 whenever dV_G/dt is negative. Their reasoning is that electrons can enter the channel only from the source and leave the channel only through the drain. In reality, only the net current flow obeys that restriction, if at all. The capacitive current, which is merely the difference between the net current and the quasi-static current that would be present in the absence of

capacitive coupling, can flow in either direction.

A sound theoretical model for channel-charge partition is of particular importance because if the partition is performed through the use of a parameter, then that parameter (actually a function of the bias voltage) is unusually difficult to extract from device measurements. In this work, the issue of channel-charge partition is appropriately handled.

In BSIM, the drain/source partitioning of the channel charge smoothly changes from 40/60 (or 0/100) in the saturation region to 50/50 distribution in the triode region.

4.2.1. The 40/60 Channel-Charge Partitioning Method

The channel-charge partitioning method proposed by Ward et al. [4.2] is used. Carrying out the integrations in Eqs. (4.11) and (4.12), with $q_c(y)$ replaced by the expression in Eq. (4.23), we obtain the total charges associated with the source and the drain,

(C) Triode Region:

Expressions for the gate charge and the bulk charge are the same as those in Eqs. (4.30) and (4.31), and

$$Q_S = -W L C_o \left[\frac{V_{GS}-V_{th}}{2} + \frac{\alpha_x V_{DS}}{12} \cdot \frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})} \right.$$

$$\left. - \frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})^2} \left[\frac{(V_{GS}-V_{th})^2}{6} - \frac{\alpha_x V_{DS}(V_{GS}-V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40} \right] \right] . \quad (4.34)$$

$$Q_D = -W L C_o \left[\frac{V_{GS}-V_{th}}{2} - \frac{\alpha_x V_{DS}}{2} + \frac{\alpha_x V_{DS}}{(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})^2} \right.$$

$$\cdot \left[\frac{(V_{GS}-V_{th})^2}{6} - \frac{\alpha_x V_{DS} (V_{GS}-V_{th})}{8} + \frac{\alpha_x^2 V_{DS}^2}{40} \right] \Bigg] . \quad (4.35)$$

(D) Saturation Region:

$$Q_G = W L C_o (V_{GS} - V_{FB} - \phi_S - \frac{V_{GS} - V_{th}}{3 \alpha_x}) . \quad (4.36)$$

$$Q_B = W L C_o [V_{FB} + \phi_S - V_{th} + \frac{(1 - \alpha_x) (V_{GS} - V_{th})}{3 \alpha_x}] . \quad (4.37)$$

$$Q_S = - \frac{2}{5} W L C_o (V_{GS} - V_{th}) . \quad (4.38)$$

$$Q_D = - \frac{4}{15} W L C_o (V_{GS} - V_{th}) . \quad (4.39)$$

4.2.2. The 0/100 Channel-Charge Partitioning Method

The 0/100 channel-charge partitioning method can be derived using the following boundary conditions.

(1) Expressions for all terminal charges and capacitances are continuous from the saturation region through the triode region.

(2) The charges Q_S and Q_D are equal and the capacitances C_{sg} and C_{dg} are equal when V_{DS} is zero.

(3) In the saturation region, all the channel mobile charge is only associated with the source and Q_D is zero [4.5].

(4) For the simplicity of model equations, partition is done using the existing terms in the Q_C expression. No additional terms are introduced.

(C') Triode region:

Expressions for the gate charge and the bulk charge are the same as those in Eqs. (4.30) and (4.31), and

$$Q_S=-WLC_o\left[\frac{V_{GS}-V_{th}}{2}+\frac{\alpha_x}{4}V_{DS}-\frac{(\alpha_x V_{DS})^2}{24\,(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right]. \tag{4.40}$$

$$Q_D=-WLC_o\left[\frac{V_{GS}-V_{th}}{2}-\frac{3}{4}\alpha_x V_{DS}+\frac{(\alpha_x V_{DS})^2}{8\,(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right]. \tag{4.41}$$

(D') Saturation region:

Expressions for the gate charge and the bulk charge are the same as those in Eqs. (4.36) and (4.37), and

$$Q_S=-\frac{2}{3}\,W\,L\,C_o\,(\,V_{GS}-V_{th}\,)\,. \tag{4.42}$$

$$Q_D=0\,. \tag{4.43}$$

4.2.3. The 50/50 Channel-Charge Partitioning Method

Gate capacitances are particularly important, more than other terminal capacitances for VLSI circuits which are mainly made up of short-channel devices. Once the gate capacitances are measured, a charge-based capacitance model can be constructed using simple channel-charge partitioning methods, for example with equal partition between Q_S and Q_D. The charge expressions for the 50/50 partitioning method are listed below.

(C'') Triode region:

Expressions for the gate charge and the bulk charge are the same as those in Eqs. (4.30) and (4.31), and

$$Q_S=-\frac{1}{2}\,WLC_o\left[V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS}+\frac{(\alpha_x V_{DS})^2}{12\,(V_{GS}-V_{th}-\frac{\alpha_x}{2}V_{DS})}\right]. \tag{4.44}$$

$$Q_D=Q_S\,. \tag{4.45}$$

(D'') Saturation region:

Expressions for the gate charge and the bulk charge are the same as those in Eqs. (4.36) and (4.37), and

$$Q_D = -\frac{1}{3} W L C_o (V_{GS} - V_{th}) , \quad (4.46)$$

$$Q_S = Q_D . \quad (4.47)$$

4.3. The BSIM Capacitance Model

Charge derivatives can be defined as transistor capacitances [4.2].

$$C_{ij} = \delta_{ij} \frac{\partial Qi}{\partial Vi} , \quad \text{and} \quad \delta_{ij} = \begin{cases} 1 & \text{if } i = j \\ -1 & \text{if } i \neq j \end{cases} . \quad (4.48)$$

where i and j stand for g, b, d and s. The factors δ_{ij} are defined so that the C_{ij}'s will normally be positive.

These sixteen transistor capacitances have the following properties. First, if all the terminal voltages are changed by an equal amount, the terminal charges remain the same. This effect of changing all the applied voltages by an equal amount is equivalent to putting an offset on the system ground [4.2]. It can be expressed as

$$\sum_{j=g,b,d,s} C_{ij} = 0 \qquad \text{for } i = g,d,s,b . \quad (4.49)$$

Second, charge neutrality implies that the sum of the terminal capacitive currents is zero. Therefore, the capacitances obey the following identities.

$$C_{gg} + C_{bg} + C_{dg} + C_{sg} = 0 , \quad (4.50)$$

$$C_{gb} + C_{bb} + C_{db} + C_{sb} = 0 , \quad (4.51)$$

$$C_{gd} + C_{bd} + C_{dd} + C_{sd} = 0 , \quad (4.52)$$

$$C_{gs} + C_{bs} + C_{ds} + C_{ss} = 0 . \quad (4.53)$$

The above two conditions put seven constraints on the capacitances. Nine of the capacitances are independent and must be calculated explicitly. Since twelve capacitances are required in the assembly of nodal admittance matrix, the remaining three may be inferred through Eqs. (4.49)-(5.53).

Figure 4.4 shows plots of the four normalized terminal charges with the 40/60 channel-charge partitioning method. Selected plots of MOS transistor capacitances normalized to the total gate-oxide capacitance, C_0WL, are shown in Fig. 4.5 and 4.6. Similar plots of terminal charges and capacitances for the 0/100 and 50/50 channel-charge partitioning methods can be easily obtained, too. Notice that the charges and capacitances are all continuous at the boundary of the triode and the saturation regions. When a transistor is biased in the saturation region, the channel is decoupled from the drain as predicted by long-channel device theories. This decoupling of the drain from the conduction channel results in all partial derivatives with respect to the drain voltage (C_{gd}, C_{bd}, C_{dd} and C_{sd}) to be zero.

As the gate bias increases and reaches the threshold voltage, the transistor channel charge starts to appear and all the 16 capacitances abruptly change in value. The discontinuities in the capacitances are caused by the strong-inversion approximation used in charge formulation. In transient analysis, the discontinuity in capacitances poses no problem because they are multiplied by terms of voltage difference which vanish as convergence is reached [4.2]. However, for small-signal ac analysis, smooth capacitance characteristics are highly desired. A common remedy for the problem of discontinuity in capacitances is to smooth out the capacitance characteristics. This proves to be a non-trivial task because MOS transistor capacitances are functions of more than one voltage. In general, smoothing has to be done on a multi-dimensional basis.

Recently, Tsividis [4.19] proposed to use different models for dc and transient than for small-signal ac analysis. Such approach has several drawbacks. Circuit designers have to deal with multiple sets of transistor parameters in circuit simulation. In addition, the results of a transient simulation of, for example, an operational amplifier in a switched-capacitor integrator, would not agree with the results of the ac simulation [4.20]. Successful modeling work should be able to produce consistent dc,

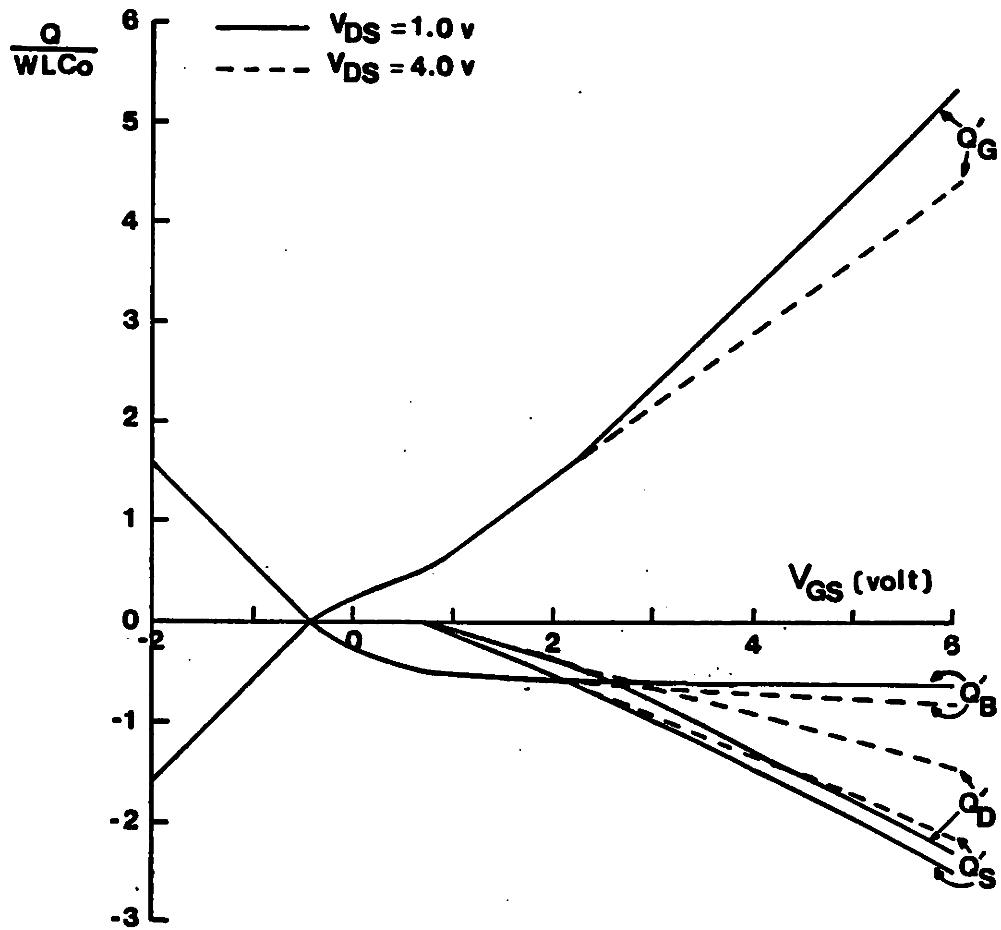


Fig. 4.4 Plots of normalized terminal charges versus gate bias for two drain voltages. The parameters are V_{BS} = 0.0 V, V_{DS} = 1.0 and 4.0 V, a = 1.224, V_{th} = 0.70 V, K_1 = 0.633, ϕ_S = 0.625 V.

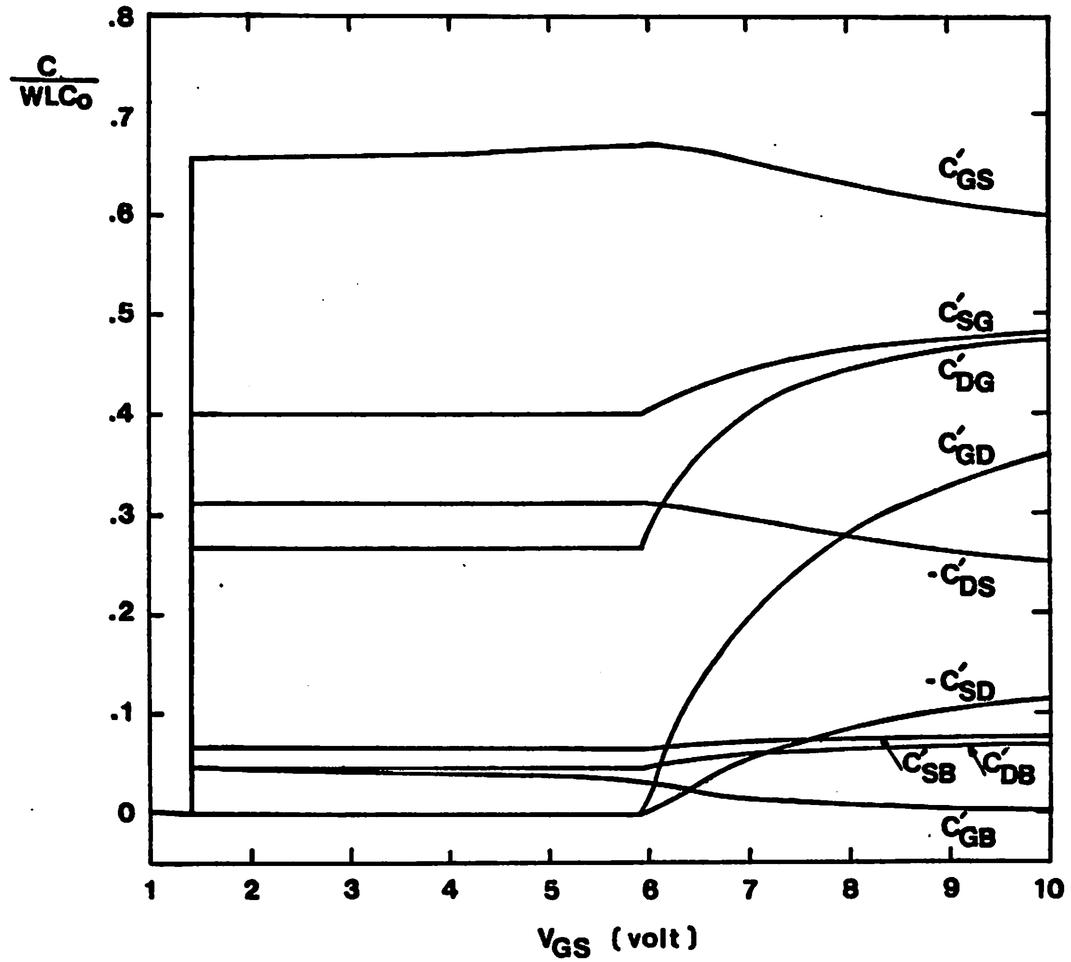


Fig. 4.5 Selected plots of normalized capacitances versus the gate bias. The parameters are V_{BS} = -3.0 V, V_{DS} = 4.0 V, a = 1.131, $V_{th}(V_{BS}$ = -3.0 V)= 1.4 V, K_1 = 0.63 $V^{1/2}$, ϕ_S = 0.62.

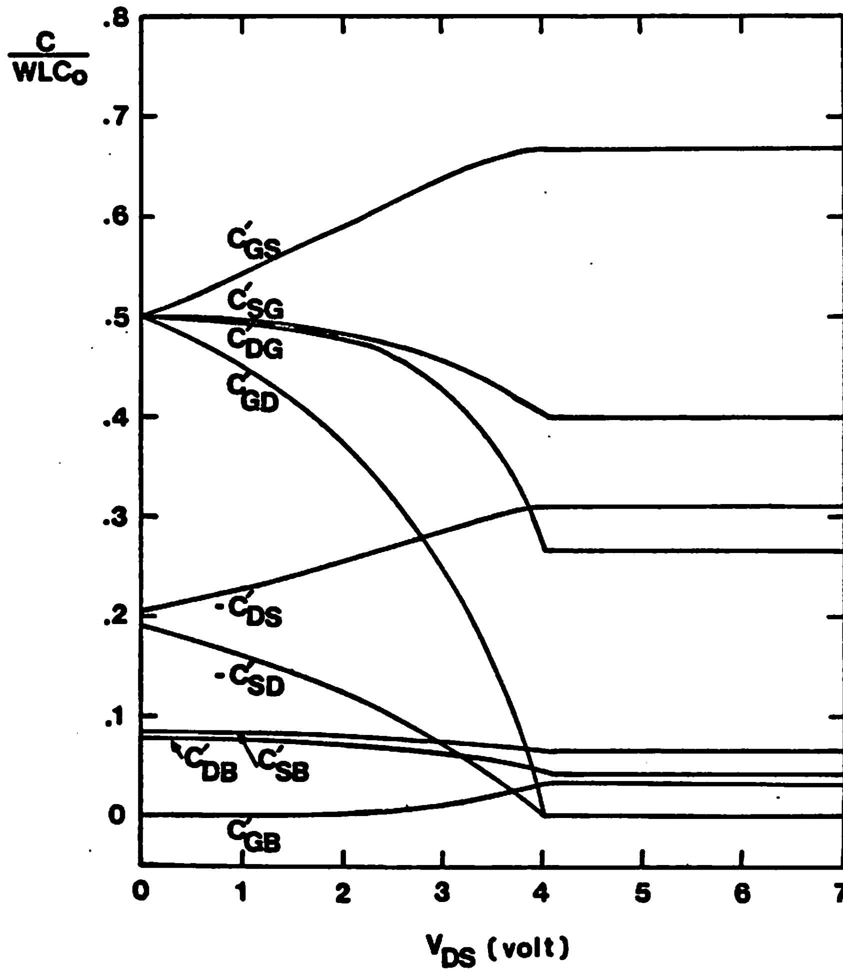


Fig. 4.6 Selected plots of normalized capacitances versus the drain bias. The parameters are $V_{BS} = -3.0$ V, $V_{GS} = 6.0$ V, a = 1.131, $V_{th}(V_{BS} = -3.0\text{ V}) = 1.4$ V, $K_1 = 0.63\ V^{1/2}$, $\phi_S = 0.62$.

transient, and small-signal ac simulation results.

4.4. Comparison with Experimental Results

Measurements of MOS transistor capacitances have been reported [4.2],[4.3] using commercially available LCR meters. The limit of this measurement method is about 1 pF, as was pointed out by Paulos et al. [4.21]. Appendix H describes in detail a newly developed technique to accurately measure gate capacitances of small-geometry MOS transistors.

Figure 4.7 compares calculated results with the measured data given in [4.19] for a long-channel transistor. Good agreement is found.

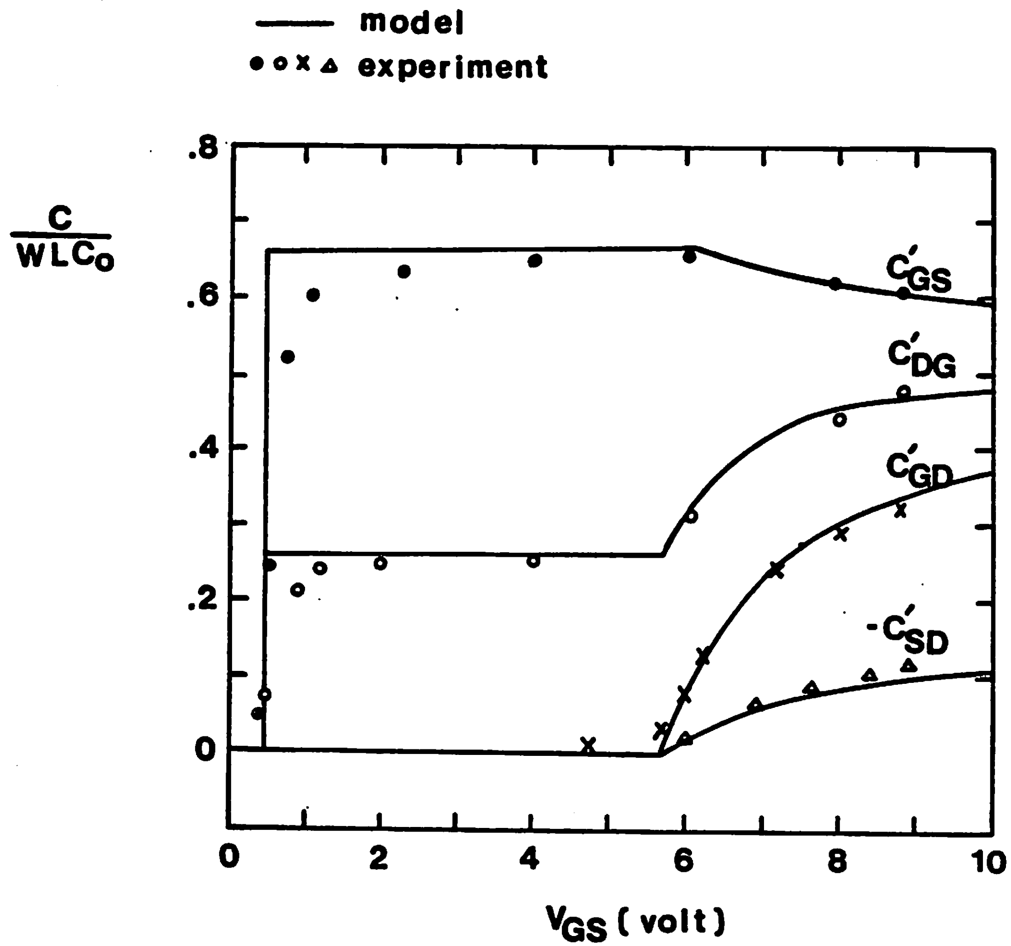


Fig. 4.7 Comparison of several calculated and measured [8] capacitances versus the gate bias with $V_{BS} = 0.0$ V, $V_{DS} = 4.0$ V.

CHAPTER 5

SPICE2 IMPLEMENTATION

5.1. Basic Considerations

It was desired that the addition of BSIM should not affect the execution of the existing SPICE2 MOS transistor models. Therefore, a new linked list was created to store BSIM model parameters. A SPICE2 example with BSIM is shown in Fig. 5.1. To activate BSIM, an MOS transistor is described with "S" as the leading character in place of "M". The transistor card refers to a process file, instead of a model card, for the parameter values.

A model pointer has been added to the resistor and capacitor linked lists. Then, the resistor (or capacitor) value can also be calculated using the data corresponding to the interconnection layer from which it is made. This mimics actual integrated-circuit construction. Whenever the fabrication process is modified, the resistor (or capacitor) value will change according to the new data in the process file.

5.1.1. Process File Format

Figure 5.2 shows the process-file format. A process file consists of two parts: keywords on the first line, and data on the other lines. In a process file, there will be two lines of data associated with each interconnect keyword and 23 lines of data associated with each transistor keyword. The mapping is sequential. For example, data on the third and fourth lines are associated with the first keyword DU1 specified on the first line. A line beginning with "*" is treated as a comment line. At present, there are 14 keywords reserved for interconnect types (DU1 to DU6, PY1 to PY4, ML1 to ML4) and 10 keywords reserved for transistor types (NM1 to NM5, PM1 to PM5).

```
EXAMPLE1 :              CMOS INVERTER
VCC  1  0  5
SMN1  2  3  0  0  PC1_NM1      L=10U  W=50U
SMP1  2  3  1  1  PC1_PM1_DU2  L=10U  W=50U
VIN  4  0  PWL (0 0  5N 5  10N 5  20N 0)
RIN  4  3          PC1_PY1      L=20U  W=60U
C1   2  0  50F
.OPTIONS  NOMOD  RELTOL=1E-5 CHGTOL=1E-16
.TRAN 0.5N 20N
.PRINT TRAN  V(3)  V(2)
.PLOT  TRAN  V(3)  V(2)
.PROCESS PC1 FILENAME=PNMED
.WIDTH OUT=80
.END
```

Fig. 5.1 A SPICE example with BSIM.

```
DU1   DU2   PY1   ML1   NM1   PM1
*N+ DIFFUSION LAYER
35.0    2.5E-4   3.8E-10   1.0E-4   0.8
0.6     0.5      0.33       2.0E-6  0.
*P+ DIFFUSION LAYER
120     3.1E-4   4.7E-10   1.0E-4   0.8
0.6     0.5      0.33       2.0E-6  0.
*POLYSILICON LAYER 1
┌ - - - - - - - - - - - - ┐
|       • • • •           |
|       • • • •           |
└ - - - - - - - - - - - - ┘
*METAL LAYER 1
┌ - - - - - - - - - - - - ┐
|       • • • •           |
|       • • • •           |
└ - - - - - - - - - - - - ┘
*NMOS TRANSISTOR : TYPICAL CASE
┌ - - - - - - - - - -     |
|       • • • •           |
|       • • • •           |
|       • • • •           |
└ - - - - - - - - - - - - ┘
*PMOS TRANSISTOR : FAST CASE
┌ - - - - - - - - - - - - ┐
|       • • • •           |
|       • • • •           |
|       • • • •           |
└ - - - - - - - - - - - - ┘
```

Fig. 5.2 Process file format.

5.1.2. New and Modified Linked Lists

The implementation of BSIM and the process-oriented simulator structure involves a large number of changes in the SPICE2G.6 source code [5.1]. New linked lists are created for the BSIM MOSFET with internal ID = 15 [5.2], transistor process information with internal ID = 25, and interconnection-line process information with internal ID = 26.

Compared to the regular MOSFET linked list in SPICE, there are more entries reserved for the BSIM MOSFET to store the electrical parameters of each individual transistor. Two model pointers are used in the BSIM MOSFET linked list (ID = 15) while only one model pointer is reserved in the regular MOSFET linked list (ID = 14).

A new linked list with ID = 25 is created to store the 69 extracted BSIM process parameters and one of which serves as a flag to choose the channel-charge partitioning method. The model pointer 1 in the BSIM MOSFET linked list (ID = 15) points to the BSIM model linked list (ID = 25) for the intrinsic gate-region information. The model pointer 2 in the BSIM MOSFET linked list (ID = 15) points to the interconnection-line model linked list (ID = 26) for the source and drain junction information. The model pointer in the resistor linked list (ID = 1) or the capacitor linked list (ID = 2) points to the interconnection-line model linked list (ID=26) for resistance or capacitance information.

In the standard SPICE2 implementation, resistor and capacitor elements have no models, hence no pointers; now they have. For such an element two more entries are added to the original linked list, one for the interconnect type and the other for the model pointer. During the read-in stage, SPICE2 stores the identification code for the keyword (PY1, ML1, DU1, etc) appearing on the element card. Later the integer code of the element is used to search for the appropriate model to which the pointer entry of the element can point. The same strategy is used for BSIM MOS transistors. A com-

plete description of the new and modified linked lists is included in Appendix B.

Geometries of resistors, capacitors and MOS transistors are stored in their own linked lists as before. Given their sizes, the resistor and capacitor values are calculated from the corresponding interconnect-layer information in a pre-processing fashion. Electrical parameters for each BSIM MOS transistor are calculated from BSIM process parameters and stored in the linked list of each transistor. This is a one-time data reduction. Since the source and drain junction capacitances of an MOS transistor are bias dependent. They have to be evaluated during each iteration cycle.

5.2. Implementation in SPICE2

5.2.1. Functions of the Newly Added Subroutines

There are 5 new subroutines. Their names and functions are described in the following:

(1) subroutine PROCHK:

This subroutine converts size-independent parameters into electrical parameters for each transistor. It prints out a list of process-file parameters, and single-transistor electrical parameters according to the user's request. Its role is similar to that of MODCHK for SPICE2G.6 MOS LEVEL-1, 2 and 3 models.

(2) subroutine BSIMEQ:

BSIM dc and charge expressions and their derivatives are implemented in this subroutine. Given all the electrical parameters and the terminal voltages of an MOS transistor, this subroutine evaluates the drain current and conductances. It also calculates terminal charges and capacitances for transient and small-signal ac analysis. Its role is equivalent to a combination of subroutines MOSEQ2 and MOSQ2.

(3) subroutine BSIM:

This subroutine processes the MOS devices using the BSIM model for dc and transient analysis. Only the companion BSIM charge and capacitance model is used for the charge-storage effect associated with the thin-oxide region. It is similar to subroutine MOSFET in the regular SPICE2G.6 code.

(4) subroutine BSMCAP:

Given the active-region charge and capacitances from subroutine BSIMEQ and the overlap capacitances and junction capacitances, this subroutine computes the equivalent conductances and complete terminal charges for an BSIM transistor. It is like subroutine MOSCAP.

(5) subroutine FNDTYP:

This subroutine establishes the connection between an element linked list, as that of a resistor, capacitor, or BSIM MOS transistor, and the linked list of corresponding process parameters. It writes the address of the process-parameter linked list to the pointer location of the element linked list. Two keys are used to search for a match: the process name and the model type. It is similar to subroutine FNDNAM in the regular SPICE2G.6 code.

5.2.2. Modifications to the Original Subroutines

Eighteen subroutines in the original SPICE2G.6 code are partially modified. Their names and modifications are described in the following:

ACLOAD	DCTRAN	LOAD	SPICE
ADDELT	ERRCHK	MATLOC	TOPCHK
ALTER	FIND	MATPTR	TRUNC
CARD	GETLIN	NXTCHR	
DCOP	LNKREF	READIN	

(1) subroutine ACLOAD:

The task of initialization and loading of the complex coefficient matrix is extended to include BSIM MOS transistors (ID = 15).

(2) subroutines ADDELT, ALTER, and FIND:

The major changes in these subroutines are made to create linked lists with ID = 15, 25 and 26, and to expand the sizes of the linked lists with ID = 1 and 2.

(3) subroutines CARD, GETLIN:

Changes are made to handle the BSIM process file.

(4) subroutine DCTRAN:

Subroutine BSIM is called by this subroutine. The line "1 + JELCNT(14)", which is near the beginning of transient analysis source code, is changed to "1 + JELCNT(14) + JELCNT(15)".

(5) subroutine DCOP:

The printing of operating-point information is extended to include BSIM MOS transistors.

(6) subroutine ERRCHK:

Changes include translating node initial conditions to device initial conditions for BSIM MOS transistors when UIC is specified on the .TRAN card, and to assign default values for transistor geometries. The added subroutine PROCHK is called by this subroutine.

(7) subroutine LNKREF:

The task of resolving unsatisfied name references is extended to include BSIM MOS transistors. Subroutine FNDTYP is called by this subroutine twice to find addresses for both pointers. This subroutine calls FNDTYP, instead of FNDNAM, to handle resistors and capacitors.

(8) subroutine LOAD:

Subroutine BSIM is called by this subroutine.

(9) subroutines MATPTR, MATLOC and TRUNC:

Changes are made to include BSIM MOS transistors.

(10) subroutine NXTCHR:

The character "_" is also treated as a delimiter.

(11) subroutine READIN:

Many modifications have been made in this subroutine. Variable strings BIDM(25), JPOLAR(24), NPROID(24), JPAR(3), JPBR(2), BMPAR(80), RESLIN(15), and ITYPES(25) are created and initialized to handle the read-in of the BSIM MOS transistor and interconnect parameters. One more entry is added to the string AIDC to recognize the keyword "PROCESS." New input syntax for resistors, capacitors, BSIM MOS devices, and interconnects is included. The keyword "PROCESS" is treated like the keyword "MODEL" except it is used with ID = 25 and 26. This subroutine opens process files and calls subroutine CARD to read the parameters.

(12) main program SPICE:

The line "WRITE (IOFILE,361) NUNODS, NCNODS, NUMNOD, NUMEL, (JELCNT(I), I=11,14)" is changed to "WRITE (IOFILE,361) NUNODS, NCNODS, NUMNOD, NUMEL, (JELCNT(I),I=11,13), 1JELCNT(14) +JELCNT(15)" to correctly count the number of MOS transistors.

(13) subroutine TOPCHK:

The line "1 1HQ,1HJ,1HM,0.0D0,0.0D0,1HT,0.0D0,0.0D0,0.0D0 /" is changed to "1 1HQ,1HJ,1HM,1HS,0.0D0,1HT,0.0D0,0.0D0,0.0D0 /" to include BSIM MOS transistors.

5.3. Program Performance

Experimental results show that the BSIM model reduces the program execution time by a factor of 2 as compared with the popular SPICE2 LEVEL-2 MOSFET model [1.8]. A comparison of selected SPICE2 simulation execution time is listed in Table 5.1.

Table 5.1

A Comparison of Selected SPICE2 Simulation Execution Time		
Circuit Description	BSIM (sec.)	MOS LEV-2 Model (sec.)
Ratioless Dynamic Logic Ckt.	24.50	29.75
Five Stage Inverter Chain	18.30	44.25
MOS Amplifier (dc & ac)	40.02	52.70
MOS Amplifier (transient)	75.08	137.50
One Stage Op-Amp	15.83	70.77
Binary-to-Octal Decorder	262.37	586.28
Telecommunication Ckt.	1784.83	2717.32

CHAPTER 6

CONCLUSION

The Berkeley Short-Channel IGFET Model (BSIM) is an accurate and computationally efficient MOS transistor model. It includes complete expressions for dc drain-current characteristics, capacitance characteristics, and extrinsic-element characteristics, and is therefore suitable for dc, transient, and small-signal circuit analysis. Both the strong-inversion and the weak-inversion current components were included in the drain-current model. For each device type there are 54 size-independent parameters stored in a process file from which the 17 electrical parameters per transistor are derived at the data structure set-up stage of circuit simulation. Nine additional size-independent parameters are needed for the weak-inversion current component. In order to speed up circuit-simulation execution time, the 3/2 power dependence of the drain current on the substrate bias has been replaced by a numerical approximation. This approximation also simplifies the charge expressions.

A dedicated parameter-extraction program has been developed. The local parameter extraction technique, instead of global optimization methods, is employed. The parameter-extraction program is modular, efficient, accurate, flexible, and user-friendly.

The charge model has been intimately derived from its drain-current counterpart. This new model conserves charge and has the non-reciprocal property. Charge conservation is guaranteed by using terminal charges, instead of terminal voltages, as state variables. Expressions for the total stored charges in the gate, bulk, drain, and source are obtained by integrating the distributed charge densities over the active gate region. Proper channel-charge partitioning methods are used to separate the channel charge into the drain and source components. The terminal charges and capacitances are all con-

tinuous at the boundary of the triode and saturation regions. Calculated capacitance characteristics compare well with the measured data.

By using BSIM, substantial improvement in accuracy and simulation time has been achieved. Experimental results show that BSIM reduces the circuit-simulation execution time by a factor of 1.5 to 2 as compared with the widely used LEVEL-2 model provided by SPICE2. The process-file approach used in this model provides a powerful interface between fabrication facilities and circuit simulation. Simulated results of the drain current agree with measured data at various bias conditions for different device sizes and gate-oxide thicknesses. Therefore, the process-oriented BSIM is well suited for circuit analysis and for process monitoring.

Some extensions can make BSIM more suitable for submicron and even sub-half-micron device applications. The source-drain series resistance becomes increasingly important in short-channel devices. Inclusion of the source-drain series resistance in a novel way is essential for submicron devices. The buried-channel structure becomes more prominent in the advanced device design. The enhancement of the drain-current expression to take into account the buried-channel effect is particularly important.

The velocity saturation effect has drastically changed the transistor capacitance characteristics. The present long-channel capacitance model needs to be overhauled to include short-channel effects. In a VLSI chip, around 60% of the silicon area is consumed by interconnection lines. Accurate modeling and parameter extraction of interconnection lines are particularly important. The substrate current, which is a good monitor of hot-electron effects, is the next candidate to be included in advanced circuit simulation models. With a substrate current model available, the circuit designers will have a very powerful tool to tackle the hot-carrier problems in the circuit environment.

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APPENDIX A

BSIM USER GUIDE

****

This is a supplement to the original "SPICE Version 2G User's Guide," and is intended for SPICE users who have access to BSIM (Berkeley Short-channel Igfet Model). It contains descriptions of the various additional device features supported by BSIM and how to activate them. To be complete, it should be used together with the original User's Guide.

****

In addition to the regular resistor and capacitor formats, BSIM also supports resistors and capacitors generated with interconnects.

A.1. Resistors

General form:

RXXXXXXX N1 N2 PNAME_LT L=VAL <W=VAL> <TC=TC1 <,TC2>>

Examples:

R1 1 2 PC1_DU1 L=10U

RC1 12 17 PC1_DU3 L=20U W=4U TC=0.001, 0.015

N1 and N2 are the two element nodes. PNAME is the process name.

LT is the interconnect type. At present, there are fourteen interconnect types available (DU1 to DU6, PY1 to PY4, and ML1 to ML4).

L and W are the resistor length and width, in meters. W should be specified if the default value in the process file is not to be used.

TC1 and TC2 are the (optional) temperature coefficients; if not specified, zero is

assumed for both. The value of the resistor as a function of temperature is given by:

value(TEMP) = value(TNOM)*(1+TC1*(TEMP-TNOM)+TC2*(TEMP-TNOM)**2))

A.2. Capacitors

General form:

CXXXXXXX N1 N2 PNAME_LT L=VAL <W=VAL>

Examples:

CBYP 13 0 PC1_PY1 L=20U

COSC 17 23 PC1_ML2 L=30U W=30U IC=3V

N1 and N2 are the two element nodes. PNAME is the process name.

LT is the interconnect type. At present, there are fourteen interconnect types available (DU1 to DU6, PY1 to PY4, and ML1 to ML4).

L and W are the capacitor length and width, in meters. W should be specified if the default value in the process file is not to be used.

The (optional) initial condition is the initial (time-zero) value of capacitor voltage (in volts).

[Note that the initial conditions (if any) apply 'only' if the UIC option is specified on the .TRAN card.]

A.3. BSIM MOSFET's

General form:

SXXXXXXX ND NG NS NB PNAME_MT_DT<_STHD> <L=VAL> <W=VAL>

+ <AD=VAL> <AS=VAL> <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL>

+ <OFF> <IC=VDS,VGS,VBS>

Examples:

S1 24 2 0 20 PC1_NM1

S31 2 17 6 10 PC2_NM2_DU2_STHD L=5U W=2U

S31 2 16 6 10 PC2_PM1_DU3 5U 2U

S1 2 9 3 0 PC2_PM2_DU3 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

S1 2 9 3 0 PC1_NM1_STHD 10U 5U 2P 2P

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively.

PNAME is the process name.

MT is the device type. At present, there are five device types for both N-channel and P-channel transistors (NM1 to NM5, and PM1 to PM5).

DT is the diffusion type to be used for the source/drain junctions. There are six diffusion types available (DU1 to DU6). The default is DU1 for N-channel transistors and DU2 for P-channel transistors.

STHD is used as a flag. If it is specified, the weak-inversion current characteristic will be included.

L and W are the channel length and width, in meters.

AD and AS are the areas of the drain and source diffusions, in sq-meters.
[Note that the suffix U specifies microns (1E-6 m) and P sq-microns (1E-12 sq-m). If any of L, W, AD, or AS are not specified, default values are used. The user may specify the values to be used for these default parameters on the .OPTIONS card. The use of defaults simplifies input deck preparation, as well as the editing required if device geometries are to be changed.]

PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .process card for an accurate representation of the series drain and source resistance components of each transistor.
[PD, PS, NRD, and NRS all default to 0.0. OFF indicates an (optional) initial condition on the device for dc analysis. The (optional) initial condition specification using IC=VDS,VGS,VBS is intended for use with the UIC option on the .TRAN card, when a

transient analysis is desired starting from other than the quiescent operating point. See the .IC card for a better and more convenient way to specify transient initial conditions.]

IV. .PROCESS Card

General form:

.PROCESS PNAME FILENAME=FNAME

Examples:

.PROCESS PC1 FILENAME=PNMED

.PROCESS PD2 FILENAME=FAST

The .PROCESS card specifies process parameter values that will be used by one or more devices.

PNAME is the process name, and FNAME is the name of the file containing the process parameter values. Special rules have to be observed in choosing FNAME. The leading character of FNAME should be alphabetical. Alphabetical characters will be recognized only in the capital form. Totally no more than 8 characters are allowed.
The process card is used together with resistors, capacitors, as well as MOS transisors.

A.5. Process File

This file is generated by the automated characterization program, and it contains the process information for the transistors as well as for the interconnects. For transistors, the L (channel-length) and W (channel-width) sensitivity factors of a basic electrical parameter are denoted by appending the italic characters '*l*' and '*w*' to the name of the parameter. For the example of the basic parameter V_{FB} (flat-band voltage), there are two corresponding sensitivity factors, V_{FBl}, V_{FBw}. If P_0 is the basic parameter and P_L and P_W are the corresponding L and W sensitivity factors. The formula

$$P = P_0 + \frac{P_L}{L_{eff}} + \frac{P_W}{W_{eff}}$$

is used to obtained the value for each transistor size with both L_{eff} (= L_{MK} - ΔL) and W_{eff} (= W_{MK} - ΔW) in μm.

(a) The format of the process parameters is listed below:

TRANSISTORS

	name	L sens. factor	W sens. factor	units of basic parameter
1	V_{FB} (VFB)	V_{FBl} (LVFB)	V_{FBw} (WVFB)	V
2	ϕ_S (PHI)	ϕ_{Sl} (LPHI)	ϕ_{Sw} (WPHI)	V
3	K_1 (K1)	K_{1l} (LK1)	K_{1w} (WK1)	$V^{1/2}$
4	K_2 (K2)	K_{2l} (LK2)	K_{2w} (WK2)	-
5	η_0 (ETA)	η_{0l} (LETA)	η_{0w} (WETA)	-
6	μ_Z (MUZ)	δ_l (DL)	δ_w (DW)	$cm^2/V{-}s$(μm , μm)
7	U_{0Z} (U0)	U_{0Zl} (LU0)	U_{0Zw} (WU0)	V^{-1}
8	U_{1Z} (U1)	U_{1Zl} (LU1)	U_{1Zw} (WU1)	$\mu m\ V^{-1}$
9	μ_{ZB} (X2MZ)	μ_{ZBl} (LX2MZ)	μ_{ZBw} (WX2MZ)	$cm^2/V^2{-}s$
10	η_B (X2E)	η_{Bl} (LX2E)	η_{Bw} (WX2E)	V^{-1}
11	η_D (X3E)	η_{Dl} (LX3E)	η_{Dw} (WX3E)	V^{-1}
12	U_{0B} (X2U0)	U_{0Bl} (LX2U0)	U_{0Bw} (WX2U0)	V^{-2}
13	U_{1B} (X2U1)	U_{1Bl} (LX2U1)	U_{1Bw} (WX2U1)	$\mu m\ V^{-2}$
14	μ_S (MUS)	μ_{Sl} (LMS)	μ_{Sw} (WMS)	$cm^2/V^2{-}s$
15	μ_{SB} (X2MS)	μ_{SBl} (LX2MS)	μ_{SBw} (WX2MS)	$cm^2/V^2{-}s$
16	μ_{SD} (X3MS)	μ_{SDl} (LX3MS)	μ_{SDw} (WX3MS)	$cm^2/V^2{-}s$
17	U_{1D} (X3U1)	U_{1Dl} (LX3U1)	U_{1Dw} (WX3U1)	$\mu m\ V^{-2}$
18	T_{ox} (TOX)	T_{emp} (TEMP)	V_{dd} (VDD)	μm (^0C . V)

19	CGDO	CGSO	CGBO	F/m
20	XPART	DUM1	DUM2	-
21	N0	LN0	WN0	-
22	NB	LNB	WNB	-
23	ND	LND	WND	-

INTERCONNECTS

1	Rsh (RSH)	Cj (CJ)	Cjw (CJW)	Ijs (IJS)	Pj (PJ)
2	P_{jw} (PJW)	Mj (MJ)	Mjw (MJW)	Wdf (WDF)	δ_l (DL)

(b) The names of the process parameters of transistors are listed below:

V_{FB}	flat-band voltage
ϕ_S	surface inversion potential
K_1	body effect coefficient
K_2	drain/source depletion charge sharing coefficient
η_0	zero-bias drain-induced barrier lowering coefficient
μ_Z	zero-bias mobility
U_{0Z}	zero-bias transverse-field mobility degradation coefficient
U_{1Z}	zero-bias velocity saturation coefficient
μ_{ZB}	sensitivity of mobility to the substrate bias at $V_{ds} = 0$
η_B	sensitivity of drain-induced barrier lowering effect to the substrate bias
η_D	sensitivity of drain-induced barrier lowering effect to the drain bias, at $V_{ds} = V_{dd}$

U_{0B}	sensitivity of transverse-field mobility degradation effect to the substrate bias
U_{1B}	sensitivity of velocity saturation effect to the substrate bias
μ_S	mobility at zero substrate bias and at V_{ds}=V_{dd}
μ_{SB}	sensitivity of mobility to the substrate bias at $V_{ds} = V_{dd}$
μ_{SD}	sensitivity of mobility to the drain bias at $V_{ds} = V_{dd}$
U_{1D}	sensitivity of velocity saturation effect to the drain bias, at $V_{ds}= V_{dd}$
T_{ox}	gate-oxide thickness
T_{emp}	temperature at which the process parameters are measured
V_{dd}	measurement bias range
N0	zero-bias subthreshold slope coefficient
NB	sensitivity of subthrehold slope to the substrate bias
ND	sensitivity of subthrehold slope to the drain bias
CGDO	gate-drain overlap capacitance per meter channel width
CGSO	gate-source overlap capacitance per meter channel width
CGBO	gate-bulk overlap capacitance per meter channel length
XPART	gate-oxide capacitance model flag

Note: XPART= 0, 0.5, and 1 selects the 40/60, 50/50, and 0/100 channel-charge partitioning methods, respectively.

The names of the process parameters of diffusion layers are listed below:

sheet resistance/square	Rsh	Ω/square
zero-bias bulk junction bottom capacitance/unit area	Cj	F/m^2

zero-bias bulk junction sidewall capacitance/unit length	Cjw	F/m
bulk junction saturation current/unit area	Ijs	A/m^2
bulk junction bottom potential	Pj	V
bulk junction sidewall potential	Pjw	V
bulk junction bottom grading coefficient	Mj	-
bulk junction sidewall grading coefficient	Mjw	-
default width of the layer	Wdf	m
average reduction of size due to side etching or mask compensation	δ_s	m

---

The names of the process parameters of poly and metal layers are listed as following:

sheet resistance/square	Rsh	Ω/square
capacitance/unit area	Cj	F/m^2
edge capacitance/unit length	Cjw	F/m
default width of the layer	Wdf	m
average variation of size due to side etching or mask compensation	δ_l	m

A.6. Examples

(a) The following is an example of a process file. The lines starting with "*" are used as comments.

```
NM1 PY1 ML1 ML2 DU1 DU2
*PROCESS=PC1
*RUN=12 medium-size devices
*OPERATOR=Bing
*DATE=07/16/85
*
*   NMOS-1 PARAMETERS
*
-1.0087E+000,   -2.1402E-001,   3.44354E-001
7.96434E-001,   0.00000E+000,   0.00000E+000
1.31191E+000,   3.23395E-001,   -5.7698E-001
1.46640E-001,   1.68585E-001,   -1.8796E-001
-1.0027E-003,   -9.4847E-003,   1.47316E-002
5.34334E+002,   7.97991E-001,   4.77402E-001
4.38497E-002,   6.38105E-002,   -6.1053E-002
-5.7332E-002,   1.01174E+000,   1.62706E-002
8.25434E+000,   -2.4197E+001,   1.95696E+001
-7.6911E-004,   9.62411E-003,   -3.7951E-003
7.86777E-004,   7.35448E-004,   -1.7796E-003
1.06821E-003,   -8.0958E-003,   4.03379E-003
-1.9209E-002,   -7.4573E-002,   1.47520E-002
5.40612E+002,   6.21401E+002,   -1.9190E+002
```

```
-1.2992E+001,   -6.4900E+001,   4.29043E+001
-9.4035E+000,   1.18239E+002,   -2.9747E+001
7.76925E-003,   -1.0940E-001,   -8.3353E-003
3.00000E-002,   2.70000E+001,   5.00000E+000
2.70000E-010,   2.70000E-010,   1.40000E-010
1.0,            0.0,            0.0
1.5,5           0.0,            0.0
0.09,           0.0,            0.0
0.0,            0.0,            0.0
*
*  poly layer-1
*
30.0,           7.0E-5,         0.0,        0.0,    0.0
0.0,            0.0,            0.0,        0.0,    0.0
*
*  metal layer-1
*
0.040,          2.60E-5,        0.0,        0.0,    0.0
0.0,            0.0,            0.0,        0.0,    0.0
*
*  metal layer-2 (top metal)
*
0.030,          1.3E-5,         0.0,        0.0,    0.0
0.0,            0.0,            0.0,        0.0,    0.0
*
*  n+ diffusion layer
*
```

```
35.0,       2.75E-4,    1.90E-10,   1.0E-8,   0.7
0.8,        0.5,        0.33,       0.0,      0.0
*
* p+ diffusion layer
*
120.0,      3.1E-4,     3.0E-010,   1.0E-8,   0.7
0.8,        0.5,        0.33,       0.0,      0.0
```

(b) The following deck determines the transient characteristics of a resistive load inverter with a capacitor connected at the output node.

```
SAMPLE CMOS INVERTER
VCC  1  0  5
SMN1  2  3  0  0  PC1_NM1_DU1  W=50U L=10U
SMP1  2  3  1  1  PC1_PM1_DU2  W=50U L=10U
VIN  4  0  PWL (0 0  5N 5  10N 5  20N 0)
RIN  4  3  PC1_PY1  L=20U  W=60U
C1  2  0  50FF
.OPTIONS  RELTOL=1E-5  CHGTOL=1E-15
.TRAN  0.5N  20N
.PRINT TRAN  V(3)  V(2)
.PLOT TRAN  V(3)  V(2)
.PROCESS PC1 FILENAME=CM0716
.WIDTH OUT=80
.END
```

Appendix B

LINKED LIST SPECIFICATIONS

B.1. Resistor (ID=1)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: element name
	+1: LOCV		+1: g (TEMP)
	+2: n1		+2: r (TNOM)
	+3: n2		+3: temp.coef. 1
	+4: (n1,n2)		+4: temp.coef. 2
	+5: (n2,n1)		+5: length
	+6: (n1,n1)		+6: width
	+7: (n2,n2)		
	+8: model type		
	+9: model pointer		
	+10: cycle number		

B.2. Capacitor (ID=2)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: element name
	+1: LOCV		+1: computed element value
	+2: n1		+2: initial condition
	+3: n2		+3: argument vector
	+4: function code		+4: length
	+5: (n1,n2)		+5: width
	+6: (n2,n1)		
	+7: tp (function coefficients)		
	+8: LXi offset	LXi	+0: q(capacitor)
	+9: exponent vector		+1: i(capacitor)
	+10: (n1,n1)		
	+11: (n2,n2)		
	+12: model type		
	+13: model pointer		
	+14: cycle number		

B.3. BSIM MOS Device (ID=15)

	-1: subckt info			
LOC	+0: next pointer	LOCV	+0: element name	
	+1: LOCV		+1: effective length	
	+2: nd		+2: effective width	
	+3: ng		+3: drain diffusion area	
	+4: ns		+4: source diffusion area	
	+5: nb		+5: IC: vds	
	+6: nd'		+6: IC: vgs	
	+7: ns'		+7: IC: vbs	
	+8: model pointer 1		+8: device mode	
	+9: off		+9: von	
	+10: (nd,nd')		+10: vdsat	
	+11: (ng,nb)		+11: drain perimeter	
	+12: (ng,nd')		+12: source perimeter	
	+13: (ng,ns')		+13: # square of drain diff.	
	+14: (ns,ns')		+14: # square of source diff.	
	+15: (nb,ng)		+15: vto	
	+16: (nb,nd')		+16: XPART	
	+17: (nb,ns')		+17: VFB	
	+18: (nd',nd)		+18: PHI	
	+19: (nd',ng)		+19: K1	
	+20: (nd',nb)		+20: K2	
	+21: (nd',ns')		+21: ETA	
	+22: (ns',ng)		+22: BETAZ	
	+23: (ns',ns)		+23: U0	
	+24: (ns',nb)		+24: U1	
	+25: (ns',nd')		+25: X2BZ	
	+26: LXi offset		+26: X2E	
	+27: (nd,nd)		+27: X3E	
	+28: (ng,ng)		+28: X2U0	
	+29: (ns,ns)		+29: X2U1	
	+30: (nb,nb)		+30: BETAS	
	+31: (nd',nd')		+31: X2BS	
	+32: (ns',ns')		+32: X3BS	
	+33: model type 1		+33: X3U1	
	+34: model pointer 2		+34: COVLGD	+37: N0
	+35: model type 2		+35: COVLGS	+38: NB
	+36: cycle number		+36: COVLGB	+39: ND

Lxi		
	+0: VBDO	+16: QD
	+1: VBSO	+17: iQD
	+2: VGSO	+18: CGGBO
	+3: VDSO	+19: CGDBO
	+4: id	+20: CGSBO
	+5: ibs	+21: CBGBO
	+6: ibd	+22: CBDBO
	+7: gm	+23: CBSBO
	+8: gds	+24: QBD
	+9: gmbs	+25: iQBD
	+10: gbd	+26: QBS
	+11: gbs	+27: iQBS
	+12: QB	+28: CDGBO
	+13: iQB	+29: CDDBO
	+14: QG	+30: CDSBO
	+15: iQG	

Comments :

(1) vto=VFB+PHI+K1* $\sqrt{PHI}$ -K2*PHI

(2) device mode: +1(-1) for normal(inverse).

(3) If RSH $\neq$0.0D0, and NRD $\neq$0.0D0

then at LOCV+13: GDPR=1.0D0/(RSH*NRD)

If RSH $\neq$0.0D0, and NRS $\neq$0.0D0

then at LOCV+14: GDPR=1.0D0/(RSH*NRS)

B.4. BSIM Model (ID=25)

LOC	-1: subckt info	+1: LOCV		
	+0: next pointer	+2: device type		
LOCV	+0: process name			
	+1: VFB	+22: U1	+43: X2MS	+64: NB
	+2: LVFB	+23: LU1	+44: LX2MS	+65: LNB
	+3: WVFB	+24: WU1	+45: WX2MS	+66: WNB
	+4: PHI	+25: X2MZ	+46: X3MS	+67: ND
	+5: LPHI	+26: LX2MZ	+47: LX3MS	+68: LND
	+6: WPHI	+27: WX2MZ	+48: WX3MS	+69: WND
	+7: K1	+28: X2E	+49: X3U1	
	+8: LK1	+29: LX2E	+50: LX3U1	
	+9: WK1	+30: WX2E	+51: WX3U1	
	+10: K2	+31: X3E	+52: TOX	
	+11: LK2	+32: LX3E	+53: TEMP	
	+12: WK2	+33: WX3E	+54: VDD	
	+13: ETA	+34: X2U0	+55: CGDO	
	+14: LETA	+35: LX2U0	+56: CGSO	
	+15: WETA	+36: WX2U0	+57: CGBO	
	+16: MUZ	+37: X2U1	+58: XPART	
	+17: DL	+38: LX2U1	+59: DUM1	
	+18: DW	+39: WX2U1	+60: DUM2	
	+19: U0	+40: MUS	+61: N0	
	+20: LU0	+41: LMS	+62: LN0	
	+21: WU0	+42: WMS	+63: WN0	

Comments :

(1) device type:

1 for NMOS

-1 for PMOS

(2) XPART:

1 for the 0/100 channel-charge partitioning method.

0 for the 40/60 channel-charge partitioning method.

0.5 for the 50/50 channel-charge partitioning method.

B.5. Interconnect Model (ID=26)

	-1: subckt info		
LOC	+0: next pointer	LOCV	+0: process name
	+1: LOCV		+1: RSH
	+2: interconnect type		+2: CJ
			+3: CJW
			+4: IJS
			+5: PJ
			+6: PJW
			+7: MJ
			+8: MJW
			+9: WDF
			+10: DL

Comments :

(1) interconnect type:

1, 2, 3, 4, 5, and 6 for DU1, DU2, DU3, DU4, DU5, and DU6.

7, 8, 9, and 10 for PY1, PY2, PY3, and PY4.

11, 12, 13, and 14 for ML1, ML2, ML3, and ML4.

APPENDIX C

The Transistor Small-Signal Model and Extrinsic Component Models

C.1. The Transistor Small-Signal Model

Four transistor model parameters, V_{FB} , ϕ_S , K_1 ,and K_2 are bias-independent, while the other four bias-dependent parameters, U_0 , U_1 , η , and β_0 ($\equiv$mu0C_oW/L) can be expressed as:

$$U_0 = U_{0Z} + U_{0B}\, V_{BS} \tag{C.1}$$

$$U_1 = U_{1Z} + U_{1B}\, V_{BS} + U_{1D}\,(\, V_{DS} - V_{DD}\,) \tag{C.2}$$

$$\eta = \eta_Z + \eta_B\, V_{BS} + \eta_D\,(\, V_{DS} - V_{DD}\,) \tag{C.3}$$

β_0 is treated in a different way. It is obtained by the quadratic interpolation through three data, β_0 at $V_{DS} = 0$, β_0 at $V_{DS} = V_{DD}$, and the sensitivity of β_0 to V_{DS} at $V_{DS} = V_{DD}$.

First, β_0 and the derivatives are calculated.

$$X_T = \beta_Z + \beta_{ZB}\, V_{BS} \tag{C.4}$$

$$X_A = \beta_S + \beta_{SB}\, V_{BS} \tag{C.5}$$

$$X_B = \beta_{SD} \tag{C.6}$$

(1) For $V_{DS} \leqslant V_{DD}$:

$$\beta_0 = C_1 \cdot V_{DS}^2 + C_2 \cdot V_{DS} + X_T \tag{C.7}$$

where

$$C_2 = \frac{2\,(\, X_A - X_T\,)}{V_{DD}} - X_B \tag{C.8}$$

$$C_1 = \frac{X_B\, V_{DD} - X_A + X_T}{V_{DD}^2} \tag{C.9}$$

and

$$\frac{\partial \beta_0}{\partial V_{DS}} = 2\, C_1 \cdot V_{DS} + C_2 \tag{C.10}$$

$$\frac{\partial \beta_0}{\partial V_{BS}} = V_{DS}^2 \cdot + V_{DS} \cdot \frac{\partial C_2}{\partial V_{BS}} + \beta_{ZB} \tag{C.11}$$

where

$$\frac{\partial C_1}{\partial V_{BS}} = \frac{\beta_{ZB} - \beta_{SB}}{V_{DD}^2} \tag{C.12}$$

$$\frac{\partial C_2}{\partial V_{BS}} = \frac{2\,(\,\beta_{SB} - \beta_{ZB}\,)}{V_{DD}} \tag{C.13}$$

(2) For $V_{DS} > V_{DD}$:

Linear extrapolation is used for this bias range.

$$\beta_0 = X_A + X_B\,(\,V_{DS} - V_{DD}\,) \tag{C.14}$$

and

$$\frac{\partial \beta_0}{\partial V_{DS}} = X_B \tag{C.15}$$

$$\frac{\partial \beta_0}{\partial V_{BS}} = \beta_{SB} \tag{C.16}$$

Second, β and the derivatives are obtained.

Let

$$Arg = 1 + U_0\,(\,V_{GS} - V_{th}\,) \tag{C.17}$$

Then,

$$\beta = \frac{\beta_0}{Arg} \tag{C.18}$$

and

$$\frac{\partial \beta}{\partial V_{GS}} = -\frac{\beta \cdot U_0}{Arg} \tag{C.19}$$

$$\frac{\partial \beta}{\partial V_{DS}} = \frac{\dfrac{\partial \beta_0}{\partial V_{DS}}}{Arg} - \frac{\partial \beta}{\partial V_{GS}} \cdot \frac{\partial V_{th}}{\partial V_{DS}} \tag{C.20}$$

$$\frac{\partial \beta}{\partial V_{BS}} = \frac{\dfrac{\partial \beta_0}{\partial V_{BS}}}{Arg} + \frac{\beta \cdot U_0}{Arg} \cdot \frac{\partial V_{th}}{\partial V_{BS}} - \frac{\beta\,(\,V_{GS} - V_{th}\,)\,U_{0B}}{Arg} \tag{C.21}$$

where

$$\frac{\partial V_{th}}{\partial V_{DS}} = -\eta - \eta_D \cdot V_{DS} \tag{C.22}$$

$$\frac{\partial V_{th}}{\partial V_{BS}} = -0.5\,\frac{K_1}{\sqrt{\phi_S - V_{BS}}} + K_2 - \eta_B \cdot V_{DS} \tag{C.23}$$

C.1.1. Transconductance, Output Conductance, and Back-Gate Transconductance

$$\frac{\partial a}{\partial V_B} = \frac{K_1}{2\sqrt{\phi_s - V_{BS}}} \left[\frac{g}{2\,(\,\phi_s - V_{BS}\,)} - 0.8364(\,1 - g\,)^2 \right] \tag{C.24}$$

Scale U_1 and its components by channel length L.

$$U_{1L} = \frac{U_1}{L} \tag{C.25}$$

$$\frac{\partial U_{1L}}{\partial V_{DS}} = \frac{U_{1D}}{L} \tag{C.26}$$

$$\frac{\partial U_{1L}}{\partial V_{BS}} = \frac{U_{1B}}{L} \tag{C.27}$$

(1) Triode Region:

Let

$$Larg1 = 1 + U_{1L}\,V_{DS} \tag{C.28}$$

$$Larg2 = V_{GS} - V_{th} - \frac{a\,V_{DS}}{2} \tag{C.29}$$

Then,

$$g_m = \frac{Larg2 \cdot V_{DS} \frac{\partial \beta}{\partial V_{GS}} + \beta V_{DS}}{Larg1} \quad (C.30)$$

$$g_d = \frac{Larg2 \cdot V_{DS} \frac{\partial \beta}{\partial V_{DS}} + \beta (V_{GS} - V_{th} - V_{DS} \cdot \frac{\partial V_{th}}{\partial V_{DS}} - a V_{DS})}{Larg1}$$

$$- \frac{I_{DS} \cdot (V_{DS} \frac{\partial U_{1L}}{\partial V_{DS}} + U_{1L})}{Larg1} \quad (C.31)$$

$$g_{mb} = \frac{Larg2 \cdot V_{DS} \frac{\partial \beta}{\partial V_{BS}} + \beta V_{DS} (- \frac{\partial V_{th}}{\partial V_{BS}} - \frac{V_{DS}}{2} \cdot \frac{\partial a}{\partial V_{BS}}) - I_{DS} \cdot V_{DS} \frac{\partial U_{1L}}{\partial V_{BS}}}{Larg1} \quad (C.32)$$

(2) Saturation Region:

$$v_c = \frac{U_1 (V_{GS} - V_{th})}{a} \quad (C.33)$$

$$Sarg = \sqrt{1+2 v_c} \quad (C.34)$$

$$K = \frac{1 + v_c + Sarg}{2} \quad (C.35)$$

$$Sarg1 = 1 + \frac{1}{Sarg} \quad (C.36)$$

$$\frac{\partial v_c}{\partial V_{GS}} = \frac{U_1}{a} \quad (C.37)$$

$$\frac{\partial v_c}{\partial V_{DS}} = \frac{(V_{GS} - V_{th}) \frac{\partial U_{1L}}{\partial V_{DS}}}{a} - \frac{\partial v_c}{\partial V_{GS}} \cdot \frac{\partial V_{th}}{\partial V_{DS}} \quad (C.38)$$

$$\frac{\partial v_c}{\partial V_{BS}} = \frac{(V_{GS} - V_{th}) \frac{\partial U_{1L}}{\partial V_{BS}} - U_{1L} [\frac{\partial V_{th}}{\partial V_{BS}} + \frac{(V_{GS} - V_{th})}{a} \frac{\partial a}{\partial V_{BS}}]}{a} \quad (C.39)$$

$$\frac{\partial K}{\partial v_c} = \frac{Sarg1}{2} \tag{C.40}$$

$$\frac{\partial K}{\partial V_{GS}} = \frac{\partial K}{\partial v_c} \cdot \frac{\partial v_c}{\partial V_{GS}} \tag{C.41}$$

$$\frac{\partial K}{\partial V_{DS}} = \frac{\partial K}{\partial v_c} \cdot \frac{\partial v_c}{\partial V_{DS}} \tag{C.42}$$

$$\frac{\partial K}{\partial V_{BS}} = \frac{\partial K}{\partial v_c} \cdot \frac{\partial v_c}{\partial V_{BS}} \tag{C.43}$$

Let

$$Sarg2 = \frac{(V_{GS} - V_{th})}{a \cdot K} \tag{C.44}$$

$$Sarg3 = Sarg2 \cdot (V_{GS} - V_{th}) \tag{C.45}$$

Then,

$$g_m = \frac{Sarg3}{2} \cdot \frac{\partial \beta}{\partial V_{GS}} + \beta \cdot Sarg2 - \frac{I_{DS}}{K} \cdot \frac{\partial K}{\partial V_{GS}} \tag{C.46}$$

$$g_d = \frac{Sarg3}{2} \cdot \frac{\partial \beta}{\partial V_{DS}} - \beta \cdot Sarg2 \cdot \frac{\partial V_{th}}{\partial V_{DS}} - \frac{I_{DS}}{K} \cdot \frac{\partial K}{\partial V_{DS}} \tag{C.47}$$

$$g_{mb} = \frac{Sarg3}{2} \cdot \frac{\partial \beta}{\partial V_{BS}} - \beta \cdot Sarg2 \cdot \frac{\partial V_{th}}{\partial V_{BS}} - I_{DS} \left(\frac{1}{a} \cdot \frac{\partial a}{\partial V_{BS}} + \frac{1}{K} \cdot \frac{\partial K}{\partial V_{BS}} \right) \tag{C.48}$$

C.1.2. Transistor Capacitances

Capacitance expressions corresponding to the 40/60 channel-charge partitioning method are listed in the following. Capacitance expressions for other partitioning methods can be obtained in a similar way.

$$V_{th0} = V_{FB} + \phi_s + K_1 \sqrt{\phi_s - V_{BS}} \tag{C.49}$$

$$\frac{\partial V_{th0}}{\partial V_B} = - \frac{K_1}{2\sqrt{\phi_s - V_{BS}}} \tag{C.50}$$

Let

$$E_{nt} = V_{GS} - V_{th} - \frac{a\, V_{DS}}{2} \tag{C.51}$$

$$V_{GST} = V_{GS} - V_{th} \tag{C.52}$$

$$V_{COM} = \frac{1}{6} V_{GST}^2 - \frac{1}{8} a\, V_{DS} \cdot V_{GST} + \frac{a^2\, V_{DS}^2}{40} \tag{C.53}$$

$$C_{ox} = C_o \cdot W_{eff} \cdot L_{eff} \tag{C.54}$$

Then,

$$\frac{\partial E_{nt}}{\partial V_G} = 1 \tag{C.55}$$

$$\frac{\partial E_{nt}}{\partial V_D} = -\frac{a}{2} \tag{C.56}$$

$$\frac{\partial E_{nt}}{\partial V_B} = -\frac{\partial V_{th0}}{\partial V_B} - \frac{V_{DS}}{2} \cdot \frac{\partial a}{\partial V_B} \tag{C.57}$$

$$Q_g = \frac{Q_G}{C_{ox}}\ ,\ Q_s = \frac{Q_S}{C_{ox}}\ ,\ Q_d = \frac{Q_D}{C_{ox}}\ ,\ \text{and}\ \ Q_b = \frac{Q_B}{C_{ox}} \tag{C.58}$$

(1) Triode Region:

(i) Q_g:

$$\frac{\partial Q_g}{\partial V_G} = 1 + \frac{a\, V_{DS}^2}{12\, E_{nt}^2} \tag{C.59}$$

$$\frac{\partial Q_g}{\partial V_D} = -\frac{1}{2} + \frac{a\, V_{DS}}{6\, E_{nt}} - \frac{a\, V_{DS}^2}{12\, E_{nt}^2} \cdot \frac{\partial E_{nt}}{\partial V_D} \tag{C.60}$$

$$\frac{\partial Q_g}{\partial V_B} = \frac{V_{DS}^2}{12\, E_{nt}} \cdot \frac{\partial a}{\partial V_B} - \frac{a\, V_{DS}^2}{12\, E_{nt}^2} \cdot \frac{\partial E_{nt}}{\partial V_B} \tag{C.61}$$

$$\frac{\partial Q_g}{\partial V_S} = -\left[\ \frac{\partial Q_g}{\partial V_G} + \frac{\partial Q_g}{\partial V_D} + \frac{\partial Q_g}{\partial V_B}\ \right] \tag{C.62}$$

(ii) Q_b:

$$\frac{\partial Q_b}{\partial V_G} = \frac{a(1-a)V_{DS}^2}{12 E_{nt}^2} \tag{C.63}$$

$$\frac{\partial Q_b}{\partial V_D} = \frac{1-a}{2} - \frac{a(1-a)V_{DS}}{6 E_{nt}} + \frac{a(1-a)V_{DS}^2}{12 E_{nt}^2} \cdot \frac{\partial E_{nt}}{\partial V_D} \tag{C.64}$$

$$\frac{\partial Q_b}{\partial V_B} = - \frac{\partial V_{th0}}{\partial V_B} - \frac{V_{DS}}{2} \frac{\partial a}{\partial V_B} - V_{DS}^2 \left(\frac{(1-2a)}{12 E_{nt}} \cdot \frac{\partial a}{\partial V_B} - \frac{a(1-a)}{12 E_{nt}^2} \cdot \frac{\partial E_{nt}}{\partial V_B} \right) \tag{C.65}$$

$$\frac{\partial Q_b}{\partial V_S} = -[\frac{\partial Q_b}{\partial V_G} + \frac{\partial Q_b}{\partial V_D} + \frac{\partial Q_b}{\partial V_B}] \tag{C.66}$$

(iii) Q_d:

$$\frac{\partial Q_d}{\partial V_G} = - \left(\frac{1}{2} + \frac{a V_{DS}}{E_{nt}^2} [\frac{1}{3} V_{GST} - \frac{1}{8} a V_{DS}] - \frac{2 a V_{DS}}{E_{nt}^3} \cdot V_{COM} \right) \tag{C.67}$$

$$\frac{\partial Q_d}{\partial V_D} = - \left(- \frac{a}{2} - \frac{2 a V_{DS} V_{COM}}{E_{nt}^3} \cdot \frac{\partial E_{nt}}{\partial V_D} + \frac{a}{E_{nt}^2} [\frac{1}{6} V_{GST}^2 - \frac{1}{4} a V_{DS} \cdot V_{GST} + \frac{3}{40} a^2 V_{DS}^2] \right) \tag{C.68}$$

$$\frac{\partial Q_d}{\partial V_B} = - \left(- \frac{1}{2} \frac{\partial V_{th0}}{\partial V_B} - \frac{V_{DS}}{2} \frac{\partial a}{\partial V_B} - \frac{2 a V_{DS} \cdot V_{COM}}{E_{nt}^3} \cdot \frac{\partial E_{nt}}{\partial V_B} + \frac{V_{DS}}{E_{nt}^2} [\frac{V_{GST}^2}{6} \cdot \frac{\partial a}{\partial V_B} + \frac{a V_{GST}}{3} \cdot \frac{\partial V_{th0}}{\partial V_B} - \frac{a V_{DS} \cdot V_{GST}}{4} \cdot \frac{\partial a}{\partial V_B} + \frac{1}{8} a^2 V_{DS} \cdot \frac{\partial V_{th0}}{\partial V_B} + \frac{3}{40} a^2 V_{DS}^2 \cdot \frac{\partial a}{\partial V_B}] \right) \tag{C.69}$$

$$\frac{\partial Q_d}{\partial V_S} = -[\frac{\partial Q_d}{\partial V_G} + \frac{\partial Q_d}{\partial V_D} + \frac{\partial Q_d}{\partial V_B}] \tag{C.70}$$

(iv) Q_s:

$$\frac{\partial Q_s}{\partial V_G} = -[\frac{\partial Q_g}{\partial V_G} + \frac{\partial Q_b}{\partial V_G} + \frac{\partial Q_d}{\partial V_G}] \tag{C.71}$$

$$\frac{\partial Q_s}{\partial V_D} = -\left[\frac{\partial Q_g}{\partial V_D} + \frac{\partial Q_b}{\partial V_D} + \frac{\partial Q_d}{\partial V_D} \right] \tag{C.72}$$

$$\frac{\partial Q_s}{\partial V_B} = -\left[\frac{\partial Q_g}{\partial V_B} + \frac{\partial Q_b}{\partial V_B} + \frac{\partial Q_d}{\partial V_B} \right] \tag{C.73}$$

$$\frac{\partial Q_s}{\partial V_S} = -\left[\frac{\partial Q_s}{\partial V_G} + \frac{\partial Q_s}{\partial V_D} + \frac{\partial Q_s}{\partial V_B} \right] \tag{C.74}$$

(2) Saturation Region:

(i) Q_g:

$$\frac{\partial Q_g}{\partial V_G} = 1 - \frac{1}{3\,a} \tag{C.75}$$

$$\frac{\partial Q_g}{\partial V_D} = 0 \tag{C.76}$$

$$\frac{\partial Q_g}{\partial V_B} = \frac{1}{3\,a} \cdot \frac{\partial V_{th0}}{\partial V_B} + \frac{V_{GST}}{3\,a^2} \cdot \frac{\partial a}{\partial V_B} \tag{C.77}$$

$$\frac{\partial Q_g}{\partial V_S} = -\left[\frac{\partial Q_g}{\partial V_G} + \frac{\partial Q_g}{\partial V_D} + \frac{\partial Q_g}{\partial V_B} \right] \tag{C.78}$$

(ii) Q_b:

$$\frac{\partial Q_b}{\partial V_G} = \frac{1}{3\,a} - \frac{1}{3} \tag{C.79}$$

$$\frac{\partial Q_b}{\partial V_D} = 0 \tag{C.80}$$

$$\frac{\partial Q_b}{\partial V_B} = -\left(\frac{2}{3} + \frac{1}{3\,a} \right) \frac{\partial V_{th0}}{\partial V_B} - \frac{V_{GST}}{3\,a^2} \cdot \frac{\partial a}{\partial V_B} \tag{C.81}$$

$$\frac{\partial Q_b}{\partial V_S} = -\left[\frac{\partial Q_b}{\partial V_G} + \frac{\partial Q_b}{\partial V_D} + \frac{\partial Q_b}{\partial V_B} \right] \tag{C.82}$$

(iii) Q_d:

$$\frac{\partial Q_d}{\partial V_G} = -\frac{4}{15} \tag{C.83}$$

$$\frac{\partial Q_d}{\partial V_D} = 0 \tag{C.84}$$

$$\frac{\partial Q_d}{\partial V_B} = \frac{4}{15} \cdot \frac{\partial V_{th0}}{\partial V_B} \tag{C.85}$$

$$\frac{\partial Q_d}{\partial V_S} = -\left[\frac{\partial Q_d}{\partial V_G} + \frac{\partial Q_d}{\partial V_D} + \frac{\partial Q_d}{\partial V_B} \right] \tag{C.86}$$

(iv) Q_s:

$$\frac{\partial Q_s}{\partial V_G} = -\left[\frac{\partial Q_g}{\partial V_G} + \frac{\partial Q_b}{\partial V_G} + \frac{\partial Q_d}{\partial V_G} \right] \tag{C.87}$$

$$\frac{\partial Q_s}{\partial V_D} = -\left[\frac{\partial Q_g}{\partial V_D} + \frac{\partial Q_b}{\partial V_D} + \frac{\partial Q_d}{\partial V_D} \right] \tag{C.88}$$

$$\frac{\partial Q_s}{\partial V_B} = -\left[\frac{\partial Q_g}{\partial V_B} + \frac{\partial Q_b}{\partial V_B} + \frac{\partial Q_d}{\partial V_B} \right] \tag{C.89}$$

$$\frac{\partial Q_s}{\partial V_S} = -\left[\frac{\partial Q_s}{\partial V_G} + \frac{\partial Q_s}{\partial V_D} + \frac{\partial Q_s}{\partial V_B} \right] \tag{C.90}$$

(3) Subthreshold Region:

$$\frac{\partial Q_g}{\partial V_G} = \left[1 + \frac{4\,(V_{GS} - V_{FB} - V_{BS})}{K_1^2} \right]^{-\frac{1}{2}} \tag{C.91}$$

$$\frac{\partial Q_g}{\partial V_B} = -\frac{\partial Q_g}{\partial V_G} \tag{C.92}$$

$$\frac{\partial Q_b}{\partial V_G} = -\frac{\partial Q_g}{\partial V_G} \tag{C.93}$$

$$\frac{\partial Q_b}{\partial V_B} = \frac{\partial Q_g}{\partial V_G} \tag{C.94}$$

All other capacitances are zero.

(4) Accumulation Region:

$$\frac{\partial Q_g}{\partial V_G} = 1 \tag{C.95}$$

$$\frac{\partial Q_g}{\partial V_B} = -1 \tag{C.96}$$

$$\frac{\partial Q_b}{\partial V_G} = -1 \tag{C.97}$$

$$\frac{\partial Q_b}{\partial V_B} = 1 \tag{C.98}$$

All other capacitances are zero.

C.2. Extrinsic Component Models

(A) Gate-to-Bulk, Gate-to-Drain, and Gate-to-Source Overlap Capacitances:

$$C_{ovgb} = C_{gbo} \cdot L_{MK} \tag{C.99}$$

$$C_{ovgd} = C_{gdo} \cdot W_{eff} \tag{C.100}$$

$$C_{ovgs} = C_{gso} \cdot W_{eff} \tag{C.101}$$

(B) Drain and Source Series Resistances:

$$R_D = R_{SH} \cdot N_{RD} \tag{C.102}$$

$$R_S = R_{SH} \cdot N_{RS} \tag{C.103}$$

(C) drain and source junction currents:

$$I_{dt} = I_{JS} \cdot A_D \tag{C.104}$$

$$I_{st} = I_{JS} \cdot A_S \tag{C.105}$$

If not specified, I_{st} and I_{dt} will default to 1.0E-14.

(D) Drain and Source Junction Capacitances

Let

$$C_{bda} = C_J \cdot A_D \tag{C.106}$$

$$C_{bsa} = C_J \cdot A_S \tag{C.107}$$

$$C_{bdw} = C_{JW} \cdot P_D \tag{C.108}$$

$$C_{bsw} = C_{JW} \cdot P_S \tag{C.109}$$

(1) drain junction:

For $V_{BD} < 0$:

$$Q_{BD} = P_J \cdot C_{bda} \cdot \frac{\left[1 - \left(1 - \frac{V_{BD}}{P_J} \right)^{1-M_J} \right]}{1 - M_J} + P_{JW} \cdot C_{bdw} \cdot \frac{\left[1 - \left(1 - \frac{V_{BD}}{P_{JW}} \right)^{1-M_{JW}} \right]}{1 - M_{JW}} \tag{C.110}$$

$$C_{BD} = \frac{C_{bda}}{\left(1 - \frac{V_{BD}}{P_J} \right)^{M_J}} + \frac{C_{bdw}}{\left(1 - \frac{V_{BD}}{P_{JW}} \right)^{M_{JW}}} \tag{C.111}$$

For $V_{BD} \geqslant 0$:

$$Q_{BD} = V_{BD} \cdot (C_{bda} + C_{bdw}) + V_{BD}^2 \cdot \left(\frac{C_{bda} \cdot M_J}{2 \cdot P_J} + \frac{C_{bdw} \cdot M_{JW}}{2 \cdot P_{JW}} \right) \tag{C.112}$$

$$C_{BD} = C_{bda} + C_{bdw} + V_{BD} \cdot \left(\frac{C_{bda} \cdot M_J}{P_J} + \frac{C_{bdw} \cdot M_{JW}}{P_{JW}} \right) \tag{C.113}$$

2) source junction:

For $V_{BS} < 0$:

$$Q_{BS} = P_J \cdot C_{bsa} \cdot \frac{\left[1 - \left(1 - \frac{V_{BS}}{P_J} \right)^{1-M_J} \right]}{1 - M_J} + P_{JW} \cdot C_{bsw} \cdot \frac{\left[1 - \left(1 - \frac{V_{BS}}{P_{JW}} \right)^{1-M_{JW}} \right]}{1 - M_{JW}}$$

(C.114)

$$C_{BS} = \frac{C_{bsa}}{(1 - \frac{V_{BS}}{P_J})^{M_J}} + \frac{C_{bsw}}{(1 - \frac{V_{BS}}{P_{JW}})^{M_{JW}}} \tag{C.115}$$

For $V_{BS} \geqslant 0$:

$$Q_{BS} = V_{BS} \cdot (C_{bsa} + C_{bsw}) + V_{BS}^2 \cdot \left[\frac{C_{bsa} \cdot M_J}{2 \cdot P_J} + \frac{C_{bsw} \cdot M_{JW}}{2 \cdot P_{JW}} \right] \tag{C.116}$$

$$C_{BS} = C_{bsa} + C_{bsw} + V_{BS} \cdot \left[\frac{C_{bsa} \cdot M_J}{P_J} + \frac{C_{bsw} \cdot M_{JW}}{P_{JW}} \right] \tag{C.117}$$

E) Interconnect Resistor:

$$R = R_{SH} \cdot \frac{L_e}{W_e} \tag{C.118}$$

F) Interconnect Capacitor:

$$C = C_J \cdot L_e \cdot W_e + 2 \cdot C_{JW} \cdot (L_e + W_e) \tag{C.119}$$

Where

$$L_e = L - \delta_S \, , \quad \text{and } W_e = W - \delta_S \tag{C.120}$$

APPENDIX D

LISTING OF SUBROUTINE BSIMEQ IN SPICE2 IMPLEMENTATION

```
      SUBROUTINE BSIMEQ(VDS,VBS,VGS,LOC,GM,GDS,GMBS,QG,QB,QD,
     1    CGGB,CGDB,CGSB,CBGB,CBDB,CBSB,CDGB,CDDB,CDSB)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
C
C     THIS ROUTINE EVALUATES THE DRAIN CURRENT, ITS DERIVATIVES AND
C     THE CHARGES ASSOCIATED WITH THE GATE, BULK AND DRAIN TERMINAL
C     USING THE BSIM (SHORT-CHANNEL IGFET) MODEL EQUATIONS.
C NEW SPICE SUBROUTINE FOR BSIM MODEL -- AUTHOR: BING J. SHEU
C
C SPICE VERSION 2G.6  SCCSID=MOSARG 3/15/83
      COMMON /MOSARG/ VTO,BETA,GAMMA,PHI,PHIB,COX,XNSUB,XNFS,XD,XJ,XLD,
     1   XLAMDA,UO,UEXP,VBP,UTRA,VMAX,XNEFF,XL,XW,VBI,VON,VDSAT,QSPOF,
     2   BETA0,BETA1,CDRAIN,XQCO,XQC,FNARRW,FSHORT,LEV
C SPICE VERSION 2G.6  SCCSID=STATUS 3/15/83
      COMMON /STATUS/ OMEGA,TIME,DELTA,DELOLD(7),AG(7),VT,XNI,EGFET,
     1   XMU,SFACTR,MODE,MODEDC,ICALC,INITF,METHOD,IORD,MAXORD,NONCON,
     2   ITERNO,ITEMNO,NOSOLV,MODAC,IPIV,IVMFLG,IPOSTP,ISCRCH,IOFILE
C SPICE VERSION 2G.6  SCCSID=KNSTNT 3/15/83
      COMMON /KNSTNT/ TWOPI,XLOG2,XLOG10,ROOT2,RAD,BOLTZ,CHARGE,CTOK,
     1   GMIN,RELTOL,ABSTOL,VNTOL,TRTOL,CHGTOL,EPS0,EPSSIL,EPSOX,
     2   PIVTOL,PIVREL
      COMMON /BLANK/ VALUE(200000)
      INTEGER NODPLC(64)
      COMPLEX CVALUE(32)
      EQUIVALENCE (VALUE(1),NODPLC(1),CVALUE(1))
C
      ICHARG=1
      IF (MODE  NE. 1) GO TO 5
      IF (MODEDC .EQ. 2 .AND. NOSOLV .NE. 0) GO TO 5
      IF (INITF .EQ. 4) GO TO 5
      ICHARG=0
C
```

```
    5 LOCV=NODPLC(LOC+1)
      LOCM=NODPLC(LOC+8)
      LOCM=NODPLC(LOCM+1)
      VFB=VALUE(LOCV+17)
      PHI=VALUE(LOCV+18)
      XK1=VALUE(LOCV+19)
      XK2=VALUE(LOCV+20)
      VDD=VALUE(LOCM+54)
      U0=VALUE(LOCV+23)+VBS*VALUE(LOCV+28)
      U1=VALUE(LOCV+24)+VBS*VALUE(LOCV+29)
     1   +(VDS-VDD)*VALUE(LOCV+33)
      DU0DVB=VALUE(LOCV+28)
C
      XLU=VALUE(LOCV+1)*1.0D6
      U1=U1/XLU
      DU1DVB=VALUE(LOCV+29)/XLU
      DU1DVD=VALUE(LOCV+33)/XLU
C
   10 ETA=VALUE(LOCV+21)+VALUE(LOCV+26)*VBS+VALUE(LOCV+27)*(VDS-VDD)
      DETDVB=VALUE(LOCV+26)
      DETDVD=VALUE(LOCV+27)
C
      IF (VBS .GE. 0.0D0) GO TO 14
      VPB=PHI-VBS
      GO TO 15
   14 VPB=PHI
   15 SQRVPB=DSQRT(VPB)
C
C DO NOT REMOVE THE VARIABLE "VON"
C
      VON=VFB+PHI+XK1*SQRVPB-XK2*VPB-ETA*VDS
      VTH=VON
      DVTDVD=-ETA-VDS*DETDVD
```

```
      DVTDVB=XK2-0.5D0*XK1/SQRVPB-VDS*DETDVB
      VGT=VGS-VTH
      IF (VGT .GE. 0.0D0) GO TO 20
C
C CUT-OFF REGION
C
      CDRAIN=0.0D0
      GM=0.0D0
      GDS=0.0D0
      GMBS=0.0D0
      GO TO 100
C
   20 G=1.0D0-1.0D0/(1.744D0+0.8364*VPB)
      A=1.0D0+0.5D0*G*XK1/SQRVPB
      DGDVBS=-0.8364D0*(1.0D0-G)*(1.0D0-G)
      DADVBS=0.25D0*XK1/SQRVPB*(2.0D0*DGDVBS+G/VPB)
      ARG=1.0D0+U0*VGT
C
C LIMIT ARG
C
      IF (ARG .LT. 0.1D0) ARG=0.1D0
C
C QUADRATIC INTERPOLATION FOR BETA0 VALUE
C
      XT=VALUE(LOCV+22)+VBS*VALUE(LOCV+25)
      XA=VALUE(LOCV+30)+VBS*VALUE(LOCV+31)
      XB=VALUE(LOCV+32)
      IF (VDS .LE. VDD) GO TO 25
      BETA0=XA+XB*(VDS-VDD)
      DB0DVD=XB
      DB0DVB=VALUE(LOCV+31)
      GO TO 30
```

```
   25 VDD2=VDD*VDD
      C1=(XB*VDD-XA+XT)/VDD2
      C2=2.0D0*(XA-XT)/VDD-XB
      DXTDVB=VALUE(LOCV+25)
      DXADVB=VALUE(LOCV+31)
      DC1DVB=(-DXADVB+DXTDVB)/VDD2
      DC2DVB=2.0D0*(DXADVB-DXTDVB)/VDD
      BETA0=(C1*VDS+C2)*VDS+XT
      DB0DVD=2.0D0*C1*VDS+C2
      DB0DVB=DC1DVB*VDS*VDS+DC2DVB*VDS+DXTDVB
   30 BETA=BETA0/ARG
      DBDVGS=-BETA*U0/ARG
      DBDVDS=DB0DVD/ARG-DBDVGS*DVTDVD
      DBDVBS=DB0DVB/ARG+BETA*U0*DVTDVB/ARG
     1  -BETA*VGT*DU0DVB/ARG
C
C LIMIT VC
C
      VC=U1*VGT/A
      IF (VC .LT. -0.4D0) VC=-0.4D0
      TERM1=DSQRT(1.0D0+2.0D0*VC)
      XK=0.5D0*(1.0D0+VC+TERM1)
      VDSAT=VGT/(A*DSQRT(XK))
      IF (VDSAT .LT. 0.0D0) VDSAT=0.0D0
      IF (VDS .GE. VDSAT) GO TO 50
C
C TRIODE REGION
C
      ARGL1=1.0D0+U1*VDS
C
C LIMIT ARGL1
C
```

```
      IF (ARGL1 .LT. 0.1D0) ARGL1=0.1D0
      ARGL2=VGT-0.5D0*A*VDS
      CDRAIN=BETA*ARGL2*VDS/ARGL1
      GM=(DBDVGS*ARGL2*VDS+BETA*VDS)/ARGL1
      GDS=(DBDVDS*ARGL2*VDS+BETA*(VGT-VDS*DVTDVD-A*VDS)
     1  -CDRAIN*(VDS*DU1DVD+U1))/ARGL1
      GMBS=(DBDVBS*ARGL2*VDS+BETA*VDS*(-DVTDVB-0.5D0*VDS*DADVBS)
     2  -CDRAIN*VDS*DU1DVB)/ARGL1
      GO TO 100
C
C SATURATION REGION
C
   50 ARGS1=1.0D0+1.0D0/TERM1
      DVCDVG=U1/A
      DVCDVD=VGT*DU1DVD/A-DVCDVG*DVTDVD
      DVCDVB=(VGT*DU1DVB-U1*(DVTDVB+VGT*DADVBS/A))/A
      DKDVC=0.5D0*ARGS1
      DKDVGS=DKDVC*DVCDVG
      DKDVDS=DKDVC*DVCDVD
      DKDVBS=DKDVC*DVCDVB
      ARGS2=VGT/(A*XK)
      ARGS3=ARGS2*VGT
      CDRAIN=0.5D0*BETA*ARGS3
      GM=0.5D0*ARGS3*DBDVGS+BETA*ARGS2-CDRAIN*DKDVGS/XK
      GDS=0.5D0*ARGS3*DBDVDS-BETA*ARGS2*DVTDVD-CDRAIN*DKDVDS/XK
      GMBS=0.5D0*DBDVBS*ARGS3-BETA*ARGS2*DVTDVB
     1  -CDRAIN*(DADVBS/A+DKDVBS/XK)
C
C INCLUDING THE WEAK INVERSION CONDUCTION. IF STHD IS NOT SPECIFIED,
C THEN 200.0 IS STORED AT VALUE(LOCV+37)
C
  100 XN0=VALUE(LOCV+37)
```

```
      XCUTH=3.5D1*XN0*VT
      IF ((XN0 .GE. 2.0D2) .OR. (VGT .LT. -XCUTH)) GO TO 150
      XNB=VALUE(LOCV+38)
      XND=VALUE(LOCV+39)
      XN=XN0+XNB*VBS+XND*VDS
C
C LIMIT XN
C
      IF (XN .LT. 0.5D0) XN=0.5D0
      ONXN=1 0D0/XN
      ONVT=1.0D0/VT
      ONDVT=ONXN*ONVT
C AVOID UNDERFLOW
      WARG1=0.0D0
      TERMW1=VDS*ONVT
      IF (TERMW1 .LT. 3.5D1) WARG1=DEXP(-TERMW1)
      WDS=1.0D0-WARG1
C AVOID OVERFLOW
      WGS=1.6D15
      IF (VGT .LT. XCUTH) WGS=DEXP(VGT*ONDVT)
      VT2=VT*VT
      EXP18=DEXP(1.8D0)
      WARG2=VALUE(LOCV+22)*VT2*EXP18
      CISL=VALUE(LOCV+22)*4.5D0*VT2
      CIEXP=WARG2*WGS*WDS
      CDEN=CISL+CIEXP
      CDRAIN=CDRAIN+CISL*CIEXP/CDEN
      XCOM1=CISL*CISL/(CDEN*CDEN)
      GM=GM+XCOM1*CIEXP*ONDVT
      GDS=GDS+XCOM1*WARG2*WGS*(-WDS*ONDVT*(DVTDVD+VGT*XND*ONXN)
     1  +WARG1*ONVT)
      GMBS=GMBS-XCOM1*CIEXP*(DVTDVB+VGT*XNB*ONXN)*ONDVT
  150 CONTINUE
```

```
C
C LIMIT CDRAIN, GM, GDS, GMBS
C
      IF (CDRAIN .LT. 0.0D0) CDRAIN=0.0D0
      IF (GM .LT. 0.0D0) GM=0.0D0
      IF (GDS .LT. 0.0D0) GDS=0.0D0
      IF (GMBS .LT. 0.0D0) GMBS=0.0D0
C
  200 IF (ICHARG .EQ. 0) GO TO 900
C
C COMMON BLOCK FOR ALL PARTITIONING METHODS
C
      COX=VALUE(LOCV+1)*VALUE(LOCV+2)*EPSOX/VALUE(LOCM+52)
      VTHO=VFB+PHI+XK1*SQRVPB
      VGST=VGS-VTHO
      ARG1=A*VDS
C     ARG2=VGST-0.5D0*ARG1
      ENT=VGST-0.5D0*ARG1
      ARG3=VDS-ARG1
      ARG4=ARG2*12.0D0
      ARG5=ARG1*ARG1
      DVTDVB=-0.5D0*XK1/SQRVPB
      DADVB=0.5D0*XK1*(0.5D0*G/VPB-0.8364D0*(1-G)*(1-G))/SQRVPB
      IF (ENT .LT. 1.0D-8) ENT=1.0D-8
      DETDVD=-0.5D0*A
      DETDVB=-DVTDVB-0.5D0*VDS*DADVB
      VGST2=VGST*VGST
      VDS2=VDS*VDS
C
C EVALUATE THE GATE, BULK, AND DRAIN CHARGES AND CAPACITANCES
C
      XPART=VALUE(LOCV+16)
      IF (XPART .GE. 1.0D0) GO TO 400
```

```
      IF (XPART .NE. 0.5D0) GO TO 500
C
C 50/50 PARTITIONING FOR DRAIN/SOURCE CHARGES AT THE SATURATION REGION
C
      IF (VGS .LE. VTHO) GO TO 350
C
      VDPOF=VGST/A
      IF (VDS .GT. VDPOF) GO TO 330
C
C  TRIODE REGION
C
      ENT2=ENT*ENT
      ARGL1=1.2D1*ENT2
      ARGL2=1.0D0-A
      ARGL3=ARG1*VDS
      ARGL5=2.0D0
      IF (ENT .GT. 1.0D-8) ARGL5=ARG1/ENT
      ARGL7=ARGL5/1.2D1
      ARGL8=6.0D0*ENT
      QG=COX*(VGS-VFB-PHI-0.5D0*VDS+VDS*ARGL7)
      QB=COX*(-VTHO+VFB+PHI+0.5D0*ARG3-ARG3*ARGL7)
      QD=-0.5D0*(QG+QB)
      CGGB=COX*(1.0D0-ARGL3/ARGL1)
      CGDB=COX*(-0.5D0+ARG1/ARGL8-ARGL3*DETDVD/ARGL1)
      CGBB=COX*(VDS2*DADVB*ENT-ARGL3*DETDVB)/ARGL1
      CGSB=-(CGGB+CGDB+CGBB)
      CBGB=COX*ARGL3*ARGL2/ARGL1
      CBDB=COX*ARGL2*(0.5D0-ARG1/ARGL8+ARGL3*DETDVD/ARGL1)
      CBBB=-COX*(DVTDVB+0.5D0*VDS*DADVB+VDS2*((1.0D0-2.0D0*A)
     1   *DADVB*ENT-ARGL2*A*DETDVB)/ARGL1)
      CBSB=-(CBGB+CBDB+CBBB)
      CDGB=-0.5D0*(CGGB+CBGB)
      CDDB=-0.5D0*(CGDB+CBDB)
```

```
      CDSB=-0.5D0*(CGSB+CBSB)
      GO TO 1000
C
C SATURATION REGION
C
  330 CON1V3=1.0D0/3.0D0
      ARGS1=CON1V3/A
      QG=COX*(VGS-VFB-PHI-VGST*ARGS1)
      QB=COX*(VFB+PHI-VTHO+(1.0D0-A)*VGST*ARGS1)
      QD=-CON1V3*COX*VGST
      CGGB=COX*(1.0D0-ARGS1)
      CGDB=0.0D0
      CGBB=COX*ARGS1*(DVTDVB+VGST*DADVB/A)
      CGSB=-(CGGB+CGDB+CGBB)
      CDGB=-COX*CON1V3
      CDDB=0.0D0
      CDBB=CON1V3*COX*DVTDVB
      CDSB=-(CDGB+CDDB+CDBB)
      CBGB=-(CGGB+2.0D0*CDGB)
      CBDB=0.0D0
      CBSB=-(CGSB+2.0D0*CDSB)
      GO TO 1000
C
C SUBTHRESHOLD REGION
C
  350 VGSMV1=VGS-(VFB+VBS)
      IF (VGSMV1 .LE. 0.0D0) GO TO 370
      XK1S=XK1*XK1
      QG=0.5D0*COX*XK1S*(-1.0D0+DSQRT(1.0D0
     1  +4.0D0*VGSMV1/XK1S))
      QB=-QG
      QD=0.0D0
      CGGB=COX/DSQRT(1.0D0+4.0D0*VGSMV1/XK1S)
```

```
      CGDB=0.0D0
      CGSB=0.0D0
      CBGB=-CGGB
      CBDB=0.0D0
      CBSB=0.0D0
      CDGB=0.0D0
      CDDB=0.0D0
      CDSB=0.0D0
      GO TO 1000
C
C ACCUMULATION REGION
C
  370 QG=COX*VGSMV1
      QB=-QG
      QD=0.0D0
      CGGB=COX
      CGDB=0.0D0
      CGSB=0.0D0
      CBGB=-COX
      CBDB=0.0D0
      CBSB=0.0D0
      CDGB=0.0D0
      CDDB=0.0D0
      CDSB=0.0D0
      GO TO 1000
C
C 0/100 PARTITIONING FOR DRAIN/SOURCE CHARGES AT THE SATURATION REGION
C
  400 IF (VGS .LE. VTHO) GO TO 350
C
      VDPOF=VGST/A
      IF (VDS .GT. VDPOF) GO TO 430
C
```

```
C TRIODE REGION
C
      ENT2=ENT*ENT
      ARGL1=1.2D1*ENT2
      ARGL2=1.0D0-A
      ARGL3=ARG1*VDS
      ARGL5=2.0D0
      IF (ENT .GT. 1.0D-8) ARGL5=ARG1/ENT
      ARGL7=ARGL5/1.2D1
      ARGL8=6.0D0*ENT
      ARGL9=0.125D0*ARGL5*ARGL5
      QG=COX*(VGS-VFB-PHI-0.5D0*VDS+VDS*ARGL7)
C     QB=COX*(-VTHO+VFB+PHI+0.5D0*ARG3-ARG3*ARGL7)
      QB=COX*(-VTHO+VFB+PHI+ARG3*(0.5D0-ARGL7))
      QD=-COX*(0.5D0*VGST-0.75D0*ARG1+0.125D0*ARG1*ARGL5)
      CGGB=COX*(1.0D0-ARGL3/ARGL1)
      CGDB=COX*(-0.5D0+ARG1/ARGL8-ARGL3*DETDVD/ARGL1)
      CGBB=COX*(VDS2*DADVB*ENT-ARGL3*DETDVB)/ARGL1
      CGSB=-(CGGB+CGDB+CGBB)
      CBGB=COX*ARGL3*ARGL2/ARGL1
      CBDB=COX*ARGL2*(0.5D0-ARG1/ARGL8+ARGL3*DETDVD/ARGL1)
      CBBB=-COX*(DVTDVB+0.5D0*VDS*DADVB+VDS2*((1.0D0-2.0D0*A)
     1  *DADVB*ENT-ARGL2*A*DETDVB)/ARGL1)
      CBSB=-(CBGB+CBDB+CBBB)
      CDGB=-COX*(0.5D0-ARGL9)
      CDDB=COX*(0.75D0*A-0.25D0*A*ARG1/ENT+ARGL9*DETDVD)
      CDBB=COX*(0.5D0*DVTDVB+VDS*DADVB*(0.75D0-0.25D0*ARGL5)
     1  +ARGL9*DETDVB)
      CDSB=-(CDGB+CDDB+CDBB)
      GO TO 1000
C
C SATURATION REGION
C
```

```
  430 CON1V3=1.0D0/3.0D0
      ARGS1=CON1V3/A
      QG=COX*(VGS-VFB-PHI-VGST*ARGS1)
      QB=COX*(VFB+PHI-VTHO+(1.0D0-A)*VGST*ARGS1)
      QD=0.0D0
      CGGB=COX*(1.0D0-ARGS1)
      CGDB=0.0D0
      CGBB=COX*ARGS1*(DVTDVB+VGST*DADVB/A)
      CGSB=-(CGGB+CGDB+CGBB)
      CBGB=COX*(ARGS1-CON1V3)
      CBDB=0.0D0
      CBBB=-COX*((1.0D0-CON1V3+ARGS1)*DVTDVB+VGST*ARGS1*DADVB/A)
      CBSB=-(CBGB+CBDB+CBBB)
      CDGB=0.0D0
      CDDB=0.0D0
      CDSB=0.0D0
      GO TO 1000
C
C 40/60 PARTITIONING FOR DRAIN/SOURCE CHARGES AT THE SATURATION REGION
C
  500 VCOM=VGST*VGST/6.0D0-1.25D-1*ARG1*VGST+2.5D-2*ARG5
      IF (VGS .LE. VTHO) GO TO 350
C
      VDPOF=VGST/A
      IF (VDS .GT. VDPOF) GO TO 530
C
C TRIODE REGION
C
      ENT2=ENT*ENT
      ARGL1=1.2D1*ENT2
      ARGL2=1.0D0-A
      ARGL3=ARG1*VDS
      ARGL4=VCOM/ENT/ENT2
```

```
      IF (ENT .LE. 1.0D-8) GO TO 520
      ARGL5=ARG1/ENT
      ARGL6=VCOM/ENT2
      GO TO 525
  520 ARGL5=2.0D0
      ARGL6=4.0D0/1.5D1
  525 ARGL7=ARGL5/1.2D1
      ARGL8=6.0D0*ENT
      QG=COX*(VGS-VFB-PHI-0.5D0*VDS+VDS*ARGL7)
      QB=COX*(-VTHO+VFB+PHI+0.5D0*ARG3-ARG3*ARGL7)
      QD=-COX*(0.5D0*(VGST-ARG1)+ARG1*ARGL6)
      CGGB=COX*(1.0D0-ARGL3/ARGL1)
      CGDB=COX*(-0.5D0+ARG1/ARGL8-ARGL3*DETDVD/ARGL1)
      CGBB=COX*(VDS2*DADVB*ENT-ARGL3*DETDVB)/ARGL1
      CGSB=-(CGGB+CGDB+CGBB)
      CBGB=COX*ARGL3*ARGL2/ARGL1
      CBDB=COX*ARGL2*(0.5D0-ARG1/ARGL8+ARGL3*DETDVD/ARGL1)
      CBBB=-COX*(DVTDVB+0.5D0*VDS*DADVB+VDS2*((1.0D0-2.0D0*A)
     1  *DADVB*ENT-ARGL2*A*DETDVB)/ARGL1)
      CBSB=-(CBGB+CBDB+CBBB)
      CDGB=-COX*(0.5D0+ARG1*(4.0D0*VGST-1.5D0*ARG1)/ARGL1
     1 -2.0D0*ARG1*ARGL4)
      CDDB=COX*(0.5D0*A+2.0D0*ARG1*DETDVD*ARGL4-A*(2.0D0*VGST2
     1  -3.0D0*ARG1*VGST+0.9D0*ARG5)/ARGL1)
      CDBB=COX*(0.5D0*DVTDVB+0.5D0*VDS*DADVB+2.0D0*ARG1*DETDVB
     1  *ARGL4-VDS*(2.0D0*VGST2*DADVB-4.0D0*A*VGST*DVTDVB-3.0D0
     2  *ARG1*VGST*DADVB+1.5D0*A*ARG1*DVTDVB+0.9D0*ARG5*DADVB)
     3  /ARGL1)
      CDSB=-(CDGB+CDDB+CDBB)
      GO TO 1000
C
C SATURATION REGION
C
```

```
  530 CON1V3=1.0D0/3.0D0
      CO4V15=4.0D0/1.5D1
      ARGS1=1.0D0/(3.0D0*A)
      QG=COX*(VGS-VFB-PHI-VGST*ARGS1)
      QB=COX*(VFB+PHI-VTHO+(1.0D0-A)*VGST*ARGS1)
      QD=-CO4V15*COX*VGST
      CGGB=COX*(1.0D0-ARGS1)
      CGDB=0.0D0
      CGBB=COX*ARGS1*(DVTDVB+VGST*DADVB/A)
      CGSB=-(CGGB+CGDB+CGBB)
      CBGB=COX*(ARGS1-CON1V3)
      CBDB=0.0D0
      CBBB=-COX*((1.0D0-CON1V3+ARGS1)*DVTDVB-VGST*ARGS1*DADVB/A)
      CBSB=-(CBGB+CBDB+CBBB)
      CDGB=-CO4V15*COX
      CDDB=0.0D0
      CDBB=CO4V15*COX*DVTDVB
      CDSB=-(CDGB+CDDB+CDBB)
      GO TO 1000
C
  900 QG=0.0D0
      QB=0.0D0
      QC=0.0D0
 1000 RETURN
      END
```

APPENDIX E

BENCHMARK CIRCUITS

Example - 1

```
RATLOG - RATIOLESS DYNAMIC LOGIC CIRCUIT
***** ANALYSIS CONTROL *****
*WIDTH  IN=72  OUT=80
*OPT  ABSTOL=1U
*OPT  ACCT
***** DEVICES *****
SM1  9  11  2  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
SM2  9  12  4  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
SM3  2   1  0  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
SM4  4   3  0  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
SM5  3  12  2  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
SM6  1  11  5  10   PC1_NM1  W=20U  L=7U  AD=1N  AS=1N
*PROCESS PC1 FILENAME=CB0716
C1   1   0   0.05PF
C2   2   0   0.05PF
C3   3   0   0.05PF
C4   4   0   0.05PF
C5   5   0   0.05PF
***** POWER SUPPLY AND SIGNAL *****
VIN   5  0  PULSE(0  10  10N  5N  10N  55N  500N)
VP1  11  0  PULSE(0  12  10N  5N   5N  35N  120N)
VP2  12  0  PULSE(0  12  70N  5N   5N  35N  120N)
VDD   9  0  DC 12
VBB  10  0
***** ANALYSIS REQUEST *****
*TRAN  2.5N  250N
*PLOT  TRAN  V(4)  V(5)
*PLOT  TRAN  V(4)  V(1)  V(2)  V(3)  V(5)  V(11)  V(12)  (-5,15)
*END
```

Example - 2

```
INVCHN - FIVE-STAGE SATURATED INVERTER CHAIN
*****. ANALYSIS CONTROL *****
.WIDTH  IN=72  OUT=80
.OPT  DEFAD=1E-12  DEFAS=1E-12
.OPT  ACCT
***** DEVICES *****
SM1   7  7  2  8   PC1_NM1  W=10U  L=8U
SM2   2  1  0  8   PC1_NM1  W=70U  L=8U
SM3   7  7  3  8   PC1_NM1  W=10U  L=8U
SM4   3  2  0  8   PC1_NM1  W=70U  L=8U
SM5   7  7  4  8   PC1_NM1  W=10U  L=8U
SM6   4  3  0  8   PC1_NM1  W=70U  L=8U
SM7   7  7  5  8   PC1_NM1  W=10U  L=8U
SM8   5  4  0  8   PC1_NM1  W=70U  L=8U
SM9   7  7  6  8   PC1_NM1  W=10U  L=8U
SM10  6  5  0  8   PC1_NM1  W=70U  L=8U
.PROCESS PC1 FILENAME=CC0716
***** POWER SUPPLY AND SIGNAL *****
VIN  1  0  PULSE(5  0  0.2N  1N  1N  5N  12N)
VDD  7  0  DC 6
VBB  8  0  DC 0
***** ANALYSIS REQUEST *****
.OP
.TRAN  0.12N  12N
.PLOT  TRAN  V(2)  V(3)  V(4)  V(5)  V(6)  V(1) (-1,5)
.END
```

Example - 3

```
BOOTINV - BOOTSTRAPPED DOUBLE INVERTER CIRCUIT
***** ANALYSIS CONTROL *****
.WIDTH  IN=72  OUT=80
.OPT  ABSTOL=10U
.OPT  ACCT
***** DEVICES *****
SM1  1  1  3  6   PC1_NM1   W=10U   L=7U   AD=0.02P AS=0.02P
SM2  3  2  0  6   PC1_NM1   W=50U   L=7U   AD=2P    AS=0.02P
SM3  1  1  4  6   PC1_NM1   W=10U   L=7U   AD=0.2P  AS=0.2P
SM4  1  4  5  6   PC1_NM1   W=10U   L=7U   AD=0.02P AS=0.02P
SM5  5  3  0  6   PC1_NM1   W=50U   L=7U   AD=2P    AS=0.02P
.PROCESS PC1 FILENAME=CD0716
CL5  5  0  0.1PF
CL2  3  0  0.1PF
CB4  4  5  0.1PF
***** POWER SUPPLY AND SIGNAL *****
VDD  1  0  DC  12
VBB  6  0  DC  -4
VIN  2  0  PULSE(10  0.4  1NS  2NS  2NS  13NS  20NS)
***** ANALYSIS REQUEST *****
.OP
.TRAN  0.2NS  20NS
.PLOT  TRAN  V(5)  V(2)
.PLOT  TRAN  V(2)  V(3)  V(4)  V(5)
.END
```

Example - 4

```
MOSAMP1 - MOS AMPLIFIER - DC/AC
***** ANALYSIS CONTROL *****
*WIDTH  OUT=80
*OPT  ACCT
*OPT  ABSTOL=10N  VNTOL=10N
*OPT  DEFAD=10P   DEFAS=10P
***** DEVICES *****
SM1   15  15   1  32   PC1_NM1  W=88.9U   L=25.4U
SM2    1   1   2  32   PC1_NM1  W=12.7U   L=266.7U
SM3    2   2  30  32   PC1_NM1  W=88.9U   L=25.4U
SM4   15   5   4  32   PC1_NM1  W=12.7U   L=106.7U
SM5    4   4  30  32   PC1_NM1  W=88.9U   L=12.7U
SM6   15  15   5  32   PC1_NM1  W=44.5U   L=25.4U
SM7    5   0   8  32   PC1_NM1  W=482.6U  L=12.7U
SM8    8   2  30  32   PC1_NM1  W=88.9U   L=25.4U
SM9   15  15   6  32   PC1_NM1  W=44.5U   L=25.4U
SM10   6  21   8  32   PC1_NM1  W=482.6U  L=12.7U
SM11  15   6   7  32   PC1_NM1  W=12.7U   L=106.7U
SM12   7   4  30  32   PC1_NM1  W=88.9U   L=12.7U
SM13  15  10   9  32   PC1_NM1  W=139.7U  L=12.7U
SM14   9  11  30  32   PC1_NM1  W=139.7U  L=12.7U
SM15  15  15  12  32   PC1_NM1  W=12.7U   L=207.8U
SM16  12  12  11  32   PC1_NM1  W=54.1U   L=12.7U
SM17  11  11  30  32   PC1_NM1  W=54.1U   L=12.7U
SM18  15  15  10  32   PC1_NM1  W=12.7U   L=45.2U
SM19  10  12  13  32   PC1_NM1  W=270.5U  L=12.7U
SM20  13   7  30  32   PC1_NM1  W=270.5U  L=12.7U
SM21  15  10  14  32   PC1_NM1  W=254U    L=12.7U
SM22  14  11  30  32   PC1_NM1  W=241.3U  L=12.7U
SM23  15  20  16  32   PC1_NM1  W=19U     L=38.1U
```

```
SM24 16  14  30  32   PC1_NM1  W=406.4U L=12.7U
SM25 15  15  20  32   PC1_NM1  W=38.1U  L=42.7U
SM26 20  16  30  32   PC1_NM1  W=381U   L=25.4U
SM27 20  15  66  32   PC1_NM1  W=22.9U  L=7.6U
*PROCESS PC1 FILENAME=CL0716
CC   7  9   40PF
CL   66 0   70PF
***** POWER SUPPLY AND SIGNAL *****
VIN   21  0  DC  15MV  AC  1
VCCP 15  0  DC  +15
VCCN 30  0  DC  -15
VB   32  0  DC  -20
*OP
*DC  VIN  -18MV  48MV  0.66MV
*AC  DEC  10  100  10MEG
*PLOT  DC  V(20)
*PLOT  AC  VDB(20)  VP(20)  VDB(66)  VP(66)
*END
```

Example - 5

```
BINARY-TO-OCTAL DECODER CIRCUIT
.WIDTH OUT=80
.PROCESS PC1 FILENAME=CK0716
***  NO JS, NO CBD & CBS
*DEVICE MODELS
* SUBCIRCUIT MODELS
.SUBCKT NAND 1 2 3 100
SM1 100 3 3 0 PC1_NM3  W=20U L=9.5U
SM2   3 1 4 0 PC1_NM1  W=20U L=2.3U
SM3   4 2 0 0 PC1_NM1  W=20U L=2.3U
.ENDS NAND
.SUBCKT NOR 1 2 3 100
SM1 100 3 3 0 PC1_NM3  W=20U L=9.5U
SM2   3 1 0 0 PC1_NM1  W=20U L=2.3U
SM3   3 2 0 0 PC1_NM1  W=20U L=2.3U
.ENDS NOR
.SUBCKT INV 1 2 100
SM1 100 2 2 0 PC1_NM3  W=20U L=9.5U
SM2   2 1 0 0 PC1_NM1  W=20U L=2.3U
.ENDS INV
* INPUT SIGNAL INVERTERS
X15 1 5 100 INV
X16 2 6 100 INV
X17 3 7 100 INV
* NOR GATES
X1 5 6 9  100 NOR
X2 2 5 10 100 NOR
X3 1 6 11 100 NOR
X4 1 2 12 100 NOR
X5 3 4 13 100 NOR
```

```
X6 4 7 14 100 NOR
* NAND GATES
X7  12 13 17 100 NAND
X8  10 13 18 100 NAND
X9  11 13 19 100 NAND
X10 9  13 20 100 NAND
X11 12 14 21 100 NAND
X12 10 14 22 100 NAND
X13 11 14 23 100 NAND
X14 9  14 24 100 NAND
* INPUT SOURCES
VCC 100 0 DC 5
VA  1 0 PULSE(5 0  5NS 10NS 10NS 20NS 60NS)
VB  2 0 PULSE(5 0 45NS 10NS 10NS 50NS 120NS)
VC  3 0 PULSE(5 0 105NS 10NS 10NS 110NS 240NS)
VD  4 0 DC 0
*ANALYSIS REQUESTS
.TRAN 1.2NS 240NS
.PLOT TRAN V(17) V(18) V(19) V(20)
+    V(21) V(22) V(23) V(24) (0,5)
.OPT ACCT DEFAS=1N DEFAD=1N
+    RELTOL=1M ABSTOL=1N VNTOL=1N LVLTIM=1
*  .OP
*  .OPT ACCT DEFAS=1N DEFAD=1N
*  +    RELTOL=1M ABSTOL=1N VNTOL=1N LVLTIM=1
.END
```

APPENDIX F

SOURCE-DRAIN SERIES RESISTANCE OF LIGHTLY-DOPED-DRAIN MOS TRANSISTORS

F.1. Introduction

As MOS transistor device size continues to shrink, the degradation of electrical characteristics induced by hot-carrier effects becomes increasingly severe. Device breakdown or degradation and substrate current due to impact ionization have become problems for aggressively-scaled devices. Recent work on lightly-doped-drain (LDD) devices [F.1]-[F.7] is an effort to alleviate the above-mentioned problems. In the LDD device, self-aligned n^- regions are introduced between the channel and the n^+ drain and source diffusions. The n^- source is not really necessary unless the device is to be operated bidirectionally. However, to eliminate the n^- source would require an additional mask step. Advantages of the LDD structure are many. It increases the transistor breakdown voltage and reduces impact ionization (and thus hot-carrier effects) by allowing the high electric field at the drain region to extend into the n^- region.

The n^- dimensions and dopant concentration are determined by the desired improvement in breakdown voltage, short-channel threshold-voltage falloff, and other electrical characteristics [F.2]. However, the introduction of the n^- region increases the source-drain resistance and degrades the transistor current-driving capability to below that of a conventional MOS transistor with the same channel length.

In this work, the characteristic of source-drain series resistance and the effective channel length of an LDD MOS transistor at a small drain bias are studied. An analytical model for the source-drain series resistance is presented.

F.2. The Model

The measured channel resistance, $R_M \equiv V_{DS}/I_{DS}$, is [F.8,F.9]

$$R_M = R_{SD} + \frac{L_{eff}}{A \cdot [\, V_{GS}' - V_T \,]} . \tag{F.1}$$

where

$$A = \frac{G}{1 + U_0 \cdot [\, V_{GS}' - V_T \,]} , \quad G = \mu_S \cdot C_o \cdot W_{eff} . \tag{F.2}$$

$$R_{SD} = R_S + R_D . \tag{F.3}$$

Here, R_S is the source resistance, R_D is the drain resistance, U_0 is the mobility degradation coefficient, and G is the conductance coefficient. Voltage $V_{GS}' \equiv V_{GS} - I_{DS} R_S$ is the effective gate bias for the intrinsic active region, as explained in the insert of Fig. F.1. For a conventional MOS transistor, R_{SD} is a constant and plots of R_M versus mask-level (or drawn) channel length, L_{MK}, for different large gate biases at a fixed small drain bias intersect at one point where the channel-length reduction, $\Delta L \equiv L_{MK} - L_{eff}$, and source-drain series resistance, R_{SD}, are determined. The source-drain series resistance consists of the contact resistance, diffusion resistance, and spreading resistance resulting from the current-crowding effect [F.10].

The electric field emerging from the gate electrode modulates the carrier concentration of the gate-overlapped n^- region directly. The external n^- region is modulated by the gate through fringing fields. Therefore, source-drain series resistance is strongly gate-bias-dependent. Figure F.1 shows the plots of R_M versus L_{MK} for an LDD MOS transistor. Lines corresponding to different gate biases fail to intersect at a single point. The traditional method to electrically determine effective channel length and source-drain series resistance can not be directly applied because it assumes the effective channel length and source-drain series resistance are independent of the gate bias. Figure F.2 shows schematic diagrams of the effective channel at high and low gate biases. At a high V_{GS}-V_T bias condition, the amount of induced mobile carriers can be comparable to the

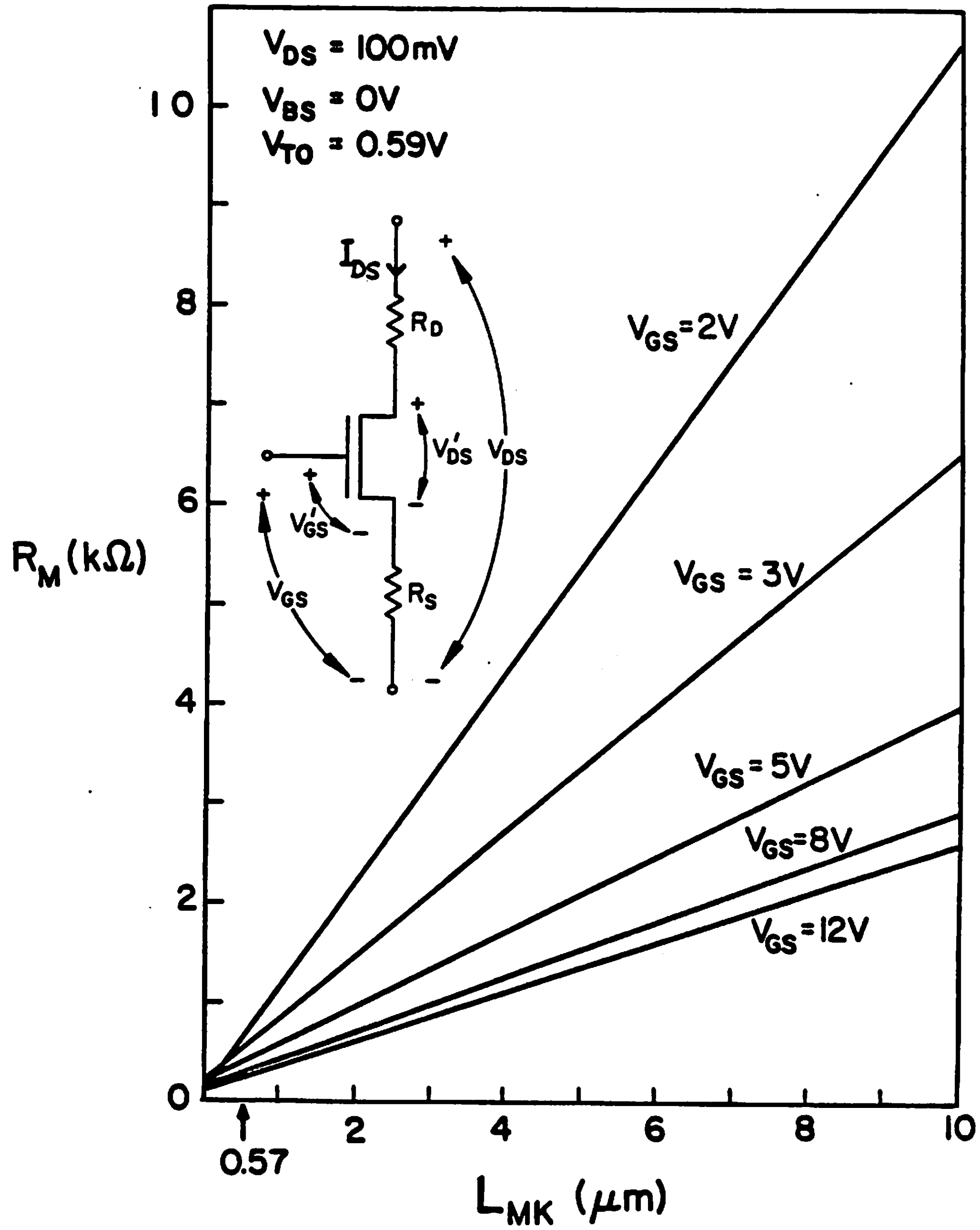
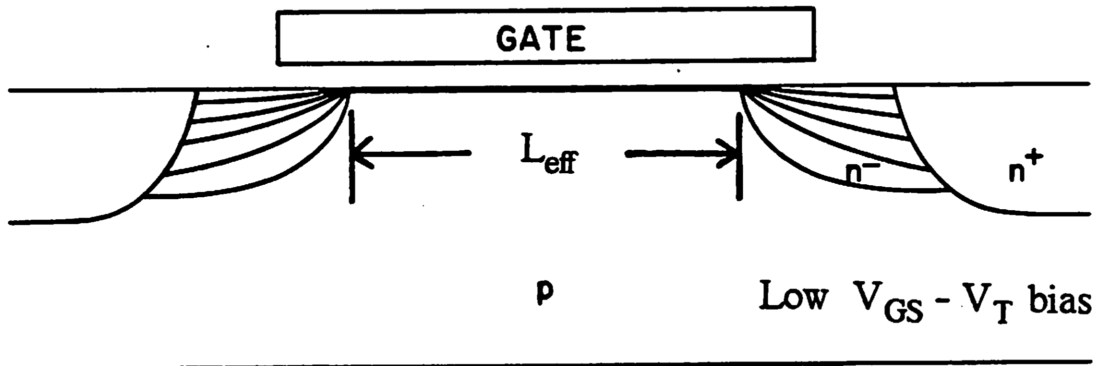
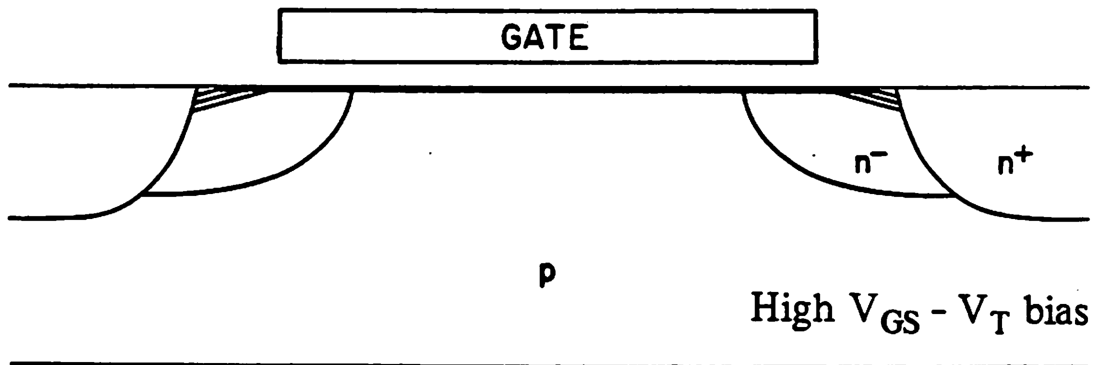


Fig. F.1 Measured channel resistance versus mask-level channel length for several gate biases. Definitions of different biasing voltages are shown in the insert.



(a)



(b)

Fig. F.2 Current flow patterns in an LDD MOS transistor.
(a) Low $V_{GS} - V_T$ condition.
(b) High $V_{GS} - V_T$ condition.

n^- region implant dose. However, the mobile carriers are confined within a layer which is much thinner than the n^- region junction. The conduction channel ends near the n^--to-n^+ junction. For a low V_{GS}-V_T bias condition, the conduction channel ends at the n^--to-"intrinsic active region" junction. The effective channel length is also gate-bias dependent.

The measured channel resistance at a small drain bias can be expressed as

$$R_M = R_{SD}(V_{GS}) + \frac{L_{eff}}{A \cdot [V_{GS} - V_T]} . \tag{F.4}$$

The gate-controlled n^- region can be regarded as a depletion-mode MOS device with the donor dopant as the threshold-voltage adjustment implant [F.11]. Let V_{Tn^-} denote the effective threshold voltage for this gate-controlled n^- region. The source-drain series resistance, R_{SD} , in Eq. (F.4) can be expressed as

$$R_{SD} = R_F + \frac{1}{B \cdot [V_{GS} - V_{Tn^-}]} \tag{F.5}$$

where R_F is the constant component of R_{SD}. The parameter B is a function of carrier mobility, gate-oxide capacitance, channel width, and the length of the n^- region. The method to determine R_F, B, and V_{Tn^-} from R_{SD} - V_{GS} characteristic is described in the next section with an example. With this interpretation of R_{SD} , L_{eff} in Eq. (F.4) should clearly be the intrinsic channel length (the length between the n^- regions).

Obviously, if one desires to determine the intrinsic channel length of an LDD transistor by plotting R_M versus L_{MK} for several V_{GS}'s, one should only use the low V_{GS} - V_T bias condition. However, any inaccuracy in the determination of V_T would cause significant error in this technique if V_{GS} - V_T is chosen to be too small. An appropriate gate bias (V_{GS}=V_{GSL}), which has enough safety margin above the threshold voltage and is not too large, should be judiciously chosen. The fact that R_{SD} is a

function of gate bias introduces a further complication. In order to minimize this difficulty, it is proposed to plot R_M versus L_{MK} for several substrate biases at a fixed (small) gate bias [F.11]. The procedure is illustrated in the next section. The complete expression for the measured channel resistance is

$$R_M = R_F + \frac{1}{B \cdot [\, V_{GS} - V_{Tn^-} \,]} + \frac{L_{eff} [\, 1 + U_0 \cdot (\, V_{GS}' - V_T \,) \,]}{G \cdot (\, V_{GS}' - V_T \,)} . \quad \text{(F.6)}$$

F.3. Experimental Results and Discussion

Test structures were designed with a set of poly-Si gate N-channel MOS transistors adjacent to one another, with L_{MK}= 0.5, 0.75, 1.5, 2, 3, 5, and 10 μm and W= 10 μm. The test transistors were fabricated on a P-type silicon wafer with resistivity of 1-2 Ω-cm. The LDD n^- region is formed by implanting 5×10^{12} cm^{-2} phosphorus at 80 Kev, followed by n^+ implant masked by 0.3 μm oxide spacer.

In performing drain current or channel resistance measurements, V_{DS} is chosen as small as 50 mV or 100 mV to minimize the drain bias effect on the device characteristics. The nominal threshold voltage for L_{MK}= 3 μm is found to be 0.59 V by linear extrapolation. From the criteria outlined in Section II V_{GSL} is chosen as 2.0 V, although the final results were insensitive to the choice of V_{GSL} within the range of 1 to 2 V above V_T. Figure F.3 shows the plots of R_M versus L_{MK} for V_{BS}= 0, -1, -2, and -3 V. The quantity ΔL = 0.57 μm is obtained. Electrical measurements show that the n^- regions from the source side and the drain side touch each other for L_{MK}= 0.5 μm. However, for L_{MK}= 0.75 μm, they do not touch. This agrees with the 0.57 μm value for ΔL. The purpose of varying V_{BS} is to vary V_T in Eq. (F.6). Clearly, this allows for the determination of L_{eff} and R_{SD} just as varying V_{GS} does (see Fig. F.1). It can be shown, however, that varying V_{BS} has smaller effect on V_{Tn^-} than on V_T. Herein lies the advantage of the

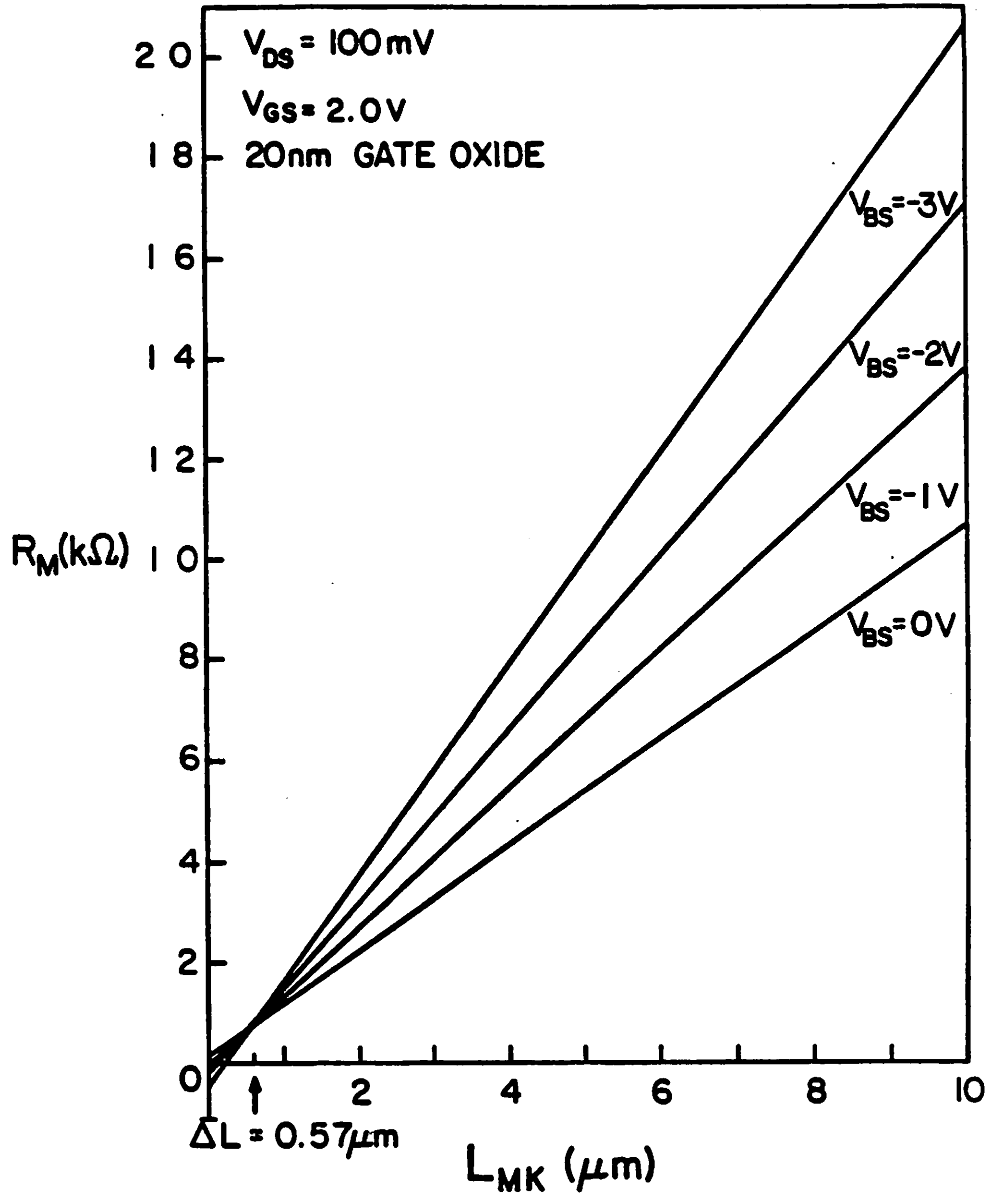


Fig. F.3 Measured channel resistance versus mask-level channel length for an LDD transistor with 20 nm gate oxide. Lines with different substrate biases intersect at one point from which ΔL is derived to be 0.57 μm.

substrate-bias-varying method.

The R_{SD} value for each V_{GS} bias is evaluated from Fig. F.1 at $\Delta L = 0.57\ \mu m$ and plotted against V_{GS} in Fig. F.4. The least-squares method is employed to find the values for the parameters R_F, B, and V_{Tn^-} in Eq. (F.5). In this example, $R_F = 173\ \Omega$, $B = 8.26 \times 10^{-4}\ V^{-1}\Omega^{-1}$, and $V_{Tn^-} = -0.38$ V are obtained.

Figure F.5 shows the measured and calculated drain current versus V_{GS} for $L_{MK} = 2$, 3, 5, and 10 μm. The solid lines are the results calculated from Eq. (F.6). The good agreement between the measured and calculated results verifies the accuracy of the model. The parameter values for G and U_0 are obtained by fitting the calculated results with the measured data for $L_{MK} = 3\ \mu m$, which gives $G = 7.52 \times 10^{-4}\ \mu m \cdot A \cdot V^{-2}$ and $U_0 = 0.045\ V^{-1}$.

Constant source-drain series resistance has been used to model LDD devices [F.12]. Calculated results obtained from Eq. (F.1), using a constant R_{SD}, are shown in Fig. F.5 with dashed lines for $L_{MK} = 1.5\ \mu m$ and 2 μm devices. The parameters used are $\Delta L = 0$ and $R_{SD} = 153\ \Omega$, which is the mean value of the intercepts between the straight lines and the vertical axis in Fig. F.1. A different R_{SD} value would only enlarge the error on the low V_{GS} or the high V_{GS} range. A large discrepancy between the measured and calculated (dashed lines) results reveals the limitation of the constant resistance model in accurate prediction of LDD device characteristics. The fact that the source-drain series resistance is gate-bias dependent, even for conventional phosphorus junction MOS transistors, has been proven with 2-D device simulations [F.13].

Recently, several papers have been published related to this topic [F.14]-[F.17]. Contrary to the understanding of Duvvury et al. [F.14], our substrate-bias-varying method does not depend on the assumption that depletion and enhancement devices have the same "substrate sensitivity" (sensitivity of V_T to V_{BS}) [F.15]. Wordeman et al.

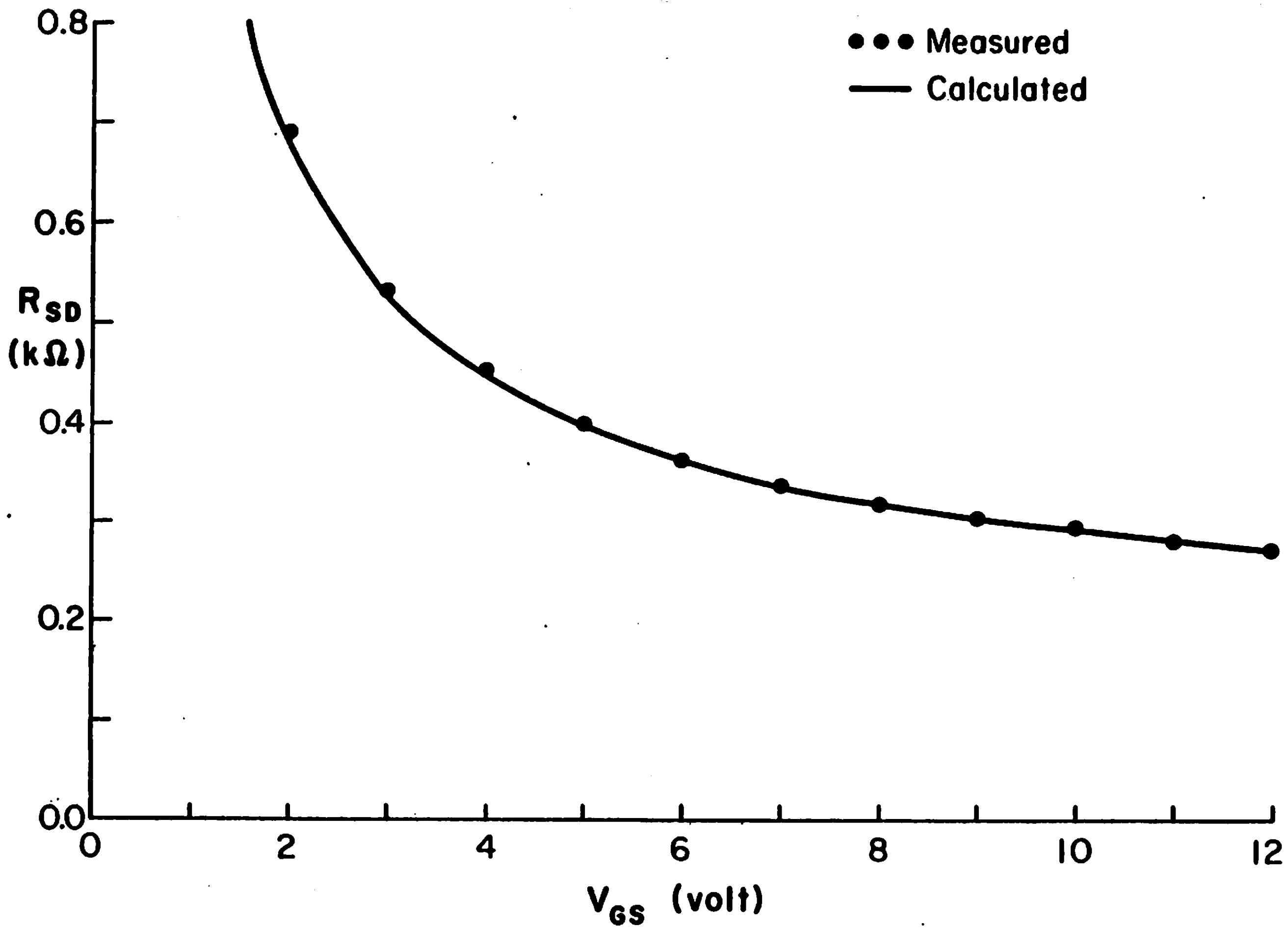


Fig. F.4 Source-drain series resistance versus gate bias. The parameter values for the model are $R_F = 173\ \Omega$, $B = 8.26\times10^{-4}\ V^{-1}\Omega^{-1}$, and $V_{Tn^-} = -0.38$ V.

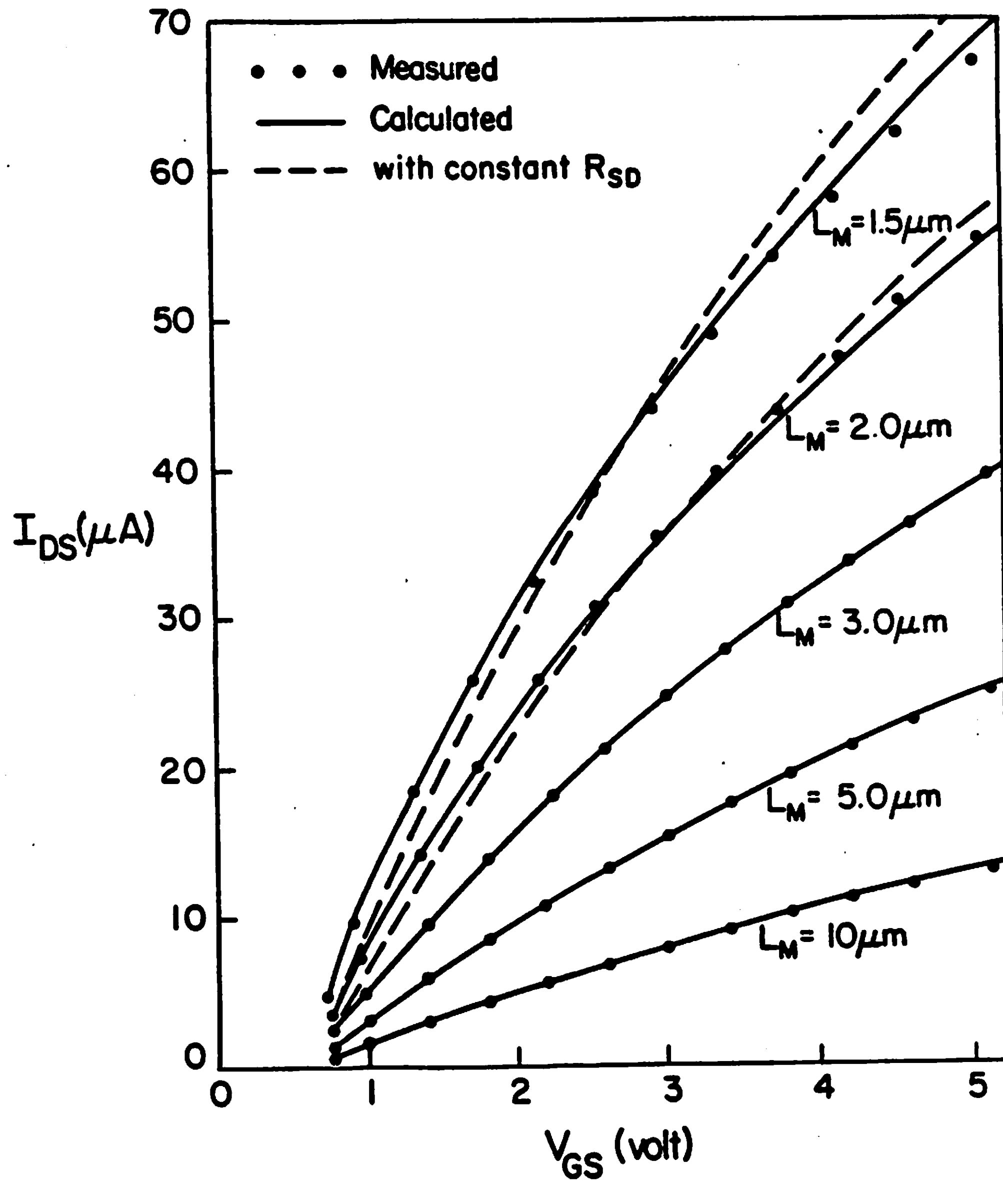


Fig. F.5 Comparison of measured and calculated drain current versus gate bias for V_{DS}= 50 mV, and V_{BS}= 0 V. The parameter values for the intrinsic active region are G= 7.52×10^{-4} $\mu m \cdot A \cdot V^{-2}$ and U_0= 0.045 V^{-1}.

[F.16] pointed out that, based on the study of a simplified MOS structure by using the two-dimensional device simulator FIELDAY, the substrate-bias-varying method might not yield the actual channel length. To circumvent the difficulty associated with the "substrate sensitivity" problem, the traditional gate-bias-varying method can be modified to electrically determine the effective channel length for LDD MOS transistors. In the plots of R_M versus L_{MK} for various gate biases, the local ΔL and R_{SD} corresponding to a specific gate bias can be determined from the intersection of two straight lines with the gate voltages adjacent to that specific gate bias.

F.4. Conclusion

The introduction of n^- regions makes an LDD MOS transistor behave differently from a conventional MOS transistor. The source-drain series resistance of the n^+ and n^- regions shows a strong dependence on the gate bias. Also, the apparent effective channel length can vary with gate bias. These special features make the traditional method to determine effective channel length and series resistance inapplicable. In this work, a simple and accurate model for the source-drain series resistance of lightly-doped-drain MOS transistors is presented. The model treats the n^- region as a depletion-mode MOS device.

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APPENDIX G

CHANNEL LENGTHS AND WIDTHS OF CONVENTIONAL AND LIGHTLY-DOPED-DRAIN MOS TRANSISTORS

LIST OF SYMBOLS

C_o gate capacitance per unit area.

X_{ox} gate-oxide thickness.

ΔL channel-length reduction.

ΔW channel width reduction (or expansion).

g_{DS} channel conductance.

I_{DS} drain current.

L_{eff} effective channel length.

L_{MK} mask-level channel length.

μ_s carrier mobility.

R_M measured channel resistance.

R_{SD} source-drain series resistance.

V_T transistor threshold voltage.

W_{eff} effective channel width.

W_{MK} mask-level channel width.

G.1. Introduction

Recent advances in VLSI technologies have successfully demonstrated submicron MOS transistors with the desired characteristics. Since the small-geometry MOS transistor characteristics are highly sensitive to device dimensions, accurate determination of the channel length, width and gate-oxide thickness is significantly important for the purposes of device analysis and process control in MOS VLSI technologies.

The lightly-doped-drain (LDD) structure can reduce the maximum channel electric field and thus ease the hot-carrier problem. The source-drain series resistance of an LDD transistor increases due to the existence of the n^- regions. The electric fields emerging from the gate electrode modulate the n^--region carrier concentration and make the source-drain series resistance strongly gate-bias dependent [G.1]. The traditional channel-resistance method does not work well for the determination of effective channel lengths and widths of LDD MOS transistors.

The goal of the work is to develop simple and accurate methods to electrically determine channel lengths, widths, and *in-situ* gate-oxide thicknesses of small-geometry conventional and LDD MOS transistors. In this report, the traditional channel-resistance technique to determine the effective channel length and the source-drain series resistance is reviewed first. An improved channel-resistance method is proposed to determine the effective channel width. Then, the capacitance method to determine channel lengths, widths, and *in-situ* gate-oxide thicknesses is described. The capacitance method applies to both conventional and LDD MOS transistors.

G.2. The Traditional Method to Determine Channel Lengths – An Overview

Several techniques, based on dc drain-current measurements, have been developed to extract the effective channel length and source-drain series resistance of conventional MOS transistors [G.2]-[G.5]. Among them, the channel-resistance technique originally proposed by Terada et al. [2] and re-formulated by Chern et al. [G.3] has been widely established as a defacto standard, primarily because the effective channel length and series resistance can be simultaneously obtained in a simple way. This method is based on the linear relationship between the measured channel resistance and effective channel length of an MOS transistor biased in the linear region.

G.2.1. Measurement Method

For an MOS transistor biased in the linear region, the measured channel resistance, $R_M \equiv V_{DS}/I_{DS}$, can be expressed as [G.3],

$$R_M = R_{SD} + A\,(L_{MK} - \Delta L) \qquad (G.1)$$

where

$$A = [\mu_s\, C_o\, W_{eff}\,(V_{GS} - V_T - 0.5\, V_{DS})]^{-1}\,. \qquad (G.2)$$

To avoid narrow-channel effects [G.6], wide test transistors are used. In Eq. (G.2), both the mobility (μ_s) and the threshold voltage (V_T) are implicit functions of the effective channel length [G.6]. At a small drain bias, dependence of these parameters on the effective channel length is minimized. In addition, application of a large gate bias (e.g. $V_{GS} \geqslant 6$ V) [G.3] further minimizes the effect of short-channel threshold-voltage falloff on the parameter A. If smaller gate biases are used ($V_{GS} \leqslant 5$ V in VLSI applications), then corrections to the threshold-voltage falloff have to be included to achieve high accuracy.

In plotting R_M versus L_{MK} for a set of adjacent transistors with the same channel width, a straight line is fitted through the data corresponding to a specific gate bias. If several lines with different gate biases are plotted, they intersect at one point, where ΔL and R_{SD} can be found simultaneously.

G.2.2. Experimental Results and Discussion

The test devices used in the experiments were N-channel MOS transistors fabricated by the Bell Labs SiGMOS process [G.7]. The substrate doping is 10^{15} cm^{-3} and the enhancement threshold implant is 8×10^{11} cm^{-2}. Measurement results on test transistors with L_{MK} = 1.5, 2, 2.5, 3, 4, and 5 μm and W_{eff} = 51 μm are presented here.

Figure G.1 shows the plots of measured channel resistance versus mask-level channel length for $V_{GS} - V_T$ = 2, 4, 6, 8, and 10 V. The least-squares method is applied twice. First, it is used to fit a straight line through the data for one specific gate bias.

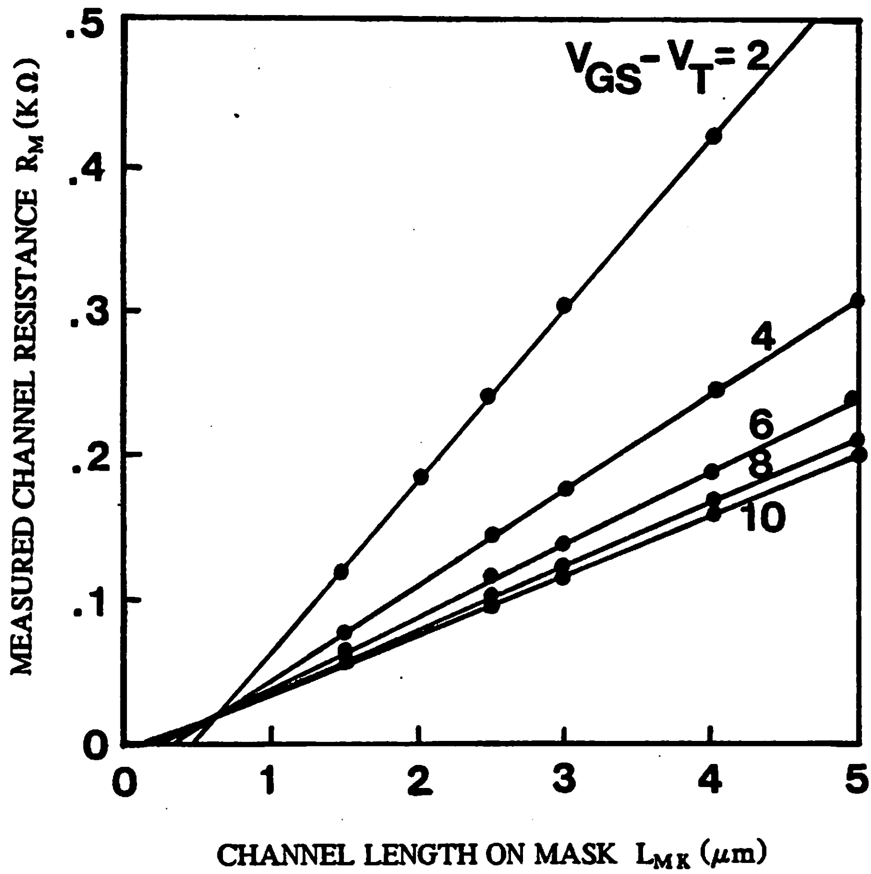

Fig. G.1 Measured channel resistance versus mask-level channel length for several gate biases.

Second, it is used to find the intersection of the straight lines [G.2], which gives $\Delta L =$ 0.62 μm and $R_{SD} = 17.8\ \Omega$.

The dc measurement results are sensitive to the parasitic resistance of the probes, especially for thin-oxide or short-channel devices for which the contact resistance is not negligible when compared to the channel resistance. The probes used in the measurements are carefully sharpened and cleaned so that probe to metal-pad contact resistance is always smaller than 2 Ω. An overall correlation coefficient better than 0.9999 can be achieved with this method.

G.3. An Improved Channel-Conductance Method to Determine Channel Widths

The expression for the measured channel resistance of an MOS transistor biased in the linear region can be rearranged to have the W_{eff} term appear in the numerator,

$$\frac{1}{R_M - R_{SD}} = W_{eff} \frac{\mu_s C_o \cdot [V_{GS} - V_T - 0.5\ V_{DS}]}{L_{eff}} . \tag{G.3}$$

Straightforward application of the channel resistance method to determine transistor channel widths does not work well, as was noted by Ma et al [G.8], because the source-drain series resistance varies with the channel width. No linear relationship exists between the measured quantity and the mask-level channel width. This is in sharp contrast to the fact that source-drain series resistance is constant among the set of adjacent transistors with the same width and different channel lengths, which were used in channel-length determination. Kotecha et al. [G.9] have already pointed out that the effective electrical channel width varies with both gate and substrate biases. However, their measurement method was not reported. Neglecting the source-drain series resistance, Ma et al. [G.8] determined W_{eff} by plotting g_{DS} (or I_{DS}) versus W_{MK} for different gate voltages at a small drain bias. That method can not be directly extended to short-channel and thin-oxide devices where the source-drain series resistance is comparable to

the intrinsic channel resistance. For example, the typical R_{SD}/Rch ratio is about $20\Omega/200\Omega$ for a conventional MOS transistor with $X_{ox} = 20$ nm, $W_{eff} = 50$ μm, $L_{eff} = 4$ μm and biased at $V_{GS} = 5$ V.

The goal of this work is to develop a simple and accurate channel-conductance method to determine the effective channel widths of MOS transistors [G.10]. A minimum of four test transistors are needed: two different channel widths with two different channel lengths for each width. One measurement at a large gate bias for each transistor is sufficient to obtain full characterization.

G.3.1. Measurement Method

The expression for the measured channel resistance of an MOS transistor biased in the linear region can be rewritten as

$$R_M = R_{SD} + \frac{L_{eff}}{\mu_S C_o W_{eff} \cdot [V_{GS} - V_T - 0.5 V_{DS}]} \quad (G.4)$$

The procedures of the first part of this improved channel-width method are similar to those of the traditional channel-length method [G.3]. In plotting R_M versus L_{MK} for a set of transistors with the same channel width, a straight line is fitted through the data corresponding to a specific gate bias by the linear regression technique. In this plot, notice that the values of the intrinsic channel-conductance coefficient ($G_i = \mu_s C_o W_{eff}(V_{GS} - V_T - 0.5V_{DS})$), are given by the inverse of the slopes of the straight lines, and are linearly dependent on the effective width at a given gate bias. The above procedures are repeated for sets of transistors with different channel widths. All G_i's obtained at the same gate bias for various channel widths are plotted against W_{MK}, and a straight line is fitted through them by the linear regression again. The x-axis intercept in this plot gives the channel width offset, ΔW. Similarly, by plotting G_i's for other gate biases, the gate-bias dependency of ΔW can be obtained.

To minimize the influence of the threshold-voltage variations caused by short-channel effects, large gate biases are used. If short-channel transistors are used in the experiments, corrections to the threshold-voltage falloff have to be included to achieve high accuracy.

G.3.2. Experimental Results and Discussion

Figure G.2 shows the plots of intrinsic channel conductivity versus mask-level channel width for $V_{GS} - V_T = 4, 6, 8,$ and 10 V from N-channel MOS transistors fabricated using a recessed LOCOS process. The measured ΔW is positive, as expected. V_{DS}= 50 mV is used in our experiments. The correlation coefficient is better than 0.9999. The insert in Fig. G.2 shows ΔW as a function of $V_{GS}-V_T$.

A qualitative illustration of the dependence of channel width on the gate bias is shown in Fig. G.3. The edges of the gate structure are on top of the tapered oxide regions. Therefore, the effective channel width is gate-bias and substrate-bias dependent. For transistors fabricated by a LOCOS process, lateral diffusion of the channel-stop implant magnifies the dependence. The effective channel width is larger at a large gate bias and a small substrate bias, because a larger portion of the edge region is inverted. The effective channel width increases as the gate bias increases, and saturates when all the edge regions are inverted.

G.3.3. Summary

A simple and accurate channel-conductance method to determine effective channel widths of MOS transistors has been described. Accuracy in channel-width determination better than 0.1 μm and correlation coefficient better than 0.9999 were obtained. This method circumvents the difficulty of different source-drain series resistances associated with different channel widths and can be applied to minimum feature-size MOS transistors fabricated by various technologies.

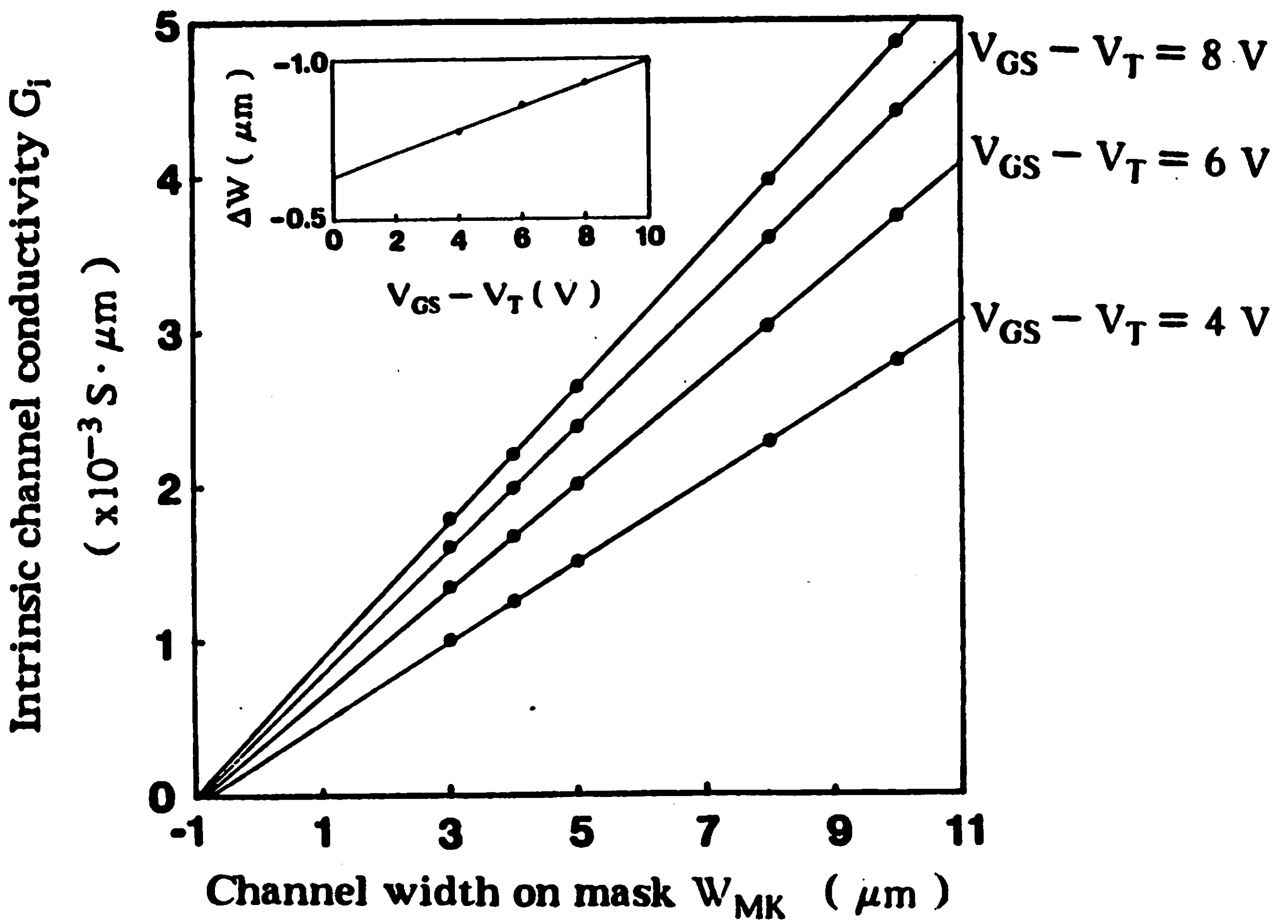

Fig. G.2 Intrinsic channel conductivity versus mask-level channel width. Linear dependence of ΔW on $V_{GS}-V_T$ can be found in the insert.

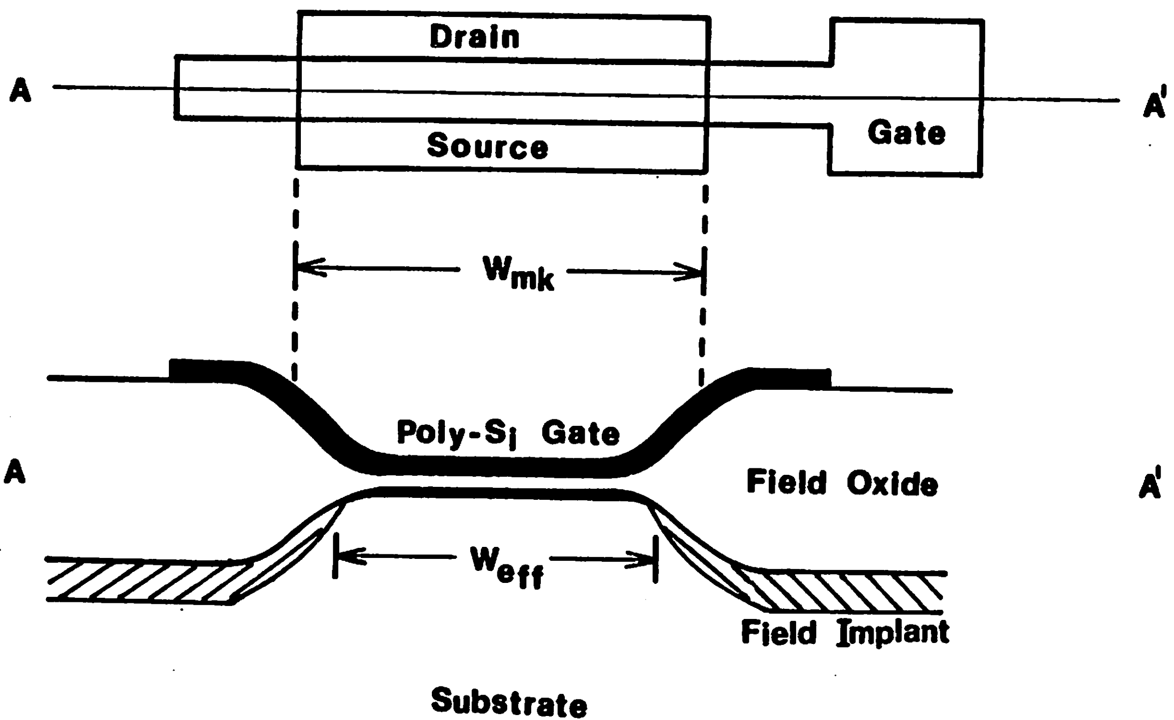

Fig. G.3 Width cross-section of an MOS transistor from a recessed LOCOS process. Notice that the edges of the gate structure is on top of the tapered-oxide regions.

G.4. The Capacitance Method to Determine Channel Lengths and in-situ Gate-Oxide Thicknesses for Conventional and Lightly-Doped-Drain MOS Transistors

A description of the capacitance measurements for small-geometry MOS transistors can be found in Appendix H. The plot of raw measured gate capacitance versus gate bias for a conventional MOS transistor with $W_{eff} = 51\ \mu m$ and $L_{MK} = 5\ \mu m$ is shown in Fig. G.4. The transistor threshold voltage is 0.32 V. When the gate bias increases from -5 V to 5 V, the transistor goes through three distinct regions of operation: accumulation, depletion, and strong inversion. In the accumulation region, the measured gate capacitance does not contain any component from the intrinsic gate area. The measured capacitance remains unchanged in this operation region. When the transistor enters the depletion region, the fringing fields between the gate and sidewalls of the source and drain junctions cause the measured gate capacitance to increase slightly [G.11]. As the gate bias reaches the threshold voltage, the transistor enters the strong inversion region. Once the inversion layer is formed in the intrinsic gate area, the measured gate capacitance will increase asymptotically to a maximum value. In the experiments, -5 V and 5 V are chosen as the two gate biases for which the transistor is in the strong accumulation and the strong-inversion regions, respectively. The intrinsic gate capacitance is obtained by subtracting the parasitic capacitance, determined by biasing the transistor in strong accumulation, from the measured capacitance with the transistor biased in strong inversion.

For LDD devices, the channel length is found to depend on the gate bias [G.1]. To find the intrinsic channel length corresponding to the spacing between the n^- regions, 0 V in place of -5 V is used such that the n^- regions are not depleted and the channel surface is not inverted because the threshold voltage of the LDD devices used in these experiments is 0.58 V.

G.4.1. Measurement Method

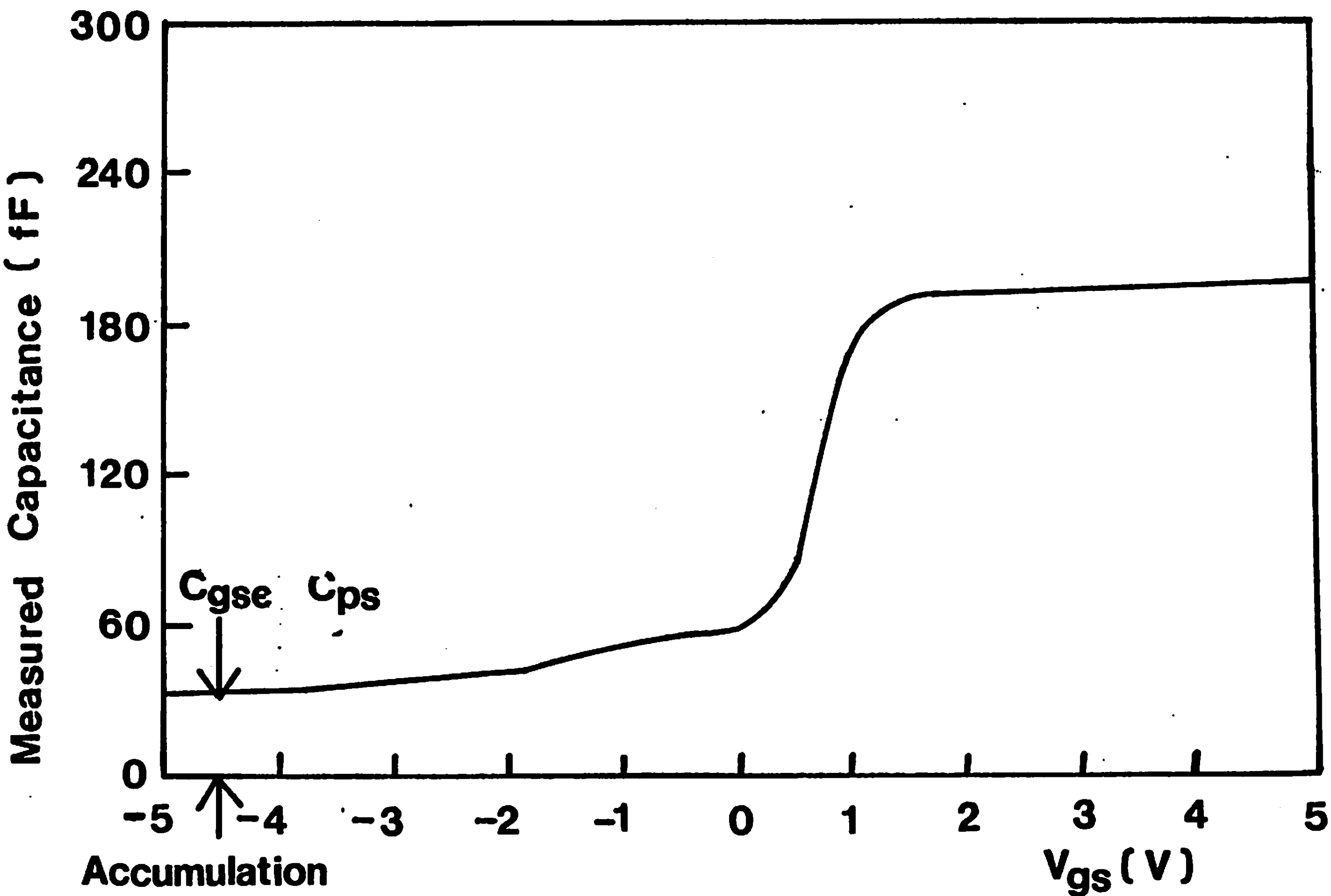

Fig. G.4 (b) Measured gate capacitance versus gate bias for a device with W_{eff} = 51 μm and L_{MK} = 5 μm. The gate bias is ramped from -5 V to 5 V. Transistor threshold voltage is 0.32 V.

The capacitance method to determine the channel length and gate-oxide thickness is conceptually simple [G.12]. The intrinsic gate capacitance can be expressed as

$$C_{ox} = \frac{\epsilon_{ox}}{X_{ox}} W_{eff} L_{eff} \tag{G.5}$$

In plotting C_{ox} versus L_{MK} for a set of transistors with the same channel width, a straight line is fitted through the data with the least-squares technique. The x-axis intercept in this plot gives ΔL. If the channel width is known, gate-oxide thickness can be determined from the slope of the straight line.

G.4.2. Experimental Results and Discussion

The conventional transistors used in the experiments have been described in Section G.2.2. From an ellipsometer measurement, the gate-oxide thickness is found to be 20.5 nm.

The plot of intrinsic gate capacitance versus mask-level channel length for conventional MOS transistors is shown in Fig. G.5. The x-axis intercept of the straight line gives $\Delta L = 0.57$ μm. The correlation coefficient for the straight line is better than 0.9999. Using $W_{eff} = 51$ μm and the slope in Fig. G.5, the gate-oxide thickness is determined to be 21.1 nm. To check the results on ΔL, the channel-resistance method is applied to the same set of transistors. Probe to metal-pad resistance adds to the source-drain series resistance, which could be comparable to the intrinsic channel resistance for thin-oxide and short-channel devices. In the capacitance method, the intrinsic capacitive impedance ($1/\omega C$) is on the order of 100 MΩ in the experiments, which is much larger than the source-drain series resistance. Hence, the capacitance method is not sensitive to the probe to metal-pad contact resistance.

The threshold voltage of the LDD transistors used in the experiments is 0.58 V. Measured results on test transistors with L_{MK} = 1.5, 2, 3, 5, and 10 μm and $W_{eff} = 8.8$ μm are presented here. The plot of intrinsic gate capacitance versus mask-level channel

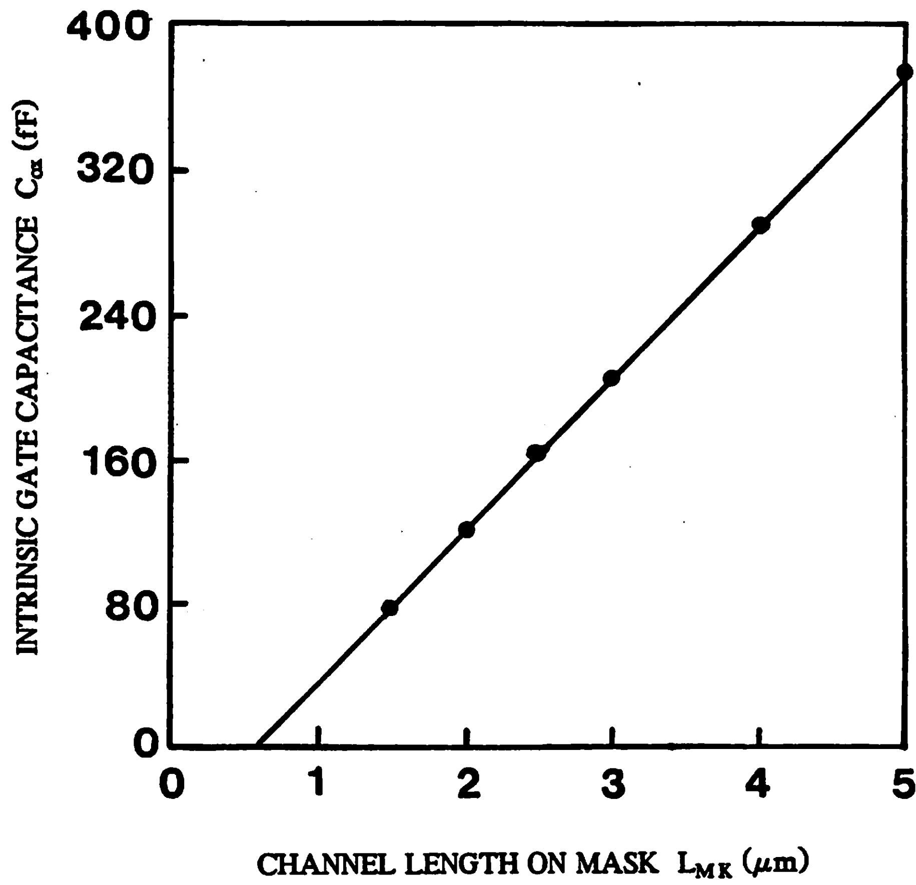

Fig. G.5 Intrinsic gate capacitance versus L_{MK} for conventional MOS transistors.

length for LDD MOS transistors is shown in Fig. G.6. The x-axis intercept of the straight line gives $\Delta L = 0.34\ \mu m$. The correlation coefficient for the straight line is better than 0.9995. Using $W_{eff} = 8.8\ \mu m$ and the slope obtained from Fig. G.6, the gate-oxide thickness is determined to be 19.5 nm. Since the threshold voltage is 0.58 V, the transistor is in the depletion region when it is biased at $V_{GS} = 0$ V. Gate capacitance measured at $V_{GS} = 0$ V contains a capacitive component due to the fringing fields between the gate and side walls of n^- regions. This causes the intrinsic gate capacitance and thus the effective channel length to be smaller than the actual values. For a conventional MOS transistor, the channel-side fringing-field capacitance could be as much as 10 percent of the intrinsic gate capacitance [G.11]. However, this fringing-field capacitance will not give rise to an error larger than $0.1\ \mu m$ in the ΔL determination of LDD MOS transistors, which is estimated to be the accuracy limit of the electrical methods.

G.4.3. Summary

A simple method to determine the channel lengths and *in-situ* gate-oxide thickness of MOS transistors is described. The method is based on the linear relationship between the intrinsic gate capacitance and the effective channel length. Measurements from two gate biases on devices of different channel lengths are sufficient to obtain a full characterization. In contrast to the channel-resistance method, the accuracy of the capacitance method is independent of the source-drain series resistance. It can be used for conventional as well as lightly-doped-drain devices. Channel length and gate-oxide thickness data determined by this method has been presented for conventional and LDD MOS transistors. For conventional MOS transistors, the new method agrees with the traditional channel-resistance method to better than $0.1\ \mu m$.

G.5. The Capacitance Method to Determine Channel Widths and in-situ Gate-Oxide Thicknesses for Conventional and Lightly-Doped-Drain MOS Transistors

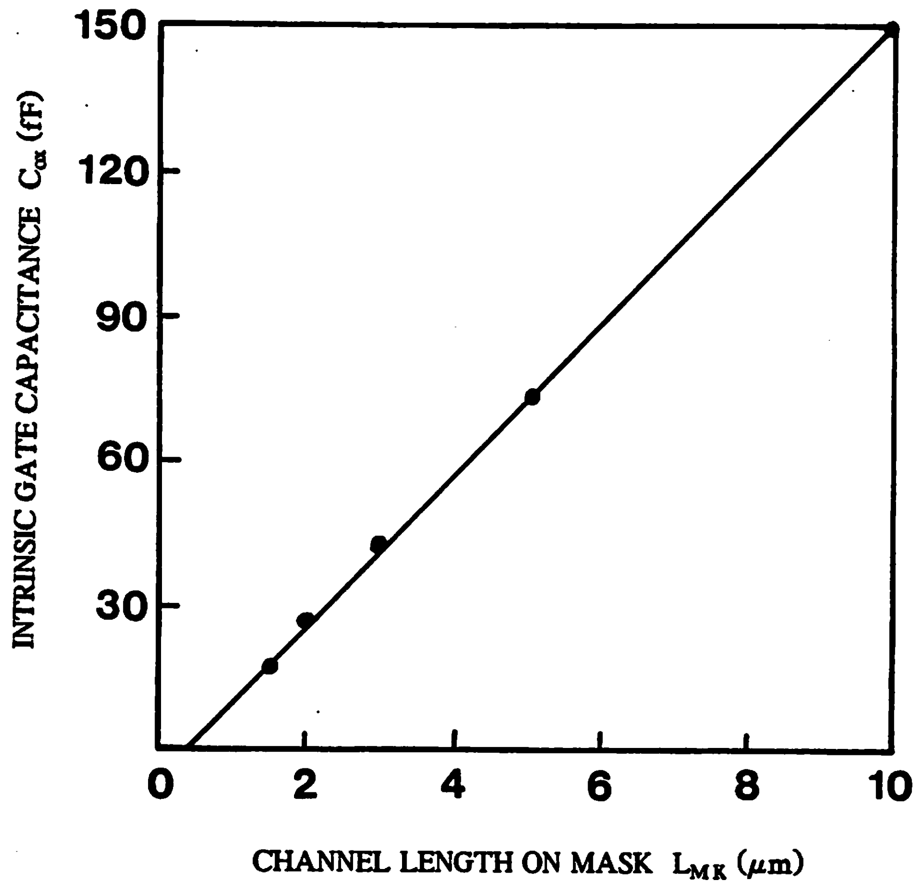

Fig. G.6 Intrinsic gate capacitance versus L_{MK} for LDD MOS transistors. Transistor threshold voltage is 0.58 V.

The capacitance method to determine the channel width and *in-situ* gate-oxide thickness from the measured C_{ox}-W_{MK} characteristics is described. Only standard test transistors are required. The method is illustrated by application to conventional and LDD MOS transistors. The validity of this method is supported by the close agreement between results obtained when it is applied to both long-channel devices and short-channel devices.

G.5.1. Measurement Method

The capacitance method to determine the channel width and gate-oxide thickness is simple [13]. The intrinsic gate capacitance can be expressed as

$$C_{ox} = \frac{\epsilon_{ox}}{X_{ox}} W_{eff} L_{eff} . \tag{G.6}$$

In plotting C_{ox} versus W_{MK} for a set of transistors with the same channel length, a straight line is fitted through the data with the least-squares technique. The x-axis intercept of the straight line gives ΔW. If the channel length is known, the gate-oxide thickness can be determined from the slope of the straight line.

G.5.2. Experimental Results and Discussion

The conventional devices used in our experiments were N-channel MOS transistors. The substrate doping is 5×10^{14} cm^{-3}. The transistor threshold voltage is -0.11 V. Measured results on test transistors with W_{MK} = 5, 8, 10, and 25 μm and L_{eff} = 2.4 and 7.4 μm are presented here. From an ellipsometer measurement, the gate-oxide thickness is found to be 27.0 nm.

The plot of intrinsic gate capacitance versus mask-level channel width for conventional MOS transistors with L_{eff} = 7.4 μm is shown in Fig. G.7. A solid line is fitted through the data. The x-axis intercept of the straight line gives ΔW = 1.12 μm. The

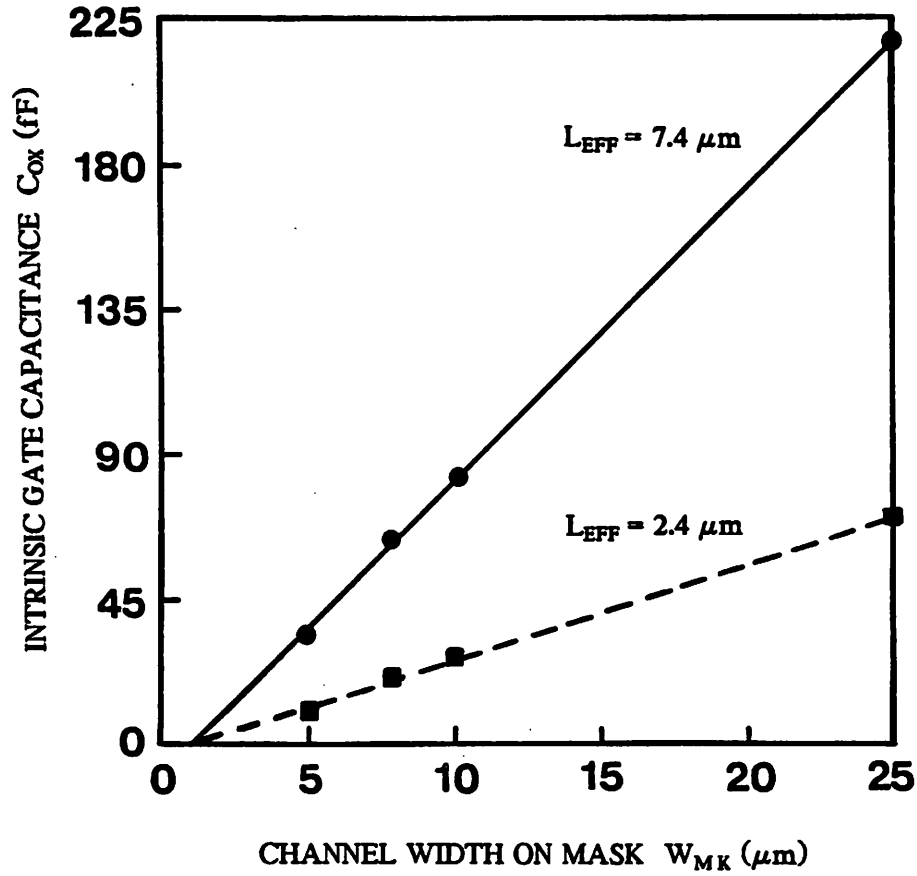

Fig. G.7 Intrinsic gate capacitance versus mask-level channel width (W_{MK}) for conventional MOS transistors. $\Delta W = 1.12$ and 1.16 μm are obtained for the sets of transistors with $L_{eff} = 7.4$ and 2.4 μm, respectively.

correlation coefficient for the straight line is better than 0.9999. By using L_{eff} = 7.4 μm and the slope of the straight line, the gate-oxide thickness is determined to be 27.8 nm. To check the result on ΔW, the capacitance method is applied to a set of transistors with L_{eff} = 2.4 μm. The plot of intrinsic gate capacitance versus mask-level channel width for this set of transistors is also shown in Fig. G.7. A dashed line is fitted through the data. ΔW = 1.16 μm is obtained with correlation coefficient better than 0.9999 for the straight line. The ΔW values obtained from the two sets of transistors are within 0.05 μm.

The threshold voltage of the LDD transistors is 0.58 V. Measured results on test transistors with W_{MK} = 2, 3, 5, 7, and 10 μm and L_{eff} = 9.7 μm are presented here. The plot of intrinsic gate capacitance versus mask-level channel width for LDD MOS transistors is shown in Fig. G.8. A straight line is fitted through the data. The x-axis intercept of the straight line gives ΔW = 1.17 μm. The correlation coefficient for the straight line is better than 0.9999. By using L_{eff} = 9.7 μm and the slope of the straight line, gate-oxide thickness is determined to be 19.6 nm.

G.5.3. Summary

A simple and accurate method to determine the channel width and gate-oxide thickness has been described. This method requires only one curve that represents the relationship between the intrinsic gate capacitance and the effective channel width. Correlation coefficients better than 0.9999 are obtained when this method is applied to conventional and LDD MOS transistors.

G.6. Conclusion

The transistor channel lengths and widths are the major parameters under a circuit designer's control. Accurate characterization of the effective lengths and widths of MOS

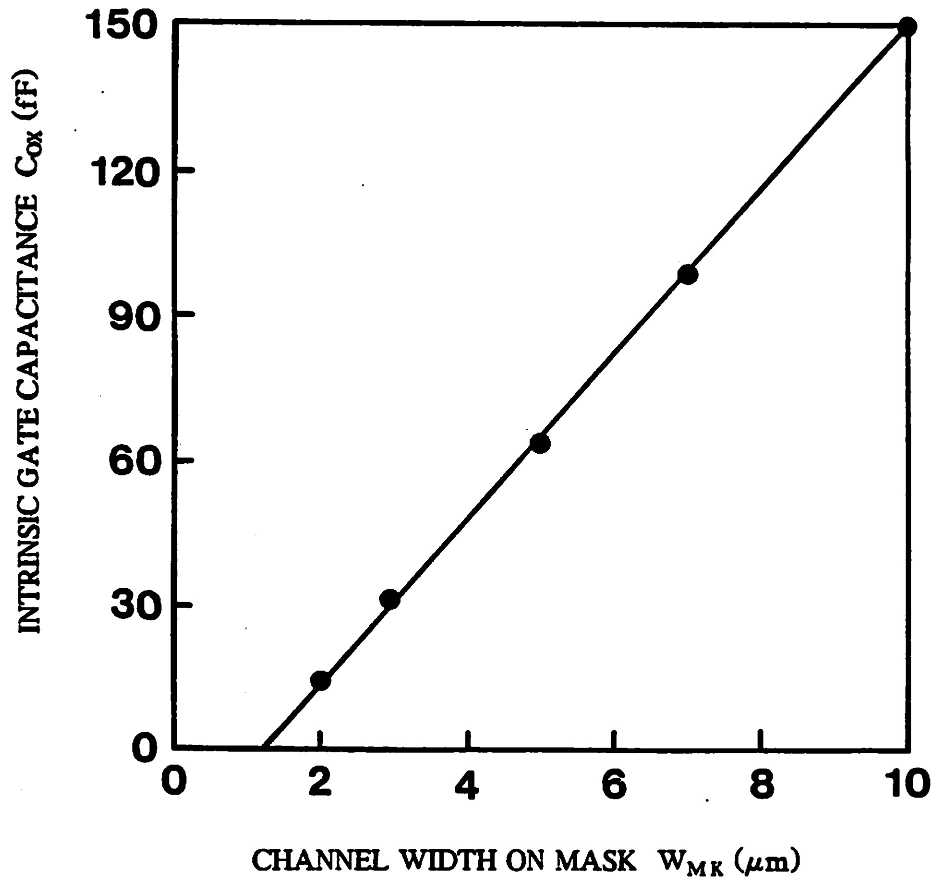

Fig. G.8 Intrinsic gate capacitance versus mask-level channel width (W_{MK}) for LDD MOS transistors. $\Delta W = 1.17\ \mu m$ is obtained.

transistors is of paramount importance in designing VLSI circuits because the characteristics of the submicron minimum-size transistors used in VLSI circuits are highly sensitive to the device dimensions. The channel-resistance method has been extended to accurately measure the channel widths of MOS transistors. The capacitance method has also been successfully applied to measure the effective channel lengths and widths of conventional and LDD MOS transistors. The capacitance method is insensitive to source-drain series resistances in contrast with the widely-used channel-resistance method.

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APPENDIX H

MEASUREMENT AND MODELING OF SMALL-GEOMETRY MOS TRANSISTOR GATE CAPACITANCES

H.1. Introduction

Precise characterization of intrinsic gate capacitances of small-geometry MOS transistors is very important in the design of MOS VLSI circuits. Recent progress in integrated-circuit technologies has advanced device geometries into the submicron range. The micron and submicron transistors show prominent short-channel effects and knowledge of the small-geometry effects on device characteristics becomes extremely important.

The intrinsic capacitances of short-channel MOS transistors have not been widely investigated, mainly due to the lack of accurate measurement techniques for characterizing extremely small capacitances (on the order of fento Farads). The goal of this research is to develop a direct-on-wafer technique capable of measuring micron and submicron transistor capacitances and to derive a physics-based short-channel transistor capacitance model useful for process optimization as well as advanced circuit simulation. The direct-on-wafer measurement method is simple, fast, and gives accurate results.

H.2. Capacitance Measurement Methods -- An Overview

Various methods are available to measure capacitance. The traditional bridge method [H.1] is suitable for two-terminal elements. For the measurement of four-terminal MOS transistor capacitances, the four-port-nulling method [H.2,H.3] has been used because a typical LCR meter or impedance analyzer is sufficient. The four-port-nulling method is typically applied to large (100 μm by 100 μm or larger) transistors [H.2]. The measurement limit of commercially-available capacitance meters is probably around 1 pF [H.4]. To accurately characterize small-geometry MOS transistor

capacitances down to the fF range, new measurement techniques are needed. On-chip circuitry measurement methods, proposed by Iwai et al. [H.5] and Paulos et al. [H.4], were the results of recent efforts in this area. Such methods can achieve good measurement resolution.. This section gives a brief review of different capacitance measurement methods. A new direct-on-wafer capacitance method that has been developed will be described in the next section.

H.2.1. The Bridge Method

The Wheatstone bridge method is commonly used in resistance measurement. Balance is achieved by adjusting the resistance in one arm so that no current flows through the detector. For the measurement of capacitance and inductance, an ac bridge is required. Figure H.1 shows the schematic diagram of the general ac bridge which is equivalent to the Wheatstone bridge except that the arms consist of impedance elements rather than resistance elements. The dc voltage source is replaced by an ac signal source, and the detector must be able to detect ac signals. The condition of balance is [H.1]

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_C} \tag{H.1}$$

H.2.2. The Four-Port-Nulling Method

The operation of the four-port-nulling method for MOS transistor capacitance measurements has been described in detail by Ward [H.2] and Conilogue [H.3]. The test instrument interfaces to the outside world through four measurement ports: low current, low potential, high current and high potential. The Hewlett-Packard series of LCR meters and impedance analyzers are based on the four-port-nulling measurement scheme [H.2]. Figure H.2 shows the equivalent circuit for the MOS transistor interelectrode capacitance measurement. Both the connections of the high potential port to the high current port and the low potential port to the low current port should be made as close to the physical device as possible in order to minimize the effect of stray

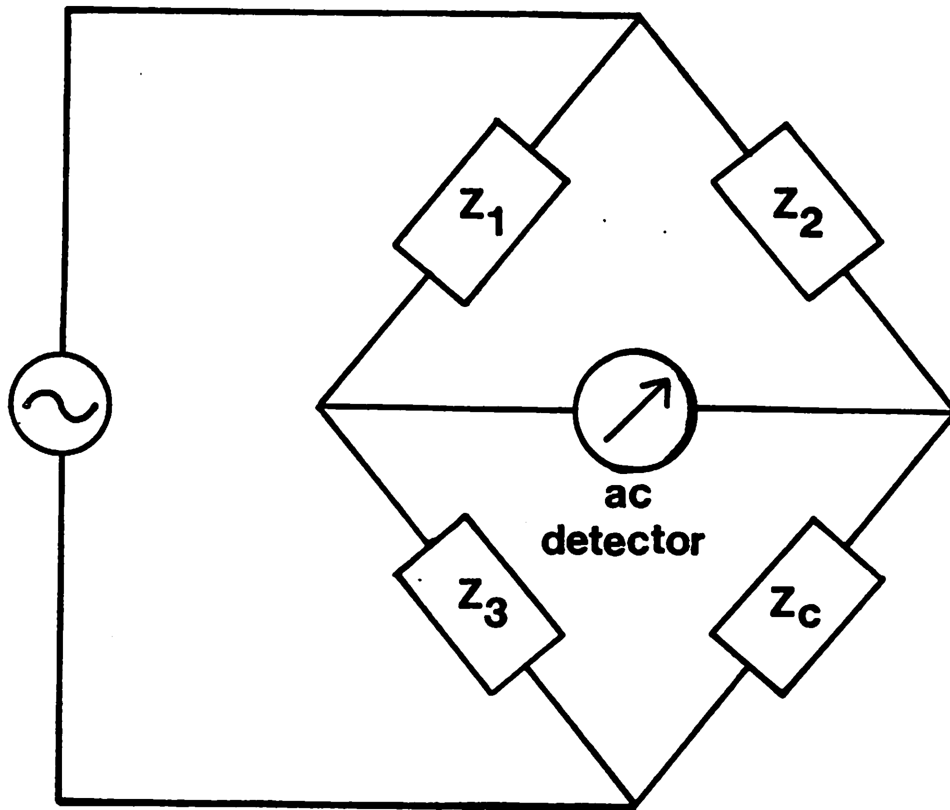
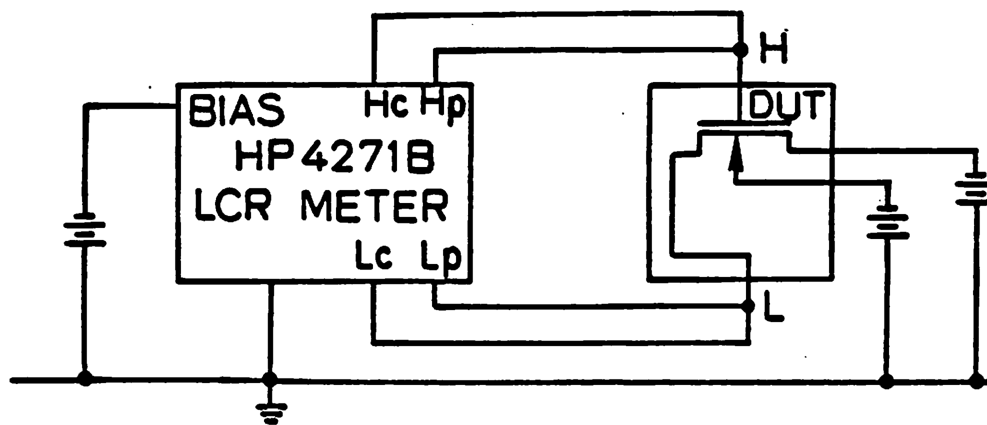


Fig. H.1 Generalized a.c. bridge circuit.



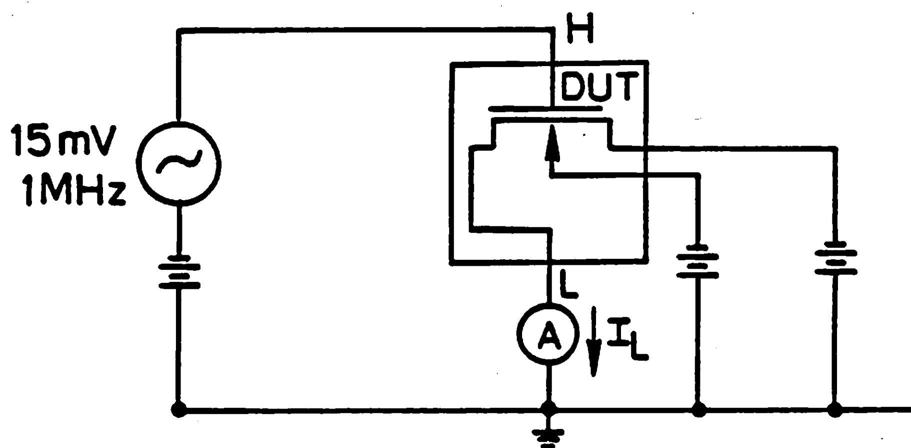


Fig. H.2 Equivalent circuit for inter-electrode capacitance measurement using an impedance analyzer [2].

capacitance on the measurement results. The ac test signal is applied to the transistor under test via the high current port. The second signal source in the low current port is adjusted to produce a null condition at the low terminal. The magnitude of the ac test signal is monitored at the high potential port, while the response information is sensed at the low potential port.

So far, the capacitance measurements at the source and drain are restricted to long-channel devices. Phase information is required to separate the capacitive component of current from the conductive component. For reasonable accuracy, the capacitive component must be an appreciable fraction of the conductive component. This fraction is proportional to the test frequency and the square of the channel length. The maximum test frequency is limited by the op-amp bandwidth, therefore, the minimum channel length is constrained [H.6].

H.2.3. The Open-Loop On-Chip Circuitry Method

The open-loop technique using on-chip circuits to measure small parasitic capacitances was first reported by Iwai and Kohyama [H.7]. This technique has been extended to measure gate capacitances of small-geometry MOS transistors [H.5], [H.8]-[H.11]. Figure H.3 shows one of the three circuit configurations necessary to determine the gate-to-drain (C_{gd}), gate-to-source (C_{gs}), and gate-to-bulk (C_{gb}) capacitances. The ac equivalent circuit is shown in Fig. H.4. By subsequently applying the ac test signal to the drain, source, and substrate terminals, the following three relationships can be obtained [H.8]:

$$C_{gd} = v_{o1} (C_{gd} + C_{gs} + C_{gb} + C_{ref}) . \tag{H.2}$$

$$C_{gs} = v_{o2} (C_{gd} + C_{gs} + C_{gb} + C_{ref}) . \tag{H.3}$$

$$C_{gb} = v_{o3} (C_{gd} + C_{gs} + C_{gb} + C_{ref}) . \tag{H.4}$$

The above equations are solved simultaneously to determine the three gate capacitances.

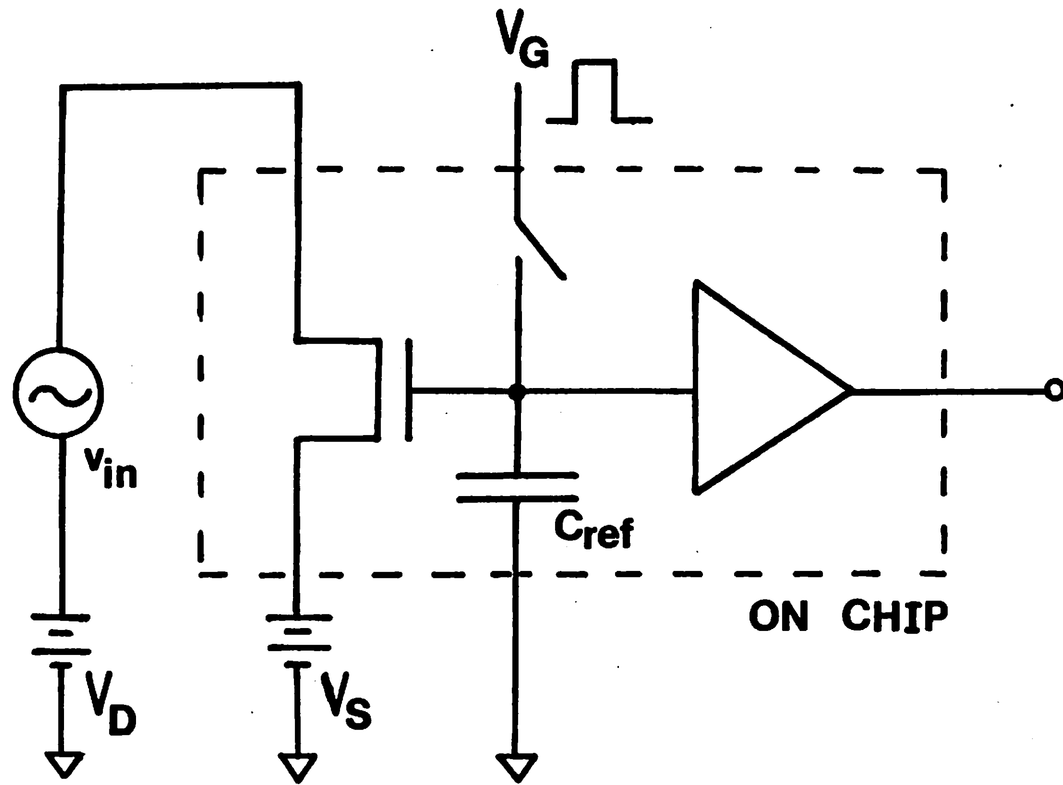


Fig. H.3 Open-loop capacitance measurement technique of Iwai et al. [6].

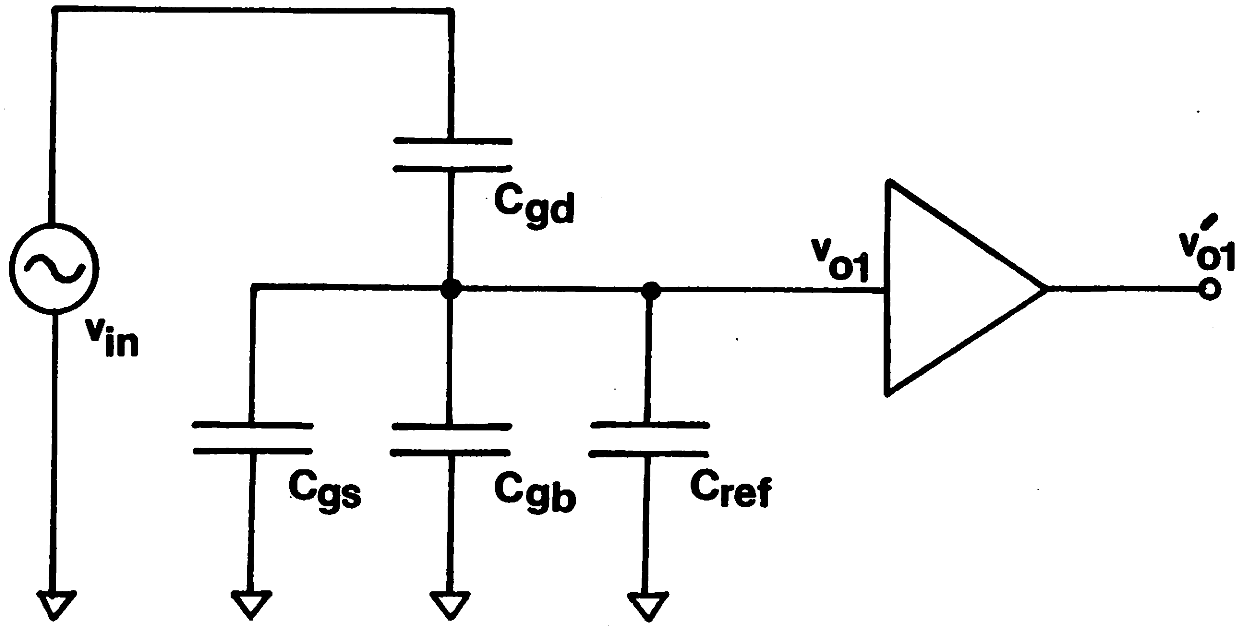


Fig. H.4 a.c. equivalent circuit for Fig. 3.

$$C_{gd} = C_{ref} \cdot \frac{v_{o1}}{[\, v_{in} - (\, v_{o1} + v_{o2} + v_{o3}\,)\,]}\,. \tag{H.5}$$

$$C_{gs} = C_{ref} \cdot \frac{v_{o2}}{[\, v_{in} - (\, v_{o1} + v_{o2} + v_{o3}\,)\,]}\,. \tag{H.6}$$

$$C_{gb} = C_{ref} \cdot \frac{v_{o3}}{[\, v_{in} - (\, v_{o1} + v_{o2} + v_{o3}\,)\,]}\,. \tag{H.7}$$

As was noted by Paulos et al. [H.4], the open-loop capacitance measurement technique has some drawbacks which makes it inferior to the closed-loop technique. The input capacitance of the amplifier, which is strongly bias-dependent, affects the reference capacitance value. The switch in Fig. H.3 is used to establish dc bias on the floating gate and to calibrate the actual ac gain of the output-buffer circuit. Charge injection from the switch when it turns off perturbs the dc bias of the floating gate. Complicated compensation is required to achieve the desired gate bias.

H.2.4. The Closed-Loop Coulombmeter Method

A closed-loop technique using on-chip circuits to measure MOS transistor capacitances has been reported by Paulos et al. [H.4]. This technique is an extension of the previously-proposed coulombmeter method [H.6]. The method is shown in Fig. H.5. Drain, source, bulk biases are applied directly to the transistor terminals, while the gate bias is applied through the noninverting node of the amplifier. A switch is required to periodically establish the dc bias condition for the gate terminal. Similar to the open-loop technique, it suffers from the problem of charge-injection from the switch [H.4]. The closed-loop approach has the following advantages over the open-loop approach. First, any of the three gate capacitances , C_{gd}, C_{gs}, and C_{gb}, can be independently measured by applying the ac test signal to the corresponding terminal. Second, the measured result is insensitive to parasitic capacitance on the virtual-ground node. Feedback have been added to ensure that all of the response current is forced through the feedback

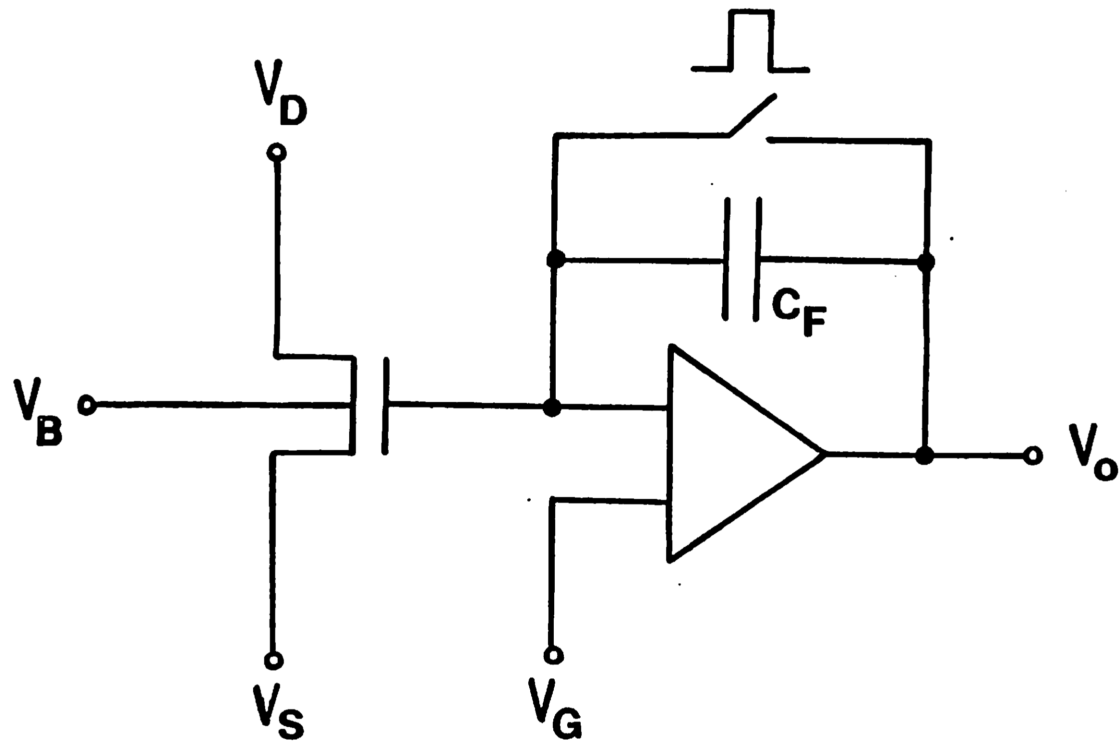


Fig. H.5 Coulombmeter Circuit [4].

capacitor. Third, the same coulombmeter circuit can be physically shared by several test devices as long as one device is measured at a time.

H.3. The New Direct-on-Wafer Capacitance Measurement Method

Although the capacitance measurement methods reported by Paulos et al. [4] and Iwai et al. [5] have good resolution, the requirement that special on-chip circuits to be fabricated near the devices of interest has prevented them from being widely adopted. The op-amp circuit consumes large area as compared to the test transistor itself. Dedicated masks are needed for the fabrication of these test structures. The performance of the op-amp circuit highly depends on the specific process being used. In addition, the inherently complicated data reduction scheme for the open-loop technique jeopardizes the accuracy of that method [H.8].

In this research, the instruments and technique to measure fF-size gate capacitances of small-geometry MOS transistors have been developed. No on-chip circuitry is needed and direct-on-wafer measurement using standard test transistors is possible [H.12]. By using a commercially-available high-performance op-amp in the external I-V converter, the measurement resolution has been improved from better than 0.2 fF [H.12] to better than 0.02 fF. High accuracy (better than 0.2fF) has also been achieved. In addition, the technique permits flexibility with regard to choices of dc biases and test devices. The direct-on-wafer measuring scheme can be easily incorporated into an automatic characterization system. This simple and accurate capacitance measurement technique is suitable for device analysis as well as process monitoring.

H.3.1. Measurement System

A schematic diagram of the measurement set-up is shown in Fig. H.6. The system contains an H-P 4145A parameter analyzer under the control of an H-P 9836 desktop

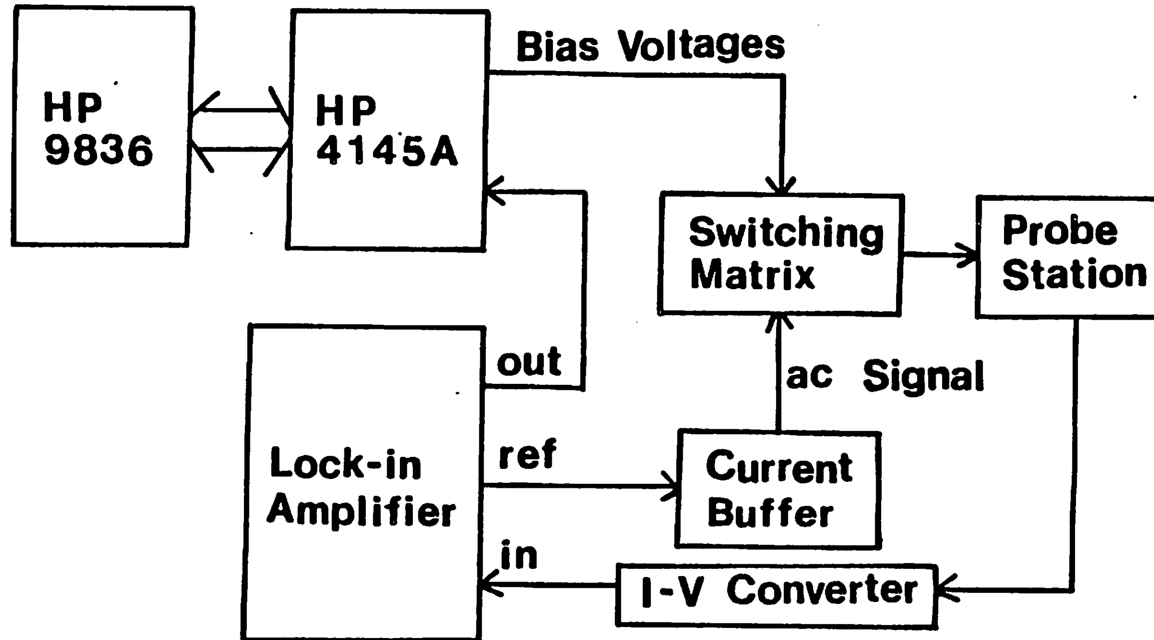


Fig. H.6 Schematic diagram of measurement setup for gate capacitances.

computer. The H-P 4145A supplies programmed dc biases to the test device. The ac test signal is derived from the built-in oscillator of the lock-in amplifier. The coupling transformer and the buffer amplifier convert the primary test signal into a truly-floating, low-impedance source. In order to improve the measurement resolution, the magnitude of the ac test signal used in the experiments has been increased from 23 mV (rms) [H.12] to 50 mV (rms). Configurations for measuring various gate capacitances can be selected with a specially designed switching matrix. The frequency of the test signal was set at 1 KHz for optimal operation of the I-V converter and for minimizing the phase shift due to cable capacitances. The I-V converter connected to the gate converts the gate capacitive current into voltage, which is detected by the lock-in amplifier. The employment of the high-performance op-amp in the I-V converter allows the test frequency to be increased to 6 KHz which is a major factor in improving the measurement resolution. The H-P 4145A monitors the output of the lock-in amplifier, which gives the capacitance information.

Figure H.7 shows the three measurement configurations to determine the gate-to-source C_{gs}, gate-to-drain C_{gd}, and gate-to-substrate C_{gb} capacitances, respectively. Capacitance C_{gs} is a measure of the change in the gate charge in response to the change in the gate-to-source voltage only. Therefore, the ac test signal is applied to the source terminal, with the gate-to-drain and gate-to-substrate voltages kept constant. Similarly, the ac test signal is applied to the drain and substrate terminals for the C_{gd} and C_{gb} capacitance measurements, respectively. This new technique contains all the advantages that the closed-loop technique has. Any of the three gate capacitances C_{gs}, C_{gd}, and C_{gb} can be measured independently. Full bias-range characterization can be easily achieved by varying the dc bias voltages V_{gs}, V_{ds}, and V_{bs}. This method does not have the switch-induced charge injection problem which is characteristic of the on-chip-circuitry methods, since the input of the I-V converter is connected to the gate terminal of the

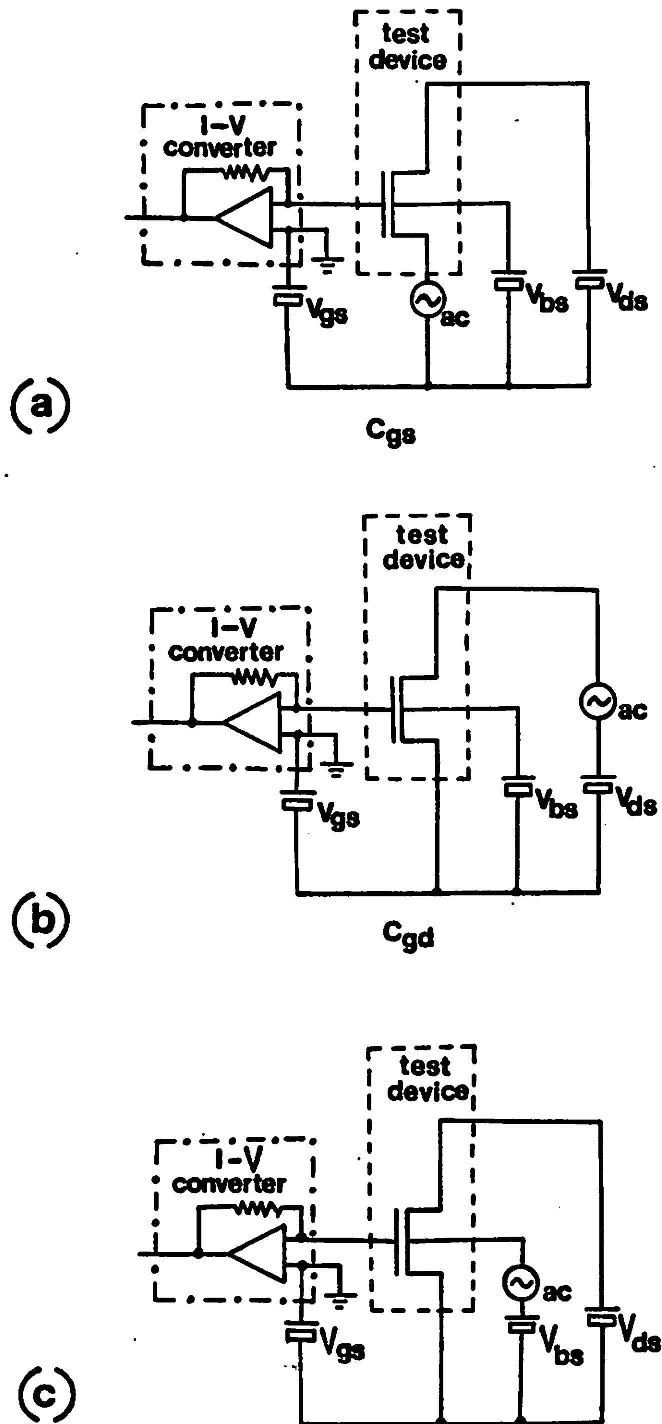


Fig. H.7 Measurement configurations to determine (a) gate-to-source capacitance C_{gs} . and (b) gate-to-drain capacitance C_{gd} . and (c) gate-to-substrate capacitance C_{gb} .

test device and it remains at virtual-grounded throughout the measurements. Measured results are insensitive to parasitic capacitances on the virtual-ground node.

H.3.2. Measurement Method

The measurement system is calibrated using standard capacitors with 5-digit accuracy. External and parasitic capacitances have to be subtracted from the raw measured results in order to obtain the intrinsic capacitances. Figure H.8 shows the external capacitances and the parasitic capacitances encountered in the C_{gs} and C_{gd} measurements. Capacitances C_{gse} and C_{gde} are the inter-probe external capacitances between the gate probe and source and drain probes. C_{ps} and C_{pd} include the overlap capacitances, outer fringing-field capacitances, and metallization capacitances associated with the pads at the source and the drain. The capacitances $C_{gse}+C_{ps}$ and $C_{gde}+C_{pd}$ are equal to the measured gate-to-source and gate-to-drain capacitances respectively when the device is in the strong accumulation region. Such measured capacitances do not contain any contribution from the intrinsic gate area. It is essential to keep the external capacitances C_{gse} and C_{gde} small in order to retain high accuracy.

Schematic diagrams of three different types of probes are shown in Fig. H.9. The darkened area denotes the conductor in direct contact with the probing pin. For the "ordinary probe to ordinary probe" arrangement, the inter-probe capacitance is as large as a few picofarads so that accurate measurement of the small-geometry MOS transistor capacitances becomes impossible. If the probe is teflon-shielded, the inter-probe capacitance is reduced to the sub-pF range. However, it is still too large to achieve high accuracy. By using the coaxial probes, the inter-probe parasitic capacitance is further reduced down to 4-5 fF for both "coaxial probe to teflon-shielded probe" and "coaxial probe to coaxial probe" arrangements. The coaxial probe arrangements are used in the experiments.

H.3.3. Experimental Results

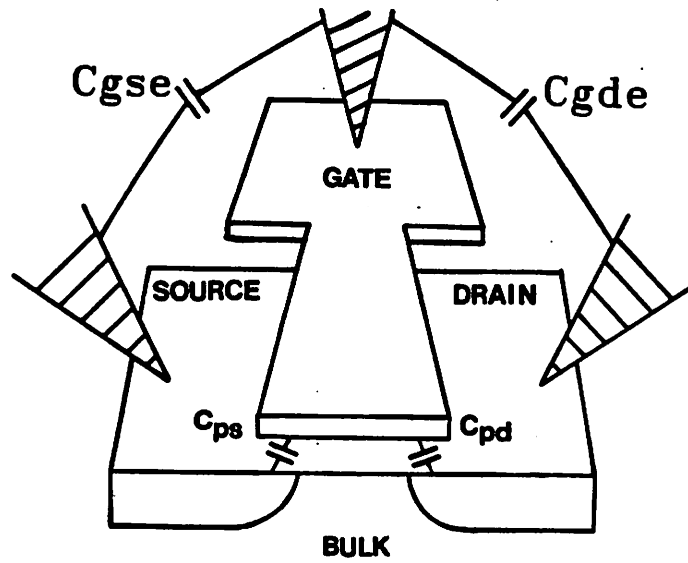
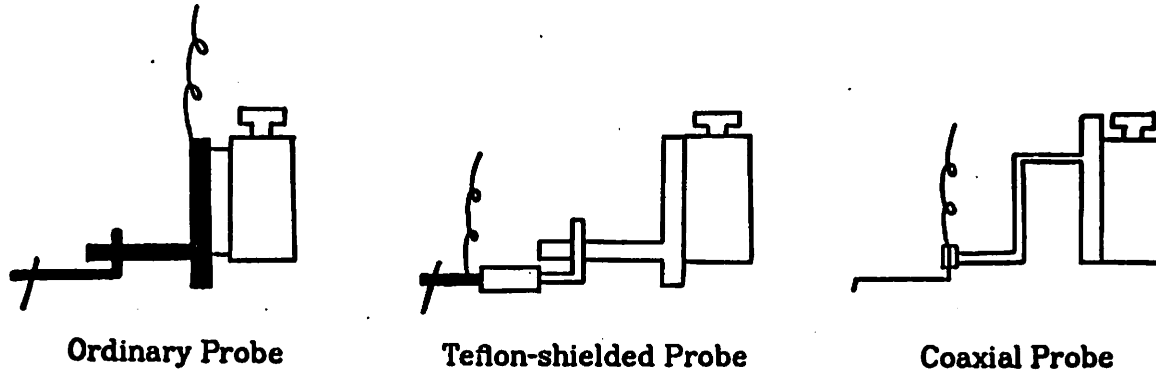


Fig. H.8 Probe arrangement indicating the external-and-parasitic capacitance components.

External Inter–probe Capacitance



Arrangement	Inter-probe Capacitance
Ordinary Probe to Ordinary Probe	a few pF
Teflon-shielded Probe to Teflon-shielded Probe	0.4 pF
Coaxial Probe to Teflon-shielded Probe	4~5 fF
Coaxial Probe to Coaxial Probe	4~5 fF

Fig. H.9 Schematic diagrams of an ordinary probe, teflon-shielded probe, and coaxial probe.

The resolution of this method is illustrated in the following example. The raw measured results for a test transistor with W_{eff}/L_{eff} = 4.2 μm/1.0 μm are shown in Fig. H.10. High resolution better than 0.1 fF is achieved in this measurement. The devices used in the experiments were N-channel MOS transistors. The gate-oxide thickness is 20.0 nm, substrate doping is 10^{15} cm^{-3}, and enhancement threshold implant is $8 \cdot 10^{11}$ cm^{-2}. Figure H.11 shows the normalized plot of the gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances of a short-channel transistor with W_{eff}/L_{eff} = 99.2 μm/1.0 μm. Included in this figure for comparison purposes are the measured capacitances of a long-channel transistor with W_{eff}/L_{eff} = 99.2 μm/99.5 μm. In this plot, the external capacitance and the parasitic capacitance have been subtracted. The curves corresponding to V_{gs}-V_T = 1 V start at a value slightly smaller than 0.5 C_{ox} because gate capacitance hasn't reached the maximum value at the low gate bias. The fact that the C_{gd} curves bend up and the C_{gs} curves bend down at large drain biases is believed to be due to the hot-carrier effect.

H.4. Short-Channel Effects

At zero drain-source bias, C_{gd} and C_{gs} are the same for both long-channel and short-channel devices, as expected. This means that the drain and source have equal amount of control over the channel charge.

For a long-channel device, C_{gd} approaches to zero and C_{gs} approaches to 2/3 C_{ox} as the device goes into the saturation region. A sharp transitions between the triode and saturation regions can be found. This behavior is well known and modeled [H.13]. The reason for C_{gd} approaching to zero is that in the saturation region the mobile carriers adjacent to the drain are depleted and the drain has very little control over the channel charge.

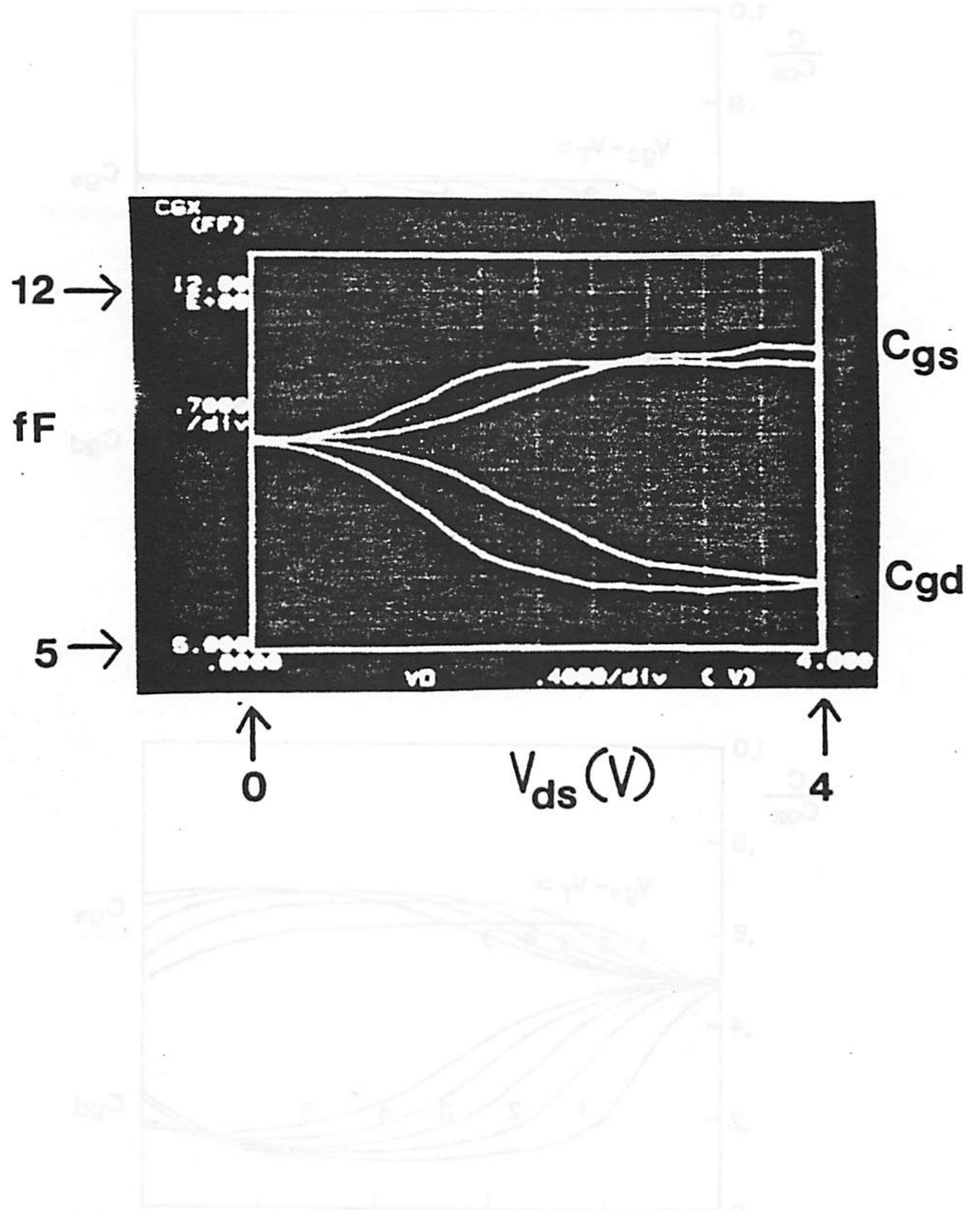
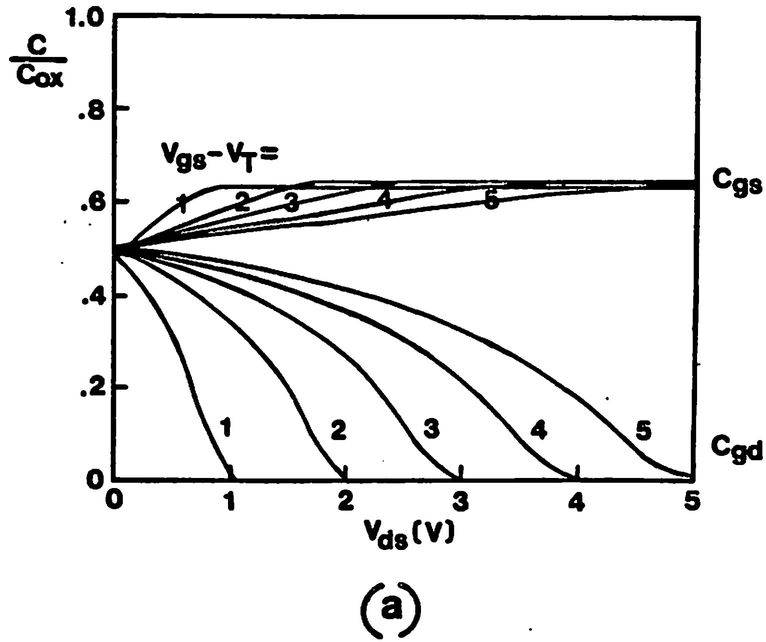


Fig. H.10 Raw measured gate-to-source and gate-to-drain capacitances for a transistor with W_{eff} = 4.2 μm and L_{eff} = 1.0 μm. The two sets of curves correspond to $V_{gs} - V_{th}$ = 2 V and 4 V, respectively. The parasitic capacitance has not been subtracted yet.



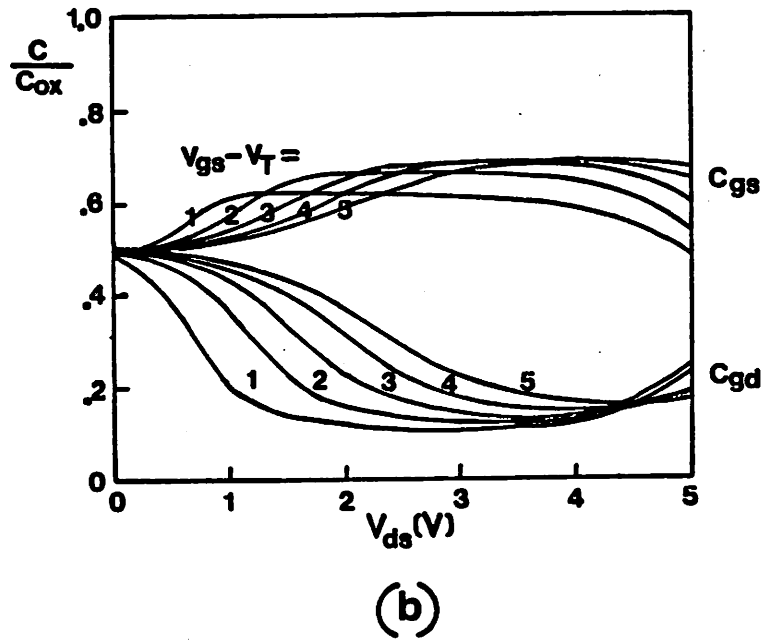


Fig. H.11 Normalized plots of measured C_{gs} and C_{gd} results for (a) a long-channel transistor with W = 100 μm and L_{eff} = 100 μm. (b) a short-channel transistor with W = 50 μm and L_{eff} = 1.0 μm. V_{gs} increases in 1 V steps.

For a short-channel device, several unusual features are observed. First, the C_{gd} and C_{gs} curves are much smoother than the long-channel device curves. No sharp transition from the triode region to the saturation region can be identified. This can be understood in terms of the phenomenon of carrier velocity saturation in short-channel devices. Second, the C_{gs} curves split in the saturation region for different gate biases. Both velocity saturation and source-drain series resistance contribute to this splitting. Because of the velocity saturation effect, a larger amount of the channel charge exists under gate control than predicted by the long-channel transistor theory. The increase in the gate-controlled channel charge is more prominent at a larger gate bias as the velocity-saturation effect is more dominant [H.14]. The source-drain series resistance, on the other hand, tends to reduce the splitting since the IR drop, which reduces the effective gate voltage, is larger at a higher gate bias. Third, C_{gd} saturates to a finite value in the saturation region. This behavior, as first described in [H.12], is due to the channel-side fringing fields between the gate and drain (source) junctions. The magnitude of this fringing capacitance is a strong function of the drain bias. At zero drain-source voltage when no channel electric field exists, the drain and source junctions are shielded from the gate on the channel side by the inversion layer. However, in the saturation region, the drain fringing-field lines can penetrate through the conducting channel to reach the gate in the region near the drain where the channel electric field is high. It is important to point out that the limiting saturated value for C_{gd} at large drain biases is a function of the drain-junction depth, gate-oxide thickness [H.14,H.15], and does not scale with device size. It, therefore, is more prominent in short-channel devices. In the experiments, the limiting saturated values for C_{gd} are approximately 4%, 8%, and 14% of C_{ox} for devices with L_{eff} = 4.5, 1.5, and 0.75 μm, respectively. Because of the Miller effect, the influence of channel-side fringing capacitance on the performance of high-speed MOS circuits is readily noticeable experimentally.

H.5. A Physics-Based Capacitance Model for Short-Channel MOS Transistors

An analytical model to explain the measured results, especially the short-channel effects and above-threshold characteristics, is described. This new model includes the mobility-degradation effect, velocity-saturation effect, bias-dependent fringing-field effect, as well as source-drain series resistance effect. The analytical capacitance model is based on the hot-electron current model previously developed by Ko [H.17]. Descriptions of the dc model can be found in [H.14] and [H.16].

H.5.1. The Charge and Capacitance Model

The gate charge, Q_G, is made up of three components, Q_{G1}, Q_{G2}, and Q_{G3}, as shown in Fig. H.12. The drawing is a schematic representation of the charge density along the channel. It is not the spatial distribution of the charge. The gradual-channel approximation can be applied to the portion of the channel near the source. The charge in this portion is designated as Q_{G1}. In the portion of the channel adjacent to the drain, the velocity of mobile carriers saturates. The charge in this portion is designated as Q_{G2}. When the device is biased in the saturation region, there is an important capacitive component between the gate and the drain, i.e., the channel-side bias-dependent fringing-field capacitance. The charge associated with the fringing-field effect is designated as Q_{G3}. The gate-charge derivatives give the intrinsic gate capacitances,

$$C_{gs}=\frac{\partial Q_G}{\partial V_{gs}}\Big|_{V_{gd},V_{gb}}, \quad C_{gd}=\frac{\partial Q_G}{\partial V_{gd}}\Big|_{V_{gs},V_{gb}}, \quad \text{and} \quad C_{gb}=\frac{\partial Q_G}{\partial V_{gb}}\Big|_{V_{gd},V_{gs}}. \tag{H.8}$$

The expression for Q_{G1} can be obtained by integrating the distributed charge density over the area of the active gate region,

$$Q_{G1}=\int_0^L Q_n(y)\,dy = WC_o\int_0^L (V_{gs}-V_T-V(y))dy = WC_o\int_0^L \frac{V_{gs}-V_T-V(y)}{E}\,dV, \tag{H.9}$$

where the integration with respect to the positional increment dy has been converted to

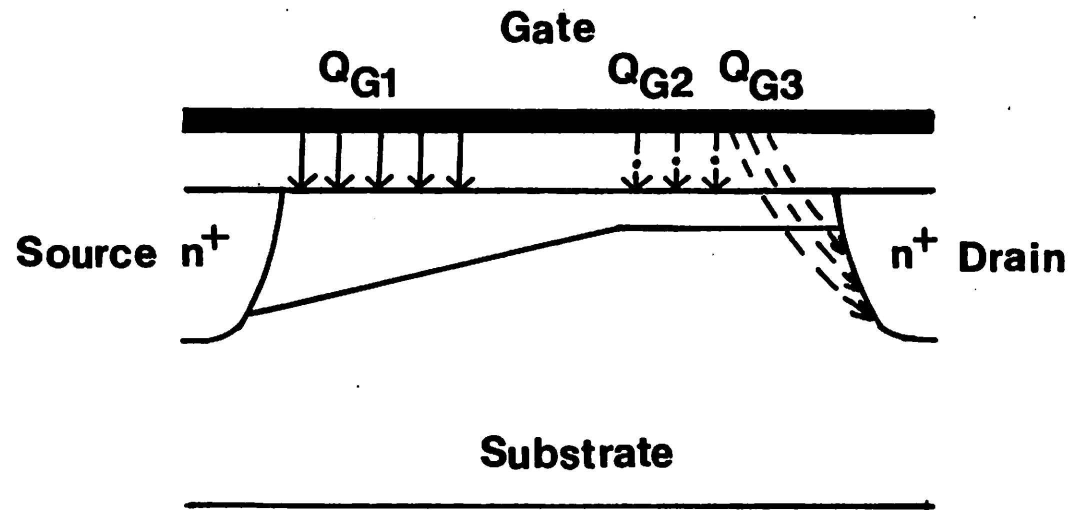


Fig. H.12 Schematic illustration of the three components of the charge stored in the gate when the device is biased in the saturation region. Q_{G1}: the charge in the source region. Q_{G2}: the charge in the saturation region. Q_{G3}: the charge associated with the channel-side bias-dependent fringing fields.

an integration with respect to the potential increment dV. Since

$$I_{dp} \equiv \frac{I_d}{W\mu_0 C_{ox}} = \frac{(V_{gs} - V_T - V)E}{1 + \frac{E}{E_c} + \eta E_{oxp}} . \quad \text{(H.10)}$$

by rearranging (H.10) we obtain

$$\frac{1}{E} = \frac{1}{(1+\eta E_{oxp})}\left[\frac{V_{gs} - V_T - V}{I_{dp}} - \frac{1}{E_c}\right] . \quad \text{(H.11)}$$

Substituting (H.11) into (H.9) and carrying out the integration.

$$Q_{G1} = \frac{WC_o}{(1+\eta E_{oxp}) E_c I_{dp}} \int_0^{V_{ds}} [(V_{gs} - V_T - V) E_c - I_{dp}](V_{gs} - V_T - V)\, dV$$

$$= \frac{WC_o}{(1+\eta E_{oxp}) E_c I_{dp}} \left\{ \frac{E_c}{3}\left[(V_{gs} - V_T)^3 - (V_{gs} - V_T - V_{ds})^3\right] \right.$$

$$\left. - \frac{I_{dp}}{2}\left[(V_{gs} - V_T)^2 - (V_{gs} - V_T - V_{ds})^2\right] \right\} . \quad \text{(H.12)}$$

By including the source-drain series resistance effect, the expression becomes

$$Q_{G1} = \frac{WC_o}{(1+\eta E_{oxp}) E_c I_{dp}} \left\{ \frac{E_c}{3}\left[(V_{gs} - V_T - I_d R_s)^3 - (V_{gs} - V_T - V_{ds} + I_d R_s)^3\right] \right.$$

$$\left. - \frac{I_{dp}}{2} (V_{gs} - V_T - I_d R_s)^2 - (V_{gs} - V_T - V_{ds} + I_d R_s)^2]\right\} . \quad \text{(H.13)}$$

The E_c term comes from the velocity-saturation effect. The $\eta\, E_{oxp}$ term comes from the vertical-field mobility-degradation effect. The $I_d\, R_s$ term comes from the source-drain series resistance effect.

When the device is biased in the saturation region, V_{ds} in the Q_{G1} expression is replaced by V_{dsat}. It is important to obtain the length of the drain region inside which the carrier velocity saturates. A pseudo two-dimensional analysis is used to find the channel electric field and potential distribution by solving the Poisson equation for the

Gaussian box enclosing the drain region. Once the electric field and potential drop inside this drain region is available, the length of this drain region can be obtained easily. Because all the carriers travel at the same saturated velocity in the drain region, the mobile carrier density is constant in this region. The multiplication of the charge density with the length gives Q_{G2}.

$$Q_{G2}=\frac{I_{dsat}\,\Delta L}{v_{sat}} \tag{H.14}$$

where v_{sat} is the saturation velocity. Accurate determination of the saturation voltage is crucial in the calculations of Q_{G1} and Q_{G2}.

The bias-dependent fringing-field capacitance associated with Q_{G3} can be determined by considering the device operation in the drain area. When the device is biased in the strong inversion region and $V_{ds} = 0$, the fringing field is shielded by channel inversion charge. In this case, the drain terminal has a strong control over the channel, and

$$C_{gdc} = \frac{\partial(Q_{G1}+Q_{G2})}{\partial V_{gd}} \Big|_{V_{gd},V_{gb}} = \frac{C_o}{2}. \tag{H.15}$$

The limiting condition corresponding to non-shielding of the channel-side fringing field is when $C_{gdc} = 0$. In this case, the drain has no control over the channel. An approximate expression for the unshielded fringing-field capacitance is given by [H.15].

$$C_f = \frac{2\epsilon_{Si}W}{\pi}\ln\left[1 + \frac{X_j}{X_{ox}}\sin\left(\frac{\pi\,\epsilon_{ox}}{2\,\epsilon_{Si}}\right)\right]. \tag{H.16}$$

Here, X_j is the drain-junction depth. However, for $V_{ds} > 0$, the control by the drain over the channel degrades. Linear interpolation is used to give a first-order model of the bias-dependent fringing-field effect.

$$C_{gd,fringing} = C_f\left(1 - \frac{2\,C_{gdc}}{C_o}\right). \tag{H.17}$$

The two limiting conditions, when $C_{gdc} = C_o/2$ and when $C_{gdc} = 0$, are satisfied by (H.17).

H.5.2. Results and Discussion

Figure H.13 shows the calculated C-V characteristics for a long-channel transistor and a short-channel transistor with the same device parameters as those for the transistors used in Fig. H.11. Good agreement between the calculated results and the measured data in Fig. H.11 is found.

When compared to the already published charge and capacitance models for long-channel devices, the salient features of this short-channel transistor model are:

(1) The vertical field and horizontal field mobility degradation effect is incorporated in the expression for Q_{G1} .

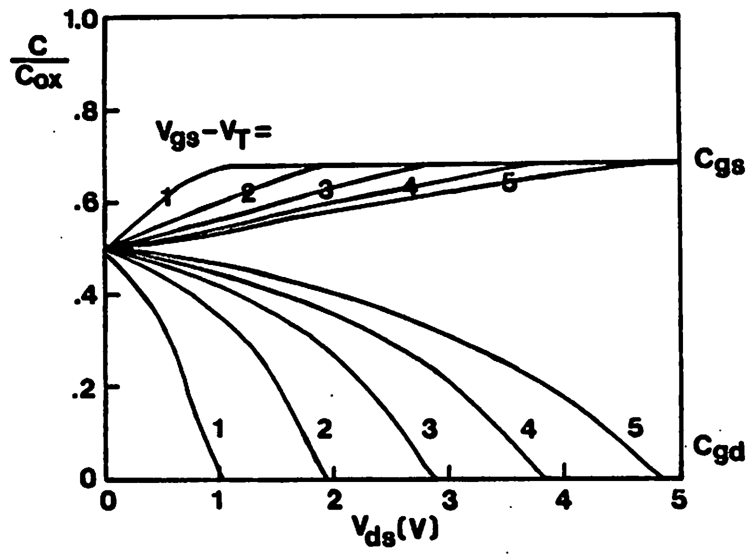
(2) The drain region charge, Q_{G2} , which takes into account the velocity saturation effect via v_{sat} and the channel-length modulation effect via ΔL , is included.

(3) The bias-dependent-fringing-field effect is incorporated. Q_{G3} is constant irrespective of the channel length, and the ratio of this capacitive component to the maximum intrinsic gate capacitance increases as channel length decreases.

(4) Source-drain series resistance is included.

The inclusion of the above features is important for a short-channel charge and capacitance model. Features (1) and (2) make the calculated characteristics smooth. Feature (3) accounts for the finite value of C_{gd} in the saturation region which has a strong influence on the high-speed performance of MOS circuits.

For the case with source-drain series resistance, C_{gd} is larger and C_{gs} is smaller as compared with those in the case without source-drain series resistance under the same bias conditions. At a finite drain bias, the voltage drop across the channel is reduced due



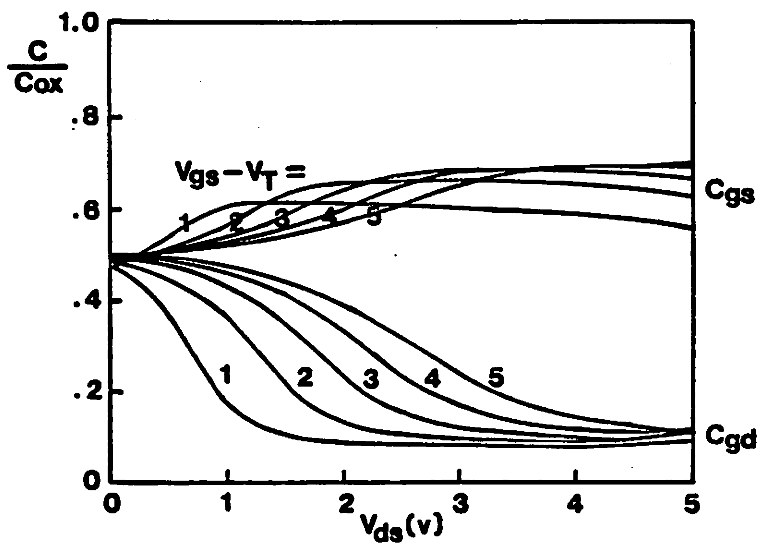


Fig. H.13 Normalized plots of calculated C_{gs} and C_{gd} results for transistors with the same device parameters as those for the transistors used in Fig. H.11. (a) a long-channel transistor, (b) a short-channel transistor.

to the voltage drop in the source-drain series resistance. The hot-electron effects which modify the C-V characteristics of short-channel transistors at large drain biases (see Fig. H.11(b)) have not been included in the model yet.

H.6. Conclusion

A new and simple technique for measuring the gate capacitances of small-geometry transistors has been described. This direct-on-wafer measurement scheme is very suitable for the purposes of device physics study and process control applications and can be easily incorporated into an automated characterization system. It applies to standard test transistors without requiring any on-chip circuitry. Very high accuracy and resolution have been achieved by using this measurement technique. An analytical model which satisfactorily explains the various unusual features observed in the intrinsic gate capacitance characteristics of short-channel MOS transistors has also been presented. The inclusion of the mobility degradation effect, velocity saturation effect, bias-dependent fringing-field effect, and source-drain series resistance effect proves to be adequate for accurate prediction of the intrinsic capacitances.

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