A HIGH-SPEED, HIGH-PRECISION COMPARATOR DESIGN FOR A 10-BIT, 15MHZ, A/D CONVERTER

by

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Dedication

This manuscript is dedicated to my wife Yoko for her patience and support during this work, and to my daughter Marie for her encouragement with her pretty smile during my hard work days.

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ABSTRACT

This research effort has been directed towards the basic design of a high speed and high precision CMOS comparators. These comparator design techniques are going to be used in the 10 bit 15 MHz A/D converter. [1]

The multi-stage fully differential amplifier and a regenerative latch are used as the basic configuration. Various candidates for the fully differential amplifier have been designed and compared. The fully differential amplifier with the DC gain of 10 and the gain band-width of 2.500 Mrad/sec has been chosen.

The author has joined in this project, when he was visiting ERL, University of California as a visiting industrial fellow from August 1984 to August 1985.

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CHAPTER 1 INTRODUCTION

Recently, the conventional video signal processing in the analog form has been replaced by digital signal processing, improving the performance, the reliability and in some cases even the production cost. This replacement has taken place first in the TV studios, where intensive and high quality signal processing is required, no matter how expensive the cost of the equipments will be.

Thanks to the development in the VLSI technology, digital video signal processing becomes affordable even for home used video equipment. Now, several manufacturers provides high quality and multi-function digital TV sets. [2] [3] The sampling rate and quantization bits required in this application are 4 f_{sc} (14.32 MHz) and 8 bits respectively. The signal bandwidth of a video signal is 4.2 MHz, so 3 f_{sc} will be enough to prevent aliasing. But, for the color signal processing (especially for the PAL), it is convenient to use 4 f_{sc}. Considering only the random quantization noise, a signal to noise ratio (SNR) of 48 dB can be achieved with the 8 bit resolution. This is high enough for the commercial TV video signal. Many Analog to Digital Converters (ADC) which satisfy these specifications, have been reported and manufactured, both in bipolar and CMOS processes. [4] [5] For high resolution TVs, a sampling rate as high as 100 MHz will be required. [10]

The next step in the digital video signal processing will be the introduction of digital video tape recorders (Digital VTR) and digital TV cameras. [6] [7] In the 3-CCD Digital TV camera [7], an analog gain adjust circuit, a limiter and an analog white balance circuit is installed between the CCD solid-state imagers and the ADCs. There is a feedback loop to the limiter to keep the black level constant. All these circuits are used to quantize the input signal effectively in 8 bits. The SNR of this camera is 52 dB for the random noise. For high quality studio cameras, an SNR above 60 dB is required. This means that a quantization of more than 10 bit is required. Even for the home used TV cameras, 10 bit resolution will be desirable. It will make possible to remove all the analog circuits between the image sensor and the ADC.

The quantization of the video signal which experiences many signal processings, requires more bits than 8. Such applications are the digital TV cameras, the digital studio equipment[8] and the Medical Electronic (ME) equipment, such as digital radiography. In a digital studio, many pieces of equipment will be connected in tandem. Each signal process will experience a rounding of the digital signal, degrading its quality.

There are many other applications for the high speed, high resolution ADCs. Fig.1-1 shows some application fields, depending on the speed and the resolution of the ADCs. [10]

For now, only one monolithic video frequency 10-bit ADC has been reported using a bipolar technology.[9] It can quantize the input signal with a sampling rate of 20 MHz. The drawback of this device is its size (40,000 Transistors, 9.2 mm x 9.8 mm) and its large power consumption (2.0 W). Moreover, to compensate the reference voltage deviation, it has 8 drivers to drive the reference resistor string, and requires laser trimming.

To realize this circuit in CMOS technology, we have to expand the circuitry of an 8 bit CMOS ADC, 4 times. Beside this expansion, one more amplification stage must be added in the comparator to get the sufficient resolution, and much attention should be paid to the precision of the resistor string and to the charge feed-through problem. A rough estimation from an 8 bit CMOS ADC [5] implies that the size and power consumption of a 10 bit video frequency CMOS ADC will be 21.6 mm x 16.0 mm and 1.2 W respectively.

Taking these problems into account, J. Doernberg has developed a novel algorithm for a high speed, high resolution ADC [1]. Basically, it is a two step ADC. However, it utilizes a parallel binary-weighted capacitor- arrays to quantize the signal. This requires neither sample and hold circuit nor subtractor circuit, which are the most critical analog parts in the conventional two step ADCs.

The most difficult component to design in this ADC is the high speed, high resolution comparator. Because of the two step conversion, it must be operated with the speed much faster than twice of the conventional flash type ADC. Moreover, it has to maintain the 10 bit resolution at that speed.

We have developed a multi-stage fully differential comparator to satisfy those requirements. Here in this paper, the basic analysis and design of the comparator has been discussed in detail.

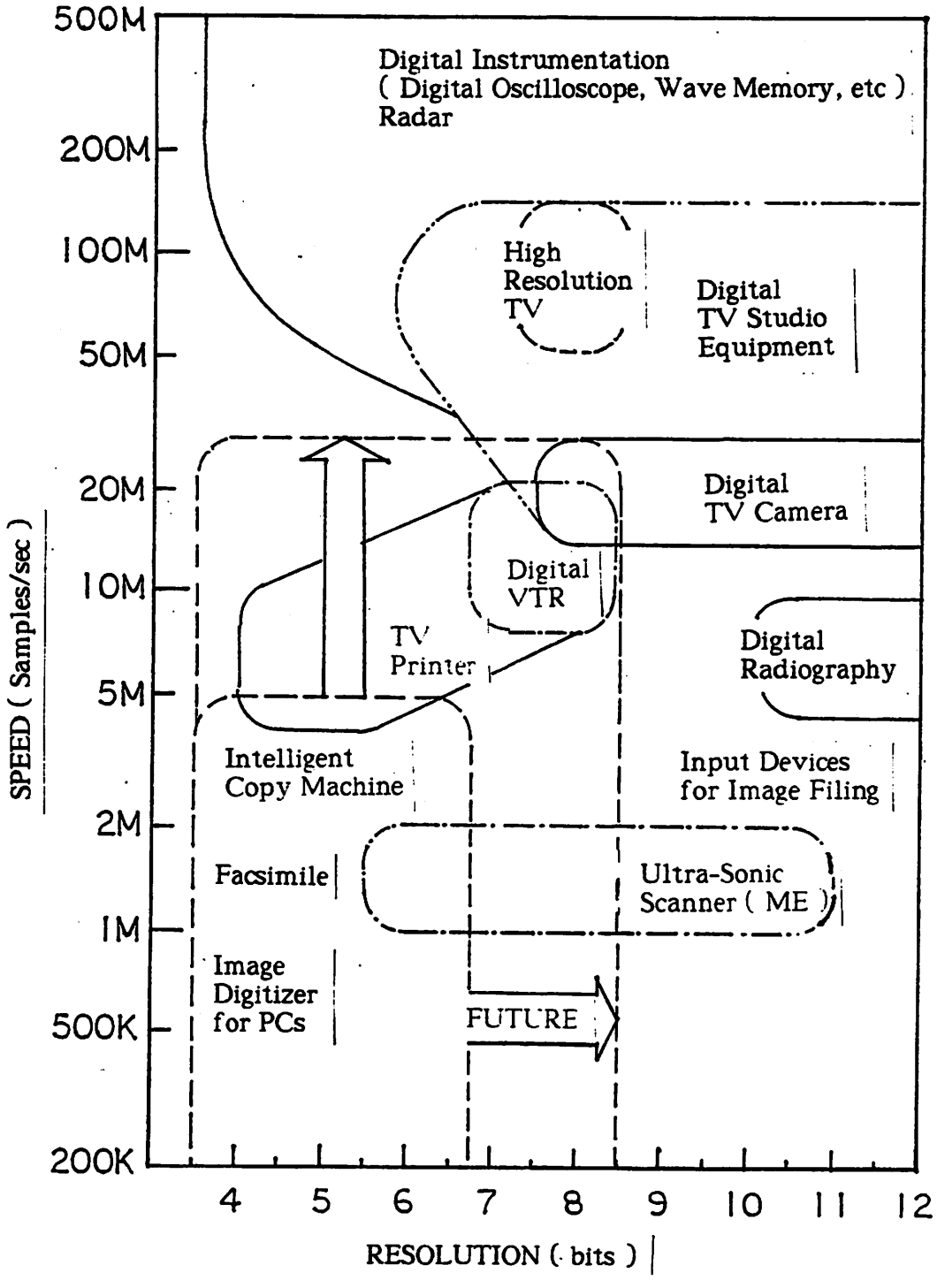


Fig. 1-1 Application Fields for the High Speed High Resolution ADC

CHAPTER 2 TWO STEP PARALLEL A/D CONVERSION

2.1 Basic Configuration and Algorithm

As mentioned in the previous section, the parallel conversion technique can perform the A/D conversion in a single clock cycle. However, it requires 2^N comparators and a precisely fabricated, and sometimes trimmed resistor string. For example, to implement a 10-bit, 20 MHz ADC , 1024 high resolution ($\approx$1 mV sensitivity) and high speed ($\approx$50 nS settling) comparators will be required.

Recently, a 10-bit, 20 MHz ADC fabricated in an ECL process has been reported.[9] However, its chip size is large, 10 x 10 mm^2, and its power dissipation is 2.08 watts. Moreover, it contains eight operational amplifiers (op. amps) to bias the resistor string . This is used for the temperature drift compensation of the bipolar transistor's input bias current in the comparators.

These factors will make it difficult to fabricate this ADC with a high yield rate, and consequently a reasonably low price.

As a solution to these problems, two or multi-step parallel conversion [11] [12] techniques have been proposed. One of the most frequently used technique is shown in Fig. 2.1-1. It executes the m-bit MSBs conversion in the first step, then subtracts the quantized MSBs signal $\hat{V}_{MSB}$ from the sampled and held input signal V_{in}, and executes the LSBs conversion as the second step. The disadvantages of this technique is the requirements for high speed settling and precise circuits for the S/H and subtractor. It is difficult to design those circuits with the settling time of less than 20 ns within the error of 0.05% (0.5 LSB resolution in 10 bits).

A promising two-step parallel conversion technique has been proposed by Joey Doernberg. [1] Instead of using a resistor string with 2^N taps as the reference voltage, it has multiple capacitor arrays connected in 2^N different bit patterns. What is important in

this technique is that the S/H and subtract functions are merged in these capacitor arrays. Neither an external S/H circuit nor a subtractor are required.

An example of the operation of 4-bit, two-step parallel ADC is shown in Fig. 2.1-3 to 4, and its algorithm in Fig. 2.1-2.

As shown in Fig. 2.1-3, the 4-bit ADC consists of 4 capacitor arrays, each of them containing 3 binary-weighted capacitors. For an N-bit ADC, these numbers will be $2^{\frac{N}{2}}$ and N/2+1 respectively. Each array has a comparator, and that is shown in the figure as an ideal amplifier with a gain of $-\infty$. The bottom plate switches of the capacitors are connected to the input, Vref or GND.

At the start, those switches are connected to the input voltage Vin. At the same time the reset switch around the comparator is closed, in order to set the voltage of the top plates of the capacitors to virtual GND for the ideal case, or to the offset voltage of the comparator generally. In this way, the input signal is sampled on the capacitors. Then all the switches are reconnected to the opposite side. Here the rightmost capacitors are connected to GND, while the other two are connected in 4 different bit patterns. From top to bottom, (11), (10), (01), (00), where we assign 0 for GND, and 1 for Vref. This is the first step of the conversion. If we assume the input voltage of 0.51V ((0101)+Δ), for the reference voltage Vref of 1.6V, then the input voltage of the comparators will take the value as shown in Fig.2.1-3. Here Δ is a signal less than 1 LSB, and in the case above, $0.51=0.5+0.1=\frac{(0101)_2}{(10000)_2}1.6 + 0.1$. The outputs from the top to the bottom are (LLHH). In this way, the input signal has been measured to be between 0.4V and 0.8V for the 1.6V reference (full scale). Therefore, the encoded binary output should be (b3,b2) = (0 1).

In Fig. 2.1-4, the second step (the LSBs conversion), is shown. Here, the left two capacitors of all arrays are connected to Vref or GND, depending on the (b3,b2) MSBs data acquired in the first step.

In this example of Vin=0.51V, the 2C's are connected to GND , and C to Vref, taking into account that (b3,b2) = (0 1) → (GND,Vref). Simultaneously, the rightmost capacitors are connected to a resistor string, picking up equally spaced voltages. The operations described above shows *THE ESSENCE* of this technique. The functions that are essential for the two step A/D has been accomplished as follows;

1) **S/H** : Holding the input data on the capacitors all through the two steps.

2) **Subtraction** : Subtract the quantized MSBs output from the input signal by setting the bit patterns of all arrays to that of the MSBs data.

The input for each comparator is shown in the Fig. 2.1-4, for the input signal of 0.51V. Then the output of the comparators will be (LLHH) from the top to the bottom. And the encoded binary data is (b1,b0) = (0 1). The full 4-bit data will be $(0101)_2$ = 5, and this means the quantized value of 0.5V for the Vref of 1.6V. Details of this operation will be discussed in the section 2.2 .

The following are the calculations of some basic design parameters.

The 4-bit ADC consists of 4 capacitor arrays, each of them containing 3 capacitors. (2C, C and C) For a N-bit ADC, the number of capacitor arrays will be $2^{\frac{N}{2}}$, and the number of the capacitors in each array will be N/2+1. If we define the minimum size capacitor as the unit capacitor, the number of unit capacitors to realize an N-bit ADC will be;

$$N_{CU} = 2^{\frac{N}{2}} \left(\sum_{k=1}^{\frac{N}{2}} 2^{k-1} + 1 \right) = 2^N \qquad (2.1\text{-}1)$$

For a 4 bit ADC (N=4), this number is 16. For 10 bits this will be 1024. Using a unit capacitor of 8 x 8 μm^2,.(0.05pF capacitor with Tox = 30 nm, and some area margin) the area will be 65,536 μm^2.

The area occupied by the switches of the capacitor array is also an important factor to be considered. To equalize the time constants for each capacitor switch pair, the width of those switches must be also scaled, depending on the size of the capacitances. The minimum size MOS switch will be used with the minimum size capacitor. And its size should be doubled, every time the accompanying capacitor is doubled. The detailed circuit will be shown in Chapter 3. Here we will only count the area of those control switches in units of a unit size MOS transistor. Each capacitor is connected to 4 switches of the same size, except the one that is connected to the resistor string. This rightmost capacitor is connected to 3 switches. So the number of unit size transistors used in the N-bit ADC will be:

$$N_{swu} = 2^{\frac{N}{2}}\left(4 \sum_{k=1}^{\frac{N}{2}} 2^{k-1} + 3 \right) = 2^{\frac{N}{2}}\left(2^{(\frac{N}{2}+2)} - 1 \right) \qquad (2.1\text{-}2)$$

For a 4 bit ADC, that number is 60. For a 10-bit ADC that will be 4064. If a unit MOS switch of W=5 microns and L=2 microns (Ron = 16 Kohm under Vgs=0.5V, Uexp = 0.4 and KP = 61 $\mu A/V^2$) is used, the area of that unit MOS switch can be estimated as 75 μm^2. Then the total area occupied by these switches will be 304,800 μm^2, which is about five times larger than the area occupied by the capacitor arrays. If folded layout is used for the wide MOS switches, this area will be reduced as far as 50% of the size above. If a fully differential configuration is used, this number will be doubled. However, with this technique, it will be possible to reduce the chip area by a large amount, compared to a parallel ADC (flash) discussed in chapter 1.

Because a large number of capacitors are used in this ADC, attention must be taken to the input capacitance Cin. It consists of the the capacitors in the capacitor arrays and the junction capacitors of the MOS switches used there. If we assume that the junction capacitance of the unit MOS switch (including both drain and source) is:

$$C_{ju} = \xi C_u$$

Then the input capacitance can be calculated as follows:

$$C_{in} = N_{cw}(1 + \xi)C_u = 2^N(1 + \xi)C_u \qquad (2.1\text{-}3)$$

For a junction area of 5 microns x 13 microns and Cj of 5 x 10^{-4} F/m^2, we get ξ = 0.65 for Cu of 0.05 pF. For an ADC of N=10 bit. Cin is calculated to be 84.5 pF.

The acquisition time for the sample and hold can be considered as the time required to charge the capacitor arrays within the desired precision of 0.5 LSB. Let's consider the worst case of sampling a full scale signal of N bits. Because of the scaling of the MOS switches mentioned above, the RC time constant for the charging is the product of the unit capacitance and the Ron of the unit MOS switch. Then the acquisition time to reach the 0.5 LSB precision can be calculated as follows:

$$T_{aq} = C_u R_{onu} \ln(\frac{0.5}{1024}) = 7.62\, C_u R_{onu} \qquad (2.1\text{-}4)$$

For Cu = 0.05pF and Ronu = 16 kΩ this value will be 6ns. But in actual design, the resistance of the signal lines, the maximum current available from the comparator and other factors must also be considered.

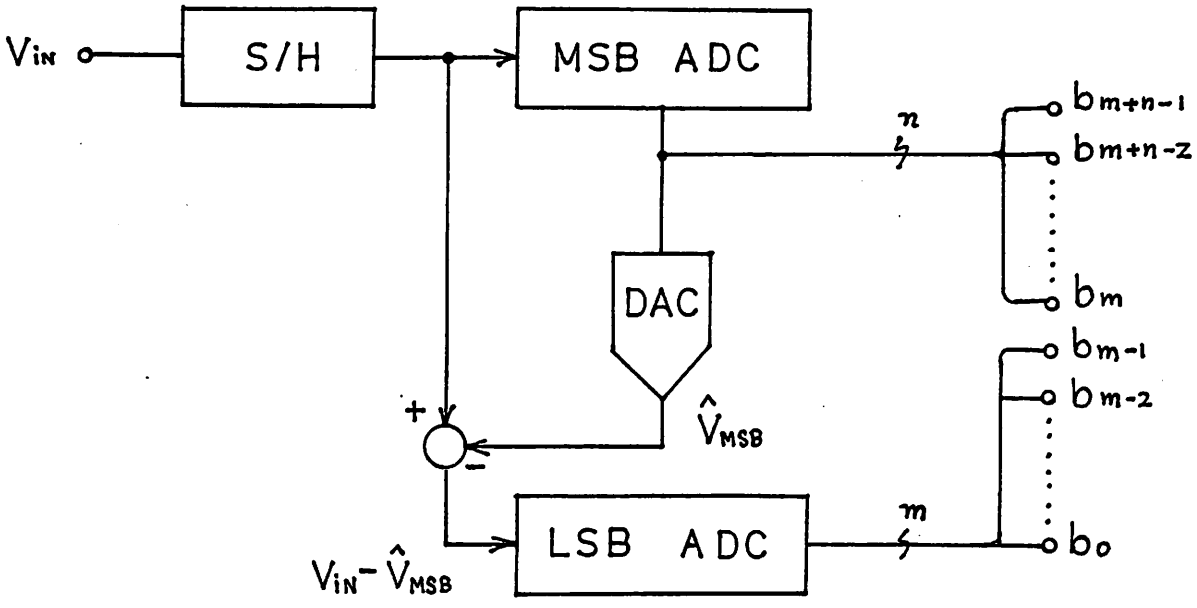


Fig. 2.1-1 Two Step Parallel ADC using S/H and Subtractor

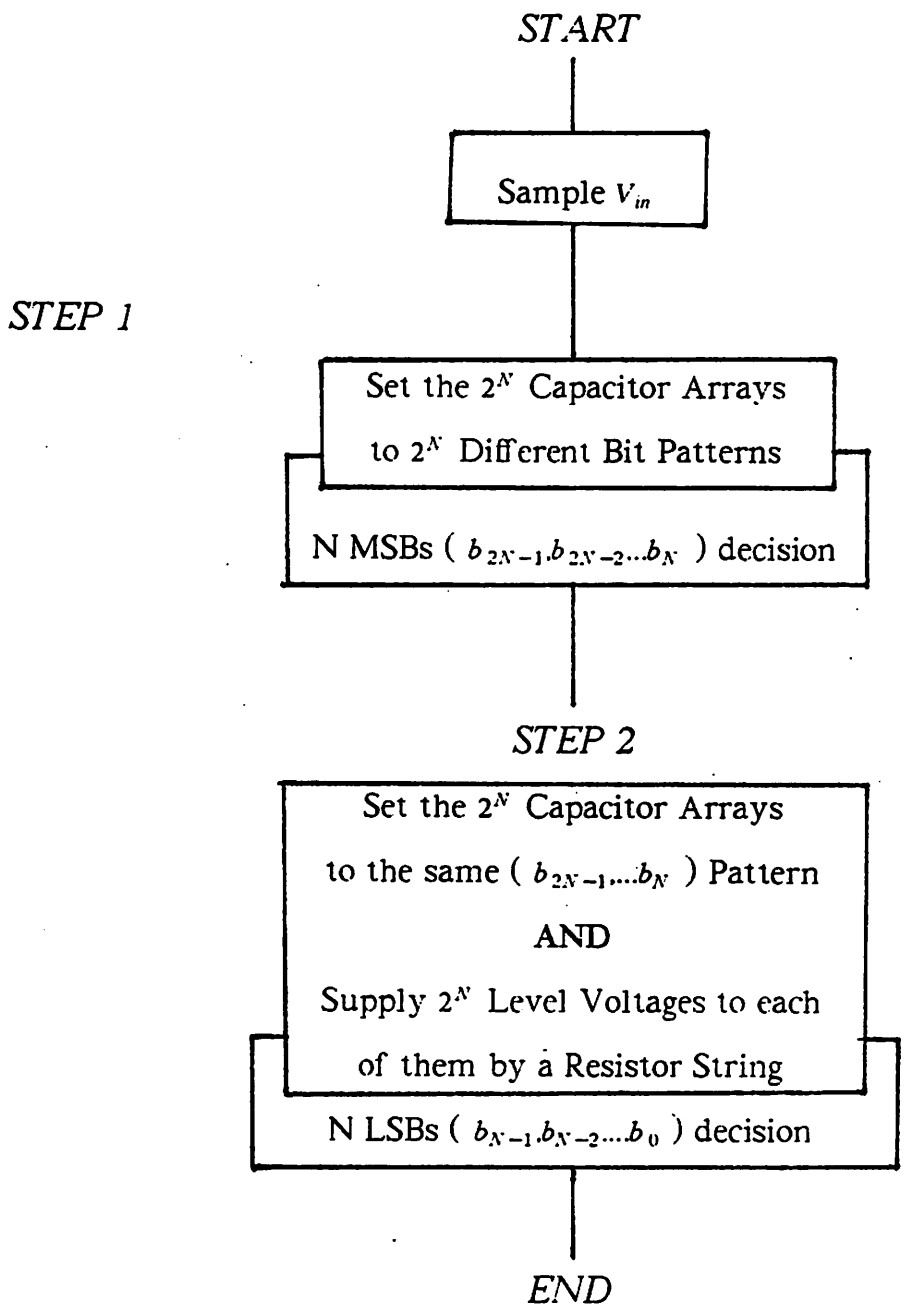


Fig. 2.1-2 Two Step Parallel ADC Algorithm

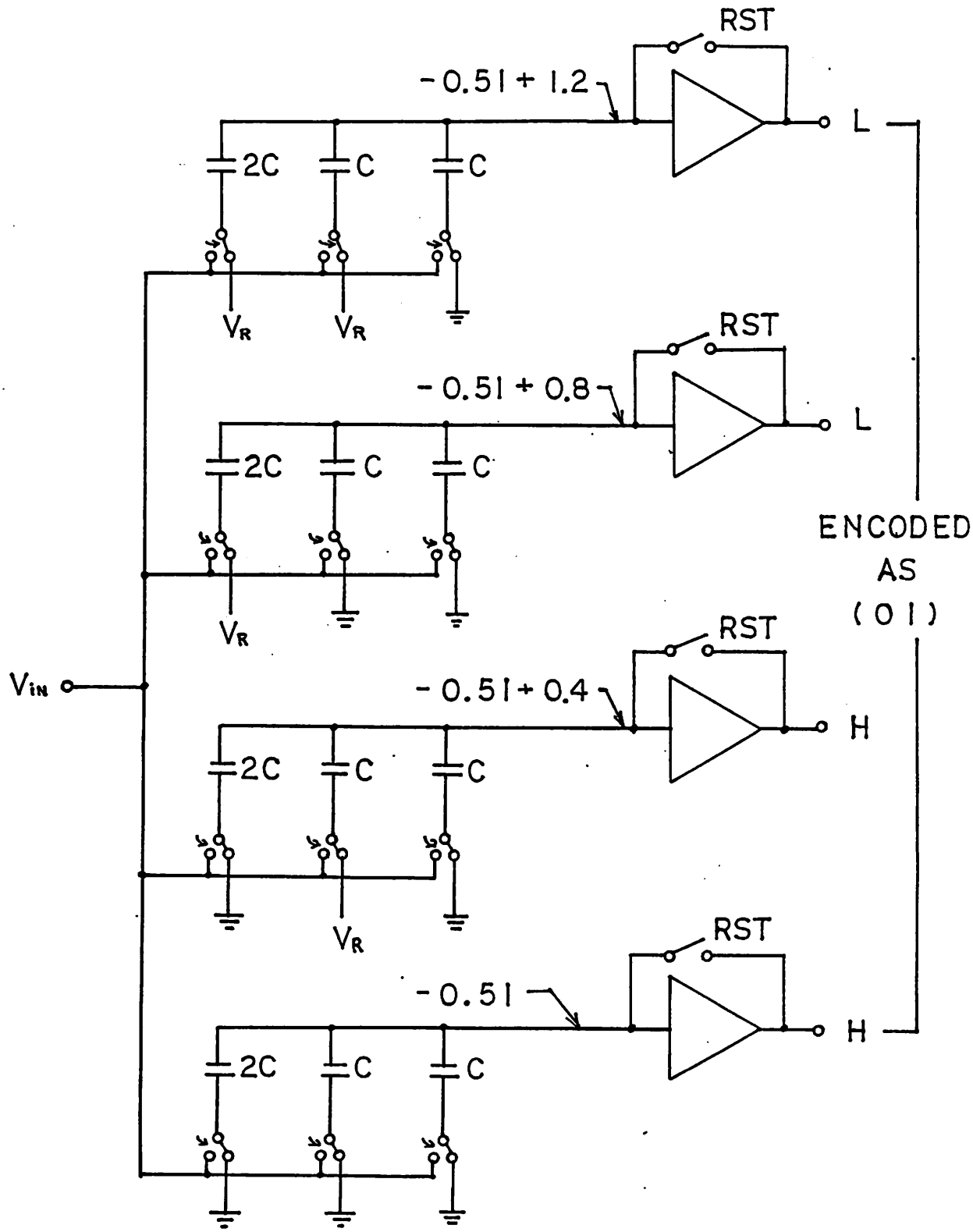


Fig. 2.1-3 MSBs A/D Conversion in the Two Step Parallel ADC

(Vref = 1.6V, Vin = 0.51V)

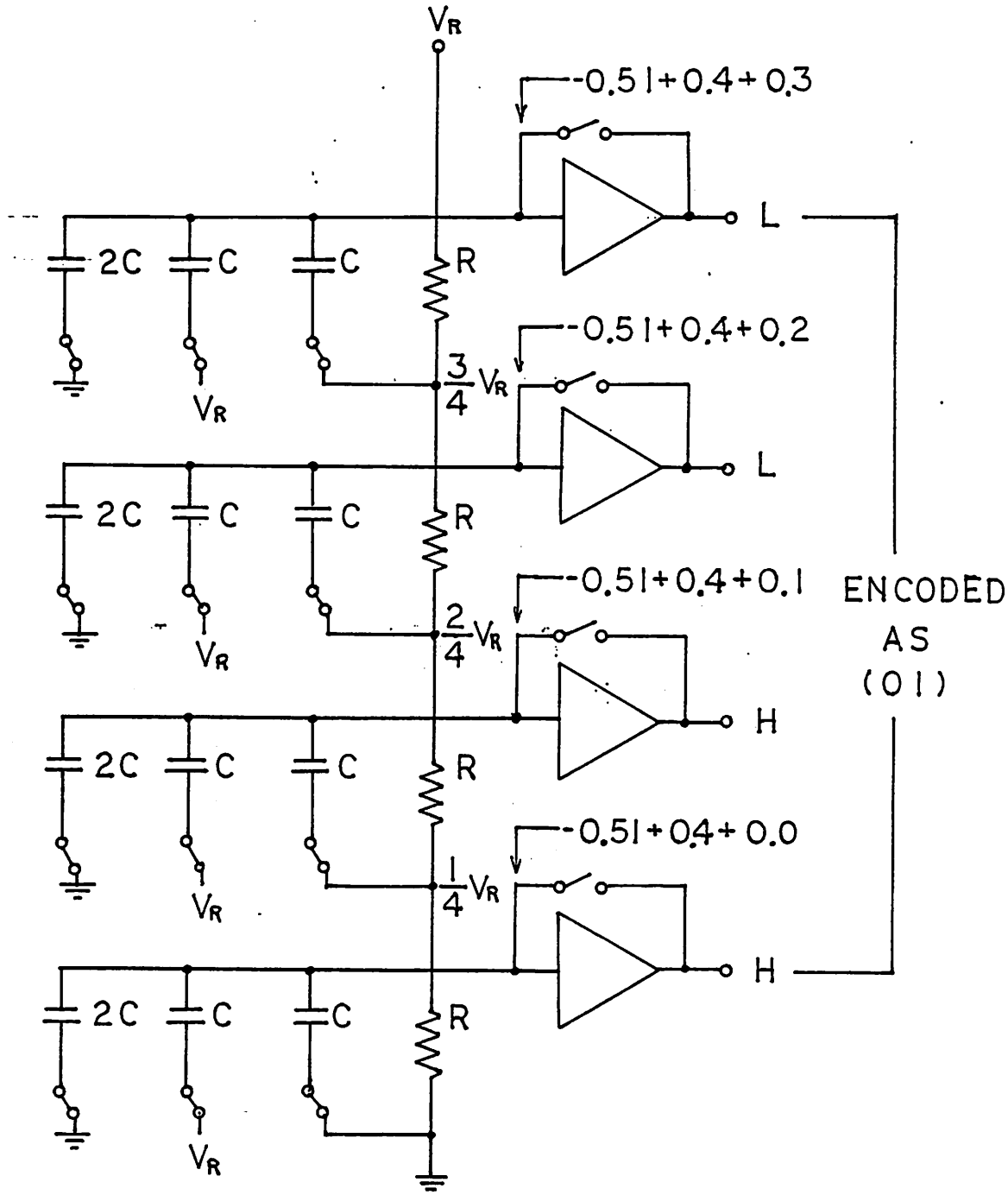


Fig. 2.1-4 LSBs A/D Conversion in the Two Step Parallel ADC

(Vref = 1.6V, Vin = 0.51V)

2.2 Fully Differential Configuration

In the previous section, the basic circuit configuration of the ADC has been described. Here, the fully differential version of the same architecture will be discussed.

The advantages of the fully differential configuration is in the increase of the immunity against various common mode noise, and in the doubling of the signal swing. These factors are important in the realization of a high speed high resolution ADC.

Fig. 2.2-1 shows the basic circuit using a 4 bit model. Fig. 2.2-2 shows the timing chart for its operation. The input signal is supplied in a differential mode at V_{in+} and V_{in-} If the input signal is supplied from a single ended device, a precise single to differential mode converter is required. The low input impedance is essential in this ADC. Consequently, a precise transformer will be the best device for this conversion.

In the following part, the A/D Conversion process will be explained. First, the sampling control signals SMPLB and SMPLT are set in their high level (H). Q1 and Q6 turns on, and the input signal is sampled in each capacitor. At the same time, the reset control signal RST is set H, and this closes the loop of the amplifier, sampling its offset voltage in the input capacitor C_{in} In the actual case, multi-stage amplifiers are used, in order to achieve a high gain and high speed. (Sec 3.4) Three reset pulses RST1, RST2 and RST3 are shown in the figure. They are opened in that order to sample the feed-through charge from the transistors closing the loop. (Sec 3.3)

After the reset of the amplifiers, (15 ns in Fig. 2.2-2) the sampling switches are open at the same time. Then at 17 ns, the evaluation begins when COMP1 is turned H. There, the capacitors in the array are connected either to ground or V_{ref} , depending on the code of the comparator. For example, the code of the uppermost comparator is $(11)_2 = 3$. In this case, both 2C and C are connected to the V_{ref} .

During the evaluation period, the small difference between the input signal and the reference is amplified to a sufficient value to turn the latch in the desired direction. This

voltage depends on the device parameter variation of the latch, and is in the order of 100 mV. (Sec 3.2) The time required to achieve this value from the smallest signal of 1 mV is around 10 nS, when three stage amplifier each of the gain-band width of 1,200 Mrad/sec is used. (Sec 3.4) When a sufficient amplification is attained, the strobe STRB is turned H and the output of the comparator is latched.

The encoder consists of three input NOR gates and a NOR form complementary 2 bit encoder. The three input NOR gates are used to decode the signal level from the outputs of the comparators. Fig. 2.2-3 shows two possible circuits for the signal level decoder. Here, the circuits in Fig.(A) are using exclusive OR (EXOR) for the decoding. In figures (A-1) and (B-1), the operation without error are shown. Only one of the EXOR or the NOR becomes 1, and that shows the place where the output of the latches turn from 1 to 0. Fig. (A-2) and (B-2) show the decoding process with the existence of an error output from the 4th comparator. In the circuit using EXOR, three gates shows the output of 1, resulting in a error after the NOR form decoder. On the other hand, the decoder using NOR indicates only one position without error. This circuit has such a redundancy that it detects only the first change from 0 to 1 in the comparator's output. However, if the error comes in the third comparator in Fig. (B-2), the decoder will indicate a wrong position. But, this does not make a fatal result. This NOR decoder is now widely used in the flash type ADCs.

For a 4 bit ADC, this NOR gate must drive 2 gates, and for 10 bit ADC, 5 gates, which is not a large load. The delay time here can be designed to be less than 1 ns.

In the NOR form 2 bit decoder, 2 transistors are connected in parallel to the vertical signal line. For the 10 bit ADC, this becomes to 16 transistors in parallel. The load capacitance here is the junction capacitances of the 16 NMOS transistors in parallel, the junction capacitance of the PMOS pull-up transistor and the gate capacitance of the output latch. Again this load is not so large and a delay time less than 2 ns can be achieved in this stage.

The output latch for the MSB signals are also used in the feed-back loop of the ADC to hold the MSB data. It must operate as quick as possible, so that output buffers are required to make its capacitive load small.

The most critical part in the MSB data feed-back path is the driving of the bottom switches for the LSB evaluation. (Q3, Q4 and so on) For a 10 bit ADC 64 bottom switches are connected in the vertical control line. If a unit transistor of W=10 μm and L=2 μm is considered, the scaled transistor Q3 or Q4 will have the width W of 160 μm. This results in the load capacitance of 30 pF. In order to design the delay time within 5 ns, a large size driver with the W of around 150 μm will be required for the driver of the most-significant-bit capacitor's bottom switch. Also to drive this large size transistor, a series of inverters scaled by the factor of 1/e will be required.

Taking all these factors into consideration, the delay of this feed-back path could be estimated to be less than 10 ns.

After the MSB data are reproduced in the capacitor array, and the 32 level reference voltages (4 level in this figure) are supplied through Q5, the LSB evaluation starts. After a sufficient amplification can be attained as before, STRB is turned H and the signal is latched.

The LSB data is decoded to a binary code by the same decoder used for MSB.

From this rough estimation, one cycle of conversion can be estimated to be 60 ns at least. In the following section, a SPICE of the full comparator circuit has been performed. It doesn't include the logics, but it shows that a 10 bit resolution can be achieved with the cycle time of 60 ns. There, 10 ns of logic delay has been assumed.

In the actual case, the change of the input signal during the evaluation must be considered. For a numerical example, the 2.5 V full swing signal of 5 MHz has the maximum rate of change of 79 mV / ns. The ADC must sample and hold this signal. The techniques used to solve this problem will be discussed in detail by J. Doernberg [1].

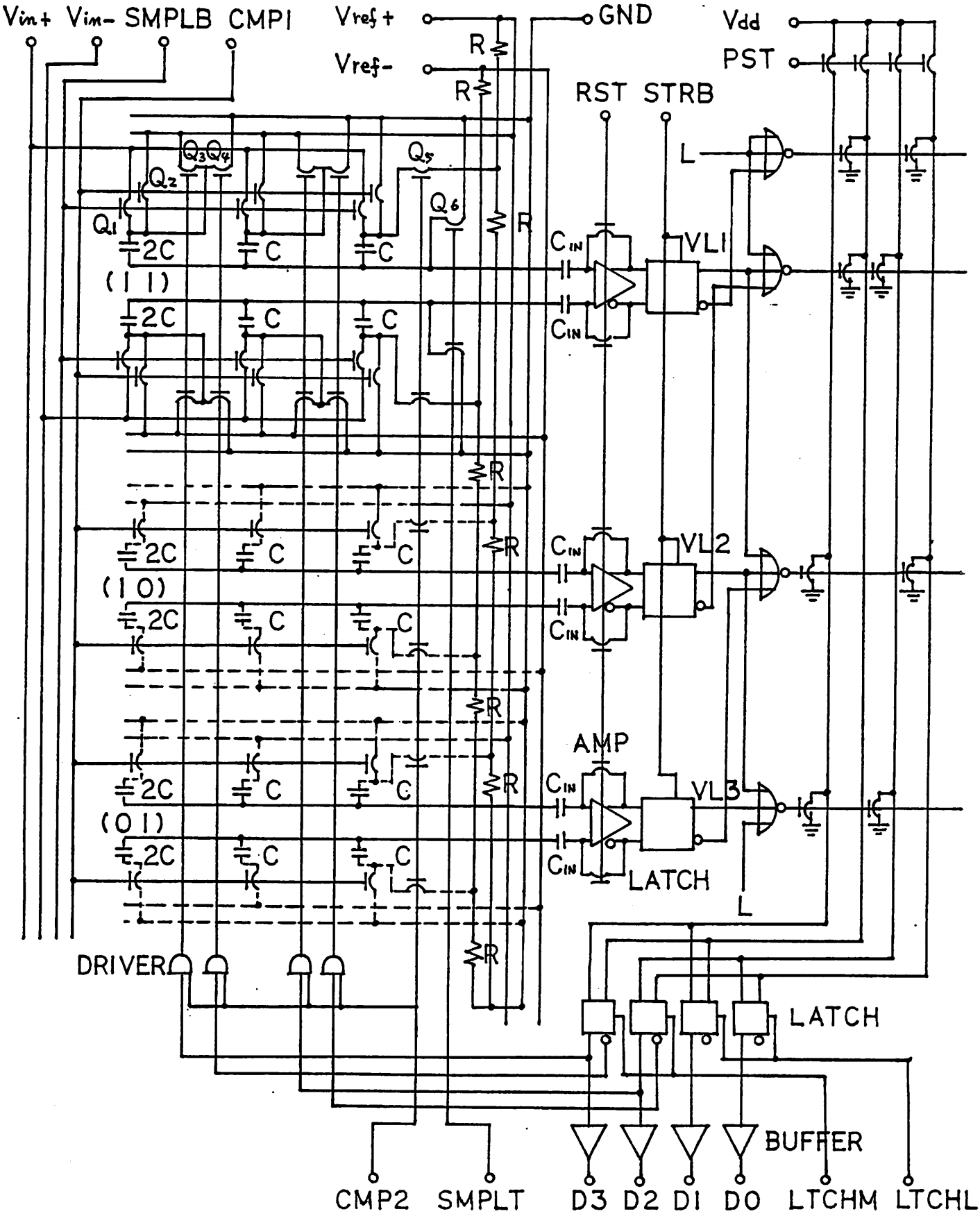


Fig. 2.2-1 Fully Differential Configuration of the A/D Converter (4 bit Model)

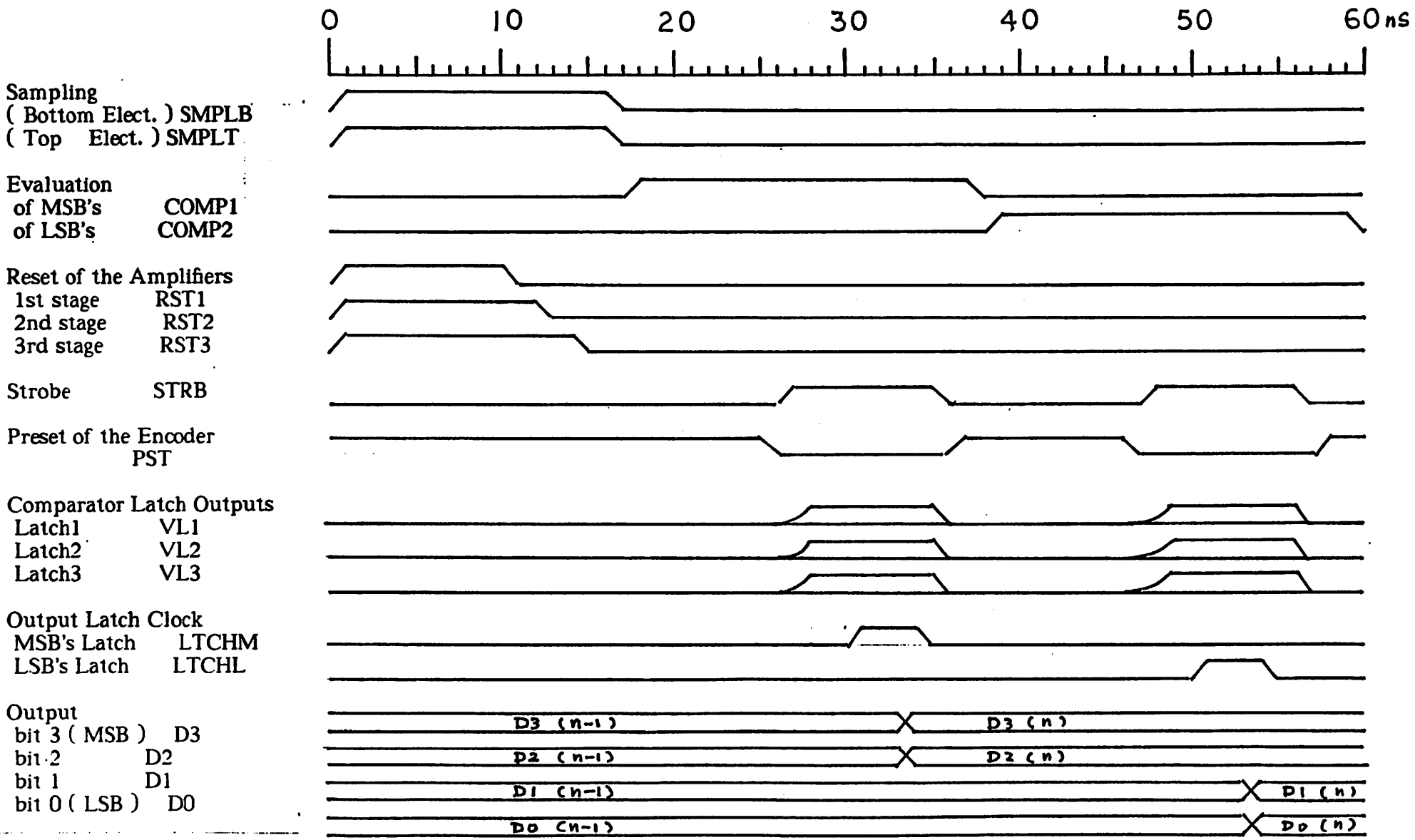


Fig. 2.2-2 Timing Chart of the A/D Converter

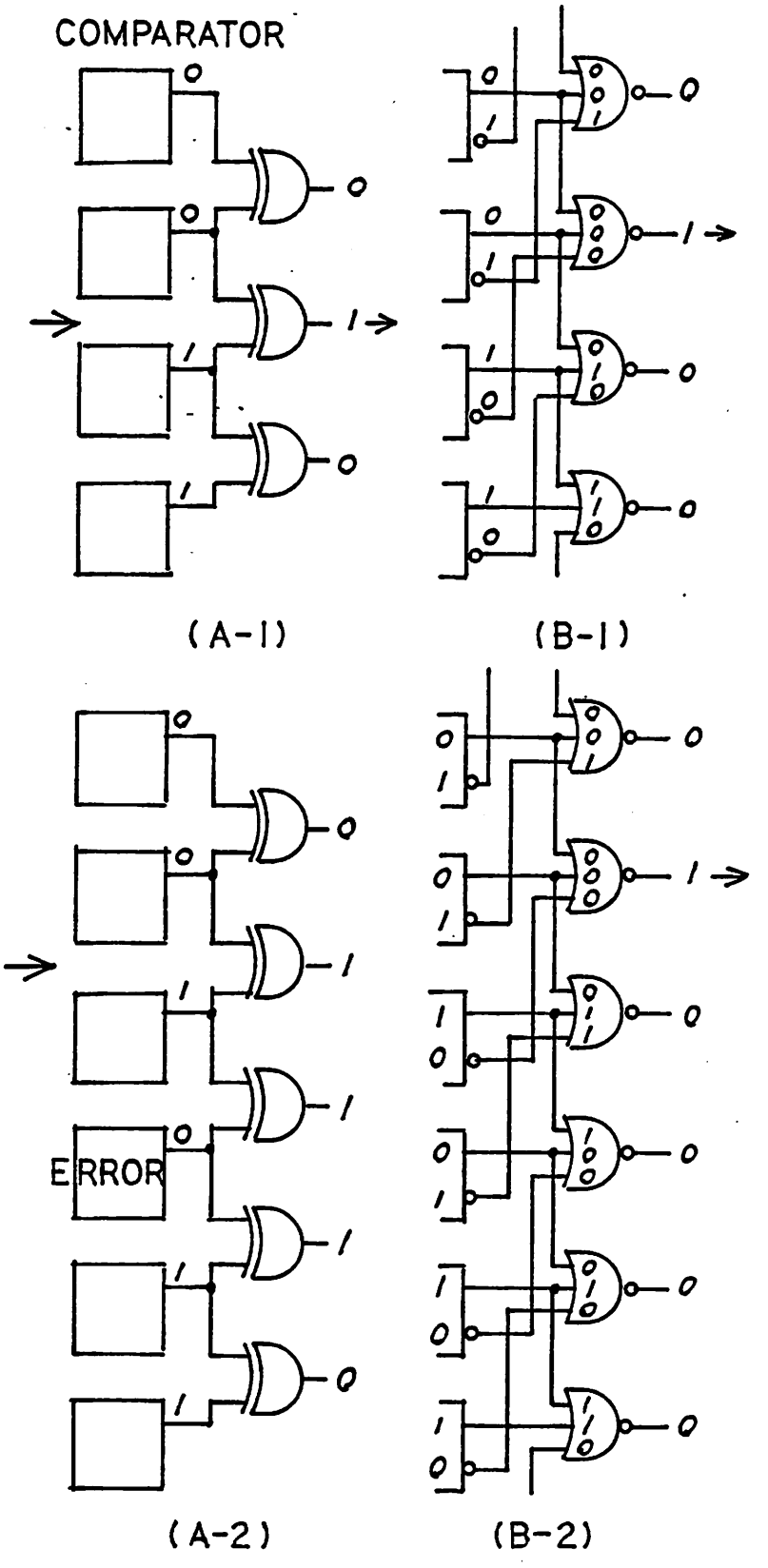


Fig. 2.2-3 Function of the Signal Level Decoder

CHAPTER 3 COMPARATOR DESIGN

3.1 Introduction

The most critical part for the designing of a high-speed high-precision ADC is the comparator. This is true especially for the two step ADC, where the comparator must operate in twice the speed of a conventional flash type ADC.

CMOS amplifiers inherently suffers from a large offset voltage. On the other hand, their input impedance is so high that it is easy to sample these offset voltages in capacitances. However, the problem of feed-through charge injection from the loop-closing switches arises. To solve this problem, a special sequence for the loop-closing switch operation is used. This is reviewed in Sec. 3.3. Moreover, the advantage of a fully differential configuration to prevent amplifier's saturation by these feed-through charge has also been discussed.

The reset speed is equally important as the signal evaluation speed. Sometimes it takes as much time as in the evaluation. The speed and stabilization during the reset operation is discussed in Sec.3.4.

For a high-speed high-precision comparator, the utilization of a multi-stage amplifier configuration is essential. Basic analysis and SPICE simulations of this multi-stage configuration are reported in Sec.3.5.

The amplifier to be used in this configuration should have a much higher gain bandwidth than the conventional CMOS amplifiers. Some new approach for the design of these amplifiers has been discussed in Sec.3.6.

A regenerative latch is required to amplify the small signal to a logic level and then hold it. The speed of a latch depends not only to the transient response speed, but also to its sensitivity, or the minimum input signal required to amplify the input signal in the correct direction. Sec. 3.2 explains these points in detail.

In the last section of this chapter, a SPICE simulation of a full circuit of the comparator has been performed. This simulation has been accomplished in an early stage, before the optimization of the amplifiers described in Sec. 3.6. Therefore, an early version of a fully differential amplifier has been used. However, it demonstrated the feasibility of this ADC architecture and the 3 stage amplifier with one latch configuration.

3.2 High Speed Latch Design

The speed of a latch can be determined by two factors. One is the transient speed, and the other is the sensitivity or the minimum input signal required to amplify the signal in the desired direction.

When a latch with a cross-coupled common-source transistor couple is considered, the transient response is an exponential one. The input signal is amplified rapidly by its positive-feedback mechanism. This is explained in detail in the appendix A. The time constant there can be calculated as C_L/g_m, where C_L is the load capacitance and g_m is the trans-conductance of the driver transistor.

Even with the high speed transient response, the overall speed of the latch depends also on its sensitivity. If the sensitivity is low, much time should be spend at the amplification in the previous stages to acquire a sufficient amplitude of the signal. The sensitivity of the latch is analyzed in detail in appendix B.

Fig. 3.2-1 shows the basic circuit of the latch used in the SPICE simulation of the full size comparator. (Sec 3.7) Here, the last stage of the multi-stage amplifier m3 and m4 is merged with the cross-coupled transistor latch m1 and m2. The load transistors m5 to m8 are used in common. The selection between the amplifier and the latch is performed by two transistors m9 and m10. By this configuration, the signal from the amplifier is directly coupled to the latch, making the transient speed fast. The drawback of this circuit is that the amplifier cannot be reset independently. However, the offset in the last stage result in a small equivalent input offset, divided by the gain of the previous stages. (Sec 3.3) In the actual circuit, more switch transistors are required for the proper operation. These are explained in Sec. 3.7.

A basic SPICE simulation has been performed for the design of the latch. Fig. 3.2-2 shows the circuit used there. Here, the differential input signal V_{in} is sampled directly to the drains of m1 and m2 through the transistors m3 and m4. During the sampling period,

the sources of m1 and m2 are connected to some bias voltage V_B to cut off these transistors. After the sampling is finished, the strobe pulse STRB is turned high and after a certain delay time of T_i, the current sources IL1 and IL2 become active. The difference in the threshold of the transistor pair m1,m2 and the difference in the current of the sources IL are described by offsets V_{os} and I_{os} respectively.

The load current is 100 μA , the load capacitance C_L is 0.1 pF and the dimensions of the driver transistors m1 and m2 are W/L = 27 μm / 2 μm.

Fig. 3.2-3-1 shows the simulation result when no offset exists. The node voltages V1 and V2 falls due to the difference between the current IL1+IL2 and the current flowing m6. The differential output V1-V2 increases exponentially as calculated in appendix A. The time constant in the simulation result is 0.5 ns. The time constant estimated from C_L / g_m = 0.1 pF/285 $\mu A / V$ is 0.35 ns.

Fig. 3.2-3-3 shows the simulation result with an offset of V_{os} = 20 mV. It is clear from appendix B, Eq. (B-18) that the minimum input voltage to amplify the signal in the desired direction is just V_{os} = 20 mV. In this simulation, the input voltage is in its critical value of 20 mV, and the signal has been amplified in the wrong direction.

In Fig. 3.2-3-3 , the offset voltage is still assumed to be 20 mV. However, the input signal is increased to 30 mV, and the signal is amplified in the correct direction.

Fig. 3.2-3-4 shows the simulation under the offset current I_{os} = 20 μA and the input signal of 20 mV. From appendix B Eq. (B-18), the sensitivity of the latch can be estimated as:

$$\frac{I_{os}}{\alpha C_L (V_{s0} - VC + V_{th})}$$

Here, α is the rate of voltage change in the source of m1 and m2, V_{s0} is the initial voltage of that source, VC is the common mode voltage at the input, and V_{th} is the threshold voltage of the driver transistors m1 and m2. This value can be calculated to be 260 mV, under the condition of α = 334 mV / ns, V_{s0} = 2.5 V, V_{th} =0.8, VC=1.0 V and C_L = 0.1pF.

This is a relatively large value.

Fig. 3.2-3-5 is the simulation result of the latch with the same current offset I_{os} as before, but with the input voltage of 100 mV. Here, the signal has been amplified in the correct direction. The critical sensitivity seems to be less than the value of 260 mV calculated above.

As shown in the appendix B, this poor sensitivity due to the offset I_{os}, can be improved by supplying the current with a certain delay T_i after the strobe. During this delay, the latch can amplify the signal to a sufficient value, without experiencing the current offset. This is shown in Fig. 3.2-3-6. Here, the load current is activated 1 ns after the strobe signal. The signal is amplified sufficiently before the current sources are activated, and the signal is amplified in the correct direction. This technique is also used in the DRAM sensing amplifiers.

As the conclusion of this section, the speed of a latch is determined not only by the transient response, but also by the sensitivity of the latch. Fqually attention should be paid to the matching of the current sources and driver transistors, as well as its current amount and device size.

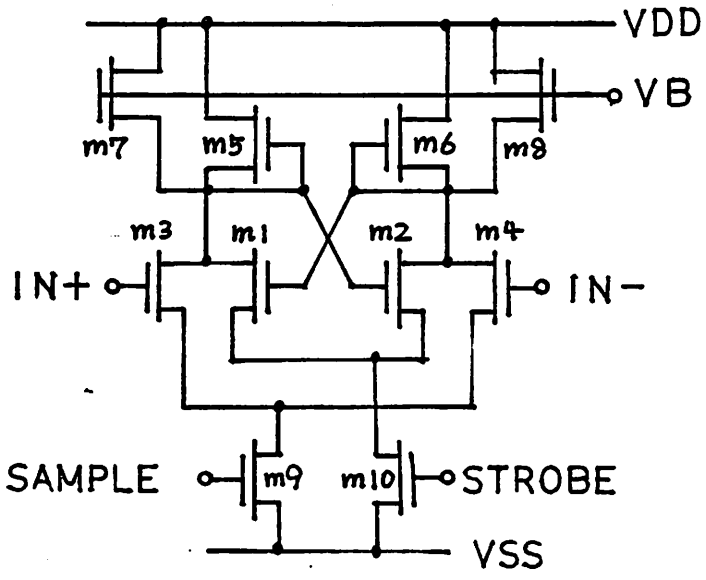


Fig.3.2-1 Basic Circuit Configuration

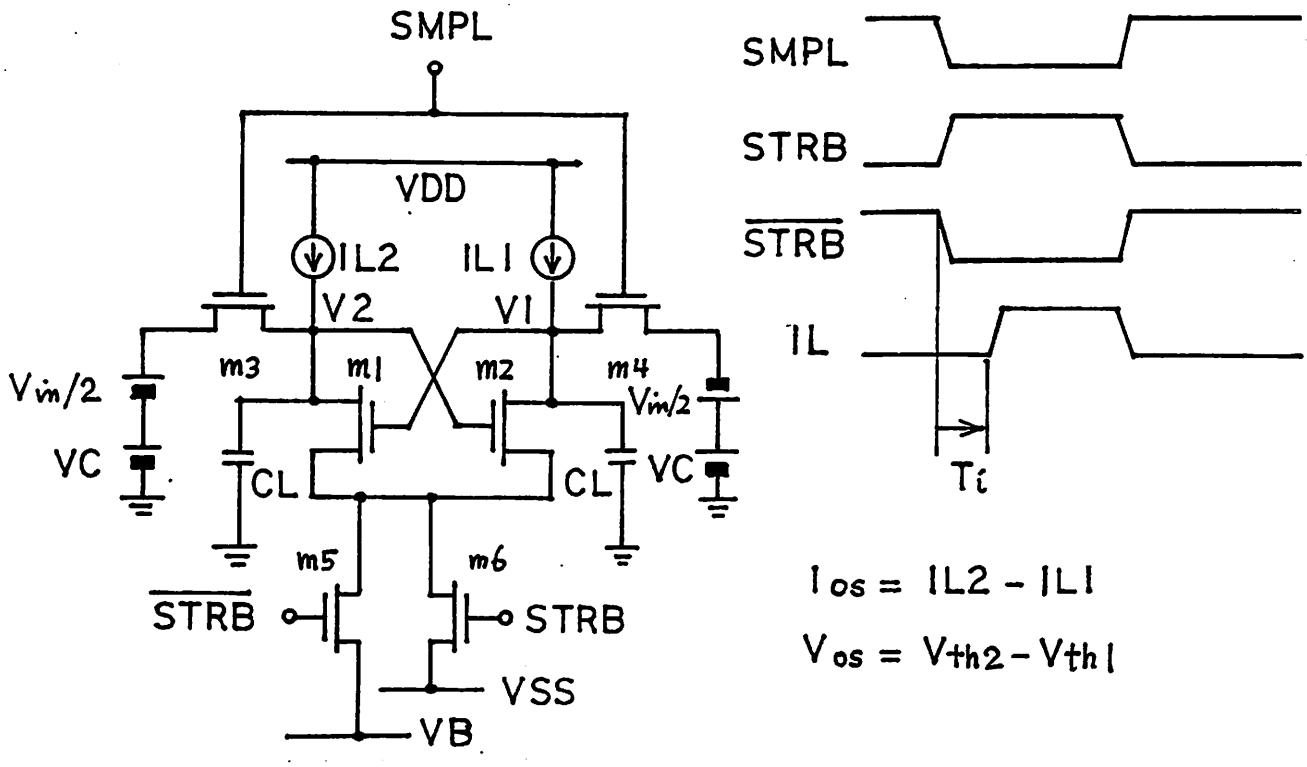


Fig.3.2-2 Circuit used for a Basic Simulation

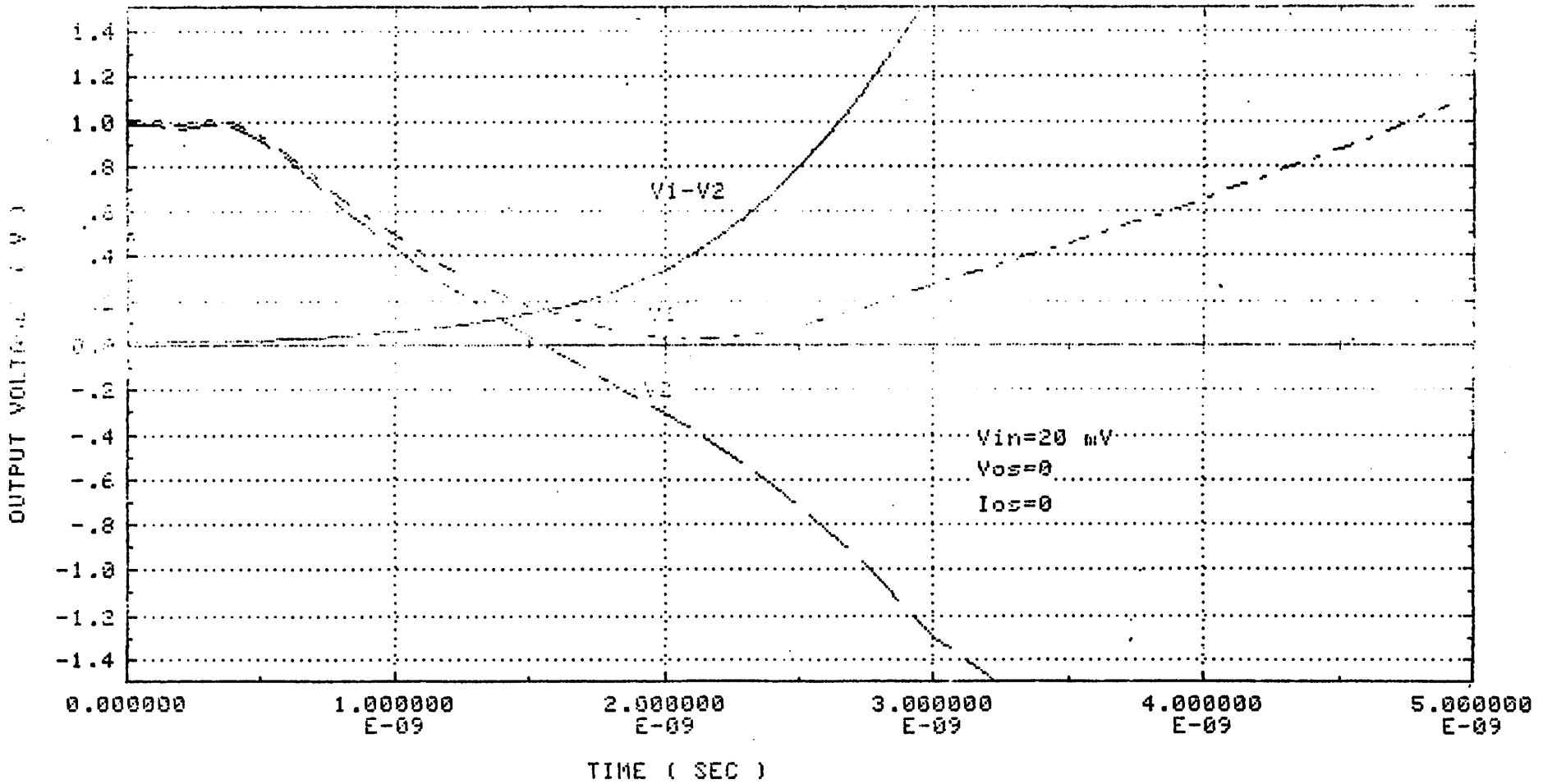


Fig.3.2-3-1 Simulation Result (1)

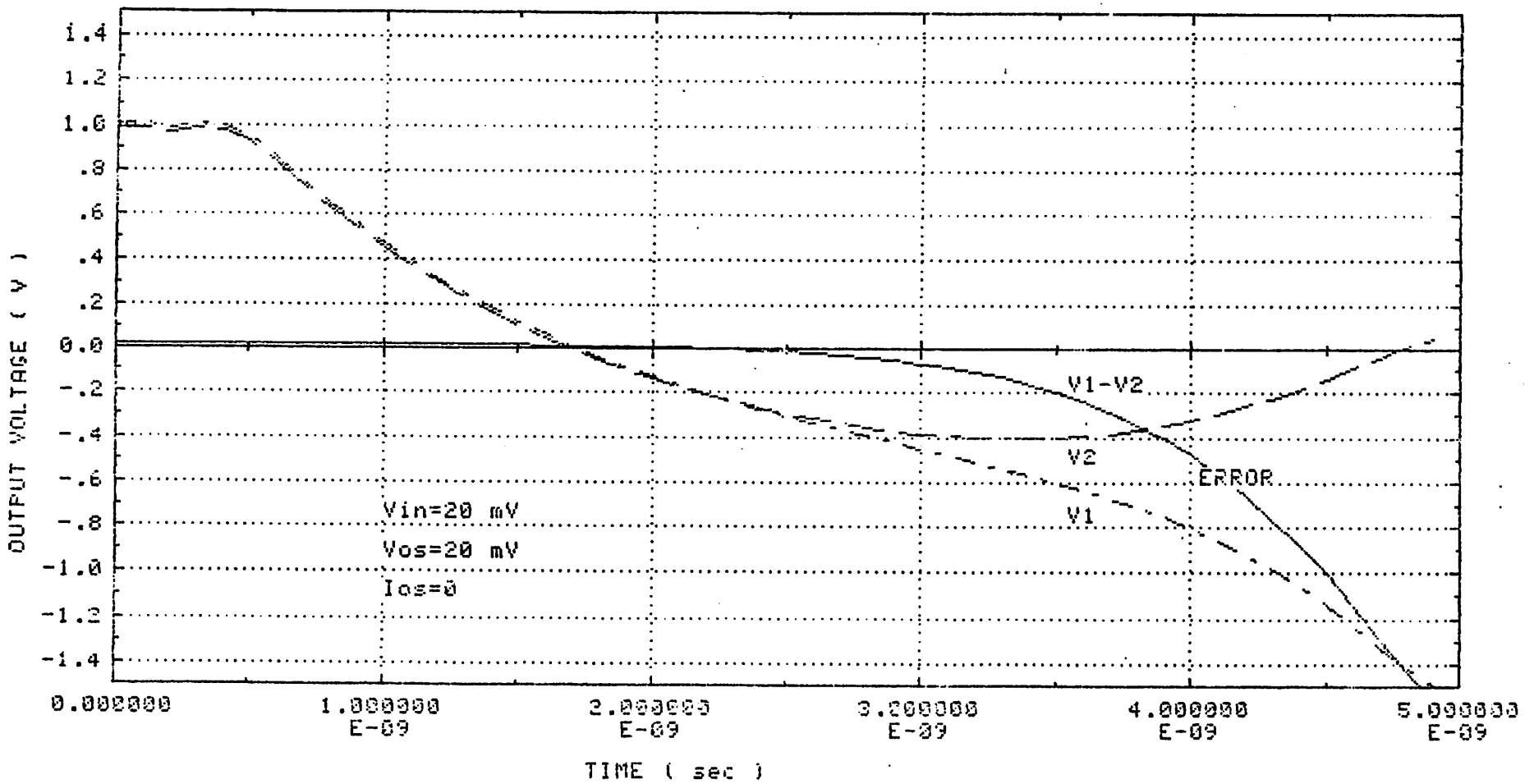


Fig.3.2-3-2 Simulation Result (2)

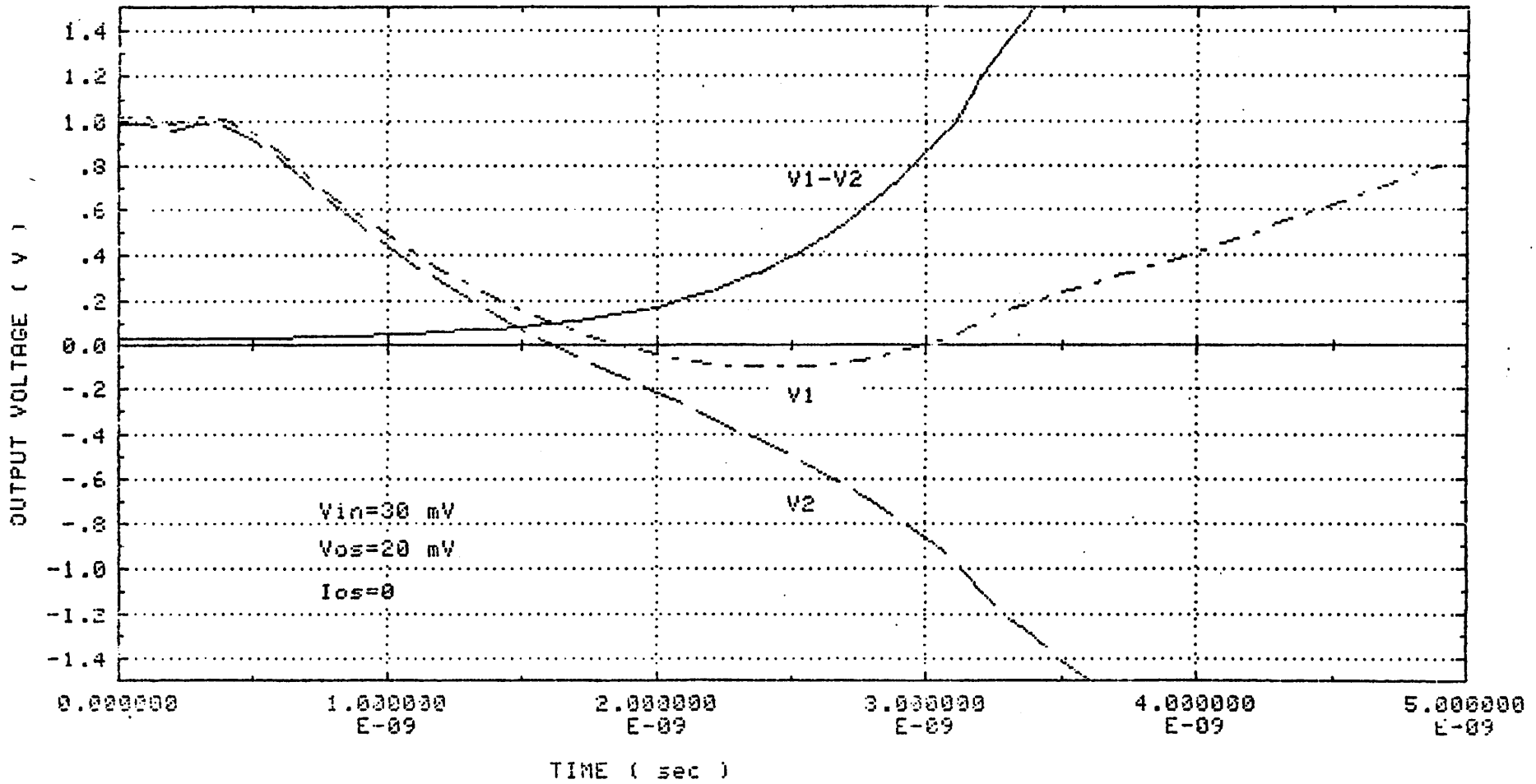


Fig.3.2-3-3 Simulation Result (3)

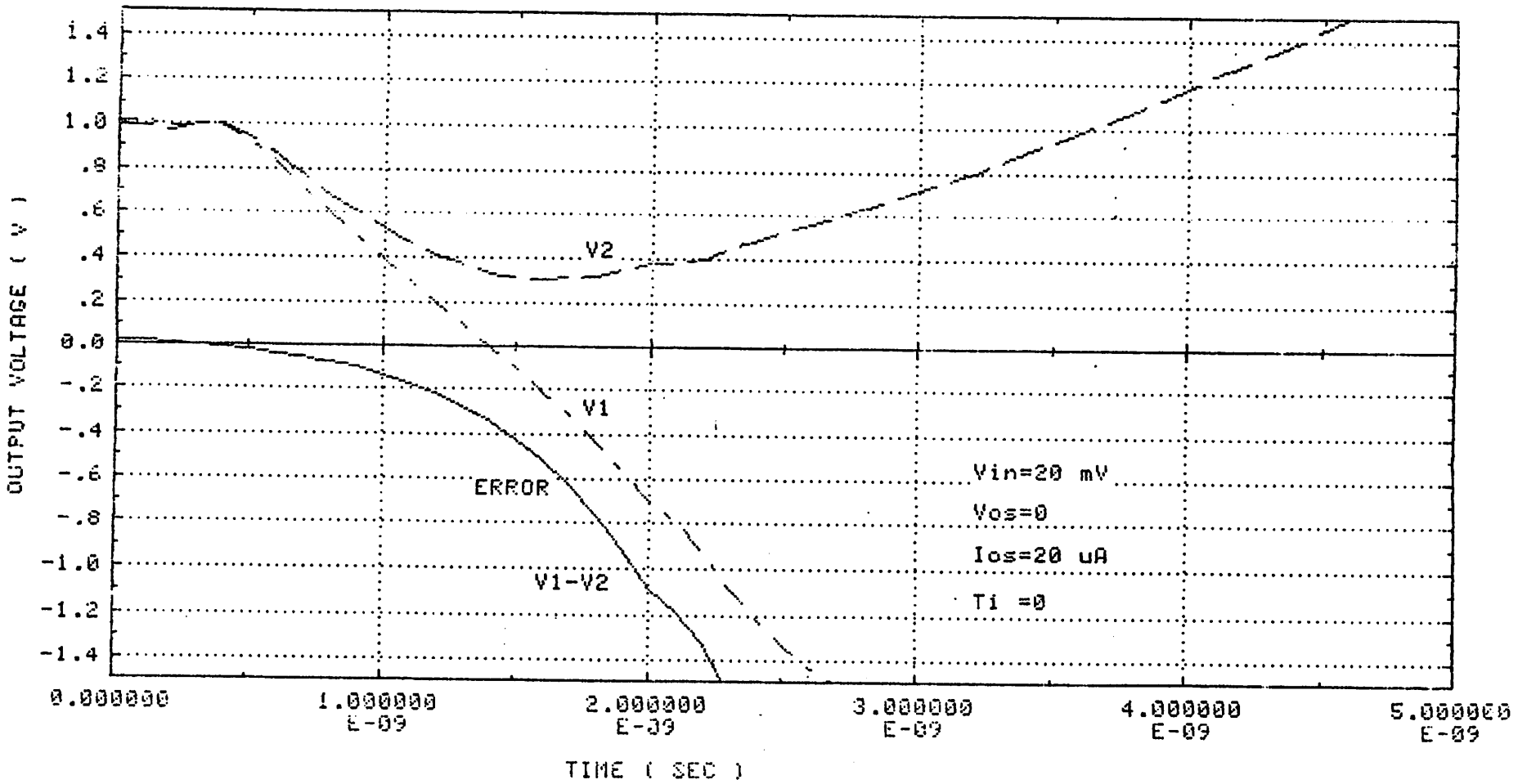


Fig.3.2-3-4 Simulation Result (4)

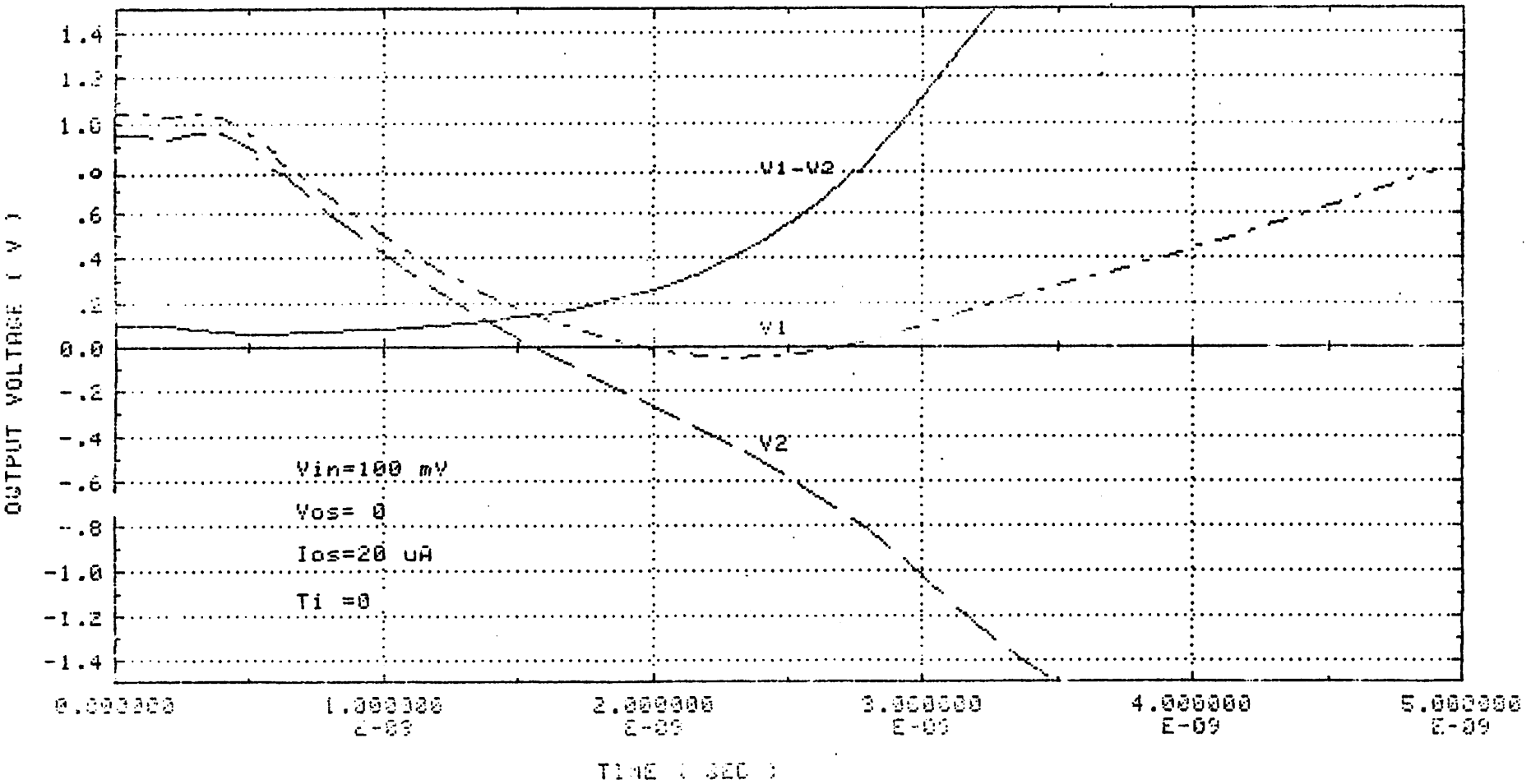


Fig.3.2-3-5 Simulation Result (5)

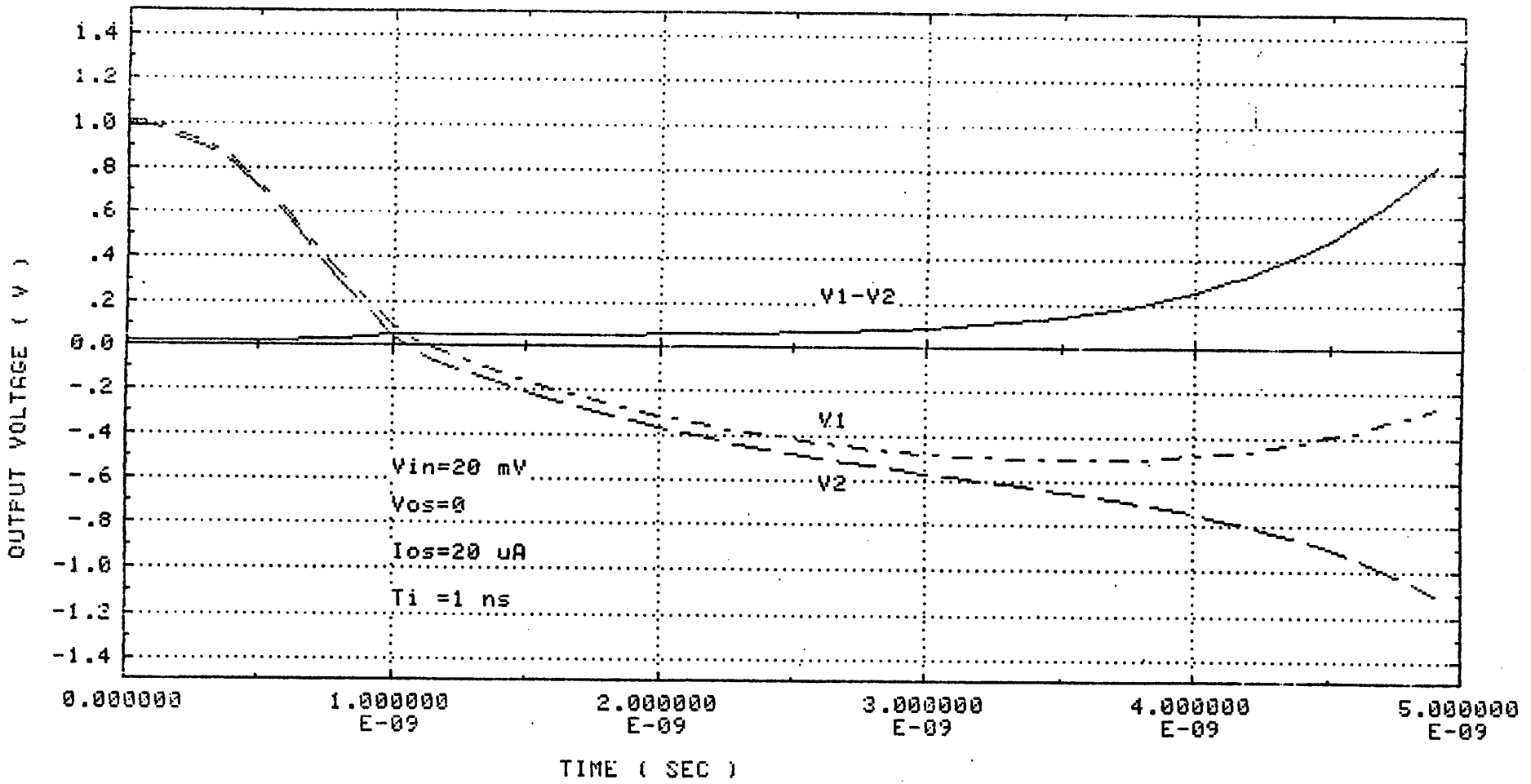


Fig.3.2-3-6 Simulation Result (6)

3.3 Offset Cancellation of the Multi-Stage Amplifier

The offset voltage of a MOS amplifier is much larger than that of the bipolar amplifiers. Even with the well controlled fabrication process, the mismatch of the threshold voltage between two adjacent transistor is larger than 10 mV. This value is about 10 times larger than the $\frac{1}{2}$ LSB voltage of 1 mV. (Here, a 10 bit ADC with the reference voltage of 2.048 V has been assumed.)

On the other hand, the MOS transistors have a very high input impedance which make the holding of a signal very easy. By utilizing this property, the offset voltage can be stored on a coupling capacitor which is connected between the multi-stage amplifiers. Moreover as described below, the feed-through charge can also be stored in these capacitors by a proper sequence of the reset switches.

Fig.3.3-1 shows a multi-stage amplifier of three stages and its reset switch operation sequence. There are many orders in the sequence to open these switches after the reset has been accomplished. (3!=6 ways) Here, the two extreme cases has been examined.

In this figure, the switches are opened from the top (left) to the last (right). When all those switches are closed, the offset voltage V_{osi} appears in the output and input terminal of each amplifier. When the leftmost switch is opened, the feed-through charge CV_{ft1} is stored at the input node. At the same time, V_{ft1} is amplified by the first amplifier and that voltage is stored on the coupling capacitor connected in the output of the first amplifier. This is capable, because the second amplifier is in a closed-loop state, and consequently its input node voltage is fixed to its offset voltage V_{os2}.

In this order, the second and third switches are opened. On the last stage, the output appears to be;

$$V_{os3} - A\,3V_{ft3}$$

This offset is referred at the input equivalent offset voltage V_{eos} as;

$$V_{eos} = \frac{V_{os3}}{A_1 A_2 A_3} - \frac{V_{ft3}}{A_1 A_2}$$

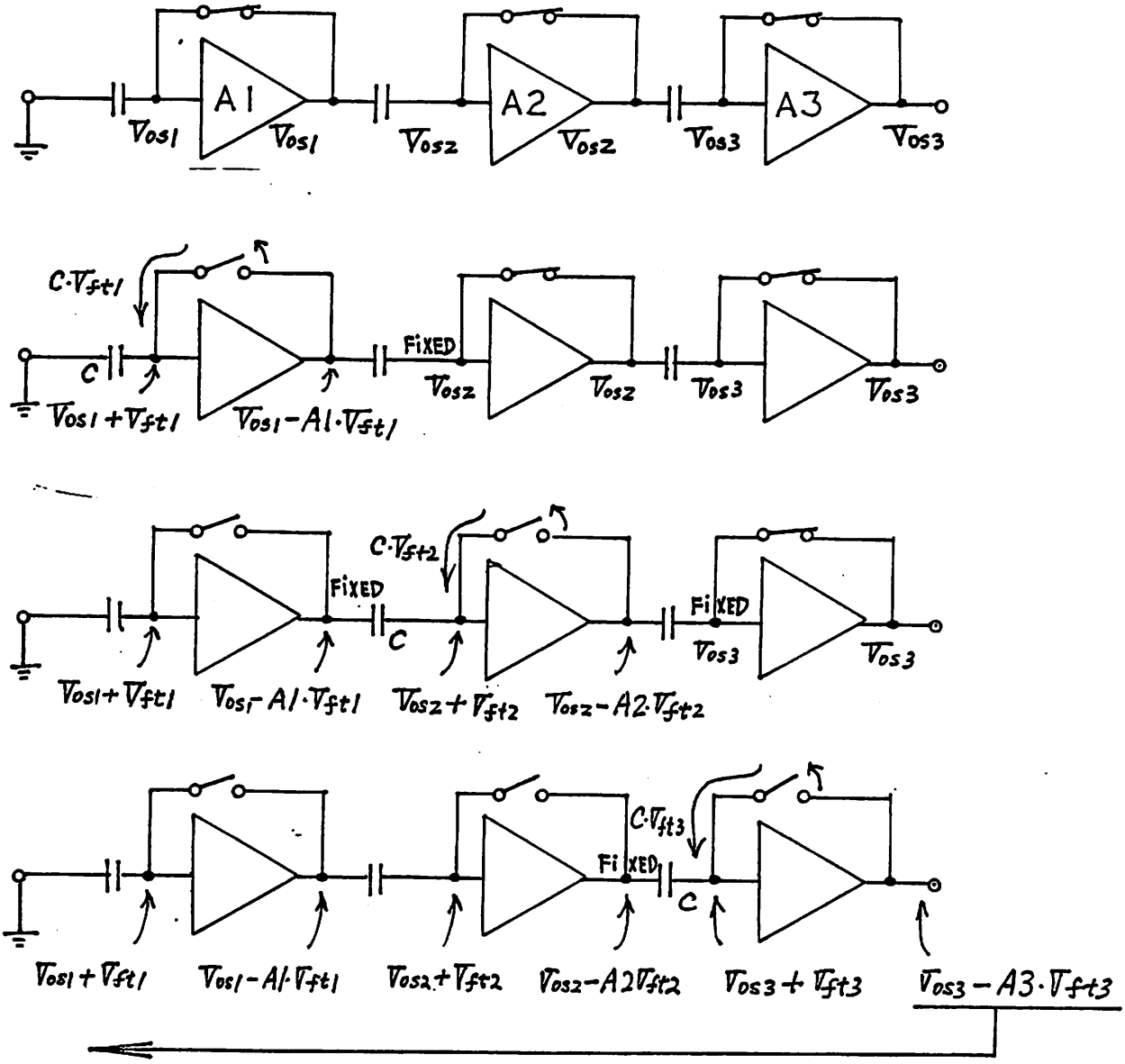
If the gain of the amplifiers is sufficiently large, the input offset voltage can be suppressed within $\frac{1}{2}$ LSB. As a numerical example, suppose that the offset voltage V_{os} is 10 mV, the feed-through voltage V_{ft} is 0.354 V (switch size W/L= 5 μm / 2 μm, C_{ox} = 1.4 fF/ μm^2, control voltage swing 5 V and C= 0.2 pF) and the gain is A1=A2=A3=10.

From the equation above, V_{eos} is -0.77 mV, which is less than $\frac{1}{2}$ LSB.

The drawback of this single-ended circuit is the saturation of the amplifier by the large feed-through voltage. For example, the output voltage of the last stage is -1.75 V, which is large enough to saturate the last stage. As described in the following, this problem can be solved by using a fully-differential configuration.

Fig.3.3-2 shows the offset voltage when the switches are opened in the order of right, middle and left. This is the other extreme case. Once the switch in A3 is opened, its input node becomes floating and the amplifier is active. Under this condition, the feed-through voltages from the previous stages are amplified. This results in a large offset voltage as shown in the figure.

Fig. 3.3-3 shows the offset sampling for a fully-differential configuration. The equivalent input offset voltage V_{eos} has the same value with the non-differential configuration. However, the advantage of this configuration is in the small feed-through voltage amplification. As shown in the figure, only the difference of the feed-through voltage ΔV_{ft} is amplified. If the dimension of the switches is matched within 10 %, the output swing due to the feed-through amplification can be reduced to 10 % of the previous value. With the same parameters used above, the output voltage due to the feed-through $A_3 \Delta V_{ft3}$ can be reduced to 177 mV. This value is small enough to prevent saturation.

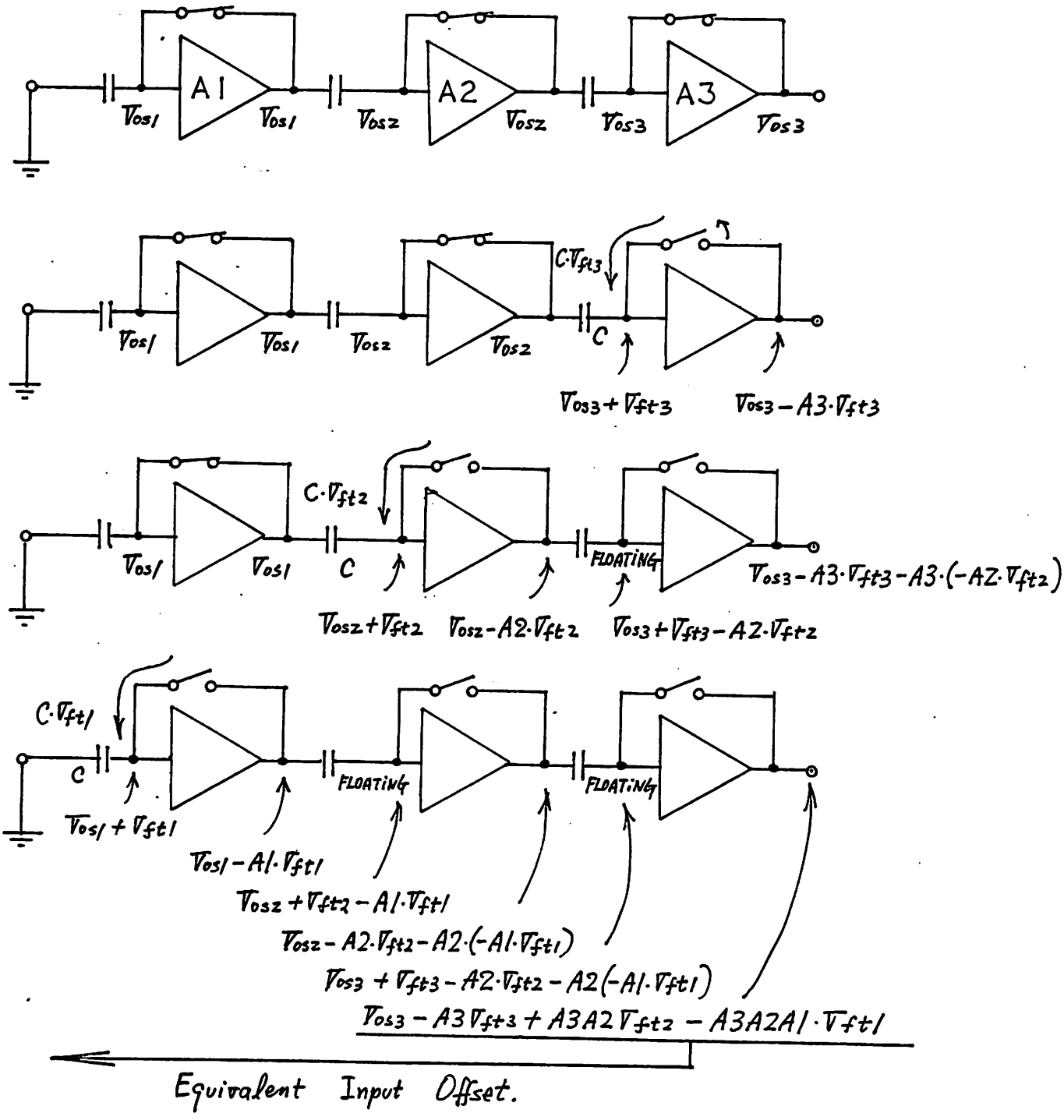


Equivalent Input Offset

$$V_{eos} = \frac{1}{A1 \cdot A2 \cdot A3} \left(V_{os3} - A3 \cdot V_{ft3} \right)$$

$$= \frac{V_{os3}}{A1 \cdot A2 \cdot A3} - \frac{V_{ft3}}{A1 \cdot A2}$$

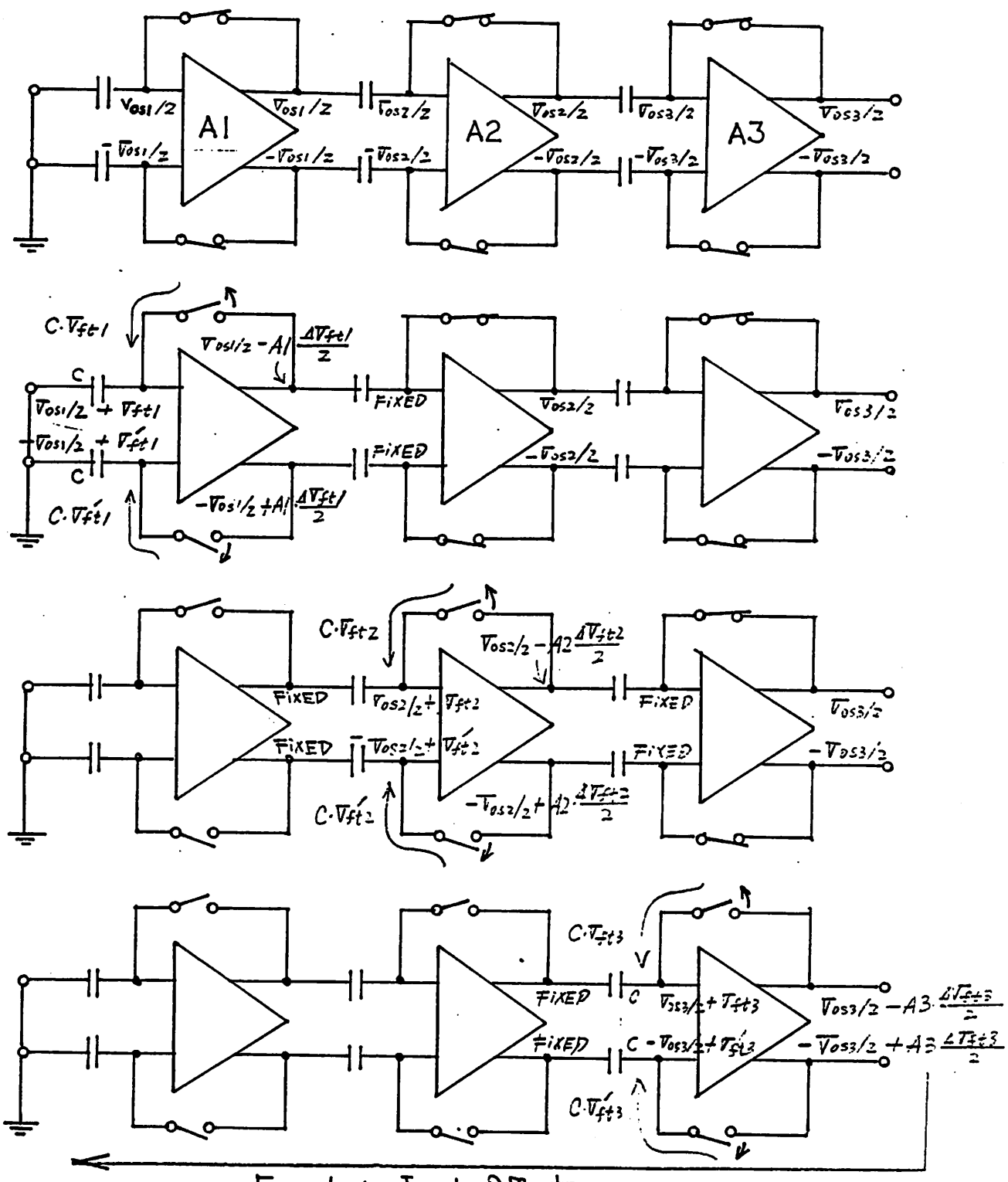
Fig.3.3-1 Sampling of the Offset and Feed-through Voltage in a Single-Ended Multi-Stage Amplifier (Correct Sequence)



$$V_{eos}=\frac{1}{A1\cdot A2\cdot A3}\left(V_{os3}-A3V_{ft3}+A3A2V_{ft2}-A3A2A1\cdot V_{ft1}\right)$$

$$=\frac{V_{os3}}{A1\cdot A2\cdot A3}-\frac{V_{ft3}}{A1\cdot A2}+\frac{V_{ft2}}{A1}-V_{ft1}$$

Fig.3.3-2 Sampling of the Offset and Feed-through Voltage in a Single-Ended Multi-Stage Amplifier (Wrong Sequence)



$$V_{eos} = \frac{1}{A1 \cdot A2 \cdot A3}\left(V_{os3} - A3 \cdot V_{ft3}\right) = \frac{V_{os3}}{A1 \cdot A2 \cdot A3} - \frac{V_{ft3}}{A1 \cdot A2}$$

Fig.3.3-3 Sampling of the Offset and Feed-through Voltage in a Fully-Differential Multi-Stage Amplifier

3.4 Transient Response of the Multi-stage Amplifier

In this section, the design of the optimum number of stages N for the multi-stage preamplifier will be discussed. For the first order approximation, a single pole amplifier will be used in the following analysis. This is a reasonable assumption for the single differential amplifier followed by a source follower, which are going to be used in this comparator design. If we assume the DC gain and cut off frequency of such an amplifier to be Ao and ω_c , respectively, its transfer characteristic will be;

$$A(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_c}} \tag{3.4-1}$$

The step response for the amplifier above can be easily calculated to be;

$$V_{out}(t) = A_0 V_{in}(1 - e^{-\omega_c t}) \tag{3.4-2}$$

Here, Vin is the amplitude of the input step. The acquisition time required to get the output to Vreq is;

$$T_{acq} = \frac{1}{\omega_c} ln\left(\frac{1}{1 - \frac{V_{req}}{A_0 V_{in}}}\right) \tag{3.4-3}$$

If the product of the DC gain Ao and the input voltage Vin is much larger than the required output swing Vreq, the equation above will be simplified as:

$$T_{acq} \approx \frac{1}{\omega_c} ln\left(1 + \frac{V_{req}}{V_{in} A_0}\right) \approx \frac{1}{\omega_c}\frac{V_{req}}{V_{in} A_0} = \frac{V_{req}}{V_{in}}\frac{1}{GBW} \tag{3.4-4}$$

The acquisition time is inversely proportional to the Gain Bandwidth, GBW = Ao ω_c .

Analogous to the single stage response, the response for the N stage preamplifier may be considered as follows. The GBW for the multi stage preamplifier can be calculated as in

the Appendix C, and its value is

$$GBW = \sqrt{2^{\frac{1}{N}}-1}\ \omega_c A_0^N \tag{3.4-5}$$

Next, some numerical examples are shown. Under the conditions of ω_c = 333Mrad , Ao=10 and Vreq/Vin=1000, Tacq is 0.723nS for N=4 and 0.0783nS for N=5. SPICE calculations have been performed for the same parameters, and the results are Tacq=7.0nS for N=4 and 5.25nS for N=5. The failure of the calculation above has come from the neglection of the phase shift for the multi-stage preamplifier. The phase shift at ω is not

$$\Phi = -Tan^{-1}(\frac{\omega}{\omega_m}) = -Tan^{-1}(\frac{\omega}{\omega_c\sqrt{2^{\frac{1}{N}}-1}}) \tag{3.4-6}$$

like a single pole amplifier, but

$$\Phi = -NTan^{-1}(\frac{\omega}{\omega_c}) \tag{3.4-7}$$

In this way, the phase shift increases proportionally to the number of stages N, and this makes the delay much greater than that estimated by Eq. (3.4-3) to (3.4-5).

The SPICE calculation can give us the correct answer, but it is insufficient if an intuitional search for the optimum number of stages N is required. In the following, a very simple analytical equation for the acquisition time Tacq will be presented. It coincides with the results of SPICE with a relatively small error, and moreover it can explain the dependence of Tacq on ω_c , A_0 and N more clearly.

The accurate calculation for the transient response of the multi stage preamplifier has been performed in Appendix C. Here, the solution is repeated.

$$V_{out}(t) = A_0^N V_{in}\left\{1-e^{-\omega_c t}\sum_{k=0}^{N-1}\frac{(\omega_c t)^k}{k!}\right\} \tag{3.4-8}$$

Fig. 3.4-1 shows the transient response for a series of multi-stage amplifiers, calculated from Eq. (3.4-8) and from SPICE. The curves calculated from the equation above coincide well with those calculated by SPICE with a small error.

Fig. 3.4-2 shows the transient response calculated from Eq. (3.4-8), but with the output voltage range equal to the input voltage of 5V. This is the situation experienced in a multi stage inverters (logic). Here, the greater the number of stages that are used, the greater the delay will be. This is different from the result above, where the input signal has to be amplified to a much higher value than the input.

Substituting Tacq for t and Vreq for Vout(t), in Eq.(3.4-8), and then solving for Tacq, we'll get:

$$T_{acq} = -\frac{1}{\omega_c} ln\left(1 - \frac{V_{req}}{A_0^N V_{in}}\right) + \frac{1}{\omega_c} \ln\left(\sum_{K=0}^{N-1} \frac{(\omega_c T_{acq})^k}{k!}\right) \qquad (3.4\text{-}9)$$

The first term in the right hand side is analogous to the right hand side of Eq. (3.4-3). The second term is added to that as the effect of the phase shift in the multi stage preamplifier. In order to make the dependence of T_{acq} on the GBW and Vreq/Vin much clearer, the following assumptions have been made.

$$V_{req} << A_0^N V_{in}$$
$$\omega_c T_{acq} << 1$$

Those mean sufficient gain and short acquisition time compared to $\frac{1}{\omega_c}$. Then Eq. (3.4-9) can be approximated as follows (Appendix E):

$$T_{acq} = \frac{1}{\omega_c}\left(\frac{6V_{req}}{A_0^N V_{in}}\right)^{\frac{1}{3}} \qquad (3.4\text{-}10)$$

From the equation above, it is much more effective to increase the gain Ao, rather than the cutoff frequency ω_c, in order to achieve a high speed acquisition. The difference is of the exponent factor of N/3-1. But in the actual implementation, the number of stages is

3 or 4. So there is not so much difference. Another interesting point is the dependence of T_{acq} on Vreq/Vin. It is proportional to the 1/3 power of Vreq/Vin and not to the value itself. This means that there is no significant acquisition time increase to get a high resolution (high Vreq/Vin) comparator. For example, the 1/10000 resolution can be achieved by only 10 times longer acquisition time compared to that of an 1/10 resolution.

Another approximation for T_{acq} has been reported. [13] That is reviewed in Appendix C and repeated here.

$$T_{acq} = \frac{1}{GBW}\left(\frac{V_{req} N!}{V_{in}}\right)^{\frac{1}{N}} \qquad (3.4\text{-}11)$$

In spite of its extreme approximation, it can explain the dependence of T_{acq} on Vreq/Vin or GBW from a qualitative point of view.

Fig. 3.4-3 shows the plot of Tacq vs N calculated from Eq. (3.4-11) , the accurate analytical Eq. (3.4-8), its approximated form of Eq. (3.4-10) and SPICE simulation. The accurate analytical equation coincides well with the SPICE simulation. Eq.(3.4-11) shows relatively small error compared to Eq (3.4-10). The following data are calculated by Eq. (3.4-8). However, Eq. (3.4-10) or Eq.(3.4-11) can help to make clear the relations between T_{acq} and Vreq/Vin or GBW. They will be discussed in the following.

Fig. 3.4-4 is a log-log plot of T_{acq} vs Vreq/Vin. It will be seen that T_{acq} is not directly proportional to Vreq/Vin, but rather proportional to its 1/N power, as in Eq.(3.4-11). The slope decreases slightly as the number of stages N increases.

Fig. 3.4-5 shows the dependence of T_{acq} on gain Ao, under the condition of a constant GBW of 1000Mrad. Here the value of Vreq/Vin=100. For N larger than 4, and gain larger than 10, T_{acq} is almost independent to the gain change. It is interesting that GBW solely can predict the response. This could be explained by Eq.(3.4-11), but not by Eq.(3.4-10). For large N, higher order terms should be included in the approximation.

When the gain A_0 is less than $(Vacq/Vin)^{1/N}$, it is impossible to acquire the value of

Vacq. Before that critical value, Tacq begins to rise, when the gain becomes relatively small. This is explained by Eq.(3.4-10). For N=6, Tacq will be inversely proportional to the gain.

The dependence of T_{acq} on the number of stages N is shown in Fig. 3.4-6. Here, Vreq/Vin=100 is assumed. The curve begins to saturate above N=3. Considering the space and power required in the multi stage comparator, it will be better not to use more than 3 stages. This will be discussed in the summary section of this chapter.

As described in the previous sections, the acquisition time should be required to be less than 10 nS. To realize this with 3 stage preamplifier, a GBW of more than 1200Mrad will be required. Here, the concept of GBW, and not of ω_c and Ao separately, is applicable, due to the result from Fig.3.4-5.

For the design of the comparator, a simple equation explaining all the characteristics mentioned above, should be used. From the previous discussion, the best way will be to use Eq.(3.4-11), with a correction coefficient α.

$$T_{acq} = \frac{\alpha}{GBW}\left(\frac{V_{req} N!}{V_{in}}\right)^{\frac{1}{N}} \qquad (3.4\text{-}12)$$

Here the value of α is approximately 1.1 to 1.4, depending to the number of stages N.

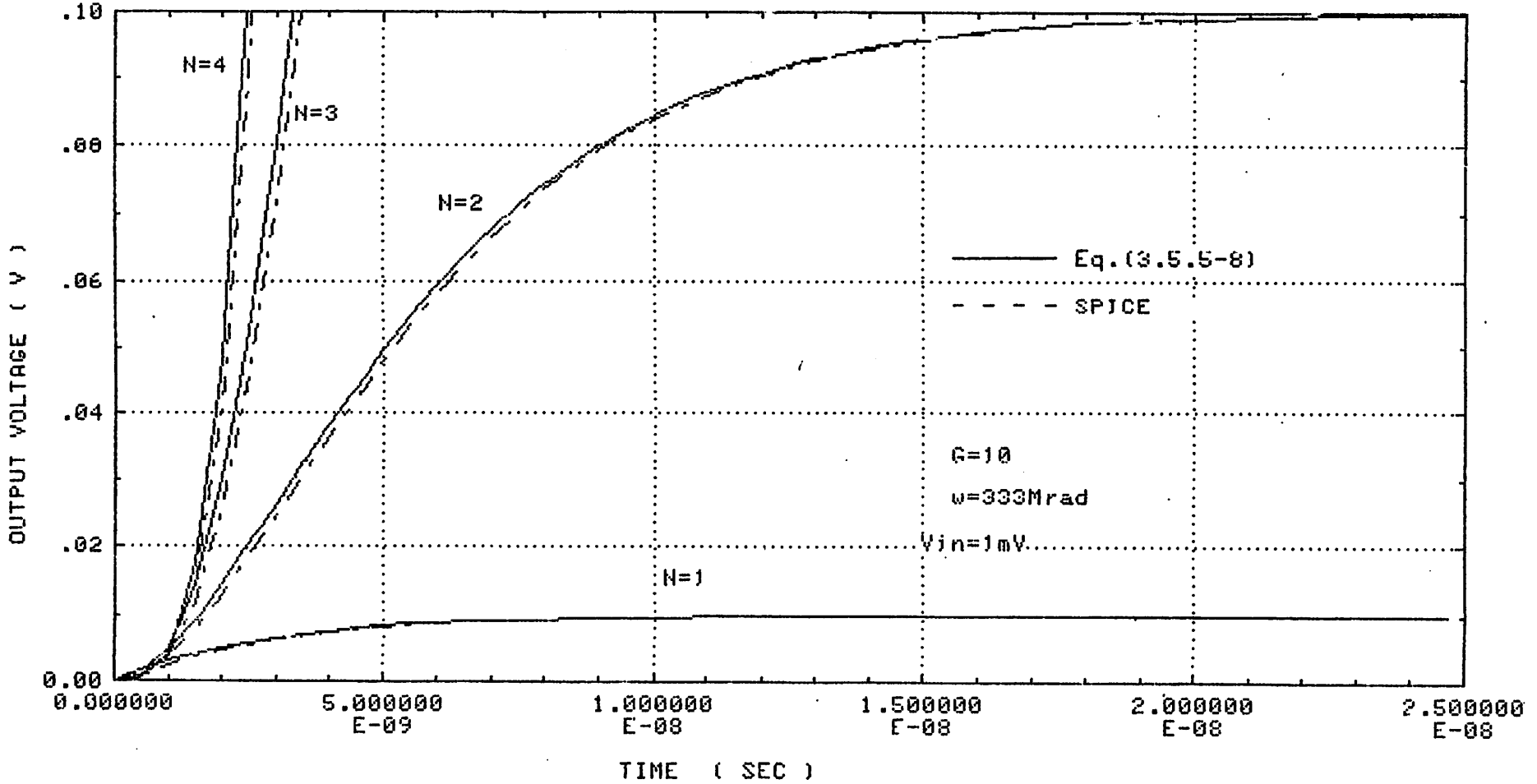


Fig.3.4-1 Transient Response of a Multi-Stage Amplifier

(Vreq/Vin=100, GBW=3330 Mrad/s)

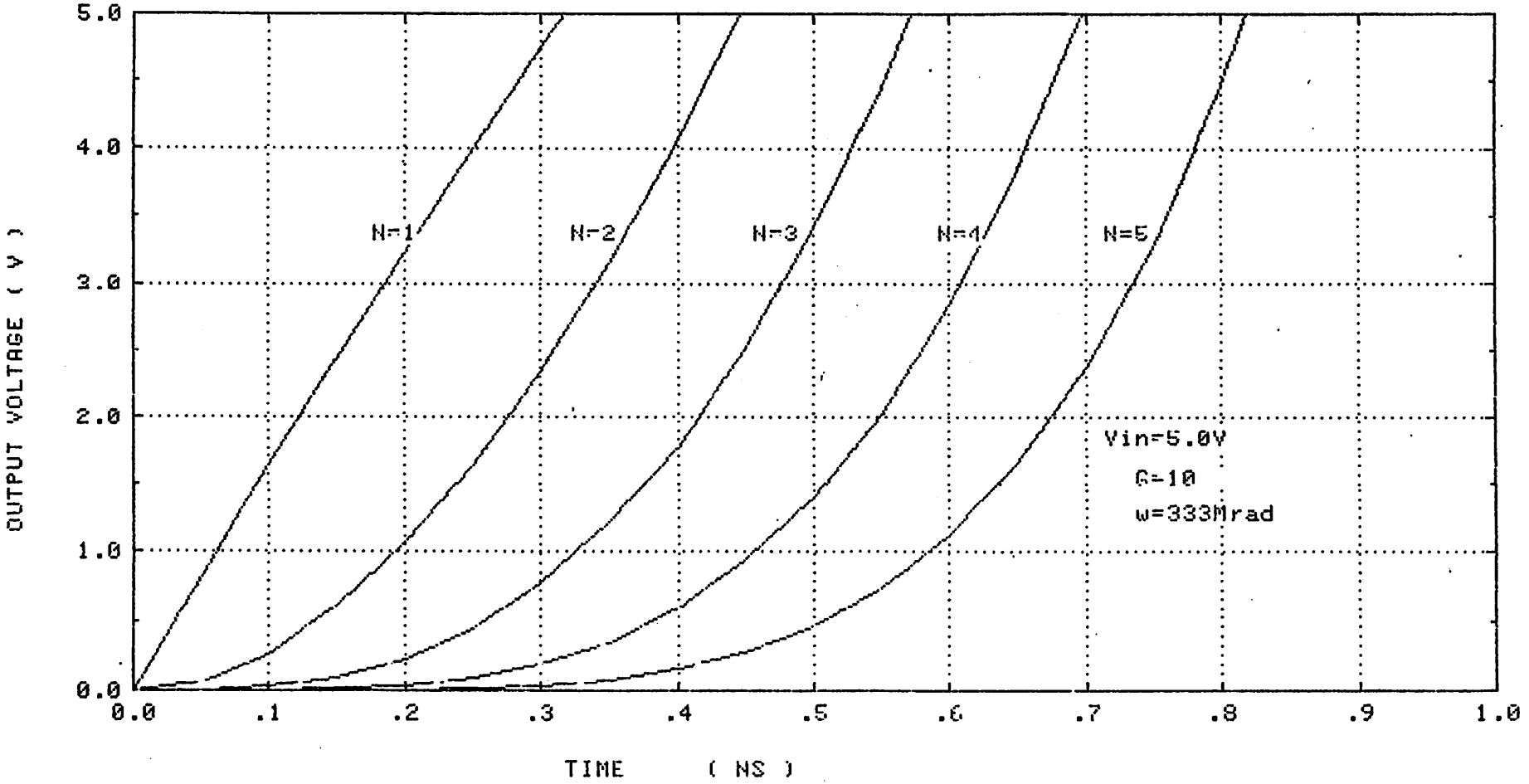


Fig.3.4-2 Transient Response of a Multi Stage Inverter

(Vreq/Vin=1.0, GBW=3330Mrad)

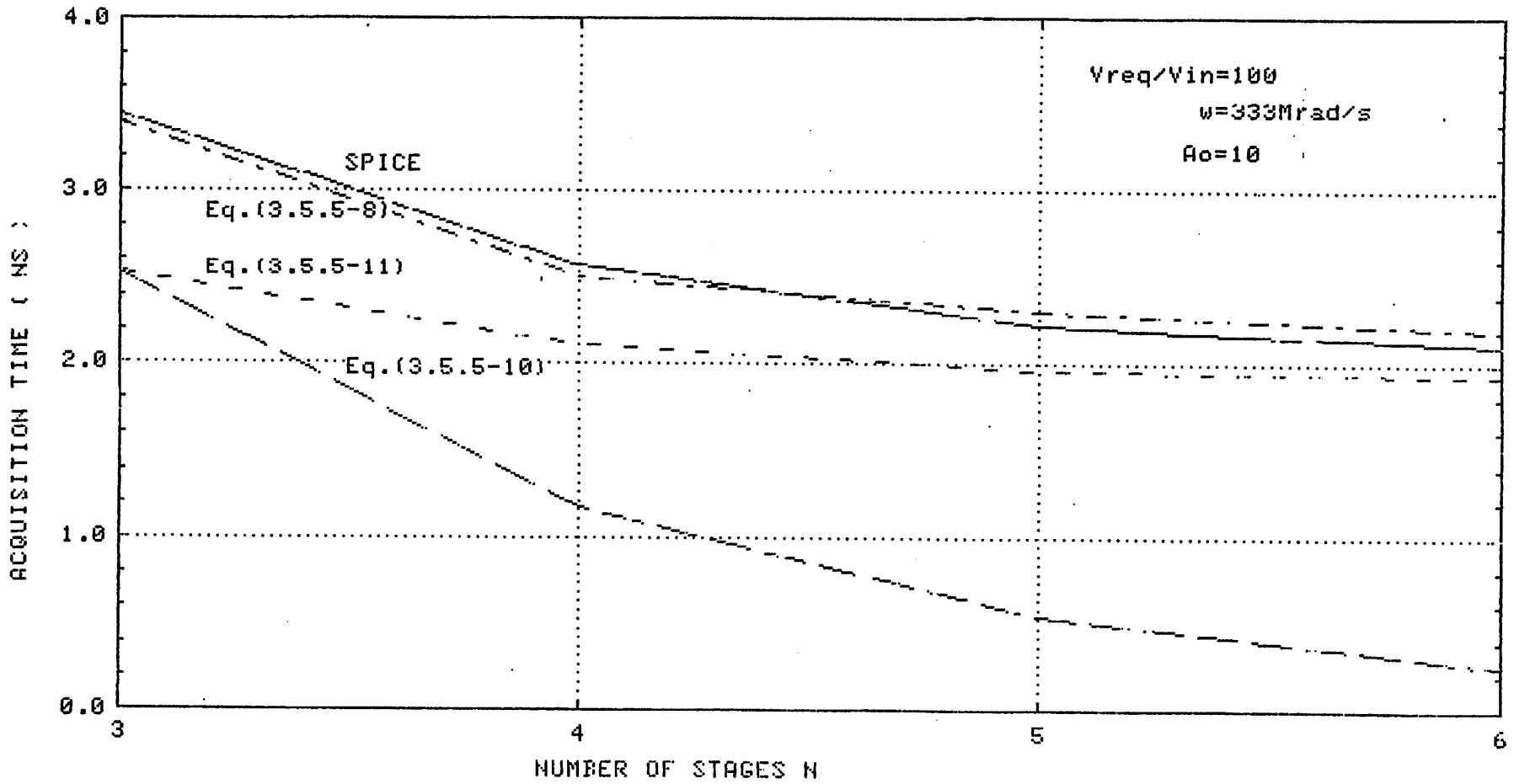


Fig.3.4-3 Acquisition Time versus Number of Stages

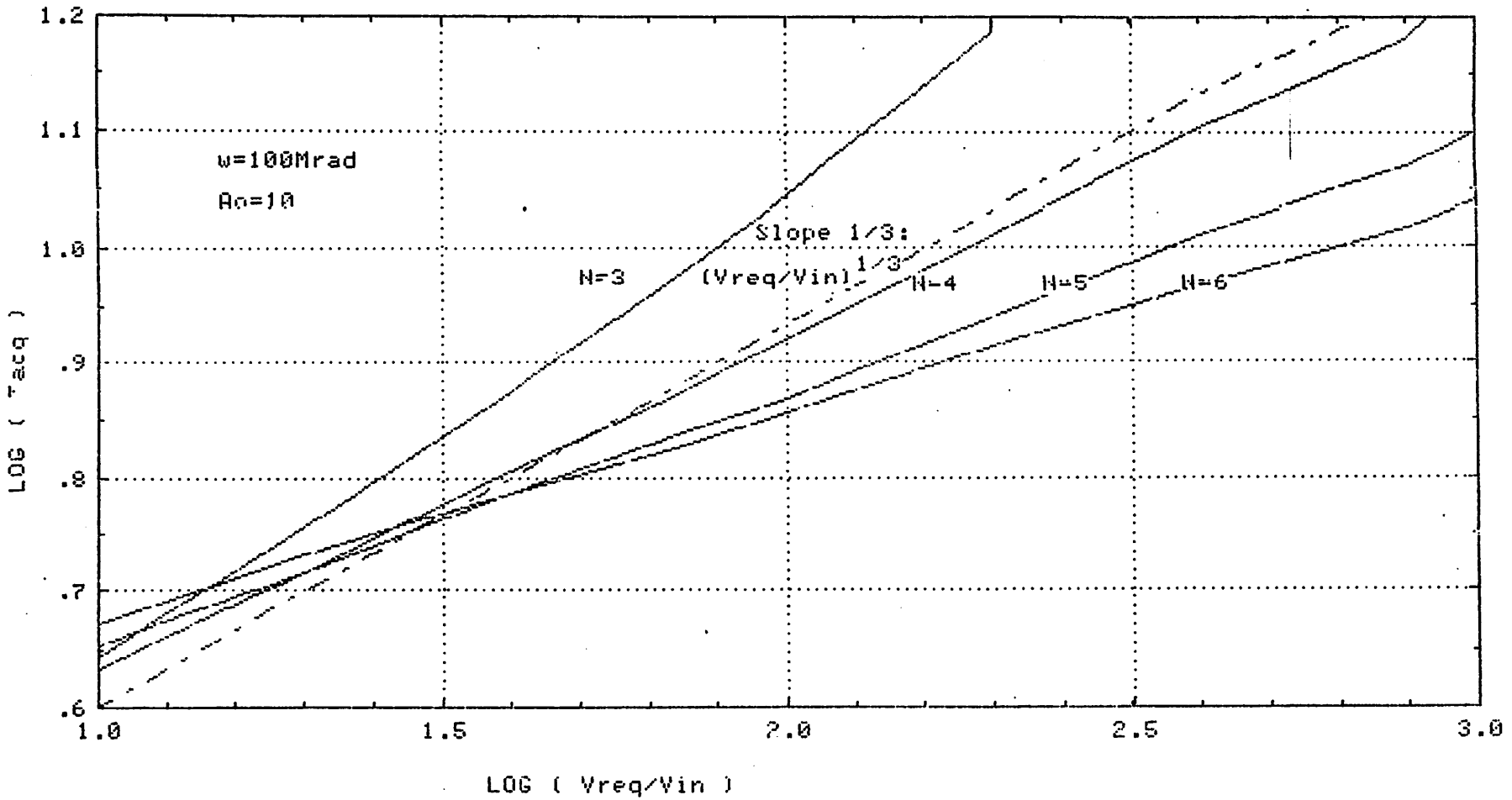


Fig.3.4-4 log-log Plot of Acquisition Time versus Vreq/Vin

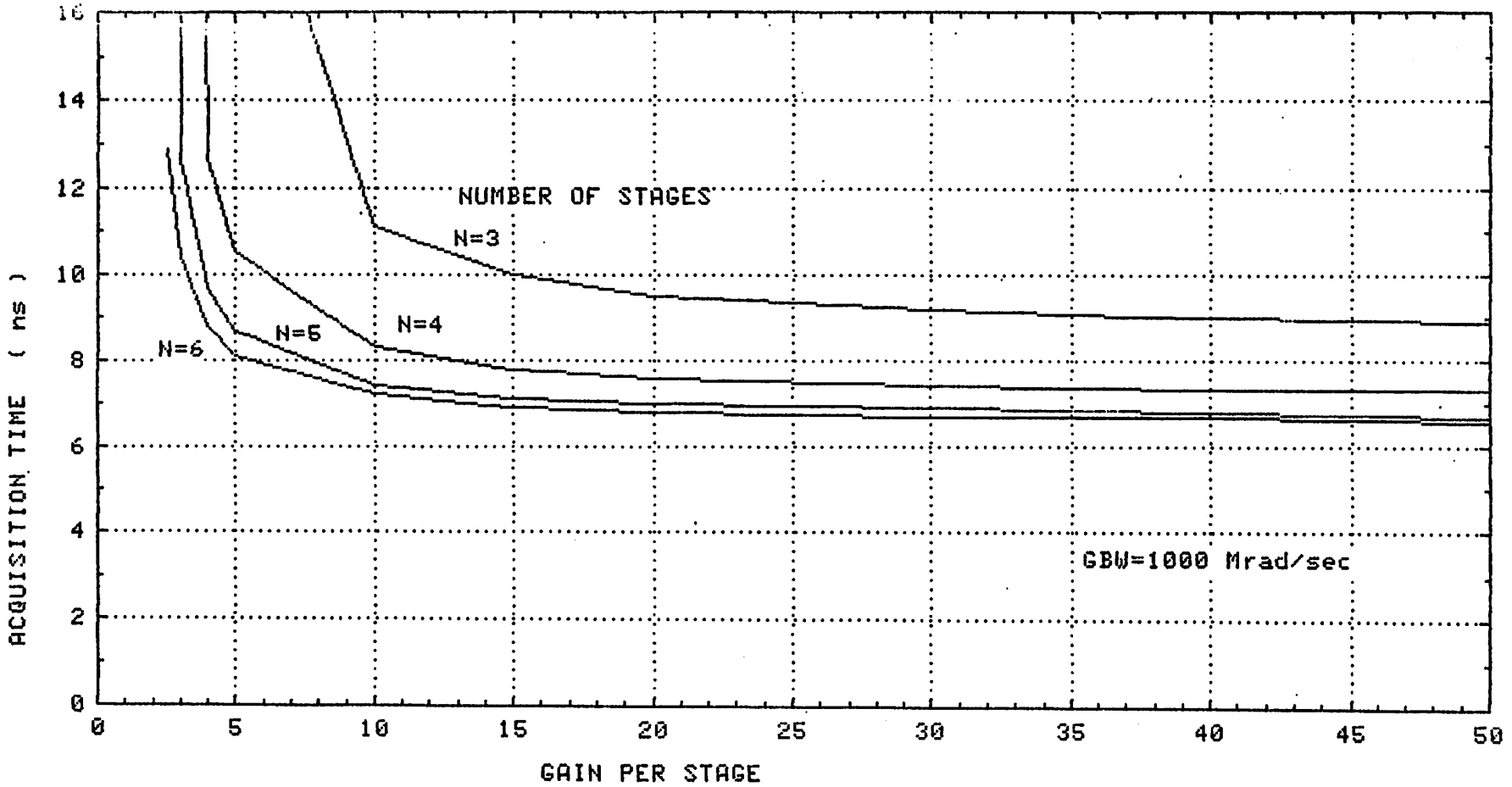


Fig.3.4-5 Acquisition Time versus Gain Ao under a constant GBW

$V_{req} / V_{in} = 100$

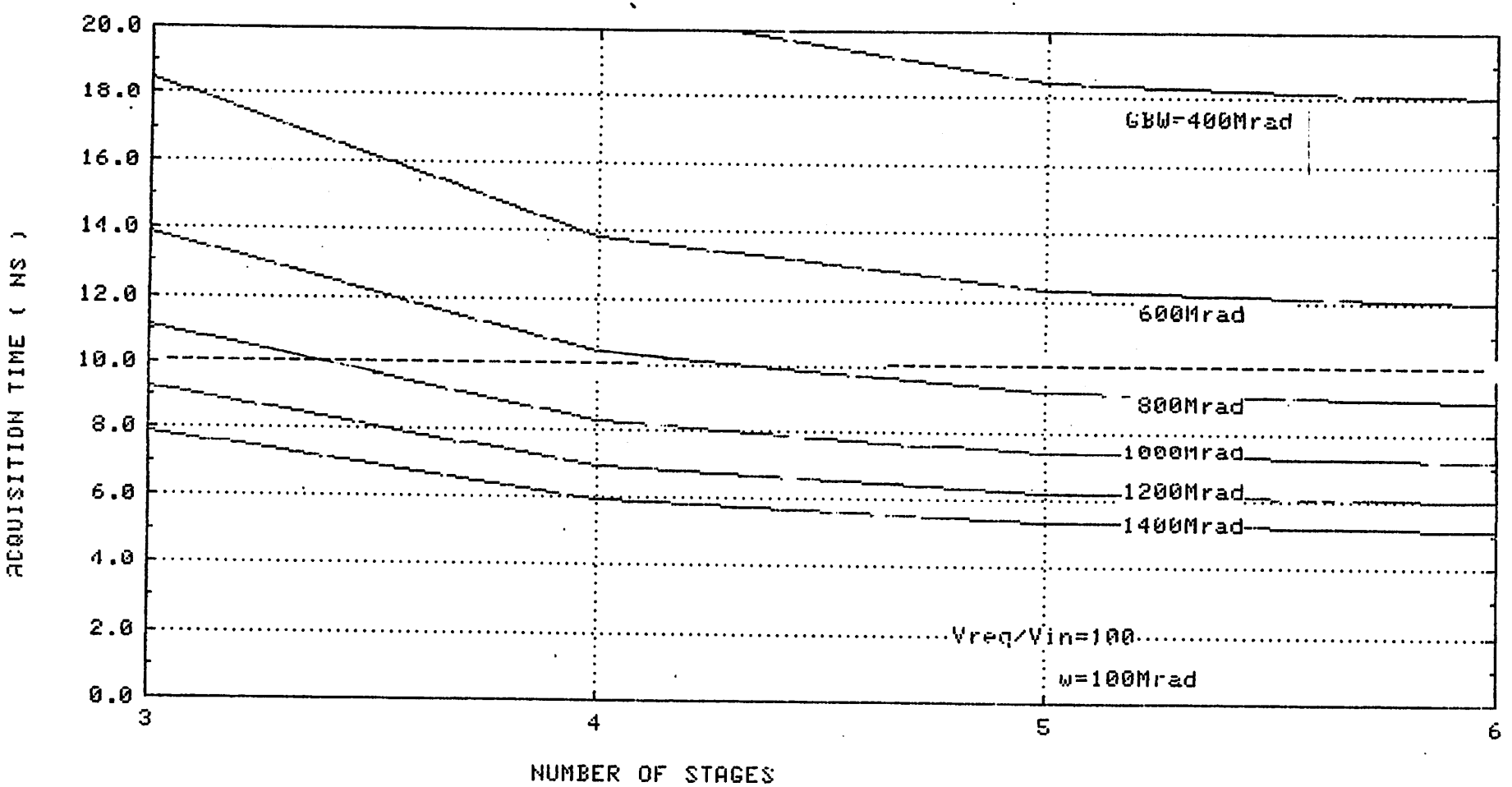


Fig.3.4-6 Acquisition Time versus Number of stages for various GBW.

3.5 Reset Speed and Stabilization

For a high speed comparator, the reset speed is equally important as the evaluation speed. In the actual case the same amount of time or more is spent for the reset.

Fig.3.5-1 (A) shows the basic circuit of the amplifier with a closed loop. L1 and L2 are the loads expressed in a general form. R is the resistance of the switch closing the loop, C_{out} and C_{in} are the output and input capacitances respectively.

From appendix D and F, it is clear that the reset process can be divided in two distinct phases. In the first phase, the reset speed is determined by the RC constant, where R is the resistance of the loop-closing switch and C is the series capacitance of C_{out} and C_{in}. (Fig. 3.5-1 (B)) During this phase, the input and output voltages approach each other.

If the time constant of the amplifier, the inverse of the cut-off frequency, is much smaller than the RC time constant, this time constant of the amplifier will determine the overall decay. This is explained in appendix F.

After V_{in} and V_{out} approach to the same value, the circuit enters to the second phase. (Fig. 3.5-1 (C)) Here, the parallel capacitor $C_{in}+C_{out}$ is charged or discharged through two conductances g_m and G_L. G_L is the conductance of the load and g_m is the conductance of the diode connected driver transistor.

If a current source load is used here, G_L is small, and it will take more time for the comparator to be reset when compared to the diode-connected MOS load. (Sec 3.6) However, a certain gain is required in each amplifier, so that G_L of the diode load cannot be made too large. In both case, g_m will dominate the time constant.

Fig. 3.5.1-(E) shows the modeled transient response during the reset.

Some SPICE simulations are performed to verify this characteristic. The amplifiers used here are; (1) Fully-differential amplifier with diode and current source loads, and (2) Fully-differential- cascode amplifier with diode and current source loads. These circuits

are described in detail in Sec. 3.6.

Fig. 3.5-2 is the results of the transient response simulations for the reset of those fully-differential amplifiers.

In Fig.3.5-2 (1) , a resistance of R=1 $k\ \Omega$ is used, so that the RC time costant can be calculated as 1k*0.1pF/2 = 0.05 ns. The time constant extracted from the simulation is 0.1 ns. The time constant calculated for the second phase is

$$\frac{C_{in}+C_{out}}{g_m} = \frac{0.2pF}{270\mu A/V} = 0.74ns$$

That value extracted from the simulation is 0.65 ns.

Fig. 3.5-2 (2) shows the simulation result for the same circuit and parameters, except the resistance R=10 $k\ \Omega$ The time constant during the first phase is 0.5 ns from calculation and 0.9 ns from simulation.

Here, the transient response shows some oscillation. This is caused by the second pole introduced by the RC circuit in the closed loop. From the criteria for preventing oscillation (Appendix F Eq. (F-12)), the gain-band width of the amplifier A ω_c must satisfy the following relation:

$$A\,\omega_c \leqslant \frac{1}{4RC_{in}}$$

Here, the gain-band width is 2200 Mrad/sec and $\frac{1}{4RC_{in}}$ is 250 Mrad/sec. To avoid any oscillation, R must be less than 1.14 $k\ \Omega$ However, the size for this switch is about W/L = $25\mu m/2\mu m$. This value is so large that a large amount of the feed-through charge will be induced into the amplifier, causing saturation. Even with a fully-differential configuration, this problem is fatal.

Fig. 3.5-2 (3) is the transient response of the reset for R= 5 $k\ \Omega$ It takes about 10 ns to settle to its final value, but the transistor size of W/L= 13 $\mu m/2\ \mu m$ is acceptable.

Fig. 3.5-3 (1) to (3) are the transient simulations for the cascode amplifier. (Appendix E, Sec 3.6) The basic characteristics are the same to the previous simulations, except

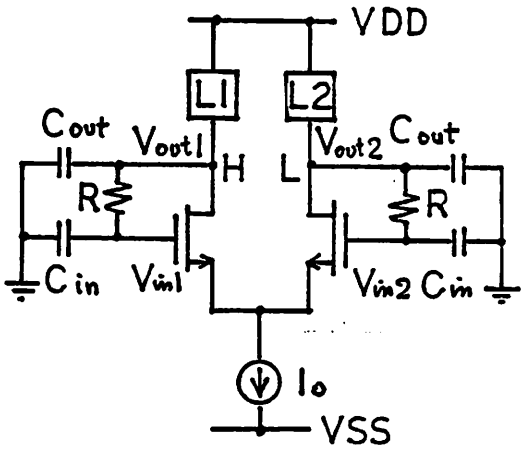
the tendency of oscillation. The reason for that is the existence of the non-dominant pole in the cascode amplifier. In order to achieve a high speed reset, attention must be paid to this pole.

Next, the reset speed of a multi-stage comparator will be discussed. Fig. 3.5-4 shows the basic circuit to be considered. To make the analysis easier, the initial condition of V_{os} =0 V has been assumed. (Fig.3.5-4(A)) This means that all nodes are set to 0 V after reset.

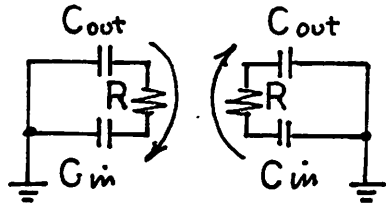
As a worst case, a large input voltage V_0 is supplied, and all of the amplifiers are saturated. The outputs are set either to V_0 or $-V_0$. (Fig.3.5-4(B))

Next, the loop-closing switches are turned on to reset the comparator. (Fig. 3.5-4(C)) All node voltages move towards their initial value of 0 V. To make the calculation easier, a simple periodic structure, or a regular structure has been assumed. (Fig. 3.5-4(D)) Here, the number of stages are infinitely expanded in both sides, and consequently the node voltages can be repeated periodically.

Fig. 3.5-6 shows the solution for this regular structure. The time constant calculated for the first phase is $C_p R/2$, where $C_p/2$ is the series capacitance of the two C_f connected in the input and output of the amplifier. There is no effect of the coupling capacitance C. This result can be understood intuitively, if we notice that there is no change in the charge stored on the coupling capacitances. (Fig. 3.5-4(C) and (D))

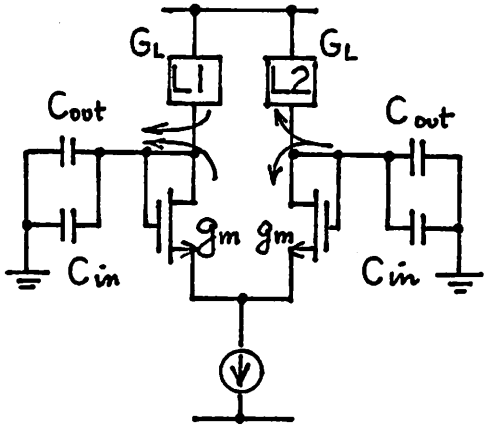


(A) General Closed-Loop Circuit



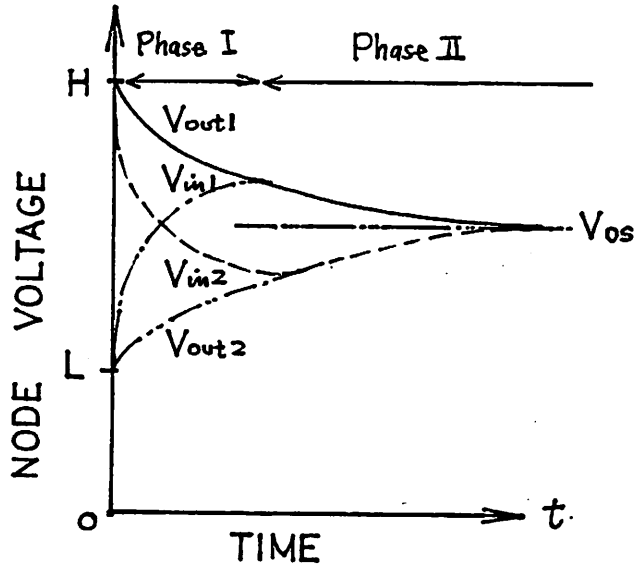
$$\text{Time Constant } \tau = \frac{C_{out}C_{in}}{C_{out}+C_{in}}R$$

(B) Phase I of the Reset



$$\text{Time Constant } \tau = \frac{C_{out}+C_{in}}{G_L+g_m}$$

(C) Phase II of the Reset



(E) Transient Response

Fig.3.5-1 Transient Response of the Reset Operation

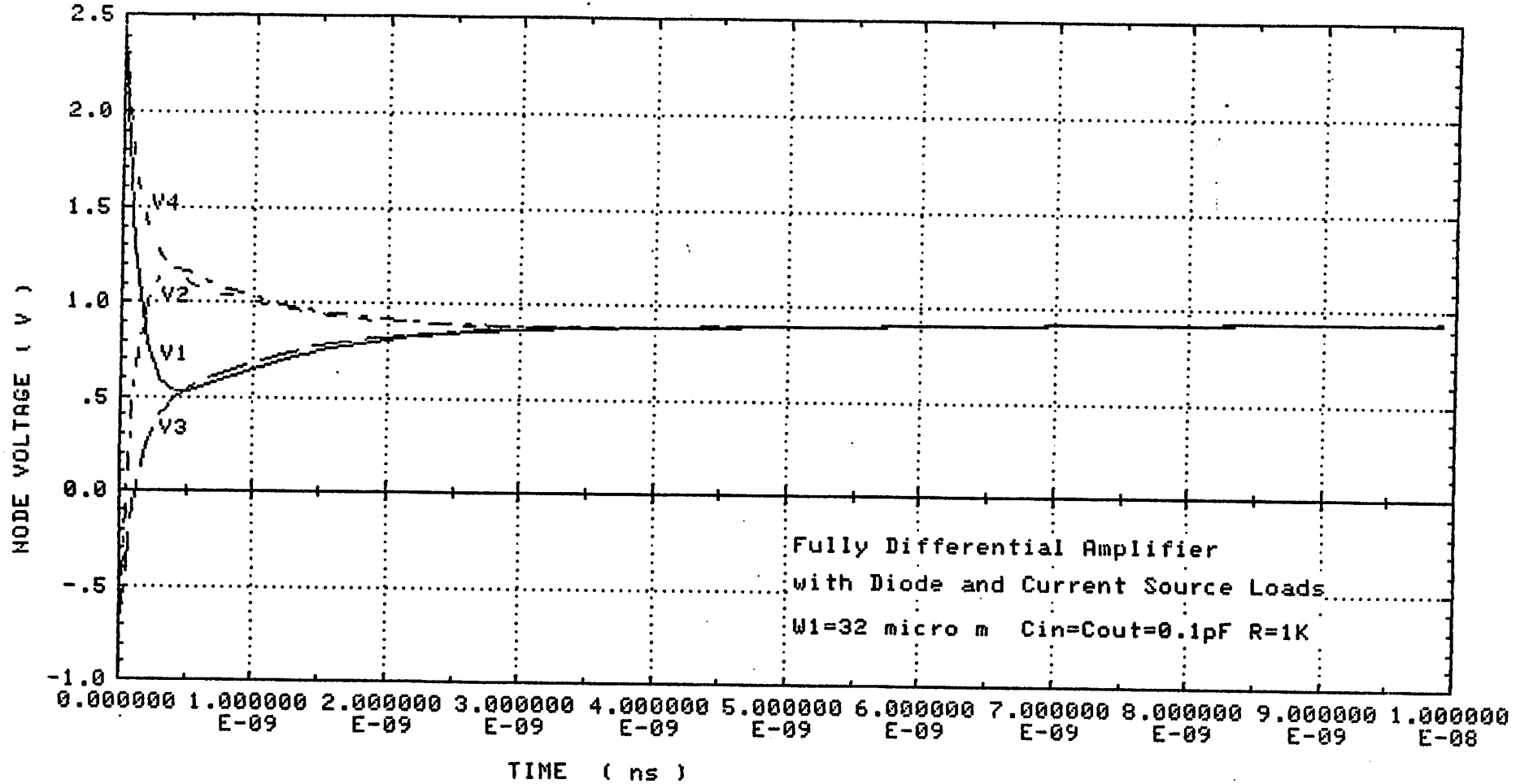


Fig.3.5-2 (1) Transient Response during the Reset of a Fully Differential Amplifier (1)

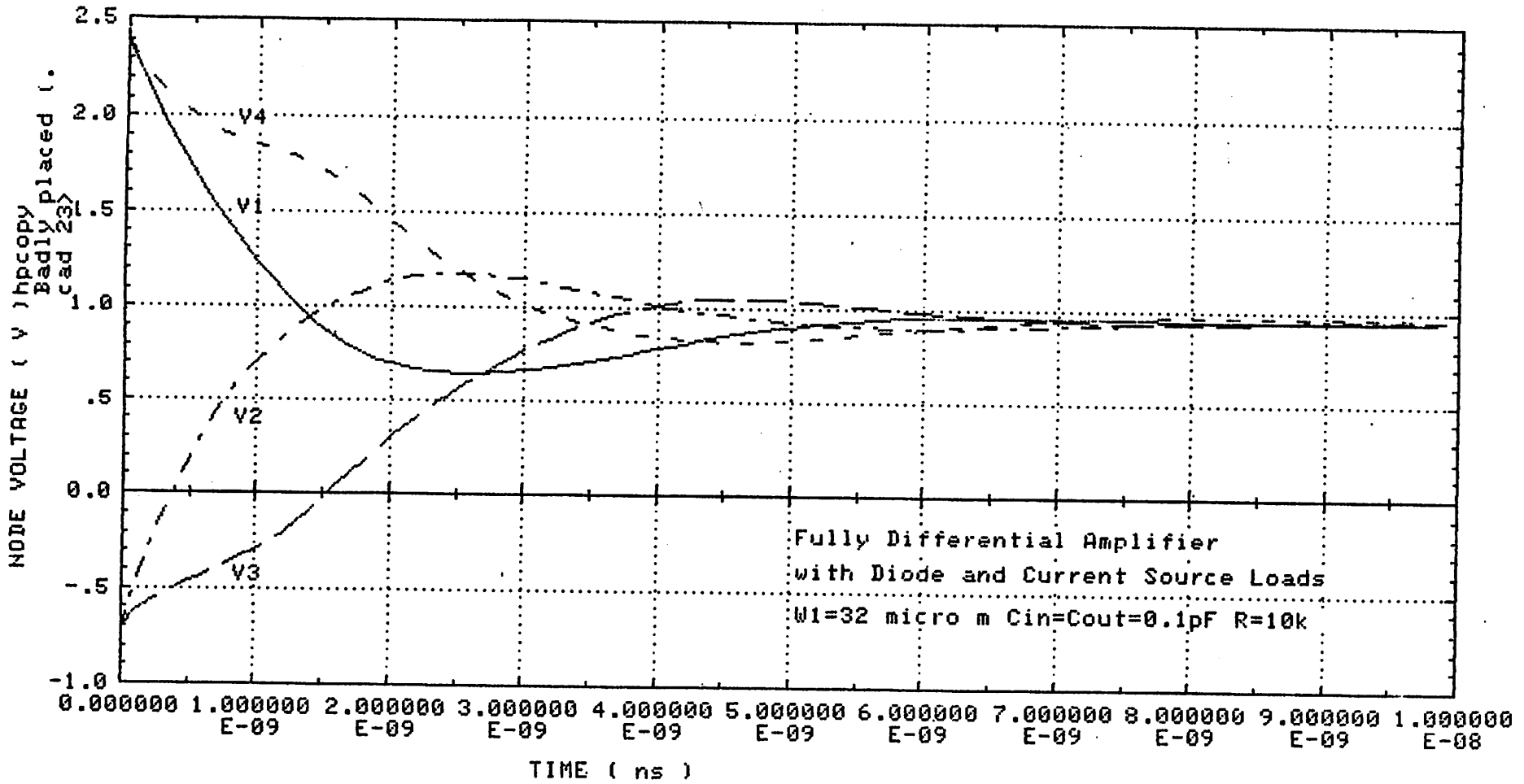


Fig.3.5-2 (2) Transient Response during the Reset of a Fully Differential Amplifier (2)

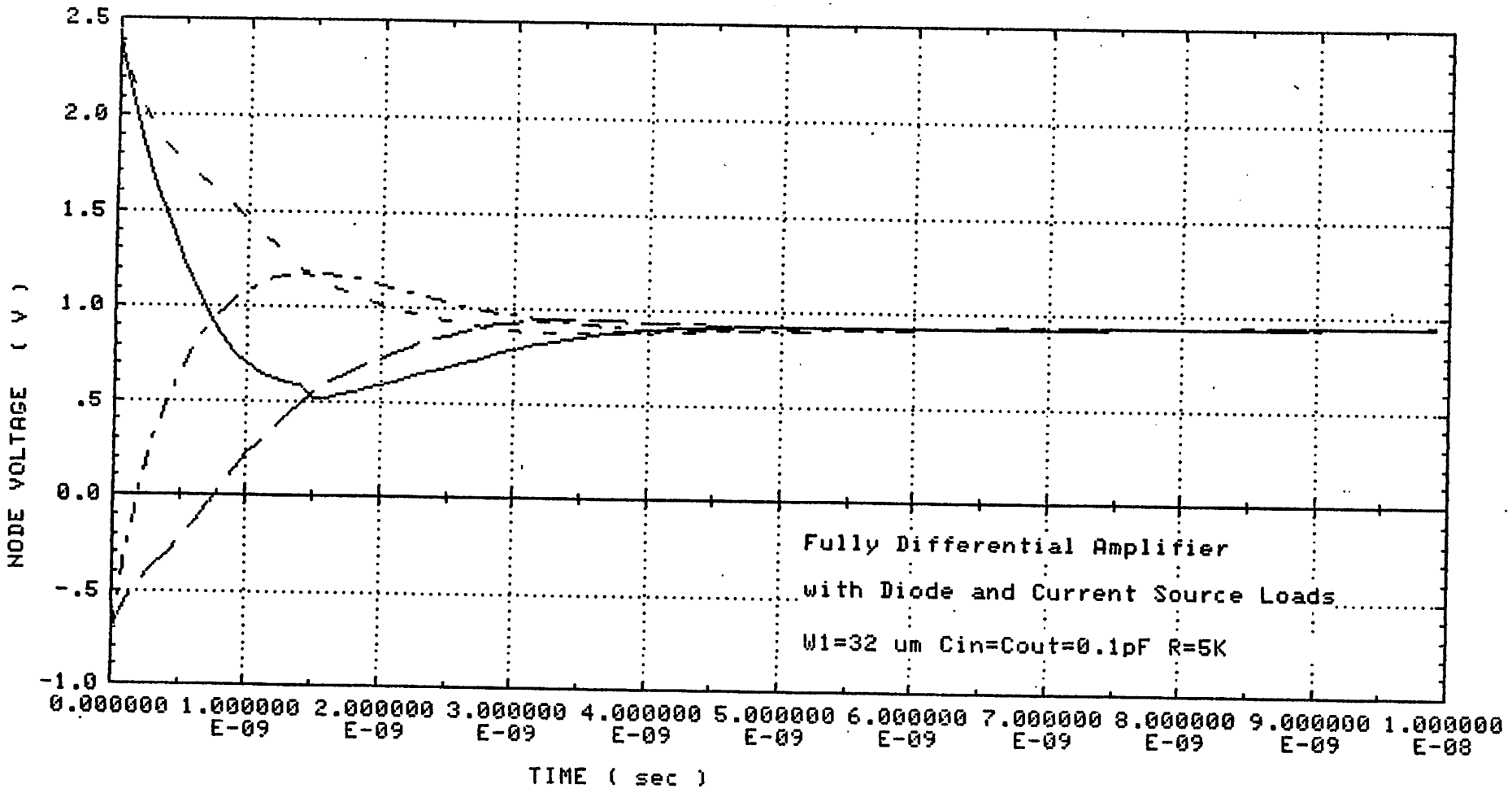


Fig.3.5-2 (3) Transient Response during the Reset of a Fully Differential Amplifier (3)

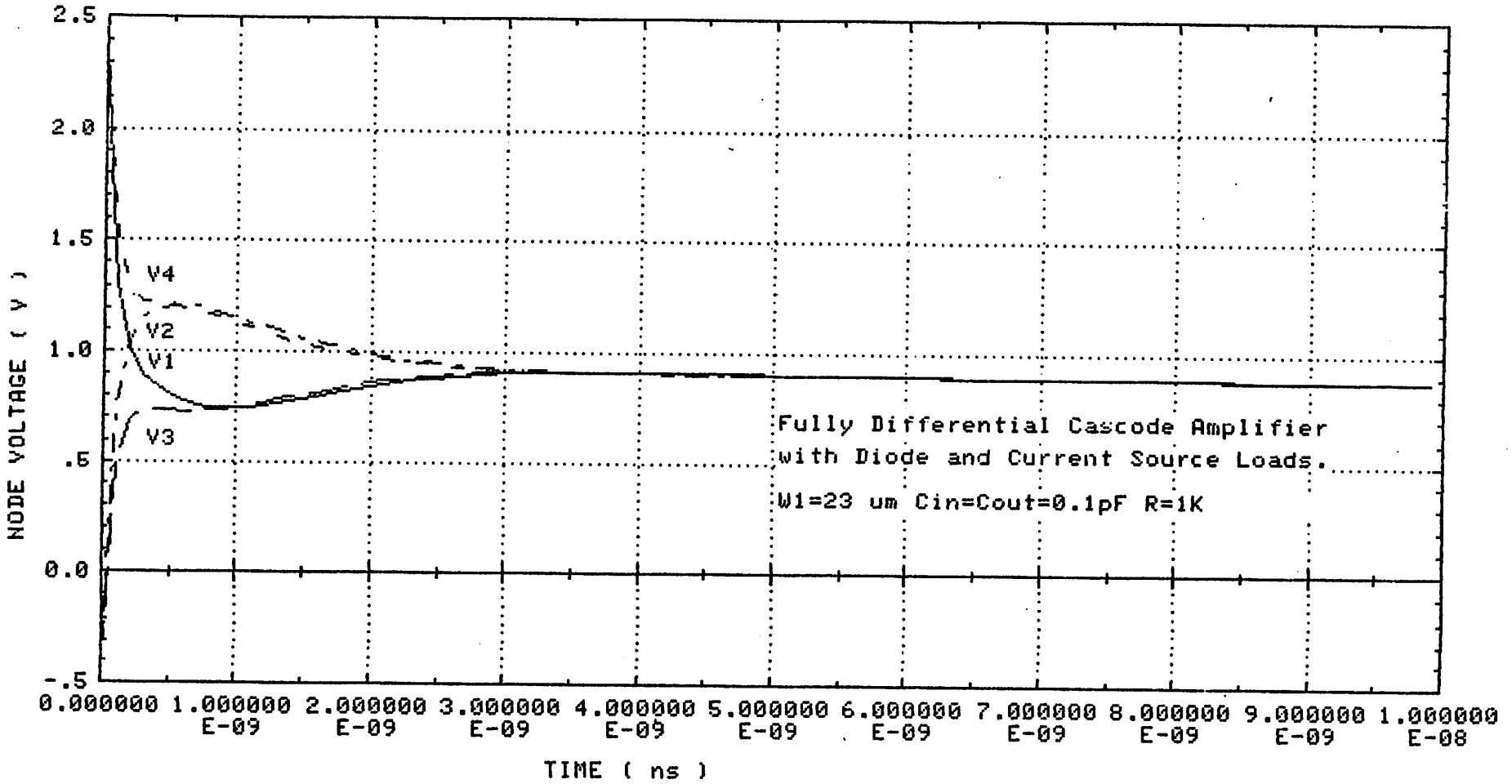


Fig.3.5-3 (1) Transient Response during the Reset of a Fully Differential Cascode Amplifier (1)

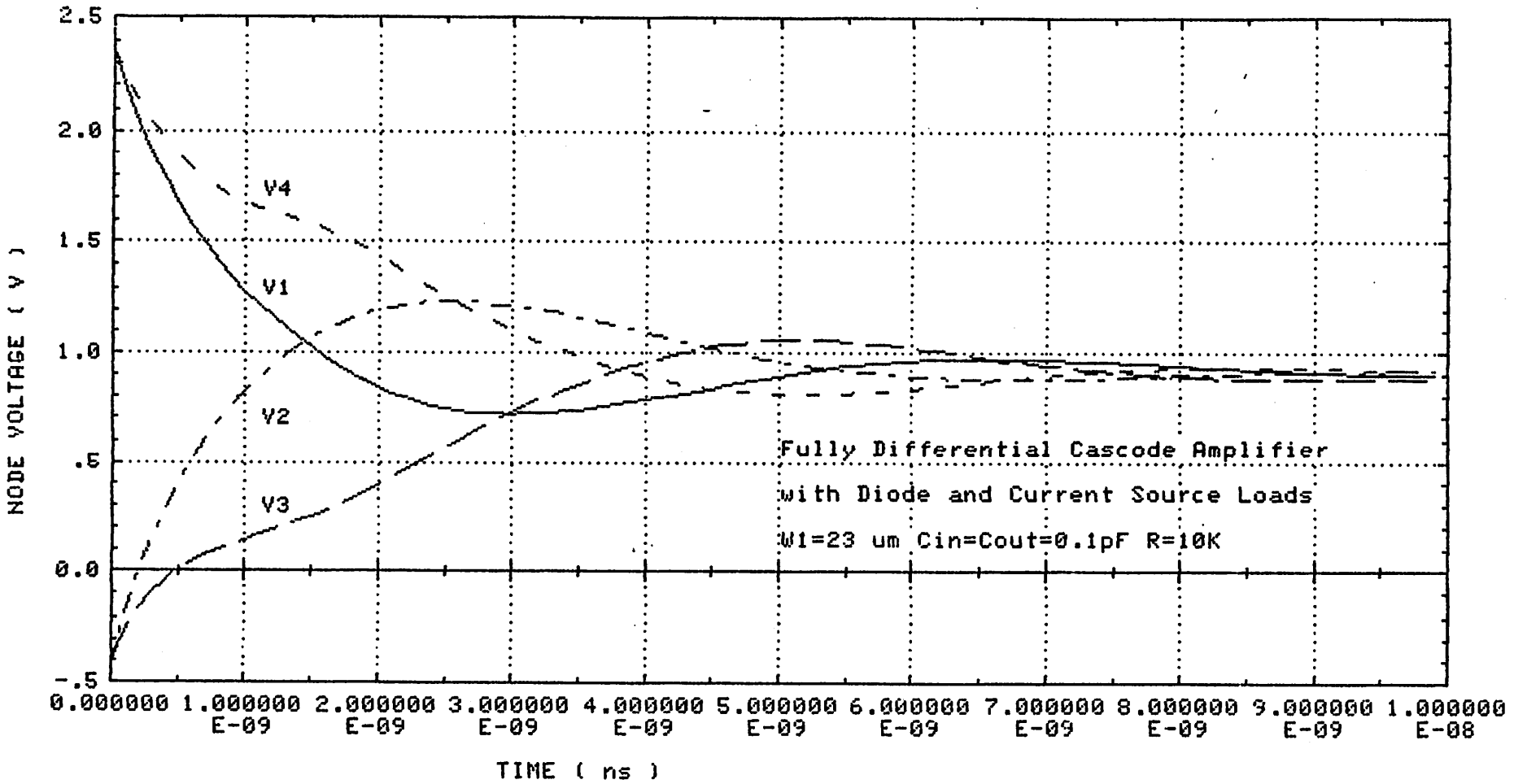


Fig.3.5-3 (2) Transient Response during the Reset of a Fully Differential Cascode Amplifier (2)

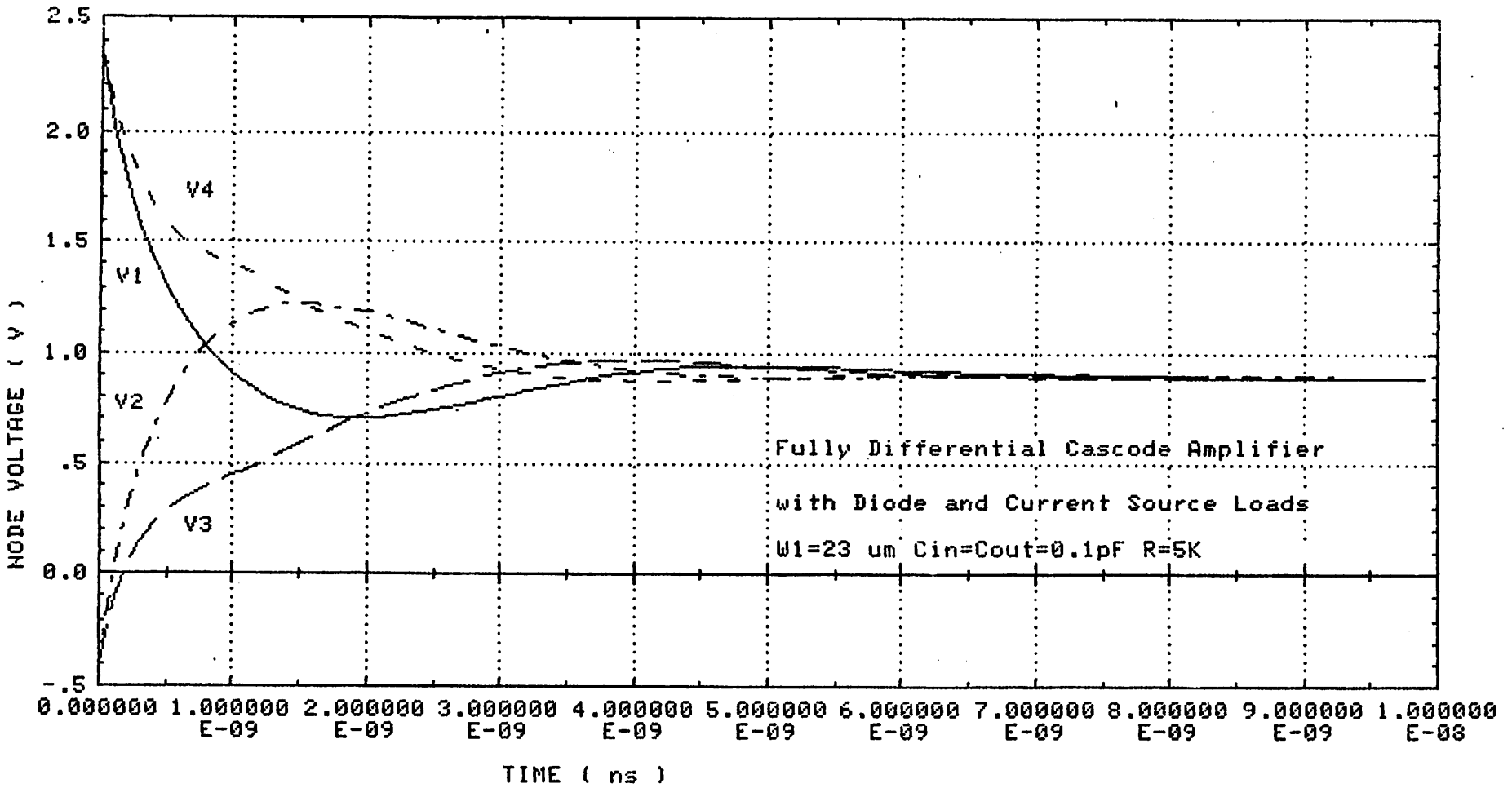
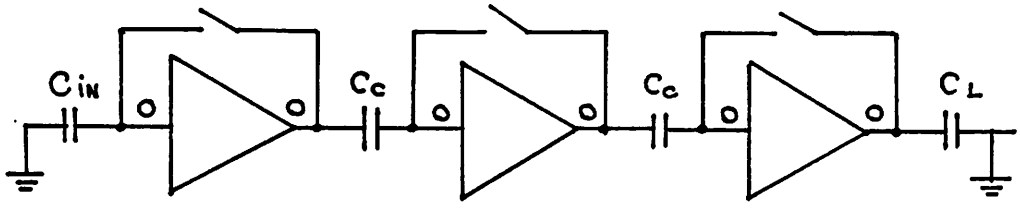
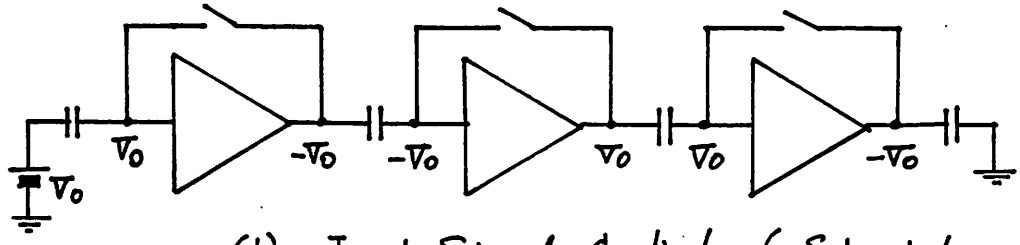


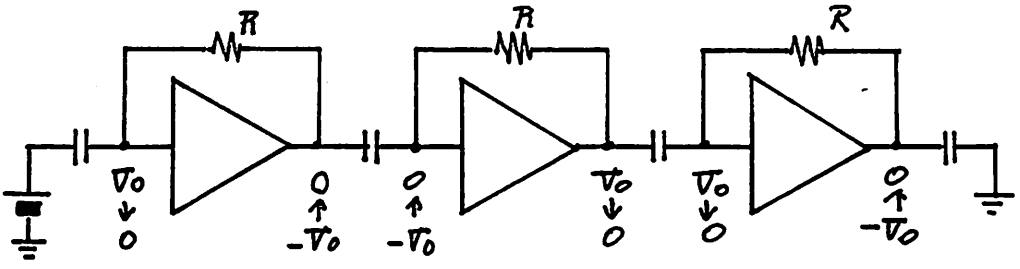
Fig.3.5-3 (3) Transient Response during the Reset
of a Fully Differential Cascode Amplifier (3)



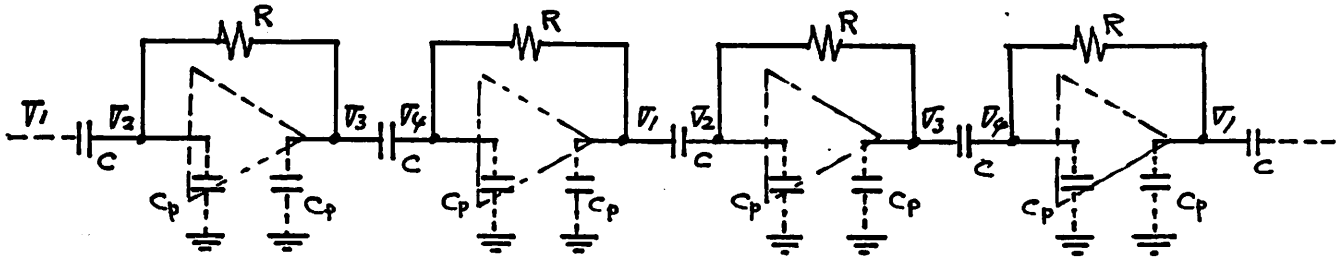
(a) Initial Condition



(b) Input Signal Applied (Saturated as a worst case)

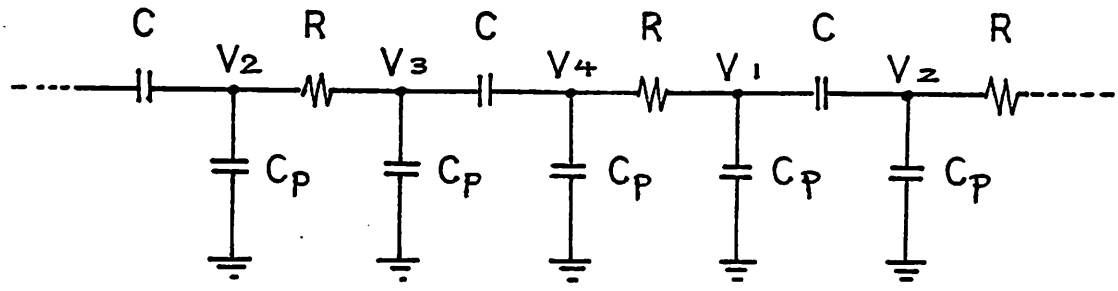


(c) Reset (Phase I ; RC time constant dominant)



(d) Simple Periodic Structure for Analytical Calculation.

Fig.3.5-4 Reset of a Multi-Stage Comparator



Regular Structure

* Initial Conditions

$V_1(0) = V_o$

$V_2(0) = V_o$

$V_3(0) = -V_o$

$V_4(0) = -V_o$

* Equation to be solved

$$\begin{bmatrix} s(C+C_p)R+1 & -sCR & 0 & -1 \\ -sCR & s(C+C_p)R+1 & -1 & 0 \\ 0 & -1 & s(C+C_p)R+1 & -sCR \\ -1 & 0 & -sCR & s(C+C_p)R+1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = C_pRV_o \begin{bmatrix} 1 \\ 1 \\ -1 \\ -1 \end{bmatrix}$$

* Solution

$$V_1(s) = V_o/(s + 2/C_pR)$$

$$v_1(t) = V_o e^{-\frac{t}{C_pR/2}}$$

Fig.3.5-6 Solution for the Regular Structure

3.6 Characteristics of Fully-Differential Amplifiers

3.6-1 Reset Sequence

The optimum amplifier configuration depends on the operation sequence of the comparator. There are basically two kinds of sequence to be considered, based on the number of reset operations used in one A/D conversion cycle.

Fig. 3.6-1 shows those two sequences. (A) is the basic circuit of the fully-differential amplifier to be considered here. Here, G_L , G_m and C_L are the conductance of the load, the transconductance of the driver and the load capacitance respectively.

Fig. 3.6-1 (B) shows the transient of the output voltage in the double reset operation. Here, the amplifiers are reset after each MSB and LSB evaluation. The time constant of the transient during the evaluation is C_L / G_L. From the calculation in Sec. 3.5, it is clear that the time constant during the reset interval is $C_L / (G_L + G_m) \approx C_L / G_m$. Here, small RC constant for the closed loop (small resistance of the loop-closing switch) has also been assumed.

Let's consider the worst case (the most time consuming case), that is the 1 LSB evaluation in the opposite direction after a saturation of the amplifier during the MSB evaluation.

The residual output voltage V_{RS} after the first reset is:

$$V_{RS} = V_S e^{-\frac{T_R}{C_L / G_m}} \tag{3.6-1}$$

Here, V_S is the output voltage of the amplifier in a saturation, and T_R is the reset time. With this voltage as an initial condition, the final voltage V_W after the LSB evaluation is:

$$V_W = V_{RS} e^{-\frac{T_L}{C_L / G_L}} - AV_{LSB}(1 - e^{\frac{-T_L}{C_L / G_L}}) \tag{3.6-2}$$

Here, T_L , A and V_{LSB} are the LSB evaluation time, the gain of the amplifier and the input signal of 1 LSB respectively.

To acquire the correct answer, this value should be negative. Therefore, the following restriction for the conductance of the load device can be derived.

$$G_L \geqslant \frac{C_L}{T_L} \ln\left(1+\frac{V_{RS}}{AV_{LSB}}\right)$$

As a numerical example:

$V_{LSB} = 1$ mV

A = 10

$C_L = 0.1$ pF

$T_L = 10$ nS

$G_m = 200\ \mu A / V$

$T_M = 10$ ns

$V_S = 1$ V

$T_R = 5$ ns

V_{RS} can be calculated to be 45 μV, and $G_L \geqslant 45\ nA / V$, which is a small value. From this estimation, it is clear that not only the MOS load connected in a diode configuration but also a current source load with low G_L is possible to use in this double reset operation. This means that an amplifier with high gain of G_m / G_L is able to be used. However, the speed of a multi-stage amplifier depends basically on the gain-band width GBW of the amplifier, (Sec 3.4) so that there is no advantage to use a high gain amplifier with current source loads, which require a common-mode feedback to maintain the CMRR and to stabilize the DC output level.

The drawback of this double reset operation is the complexity of the control. As is shown in Sec. 3.3, the loop-closing switches of the amplifiers must be opened in a certain delayed sequence to sample the feed-through charge. In order to satisfy this sequence, a total time of 8 ns will be required for a reset time of 5 ns. This is a large time consuming portion for a high speed ADC.

Another possible reset sequence is the single reset operation. This is shown in Fig. 3.6-1 (C) In this operation, the reset is performed only after the LSB evaluation. Here,

much attention should be paid to the relatively large time constant of C_L / G_L during the LSB evaluation.

Let's assume the worst case, that is the 1 LSB evaluation in the opposite direction after the saturation of the amplifier during the MSB evaluation. The final output voltage after the LSB evaluation period T_L is:

$$V_w = V_S e^{\frac{-T_L}{C_L / G_L}} - AV_{LSB}(1 - e^{-\frac{T_L}{C_L / G_L}}) \qquad (3.6\text{-}3)$$

Again, to acquire the correct answer, this voltage should be negative. The conductance of the load should satisfy the following condition;

$$G_L \geq \frac{C_L}{T_L} \ln(1 + \frac{V_S}{AV_{LSB}}) \qquad (3.6\text{-}4)$$

Using the same numbers as the previous numerical example, we get the result of $G_L \geq 46\mu A / V$. This large value cannot be realized by a current source load. Beside this condition, a certain gain G_m / G_L is required for the amplification of small signals. These conditions are satisfied with the multi-stage configuration, and in some cases, a high speed low gain amplifier at the head of that multi stage amplifier. Also, a MOS diode clamp may be used in the head amplifier to reduce the V_S.

The considerations so far was dealing with a single stage. This concept can also be expanded for the multi-stage amplifier.

In this report, fully-differential amplifiers with MOS loads connected in a diode configuration will be discussed. These amplifiers have a high band-width of G_L / C_L and low gain of G_m / G_L.

The discussions and SPICE simulations in this report are based on the single reset operation. The upcoming report by J. Doernberg [4] will discuss also the double reset operation.

3.6-2 Characteristics of Fully-Differential Amplifiers.

Fig. 3.6-2 shows various differential amplifiers examined here. Every circuit has a diode connected MOS loads, except (C) which has a current source load and a common-mode feedback (CMFB) circuit. The details of the calculations are explained in appendix D. Here, only the essential characteristics of each amplifier will be reviewed.

Fig.(A) is the simplest circuit using MOS loads M3 and M4 connected in a diode configuration. (diode load) The drawback of this circuit is that the gain is determined only by the square of the dimension ratio of the driver to the load device. For a 3 stage amplifier used in a 10 bit ADC, at least the gain of 10 is required for each stage. To realize this, the W1/W3 ratio of 100 , or the (W1L3)/(W3L1) ratio of 100 will be required. This makes the device size large.

Fig.(B) is the improved circuit proposed by J. Doernberg. Two current sources M5 and M6 are added to the previous circuit. These current sources supply extra current to the driver transistors M1 and M2. The desired gain can be attained by the ratio W1/W3 and the current ratio Id1/Id3. This circuit shows enough GBW of 1570 Mrad/sec and reasonable size of 296 μm^2, which is around half of the previous circuit. A detail design of this amplifier is reported in appendix E.

Fig. (C) is the only circuit examined here that uses current source loads. In order to get a high CMRR ratio, a CMFB circuit is used. Here the CMFB circuit is expressed by a general form, which consists of an adder to extract the common mode voltage from the output and an amplifier. Usually a common-source differential amplifier is used here as a source follower. The gain of this CMFB circuit is close to unity. There are many other way to implement this type of amplifiers, but they are not discussed here.

This circuit shows a high gain of $g_{m1}(r_{o1} // r_{o3})$, but its cut off frequency $1/ C_L(r_{o1} // r_{o2})$ is relatively low. It is difficult to use this circuit in the single reset operation.

Fig.(D) is an improved version of (B). The problem in the previous circuit was the relatively large Miller capacitance. Coupling capacitance C_c is used between each amplifier

stage, and the output voltage from the previous stage is attenuated by the ratio of $C_c / (C_c + C_{in})$, where C_{in} is the input capacitance of the amplifier containing the Miller capacitance. With that Miller capacitance, the input capacitance is almost doubled, resulting in a large attenuation. Moreover, this large capacitance results in a large load capacitance for its previous stage, degrading its GBW. In the circuit of Fig.(D), cascode transistors M3 and M4 are added to suppress the voltage change in the drain of M1 and M2, and consequently to reduce the Miller capacitance. This suppression depends on the dimension ratio of the cascode transistor and the driver transistor. By this configuration, a very high GBW of 2,500 Mrad/sec has been achieved. The optimum design of this circuit will discussed in Sec. 3.6-3.

Here, a non-dominant pole is induced by the parasitic capacitance C_p at the node between the cascode transistor and the driver transistor. This degrades the stabilization during the reset operation. Details are discussed in appendix D.

Fig.(E) shows the folded version of the previous circuit. Using this configuration, the output swing can be increased. However, even with the previous circuit, an output swing of 3.0 V can be achieved for a 5 V power supply, which is sufficient for our application.

Fig.(F) shows another method to solve the problem of large load capacitance due to the Miller effect of the next stage. Source followers M7 and M8 are added, so that the load capacitance can be reduced to a relatively small value of C_p. The drawback of this problem is the large power consumption. To maintain the unity gain of the source follower over the GBW of the differential circuit, the transconductance of M7 and M8 must be the same to that of M1 and M2. This results in doubling the power consumption if the same transistor dimension is used.

This circuit has been used in the simulation of the full comparator. (Sec. 3.7) The power consumption for a comparator with three amplifiers of this type and a latch is 20.2 mW, resulting in a large power consumption of 646.4 mW for the 10 bit ADC.

Fig.(G) shows a class AB amplifier. This circuit is very attractive for its high drivability in the class B operation. The drawback of this circuit is the large input capacitance of around 0.4 pF. In this amplifier, the input signal must drive two complementary transistors, and this doubles the input capacitance.

3.6-3 Optimum Design of the Fully-Differential Amplifier

(1) Amplifier with Diode Loads

Three circuits are chosen from the previous section and studied in detail. The first one is the fully-differential amplifier with diode loads. As shown in Fig. 3.6-3 (A), all the dimension of the transistors and the current flowing the current sources are scaled with respect to the width W1 of the driver transistor. Here, the conditions for the optimum design is the output voltage V_0 in the reset state, the DC gain G and the attenuation rate ξ due to the coupling capacitance between amplifiers. Details of this calculation are described in appendix E. As the final result, the gain bandwidth GBW can be expressed with respect to W1 as:

$$GBW = \frac{\alpha_g W1}{\alpha_c W1 + C_M} \tag{3.6-5}$$

Here, α_g and α_c are the coefficients that show the linear dependence of the transconductance and load capacitance on W1 respectively.

The gain bandwidth increases asymptotically to a maximum value of $GBW_{max} = \alpha_g / \alpha_c$.

Under the conditions of G=20, ξ = 0.5 and V_0 = 1 V, the maximum value of GBW_{max} = 267 Mrad/sec can be achieved. This is a relatively small value. To attain 90% of this value, a channel width W1 of more than 21 μm is required.

(2) Amplifier with Diode and Current Source Loads

The circuit is shown in Fig. 3.6-3 (B). Under the same condition described before, the GBW can be expressed in the same form as in the Eq. (3.6-5). The dependence of the GBW on W1 has been calculated and simulated. This result is shown in Fig. 3.6-4. Here, the GBW increases asymtotically to its maximum value in both cases. However, the maximum value differs each other. the maximum value from the analytical calculation is 1660 Mrad/sec, while that value from simulation is 2500 Mrad/sec. In the analytical calculation, a channel width of more than 16 μm is required to achieve a 90% GBW of the maximum GBW.

Here, some characteristics for an amplifier of W1 = 32 μm has been simulated. Fig. 3.6-5 shows the DC transfer curve. The output swing is around 3.0 V which is a value large enough for our application. The cross point of the two outputs, which is the point set after the reset, is 1.0 V which is just the expected value for the calculation.

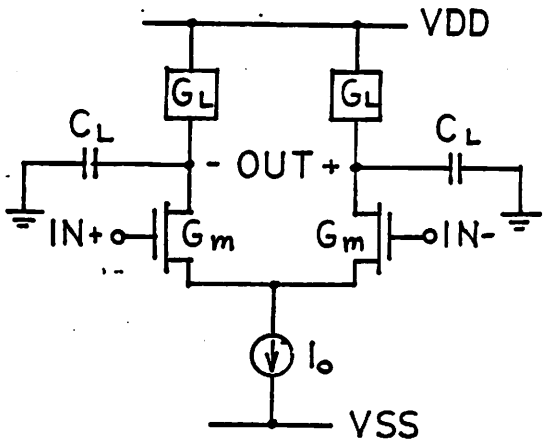
Fig. 3.6-6 is the transient response for the input voltage of 10 mV. Due to the Miller effect in the input capacitance, the input signal is attenuated to about 70% of its value. (V1) The response for this short time period is almost linear with the slew-rate of 9 mV/sec, which is well predicted by Eq.(3.4-2). If the cut off frequency and time product $\omega_c t$ is much smaller than unity, the equation above can be approximated as:

$$V_{out}(t) = GBW\ V_{in}\ t$$

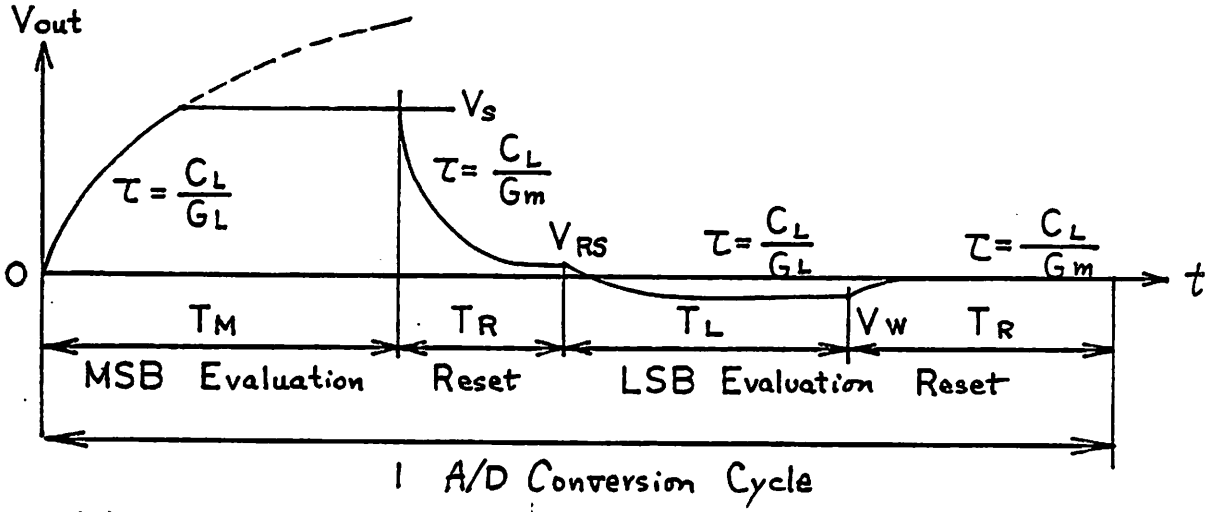
From this equation the slew-rate can be approximated as 1600 Mrad/sec x 7 mV $\approx$ 11 mV/sec.

(3) Cascode Amplifier with Diode and Current Source Loads

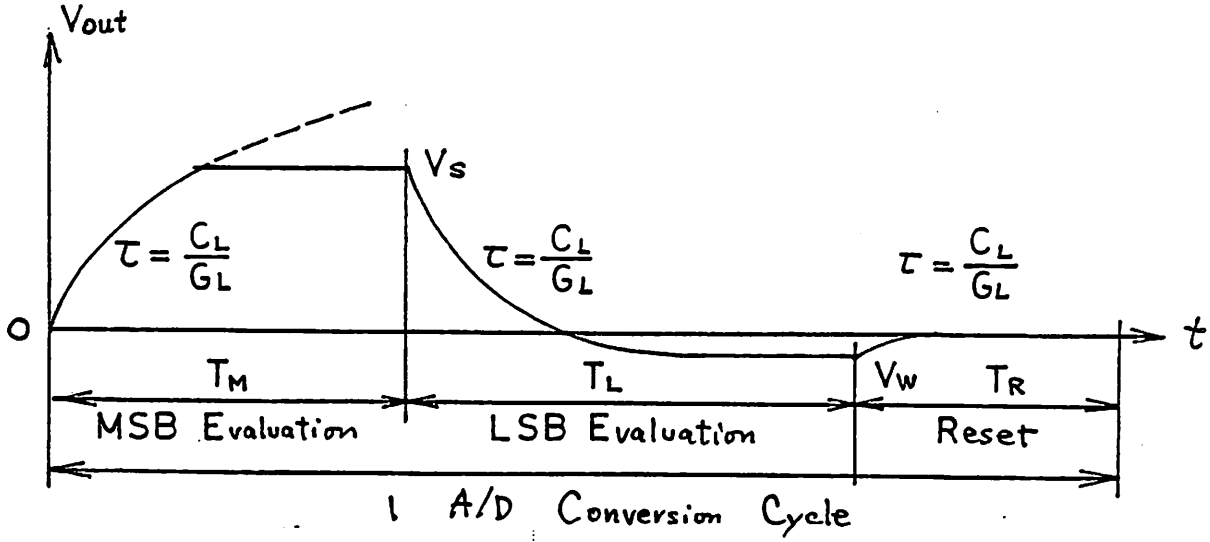
This circuit is shown in Fig. 3.6-3 (C). Under the same condition described before, the GBW can be expressed in the same form as in the Eq. (3.6-5). The dependence of the GBW on W1 has been calculated and simulated. This result is shown in Fig. 3.6-7. Here, the GBW increases asymtotically to its maximum value for the analytical calculation. However, GBW has a maximum peak for the SPICE simulation. The maximum value from



(A) General Circuit Configuration of a Differential Amplifier

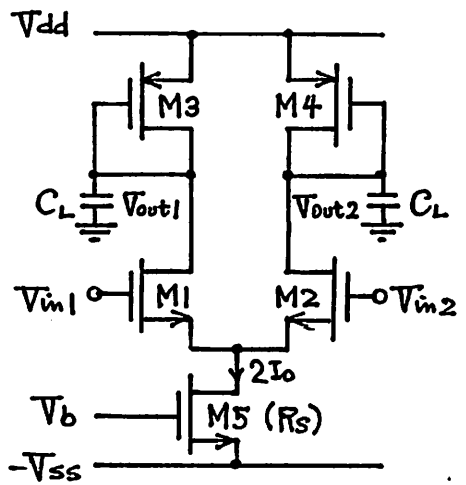
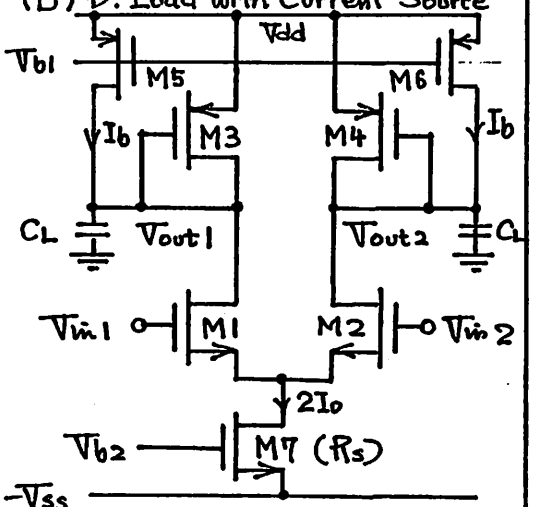
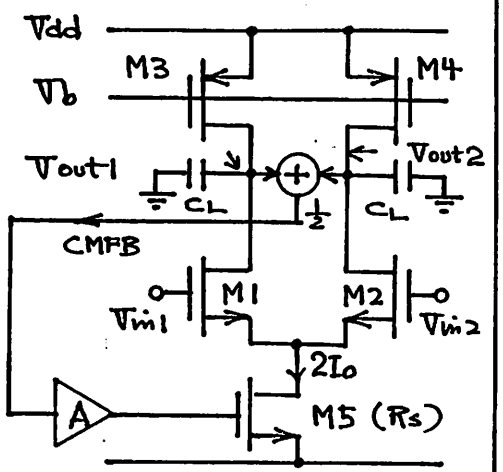


(B) Double Reset Operation



(C) Single Reset Operation

Fig.3.6-1 Reset Operation

Basic Circuit Configuration	(A) Diode Load	(B) D. Load with Current Source	(C) Current Source Loads & CMFB
			
diff. mode gain Ad	$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\beta_1}{\beta_3}}$	$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\beta_1 I_{d1}}{\beta_3 I_{d3}}}$	$g_{m1}(r_{o1} // r_{o3})$
cut off frequency ω_c	$\frac{g_{m3}}{C_L}$	$\frac{g_{m3}}{C_L}$	$\frac{1}{C_L(r_{o1} // r_{o3})}$
gain band width GBW	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$
common mode gain Ac	$\frac{g_{m1}}{g_{m3}} \frac{1}{2R_s g_{m1}+1}$	$\frac{g_{m1}}{g_{m3}} \frac{1}{2R_s g_{m1}+1}$	$\frac{1}{A g_{m5} \cdot R_s}$
gains for AC power supply: Add	1 (diode connection)	1 (diode connection)	$1/A g_{m5} \cdot r_{o3}$
gains for AC power supply: Ass	$1/2R_s g_{m3}$	$1/2R_s g_{m3}$	$1/A$
Reset Time Const.: non-linear	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/(g_{m1}+g_{m3})$	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/(g_{m1}+g_{m3})$	$R_f(C_{in} // C_{out}) \rightarrow (C_{in}+C_{out})/g_{m1}$
Reset Time Const.: linear	$(1/R_f \cdot C_{in} + g_{m3}/C_L)^{-1}$	$(1/R_f \cdot C_{in} + g_{m3}/C_L)^{-1}$	$(1/R_f \cdot C_{in} + 1/(r_{o1} // r_{o3}) \cdot C_L)^{-1}$
Dynamic Range (Vout)	$V_{dd}-V_{thp}-2\sqrt{I_o/\beta_3} < V_{out} < V_{dd}-V_{thp}$	$V_{dd}-V_{thp}-2\sqrt{(I_o-I_b/2)/\beta_3} < V_{out} < V_{dd}$	$-V_{ss}+V_{thN}+2\sqrt{\frac{I_o}{\beta_5}}+V_{thp}+2\sqrt{\frac{I_b}{\beta_7}} < V_{out} < V_{dd}$
Size [1]	554 μm² (273 Mrad/s)	296 μm² (1570 Mrad/s)	
Power Dissipation [1]	32 μW (〃)	760 μW (〃)	
GBW_{max}.	267 Mrad/s	1661 Mrad/sec ℓ C_{in} = 0.14pF	

[1] Size and Power for an Optimum Design ($GBW \geq 0.9 GBW_{max}$, $G_{effective}=10$, $W_{min}=2\mu m$, V_{out} level considered at $V_{di}=0$)

Fig.3.6-2 Basic Characteristics of Fully Differential Amplifiers (1)

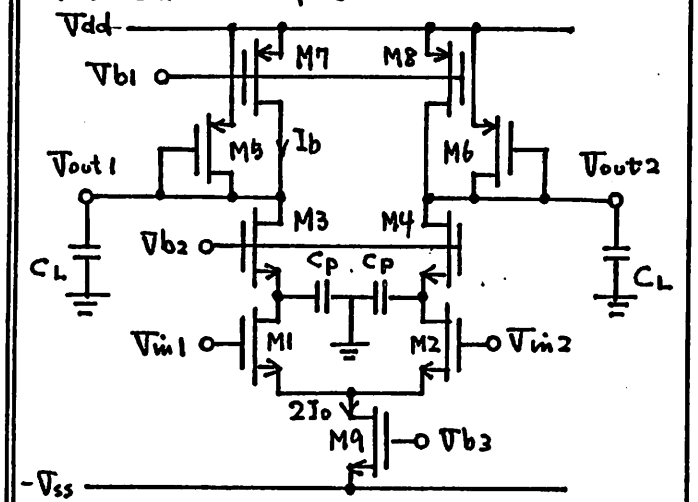
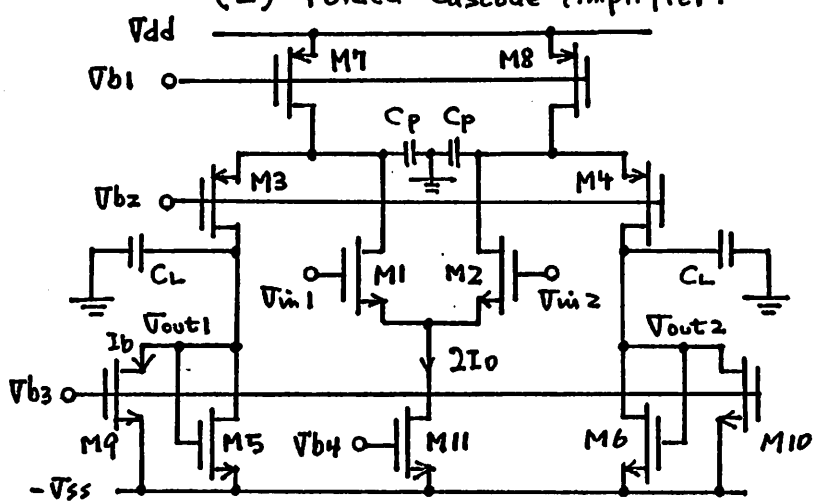
Basic Circuit Configuration	(D) Cascode Amplifier 	(E) Folded Cascode Amplifier. 
Diff. Mode Gain Ad	$\frac{g_{m1}}{g_{m5}} = \sqrt{\frac{\beta_1 \cdot Id1}{\beta_5 \cdot Id5}}$	$\frac{g_{m1}}{g_{m5}} = \sqrt{\frac{\beta_1 \cdot Id1}{\beta_5 \cdot Id5}}$
Cut-off Freq. Wc	$\frac{g_{m5}}{C_L}$ (non dominant pole $\frac{g_{m3}}{C_p}$)	$\frac{g_{m5}}{C_L}$ (non dominant pole $\frac{g_{m3}}{C_p}$)
Gain Band Width	$\frac{g_{m1}}{C_L}$, phase margin $-\frac{\pi}{2} - \tan^{-1}\left(\frac{g_{m1}}{g_{m3}} \cdot \frac{C_p}{C_L}\right)$	$\frac{g_{m1}}{C_L}$, phase margin $-\frac{\pi}{2} - \tan^{-1}\left(\frac{g_{m1}}{g_{m3}} \cdot \frac{C_p}{C_L}\right)$
Comm. Mode Gain Ac	$\frac{g_{m1}}{g_{m5}} \cdot \frac{1}{2R_s g_{m1} + 1}$	$\frac{g_{m1}}{g_{m5}} \cdot \frac{1}{2R_s g_{m1} + 1}$
Gain for AC Power Supply — Add	1 (diode Connection)	$1/R_L \cdot g_{m5}$ ($R_L = r_{o7}$)
Gain for AC Power Supply — Ass	$1/2R_s g_{m5}$	1 (diode connection)
Reset Time Const. — non-linear	$R_f (C_{in} // C_{out}) \rightarrow \tau_f = C_p/g_{m5}$, $\tau_s = 2(C_{in}+C_{out})/g_{m5}$	$R_f (C_{in} // C_{out}) \rightarrow \tau_f = C_p/g_{m5}$, $\tau_s = 2(C_{in}+C_{out})/g_{m5}$
Reset Time Const. — linear	$(1/R_f \cdot C_{in} + g_{m5}/C_L)^{-1}$	$(1/R_f \cdot C_{in} + g_{m5}/C_L)^{-1}$
Dynamic Range (out)	$V_{dd} - V_{thP} - 2\sqrt{\frac{I_o - I_b/2}{\beta_5}} < V_{out} < V_{dd} - V_{thP}$	$-V_{ss} + V_{thN} < V_{out} < -V_{ss} + 2\sqrt{\frac{I_b - I_o}{\beta_6}} + V_{thN}$
Size	218 μm² (2563 Mrad/sec)	
Power Dissipation	550 μW (")	
GBW max	3189 Mrad/sec	
Cin	0.058pF	

Fig.3.6-2 Basic Characteristics of Fully Differential Amplifiers (2)

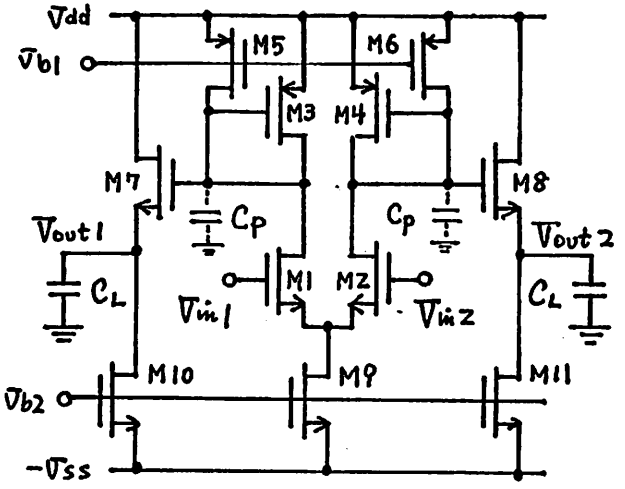
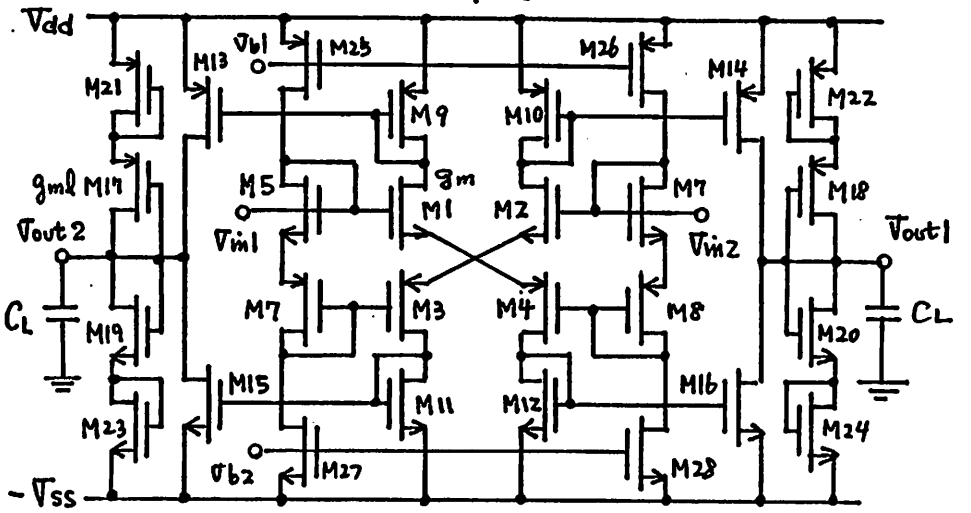
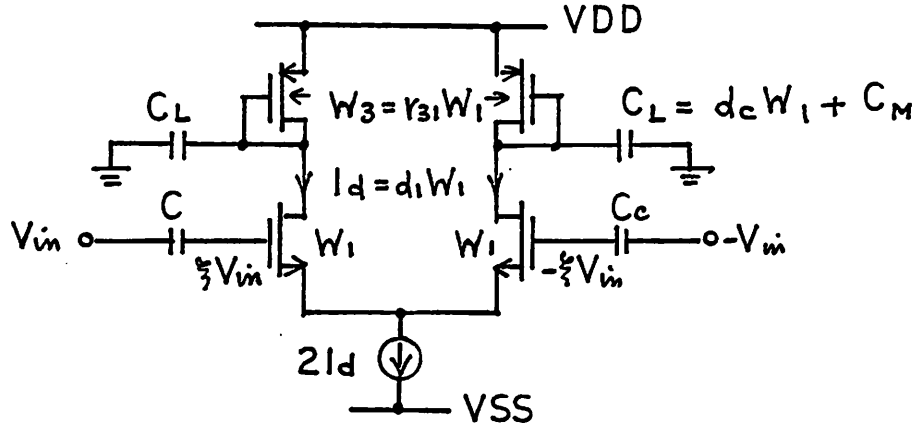
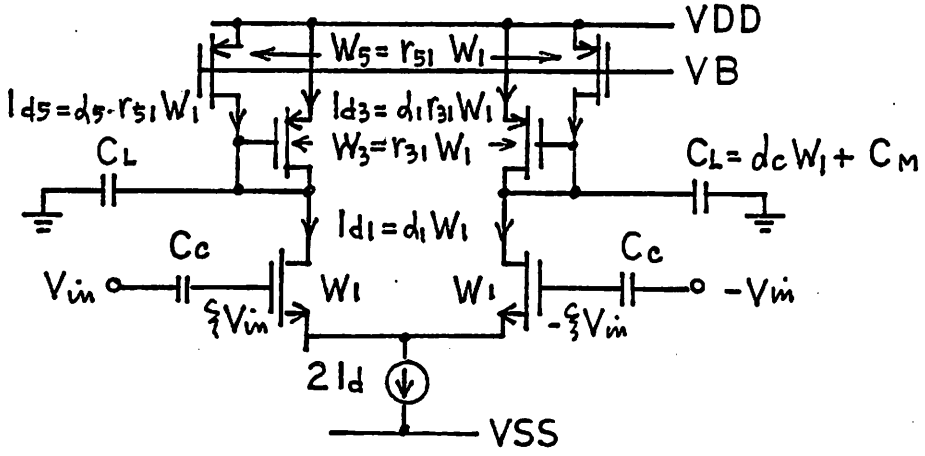
		(F) (B)+Source Follower	(G) Class AB Amplifier
Basic Circuit Configuration			
Diff. Mode Gain Ad		$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\beta_1 I_{d1}}{\beta_3 I_{d3}}}$	$\xi \frac{2g_m}{g_{m1}}$ $\left(\xi = \frac{g_{m13}}{g_{m9}} = \frac{g_{m15}}{g_{m11}} = \frac{g_{m14}}{g_{m10}} = \frac{g_{m16}}{g_{m12}}\right)$
Cutt Off Freq. ω_c		$\frac{g_{m3}}{C_p}$	$\frac{g_{m1}}{C_L}$
Gain Band Width GBW		$\frac{g_{m1}}{C_p}$	$2\xi \frac{g_m}{C_L}$
Common Mode Gain Ac		$\frac{g_{m1}}{g_{m3}} \cdot \frac{1}{2R_s \cdot g_{m1} + 1}$	
Gain for	Add	≒ 1 (diode connection)	≒ 1 (diode connection)
	Ass	g_{m10}/g_{m7}	≒ 1 (diode connection)
Reset Time	non-linear	$R_f (C_{IN} // C_p) \rightarrow (C_{in}+C_p)/(g_{m1}+g_{m3})$	
	linear	$(1/R_f \cdot C_{in} + g_{m3}/C_p)^{-1}$	$(1/R_f \cdot C_{in} + g_{m1}/C_L)^{-1}$
Dynamic Range (out)		V_{out} of Fig.(B) $- V_{thN} - \sqrt{\frac{2I_{d7}}{\beta_7}}$	
Size			768 μm² (GBW = 5013 Mrad/s , G = 45.6)
Power Dissipation			670 μW (")
GBW max.			
Cin			0.3852 pF

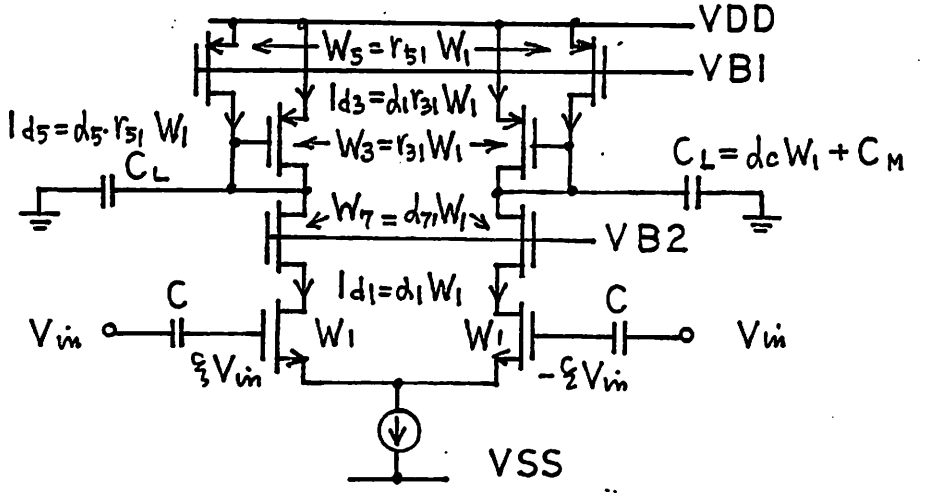
Fig.3.6-2 Basic Characteristics of Fully Differential Amplifiers (3)



(A) Amplifier with MOS loads in Diode Connection



(B) Amplifier with Diode and Current Source Loads



(C) Cascode Amplifier with Diode and Current Source Loads

Fig.3.6-3 Optimum Design of the Differential Amplifiers

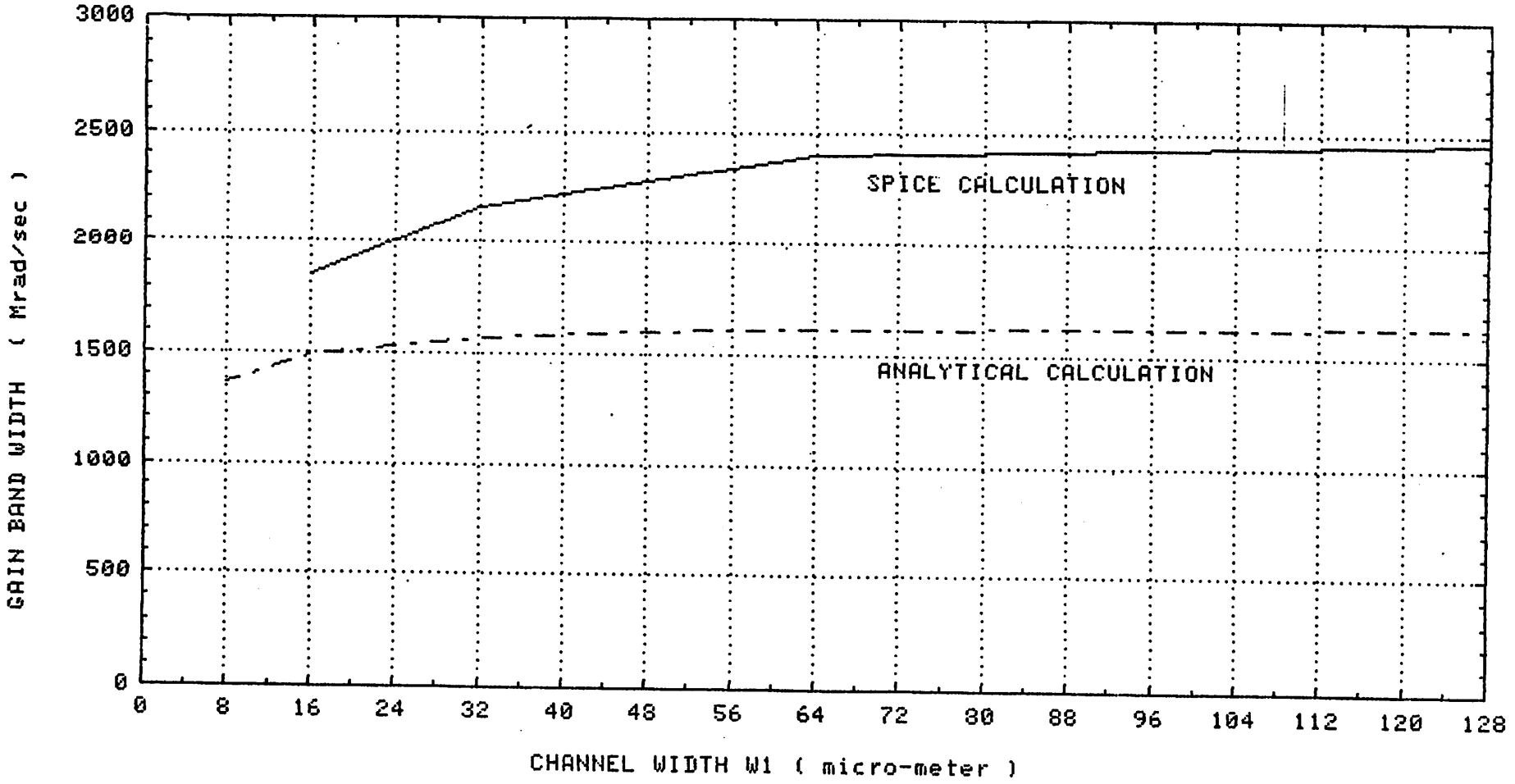


Fig.3.6-4 Gain Bandwidth Dependence on W1

for a Differential Amplifier with Diode and Current Source Loads

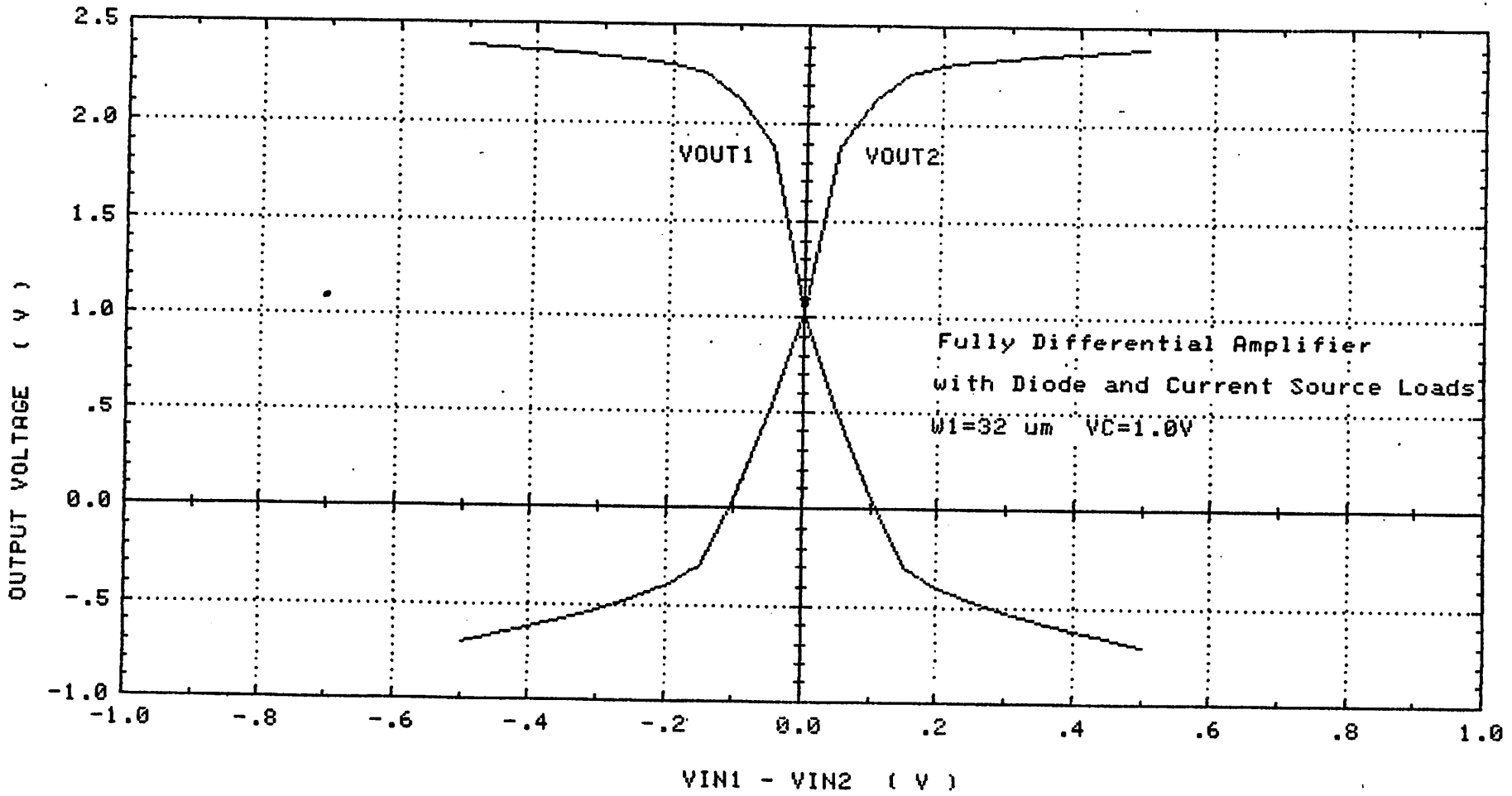


Fig.3.6-5 DC Transfer Characteristics

for a Differential Amplifier with Diode and Current Source Loads

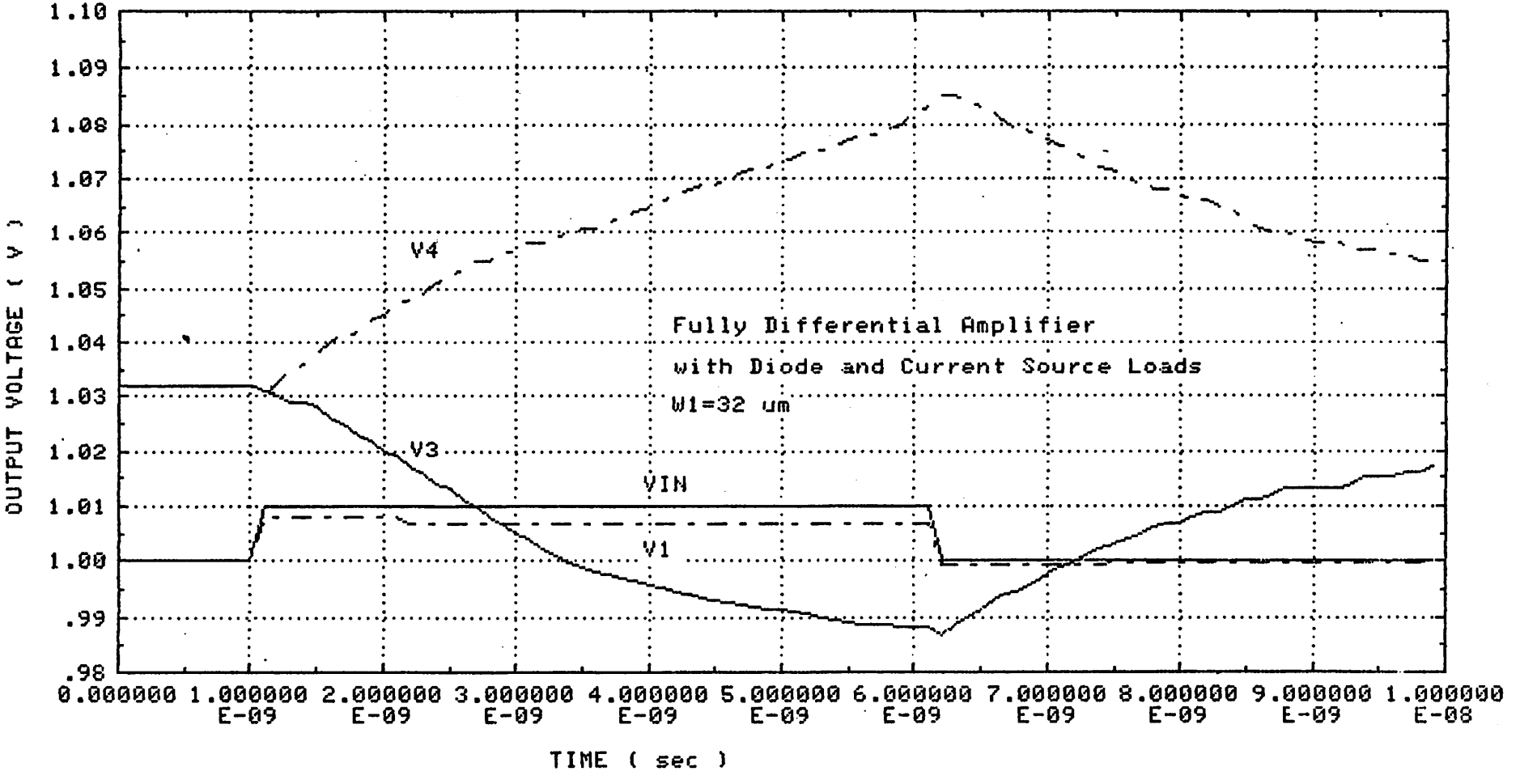


Fig.3.6-6 Transient Response of the Amplifier

with Diode and Current Source Loads (Vin = 10 mV)

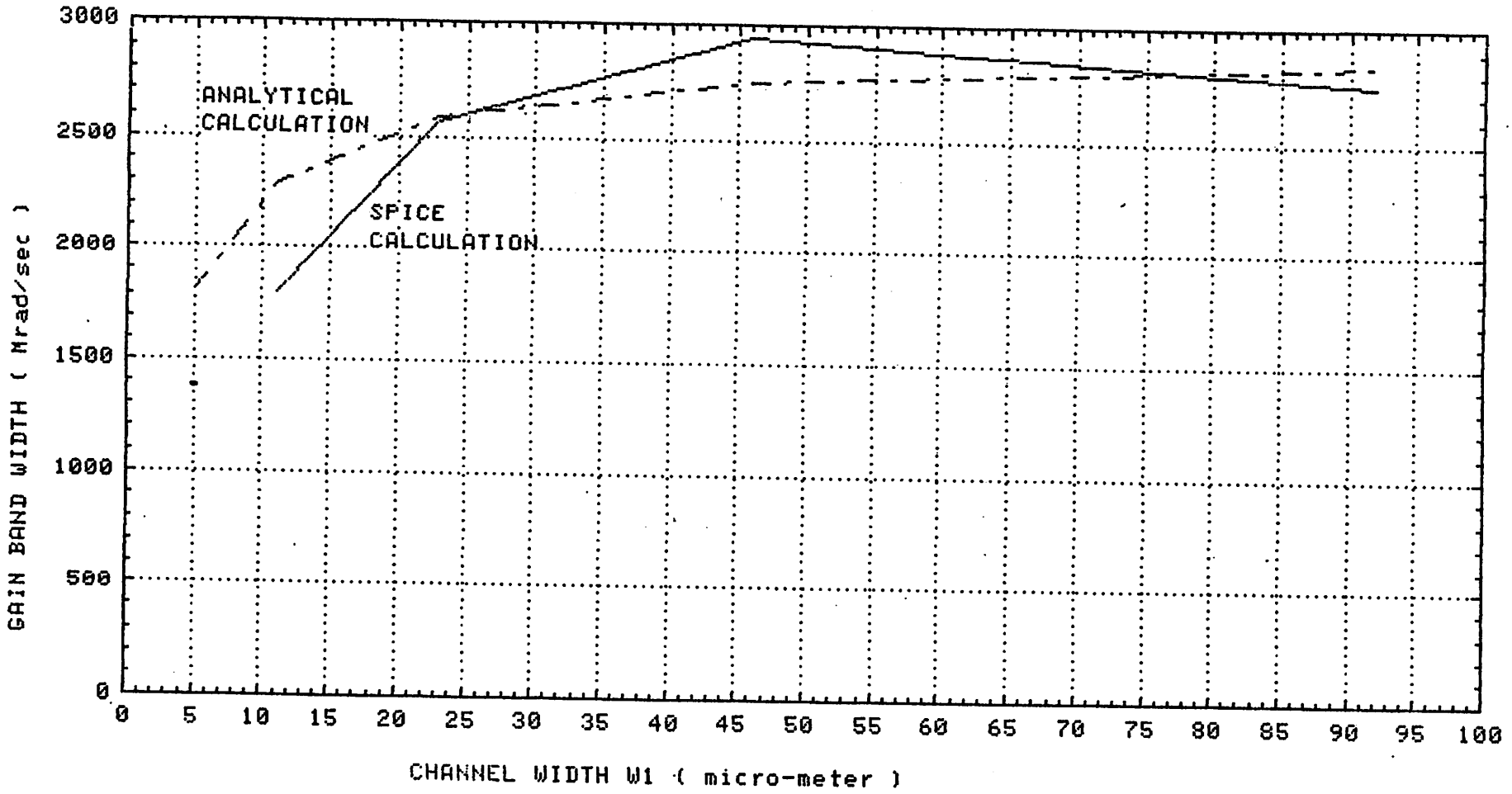


Fig.3.6-7 Gain Bandwidth Dependence on W1 for a Cascode

Differential Amplifier with Diode and Current Source Loads

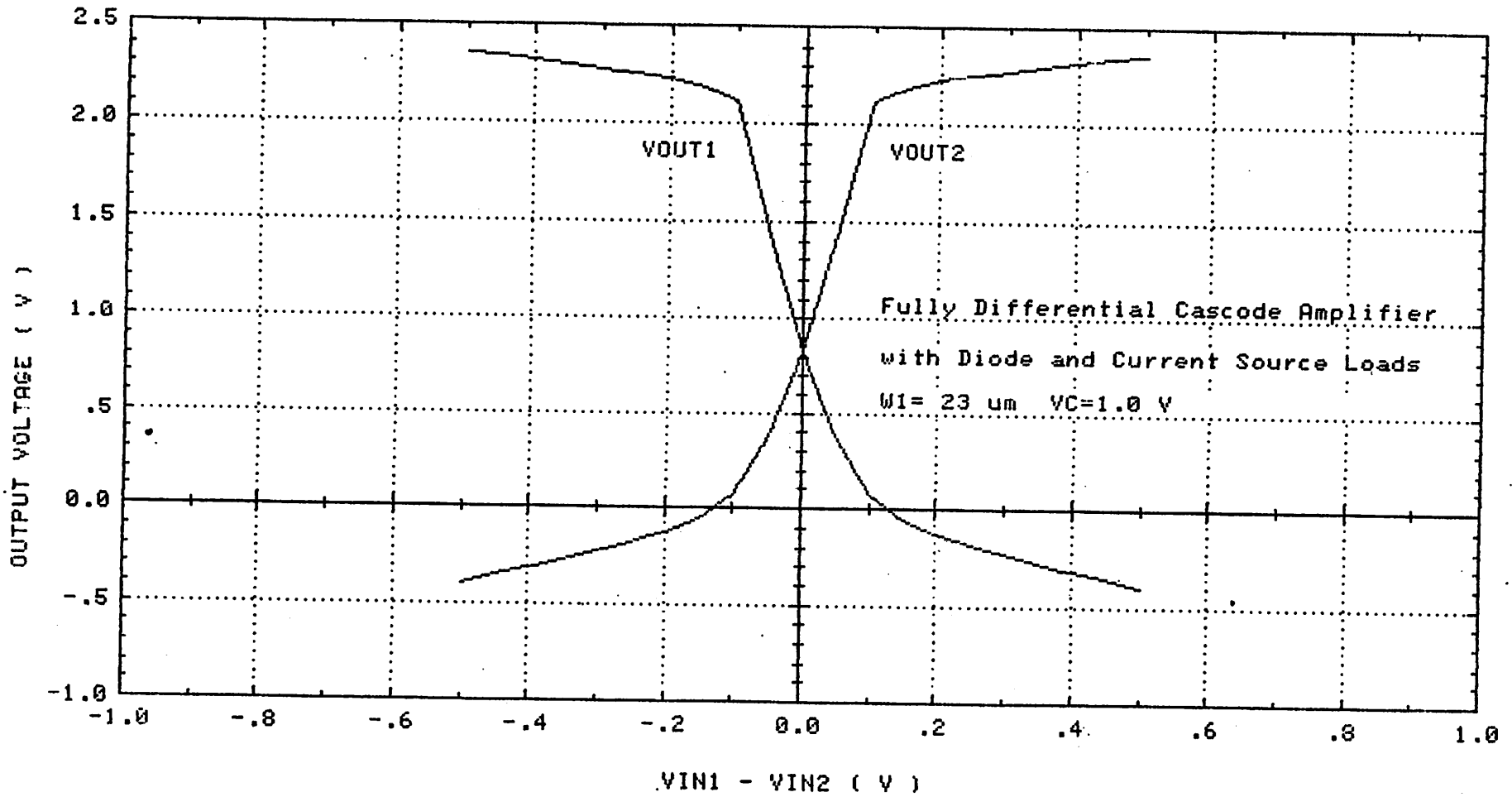


Fig.3.6-8 DC Transfer Characteristics of the Cascode

Differential Amplifier with Diode and Current Source Loads

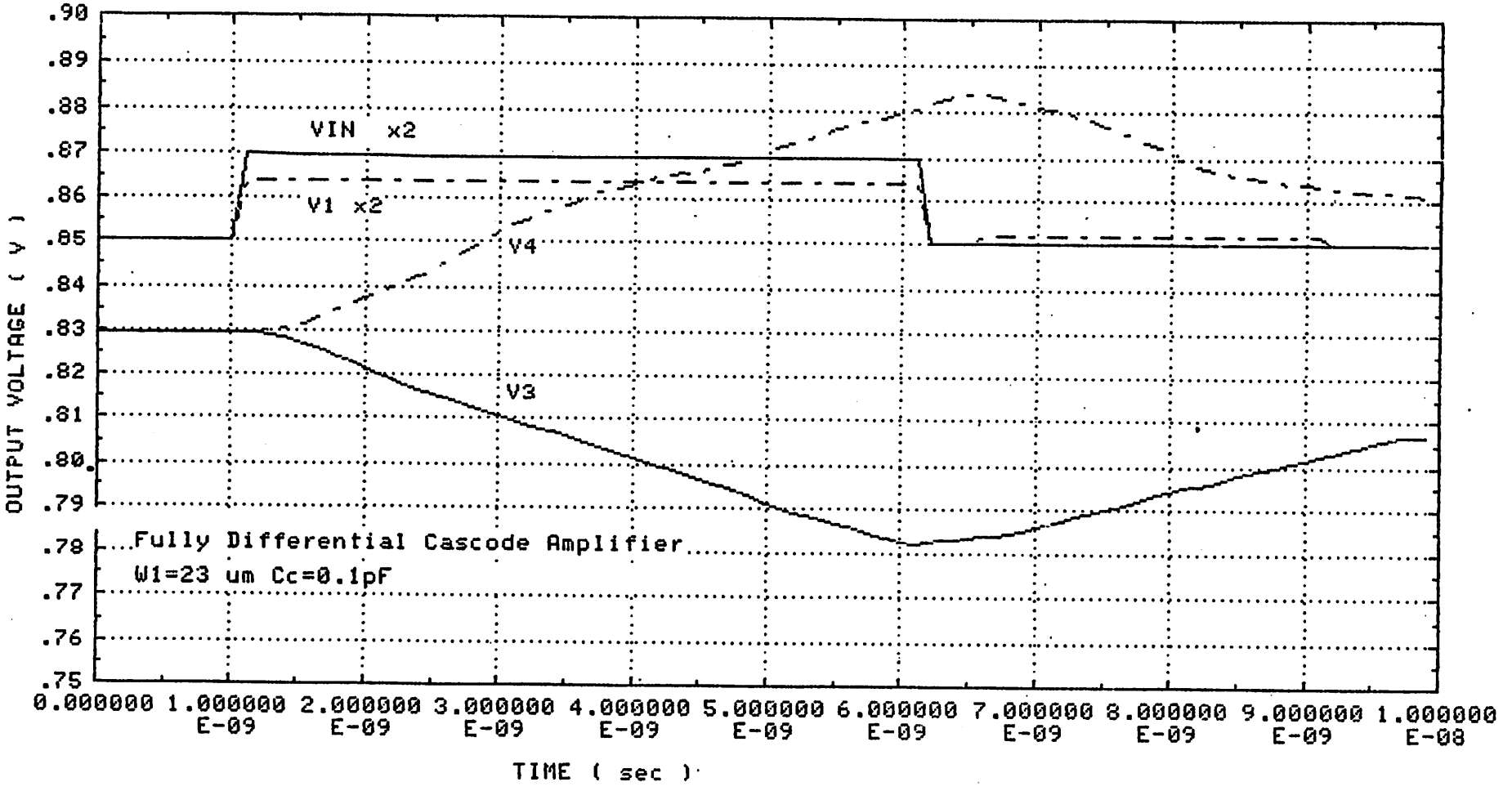


Fig.3.6-9 Transient Response of a Single-Stage Cascode Amplifier

with Diode and Current Source Loads (Vin = 10 mV)

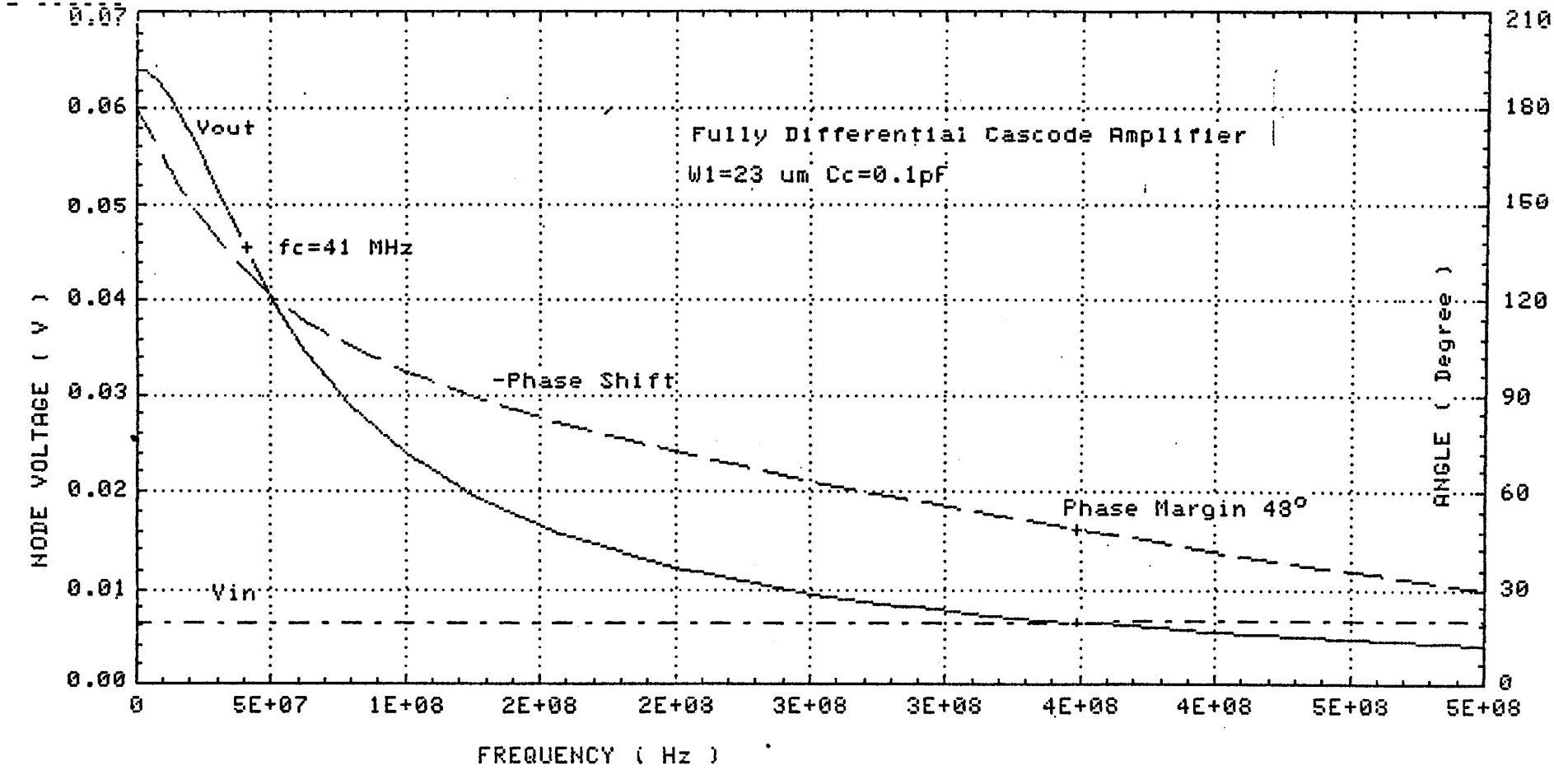


Fig.3.6-10 Amplitude and Phase Characteristics of a Cascode Differential Amplifier.

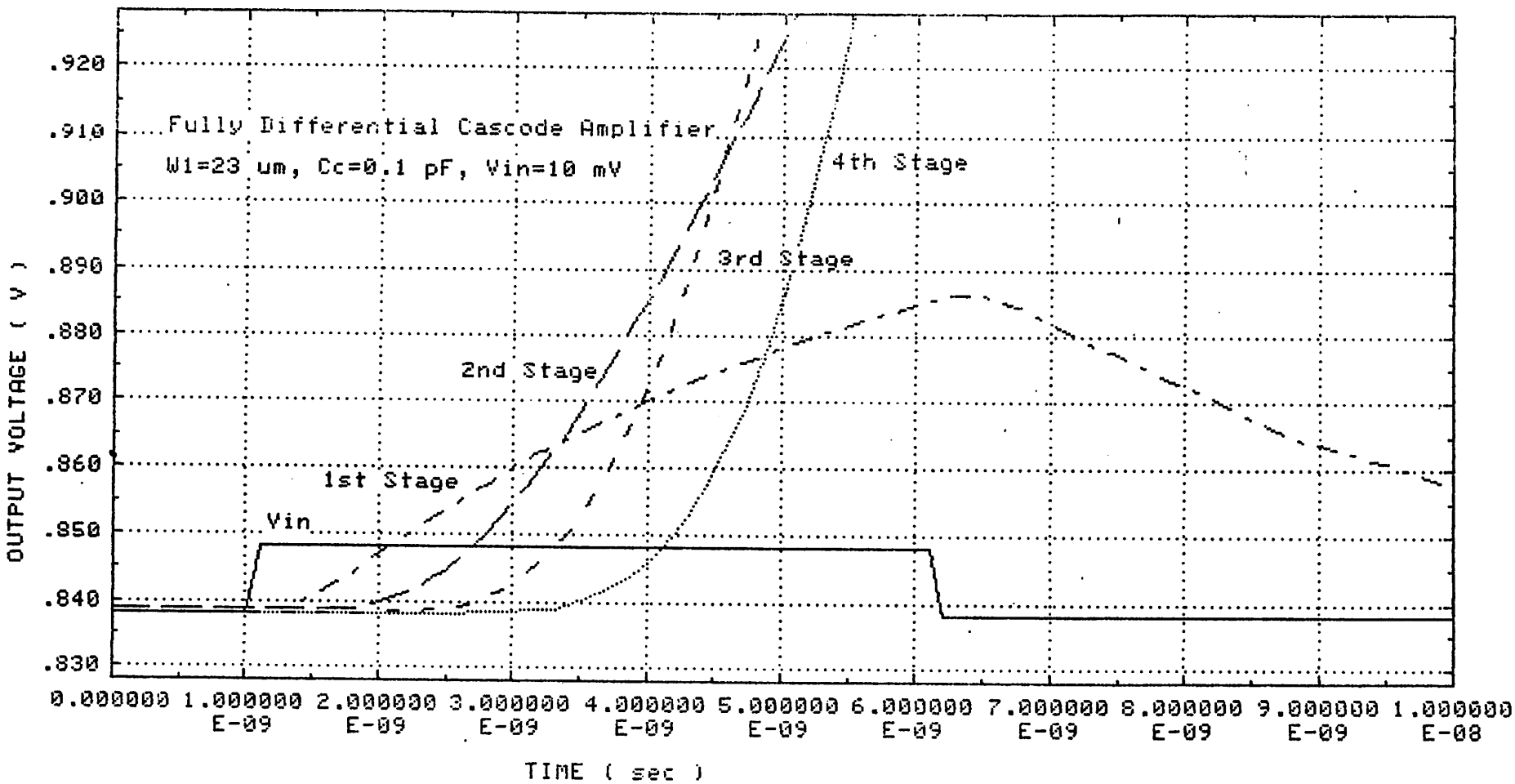


Fig.3.6-11 Transient Response of a Multi-Stage Cascode Amplifier with Diode and Current Source Loads (Vin = 10 mV)

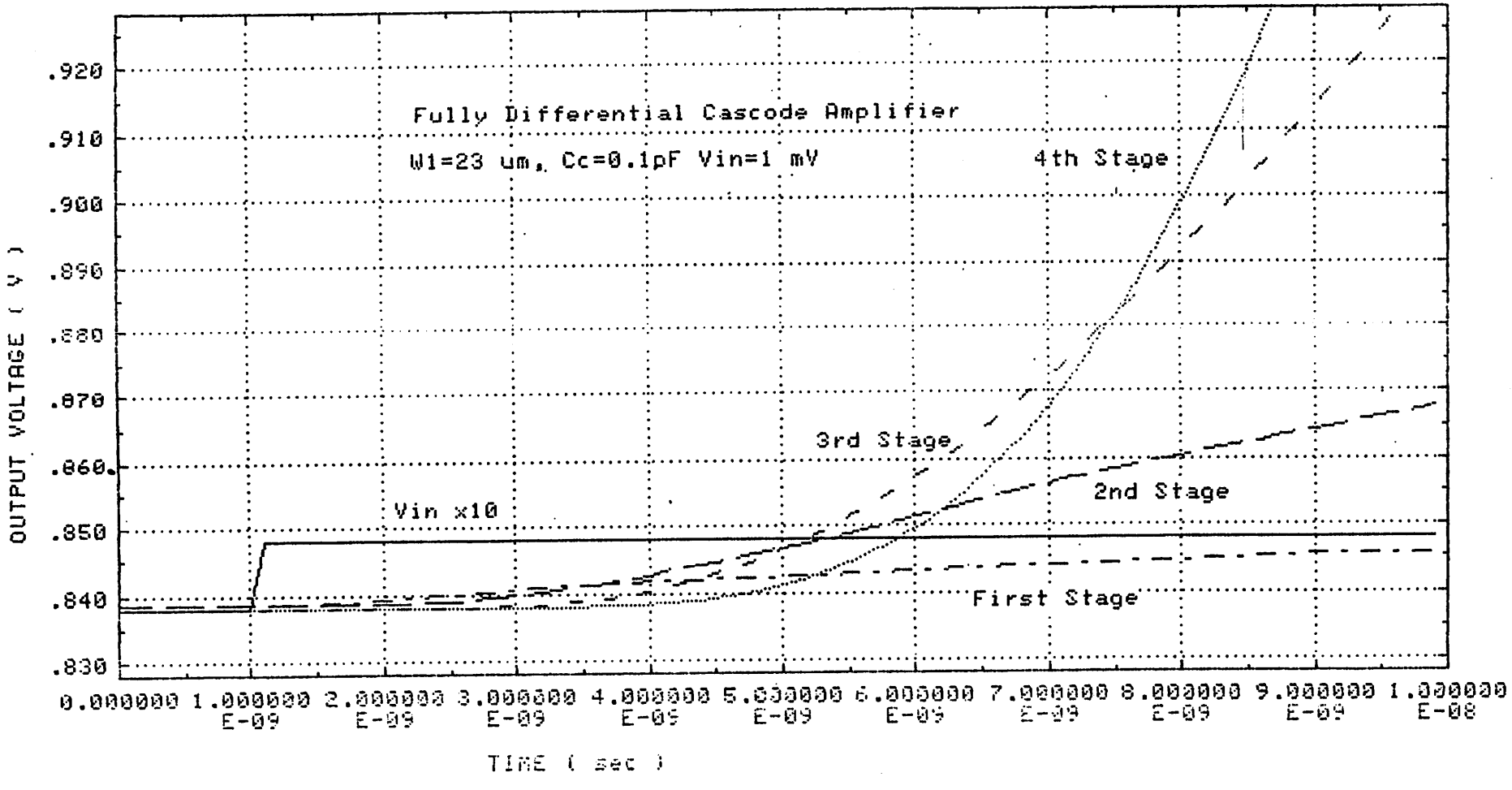


Fig.3.6-12 Transient Response of a Multi-Stage Cascode Amplifier

with Diode and Current Source Loads (Vin = 1 mV)

3.7 Simulation of the Comparator

A SPICE simulation of the full size comparator has been performed in the early stage of this project, for the purpose to check the feasibility of the architecture. The optimization of the amplifier used in the comparator has finished after this simulation. The amplifier used in this simulation is not the cascode type, but the diode and current source load type with a source follower buffer. Consequently, the speed is not as fast as the final version which will be reported in the upcoming paper. [1] However, even with this circuit the 10 bit, 15 MHz ADC can be realized, and the result of this simulation has encouraged us to proceed to the next step.

Fig. 3.7-1 shows the full circuit used in the simulation. The binary weighted capacitor array has been modeled as a pulse generator, a resistor and a capacitor connected in series. The pulse generator simulates the input signal or the reference voltage appearing in the bottom plate of the capacitors. The resistor is the on resistance of the bottom plate switches and is scaled, depending on the size of the capacitors. The minimum size resistor and capacitor have the value of 8 k Ω and 0.05 pF respectively. COMP5 is the comparator sub-circuit including the multi-stage amplifier and latch.

Fig.3.7-2 is the timing chart used in this simulation. The code of the comparator used here is assumed to be $(01000)_2 = 2^3 = 8$, and the input signal is $(0100100111)_2 = 2^8+2^5+7 = 295$. The reference voltage V_{ref} is 1.024 V, so that the input voltage is 295 mV.

From 0 to 20 ns, This input voltage is applied to the capacitors through the pulse generators VP1 to VP6. Then for the MSB evaluation period, the reference voltage is supplied only to the bit3 capacitor. This corresponds to the code (01000) of this comparator. The five most significant bits of the input data are (01001), and is larger than the comparator code. Then low level output L appears in the output MSB+. (From the sense that the input is larger than the reference, it might be better to set the output MSB+ to high

level H.) A 5 bit data of (01001) is supposed to be attained from the decoder, and this code is fed back to the capacitor array, turning its bottom plate voltage as 0.0, 1.024, 0.0, 0.0, 1.024 from the MSB to the LSB capacitors. A reference voltage of 256 mV, corresponding to the code (01000) is supplied to the bit0-B capacitor. Here, the five least significant bits of the input is (00111), which is smaller than the comparator code (01000). The output of H appears at LSB+ in this case.

Fig. 3.7-3 shows the comparator subcircuit COMP5. It consists of four subcircuits. Two of them are the fully differential amplifier HEADAMP2, and the other two are the differential amplifier merged with the latch. Transistors m1 and m2 are the sampling switches for the top electrode of the capacitor arrays.

HEADCMP2 is a fully differential amplifier with diode connected loads m3 and m4, and current sources m5 and m6. The number of transistors is 12.

LATCHD is the latch subcircuit with a differential amplifier. The driver transistors m13 and m14 of the latch share the same loads m3 to m6 with the driver transistors m1 and m2 of the amplifier. By this configuration, the smooth transfer of signals from the multi-stage amplifier to the latch can be realized. Transistors m26 and m27 are used to disconnect the amplifier drivers from the latch. These switches are essential to prevent the interference from the amplifier to the latch. (The node voltages of the source of m1 and m2 are pulled high during the latch operation. However it takes time to cut off m1 and m2, and they interfere the latch operation.)

Current source I1 and the differential amplifier composed by m16 to m18 are used to switch the amplifier and adjust its current.

Here in this comparator, two latches are used. One for the MSB evaluation and the other for the LSB evaluation. The purpose of this dual latch structure is to feed-back the MSB data to the capacitor array as soon as possible, without using any extra latch to hold the MSB data.

Fig.3.7-4 shows the program list of this simulation. SPICE Version 2G.1 is used here. Fig. 3.7-5 shows the node voltage as the result of the initial DC calculation, and the power dissipation. As was described in the previous section, the amplifier with source follower buffers consume more power than the other configurations. The total power dissipation here is 20.2 mW. Using 32 comparators will results in the power consumption of 646.4 mW, which is a relatively large value.

The result of the simulation is shown in Fig. 3.7-6. Here the MSB data can be evaluated at 30 ns from the sampling of the signal, and the LSB data can be acquired at 57 ns. The LSB data can be held by the latch during the next sampling and MSB evaluation cycle, so that a sampling cycle time of 60 ns is feasible.

The input voltage of the comparator is shown in Fig. 3.7-7. Here, no offset voltage is assumed in the comparator. During the sampling period, the input voltage jumps high and then saturates to zero. (less than a half LSB of 1 mV in the simulation) Then for the MSB evaluation there is a differential input of -74 mV.(Ideally it should be -78 mV.) And for the LSB evaluation the differential input is +2 mV as estimated in Fig. 3.7-2.

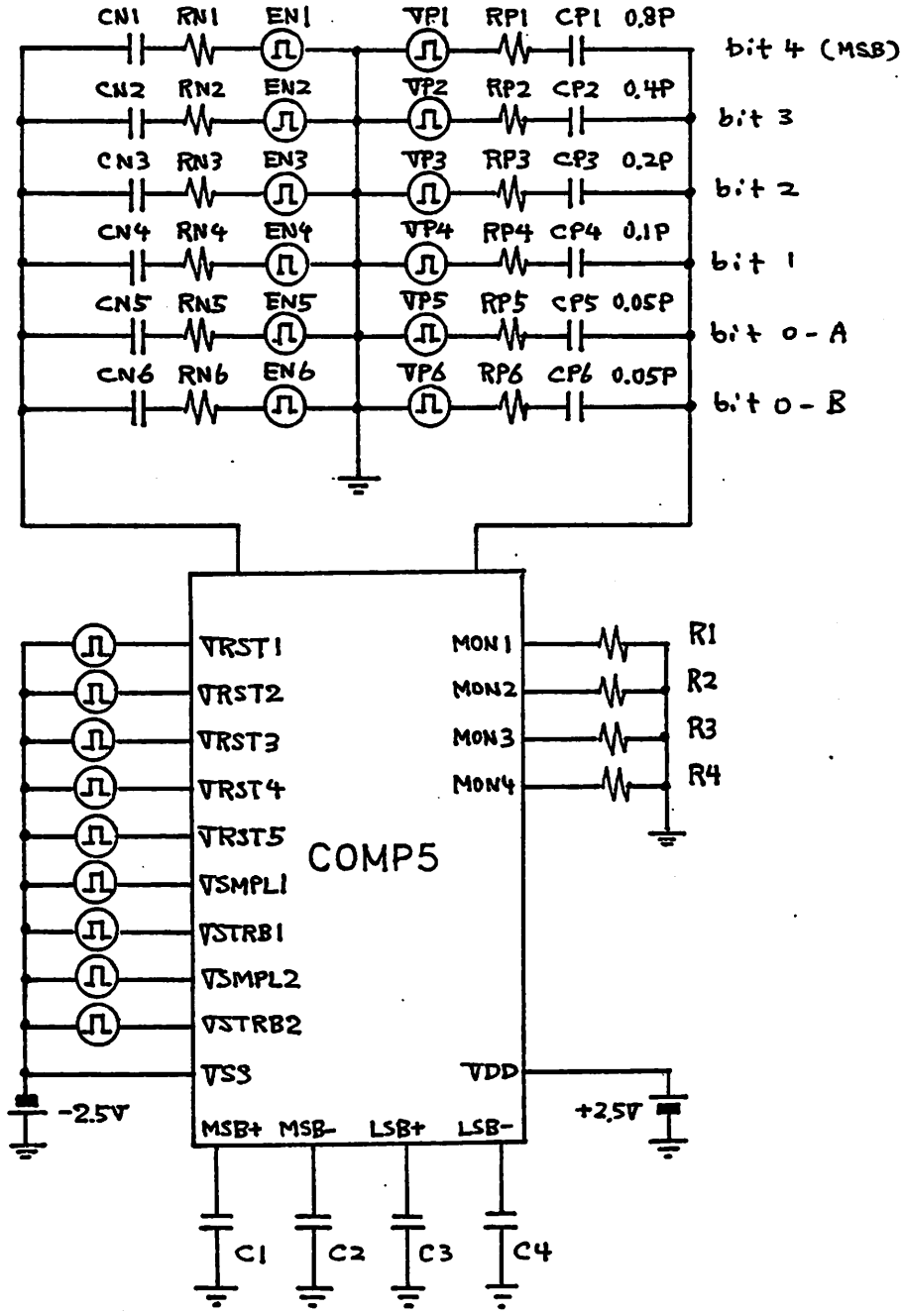


Fig. 3.7-1 Full Size Comparator Simulation

* Comparator Code (01000) .....$2^3 = 8$
* Input Signal (0100100111) .....$2^8+2^5+7 = 295$
* V_{ref} = 1.024 V
* Input Signal in Volts 1.024 x (288 + 7) / 1024 = 295 mV
* Unit Resistor in the Capacitor Array R_{on} = 8 k Ω
* Unit Capacitor in the Capacitor Array C_{unit} = 0.05 pF

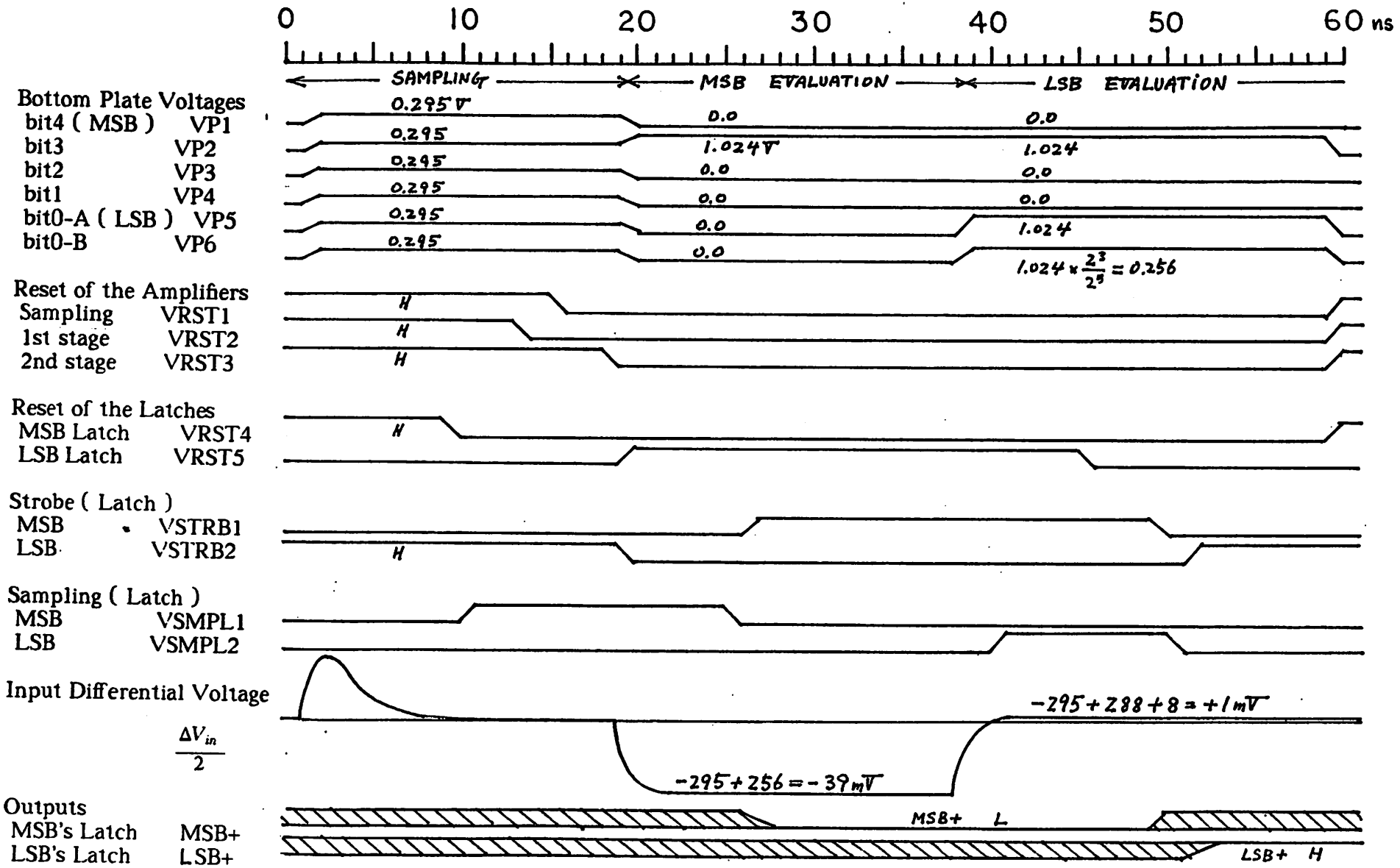


Fig. 3.7-2 Timing Chart for the Simulation

* Comparator Code (01000) .....$2^3 = 8$
* Input Signal (0100100111) .....$2^8+2^5+7 = 295$
* V_{ref} = 1.024 V
* Input Signal in Volts 1.024 x (288 + 7) / 1024 = 295 mV
* Unit Resistor in the Capacitor Array R_{on} = 8 k Ω
* Unit Capacitor in the Capacitor Array C_{unit} = 0.05 pF

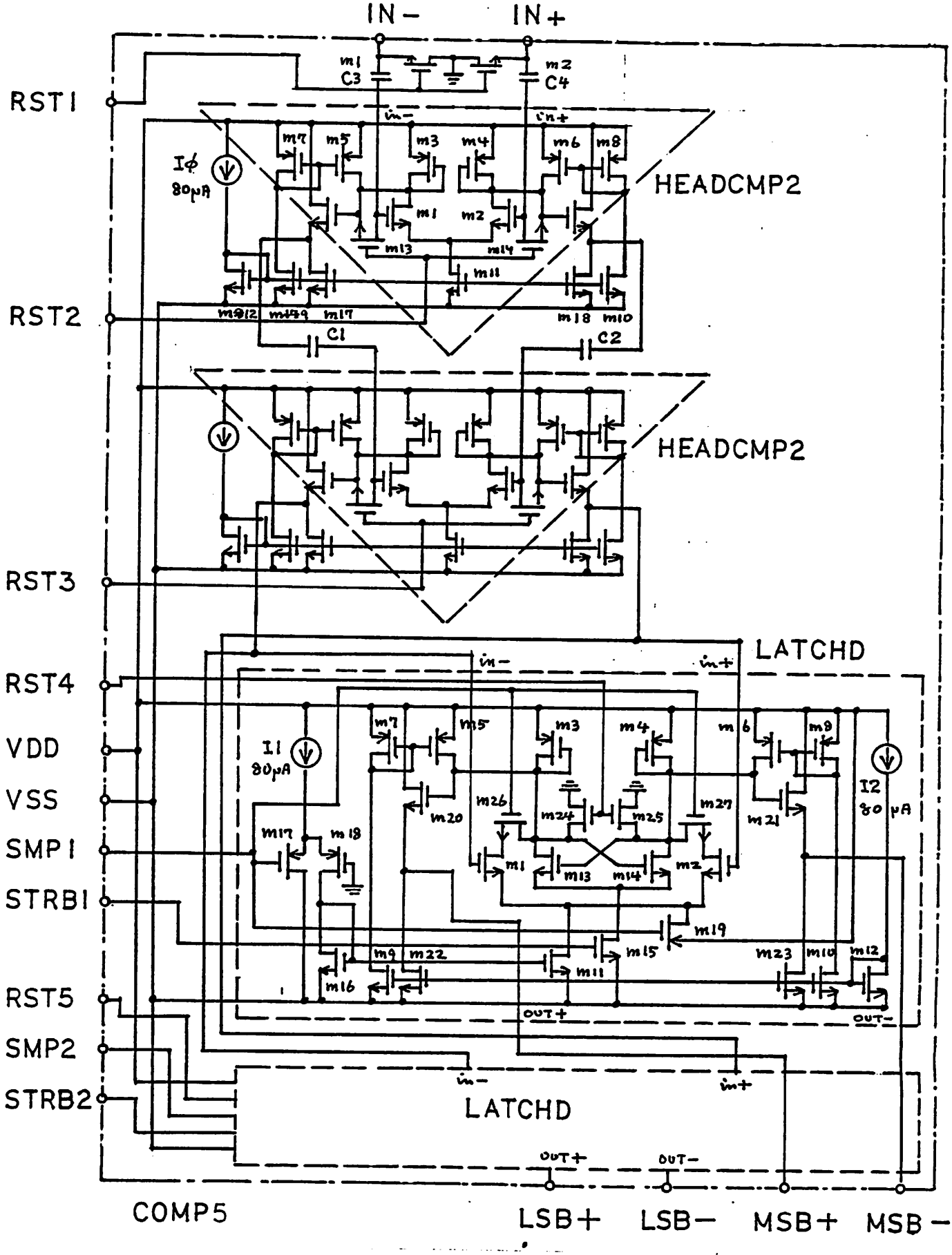


Fig. 3.7-3 Comparator Sub-Circuit COMP

```
********05/05/85 ******** SPICE 2G.6    5/15/85 ********14:47:42******

FULL SIZE COMPARATOR COMP4 TEST

****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************


*3 APRIL 1985
*3 STAGE OF HIGH SPEED AMP
*  COMP CODE 01000
*  INPUT     01001 00111 ( 0.295V)
*  VREF      1.024V
*  CUNIT     0.05PF
*  RUNIT     8KOHM
*  1CYCLE    60NS ( 16.7MHZ ) , 4 APRIL
*  INCREASE THE POWER OF THE SOURCE FOLLOWER. 4 APR
*  INCREASE THE BW OF HEADAMP BY THE FACTOR OF 2 ( M3,4 )
*  ADD M2 (BIG SW) IN COMP4 AND KEEP VRST2 H FOR T=0, 29 APRIL
*  ADD CAPACITORS AT THE FRONT OF THE COMPARATORS. 2 MAY
*  CHANGE THE CONVERSION CONDITION IN .OPTIONS, 3 MAY
C1   3   0   0.1P
C2   4   0   0.1P
C3   5   0   0.1P
C4   6   0   0.1P
R1  18   0   1T
R2  19   0   1T
R3  20   0   1T
R4  21   0   1T
CP1 22   1   0.8P
CP2 23   1   0.4P
CP3 24   1   0.2P
CP4 25   1   0.1P
CP5 26   1   0.05P
CP6 27   1   0.05P
CN1 34   2   0.8P
CN2 35   2   0.4P
CN3 36   2   0.2P
CN4 37   2   0.1P
CN5 38   2   0.05P
CN6 39   2   0.05P
RP1 28  22   0.5K
RP2 29  23   1K
RP3 30  24   2K
RP4 31  25   4K
RP5 32  26   8K
RP6 33  27   8K
RN1 40  34   0.5K
RN2 41  35   1K
RN3 42  36   2K
RN4 43  37   4K
RN5 44  38   8K
RN6 45  39   8K
VDD  7  0    DC  2.5
VSS  8  0    DC -2.5
VRST1   9   8   PULSE(5 0 15N 1N 1N 53N 60N)
VRST2  10   8   PULSE(5 0 13N 1N 1N 49N 70N)
VRST3  11   8   PULSE(5 0 18N 1N 1N 40N 60N)
VRST4  12   8   PULSE(5 0 9N 1N 1N 49N 60N)
VRST5  13   8   PULSE(0 5 19N 1N 1N 25N 60N)
VSMPL1 14   8   PULSE(0 5 10N 1N 1N 14N 60N)
VSTRB1 15   8   PULSE(0 5 26N 1N 1N 22N 60N)
VSMPL2 16   8   PULSE(0 5 40N 1N 1N  9N 60N)
VSTRB2 17   8   PWL(0 0 51N 0 52N 5 79N 5 80N 0)
VP1    28   0   PULSE(0 0.295 1N 1N 1N 17N 70N)
VP2    29   0   PWL(0 0 1N 0 2N 0.295 19N 0.295 20N 1.024 59N 1.024 60N 0)
EP3    30   0    28  0  1
EP4    31   0    28  0  1
VP5    32   0   PWL(0 0 1N 0 2N 0.295 19N 0.295 20N 0 38N 0 39N 1.024 59N 1.024
+                 60N 0)
VP6    33   0   PWL(0 0 1N 0 2N 0.295 19N 0.295 20N 0 38N 0 39N 0.256 59N 0.256
+                 60N 0)
```

Fig. 3.7-4-1 Simulation Program List (1)

```
EN1    40   0   28   0   -1
EN2    41   0   29   0   -1
EN3    42   0   30   0   -1
EN4    43   0   31   0   -1
EN5    44   0   32   0   -1
EN6    45   0   33   0   -1
X1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 COMP4
.SUBCKT COMP4 1 2   3    4    5    6    7    8    9    10   11   12   13
*           IN+ IN- MSB+ MSB- LSB+ LSB- VDD VSS RST1 RST2 RST3 RST4 RST5
+ 14   15    16   17    18   19   20   21
*SMP1 STRB1 SMP2 STRB2 MON1 MON2 MON3 MON4

C1   18 22   0.1P
C2   19 23   0.1P
C3   1  24   0.1P
C4   2  25   0.1P
M1   1   9   0   8   NMOS   W=40U   L=2U   AD=260P AS=260P PD=53U PS=53U
M2   2   9   0   8   NMOS   W=40U   L=2U   AD=260P AS=260P PD=53U PS=53U
X1   24 25 18 19 7  8   10   HEADCMP2
X2   22 23 20 21 7  8   11   HEADCMP2
X3   20 21 4  3   14 15 7  8 12 LATCHD
X4   20 21 6  5   16 17 7  8 13 LATCHD
.ENDS COMP4
*HEADCMP2 SUBCIRCUIT
*3 APRIL 1985
*HEADCMP WITH SOURCE FOLLOWER
.SUBCKT HEADCMP2  1    2    12   13   8   9   11
*                 IN+ IN- OUT- OUT+ VDD VSS RST
I0   8 10 DC 80U
RS   8 10 1MEG
M1   4  1  3  9   NMOS W=27U AD=175.5P AS=175.5P PD=40U  PS=40U
M2   5  2  3  9   NMOS W=27U AD=175.5P AS=175.5P PD=40U  PS=40U
M3   4  4  8  8   PMOS W=12U AD=78P    AS=78P    PD=23U  PS=23U
M4   5  5  8  8   PMOS W=12U AD=78P    AS=78P    PD=23U  PS=23U
M5   4  6  8  8   PMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M6   5  7  8  8   PMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M7   6  6  8  8   PMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M8   7  7  8  8   PMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M9   6 10  9  9   NMOS W=16U AD=104P   AS=104P   PD=29U  PS=29U
M10  7 10  9  9   NMOS W=16U AD=104P   AS=104P   PD=29U  PS=29U
M11  3 10  9  9   NMOS W=36U AD=234P   AS=234P   PD=49U  PS=49U
M12 10 10  9  9   NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
M13  4 11  1  9   NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
M14  5 11  2  9   NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
M15  8  4 12  9   NMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M16  8  5 13  9   NMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M17 12 10  9  9   NMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
M18 13 10  9  9   NMOS W=24U AD=156P   AS=156P   PD=37U  PS=37U
*M15  8  4 12  9  NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
*M16  8  5 13  9  NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
*M17 12 10  9  9  NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
*M18 13 10  9  9  NMOS W=8U  AD=52P    AS=52P    PD=21U  PS=21U
.ENDS HEADCMP2
.SUBCKT LATCHD  1    2    16   17   14   13   8   9   18
*               IN+ IN- OUT- OUT+ SMPL STRB VDD VSS RST
*19 MAR. 1985 , REVISED 22 MARCH 1985.
I0   8 10 DC 80U
I1   8 15 DC 80U
RS0  8 10 1MEG
RS1  8 15 1MEG
```

Fig. 3.7-4-2 Simulation Program List (2)

```
M1   19 1   3   9   NMOS W=27U AD=175.5P AS=175.5P PD=40U   PS=40U
M2   20 2   3   9   NMOS W=27U AD=175.5P AS=175.5P PD=40U   PS=40U
M3   4  4   8   8   PMOS W=3U  AD=19.5P  AS=19.5P  PD=16U   PS=16U
M4   5  5   8   8   PMOS W=3U  AD=19.5P  AS=19.5P  PD=16U   PS=16U
M5   4  6   8   8   PMOS W=24U AD=156P   AS=156P   PD=37U   PS=37U
M6   5  7   8   8   PMOS W=24U AD=156P   AS=156P   PD=37U   PS=37U
M7   6  6   8   8   PMOS W=24U AD=156P   AS=156P   PD=37U   PS=37U
M8   7  7   8   8   PMOS W=24U AD=156P   AS=156P   PD=37U   PS=37U
M9   6  10  9   9   NMOS W=16U AD=104P   AS=104P   PD=29U   PS=29U
M10  7  10  9   9   NMOS W=16U AD=104P   AS=104P   PD=29U   PS=29U
M11  3  12  9   9   NMOS W=36U AD=234P   AS=234P   PD=49U   PS=49U
M12  10 10  9   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M13  4  5   11  9   NMOS W=27U AD=175.5P AS=175.5P PD=40U   PS=40U
M14  5  4   11  9   NMOS W=27U AD=175.5P AS=175.5P PD=40U   PS=40U
M15  11 13  9   9   NMOS W=4U  L=4U AD=26P AS=26P  PD=17U   PS=17U
M16  12 12  9   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M17  9  14  15  8   PMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M18  12 0   15  8   PMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M19  3  14  8   8   PMOS W=36U AD=234P   AS=234P   PD=49U   PS=49U
M20  8  4   16  9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M21  8  5   17  9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M22  16 10  9   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M23  17 10  9   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M24  4  18  0   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M25  5  18  0   9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M26  4  14  19  9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
M27  5  14  20  9   NMOS W=8U  AD=52P    AS=52P    PD=21U   PS=21U
.ENDS LATCHD
*MOS MODELS  (FIRST VERSION, XEROX 2U)
*19 MAR. 1985
*
.MODEL PMOS PMOS LEVEL=2 VTO=-0.70 KP=48.0U GAMMA=.49 TOX=30N
+ NSUB=1E16 TPG=-1 XJ=0.5U LD=0.375U XQC=0.5
+ UEXP=0.440 VMAX=9.0E4 LAMBDA=.024
* MAX CAPS
+ CGSO=5.1E-10 CGDO=5.1E-10 CJ=3.4E-4 CJSW=3.8E-10 CGBO=1.5E-10
* TYPICAL CAPS
* CGSO=4.4E-10 CGDO=4.4E-10 CJ=3.1E-4 CJSW=3.0E-10 CGBO=1.4E-10
*

.MODEL NMOS NMOS LEVEL=2 VTO=.7 KP=67U GAMMA=.44 TOX=30N
+NSUB=1.0E16 XJ=0.3U LD=.375U UEXP=.12 VMAX=5.2E4 LAMBDA=.024
+XQC=0.5
* MAX CAPS
+ CGSO=3.1E-10 CGDO=3.1E-10 CJ=3.0E-4 CJSW=1.9E-10 CGBO=1.5E-10
* TYPICAL CAPS
* CGSO=2.7E-10 CGDO=2.7E-10 CJ=1.5E-4 CJSW=2.5E-10 CGBO=1.4E-10
*
*MOS WITH OFFSET
.MODEL NMOSD NMOS LEVEL=2 VTO=1.0 KP=67U GAMMA=.44 TOX=30N
+NSUB=1.0E16 XJ=0.3U LD=.375U UEXP=.12 VMAX=5.2E4 LAMBDA=.024
+XQC=0.5
* MAX CAPS
+ CGSO=3.1E-10 CGDO=3.1E-10 CJ=3.0E-4 CJSW=1.9E-10 CGBO=1.5E-10
* TYPICAL CAPS
* CGSO=2.7E-10 CGDO=2.7E-10 CJ=1.5E-4 CJSW=2.5E-10 CGBO=1.4E-10
.OPTIONS ACCT LIMTIM=10 DEFL=2U ITL1=500
+ABSTOL=10P VNTOL=10U


.TRAN 0.5N 70N
.PRINT TRAN V(1,2) V(22,1) V(28) V(18) V(19) V(20) V(21) V(3) V(5)
.PLOT  TRAN V(18) V(19) (-0.5,3.5) V(20) V(21) (-1.5,2.5)
+V(3) V(4) (-12.5,7.5) V(5) V(6) (-17.5,2.5)
.WIDTH OUT=80
.END
```

Fig. 3.7-4-3 Simulation Program List (3)

```
********05/05/85 ******** SPICE 2G.6    3/15/83 ********14:47:42*****

FULL SIZE COMPARATOR COMP4 TEST

****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************
```

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-0.0000	(2)	-0.0000	(3)	-0.9909	(4)	-0.9909
(5)	0.8282	(6)	0.8282	(7)	2.5000	(8)	-2.5000
(9)	2.5000	(10)	2.5000	(11)	2.5000	(12)	2.5000
(13)	-2.5000	(14)	-2.5000	(15)	-2.5000	(16)	-2.5000
(17)	-2.5000	(18)	-0.1698	(19)	-0.1698	(20)	-0.1698
(21)	-0.1698	(22)	0.0	(23)	0.0	(24)	0.0
(25)	0.0	(26)	0.0	(27)	0.0	(28)	0.0
(29)	0.0	(30)	0.0	(31)	0.0	(32)	0.0
(33)	0.0	(34)	0.0	(35)	0.0	(36)	0.0
(37)	0.0	(38)	0.0	(39)	0.0	(40)	0.0
(41)	0.0	(42)	0.0	(43)	0.0	(44)	0.0
(45)	0.0	(46)	1.4149	(47)	1.4149	(48)	1.4149
(49)	1.4149	(50)	-1.1018	(51)	1.4149	(52)	-0.0496
(53)	1.4149	(54)	0.7249	(55)	0.7249	(56)	-1.1018
(57)	1.4149	(58)	-0.0496	(59)	1.4149	(60)	0.7249
(61)	0.7249	(62)	-1.1018	(63)	-0.3122	(64)	-0.9462
(65)	2.4993	(66)	-0.9462	(67)	0.5119	(68)	0.5119
(69)	0.7249	(70)	0.7249	(71)	-1.8734	(72)	-0.3319
(73)	-1.1018	(74)	-0.3122	(75)	-0.9462	(76)	2.4993
(77)	-0.9462	(78)	2.5000	(79)	2.5000	(80)	0.7249
(81)	0.7249	(82)	-1.8734	(83)	1.5627		

```
    TOTAL POWER DISSIPATION   2.02D-02  WATTS
```

Fig. 3.7-5 Node Voltage and Power Dissipation

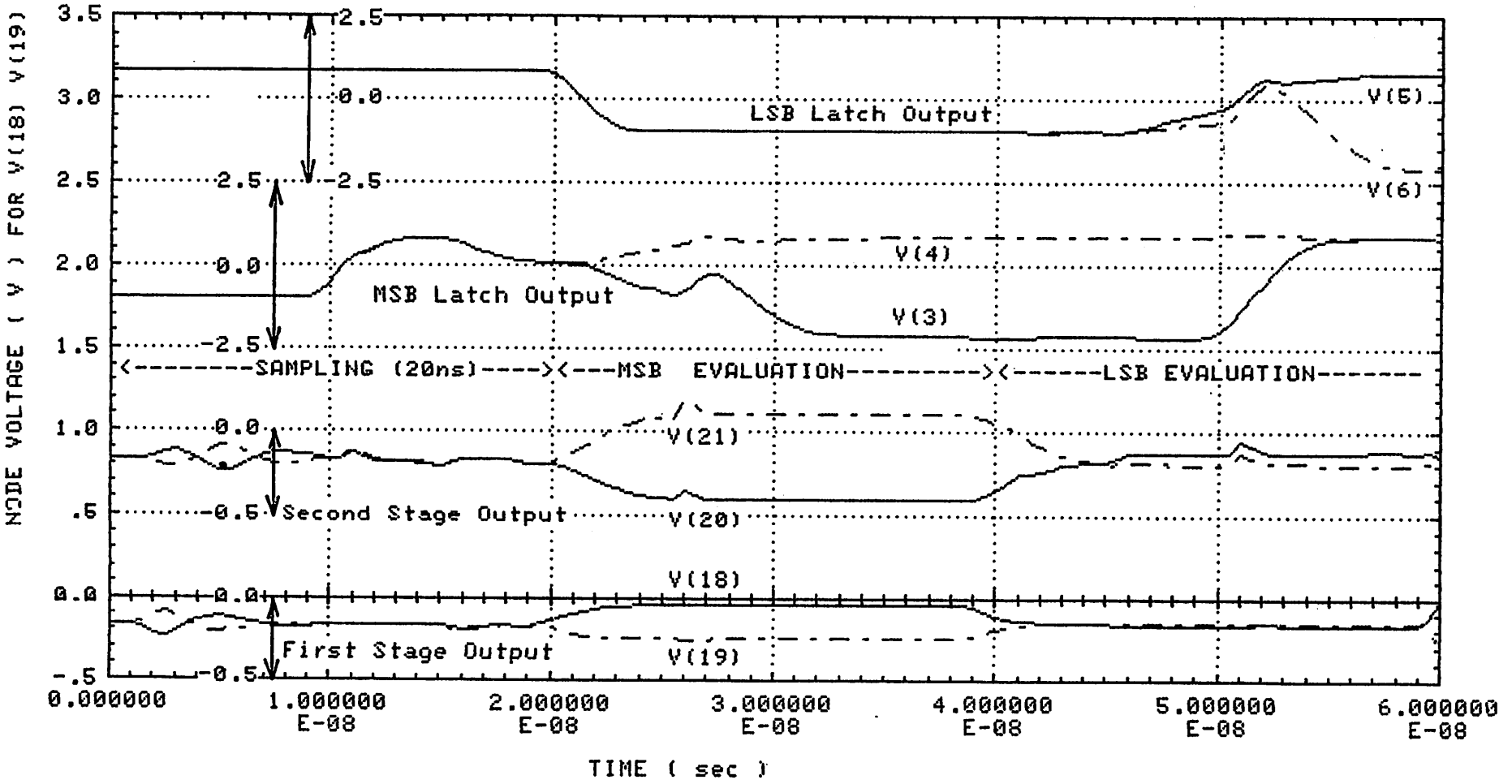


Fig. 3.7-6 Simulation Result

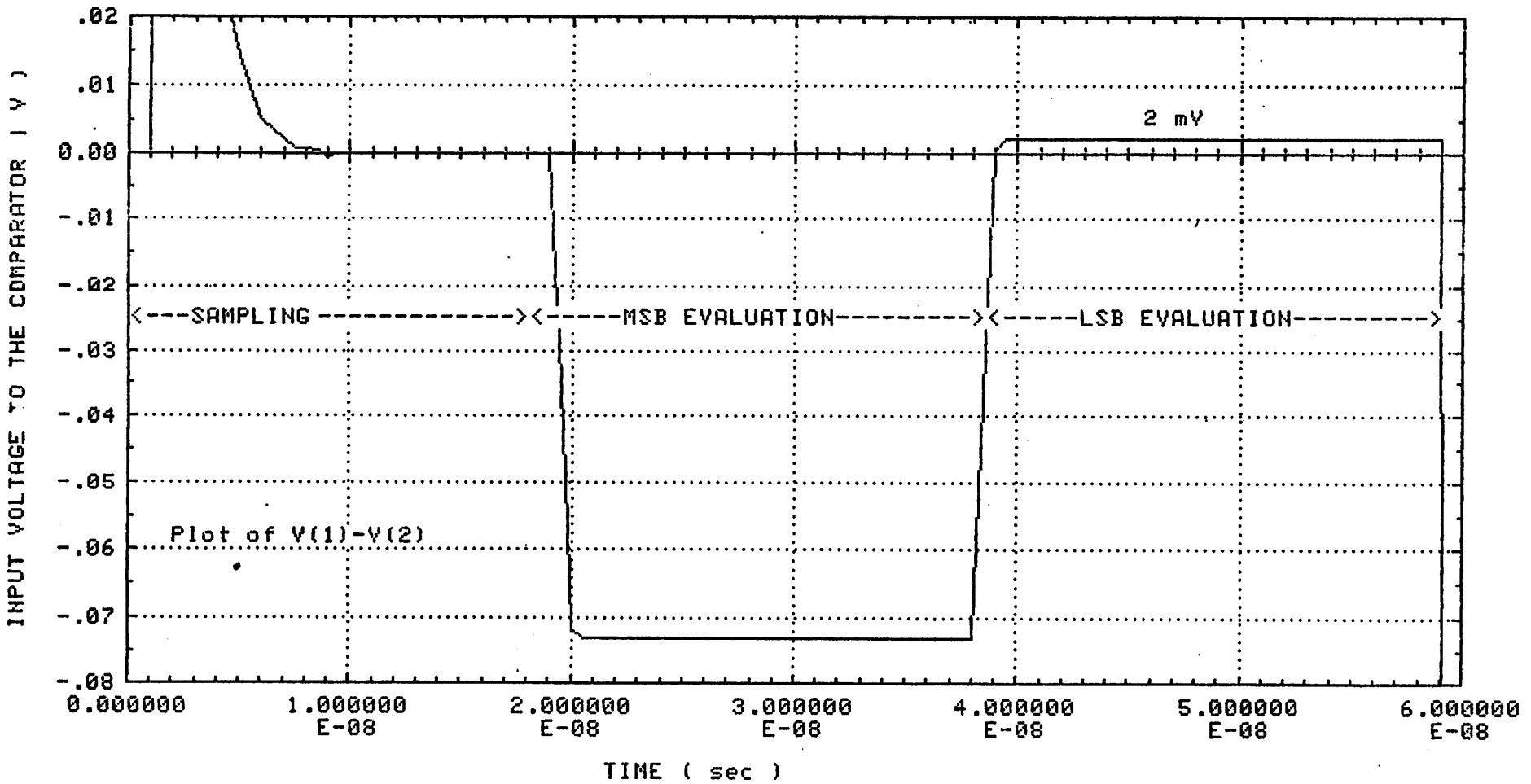


Fig. 3.7-7 Comparator Input Voltage

CHAPTER 4 CONCLUSION

A brief review about a new high-speed, high-precision ADC architecture originally proposed by J. Doernberg [1] has been presented.

Then, the design of the comparator, which is the most critical part in that ADC, has been discussed in detail.

A SPICE simulation of the full comparator circuit shows the feasibility of this ADC algorithm and the comparator configuration.

The author has joined in this project for only 8 month, which is too short to finish the design of a full ADC circuit. Therefore, he made a concentration on the analysis and design of the high-speed high-precision comparator. The author wishes that all these analysis and simulations will be of some help to those who are engaged in the design of a high-speed and high-precision comparators.

Appendix A Transient Response of the Latch

(1) Latch without Loads

As discussed in Sec. 3.2, at the beginning, the cross-coupled common-source MOS transistors operate without loads, in order to avoid the large offset error induced by the mis-match of the current source loads. In this state, the circuit has the configuration as shown in Fig. A-1. The relations among the currents and voltages can be expressed in the following five equations.

$$I1 = \frac{\beta}{2}(V2-Vs-Vt)^2 \tag{A-1}$$

$$I2 = \frac{\beta}{2}(V1-Vs-Vt)^2 \tag{A-2}$$

$$I1 + I2 = Io+Co\frac{dVs}{dt} \tag{A-3}$$

$$I1 = -C\frac{dV1}{dt} \tag{A-4}$$

$$I2 = -C\frac{dV2}{dt} \tag{A-5}$$

And let's assume the following initial conditions.

$$V1(0) = Vo+\frac{S}{2} \tag{A-6}$$

$$V2(0) = Vo-\frac{S}{2} \tag{A-7}$$

$$Vs(0) = Vso$$

Here,Vo is the common mode input signal, and S is the differential mode input signal.

By indicating the common mode voltage by Vc, and the differential mode voltage by Vd, then V1 and V2 can be expressed as follows:

$$V1 = Vc+\frac{Vd}{2}$$

$$V2 = Vc-\frac{Vd}{2}$$

Then from Eq. (A-1)(A-2)and (A-3), the common mode voltage transient can be solved as

$$Vc = Vo-\frac{Io\ t}{2C}-\frac{Co}{2C}(Vs-Vso) \tag{A-8}$$

From Eq.(A-1) and (A-2), a differential equation for the differential mode voltage can be derived;

$$\frac{dVd}{dt} = \frac{\beta}{C}(Vc - Vs - Vt)Vd \qquad \text{(A-9)}$$

Here an essential approximation must be considered for the estimation of Eq. (A-9). Let's assume the common source voltage Vs to be,

$$Vs = Vso - \alpha t \qquad \text{(A-11)}$$

The value of α can be approximated as follows for the first order calculation, that is the discharge of the capacitors by Io.

$$\alpha = \frac{Io}{2C + Co}$$

For the sink current Io of 10 μ A and the total capacitance of 0.1pF, this value is 100 mV/nS.

From Eq.(A-8),(A-9) and (A-11), a differential equation for Vd can be derived as follows;

$$\frac{dVd}{dt} = \frac{\beta}{C}(Vo - Vso - Vt)Vd = \frac{g_{m0}}{C}Vd \qquad \text{(A-12)}$$

Here g_{m0} is the initial mutual conductance of each cross coupled MOS transistors.

This can be easily solved to get;

$$Vd(t) = S\ exp\left(\frac{g_{m0}}{C}t\right) \qquad \text{(A-13)}$$

The differential mode signal grows exponentially with the time constant $\frac{C}{g_{m0}}$.

(2) Latch with Current Source Loads

To drive external loads, current source pull up circuits will be required as shown in Fig. A-2. As described in sec. 3.2, these current sources are connected to the cross coupled MOS FETs after the amplified difference voltage Vd(t) reaches a value much larger than its offset.

Again, the relations among the currents and voltages can be expressed in the following five equations.

$$I1 = \frac{\beta}{2}(V2-Vs-Vt)^2 \qquad \text{(A-14)}$$

$$I2 = \frac{\beta}{2}(V1-Vs-Vt)^2 \qquad \text{(A-15)}$$

$$I1 + I2 = Io + Co\frac{dVs}{dt} \qquad \text{(A-16)}$$

$$I1 = -C\frac{dV1}{dt} + IL \qquad \text{(A-17)}$$

$$I2 = -C\frac{dV2}{dt} + IL \qquad \text{(A-18)}$$

Here,IL is the current flowing in the load.

Then from Eq. (A-14)(A-15)and (A-16), the common mode voltage transient can be solved as

$$Vc = Vo - \frac{(Io-2IL)t}{2C} - \frac{Co}{2C}(Vs-Vso) \qquad \text{(A-19)}$$

From Eq.(A-14) and (A-15), a differential equation for the differential mode voltage can be derived.

$$\frac{dVd}{dt} = \frac{\beta}{C}(Vc-Vs-Vt)Vd \qquad \text{(A-20)}$$

Again an approximation must be considered for the estimation of Eq. (A-20). Let's assume the common source voltage Vs to be,

$$Vs = Vso-\alpha t \qquad \text{(A-21)}$$

The value of α can be approximated as follows for the first order calculation, that is the discharge of the capacitors by Io-2IL.

$$\alpha = -\frac{(Io-2IL)}{2C+Co}$$

If Io is equal to 2IL, no change in the common source voltage Vs is observed.

From Eq.(A-19),(A-20) and (A-21), the same results Eq.(A-12) and (A-13) can be derived.

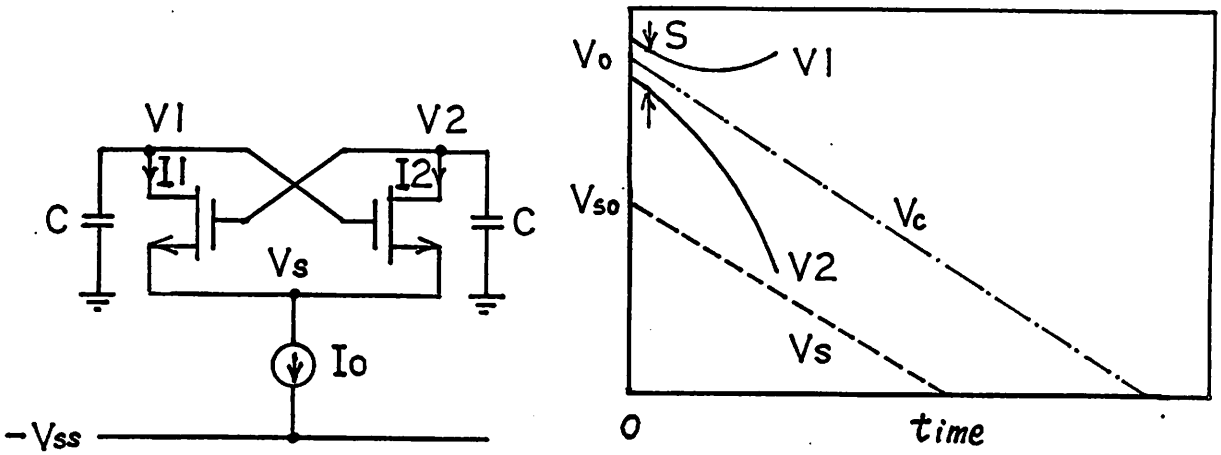


Fig. A-1 Transient Response of a Latch without Loads.

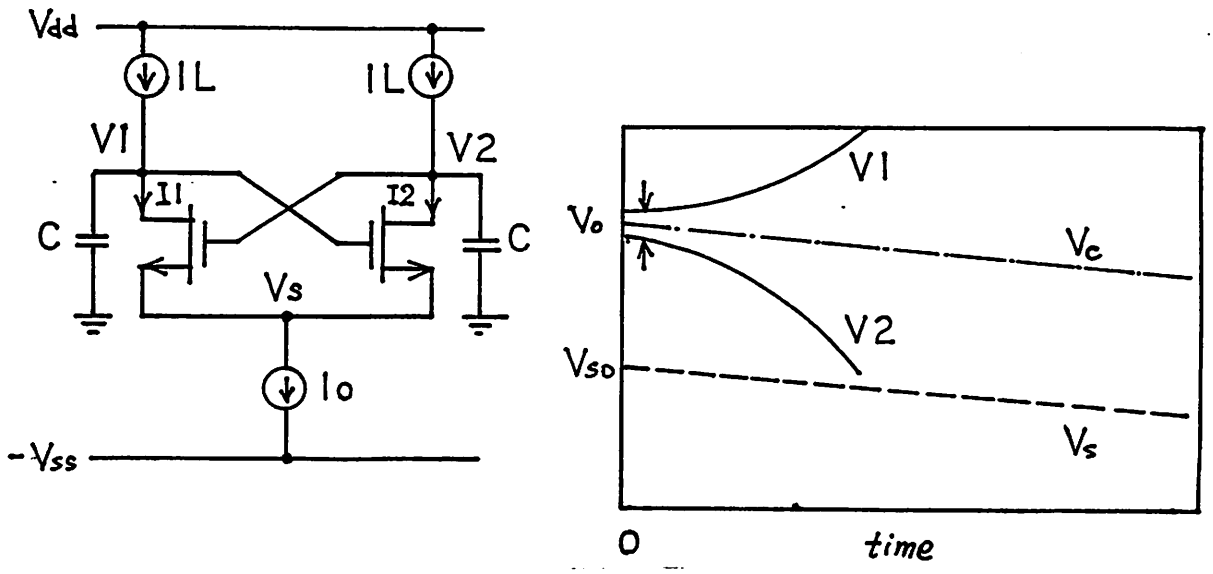


Fig. A-2 Transient Response of a Latch with Current Source Loads.

Appendix B Latch Sensitivity

(1) Latch without Load

The analytical calculation for the sensitivity of the latch (cross coupled MOS FETs), without loads has been reported in [6]. Here, a brief review of that calculation will be presented. Fig. B-1 shows the circuit of the basic regenerative latch. The same circuit with a number of reset switches and transfer gates is used widely in DRAM sense amplifiers. If the parameters of both Trs and the capacitors are perfectly matched, as in Appendix A, the theoretical sensitivity will be infinitely small. But, as shown in the figure, these parameters are not completely matched, so that to amplify the input signal in the proper direction, a certain amount of input signal S must be supplied. This is the definition of the sensitivity S. For the worst case, lets assume the following conditions;

(1) Initial Condition.

V1(0)=Vo

V2(0)=Vo+S

(2) Parameters.

$$C_1 \geqslant C_2,\ \beta_1 \leqslant \beta_2,\ Vth\,1 \geqslant Vth\,2$$

Assuming that both transistors are operating in the saturation region, the change of the node voltages V1 and V2, during a small time interval Δt can be written as;

$$\Delta V1 = \frac{\beta_1}{2C_1}(V2(0)-Vth\,1-Vs)^2\Delta t \qquad \text{(B-1)}$$

$$\Delta V2 = \frac{\beta_2}{2C_2}(V1(0)-Vth\,2-Vs)^2\Delta t \qquad \text{(B-2)}$$

And similarly to the derivation in Appendix A, the transient response of the common source voltage, Vs(t), is assumed as:

$$Vs(t) = Vso - \alpha t \qquad \text{(B-3)}$$

From Eq.(B-1) and (B-3), the time t1 when M1 turns on is:

$$t1 = \frac{1}{\alpha}(Vso - Vo - S + Vth1) \tag{B-4}$$

Similarly, the time t2 when M2 turns on is:

$$t2 = \frac{1}{\alpha}(Vso - Vo + Vth2) \tag{B-5}$$

After the turn on of M1, the voltage V1 begins to decrease. However, for a critical condition where t1 $\approx$ t2, V1 can be assumed to stay constant until M2 turns on. In this way, the estimation for t2 was done similarly to t1.

The sensitivity can be considered as the minimum input voltage S, which can increase the difference | V1-V2 |, after both transistors M1 and M2 turn on. In the following, the change of $\Delta V1$ and $\Delta V2$ after t2 will be calculated.

The node voltage V1(t) at the time t2 can be calculated by integrating Eq.(B-1) between t1 and t2. Here, t1 and t2 are substituted by Eq's (B-4) and (B-5).

$$V1(t2) = -\frac{\beta_1}{6C_1\alpha}(S + (Vth2 - Vth1))^3 + Vo \tag{B-6}$$

And V2 at t2 is:

$$V2(t2) = Vo + S \tag{B-7}$$

The voltage change $\Delta V1$ between t2 and t2 + Δt is:

$$\begin{aligned}\Delta V1 &\approx \frac{\beta_1}{2C_1}(V2(t2) - Vth1 - Vso + \alpha(t2 + \Delta t))^2 \Delta t \\ &= \frac{\beta_1}{2C_1}(S + \alpha\Delta t + (Vth2 - Vth1))^2 \Delta t\end{aligned} \tag{B-8}$$

Here, the change of V2 has been neglected compared to the rapid change $\alpha\Delta t$ of the common source voltage Vs.

Similarly, for the change in V2(t) after t2:

$$\begin{aligned}\Delta V2 &\approx \frac{\beta_2}{2C_2}(V1(t2) - Vth2 - Vs)^2 \Delta t \\ &\approx \frac{\beta_2}{2C_2}\left[\alpha\Delta t - \frac{\beta_1}{6C_1\alpha}(S + (Vth2 - Vth1))^3\right]^2 \Delta t\end{aligned}$$

$$\approx \frac{\beta_2}{2C2}(\alpha\Delta t - \Delta V1_{t1 \to t2})^2 \Delta t \qquad \text{(B-9)}$$

If the change $\Delta V1$ during t1 to t2 is much smaller than the change in the source voltage $\alpha\Delta t$, the equation above can be approximated as follows:

$$\Delta V2 \approx \frac{\beta_2}{2C2}\alpha^2 \Delta t^3 \qquad \text{(B-10)}$$

For the accurate signal amplification, the following relation should be satisfied.

$$\Delta V1 \geqslant \Delta V2$$

Then from Eq.(B-8) and (B-9), the sensitivity S can be derived as:

$$S \geqslant \left(\sqrt{\frac{\overline{C1}}{\overline{C2}}\frac{\overline{\beta 2}}{\overline{\beta 1}}} - 1\right)(\alpha\Delta t) + (Vth1 - Vth2) \qquad \text{(B-11)}$$

(2) Latch with Current Source Loads

The introduction of current source loads to the cross coupled transistor pair brings about a large offset, and consequently the sensitivity is degraded. Although this is not refered in [6], it will be calculated here as a comparison to the previous result without loads.

Fig B-2 shows the basic circuit. Here, in order to assume the worst case, the following assumption is added to those in the previous calculation.

$$IL1 \geqslant IL2$$

The node voltages satisfy the following differential equations.

$$IL1 - C_1\frac{dV_1}{dt} = \frac{\beta_1}{2}(V2(t) - Vs - Vth1)^2 \qquad \text{(B-12)}$$

$$IL2 - C_2\frac{dV_2}{dt} = \frac{\beta_2}{2}(V1(t) - Vs - Vth2)^2 \qquad \text{(B-13)}$$

Before M1 and M2 turn on, current sources charge the load capacitors C_1 and C_2, increasing V1 and V2 as follows:

$$V1(t) = \frac{IL1}{C_1} + Vo \tag{B-14}$$

$$V2(t) = \frac{IL2}{C_2} + Vo + S \tag{B-15}$$

Assuming that the common source voltage follows Eq.(B-3), the time when M1 turns on can be calculated from Eq.(B-12) and (B-15) as:

$$t1 = \frac{Vso - Vo - S + Vth1}{\alpha + \frac{IL2}{C_2}} \tag{B-16}$$

And the time when M2 turns on can be calculated similarly as:

$$t2 = \frac{Vso - Vo + Vth1}{\alpha + \frac{IL1}{C_1}} \tag{B-17}$$

In order to evaluate the sensitivity S for this case, we'll only assume the degradation of S due to the mis-match in IL/C and Vth. Then, in order to amplify the input signal S in the proper direction, the following condition will be sufficient.

$$t1 \leqslant t2$$

M1 should be turned on first. Thus, comparing Eq.(B-16) and (B-17),the sensitivity S can be calculated as:

$$S \geqslant \frac{\left(\frac{IL1}{C_1} - \frac{IL2}{C_2}\right)}{\left(\alpha + \frac{IL1}{C_1}\right)}(Vso - Vo + Vth2) - \Delta Vth \tag{B-18}$$

Here, Vth1= Vth2+ ΔVth.

For the latch without current source loads, the sensitivity was proportionally increasing with the square root of the errors of $\frac{C_1}{C_2}$ and $\frac{\beta 2}{\beta 1}$. But here, it is proportional to the error of IL/C directly. So, more care should be paid for this circuit. And if possible, it is better to cut off the loads for the early stage of operation, and after a sufficient amplification has been attained, connect the loads to drive the next stages. This method is also applied in DRAM sensing amplifiers.

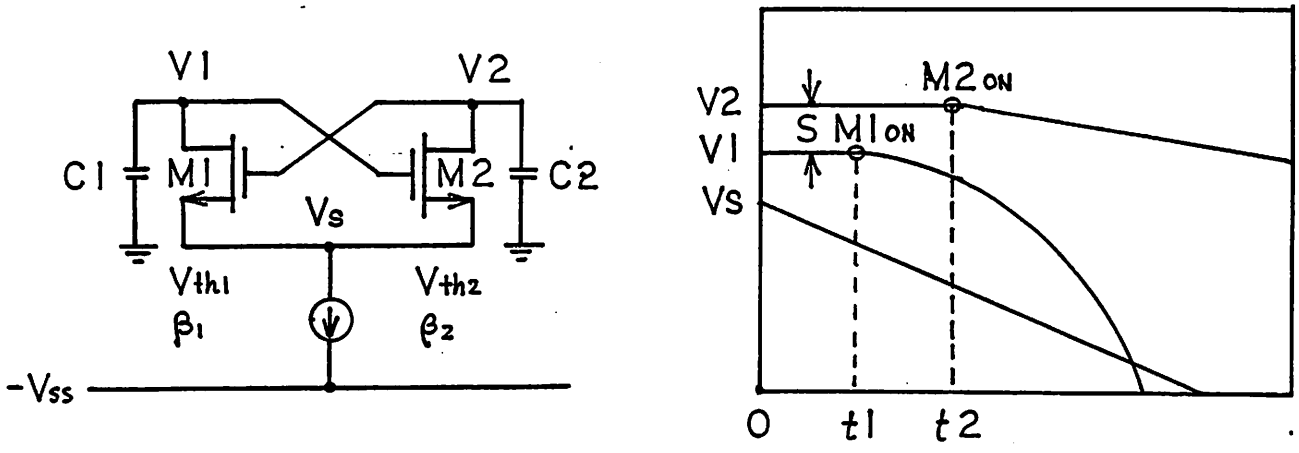


Fig. B-1 Sensitivity of a Latch without Loads.

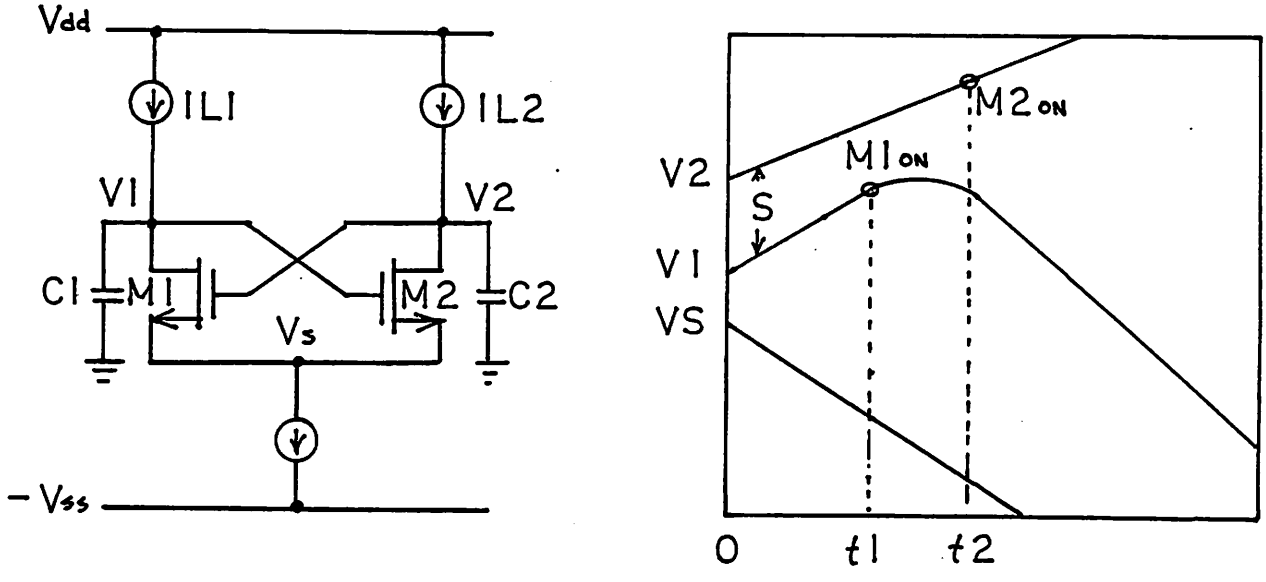


Fig. B-2 Sensitivity of a Latch with Current Source Loads.

Appendix C Transient Response of the Multi Stage Amplifier

(1) Small Signal Approximation

If we assume a single pole amplifier with a DC gain of A_0, and cutoff frequency of ω_c, the transfer characteristic of a single stage is:

$$A(\omega) = \frac{A_0}{1+j\frac{\omega}{\omega_c}} \tag{C-1}$$

The cut off frequency (-3dB frequency) of the N stage amplifier is ω_m, and the gain is:

$$\left| \left(\frac{1}{1+j\frac{\omega_m}{\omega_c}} \right)^N \right| = 10^{-\frac{3}{20}} = \frac{1}{\sqrt{2}} \tag{C-2}$$

Solving for ω_m.

$$\omega_m = \sqrt{2^{\frac{1}{N}}-1}\ \omega_c \tag{C-3}$$

The Gain Band Width (GBW is:

$$GBW = \sqrt{2^{\frac{1}{N}}-1}\ \omega_c\ A_0{}^N \tag{C-4}$$

When the number of stages N is increased, the cutoff frequency decreases, but the gain increases. ω_m decreases monotonically, and shows no significant change over the value of N=15. Here the ω_m is almost 0.22 ω_c.

(2) Large Signal Transient Response

The transfer function for each stage, assuming a single pole, is

$$H_0(s) = \frac{A_0\,\omega_c}{s+\omega_c} \tag{C-5}$$

The transfer function for the multi-stage amplifier(N stages) is

$$H(s) = \frac{(A_0 \omega_c)^N}{(s+\omega_c)^N} \tag{C-6}$$

For a step input Vin(t) = Vin u(t), the output Vout of the multi stage amplifier will be;

$$Vout(s) = H(s)\, Vin(s) = \frac{(A_0 \omega_c)^N Vin}{(s+\omega_c)^N s} \tag{C-7}$$

The inverse Laplace transform can be performed as follows.

$$Vout(t) = L^{-1}(\,Vout(s)) \equiv \frac{1}{2\pi j}\int_{\gamma-j\infty}^{\gamma+j\infty} \frac{(A_0\omega_c)^N Vin}{(s+\omega_c)^N s} e^{st}\, ds = R_{\omega_c} + R_0 \tag{C-8}$$

Here, R_{ω_c} and R_0 are the residuals on poles - ω_c and 0 respectively. Those residuals can be calculated as follows.

$$R_{\omega_c} \equiv \frac{1}{(N-1)!} \lim_{s \to -\omega_c} \frac{d^{N-1}}{ds^{N-1}} \left[(s+\omega_c)^N \frac{(A_0\omega_c)^N Vin}{(s+\omega_c)^N s} e^{st} \right]$$

$$= \frac{1}{(N-1)!} (A_0\omega_c)^N Vin \lim_{s \to -\omega_c} \frac{d^{N-1}}{ds^{N-1}} \left[\frac{e^{st}}{s} \right] \tag{C-9}$$

Here the differential can be calculated by first making a Taylor Expansion of

$$\frac{e^{st}}{s} = \sum_{k=0}^{\infty} \frac{t^k s^{k-1}}{k!} \tag{C-10}$$

And then, the differential in (C-9) is calculated as.

$$\frac{d^N}{ds^N}\left[\frac{e^{st}}{s}\right] = \sum_{k=0}^{N} \frac{{}_{k-1}P_N}{k!} t^k s^{k-N-1} = \sum_{k=0}^{N} (-1)^k \frac{n!}{(N-k)!} \frac{t^{N-k}}{s^{k+1}} e^{st} \tag{C-11}$$

Substituting (C-11) to (C-9), we get

$$R_{\omega_c} = -A_0^N \; Vin \; e^{-\omega_c t} \sum_{k=0}^{N-1} \frac{(\omega_c t)^K}{k!} \tag{C-12}$$

The other residue can be easily calculated as,

$$R_0 \equiv \lim_{s \to 0} \frac{d^{N-1}}{ds^{N-1}} \left[s \frac{(A_0 \omega_c)^N Vin}{(s+\omega_c)^N s} e^{st} \right] = A_0{}^N Vin \tag{C-13}$$

Then the output voltage *Vout*(t) is calculated as,

$$Vout(t) = A_0^N Vin \left[1 - e^{\omega_c t} \sum_{k=0}^{N-1} \frac{(\omega_c t)^K}{k!} \right] \tag{C-14}$$

For a single stage of N=1, the familiar result (C-15) is obtained from (C-14).

$$Vout(t) = A_0(1-e^{-\omega_c t}) \tag{C-15}$$

For 2 stage amplifier,

$$Vout(t) = A_0^2 (1-e^{-\omega_c t}(1+\omega_c t)) \tag{C-16}$$

And for 3 stage amplifier,

$$Vout(t) = A_0^3 (1-e^{-\omega_c t}(1+\omega_c t + \frac{(\omega_c t)^2}{2})) \tag{C-17}$$

The number of stages N appears as the exponent in the gain A_0. and as a power series of $\omega_c t$ after the exponential term. The former increase the response speed to achieve a certain voltage, while the latter decrease the speed. It is interesting that at the limiting case of N=∞, the power series converge to $e^{\omega_c t}$, and this cancels the $e^{-\omega_c t}$ term completely. The result of (C-14) can be verified by a straightforward calculation of the multistage amplifier. But it is difficult to perform the calculation for N more than 4 stages.

(3) Acquisition Time Estimation (I)

Substituting Tacq for t and Vreq for Vout(t) in Eq.(C-14), and then solving for the acquisition time Tacq, we get:

$$T_{acq} = -\frac{1}{\omega_c} ln\left(1 - \frac{V_{req}}{A_0^N V_{in}}\right) + \frac{1}{\omega_c} \ln\left(\sum_{K=0}^{N-1} \frac{(\omega_c T_{acq})^k}{k!}\right) \qquad \text{(C-18)}$$

The first term in the right hand side is analogous to the right hand side of Eq. (3.5.5-3). The second term is the effect of the phase shift in the multi-stage preamplifier. In order to make the dependence of T_{acq} on the GBW and Vreq/Vin much clearer, the following assumptions have been made.

$$V_{req} << A_0^N V_{in}$$
$$\omega_c T_{acq} << 1$$

These mean sufficient gain and short acquisition time compared to $\frac{1}{\omega_c}$. Then Eq. (C-18) can be approximated as follows;

$$T_{acq} \approx \frac{V_{req}}{A_0^N \omega_c V_{in}} + \frac{1}{\omega_c} \ln\left(1 + \omega_c T_{acq} + \frac{(\omega_c T_{acq})^2}{2}\right)$$

$$\approx \frac{V_{req}}{A_0^N \omega_c V_{in}} + \frac{1}{\omega_c}\left(\omega_c T_{acq} + \frac{(\omega_c T_{acq})^2}{2} - \frac{1}{2}\left(\omega_c T_{acq} + \frac{(\omega_c T_{acq})^2}{2}\right)^2 + \frac{1}{3}\left(\omega_c T_{acq} + \frac{(\omega_c T_{acq})^2}{2}\right)^3\right)$$

$$\approx \frac{V_{req}}{A_0^N \omega_c V_{in}} + \frac{1}{\omega_c}\left(\omega_c T_{acq} - \frac{1}{6}(\omega_c T_{acq})^3\right)$$

And solving for Tacq.

$$T_{acq} = \frac{1}{\omega_c}\left(\frac{6V_{req}}{A_0^N V_{in}}\right)^{\frac{1}{3}} \qquad \text{(C-20)}$$

(4) Acquisition Time (II)

Another approximation which is derived in a different way has been reported. [5] Here, the outline of that calculation is reviewed. The inverse Laplace transform of Eq.(C-

7) can be also expressed in the following form:

$$V_{out}(t) = V_{in}(\omega_c A_0)^N \int_0^t \frac{1}{(n-1)!} t^{n-1} e^{-\omega_c t}\, dt \qquad \text{(C-21)}$$

If t is much smaller than $1/\omega_c$, then the exponential term can be approximated to be 1. But, as a result, this is not so bad an approximation. Then, Eq.(C-21) can be calculated easily to be:

$$V_{out}(t) = V_{in}(\omega_c A_0 t)^N / n!$$

Substituting T_{acq} for t, and Vreq for Vout(t), the following conclusion can be derived:

$$T_{acq} = \frac{1}{GBW}\left(\frac{V_{req} N!}{V_{in}}\right)^{\frac{1}{N}} \qquad \text{(C-22)}$$

Here GBW= $\omega_c A_0$ is the gain bandwidth of a single stage.

Appendix D Characteristics of Fully Differential Amplifiers.

1. Amplifier with pMOS Loads in Diode Connection

1.1. Differential Gain

Fig.D-1(A) shows the basic configuration of the fully differential amplifier with pMOS loads in diode connection. Fig. F-1(B) is the AC equivalent circuit for the differential half circuit. For simplicity neither body bias effect nor short channel effects will be included here. From the current conservation rule,

$$i = -g_{m3}V_{out} = sC_L V_{out} + g_{m1}V_{in}$$

Solving this equation for the differential gain, A_d =Vout/Vin:

$$A_d(s) = -\frac{g_{m1}/\ g_{m3}}{s\frac{C_L}{g_{m3}} + 1} \qquad \text{(D-1)}$$

From this result, we get the DC differential gain of $\frac{g_{m1}}{g_{m3}}$, and the cut off frequency ω_c *of* $\frac{g_{m3}}{C_L}$.

1.2. Common Mode Gain

The common mode gain A_c can be derived using Fig.D-1(C). Here the resistance Rs is the output resistance of the current source M5.

$$i = -g_{m3}V_{out} = sC_L V_{out} + g_{m1}(V_{in} - V_S) = \frac{V_S}{2R_S}$$

Solving this equation for the common mode gain Ac=Vout/Vin.

$$A_c(s) = -\frac{1}{2R_S g_{m1} + 1}A_d(s) \qquad \text{(D-2)}$$

The common mode rejection ratio is $2R_S g_{m1} + 1$ over all frequency, and the cutoff frequency is same as that of the differential mode half circuit.

1.3. PSRR (Power Supply Rejection Ratio)

Next, the PSRR (Power Supply Rejection Ratio) will be considered. Fig.D-1(D) shows the AC equivalent circuit with an AC input of Vd from the Vdd power supply. The current continuity can be satisfied by the following equation:

$$g_{m3}(V_d - V_{out}) = g_{m1}(0 - V_s) + \frac{V_{out} - V_s}{r_{o1}} = \frac{V_s}{2R_s}$$

Here, r_{o1} is the output resistance of M1. Solving this for the gain of Add=Vout/Vd,

$$Add \approx \frac{1}{1 - \frac{1}{(g_{m1}r_{o1})(g_{m3}r_{o1})}} \approx 1 \qquad \text{(D-3)}$$

This large gain of 1 is the result of the diode connection of M3 between the Vdd line and the output terminal. This large signal is transmitted to the next stage as a common mode signal. So, it will be necessary to drive into an amplifier having a high CMRR.

Fig.D-1(E) shows the AC equivalent circuit with an AC input of Vi from the Vss power supply. This circuit satisfies the following equation:

$$-g_{m3}V_{out} = -g_{m1}V_s = \frac{V_s - V_i}{2R_s}$$

Solving this for the gain of Ass=Vout/Vi,

$$Ass \approx \frac{1}{2R_s g_{m3}} \qquad \text{(D-4)}$$

This value is small enough to prevent the noise from the Vss power line being coupled to the output.

1.4. Dynamic Range

Next, the dynamic range of this amplifier will be calculated. Fig.D-1(F) shows the amplifier under saturation. Here, M2 is completely cut off, and the bias current Io flows through M1 and M3. Thus, the highest output voltage Vh is Vdd-VthP, and the lowest voltage VL can be determined from M3 as:

$$V_L = V_{dd} - V_{thP} - 2\sqrt{\frac{I_0}{\beta_3}} \qquad \text{(D-5)}$$

Here, VthP is the threshold voltage of M3, and β_3 is the value of KP*W/L for M3.

When the circuit is in a balanced state, a current Io is flowing on both sides, so that the output voltage Vm is:

$$V_m = V_{dd} - V_{thP} - \sqrt{2\frac{I_0}{\beta_3}} \qquad \text{(D-6)}$$

1.5. Closed Loop Response

In appendix H,the transient response of the reset in the linear operation region has been calculated. In the actual case, we have to consider the large signal response in the nonlinear operation region. Fig. F-1(D-1) shows the circuit with the loop closed during the reset. Here, the MOS switch used to close the loop is modeled by an ideal resistor R. The input and output nodes are set in their maximum or minimum value as the worst case for a reset. (The amplifier is saturated.)

Precise calculation by SPICE shows that, the reset is performed in two phases. In the first phase, the charge on the capacitors is redistributed quickly through the resistor R. There, the time constant is simply:

$$T_1 = (C_1 // C_2)R \qquad \text{(D-7)}$$

Here, // describes the series capacitance. For the second phase, the input and output voltage are the same, and converge together to the final value. The transient response for this phase will be calculated using Fig.D-1(D-2). The current continuity at each output node can be expressed as follows:

$$\frac{\beta_L}{2}(V_{dd} - V_1 - V_{thP})^2 = (C_1 + C_2)\frac{dV_1}{dt} + \frac{\beta_D}{2}(V_1 - V_S - V_{thN})^2 \qquad \text{(D-8)}$$

$$\frac{\beta_L}{2}(V_{dd} - V_2 - V_{thP})^2 = (C_1 + C_2)\frac{dV_2}{dt} + \frac{\beta_D}{2}(V_2 - V_S - V_{thN})^2 \qquad \text{(D-9)}$$

Here, β_L and β_D are MOS current coefficients for the load (M3,M4) and driver (M1, M2) transistors respectively.

By subtracting Eq.(D-9) from Eq.(D-8), and taking account the following equations:

$$V_d = V_1 - V_2$$
$$V_c = \frac{(V_1 + V_2)}{2}$$

the following differential equation can be derived:

$$\frac{dV_d}{dt} = -\frac{1}{C_1+C_2}\left\{\beta_L(V_{dd}-V_c-V_{thP}) + \beta_D(V_c-V_S-V_{thN})\right\}V_D$$

This differential equation can be solved easily.

$$V_D = V_{D0}\, e^{\frac{-t}{T2}}$$

Here, the time constant $T2$ is:

$$T2 = \frac{C_1 + C_2}{g_{mL} + g_{mD}} \qquad \text{(D-10)}$$
$$g_{mL} = \beta_L(V_{dd}-V_c-V_{thP})$$
$$g_{mD} = \beta_D(V_c-V_S-V_{thN})$$

g_{mL} and g_{mD} are the transconductance of the load transistor and driver transistor, respectively.

2. Amplifier with Diode and Current Source Loads

2.1. Differential Gain

Fig.D-2(A) shows the basic configuration of the fully differential amplifier with pMOS loads in diode connection and current-source loads in parallel. Fig. F-2(B) is the AC equivalent circuit for the differential mode input. For simplicity neither the body-bias effect nor the short-channel effect will be included here. From current conservation rule.

$$i = -g_{m3}V_{out}\frac{-V_{out}}{R_L} = sC_L V_{out} + g_{m1}V_{in}$$

Here R_L is the output resistance of the current source load and can be neglected, compared to the small impedance of m3, $\frac{1}{g_{m3}}$. Solving this equation for the differential gain Ad=Vout/Vin;

$$A_d(s) = -\frac{g_{m1}/g_{m3}}{s\frac{C_L}{g_{m3}} + 1} \qquad \text{(D-11)}$$

From this result, we get the DC differential gain of $\frac{g_{m1}}{g_{m3}}$, and the cutoff frequency ω_c *of* $\frac{g_{m3}}{C_L}$. What is different compared to the previous circuit is that the current flowing through M1 and M3 can be adjusted independently. No large ratio of W1/W3 is required to get high gain.

2.2. Common Mode Gain

The common mode gain Ac can be derived using Fig.D-2(C). Here the resistance Rs is the output resistance of the current source M5.

$$i = -g_{m3}V_{out} = sC_L V_{out} + g_{m1}(V_{in} - V_S) = \frac{V_S}{2R_S}$$

Solving this equation for the common mode gain Ac=Vout/Vin.

$$A_c(s) = -\frac{1}{2R_S g_{m1} + 1}A_d(s) \qquad \text{(D-12)}$$

The common mode rejection ratio is $2R_S g_{m1} + 1$ over all frequencies, and the cutoff frequency is same to that of Ad.

2.3. PSRR

Next, the PSRR (Power Supply Rejection Ratio) will be considered. Fig.D-2(D) shows the AC equivalent circuit with an AC input of Vd from the Vdd power supply. The current continuity can be satisfied by the following equation:

$$g_{m3}(V_d - V_{out}) = g_{m1}(0 - V_s) + \frac{V_{out} - V_s}{r_{o1}} = \frac{V_s}{2R_s}$$

Here, r_{o1} is the output resistance of M1. Solving this for the gain Add=Vout/Vd,

$$Add \approx \frac{1}{1 - \frac{1}{(g_{m1}r_{o1})(g_{m3}r_{o1})}} \approx 1 \qquad \text{(D-13)}$$

This large gain of 1 is the result of m3 being diode connected between the Vdd line and the output terminal. This large signal is transmitted to the next stage as a common mode

signal. So. it will be necessary to receive that with an amplifier of high CMRR.

Fig.D-2(E) shows the AC equivalent circuit with an AC input of Vi from the Vss power supply. This circuit satisfies the following equation.

$$-g_{m3}V_{out} = -g_{m1}V_s = \frac{V_s - V_i}{2R_s}$$

Solving this for the gain. Ass=Vout/Vi.

$$Ass \approx \frac{1}{2R_s g_{m3}} \qquad \text{(D-14)}$$

This value is small enough to prevent coupling noise from the Vss power line to the output.

2.4. Dynamic Range

Next. the dynamic range of this amplifier will be calculated. Fig.D-2(F) shows the amplifier in a saturated state. Here. M2 is completely cutoff. and the bias current Io flows through M1 and M3. Thus. the highest output voltage Vh is Vdd-VthP. and the lowest voltage VL can be determined from M3 as:

$$V_L = V_{dd} - V_{thP} - 2\sqrt{\frac{(I_0 - I_{b/2})}{\beta_3}} \qquad \text{(D-15)}$$

Here. VthP is the threshold voltage of M3. β_3 is the value of KP*W/L for M3 and I_b is the bias current flowing through the current sources M5 and M6.

When the circuit is in a balanced state. current Io is flowing on both sides. so that the output voltage Vm is:

$$V_m = V_{dd} - V_{thP} - \sqrt{2\frac{(I_0 - I_{b/2})}{\beta_3}} \qquad \text{(D-16)}$$

2.5. Closed Loop Response

For the reset time calculation in the nonlinear mode. the same equations Eq.(D-7) to Eq.(D-10) can be derived. if the bias current in both sides has the same value of I_b.

3. Amplifier with Current Source Loads and a Common Mode Feedback (CMFB)

Fig.D-3(A) shows one possible configuration of the fully differential amplifier with current source loads and a CMFB circuit. THe CMFB circuit consists of a common mode signal extractor circuit, which average the signal of the output nodes, and an amplifier of gain A (usually less than 1). The purpose of this circuit is the reduction of the common mode gain, which will be explained below, and the stabilization of the DC level of the output nodes.

3.1. Differential Mode Gain

Fig. F-3(B) is the AC equivalent circuit for the differential mode input. For simplicity neither body bias effect nor short channel effect will be included here. Because the CMFB circuit doesn't pick up a differential mode signal the CMFB circuit does not appear in this figure. From KCL,

$$i = \frac{-V_{out}}{(r_{o1} // r_{o3})} = sC_L V_{out} + g_{m1} V_{in}$$

Here, r_{o1} and r_{o3} are the output resistance of transistor M1 and M3 respectively. Solving this equation for the differential gain Ad=Vout/Vin;

$$A_d(s) = -\frac{g_{m1}(r_{o1} // r_{o3})}{sC_L(r_{o1} // r_{o3}) + 1} \qquad \text{(D-21)}$$

From this result, we get the DC differential gain of $g_{m1}(r_{o1} // r_{o3})$, and the cutoff frequency ω_c of $\frac{1}{C_L(r_{o1} // r_{o3})}$.

3.2. Common Mode Gain

At first, the common mode gain Ac without CMFB will be derived using Fig.D-3(C). Here the resistance Rs is the output resistance of the current source M5.

$$i = -\frac{V_{out}}{r_{o3}} = g_{m1}(V_{in} - V_S) + \frac{(V_{out} - V_S)}{r_{o1}} = \frac{V_S}{2R_S}$$

Solving this equation for the common mode gain Ac=Vout/Vin,

$$A_c = -\frac{r_{o3}}{2}R_S$$

This is such a large value that a common mode voltage may saturate the amplifier. There is another problem with this circuit. The DC level of V_{out} changes drastically, even with a slight change in the drain conductance.

To solve these problems, the common mode feedback circuit (CMFB) has been introduced. Fig. F-3(D) shows the AC equivalent circuit using this CMFB, for the common mode input. The output voltage satisfies the following equation:

$$-\frac{V_{out}}{r_{o3}} = g_{m1}(V_{in} - V_S) = \frac{V_S}{2R_S} + A\frac{g_{m5}}{2}V_{out}$$

Solving this equations, the common mode gain is:

$$A_c = \frac{1}{Ag_{m5}R_S} \qquad \text{(D-32)}$$

The common mode gain can be reduced enough in this way.

3.3. PSRR

Next, the PSRR (Power Supply Rejection Ratio) will be considered. Fig.D-3(E) shows the AC equivalent circuit with an AC input of Vd from the Vdd power supply. The current continuity can be satisfied by the following equation:

$$\frac{(V_d - V_{out})}{r_{o3}} = g_{m1}(0 - V_s) = \frac{V_s}{2R_s} + \frac{g_{m5}}{2}AV_{out}$$

Solving this for the gain of Add=Vout/Vd,

$$Add \approx \frac{2}{Ag_{m5}r_{o3}} \qquad \text{(D-33)}$$

Fig.D-3(F) shows the AC equivalent circuit with an AC input of Vi from the Vss power supply. This circuit satisfy the following equation.

$$-\frac{V_{out}}{r_{o3}} = -g_{m1}V_s = \frac{V_s - V_i}{2R_S} + \frac{g_{m5}}{2}(AV_{out} - V_i)$$

Solving this for the gain of Ass=Vout/Vi,

$$Ass \approx \frac{1}{A} \qquad \text{(D-34)}$$

Because the gain A is very close to 1, this value is not so small, and much care must be taken to prevent the noise from Vss line. line.

3.4. Dynamic Range

Next, the dynamic range of this amplifier will be calculated. Fig.D-3(G) shows the amplifier in a saturated state. Here the CMFB circuit consists of three transistors M6,M7 and M8. For the common mode signal it works as a source follower , and for a differential mode it has no gain. (But, detail calculation can show a certain gain for the large swing differential mode signal.) Here, M2 is completely cut off, and the bias current Io flows through M1 and M3. In the CMFB circuit, all the bias current 2Ib flows through M7. Thus, the highest output voltage Vh is Vdd, and the lowest voltage VL can be determined from M3 and M7 as:

$$V_L = -V_{ss} + V_{thN} + 2\sqrt{\frac{I_0}{\beta_5}} + V_{thN} + 2\sqrt{\frac{I_b}{\beta_7}} \qquad \text{(D-35)}$$

Here, VthN is the threshold voltage of M5 and M7. β_5 and β_7 is the value of KP*W/L for M5 and M7, respectively.

When the circuit is in a balanced state, current Io is flowing on both sides, so that the output voltage Vm is:

$$V_m = -V_{ss} + V_{thN} + 2\sqrt{\frac{I_0}{\beta_5}} + V_{thN} + \sqrt{2\frac{I_b}{\beta_7}} \qquad \text{(D-36)}$$

The frequency response of this CMFB circuit will be calculated using Fig. F-3(H), for the common mode signal. From the figure.

$$-sC_L - \frac{V_{out}}{r_{o3}} = g_{m1}(V_{in} - V_S) = \frac{g_{m5}}{2}V_{out} + \frac{V_S}{2R_S}$$

The common mode gain can be calculated as:

$$A_d(s) = \frac{1}{R_S(2sC_L + g_{m5})} \qquad \text{(D-37)}$$

The -3dB frequency of $\omega_{cc} = \frac{g_{m5}}{2C_L}$ is much higher than the cutoff frequency ω_c for the

differential mode input. So, the CMRR will become worse above this frequency. But as a preamplifier for tyhe comparator, and as long as the common mode gain is small enough, there should be no problem.

3.5. Closed Loop Response

The reset of this amplifier can be considered similarly to the previous circuits. The process can be divided in two phases. The first phase has the RC dominant time constant. Here, in Fig. F-3(I), the second phase is considered. The current continuity for each sides can be expressed as follows:

$$I_b = (C_1 + C_2)\frac{dV_1}{dt} + \frac{\beta_D}{2}(V_1 - V_S - V_{thN})^2 \qquad \text{(D-38)}$$

$$I_b = (C_1 + C_2)\frac{dV_2}{dt} + \frac{\beta_D}{2}(V_2 - V_S - V_{thN})^2 \qquad \text{(D-39)}$$

Here, β_D is the MOS current coefficient for the driver (M1, M2) transistors.

By subtracting Eq.(D-39) from Eq.(D-38), and taking account the following equations:

$$V_d = V_1 - V_2$$

$$V_c = \frac{(V_1 + V_2)}{2}$$

the following differential equation can be derived:

$$\frac{dV_d}{dt} = -\frac{1}{C_1 + C_2}\beta_D (V_c - V_S - V_{thN})V_d$$

This differential equation can be solved easily.

$$V_D = V_{D0}\, e^{\frac{-t}{T2}}$$

Here, the time constant $T2$ is:

$$T1 = \frac{C_1 + C_2}{g_{mD}} \qquad \text{(D-40)}$$

$$g_{mD} = \beta_D (V_c - V_S - V_{thN})$$

g_{mD} is the mutual conductance of the driver transistor.

4. Cascode Amplifier with pMOS Loads in Diode Connection.

Fig.D-4(A) shows the basic configuration of the fully differential cascode amplifier M1 to M4 with pMOS loads M5, M6 in diode connection and current loads M7, M8, to supply extra current to the driver transistors.

4.1. Differential Mode Gain

Fig. F-4(B) is the AC equivalent circuit for the differential mode input. For simplicity neither body bias effect nor short channel effect will be included here. From KCL:

$$-g_{m5}V_{out} = sC_L V_{out} - g_{m3}V_1$$
$$-g_{m3}V_1 = sC_P V_1 + g_{m1}V_{in}$$

Solving these equation for the differential gain Ad=Vout/Vin:

$$A_d(s) = -\frac{g_{m1}/\ g_{m5}}{(s\frac{C_L}{g_{m5}} + 1)(s\frac{C_P}{g_{m3}} + 1)} \qquad \text{(D-41)}$$

From this result, we get the DC differential gain of $\frac{g_{m1}}{g_{m5}}$, and two poles:

$p_1 = \frac{g_{m5}}{C_L}$.

$p_2 = \frac{g_{m3}}{C_P}$. The first one is the dominant pole. If $p_2 \gg p_1$, then the unity gain band width or the GBW is:

$\frac{g_{m1}}{C_L}$.

4.2. Differential Mode Gain

The common mode gain Ac can be derived using Fig.D-4(C). Here the resistance Rs is the output resistance of the current source M9.

$$-g_{m5}V_{out} = sC_L V_{out} - g_{m3}V_1$$
$$-g_{m3}V_1 = sC_P V_1 + g_{m1}(V_{in} - V_S)$$
$$g_{m1}(V_{in} - V_S) = \frac{V_S}{2R_S}$$

Solving these equation for the common mode gain Ac=Vout/Vin.

$$A_c(s) = -\frac{1}{2R_S g_{m1} + 1} A_d(s) \qquad \text{(D-42)}$$

The common mode rejection ratio is $2R_S g_{m1} + 1$ over all frequency. and the poles are same to that of Ad.

4.3. PSRR

Next. the PSRR (Power Supply Rejection Ratio) will be considered. Fig.D-4(D) shows the AC equivalent circuit with an AC input of Vd from the Vdd power supply. The current continuity can be satisfied by the following equation;

$$g_{m5}(V_d - V_{out}) = g_{m3}(0 - V_1) + \frac{V_{out} - V_1}{r_{o3}} = g_{m1}(0 - V_s) + \frac{V_{out} - V_s}{r_{o1}} = \frac{V_s}{2R_s}$$

Here, r_{o1} and r_{o3} are the output resistance of M1 and M3, respectively. Solving this for the gain of Add=Vout/Vd.

$$Add \approx \frac{1}{1 + \frac{1}{(g_{m1}r_{o1})(g_{m3}r_{o3})2R_S g_{m5}}} \approx 1 \qquad \text{(D-3)}$$

This large gain of 1 is the result of the diode connection of M5 between the Vdd line and the output terminal. This large signal is transmitted to the next stage as a common mode signal. So, it will be necessary to receive that with an amplifier of high CMRR.

Fig.D-4(E) shows the AC equivalent circuit with an AC input of Vi from the Vss power supply. This circuit satisfy the following equation.

$$-g_{m5}V_{out} - g_{m3}V_1 = -g_{m1}V_s = \frac{V_s - V_i}{2R_s}$$

Solving this for the gain of Ass=Vout/Vi.

$$Ass \approx \frac{1}{2R_s g_{m5}} \qquad \text{(D-44)}$$

This value is small enough to prevent the noise from the Vss power line.

4.4. Dynamic Range

Next, the dynamic range of this amplifier will be calculated. Fig.D-4(F) shows the amplifier under saturation. Here, M2 is completely cut off, and the bias current Io flows

through M1, M3 and M5. Thus, the highest output voltage Vh is Vdd-VthP, and the lowest voltage VL can be determined from M5 as:

$$V_L = V_{dd} - V_{thP} - 2\sqrt{\frac{I_0 - \frac{I_b}{2}}{\beta_5}} \qquad \text{(D-45)}$$

Here, VthP is the threshold voltage of M5, and β_5 is the value of KP*W/L for M5. I_b is the bias current flowing through M7.

When the circuit is in a balanced state, current Io is flowing on both sides, so that the output voltage Vm is:

$$V_m = V_{dd} - V_{thP} - \sqrt{\frac{(2I_0 - I_b)}{\beta_5}} \qquad \text{(D-46)}$$

For the cascode amplifier, one more restriction must be considered. This is due to the extra voltage drop induced by the cascode transistor M3. To keep M1, M3 and M9 operating in the saturated region, V_L must satisfy the following condition:

$$V_L \geq -V_{ss} + 2\sqrt{\frac{I_0}{\beta_1}} + 2\sqrt{\frac{I_0}{\beta_3}} + 2\sqrt{\frac{I_0}{\beta_9}}$$

4.5. Closed Loop Response

In appendix F,the transient response of the reset in the linear operation region has been calculated. But in the actual case, we have to consider the large swing signal in the nonlinear operation region.

Precise calculation by SPICE shows that, the reset is performed in two phases. In the first phase, the charge of the capacitors are redistributed quickly through the resistor R. There, the time constant is simply:

$$T_1 = (C_L \,//\, C_{in})R \qquad \text{(D-47)}$$

Here, the MOS switch to close the loop is expressed by an ideal resistor R. For the second phase, the input and output voltage has no difference, and converge together to the final value. In this situation, the 2 pole amplifier is in closed loop configuration. Care must be

taken in its phase margin.

From Eq.(D-41), the phase shift $\Phi(\omega)$ can be expressed as:

$$\Phi(\omega) = -Tan^{-1}(\frac{C_L \omega}{g_{m5}}) - Tan^{-1}(\frac{C^P \omega}{g_{m3}})$$

Here, the unity gain frequency ω_1 is much larger than the dominant pole $\frac{g_{m5}}{C_L}$, but less than the nondominant pole $\frac{g_{m3}}{C_P}$.

Then, the equation above can be approximated as follows:

$$\Phi(\omega) = -\frac{\pi}{2} - Tan^{-1}(\frac{C^P \omega}{g_{m3}})$$

For the phase margin of 60° *at* ω_1.

$$\Phi(\omega_1) \geqslant -\pi + \frac{\pi}{3}$$

and:

$$A_d(\omega_1) \approx \frac{g_{m1}/\ g_{m5}}{\omega_1/\ p_1} = 1$$

$$\omega_1 = \frac{g_{m1}}{C_L} \quad (GBW)$$

Thus,

$$\frac{g_{m3}}{g_{m1}} \frac{C_P}{C_P} \geqslant \sqrt{3} \qquad \text{(D-48)}$$

Or,

$$\frac{nondominant\ \ pole\ p_2}{GBW} \geqslant \sqrt{3}$$

From the large signal analysis, and under the stable condition above, there are two time constants during the reset procedure in the nonlinear operation region. The fast time constant is:

$$\tau_f = \frac{C_P}{g_{m5}}$$

And the slow time constant is:

$$\tau_s = \frac{2(C_{out} + C_{in})}{g_{m5}}$$

The input impedance is purely capacitive, and can be calculated using Fig. F-4 (G). Here, the dominant factor of the Miller capacitance is considered. From the figure:

$$-g_{m3}V_1 = sC_{gd}(V_1 - V_{in}) + g_{m1}V_{in}$$
$$I_{in} = sC_{gd}(V_{in} - V_1)$$

Solving these equations for the input Miller capacitance:

$$C_{in} = \frac{I_{in}}{sV_{in}} = C_{gd}(1 + \frac{g_{m1}}{g_{m3}})$$

for $\omega \ll \frac{g_{m3}}{C_{gd}}$ which is usually the case.

5. Folded Cascode Amplifier with nMOS Loads in Diode Connection

Fig.D-5(A) shows the basic configuration of the fully differential cascode amplifier M1 to M4 with nMOS loads M5, M6 in diode connection and current sources M7, M8, to fold the signal path.

5.1. Differential Mode Gain

Fig. F-5(B) is the AC equivalent circuit for the differential mode input. For simplicity neither body bias effect nor short channel effect will be included here. From KCL:

$$g_{m3}V_1 = sC_L V_{out} + g_{m5}V_{out}$$
$$\frac{-V_1}{R_L} = sC_P V_1 + g_{m1}V_{in} + g_{m3}V_1$$

Solving these equation for the differential gain Ad=Vout/Vin, under the assumption of $R_L \gg g_{m3}^{-1}$:

$$A_d(s) = -\frac{g_{m1}/g_{m5}}{(s\frac{C_L}{g_{m5}} + 1)(s\frac{C_P}{g_{m3}} + 1)} \qquad \text{(D-51)}$$

From this result, we get the DC differential gain of $\frac{g_{m1}}{g_{m5}}$, and two poles

$p_1 = \frac{g_{m5}}{C_L}$.

$p_2 = \frac{g_{m3}}{C_P}$.

The first one is the dominant pole.

Assuming that $p_2 \gg p_1$, the unity gain bandwidth or GBW can be calculated as:

$\omega_1 = \frac{g_{m1}}{C_L}$.

5.2. Common Mode Gain

The common mode gain Ac can be derived using Fig.D-5(C). Here the resistance Rs is the output resistance of the current source M9.

$$g_{m3}V_1 = sC_L V_{out} + g_{m5}V_{out}$$

$$-g_{m3}V_1 - \frac{V_1}{R_L} = sC_P V_1 + g_{m1}(V_{in} - V_S)$$

$$g_{m1}(V_{in} - V_S) = \frac{V_S}{2R_S}$$

Solving these equation for the common mode gain Ac=Vout/Vin,

$$A_c(s) = -\frac{1}{2R_S g_{m1} + 1} A_d(s) \qquad \text{(D-52)}$$

The common mode rejection ratio is $2R_S g_{m1} + 1$ over all frequency, and the poles are same to that of Ad.

5.3. PSRR

Next, the PSRR (Power Supply Rejection Ratio) will be considered. Fig.D-5(D) shows the AC equivalent circuit with an AC input of Vd from the Vdd power supply. The current continuity can be satisfied by the following equation:

$$g_{m5}V_{out} = g_{m3}V_1 - \frac{V_{out} - V_1}{r_{o3}}$$

$$g_{m1}(0 - V_s) + \frac{V_1 - V_s}{r_{o1}} = \frac{V_s}{2R_s}$$

$$\frac{V_d - V_1}{R_L} = -g_{m1}V_S + \frac{V_1 - V_S}{r_{o1}} + g_{m3}V_1 + \frac{V_1 - V_{out}}{r_{o3}}$$

Here, r_{o1} and r_{o3} are the output resistance of M1 and M3, respectively. Solving this for the gain of Add=Vout/Vd,

$$Add \approx \frac{1}{R_L g_{m5}} \qquad \text{(D-53)}$$

This value is small enough to prevent the noise from the Vss power line.

Fig.D-5(E) shows the AC equivalent circuit with an AC input of Vi from the Vss power supply. This circuit satisfy the following equation.

$$g_{m5}(V_{out}-V_i) = g_{m3}V_1$$
$$\frac{V_s - V_i}{2R_s} = -g_{m1}V_S$$
$$g_{m3}V_1 - g_{m1}V_S = -\frac{V_1}{R_L}$$

Solving this for the gain of Ass=Vout/Vi,

$$Ass \approx 1 \qquad \text{(D-54)}$$

This large gain of 1 is the result of the diode connection of M5 between the Vss line and the output terminal. This large signal is transmitted to the next stage as a common mode signal. So, it will be necessary to receive that with an amplifier of high CMRR.

5.4. Dynamic Range

Next, the dynamic range of this amplifier will be calculated. Fig.D-5(F) shows the amplifier under saturation. Here, M1 draws all the available current I_b from M7. So, there is no current flow in the path of M3 and M5. On the other hand, the rest of the current $2I_0-I_b$ flows through M2, and consequently, $2(I_b-I_0)$ flows through M4 and M6. Thus, the lowest output voltage VL is -Vss+VthN, and the highest voltage Vh can be determined from M6 as:

$$V_h = -V_{ss} + 2\sqrt{\frac{I_b-I_0}{\beta_6}} + V_{thN} \qquad \text{(D-55)}$$

Here, V_{thN} is the threshold voltage of M6, and β_6 is the value of KP*W/L for M6. I_b is the bias current flowing through M8.

When the circuit is in a balanced state, current Io is flowing on both sides, so that the output voltage Vm is:

$$V_m = -V_{ss} + V_{thN} - \sqrt{\frac{2(I_b-I_0)}{\beta_6}} \qquad \text{(D-56)}$$

For the cascode amplifier, one more restriction must be considered. This is due to the extra voltage drop induced by the cascode transistor M4. To keep M4 and M8 operating in the saturated region, V_h must satisfy the following condition:

$$V_h \leqslant V_{dd} - \sqrt{2\frac{I_b}{\beta_8}} - 2\sqrt{\frac{I_b - I_0}{\beta_4}}$$

5.5. Closed Loop Response

In appendix F,the transient response of the reset in the linear operation region has been calculated. But in the actual case, we have to consider the large swing signal in the nonlinear operation region.

Precise calculation by SPICE shows that, the reset is performed in two phases. In the first phase, the charge of the capacitors are redistributed quickly through the resistor R. There, the time constant is simply;

$$T_1 = (C_L // C_{in})R \qquad \text{(D-57)}$$

Here, the MOS switch to close the loop is expressed by an ideal resistor R. For the second phase, the input and output voltage has no difference, and converge together to the final value. In this situation, the 2 pole amplifier is in closed loop configuration. Care must be taken in its phase margin.

The condition is similar to that of the non-folded cascode amplifier.

The input impedance is pure capacitive, and can be calculated using Fig. F-5 (G). Here, the dominant factor of the Miller capacitance is considered. From the figure;

$$-\frac{V_1}{R_L} = sC_{gd}(V_1 - V_{in}) + g_{m1}V_{in} + g_{m3}V_1$$

$$I_{in} = sC_{gd}(V_{in} - V_1)$$

Solving these equations for the input Miller capacitance:

$$C_{in} = \frac{I_{in}}{sV_{in}} = C_{gd}(1 + \frac{g_{m1}}{g_{m3}})$$

for $\omega \ll \frac{g_{m3}}{C_{gd}}$ that is usually the case.

To keep this value sufficiently small, g_{m3} must be sufficiently large compared to g_{m1}. To satisfy this condition, a folded cascode amplifier with extra current sources as shown in Fig. F-5(H) is preferred.

6. Amplifier with Diode Load, Current Source and Source Follower

To drive the large mirror capacitance of the next stage, the circuit configuration of Fig. 3.5.7-1 (F), that is the fully differential amplifier with source follower drivers can be considered. Because M3 and M1 drive a relatively small capacitance Cp, the band width can be improved by the ratio of CL/Cp.

The gain for the signal imput from the power supply line has increased for Vss as follows:

$$A_{ss} = \frac{g_{m10}}{g_{m7}} \tag{D-61}$$

This is due to the amplification by M10 as the driver and M7 as the load transistor. Generally its value is close to 1.

The output voltage is shifted down by the amount below:

$$\Delta V_{out} = -V_{thN} - \sqrt{\frac{2I_{d7}}{\beta_7}} \tag{D-62}$$

The transfer function of the source follower itself can be calculated as:

$$\frac{V_7}{V_{out}} = \frac{s\frac{C_{gb7}}{g_{m7}} + 1}{s\frac{C_L}{g_{m7}} + 1} \tag{D-63}$$

Here, C_{gb7} is the gate-base capacitance of M7. It has one high frequency zero and one low frequency pole. The gain of 1 persists until the frequency of the pole. So the GBW of this amplifier may be considered as :

$$GBW = \frac{g_{m7}}{C_L} \tag{D-64}$$

To get the advantage of the source follower, this value should be higher than the cutoff frequency of the main amp $\frac{g_{m3}}{C_P}$.

The input impedance of M7 is capacitive, and can be calculated as:

$$C_{in7} = C_{gb7}\frac{s(C_L - C_{gb7})}{sC_L - g_{m7}} \qquad \text{(D-65)}$$

For the frequency range much higher than $\frac{g_{m7}}{C_L}$ this value approaches to C_{gb7}. For the frequency less than $\frac{g_{m7}}{C_L}$, this value is less than C_{gb7}, but it is not capacitive.

The reset in this circuit should be performed by connecting the input terminal not to the output terminal, but to the intermediate node, the gate of M7. This should be done to prevent the extra phase shift of the source follower. This extra phase shift has the possibility to make the reset transition unstable.

7. Fully Differential Class AB Amplifier

Fig.D-7(A) shows the basic configuration of the fully differential class AB amplifier with diode and current source loads. Here, 2Vgs is the bias voltage source to drive the complementary transistor. When a large signal is applied to the input, the current flowing M1 ~ M4 change drastically, and consequently change the g_m of the transistors. This results in a high drivability of this circuit as a class AB amplifier. But, here only the small signal analysis will be performed. This is reasonable for the small signal amplification in the comparator.

There are a few ways to bias the input stage. Fig.D-7(B) shows one of those methods. Here, M5 and M7 under the constant bias current of I_b generates the bias voltage of $2V_{gs}$. The input signal is applied in the drains of M5 and M7. If the frequency of the signal is less than $\frac{g_m}{C}$, $V_1 \approx V_2 \approx V_{in}$.

The input impedance Z_{in} is:

$$Z_{in} = \frac{1}{2g_m} \frac{sC + g_m}{sC + \frac{1}{R}}$$

For frequency less than 1/RC, this takes the value of R/2, and for frequency over $\frac{g_m}{C}$, this approaches to $\frac{1}{2g_m}$, which is the parallel resistance of the bias transistors. This value is very small, and will be a heavy load to the previous stage.

Another method of biasing is shown in Fig.D-7(C). Here, the input signal is applied to the gates of M5 and M1. If $g_m R >> 1$, then:

$V_1 \approx V_2 \approx V_{in}$.

The input conductance G_{in} for this circuit is:

$$G_{in} = 2sC \frac{g_m + sC}{g_m + 2sC}$$

For the frequency less than $\frac{g_m}{2C}$, this is equivalent to 2C. For the frequency higher than $\frac{g_m}{C}$, this is eqivalent to C. Here, C is the input capacitance of M1 and M3, including the mirror effect. This bias circuit can offer less load to the previous stage. The only drawback is that it will shift the input signal by Vgs.

7.1. Differential Mode Gain

Fig. F-7(D) is the AC equivalent circuit for the differential mode input. For simplicity neither body bias effect nor short channel effect will be included here. And, the $g_{m's}$ of the transistors are matched perfectly as in the figure. (Also for the complimentaries.)

Because the circuit is perfectly matched, the crossing nodes of A and A' can be supposed to be at the virtual ground.

The current mirrors of M9, M13 and so on are scaled by a factor of ξ. From current conservation rule,

$$I = g_m V_{in}$$

$$2\xi I = sC_L V_{out} + 2g_{ml} V_{out}$$

Solving this equation for the differential gain Ad=Vout/Vin:

$$A_d(s) = \xi \frac{g_m / g_{ml}}{s\frac{C_L}{2g_{ml}} + 1} \qquad \text{(D-71)}$$

From this result, we get the DC differential gain of $\xi \frac{g_{m1}}{g_{ml}}$, and the cut off frequency ω_c of $2\frac{g_{ml}}{C_L}$.

7.2. PSRR

The loads M17 ~ M20 are connected in a diode configuration. So the gain for the AC power supply is approximately 1 for both Vdd and Vss.

The resistance of the loads M17 ~ M20 are too low to get a high gain. So in the actual design, two diode loads in series are used as in Fig. F-7(E).

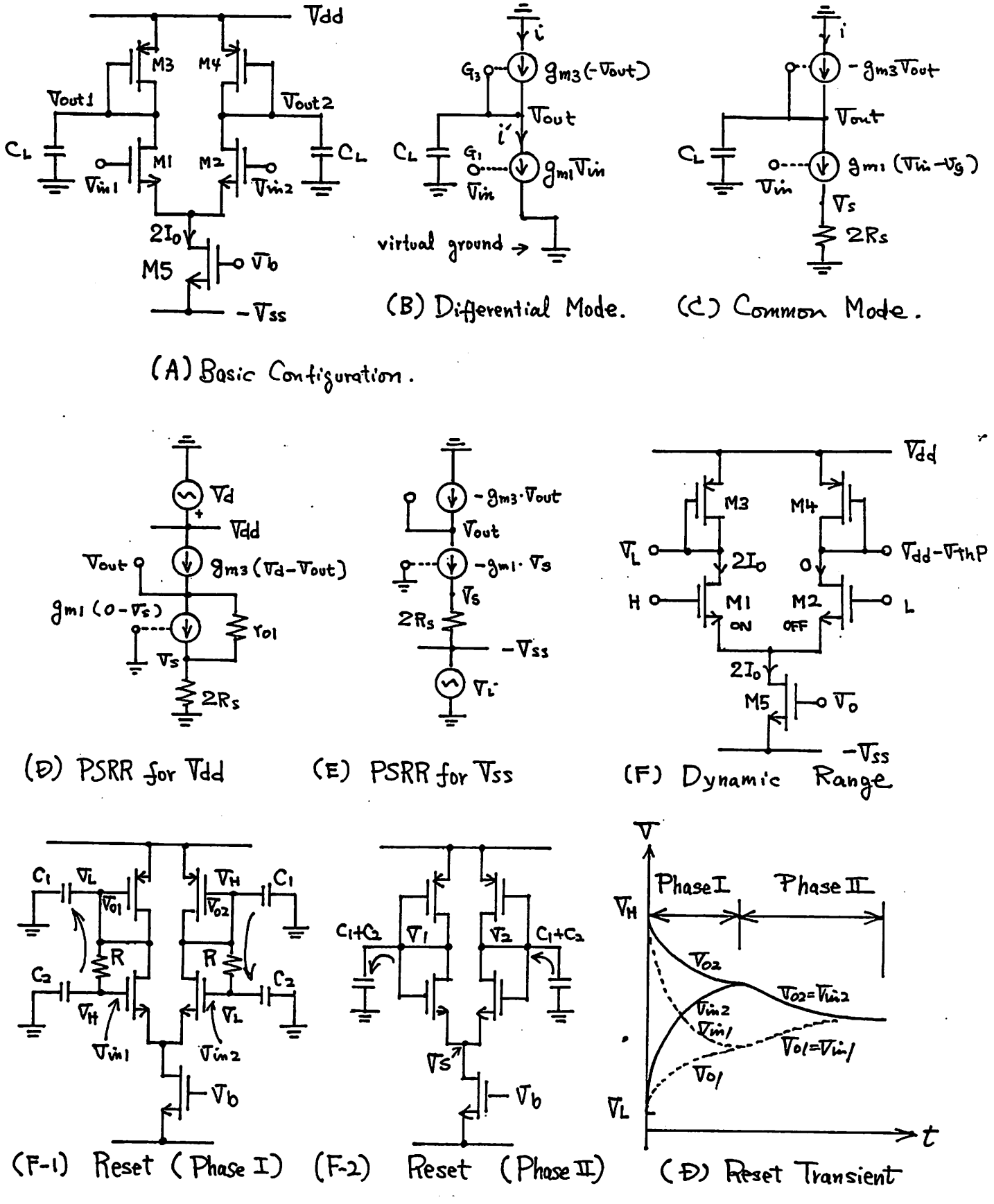


Fig.D-1 Fully Differential Amplifier with Diode Loads

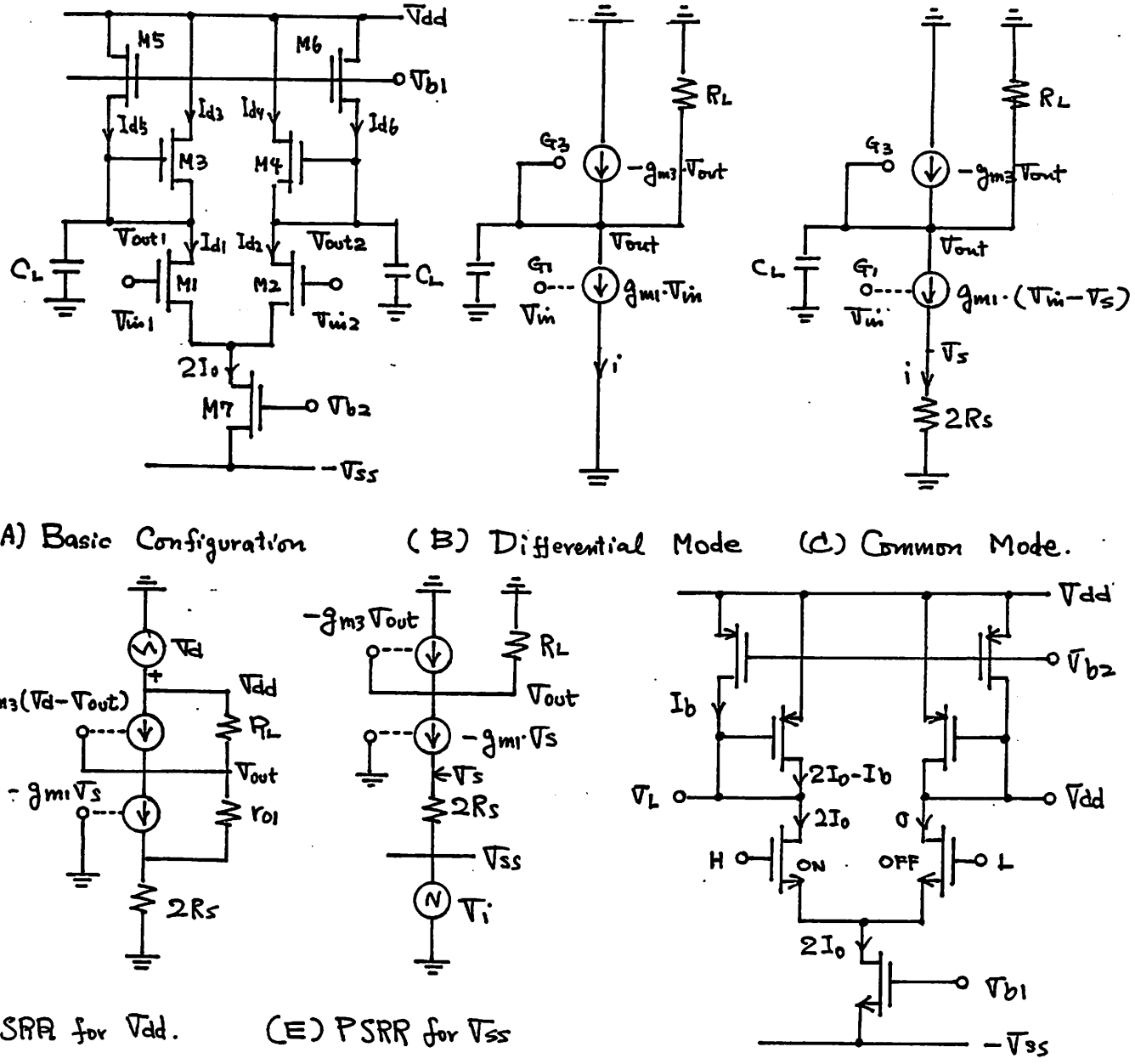
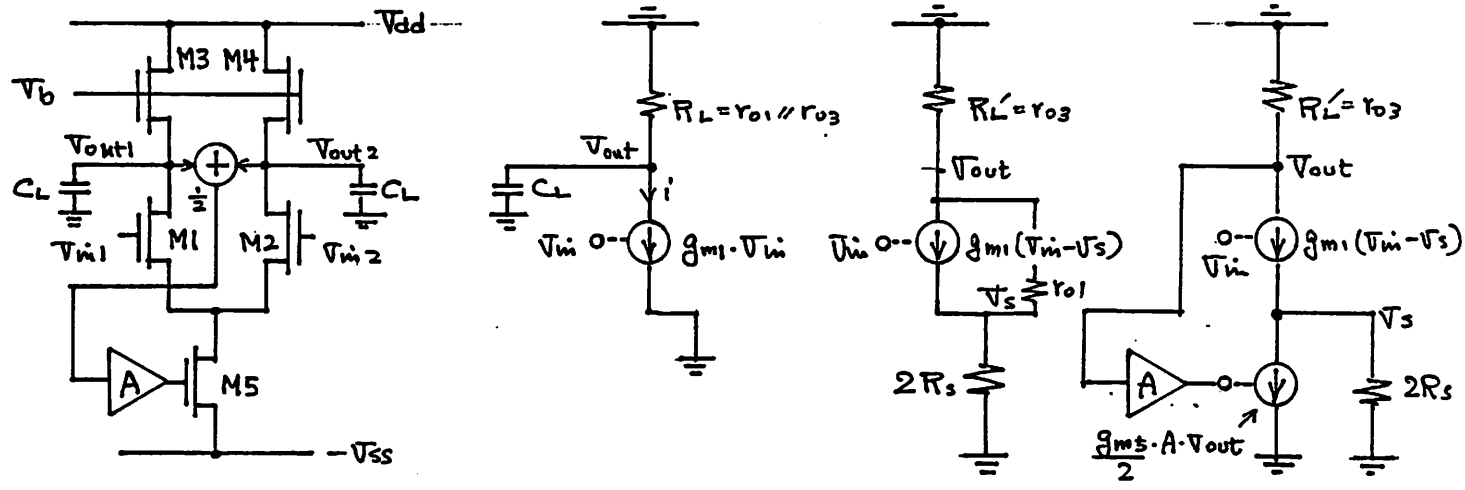
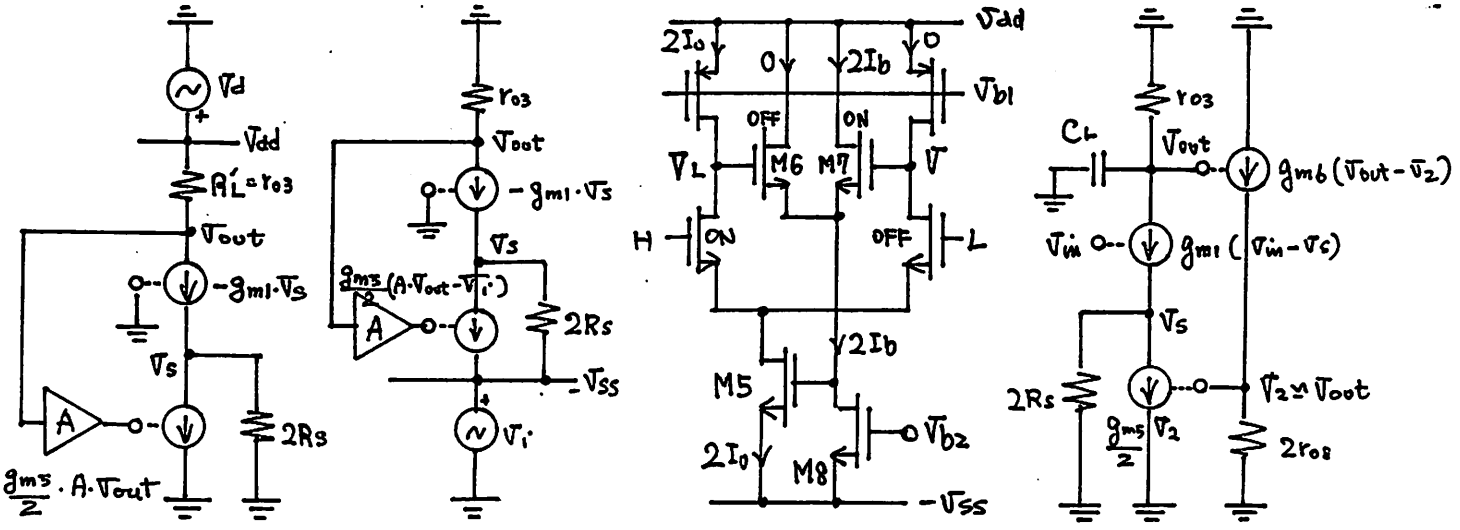


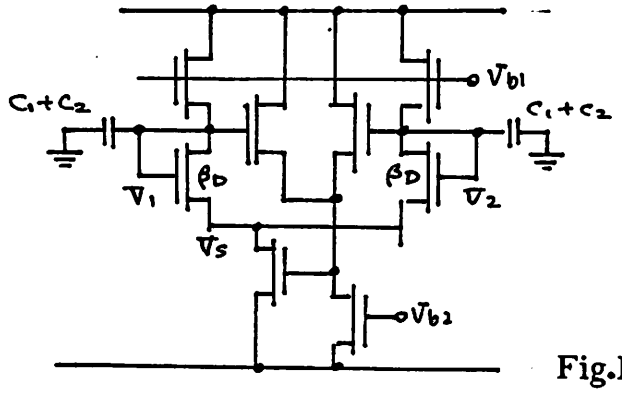
Fig.D-2 Fully Differential Amplifier with Diode and Current Source Loads.



(A) Basic Configuration (B) Differential Mode (C) Common Mode without CMFB. (D) Common Mode with CMFB

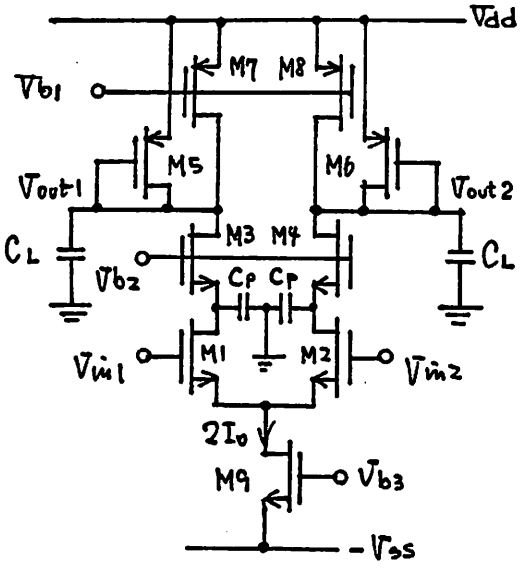


(E) PSRR for Vdd (F) PSRR for Vss (G) Dynamic Range (H) Frequency Response of the CMFB.

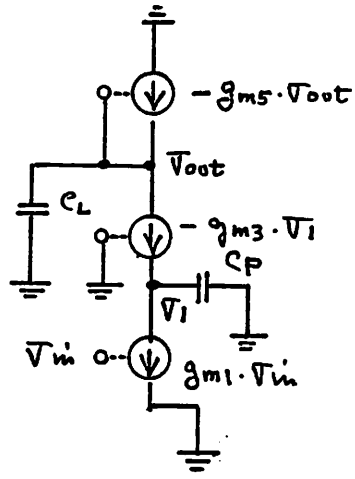


(I) Reset (Phase II)

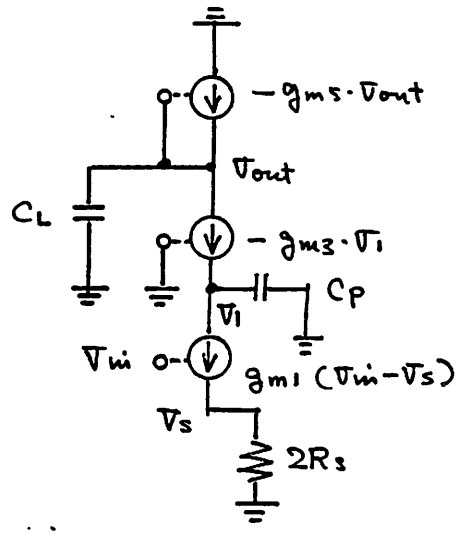
Fig.D-3 Fully Differential Amplifier with Current Source Loads and a CMFB Circuit.



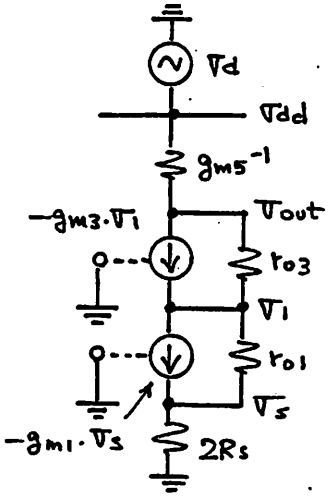
(A) Basic Configuration



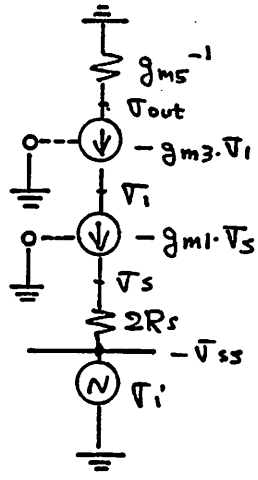
(B) Differential Mode.



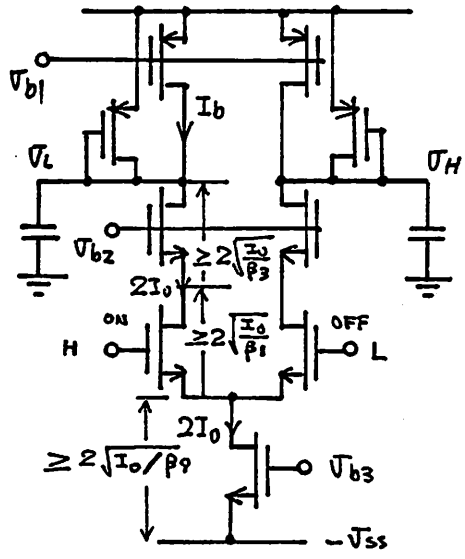
(C) Common Mode.



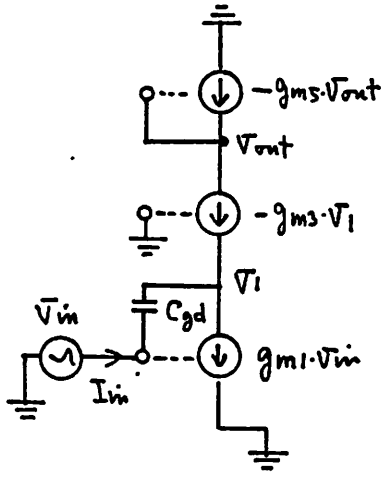
(D) PSRR for Vdd.



(E) PSRR for Vss.



(F) Dynamic Range.



(G) Imput Impedance.

Fig.D-4 Fully Differential Cascode Amplifier with Diode and Current Source Loads .

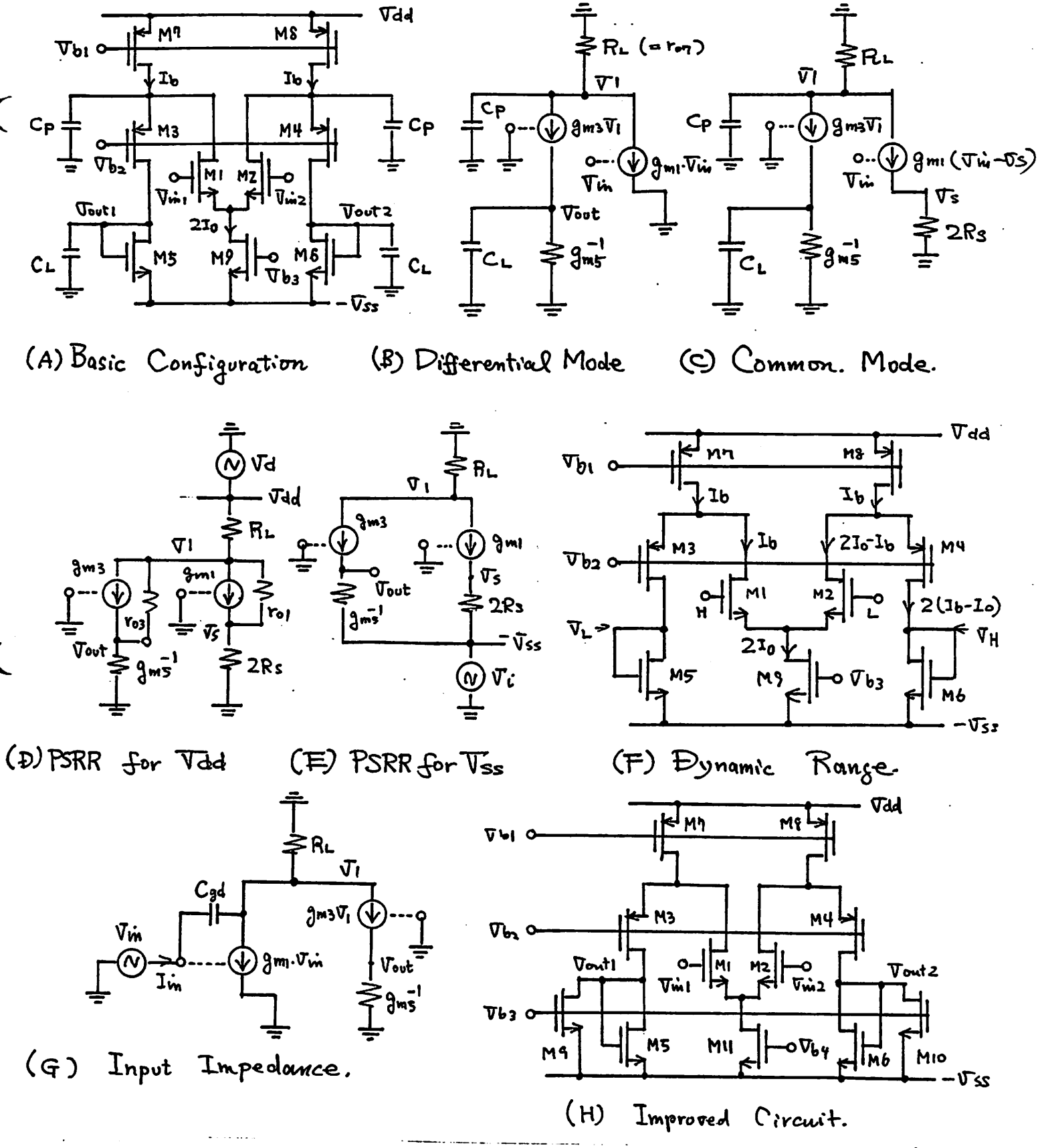
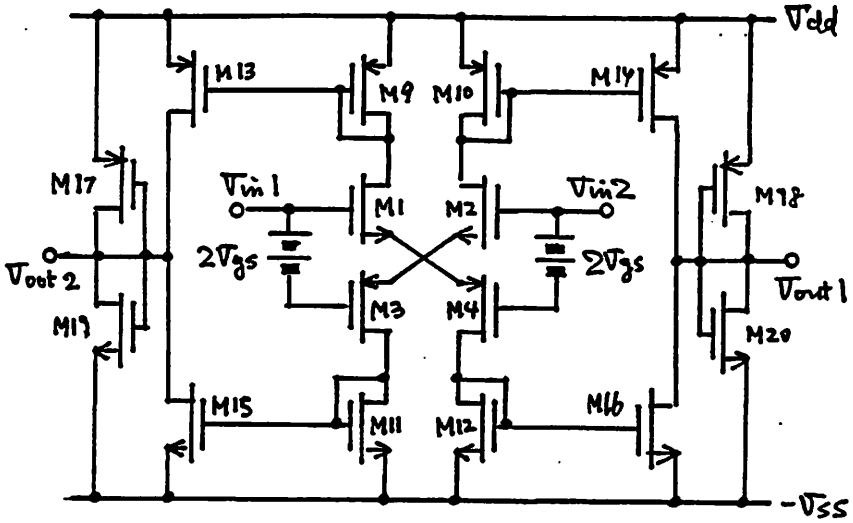
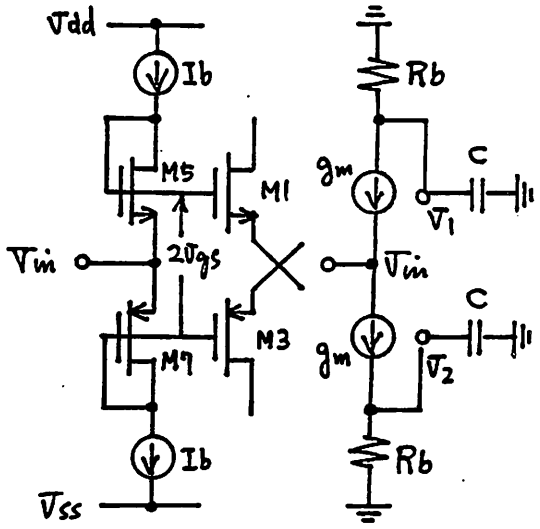


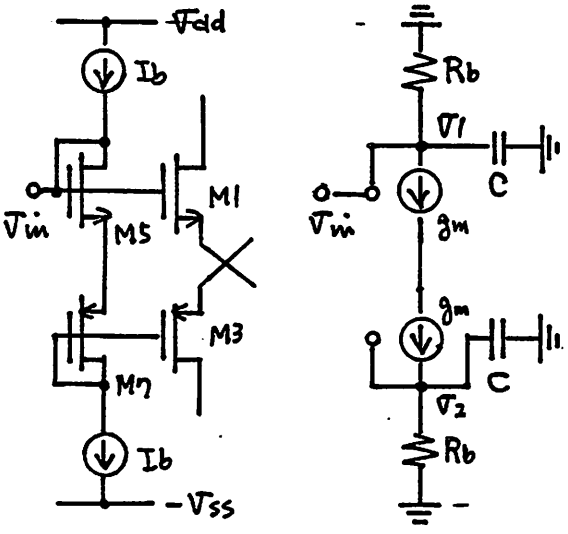
Fig.D-5 Fully Differential Folded Cascode Amplifier with Diode and Current Source Loads .



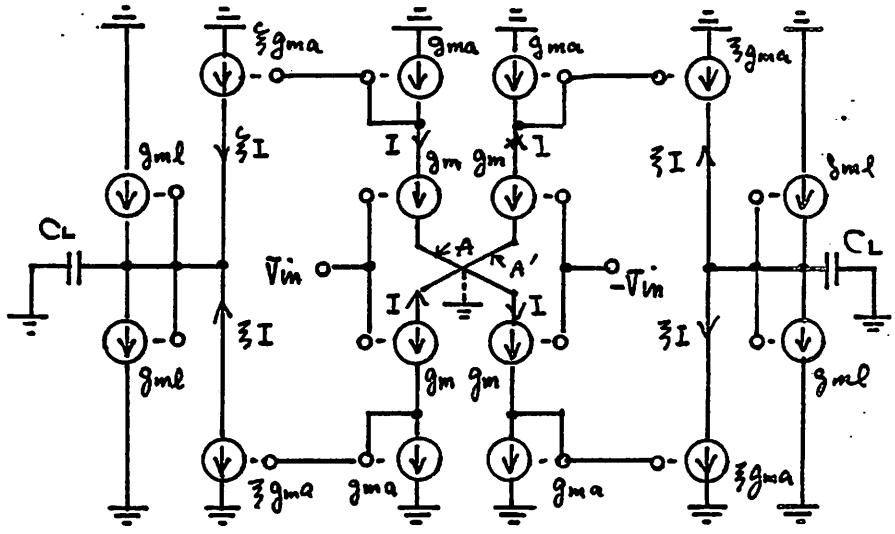
(A) Basic Configuration.



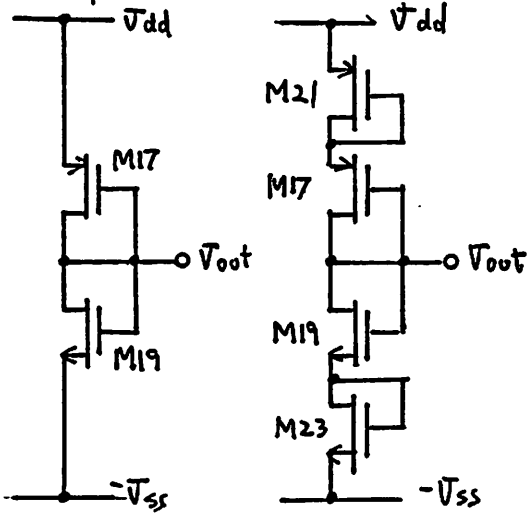
(B) Input Bias Circuit I



(C) Input Bias Circuit.



(D) Differential Mode.



(E) Two kinds of Diode Loads.

Fig.D-7 Fully Differential Class AB Amplifier with Diode and Current Source Loads.

Appendix E Optimum Design of the Fully Differential Amplifier.

(1) Amplifier with pMOS Loads in Diode Connection.

For the optimum design, we should find the maximum value of the GBW under the following conditions. Here, the same figures in the appendix F will be refered.

(1) When the circuit is in its balanced or idle state, (Id1=Id2) the output voltage stays at V_0 volt. That is:

$$I_{d3} = (V_{dd} - V_{thP} - V_0)^2 \frac{KP_3}{2L_3} W_3 = \alpha_3 W_3 \tag{E-1}$$

(2) The required gain G is achieved by the ratio W/L of the driver and load transistors. That is:

$$G = \frac{KP_1 \frac{W_1}{L_1}}{2\sqrt{\frac{KP_3 \frac{W_3}{L_3}}{}}} \tag{E-2}$$

$$r_{31} = \frac{W_3}{W_1} = \frac{1}{G^2} \frac{KP_1 L_3}{KP_3 L_1} \tag{E-3}$$

From Eq.(E-3), (E-1) and the relation of $I_{d1}=I_{d3}=I_d$:

$$I_d = \alpha_1 W_1 = \alpha_3 W_3 \tag{E-4}$$

$$\alpha_1 = \alpha_3 r_{31} \tag{E-5}$$

The transconductance of transistor M1 can be rewritten as a function of W_1 as:

$$g_{m1} = \sqrt{2KP_1 \alpha_1 / L_1} W_1 = \alpha_g W_1 \tag{E-7}$$

The total load capacitance at the output terminal is:

$$C_{LT} = C_c // C_{in} + C_{jd1} + C_{jd3} + C_{dg1} + C_{gb3}$$

Here, C_c is the coupling capacitance between each amplifiers. C_{in} is the next stage input capacitance including the Miller effect:

$$C_{in} = GC_{ox} L_D W_1 + C_{ox} L_1 W_1$$

Here, C_{ox} is the oxide capacitance per unit area, and L_D is the channel overlap length.

C_{jd}'s are the junction capacitances in the drain and can be expressed as:

$$C_{jd} = C_j L_M W$$

Except for C_{jd3} of M3, which will take the minimum size junction area of $L_M W_M$. Here, C_j is the junction capacitance per unit area. Each junctions are biased at different voltages, so that the junction capacitances per unit area, C_{j1}, C_{j3}, for transistors M1 and M3, are different and can be expressed as follows:

$$C_{j1} = \frac{C_j}{\sqrt{1 + \frac{V_0 - V_{ss}}{V_P}}}$$

$$C_{j3} = \frac{C_j}{\sqrt{1 + \frac{V_{dd} - V_0}{V_P}}}$$

C_{dg} is the drain gate overlap capacitance:

$$C_{dg} = C_{ox} L_D W$$

C_{gb} is the gate-base capacitance:

$$C_{gb} = C_{ox} LW$$

The attenuation ξ by the AC coupling capacitor C_c can be expressed as follows:

$$\xi = \frac{C_c}{C_c + C_{in}} = (C_c \,//\, C_{in}) \frac{1}{C_{in}}$$

Using all these equations, the total load capacitance can be expressed by W_1 as:

$$C_{LT} = \alpha_c W_1 + C_M \qquad \text{(E-8)}$$

Here,

$$\alpha_c = \xi C_{ox}(GL_D + L_1) + C_{ox}(L_D + r_{31} L_3) + C_{j1} L_M$$

and

$$C_M = C_{j3} L_M W_M$$

The gain band width GBW can be expressed from Eq. (E-7) and (E-8) as:

$$GBW = \frac{\alpha_g W_1}{\alpha_c W_1 + C_M} \qquad \text{(E-9)}$$

This GBW increases asymptotically to a maximum value with W_1, and the maximum value achieved is:

$$GBW_{max} = \frac{\alpha_g}{\alpha_c} \qquad ($$

To reach the 90% value of this maximum, W_1 should satisfy the following relationship:

$$W_1 \geqslant 9\frac{C_M}{\alpha_c} \qquad \text{(E-10-2)}$$

*** Numerical Example ***

The following conditions have been assumed:

$V_{dd}=2.5V$, $V_0=1V$, $V_{thP}=0.8V$, $L_D=0.23\mu m$,

effective $L_1=2-0.23*2=1.54u$,

effective $L_3=5-0.23*2=4.54u$,

effective $KP_3=15\mu S$,

effective $KP_1=45\mu S$,

$G\xi=10$, $\xi=0.5$, $G=20$,

$C_{ox}=1.2fF/\mu m^2$, $C_j=0.5fF/\mu m^2$

Then each coefficients can be calculated as follows:

$\alpha_1=0.0358$ (A/m)

$r_{31}=0.0221$

$\alpha_g=1.45\ (\frac{1}{\Omega m})$

$\alpha_c=5.44fF/\mu m$

$C_M=12.5fF$

And:

$GBW_{max}=267$ Mrad/s

To get 90% of the value above:

$W_1 \geqslant 21\mu m$

(2) Amplifier with Diode and Current Source Loads.

For the optimum design, we should find the maximum value of the GBW under the following conditions. Here, the same figures in the appendix F will be refered.

(1) When the circuit is in its balanced or idle state, (Id1=Id2) the output voltage stays at V_0 volt. That is:

$$I_{d3} = (V_{dd} - V_{thP})^2 \frac{KP_3}{2L_3} W_3 = \alpha_3 W_3 \qquad \text{(E-11)}$$

(2) The required gain G is achieved by equally ratioed current and channel width. That is:

$$G = \sqrt{\frac{KP_1 W_1 I_{d1}}{KP_3 W_3 I_{d3}}} \qquad \text{(E-12)}$$

$$r_{31} = \frac{I_{d3}}{I_{d1}} = \frac{W_3}{W_1} = \frac{1}{G}\sqrt{\frac{KP_1}{KP_3}} \qquad \text{(E-13)}$$

(3) M5 must be operated in a saturated region, until V_{out} reaches the value of $V_{dd} - V_{thP}$. (Ideally it should be V_{dd} .)

$$V_{ds5} = V_{thP} \geqslant V_{gs} - V_{thP} = \sqrt{\frac{2I_{d5}}{KP_5 \frac{W_5}{L_5}}}$$

To satisfy this condition with the minimum $\frac{W_5}{L_5}$, let's equate that and:

$$I_{d5} = V_{thP}^2 \frac{KP_5}{2L_5} W_5 = \alpha_5 W_5 \qquad \text{(E-14)}$$

From Eq.(E-13) and (E-11):

$$I_{d1} = \alpha_1 W_1 \qquad \text{(E-15)}$$

$$\alpha_1 = \alpha_3$$

Substituting (E-11), (E-14) and (E-15) to the current continuity equation of:

$$I_{d1} = I_{d3} + I_{d5}$$
$$\alpha_1 W_1 = \alpha_3 W_3 + \alpha_5 W_5$$

From Eq.(E-13) and the relation of $\alpha_1 = \alpha_3$, W_5 can be expressed by W_1 as follows:

$$W_5 = \frac{\alpha_1}{\alpha_5}(1-r_{31})W_1 = r_{51}W_1 \qquad \text{(E-16)}$$

The mutual conductance of transistor M1 can be rewritten as a function of W_1 as:

$$g_{m1} = \sqrt{2KP_1\alpha_1 / L_1}W_1 = \alpha_g W_1 \qquad \text{(E-17)}$$

The total load capacitance at the output terminal is:

$$C_{LT} = C_c / / C_{in} + C_{jd1} + C_{jd3} + C_{jd5} + C_{dg1} + C_{gb3} + C_{dg5}$$

Here, C_c is the coupling capacitance between each amplifiers, C_{in} is the next stage input capacitance including the Miller effect:

$$C_{in} = GC_{ox}L_D W_1 + C_{ox}L_1 W_1$$

Here, C_{ox} is the oxide capacitance per unit area, and L_D is the channel overlap length.

C_{jd}'s are the junction capacitances in the drain and can be expressed as:

$$C_{jd} = C_j L_M W$$

Except for C_{jd3} of M3, which will take the minimum size junction area of $L_M W_M$. Here, C_j is the junction capacitance per unit area. Here, each junctions are biased at different voltages, so that the junction capacitances per unit area, C_{j1}, C_{j3}, C_{j5}, for transistors M1, M3 and M5, are different and can be expressed as follows:

$$C_{j1} = \frac{C_j}{\sqrt{1 + \frac{V_0 - V_{ss}}{V_P}}}$$

$$C_{j3} = C_{j5} = \frac{C_j}{\sqrt{1 + \frac{V_{dd} - V_0}{V_P}}}$$

C_{dg} is the drain gate overlap capacitance:

$$C_{dg} = C_{ox}L_D W$$

C_{gb} is the gate-base capacitance:

$$C_{gb} = C_{ox} LW$$

The attenuation ξ by the AC coupling capacitor C_c can be expressed as follows:

$$\xi = \frac{C_c}{C_c + C_{in}} = (C_c / / C_{in}) \frac{1}{C_{in}}$$

Using all these equations, the total load capacitance can be expressed by W_1 as:

$$C_{LT} = \alpha_c W_1 + C_M \qquad \text{(E-18)}$$

Here,

$$\alpha_c = \xi C_{ox}(GL_D + L_1) + C_{ox}(L_D + r_{31}L + r_{51}L_D) + L_M(C_{j1} + r_{51}C_{j5})$$

and

$$C_M = C_{j3} L_M W_M$$

The gain band width GBW can be expressed from Eq. (E-17) and (E-18) as:

$$GBW = \frac{\alpha_g W_1}{\alpha_c W_1 + C_M} \qquad \text{(E-19)}$$

This GBW increases monotonically with W_1, and the maximum value achieved is:

$$GBW_{max} = \frac{\alpha_g}{\alpha_c} \qquad \text{(E-20-1)}$$

To reach the 90% value of this maximum, W_1 should satisfy the following relationship:

$$W_1 \geq 9 \frac{C_M}{\alpha_c} \qquad \text{(E-20-2)}$$

***** Numerical Example *****

The following conditions have been assumed:

$V_{dd} = 2.5V$, $V_{thP} = 0.8V$, $V_0 = 1V$, $L_D = 0.23\mu m$,

effective $L = 2 - 0.23 * 2 = 1.54u$,

effective $KP_3 = KP_5 = 15\mu S$,

effective $KP_1 = 45\mu S$,

$G\xi = 10$, $\xi = 0.5$, $G = 20$,

$C_{ox} = 1.2fF / \mu m^2$, $C_j = 0.5fF / \mu m^2$

Then each coefficients can be calculated as follows:

$\alpha_1=\alpha_3=2.39$ (A/m)

$\alpha_5=3.01$ (A/m)

$r_{31}=0.0866$, $r_{51}=0.725$.

$\alpha_g=11.8\ (\frac{1}{\Omega m})$

$C_{j1}=0.216 fF/\ \mu m^2$

$C_{j3}=C_{j5}=0.295 fF/\ \mu m^2$

$\alpha_c=7.11 fF/\ \mu m$

$C_M=12.5 fF$

And:

$GBW_{max}=1661$ Mrad/s

To get 90% of the value above:

$W_1 \geqslant 16\mu m$

The following is a design example:

$W_1=32\mu m$, $W_3=2\mu m$, $W_5=24\mu m$,

$I_{d1}=76\mu A$, $C_c=C_{in}=0.235pF$

Power Dissipation $P_0=76\mu A\ X\ 2\ X\ 5V=0.76mW$

When 32 comparators, each with 3 stage amplifiers, are considered, the total power dissipation will be 73 mW.

At last the optimum value for the attenuation factor ξ will be considered. The effective gain band width is the product of the GBW calculated above and ξ. On the other hand the load capacitance can divided in two parts, one containing ξ, and the other not. Then:

$$\alpha_c = \alpha_{c\xi}\xi + \alpha_{c0}$$

Here,

$$\alpha_{c\xi} = C_{ox}(GL_D + L_1)$$

and

$$\alpha_{c0} = C_{ox}(L_D + r_{31}L + r_{51}L_D) + L_M(C_{j1} + r_{51}C_{j5})$$

For the numerical example shown above.

$\alpha_{c\xi} = 7.37 fF/\mu m$

$\alpha_{c0} = 3.43 fF/\mu m$ There is a large contribution from the Miller capacitance of the next stage in $\alpha_{c\xi}$.

The effective gain band width under $W_1 \gg 1$ is:

$$GBW_{effective} = \frac{\alpha_g \xi}{\alpha_{c\xi}\xi + \alpha_{c0}}$$

($0 \leqq \xi \leqq 1$)

So the maximum effective gain band width will be:

$$GBW_{emax} = \frac{\alpha_g}{\alpha_{c\xi} + \alpha_{c0}}$$

when $\xi = 1$.

Taking the same number of the example above. this will be: $GBW_{emax} = 1092\ Mrad/s$.

For $\xi = 0.5$ as before . this value is 831 Mrad/sec.

(4) Cascode Amplifier with Diode and Current Source Loads.

For the optimum design. we should find the maximum value of the GBW under the following conditions. Here. the same figures in the appendix F will be refered.

(1) When the circuit is in its balanced or idle state. (Id1=Id2) the output voltage stays at V_0 volt. That is:

$$I_{d5} = (V_{dd} - V_{thP} - v0)^2 \frac{KP_5}{2L_5} W_5 = \alpha_5 W_5 \qquad \text{(E-41)}$$

(2) The required gain G is achieved by equally ratioed current and channel width. That is:

$$G = \sqrt{\frac{KP_1 W_1 I_{d1}}{KP_5 W_5 I_{d5}}} \qquad \text{(E-42)}$$

$$r_{51} = \frac{I_{d5}}{I_{d1}} = \frac{W_5}{W_1} = \frac{1}{G}\sqrt{\frac{KP_1}{KP_5}} \qquad \text{(E-43)}$$

(3) M7 must be operated in a saturated region, until V_{out} reaches the value of $V_{dd}-V_{thP}$. (Ideally it should be V_{dd} .)

$$V_{ds7} = V_{thP} \geqslant V_{gs}-V_{thP} = \sqrt{\frac{2I_{d7}}{KP_7 W_7/ L_7}}$$

To satisfy this condition with the minimum $\frac{W_5}{L_5}$, let's equate that and:

$$I_{d7} = V_{thP}^2 \frac{KP_7}{2L_7} W_7 = \alpha_7 W_7 \qquad \text{(E-44)}$$

From Eq.(E-43) and (E-41):

$$I_{d1} = \alpha_1 W_1 \qquad \text{(E-45)}$$
$$\alpha_1 = \alpha_5$$

Substituting (E-41), (E-44) and (E-45) to the current continuity equation of:

$$I_{d1} = I_{d5} + I_{d7}$$
$$\alpha_1 W_1 = \alpha_5 W_5 + \alpha_7 W_7$$

From Eq.(E-43) and the relation of $\alpha_1 = \alpha_5$, W_7 can be expressed by W_1 as follows:

$$W_7 = \frac{\alpha_1}{\alpha_7}(1-r_{51})W_1 = r_{71}W_1 \qquad \text{(E-46)}$$

The mutual conductance of transistor M1 can be rewritten as a function of W_1 as:

$$g_{m1} = \sqrt{2KP_1\alpha_1/ L_1}W_1 = \alpha_g W_1 \qquad \text{(E-47)}$$

The total load capacitance at the output terminal is:

$$C_{LT} = C_c / / C_{in} + C_{jd3} + C_{jd5} + C_{jd7} + C_{dg3} + C_{g55} + C_{dg7}$$

Here, C_c is the coupling capacitance between each amplifiers. C_{in} is the next stage input capacitance including the Miller effect:

$$C_{in} = C_{ox} L_D W_1 (1+\frac{g_{m1}}{g_{m3}}) + C_{ox} L_1 W_1$$
$$= C_{ox} L_D W_1 (1+\sqrt{\frac{W_1}{W_3}}) + C_{ox} L_1 W_1$$

Here, C_{ox} is the oxide capacitance per unit area, and L_D is the channel overlap length.

C_{jd}'s are the junction capacitances in the drain and can be expressed as:

$$C_{jd} = C_j L_M W$$

Except for C_{jd5} of M5, which will take the minimum size junction area of $L_M W_M$. Here, C_j is the junction capacitance per unit area. Here, each junctions are biased at different voltages, so that the junction capacitances per unit area, $C_{j1}, C_{j3}, C_{j5}, C_{j7}$, for transistors M1, M3 ,M5 and M7, are different and can be expressed as follows:

$$C_{j1} = \frac{C_j}{\sqrt{1 + \frac{V_{d1} - V_{ss}}{V_P}}}$$

$$C_{j3} = \frac{C_j}{\sqrt{1 + \frac{V_0 - V_{ss}}{V_P}}}$$

$$C_{j5} = C_{j7} = \frac{C_j}{\sqrt{1 + \frac{V_{dd} - V_0}{V_P}}}$$

C_{dg} is the drain gate overlap capacitance:

$$C_{dg} = C_{ox} L_D W$$

C_{gb} is the gate-base capacitance:

$$C_{gb} = C_{ox} LW$$

The attenuation ξ by the AC coupling capacitor C_c can be expressed as follows:

$$\xi = \frac{C_c}{C_c + C_{in}} = (C_c \,//\, C_{in}) \frac{1}{C_{in}}$$

In order to get the optimum ratio ,

$r_{31} = \frac{W_3}{W_1}$.

the dependence of C_{LT} on W_3 will be considered. C_{LT} increase proportional to $\frac{1}{\sqrt{W_3}}$ in the input capacitance, and proportional to W_3 in cgd 3. THat is:

$$C_{LT} = \frac{A}{\sqrt{W_3}} + BW_3 + C$$

Here,

$$A = C_{ox}\frac{L_D}{2}W_1^{\frac{3}{2}}$$

$$B = C_{ox}L_D$$

C: *capacitance independent of* W_3

By differentiating the equation above, we can get the optimum (minimum) value in:

$$r_{31} = \frac{W_3}{W_1} = (\frac{4}{\xi})^{\frac{2}{3}}$$

Using all these equations, the total load capacitance can be expressed by W_1 as:

$$C_{LT} = \alpha_c W_1 + C_M \qquad \text{(E-48)}$$

Here,

$$\alpha_c = \xi C_{ox}(\frac{(1+1}{\sqrt{r_{31}}})L_D + L_1) + C_{ox}(r_{31}L_D + r_{51}L + r_{71}L_D) + L_M(r_{31}C_{j3} + r_{71}C_{j7})$$

and

$$C_M = C_{j5}L_M W_M$$

The gain band width GBW can be expressed from Eq. (E-47) and (E-48) as:

$$GBW = \frac{\alpha_g W_1}{\alpha_c W_1 + C_M} \qquad \text{(E-49)}$$

This GBW increases monotonically with W_1, and the maximum value achieved is:

$$GBW_{\max} = \frac{\alpha_g}{\alpha_c} \qquad \text{(E-50-1)}$$

To reach the 90% value of this maximum, W_1 should satisfy the following relationship:

$$W_1 \geqslant 9\frac{C_M}{\alpha_c} \qquad \text{(E-50-2)}$$

***** Numerical Example *****

The following conditions have been assumed:

V_{dd} =2.5V, V_{thP}=0.8V, V_0=1V, L_D =0.23μm,

effective L =2—0.23*2=1.54u,

effective KP_5=KP_7=15μS,

effective KP_1=KP_3=45μS,

$G\xi=10.\ \xi=0.5.\ G=20.$

$C_{ox}=1.2fF/\ \mu m^2.\ C_j=0.5fF/\ \mu m^2$

Then each coefficients can be calculated as follows:

$\alpha_1=\alpha_5=2.39$ (A/m)

$\alpha_7=3.12$ (A/m)

$r_{31}=0.250.\ r_{51}=0.0866.$

$r_{71}=0.700.$

$\alpha_g=11.8\ (\frac{1}{\Omega m})$

$C_{j3}=0.216fF/\ \mu m^2$

$C_{j5}=C_{j7}=0.295fF/\ \mu m^2$

$\alpha_c=3.70fF/\ \mu m$

$C_M=12.5fF$

And:

$GBW_{max}=3189$ Mrad/s

To get 90% of the value above:

$W_1 \geqslant 30\mu m$

The following is a design example:

$W_1=23\mu m\ .\ W_3=6\mu m\ .\ W_5=2\mu m\ .\ W_7=16\mu m$

$I_{d1}=55\mu A\ .\ C_c=0.061P\ .\ C_{in}=0.061pF$

Power Dissipation $P_0=55\mu A\ X\ 2\ X\ 5V=0.55mW$

When 32 comparators, each with 3 stage amplifiers, are considered, the total power dissipation will be 53 mW.

Appendix F Reset Speed and Stabilization

(1) Static Calculation of the Offset Sampling.

By making a close loop connection of the fully differential amplifier, its input offset voltage Vos can be sampled in both the output and input terminals. In this way, the equivalent offset can be reduced.

Fig.F-1(B) shows the DC transfer characteristic of a fully differential amplifier with an input offset of Vos. As shown in the figure, the two complementary transfer curves cross at Vin1-Vin2=Vos. Those curves can be described by the following equations.

$$Vo1 = -A(Vin1-Vin2-Vos)-B(V1+V2)+Vco \quad \text{(F-1)}$$

$$Vo2 = A(Vin1-Vin2-Vos)-B(V1+V2)+Vco \quad \text{(F-2)}$$

Here, A,B and Vco are the differential mode gain, the common mode gain and the common mode output offset in the cross point, respectively.

By making a close loop as in the Fig. F-1(C), the offset Vos can be sampled in each terminals as follows:

$$Vin1 = Vo1 = \frac{Vco}{1-2B} + \frac{2A}{1+2A}\frac{Vos}{2} \quad \text{(F-3)}$$

$$Vin2 = Vo2 = \frac{Vco}{1-2B} - \frac{2A}{1+2A}\frac{Vos}{2} \quad \text{(F-4)}$$

For the differential amplifiers considered here, B is kept much smaller than 1.

The input equivalent offset voltage Veos can be calculated as:

$$Veos = \frac{Vo1-Vo2}{2A} = \frac{Vos}{1+2A} \quad \text{(F-5)}$$

Here, the residual offset is inversely proportional to the differential gain.

(2) Transient Response of the Reset in Linear Region.

For a simplification, the reset of a single ended amplifier shown in Fig. F-2 will be calculated. Here, Rf is the on resistance of the MOS transfer switch used to close the loop. For the first order calculation, the transfer characteristic of the amplifier is assumed as

follows:

$$H(s) = -\frac{A\,\omega_c}{s+\omega_c} \tag{F-6}$$

The effect of the load capacitance has been included in ω_c.

The relation between the input voltage Vin and output voltage Vo. after the Laplace transformation can be described as;

$$Vo(s) = H(s)\,Vin(s) \tag{F-7}$$

$$\frac{Vo(s)-Vin(s)}{R_f} = C_{in}(sVin(s)-Vino) \tag{F-8}$$

Here. Vino is the initial condition of the input voltage.

Solving for Vout(s). the following equation can be derived:

$$Vout(s) = \frac{A\ Vino}{s^2 + (\omega_c + \frac{1}{R_f C_{in}})s + (A+1)\frac{\omega_c}{R_f C_{in}}} \tag{F-9}$$

The time domain solution of the equation above can be solved to be;

$$Vout(t) = A\ Vino\ e^{-\frac{t}{2R_f C_{in}}} \sin\left(\frac{1}{2R_f C_{in}}\sqrt{4\omega_c A R_f C_{in} - 1}\ t\right) \tag{F-10}$$

Here. the approximation of $\omega_c << \frac{1}{R_f C_{in}}$ and the condition of $4\omega_c A R_f C_{in} \geqslant 1$. which is usually the case. has been applied. Thus. the initial voltage decay with the time constant of $\frac{1}{2R_f C_{in}}$. and with the oscillation of a certain frequency. For a numerical example of ω_c = 100 Mrad/s Cin=0.1pF and Rf=10Kohm. the time constant is 2ns. while the period of the oscillation is 1 15nS.

For the general case. the time constant for the decay. can be calculated from Eq.(F-9) as:

$$\tau = \frac{2}{\omega_c + \frac{1}{R_f C_{in}}} \tag{F-11}$$

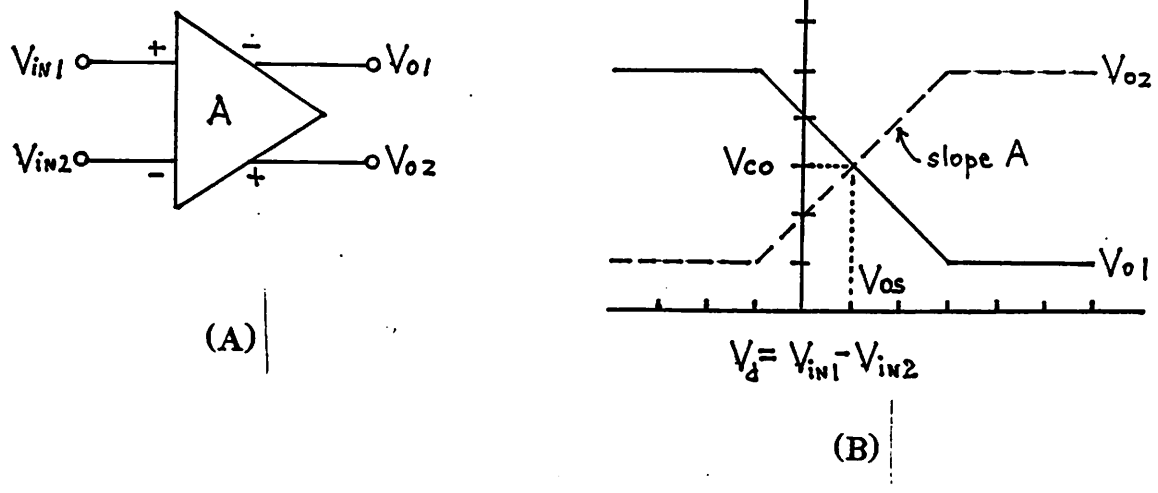
In the linear region operation. the shorter time constant dominates the time constant for the decay.

From Eq.(F-10), it is clear that to prevent the oscillation, the GBW ($A\,\omega_c$) of the amplifier should satisfy the following condition;

$$A\,\omega_c \leqslant \frac{1}{4R_f\,C_{in}} \qquad \text{(F-12)}$$

(2) Transient Response of the Reset in the Non-Linear Region.

Before the amplifier enters in its quasi-static linear operation region, it is in a saturated status, or in the nonlinear operation region. The response there depends in the circuit configuration, so that no general response can be calculated analytically as in the case above. The response for each circuit configuration will be discussed in the section 3.5.7 and appendix F.



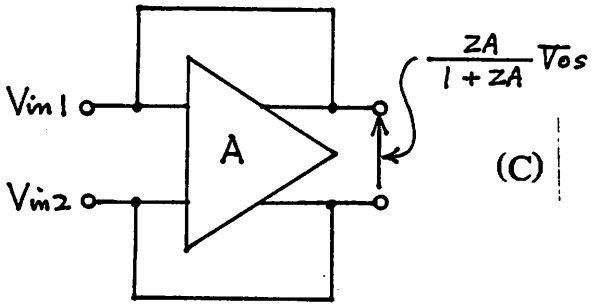
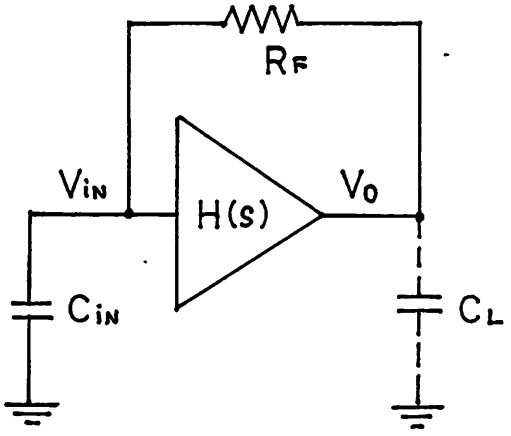


Fig.F-1 DC Transfer Characteristics of a Fully Differential Amplifier.



$$H(s) = -\frac{A\,\omega_c}{s+\omega_c}$$

Fig.F-2 Reset Circuit Model.

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