HIGH-FREQUENCY VOLTAGE AMPLIFICATION AND COMPARISON IN A ONE-MICRON MOS TECHNOLOGY

by

David C. Soo

Memorandum No. UCB/ERL M85/96

4 December 1985

HIGH-FREQUENCY VOLTAGE AMPLIFICATION AND COMPARISON IN A ONE-MICRON MOS TECHNOLOGY

by

David C. Soo

Memorandum No. UCB/ERL M85/96

4 December 1985

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

To my loving parents

High-Frequency
Voltage Amplification and Comparison
in a One-Micron NMOS Technology

Ph. D. David C. Soo Department of EECS

Robert G. Meyer
Chairman of Committee

Abstract

This thesis is concerned with methods of realizing wide-band amplifiers and high-speed voltage comparators in a 1μm NMOS process. Three amplifier and four comparator configurations are analyzed theoretically, and based on these analyses, design curves and equations are generated to facilitate circuit optimization. Optimized circuits for each configuration are compared via simulation and design trade-offs are considered. Results from this study lead to new circuit configurations for voltage amplification and comparison. A new amplifier configuration using active shunt feedback to obtain stable wide-band voltage gain is proposed. This amplifier configuration is incorporated into the design of a high-speed voltage comparator. The simulated comparison rate of the proposed circuit is highest among the eight comparators considered in this study.

A high-speed voltage comparator, a wide-band amplifier and a 50Ω output buffer have been fabricated using a 1μm NMOS technology and tested at high frequencies. The voltage comparator achieves 5 bits of input resolution at 750 MS/s. The amplifier has a gain of 9dB and a bandwidth of 1.17GHz. The output buffer can deliver 12.5dBm of power to a 50Ω load with a loss of 3dB and a bandwidth of 3.5GHz.

Acknowledgement

I would like to thank Prof. Bob Meyer for his support and encouragement throughout the course of this work. It is my privilege to be his student. I also wish to thank Prof. Paul Gray for being an excellent teacher and for his advice during these years.

I owe my deepest gratitude to Ping and Evelyn Ko who gave me their friendship and assistance at a time when they were needed most. Ping also taught me a lot about process technology, device physics, and above all, his ways to approach and analyze a problem.

I am also in debt to many graduate students in 401 Cory; especially to Tat Choi and John Hui who helped me throughout my years in Berkeley and during my Ph.D preliminary examination. Other students who contributed to this work in different ways are Sik Lui, Ping Li, Wingyu Leung, Simon Wong, T.Y. Chiu, Kai Toh, Simon Tam, Simon Szeto and Wayne Lo.

Among my colleages in Bell Labs, I wish to thank them for their friendship and their assistance towards this research effort. Especially, I wish to thank Bruce Wooley for arranging my research position with Bell Labs' management and for his suggestions on the thesis, Gen Chin for his expertise in integrated-circuit fabrication, Bob Swartz for proofreading the thesis, Alex Voshchenkov and P.K. Tien for their encouragement.

I would like to thank my brother Jason for taking up my responsibilities to my parents so that I can complete my lengthy education. Last, but not least, I wish to thank my wife, Audrey, for her patience and for providing me with a comfortable home where I can work and rest during the preparation of this manuscript.

Research sponsored by the U. S. Army Research Office Contracts DAAG29-80-K-0067 and DAAG29-84-K-0043.

Table of Content

Chapter 1 Introduction

The driving force behind MOS technology has been the constant advancement in photolithography. From a $10\mu m$-aluminum-gate NMOS process, this technology has evolved into the $2\mu m$-polysilicon-gate CMOS process. Next generation processes will produce MOS transistors with channel lengths below one micron. In addition to higher packing density, these sub-micron technologies have higher switching speed because of the improved transistor f_T.

Ring oscillator delay is a useful indication of the intrinsic speed of an integrated-circuit process. Among the different silicon technologies, NMOS has demonstrated the fastest ring oscillator speed - 70ps, 32ps and 28ps for the $1\mu m$, $0.5\mu m$ and $0.35\mu m$ gate length, respectively [5] [35]. For comparable design rules, the ring oscillator speed of a CMOS process [36] has always been a factor of two or more slower than that of the NMOS because of the lower hole mobility of the P-channel transistor and the higher parasitic capacitance associated with the N-well. Bipolar technology has also taken advantage of the improving photolithography to enhance its speed performance. Using emitter dimension down to $0.35\mu m$, a ring oscillator delay of 30ps has been reported [4]. NMOS and bipolar are the two silicon technology competing in the high-speed arena.

A/D, D/A converters and optical repeaters are needed for telecommunication at data rate above 1GHz. In these applications, bipolar technology has the advantage of high transistor voltage gain $g_m r_o$ which makes realization of analog circuits with high gain and high accuracy possible. However, its disadvantage when compared to MOS is its finite current gain $g_m r_\pi$ which makes it difficult to design analog sample-and-hold at speeds above 1GS/s. Because of the requirement for analog S/H and the compatibility with existing digital circuits, it may be more suitable to implement high-speed low-resolution analog circuits such as 4-bit A/D converter and optical repeater in $1\mu m$ NMOS technology.

Because short-channel MOS is a relatively new technology, many of the basic circuit functions are still dependent on further research. For example, voltage amplification and

comparison are two basic circuit functions that need to be studied. These functions are essential to the implementation of A/D, D/A converters and optical repeaters. Furthermore there is no general theory or design principle available in the literature that deals with voltage comparators. This thesis reports on an investigation in the design, the speed and the various trade-offs of wide-band amplifiers and high-speed voltage comparators in a $1\mu m$ NMOS technology. The technology used to fabricate the test circuits in this report was originally developed at Bell Laboratories, Holmdel. The technology is referred to as SiGMOS - Silicon Gigabits-per-second NMOS technology [5]. The process flow and design rules of the SiGMOS technology are shown in appendix A-3 and A-4 respectively.

Chapter 2 investigates the design of wide-band amplifiers. Three amplifier configurations are considered. They are the open-loop, the single-stage shunt feedback and the three-stage shunt feedback. It is shown that an amplifier which employs active shunt feedback around a single gain stage has the best speed performance. Using the SiGMOS technology, wide-band voltage amplification up to 2 GHz seems feasible. Gain-bandwidth-products, transistor f_T, and ring oscillator delay of the SiGMOS technology are also considered. Finally the chapter concludes with a discussion of the trade-offs between gain, bandwidth and gain sensitivity for the three amplifier configurations.

Chapter 3 focuses on the design of high-speed voltage comparators. Unlike operational amplifiers which have feedback, voltage comparators are open-loop circuits. With the addition of transfer gate, and analog S/H from the MOS technology, voltage comparator designs can have many variations; there is no general consensus as to which comparator configuration should give the best performance. This chapter analyzes four basic comparator configurations - cascade of open-loop amplifiers, cascade of open-loop amplifier with reset, pipeline of differential amplifiers and preamplifier plus regenerative latch. For each configuration, first order design equations and curves are presented, and optimized examples are compared in terms of sampling rate, comparison delay and power dissipation. For the last two comparator configurations, its is shown that applying negative feedback can improve the recovery time of the comparator significantly.

Chapter 4 gives experimental results to support the theories developed in the previous two chapters. A 3.5GHz 50Ω output buffer is first described. Then a 1.17GHz, 9dB

gain wide-band amplifier is presented. This amplifier employs single-stage shunt feedback to stablize its characteristics. The same amplifier configuration is incorporated in the preamplifier of a high-speed voltage comparator which relies on the positive feedback regeneration of a latch to generate the large digital signal at its outputs. This comparator has achieved 5 bits of input resolution at 750MS/s.

Chapter 2 Wide-Band Amplifiers

In this chapter, the design of wide-band amplifiers in the SiGMOS technology is considered. In particular, amplifiers intended to drive only internal capacitance are considered here because these amplifiers are to be integrated as part of a larger system on a single chip. One example is a preamplifier of the latched comparator described in chapter 3, that employs negative feedback to obtain stable wide-band voltage gain. Other applications include clock input buffers, amplifiers in fiber optics repeaters, and amplifiers for high frequency prescalers.

Three basic wide-band amplifier configurations are considered here in detail. They are the open-loop amplifiers in section 2.1, the single-stage active shunt feedback amplifier in section 2.3, and the three-stage active shunt feedback amplifier in section 2.4. Each amplifier design has its advantages and disadvantages. For example, the open-loop amplifier has the lowest power dissipation among the three amplifier designs, but poor frequency response and poor amplifier gain stability. The single-stage active shunt feedback amplifier on the other hand has the highest frequency response among the three, but only moderate gain stability. Finally the three-stage active shunt feedback amplifier has the best gain stability but only moderate frequency response.

Section 2.2 defines the normalized gain-bandwidth product as a figure of merit in the performance evaluation of different amplifier designs. The relationship between gain-bandwidth product, transistor f_T and ring oscillator delay are also considered in this section. Finally in section 2.5, sensitivities of the three types of amplifier are considered and conclusions are drawn based on amplifier performance.

2.1 Open Loop Amplifiers - Inverter and Source Follower

2.1.1 Depletion Mode Inverter

DC Biasing and Other Considerations

The depletion mode inverter, shown in figure 2.1 has been used extensively in digital systems as a logic inverter. This section investigates the possibilities and the problems of using this simple circuit as small signal amplifier within a larger integrated circuit.

By cascading these inverters in series, we can achieve large voltage gain. The a.c. equivalent circuit of such a cascade resembles that of the bipolar amplifier proposed by Gilbert [1]. The success of these bipolar open loop amplifiers [9] is mainly due to the well behaved exponential characteristic of the bipolar transistor and the good matching properties of the bipolar process. On the other hand, short channel MOS transistors are plagued with non-idealities and short channel effects. These problems when compounded with temperature and process variations, may render the inverter unacceptable in applications where gain stability is of concern. In which case, negative feedback amplifiers presented in section 2.3 and 2.4 should be used.

In figure 2.1, an active load is used instead of a resistive load because in most digital NMOS technologies, well characterized resistors are not available. A 5V supply is assumed because a higher supply voltage would induce hot electron currents (since V_{DD} can appear across the drain-source of the short-channel transistor under large input signals) which in turn causes long term reliability problems [2]. The use of a 5V supply and active load impose constraints in circuit designs.

To achieve high frequency response and low sensitivity to processing variations, the following design (summarized in table 2-1) is proposed. This design is based on an inverter aspect ratio $\frac{W_E}{W_D}$ of 1. Conventional NMOS logic inverters, usually have a $\frac{W_E}{W_D}$ ratio between 2 to 4, because the enhancement and depletion thresholds are fixed at 0.7V

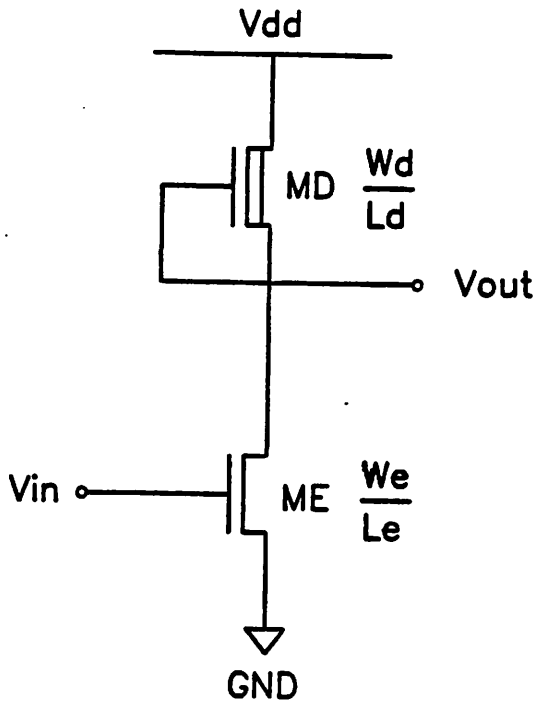


Fig. 2.1 Depletion-mode inverter.

Design Parameters	
Vdd	+5V
Vss	−5V
Wd	W
Ld	1um
We	W
Le	1um
Vtd	−1.5V
Vte	1V

Table 2.1 Summary of Depletion Mode Inverter Design.

and -3V respectively in a conventional technology, and the inverter ratio is chosen such that V_{OL} is below the enhancement threshold to ensure good noise margins. In the SiGMOS technology, an alternative approach was taken, such that the inverter ratio is fixed at 1 and the threshold voltages are optimized so that the dc transfer curve goes through the point where $V_{IN}=V_{OUT}=2.5V$. This way, noise-margin high is approximately equal to noise-margin low. We will show that the "one-one" design improves speed performance and lowers amplifier sensitivities to processing variations.

In the one-one design, frequency response is improved because parasitic edge capacitance at the output node is minimized. Consider a typical layout of the inverter shown in figure 2.2. In this layout, the edge capacitor at the output node is only 10 microns long and it does not scale with the inverter width W. Therefore by making W large, edge capacitance can be made neglectable compared to other loading capacitances. Measured values of the different capacitors in the SiGMOS technology are summarized in table A-1 in the appendix. Using these data and assuming W equals $10\mu m$, the gate capacitance of the following stage is calculated to represent only about 40% of the total capacitive loading at the output; therefore minimizing edge and junction capacitance is essential for high frequency operation.

The one-one design also improves control of the amplifier dc gain against processing variations. The dc gain of the amplifier is given by

$$\frac{v_o}{v_i} = -g_m R \tag{2.1}$$

where

$$R = \left(r_{oE} \| r_{oD} \| \frac{1}{g_{mb_D}} \right)$$

For the MOS transistor, transconductance is proportional to device width W, and output resistance is proportional to $\frac{1}{W}$, therefore by making $W_E = W_D$, the gain of the amplifier is insensitive to overetch during the field oxide cut that defines the device width.

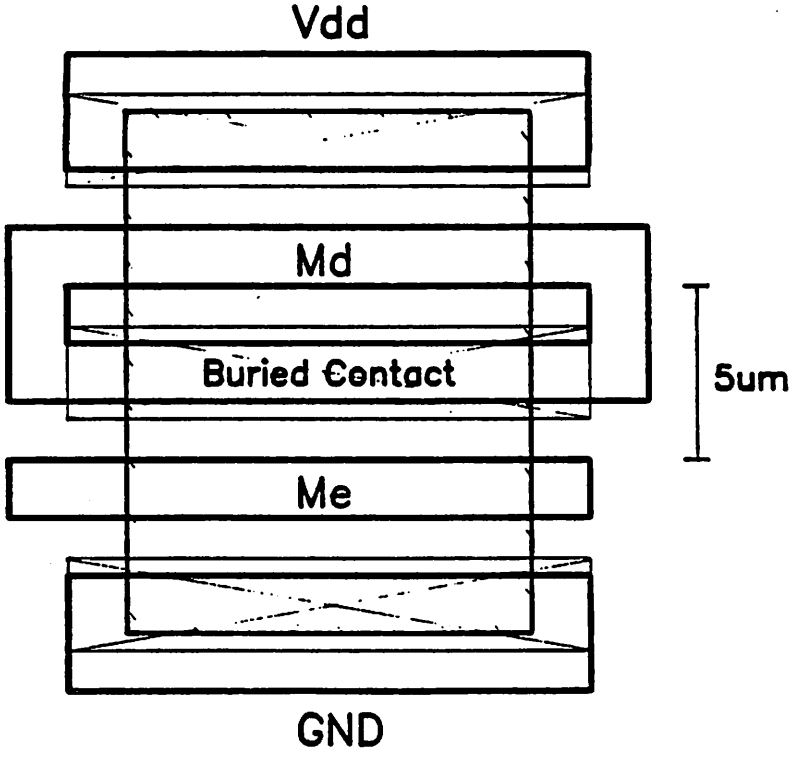


Fig. 2.2 Typical layout of a depletion-mode inverter.

To achieve wide bandwidth, the transistor should be operated in the high transconductance region because the transistor f_T is $\frac{g_m}{2\pi C_g}$. Figure A-1 shows the I-V characteristics of a 0.95 micron gate length MOS transistor. Because of velocity saturation, its characteristics deviate from ideal square law, and the measured g_m curve in figure A-2 saturates at high $V_{GS}-V_T$. To operate at 90% of maximum g_m, a $V_{GS}-V_T$ of 1.5V is chosen as the desired bias point. Biasing the transistor at higher $V_{GS}-V_T$ would not improve speed performance but would increase power dissipation, degrade output resistance and above all, lower the gain of the transistor.

Once the desired $V_{GS}-V_T$ is chosen at 1.5V, and the inverter ratio is set to 1, the enhancement and the depletion thresholds are optimized in the following manner. The measured saturation current for the transistor in figure A-2 shows that at $V_{GS}-V_T$ higher than 1.5V, Idsat versus $V_{GS}-V_T$ can be approximated by a straight line.

$$I_{DsatE} \approx k_E W_E \left(V_{GSE}-V_{TE}-0.45 \right) \tag{2.2}$$

and

$$I_{DsatD} \approx k_D W_D \left(V_{GSD}-V_{TD}-0.45 \right) \tag{2.3}$$

for the enhancement and the depletion devices respectively, and $k_E \approx k_D \approx 80 \mu A/V$. Since $I_{DsatE}=I_{DsatD}$ and $V_{GSD}=0$ in figure 2.1, we have

$$V_{GSE}-V_{TE} \approx \left(-V_{Td}-0.45 \right) \frac{W_D}{W_E} + 0.45 \tag{2.4}$$

If $W_E=W_D$, equation 2.4 reduces to

$$V_{GSE}-V_{TE}=-V_{TD}$$

which implies that the desired $V_{GS}-V_T$ of the E-device is governed by only one process variable, the depletion threshold. Since the desired $V_{GS}-V_T$ is 1.5V, V_{TD} should equal -1.5V. In order for the inverter to be dc cascadable, the desired operating point is $V_{IN}=V_{OUT}=2.5V$. Since $V_{IN}=V_{GSE}$, according to equation 2.4 V_{TE} equals 1V.

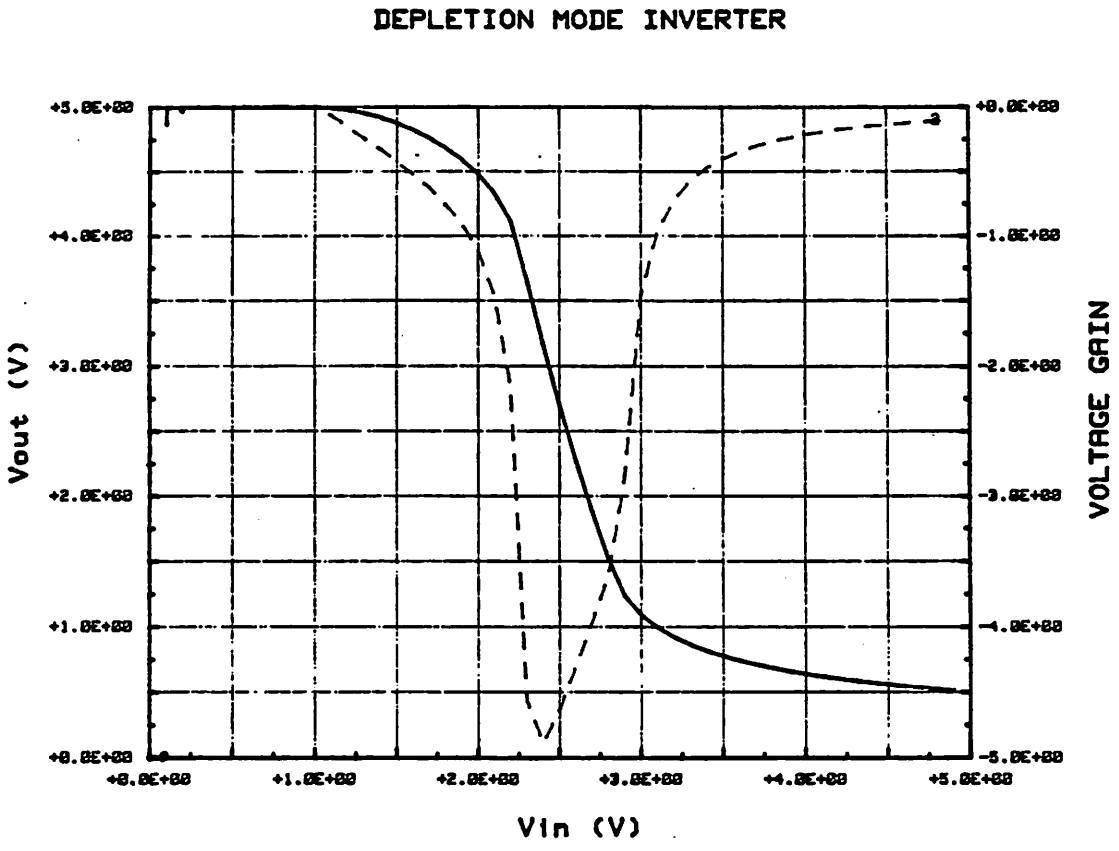


Fig. 2.3 Simulated DC transfer curve and gain of inverter.

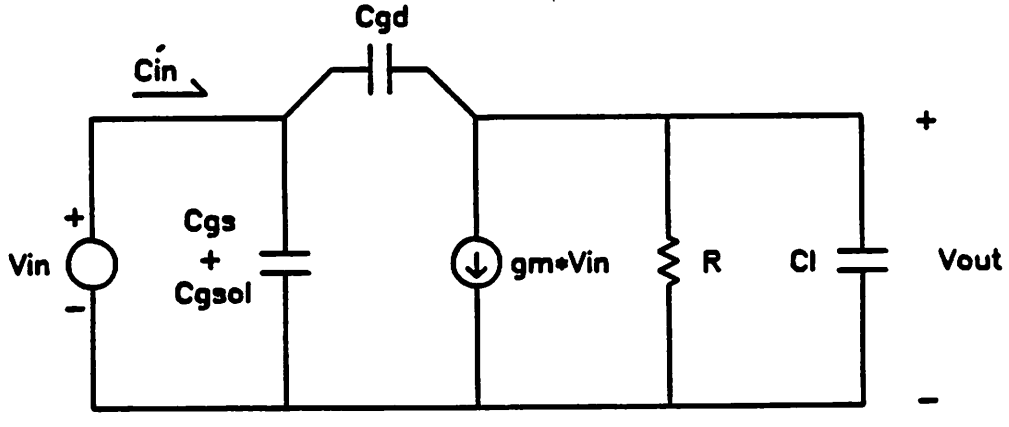


Fig. 2.4 Small signal equivalent circuit of inverter.

The simulated dc transfer curve is plotted along with the dc gain in figure 2.3. The maximum gain point occurs at V_O=2.5V because the output resistance R in equation 2.1 is maximized when V_{DSE}=V_{DSD}=2.5V. Measured device output resistance versus V_{DS} is shown in figure A-3. For the one-one inverter design if we choose the dc operating point at V_{IN}=V_{OUT}=2.5V, we have the following desirable properties:

1. maximum dc voltage gain,
2. dc cascadable,
3. the enhancement transistor operates at 90% of its maximum f_T and
4. dc gain and bias point is insensitive to variation in device width.

Small Signal AC Analysis

A first order analysis of the small signal equivalent circuit in figure 2.4 shows that the transfer function of the inverter has a real pole and a zero.

$$\frac{v_o}{v_{in}}(s) = -g_m R \frac{\left(1 - s\frac{C_{gd}}{g_m}\right)}{\left[1 + sR\left(C_l + C_{gd}\right)\right]} \tag{2.5}$$

where

$$R = r_{oE} \| r_{oD} \| \frac{1}{g_{mD}}$$

$$C_{gs} = C_{gsE} + C_{gsolE}$$

$$C_{gd} = C_{gdE} + C_{gdolE}$$

and

$$C_l = C_{in} + C_{sbD} + C_{dbE} + C_{gdD} + C_{gdolD}$$

C_{in} is the input capacitance of the next stage. C_{gsolE} and C_{gdolE} are the source and drain overlap capacitances of transistor M_E in figure 2.1, respectively. C_{gsE} and C_{gdE} are the small signal gate-to-source and gate-to-drain capacitance of transistor M_E when it is

operating in the saturation region. Other capacitances used in equation 2.5 are defined accordingly. Figure A-6 and table A-1 summarized the measured device and parasitic capacitances.

A word on the symbol convention for circuit elements (especially capacitances) adopted in this thesis is approapriate at this point. The lower case subscripts g, s, d, and b refer to the gate, the source, the drain and the bulk of a MOS transistor respectively. The subcript ol for a capacitor means overlap capacitance. A upper case subscript refers to a particular transistor named in the figure being considered. For example, C_{gdol_E} refers to the gate-to-drain overlap capacitance of transistor M_E in figure 2.1.

The pole has a magnitude equal to the reciprocal of the output RC time constant, and the zero which is due to the feed forward capacitor C_{gd}, has a magnitude higher than the f_T of the transistor. Substituting measured values into equation 2.5, the calculated pole magnitude is 800MHz, the inverter gain is 4.5, and the unity gain frequency is 3.6GHz. These calculated values agree well with the simulated results in figure 2.5, which shows the magnitude and phase response of the inverter when driving an identical inverter with $W=20\mu m$.

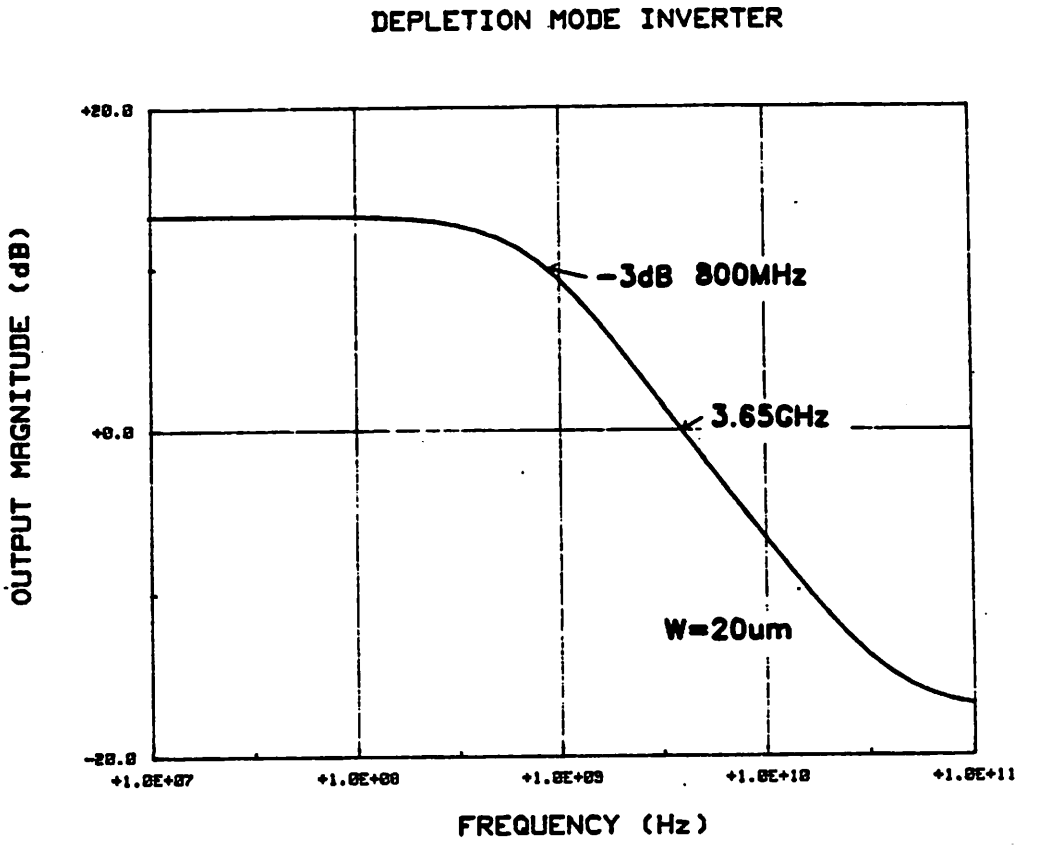
Referring to figure 2.4, the input impedance is

$$Z_i(s) = \frac{1}{s\left\{C_{gs}+C_{gd}\left[1+gmR\frac{\left(1-s\frac{C_{gd}}{gm}\right)}{\left[1+sR\left(C_l+C_{gd}\right)\right]}\right]\right\}} \tag{2.6}$$

At low frequencies, the input impedance is capacitive and the equivalent capacitance is

$$C_{in} = C_{gs}+C_{gd}\left(1+gmR\right) \tag{2.7}$$

where the term $\left(1+g_mR\right)$ represents the Miller multiplication factor. For the present design g_mR is 4.5, therefore Miller capacitance can be a considerable part of the total loading capacitance. Figure 2.6, the simulated input capacitance of the amplifier ($W=20\mu m$), agrees with equation 2.6. The simulated low frequency input capacitance per



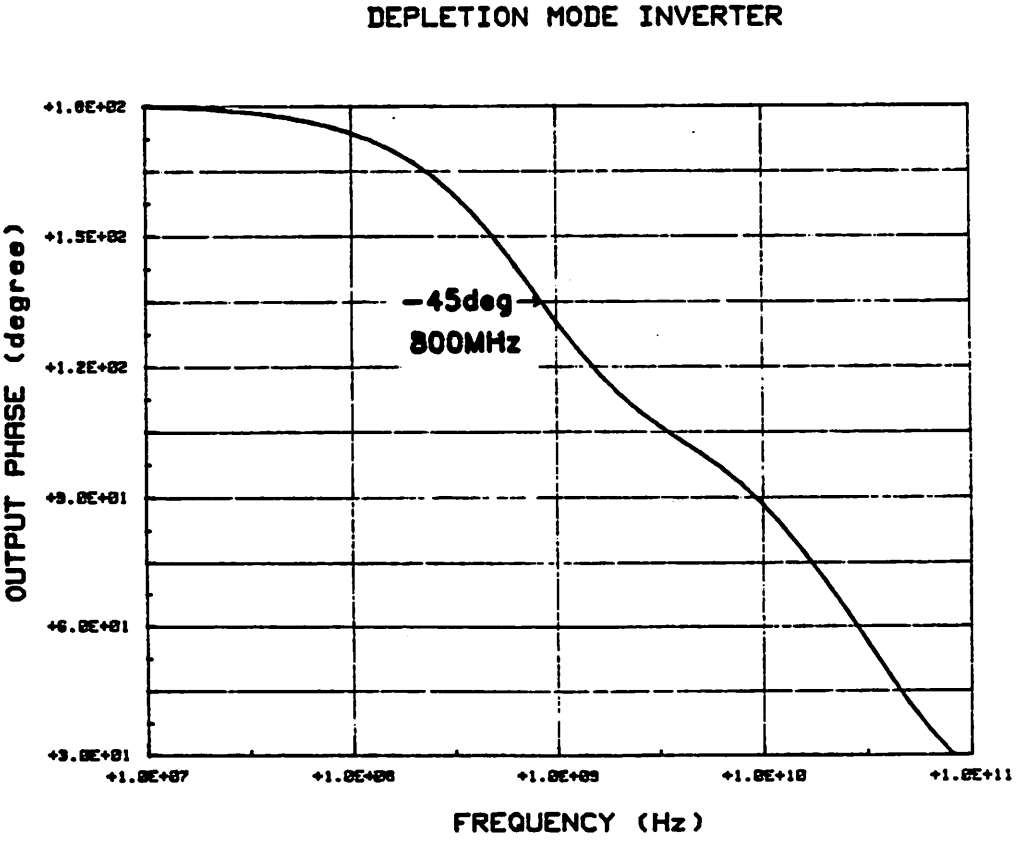


Fig. 2.5 Simulated frequency response of inverter.

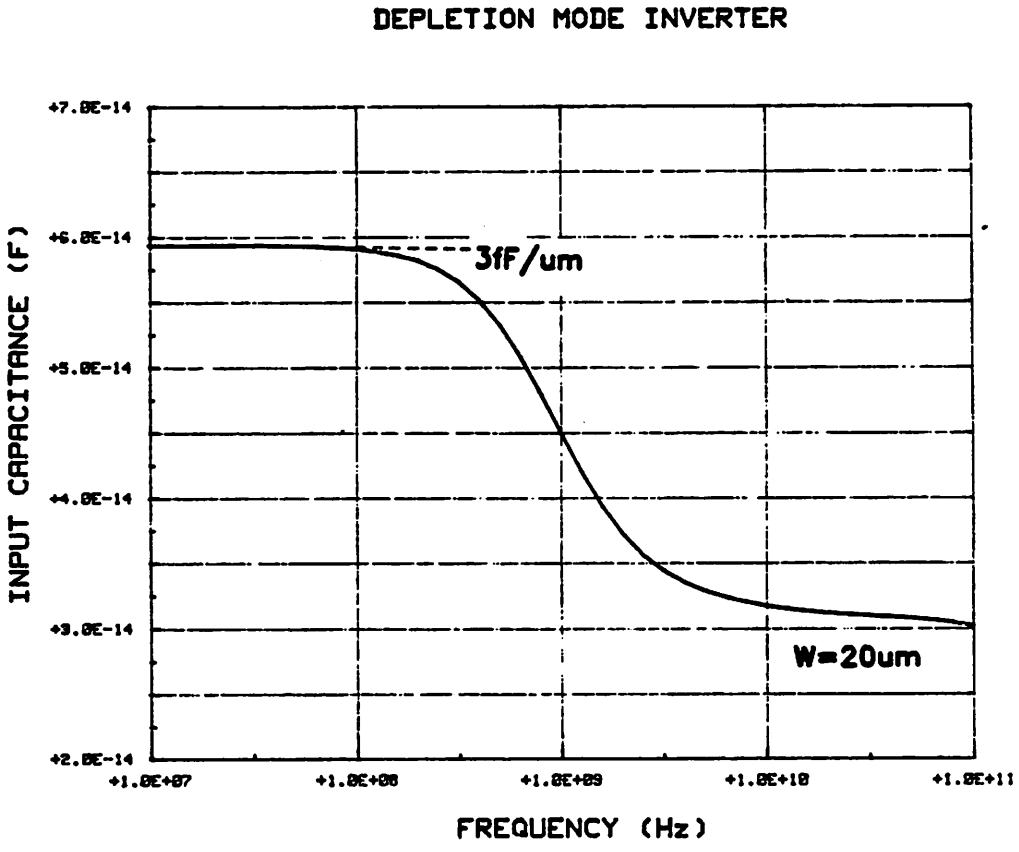


Fig. 2.6 Simulated input capacitance of inverter.

micron of gate width is about $3fF/\mu m$.

Disadvantages

Potentially, the simple depletion inverter can be used as a small signal amplifier to drive internal capacitance; unfortunately this circuit has many disadvantages:

1. The gain is proportional to device $g_m r_o$ therefore it is sensitive to temperature variations. r_o is especially sensitive to variations in channel length and punch-through implant.

2. The gain of the circuit is approximately equal to $\frac{g_m r_o}{2}$ and cannot be varied controllably by device ratioing in the layout without losing some of the advantages mentioned earlier.

3. The dc bias voltage for the gate of transistor M_E has to track with variations in threshold voltages since $V_{GSE}=V_{TE}-V_{TD}$. V_T in a NMOS process can vary by as much as $\pm 100mV$ from wafer to wafer.

4. A cascade of these inverters would suffer gain-bandwidth shrinkage since each stage has a single-pole response, making it unsuitable for high gain applications at high frequencies.

Because of these disadvantages, the inverter is only useful in some non-critical applications such as clock buffers and output drivers. In more demanding situations, negative feedback (section 2.3 and 2.4) has to be incorporated to improve overall amplifier performance.

2.1.2 Source Follower

DC Biasing and Other Considerations

Another type of open loop amplifier to be considered is the source follower shown in figure 2.7. This amplifier has only current gain which is suitable for driving capacitive load, and its voltage gain is less than 1. Its counterpart in bipolar technology is the emitter follower which is commonly used for level shifters and output drivers in circuits such as ECL, operational amplifiers, etc. In GaAs technology, the source follower is used extensively to drive 50Ω transmission lines and to perform level shifting in depletion mode GaAs logic. In this section we will investigate using this circuit in the MOS technology to drive capacitive loads.

Again based on an aspect ratio $\frac{W_1}{W_2}$ of 1, the design of the source follower is summarized in table 2.2. As in the case of the inverter, the one-one design minimizes parasitic capacitances at the output node and improves frequency response. Biasing point and dc gain of the circuit is also stablized against variations in device W. The dc voltage gain of the source follower is

$$\frac{v_o}{v_i} = \frac{g_{m1}R_o}{1+g_{m1}R_o} \tag{2.8}$$

where

$$R_o = r_{o1}||r_{o2}||\frac{1}{g_{mb1}}$$

Substituting the measured small signal device parameters in appendix A-1 into equation 2.8, the dc voltage gain is 0.78. The simulated dc transfer curve and dc gain of the source follower are plotted in figure 2.8. Notice that the transfer curve also goes through the point $V_{IN}=V_{OUT}=2.5V$. Apply equation 2.3 to the source follower in figure 2.7, and assuming both transistors in saturation and $W_1=W_2$, we have

$$\begin{aligned} V_{IN}-V_{OUT} &= V_{GS1} \\ &= V_{TD1}-V_{TD2} \\ &= V_{TD}\Big|_{V_{SB}=7.5V} - V_{TD}\Big|_{V_{SB}=5V} \end{aligned}$$

Since body effect is small in short channel devices, $V_{IN}-V_{OUT}$ is approximately 0V (refer to figure A-4). This design is intended to achieve current gain with no dc level shift. Level shifting is not

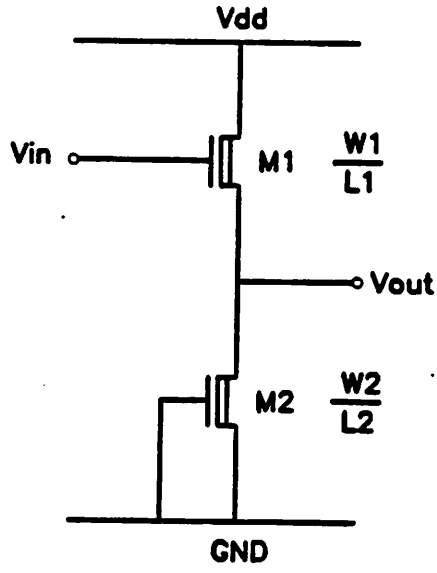


Fig. 2.7 Source follower.

Design Parameters	
Vdd	+5V
Vss	−5V
W1	W
L1	1um
W2	W
L2	1um
Vtd	−1.5V

Table 2.2 Summary of Source Follower Design.

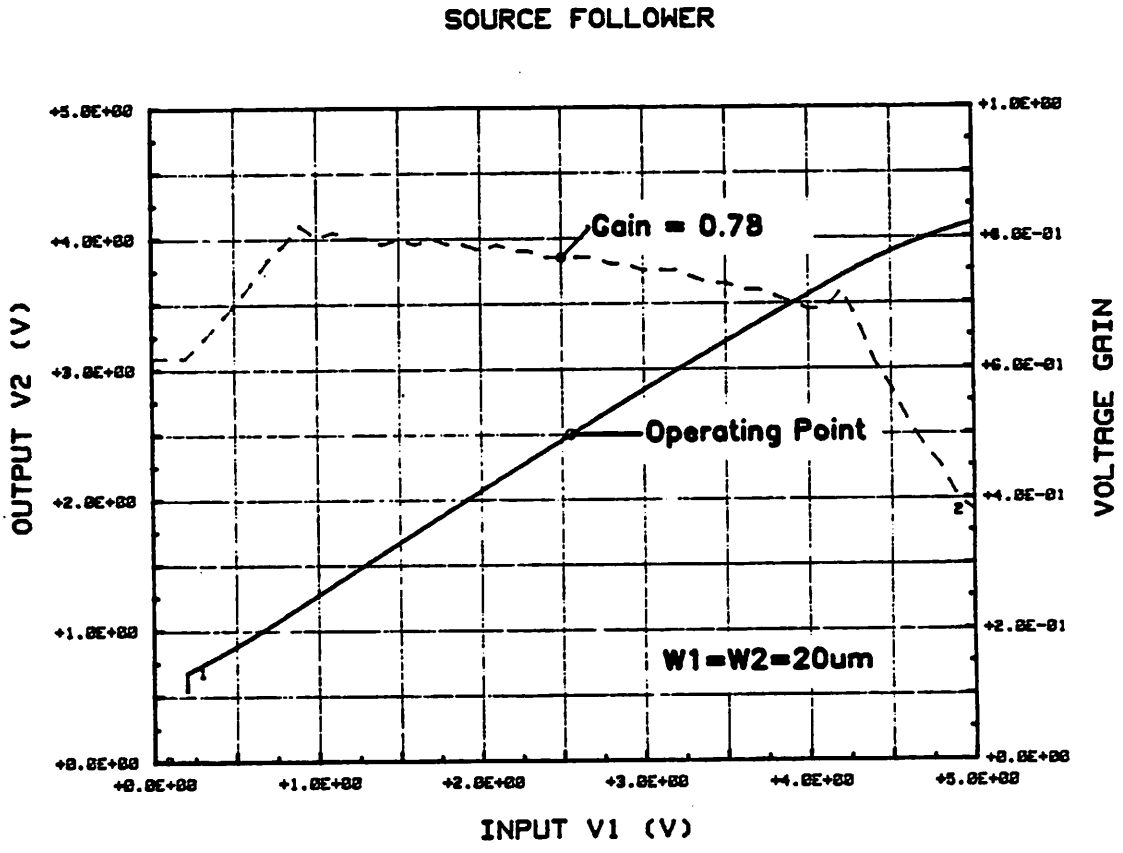


Fig. 2.8 Simulated DC transfer curve and gain of source follower.

called in a E/D NMOS technology because the inverter is dc cascadable.

The desired dc operating point of this circuit is again at $V_{IN}=V_{OUT}=2.5V$ making it dc cascadable either to itself or to the inverter amplifier in the previous section. $V_{GS1}-V_{TD1}$ is 1.5V, thus g_m of transistor M_1 is at 90% of its maximum value.

Small Signal AC analysis

The small signal equivalent circuit of figure 2.7 is shown in figure 2.9 where

$$R_o = r_{o1}||r_{o2}||\frac{1}{g_{mb_1}} \tag{2.9}$$

$$C_l = C_{load}+C_{sb_1}+C_{db_2}+C_{gd_2}+C_{gdol_2}$$

$$C_{gd} = C_{gd_1}+C_{gdol_1}$$

and

$$C_{gs} = C_{gs_1}+C_{gsol_1}$$

The symbol convention for circuit elements here is similar to those in equation 2.5. The subscripts 1 and 2 refer to transistor M_1 and M_2 in figure 2.7. This equivalent circuit is based on the hybrid-π model and can be easily transformed to the Y-parameter equivalent circuit in figure 2.10. Y-parameter representation is especially convenient when analyzing circuits with two port shunt-shunt feedback. By definition,

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2.10}$$

where

$$Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = s\left(C_{gs}+C_{gd}\right)$$

$$Y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = -sC_{gs}$$

$$Y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} = -g_m-sC_{gs}$$

$$Y_{22} = \left.\frac{i_2}{i_2}\right|_{v_1=0} = sC_l+\frac{1}{R_o}+g_m+sC_{gs}$$

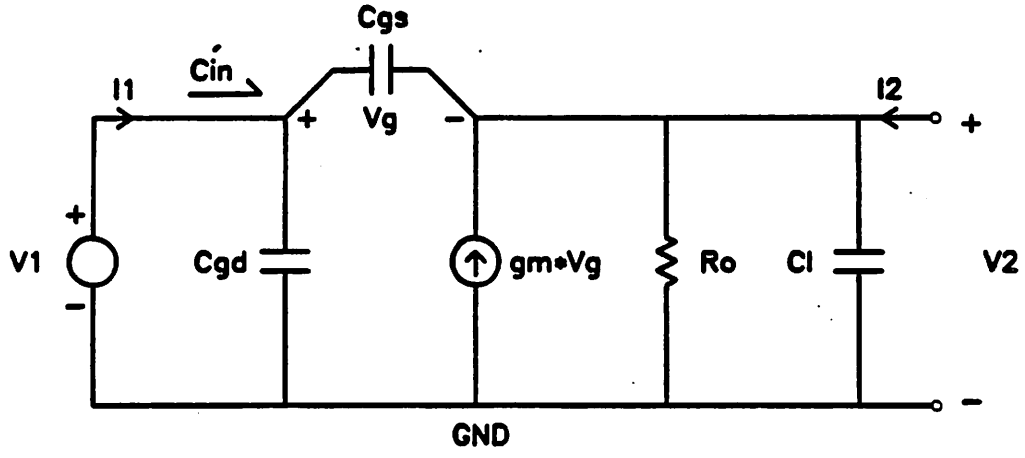


Fig. 2.9 Small signal equivalent circuit of source follower.

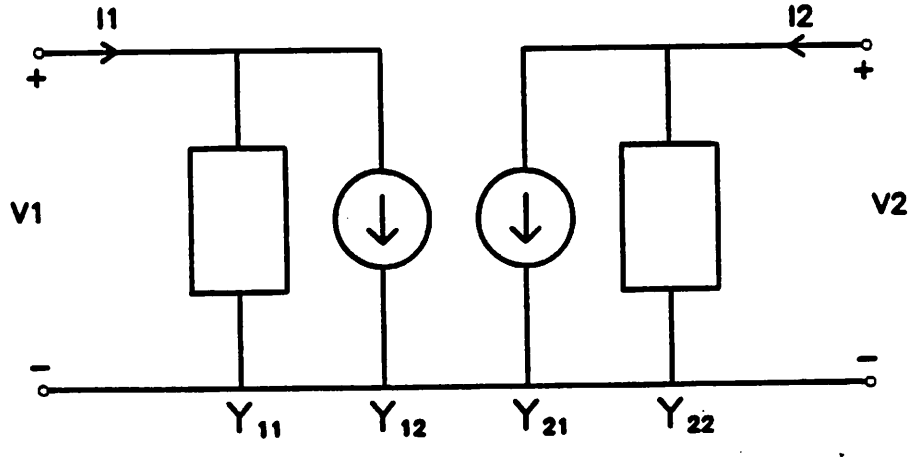


Fig. 2.10 Y-Parameter two-port representation of source follower.

Using the Y-parameter representation, the circuit frequency response is calculated by setting $i_2=0$ in equation 2.10 and solving for v_2,

$$\frac{v_2}{v_1}(s) = -\frac{y_{21}}{y_{22}} \tag{2.11}$$

$$= \frac{1+s\frac{C_{gs}}{g_m}}{1+\frac{1}{g_m R_o}+s\frac{C_{gs}+C_l}{g_m}}$$

Rearranging terms in equation 2.11, we have

$$\frac{v_2}{v_1}(s) = \frac{G\left(1+\frac{s}{z}\right)}{\left(1+\frac{s}{p}\right)} \tag{2.13}$$

where

$$G = \frac{g_m R_o}{1+g_m R_o} \tag{2.12}$$

$$z = \frac{g_m}{C_{gs}}$$

and

$$p = \frac{g_m}{G\left(C_{gs}+C_l\right)}$$

The pole p of the transfer function depends on loading capacitor C_l, and the zero z is at a frequency close to the device f_T.

A sequence of simulations was performed on the circuit shown in figure 2.11 where a source follower was used to drive the one-one inverter of the previous section. The width of the inverter was varied such that the ratio of inverter width to source follower width ($\frac{W_{inv}}{W_{sf}}$) of $\frac{10\mu m}{20\mu m}$, $\frac{20\mu m}{20\mu m}$, $\frac{40\mu m}{20\mu m}$, and $\frac{60\mu m}{20\mu m}$ were used in the simulation of figure 2.12. The corresponding -3dB bandwidth of the source followers are 10GHz, 4GHz, 2GHz, and 1.5GHz respectively, and the simulated transfer function exhibits one pole and one zero.

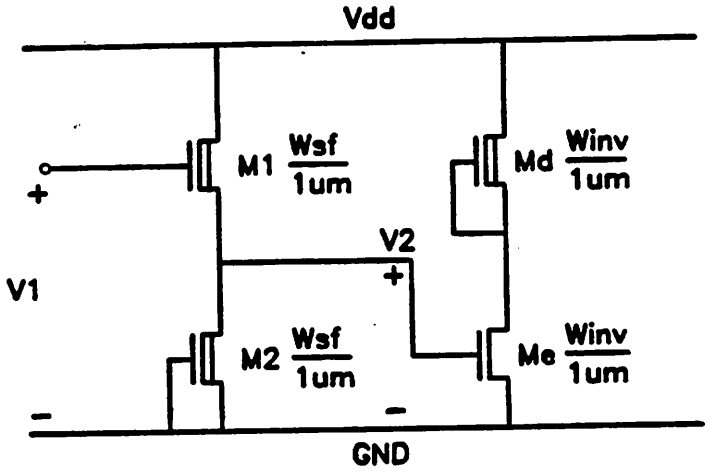
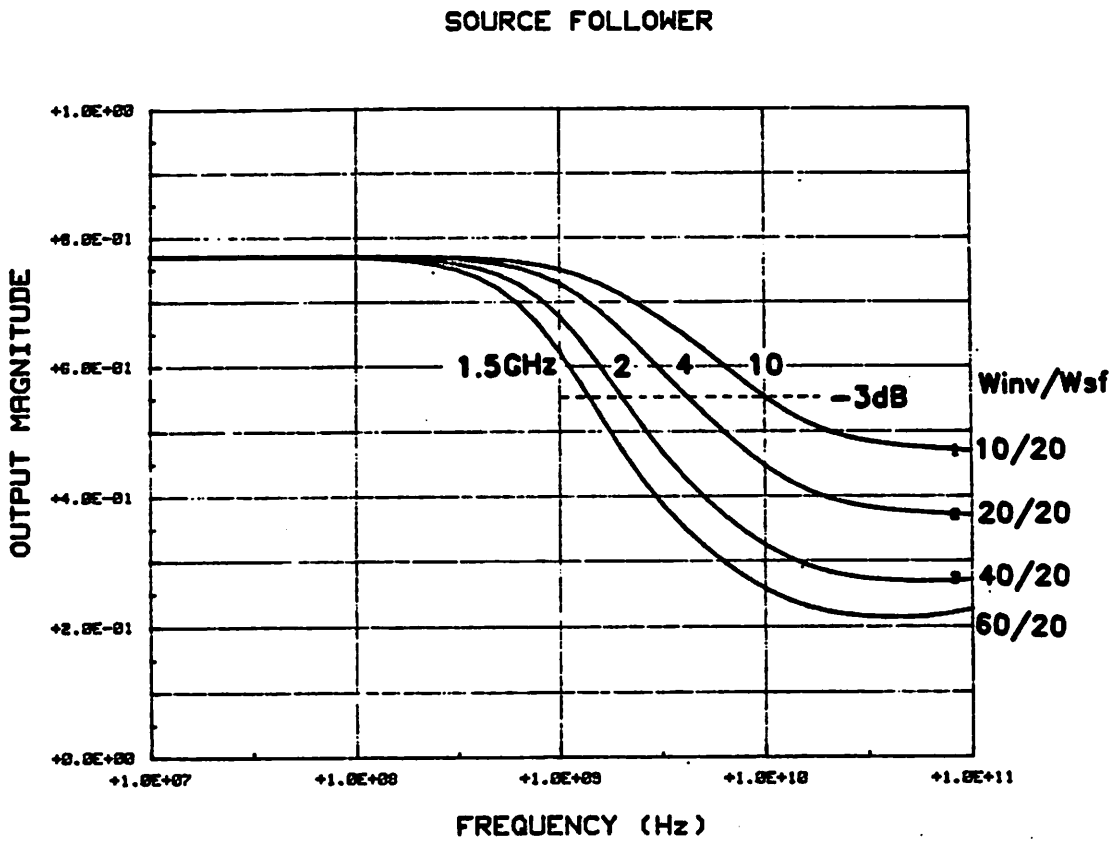


Fig. 2.11 Circuit used in source follower simulations.



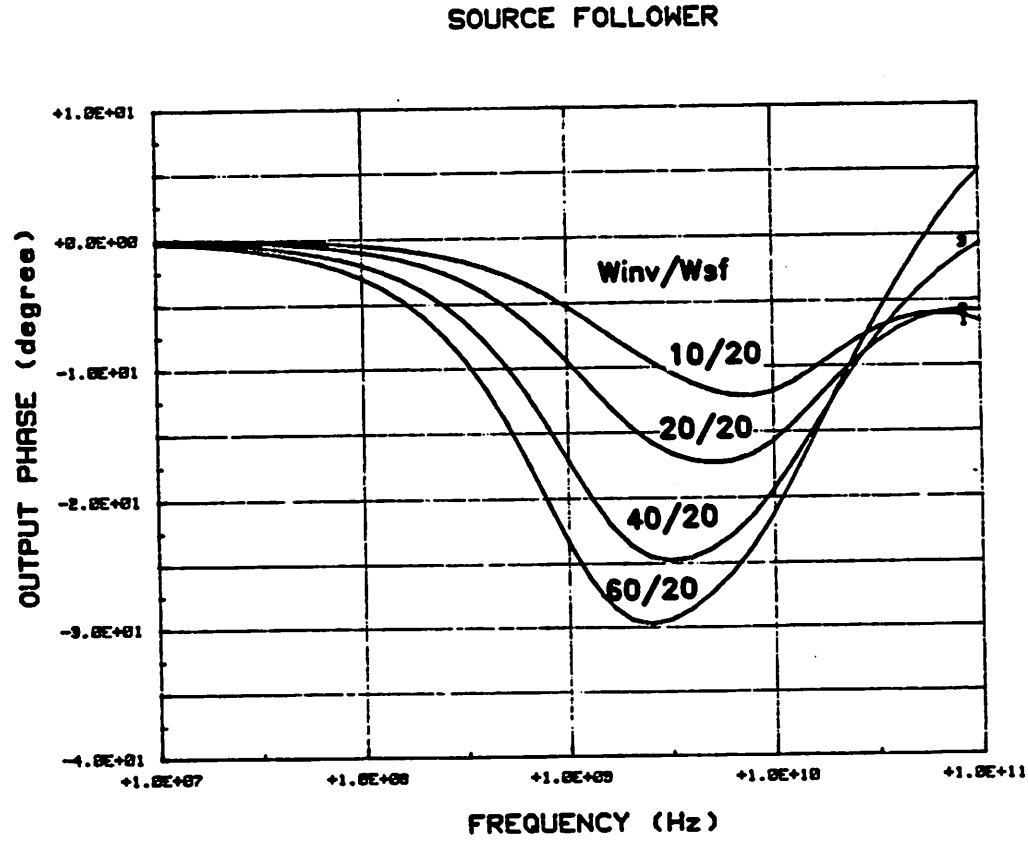


Fig. 2.12 Simulated frequency response of source follower.

The source follower is useful as a buffer to drive large on-chip capacitance from dc to frequencies above 1GHz. Its efficiency depends on its input capacitance. The input impedance is defined as

$$\left.\frac{i_1}{v_1}(s)\right|_{i_2=0} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22}} \tag{2.14}$$

$$= s\left[C_{gd} + C_{gs}\left(1 - G\frac{\left(1+\frac{s}{z}\right)}{\left(1+\frac{s}{p}\right)}\right)\right]$$

At low frequencies, the input impedance is capacitive and the equivalent input capacitance is

$$C_{in}\Big|_{s=0} = C_{gd} + C_{gs}(1-G) \tag{2.15}$$

At high frequencies, input impedance is also capacitive with an equivalent input capacitance

$$C_{in}\Big|_{s=\infty} = C_{gd} + C_{gs}\left(\frac{C_l}{C_{gs} + C_l}\right) \tag{2.16}$$

Simulated input capacitance of the source follower when driving inverters of different W_{inv} is plotted in figure 2.13. Input capacitance of the source follower at low frequencies is $0.6fF/\mu m$, which is in agreement with equation 2.15. At high frequencies, simulated results agree well with values given by equation 2.16.

In summary, the source follower in figure 2.11 with $\frac{W_{inv}}{W_{sf}}=1$ has a voltage gain of 0.78 and a -3dB bandwidth of 4GHz. In the SiGMOS technology, its input capacitance is 0.6fF per micron of gate width and its loading capacitance (the input capacitance of the inverter) is $3fF/\mu m$. Therefore its capacitance buffering ratio is 1:5, making it suitable in many applications such as clock drivers and output buffers.

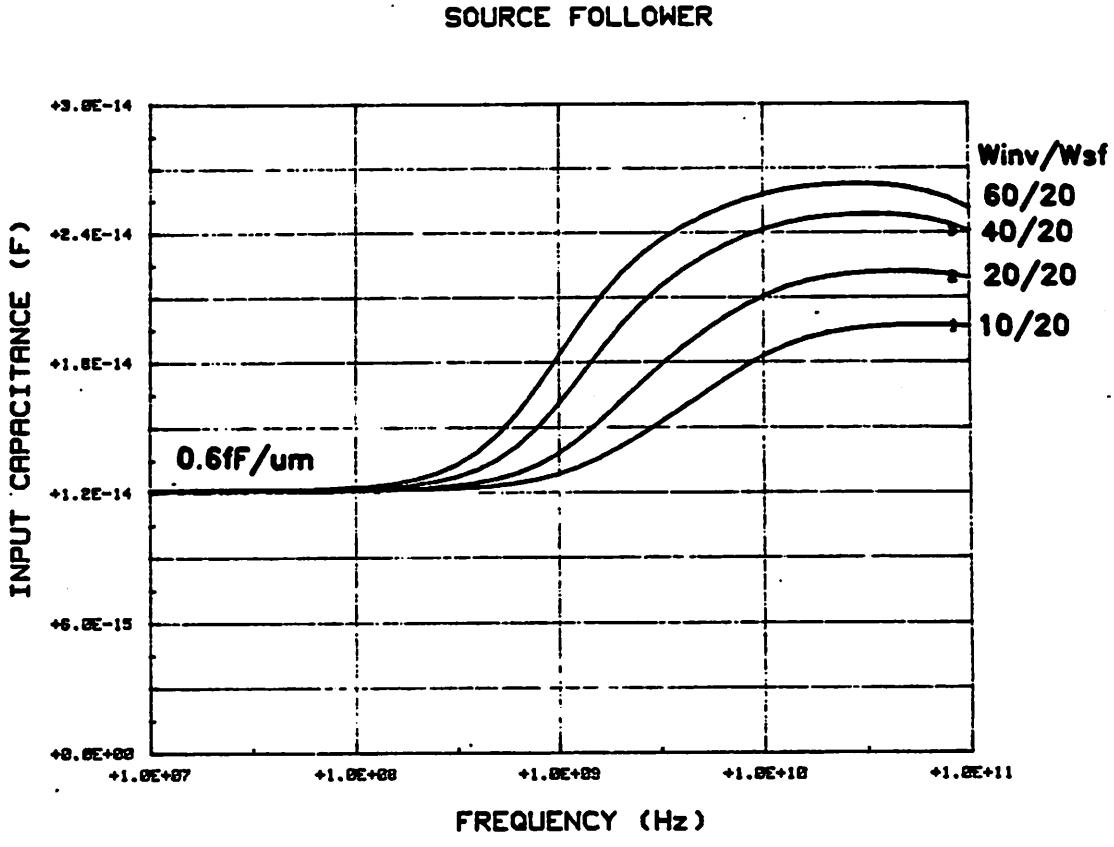


Fig. 2.13 Simulated input capacitance of source follower.

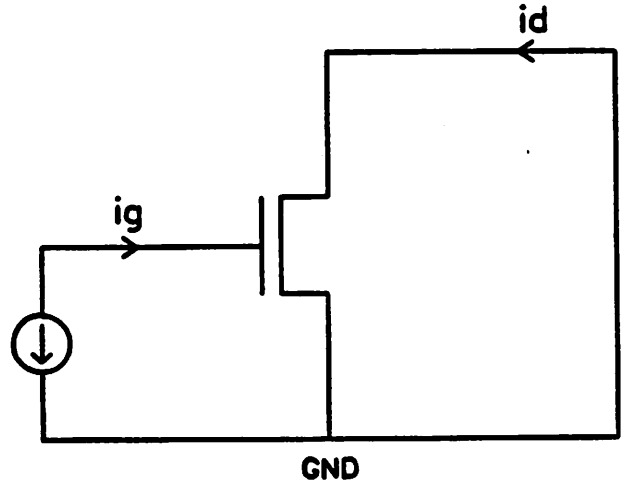


Fig. 2.14 Circuit used in f_T definition.

2.2 Transistor f_T, GBW, and τ_d

Transistor unity gain frequency (f_T), gain-bandwidth product (GBW), and ring oscillator stage delay (τ_d) are frequently used as figures of merit for the sake of comparisons. Care must be taken when using these figures because if we compare f_T of one process to the $\frac{1}{2\pi\tau_d}$ of another, we are comparing different quantities. In this section, we try to define the relationship between these figures, and more importantly, to give an idea about the speed performance of the SiGMOS technology.

In section 2.2.1, f_T of a MOS transistor is defined and plotted as function of its biasing voltages. In section 2.2.2, GBW and Gain-bandwidth shrinkage of some open loop amplifiers are considered. Finally in section 2.2.3 τ_d for the SiGMOS process is evaluated.

2.2.1 Transistor f_T

f_T is commonly defined as the frequency at which the transistor current gain $\frac{i_d}{i_g}$ equals unity when the transistor is connected as shown in figure 2.14. An equivalent statement for f_T is the frequency at which h_{21} of the h-parameter 2 port representation equals one.

Direct measurement of h_{21} at high frequencies is usually difficult since a low inductance short circuit is difficult to realize. Generally, s-parameters are measured instead and then convertered to h_{21} using [3]

$$h_{21} = \frac{-2S_{21}}{\left(1-S_{11}\right)\left(1+S_{22}\right) + S_{12}S_{21}} \tag{2.17}$$

This method requires the use of a high frequency vector network analyzer and a powerful computer. Transistor width should be large so that C_g is much larger than package parasitics. Alternatively, accurate terminations can be used to calibrate the reference planes right up to the transistor input and output.

A simpler, but less accurate method to measure f_T is to measure the small signal transistor parameters used in Spice AC model and then calculate or simulate f_T using the equivalent circuit shown in figure 2.15. In figure 2.15, C_{gs} and C_{gd} are the total gate-to-source and gate-to-drain capacitance of the transistor respectively. They include the overlap capacitance of the transistor. The accuracy of this method is limited by the validity of the model used. By inspecting the equivalent circuit in figure 2.15,

$$\frac{i_d}{i_g}(s) = \frac{g_m\left[1-s\frac{C_{gd}}{g_m}\right]}{s\left[C_{gs}+C_{gd}\right]} \tag{2.18}$$

Since C_{gd} is usually less than C_{gs},

$$f_T \approx \frac{g_m}{2\pi\left[C_{gs} + C_{gd}\right]} \tag{2.19}$$

For a $1\mu m$ MOS transistor (effective channel length = $1\mu m$) biased at $V_{GS}-V_T=1.5V$ and

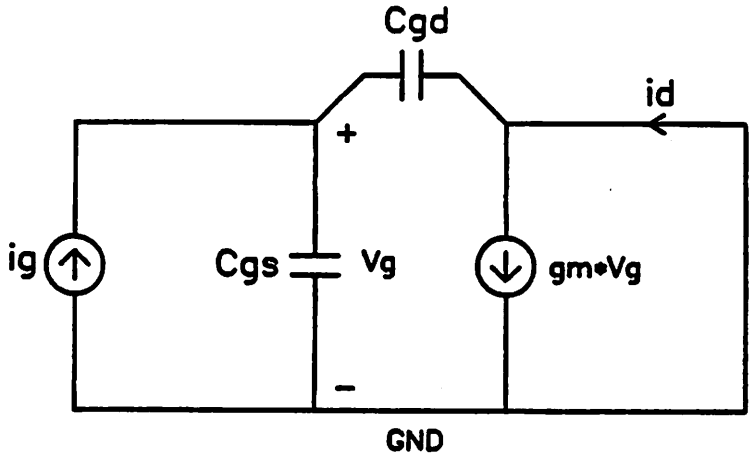


Fig. 2.15 Equivalent circuit used in f_T calculation.

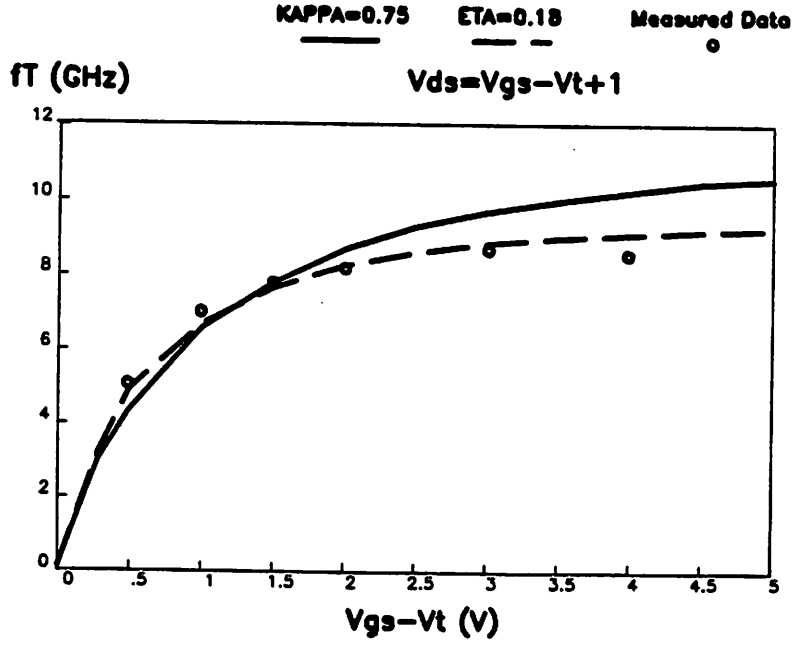


Fig. 2.16 Transistor f_T versus bias voltage.

V_{DS}=2.5V, measured g_m from figure A-1 is 80$\mu A/V\mu m$ (80mS/mm). Using measured values of C_{gs}, C_{gd}, C_{gsol} and C_{gdol} from table A-1. f_T equals 8.2GHz. (If one considers that overlap capacitances are extrinsic to the device and wishes to exclude them in the calculation, then f_T equals 10.2GHz.)

Figure 2.16 compares the simulated f_T using Spice to the measured f_T using s-parameters. The close agreement implies that the model used in Spice is accurate. Note that f_T reaches 90% of its maximum value when $V_{GS}-V_T$ equals 1.5V.

2.2.2 Gain-Bandwidth Product - GBW

GBW of the Depletion Mode Inverter

From the previous section, f_T of a $1\mu m$ MOS transistor is about 9 GHz. This figure can rival the best that bipolar technology has to offer [4]. Unfortunately, parasitic capacitances are important in the SiGMOS technology and they degrade the speed performance of the transistors in an integrated circuit.

Consider the gain-bandwidth product of the inverter in section 2.1 (figure 2.1). From equation 2.5,

$$G = g_m R \tag{2.20}$$

and

$$BW = \frac{1}{2\pi R\left(C_{total}\right)}$$

Therefore

$$GBW = \frac{g_m}{2\pi\left(C_{total}\right)} \tag{2.21}$$

$$C_{total} = C_l + C_{gd}$$

If the inverter is driving an identical inverter stage, equation 2.7 can be used with equation 2.5 to give

(2.22)

$$C_{total} = C_{gs_E} + C_{gsol_E} + \left(C_{gd_E} + C_{gdol_E}\right)\left(1 + g_m R\right) + C_{sb_D} + C_{db_E} + C_{gd_D} + C_{gdol_D} + C_{gd_E} + C_{gdol_E}$$

The subscripts E and D refer to transistor M_E and M_D in figure 2.1. $C_{sb_D} + C_{db_E}$ is the junction capacitance of the output node to the silicon substrate. It consists of two components -

an area junction capacitor and a sidewall junction capacitor. Looking at figure 2.2, the sidewall junction capacitor does not scale with the inverter width W, whereas, all other capacitive components in equation 2.22 do scale with W. Figure 2.17 shows the simulated magnitude and phase response of the inverter with four different W designs (W equals $2\mu m$, $5\mu m$, $10\mu m$ and $20\mu m$). Using data from figure 2.17, GBW versus W is plotted in figure 2.18. Comparing equation 2.21 to equation 2.19, we see that the combined effects of parasitic capacitances and Miller multiplication reduce the GBW to only 45% of f_T which is 8.2GHz. Since only the sidewall junction capacitance does not scale with W, for W larger than $10\mu m$ GBW approaches 3.65GHz in figure 2.18.

Gain-bandwidth Shrinkage of a Cascade of Inverters

As mentioned in section 2.1, one way to achieve small signal gain is by cascading N identical inverters in series. If the gain is G and the -3dB bandwidth is BW for a single inverter stage, then the overall gain for N stages is simply

$$G_N = G^N$$

and the overall bandwidth is

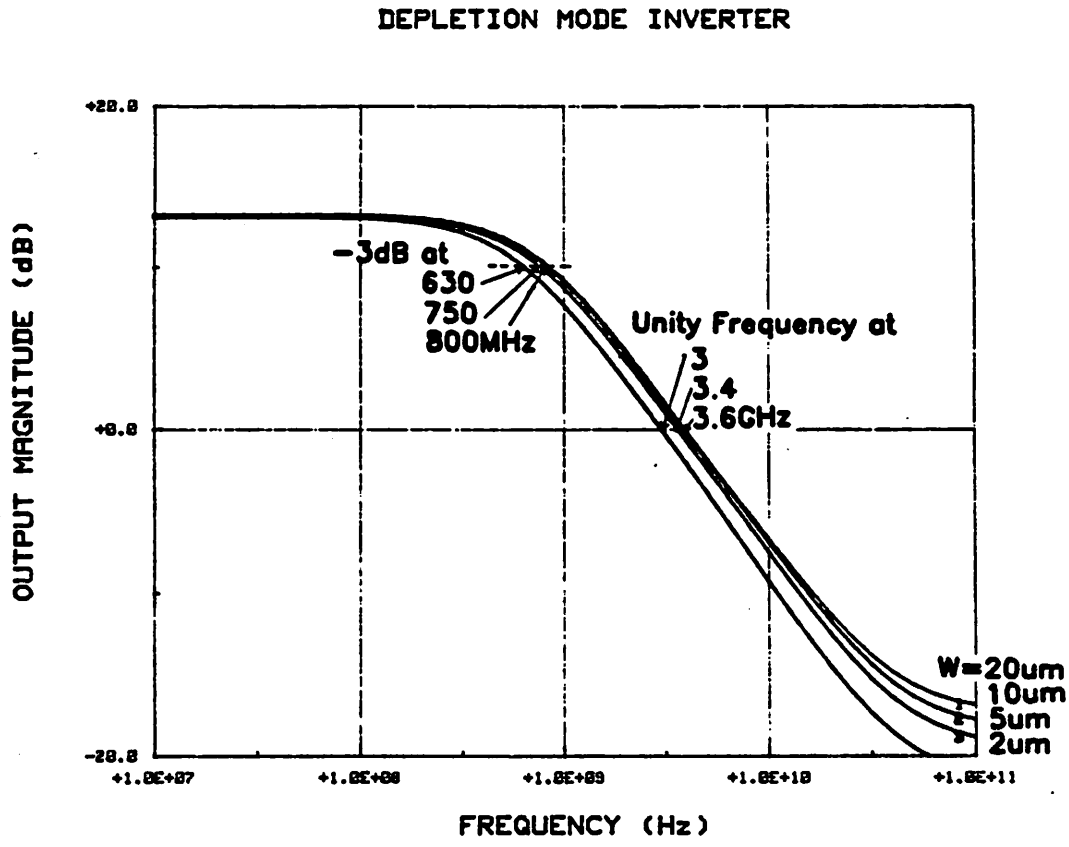
$$BW_N = BW\left(2^{\frac{1}{N}}-1\right)^{1/2}$$

The total gain-bandwidth product is

$$GBW_N = G^N BW\left(2^{\frac{1}{N}}-1\right)^{1/2} \tag{2.24}$$

which is clearly larger than the gain-bandwidth product for a single stage (GBW_1). A useful figure of merit in multi-stage amplifier designs is to use the normalized gain-bandwidth product $G_N^{\frac{1}{N}}BW_N$. For N stages,

$$G_N^{\frac{1}{N}}BW_N = GBW\left(2^{\frac{1}{N}}-1\right)^{1/2} \tag{2.25}$$



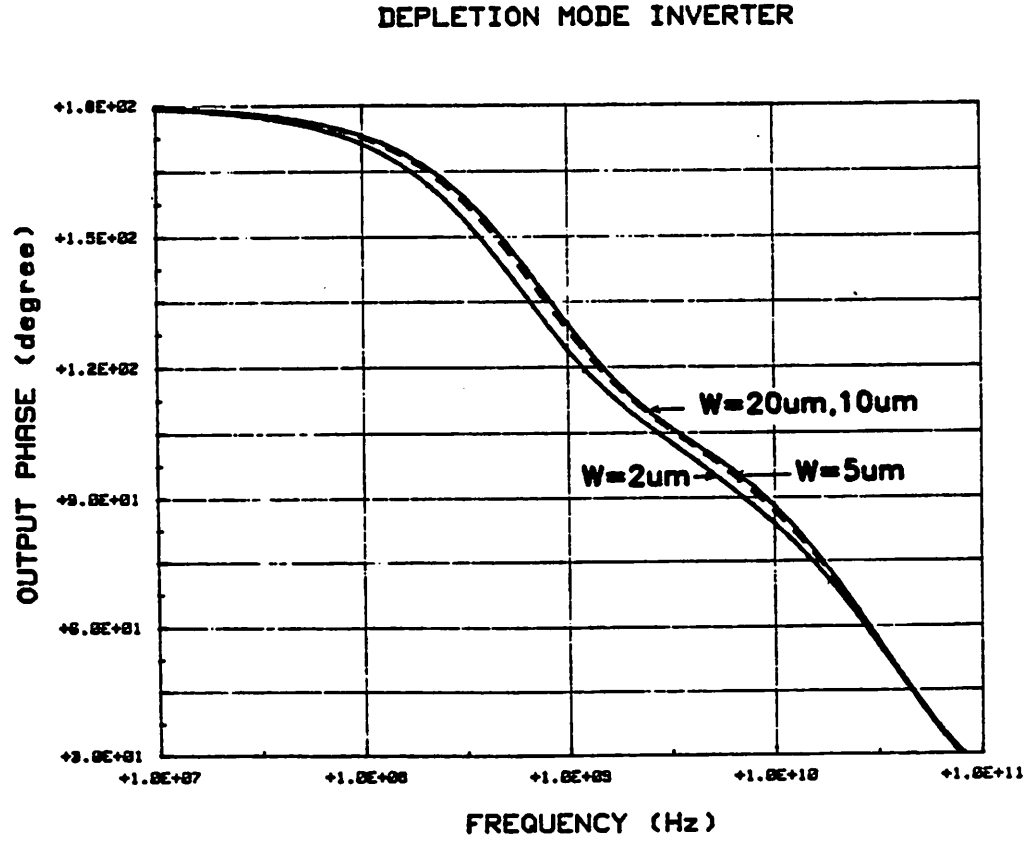


Fig. 2.17 Simulated frequency response of inverters with different width W.

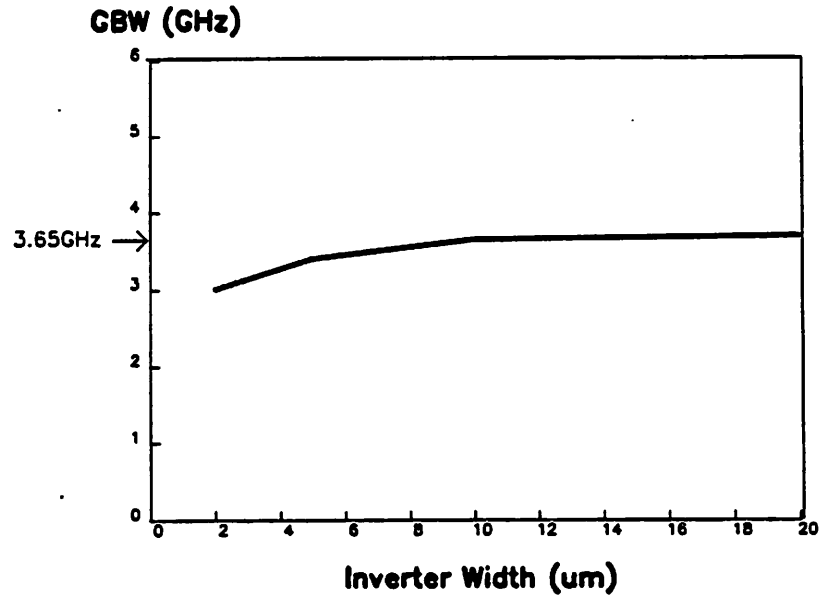


Fig. 2.18 Gain-bandwidth product of inverter versus width.

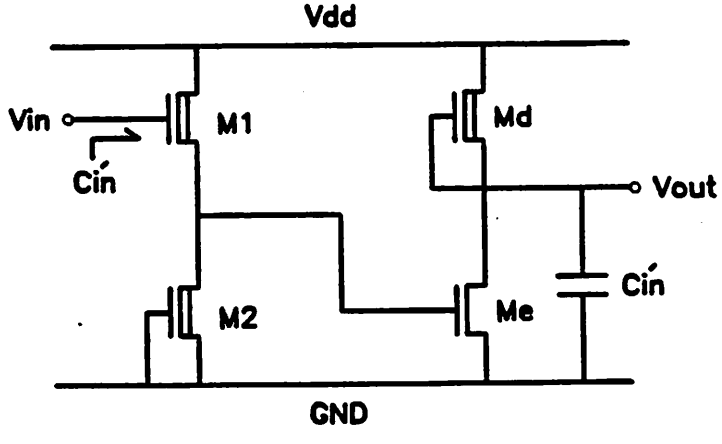


Fig. 2.19 Common-drain-common-source pair.

For N=2, normalized GBW equals $0.643\times GBW$. In other words, normalized gain-bandwidth shrinks by 36% if we cascade two single-pole amplifiers in series. In section 2.3, we will show that the normalized GBW of a feedback amplifier can approach GBW_1.

GBW of a CD-CS Pair

In bipolar technology a common-collector-common-emitter configuration is used as a composite device to improve the input impedance and current gain of the bipolar transistor. The equivalent configuration in the MOS technology is the common-drain-common-source (CD-CS) pair shown in figure 2.19. This configuration is useful because the input capacitance of the composite connection is reduced as given by equation 2.14. By combining equation 2.5, 2.7, 2.9, 2.13, and 2.15 , the transfer function of the CD-CS pair has two poles and two zero.

$$\frac{v_o}{v_{in}}(s) = \frac{-g_m RG\left[1+\frac{s}{z_1}\right]\left[1+\frac{s}{z_2}\right]}{\left[1+\frac{s}{p_1}\right]\left[1+\frac{s}{p_2}\right]} \tag{2.26}$$

where

$$z_1 = \frac{g_{m_1}}{C_{gs_1}+C_{gsol_1}}$$

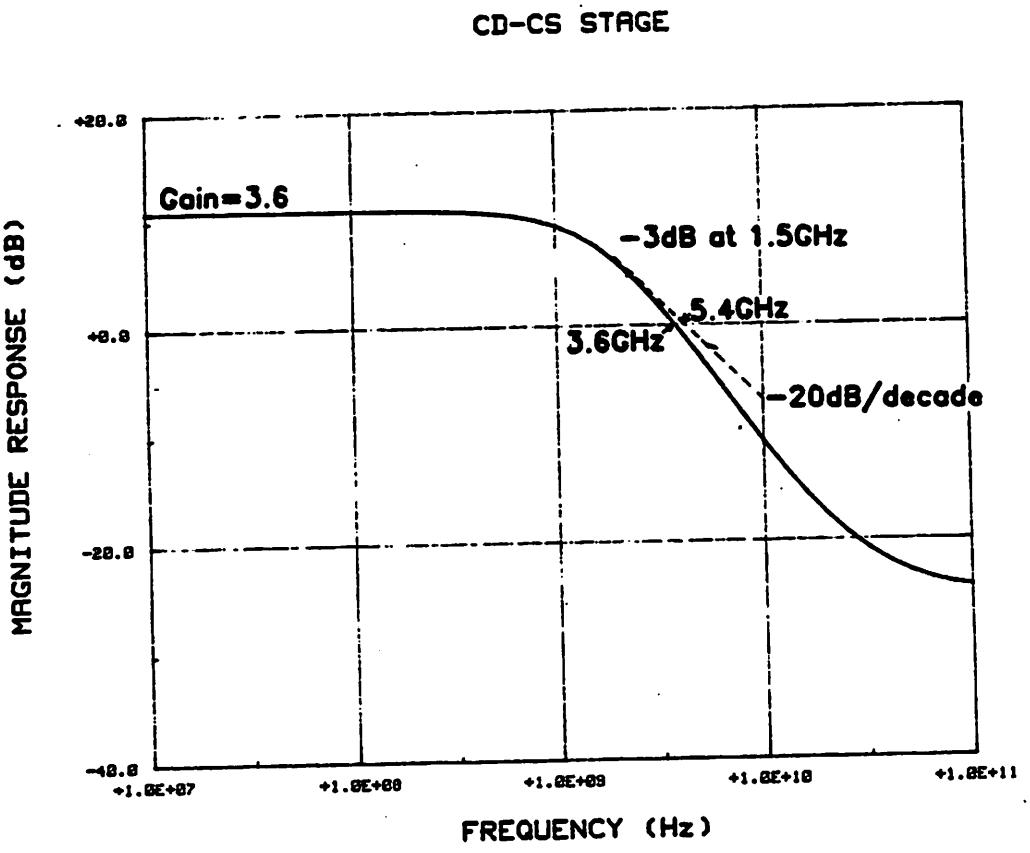
$$z_2 = \frac{g_{m_E}}{C_{gd_E}+C_{gdol_E}}$$

$$p_1 = \frac{g_{m_1}}{G\left[C_{gs_1}+C_{gsol_1}+C_{sb_1}+C_{db_2}+C_{gd_2}+C_{gdol_2}+C_{gs_E}+C_{gsol_E}+\left(C_{gd_E}+C_{gdol_E}\right)\left(1+g_m R\right)\right]}$$

$$p_2 = \frac{1}{R\left[C_{gd_E}+C_{gdol_E}+C_{sb_D}+C_{db_E}+C_{gd_D}+C_{gdol_D}+C_{gd_1}+C_{gdol_1}+\left(C_{gs_1}+C_{gsol_1}\right)\left(1-G\right)\right]}$$

The subscripts E, D, 1 and 2 refer to those transistors in figure 2.19. G and R are defined in equation 2.12 and 2.5 respectively. Qualitatively, z_1 is at the transistor f_T, z_2 can be neglected, p_1 is near GBW_1 (equation 2.21) and p_2 is somewhat less than GBW_1 depending

on the value of R. DC gain of the CD-CS pair is $g_m R \times G$, which is equal to 3.5 (4.5×0.78). The -3dB bandwidth of the composite pair is harder to determine since there are two interacting poles in the transfer function. So relying on computer simulation, the transfer function for the CD-CS pair is plotted in figure 2.20. The simulated -3db bandwidth is at 1.5GHz, therefore the GBW of the CD-CS stage is 5.4GHz. Because this is a two-stage amplifier, the normalized gain-bandwidth product is $G_2^{\frac{1}{2}} BW_2$, which equals 2.8GHz. The fact that this is less than the GBW of the inverter (3.65GHz) means that the CD-CS stage is not very effective in trading power dissipation for small signal bandwidth as compared to other circuit technigues such as feedback. Since the frequency response of a CD-CS pair has a single-pole roll off characteristic at frequencies between p_1 and p_2, it can be considered as a single-stage inverter with effective GBW product at 5.4GHz. This is analogous to the concept of *composite transistor* in bipolar circuit designs [7]. It is shown in section 2.3.2 that the use of the CD-CS configuration (together with feedback) can extend the bandwidth of feedback amplifiers.



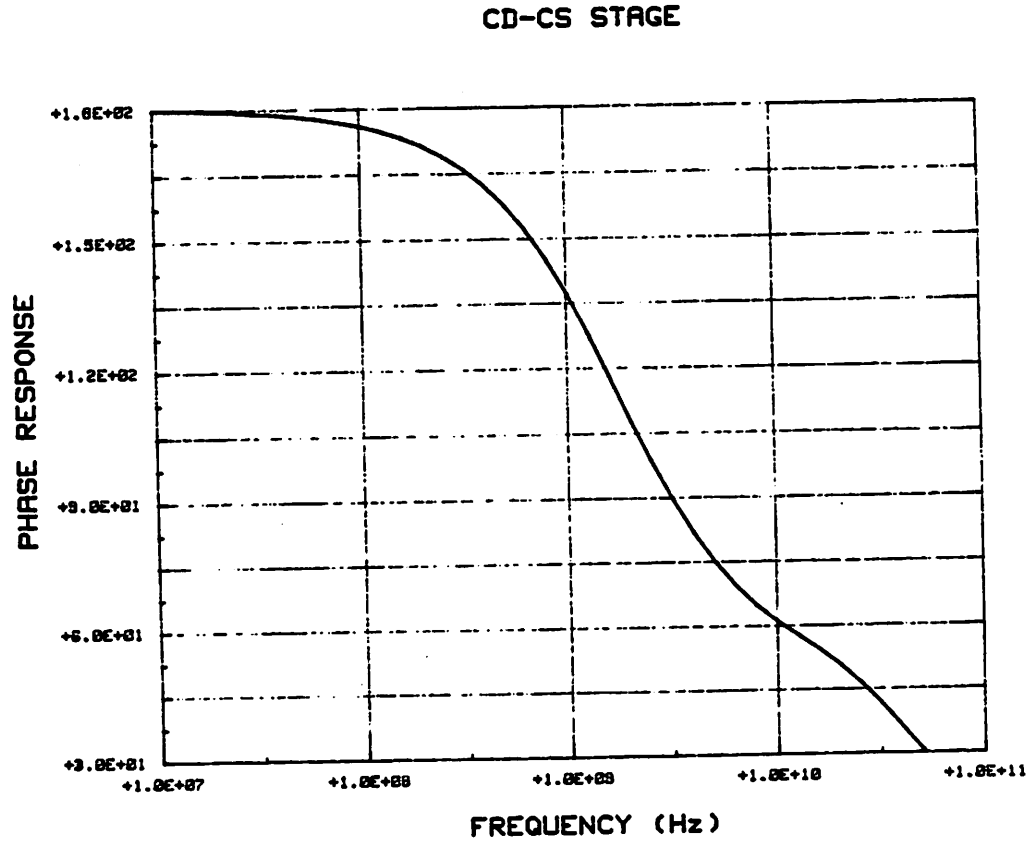


Fig. 2.20 Simulated frequency response of CD-CS stage.

2.2.3 Ring Oscillator Stage Delay - τ_d

Ring oscillator stage delay, τ_d, is the most common figure of merit in current use. It indicates the speed performance of the technology and the delay in digital circuits. Its popularity arises from the fact that it is relatively easy to measure accurately. At this time, the best reported value for τ_d on silicon is in NMOS technology [35] where a τ_d of 28ps has been achieved with $0.35\mu m$ channel length MOS transistors. However, Si-bipolar technology is rapidly improving with the fastest ring osillator speed reported at 30ps for an emitter window of $0.35\mu m$ wide [4].

To obtain an analytical closed form solution for τ_d is not a trivial task because the ring oscillator is a non-linear circuit. Recently, Bayruns et al. [6] have attempted a solution based on a system of piece-wise linear approximations. The mathematics used in the derivation is quite involved, so only the final result is repeated here for reference.

$$\tau_d = C_o \frac{NM0}{2} I' + 0.5 \left(\frac{2NM1 C_{out} C_{in}}{g_m I'} \right)^{1/2} \tag{2.27}$$

where C_o, C_{in} and C_{out} are the total capacitance at the output of the first stage, the input of the second stage, and the output of the second stage respectively. NM1 and NM0 are the high and low noise margins respectively. I' is approximately the current of the load device.

The easiest way to estimate τ_d is to perform a transient analysis on computer. A simulated output is shown in figure 2.21 for a five stage ring oscillator with inverter width W of $10\mu m$. The simulated stage delay of 74ps compares well with our measured ring oscillator stage delay of 70ps. From the previous section, GBW_1 of an inverter is about 3.6GHz, and transistor f_T is 9 GHz. Using these values, we find

$$f_T \approx 2.5 GBW_1 \approx \frac{4.18}{2\pi\tau_d} \tag{2.28}$$

Equation 2.28 is only valid for the SiGMOS technology using one-one inverter design. In

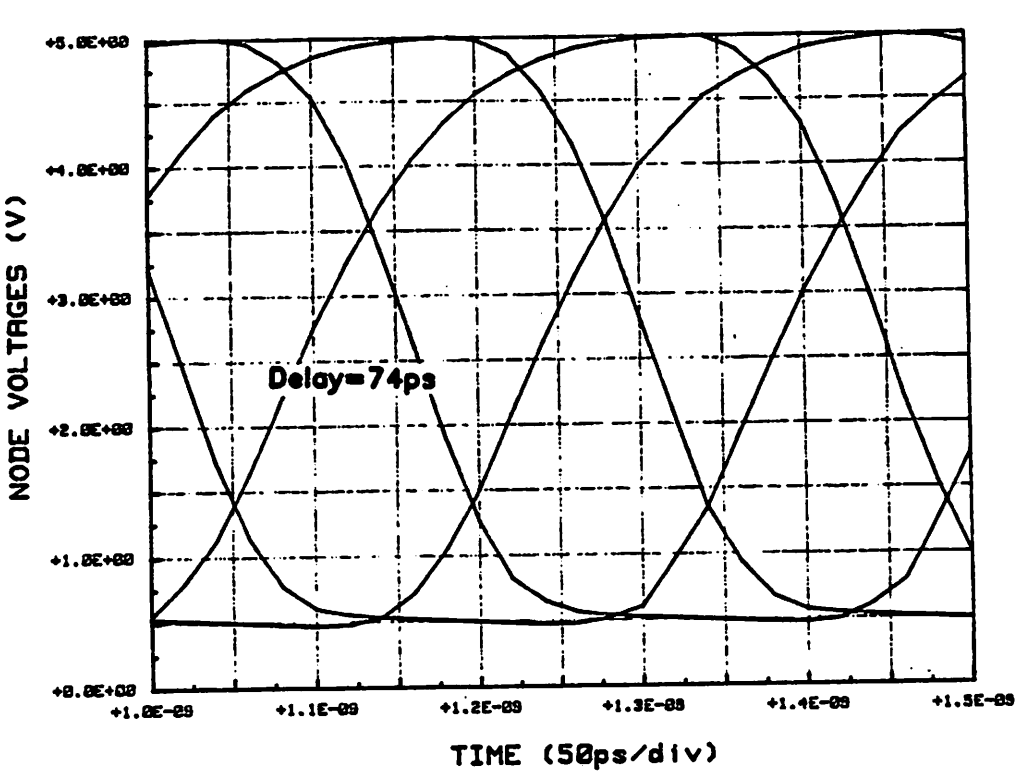


Fig. 2.21 Simulated ring oscillator delay.

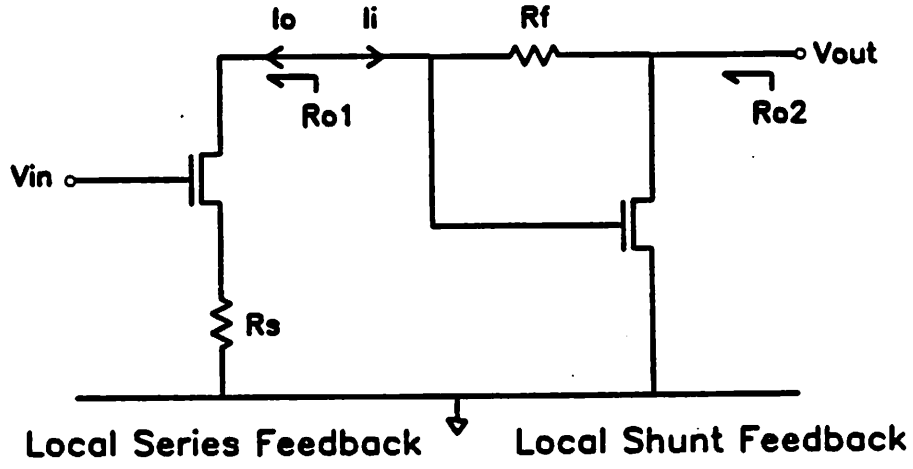


Fig. 2.22 Resistive local-series-local-shunt feedback amplifier configuration.

general, it is necessary to know the DC transfer characteristics of the inverter before one can work out the relationship between f_T and τ_d by using equation 2.27 and 2.19.

2.3 Single-Stage Active Shunt Feedback

The open loop amplifiers discussed in section 2.1 are suitable for some non-critical on-chip applications. Unfortunately, their disadvantages (especially 1 and 2 in section 2.1) render them useless in many situations. This section investigates the use of negative feedback around one gain stage to improve amplifier characteristics.

Negative feedback is widely used in amplifier design since it improves amplifier stability against temperature and processing variations, and extends amplifier bandwidth [7]. If the feedback elements are linear, such as resistors and capacitors, distortion in the amplifier is also reduced. In this section we introduce an amplifier that employs non-linear or active feedback to improve amplifier bandwidth and stability [10]. Linearity is not our primary concern here because the assumed input signal is a binary digital waveform with small amplitude. The amplifier can drive only on-chip capacitance and is intended to be a part of a larger LSI system. Specifically, this amplifier is used as the preamplifier of the high speed voltage comparator discussed in section 3.4.

2.3.1 Single-Stage Feedback Configurations

Single-stage feedback, sometimes known as local feedback, is an important concept in feedback amplifier design. One virtue of local feedback is that the amplifier is free from oscillation problems because the feedback is applied locally and the phase shift around the loop is much less than 180 degrees at frequencies where loop gain is larger than one. In some multi-stage feedback amplifier designs [8], local feedback is embedded within multiple feedback loops to improve phase margins and frequency response characteristics.

Only two feedback configurations are possible around a single transistor. They are the local series feedback and the local shunt feedback shown in figure 2.22. A local series feedback stage functions as a transconductance amplifier because both its input and output impedance are increase by the loop gain. From standard theory [7], overall transconductance G_m is

$$\left.\frac{i_o}{v_s}\right|_{s=0} = \frac{g_{m1}}{1 + T_{series}} \tag{2.29}$$

where the series feedback loop gain is

$$T_{series} \approx g_{m1}R_s$$

On the other hand, a local shunt feedback stage is a transresistance amplifier since the loop gain serves to reduce both its input and output impedance.

$$\left.\frac{v_o}{i_i}\right|_{s=0} \approx \frac{-R_f}{1 + \frac{1}{T_{shunt}}} \tag{2.30}$$

where the shunt feedback loop gain is

$$T_{shunt} \approx g_{m2}\left(R_f||R_{o2}\right)\frac{1}{R_f}\left(R_{o1}||R_f\right)$$

$$\approx g_{m2}R_{o2}\left(\frac{1}{1 + \frac{g_{m2}R_{o2}}{g_{m2}R_f}}\right)\left(\frac{1}{1 + \frac{g_{m1}R_f}{g_{m1}R_{o1}}}\right)$$

One means of obtaining voltage gain is to use the local series feedback stage to drive the local shunt feedback stage. This configuration minimizes interactions between the two stages because the output impedance of the transconductance stage is high while the input impedance of the transresistance stage is low. For such a cascade,

$$\frac{v_o}{v_{in}} = \frac{g_{m1}}{1+T_{series}} \frac{R_f}{1 + \frac{1}{T_{shunt}}} \tag{2.31}$$

If T_{series} and T_{shunt} are much larger than one, the overall voltage gain of the amplifier approaches $\frac{R_f}{R_s}$, and the amplifier response has all of the improved characteristics mentioned earlier from using linear negative feedback.

Unfortunately, this configuration suffers from three major problems in the SiGMOS technology.

1. The series feedback loop gain T_{series} may not be large, because in equation 2.29, g_m is small (80 mS/mm). If we make R_s large instead, voltage drop across R_s becomes too large. To demonstrate this, note that

   $$T_{series} \approx g_m R_s \gg 1$$

   Together with equation 2.2, this implies

   $$\frac{I_{dsat_1} R_s}{\left(V_{GS}-V_T-0.45\right)} \gg 1$$

   and therefore

   $$V_S = I_{Dsat_1} R_s \gg \left(V_{GS}-V_T-0.45\right)$$

   Since $V_{GS}-V_T$ is 1.5V, V_S should be much larger than 1V in order for the series feedback to be effective. In general, source degeneration in MOS is not as effective as emitter degeneration in bipolar.

2. The shunt feedback loop gain T_{shunt} is also relatively small, because the term $g_m R_O$ in equation 2.30 is approximately equal to $g_m\left[r_{oD}\|r_{oE}\|\frac{1}{g_{mbD}}\right]$, which is about 4.5. If we use typical values in equation 2.30, the calculated value for T_{shunt} is about 1.
3. The fabrication of the resistors may contribute unnecessary complications to the existing SiGMOS process, because thin film resistors of the right sheet resistivity are not available.

Because of low loop gain factors, the amplifier gain does not approach $\frac{R_f}{R_s}$, and a better solution using active shunt feedback is proposed instead. In figure 2.23, transistor M_1 is the transconductance stage, transistor M_2 together with feedback transistor M_f form the second transresistance stage. The dc voltage gain is given by

$$\frac{v_o}{v_i} = \frac{g_{m1}}{g_{mf}}\left(\frac{1}{1+\frac{1}{T_{as}}}\right) \qquad (2.32)$$

where T_{as}, the loop gain of the transresistance stage, is

$$T_{as} = g_{m2}R_{o2}g_{mf}\left[R_{o1}\|\frac{1}{g_{mf}}\right]$$

and R_{o1} and R_{o2} are defined in equation 2.34. By expanding terms in equation 2.32, we have

$$T_{as} = g_{m2}R_{o2}\left[1+\frac{1}{g_{m1}R_{o1}\frac{g_{mf}}{g_{m1}}}\right]^{-1} \qquad (2.33)$$

If T_{as} is much larger than 1, dc voltage gain of the active shunt feedback configuration should approach $\frac{g_{m1}}{g_{mf}}$. Since the transconductances of two MOS devices fabricated in close proximity are expected to track each other, the gain of the amplifier is stablized against variations in temperature and processing conditions. By using active feedback, difficulties 1 and 3 mentioned above are solved, whereas problem 2 still exists but the situation is slightly better. Comparing equation 2.32 to 2.30, we see that T_{as} is larger than T_{shunt}. This

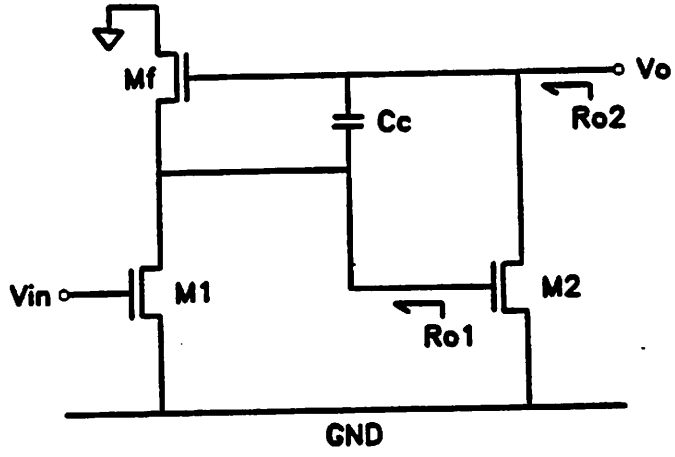


Fig. 2.23 Active shunt feedback amplifier configuration.

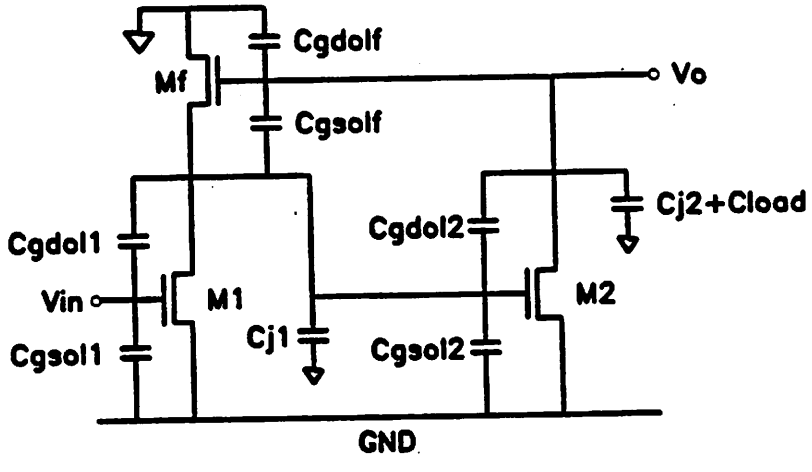


Fig. 2.24 Important parasitic capacitances of ASF-amp.

is because the drain of M_2 is only loaded by R_{o1} and not by R_f as in the former case. Substituting $g_{m2}R_{o2}=4.56$, $g_{m1}R_{o1}=4$ and $\frac{g_{mf}}{g_{m1}}=\frac{1}{7}$ in equation 2.33 gives $T_{as}=1.65$. If we used the same values in equation 2.30 and assume $g_{m2}R_f=g_{m1}R_f=8$, $T_{shunt}=1.18$.

Since T_{as} is low, the temperature coefficient of the active shunt feedback amplifier is only slightly better than that of the open loop amplifier. If better gain stability is needed, the circuit should be improved to provide more loop gain. This approach is investigated in section 2.4 where active shunt feedback around three stages is applied.

In summary, the active shunt feedback amplifier has three advantages over an open loop amplifier.

1. The dc gain can be controlled by the ratio $\frac{g_{m1}}{g_{mf}}$, which is set by the width of two devices in the layout.
2. The open loop gain of the amplifier can be traded for bandwidth with the use of feedback.
3. Peaking response can be selectively introduced in a cascade of these feedback amplifiers to reduce gain-bandwidth shrinkage.

2.3.2 Small Signal AC Analysis of Active Shunt Feedback

To analyze the frequency response of the active shunt feedback amplifier, refer to the ac equivalent circuit in figure 2.24 where all important parasitic capacitances are included. Replacing the transistors with their hybrid-π model, figure 2.25 is generated. If we use the Y-parameter representation in figure 2.10 for transistor M_f, figure 2.25 reduces to figure 2.26, where

$$C_{in} = C_{gs1}+C_{gsol1} \tag{2.34}$$

$$C_1 = C_{j1}+C_{gs2}+C_{gsol2}$$

$$C_f = C_{gsf}+C_{gsolf}+C_{gd2}+C_{gdol2}+C_c$$

$$C_2 = C_{load}+C_{j2}+C_{gdolf}$$

$$R_{o1} = r_{o1}||r_{of}||\frac{1}{g_{mbf}}$$

and

$$R_{o2} = r_{o2}$$

The AC transfer function is given by

$$\frac{v_o}{v_i}(s) = \frac{\left[1-\frac{s}{z}\right]}{as^2 + bs + c} \tag{2.35}$$

$$= \frac{G\left[1-\frac{s}{z}\right]}{\left[1-\frac{s}{p1}\right]\left[1-\frac{s}{p2}\right]}$$

where

$$a = \frac{C_1C_2}{G_{m1}g_{m2}}\left[1 + \frac{C_f}{C_1} + \frac{C_f}{C_2}\right]$$

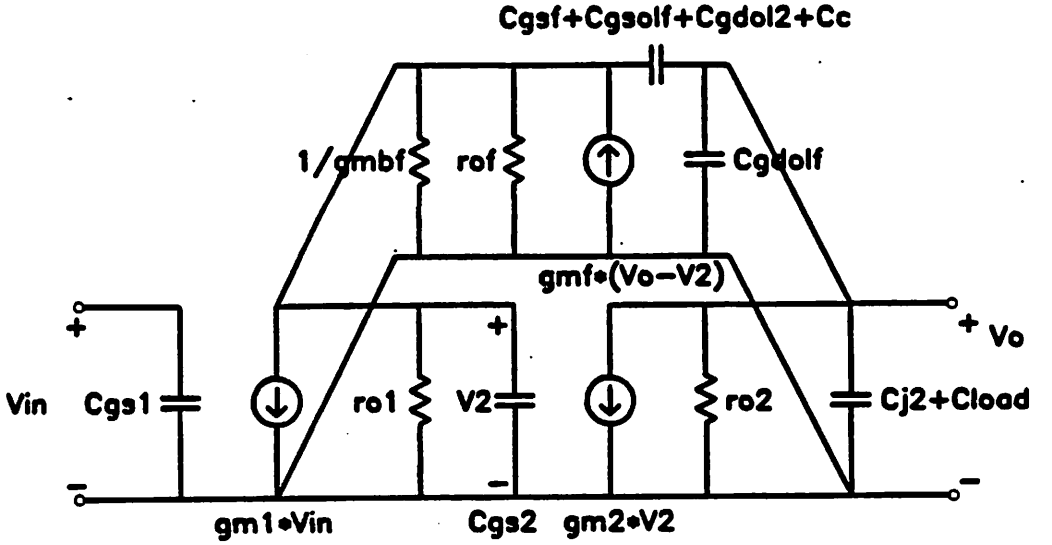


Fig. 2.25 Equivalent circuit of ASF-amp.

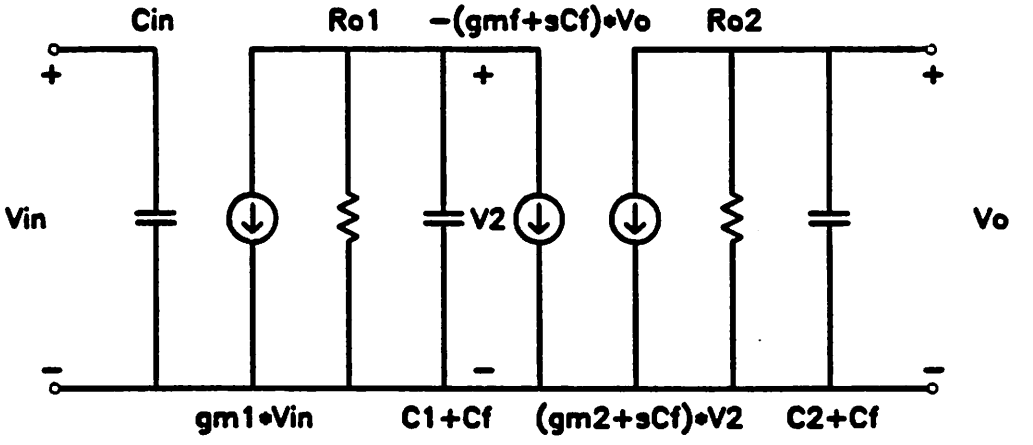


Fig. 2.26 Simplified equivalent circuit of ASF-amp.

$$b = \frac{1}{g_{m1}g_{m2}}\left(\frac{C_1+C_f}{R_{o2}} + \frac{C_2+C_f}{R_{o1}} + C_2g_{mf} + C_fg_{m2}\right)$$

$$c = \frac{g_{mf}}{g_{m1}}\left[1+\frac{1}{g_{m2}R_{o2}}\left(1+\frac{1}{g_{mf}R_{o1}}\right)\right]$$

and

$$z = \frac{g_{m2}}{C_f}$$

At low frequencies (s=0), the dc gain is

$$G = \frac{1}{c} \tag{2.36}$$

$$= \frac{g_{m1}}{g_{mf}}\left[1+\frac{1}{g_{m2}R_{o2}}\left(1+\frac{1}{g_{mf}R_{o1}}\right)\right]^{-1}$$

which is identical to equation 2.32. The amplifier asymptotic bandwidth is defined as

$$BW = \sqrt{\frac{c}{a}} \tag{2.37}$$

$$= \left\{\frac{g_{mf}g_{m2}\left[1+\frac{1}{g_{m2}R_{o2}}\left(1+\frac{1}{g_{m1}R_{o1}}\right)\right]}{C_1C_2\left(1+\frac{C_f}{C_1}+\frac{C_f}{C_2}\right)}\right\}^{\frac{1}{2}}$$

Combining equations 2.36 and 2.37, the normalized gain-bandwidth product is

$$\sqrt{G}\times BW = \sqrt{\frac{1}{a}} \tag{2.38}$$

$$= \left\{\frac{g_{m1}g_{m2}}{C_1C_2}\left(\frac{1}{1+\frac{C_f}{C_1}+\frac{C_f}{C_2}}\right)\right\}^{\frac{1}{2}}$$

If $\frac{C_f}{C_1}$ and $\frac{C_f}{C_2}$ are much smaller than 1,

$$\sqrt{G}\times BW \approx \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

which implies that the amplifier normalized gain-bandwidth product approaches that of the single-stage inverter (GBW_1), and the speed performance of the amplifier has reached the theoretical maximum for a two stage amplifier design.

In equation 2.35, the two quadratic roots in the denominator are given by

$$p_{1,2} = \frac{-b \pm \sqrt{b^2-4ac}}{2a} \tag{2.39}$$

The amplifier is stable as long as the poles stay in the left-half s-plane of the root locus plot. In equation 2.35, coefficients a and b are always positive; therefore the real part of $p_{1,2}$, which is $\frac{-b}{2a}$, is negative. This implies the amplifier is unconditionally stable.

The root locus is plotted qualitatively in figure 2.27. As T_{as} increases the two poles become complex and move towards the $j\omega$ axis, and as C_f increases, the poles move towards the negative real axis following a semi-circular locus [11]. By controlling the designed value of C_f, the positions of the two complex poles can be adjusted such that the amplifier can have different types of response functions. Some well known response functions are the Bessel response, the Butterworth response and the Elliptic response.

Complete Circuit Implementation and Simulation Results

To illustrate the effects of active shunt feedback, computer simulations are used to evaluate the circuits shown in figure 2.28a and b. Each circuit is assumed to drive a capacitive load equal to its own input capacitance.

Figure 2.28a shows the complete schematics of the active shunt feedback amplifier (referred to as ASF-amp), where transistor M_1, M_2 and M_f correspond to those in figure 2.23. M_3–M_4 are depletion current sources to provide internal dc biasing. From simulation results, no C_c is needed to suppress peaking in the frequency response, therefore C_c equals 0 in equation 2.34. The simulated closed-loop frequency response of the ASF-amp is compared to its open-loop response in figure 2.29 (open-loop response is generated by connecting the gate of M_f to a dc source instead of to the output) which clearly demonstrates the effect of exchanging gain for bandwidth in the ASF-amp. The -3dB bandwidth

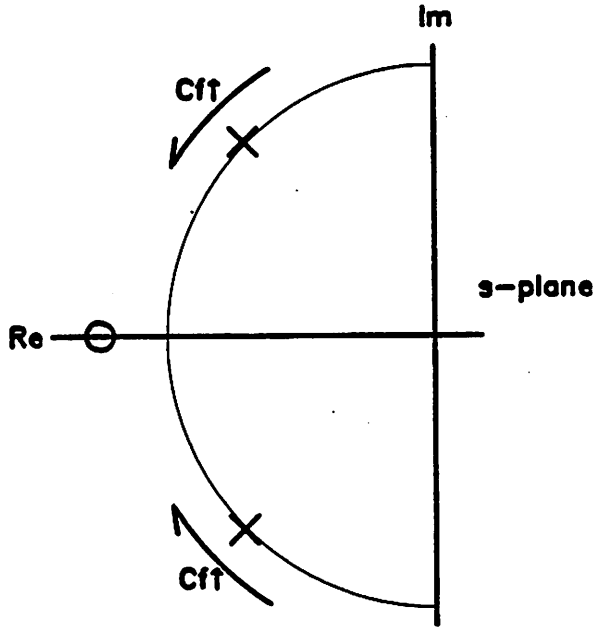


Fig. 2.27 Root locus of active shunt feedback amplifier.

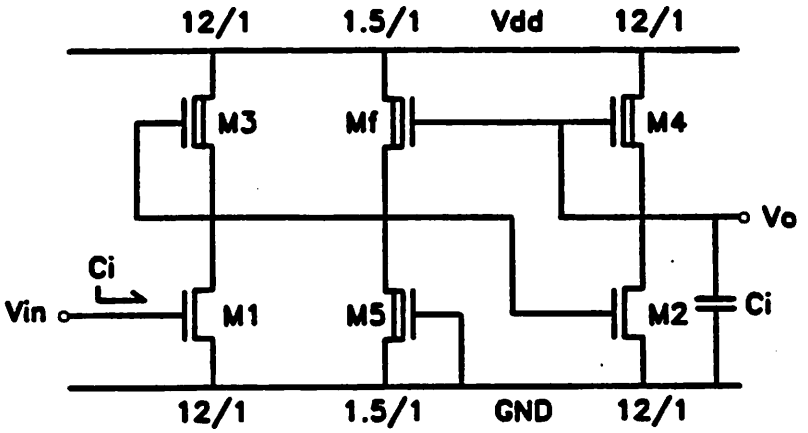


Fig. 2.28a Active shunt feedback amplifier (ASF-amp).

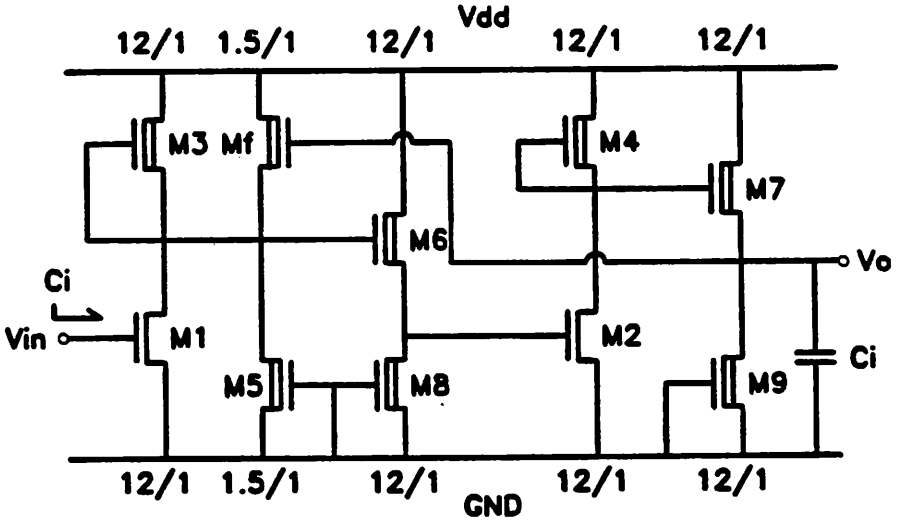


Fig. 2.28b Buffered active shunt feedback amplifier (BASF-amp).

of the ASF-amp is extended to 1.75GHz while the open-loop bandwidth is only 600MHz. The simulated loop gain is 1.69 which is close to the value given by equation 2.33. The simulated dc gain is 4.4. Since there are two gain stages in the ASF-amp, the normalized gain-bandwidth product ($G_2^{\frac{1}{2}}BW_2$) is 3.6GHz which approaches the value of GBW_1 of a single-stage inverter (section 2.2.2). This result is predicted by equation 2.38 of the previous section. The amplifier has a -40dB per decade roll-off at high frequencies and a unity-gain frequency at 3.9GHz.

From equation 2.37, the ASF-amp bandwidth is inversely proportional to C_1 and C_2. One way to reduce C_1 and C_2 is by using source followers to buffer loading capacitance from the two high impedance nodes. This is illustrated in the circuit shown in figure 2.28b where transistors M_6–M_9 are added to the original ASF-amp in figure 2.28a. The circuit in 2.28b will be referred to as the Buffered Active Shunt Feedback amplifier or BASF-amp. The penalty for adding source followers in the feedback loop is that the dc loop gain is lowered. Similar to equation 2.32, the dc gain of the BASF-amp is given by

$$\frac{v_o}{v_i} = \frac{g_{m1}}{g_{mf}}\left(\frac{1}{1+\frac{1}{T_{bas}}}\right) \tag{2.40}$$

where

$$T_{bas} = \frac{g_{m6}R_{o6}}{1+g_{m6}R_{o6}} g_{m2}R_{o2} \frac{g_{m7}R_{o7}}{1+g_{m7}R_{o7}} g_{mf}\left(R_{o1}\|\frac{1}{g_{mf}}\right)$$

The simulated result in figure 2.30 shows a slight improvement in bandwidth for the BASF-amp over the ASF-amp. The -3dB bandwidth is increased to 2.6GHz while the loop gain is decreased to 1.13. The source follower buffers reduce the dc open-loop gain of the BASF-amp to 8.15 but extends its open-loop bandwidth to 1.2GHz. The BASF-amp has a high frequency roll-off greater than -40dB per decade and a unity-gain frequency at 3.8GHz. The simulated dc gain is 3.8. If we calculate the normalized gain-bandwidth product with N=2, $G_2^{\frac{1}{2}}BW_2=5GHz$ which is larger than the GBW of the single-stage inverter. The reason for this discrepancy is that the BASF-amp is really a four-stage

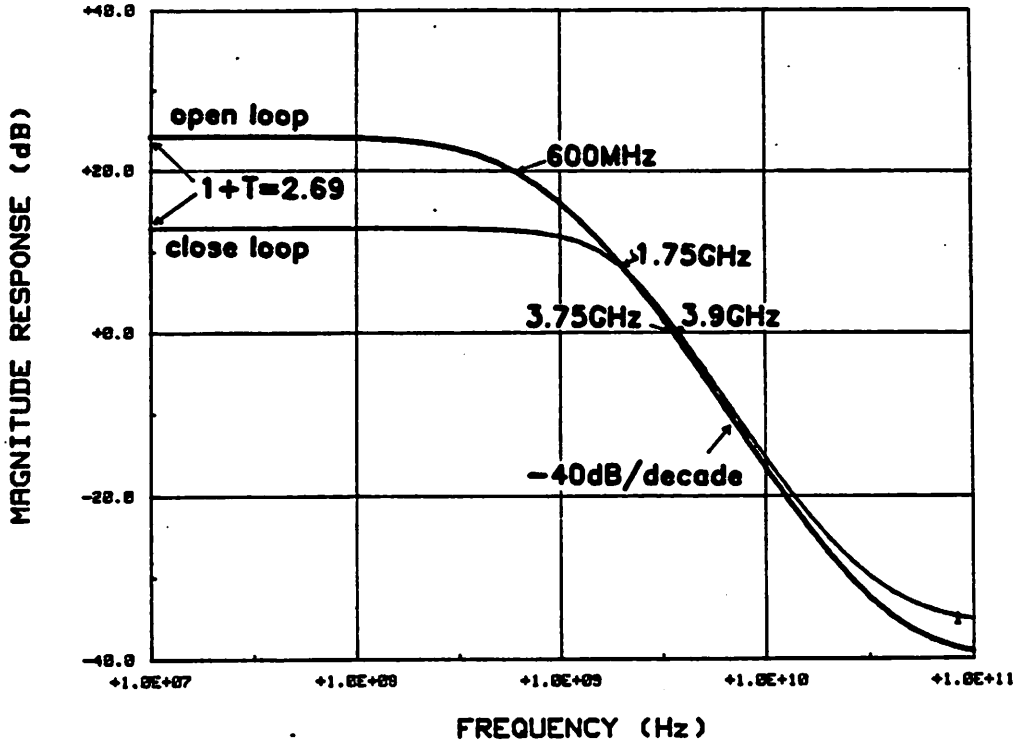


Fig. 2.29 Simulated frequency response of ASF-amp.

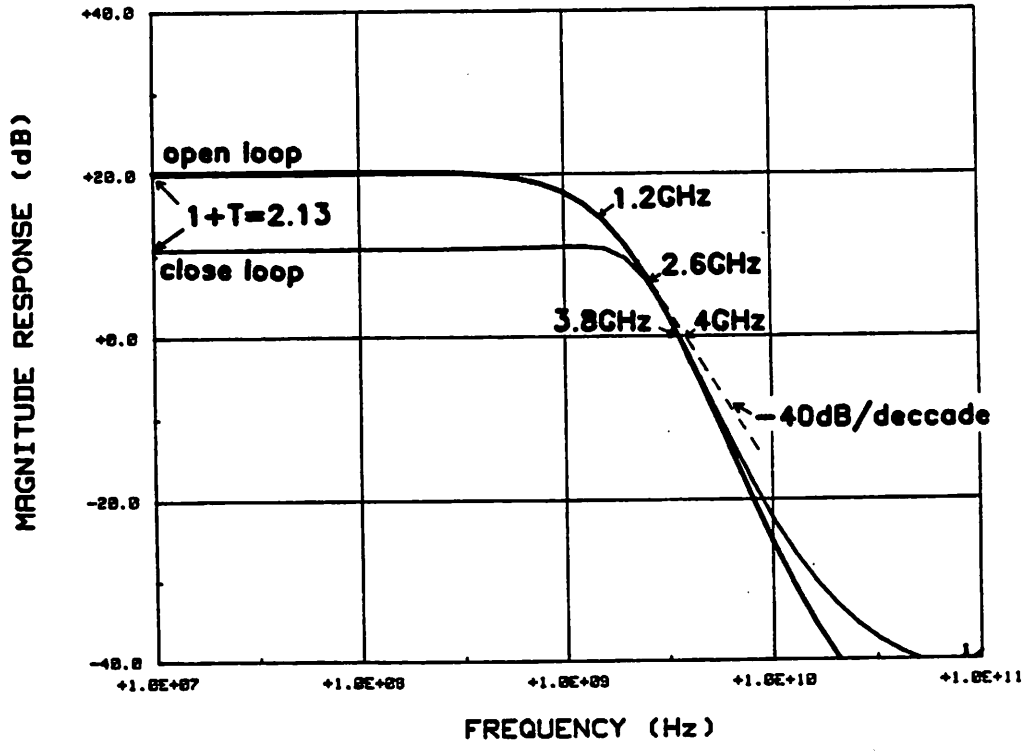


Fig. 2.30 Simulated frequency response of BASF-amp.

amplifier (since we have added two source followers), and N should equal to 4 in normalized gain-bandwidth product calculations which gives $G_4^{\frac{1}{4}}BW_4=3.6GHz$.

The simulated dc transfer curves for the ASF-amp and the BASF-amp are plotted in figure 2.31a and b respectively. The desired amplifier operating point is at $V_{in}=V_{out}=2.5V$. From simulated results, the two feedback amplifiers have the same input capacitance at $2fF/\mu m$.

From these simulation results, it is clear that the SiGMOS technology can provide wide-band amplifiers with low to moderate gain at frequencies up to 2GHz if active negative feedback is applied. Since the normalized GBW of the two amplifiers has approached that of a single-stage inverter, the speed performance of these amplifiers has reached the theoretical maximum.

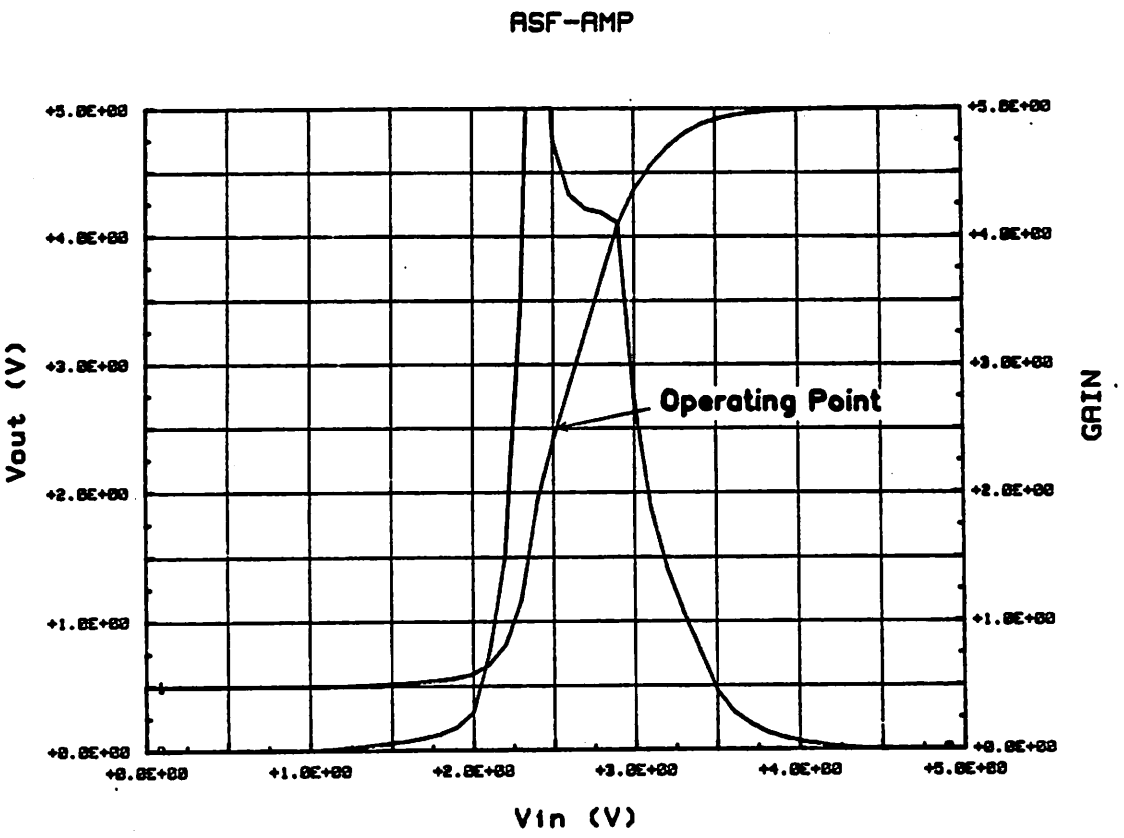


Fig. 2.31a Simulated DC transfer curve and gain of ASF-amp.

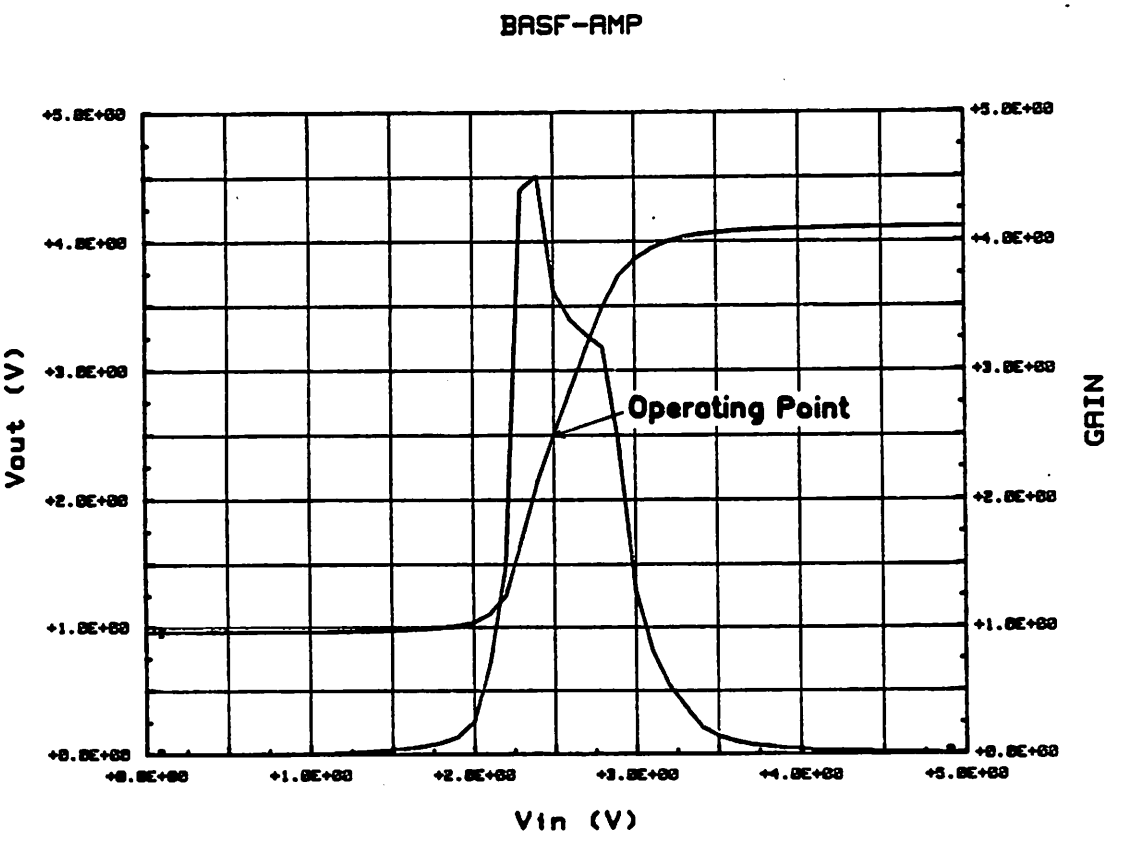


Fig. 2.31b Simulated DC transfer curve and gain of BASF-amp.

2.3.3 Noise Analysis of the Active Shunt Amplifier

This section will provide first order equations for the calculation of equivalent input noise power density of the BASF-amp. In the MOS-III model of SPICE, the equivalent transistor input thermal noise voltage is given by

$$\overline{v_t^2} = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f$$

where 4kT equals 1.66e-20 V-C. Referring to figure 2.28c, the total referred input noise voltage is given by

$$\overline{v_{ieqT}^2} = \sum_{x=1}^{x=9}\overline{v_{ieqx}^2} + \overline{v_{ieqf}^2} \tag{2.41}$$

where $\overline{v_{ieqx}^2}$ is the equivalent amplifier input noise voltage due to the transistor M_x. By inspection, the noise contribution of each transistor to the total input noise is given by the following set of equations.

$$\overline{v_{ieq1}^2} = \overline{v_1^2} \tag{2.42}$$

$$\overline{v_{ieq2}^2} = \overline{v_2^2}\left(G_{sf6}G_{cs1}\right)^{-2}$$

$$\overline{v_{ieq3}^2} = \overline{v_3^2}\left(\frac{g_{m1}}{g_{m3}}\right)^{-2}$$

$$\overline{v_{ieq4}^2} = \overline{v_4^2}\left(\frac{g_{m2}}{g_{m4}}G_{sf6}G_{cs1}\right)^{-2}$$

$$\overline{v_{ieq5}^2} = \overline{v_5^2}\left(\frac{g_{m1}}{g_{m5}}\right)^{-2}$$

$$\overline{v_{ieq6}^2} = \overline{v_6^2}\left(G_{cs1}\right)^{-2}$$

$$\overline{v_{ieq7}^2} = \overline{v_7^2}\left(G_{cs2}G_{sf6}G_{cs1}\right)^{-2}$$

$$\overline{v_{ieq8}^2} = \overline{v_8^2}\left(\frac{g_{m6}}{g_{m8}}G_{cs1}\right)^{-2}$$

$$\overline{v_{ieq9}^2} = \overline{v_g^2}\left(\frac{g_{m7}}{g_{m9}}G_{sf7}G_{cs2}G_{sf6}G_{cs1}\right)^{-2}$$

and

$$\overline{v_{ieqf}^2} = \overline{v_f^2}\left(\frac{1}{g_{mf}}G_{cs1}\right)^{-2}$$

where G_{cs1} is the gain of the input common source stage with the negative feedback loop disconnected at the gate of M_f, G_{sf6} is the gain of the source follower M_6, G_{cs2} is the gain of the second inverter stage, and G_{sf7} is the gain of the output source follower stage. G_{sf6} and G_{sf7} are given by equation 2.12. G_{cs2} is given by equation 2.1, and G_{cs1} is given by

$$G_{cs1} = g_{m1}\left(r_{o1}||r_{o3}||r_{of}||r_{o5}||\frac{1}{g_{mb3}}||\frac{1}{g_{mbf}}||\frac{1}{g_{mf}}\right)$$

The above equations for circuit noise analysis were verified using computer simulations. The circuit in figure 2.32 was used in the simulation where 50Ω source and termination resistors were assumed. Figure 2.33 is the simulated circuit noise figure versus frequency. A noise figure of 23dB is achieved at frequencies between 0.1GHz to 1GHz. Table 2.4 is the Spice Noise Analysis output summary at 0.1GHz, which clearly shows that the amplifier noise is dominated by noise generated in M_1 and M_3. If it is necessary to improve the amplifier noise performance, the width of transistor M_1 and M_3 must be increased such that the $\frac{1}{g_m}$ of those transistors is less than 50Ω. The ASF-amp has a lower noise figure than the BASF-amp, because the added source followers in the BASF-amp contribute noise to the signal. If the width of the transistors in the ASF-amp in figure 2.28a is increased by a factor of 100 the simulated amplifier noise figure is 6dB. This is because the 50Ω termination resistor already contributes 3dB to the noise figure. If a noise figure of better than 3dB is desired, resistive shunt feedback at the input must be used instead of the external 50Ω resistor to provide 50Ω termination.

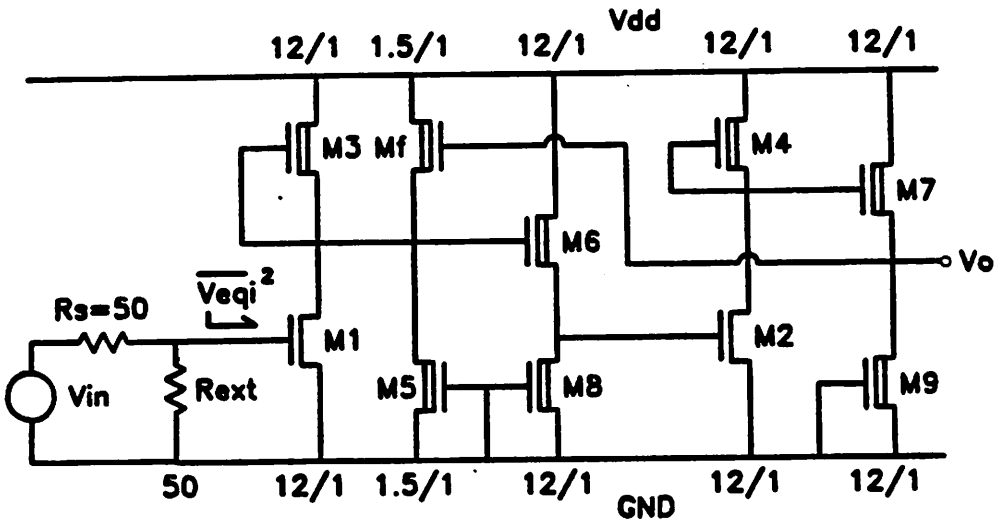


Fig. 2.32 Circuit used in noise analysis of BASF-amp.

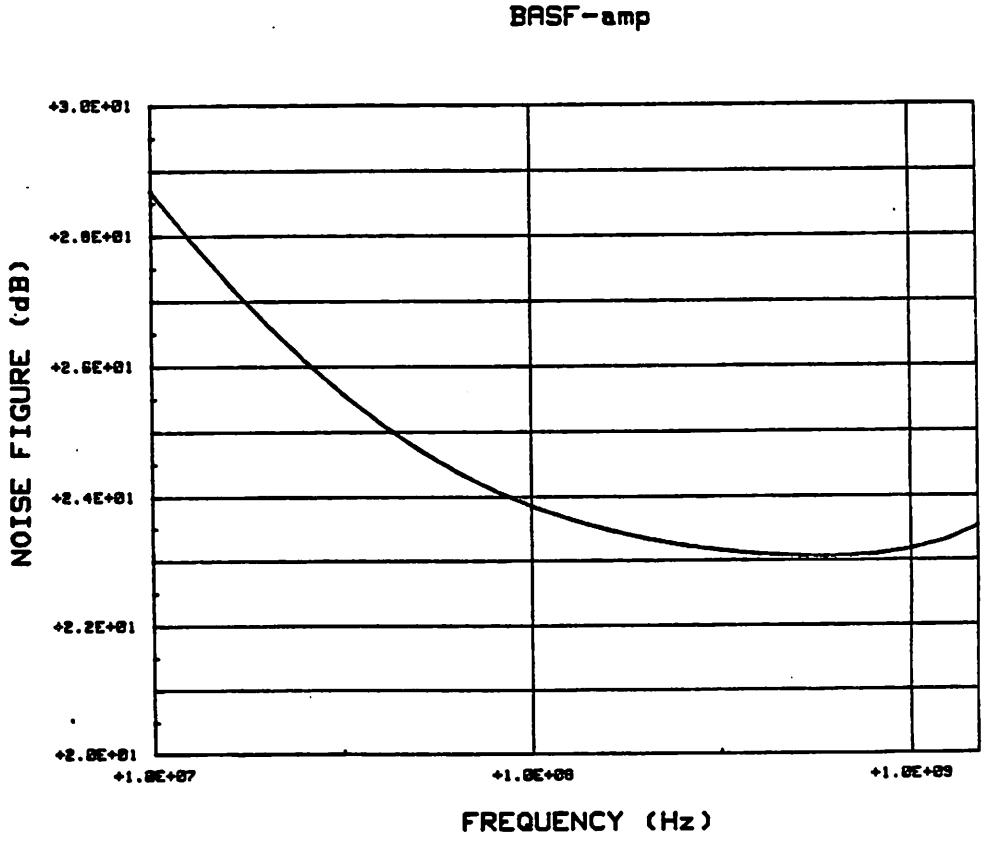


Fig. 2.33 Simulated noise figure of BASF-amp.

```
0     FREQUENCY =  1.000d+08 HZ

0**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/HZ)


                RS          REXT
0TOTAL      2.438d-18   2.438d-18

0**** MOSFET SQUARED NOISE VOLTAGES (SQ V/HZ)

                M1          M3          M6          M8          M4          M2          M7
0RD         5.781d-20   1.298d-20   9.744d-21   9.530d-21   1.593d-20   3.858d-21   9.071d-22
0RS         4.296d-18   3.516d-18   6.425d-19   6.592d-19   1.191d-18   9.758d-19   6.001d-20
0ID         1.432d-16   1.372d-16   2.067d-17   2.084d-17   3.948d-17   3.774d-17   1.937d-18
0FN         4.300d-17   4.216d-17   6.580d-18   6.577d-18   1.185d-17   1.191d-17   6.120d-19
0TOTAL      1.906d-16   1.829d-16   2.791d-17   2.808d-17   5.254d-17   5.063d-17   2.610d-18

                M9          Mf          M5
0RD         8.873d-22   7.563d-22   1.140d-21
0RS         6.105d-20   6.636d-20   7.823d-20
0ID         1.937d-18   1.829d-17   1.942d-17
0FN         6.119d-19   5.085d-18   6.188d-18
0TOTAL      2.611d-18   2.344d-17   2.569d-17


0**** TOTAL OUTPUT NOISE VOLTAGE          =  5.918d-16 SQ V/HZ
0                                         =  2.433d-08 V/RT HZ
0     TRANSFER FUNCTION VALUE:
0       V(7)/VINAC                        =  1.715d+00
0     EQUIVALENT INPUT NOISE AT VINAC     =  1.418d-08 /RT HZ
1*******03/05/85 ********  SPICE 2G.5 (10AUG81)  ********15:19:34*****
```

Table 2.3 Spice Noise Analysis Output Summary at 0.1GHz.

2.4 Three-Stage Active Shunt Feedback Amplifier

In section 2.3.1, it was shown that the gain stability of the ASF-amp is only slightly better than that of the open-loop amplifiers because the loop gain is low (T_{as}=1.62). Loop gain can be increased by either improving the $g_m r_o$ of the transistors or by using more than one gain stage in the feedback loop. Since $g_m r_o$ cannot be increased without modifying the process, we will examine multi-stage feedback in this section.

In bipolar technology, resistive feedback around three stages is not common among wide-band amplifier designs because the high transistor $g_m r_o$ may result in such large loop gain that the amplifier becomes unstable or difficult to compensate. In section 2.4.1, a three-stage feedback configuration is proposed which employs a MOS transistor as the feedback element. Active feedback is chosen because well defined resistors of the appropriate values are not readily available in a NMOS digital process. Computer simulation results in section 2.4.2 suggest that dominant pole compensation is needed to suppress peaking in the amplifier frequency response. This usually translates to lower amplifier bandwidth. In some applications, the increase in gain stability may outweight the loss in amplifier bandwidth.

2.4.1 Three-Stage Active Shunt Feedback

The circuit configuration of a three-stage active shunt feedback amplifier (ASF3-amp) is shown in figure 2.34. Transistor M_1 is the input transconductance stage, while transistor M_2–M_4 together with feedback transistor M_f form the second tranresistance stage. The dc gain of the amplifier is given by

$$\frac{v_o}{v_i} = \frac{g_{m1}}{g_{mf}}\left(1 + \frac{1}{T_{as3}}\right)^{-1} \tag{2.43}$$

where

$$T_{as3} = g_{m2}R_{o2}g_{m3}R_{o3}\frac{g_{m4}R_{o4}}{1+g_{m4}R_{o4}}g_{mf}\left(R_{o1}\|R_{of}\right)$$

$$= g_{m2}R_{o2}g_{m3}R_{o3}\frac{g_{m4}R_{o4}}{1+g_{m4}R_{o4}}\left(\frac{1}{\frac{g_{mf}}{g_{m1}}g_{m1}R_{o1}} + \frac{1}{g_{mf}R_{mf}}\right)^{-1}$$

and

$$R_o = r_{oE}\|r_{oD}\|\frac{1}{g_{mbD}}$$

Using the values from table A-1 in the appendix, $g_{m1}R_{o1}=g_{m2}R_{o2}=g_{m3}R_{o3}=g_{m4}R_{o4}\approx 4.5$ and assuming $\frac{g_{m1}}{g_{mf}}=8$, the calculated loop gain according to equation 2.43 is 8.3. This value agrees with simulated results in figure 2.3 . The improved loop gain can stablize dc gain of the ASF3-amp. Section 2.5 compares the gain sensitivity of the three types of amplifiers mentioned thus far.

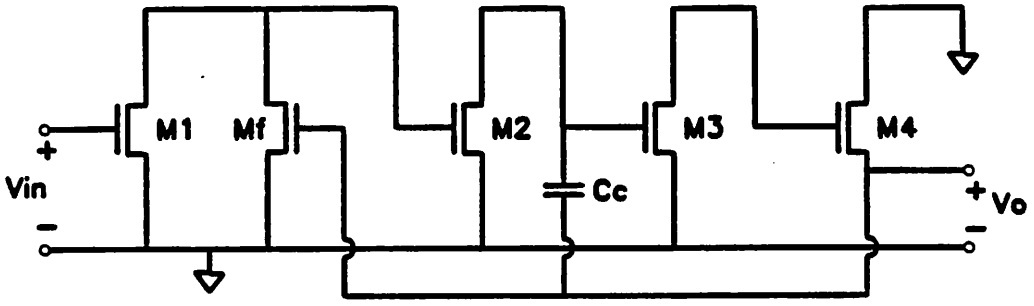


Fig. 2.34 Three-stage active shunt feedback configuration.

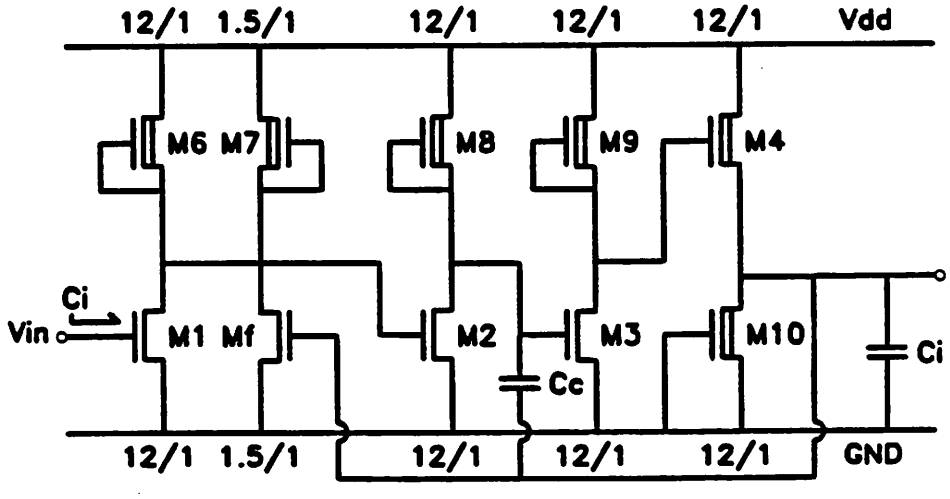


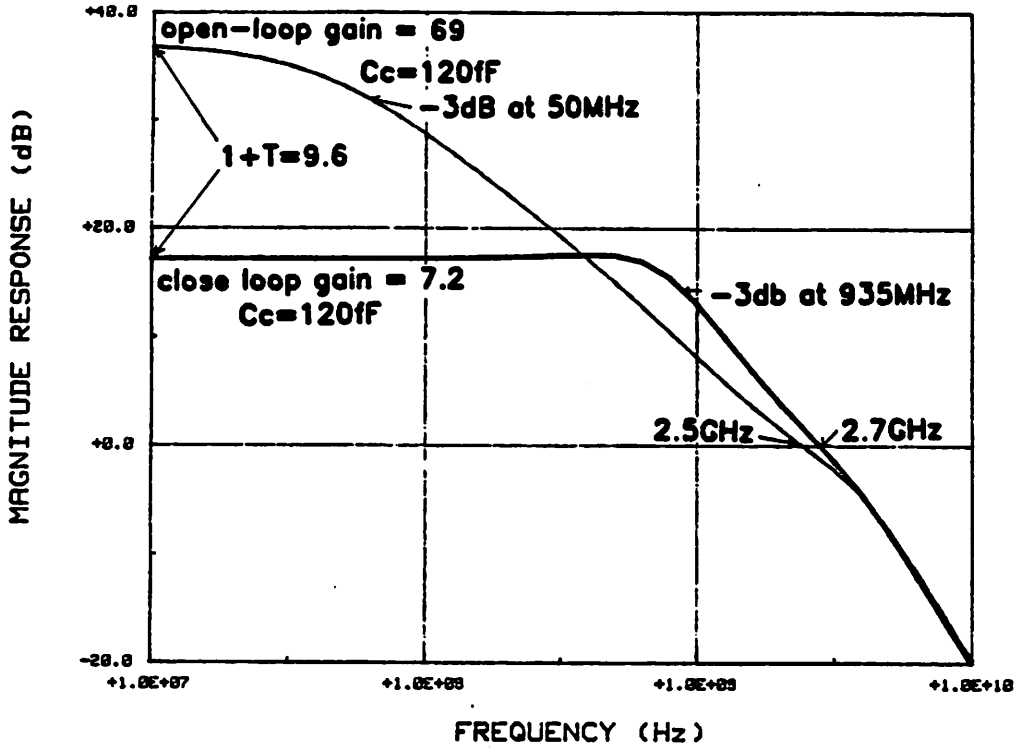
Fig. 2.35 Three-stage active shunt feedback amplifier (ASF3-amp).

2.4.2. Computer Simulations and Frequency Compensation

The complete circuit schematic of the ASF3-amp is shown in figure 2.35. Transistor M_1–M_4 and M_f correspond to those in figure 2.34, and all other transistors are depletion current sources for dc biasing. A compensation capacitor C_c is needed to suppress peaking in the frequency response. Since there are three gain stages, the system transfer function should have three poles. Assuming the amplifier is driving its own input capacitance, we use computer simulation to obtain the amplifier frequency response.

Figure 2.36 again shows the familiar gain-bandwidth-trade-off property of negative feedback amplifiers. The -3dB bandwidth of the ASF3-amp is extended to 925MHz, while the open-loop response of the same amplifier has only 50MHz of bandwidth. Open-loop response is obtained by connecting the gate of M_f to a dc voltage source in figure 2.35. Both the -3dB and the unity-gain frequency of the ASF3-amp are lower than that of the single-stage shunt feedback amplifier of the previous section. This loss of bandwidth is compensated with an increase in loop gain which translates to an amplifier with better gain stability. In some situations, gain stability requirements may outweight the need for maximum frequency response. To demonstrate the increase in gain stability, a sequence of simulations were performed by varying the gain of the inverter (g_mR_o) by ±10%. Simulated dc gain of the ASF3-amp in figure 2.37 changes roughly by ±2.5%. Therefore the gain sensitivity of ASF3-amp to g_mR_o is 0.25.

The compensation scheme used in this amplifier is similar to the pole-splitting compensation used in conventional operational amplifiers. A single dominant pole is created inside the loop at the gate of M_3. The designed value of C_c is 120fF, and the frequency response peaks by 0.4dB before a -30dB roll-off at high frequencies. If the value of C_c is varied by ±25%, peaking of the response would not exceed 1.2dB (refer to figure 2.38). In practice, the control of C_c is better than ±25%.



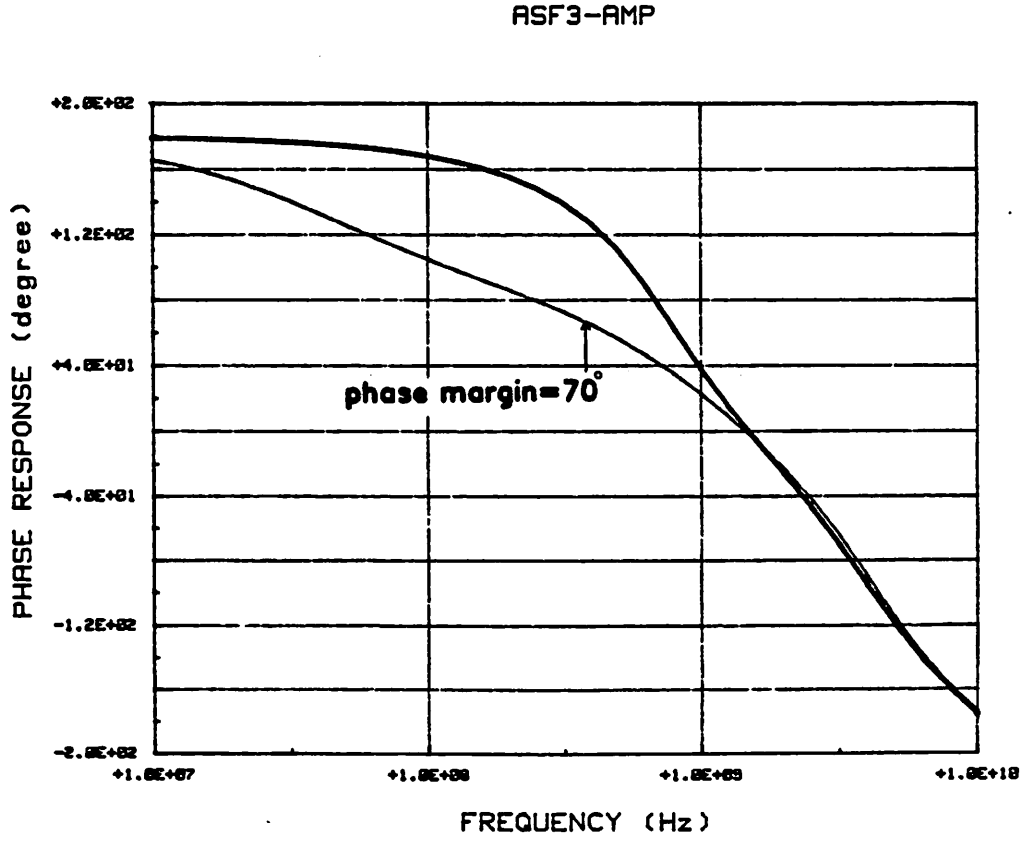
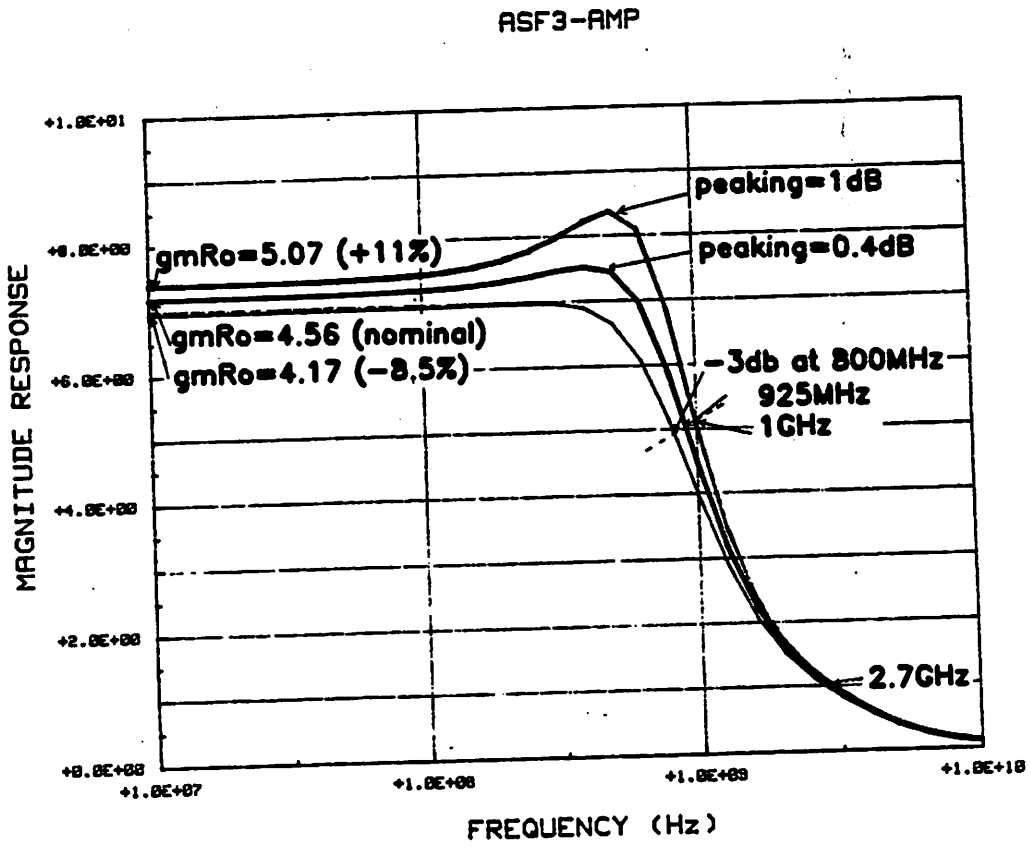


Fig. 2.36 Simulated frequency response of ASF3-amp.



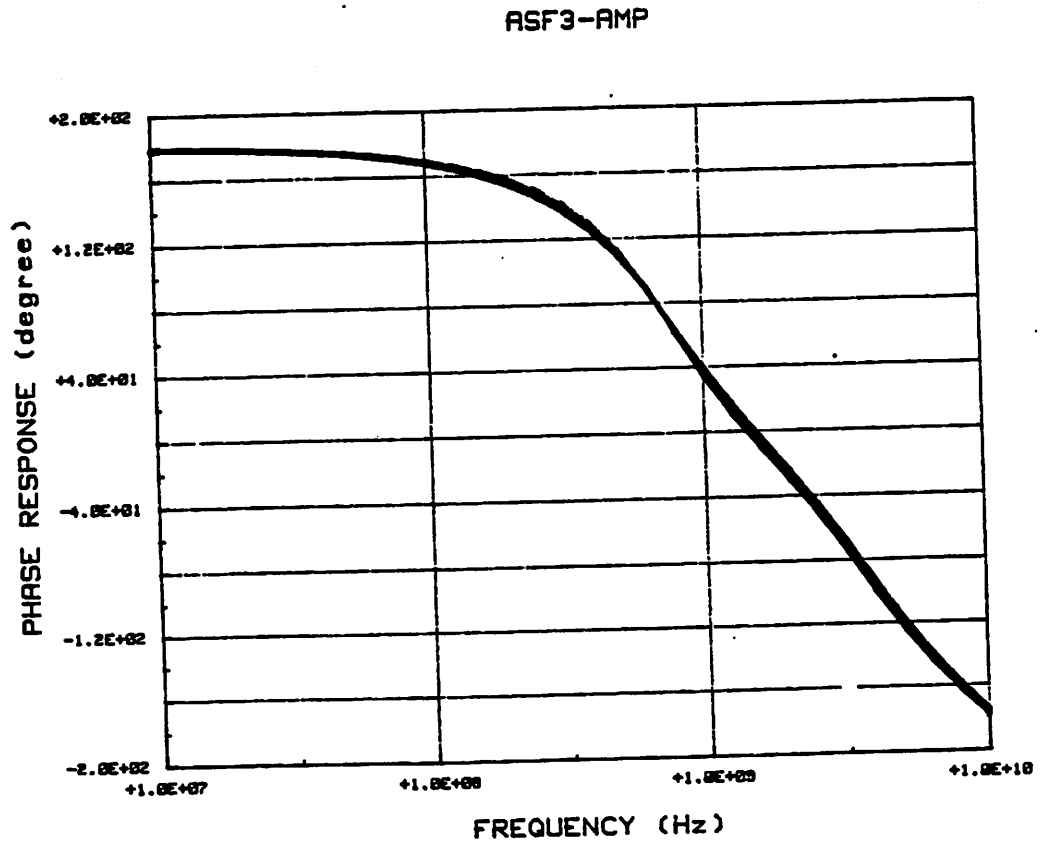
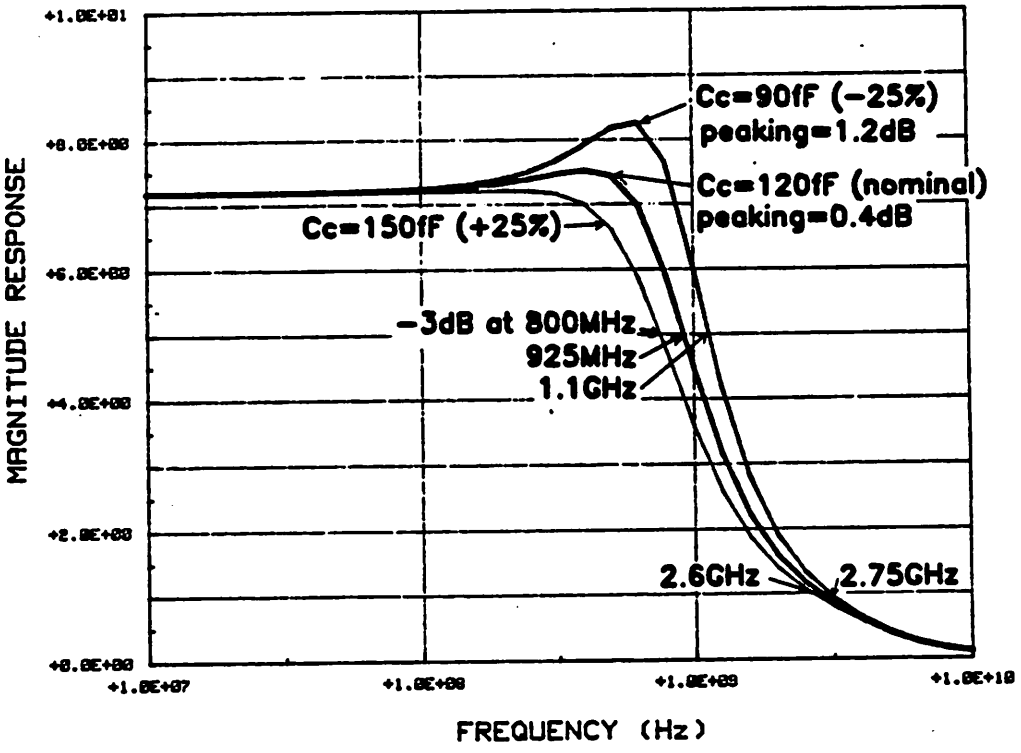


Fig. 2.37 Simulated frequency response of ASF3-amp when $g_m R_o$ is varied by $\pm 10\%$.



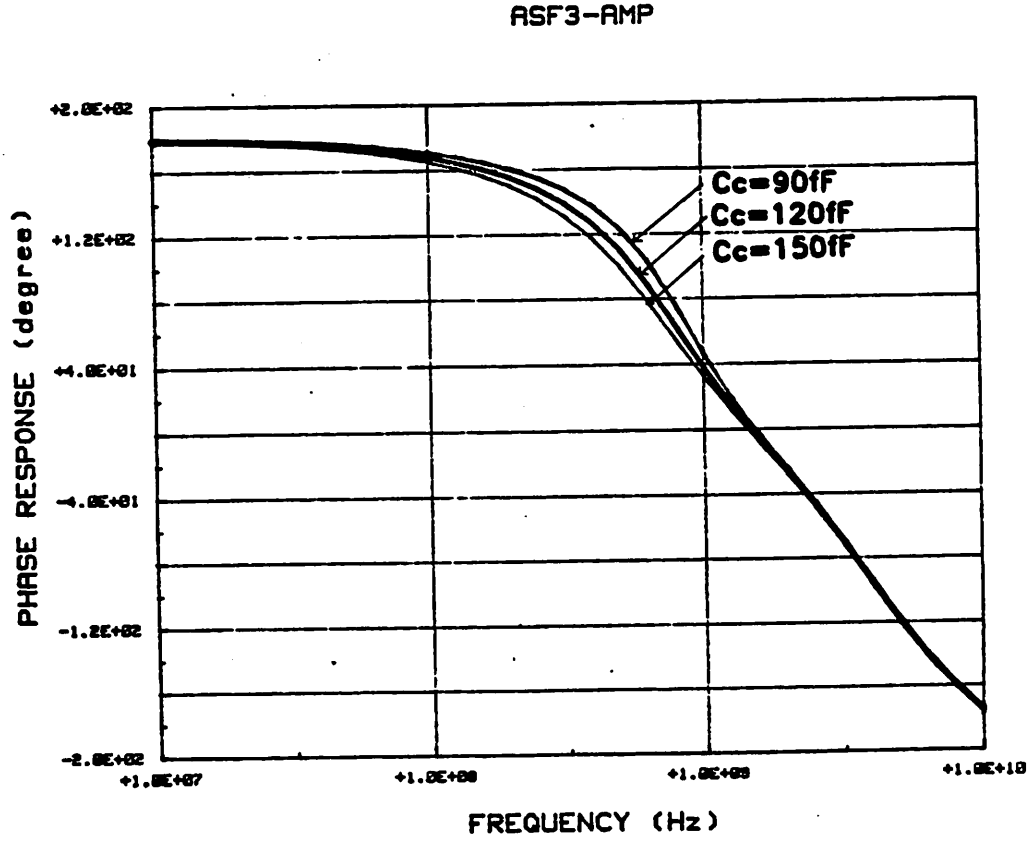


Fig. 2.38 Simulated frequency response of ASF3-amp when C_c is varied by $\pm 25\%$.

2.5 Sensitivity Analysis and Conclusion

In this chapter, we have considered three types of wide-band amplifiers. They are the open-loop amplifiers in section 2.1 (Inverter and CD-CS cascade), the single-stage active shunt feedback amplifiers in section 2.3 (ASF-amp and BASF-amp), and the three-stage active shunt feedback amplifier in section 2.4 (ASF3-amp). Before comparing the performance of these amplifiers, let us first examine their dc gain sensitivities to variations in temperature and processing.

As temperature is increased from 23 to 100 degrees C, the measured device g_m is decreased by 20% and device r_o is increased by 13%. Therefore transistor $g_m r_o$ decreases by about 6% in this temperature range. Besides temperature variations, device $g_m r_o$ changes due to process variations. From lot to lot, $g_m r_o$ varies by as much as ±15%. This variation is mainly due to changes in device channel length. This figure is expected to reduce as photolithographic control is improved in the future.

The dc gain of the inverter is given by equation 2.1 and is repeated here as

$$G_{inv} = g_m R_o \tag{2.44}$$

where

$$R_o = r_{oE} \| r_{oD} \| \frac{1}{g_{mbD}}$$

The sensitivity of G_{inv} to $g_m R_o$ is defined as

$$S_{g_m R_o}^{G_{inv}} = \frac{\frac{\partial G_{inv}}{G_{inv}}}{\frac{\partial g_m R_o}{g_m R_o}} \tag{2.45}$$

$$= 1$$

The dc gain of the ASF-amp is given by equation 2.32. To calculate the gain sensitivity of the ASF-amp with respect to loop-gain variations, we differentiate equation 2.32 with respect to T_{as}. After rearranging terms, we have

$$S_{T_{as}}^{G_{ASF-amp}} = \frac{1}{1+T_{as}} \tag{2.45}$$

If we neglect loading effects in the feedback loop, $T_{as} \approx \left(g_m R_o\right)^2$, therefore the sensitivity of T_{as} to $g_m R_o$ is

$$S_{g_m R_o}^{T_{as}} \approx 2 \tag{2.46}$$

Combining equations 2.45 and 2.46, the amplifier gain sensitivity to variations in $g_m R_o$,

$$S_{g_m R_o}^{G_{ASF-amp}} \approx \frac{2}{\left(1+T_{as}\right)} \tag{2.47}$$

Similarly, we can use equation 2.40 and 2.43 to calculate the gain sensitivities of the BASF-amp and the ASF3-amp respectively. Using equation 2.40 and assuming no loading effects in the feedback loop, $T_{bas} \approx \left(g_m R_o\right)^2$. Overall gain sensitivity to $g_m R_o$ of the BASF-amp is

$$S_{g_m R_o}^{G_{BASF-amp}} \approx \frac{2}{\left(1+T_{bas}\right)} \tag{2.48}$$

Applying similar assumptions to equation 2.43,

$$S_{g_m R_o}^{G_{ASF3-amp}} \approx \frac{3}{\left(1+T_{as3}\right)} \tag{2.49}$$

Since T_{as3} is larger than T_{ac} and T_{bas}, the ASF3-amp has the lowest gain sensitivity among the four amplifiers.

If loading effects are important, we can evaluate equation 2.1, 2.32, 2.40 and 2.43 directly as function of $g_m R_o$. The four equations are plotted in figure 2.39 where $\frac{g_{m1}}{g_{mf}} = 8$ is assumed. Notice that the calculated amplifier gain at $g_m R_0 = 4.5$ agrees well with the

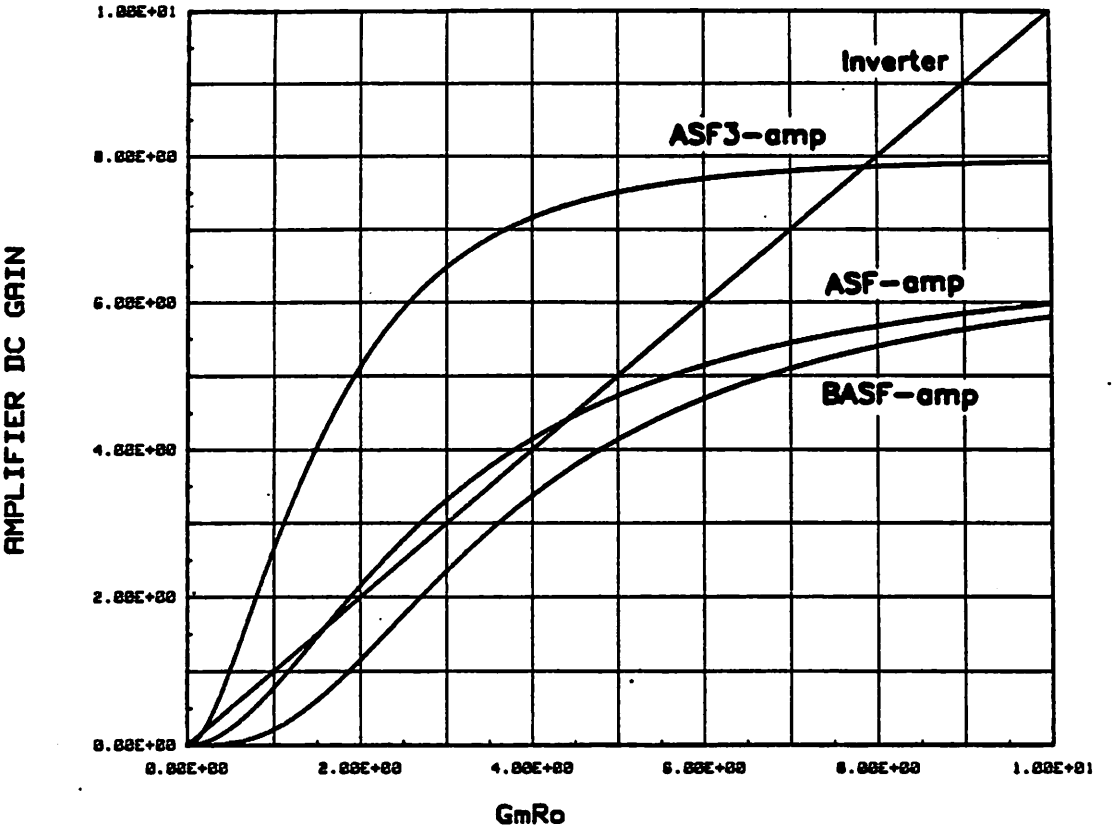


Fig. 2.39 Calculated amplifier gain versus $g_m R_o$.

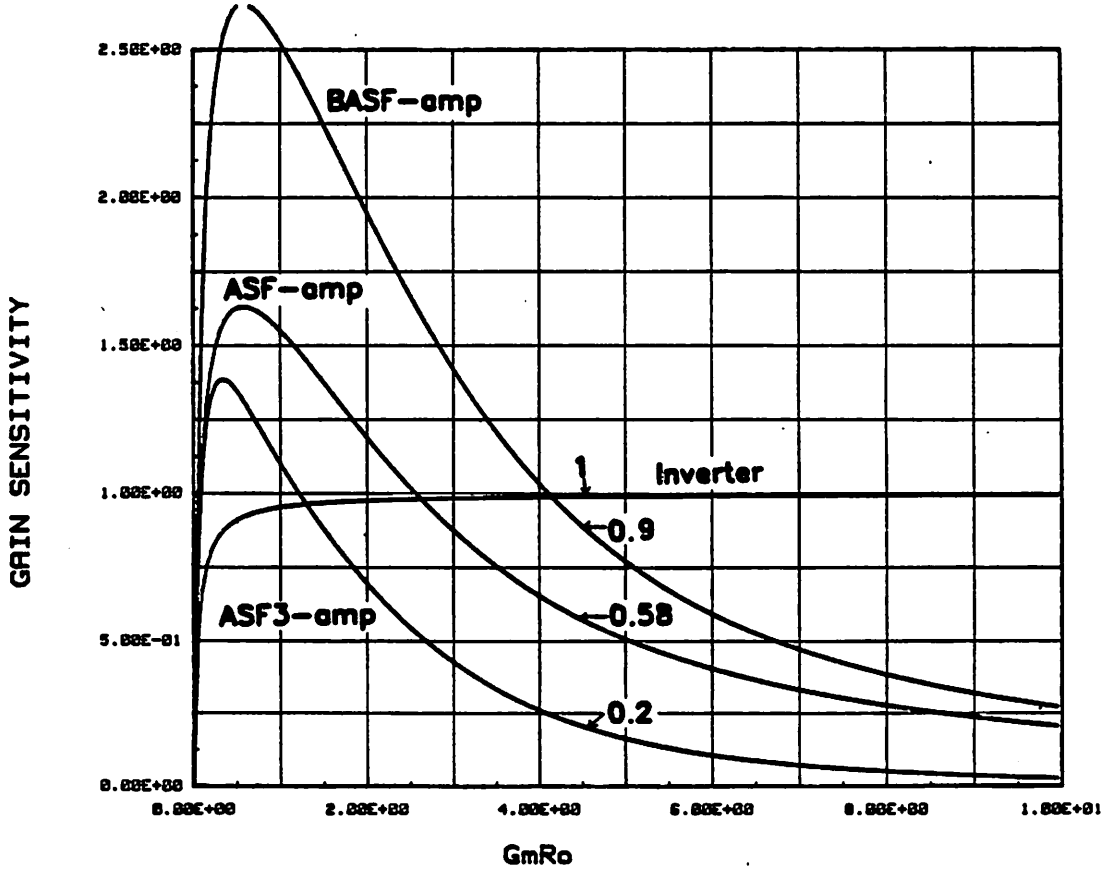


Fig. 2.40 Calculated amplifier gain sensitivity to $g_m R_o$.

simulated results in section 2.3 and 2.4. Using numerical differentiation, the sensitivities of the three amplifiers are plotted in figure 2.40 versus $g_m R_o$. Since our inverter gain is 4.5, the sensitivities of the Inverter, the ASF-amp, the BASF-amp and the ASF3-amp to $g_m R_o$ are 1, 0.58, 0.9 and 0.2 respectively.

Table 2.4 summarizes the performance of the four amplifiers. Each amplifier has its advantage over the others. For example, the Inverter has the lowest power consumption because it has only a single stage. The -3dB bandwidth of the BASF-amp is highest among the four amplifiers at 2.6GHz. The gain sensitivity of the ASF3-amp is lowest among the different designs, but the normalized gain-bandwidth product is only 1.77GHz. This is because frequency compensation is required for the ASF3-amp. The normalized gain-bandwidth products of the ASF-amp and the BASF-amp are equal to the GBW of the single-stage inverter.

The choice of which amplifier topology to use ultimately depends on the application. In chapter 3, where we consider the design of high-speed voltage comparators, a preamplifier is needed with the highest possible bandwidth but only moderate gain stability. From table 2.4, the BASF-amp seems suitable for such an application. Indeed, it will be shown in chapter 3 that the comparator which incorporates the BASF-amp design in its preamplifier has the highest speed performance.

	Gain	BW (GHz)	$G^{1/N}BW^{*}$	S^{G}_{gmRo}
Inverter	4.5	0.8	3.6	1
ASF-amp	4.4	1.7	3.6	0.6
BASF-amp	3.8	2.6	3.6	0.9
ASF3-amp	7.2	0.93	1.7	0.2

* N=1 for Inverter, N=2 for ASF-amp, N=4 for BASF-amp, N=3 for ASF3-amp.

Table 2.4 Summary of Amplifier Performances.

Chapter 3 High Speed Voltage Comparators

This chapter focuses on the design of high-speed voltage comparators in the SiGMOS technology. The comparators discussed here are applicable to flash A/D converters and to optical repeaters. Some applications require a comparator with the highest comparison rate, while others require a comparator with the shortest delay. A design that achieves high comparison rate may not be the one that gives the shortest possible delay, and vice versa. Since there is no design theory or principle in today's literatures that deals with high-speed voltage comparators in general, this chapter approaches the problem by analyzing four basic comparator configurations. Most existing comparators should fall into one of these four categories. For each configuration, a first order analysis of the dynamic behavior of the circuit is presented. This analysis generates useful design equations and curves which are used to optimize the comparator performance. In order to compare the performance of each configuration, optimized design examples based on the four configurations are simulated using SPICE with a worst-case input waveform - the previous sample is always driven to the negative full-scale input voltage $-V_{fs}$ while the present sample is either +31mV or -31mV ($\pm lsb$) around the reference voltage. This input is equivalent to 6 bits of input resolution.

Section 3.1 discusses the design and the non-idealities of the MOS input sample-and-hold. Section 3.2 investigates the simplest comparator configuration - a cascade of open-loop amplifiers. Although this configuration is straight forward, its analysis is complicated by the fact that the initial conditions are large signals and the problem cannot be assumed linear. A non-linear simulation program that gives useful design informations about this configuration is described in section 3.2.1. In section 3.3, the comparator configuration presented in section 3.2 is modified by using MOS switches to reset the node voltages to zero in every clock cycle. In this case, the zero-state response can be obtained by Laplace transforms. Closed form solutions are derived for the two cases where the gain per stage is either finite or infinite. In section 3.4, a comparator configuration based on pipelined processing is described. Here, real-time delays are traded for high comparison rate.

Section 3.5 presents an analysis of a simple MOS latched comparator which is similar in configuration to the popular latched comparator in bipolar technology [30]. Two improved designs relying on the positive feedback regeneration in the latch are then described. Finally, section 3.6 summarizes the performance of the different comparators.

3.1 Input Sample-and-Hold

The function of a comparator is to decide whether its input signal is positive or negative with respect to some reference at a given instant in time. Most comparators use an input sample-and-hold (*S/H*) to sample the input waveform at a time defined by a clock and to hold the sampled value long enough for the comparator to make its decision. *S/H* is commonly used in digital signal processors with an A/D converter to digitize analog waveforms and in discrete-time analog systems such as switched-capacitor filters.

An ideal *S/H* samples the instantaneous value of the input waveform. Typical waveforms of an ideal *S/H* are depicted in figure 3.1. An ideal *S/H* can be implemented by a multiplier with one of its inputs driven by a *comb* of delta functions. The problem with this approach is that the *comb* of delta functions is hard to generate at high frequencies. In practice, two track-and-hold (*T/H*) circuits connected in series function as an ideal *S/H*, as illustrated by the waveforms in figure 3.2. Each *T/H* consists of an ideal switch, a capacitor and a unity-gain output buffer. The switches are toggled by two square pulses of 50% duty cycle. When ϕ_1 is high, V_{o1} tracks the input waveform, and when ϕ_1 is low, V_{o1} is held at the previous level. Notice that V_{o2} is the output waveform of an ideal *S/H* shown in figure 3.1.

MOS technology is well suited to implementing a fast *T/H*. First, the gate of a MOS transistor is capacitive and charge can be stored at the gate node. The output voltage can be held for a longer time without significant droop. Secondly, a MOS transistor acts like a voltage switch with zero offset. Non-idealities of the MOS transistor such as $\frac{kT}{C}$ noise, charge injection, clock coupling, and finite on-resistance limit the ultimate resolution and sampling rate of the MOS *T/H*.

Using half-circuit representation, non-idealities are analyzed and design equations are presented in section 3.1.1 for a differential MOS *T/H*. A design example of a 6-bit MOS *T/H* then follows in section 3.1.2. The maximum sampling rate of this *T/H* is 1 GS/s which is an order of magnitude faster than existing MOS *S/H* circuits.

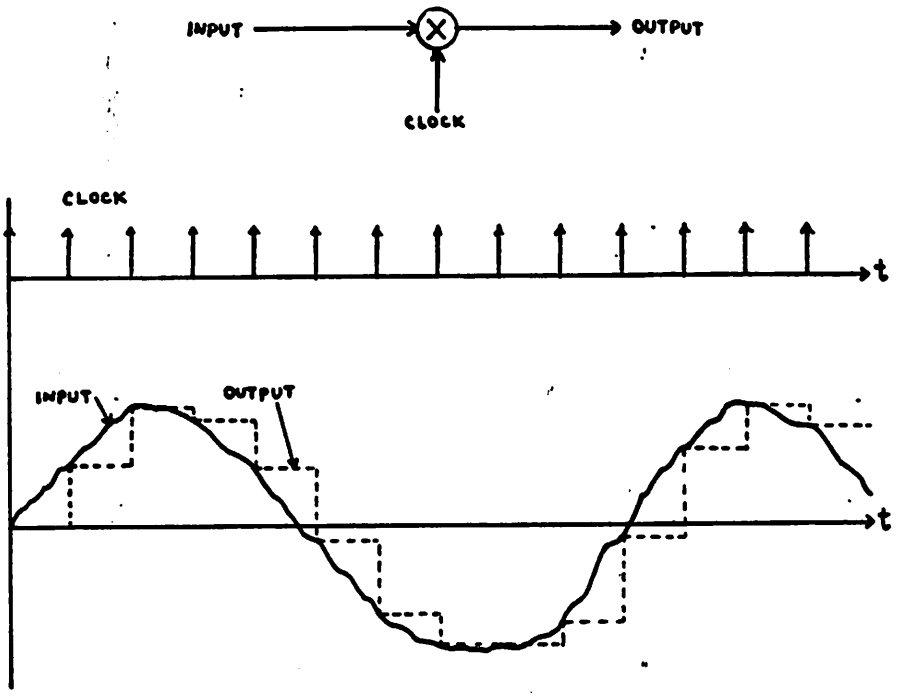


Fig. 3.1 An ideal input sampler with clock, input and output waveforms.

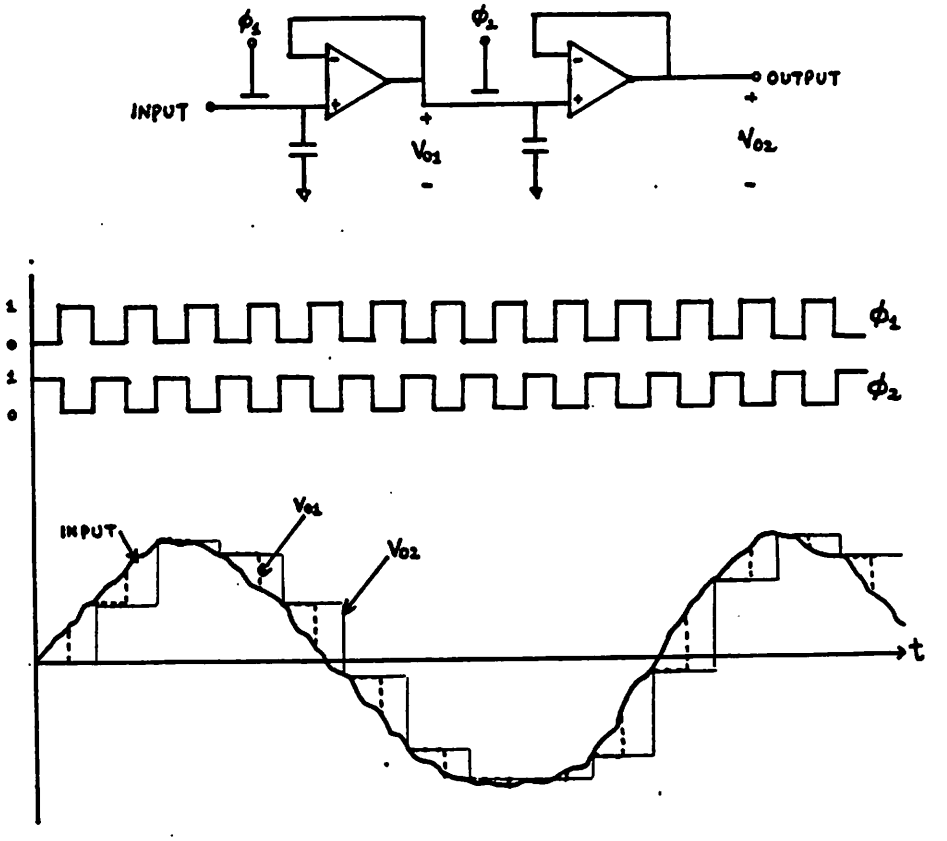


Fig. 3.2 A MOS sample-and-hold which consists of two MOS track-and-hold.

3.1.1 Non-Idealities of A Differential MOS T/H.

The effect of clock coupling and charge injection in MOS circuits can be reduced most effectively by using differential circuits [15]. In this section, we consider the design of the the differential *T/H* shown in figure 3.3. In this circuit, when ϕ_1 is high the differential voltage across the input of the differential pair tracks $V_{in}-V_{ref}$. At the falling edge of ϕ_1, the input is sampled onto a pair of matching capacitors C_1 and C_2. The sampled value is held constant when $\phi 1$ is low. The differential pair in figure 3.3 can be the input stage of a comparator. The limitations on the performance of this circuit are as follows.

$\frac{kT}{C}$ noise

To analyze the effect of $\frac{kT}{C}$ noise, refer to the differential-mode half-circuit in figure 3.5 where C_{dm} is the differential capacitance seen by M_1 and M_2 (refer to equation 3.11). When a MOS switch is turned on, the resistance across its drain and source is finite. The thermal noise of the channel resistance R_{ch} is sampled onto the capacitor at the falling edge of the clock. The variance of this noise, according to [16], is

$$\int_0^\infty 4kTR_{ch}|H(jf)|^2df = \frac{kT}{C_{dm}} \tag{3.1}$$

where

$$H(jf) = \frac{1}{1+j2\pi fR_{ch}C_{dm}} \tag{3.2}$$

Since its variance is independent of R_{ch}, this noise is commonly referred to as $\frac{kT}{C}$ noise.

The resolution of the MOS *T/H* is ultimately limited by this noise component. The root-mean-square value of the $\frac{kT}{C}$ noise must be less than the expected resolution of the comparator (V_{lsb}). In terms of the number-of-bits B and assuming 2V full scale, we have

$$\left(\frac{kT}{C_{dm}}\right)^{\frac{1}{2}} \leq 2^{1-B} \tag{3.3}$$

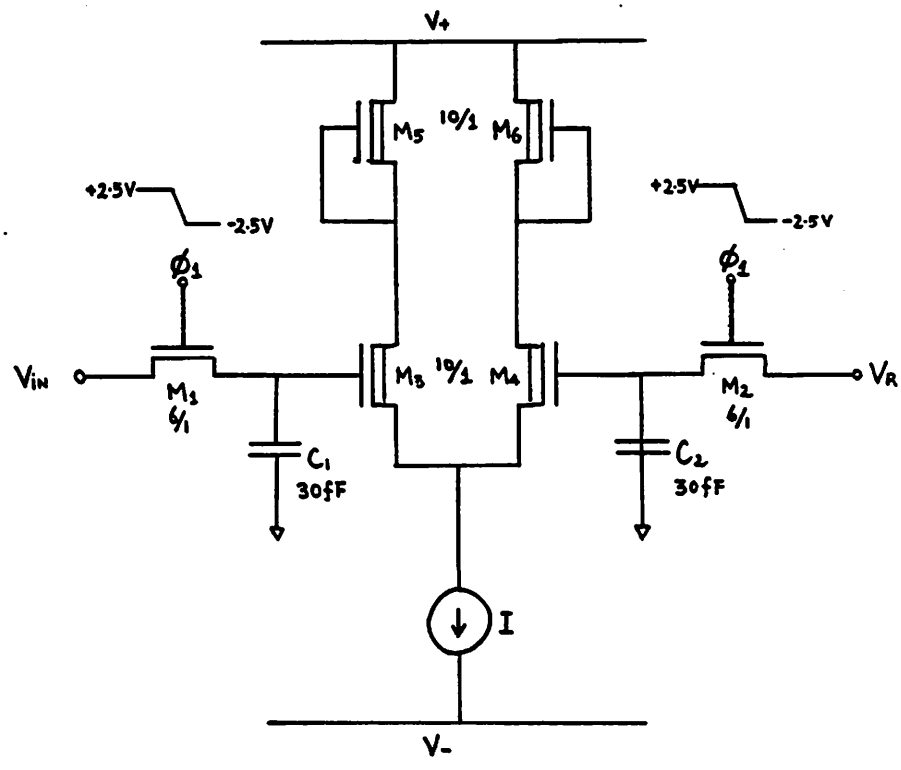


Fig. 3.3 A differential MOS T/H.

At room temperature, kT=4.15e-21; therefore

$$B \leq 34.85 + 1.66log(C_{dm}) \tag{3.4}$$

Equation 3.4 relates the size of the sampling capacitor to the resolution of the *T/H*. For example if C_{dm} is 60fF, $\frac{kT}{C}$ noise would limit the resolution of the *T/H* to about 13 bits.

Charge Injection and Clock Coupling

If M_1, M_3 and C_1 in figure 3.3 are perfectly matched to M_2, M_4 and C_2 respectively, then to the first order, charge injection and clock coupling from the two MOS switches will not affect the resolution of the *T/H*. The clock that drives the *T/H* in figure 3.3 is a periodic pulse train that oscillates between V_H and V_L with a 50% duty cycle. When ϕ_1 is high, $V_1=V_{in}$ and $V_2=V_{ref}$. As ϕ_1 goes low, both channel-charge injection and clock coupling occur. The problem is best analyzed using the concept of equivalent half-circuit.

The common-mode half-circuits of the *T/H* before and after the clock transition are shown in figure 3.4. In figure 3.4, the initial common-mode voltage at the output is

$$v_{cmi} = \frac{V_{in}+V_{ref}}{2} \tag{3.5}$$

the common-mode channel charge is

$$q_{cm} = C_{ox1,2}(V_H - v_{cmi} - V_T) \tag{3.6}$$

and the common-mode capacitance seen by the two MOS switches is

$$C_{cm} = C_{1,2} + C_{gd3,4} \tag{3.7}$$

Assuming the worst condition, where the clock fall time is much less than $R_{ch}C_{ox1,2}$, half of q_{cm} is injected into the output nodes as common-mode signal. The final common-mode voltage at the output is

$$v_{cmf} = \frac{V_{in}+V_{ref}}{2} - \frac{C_{ol1,2}}{C_{ol1,2}+C_{cm}}(V_H - V_L) - \frac{C_{ox1,2}}{2(C_{ol1,2}+C_{cm})}\left(V_H - \frac{V_{in}+V_{ref}}{2} - V_T\right) \tag{3.8}$$

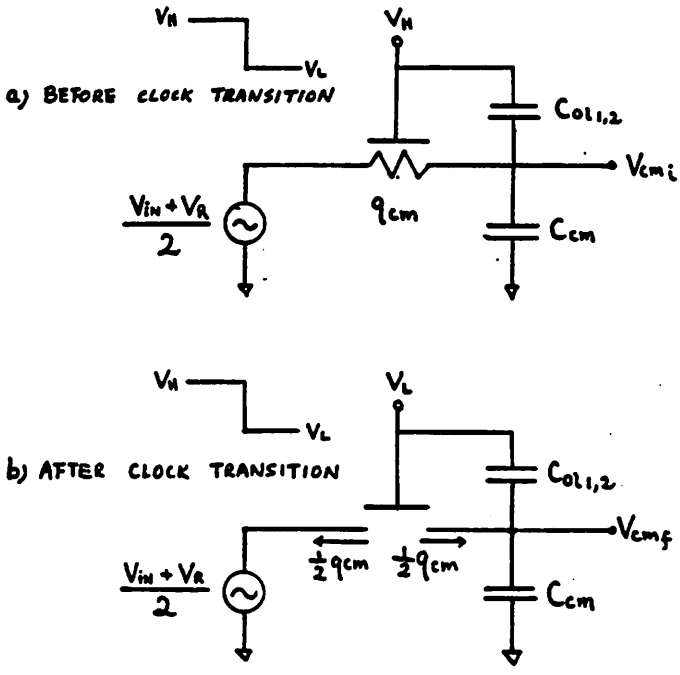


Fig. 3.4 Common-mode half-circuit of MOS T/H before and after clock transition.

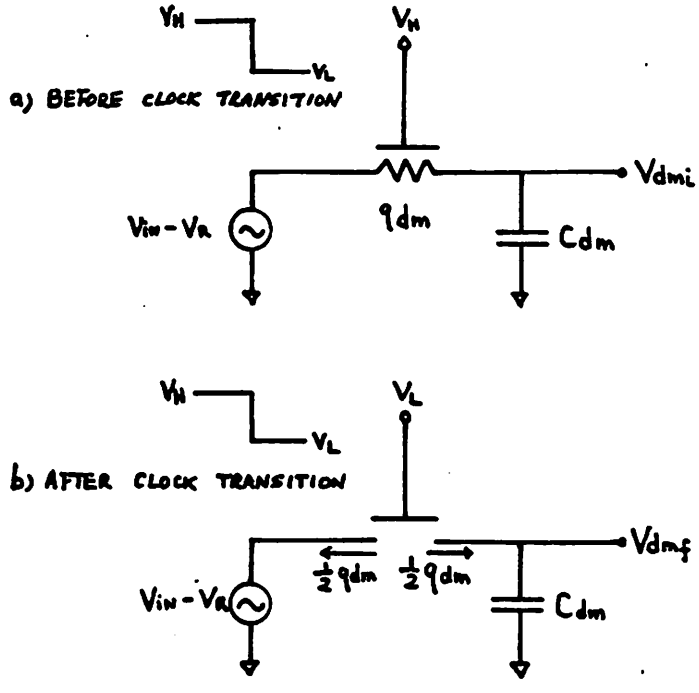


Fig. 3.5 Differential-mode half-circuit of MOS T/H before and after clock transition.

In equation 3.8, the second and third term represent a common-mode voltage shift due to clock coupling and channel charge injection respectively. This shift of common-mode voltage degrades the common-mode range of the comparator.

If the transistor and capacitors are perfectly matched, the differential-mode half-circuits before and after the clock transition are shown in figure 3.5. The initial differential-mode voltage at the output is

$$v_{dmi} = V_{in} - V_{ref} \tag{3.9}$$

the differential charge stored in the channel is

$$q_{dm} = C_{ox1,2} v_{dmi} \tag{3.10}$$

and the differential capacitance seen by the switches is

$$C_{dm} = C_{1,2} + C_{ol_{1,2}} + C_{gs_{3,4}} + C_{gd_{3,4}}(1+A) \tag{3.11}$$

where A is the voltage gain of the differential pair $M_{3,4}$. The final output differential voltage is

$$v_{dmf} = (V_{in} - V_{ref})\left(1 + \frac{C_{ox1,2}}{2C_{dm}}\right) \tag{3.12}$$

The second term in equation 3.12 represents an error in the gain of the *T/H*. Gain error can be easily compensated for and is not a serious problem in *A/D* and comparator applications.

If the transistors and the capacitors in figure 3.4 are not perfectly matched, error introduced by charge injection and clock coupling can be modeled as a dc offset voltage in series with the *T/H* outputs. If the capacitances are mismatched by $\frac{\Delta C}{C}$%, the worst-cast offset voltage is

$$v_{os} \approx \frac{C_{ol}(V_H - V_L)}{C_{dm}}\left(4\frac{\Delta C}{C}\right) + \frac{C_{ox1,2}(V_H - V_{ref} - V_T)}{2C_{dm}}\left(4\frac{\Delta C}{C}\right) \tag{3.13}$$

This offset voltage is reduced by making C_{dm} large which in turn slows down the

acquisition time of the *T/H*. In practice, it is the matching of components that limits the resolution and the sampling rate of the *T/H*.

Channel Resistance and Acquisition Time.

Acquisition time of the *T/H* determines the maximum sampling rate of the *T/H*. The worst situation occurs when the previous sample equals the full scale voltage $-\frac{V_{fs}}{2}$ and the present sample equals to one *lsb* larger than the reference voltage which is at $+\frac{V_{fs}}{2}$. The acquisition time of a *T/H* is the time for the output to acquire a differential voltage equal to kV_{lsb} where k is less than 1 but larger than 0.707 (corresponding the gain of the T/H at the -3dB sampling frequency) when the initial differential voltage across the capacitor C_{dm} is $-V_{fs}$ and the present differential input being sampled equals V_{lsb}. For a *T/H* with resolution of B bits

$$V_{lsb} = V_{fs}2^{-B} \tag{3.14}$$

Referring to the differential-mode half-circuit in figure 3.5, the differential output voltage is

$$v_{dm}(t) = V_{lsb}+\frac{V_{fs}}{2}-(V_{lsb}+V_{fs})\exp\left[-\frac{t}{R_{ch}C_{dm}}\right] \tag{3.15}$$

The channel resistance is given by

$$R_{ch} \approx \frac{1}{\mu_o C'_{ox}\frac{W}{L}(V_{gs}-V_T)} \tag{3.16}$$

The acquisition time is

$$t_{ac} = R_{ch}C_{dm}\ln\left[\frac{V_{lsb}+V_{fs}}{V_{lsb}(1-k)}\right] \tag{3.17}$$

Together with equation 3.14, and assuming V_{fs}=2V

$$t_{ac} = R_{ch}C_{dm}[0.693B-ln(1-k)] \tag{3.18}$$

If B=6 and k=0.9, equation 3.16 gives $t_{ac}=6.46R_{ch}C_{dm}$. Equation 3.18 relates the small signal bandwidth of the *T/H* ($\frac{1}{2\pi R_{ch}C_{dm}}$) to the worst case acquisition time.

3.1.2 Design Example - A 6-bit 1GS/s T/H

Based on the equations derived in the previous section, a high-speed track-and-hold circuit capable of 6-bit resolution and 1 GS/s sampling rate has been designed. Computer simulation is used to verify the performance and the design equations used.

In the MOS *T/H* of figure 3.3. The width of transistor M_3 and M_4 is $10\mu m$ and the size of $C_{1,2}$ is 30fF. According to equation 3.7 and 3.11, C_{cm} and C_{dm} is about 30fF and 60fF respectively. From equation 3.4, $\frac{kT}{C}$ noise is seen to limit the resolution of this *T/H* to about 13 bits and this is not a concern in this design.

Since the intended sampling rate of the *T/H* is 1GS/s and the assumed clock rise and fall times are 150ps, the worst-case acquisition time of the *T/H* must be less than 350ps. From equation 3.18, the small signal bandwidth of the *T/H* is

$$\frac{1}{2\pi R_{ch} C_{dm}} = 2.93GHz$$

Together with equation 3.16 with $V_{gs}-V_T=2.5V$ and L=1, the width of switch M_1 and M_2 should be $6\mu m$ resulting in $R_{ch}\approx 900\Omega$. The common-mode voltage shift is 0.4V (from equation 3.8) and the differential-mode gain error is 1.09 (from equation 3.12).. Finally, using equation 3.13, the worst cast offset voltage due to capacitive mismatch is 35mV if $\frac{\Delta C}{C}=0.03$. To improve offset voltage, the size of $C_{1,2}$ can be increased, but this in turn will reduce the maximum sampling rate of the *T/H*.

To verify the above design, SPICE [12] has been used to simulated the ac and the transient response of the *T/H*. Figure 3.6 is the simulated small signal ac response of the *T/H* where $V_{ref}=V_{in}=1V$ and the clock input is at $V_H=3.5V$. In this simulation $C_{1,2}=30fF$, $W_{3,4}=10\mu m$ and $W_{1,2}$ is varied from $2\mu m$ to $10\mu m$ at $2\mu m$ per step increment. For the *T/H* with $W_{1,2}=6\mu m$, the -3dB bandwidth is 3.6GHz, which is higher than the required bandwidth of 2.93GHz.

Shown in figures 3.7 and 3.8 are the simulated transient responses of the common-mode and differential-mode output voltage, respectively. In these simulation the clock frequency is 500MHz with $V_H=3.5V$ and $V_L=-1.5V$. Clock waveform is also included in

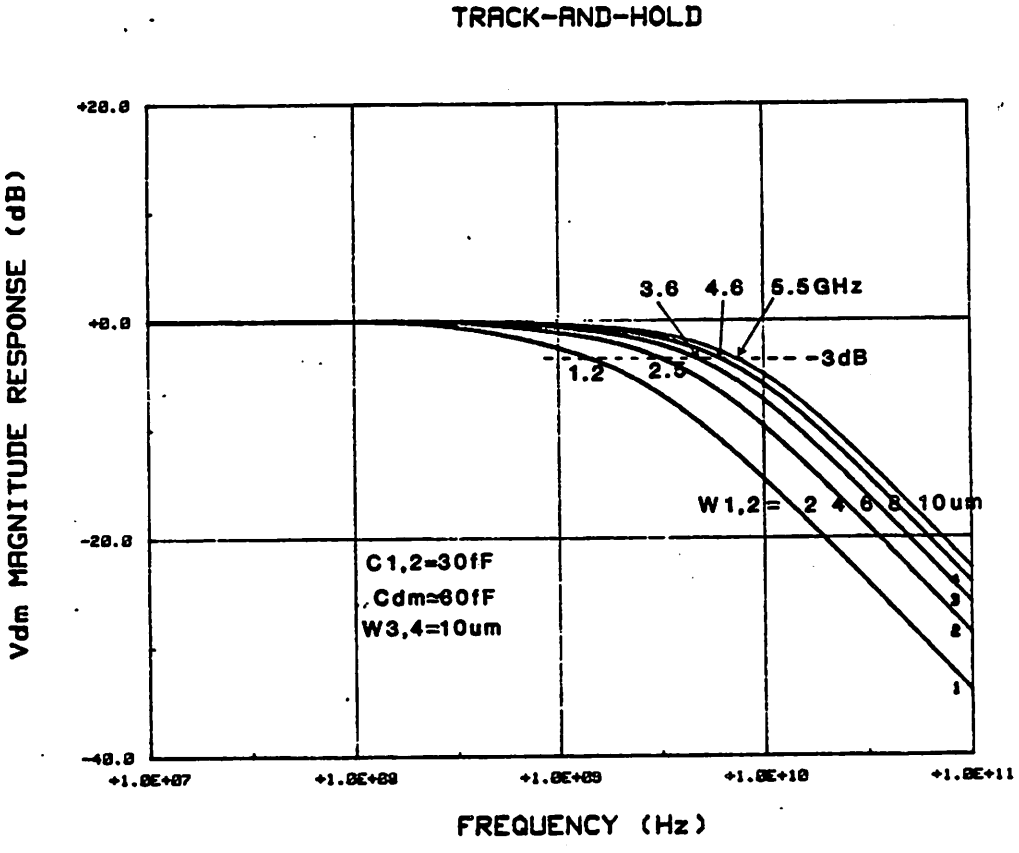


Fig. 3.6 Simulated frequency response of T/H for various values of $W_{1,2}$.

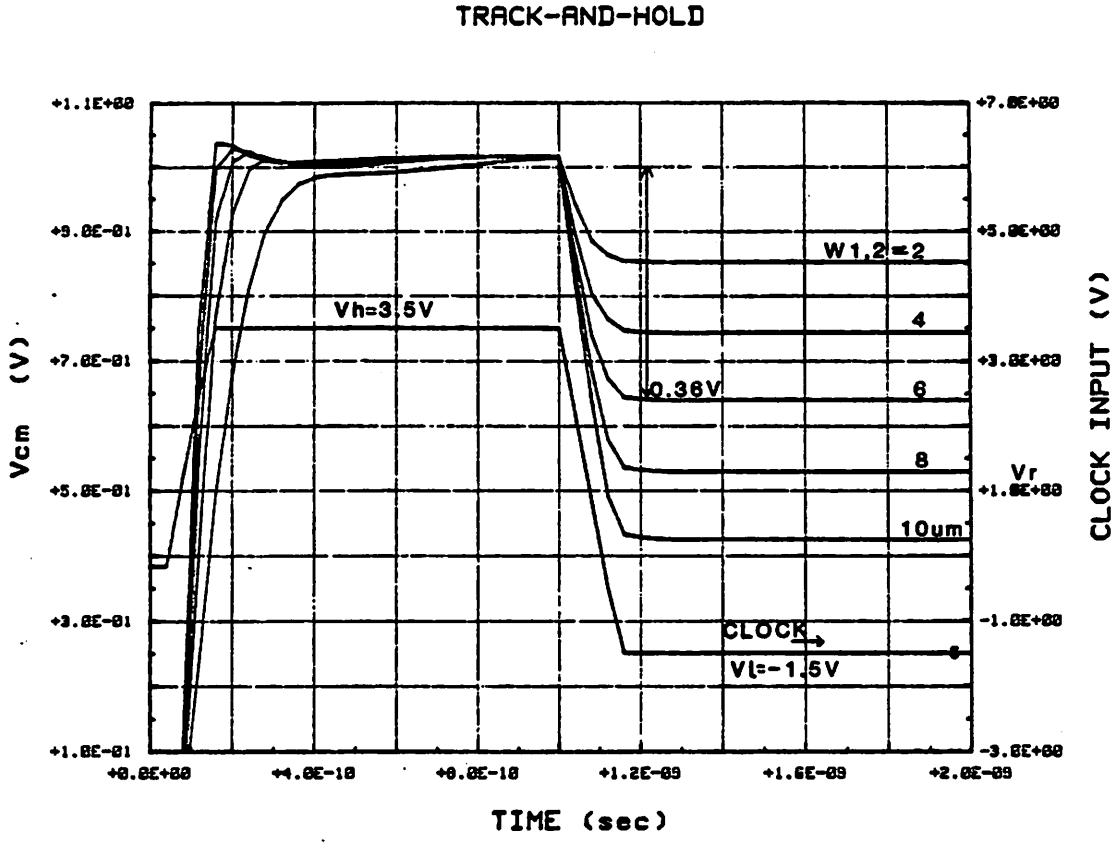


Fig. 3.7 Simulated common-mode output voltage of T/H

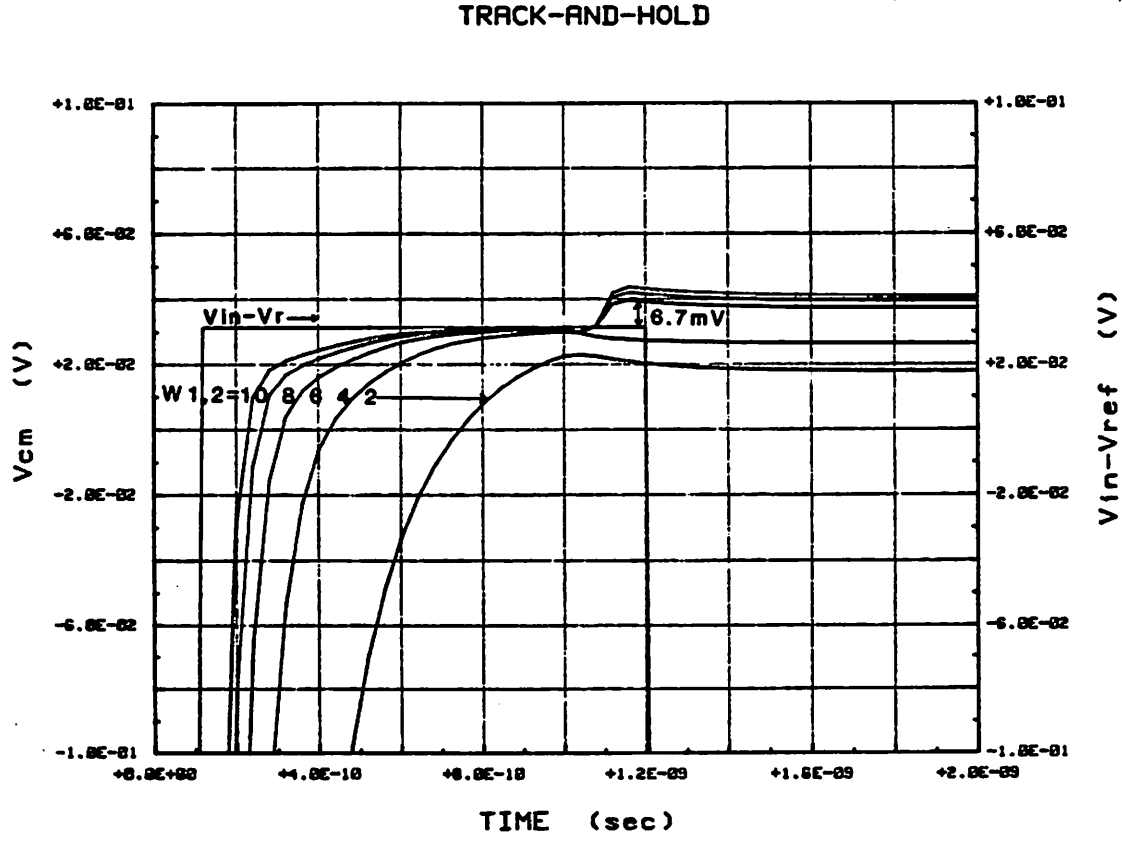


Fig. 3.8 Simulated differential-mode output voltage of T/H.

figure 3.7. The common-mode voltage shift is 0.36V and the differential-mode gain error is about, 1.18 which is higher than the prediction given by equation 3.12. The acquisition time is about 500ps (including clock rise-time); therefore the maximum sampling rate is 1GHz. In general, the design equations in the previous section are accurate enough to estimate the performance of the *T/H*.

3.2 Comparator I - Cascade of Open Loop Amplifiers

Let us first consider the simplest voltage comparator configuration, namely a cascade of differential open-loop amplifiers as shown in figure 3.9. A similar comparator design in MOS was used in a voice-frequency PCM CODEC [17]. This comparator configuration is not the fastest considred in this chapter because its speed performance is limited by the overdrive recovery time of the entire cascade. Nevertheless, an understanding of the various trade-off in this configuration gives insights to comparator design in general.

The small signal ac equivalent circuit of figure 3.9 is shown in figure 3.10. The equivalent circuit of bipolar comparators that employ open-loop amplifiers [18,19] is similar to figure 3.10. Most commercial comparators (i.e. [37]) are uncompensated operational amplifiers with two stages of open loop gain. In general, the analysis presented in this section applies equally well to bipolar comparator design.

The circuit of figure 3.9 is fully differential and the common-mode rejection ratio of the differential pairs is assumed to be infinite. If all voltage levels considered in this section are within the common-mode range of the differential pairs, we only need to consider differential signals. If it is not stated specifically, all voltages referred to in this section are differential quantities.

The input of the comparator is driven by an input *T/H* which defines the instant of comparison and holds the sampled signal long enough for the comparator to make its decision. To simplify hand calculations, we assume that the *T/H* has infinite bandwidth and its acquisition time approaches zero. Under this assumption, the worst-case comparator delay (t_c) is the time required by the comparator to establish a large signal voltage at its output ($+V_{final}$) when its input is first over driven to the negative full-scale voltage ($-V_{fs}$) at t_{0-} and then driven to a voltage (V_{lsb}) equals to the expected resolution of the comparator at time t_{0+}, where $t_{0+} - t_{0-} \to 0$. If the comparator is used to directly drive MOS logic gates, V_{final} should equal 5V. Given the equivalent input resolution in terms of the number of bits B, V_{lsb} is related to V_{fs} by

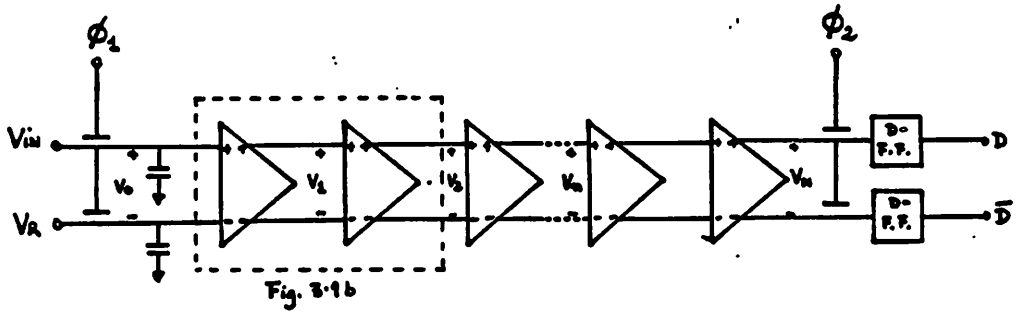


Fig. 3.9a Configuration of Comparator I - cascade of open-loop amplifiers.

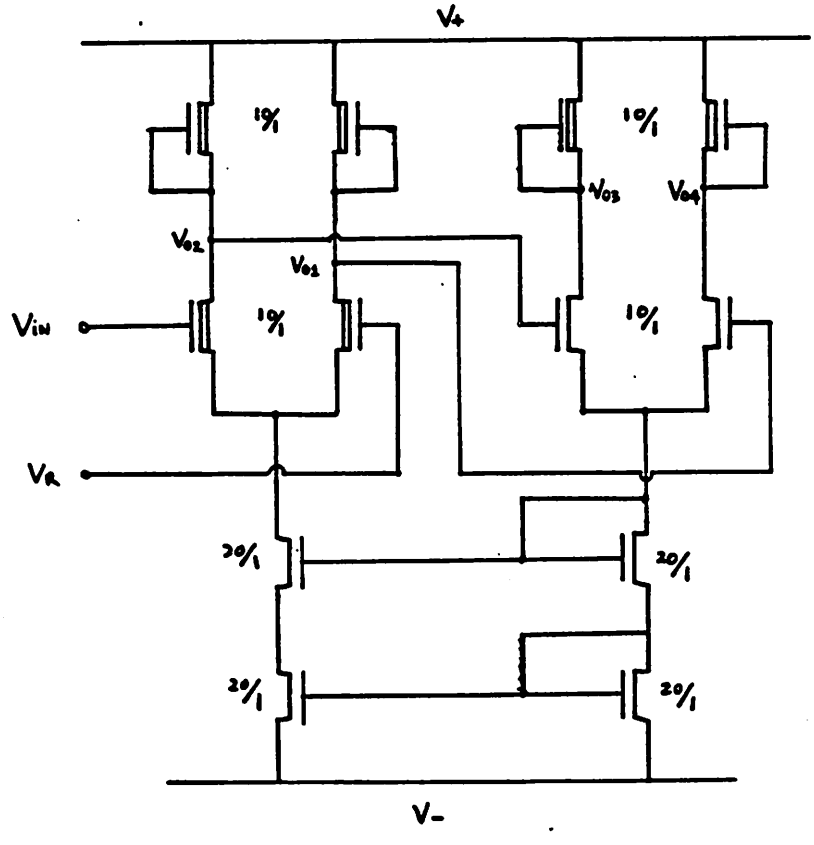


Fig. 3.9b Complete circuit schematics of a pair of open-loop amplifiers used in figure 3.9a with a common-mode feedback biasing scheme.

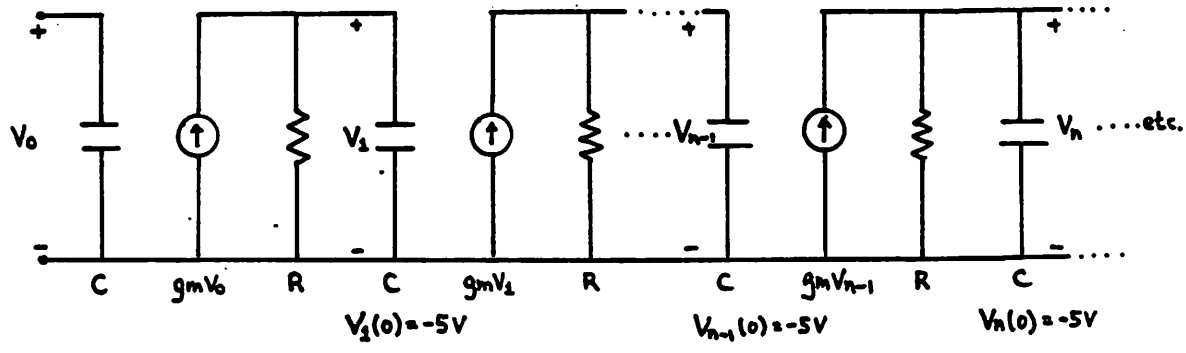


Fig. 3.10 Small signal equivalent circuit of figure 3.9.

$$V_{lsb} = V_{fs}2^{-B} \tag{3.19}$$

The number of stages N and the gain per stage g_mR are left as variables. R is the output resistance of the differential pair. Given B, V_{fs} and V_{final}, what number of stages N and gain per stage g_mR give minimum t_c?

To state the problem more concisely and to define the terms in this section:

For the comparator configuration shown in figure 3.9, system constants are as follow:

1 $V_{final} = 5V$ (final output voltage large enough to drive digital logic),

2 $V_{fs} = 2V$ (full scale input voltage, which is s limited by common mode range of the input differential pair), and

3 $\frac{g_m}{C} = 2\pi \times 3.65\times 10^9$ (gain-bandwidth-product for the SiGMOS technology).

The variables of the problem are:

1 $B \in integer[1,2,....,16]$ (input resolution in term of number of bit),

2 $g_mR \in real[1,\infty]$ (gain per stage),

3 $N \in integer[1,.....,20]$ (number of stage), and

4 $V_n(0) \in real$ where $n \epsilon N$ (initial condition).

For all possible values of the above variables, we need to find the following unknowns,

1 $V_n(t)$, the output waveform of stage n

2 $t_c(n)$, the time at which $V_n(t) \geq V_{final}$.

3.2.1 Transient Analysis

For the configuration in figure 3.9, the comparator is first driven to $-V_{fs}$ at time t_{0-}. Therefore the initial conditions of the N capacitors are not zero. Furthermore, the initial conditions are large signals and the system can not be assumed linear. Consequently, no close form solution exists for $t_c(n)$ and $V_n(t)$.

The transient analysis in SPICE could be used to simulate the complete response of the comparator accurately. However to find the optimum N and g_mR, it is necessary to iterate for different values of N, g_mR, and B, and this requires excessive computer time. Therefore the computer program listed in appendix A-5 was written to provide transient analyses of the circuit in figure 3.9. The program is written in Basic for the HP-9836 personnel computer.

Referring to figure 3.10, the nodal equation at the output node of the nth stage in the comparator is simply

$$C\frac{dV_n(t)}{dt} = g_mV_{n-1}(t)-V_n\frac{(t)}{R} \tag{3.20}$$

where $V_n(t)$ is the differential voltage across the outputs of the nth stage. After integrating both sides and rearranging terms,

$$V_n(t) = \frac{1}{C}\int_0^t\left(g_mV_{n-1}(t')-\frac{V_n(t')}{R}\right)dt'+V_n(0)$$

A discrete time version of the above equation is

$$V_n(T) = \frac{1}{C}\sum_{k=0}^{T}\left(g_mV_{n-1}(k)-\frac{V_n(k)}{R}\right)\Delta T+V_n(0)$$

$$= V_n(T-1)+\frac{1}{C}\left(g_mV_{n-1}(T)-\frac{V_n(T)}{R}\right)\Delta T$$

where $k\times\Delta T=t$. Solving for $V_n(T)$

$$V_n(T) = \frac{V_n(T-1)+\frac{g_m}{C}V_{n-1}(T)\Delta T}{1+\frac{\Delta T}{RC}} \tag{3.21}$$

If all initial conditions are set to -5V ($V_n(0)=-5$ for all n), and the input is constant for T>0 ($V_0(T)=V_{lsb}$ for all T), equation 3.21 can be evaluated directly for all values of n and T. The program listed in appendix A-5 (referred to as *program A−5*) calculates $V_n(T)$ using two nested *do loops* with T as the first index and n as the second index. To include the effect of clipping caused by nonlinearities and power supply at output nodes, the following conditions are imposed inside the *do loops*.

1 If $V_n(T)\geq V_{final}$, then $V_n(T)=V_{final}$.

2 If $V_n(T)\leq V_n(0)$, then $V_n(T)=V_n(0)$.

For the MOS differential pair in figure 3.9, the output resistance R is not linear for the voltage range of concern. As shown in appendix A-1 (figure A-3), R can be modeled by a Gaussian function with 0V mean and 3.5V standard deviation. The large signal output resistance is

$$R_l=R\ \exp\left[-\frac{1}{2}\left(\frac{V_n(T)}{3.5}\right)^2\right] \tag{3.22}$$

where

$$R=r_{oE}||r_{oD}||\frac{1}{g_{mbD}}$$

r_{oE} and r_{oD} are the small signal output resistance of the enhancement and the depletion transistor,respectively, and g_{mbD} is the backgate transconductance of the depletion transistor. Their measured values are listed in table A-1 in appendix A-1. R_l is substituted for R in equation 3.21. Equation 3.19 to 3.22 summarize the implementation of *program A−5*. If we use this program to simulate transient response of a bipolar comparator with an open-loop configuration, V_{final} and $V_n(0)$ would typically equal +1V and -1V respectively (ECL levels), while R_l would be the linear load resistor.

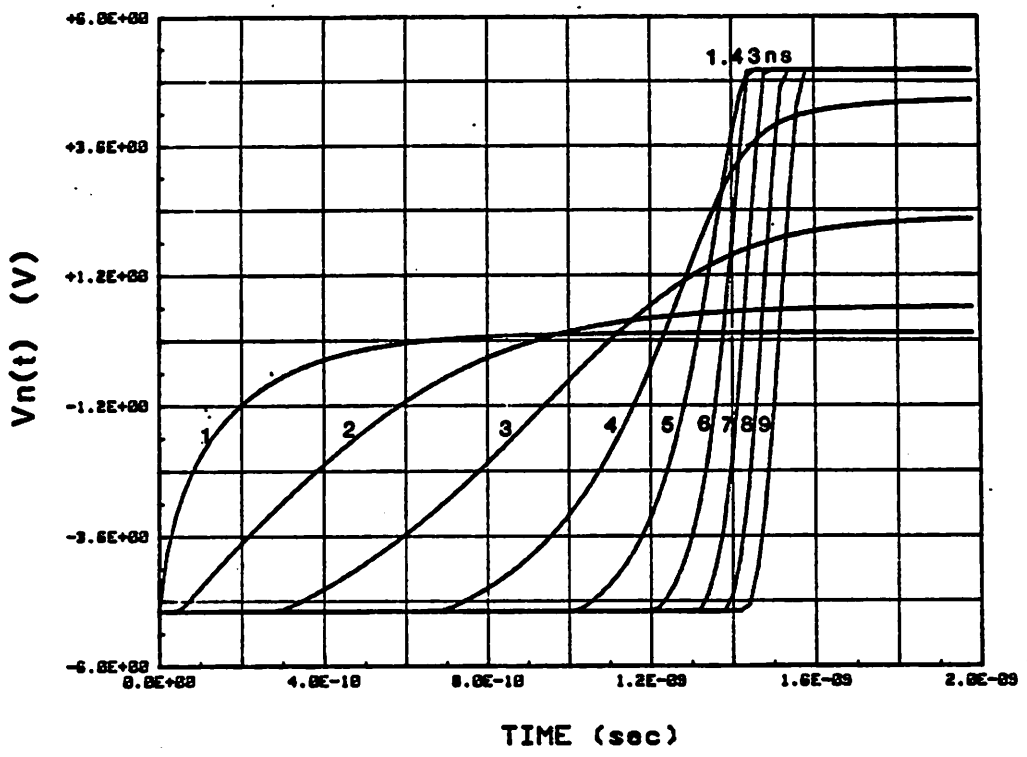


Fig. 3.11 Simulated step response of the comparator in figure 3.9 using *program* $A-5$ with B=6, $V_n(0)=-5V$ and $g_m R=4.5$.

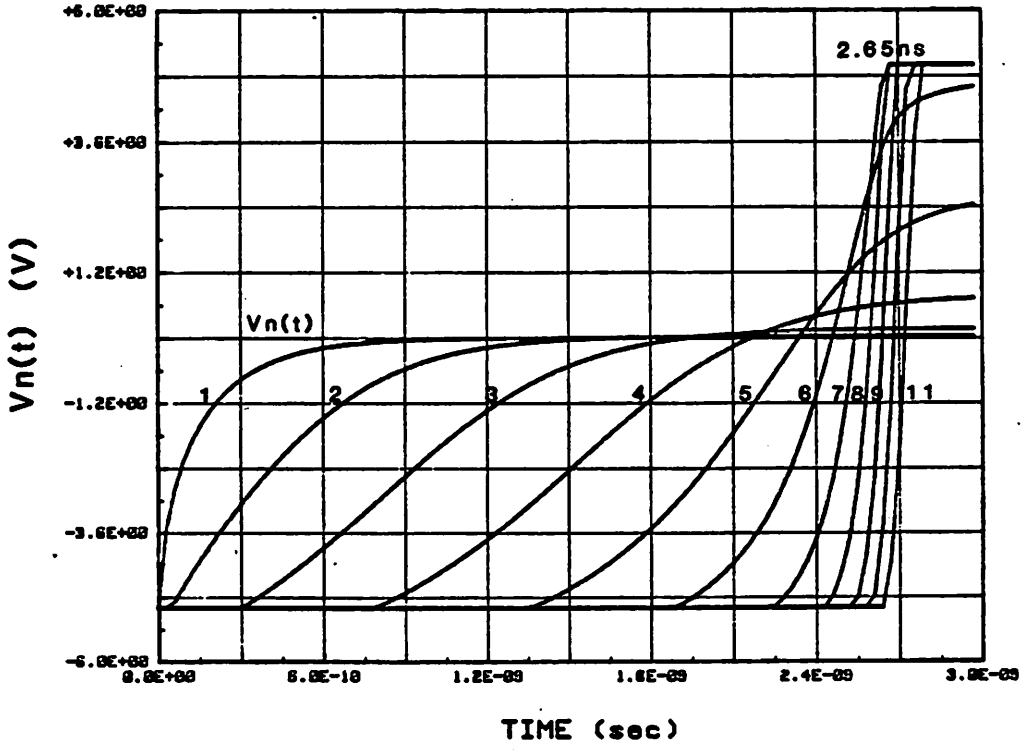


Fig. 3.12 Simulated step response of the comparator in figure 3.9 using *program* $A-5$ with B=10, $V_n(0)=-5V$ and $g_m R=4.5$.

Simulation and Interpretation

Using *program A−5*, $V_n(t)$ is plotted in figure 3.11 where n ranges from 1 to 9. In figure 3.11, B=6, and g_mR=4.5. In figure 3.18, SPICE is used to simulate $V_n(t)$ with results in good agreement with figure 3.11. The output of the sixth stage reached 5V in 1.45ns. The output of stages one through four never reached V_{final} because of the small g_mR. For n higher than 6, $V_n(t)$ is a constant delay of its input $V_{n-1}(t)$, and the delay is about 60ps. This delay is equivalent to the ring oscillator delay discussed in section 2.2. The comparator delay t_c is the time for V_n to reach V_{final}. Therefore $t_c(n)$ is infinite for n<5, has a minimum at n=6, and increases at a 60ps/n rate for n>6. $t_c(n)$ can be simulated for any combinations of B and g_mR. In figure 3.12, only B is changed (to 10). For this case, $t_c(n)$ has a minimum at n=8 and $t_c(8)=2.65ns$.

In figure 3.13 $t_c(n)$ is plotted for various values of B while g_mR is fixed at 4.5. For a given B, there exists a minimum $t_c(n)$ which corresponds to the optimum design in terms of the number of stages (n_{opt}) required to provide minimum comparator delay. When a minimum in $t_c(n)$ is detected, *program A−5* prints the current value of B at the location of the local minimum. Since in the SiGMOS technology, the voltage gain of a one-one inverter is determined by device g_mr_o and cannot be varied easily, figure 3.13 gives an overview of the delay performance for the comparator in figure 3.9. Based on only dc considerations, the relationship for the minimum number of stages $n_{\min}$ required is

$$V_{final} \leq \frac{V_{fs}}{2^B}(g_mR)^{n_{\min}}$$

Thus

$$n_{\min} \geq \frac{\log\left(\frac{V_{final}}{V_{fs}}2^B\right)}{\log\,(g_mR)} \tag{3.23}$$

From figure 3.13,

$$n_{opt} \approx n_{\min}+3 \tag{3.24}$$

and equation 3.24 can be used as a rule of thumb if g_mR=4.5.

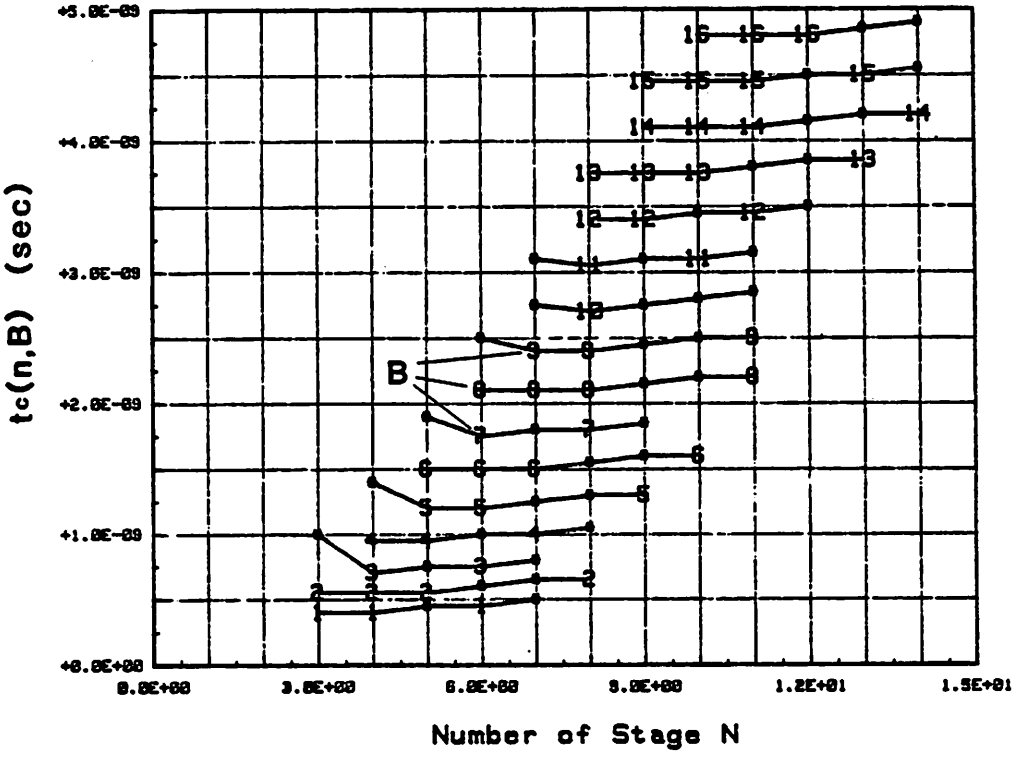


Fig. 3.13 Simulated comparison time t_c of the comparator in figure 3.9 versus n and B using *program* $A-5$ with $g_m R=4.5$, $V_n(0)=-5V$ and $V_{final}=+5V$.

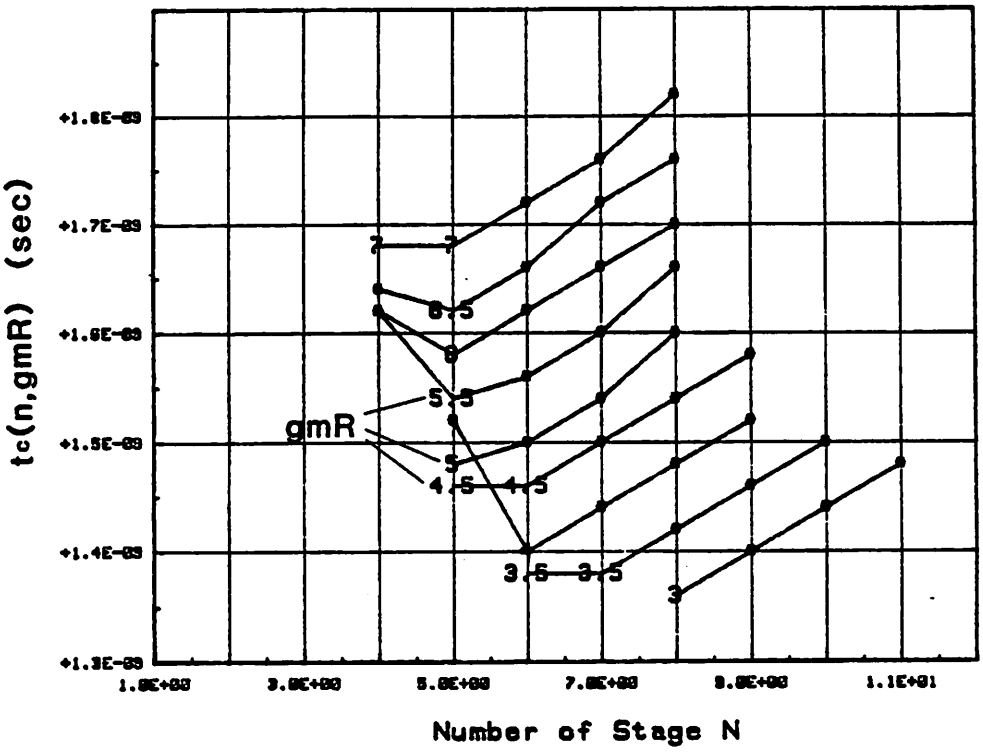


Fig. 3.14 Simulated comparison time t_c of the comparator in figure 3.9 versus n and $g_m R$ using *program* A_5 with B=6, $V_n(0)=-5V$ and $V_{final}=+5V$.

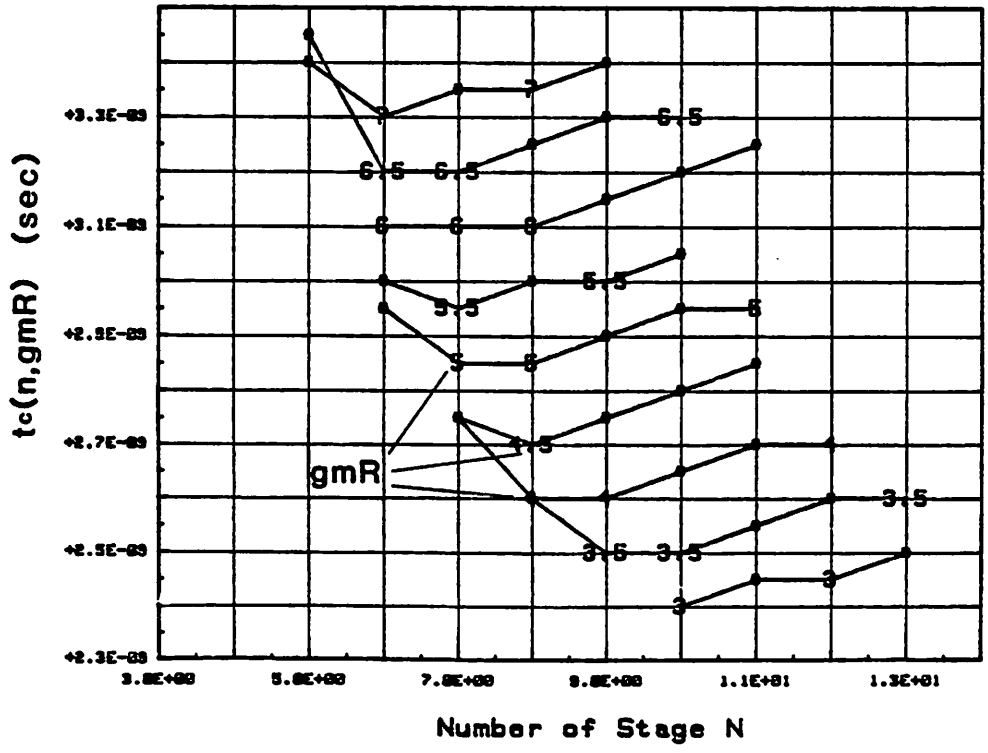


Fig. 3.15 Simulated comparison time t_c of the comparator in figure 3.9 versus n and $g_m R$ using *program* $A-5$ with B=10, $V_n(0)=-5V$ and $V_{final}=+5V$.

To this point, we have fixed g_mR to 4.5, and allowed only n and B to vary when. To determine the optimun gain per stage, g_mR is allowed to change in the program. Figure 3.14 is a plot of $t_c(n)$ for various values of g_mR while B is fixed. For a comparator with 6-bit resolution, the optimal design for this configuration is N=8 and g_mR=3 (assuming g_mR can be changed at will). The comparator delay for this design is 1.37ns, which represents a 10% improvement over the design with n=6 and g_mR=4.5. Figure 3.15 plots the same information as figure 3.14, but for B=10. Again optimum g_mR is 3, and n_{opt}=10.

Since the initial conditions are not zero at time t_0, the speed performance of this type of comparator is limited by the overdrive recovery time of the cascade of differential pairs. Referring to figure 3.10, the charge stored on the capacitor C is initially discharged through the resistor R (when $V_{n-1}(t)\leq 0$), therefore overdrive recovery time is proportional to the RC time constant at the output nodes (or equivalently to g_mR). As g_mR approaches unity, $n_{\min}$ in equation 3.23 approaches infinity. This means as g_mR becomes smaller, the number of stage increases, $t_c(n,g_mR)$ increases, and a minimum exists for $t_c(n,g_mR)$. According to simulations this minimum occurs at g_mR=3.

It will be shown in section 3.2 that if we reset the initial conditions to 0 before applying V_{lsb} to the inputs, the comparator delay will be fastest when $g_mR=\infty$.

3.2.2 Design Example - A 6-bit Open-Loop Comparator.

In this section, we present the design of a 6-bit comparator and its performance in terms of comparison rate and phase margin. The design with $g_mR=4.5$ and n=6 is considered, although it is not quite optimum, because the gain of an one-one inverter is 4.5.

Figure 3.16 shows the complete schematic of a 6-bit comparator. It consists of six differential pairs with three common-mode feedback loops to control the common-mode voltages of the outputs. Input signal is sampled at the falling edge of ϕ_1 by the input *T/H*. Two D flip-flops then sample the comparator outputs at the falling edge of ϕ_2. The positive and negative supplies are +5v and -5V respectively. For reliability reasons, circuit design has to ensure that no single transistor has more than 5V appearing across its drain and source even when the differential pairs are over-driven at the inputs. Common-mode feedback is used in this design to

1 set up output common-mode voltage under small signal input and

2 limit output voltage swing to 5V under large-signal input.

The simulated dc transfer curve of two differential pairs is given in figure 3.17. It clearly shows that the input-output common-mode voltage is stablized at 2.5V while the large signal output voltage swing is limited to 5.5V. If common-mode feedback is not applied, the output voltage swing could be as large as 7V.

The transient analysis in SPICE is used to verify the accuracy of the results produced by *program A−5*. Figure 3.18 is the SPICE output showing $V_n(t)$, which is close to the results given in figure 3.11. The input is a pulse waveform with a -2V initial condition, a 100ps rise-time and a +31.25mV V_{lsb}. The SPICE simulated worst-case comparator delay is about 1.55ns.

Decision Circuit in Data Transmission System

So far we have only examined the time required for a cascade of open-loop inverters to produce a digital signal ($V_{final}=5V$) at its outputs when its input is driven by a pulse waveform. Let us now consider applying the comparator in figure 3.16 to data transmission systems.

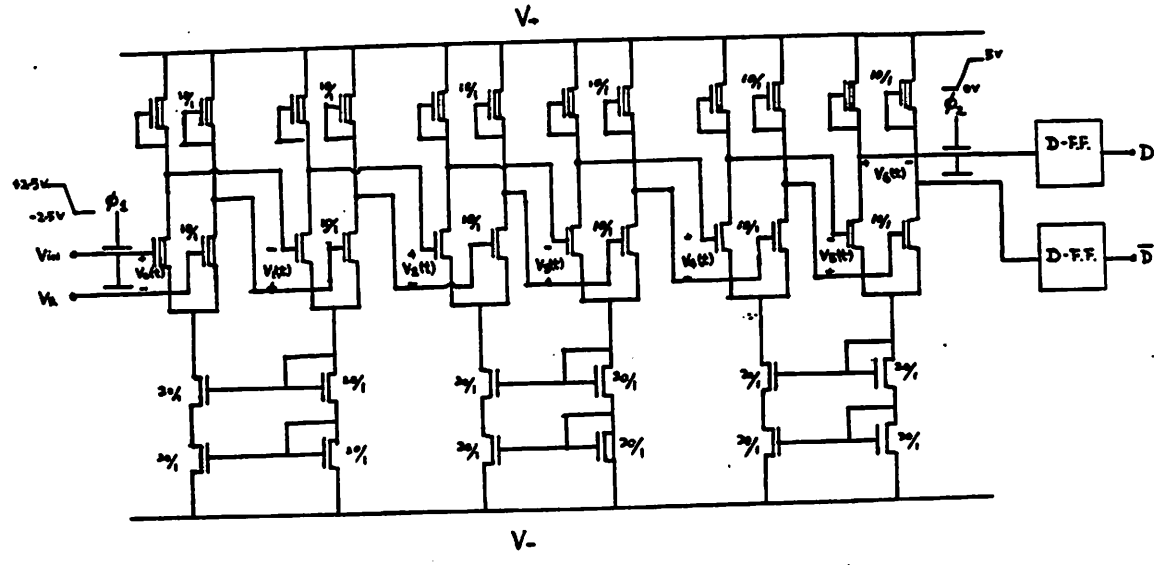


Fig. 3.16 Complete schematic of a 6-bit comparator based on a cascade of open-loop amplifiers.

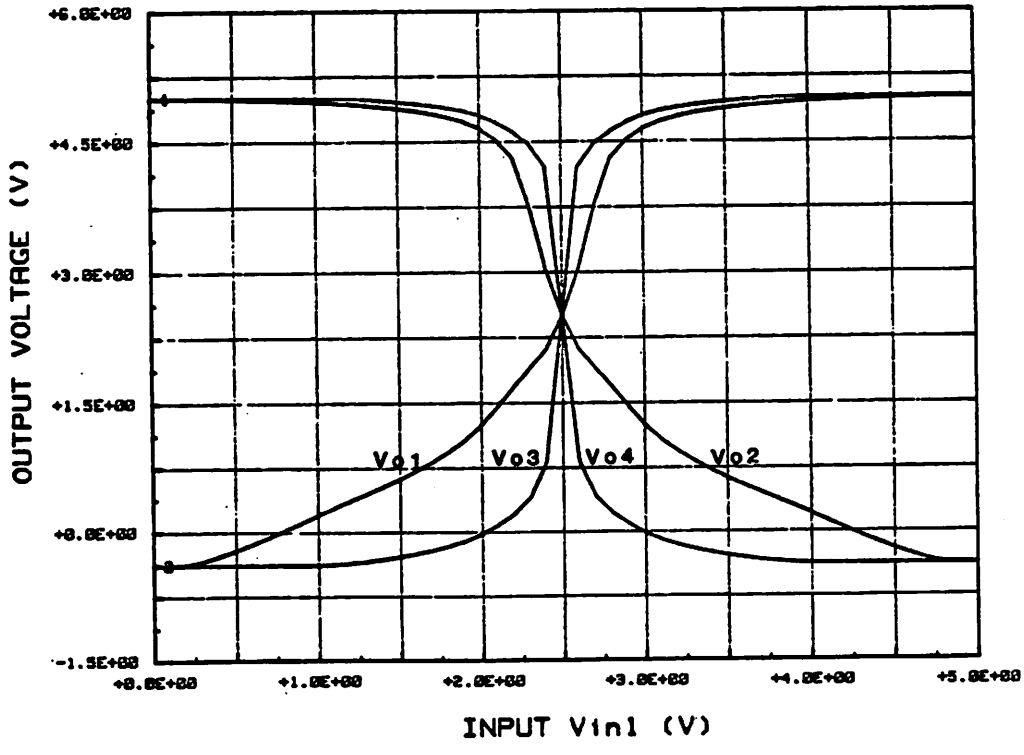


Fig. 3.17 Simulated DC transfer curve of the open-loop amplifier in figure 3.9b.

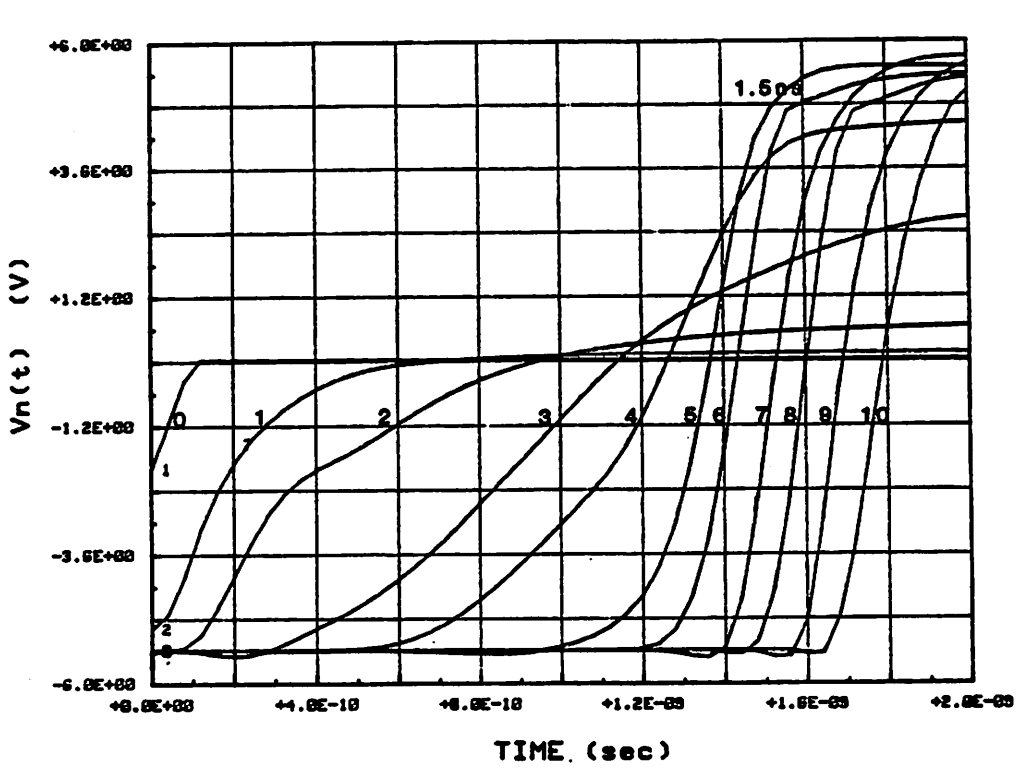


Fig. 3.18 Simulated step response of the comparator in figure 3.16 using SPICE.

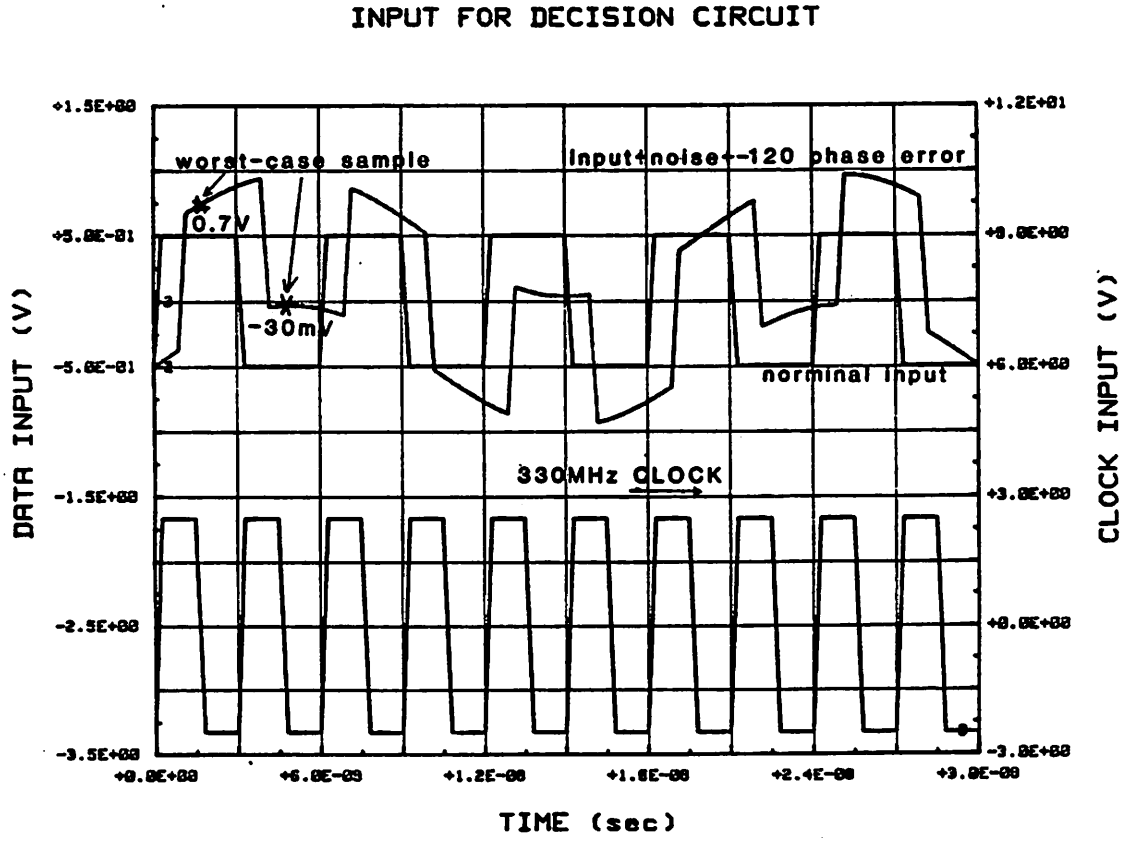


Fig. 3.19 Typical input and clock waveform of a decision circuit.

The function of a decision circuit in data transmission is to decide whether the input is larger than or smaller than a reference voltage, corresponding to the transmission of an 1 or a 0. Figure 3.19 depicts the received data train (0,1,0,1,etc) after amplification and automatic-gain-control with no added noise and no phase error with respect to the clock shown. Usually a low-pass filter is used to remove high-frequency noise from the transmission channel and to reduce intersymbol interference [20]. However, low-frequency noise is always present and a typical input waveform seen by the decision circuit is also shown in figure 3.19. Besides low-frequency noise, a phase error that approaches -120 degree is assumed in figure 3.19. This input waveform represents the most demanding situation for both the input *T/H* and the comparator.

SPICE is used to simulate the transient response of the comparator for the worst-case input. The clock and the input waveform used in the simulation are plotted in figure 3.20a. Here the input resembles the one in figure 3.19 where a minimum overdrive of 31.25mV and a phase error of -120 degree is presumed. Since the clock has 50% duty cycle, the hold time of the *T/H* (t_{hold}) equals $\frac{1}{2f_c}$ where f_c is the sampling rate. For the worst-case input, $t_{hold} \approx t_c + t_{clock}$ in order for the comparator to function properly. t_{clock} is the rise-fall time of the clock. Therefore the maximum sampling rate for this comparator is

$$f_c = \frac{1}{2(t_c + t_{clock})} \tag{3.25}$$

$$= 300MS/s$$

Simulated output voltages $V_n(t)$ are plotted in figure 3.20b. Notice that $V_6(t)$ just barely reaches +5V at the falling edge of ϕ_2 when the input is over driven by $\pm 31mV$.

In the above simulation, we deliberately included an input phase error of -120 degree with respect to the clock to demonstrate the worst-case situation. If there is no phase error in the input, the comparator employs the entire clock period (instead of just t_{hold}) to amplify the input. In that case, the sampling rate is

Fig. 3.20 SPICE simulation of the comparator in figure 3.16.

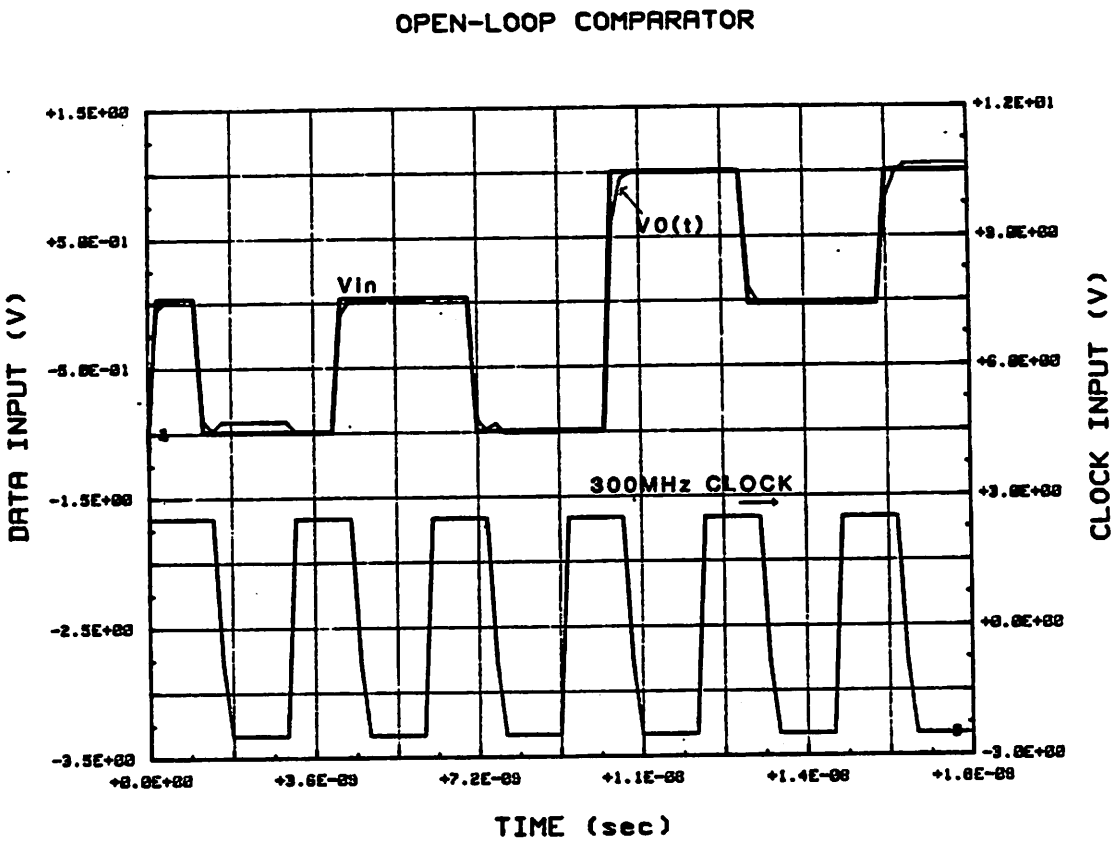


Fig. 3.20a Worst-case input and clock waveform used in the simulation.

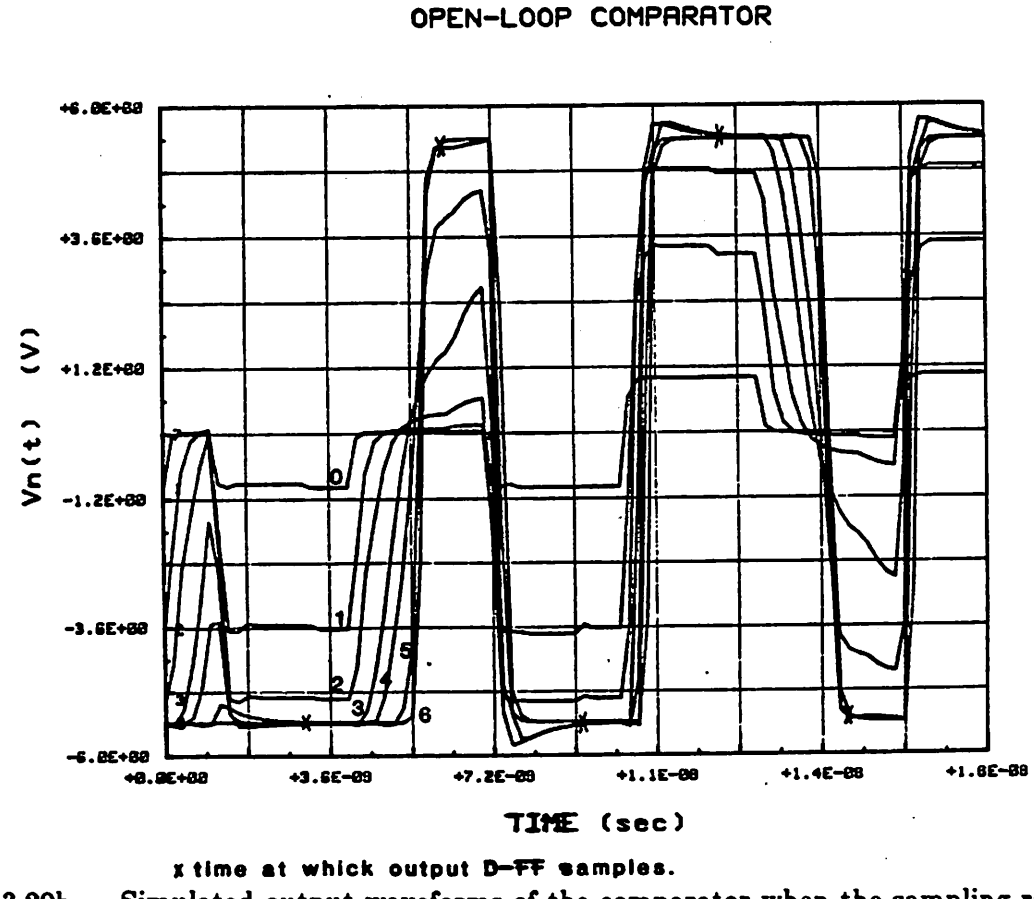


Fig. 3.20b Simulated output waveforms of the comparator when the sampling rate is 300MS/s and the input phase error is -120 degrees.

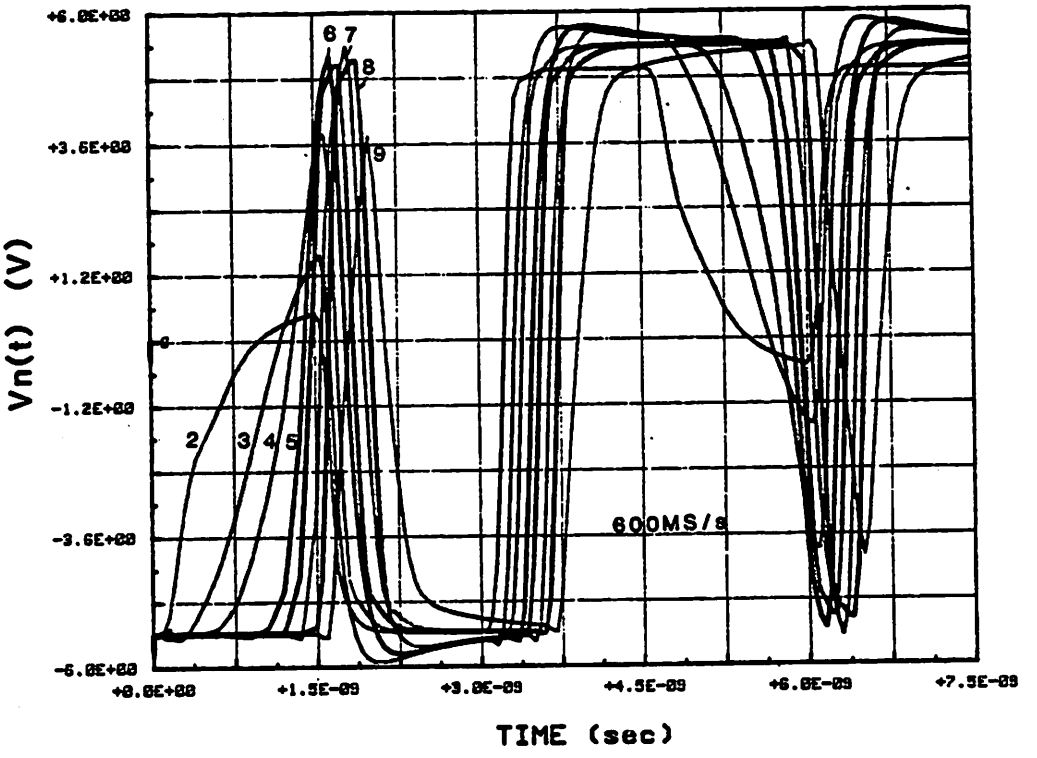


Fig. 3.20c Simulated output waveforms of the comparator when the sampling rate is 600MS/s and the input phase error is 0 degree.

$$f_c = \frac{1}{t_c + t_{clock}}$$

$$= 600MS/s$$

If the comparator is designed for data transmission system, its sampling rate is the parameter to maximize because it limits the data rate of the transmission system. However the comparator delay, which is the time between the sampling instant (falling edge of ϕ_1) and the time when the output reaches V_{final}, is not important to the performance of the transmission system. On the other hand, if this comparator is used in a feedback system such as successive approximation A/D converters, delta-modulation, etc, real-time delays through the comparator becomes the most significant factor. The comparator delay of this design is about 1.5ns.

In this design, we have not accounted for the effects of offset voltages of the differential pairs. If the system requires an offset voltage less than V_{lsb} then this design is only limited to low resolution applications. The input-referred offset voltage is

$$V_{os} = V_{os_s} + \sum_{k=1}^{N} \frac{V_{os_k}}{(g_m R)^{k-1}} \tag{3.26}$$

where V_{os_s} is the offset voltage due to mismatches in the input *T/H* as given by equation 3.13 and V_{os_k} is the offset voltage of the kth differential pair. Since the offset voltage of a MOS differential pair is about 15mV, this design would not perform well in high resolution applications, i.e. $B>6$. Offset cancellation and self-calibration techniques can be used to reduce the effect of offset voltages. Self-calibration is preferred over offset cancellation in high-frequency applications since the latter usually slows down the comparator acquisition time. This chapter does not discuss the different self-calibration schemes and assumes that the input reference voltage V_{ref} can be adjusted to include the effective offset voltage.

3.3 Comparator II - Cascade of Open Loop Amplifiers with Reset

In section 3.2, we have investigated the delay of a cascade of open-loop amplifiers. In this case, the comparator delay is dominated by the over-drive recovery time of the cascade because initial conditions on the gate capacitors are not zero. Since a MOS transistor can function like an ideal switch, it can be used to reset the initial conditions to zero before applying the input sample. In this section we show that the comparator delay is improved by employing reset-switches as in either figure 3.21a or b.

Because a voltage switch is not available in bipolar technology, the concept of resetting the amplifiers for improved speed performance has not been used in a bipolar comparator. In MOS technology, switch-reset was proposed by Yee and Terman in 1978 in a single-ended design [21]. Since then, many comparators based on the original design were used in A/D converters [22-25]. Figure 3.21c reproduces the comparator circuit of a 25MHz flash A/D [22]. The single-ended approach of this design has many problems especially in high-speed applications.

1 C_1 and C_2 in figure 3.21c are coupling capacitors. Although these coupling capacitors are not charged and discharged during the comparison cycles, they always introduce a long settling component in the transient response. The corresponding bottom plate capacitors C_{p1} and C_{p2} also increase the capacitive loading at the output nodes. These effects can significantly reduce the speed of the comparator.

2 Charge injection and clock coupling from the reset-switches (q_1 and q_2) can limit the resolution of the comparator. A complicated clocking scheme is necessary to reduce these effects. The clock waveforms shown in figure 3.21c are difficult to generate at high frequencies.

In light of the above problems, a fully differential design in CMOS was proposed by Allstot [26].

No existing literature discusses the design philosophies and the speed trade-off of this type of *open−loop comparator with reset*. For example, the comparators in [23], [24],

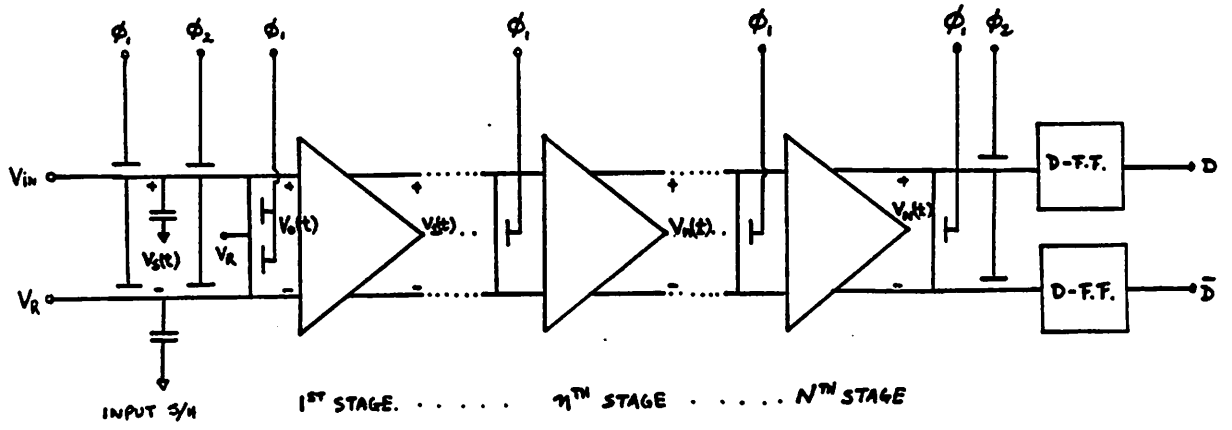


Fig. 3.21a Configuration of Comparator IIa - cascade of open-loop amplifiers with shunt MOS reset-switches.

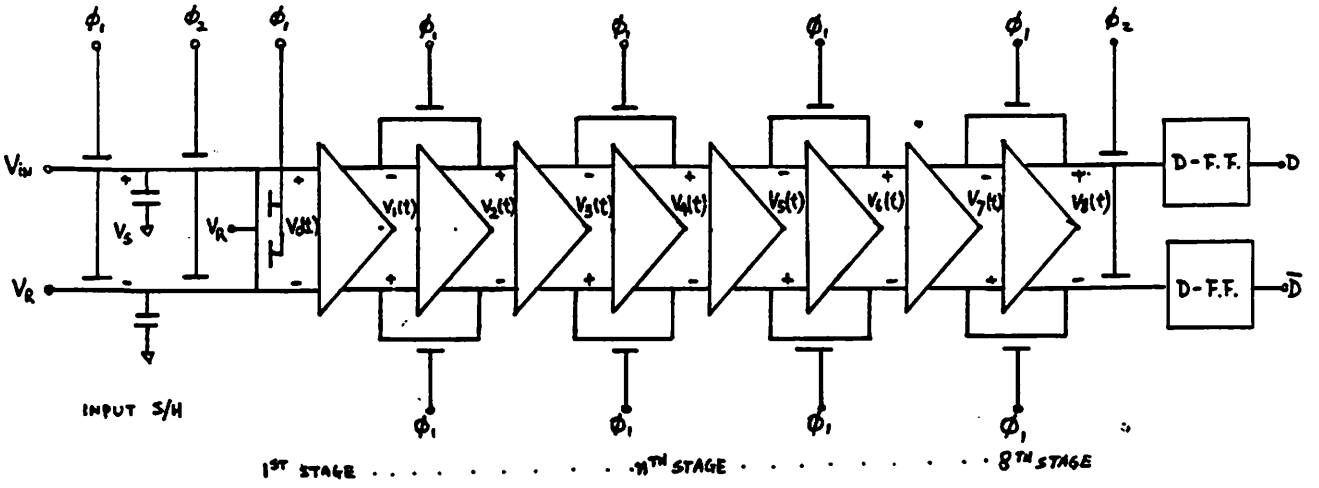


Fig. 3.21b Configuration of Comparator IIb - cascade of open-loop amplifiers with feedback MOS reset-switches.

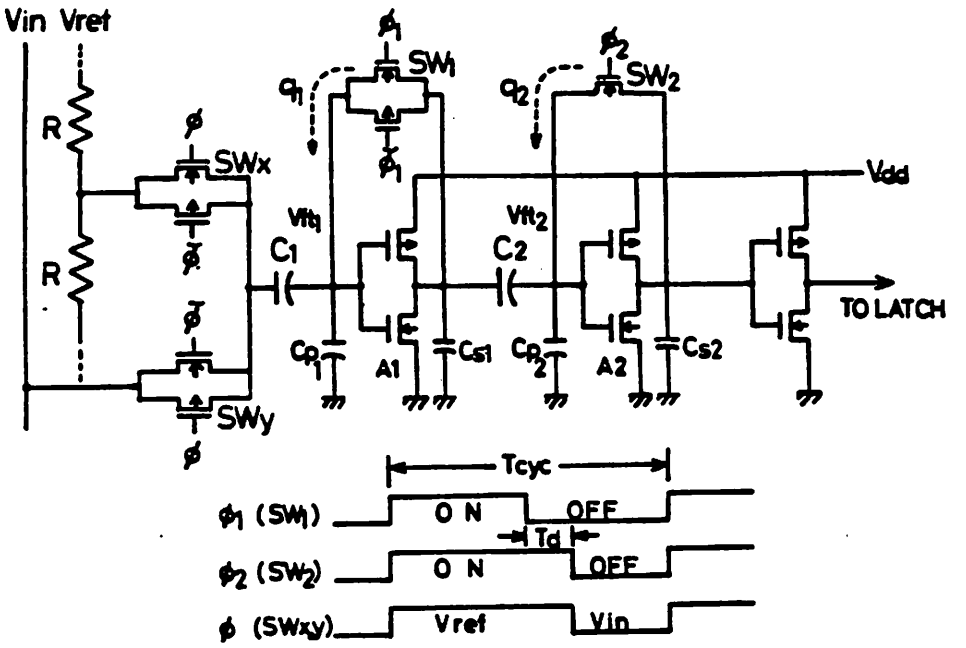


FIGURE 1—Offset-reduced CMOS sample-and-hold comparator. Feedthrough voltage V_{ft1}, if small, can be absorbed in capacitor C2 during the Td period.

Fig. 3.21c The single-ended comparator of a 25MS/s flash A/D.

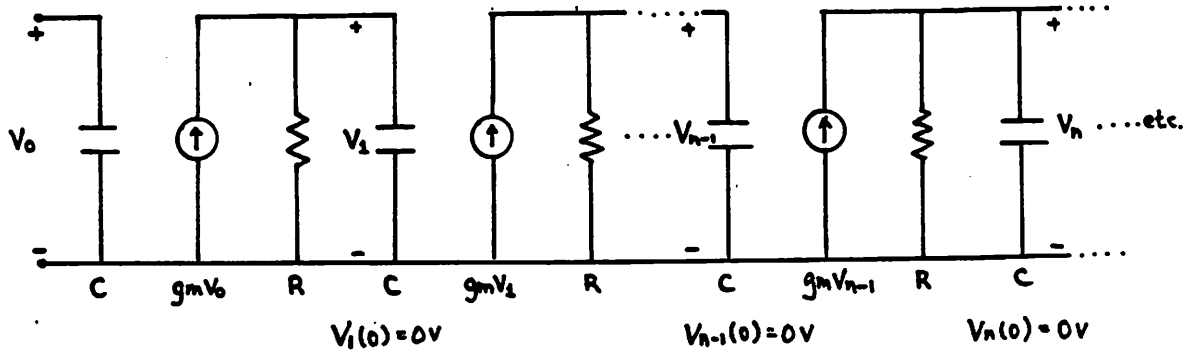


Fig. 3.22 Small signal equivalent circuit of figure 3.21a and 3.21b when ϕ_1 is low.

[21], [25] and [26] have one, two, three, four, and five gain stages respectively. In section 3.3.1, a generalized transient analysis is performed on the circuit in figure 3.22. From this analysis, we can determine the optimum number-of-stage N and the optimum gain-per-stage g_mR for a particular application with B bits of input resolution. Two 6-bit comparator based on the configurations in figure 3.21a and b are presented in section 3.3.2.

3.3.1 Transient Analysis and First Order Theory

When ϕ_1 is low, the differential-mode half-circuits of figure 3.21a and b are identical as given in figure 3.22. Although this equivalent circuit is similar to the one in section 3.2.1 (figure 3.10), the analysis differs in that the initial conditions are now zero. *Program A−5* can still be used with $V_n(0)=0$ to simulate the zero-state response of the chain of amplifiers to an input step function.

To verify the accuracy of *program A−5*, transient simulation for an input step of 31.25mV (B=6 bits) is performed using both SPICE and *program A−5*, and the outputs are compared in figure 3.23. In figure 3.23, $V_n(0)=0$, $g_mR=4.5$, $V_{lsb}=31.25mV$ and $V_{final}=5V$. The two output waveforms are virtually identical for $n=<8$, but they deviate for $n>8$. This is because the effects of saturation and Miller multiplication are not carefully modeled in *program A−5*. As in section 3.2.1, we can used *program A−5* to solve for $t_c(n)$ with various combinations of B and g_mR, and quickly converge to the optimum design in terms of the number-of-stages and the gain-per-stage. Before doing this, some theoretical considerations may give some insight to the problem.

Linear Circuit Theory

In contrast to the problem in section 3.2.1, the initial conditions are now zero; therefore the circuit can be assumed linear as long as the transistors do not enter the triode region. Laplace transforms can be used to generate closed form solutions for $V_n(t)$ if the input is a step function. In figure 3.22 the transfer function per stage is

$$\frac{V_n}{V_{n-1}}(s) = \frac{g_m}{C}\left(\frac{1}{s+\frac{1}{RC}}\right) \tag{3.27}$$

where C is the total capacitive load at the output and R is the output resistance. For n stages, the overall transfer function is

$$\frac{V_n}{V_0}(s) = \frac{1}{\tau_T{}^n}\left(\frac{1}{s+a}\right)^n \tag{3.28}$$

In equation 3.28, $\tau_T=\frac{C}{g_m}$ and $a=\frac{1}{RC}$. Since Laplace transform of an input step is

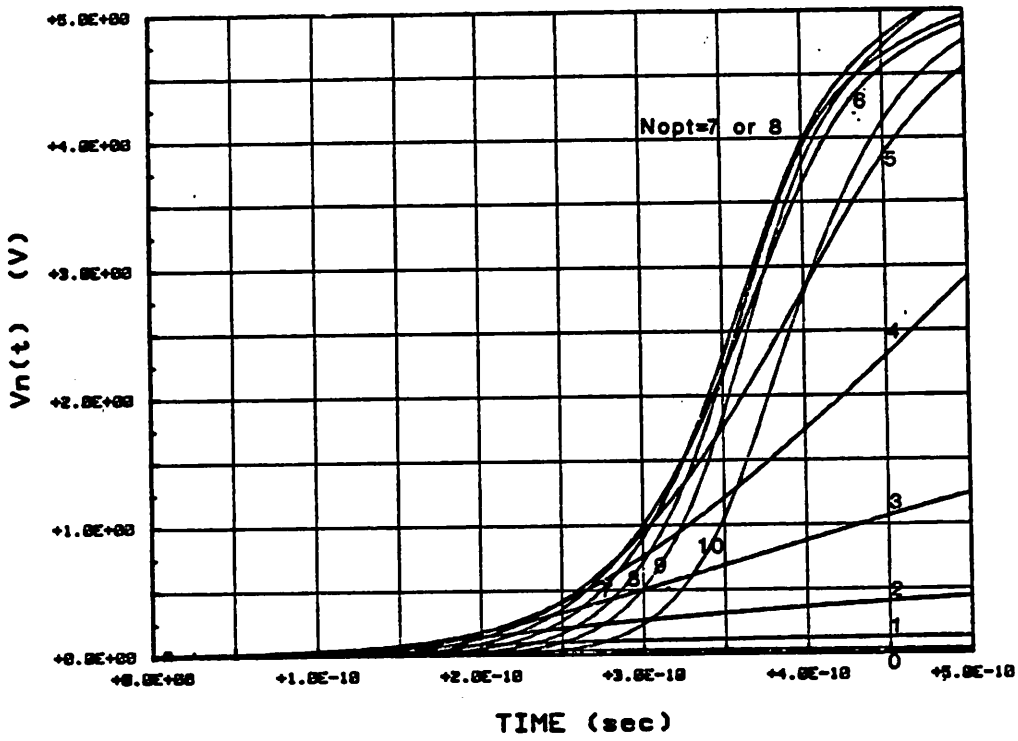


Fig. 3.23a Simulated step response of a cascade of open-loop amplifiers with reset (no initial conditions) using SPICE with $V_{lsb}=31mV$.

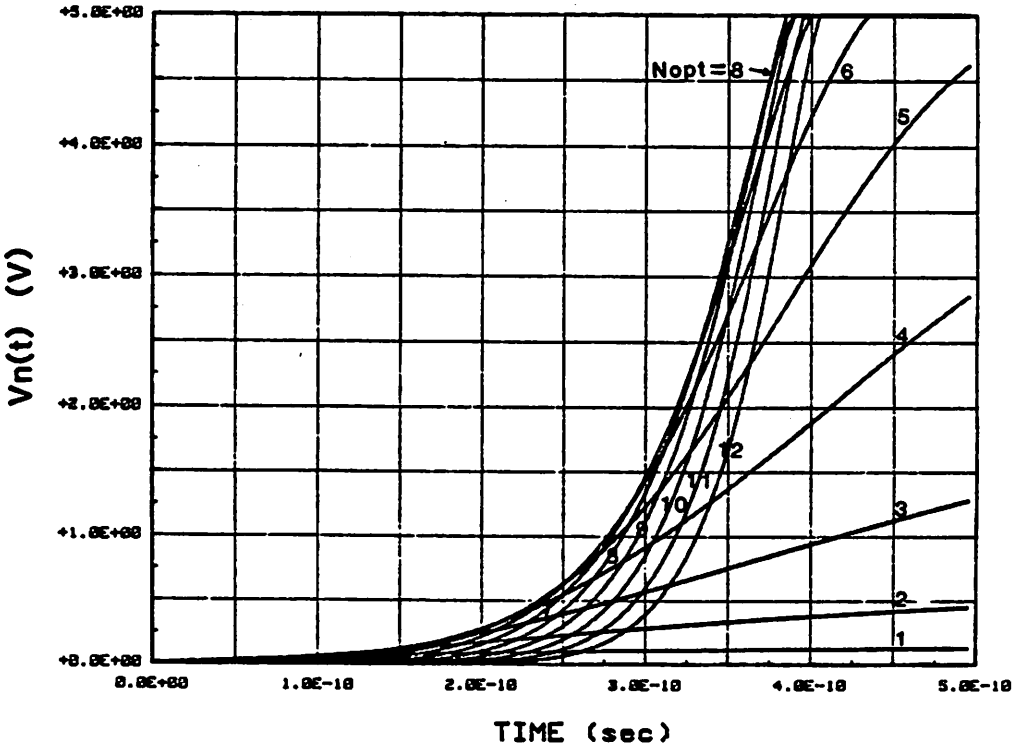


Fig. 3.23b Simulated step response of a cascade of open-loop amplifiers with reset (no initial conditions) using *program* $A-5$ with $g_m R=4.5$ and B=6.

$$V_0(s) = \frac{V_{lsb}}{s} \tag{3.29}$$

the output waveform in the time domain is

$$V_n(t) = \frac{V_{lsb}}{\tau_T{}^n} L^{-1}\left[\frac{1}{s(s+a)^n}\right] \tag{3.30}$$

$$= \frac{V_{lsb}}{\tau_T{}^n} L^{-1}\left[\frac{1}{s}\right] * L^{-1}\left[\frac{1}{(s+a)^n}\right],$$

where the symbol L^{-1} represents inverse Laplace transform and * represents convolution in time. From standard transform tables,

$$V_n(t) = \frac{V_{lsb}}{\tau_T{}^n (n-1)!} \int_0^t t'^{n-1} e^{-at'} dt'$$

Evaluating the integral using integration-by-parts

$$V_n(t) = V_{lsb}(g_m R)^n \left[1 - e^{\frac{-t}{\tau_T g_m R}} \left(\sum_{k=0}^{n-1} \frac{1}{k!} \left(\frac{t}{\tau_T g_m R}\right)^k\right)\right] \tag{3.31}$$

Equation 3.31 is plotted in figure 3.24 for n ranging from 1 to 10, $g_m R = 4.5$, $V_{lsb} = 31.25mV$ and $\tau_T = 43.6ps$. $V_8(t)$ reaches 5V in 380ps ($\frac{t}{\tau_T} = 8.75$). This result agrees with SPICE simulated results and results generated from *program A−5* in figure 3.23.

The time for the output to reach 5V is shortened if all initial conditions are reset to zero. Since the algebraic inverse does not exist in equation 3.31, we cannot solve for t_c directly by setting $V_n(t_c) = 5V$. A computer is used to solve for $t_c(n)$ from equation 3.31 numerically and the results are plotted in figure 3.25a. The comparator resolution B is related to V_{lsb} through equation 3.19. In figure 3.25a, $t_c(n)$ is plotted for B ranging from 1 to 16 and for $g_m R = 4.5$. The program detects any local minimum in $t_c(n)$ and prints the value of B at the location of the local minimum. For 6 bits of resolution, the optimum design is 8 stages which gives a comparator delay at 380ps. Figure 3.25b gives the exact information as in figure 2.25a except that the results were generated using *program A−5* with $g_m R = 4.5$ and $V_n(0) = 0V$. The difference between the two sets of curves are caused

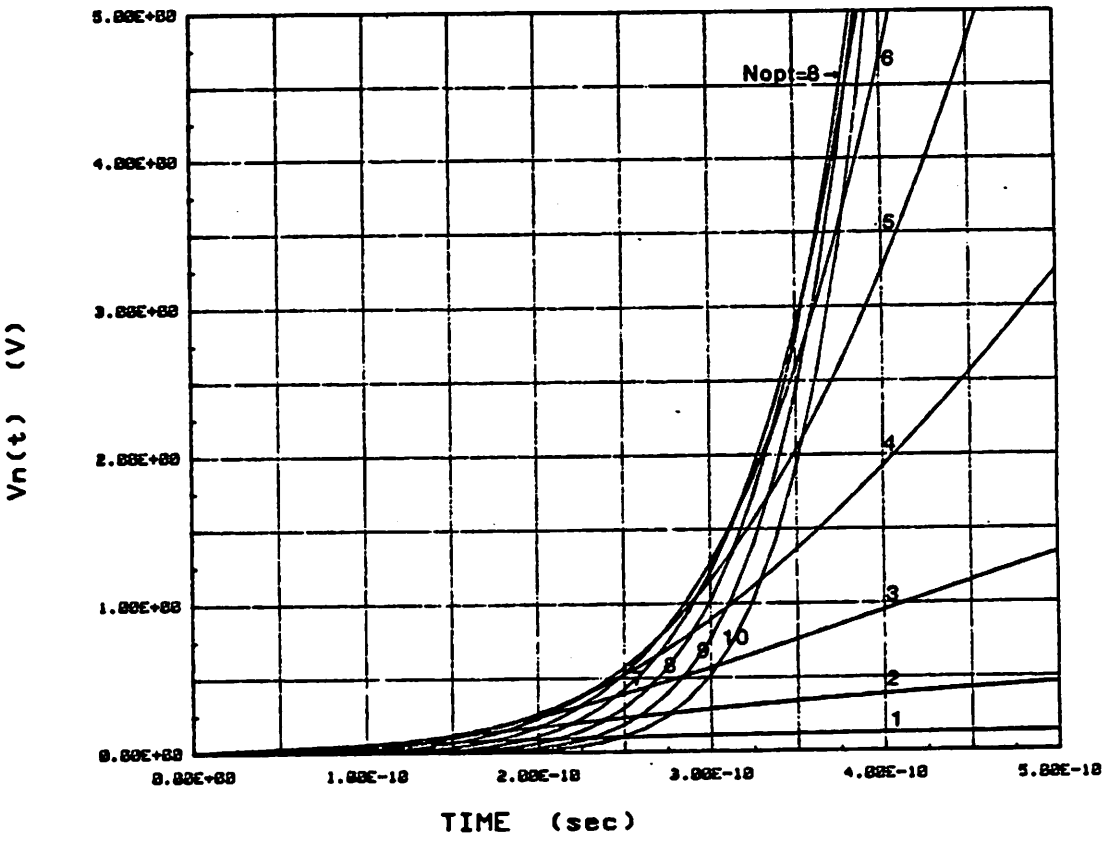


Fig. 3.24 Calculated step response of a cascade of open-loop amplifiers with reset using equation 3.31 where $g_m R = 4.5$, $V_{lsb} = 31mV$ and $\tau_T = 43.6ps$.

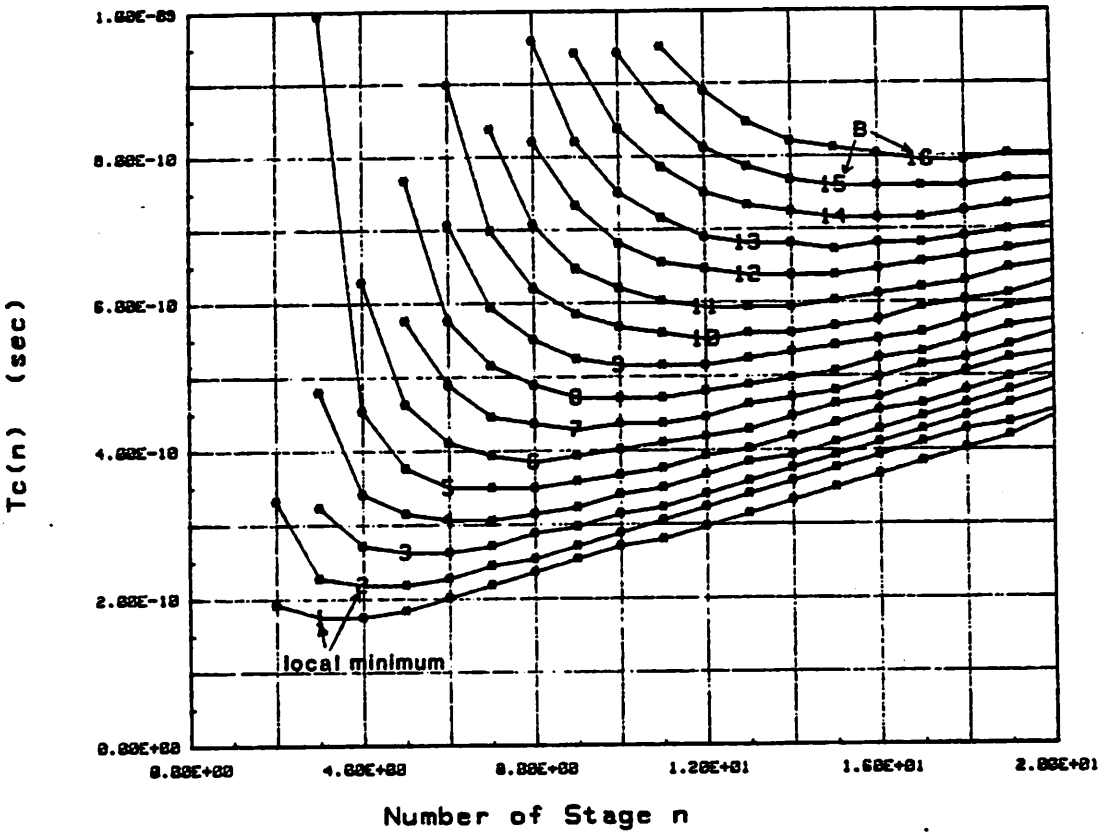


Fig. 3.25a Calculated comparison time t_c of Comparator II versus n and B using equation 3.31 where $g_m R = 4.5$ and $\tau_T = 43.6ps$.

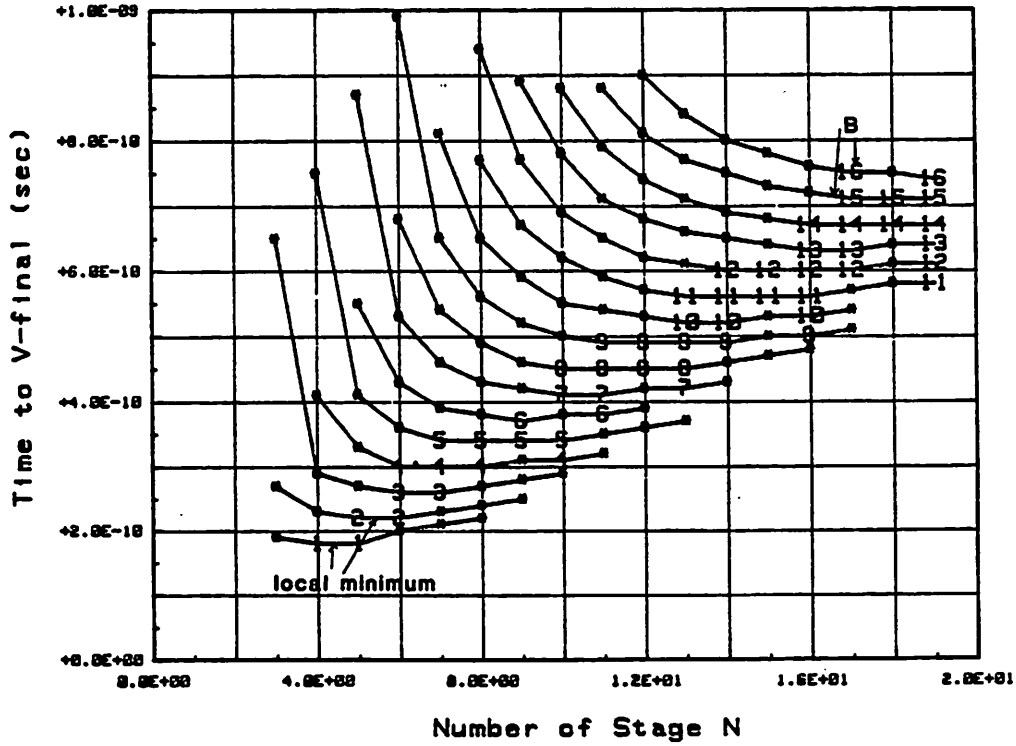


Fig. 3.25b Simulated comparison time t_c of Comparator II versus n ans B using *program A−5* with $g_m R = 4.5$ and $\tau_T = 43.6ps$.

by non-linear effects. The effects of non-linear output resistance and transistor saturation due to finite power supply voltages are briefly modeled in *program A−5*, whereas only linear elements are assumed by equation 3.3.1. Notice that the shape of the two sets of curves and the locations of the minima are close to each other, this shows that non-linear effects are secondary in this analysis. Since g_mR is determined by the intrinsic gain of the transistors and cannot be changed easily, figure 3.25 gives a general view of the delay performance of this type of comparator.

The obvious question to ask next is what is the optimum gain-per-stage or g_mR to give minimum comparator delay? This can be answered physically by referring to the equivalent circuit in figure 3.22. If R is infinite, all of the current available from the dependent current source is used to charge the input capacitor of the following stage; thus $t_c(n)$ as a function of g_mR would decrease monotonically as g_mR approaches infinity.

If g_mR is infinite, a closed form solution for $t_c(n)$ does exist. The overall transfer function is

$$\frac{V_n}{V_0}(s) = \frac{1}{\tau_T^n\, s^n} \tag{3.32}$$

Again assuming an input pulse with V_{lsb} pulse height,

$$V_n(t) = \frac{V_{lsb}\, t^n}{\tau_T^n\, n!} \tag{3.33}$$

$t_c(n)$ is defined by

$$V_n(t_c) = V_{final} \tag{3.34}$$

Combining equation 3.33 and 3.34, we have

$$t_c(n) = \tau_T \left(\frac{V_{final}}{V_{lsb}} n! \right)^{\frac{1}{n}} \tag{3.35}$$

Equation 3.33 is plotted in figure 3.26 with V_{lsb}=31.25mV. In figure 3.26, the output of the 6th stage reaches 5V in 308ps. This represents a 20% improvement over the design with g_mR=4.5 and N=8. Equation 3.35 is plotted in figure 3.27a where B is varied from

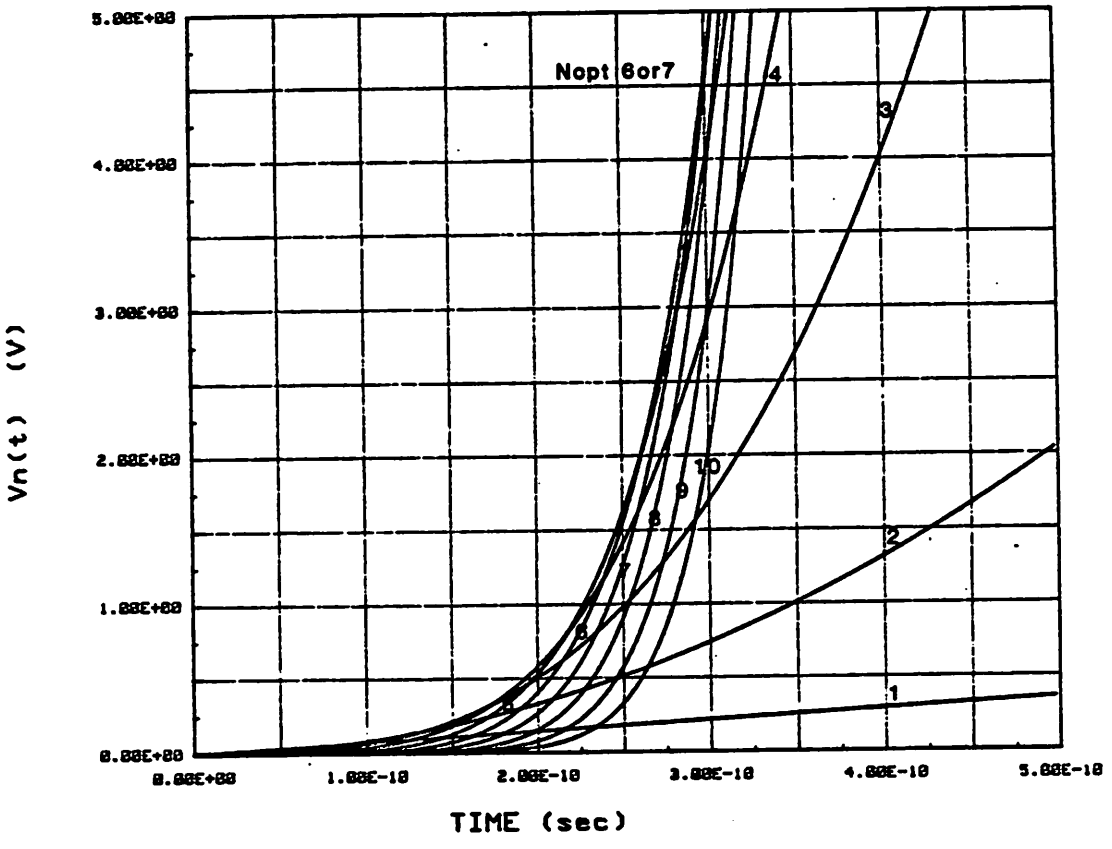


Fig. 3.26 Calculated step response of a cascade of open-loop amplifiers with reset using equation 3.33 where $g_m R$ is assumed ∞.

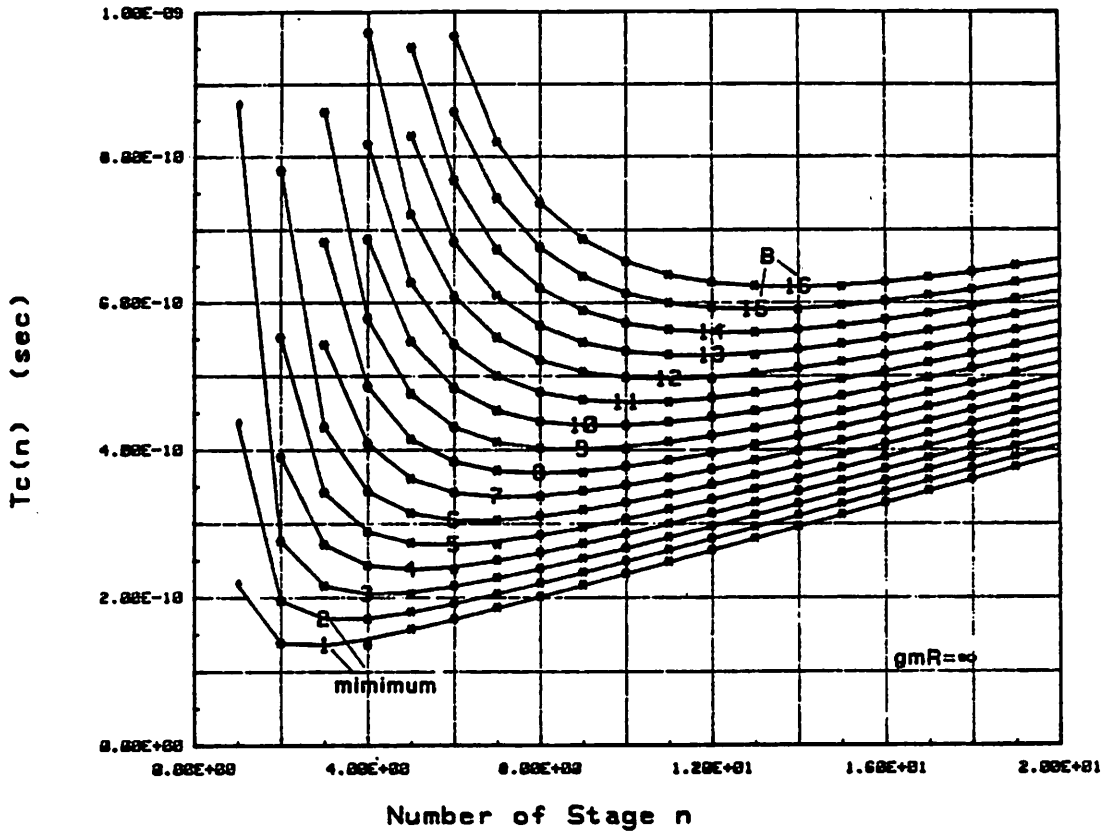


Fig. 3.27a Calculated comparison time t_c of Comparator II versus n and B using equation 3.35 where $V_{final}=5V$.

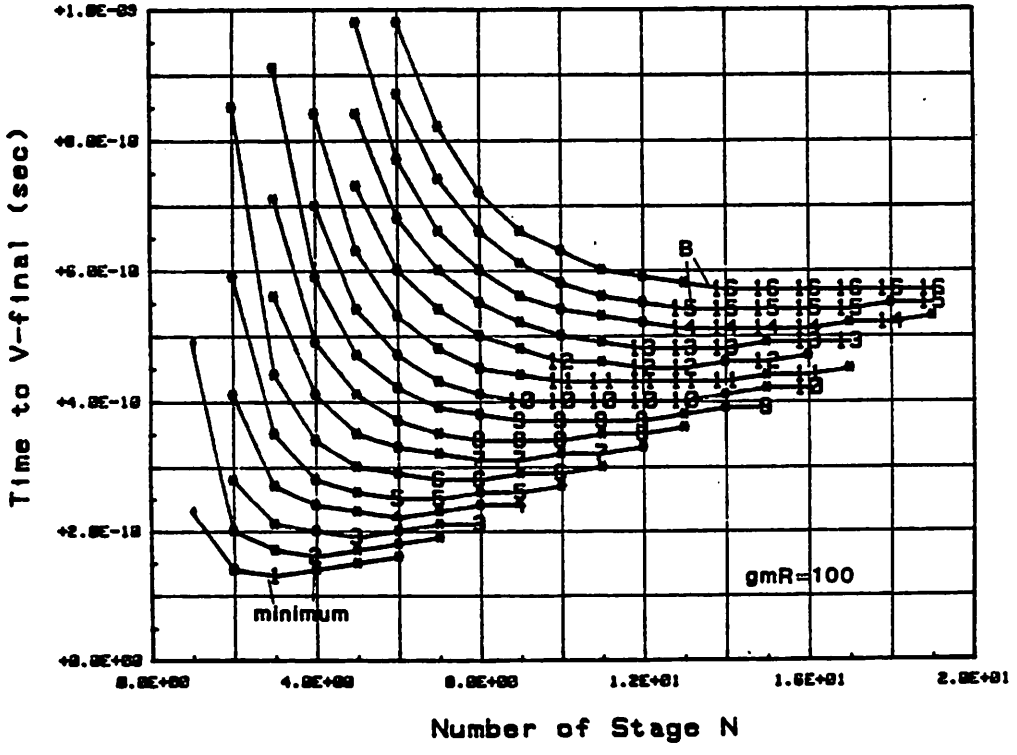


Fig. 3.27b Simulated comparison time t_c of comparator II versus n and B using *program* $A-5$ with $g_m R=100$, $V_n(0)=0$, and $V_{final}=5V$.

1 to 16. Since g_mR is infinite in this calculation, figure 3.27a represents the best-case delay for this type of comparator. For 6-bit resolution, optimum number of stages is 6 and the comparator delay is 308ps. Figure 3.27b presents the same information as in figure 3.27a but the data is obtained from *program A−5* where g_mR is set to 100.

From the above analysis, it is shown that $t_c(n)$ decreases monotonically as g_mR approaches infinity for any value of B. Since we cannot have $g_mR=\infty$ in reality, what is a good value for g_mR such that $t_c(n_{opt})$ is acceptable? This question is answered in figure 3.28 which is generated by *program A−5*. Here, $t_c(n)$ is plotted for various values of g_mR with B equal to 6. For $g_mR=10$, optimum number-of-stage is 6 and $t_c(n_{opt})$ is only 4% slower than that when $g_mR=\infty$. Therefore, a g_mR larger than 10 is as good as a $g_mR=\infty$.

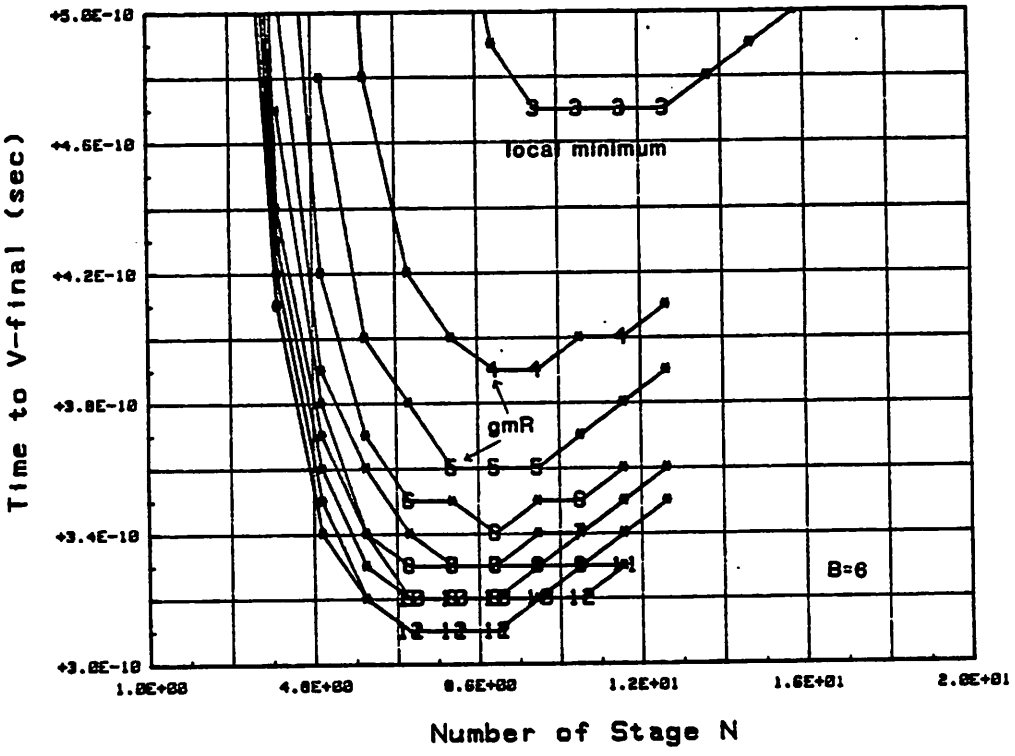


Fig. 3.28 Simulated comparison time t_c of comparator II versus n and $g_m R$ using *program* $A-5$ with B=6 and $V_{final}=5V$.

3.3.2 Design Example - A 6-bit Open-Loop Comparator with Reset

The simulated results in figure 3.23, 3.24, and 3.25 confirm that the optimum number-of-stages for the two comparators in figure 3.21a and b is between 7 and 8, if B=6 and $g_mR=4.5$. The complete schematics of the two comparator designs are shown in figure 3.29a and b. Common-mode feedback is used to stablize the common-mode output voltages. The two designs only differ in how the reset switches are connected. In figure 3.29a, the reset switches short the output nodes of each stage, while in figure 3.29b, the reset switches provide negative feedback between the outputs and the inputs of every other stage. The capacitance added to the signal path because of the reset switches is only about 10% of the total loading capacitance at the output nodes; therefore the $t_c(7)$ is about 420ps (instead of 380ps as calculated in the previous section where ideal MOS switch with no parasitic capacitance was assumed). The maximum comparison rate (assuming a 50% duty-cycle) is

$$f_c \approx \frac{1}{2(t_c+t_{clock})} \tag{3.36}$$

where t_{clock} is the rise-fall time of the clock and is assumed to be 150ps. The maximum comparison rate according to equation 3.36 is 877MS/s.

SPICE has been used to simulate the transient response of the complete circuit shown in figure 3.29a. The clock and the input waveforms are shown in figure 3.30a. The clock rate is 770MHz, and the input assumes the worst-case waveform where the over-drive voltages are -1V, +30mV, +1V, -30mV, +1V and +30mV. The output waveforms $V_n(t)$ in figure 3.30b clearly show that the reset switches function as expected and reset the output voltages to zero in less than 400ps. $V_7(t)$ always reaches $\pm V_{final}$ within the allowed time interval. The input voltage $V_{in}(t)$, the sampled voltage $V_s(t)$, and $V_0(t)$ are plotted in figure 3.30c using an expanded scale. Transistor M_1 to M_6 together with capacitor C_1 and C_2 form the input sample-and-hold. This *S/H* is functionally similar to the one shown in figure 3.2, and it resets the input voltage to zero in every clock cycle. With minor modifications, the design equations derived in section 3.1.1 for the *T/H* can be applied to this *S/H*.

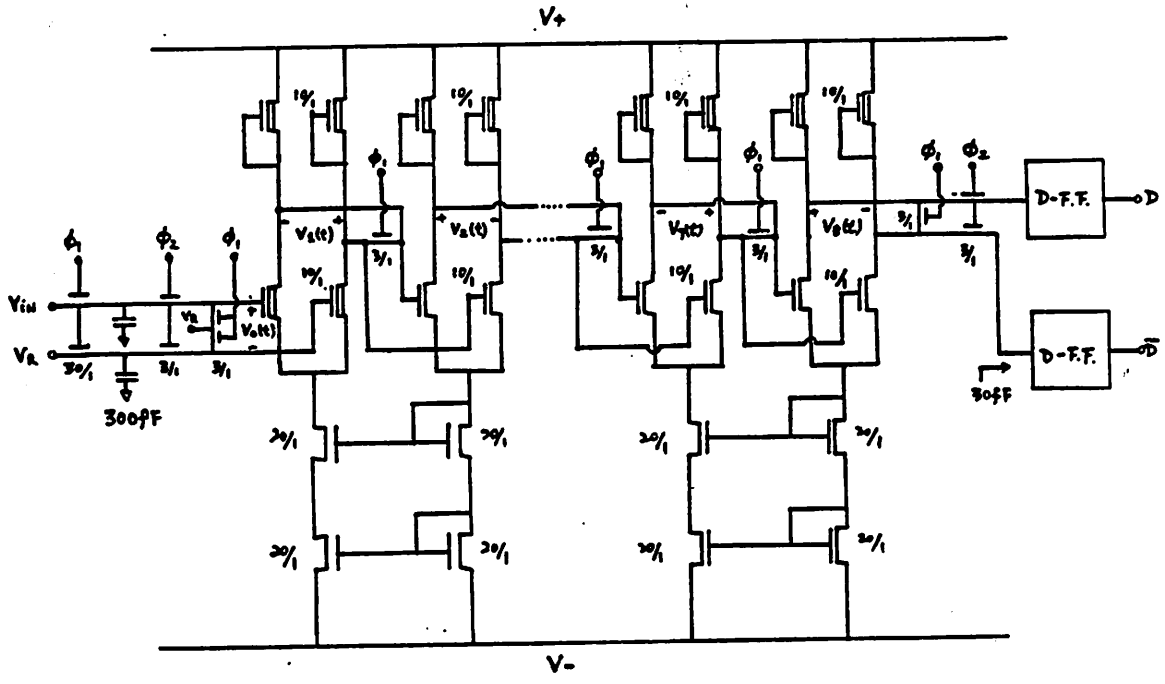


Fig. 3.29a Complete schematic of a 6-bit open-loop comparator with *shunt* MOS reset-switches.

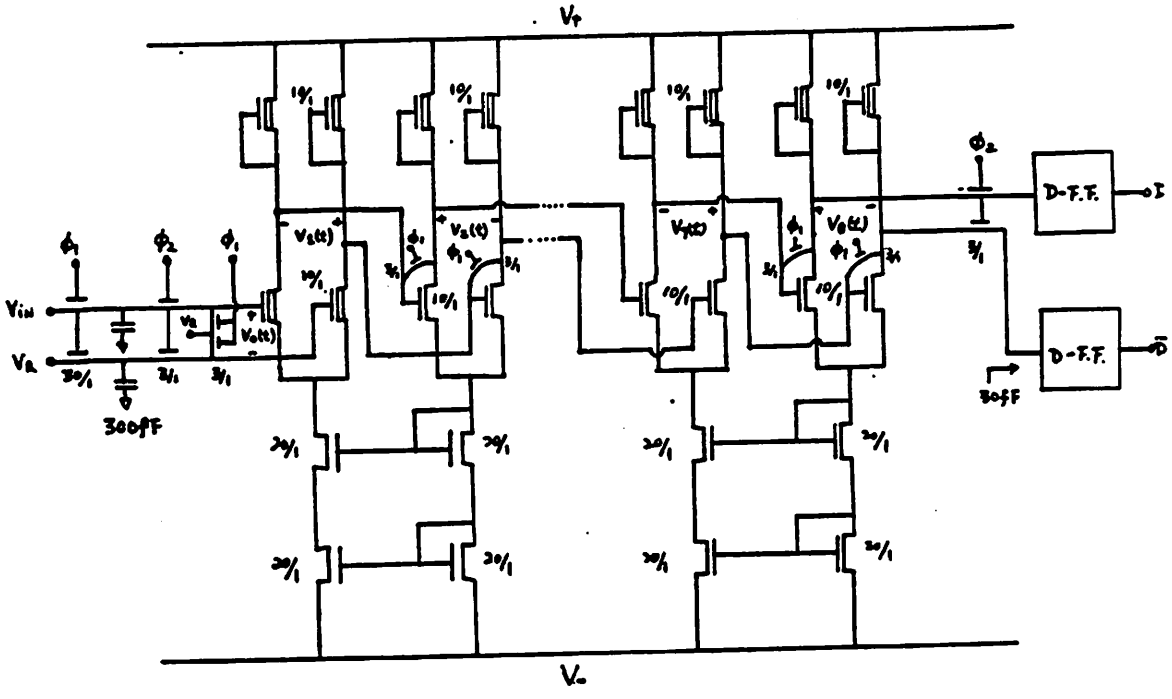


Fig. 3.29b Complete schematic of a 6-bit open-loop comparator with *feedback* MOS reset-switches.

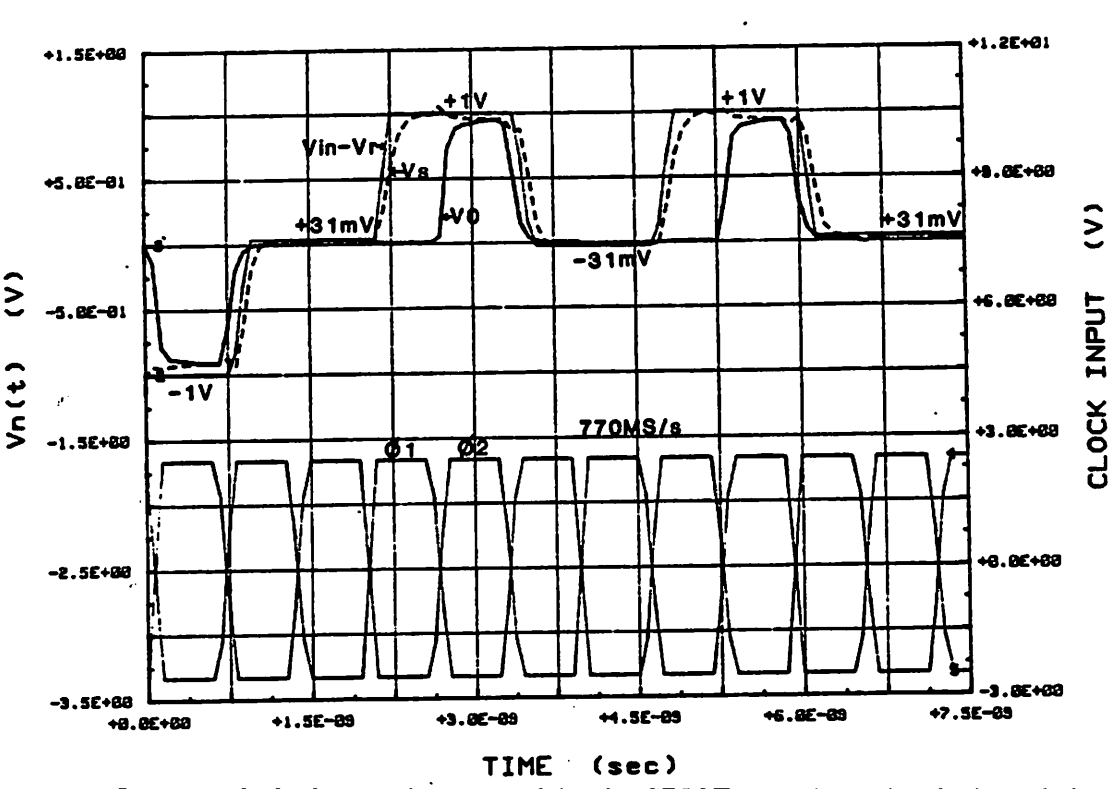


Fig. 3.30a Input and clock waveforms used in the SPICE transient simulation of the comparator in figure 3.29a

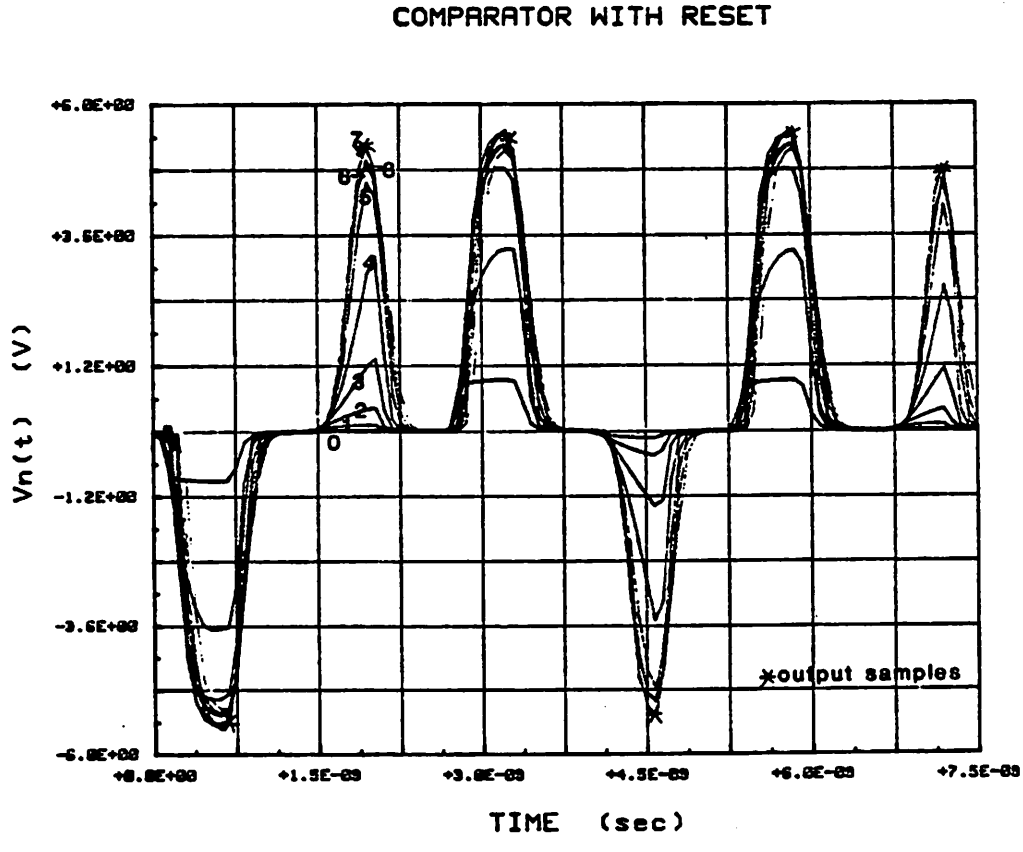


Fig. 3.30b Simulated output waveforms of the circuit in figure 3.29a with all offset voltages equal to zero using SPICE.

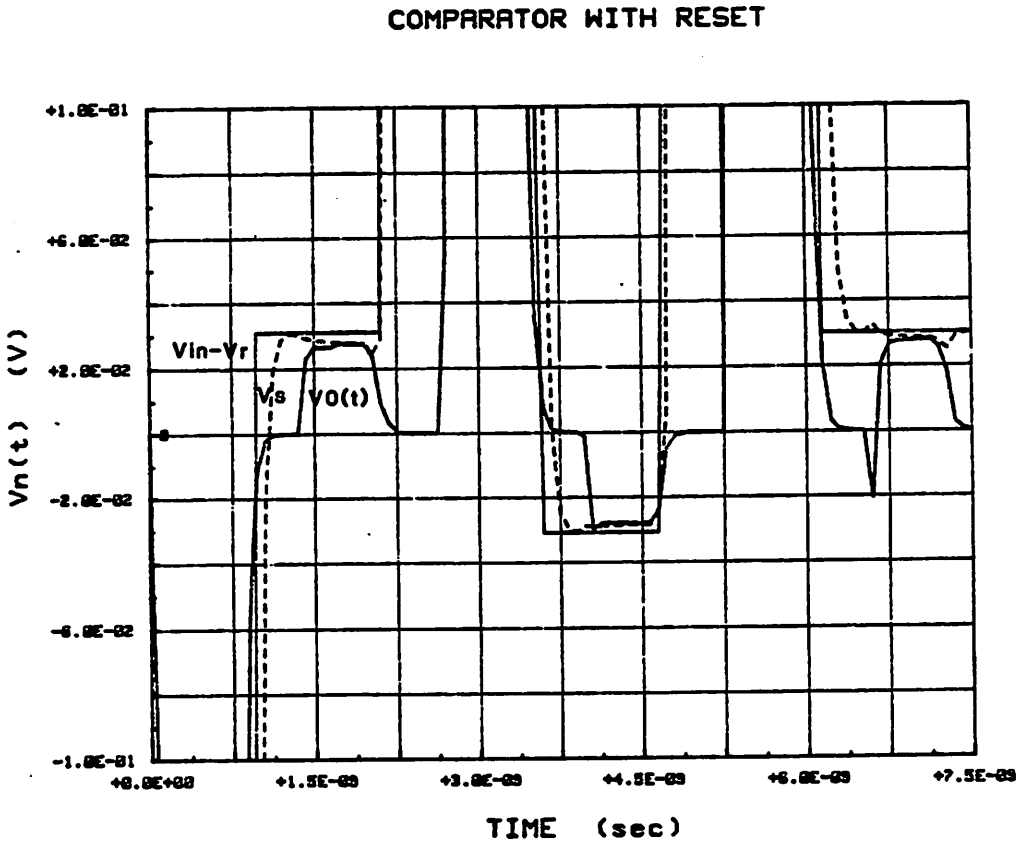


Fig. 3.30c A detail plot of the voltages in the input S/H of figure 3.29a.

Offset Voltage

So far we have not distinguished the difference between the two designs in figure 3.29. In fact the two circuits have identical behavior and their performance is similar as long as we do not consider the effect of offset voltages. The reset times of the two designs are not the limiting factor because the on-resistance of the MOS switches is much smaller than the output resistance of the open-loop differential pairs. It will be shown in this section that the circuit in figure 3.29b is more tolerant to offsets of the differential pairs than the comparator in figure 3.29a.

The equivalent dc input-referred offsets for both circuits are identical and are given by

$$V_{os} = V_{oss} + \sum_{k=1}^{N} \frac{V_{osk}}{(g_m R)^{k-1}} \tag{3.37}$$

where V_{oss} is the offset voltage due to the input *S/H* and V_{osk} is the offset voltage of the kth differential pair. But the transient response or the dynamics of the two circuits are different if input offset voltages are present. In the following simulations the input reference voltage V_{ref} is set to equal V_{os} so that we can concentrate on the dynamic behavior of the two circuits. In reality V_{ref} can be forced to equal V_{os} if self-calibrating techniques are employed in the system design.

In figure 3.29a, the MOS switches reset all output voltages to zero when ϕ_1 is high. As ϕ_2 goes high, the output voltages would initially swing in the direction as imposed by the offset voltages, then the input signal would take over and drive the outputs in the correct direction. A SPICE simulation was performed using the same clock and input waveform as those in figure 3.30a. The effects of offset voltages are modeled by adding voltage sources ($\pm 15mV$) in series with the inputs of the differential pairs. The effect is cumulative if the offset voltages have alternating signs. Figure 3.31a plots the simulated $V_n(t)$. On the fourth sample, the outputs swings to the positive side initially then the input drives the output voltages toward -5V. This effectively increases the delay of the comparator.

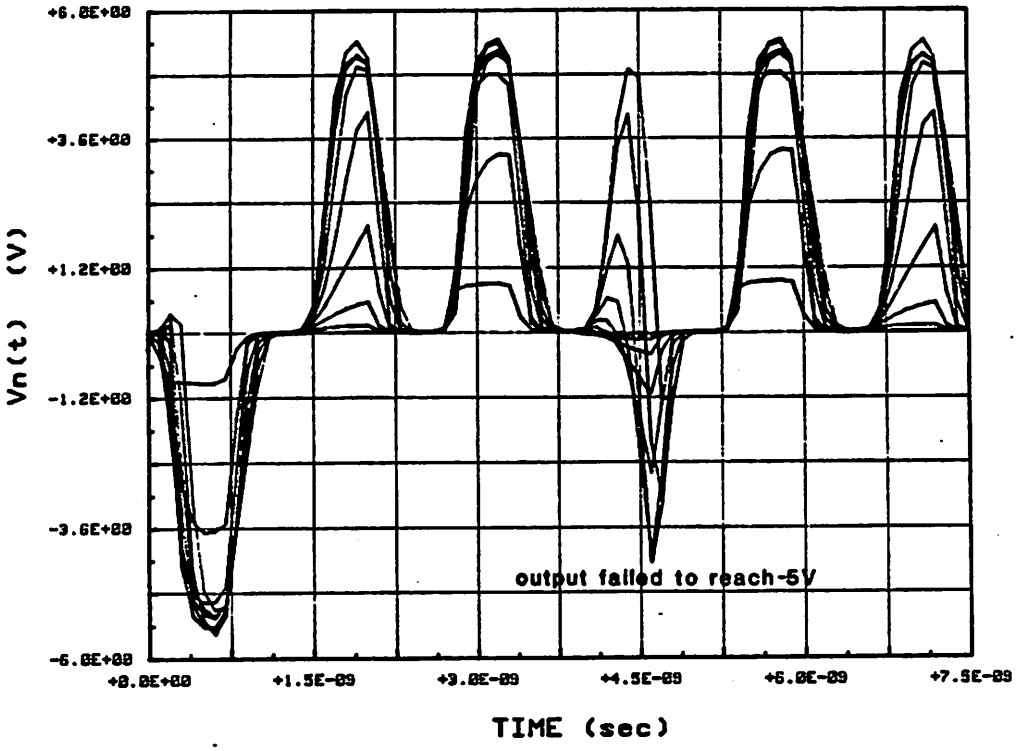


Fig. 3.31a Simulated output waveforms of the circuit in figure 3.29a with offset voltages of alternating sign (+15mV, -15mV, etc.) using SPICE.

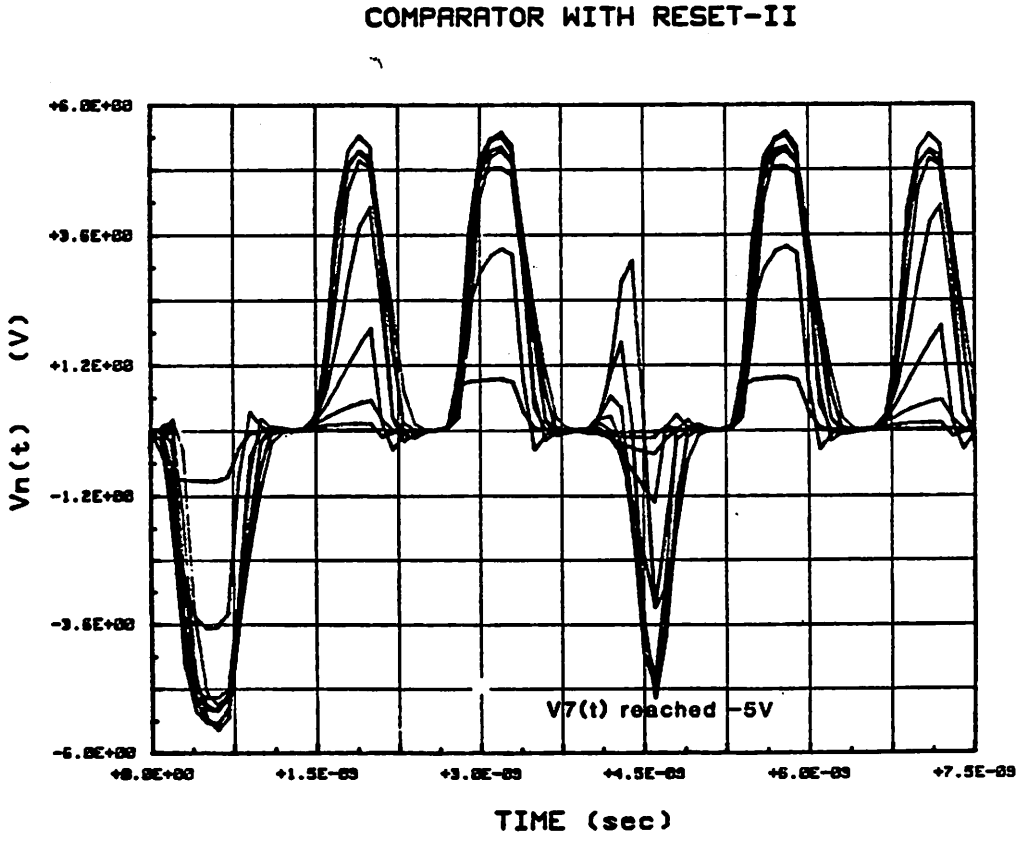


Fig. 3.31b Simulated output waveforms of the circuit in figure 3.29b with offset voltages of alternating sign (+15mV, -15mV, etc.) using SPICE.

In figure 3.29b, the MOS switches reset the node voltages by applying negative feedback around the differential pairs. The offset voltages are embedded in the feedback loops and first order cancellation occurs. This is confirmed by the simulated results shown in figure 3.31b. Comparing figure 3.31b to 3.31a, the effect of offset voltages is less pronounced and the output of the seventh stage $V_7(t)$ reaches -5V within the designated time.

In the above simulations, the offset voltage of the first stage is +15mV, the second stage is -15mV, and so on (with alternating signs). This represents the worst situation because the effect of these offsets on $V_n(t)$ is cumulative. In reality, this situation is unlikely to occur because offset voltage of a differential pair is theoretically a random variable with zero mean. If the mean of the offset voltages is not zero (this can be caused by systematic error such as oxide gradient, etc), then first-order cancellation occurs. Figure 3.31c is the simulated $V_n(t)$ of the comparator in figure 3.29a when all offset voltages are set to +15mV. Notice that the output waveforms of the fourth sample does not swing to the positive direction initially as those in figure 3.31a and b.

In conclusion, using the MOS switches to reset the node voltages on a cascade of differential pairs can reduce the delay of the comparator. The delay t_c of this comparator is about 420ps and the maximum sampling rate is about 880MS/s. However the effect of offset voltage may be important and the effective comparison rate may have to be reduced to 770MS/s.

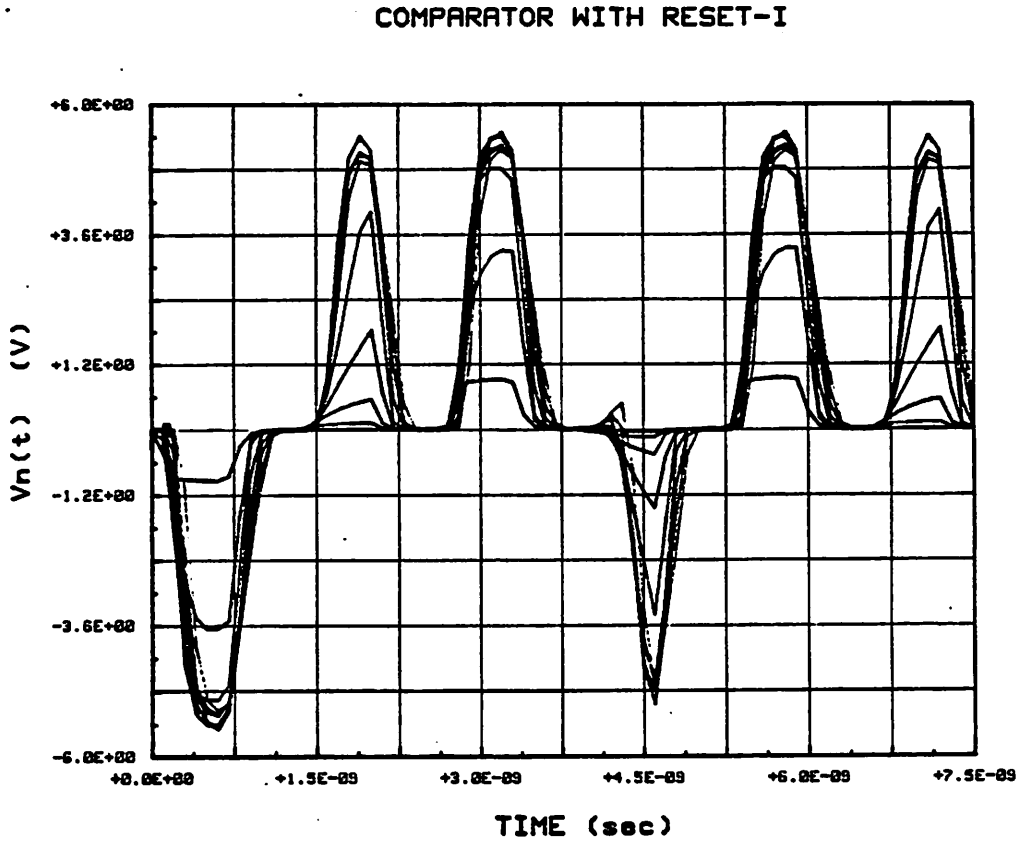


Fig. 3.31c Simulated output waveforms of the circuit in figure 3.29a with offset voltages of the same sign (+15mV) using SPICE.

3.4 Comparator III - Pipeline of Differential Amplifiers

Pipeline processing is commonly used in digital systems to improve the data throughput. Analog circuits can also benefit from this architecture. However, the concept of pipelining in comparator designs was never considered seriously. One reason for this is that the real-time delay through the pipeline is longer than that of conventional approaches. It is shown in this section that the comparison rate of a pipeline comparator is the highest among the designs considered in this chapter. Since real-time delay is not important in data transmission systems, a pipeline comparator can function as the decision circuit in fiber-optic communication. In applications where the delay is important, this approach is not recommended.

Figure 3.32 is the block diagram of a pipeline comparator. The differential amplifier could be any of the three designs in figure 3.33. MOS technology is ideal for implementing such an approach because the MOS *T/H* is both fast and simple. In figure 3.32, the input signal is sampled and amplified by a fixed gain G when ϕ_1 is high, then the amplified sample is passed on to the next stage as ϕ_2 goes high. The sampled signal continues to be amplified as it propagates down the pipeline until the signal is large enough to trigger the D-flip-flop at the end of the chain. The final output voltage is related to the input by

$$V_{final} = V_{lsb}G^N \tag{3.38}$$

Together with equation 3.14, the required number of stages N is

$$N \geq \frac{\log\left[\frac{V_{final}}{V_{fs}}2^B\right]}{\log(G)} \tag{3.39}$$

This shows that for a 6-bit comparator, we need at least 4 stages if G=4, V_{final}=5*V*, and V_{fs}=2*V*. The comparison rate of this type of comparator depends on the settling time of the individual amplifier. In the next section, the simulated settling times of the three amplifiers shown in figure 3.33 are compared. These amplifiers are differential versions of

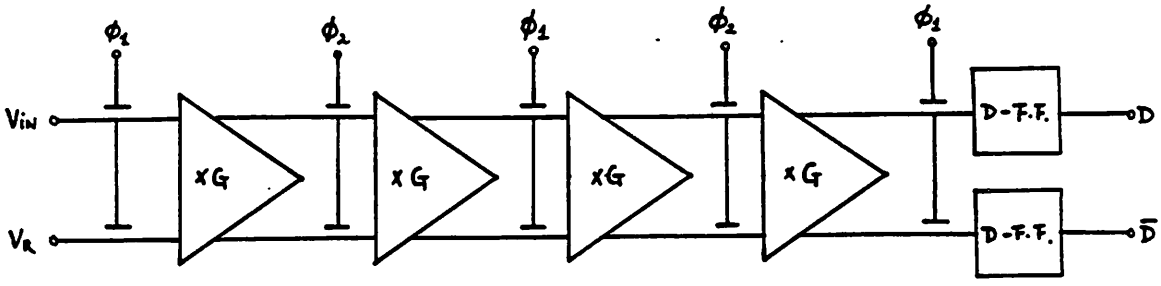


Fig. 3.32 Configuration of Comparator III - Pipeline of differential amplifiers.

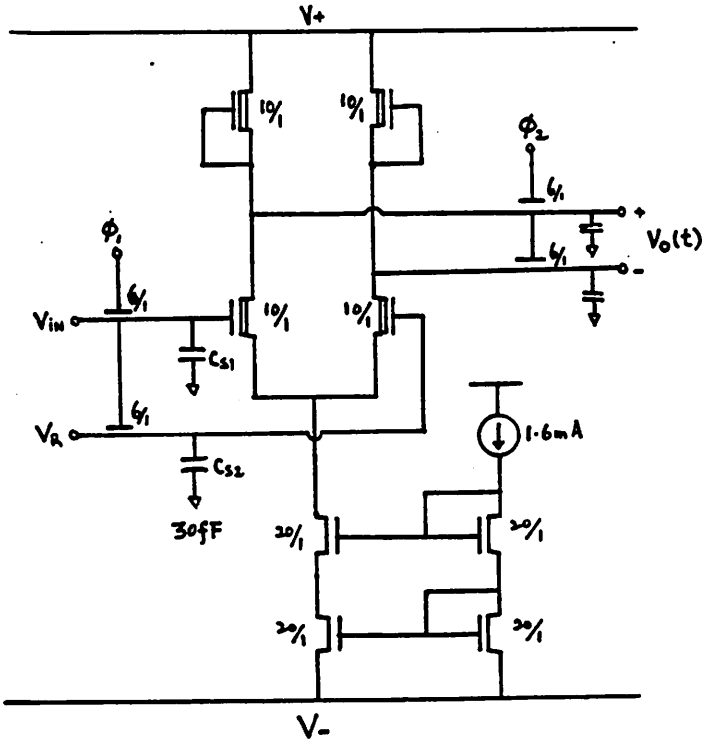


Fig. 3.33a Pipeline of simple differential pairs - OL-amp.

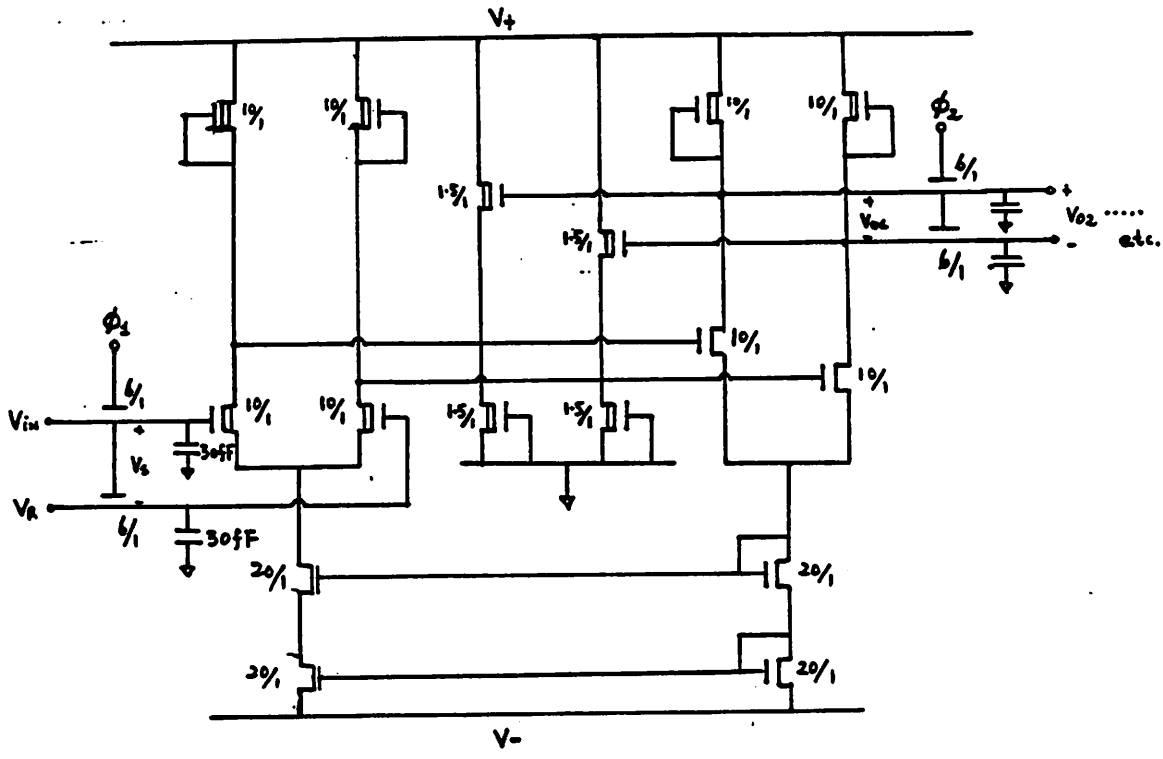


Fig. 3.33b Pipeline of differential Active Shunt Feedback Amplifier - ASF-amp.

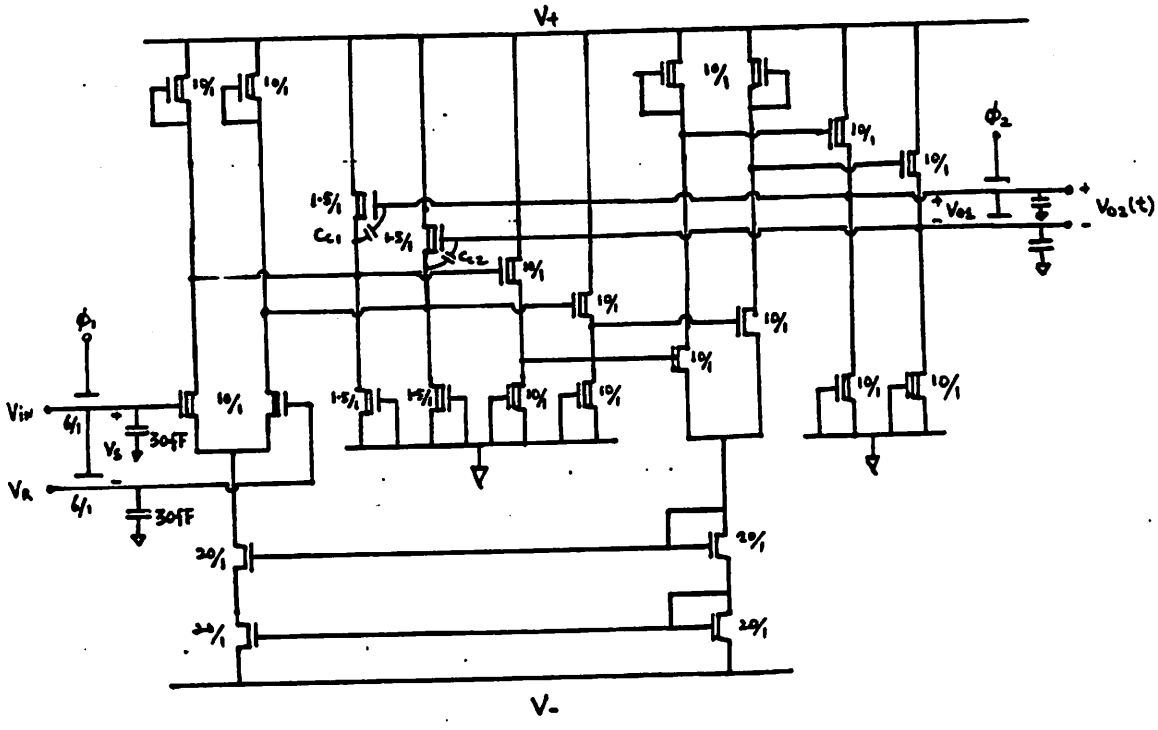


Fig. 3.33c Pipeline of differential Buffered Active Shunt Feedback Amplifier - BASF-amp.

the amplifiers discussed in chapter 2, namely open-loop, active-shunt-feedback and buffered-active-shunt-feedback amplifiers.

3.4.1 Transient Simulations

Simulating the complete response of all the outputs as the signal propagates down the pipeline using SPICE would require too much computer time. An alternate approach is to simulate the response of the first stage, which is the most critical because it is only over-driven by V_{lsb}, and to assume that the following stages have the same settling time as the first stage. To include the delays through the input and the output *T/H* (refer to figure 3.33a) both ϕ_1 and ϕ_2 are turned on. A step input with a 150ps rise-time, a -2V initial voltage and $\pm 31mV$ overdrive is applied at t=0. The settling time is the time for $V_2(t)$ to reach a certain percentage (usually >90%) of the final value.

First, we consider the simple differential pair in figure 3.33a. Transistor M_1, M_2, C_{s1} and C_{s2} form the input *T/H*. C_{s1} and C_{s2} are included to reduce the effect of common-mode charge injection and clock coupling from the two MOS switches (refer to section 3.1.1). The dominant time constant of this circuit is the RC time constant at the output nodes of the differential pair, where R is given by equation 2.1 and C is the total capacitive loading looking into the output nodes. The small-signal bandwidth from the input to the output ($V_1(t)$) is only 400MHz because the added capacitance C_{s1} and C_{s2} equals 30fF. Two simulations were performed for the two cases where the input pulse went from -2V to +31mV and from -2V to -31mV. The simulated step response of the amplifier and the input steps are shown in figure 3.34. In figure 3.34 the output settles to 90% of its final value in 3.3ns. This implies that the sampling rate of the comparator is only 300MHz.

The sampling rate is greatly improved if the amplifier in figure 3.33b is used instead. This amplifier is the differential version of the ASF-amp in section 2.3. DC biasing of the amplifier is controlled by the common-mode feedback loop. Since the output impedance is reduced by the loop gain, the frequency response of this amplifier is less sensitive to capacitive loading at the output, and the small signal bandwidth is greater than 1GHz. Figure 3.35 is the simulated step response of the amplifier. The amplifier settles to the final value in 1.3ns implying a sampling rate of 770MS/s.

Finally, consider the differential amplifier shown in figure 3.33c. Its design is based on the BASF-amp in section 2.3. The added source follower buffers decreases the phase

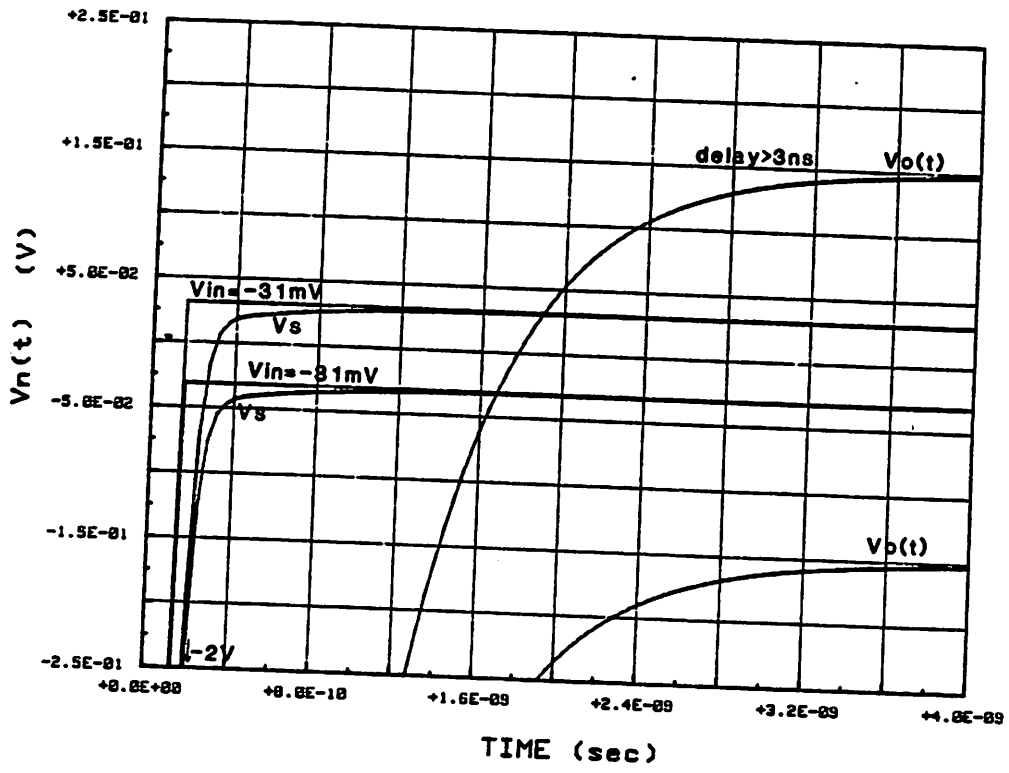


Fig. 3.34 Simulated step response of the simple differential pair in figure 3.33a.

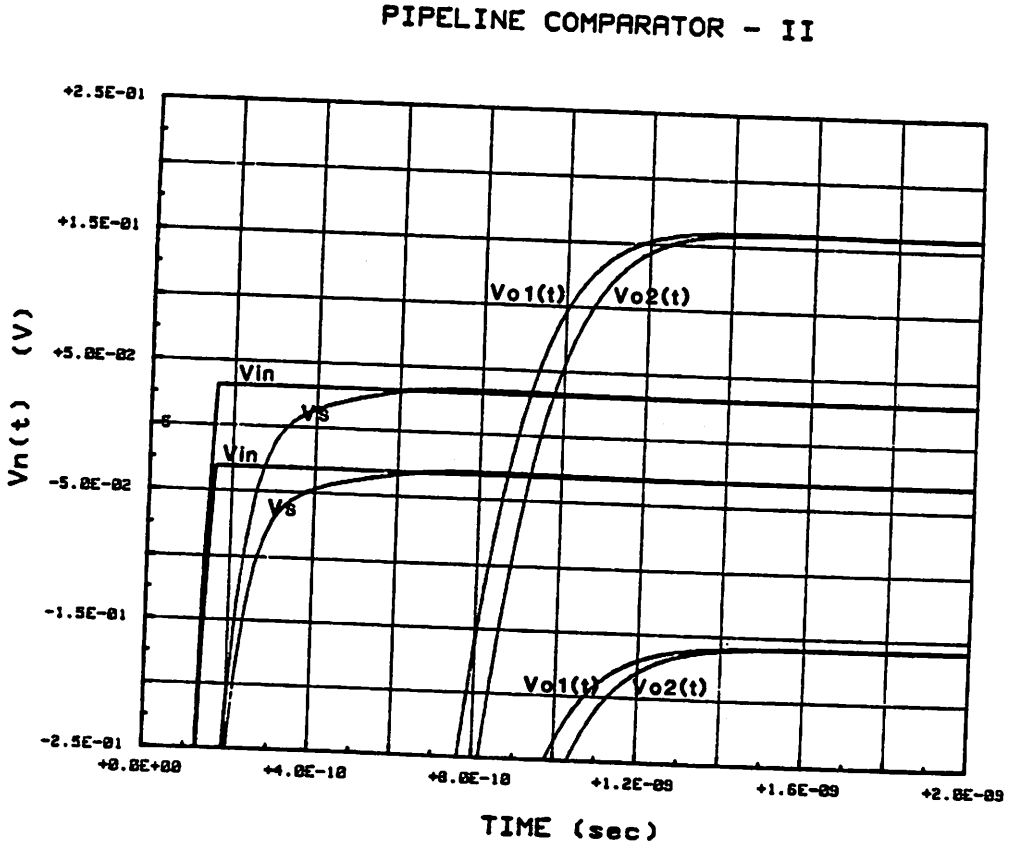


Fig. 3.35 Simulated step response of the ASF-amp in figure 3.33b.

margin of this amplifier and the step response in figure 3.36a shows substantial overshoot (C_c=0). However the ringing settles out in less than 1.3ns. In order to suppress ringing, two 10fF compensation capacitors (C_{c1} and C_{c2}) are included in the simulation of figure 3.36b. Here the overshoot is reduced and the settling time of the stage is 900ps. This implies a maximum comparison rate of 1.1GS/s is possible with this architecture.

If we can control the values of the compensation capacitor, simulation shows that the maximum sampling rate of a pipeline comparator with BASF-amp as the basic amplifier can exceed 1GHz. Four stages are needed in the pipeline to amplify the input signal to 5V, and therefore the comparator delay is 1.8ns. This design achieves high sampling rate in the expense of real-time delay.

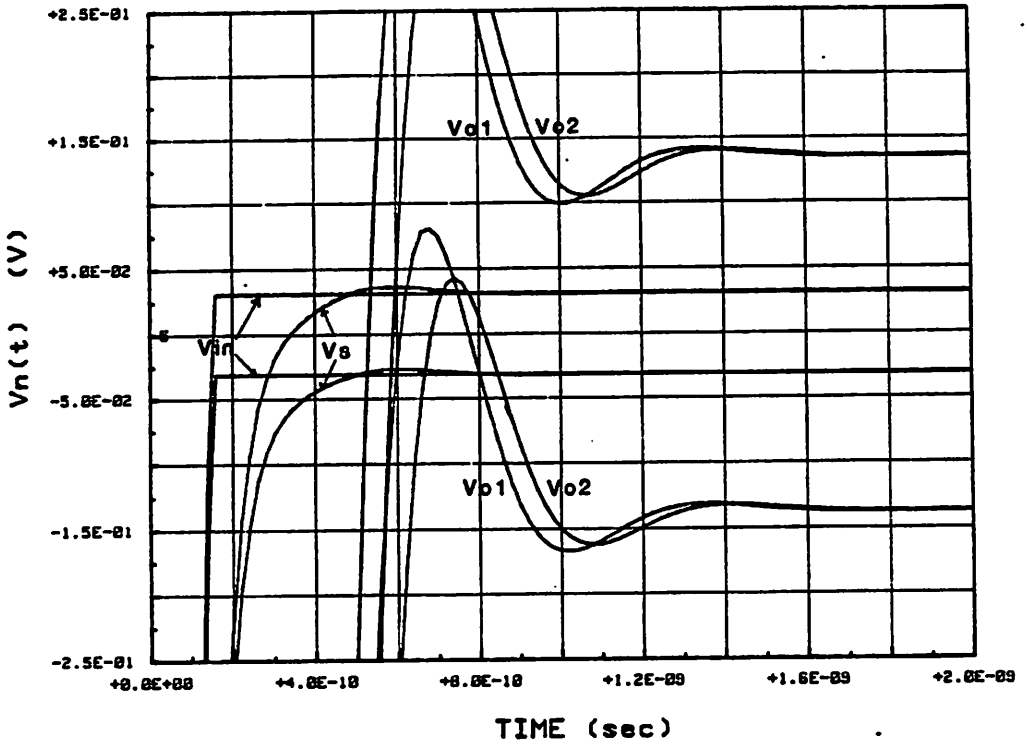


Fig. 3.36a Simulated step response of the BASF-amp in figure 3.33c with $C_c = 0$.

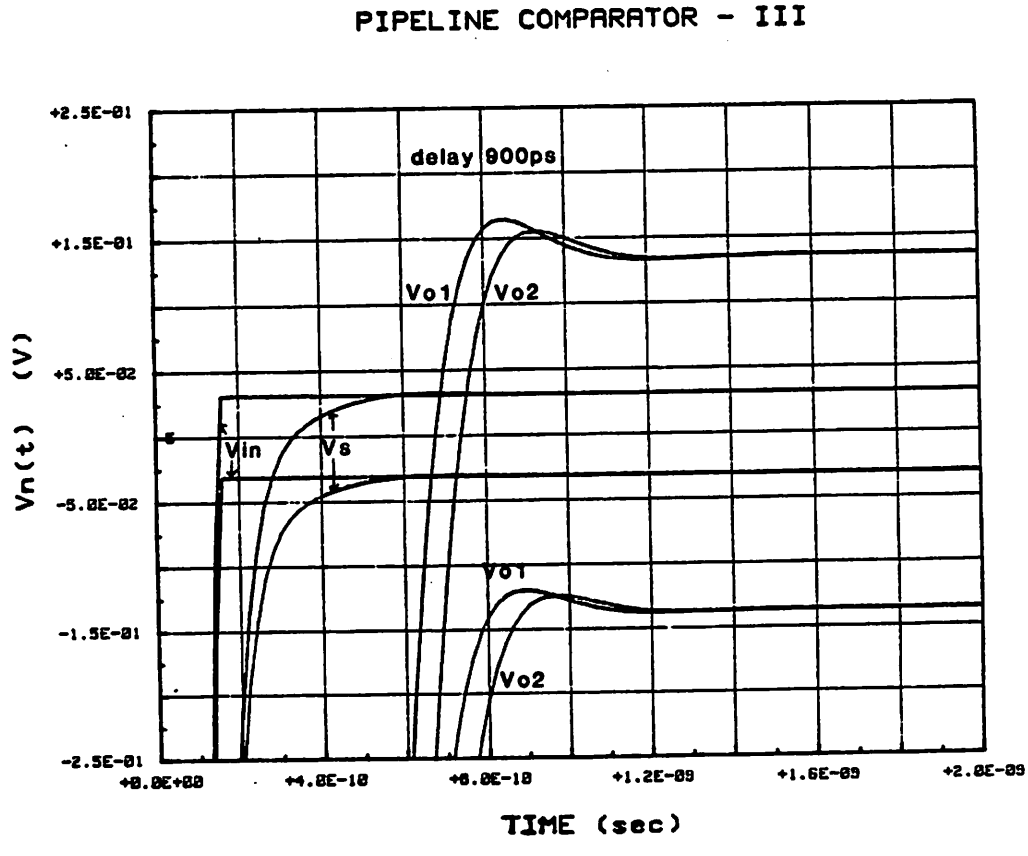


Fig. 3.36b Simulated step response of the BASF-amp in figure 3.33c with $C_c = 10fF$.

3.5 Comparator IV - Preamplifier + Regenerative Latch

The two D flip-flops that sample the output of the comparators in the previous sections are assumed to be simple dynamic MOS registers (MOS switch followed by an inverter). The comparators are expected to generate a large digital signal (5V) at their outputs in order to trigger the D flip-flop reliably. In this section, we consider a class of comparators that drive a regenerative latch with a small signal-voltage and relies on the positive feedback in the latch to generate the final digital signal.

A simple bipolar latched comparator is shown in figure 3.37. The advantage of this circuit is that it can function without an input sample-and-hold. As ϕ_2 goes high, the positive feedback loop is enabled and the output voltage is sampled by the latch. Since it is difficult to implement a fast *S/H* in bipolar technology, the positive feedback latch became the basic building block in many fast bipolar comparator designs [27-30]. However, there is a penalty for not having a good input *S/H*. In figure 3.37, the latch samples the output of the differential pair that has a certain small-signal bandwidth. If the input signal has frequency components higher than the bandwidth of the amplifier, the signal at the output would be a highly distorted version of the input. This effect is complicated because the amplifier is both non-linear (due to saturation) and time-varying (due to the switching of ϕ_1). This distortion in both amplitude and phase at the amplifier output is referred to the input as *S/H* delay and apperture jitters. Therefore in a commercial flash 6-bit 20MS/s A/D such as the TDC1025 from TRW [28], the manufacturer requires that either the input be low pass filtered at less than the bandwidth of the preamplifier (which is usually lower than the Nyquist frequency) or an input *S/H* be used with the A/D. In this section, we assume that the input is sampled by a *S/H* and its bandwidth is much higher than the sampling frequency. The sampling instant is therefore well defined and the aperture uncertainty is solely a function of the phase jitter of the clock.

An analysis on the circuit in figure 3.37 is performed in section 3.5.1. This analysis suggests that at least two different design approaches can be adopted to improve the speed of the basic latched comparator. Section 3.5.2 presents a 6-bit comparator design which is

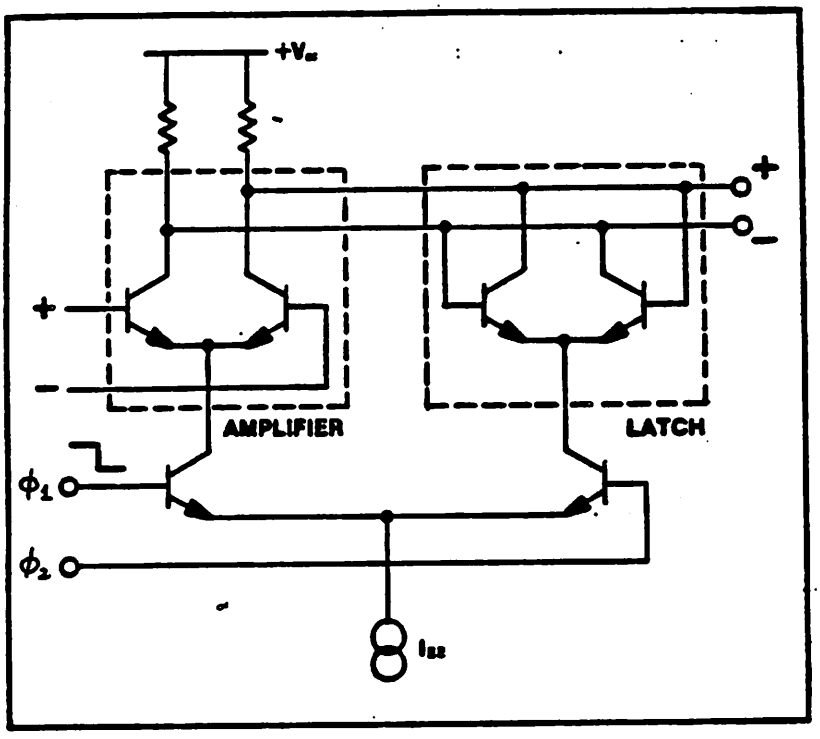


Fig. 2: Latching Comparator

Fig. 3.37 A simple bipolar latched comparator.

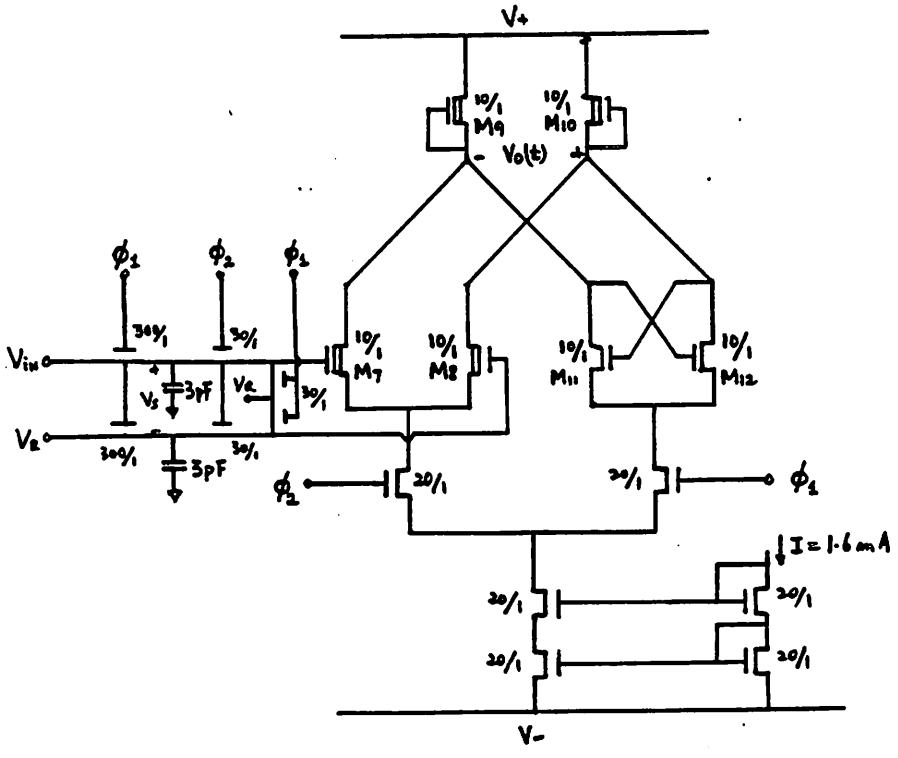


Fig. 3.38 A simple MOS latched comparator with input S/H.

based on over-driving the latch at its input. Finally in section 3.5.3, a new approach that employs negative feedback in the preamplifier section of the comparator to speed up recovery time is presented [34].

3.5.1 An Analysis on the Simple Latched Comparator

An MOS version of the bipolar latched comparator of figure 3.37 is shown in figure 3.38. An input *S/H* is added such that the sampling instant is well defined. During the period when ϕ_1 is high, the input is tracked by the two sampling capacitors, and the output voltage is regenerated by the positive feedback loop to one of the two stable states according to the sign of the previous sample. Then the input signal is sampled and transferred to the gate of M_7 and M_8 when ϕ_2 goes high. The length of time that ϕ_2 has to be kept high depends on the signal delay through the input differential pair and it will be referred to as the acquisition time t_{ac}. The length of time that ϕ_1 has to be kept high depends on the regeneration speed of the positive feedback loop (t_{reg}). In high-speed applications, only a two-phase 50%-duty clock scheme is practical because it can be generated by using a differential pair. If a 50% duty clock is assumed, then

$$t_{ac}=t_{reg} \tag{3.40}$$

when the comparator is operating at maximum speed. In this section we will solve for t_{ac} and t_{reg}, and conclude with a design curve for this simple comparator.

To simplify hand calculations, we assume that the delays in the MOS *S/H* and the clock rise-fall time are zero. The two equivalent circuits in figure 3.39a and b represent the differential-mode half-circuit for figure 3.38 when ϕ_1 and ϕ_2 are turned on respectively. To calculate t_{reg}, we can refer to figure 3.39a. In figure 3.39a, R is the resistance looking into the output nodes and C_{l1} represents the differential-mode capacitance loading the output nodes

$$C_{l1} = C_{gs_{11,12}}+4C_{gd_{11,12}}+C_{gd_{9,10}}+C_{sb_{9,10}}+C_{db_{11,12}}+C_{db_{7,8}}+C_{gd_{7,8}} \tag{3.41}$$

$$\approx 34fF$$

The differential equation that governs the dynamics of the positive feedback loop is

$$\frac{dv_o}{dt}+\frac{v_o}{RC_{l1}}-\frac{g_{m_{11,12}}}{C_{l1}}v_o = 0 \tag{3.42}$$

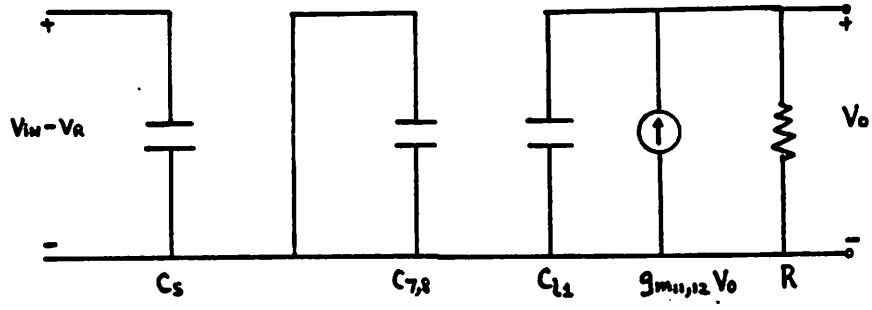


Fig. 3.39a Differential-mode half-circuit of figure 3.38 when ϕ_1 is high.

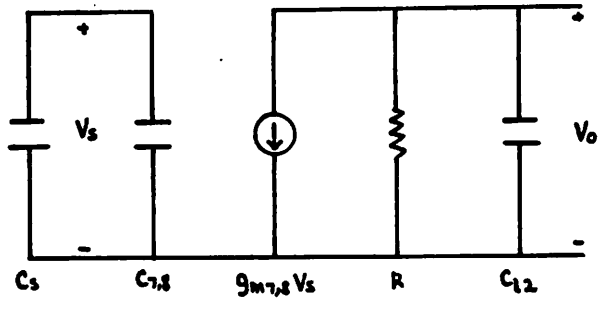


Fig. 3.39b Differential-mode half-circuit of figure 3.38 when ϕ_2 is high.

The solution to this equation is

$$v_o(t) = v_o(t_{ac})\exp\left[t\frac{g_{m11,12}}{C_{l1}}\left(1-\frac{1}{g_{m11,12}R}\right)\right] \tag{3.43}$$

where $V_o(t_{ac})$ is the initial voltage at the output when ϕ_1 first goes high. Since t_{reg} is the time required for the output voltage to reach V_{final}, it follows that

$$v_o(t_{ac}) = V_{final}\exp\left[-t_{reg}\frac{g_{m11,12}}{C}\left(1-\frac{1}{g_{m11,12}R}\right)\right] \tag{3.44}$$

To solve for t_{reg}, we need to know $v_o(t_{ac})$.

In figure 3.39b, R is again the output resistance of the differential pair M_7 and M_8. C_{l2} is the capacitive loading at the output

$$C_{l2} = 4C_{gd11,12}+C_{db11,12}+C_{sb9,10}+C_{gd9,10}+C_{gd7,8}+C_{db7,8} \tag{3.45}$$

$$\approx 40fF$$

The initial output voltage (V_{ic}) when ϕ_2 goes high is -5V (digital output of the previous sample). During ϕ_2, the input sample stored in C_s is dumped onto the inputs of the differential pair. Under worst-case condition, the differential input voltage is $+V_{lsb}$. From figure 3.39b, it can be shown that

$$v_o(t_{ac}) = (g_{m7,8}RV_{lsb}-V_{ic})\left[1-\exp\left(\frac{-t_{ac}}{RC_{l2}}\right)\right] + V_{ic} \tag{3.46}$$

Using equation 3.40, 3.44 and 3.46 and assuming $g_{m11,12}=g_{m7,8}=g_m$,

$$V_{final}\exp\left[-t_{ac}\frac{g_m}{C_{l1}}\left(\frac{1-1}{g_m}R\right)\right] - (g_mRV_{lsb}-V_{ic})\left[1-\exp\left(\frac{-t_{ac}}{RC_{l2}}\right)\right] = 0 \tag{3.47}$$

Newton's method can be used to solve for t_{ac} in equation 3.47 and the solution is plotted in figure 3.40 for different values of g_mR and V_{lsb} (input resolution B ranges 1 to 10).

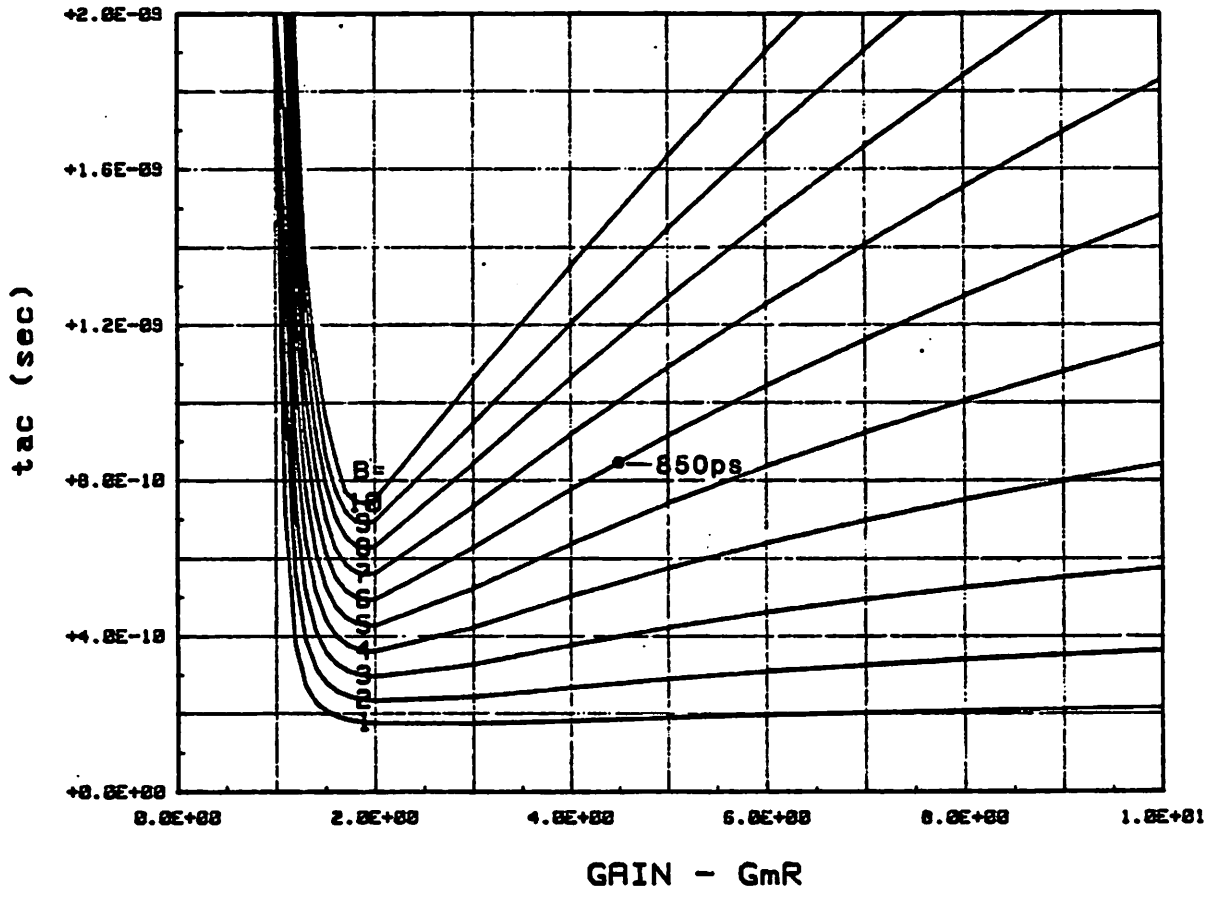


Fig. 3.40 Calculated acquisition time t_{ac} versus $g_m R$ and B of a simple latched comparator using equation 3.47.

In figure 3.40, t_{ac} approaches ∞ for $g_mR \leq 1$ because the positive feedback loop gain is less than 1. t_{ac} has minima at $g_mR=2$ and it increases monotonically as g_mR increases. If g_mR is 4.5 and V_{lsb} is 31mV, equivalent to 6-bit resolution, t_{ac} equals 850ps. Since we have neglected the delays in the *S/H* which is roughly equal to the rise and fall times of the clock ($t_{clock}=150ps$), the maximum sampling rate is

$$f_s\ mark = \frac{1}{2(t_{ac}+t_{clock})} \tag{3.48}$$

$$= 500MS/s$$

SPICE Simulation of the Simple Latched Comparator

To verify the design curve in figure 3.40, the transient response of the circuit in figure 3.38 is simulated using SPICE with a 500MHz two-phase clock. The simulated results are presented in figure 3.41a to d. The input, which is over-driven by -2V, +31mV, -2V, -31mV, etc., and clock waveforms are shown in figure 3.41a. The input voltage V_{in}, the sampled signal V_s and the input to the differential pair $v_{id}(t)$ are shown in figure 3.41b using an expanded scale. The simulated output voltage $v_o(t)$ in figure 3.41c shows that the comparator latches onto the correct state during ϕ_1 and that the comparator exhibits no *memory* of the previous sample, even when the previous sample is over-driven by the full-scale voltage (-2V). Finally, figure 3.41d plots the output waveform when it changes from -5V to +5V (2ns<t<4ns). The output voltage became positive at the 3ns mark. This implies that t_{ac} equals 1ns which is predicted by the above analysis and the design curve in figure 3.40 is accurate enough.

Figure 3.40 suggests that there are at least two ways to improve the speed of the simple latched comparator. First, we can use a preamplifier to over-drive the latch at the input - equivalent to decreasing B. Secondly, we can reduce the output resistance of the latch - equivalent to decreasing g_mR. In fact a combination of these two methods may prove beneficial. In the following sections, we will present two improved comparator designs based on these approaches.

Fig. 3.41 SPICE simulation of the simple latched comparator in figure 3.38.

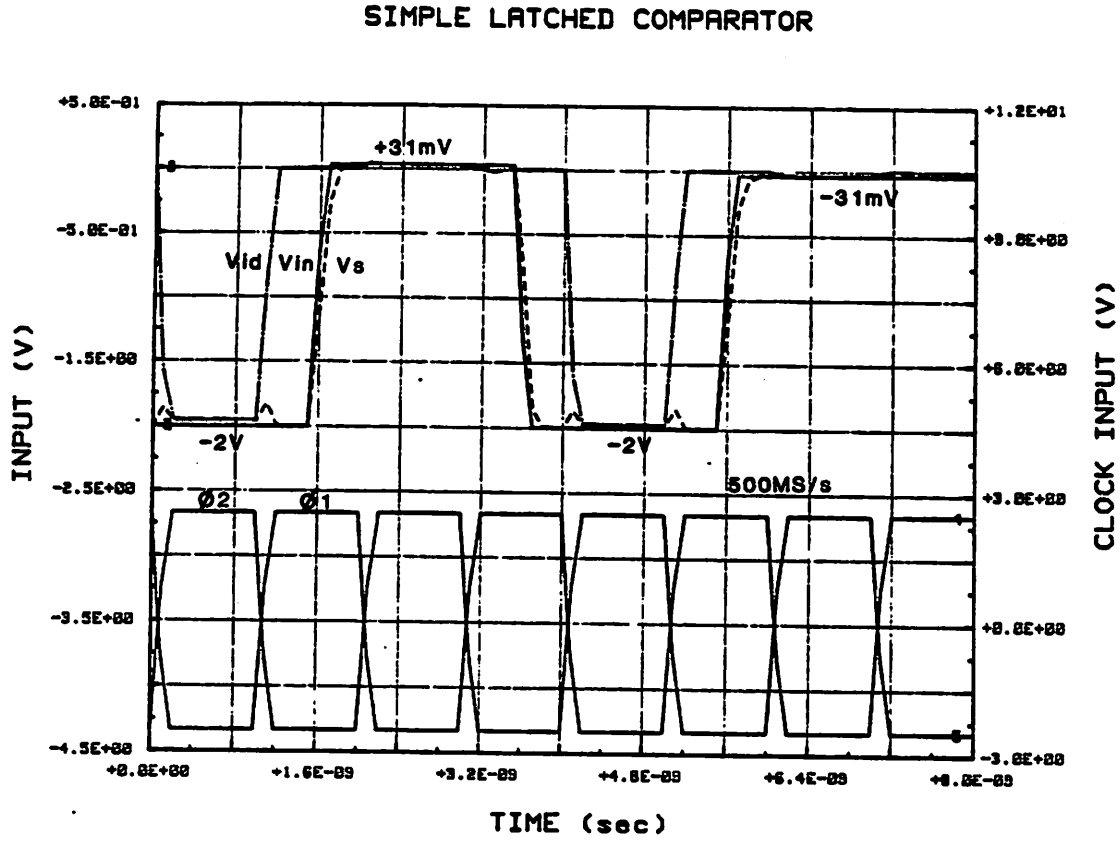


Fig. 3.41a Clock and input waveforms of the simulation.

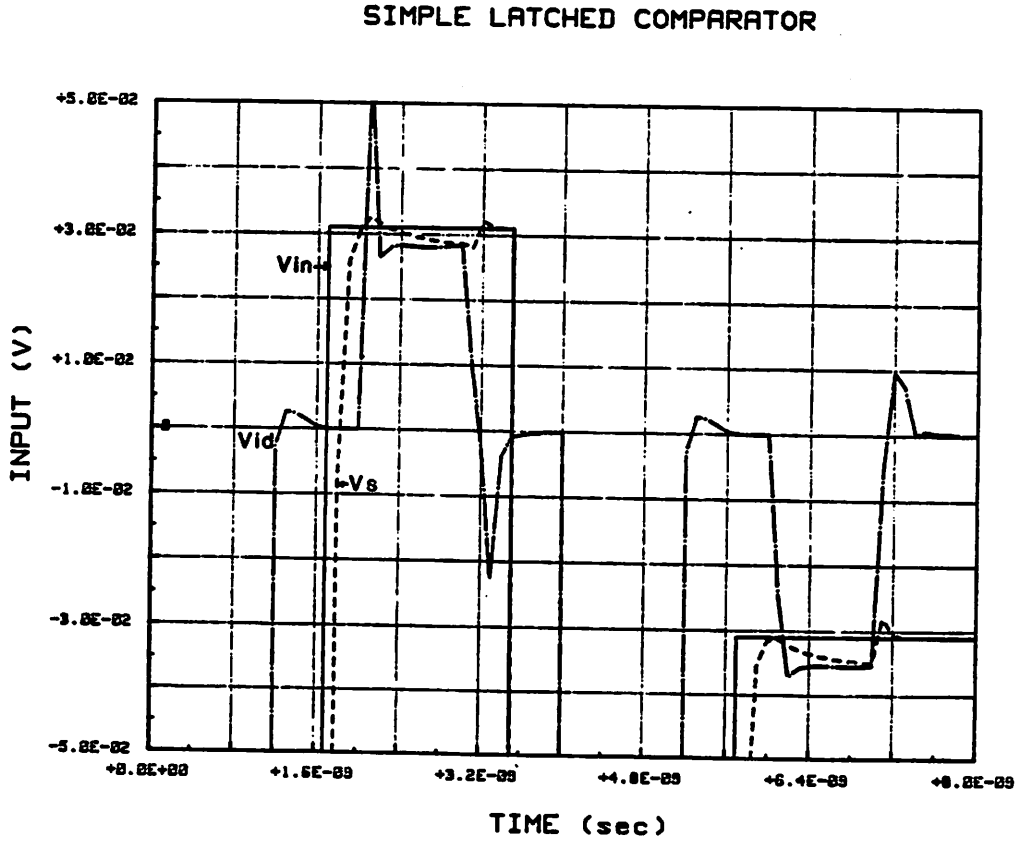


Fig. 3.41b Simulated waveforms in the input S/H.

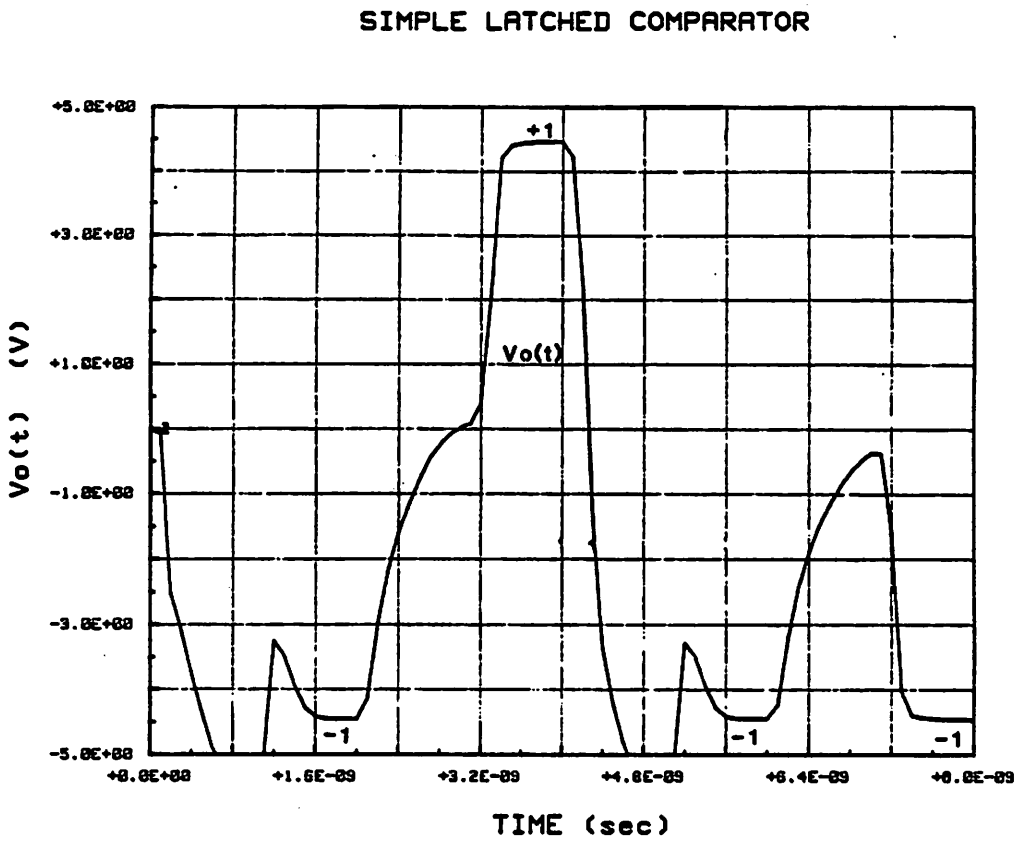


Fig. 3.41c Output waveform of the simple latched comparator.

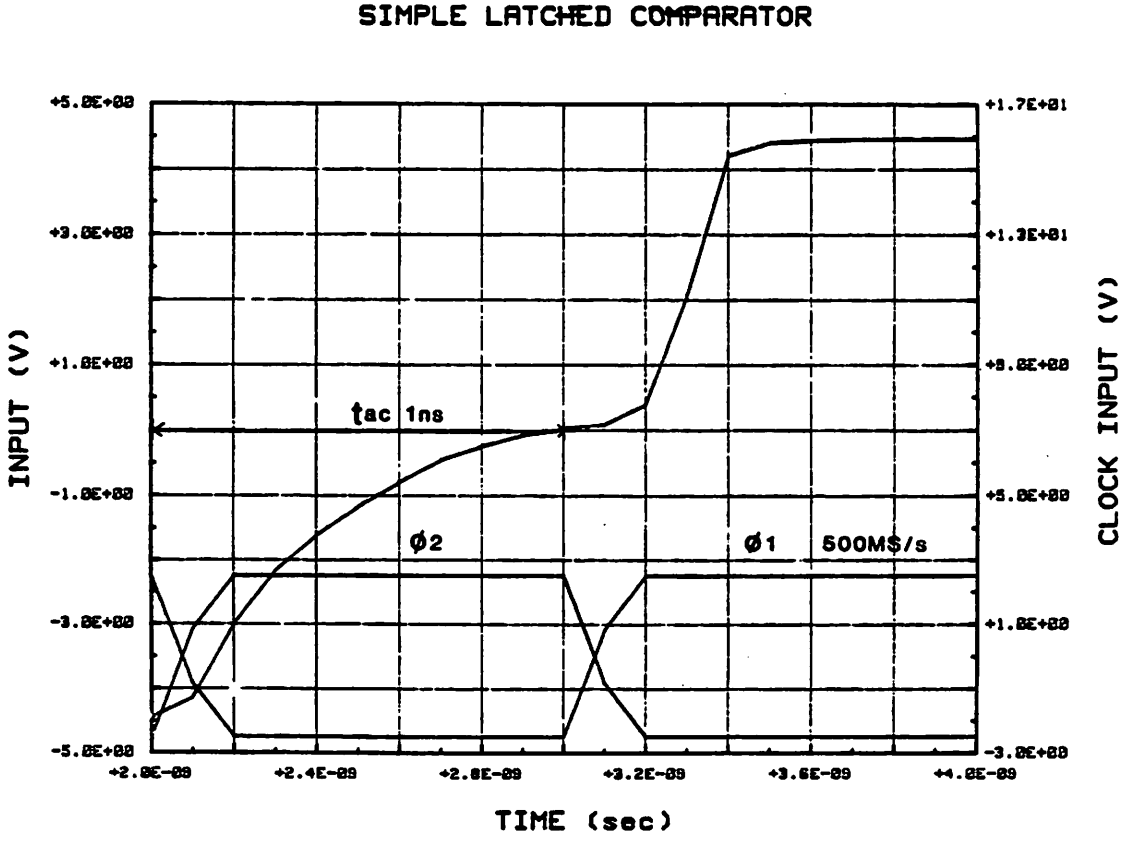


Fig. 3.41d Detailed output waveform showing acquisition time of the comparator.

In summary, the maximum sampling rate of the simple latched comparator is 500MS/s, with a delay through the comparator of 2ns.

3.5.2 Open-Loop Preamplifier with Reset + Latch

In this section, we investigate the use of a preamplifier to increase the drive to the simple latched comparator. Most bipolar latched comparators have one to two preamplifier stages [29] [30] because cascading more open-loop amplifiers would result in substantial bandwidth shrinkage. Since these bipolar comparators are usually used without an input *S/H* and they rely on the positive feedback latch to define the sampling instant, the bandwidth of the preamplifier must be kept as high as possible. If the input has frequency components higher than the bandwidth of the preamplifier, those components would have a different phase shift at the output of the preamplifier. The problem would be enhanced if the preamplifier is driven into saturation at the same time. In general, these non-linear effects when referred back to the input constitute sampling delay and aperture jitter in the comparator.

In MOS, we can correct the above problem by using an input S/H; then which preamplifier configuration is fastest in over-driving the simple latched comparator? If another differential pair is added between the input *S/H* and the latched comparator in figure 3.38, the acquisition time of the resulted comparator would increase. Since the output of the added differential pair is also over-driven during the previous sample, the delay through the added differential pair is comparable to the delay of through transistor M_7 and M_8 and the combined delay from the input to the output of the comparator is actually worse than that of the simple latched comparator. In order for *input overdrive* to work, the speed of the preamplifier must be much faster than that of the simple differential pair. In section 5.3, we learned that the delay through a cascade of open-loop amplifiers is greatly reduced if MOS switches are used to reset the internal nodes of the cascade. In this section, we investigate the use of a cascade of open-loop amplifiers with reset to improve the acquisition time of the comparator.

Consider the design in figure 3.42, where two differential pairs with common-mode feedback are added between the input *S/H* and the latched comparator. Source followers are used at the output to reduce loading capacitance and to isolate any switching transients generated from M_{31} and M_{32} from the positive feedback loop. During ϕ_1, the input waveform is sampled, the positive feedback loop is enabled through M_{26} and the outputs

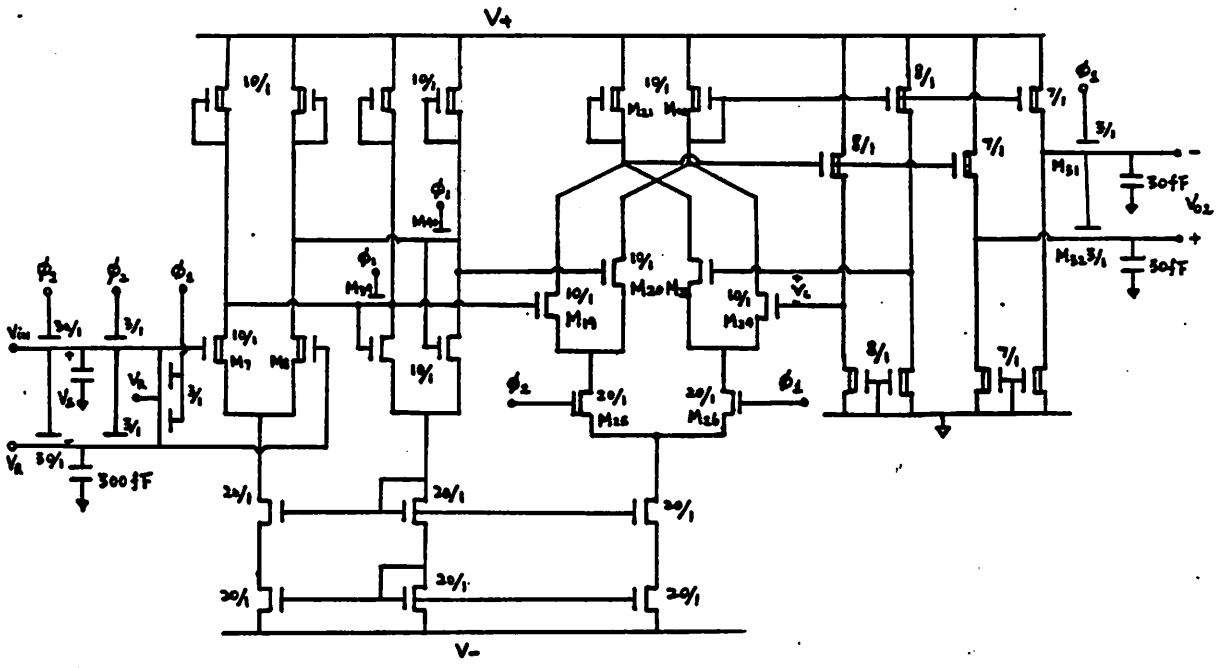


Fig. 3.42 Complete schematic of a comparator using open-loop preamplifiers with reset-switch and regenerative output latch.

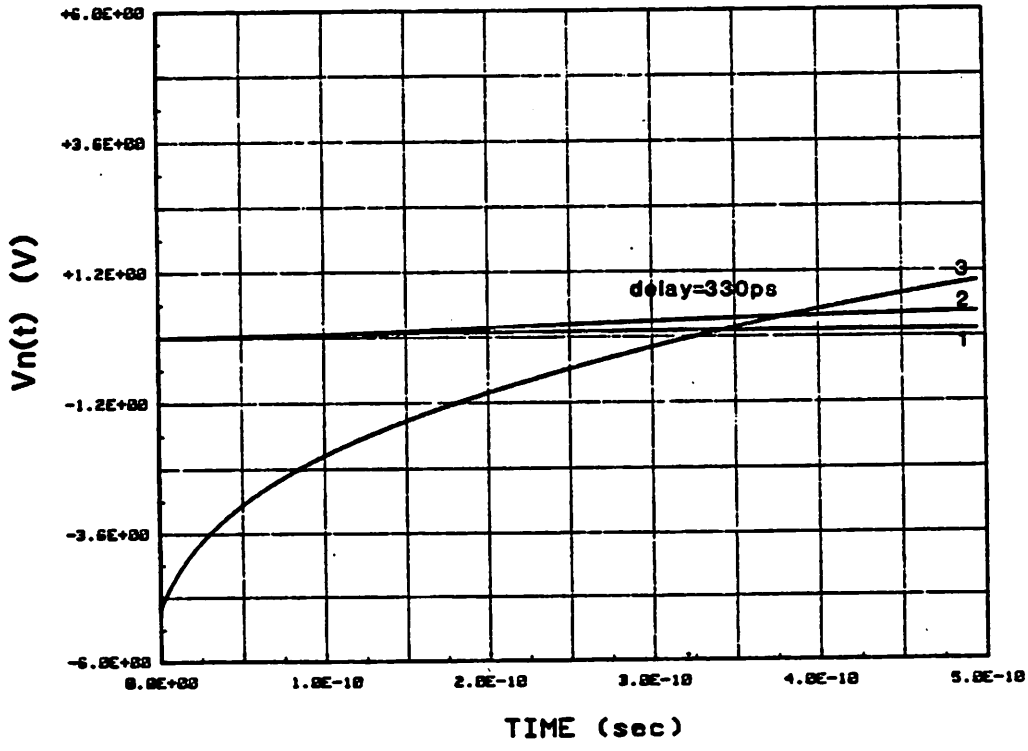


Fig. 3.43 Simulated acquisition time of the comparator in figure 3.42 using *program A*-5 with $g_m R$=4.5, B=6, $V_1(0)=V_2(0)=0V$ and $V_3(0)=-5V$.

of the preamplifier are reset to zero by turning on M_{39} and M_{40}. During ϕ_2 the preamplifier quickly establishes a signal at its output which drives the drains of M_{19} and M_{20} from its initial voltage (-5V) to an intermediate voltage according to the sign of the input. As ϕ_1 goes high again, positive feedback would latch onto the intermediate voltage, and regenerate the outputs to their final digital states.

We can use SPICE to simulate the delay in the preamplifier, but this configuration is similar to the one considered in section 5.3 - except that the output voltage of the last stage is not reset to zero when ϕ_2 goes high. Therefore, with minor changes to *program A−5*, we can use it to simulate the delay through the preamplifier - by setting the initial condition of the last stage to -5V. The output of *program A−5* is shown in figure 3.43. The output of the third stage crosses over to the positive side in 330ps. *Program A−5* neglects the effect of finite clock rise-fall time and assumes the reset switches added zero parasitic capacitance. Reset-switches actually contribute to about 10% of the total capacitive loading. The estimated delay in the preamplifier is equal to $330ps \times 1.1 + 150ps = 510ps$. Thus the two extra stages of open-loop amplification increase the sampling rate by a factor of two.

SPICE is used to verify the above design using a two-phase 1GHz clock. Outputs from this simulation is presented in figure 3.44a to 3.44d. The input waveform used in this simulation is similar to the one in the previous section where the overdrive voltages are -2V, +31mV, -2V, -31mV, etc. Inputs and clock waveforms are plotted in figure 3.44a. The output waveform plotted in figure 3.44c clearly shows that the comparator made the correct decisions. Figure 3.44d shows that the delay of the preamplifier is 470ps which is in agreement with the above estimation.

If the two added open-loop amplifier stages *with reset* can improve the sampling rate of the simple latched comparator from 500MS/s to 1GS/s, what is the optimum number of stage for this configuration? According to *program A−5* the optimum number of preamplifier stages is 5 and the simulated result corresponding to this case is presented in figure 3.45. In figure 3.45, the output of the sixth stage crosses over to the positive side in 270ns; this represents only a 60ps improvement over the 2-stage design (refer to figure

Fig. 3.44 SPICE simulation of the comparator in figure 3.42.

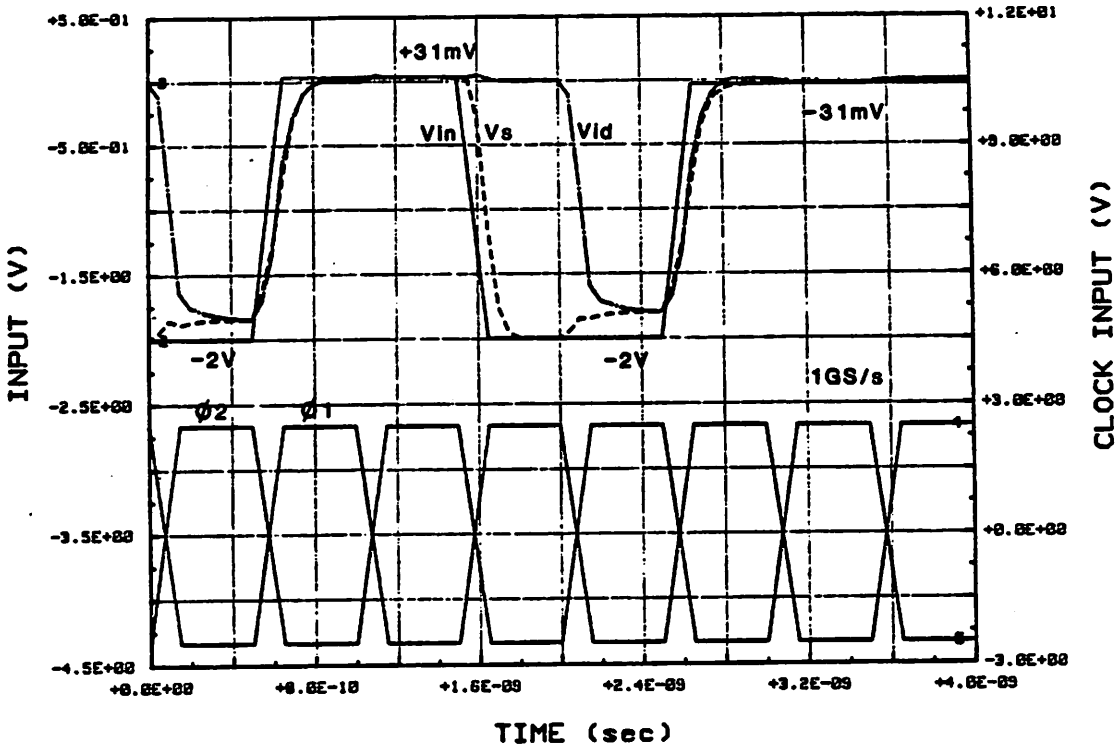


Fig. 3.44a Clock and input waveforms of the simulation.

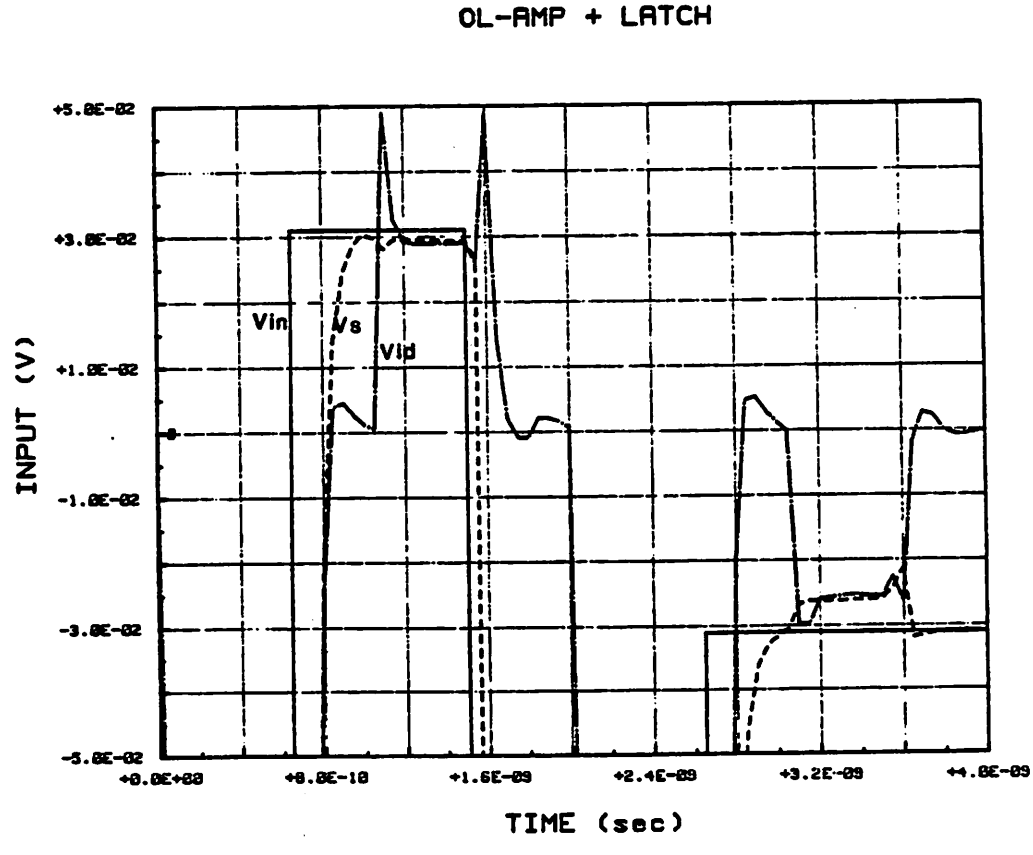


Fig. 3.44b Simulated waveforms in the input S/H.

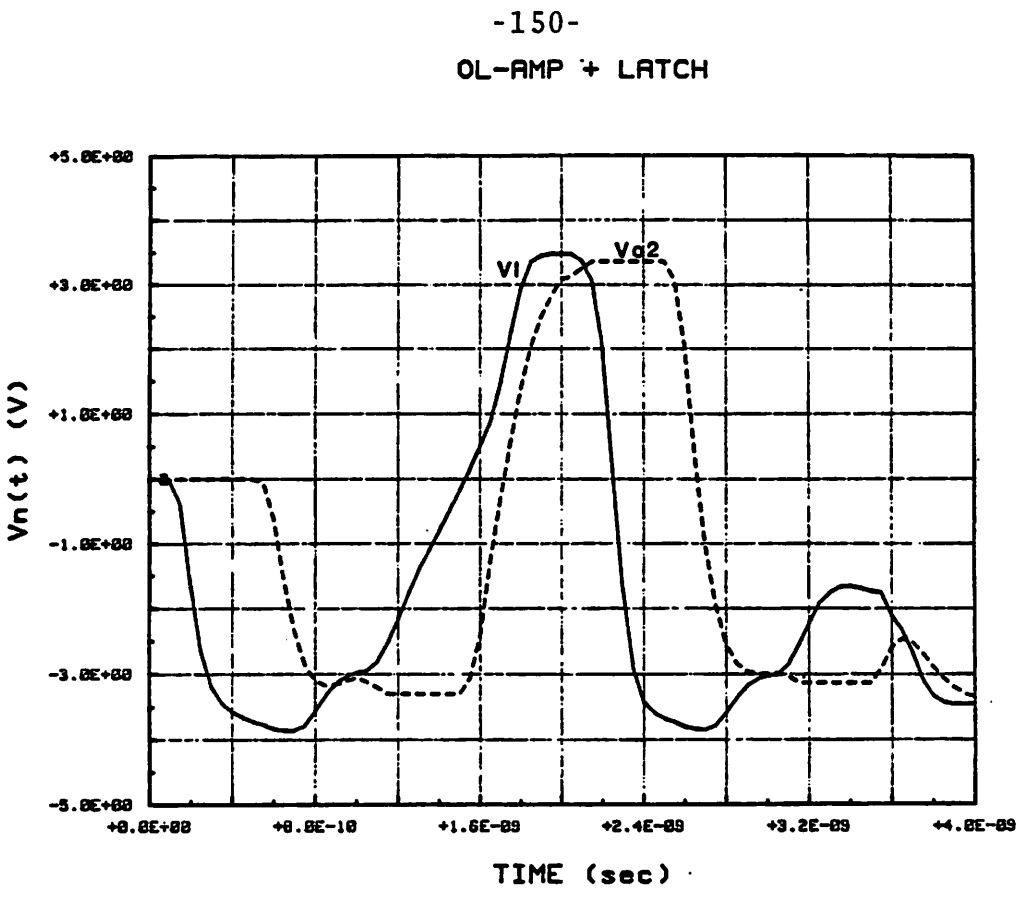


Fig. 3.44c Output waveforms of the comparator.

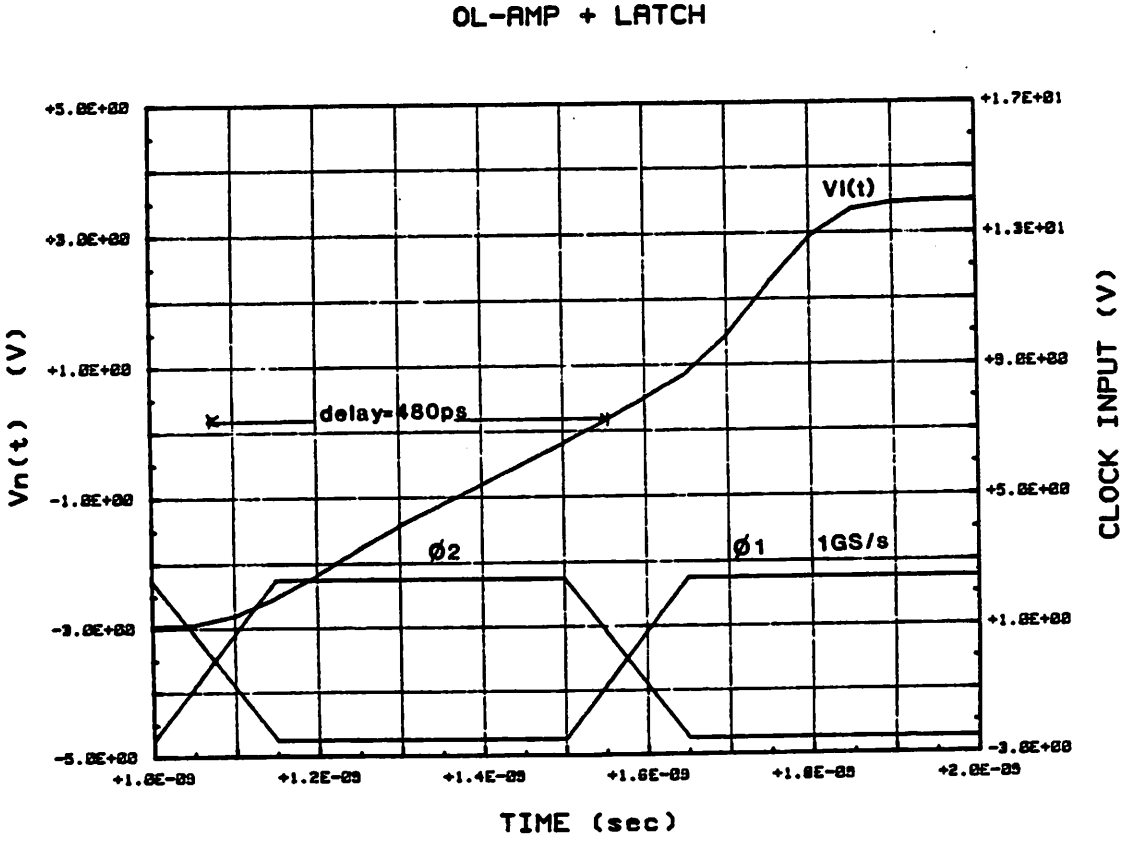


Fig. 3.44d Detailed output waveform showing acquisition time of the comparator.

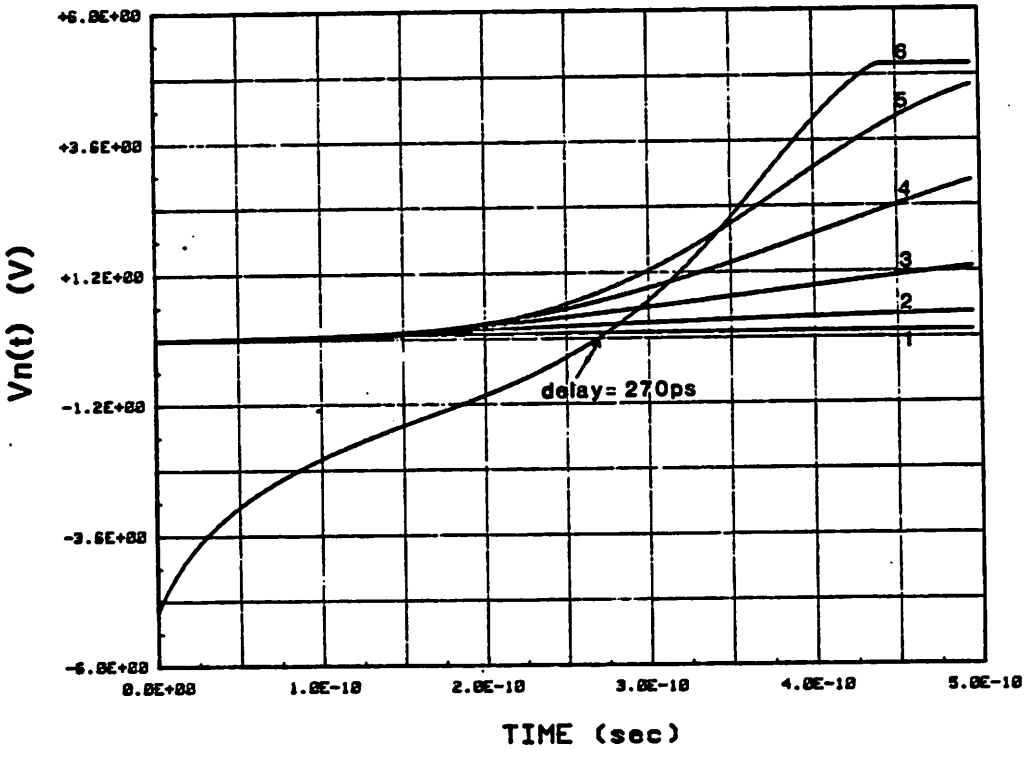


Fig. 3.45 Simulated delay of a cascade of 5 open-loop amplifiers with reset driving a simple latched comparator using *program* $A-5$ with $g_m R=4.5$, B=6, $V_1(0)$ to $V_5(0)=0$, and $V_6(0)=-5V$.

3.43). The expected maximum sampling rate for the 5-stage preamplifier design should approach 1.2GS/s. The penalty for this design is higher power dissipation.

In the next section, negative feedback is used to reduce the output impedance of the latch. It is shown that the maximum sampling rate for such a design also approaches 1.2GS/s but with a power dissipation lower than the 5-stage preamplifier design of this section.

3.5.3 Feedback Preamplifier + Latch

Figure 3.40 suggests that the speed of the simple latched comparator can be increased by reducing the output resistance of the latch. This means reducing the gain of the differential pair to about 2. This can be accomplished either by using an inverter ratio other than one, or by using an enhancement-mode load. However, both methods have their disadvantages. In this section we resort to negative feedback since it can trade open-loop gain for bandwidth and reduce the input-output impedance of an amplifier.

Figure 3.46 is the complete schematic of the latched comparator. The preamplifier section of this comparator, M_7 to M_{22}, has the same configuration as that of the BASF-amp in section 2.3. The circuit is functionally similar to the comparator in the previous section (fig. 3.42). They share the same clocking scheme, the same output buffer design and the same input *S/H* design. Instead of using reset switches to speed up over-drive recovery, this design employs negative feedback to inject part of the output signal (of the previous sample) to the internal nodes of the amplifier. The acquisition time of the comparator is determined by the bandwidth of the BASF-amp and the regeneration time is given by equation 3.43. Since the gain of the BASF-amp is controlled by the the ratio $\frac{g_{m7,8}}{g_{m11,12}}$ and the normalized gain-bandwidth product of the amplifier is a constant, the width of the feedback source follower stage M_{11} and M_{12} is optimized such that the acquisition time equals the regeneration time when the latch is driven under the worst-case condition. Compensation capacitors (C_{c1} and C_{c2}) are needed to suppress ringing at the amplifier outputs. In this particular design $W_{7,8}$ is $10\mu m$, $W_{11,12}$ is $1.5\mu m$ and $C_{c1}=C_{c2}=10fF$.

The dc biasing of the circuit in figure 3.46 is somewhat unconventional. During ϕ_2, the common-mode voltage of the amplifier is controlled by the common-mode feedback loop. When ϕ_1 is enabled, the current in the Cascode current source is controlled by M_{21} and M_{22} which are of the same size as transistor M_9 and M_{10}. According to SPICE simulations, this switching back and forth between common-mode feedback and *tracking bias* does not affect the operation of the comparator.

SPICE is used to simulate the transient response of this comparator, and the simulated results are presented in figure 3.47a to 3.47d. The input and the clock waveforms

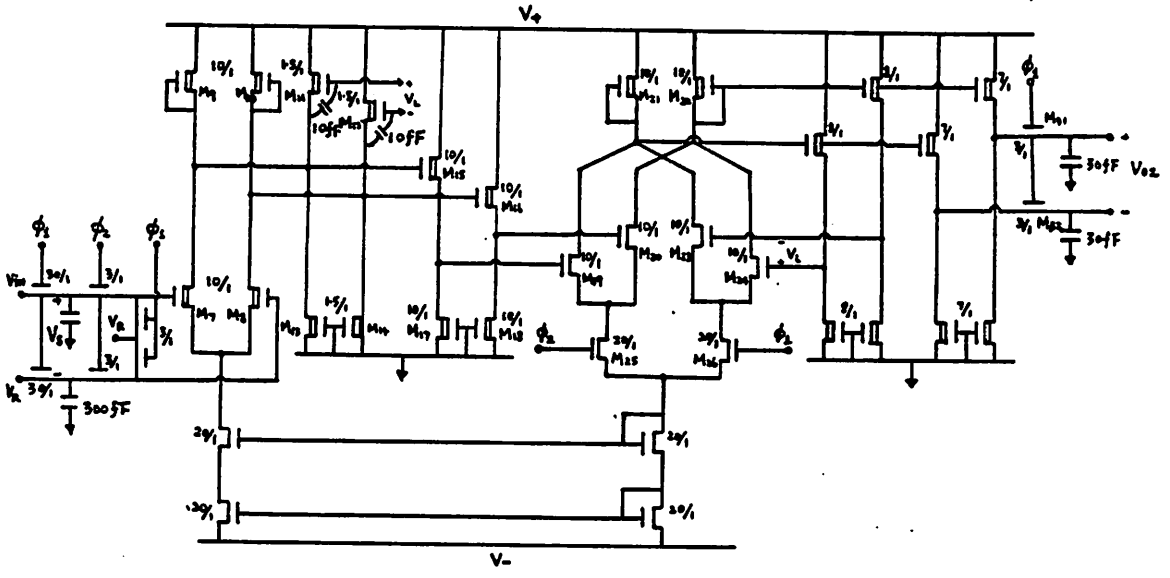


Fig. 3.46 Complete schematic of a comparator using feedback preamplifier and regenerative output latch.

Fig. 3.47 SPICE simulation of the comparator in figure 3.46.

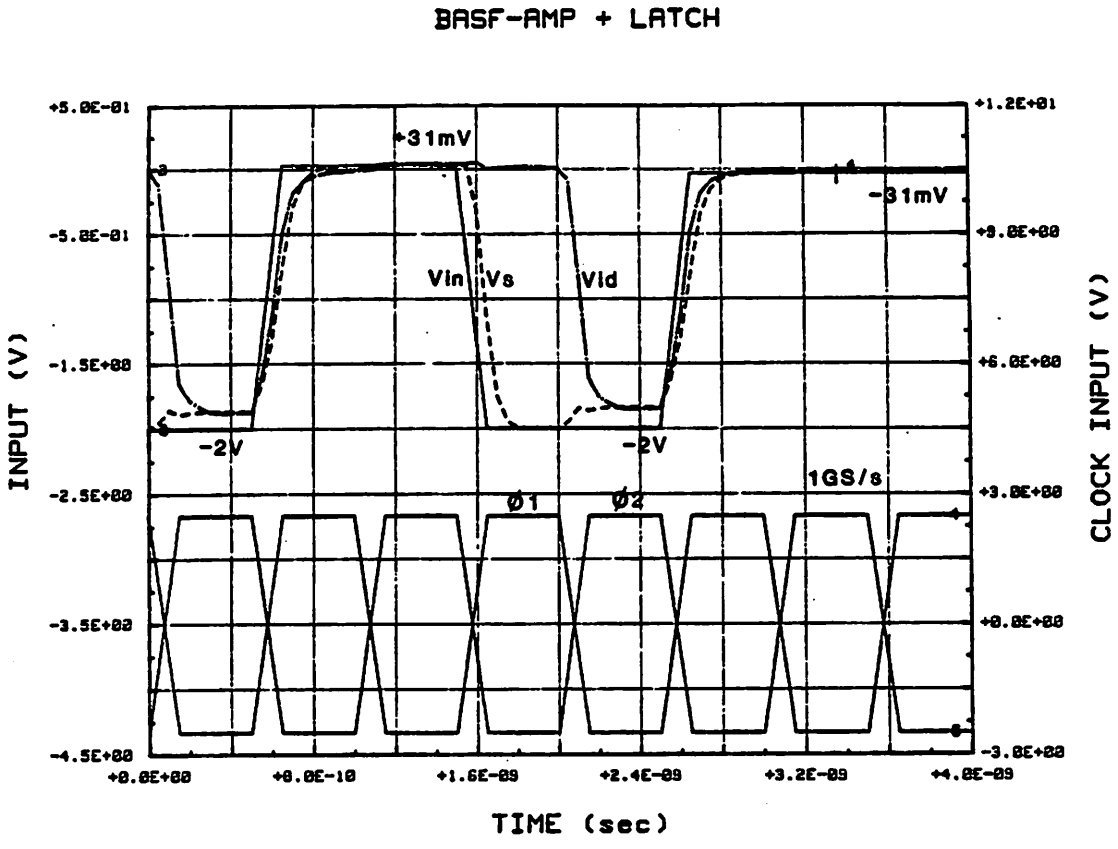


Fig. 3.47a Clock and input waveforms of the simulation.

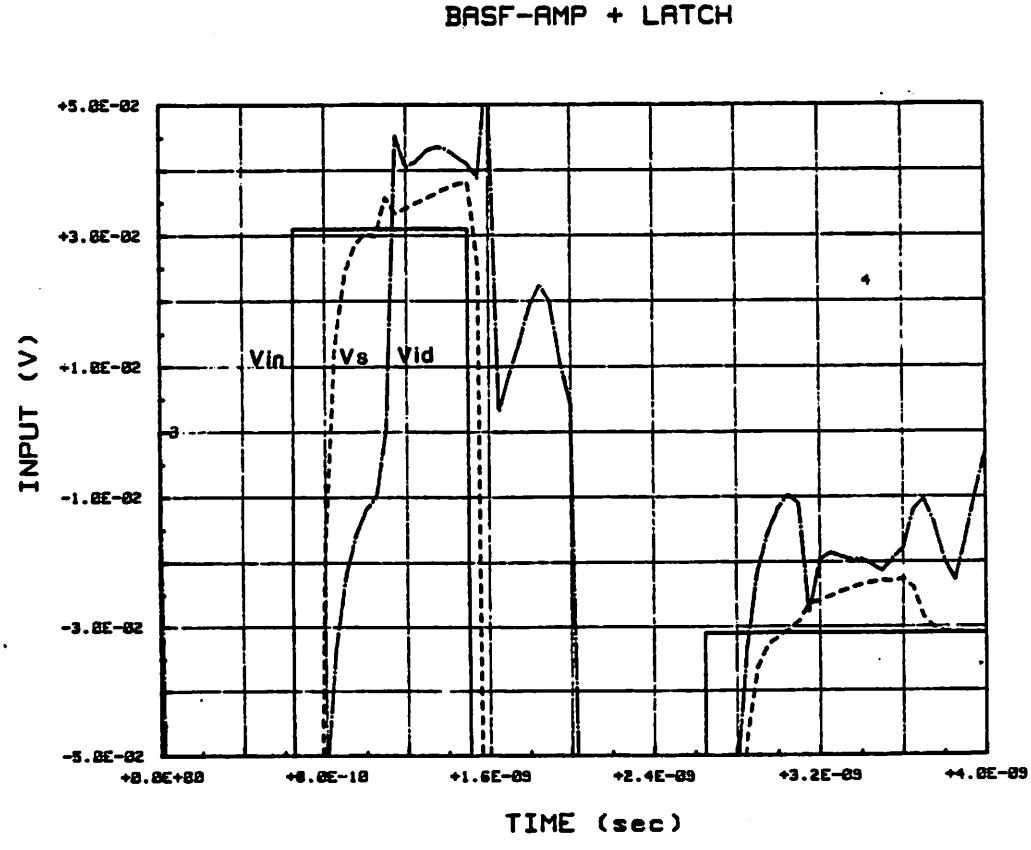


Fig. 3.47b Simulated waveforms in the input S/H.

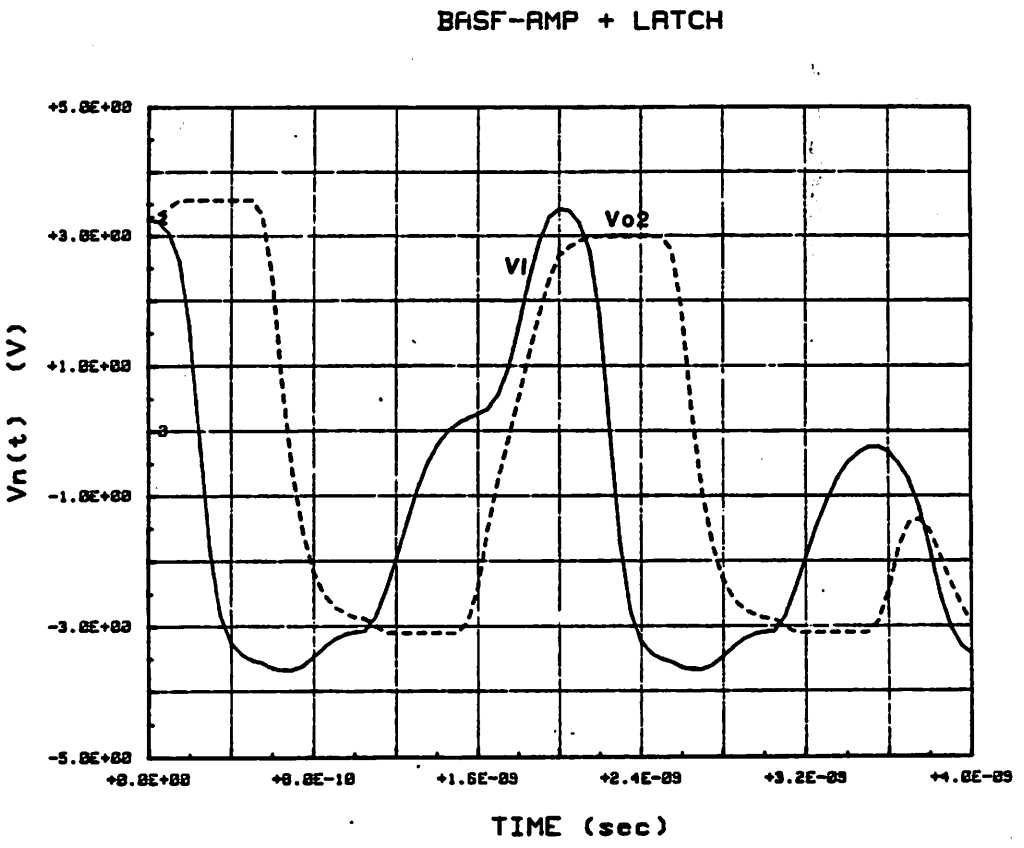


Fig. 3.47c Output waveforms of the comparator.

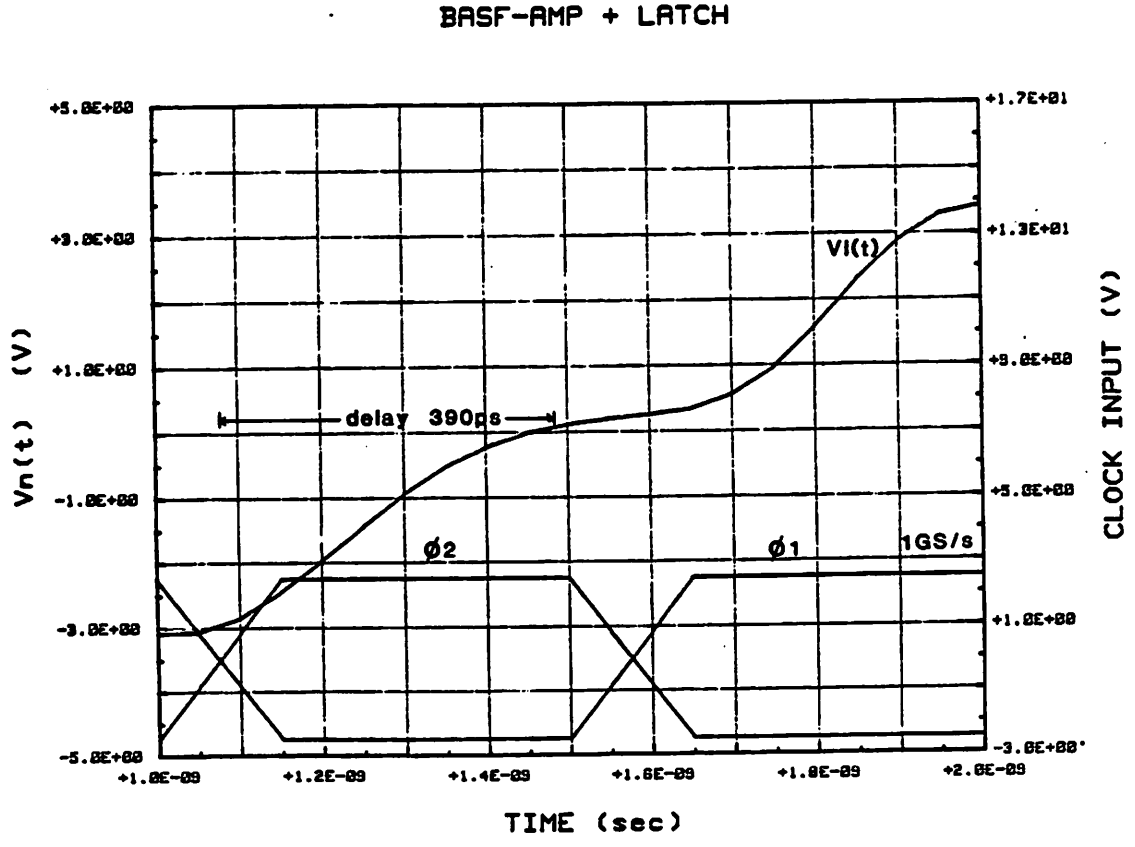


Fig. 3.47d Detailed output waveform showing acquisition time of the comparator.

plotted in figure 3.47a and b are identical to those plotted in figure 3.44a and b of the previous section. A 1GHz clock is again used in this simulation. The output waveform in figure 3.47c not only showed that the comparator is functioning properly, but this design is faster than the one in the last section. Figure 3.47d shows the comparator output when it is making a transition from -5V to +5V while the input is over-driven by V_{lsb}. The output became positive in only 390ps after the clock transition. This implies that the maximum sampling rate of this comparator is 1.2GS/s and the comparator delay is about 830ps.

3.6 Performance Summary and Conclusion

In this chapter, four basic comparator configurations that are suitable for the MOS technology have been investigated, and eight different comparators have been designed based on these four configurations. Table 3.1 summarizes the simulated performance of these comparators. The design principle established by this work are as follow:

1. Cascade of open-loop amplifiers - The comparison delay as predicted in figure 3.13 to 3.15 is surprising because the findings are contrary to conventional practice in the design of comparators in this configuration. Figure 3.14 and 3.15 suggested that the optimal gain per stage is about 3 and as g_mR is increased, the comparison delay increases significantly. Most conventional comparator designs are basically uncompensated operational amplifiers with two stages of open-loop gain at 40dB per stage. This is why the delay associated with such designs are typically about 20ns [37]. The speed of this type of comparator can be improved if we use more stages and less gain per stage (refer to figure 3.13).

2. Cascade of open-loop amplifiers with reset - The comparator delay of this configuration is predicted in figure 3.25 and 3.27. Figure 3.25 is for the case when g_mR is 4.5 while 3.27 is for the case when g_mR is infinite. Figure 3.8 suggests that the comparison time decreases monotonically as g_mR approaches infinity and that if g_mR is greater than 10, it can be treated as infinite. The result shown in figure 3.27a is then somewhat surprising. Although $g_mR=\infty$, we still require a large number of stages in order that we reach the optimal design. Most existing comparators based on this configuration have three to five stages. As seen from figure 3.27a, an optimal 16-bit comparator should have 14 stages and a per-stage gain of at least 10!

3. Pipeline of differential amplifiers - The clock rate of this configuration depends on the settling time of the differential amplifiers used. Since the MOS *T/H* added additional capacitive loading onto the output nodes of the amplifiers, designs with a low output resistance settle faster. Both the output source follower buffer and the

COMPARATOR CONFIGURATION	RATE MS/s	DELAY ps	POWER mW
I : Cascade of open–loop amplifiers	600	1500	96
II : Cascade of open–loop amplifiers with reset	870	570	128
IIIa : Pipeline of open–loop amplifier	300	6600	64
IIIb : Pipeline of ASF–amp	770	2600	160
IIIc : Pipeline of BASF–amp	1100	1800	192
IVa : Simple latched comparator	500	2000	16
IVb : Open–loop preamplifier + latch	1100	900	60
IVc : Feedback preamplifier + Latch	1200	830	52

TABLE 3.1 Summary of comparator performances.

negative feedback in the BASF-amp contributed to the reduction of its output resistance, and therefore the BASF-amp is preferred in this configuration.

4. Preamplifier + regenerative latch - the acquisition time of the simple latched comparator is shown in figure 3.40 which suggested that the two methods can be used to improve its speed performance - by either overdriving the latched comparator at its input or by reducing the output resistance of the latch. Both methods are explored in section 3.5. Negative feedback and reset-switches are two effective circuit techniques in the MOS technology to reduce the overdrive recovery of an amplifier.

Table 3.1 summarizes the preformance of the eight examples of a 6-bit comparator in this technology. Comparator-I has the worst overall performance. Comparator-II has the shortest comparison delay. Comparator-III and comparator-IV have the highest sampling rate (exceeding 1GS/s). Besides speed considerations, power consumption also plays an important role in deciding which configuration is more suitable. The simple latched comparator consumes the least power, however with a moderate increase in power, the sampling rate of comparator-IVc is increased by a factor of 2.

Chapter 4 Experimentation

In this chapter, experimental results are presented to support the theories presented in chapter 2 and 3. Four amplifiers and eight comparators have been considered in chapter 2 and chapter 3 respectively. Not all of these designs were fabricated and tested because the experiment was planned months before the completion of the theory itself. The circuit configurations of the feedback amplifier and the latched comparator presented in this chapter are similar to that of the BASF-amp in section 2.3 and that of the feedback-preamplifier latched comparator in section 3.5.3, respectively. These two circuit configurations have the best speed performance among those considered in this report.

For high frequency measurements, it is necessary to drive 50Ω transmission lines. This chapter begins by first presenting a 50Ω output buffer that has a loss of 3dB, a small signal bandwidth of 3.5GHz and an input capacitance of 120fF. In section 4.2, the measured insertion gain of the feedback amplifier is 9dB with a 1.17GHz bandwidth when driving the input capacitance of the 50Ω output buffer. Section 4.3 presents the measured results of the latched comparator. At 750 MS/s, the achieved input resolution of the comparator is 5 bits. The output signal amplitude is 1Vp-p and the measured error rate is less than 10^{-9}. Although the measured speed performance of the latched comparator is worse than that predicted by SPICE simulation, this result is already the fastest ever reported for a MOS technology. This comparator was reported at ISSCC 1985 [34].

4.1 A 3.5GHz 50Ω Output Buffer

In a test system, the measurement equipments are usually located at a few feet from the circuit under test. This distance is longer than the wavelength of the high frequency test signal, therefore the system components cannot be treated as lumped elements. 50Ω transmission lines such as coaxial cables must be used to bring high frequency signals to and from the test circuit. To minimize reflections, most high frequency measurement equipments have 50Ω terminal impedance. Because of this, it is necessary to fabricate on-chip output buffers that can drive the 50Ω load.

Figure 4.1 is the schematic of the output buffer which has a CD-CS configuration (section 2.2.2). The width of the source follower W_{sf} is $200\mu m$ and the width of the output inverter W_{inv} is $400\mu m$. The supply voltages (+2.5V and -3V) are chosen such that the dc transfer curve goes through the point where $V_{in}=V_{out}=0V$. This way, no dc power is delivered to the 50Ω load from the output buffer, and the system is dc coupled at both the input and the output. The measured dc transfer curve and gain of the 50Ω loaded output buffer is shown in figure 4.2. From figure 4.2, the maximum output voltage swing across the 50Ω load is 2.5Vp-p. This implies that the maximum output power of this buffer is 12.4dBm.

The measured and the simulated frequency response of the output buffer are shown in figure 4.3a and 4.3b respectively. The dominant RC time constant of this circuit is at the output node of the source follower and the RC time constants at both the input and the output of the buffer are neglectable. The measured bandwidth of the output buffer is 3.5GHz which is higher than the simulated bandwidth of 3GHz. This discrepancy can easily be accounted for because the measured effective channel length of this wafer is $0.9\mu m$.

The input impedance of a source follower is given by equation 2.14. Figure 2.13 is the simulated input capacitance of a source follower. According to SPICE simulation, the input capacitance is at $0.6fF/\mu m$, therefore the input capacitance of the 50Ω output buffer

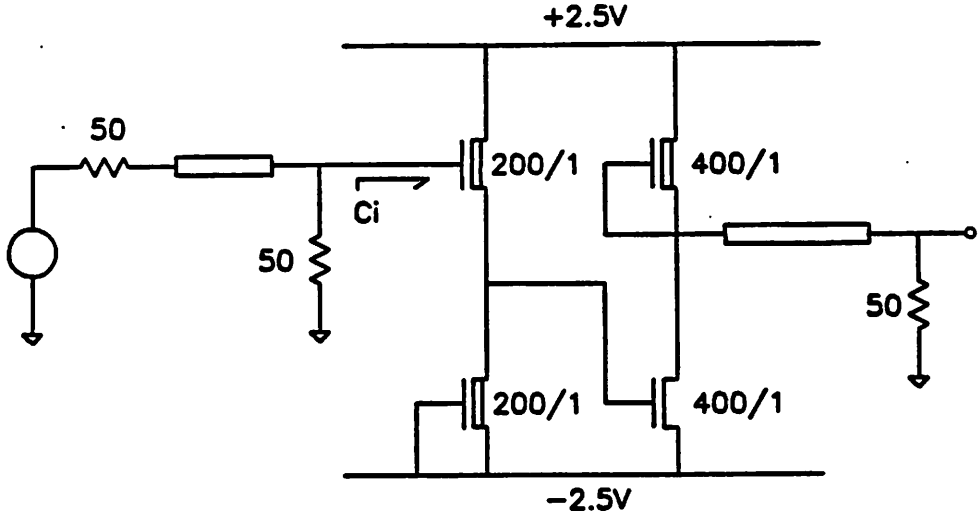


Fig. 4.1 50Ω output buffer.

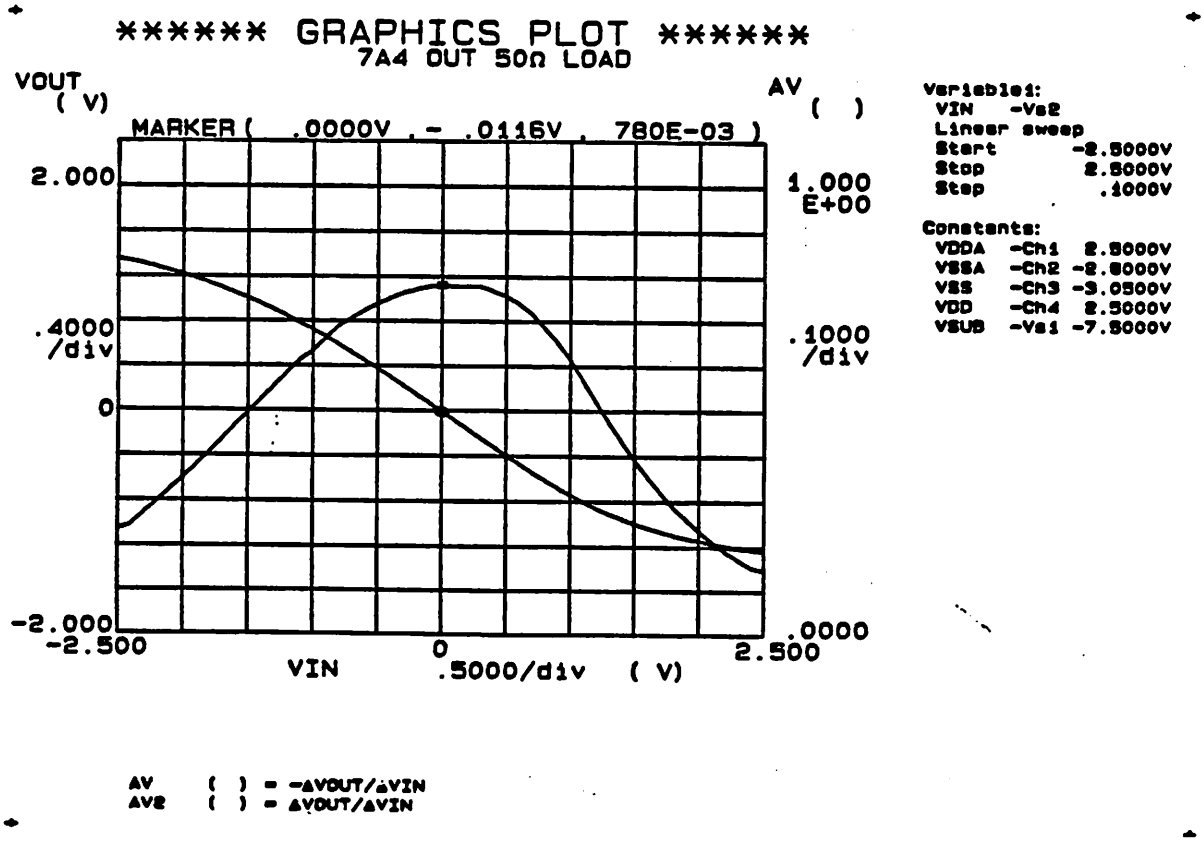


Fig. 4.2 Measured dc transfer curve and gain of the 50Ω output buffer.

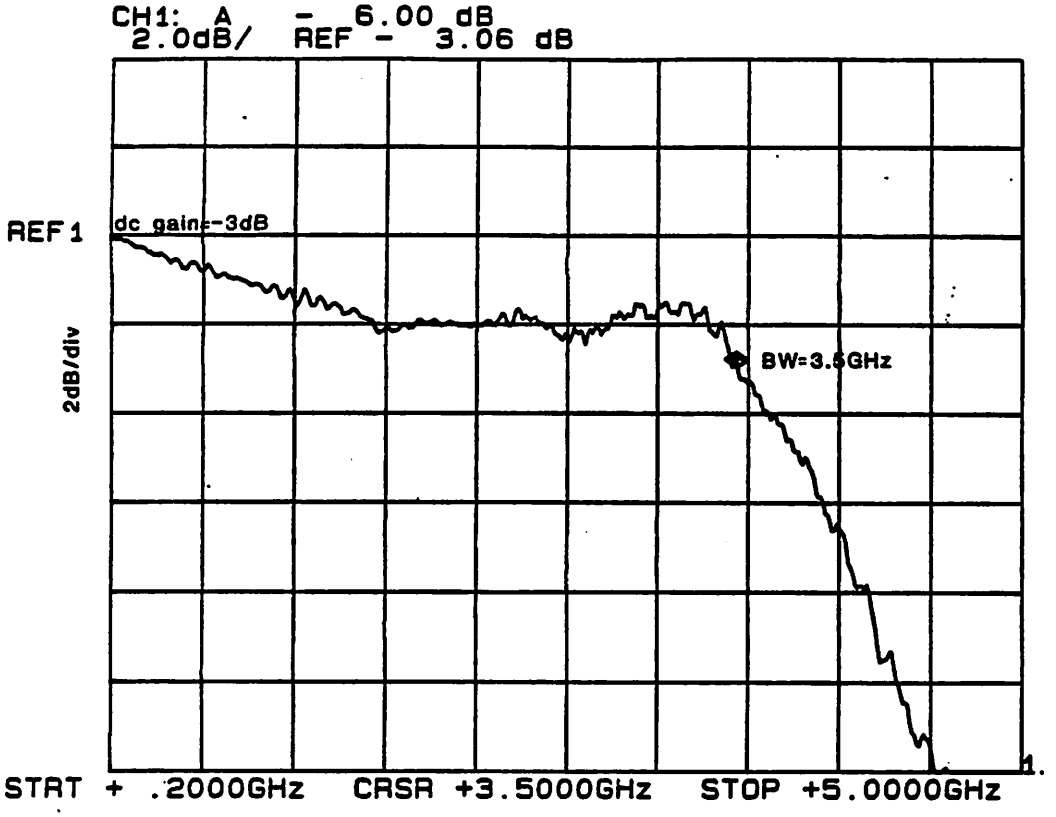


Fig. 4.3a Measured frequency response of the 50Ω output buffer.

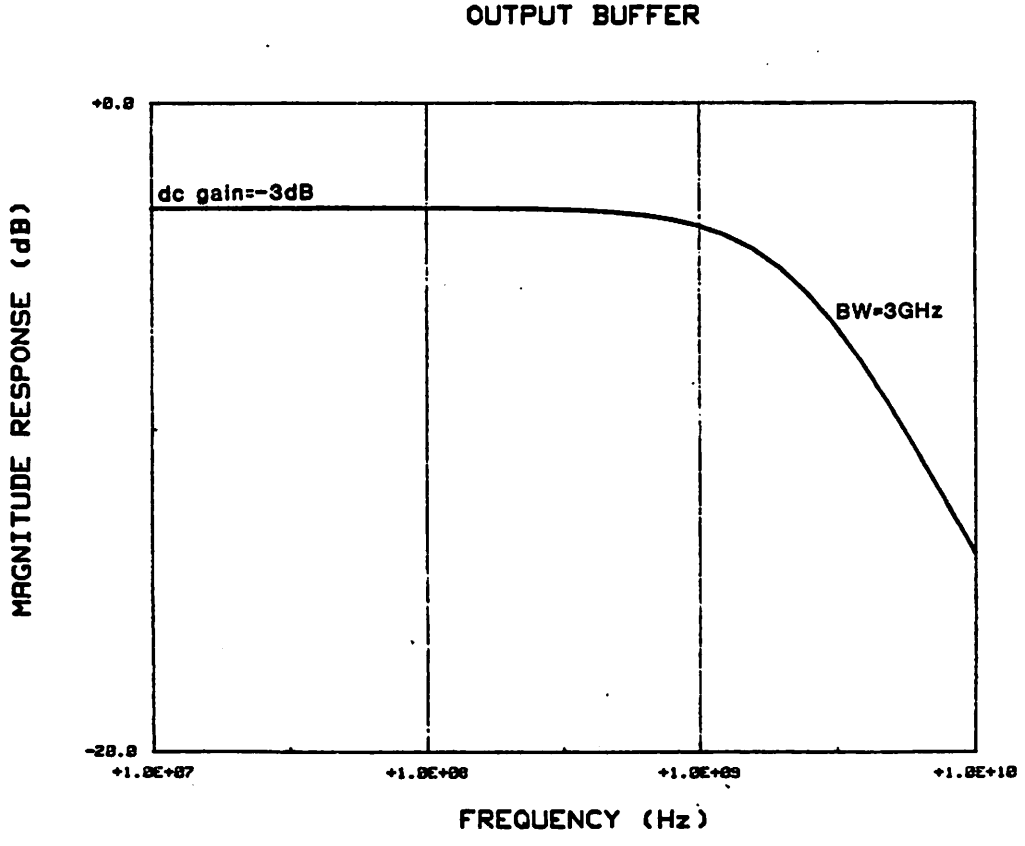


Fig. 4.3b Simulated frequency response of the 50Ω output buffer.

is about 120fF.

Because of its wide bandwidth, this output buffer has been successfully incorporated into the measurement systems of the amplifier and the comparator in section 4.2 and 4.3 respectively.

4.2 A 1.17GHz Wide-Band Feedback Amplifier

A variation of the BASF-amp has been fabricated and tested at high frequencies. Its design is shown in figure 4.4. Transistor M_1 is the input transconductance stage and transistor M_2 together with the feedback transistor M_f form the trans-resistance stage. Transistor M_6 and M_7 are source follower buffers that serve to reduce the capacitive loadings at the two high impedance nodes of the amplifier. Compared to the BASF-amp in figure 2.28b, this design has two minor differences. First, the gate of the feedback transistor M_f is connected to the drain of M_2 instead of to the output of the source follower M_7. Therefore the delay in the feedback loop is reduced and its is not necessary to include any compensation capacitor to suppress overshoot in the amplifier step response. Secondly, the width of transistor M_4 and M_2 is reduced to $6\mu m$ such that the power dissipation in the amplifier is reduced. This results in a slight compromise in the amplifier frequency response.

To test the amplifier frequency response, an output buffer is required to isolate the feedback amplifier from the 50Ω load. The measurement setup is shown in figure 4.5. An identical output buffer fabricated on-chip is used as a reference for calibration. Losses due to the output buffer, the coaxial cables, and the package are subtracted from the measurement. The difference between the amplitude response of channel 1 and 2 in dB represents the insertion gain of the feedback amplifier when it is driving the input capacitance of the output buffer which is 120fF. This capacitive loading is equivalent to a *fanout* of 5 because the input capacitance of the feedback amplifier is 24fF. Figure 4.6 shows the die-photo of the feedback amplifier together with its 50Ω output buffer. Figure 4.7a is the measured amplifier insertion gain. The gain of the amplifier is 9dB and the bandwidth of the amplifier is 1.17GHz.

To correlate the measured results to SPICE simulations, the setup in figure 4.5 was simulated. The simulated amplifier insertion gain in figure 4.7b is 10dB and the simulated bandwidth is 1.4GHz. Both the measured amplifier gain and bandwidth are lower than

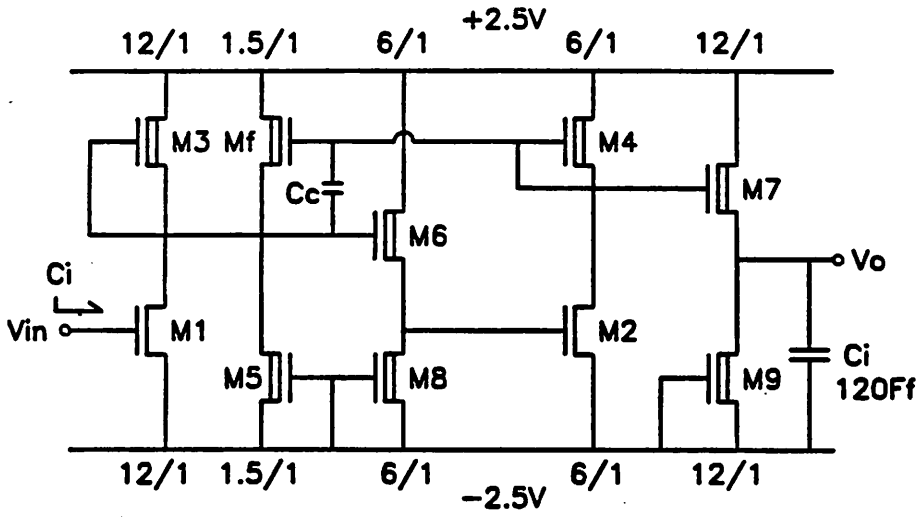
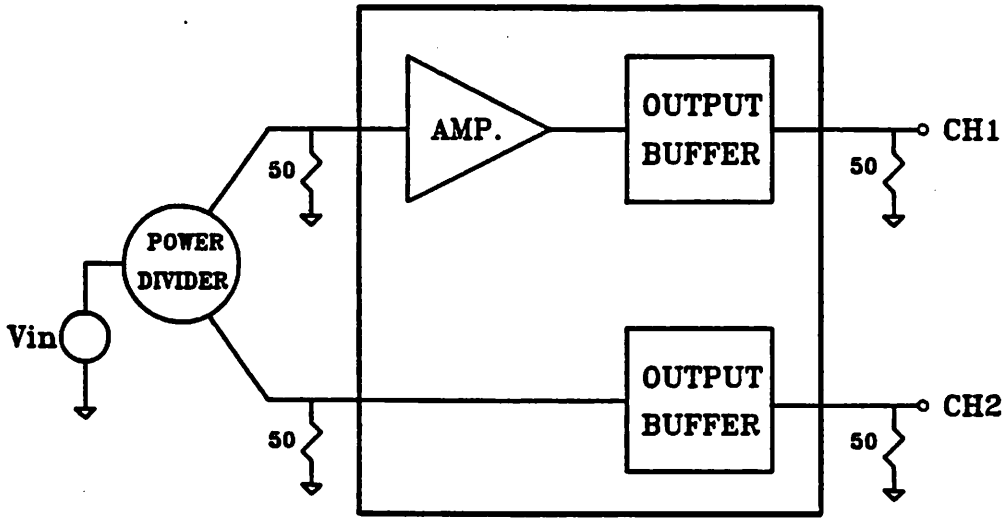


Fig. 4.4 Wide-band feedback amplifier.



*INSERTION GAIN = CH1 − CH2

Fig. 4.5 Measurement setup for the feedback amplifier.

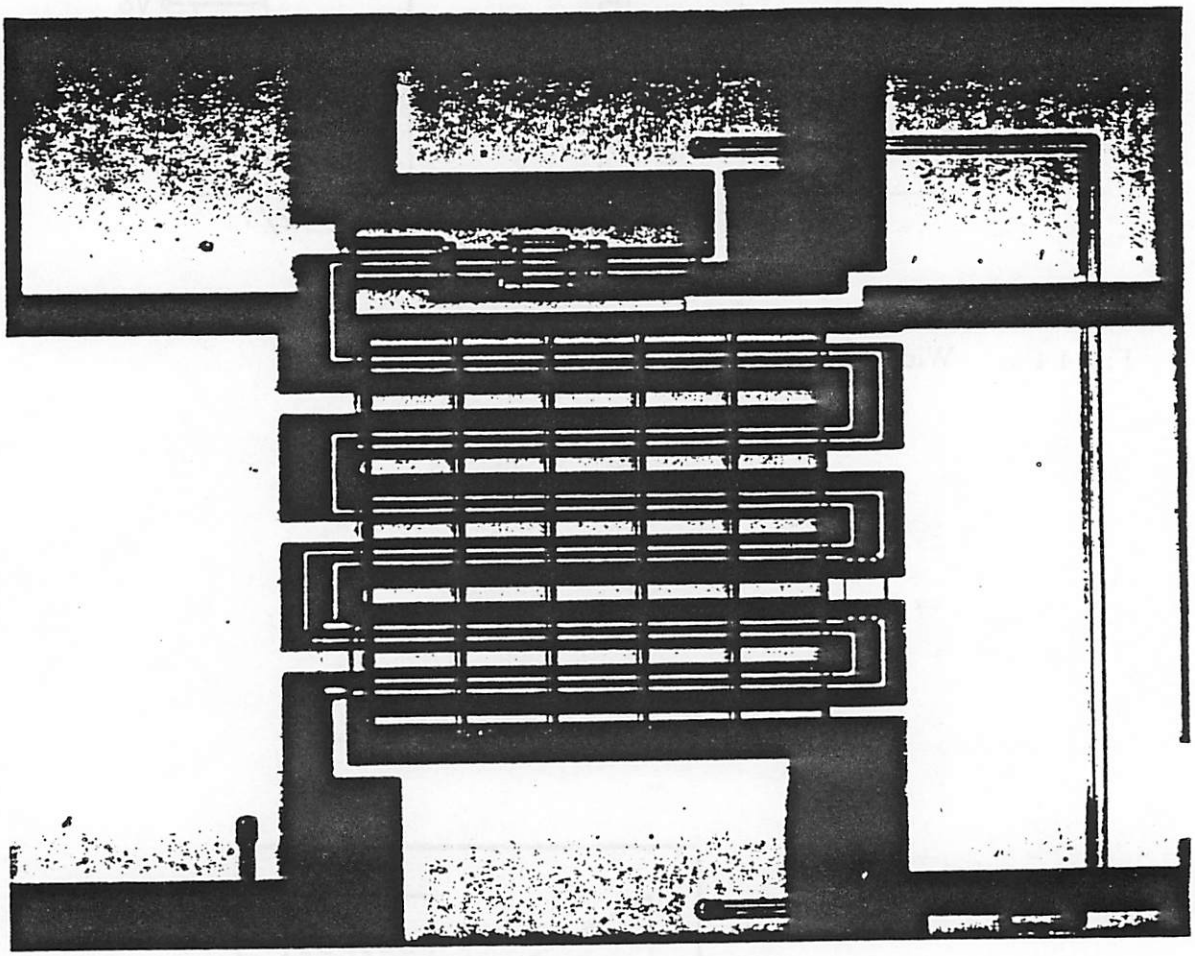


Fig. 4.6 Die-photo of the feedback amplifier and its output buffer.

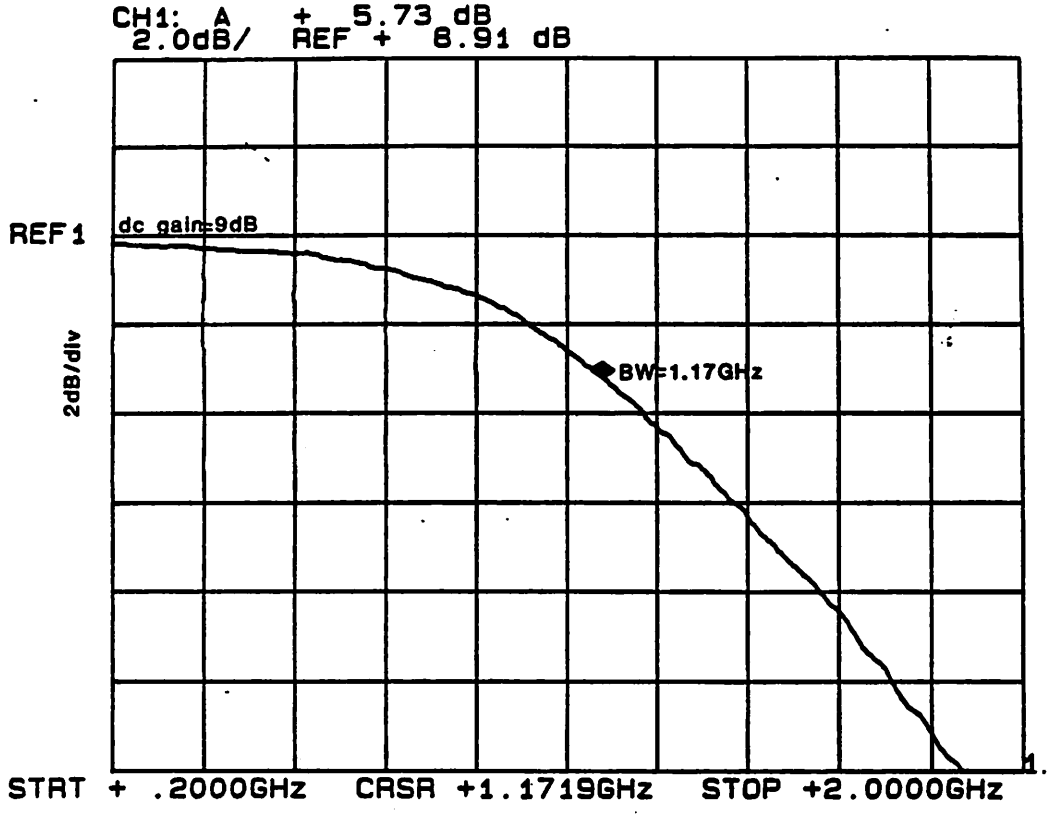


Fig. 4.7a Measured frequency response of the feedback amplifier.

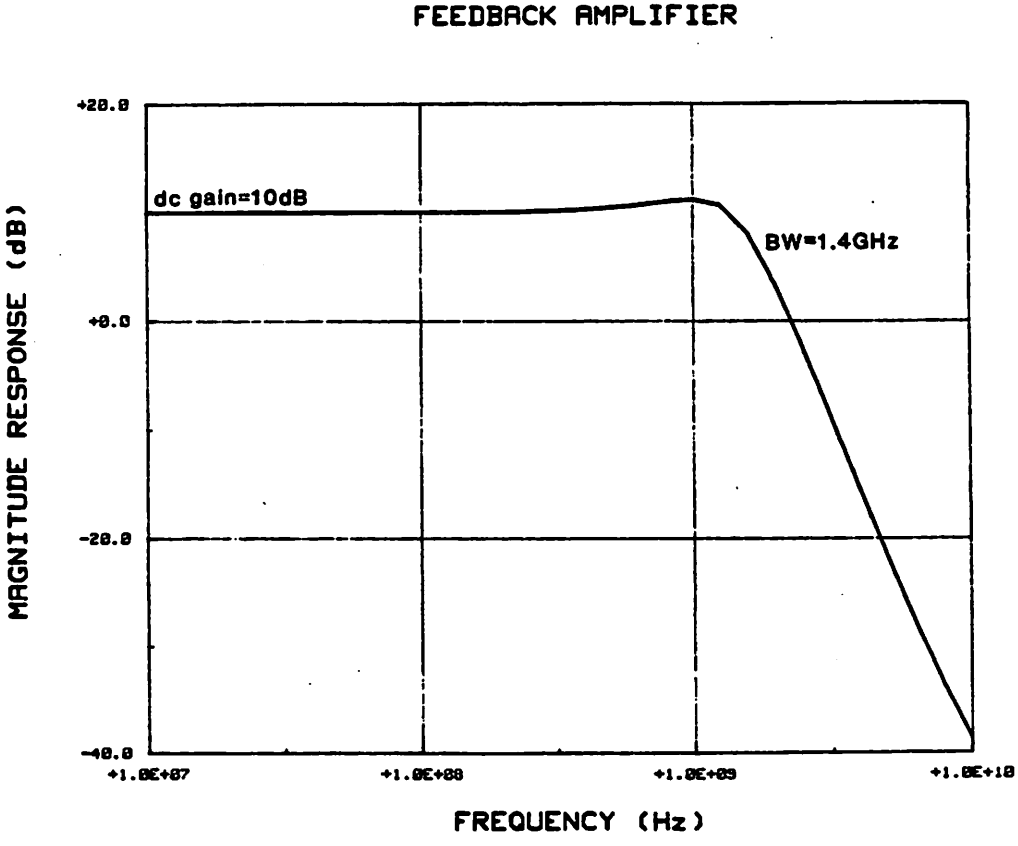


Fig. 4.7b Simulated frequency response of the feedback amplifier.

those of simulation because the actual channel length of the transistors is less than $1\mu m$. Because of this, the $g_m r_o$ of the transistors is lower than expected and the input capacitance of the output buffer is increased according to equation 2.15. This increases the capacitive loading at the amplifier output node where frequency limitation occurs.

Figure 4.8 is the measured noise figure of the feedback amplifier at room temperature. In this measurement, two feedback amplifiers and a 50Ω output buffer are connected in series. An external 50Ω resistor shunting the amplifier input to ground is used to guarantee 50Ω match. An HP-8970A noise figure meter which has a 50Ω terminal impedance is used in the measurement system. The measured 1/f noise corner is around 30MHz and the measured thermal noise component is 3dB above the SPICE simulated value shown in figure 2.33.

Since the measured amplifier performances correspond to simulated values using SPICE, the performances of the four amplifiers predicted in chapter 2 are reasonable. The configuration of this feedback amplifier is incorporated in the latched comparator of the next section.

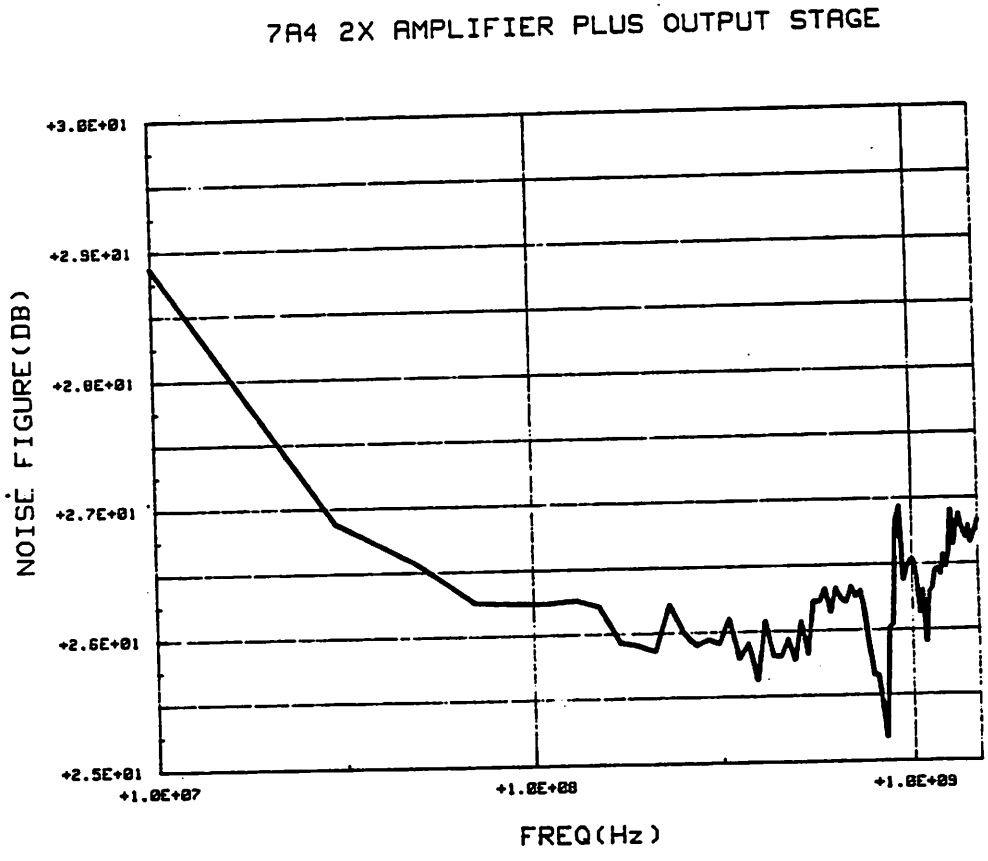


Fig. 4.8 Measured noise figure of the feedback amplifier.

4.3 A 750MS/s Latched Comparator

Based on the configuration of Comparator-IVc in section 3.5.3, a high-speed comparator has been designed, fabricated, and tested at high frequencies. This comparator was designed for application in a 4-bit flash A/D converter. The circuit schematic of the latched comparator is shown in figure 4.9. The preamplifier of this comparator (M_1 to M_{23}) is the differential version of the feedback amplifier in the last section. Compared to Comparator-IVc in figure 3.46, this design has the following minor modifications:

1 The gates of the feedback transistors M_{13} and M_{14} are connected to the drains of the second gain stage M_{19} and M_{20} instead of to the sources of the output source followers. This improves the phase margin of the feedback loop and the overshoot in the preamplifier step response is acceptable even if C_c equals zero.

2 The width of the transistor M_{15} to M_{25} is $5\mu m$ instead of $10\mu m$. This resulted in a reduction of dc power dissipation which is important since there are 15 comparators in a 4-bit flash A/D converter.

3 The bias voltages V_{b1} and V_{b2} are generated using replica biasing which are shared by the 15 comparators in a 4-bit flash A/D converter. The advantage of this biasing scheme over the original common-mode feedback biasing in figure 3.46 is that the dc power dissipation is reduced. The disadvantage is that the common-mode signal at the comparator outputs is more sensitive to the dc level of the clock ϕ_1 and ϕ_2.

4 The input stage of the latched comparator is a cascode configuration which is driven by an input *T/H* instead of an input *S/H* as in figure 3.46. The cascode transistors M_5 and M_6 are needed to isolate the drains of M_1 and M_2 from the feedback transistors M_{13} and M_{14} because the feedback signal can corrupt the input sample stored at the input capacitance of the differential pair.

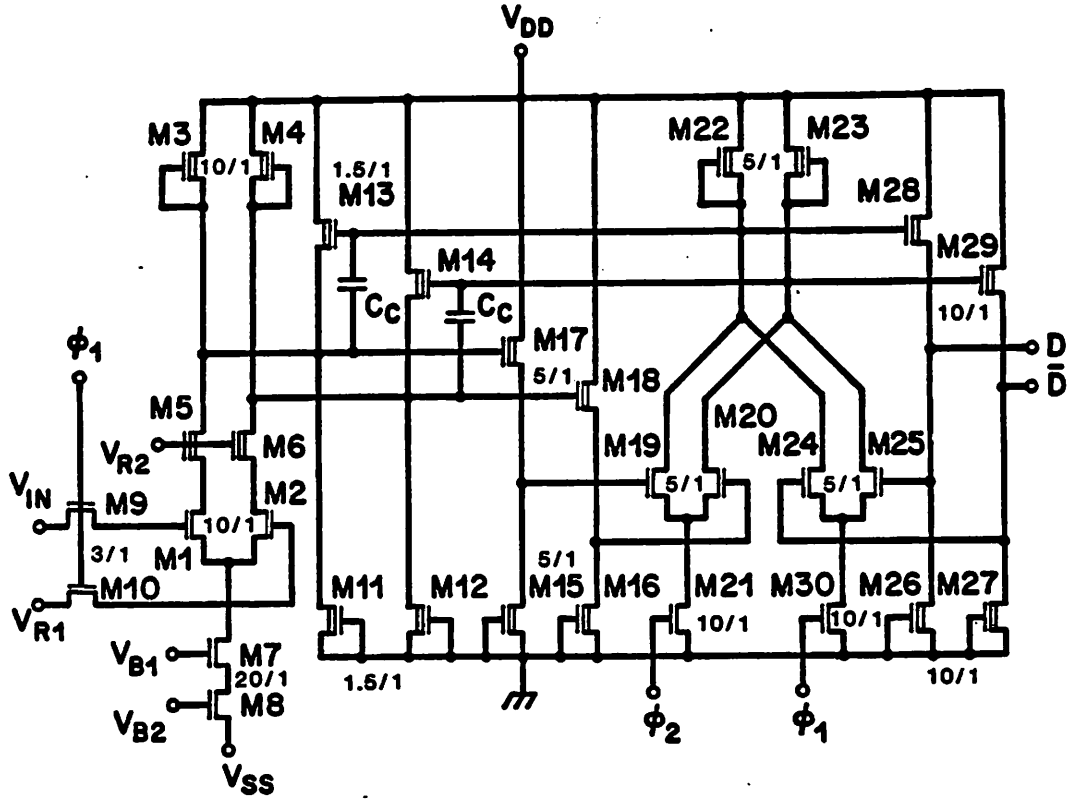


Fig. 4.9 Latched comparator.

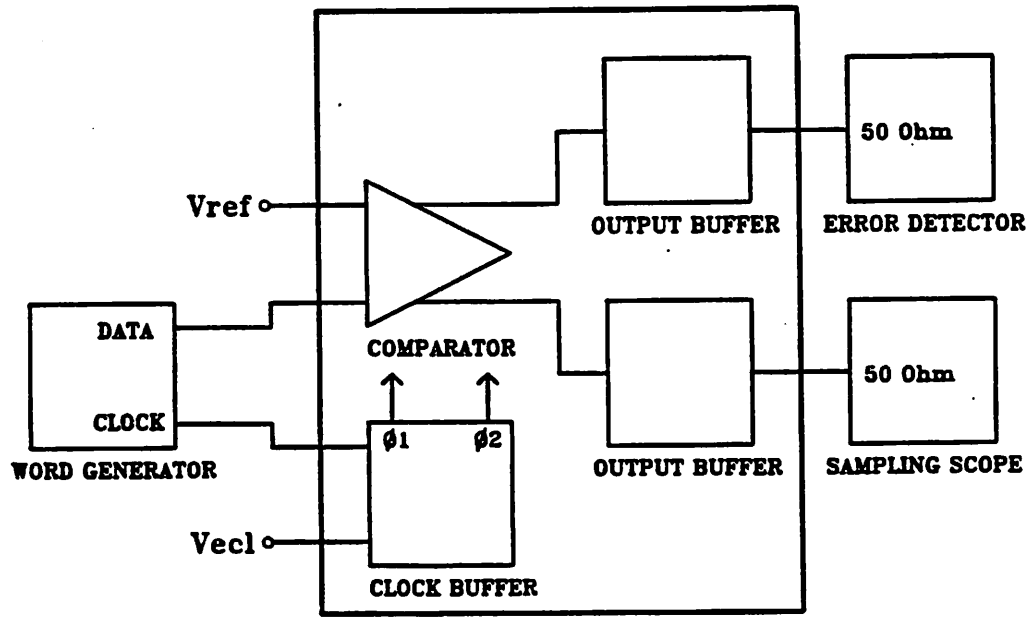


Fig. 4.10 Measurement setup for the latched comparator.

5 The two output S/H in figure 3.46 are removed from this test circuit to facilitate monitoring the waveform at the outputs of the positive feedback latch with 50Ω output buffers.

A test IC which integrates the high-speed comparator, two 50Ω output buffers and a clock buffer was fabricated. The measurement setup is shown in figure 4.10. The clock buffer generates the two-phase 50% duty clocks from a single ECL clock. The output buffer is similar to the 50Ω buffer in section 4.1 which drives off-chip 50Ω load. A 2Gbits/s pseudo-random pattern generator and an error detector are used to ensure that the error rate of the comparator is less than 10^{-9} during a measurement. A die-photo of the latched comparator is shown in figure 4.11.

The measured waveforms of the latched comparator at 250MS/s and 750MS/s are shown in figure 4.12. The upper trace is the input waveform which is a periodic NRZ (Non Return to Zero) data pattern (101100111000...). The center trace is the output waveform which has a 1Vp-p swing. The bottom trace is the system clock which controls the sampling rate of the comparator. Figure 4.12 clearly demonstrates the functionality of the comparator. An input over-drive voltage of $\pm 80mV$ (160mVp-p) is required when the comparator is sampling at 750MS/s. The measured input common-mode range of the comparator is $\pm 1.5V$. If a full-scale input voltage V_{fs} of 2.5V is assumed, this comparator achieves a 5-bit input resolution at 750MS/s. A measured eye-diagram at 750MS/s is shown in figure 4.13. Figure 4.14 summarized the measured input resolution at various sampling frequencies.

Computer simulation of the comparator test circuit in figure 4.10 shows that input resolution of this IC should be better than 6 bits at 750MS/s ($V_{lsb}=31mV$). After careful investigations, the problem can be traced to an unexpected error in the the layout of the actual test circuit. The actual width of transistor M_{21} and M_{30} is less than the desired value which is $10\mu m$. This degrades the regeneration speed of the latch (M_{24} and M_{25}) which can be seen from figure 4.12. At 750MS/s, the input of the comparator have to be over-driven with 80mV such that the output amplitude is large enough to drive the error detector which requires a 1Vp-p input signal.

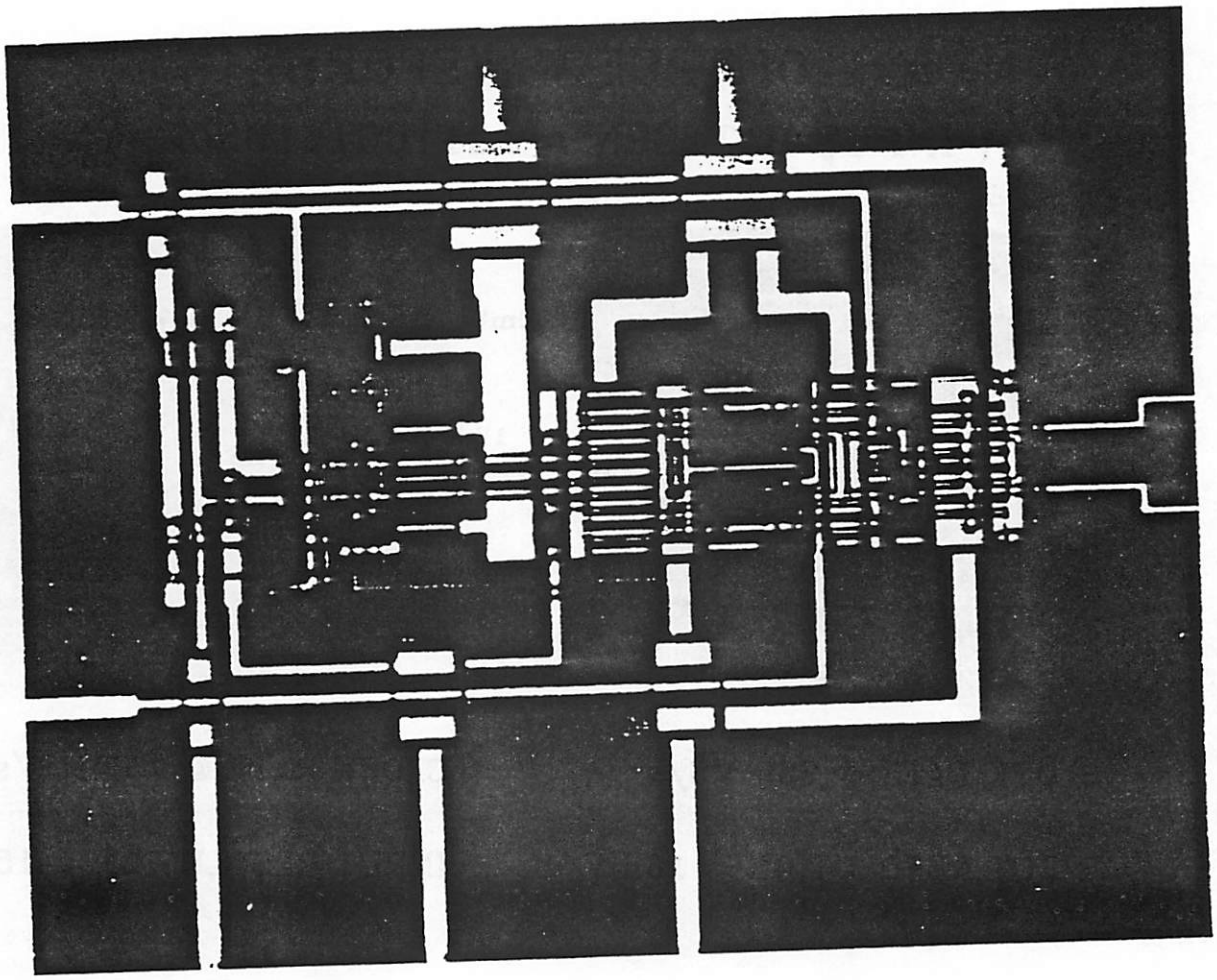


Fig. 4.11 Die-photo of the latched comparator.

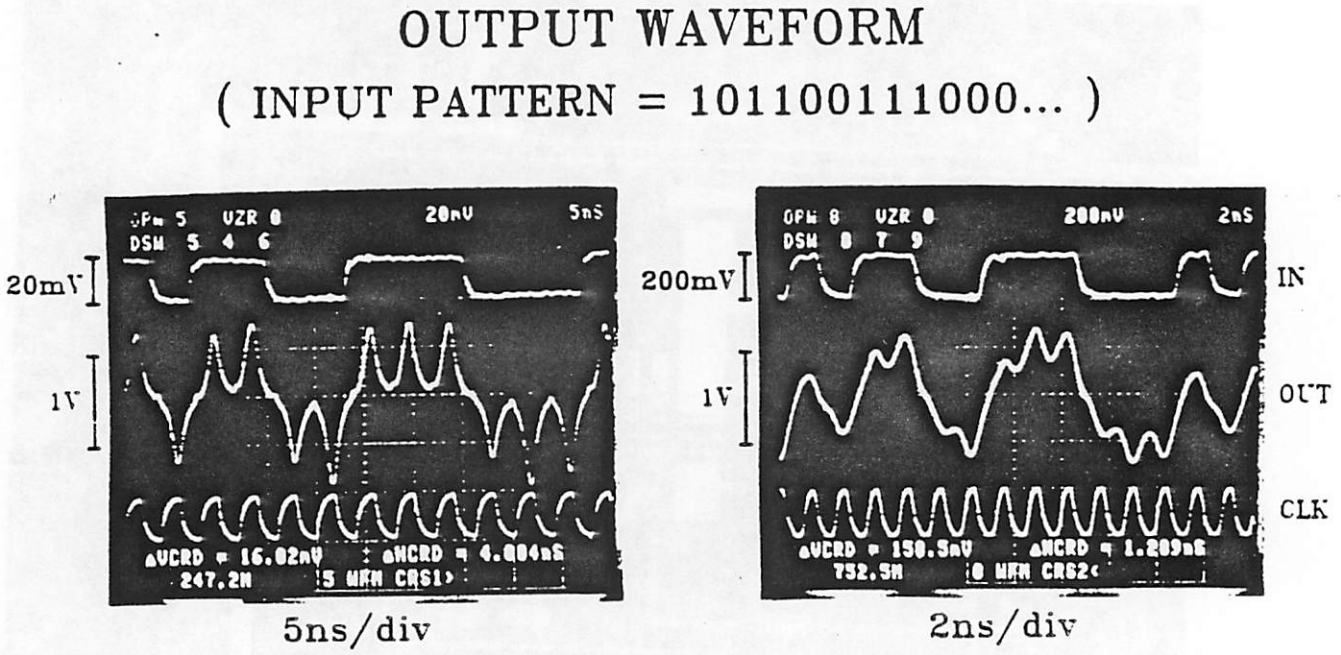


Fig. 4.12 Measured waveforms of the latched comparator at 250MS/s and 750MS/s.

OUTPUT EYE DIAGRAM AT 750 MS/s

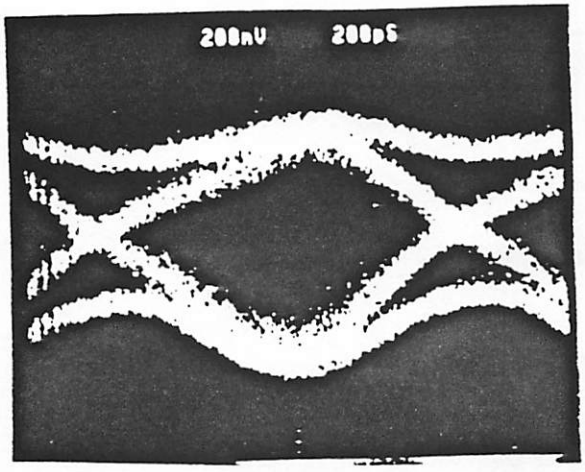


Fig. 4.13 Measured output eye-diagram at 750MS/s.

INPUT RESOLUTION (ERROR RATE < 1E−9)

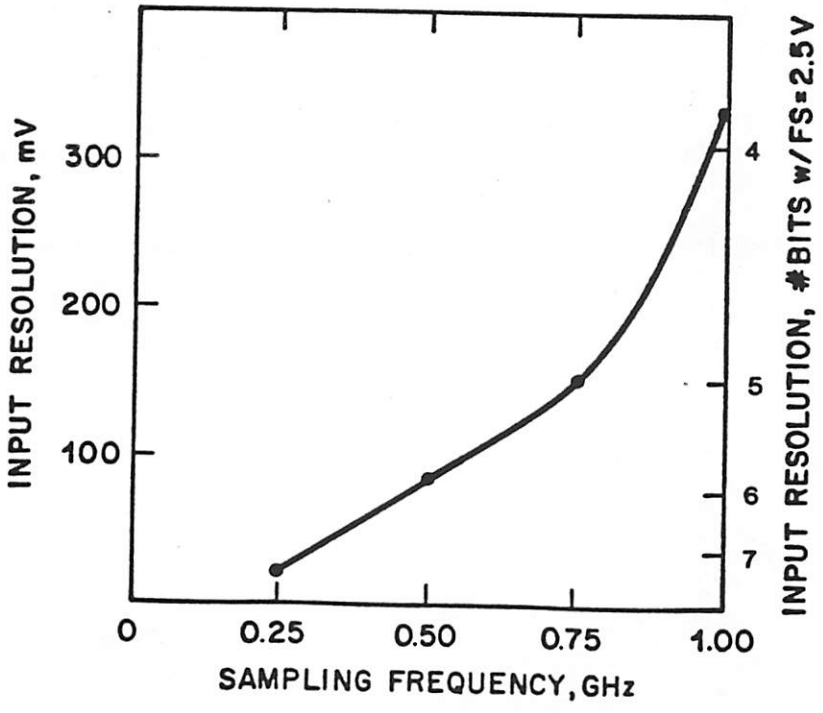


Fig. 4.14 Measured input resolution of the latched comparator.

Although the measured input resolution is 2.6 times lower than the simulated value, this performance is already the fastest ever reported for a MOS technology [34]. Based on Comparator-IVc, a 4-bit flash A/D converter is being designed. This A/D is expected to sample at 1GS/s.

Chapter 5 Conclusions

This research represents a comprehensive study on the design of wide-band amplifiers and high-speed voltage comparators in a 1μm NMOS technology. In particular, this work has contributed to the understanding and to the design philosophy behind high-speed voltage comparators. This study suggested that on-chip voltage amplification up to 2GHz and voltage comparison up to 1GS/s are possible, and that the short channel NMOS technology is suitable for realizing high-frequency but low resolution analog circuits such as 4-bit flash A/D converters and optical repeaters.

Experimentally, we have demonstrated a 1.17GHz bandwidth amplifier and a 750MS/s latched comparator. The amplifier has a voltage gain of 9dB when driving 120fF of on-chip capacitance (equivalent to a *fanout* of 5.) The comparator achieves 5 bits of input resolution at 750MS/s. Because this circuit employs a differential S/H at the input to define the sampling time, sampling ambiguity or phase jitter of the comparator is only a function of the phase noise in the clock. Since the bandwidth of the S/H is about 3GHz, it is not necessary to band-limit the input signal to below the Nyquist frequency. Power dissipation for a single comparator is about 35mW, and therefore a 4-bit flash A/D employing this comparator design is expected to dissipate less than 1.5W of power.

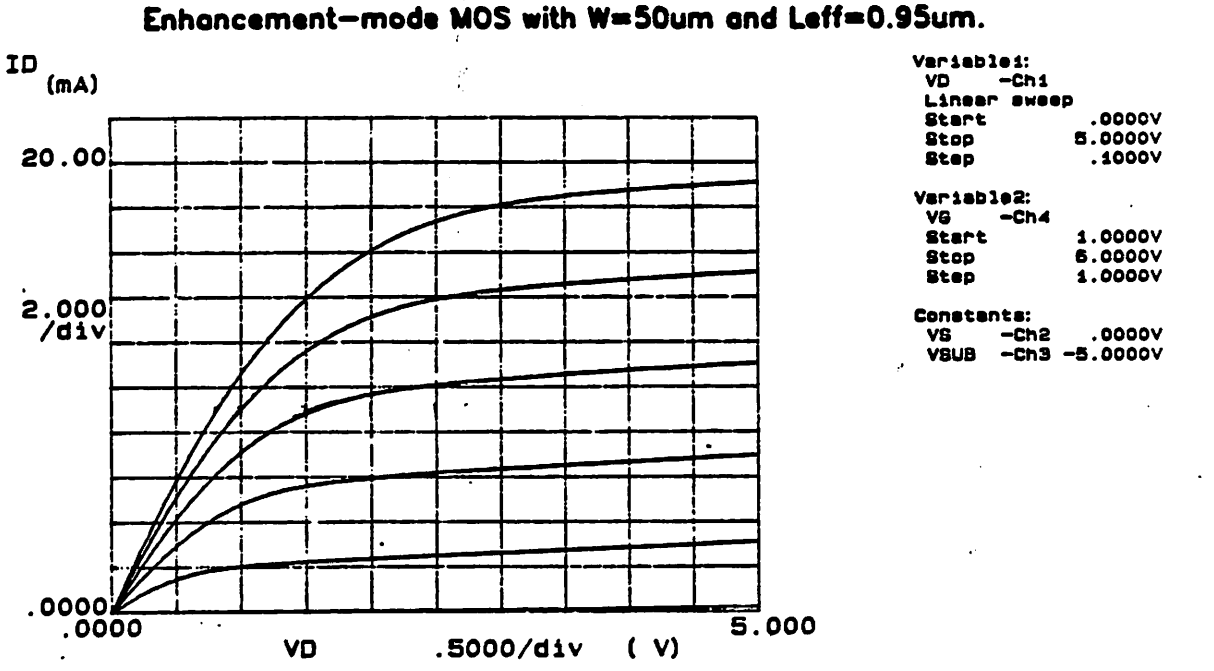
Because of the low transistor gain $g_m r_o$, it is difficult to design highly accurate wide-band amplifiers (chapter 2) or high-speed operational amplifiers in this technology. The situation in CMOS is slightly better because the cascode configuration can be used to obtain higher voltage gain in a single stage. Conventional MOS analog circuits such as switched-capacitor filters and charge-redistribution A/D converters are more easily implemented in a CMOS technology. However, as channel length is reduced to improve transistor f_T, $g_m r_o$ decreases dramatically in this technology also. In order to ensure an op-amp gain larger than 80dB, a triple or even quadruple CMOS cascode may have to be used. This approach may render the op-amp useless in terms of common-mode range. Since the $g_m r_o$ of a scaled bipolar transistor can easily exceed 500, it would only seem natural to merge bipolar and MOS into one technology. Having both high current gain (for S/H) and

high voltage gain (for op-amp), perhaps BiCMOS is the logical technology for high-frequency and high-resolution analog circuits.

A-1 Measured Transistor DC Characteristics and Capacitances

In this appendix, measured dc characteristics of the enhancement and depletion mode $1\mu m$ MOS transistor are presented. The enhancement and the depletion threshold voltages are 1V and -1.5V, respectively. The drawn channel width is $50\mu m$ and the measured effective channel length is $0.95\mu m$ for both transistors. The gate oxide was measured to be $0.02\mu m$ thick.

Figures A-1a and A-1b show the I-V characteristics of the two transistors. In figure A-2, measured saturation current (I_{dsat}) versus V_{gs} is plotted along with the transistor tranconductance (g_m). From figure A-2a, maximum transistor g_m is about $88mS/mm$. In figure A-3, measured output resistance (r_o) of the two transistors is presented. Figure A-4 is the measured back-gate transconductance (g_{mb}) of the two devices. Figure A-5, is the measured transistor capacitance [13] at various bias voltages. The cross-section of a typical MOS transistor is shown in figure A-6 illustrating intrinsic device and parasitic capacitances. Finally, all important measured device and parasitic parameters are summarized in Table A-1 where the transistor operating point is assumed to be at $V_{GS}-V_T=1.5V$ and $V_{DS}=2.5V$.



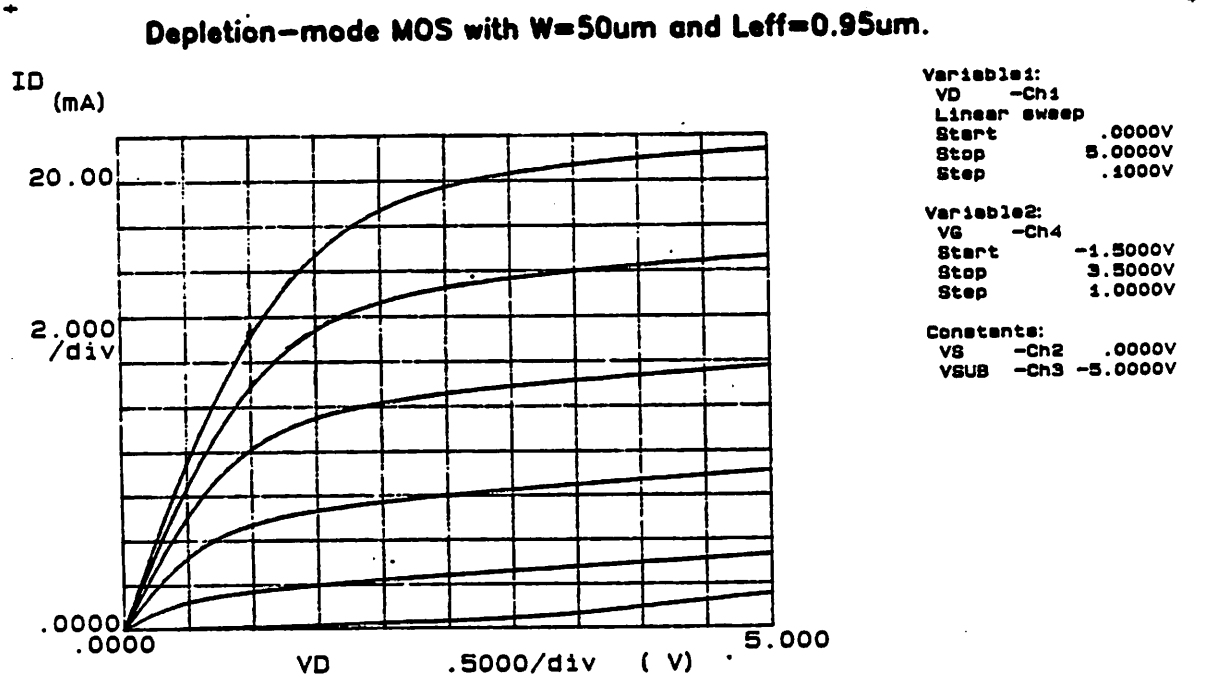
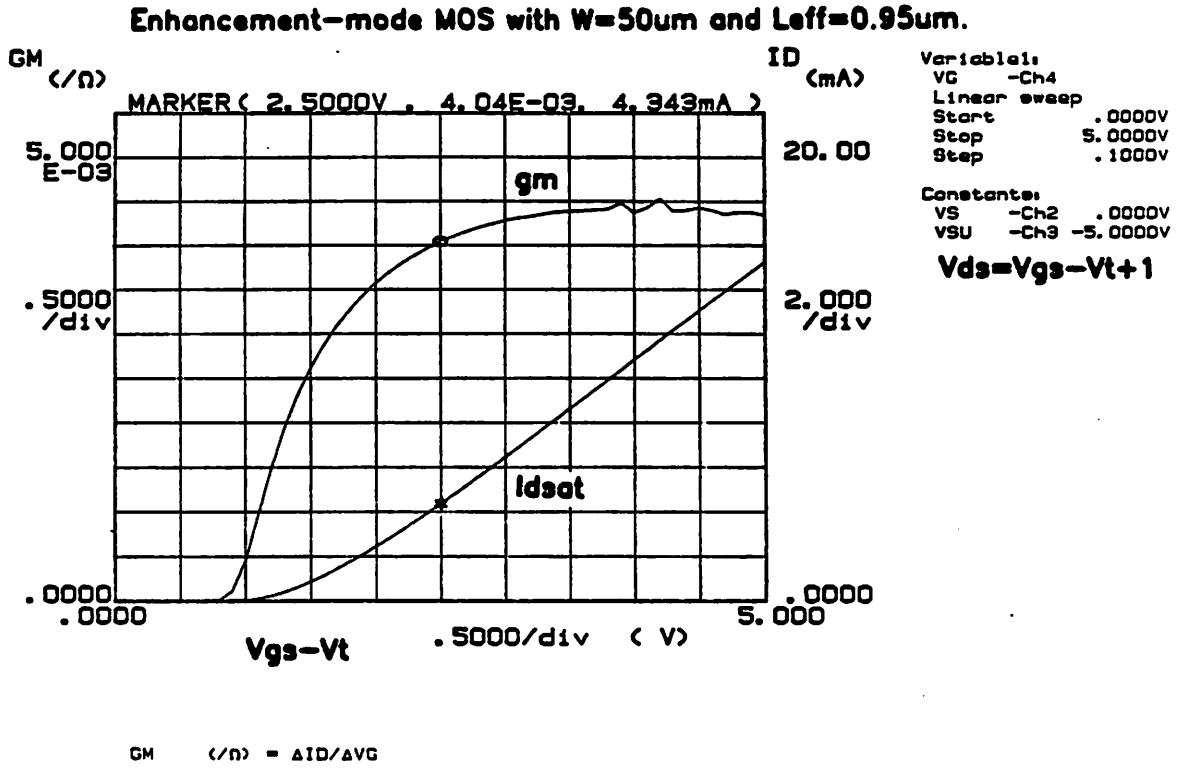


Fig. A-1 Measured transistor I-V characteristics.



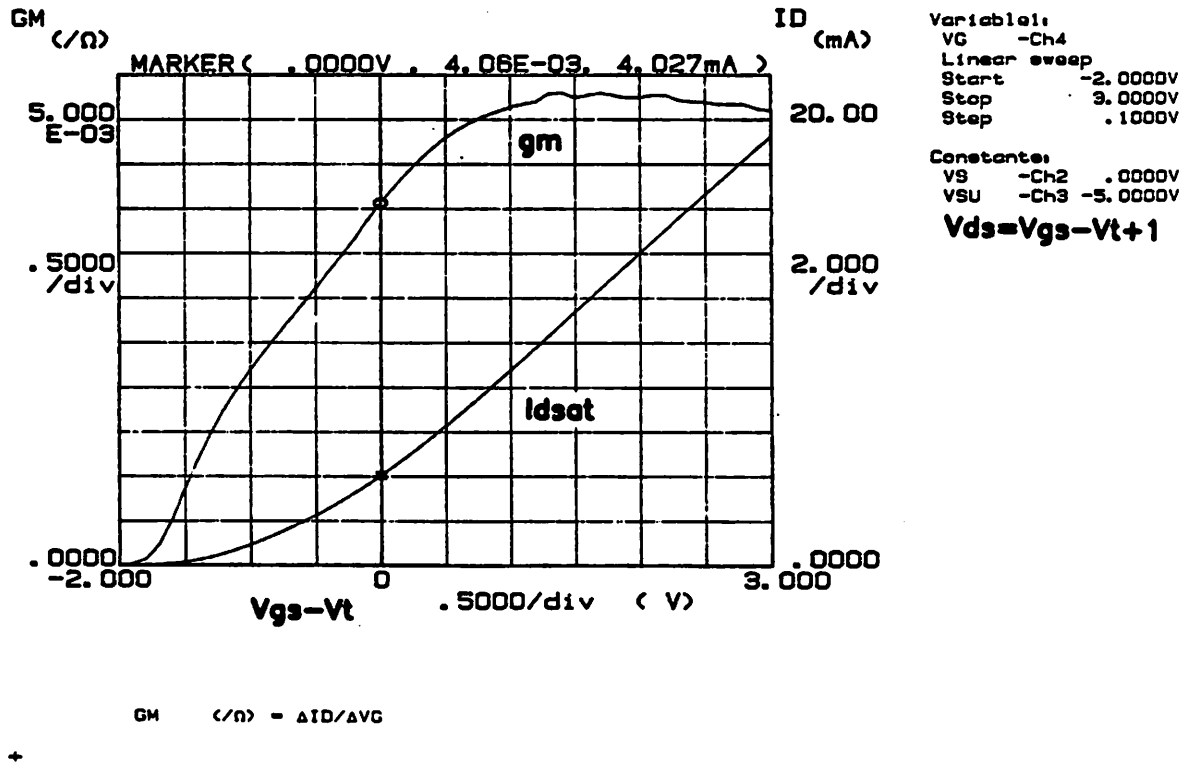
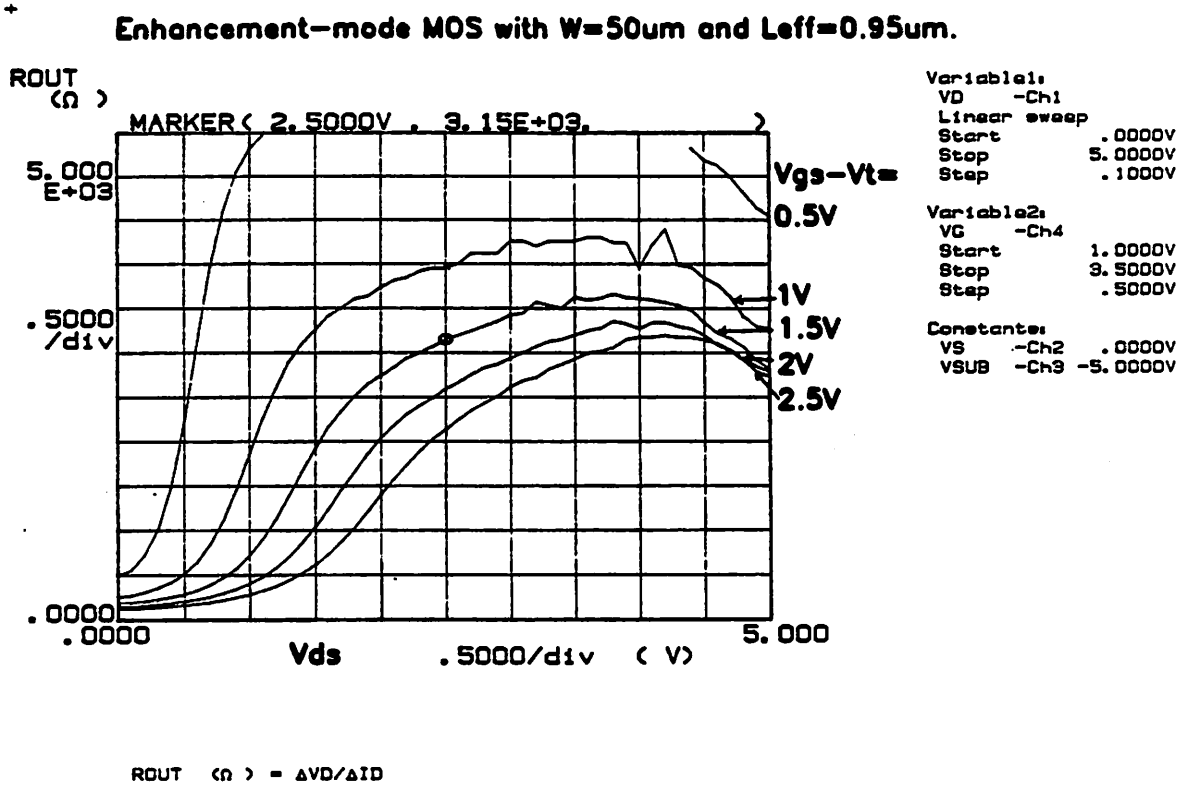


Fig. A-2 Measured transistor transconductance and saturation current.



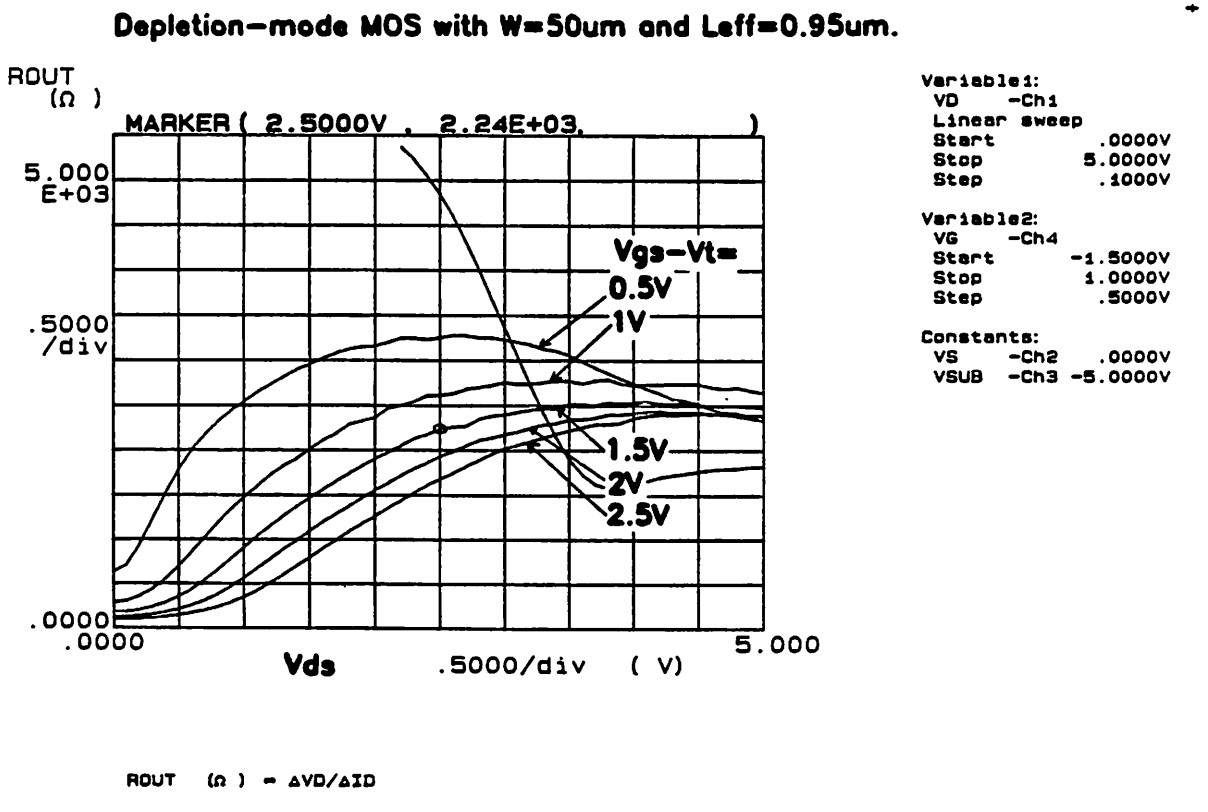
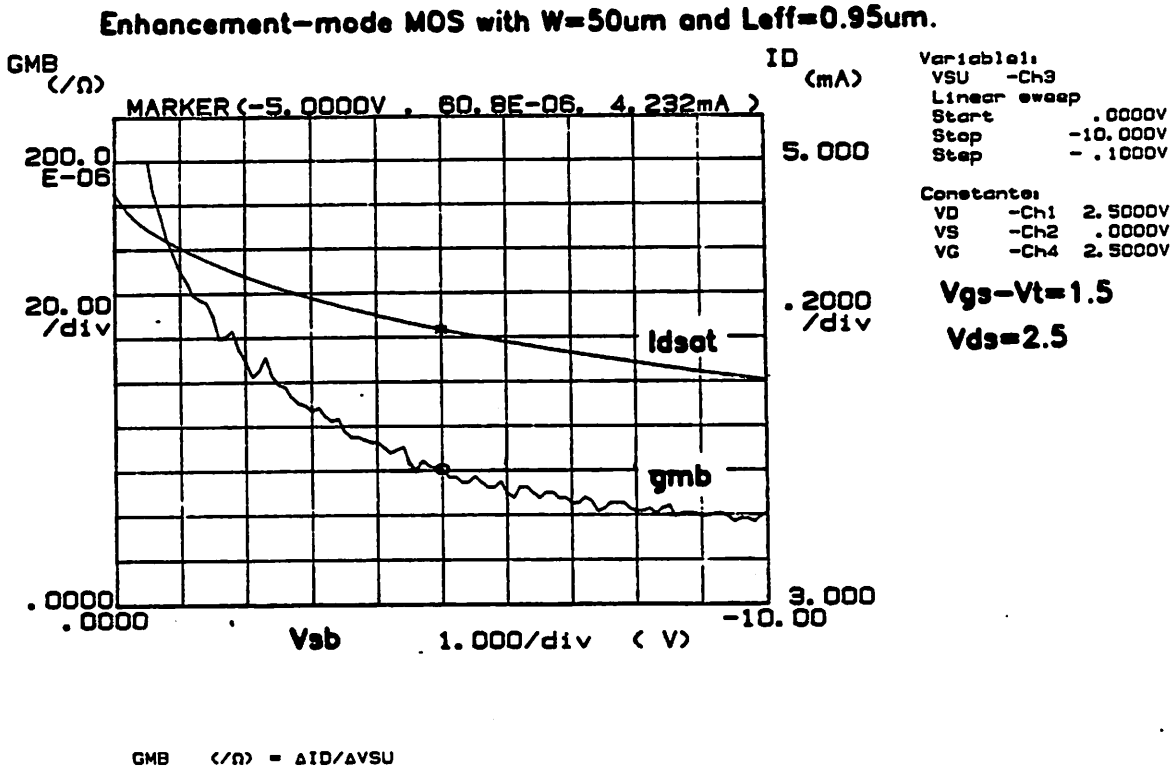


Fig. A-3 Measured transistor output resistance.



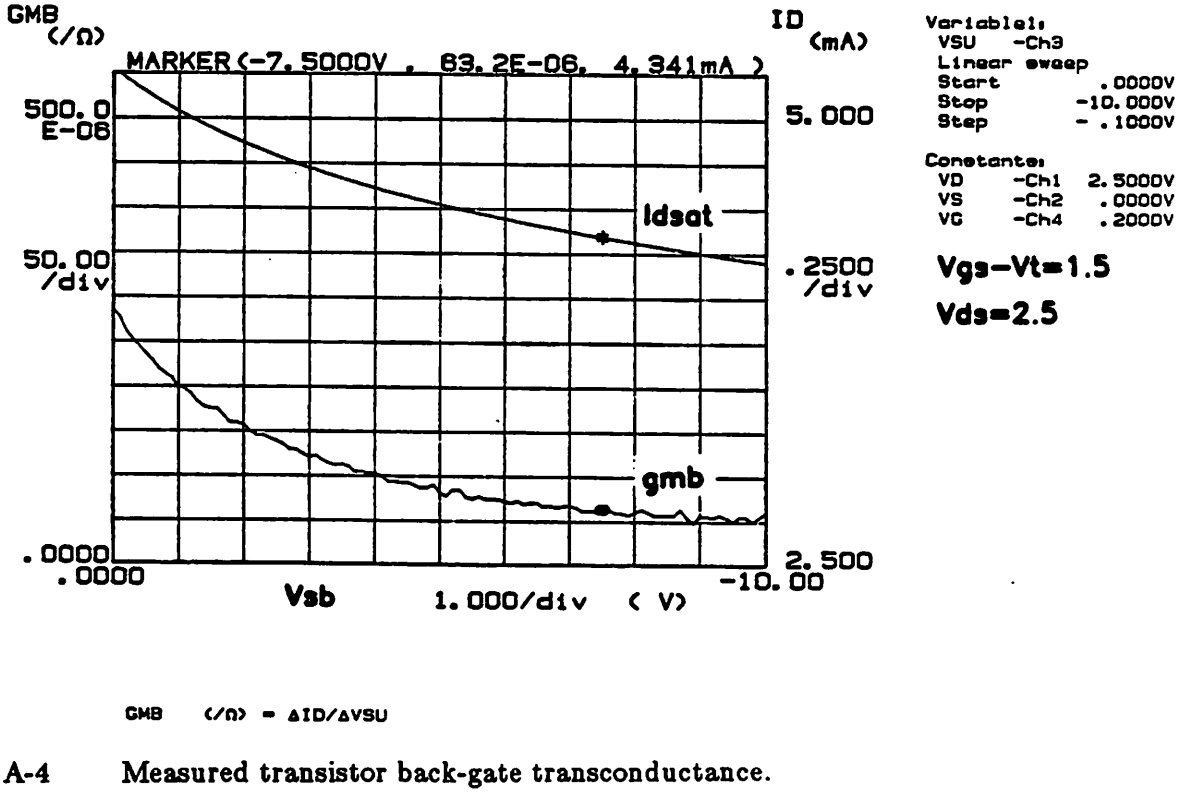


Fig. A-4 Measured transistor back-gate transconductance.

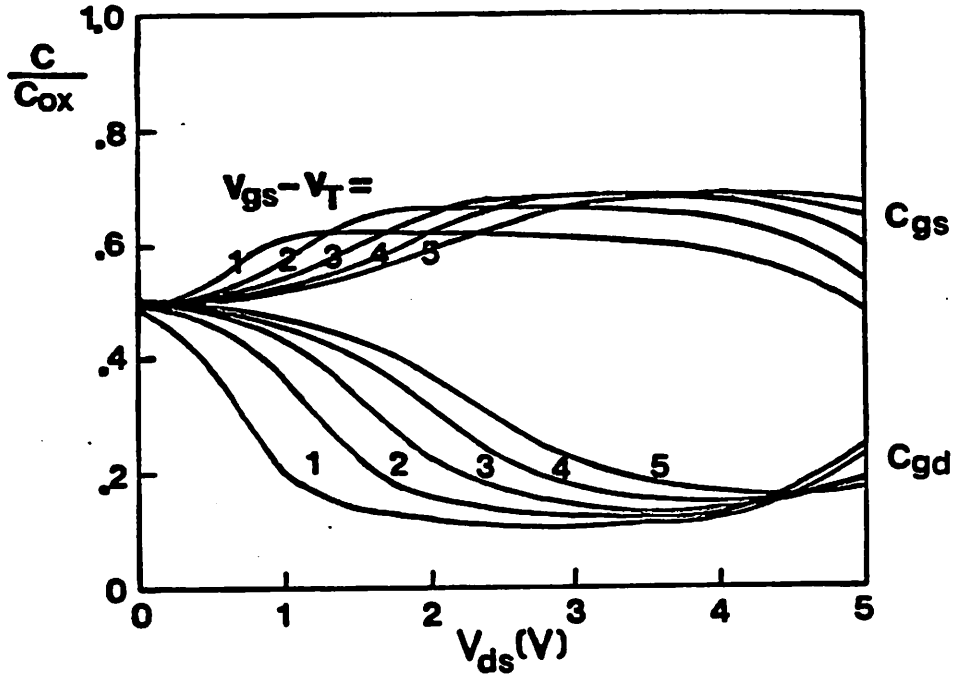


Fig. A-5 Measured normalized transistor capacitance.

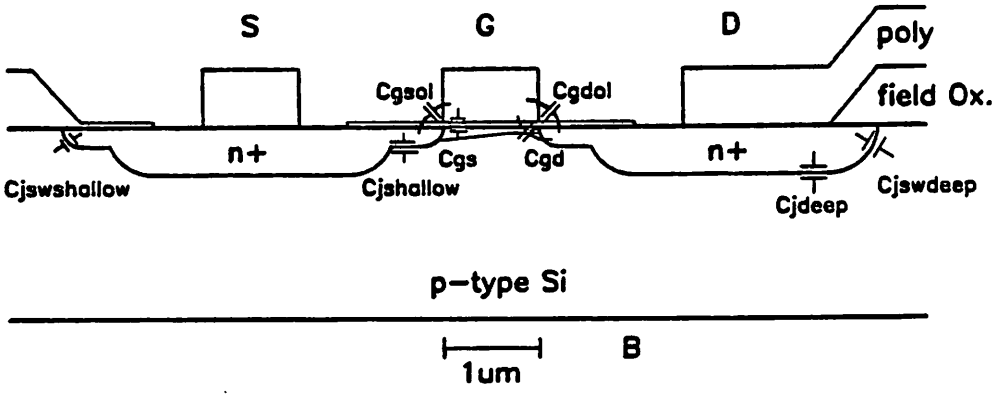


Fig. A-6 Cross section of a MOS transistor showing parasitic and intrinsic capacitances.

Parasitic Capacitances		Device Capacitances	
C field	0.057 fF/um^2	Cox	1.7 fF/um^2
Cj deep	0.11 fF/um^2	Cgs	1.05 fF/um *
Cjsw deep	0.5 fF/um	Cgsol	0.15 fF/um
Cj shallow	0.45 fF/um^2	Cgd	0.2 fF/um *
Cjsw shallow	0.6 fF/um	Cgdol	0.15 fF/um

* Leff=1um Vgs−Vt=1.5V Vds=2.5V

Table A−1a Summary of Parasitic and Device Capacitances.

	Enhancement	Depletion
gm	78 mS/mm	81 mS/mm
ro	157 ohm•mm	112 ohm•mm
gmb	1.2 mS/mm	1.26 mS/mm
Vt	1 V	−1.5 V

Vgs−Vt=1.5V Vds=2.5V Vsb=−5V Leff=1um

Table A−1b Summary of Measured Device Small Signal DC Parameters.

A-2 Spice MOS Level-III Input Parameters

Computer simulation is a powerful tool in integrated circuit design, especially for high frequency circuits which are essentially impossible to breadboard. In this research, the circuit simulation program SPICE version 2G.5 was used. The accuracy of the transistor model used in Spice deserves some attention.

In SPICE version 2G.5, there are three MOS transistor models. Models 1 and 2 are for long channel MOS transistors, and are not applicable to our situation. Although MOS level-III model [12] was intended for channel lengths below $2\mu m$, parameters used in the model have to be changed from their measured or extracted values before good fitting results are obtained.

Using selected values for μ_o, θ, and v_{max} in model-III, the simulated drain current can be made to fit well in the triode region. However in the saturation region, the simulated drain current does not fit measured device I-V characteristics. Device output conductance is controlled by two model parameters, KAPPA and ETA. KAPPA is used to model the channel shortening effect and ETA is used in the electro-static feedback model. Best fit model for the E-device is presented in figure B-1, with the input model parameters and small-signal table listed in table B-1. Measured device I-V characteristics are also included for comparison. With ETA=0.18 and KAPPA=0, level-III seems to generate good overall fit. Unfortunately a programming error exists in the electro-static feedback model which causes the output conductance r_o in the extracted small signal table to be much smaller than that obtained from large signal dc analysis. This causes serious problems in ac analysis. To bypass the problem for ac analysis, Eta is set to zero and KAPPA is used to fit the output conductance around the desired operating point ($V_{GS}-V_T=1.5V$ and $V_{DS}=2.5V$). Figure B-2 is the best fit result when KAPPA=0.8 is used. Notice that output conductance is overestimated at high $V_{GS}-V_T$. Simulated I-V curves for the depletion device using either ETA or KAPPA is shown in figure B-3 and B-4 respectively. Tables B-3 and B-4 contain the corresponding input model parameters

and small-signal table.

In conclusion, the MOS input model parameters summarized in table B-2 and B-4 are used in small signal ac analysis so that the extracted small signal model has the correct value for r_o. However, when doing dc analysis and transient analysis, the parameters in table B-1 and B-3 can be used to give better overall simulation results.

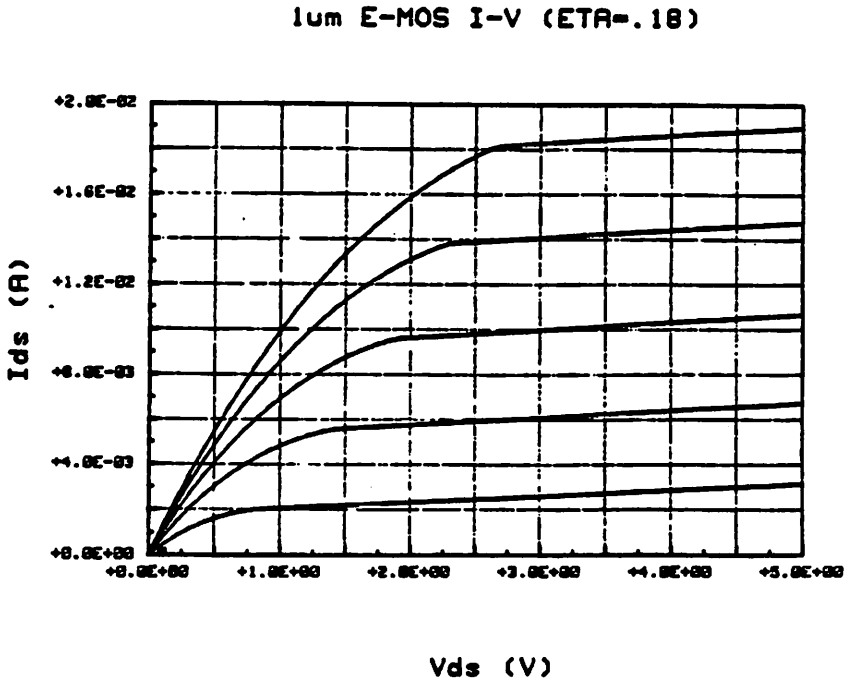


Fig. B-1 Simulated E-device I-V characteristic using MOS level-3 with ETA=0.18.

Model Card:

```
.MODEL MENH NMOS (LEVEL=3 VTO=.76 CGSO=150P CGDO=300P CGBO=138P
+ RSH=15 CJ=170U CJSW=500P TOX=.02U NSUB=2E16 XJ=.2U LD=.15U UO=700
+ VMAX=1.30E5 NFS=1E10 THETA=.116 KAPPA=0 GAMMA=.235 XQC=.27 ETA=.18
+ AF=1 KF=6E-28
```

Operating Point Information:

0**** MOSFETS

0	M1	M2	M3	M4	M5	M6
0MODEL	MENH	MENH	MENH	MENH	MENH	MENH
ID	2.46e-03	5.92e-03	9.81e-03	1.39e-02	1.77e-02	4.12e-03
VGS	2.000	3.000	4.000	5.000	6.000	2.500
VDS	2.500	2.500	2.500	2.500	2.500	2.500
VBS	-5.000	-5.000	-5.000	-5.000	-5.000	-5.000
VTH	0.795	0.805	0.817	0.829	0.840	0.800
VDSAT	0.870	1.288	1.603	1.867	2.106	1.098
GM	3.41e-03	4.12e-03	4.42e-03	4.57e-03	3.74e-03	3.85e-03
GDS	2.73e-05	3.94e-05	4.80e-05	5.50e-05	3.39e-03	3.40e-05
GMB	9.97e-05	1.24e-04	1.37e-04	1.45e-04	1.30e-04	1.14e-04
CBD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CBS	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGSOVL	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15
CGDOVL	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14
CGBOVL	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16
CGS	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.75e-14	5.76e-14
CGD	0. e+00	0. e+00	0. e+00	0. e+00	2.09e-15	0. e+00
CGB	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00

Extracted output conductance GDS is too small when compared with .dc output in figure B-1!

Table B-1 Spice .MODEL Card and Operating Point Informations with ETA=0.18.

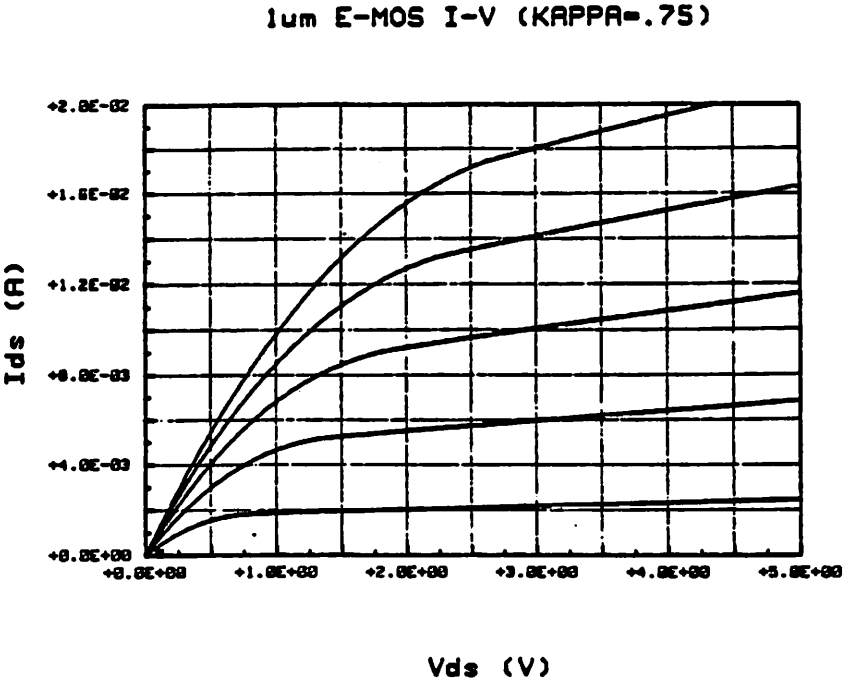


Fig. B-2 Simulated E-device I-V characteristic using MOS level-3 with KAPPA=0.75.

Model Card:

```
.MODEL MENH NMOS (LEVEL=3 VTO=.76 CGSO=150P CGDO=300P CGBO=138P
+ RSH=15 CJ=170U CJSW=500P TOX=.02U NSUB=2E16 XJ=.2U LD=.15U UO=700
+ VMAX=1.30E5 NFS=1E10 THETA=.116 KAPPA=.75 GAMMA=.235 XQC=.27
+ AF=1 KF=6E-28
```

Operating Point Information:

0**** MOSFETS

0	M1	M2	M3	M4	M5	M6
0MODEL	MENH	MENH	MENH	MENH	MENH	MENH
ID	2.10e-03	5.75e-03	9.66e-03	1.35e-02	1.72e-02	3.85e-03
VGS	2.000	3.000	4.000	5.000	6.000	2.500
VDS	2.500	2.500	2.500	2.500	2.500	2.500
VBS	-5.000	-5.000	-5.000	-5.000	-5.000	-5.000
VTH	1.001	1.002	1.004	1.005	1.007	1.001
VDSAT	0.758	1.213	1.546	1.821	2.066	1.007
GM	3.44e-03	4.18e-03	4.28e-03	4.19e-03	3.81e-03	3.94e-03
GDS	1.54e-04	4.94e-04	9.13e-04	1.39e-03	2.80e-03	3.11e-04
GMB	1.00e-04	1.26e-04	1.35e-04	1.37e-04	1.31e-04	1.17e-04
CBD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CBS	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGSOVL	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15
CGDOVL	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14
CGBOVL	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16
CGS	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.75e-14	5.76e-14
CGD	0. e+00	0. e+00	0. e+00	0. e+00	1.27e-15	0. e+00
CGB	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00

Output Conductance at large Vgs-Vt is overestimated by the model.

Table B-2 Spice .MODEL CARD and Operating Point Informations with KAPPA=0.75.

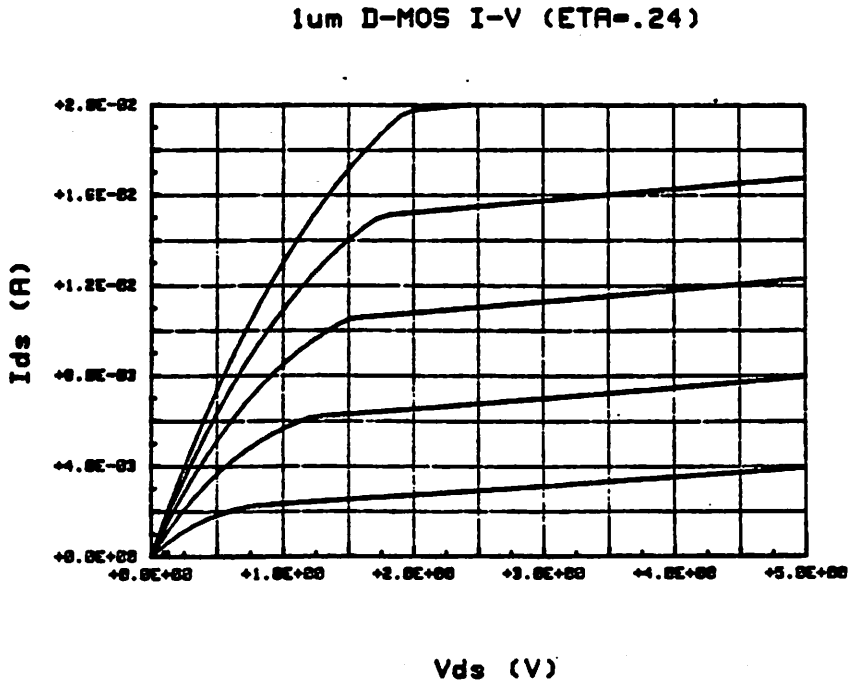


Fig. B-3 Simulated D-device I-V characteristic using MOS level-3 with ETA=0.24.

Model Card:

```
.MODEL MDEP NMOS (LEVEL=3 VTO=-1.74 CGSO=150P CGDO=300P CGBO=138P
+ RSH=15 CJ=170U CJSW=500P TOX=.02U NSUB=2E16 XJ=.2U LD=.15U UO=740
+ VMAX=1.2E5 NFS=1E10 THETA=0 KAPPA=0 GAMMA=.235 XQC=.27  ETA=.24
+ AF=1 KF=6E-28
```

Operating Point Information:

0**** MOSFETS

0	M1	M2	M3	M4	M5	M6
0MODEL	MDEP	MDEP	MDEP	MDEP	MDEP	MDEP
ID	2.91e-03	6.76e-03	1.10e-02	1.55e-02	2.00e-02	4.76e-03
VGS	-0.500	0.500	1.500	2.500	3.500	0.
VDS	2.500	2.500	2.500	2.500	2.500	2.500
VBS	-5.000	-5.000	-5.000	-5.000	-5.000	-5.000
VTH	-1.772	-1.758	-1.741	-1.724	-1.707	-1.765
VDSAT	0.818	1.078	1.217	1.302	1.358	0.970
GM	3.86e-03	4.56e-03	4.84e-03	4.96e-03	5.03e-03	4.30e-03
GDS	4.37e-05	4.80e-05	4.46e-05	3.98e-05	3.54e-05	4.76e-05
GMB	1.05e-04	1.21e-04	1.27e-04	1.28e-04	1.29e-04	1.15e-04
CBD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CBS	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGSOVL	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15
CGDOVL	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14
CGBOVL	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16
CGS	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.76e-14
CGD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGB	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00

Extracted output conductance GDS is too small when compared with .dc output in figure B-11

Table B-3 Spice .MODEL Card and Operating Point Informations with ETA=0.24.

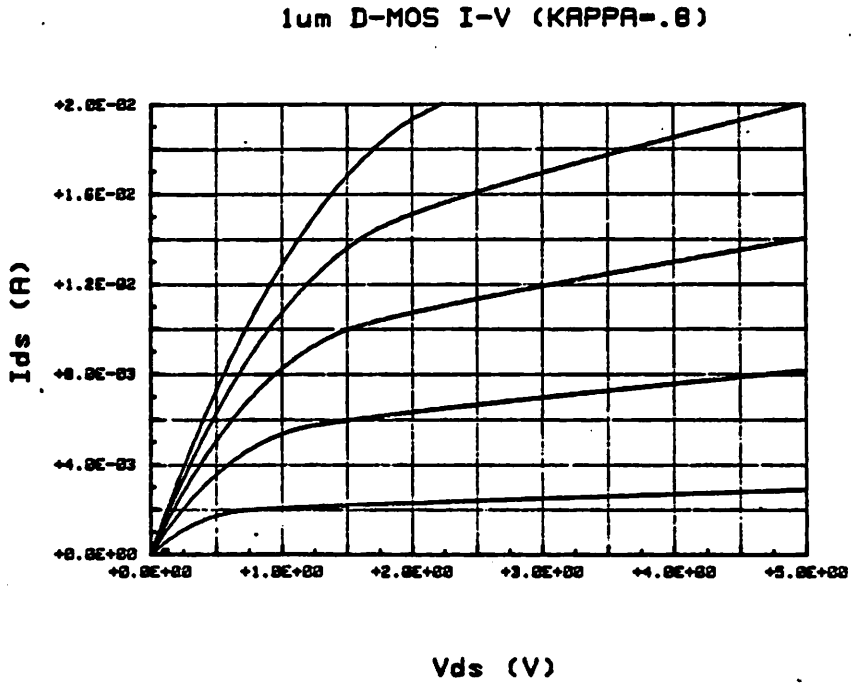


Fig. B-4 Simulated D-device I-V characteristic using MOS level-3 with KAPPA=0.8.

Model Card:

```
.MODEL MDEP NMOS (LEVEL=3 VTO=-1.74 CGSO=150P CGDO=300P CGBO=138P
+. RSH=15 CJ=170U CJSW=500P TOX=.02U NSUB=2E16 XJ=.2U LD=.15U UO=740
+ VMAX=1.2E5 NFS=1E10 THETA=0 KAPPA=.8 GAMMA=.235 XQC=.27  ETA=0
+ AF=1 KF=6E-28
```

Operating Point Information:

0**** MOSFETS

0	M1	M2	M3	M4	M5	M6
0MODEL	MDEP	MDEP	MDEP	MDEP	MDEP	MDEP
ID	2.39e-03	6.66e-03	1.13e-02	1.61e-02	2.07e-02	4.43e-03
VGS	-0.500	0.500	1.500	2.500	3.500	0.
VDS	2.500	2.500	2.500	2.500	2.500	2.500
VBS	-5.000	-5.000	-5.000	-5.000	-5.000	-5.000
VTH	-1.499	-1.497	-1.495	-1.494	-1.492	-1.498
VDSAT	0.703	1.022	1.186	1.283	1.346	0.891
GM	4.01e-03	5.03e-03	5.31e-03	5.37e-03	5.33e-03	4.68e-03
GDS	2.17e-04	7.01e-04	1.32e-03	2.04e-03	2.90e-03	4.38e-04
GMB	1.10e-04	1.35e-04	1.40e-04	1.40e-04	1.37e-04	1.27e-04
CBD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CBS	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGSOVL	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15	7.50e-15
CGDOVL	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14	1.50e-14
CGBOVL	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16	1.38e-16
CGS	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.76e-14	5.76e-14
CGD	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00
CGB	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00	0. e+00

Output Conductance at large Vgs-Vt is overestimated by the model.

Table B-4 Spice .MODEL CARD and Operating Point Informations with KAPPA=0.8.

A-4 SIGMOS Design Rules

The photolithographic capability of the SiGMOS process assumes a minimum line width of $1.5\mu m$ and a minimum line spacing of $1.5\mu m$. Alignment tolerance between different mask levels is $0.75\mu m$. Based on these figures, the design rules of the SiGMOS technology are summarized in table D-1. The symbols used in the table are explained as follows:

Wx: width of x

Sxy: separation between x and y

Exy: extension of x over y

a: active area, or thin oxide region

b: buried contact

c: metal contact (first layer)

g: poly gate (and buried contact poly)

i: implant

m: metal

v: via hole above field oxide only

SIGMOS DESIGN RULES		
FEATURES	MIN. DIMENSIONS	
	(um)	(λ)
Wa	1.5	3
Wc	1.5	3
Wg	1.5	3
Wm1	1.5	3
Wm2	5.0	10
Wv	2.25	4.5
Saa	5.0	10
Sam	1.5	3
Scc	1.5	3
Sga	1.5	3
Sgg	1.5	3
Smm1	1.5	3
Smm2	4.0	8
Svv	3.0	6
Eba	1.5	3
Ebg	0.5	1
Ega	1.5	3
Egc	0.75	1.5
Eia	1.5	3
Eig	1.5	3
Emc	0.75	1.5
Emv	1.5	3

$\lambda = 0.5\ u$

Table D-1 SiGMOS design rules.

A-5 A Transient Analysis Program - Program A−5.

Program A−5 performs a transient analysis on the circuit in figure 3.9. It was written in BASIC for the HP-9836 computer. The program is based on the equivalent circuit in figure 3.10 and is implemented using equation 3.20 to equation 3.22. The program produces three types of output:

1 $V_n(t)$ - output voltages of the N differential pairs versus time,

2 $t_c(n,B)$ - comparison time versus the number of stage n and the number of bit B for a given g_mR, and

3 $t_c(n,g_mR)$ - Comparison time versus the number of stage n and the gain per stage g_mR for a given B.

The program prompts for input variables and is soft-key driven.

```
10    !-------------------------------------------------------------------
20    !PROGRAM "COMPARATOR ANALYSIS" 4/8/85 BY D. SOO
30    !-------------------------------------------------------------------
40    GRAPHICS OFF
50    PRINTER IS 1
60    MASS STORAGE IS ":INTERNAL,4,1"
70    COM Vic,Gmr,Vfinal,Nstart,Nstop,Bitstart,Bitstop,Tstart,Tstop
80    COM Vlsb,Sum,R,Gm,B,I,N,Tstep,C,Gstart,Gstop
90    ALLOCATE Filename$[20]
100   DIM Tmin(0:20,1:16),Vout(0:20,0:100),Ic(0:100),Tmin3(0:20,0:10)
110   DIM Tmin2(0:20,1:16),Vout1(0:20,0:100),Tmin4(0:20,0:10)
120   PRINT "COMPARATOR ANALYSIS - 3 by David Soo"
130   ASSIGN @Input TO "COMP3_IN"
140   ENTER @Input:Nstart,Nstop,Bitstart,Bitstop,Tstart,Tstop,Vic,Vfinal,Gmr,Gst
art,Gstop
150   ASSIGN @Input TO *
160 D:!
170   FOR I=0 TO 10
180     PRINT ""
190   NEXT I
200   PRINT " NSTART     = ";Nstart
210   PRINT " NSTOP      = ";Nstop
220   PRINT " BITSTART   = ";Bitstart
230   PRINT " BITSTOP    = ";Bitstop
240   PRINT " TSTART     = ";Tstart
250   PRINT " TSTOP      = ";Tstop
260   PRINT " VIC        = ";Vic
270   PRINT " VFINAL     = ";Vfinal
280   PRINT " GMR        = ";Gmr
290   PRINT " GSTART     = ";Gstart
300   PRINT " GSTOP      = ";Gstop
310   INPUT "INPUT NSTART",Nstart
320   INPUT "INPUT NSTOP",Nstop
330   INPUT "INPUT BITSTART",Bitstart
340   INPUT "INPUT BITSTOP",Bitstop
350   INPUT "INPUT TSTART",Tstart
360   INPUT "INPUT TSTOP",Tstop
370   INPUT "INPUT VIC ",Vic
380   INPUT "INPUT VFINAL",Vfinal
390   INPUT "INPUT GMR",Gmr
400   INPUT "INPUT GSTART",Gstart
410   INPUT "INPUT GSTOP",Gstop
420   PURGE "COMP3_IN"
430   CREATE BDAT "COMP3_IN",11,8
440   ASSIGN @Input TO "COMP3_IN"
450   OUTPUT @Input;Nstart,Nstop,Bitstart,Bitstop,Tstart,Tstop,Vic,Vfinal,Gmr,Gs
tart,Gstop
460   ASSIGN @Input TO *
470   ON KEY 1 LABEL "PLOT T(N,B)" GOSUB E
480   ON KEY 0 LABEL "PLOT Vo(T,N)" GOSUB A
490   ON KEY 2 LABEL "PLOT T(N,GmRo)" GOSUB G
500   ON KEY 8 LABEL "INPUT TABLE" RECOVER D
510   ON KEY 9 LABEL "PLOT " GOSUB C
520   ON KEY 5 LABEL "CAL Vo(T,N)" GOSUB B
530   ON KEY 6 LABEL "CAL T(N,B)" GOSUB F
540   ON KEY 7 LABEL "CAL T(N,GmRo)" GOSUB H
550 Wait:   !
560   GOTO Wait
570   !
580   !-----------------------SUBROUTINES-------------------------------
590   !
600 A:   !----------  ----------TO PLOT Vo(T,N)-----------------------------
610   PRINT "CURRENT FILENAME IS":Filename$
620   INPUT "INPUT DATA FILENAME?",Filename$
630   ASSIGN @Input TO Filename$
640   ENTER @Input;Nstop2,Tstart,Tstop
650   ENTER @Input;Vout1(*)
660   ASSIGN @Input TO *
670   Xlab$="TIME (sec)"
680   Ylab$="Vod (V)"
690   Xmin=Tstart
700   Xmax=Tstop
710   Ymin=-6
720   Ymax=6
730   Xstep=10
740   Xlabel=5
750   Ystep=10
760   Ylabel=5
770   GOSUB Linlin
780   CLIP ON
790   PEN 5
800   Tstep=(Tstop-Tstart)/100
810   IF Nstart<1 THEN
820     Nstart2=1
830   ELSE
840     Nstart2=Nstart
850   END IF
860   FOR N=Nstart2 TO Nstop2 STEP 1
870     MOVE 0,-5
880     FOR T=0 TO 99 STEP 1
890       DRAW T*Tstep,Vout1(N,T)
900     NEXT T
910   NEXT N
920   INPUT "DO YOU WISH TO RE-SCALE",Junk$
930   IF Junk$="Y" THEN
940     PRINT "YMAX=",Ymax
950     INPUT "INPUT YMAX",Ymax
960     PRINT "YMIN=",Ymin
970     INPUT "INPUT YMIN",Ymin
980     PRINT "XMAX=",Xmax
990     INPUT "INPUT XMAX",Xmax
1000    PRINT "XSTEP=",Xstep
1010    INPUT "INPUT XSTEP (10,15,20 ETC)",Xstep
1020    PRINT "YSTEP=",Ystep
1030    INPUT "INPUT YSTEP (10,15,20 ETC)",Ystep
1040    PRINT "XLABEL=",Xlabel
1050    INPUT "INPUT XLABEL (5,6,7 ETC)",Xlabel
1060    PRINT "YLABEL=",Ylabel
1070    INPUT "INPUT YLABEL (5,6,7 ETC)",Ylabel
1080    GOTO 770
1090  END IF
1100  Plot$="N"
1110  INPUT "DO YOU WISH TO PLOT?",Plot$
1120  IF Plot$="Y" THEN GOTO 770
1130  Plot$="N"
1140  RETURN
1150 C:!-----  ----------TO ENABLE PLOTTER-----------------------------
1160  Plot$="N"
1170  INPUT " DO YOU WANT TO PLOT? ",Plot$
1180  RETURN
1190 B:!-----------------TO CALCULATE Vo(T,N)-----------------------------
```

```
1200  Gm=8.0E-5
1210  R=Gmr/8.0E-5
1220  C=Gm/(2*3.1416*3.65E+9)
1230  IF Nstart<1 THEN
1240    Nstart2=1
1250  ELSE
1260    Nstart2=Nstart
1270  END IF
1280  Tstep=(Tstop-Tstart)/100
1290  FOR B=Bitstart TO Bitstop STEP 1
1300    Vlsb=2/(2^B)
1310    FOR T=1 TO 100 STEP 1
1320      Vout(0,T)=Vlsb
1330    NEXT T
1340    FOR N=Nstart2 TO Nstop STEP 1
1350      Vout(N,0)=Vic
1360      Tmin(N,B)=1
1370    NEXT N
1380    Tmin(0,B)=1
1390  !
1400  !    CALCULATE:
1410  !
1420    Nstop2=Nstop
1430    Flag=1
1440    FOR N=Nstart2 TO Nstop STEP 1
1450      FOR T=1 TO 99 STEP 1
1460        R2=R*EXP(-1/2*(Vout(N,T-1)/3.5)^2)
1470        Vout(N,T)=(Vout(N,T-1)+(Gm/C*Vout(N-1,T)*Tstep))/(1+(Tstep/(R2*C)))
1480        IF Vout(N,T)<Vic THEN Vout(N,T)=Vic
1490        PRINT "B=";B,"N=";N,"T=";T,"VOUT=";Vout(N,T)
1500        IF Vout(N,T)>Vfinal THEN
1510          Vout(N,T)=Vfinal
1520          Tmin(N,B)=T*Tstep
1530          IF Tmin(N,B)>Tmin(N-1,B) AND Flag=1 THEN
1540            Flag=0
1550            Nstop2=N+2
1560          END IF
1570          FOR T2=T+1 TO 99 STEP 1
1580            Vout(N,T2)=Vfinal
1590          NEXT T2
1600          IF N=Nstop2 THEN GOTO 1650
1610          GOTO 1640
1620        END IF
1630      NEXT T
1640    NEXT N
1650  NEXT B
1660  !
1670  !   STORE DATA ONTO DISC:
1680  !
1690  CAT
1700  Junk$="Y"
1710  PRINT "CURRENT FILENAME IS";Filename$
1720  INPUT "INPUT DATAFILE NAME",Filename$
1730  IF Filename$="" THEN GOTO 1830
1740  INPUT "DO YOU WANT TO PURGE OLD FILE? (Y)",Junk$
1750  IF Junk$="Y" THEN
1760    PURGE Filename$
1770  END IF
1780  CREATE BDAT Filename$,2200,8
1790  ASSIGN @Input TO Filename$
1800  OUTPUT @Input;Nstop2,Tstart,Tstop
1810  OUTPUT @Input;Vout(*)
1820  ASSIGN @Input TO *
1830  RETURN
1840 F:  !----------------------TO CALCULATE T(N,B)-----------------------
1850  Gm=8.0E-5
1860  R=Gmr/8.0E-5
1870  C=Gm/(2*3.1416*3.65E+9)
1880  IF Nstart<1 THEN
1890    Nstart2=1
1900  ELSE
1910    Nstart2=Nstart
1920  END IF
1930  Tstep=(Tstop-Tstart)/100
1940  FOR B=Bitstart TO Bitstop STEP 1
1950    Vlsb=2/(2^B)
1960    FOR T=1 TO 100 STEP 1
1970      Vout(0,T)=Vlsb
1980    NEXT T
1990    FOR N=Nstart2 TO Nstop STEP 1
2000      Vout(N,0)=Vic
2010      Tmin(N,B)=1
2020    NEXT N
2030    Tmin(0,B)=1
2040  !
2050  !    CALCULATE:
2060  !
2070    Nstop2=Nstop
2080    Flag=1
2090    FOR N=Nstart2 TO Nstop STEP 1
2100      FOR T=1 TO 99 STEP 1
2110        R2=R*EXP(-1/2*(Vout(N,T-1)/3.5)^2)
2120        Vout(N,T)=(Vout(N,T-1)+(Gm/C*Vout(N-1,T)*Tstep))/(1+(Tstep/(R2*C)))
2130        IF Vout(N,T)<Vic THEN Vout(N,T)=Vic
2140        PRINT "B=";B,"N=";N,"T=";T,"VOUT=";Vout(N,T)
2150        IF Vout(N,T)>Vfinal THEN
2160          Vout(N,T)=Vfinal
2170          Tmin(N,B)=T*Tstep
2180          IF Tmin(N,B)>Tmin(N-1,B) AND Flag=1 THEN
2190            Flag=0
2200            Nstop2=N+2
2210          END IF
2220          FOR T2=T+1 TO 99
2230            Vout(N,T2)=Vfinal
2240          NEXT T2
2250          IF N=Nstop2 THEN GOTO 2300
2260          GOTO 2290
2270        END IF
2280      NEXT T
2290    NEXT N
2300  NEXT B
2310  !
2320  ! STORE DATA ONTO DISC:
2330  !
2340  CAT
2350  Junk$="Y"
2360  PRINT "CURRENT FILENAME IS";Filename$
2370  INPUT "INPUT DATAFILE NAME.",Filename$
2380  IF Filename$="" THEN GOTO 2480
2390  INPUT "DO YOU WANT TO PURGE OLD FILE? (Y)",Junk$
```

```
2400  IF Junk$="Y" THEN
2410    PURGE Filename$
2420  END IF
2430  CREATE BDAT Filename$,(21*16)+6.8
2440  ASSIGN @Input TO Filename$
2450  OUTPUT @Input;Bitstart,Bitstop,Nstart,Nstop,Tstart,Tstop
2460  OUTPUT @Input;Tmin(*)
2470  ASSIGN @Input TO *
2480  RETURN
2490 E:  !-------------------TO PLOT T(N,B)---------------------------------
2500  CAT
2510  PRINT "CURRENT FILE IS ";Filename$
2520  INPUT "INPUT DATA FILE NAME?",Filename$
2530  ASSIGN @Input TO Filename$
2540  ENTER @Input;Bitstart,Bitstop,Nstart,Nstop,Tstart,Tstop
2550  ENTER @Input;Tmin2(*)
2560  ASSIGN @Input TO *
2570  Xlab$="Number of Stage N"
2580  Ylab$="Time to V-final (sec)"
2590  Ymin=Tstart
2600  Ymax=Tstop
2610  Xmin=0
2620  Xmax=Nstop
2630  Xstep=10
2640  Ystep=10
2650  Ylabel=5
2660  Xlabel=5
2670  GOSUB Linlin
2680  CLIP 1,Xmax,Ymin,Ymax
2690  PEN 5
2700  LORG 5
2710  FOR B=Bitstart TO Bitstop STEP 1
2720    Flag=1
2730    FOR N=Nstart TO Nstop-1 STEP 1
2740      IF Tmin2(N,B)>Tstop THEN
2750        GOTO 2830
2760      ELSE
2770        IF Tmin2(N-1,B)>Tstop THEN
2780          MOVE N,Tmin2(N,B)
2790        ELSE
2800          DRAW N,Tmin2(N,B)
2810        END IF
2820      END IF
2830      IF Tmin2(N,B)<=Tmin2(N-1,B) AND Tmin2(N,B)<=Tmin2(N+1,B) AND Tmin2(N,B
)<Tstop THEN
2840        CSIZE 3,.6
2850        LABEL B
2860        CSIZE 2,.6
2870        MOVE N,Tmin2(N,B)
2880      ELSE
2890        IF Tmin2(N,B)<Tstop THEN
2900          LABEL "*"
2910          MOVE N,Tmin2(N,B)
2920        END IF
2930      END IF
2940    NEXT N
2950    MOVE 0,0
2960  NEXT B
2970  INPUT "DO YOU WISH TO RE-SCALE",Junk$
2980  IF Junk$="Y" THEN
2990    PRINT "YMAX=",Ymax
3000    INPUT "INPUT YMAX",Ymax
3010    PRINT "YMIN=",Ymin
3020    INPUT "INPUT YMIN",Ymin
3030    PRINT "XMAX=",Xmax
3040    INPUT "INPUT XMAX",Xmax
3050    PRINT "XMIN=",Xmin
3060    INPUT "INPUT XMIN",Xmin
3070    PRINT "XSTEP=",Xstep
3080    INPUT "INPUT XSTEP (10,15,20 ETC",Xstep
3090    PRINT "YSTEP=",Ystep
3100    INPUT "INPUT YSTEP (10,15,20 ETC)",Ystep
3110    PRINT "XLABEL=",Xlabel
3120    INPUT "INPUT XLABEL (5,6,7 ETC)",Xlabel
3130    PRINT "YLABEL=",Ylabel
3140    INPUT "INPUT YLABEL (5,6,7 ETC)",Ylabel
3150    GOTO 2670
3160  END IF
3170  Plot$="N"
3180  INPUT "DO YOU WISH TO PLOT?",Plot$
3190  IF Plot$="Y" THEN GOTO 2670
3200  RETURN
3210 H:  !-------------------TO CALCULATE T(N,GmRo)-------------------------
3220  Gm=8.0E-5
3230  C=Gm/(2*3.1416*3.65E+9)
3240  IF Nstart<1 THEN
3250    Nstart2=1
3260  ELSE
3270    Nstart2=Nstart
3280  END IF
3290  Tstep=(Tstop-Tstart)/100
3300  FOR G=1 TO 10 STEP 1
3310    Gstep=(Gstop-Gstart)/10
3320    Gain=Gstart+(G-1)*Gstep
3330    R=Gain/8.0E-5
3340    FOR B=Bitstart TO Bitstop STEP 1
3350      Vlsb=2/(2^B)
3360      FOR T=1 TO 100 STEP 1
3370        Vout(0,T)=Vlsb
3380      NEXT T
3390      FOR N=Nstart2 TO Nstop STEP 1
3400        Vout(N,0)=Vic
3410        Tmin3(N,G)=1
3420      NEXT N
3430      Tmin3(0,G)=1
3440  !
3450  !    CALCULATE:
3460  !
3470      Nstop2=Nstop
3480      Flag=1
3490      FOR N=Nstart2 TO Nstop STEP 1
3500        Sum=0
3510        Vout(N,1)=Vout(N,0)
3520        FOR T=1 TO 99 STEP 1
3530          R2=R*EXP(-1/2*(Vout(N,T-1)/3.5)^2)
3540          Vout(N,T)=(Vout(N,T-1)+(Gm/C*Vout(N-1,T)*Tstep))/(1+(Tstep/(R2*C))
)
3550          IF Vout(N,T)<Vic THEN Vout(N,T)=Vic
3560          PRINT "GAIN=";Gain,"N=";N,"T=";T,"VOUT=";Vout(N,T)
3570          IF Vout(N,T)>Vfinal THEN
3580            Vout(N,T)=Vfinal
```

```
3590            Tmin3(N,G)=T+Tstep
3600            IF Tmin3(N,G)>Tmin3(N-1,G) AND Flag=1 THEN
3610              Flag=0
3620              Nstop2=N+2
3630            END IF
3640            FOR T2=T+1 TO 99
3650              Vout(N,T2)=Vfinal
3660            NEXT T2
3670            IF N=Nstop2 THEN GOTO 3720
3680            GOTO 3710
3690          END IF
3700        NEXT T
3710      NEXT N
3720    NEXT B
3730  NEXT G
3740  !
3750  ! STORE DATA ONTO DISC:
3760  !
3770  CAT
3780  Junk$="Y"
3790  PRINT "CURRENT FILENAME IS";Filename$
3800  INPUT "INPUT DATAFILE NAME.",Filename$
3810  IF Filename$="" THEN GOTO 3910
3820  INPUT "DO YOU WANT TO PURGE OLD FILE? (Y)",Junk$
3830  IF Junk$="Y" THEN
3840    PURGE Filename$
3850  END IF
3860  CREATE BDAT Filename$,(21+11)+6,8
3870  ASSIGN @Input TO Filename$
3880  OUTPUT @Input;Nstart,Nstop,Tstart,Tstop,Gstart,Gstop
3890  OUTPUT @Input;Tmin3(*)
3900  ASSIGN @Input TO *
3910  RETURN
3920 G:  !------------------TO PLOT T(N,GMRO)-------------------------------
3930  CAT
3940  PRINT "CURRENT FILE IS ";Filename$
3950  INPUT "INPUT DATA FILE NAME?",Filename$
3960  ASSIGN @Input TO Filename$
3970  ENTER @Input;Nstart,Nstop,Tstart,Tstop,Gstart,Gstop
3980  ENTER @Input;Tmin4(*)
3990  ASSIGN @Input TO *
4000  Xlab$="Number of Stage N"
4010  Ylab$="Time to V-final (sec)"
4020  Ymin=Tstart
4030  Ymax=Tstop
4040  Xmin=Nstart
4050  Xmax=Nstop
4060  Xstep=10
4070  Ystep=10
4080  Xlabel=5
4090  Ylabel=5
4100  GOSUB Linlin
4110  CLIP 1,Xmax,Ymin,Ymax
4120  PEN 5
4130  LORG 5
4140  FOR G=1 TO 10 STEP 1
4150    Gstep=(Gstop-Gstart)/10
4160    Gain=Gstart+((G-1)*Gstep)
4170    FOR B=Bitstart TO Bitstop STEP 1
4180      Flag=1
4190      FOR N=Nstart TO Nstop-1 STEP 1
4200        IF Tmin4(N,G)>Tstop THEN
4210          GOTO 4290
4220        ELSE
4230          IF Tmin4(N-1,G)>Tstop THEN
4240            MOVE N,Tmin4(N,G)
4250          ELSE
4260            DRAW N,Tmin4(N,G)
4270          END IF
4280        END IF
4290        IF Tmin4(N,G)<=Tmin4(N-1,G) AND Tmin4(N,G)<=Tmin4(N+1,G) AND Tmin4(N
,G)<Tstop THEN
4300          CSIZE 3,.6
4310          LABEL Gain
4320          CSIZE 2,.6
4330          MOVE N,Tmin4(N,G)
4340        ELSE
4350          IF Tmin4(N,G)<Tstop THEN
4360            LABEL "*"
4370            MOVE N,Tmin4(N,G)
4380          END IF
4390        END IF
4400      NEXT N
4410      MOVE 0,0
4420    NEXT B
4430  NEXT G
4440  INPUT "DO YOU WISH TO RE-SCALE",Junk$
4450  IF Junk$="Y" THEN
4460    PRINT "YMAX=",Ymax
4470    INPUT "INPUT YMAX",Ymax
4480    PRINT "YMIN=",Ymin
4490    INPUT "INPUT YMIN",Ymin
4500    PRINT "XMAX=",Xmax
4510    INPUT "INPUT XMAX",Xmax
4520    PRINT "XMIN=",Xmin
4530    INPUT "INPUT XMIN",Xmin
4540    PRINT "XSTEP=",Xstep
4550    INPUT "INPUT XSTEP (10,15,20 ETC)",Xstep
4560    PRINT "YSTEP=",Ystep
4570    INPUT "INPUT YSTEP (10,15,20 ETC)",Ystep
4580    PRINT "XLABEL=",Xlabel
4590    INPUT "INPUT XLABEL (4,5,6 ETC)",Xlabel
4600    PRINT "YLABEL=",Ylabel
4610    INPUT "INPUT YLABEL (4,5,6 ETC)",Ylabel
4620    GOTO 4100
4630  END IF
4640  Plot$="N"
4650  INPUT "DO YOU WISH TO PLOT?",Plot$
4660  IF Plot$="Y" THEN GOTO 4100
4670  RETURN
4680  !-------------------------SUBROUTINES-------------------------------
4690  !THIS PROGRAM MAKES A LIN-LIN GRAPH PAPER
4700  !THE SCALE ,LABELS CAN BE INPUTED THROUGH THE KEYBOARD
4710  !-------------------------------------------------------------------
4720 Linlin:  !
4730  GINIT
4740  IF Plot$="Y" THEN
4750    PLOTTER IS 708,"HPGL"
4760  ELSE
4770    GRAPHICS ON
4780  END IF
```

```
4790  DIM Xlab$[40],Ylab$[40]
4800  DEG
4810  MOVE 70,2
4820  LORG 5
4830  CSIZE 3.5,.6
4840  LDIR 0
4850  PEN 5
4860  LABEL Xlab$
4870  MOVE 5,50
4880  LDIR 90
4890  LABEL Ylab$
4900  VIEWPORT 20,115,10,85
4910  WINDOW Xmin,Xmax,Ymin,Ymax
4920  PEN 1
4930  IF Plot$="Y" THEN
4940    LINE TYPE 1
4950  ELSE
4960    LINE TYPE 3
4970  END IF
4980  GRID (Xmax-Xmin)/Xstep,(Ymax-Ymin)/Ystep,Xmin,Ymin,1,1
4990  LINE TYPE 1
5000  AXES (Xmax-Xmin)/Xstep/2,(Ymax-Ymin)/Ystep/2,Xmin,Ymin,2,2
5010  PEN 5
5020  LINE TYPE 1
5030  FRAME
5040  PEN 1
5050  CLIP OFF
5060  GOSUB Lxaxes
5070  GOSUB Lyaxes
5080  PENUP
5090  MOVE Xmin,Ymin
5100  RETURN
5110 Lxaxes: !
5120  FOR Xp=Xmin TO Xmax STEP (Xmax-Xmin)/Xlabel
5130    MOVE Xp,Ymin-(Ymax-Ymin)/50
5140    CSIZE 2,.6
5150    LORG 6
5160    LDIR 0
5170    LABEL USING "D.DESZZ";Xp
5180  NEXT Xp
5190  RETURN
5200 Lyaxes: !
5210  FOR Yp=Ymin TO Ymax STEP (Ymax-Ymin)/Ylabel
5220    MOVE Xmin-(Xmax-Xmin)/80,Yp
5230    CSIZE 2,.6
5240    LORG 8
5250    LDIR 0
5260    LABEL USING "SD.DESZZ";Yp
5270  NEXT Yp
5280  RETURN
5290  END
```

Figure Captions

Fig. 3.27a Calculated comparison time t_c of Comparator II versus n and B using equation 3.35 where $V_{final}=5V$.

Fig. 3.27b Simulated comparison time t_c of comparator II versus n and B using *program* $A-5$ with $g_mR=100$, $V_n(0)=0$, and $V_{final}=5V$.

Fig. 3.28 Simulated comparison time t_c of comparator II versus n and g_mR using *program* $A-5$ with B=6 and $V_{final}=5V$.

Fig. 3.29a Complete schematic of a 6-bit open-loop comparator with *shunt* MOS reset-switches.

Fig. 3.29b Complete schematic of a 6-bit open-loop comparator with *feedback* MOS reset-switches.

Fig. 3.30a Input and clock waveforms used in the SPICE transient simulation of the comparator in figure 3.29a

Fig. 3.30b Simulated output waveforms of the circuit in figure 3.29a with all offset voltages equal to zero using SPICE.

Fig. 3.30c A detail plot of the voltages in the input *S/H* of figure 3.29a.

Fig. 3.31a Simulated output waveforms of the circuit in figure 3.29a with offset voltages of alternating sign (+15mV, -15mV, etc.) using SPICE.

Fig. 3.31b Simulated output waveforms of the circuit in figure 3.29b with offset voltages of alternating sign (+15mV, -15mV, etc.) using SPICE.

Fig. 3.31c Simulated output waveforms of the circuit in figure 3.29a with offset voltages of the same sign (+15mV) using SPICE.

Fig. 3.32 Configuration of Comparator III - Pipeline of differential amplifiers.

Fig. 3.33a Pipeline of simple differential pairs - OL-amp.

Fig. 3.33b Pipeline of differential Active Shunt Feedback Amplifier - ASF-amp.

Fig. 3.33c Pipeline of differential Buffered Active Shunt Feedback Amplifier - BASF-amp.

References

[1] B. Gilbert, "A new wide-band amplifier technique," IEEE J.Solid-State Circuit, vol.SC-3, pp. 353-365, Dec. 1968.

[2] M-S. Liang et.al., "Hot carrier induced degradation in thin gate oxide MOSFETs," IEDM Technical Digest, pp. 186-189, 1983.

[3] R. Anderson, "S-parameter techniques for faster, more accurate network design," Hewlett-Packard Application Note 95-1.

[4] S. Konaka, et.al.,"A 30ps Si bipolar IC using super self-aligned process technology," in Ext. Abst. 16th Conf. Solid State Devices and Mater., Aug.-Sept. 1984, pp. 209-212.

[5] P. Ko et.al., " SiGMOS - A silicon gigabit/s NMOS technology," IEDM Technical Digest, pp. 751-753, 1983.

[6] R. Bayruns et.al., " Delay analysis of Si NMOS Gbit/s logic circuit," IEEE J. of Solid-State Circuit, vol SC-19, no. 5 Oct.,1984.

[7] P. Gray and R. Meyer, "Analysis and design of analog integrated circuits," 2nd Edition, John Wiley & Sons, 1984.

[8] A. Abidi, "Gigahertz transconductance amplifiers in fine line NMOS," IEEE J. of Solid-State Circuits, Vol. SC-19, No. 6, Dec. 1984.

[9] H. Ichino et.al., "Si bipolar multi-Gbit/s logic family using super self-aligned process technology," in Ext. Abst. 16th Conf. Solid State Devices and Mater., Aug.-Sept. 1984, pp. 217-220.

[10] D. Estreich, " A monolithic wide-band GaAs IC amplifier," IEEE J. of Solid-State Circuits, Vol SC-17, No. 6, Dec. 1982.

[11] R. Meyer, "EECS 241 class notes on wide-band amplifiers," Dept. of EECS, U.C. Berkeley.

[12] A. Vladimirescu and S. Liu, " The simulation of MOS integrated circuits using SPICE2," Memo. No. UCB/ERL M80/7, Oct. 1981, U.C. Berkeley.

[13] B. Sheu et.al., " Characterization of intrinsic capacitances of small-geometry MOSFETs," in Tech. Dig. of IEEE 1984 Symp. VLSI Technol.

[14] B. Sheu et.al., "A capacitance method to determine channel lengths for conventional and LDD MOSFET's," IEEE Electron Device Letters, Vol. EDL-5, No. 11, Nov. 1984.

[15] R. Yen and P. Gray, "A MOS switched-capacitor instrumentation amplifier," IEEE J. of Solid-State Circuits, Vol. SC-17, No. 6, pp. 1008-1013, Dec. 1982.

[16] P. Li, "Ratio-independent algorithmic analog to digital conversion techniques," Ph. D thesis, Department of EECS, U.C. Berkeley, 1984.

[17] Y. Haque, et al., "A two chip PCM voice CODEC with filters," IEEE J of Solid-State Circuits, vol. SC-14, pp.961-969, Dec. 1979.

[18] P. Saul, "A high-speed comparator design technique," IEEE J. of Solid-State Circuit, Vol. SC-17, No. 3, pp. 529-532, Jun. 1982.

[19] G. Erdi, "Comparator sets up high-speed, high-accuracy A/D conversion," Electronic Design, Vol. 28, No. 19, pp.85-87, Sept. 1980.

[20] Member of Technical Staff, Bell Telephone Laboratories, "Transmission system for communications," 5th Edition, pp. 703-758, 1982.

[21] Y. Yee, L. Terman, and Heller, "A 1mV MOS comparator,"IEEE J. Solid-State Circuits, vol. SC-13, pp.294-298, jun. 1978.

[22] T. Tsukada, et al., "CMOS 8b 25MHz flash ADC," IEEE ISSCC Digest of Technical Papers, pp. 34-35, 1985.

[23] A. Dingwall, "Monolithic expandable 6 bit 20 MHz CMOS/SOS A/D converter," IEEE J. of Solid-State Circuits, vol.SC-14, No. 6, pp.926-932, Dec. 1979.

[24] A. Dingwall and V. Zazzu, "An 8MHz 8b CMOS subranging ADC," IEEE ISSCC Digest of Technical Papers, pp. 72-73, 1985.

[25] A. Hamade, "A single chip all-MOS 8-bit A/D converter," IEEE J. Solid-State Circuits, vol. SC-13, pp. 785-791, Dec. 1978.

[26] D. Allstot, "A precision variable-supply CMOS comparator," IEEE J. Solid-State Circuits, vol. SC-17, No. 6, pp. 1080-1087, Dec. 1982.

[27] B. Zojer, et al, "A 6-bit 200 MHz full Nyquist A/D converter," IEEE J. Solid-State Circuits, vol. SC-20, No. 3, pp. 780-786, June 1985.

[28] J. Eldon and R. Olsen, "Single chip flash A/D with evaluation boards," Proceedings of the IEEE 1982 Region 6 Conference, pp. 26-29, Feb. 1982.

[29] P. Saul, A. Fairgrieve and A. Fryers, "Monolithic components for 100MHz data conversion," IEEE J.Solid-State Circuits, vol. SC-15, No. 3, June 1980.

[30] M. Suzuki, et al, "A bipolar monolithic multigigabit/s decision circuit," IEEE J. of Solid-State Circuits, vol. SC-19, No. 4, pp. 462-467, Aug. 1984.

[31] D. Meignant and M. Binet, "A high performance 1.8GHz strobed comparator for A/D converter," IEEE GaAs IC Symposium, Technical Digest, pp. 66-69, 1983.

[32] H. Fiedler and B. Hoefflinger, "High-speed low-power MOS-comparator for 20 MHz LSI parallel A/D converters," IEE ESSCIR, pp. 73-75, 1979.

[33] H. Lee, D. Hodges and P. Gray, "A self-calibrating 15 bit CMOS A/D converter," IEEE J.Solid State Circuits, vol SC-19, No. 6, pp. 813-819, Dec. 1984.

[34] D. Soo, et al., "A 750MS/s NMOS latched comparator," IEEE ISSCC Digest of Technical Papers, pp. 146-147, 1985.

[35] G. Smith, "Fine line MOS technology for high speed integrated circuits," IEEE Trans. Electron Devives, vol ED-30, No. 11, pp. 1564, Nov. 1983.

[36] G.J. Hu, et al., "A self-aligned 1-um CMOS technology for VLSI," IEDM Technical Digest, pp. 739-741, 1983.

[37] Texas Instruments, "Types TL510, differential comparators with strobe," Linear Circuit Data Book, pp. 4-45 to 4-47, 1984.