Power and Ground Requirements for a High-speed 32 Bit Computer Chip Set

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ABSTRACT

The trend, as technology advances, is for VLSI implementations of computer systems to use increasingly wider busses and faster clock rates. This report illustrates how the trend affects integrated circuit design in the areas of power and ground design, and output pads. The first section of the report discusses the circuit design issues of inductance effects, CMOS noise margins, clean and dirty supply lines, pad loading and delay, process variation effects, and pad driver design approaches. The second section is an in depth description of the technique used and results obtained for inductance characterization of pin grid arrays. Following that is a section discussing design issues for input and output pad cells, along with a description of the pad cells developed for the Berkeley SPUR project.

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1. Motivation and Problem Statement

The trend in VLSI implementations of computer systems is clear: 8 bit microprocessors have given way to 16 and 32 bit versions. Clock rates of 1 to 2 MHz are no longer as common as 8 to 12 MHz. At the same time, the capacitive loads on each line of the increasingly wide busses are remaining essentially constant. From a simplified circuit perspective, this implies that advancing technology requires that VLSI chips switch current more rapidly. The rate of change of current in a processor chip rises linearly with the width of the busses and linearly with the reciprocal of the rise time of the chip output signals. This trend towards faster current switching collides with parasitic inductance present in any physical circuit and requires innovative chip designs for power and ground connections.

There are a variety of electrical issues which are affected by the trend towards faster current switching [Scha83]. Chief among these is inductance. The most significant parasitic inductances are present on package traces and input and output pins. Inductance of wiring traces on chips may also be troublesome, but is not considered in this report. Rapid changes in current in these parasitic inductors create voltage spikes. In the typical integrated circuit design the inductance we must be most concerned with is that of the bond wires to our chips and the leads of the integrated circuit packages. Figure 1 illustrates how this affects our chips.

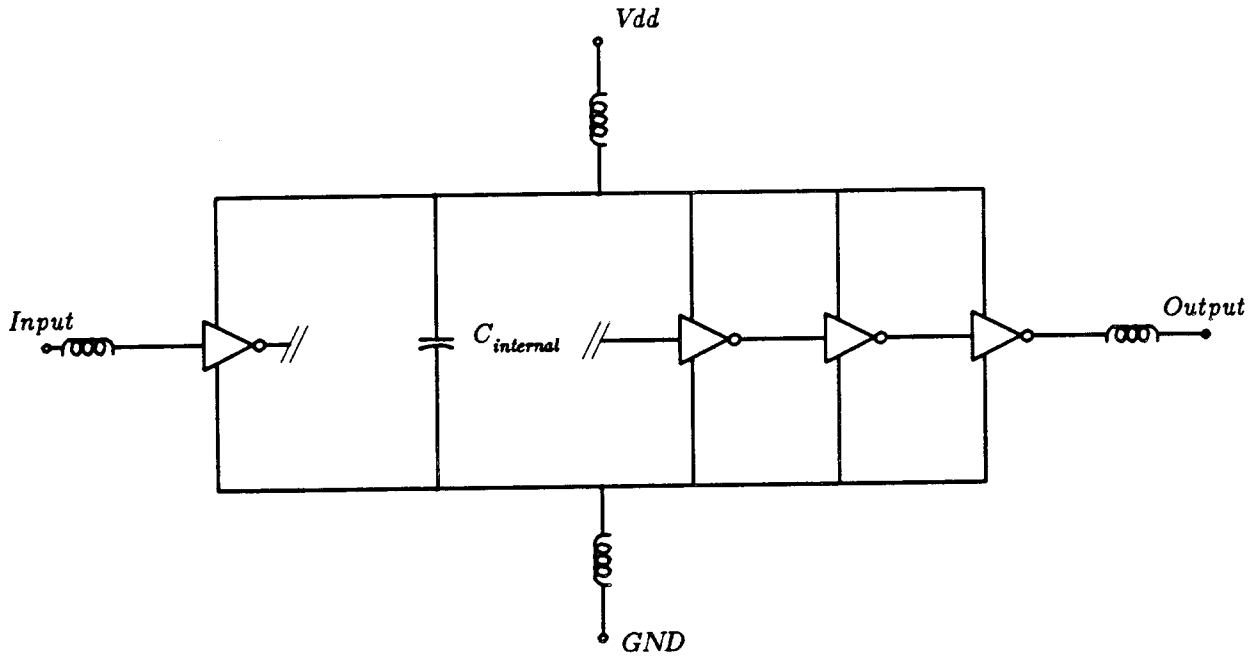

Figure 1: Each pad on the chip is connected to the PC board through a parasitic inductor.

In Figure 1, we see pad drivers and input buffers represented, which are the most troublesome parts of the chip. The output drivers typically drive large capacitances external to the chip, and hence cause the largest current transients on the power and ground busses. These current transients produce voltages (noise) on the parasitic inductors as given by the relationship:

$$v = L \frac{di}{dt} \tag{1}$$

Where v is the voltage across the parasitic inductor, L is the inductance of the lead or connection of concern, and $\frac{di}{dt}$ is the derivative of the current carried by the connection.

Equation (1) suggests two strategies for reducing noise caused by parasitic inductance: Reduce the parasitic inductance or reduce the derivative of the current. Reducing the parasitic inductance is the concern in pin-out for power and ground, as well

as chip level and board level bussing and decoupling. The most straight forward methods to reduce the effects of parasitic inductance are to increase the number of pins devoted to power and ground, and to add to the decoupling capacitors on PC boards. Reducing $\frac{di}{dt}$ tends to increase the time that a given pad driver takes to present a valid output level to its load. We will find that pad delay is a fundamental parameter in the solution of the power and ground design problem.

The load that each driver faces is another important factor. Ideally, I/O pad and power and ground design solutions will be flexible enough to be applicable to a variety of loading conditions. The minimum capacitive load imaginable is about 20 pF. On the high end, loads can range up to the 100 pF range. For the current generation of high speed chips, the transitions on these outputs should be in the 20 to 30 nanosecond range.

Parasitic inductance is, of course, strongly dependent on the type of package chosen for a particular integrated circuit. Since a number of different packaging techniques are used, it would be desirable to provide general solutions applicable to plastic and ceramic dual in-line packages, surface mount, solder bump and pin grid array techniques. This report, however, limits itself to pin grid arrays since this is the technique most applicable to high pin count chips which are the primary concern of the report. Moreover, much of the material presented is generally applicable to alternative packaging technologies.

Additionally, the discussion of this report is generally limited to CMOS technology. As in the case of the packaging technology to which the report is limited, the general concepts investigated are relevant to NMOS and even bipolar technology.

2. Issues in Power and Ground Design

2.1. Effects of Inductance

Referring again to Figure 1, we consider the effects of the voltages indicated by equation (1). For output drivers, we have one power and one ground pin supplying some number n of output drivers. When an output driver turns on it switches the current that will charge its load. In the worst case, power and ground will switch a current that is n times as large as the current switched by each output driver. This worst case will occur if all n of the outputs make the same state change at the same time. As the current in the power or ground busses rises from 0 to n times the current of each output driver, the voltage of equation (1) is produced. The parasitic problem is not a matter of waiting for the outputs to settle down. The outputs have lower currents switched in them than the power and ground lines do. Hence, the outputs don't show voltage spikes which are as large as those on the power and ground lines. Figure 2 gives SPICE simulation results showing power and ground noise caused by an output transition on a bus. This example is for a simplified bus driver with 16 drivers per power and ground line.

There are three important effects illustrated in Figure 2. The noise spikes on power and ground, which are greater than 2 V in magnitude, are obvious. In general, the voltage spikes for high going and low going output transitions will have the same impact. This is because either transition requires the same amount of charge to be supplied by the driver in about the same amount of time. Second, note that while chip power and ground fluctuate widely from the external supply values, the difference between power and ground tends to remain close to constant. The circuit illustrated in Figure 1 is somewhat simplified. With more sophisticated consideration of the inductance of on-chip wiring, a

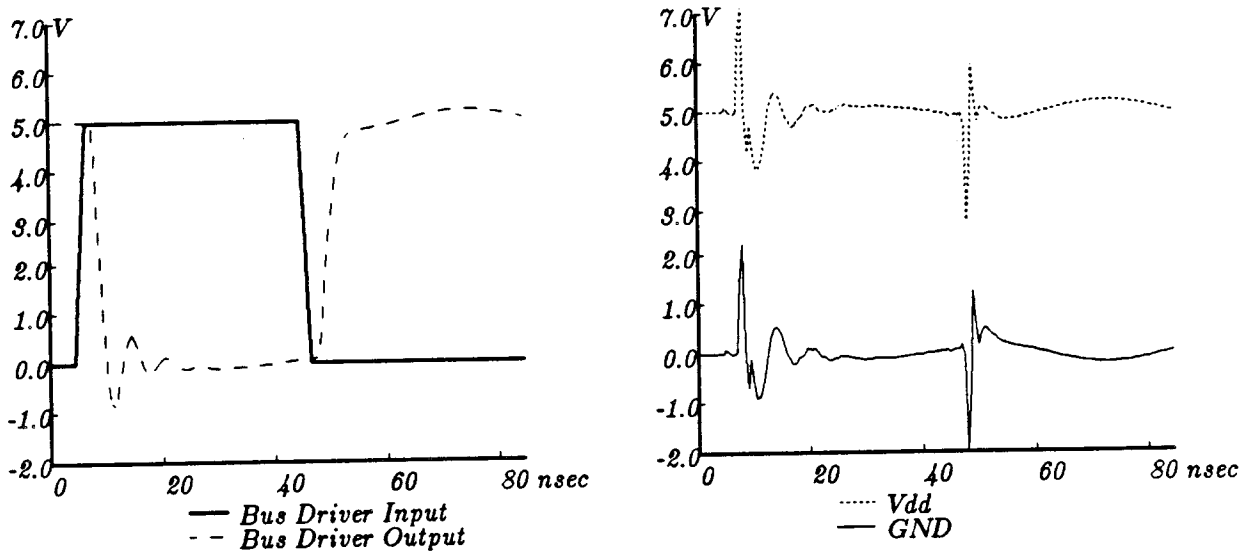

Figure 2: SPICE simulation results showing power and ground noise for bus output transition.

voltage less close to constant would be seen between the power and ground busses. None the less, the internal circuitry will be less affected by power and ground fluctuations than the input and output circuitry. The reason that the power and ground busses tend to stay a constant voltage apart is the large capacitance, shown in Figure 1 as $C_{internal}$. Most of the junctions on the chip contribute to this capacitance, which will be in the range of a few hundred picofarads. The third point demonstrated by Figure 3 is the oscillation of the bus driver output. The oscillation is caused by the parasitic inductance shown in Figure 1 at the output driver in series with the capacitance of the output load. The magnitude of this oscillation will always remain less than that of the power and ground spikes.

Figure 1 also shows a parasitic inductance at the chip input pins. This is not a concern since the impedance this represents is in series with the very large input impedance of a MOS transistor.

The place where this noise most affects us is at the input buffer. Signals input to the chip are referenced to PC board ground, while the input buffer must be referenced to the ground internal to the chip. Noise on the chip power and ground have the same effect as noise on an input signal. If voltage spikes on power and ground are large enough, they could be misconstrued as faulty logic levels; i.e. if a logic zero is noisy enough, it will be taken as a one. For example, an input signal to a chip which is 0.3 V above the PC board ground should be interpreted as a logic zero. If however, due to noise on the chip power and ground busses, the chip ground is 0.8 V below the PC board ground, the signal will appear to be 1.1 V above ground. This is in the undefined region for TTL inputs and the behavior of the input buffer is unpredictable. Especially for the clock input to our chips, we cannot tolerate noise on the chip power and ground lines to cause glitches in the signals.

Clock jitter is another problem which can be adversely affected by parasitic inductance. Rather than causing an out right error in a clock input, this problem affects the timing of clock edges. Many integrated circuits are quite sensitive to the timing of these edges. It may be fatal for the non-overlap time between two clock phases to vary on account of delays caused by parasitic inductance.

2.2. CMOS Noise Margins

A detailed look at the amount of noise that is tolerable requires consideration of noise margins. TTL signal levels are assumed for all inputs and outputs. In a full custom CMOS chip set, it would be possible to use special signal levels for the critical inputs and outputs to obtain better noise immunity. It was decided not to do this for the SPUR chip set since it would greatly complicate the electrical specifications of the chip interfaces.

Using TTL levels means that the output drivers must give a signal of 2.4 V or higher for a one and 0.4 V or lower for a zero. The input buffers must accept a signal of 2.0 V or higher as a one and 0.8 V or lower as a zero. The noise margin of each of these is 0.4 V. That is, a proper TTL output signal can be off by at most 0.4 V and still be received correctly. The noise created through parasitic inductance must be included in this 0.4 V noise margin.

A crucial design question is to decide how much of the 0.4 V noise margin will be used up in the power and ground design. That is, the power and ground design will assume that some noise will be generated. Just how much noise will be generated is up to the designer. For the SPUR chip set a conservative decision was made not to allow the worst case noise due to parasitic inductance to use up more than half, 0.2 V, of this noise margin. In a more aggressive design, it could be decided to use up the entire 0.4 V noise margin. This could be done based on the assumption that noise spikes caused by output drivers switching are rarely as bad as would be caused by the worst case of all outputs changing simultaneously and are unlikely to coincide with noise from other sources.

2.3. Clean and Dirty Supply Lines

2.3.1. Noise Reduction

Clean and dirty supply lines are a technique frequently used to reduce the the effects of parasitic voltages. Figure 3 represents two approaches that may be used to do this for bussing ground. Each of the two methods shown in Figure 3 distribute ground to the same pair of large ground bus branches. Parasitic voltages may appear across either the parasitic inductance, which is the chief interest of this report, or resistance in the

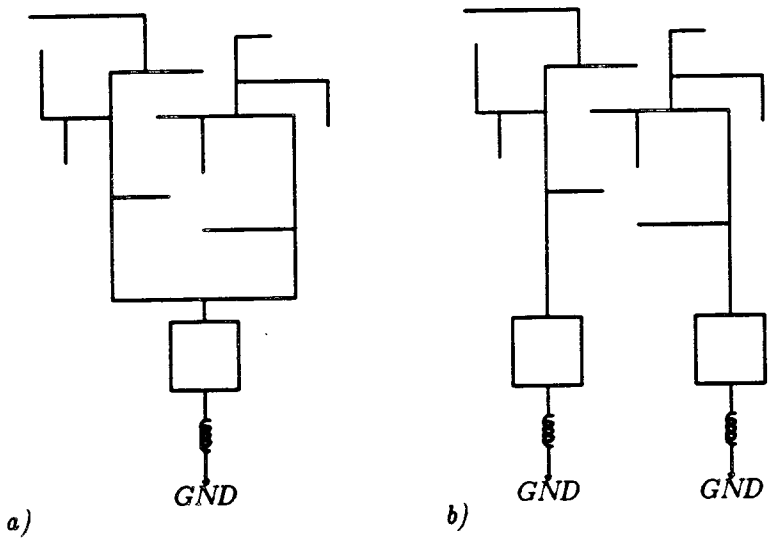

Figure 3: Two approaches to power distribution in 'clean' and 'dirty' branches.

ground lines themselves. In Figure 3a, large DC currents in the left branch of the ground distribution tree could cause unwanted voltage drops in the ground line. This does not affect the right branch of the ground tree (which may contain sensitive precharged or sensing circuits) since the two branches are connected together close the to ground pad. If this scheme is to be successful, the voltages induced on the bonding wire, package lead and PC board trace to the power supply must be of insignificant value given the total current in the ground line. If this in not the case, a scheme such as that in Figure 3b would be more appropriate. Here the "dirty" and "clean" branches have their own bonding pads and package leads. In this example the dirty branch on the left might be used for output driver power and ground, while the clean branch would be used for internal circuitry.

2.3.2. Latch-up Hazard for Separate Power and Ground Pins

The technique shown in Figure 3b has a particular hazard when it is used in a CMOS technology [Hodg83]. Figure 4 shows the cross-section of an inverter in an n-well CMOS process, such as the Xerox 2μ process used for the SPUR chip set. Figure 5 is a schematic of the parasitic bipolar npn and pnp transistors formed by the inverter.

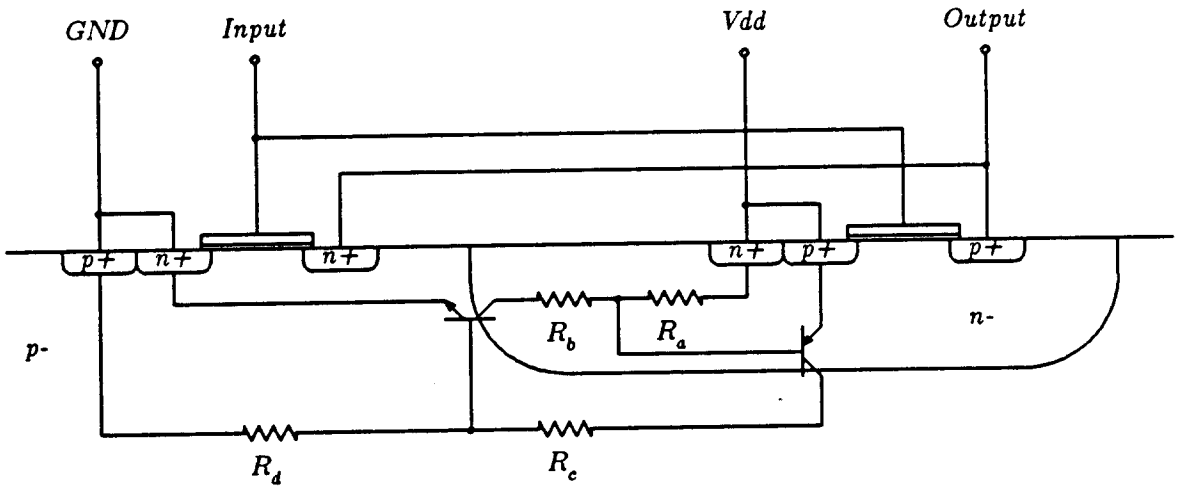

Figure 4: Cross-section of device structure of N-well CMOS inverter.

In Figure 5, the pnp transistor is formed by the diffusions for the PMOS transistor, n-well and p-type substrate. The npn transistor is formed by the diffusions for the NMOS transistor, p-type substrate and the n-well. The resistors R_a and R_b represent resistances of the n-well. The resistors R_c and R_d represent resistances of the substrate. Under normal circuit conditions, the currents in the substrate and n-well are very small. The voltages across R_a and R_d will be less than those necessary to turn on the bipolar transistors. With both bipolar transistors off we can ignore this parasitic circuit.

If, however, through some mechanism not represented in Figure 5, the node between R_c and R_d rises more than 0.7 V above ground, the npn transistor will turn on. This will cause a current to flow in R_a and R_b, lowering the voltage at the node between the two

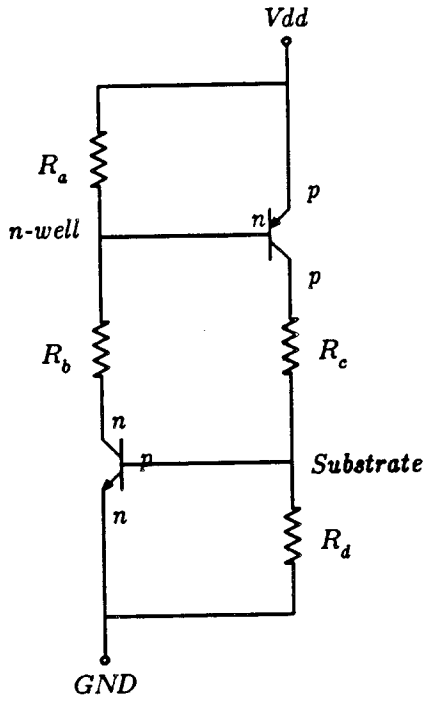

Figure 5: Schematic of parasitic bipolar transistors causing CMOS latch-up.

resistors. This causes the npn transistor to turn on, increasing any existing current flow in R_c and R_c. The effect of a small voltage at the node between R_c and R_d is amplified. The current in the two transistors increases until it is limited by the substrate and n-well resistances. This is the latch-up condition: The unwanted current cannot be shut off unless the circuit is disconnected from the power supply.

The layout allowed in CMOS generally precludes conditions which are a danger in initiating latch-up. Chief among these provisions are rules for well and substrate contacts. The function of these restrictions is to minimize the currents in the well and substrate, the currents that could create voltages on R_a and R_d. In adopting the approach of clean and dirty supply lines, there are conditions in which those restrictions would be violated. Figure 6 illustrates this case. If we were to use separate power and ground connections for the drivers and logic, we would use separate n-wells for the drivers and logic. Each n-

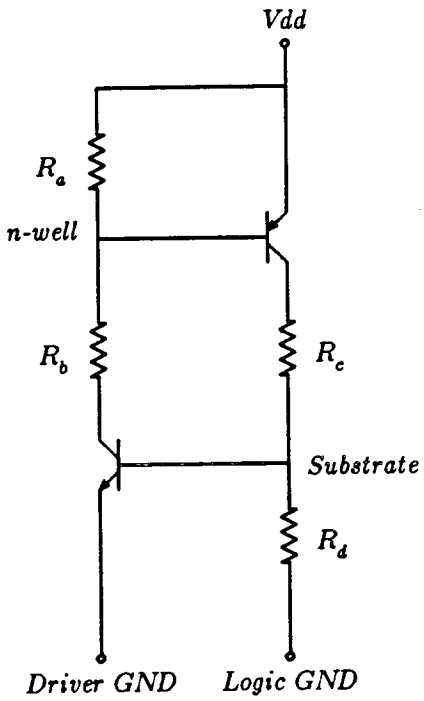

Figure 6: Latch-up schematic for chip with separate driver and logic ground pins.

well would be connected to only to the Vdd pad appropriate for that n-well. For output pads, the n-wells are usually well connected to the power supply and surrounded by guard rings. This provides that the base-emitter junction of the pnp transistor is reverse biased in all cases. Thus, the top of Figure 6 is no different than Figure 4. The base-emitter junction of the npn transistor is another case, however. In using separate grounds for the driver and logic, we would be forced to choose one or the other to ground the substrate. Let us choose to ground the substrate with the logic ground, since this will isolate any possible problems to the output pads. We see that, in the region around the output pads, the emitter of the npn transistor will be connected to the driver ground and the base will be connected, through the substrate, to the logic ground. Driving large capacitances with the drivers will cause the previously mentioned voltage spikes on power and ground. These will appear across R_d, possibly forward biasing the the base-emitter junction of the

npn transistor. By separating the logic and driver ground connections, we have created conditions which increase the chance of latch-up.

There does seem, however, to be a special case where separate power and ground for the I/O drivers would be an acceptable solution. Referring to Figure 5, we see that latch-up is initiated when the base-emitter junction of the npn transistor is forward biased by 0.6 to 0.7 volt. We might consider allowing separate power and grounds for the I/O drivers if the design of the drivers were such that logic ground and the driver ground never differed by more than some small amount. A reasonable 'small amount' might be in the range of the 0.2 volt we have already decided was a sensible choice for noise spikes in consideration of the noise margins of TTL signals. A possible strategy for power and ground design would then be to supply enough power and ground pins for the output drivers to produce voltage spikes on the I/O driver power and ground of no more than 0.2 volt. Separate power and ground pins are provided for the remainder of logic on the chip. This could only be done once it had been verified that the differences between the corresponding power rails would be small enough not to trigger latch-up. This approach has the advantage of providing additional isolation of the logic from I/O driver induced power and ground spikes over a design without separate power and ground.

2.4. Pad Loading and Delay

Capacitance is the first concern in estimating the load that an output pad will be required to drive. Typical values for chip input capacitances are 5 pF. In addition to this, each chip input is connected to PC board traces. Typical capacitance for PC boards is 2 pF per inch, although this value can vary considerably. To estimate load capacitance, we assumed that each driven load contributed 5 pF of PC board trace capacitance. Another

10 pF per output was added for the capacitance of the output pin itself and unaccounted capacitance. This gives a relationship for the load capacitance of:

$$C_{tot} = 10\,pF + (FanOut)(10pF) \tag{2}$$

For the initial analysis of pad drivers, we assumed that each output pad would drive no more than one load. Greater fan-outs are considered in a later section of the report.

Another concern of pad loading is the DC current that an output must handle. TTL buffers have worst case input currents of 20 μA for ones and -0.6 mA for zeroes. These values are for FAST logic; other TTL families have similar or lower current requirements. MOS inputs, of course require no DC current. For the present generation of integrated circuits, the DC current values generally are not a major concern. This is because pad drivers which are capable of driving the typical output load (20 pF or more) with the typical delay time (30 ns or less), can also sink the required current.

The goal for the power and ground design is to obtain the minimum delay possible in the output drive with the minimum number of power and ground pins. The primary trade-off in achieving these delays is the number of power and ground pins required. As an example, the CPU for the SPUR chip set has 109 signal pins and it is desirable to fit this chip into a 144 pin pin grid array. Initial efforts for the CPU were to try to do a pair of designs, one for 10 nsec delay in the output drivers and one for a 20 nsec delay.

2.5. Process Variation Effects on Power and Ground Design--Non-scalability of Power and Ground Design

The variation of process parameters has a profound effect on parasitic inductance behavior and hence on the chip design for power and ground. Obviously, the slowest possible transistor performance results in maximum delay time for the output drivers.

The fastest possible performance of the transistors is the worst case for parasitic inductance considerations. In the case of the fastest possible device performance, the output drivers will carry the most current and turn on the fastest. Both factors exacerbate the voltage spikes caused by inductance. The circuit illustrated in Figure 7 was simulated to demonstrate the effects of process variation. This is a typical output driver example where it was assumed that each chip lead would have a 5 nH parasitic inductance and each power and ground pin would supply 5 drivers.

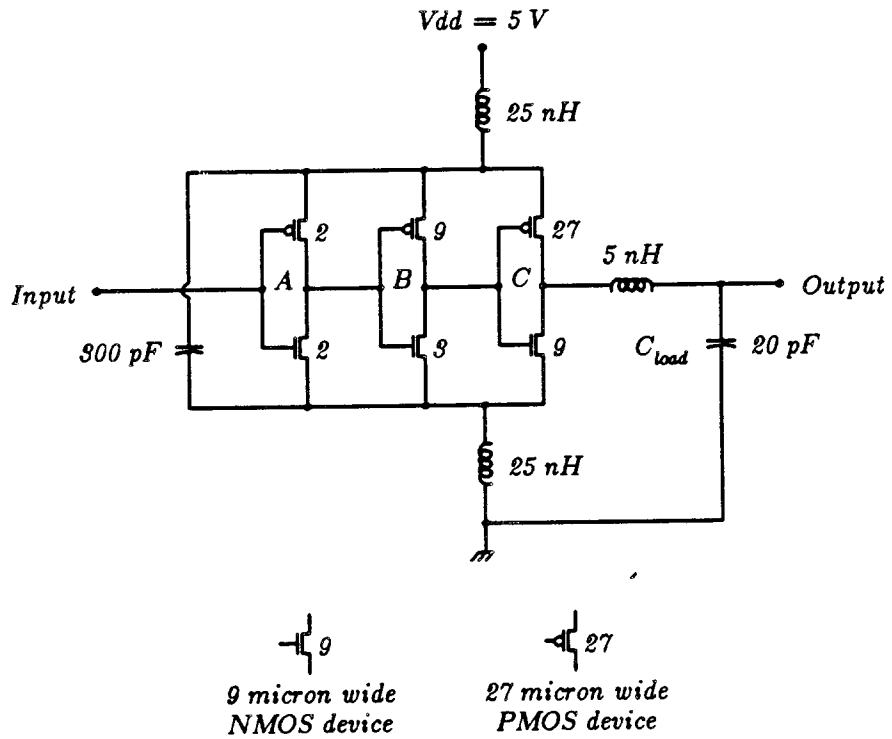

Figure 7: Output buffer example simulated to demonstrate process variation effects.

We see from the results of Table 1 that pad driver delay and worst case noise are determined at opposite ends of the process spread. The process parameters used in these simulations are those for the Xerox 2u process as described in Xerox' design rules. These parameters are given in Appendix B. In addition to the device variations, a temperature range of 0 to 100 degrees C. was assumed along with 10% supply variations.

Table 1: Pad driver delay and noise spikes for varying process conditions.

Pad Driver Delay and Noise Spikes			
Process Case	t_{phl} (Fall Time)	t_{plh} (Rise Time)	Noise Spikes
Best Case	5.0 ns	4.5 ns	0.57 V
Typical Case	6.0	7.0	0.27 V
Worst Case	9.5	14.0	0.082 V

It should be emphasized that the most important factor in output driver and power and ground design is the process spread. The speed of the typical case devices for a process is not significant in the design process. For example, in the event that the process for which a chip is designed had its typical device performance changed, without affecting the best case and worst case performance, there will be no required change in power and ground or pad driver design. This change will not affect the worst case noise on chip Vdd and ground, nor will the worst case pad drive delay be affected. Only the average performance of the chips manufactured would be affected. Widening the process spread, however, even about the same typical value, requires a redesign to either increase the number of power and ground pins or to decrease the performance of the output drivers. In general, since the process spreads do not necessarily decline as lambda decreases, the power and ground design for a chip is not scalable.

2.6. I/O Driver Approaches

A number of approaches could be considered in sizing the inverters indicated in Figure 1 for the output buffers. The various approaches to I/O driver design all are attempts to cut down on $\frac{di}{dt}$, the rate of change of current in the power and ground leads

of the chip.

The assumptions used for initial analysis of pad drivers include: Total inductance of bond wires and power and PGA leads is 5 nH or less. Good decoupling on our boards is assumed. Between the multi-layer boards and decoupling capacitors, we assume there is no noise on Vdd and GND outside of the pin grid arrays.

2.6.1. Pad Driver with Inverter Chain Ratio = 3

In the absence of parasitic inductance, the results given of Mohsen and Mead could be used [Mohs79]. Their work showed that a capacitive load could be driven in a minimum amount of time by a string of inverters which were sized in the ratio of the natural logarithm base, e (2.71828). As an approximation to this, a ratio of 3 is often chosen. That would be, referring to Figure 7, to have the ratios of the gate capacitance of the inverters A, B and C and the load capacitance, C_{load}, be 1:3:9:27. This solution would create large voltage spikes on power and ground when a wide bus was driven. Table 2 illustrates these voltage spikes for a bus driving 20 pF on each output with device parameters for the Xerox 2μ process. Table 3 is also included to illustrate the minimum pad delay possible for worst case simulations in this technology. This is important to keep in mind as an asymptotic limit, any other solution will be slower. The minor differences between entries in Table 3 are primarily a result of granularity in the simulation.

Table 2: Power and ground voltage spikes for pad driver with inverter chain ratio = 3.

Power and Ground Voltage Spikes Units: Volt				
$C : C_{load}$ [Driver Size, Wn:Wp]	Number of Drivers per Vdd and Gnd 32	16	8	4
1:3 [282:846]	3.57 V	2.57 V	1.50 V	0.71 V

Table 3: Pad driver delay for pad driver with inverter chain ratio = 3.

Pad Driver Delay Units: Nanoseconds, +/- 0.5 ns				
$C : C_{load}$ [Driver Size, Wn:Wp]	Number of Drivers per Vdd and Gnd 32	16	8	4
1:3 [282:846]	10.5 ns	11.0 ns	10.0 ns	10.5 ns

2.6.2. Reduced Speed Output Driver

The two straight forward approaches to reducing power and ground voltage spikes are to increase the number of power and ground pins and to decrease the speed of the output drivers. Tables 4 and 5 show power and ground spikes and pad driver delay for drivers of a 32 bit bus. The simulated results are for a pad driver the same as that in Figure 7, but with different device sizes. The final inverter is sized according to the ratio of its gate capacitance to the load capacitance driven. The ratios of final inverter gate capacitance to load capacitance used for these simulations were $C{:}C_{load}$ = 1:3, 1:6, 1:9, and 1:12. The ratio of gate capacitance between stages was 3 in all cases, i.e. $A{:}B{:}C$= 1:3:9. For the final inverter, the size of the p-channel device was chosen to be three times that of the n-channel device. For the Xerox 2μ n-well process, the p-channel drive is actually less than one third that of the n-channel device. The ratio of three for n-channel to p-channel size was chosen because the voltage transition required for pull-up (0.0 V to 3.0 V) doesn't require as much drive as the voltage transition required for pull-down (5.0

V to 0.2 V).

Table 4: Power and ground voltage spikes for reduced speed pad driver.

Power and Ground Voltage Spikes Units: Volt				
$C : C_{load}$ [Driver Size, Wn:Wp]	Number of Drivers per Vdd and Gnd 32	16	8	4
1:3 [282:846]	3.57 V	2.57 V	1.50 V	0.71 V
1:6 [141:423]	2.85	1.71	0.71	0.29
1:9 [94:283]	2.29	1.14	0.46	0.24
1:12 [71:212]	1.71	0.71	0.36	0.21

Table 5: Pad driver delay for reduced speed pad driver

Pad Driver Delay Units: Nanoseconds, +/- 0.5 ns				
$C : C_{load}$ [Driver Size, Wn:Wp]	Number of Drivers per Vdd and Gnd 32	16	8	4
1:3 [282:846]	10.5 ns	11.0 ns	10.0 ns	10.5 ns
1:6 [141:423]	14.5	15.0	14.5	14.5
1:9 [94:283]	18.5	19.0	18.0	18.0
1:12 [71:212]	22.5	22.5	22.0	22.0

We see that none of these pad drivers meet the 0.2 V noise spike goal, though all but the slowest pads provides better than 20 ns pad driver delays.

2.6.3. Increased Drive Ratio Inverter Chain

Note that equation (1) tell us that slowing down the speed of pad drivers by reducing their size does not reduce voltage spikes directly. What we really want is to switch

current more slowly; we don't necessarily want output drivers that source less current once they are fully turned on. Another possible approach is to have a rather large size inverter C, but a weak inverter B. The small inverter B will turn on the final inverter slowly. Once the final inverter is fully on, however, it will have a large steady-state current.

Tables 6 and 7 show the results of simulations of this so called *increased drive ratio inverter chain*. Results are shown for the example of the SPUR CPU. The SPUR CPU has a total of 96 output pins. 15 Vdd and 15 GND pins were assumed, a ratio slightly in excess of 6 output pins for each power and ground pin. The simulations shown in the two tables are all for best case speed device parameters. The delay values should be taken for comparison with the other cases of Table 7 only. The corners of the design space with the highest voltage transients and slowest driver performance were omitted from the simulations.

Table 6: Power and ground voltage spikes for increased drive ratio inverter chain.

Power and Ground Voltage Spikes Units: Volt					
$B:C$	C N-Channel Device Width				
	63	85	113	150	200
1:3	.29 V	.27 V	.36 V	-	-
1:5	.20	.24	.30	-	-
1:7	.16	.22	.26	.23	.37
1:10	-	-	.17	.24	.33
1:13	-	-	.14	.24	.26

The case of B:C=1:10 and n-channel device width of 113 μ for inverter C were selected as giving the best trade off between power and ground voltage spikes and delay. This was additionally simulated for the worst case and showed a 23.5 nanosecond delay for the worst case device parameters.

Table 7: Pad driver delay for increased driver ratio inverter chain.

Pad Driver Delay Units: Nanoseconds, +/- 0.5 ns					
$B:C$	C N-Channel Device Width				
	63	85	113	150	200
1:3	13.0 n	10.5 n	9.0 n	-	-
1:5	13.0	11.0	9.0	-	-
1:7	13.5	11.0	9.5	8.0	7.0
1:10	-	-	10.0	8.5	7.5
1:13	-	-	11.0	9.5	8.5

An additional advantage of this approach is that it provides reduced variation in delay with varying output driver load. Examples of this feature are presented in Appendix A, since this output driver was chosen for the Berkeley SPUR pad cell library. The worst case delays were found to be 23.5 ns, 27.5 ns and 43.0 ns for output loads of 20 pF, 30 pF and 60 pF respectively.

3. Package Inductance Characterization

3.1. LC Circuit Approach--Ideal Behavior

Fundamental to simulations of parasitic inductance is a characterization of packages for this parameter. As mentioned previously, the interest of this report is limited to pin grid arrays. This is because problems associated with power and ground are most pronounced in high pin-out chips, for which PGA's are the customary package.

Measurement of package parasitic inductance is not a completely straight-forward procedure. This inductance is anticipated to be in the 10 nanohenry range, which is too small to be detectable by commercial impedance bridges. The approach taken for this characterization was to create a parallel LC resonant circuit with a PGA, measure the resonant frequency and calculate the inductance. To do this, a PGA without a die was

bonded. Inside the package cavity, bonding pads were connected that had adjacent leads on the outside of the package. A capacitor of known value was soldered to the package leads. This loop of two adjacent leads was used because the attached capacitor could have the minimum possible length leads.

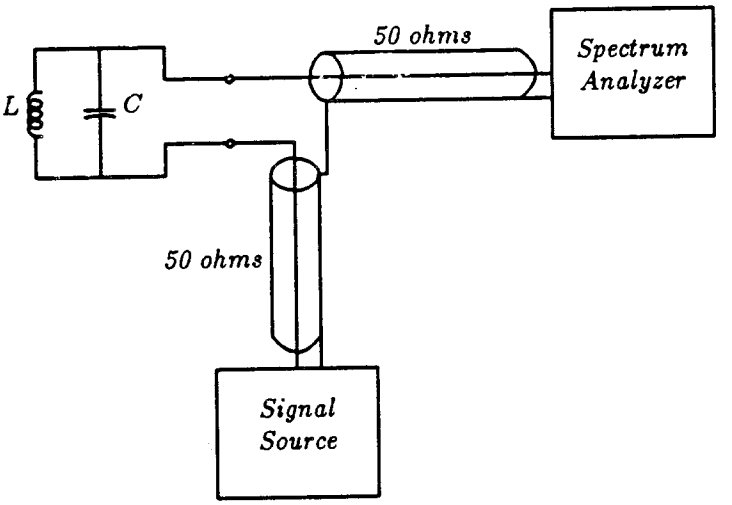

Figure 8: Instrument configuration for parasitic inductance measurements.

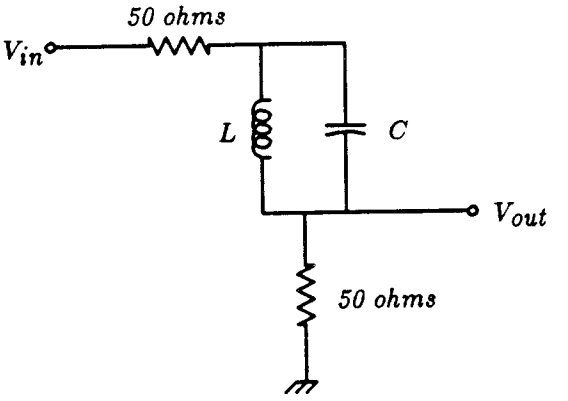

Figure 9: Equivalent circuit of parasitic inductance measurement instrument configuration.

The experimental set-up used to measure the resonant frequency is illustrated in Figure 8. The equivalent circuit of this configuration is shown in Figure 9. The resonance

for this circuit is found by considering the impedance of the parallel L and C. In the frequency domain, this is given as:

$$Z_{tot} = Z_C \,||\, Z_L \tag{3}$$

$$= \frac{1}{j\omega C} \,||\, j\omega L$$

$$= \frac{\left[\frac{1}{j\omega C}\right](j\omega L)}{\frac{1}{j\omega C} + j\omega L} \frac{j\omega C}{j\omega C}$$

$$= \frac{j\omega L}{1 - \omega^2 LC} \tag{4}$$

The pole of this expression gives the resonant frequency:

$$0 = 1 - \omega_0^2 LC$$

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}} \tag{5}$$

To make the measurement of the resonant frequency indicated by equation (5), a special cable connection was built to provide 50 ohm coax connections from the instruments to closest possible point on the PGA. The signal source used was a Fluke model 6071A synthesized RF signal source. This instrument could be programmed to sweep over a frequency range of interest. The spectrum analyzer used was an Hewlett-Packard model 8568A. The features of this instrument important to the measurement

were its storage and mathematics capability. Measurements of the resonant frequency were made first by disconnecting the LC resonator from the instruments and storing a sweep in the spectrum analyzer memory that showed the frequency response of the connection cables. Then another sweep was made with the LC resonator replaced in the circuit. This sweep was then subtracted from the first and the difference was examined to find the resonance point.

3.2. Analysis of Physical Resonant Circuit

The simplified circuit of Figure 9 ignores two important characteristics of the actual pin grid array LC resonator. These are resistive losses in the PGA traces forming the inductor and the inductance of the leads of the capacitor used.

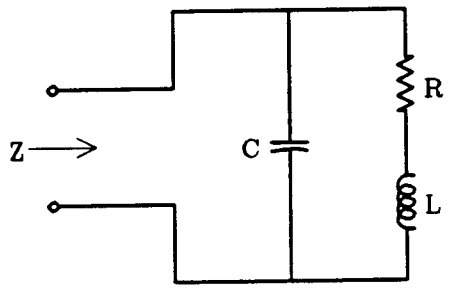

Figure 10: Circuit schematic for LC resonator with lossy inductance.

3.2.1. Lossy Inductance

A more realistic schematic diagram for the LC resonator is shown in Figure 10. The impedance expression for parallel LC circuit is changed to include the resistance loss in the inductor.

$$Z = \frac{1}{j\omega C} \Big| \Big| (R + j\omega L) \tag{6}$$

$$= \frac{\left[\frac{1}{j\omega C}\right](R+j\omega L)}{\frac{1}{j\omega C} + R + j\omega L}$$

$$= \frac{R+j\omega L}{(1-\omega^2 LC) + j\omega RC}$$

$$= \frac{R(1-\omega^2 LC)+\omega^2 LRC + j\left[\omega L(1-\omega^2 LC)-\omega R^2 C\right]}{(1-\omega^2 LC)^2 + \omega^2 R^2 C^2} \qquad (7)$$

Note that the resonance is at the same frequency, as given by the zero of the $1-\omega^2 LC$ term. Plots of equation (7) for a number of different conditions of interest are given in Figure 11. The impedance scale of Figure 11 is given in decibels. This is referenced to the low frequency impedance, i.e. the DC resistance of the inductor. The conditions which are fixed by the PGA physical parameters include $L = 10\ nH$ and $R = 1\ \Omega$. Clearly, we see that the parasitic inductance measurement must be made at a frequency in excess of 10 MHz in order to avoid a condition where the resonance is dominated by losses in the inductance. Initially, the inductance characterization was to have been done using $f_0 = 1$MHz. After consideration of the effects of a lossy inductance, this was changed to 100 MHz. This changed the capacitor required from 0.3 μF to 250 pF.

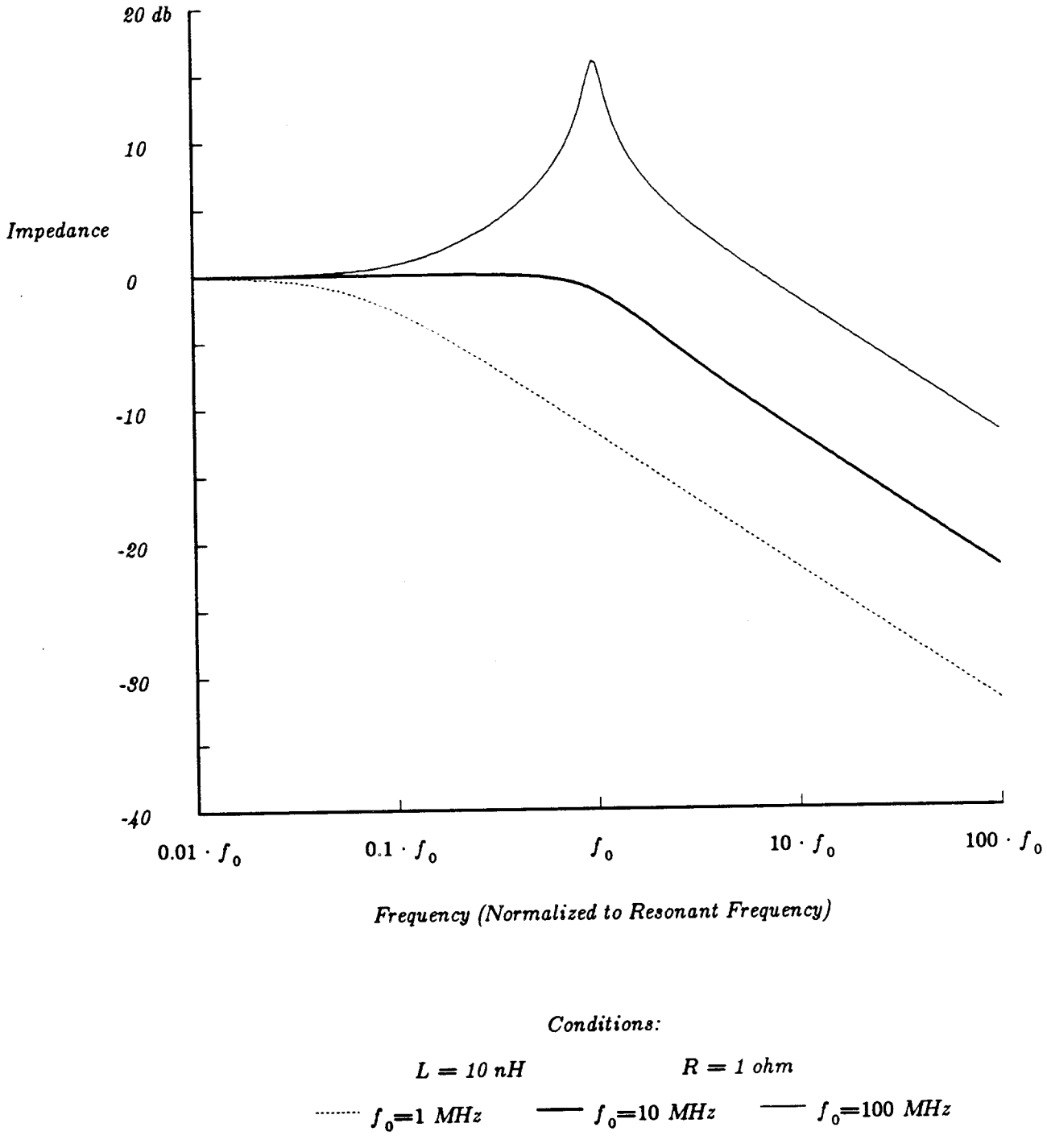

Figure 11: Frequency responce of PGA LC resonator with lossy inductance for various resonant frequencies.

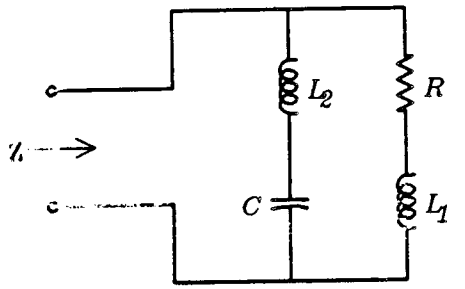

Figure 12: Circuit schematic for LC resonator with lossy inductance and capacitor leads with parasitic inductance.

3.2.2. Inductance Parasitic to Package Characterization

Another complication of the parasitic inductance characterization is that the leads of the capacitor soldered to the PGA has parasitic inductance itself. It is important to understand the significance of this inductance to the measurement made. As indicated by Figure 12, the impedance of the LC circuit is given as:

$$Z = \left[\omega L_2 + \frac{1}{j\omega C}\right](R + j\omega L_1) \tag{8}$$

$$= \frac{\left[j\omega L_2 + \frac{1}{j\omega C}\right](R + j\omega L_1)}{\left[R + j\omega L_1 + j\omega L_2 + \frac{1}{j\omega C}\right]}$$

$$= \frac{\left[(R-\omega^2 L_2 RC)(1-\omega^2 L_1 C-\omega^2 L_2 C) + \omega RC(\omega L_1-\omega^3 L_1 L_2 C)\right]}{(1-\omega^2 L_1 C-\omega^2 L_2 C)^2+(\omega RC)^2} + \tag{9}$$

$$\frac{j\left[(\omega L_1-\omega^3 L_1 L_2 C)(1-\omega^2 L_1 C-\omega^2 L_2 C) - \omega RC(R-\omega^2 L_2 RC)\right]}{(1-\omega^2 L_1 C-\omega^2 L_2 C)^2+(\omega RC)^2}$$

Note that from the denominator we see that resonance occurs for the condition:

$$0 = 1-\omega_0^2 L_1 C-\omega_0^2 L_2 C \tag{10}$$

The resonant frequency is then given as:

$$\omega_0^2 = \frac{1}{C(L_1+L_2)} \tag{11}$$

The resonant frequency is then the frequency due to the sum of the inductances of the package and the leads of the capacitor. Figure 13 helps to illustrate the importance of this result. The leads attached to the RC circuit are similar in size to the external PGA leads and the leads of the attached capacitor. Equation (11) tells us that the exact placement of these leads is not significant to the measured resonant frequency. This was experimentally verified with resonator circuits with particularly long capacitor leads. Equation (11) also tells us that a measurement of the parasitic inductance of the leads of the capacitor will have to be made to extract the inductance of the PGA alone.

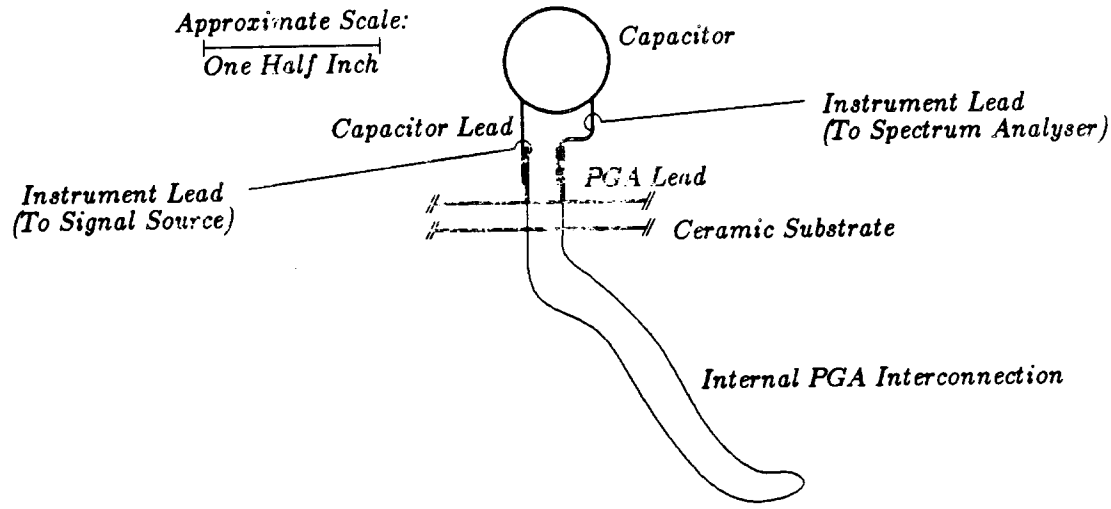

Figure 13: Sketch of capacitor bonded to PGA for LC resonator.

3.2.3. Methods to Separate Inductances

Three methods are proposed for extracting the parasitic inductance of the capacitor from the RC resonator. The two experimental techniques are the capacitor lead loop and resonance magnitude variation. In addition to these, an analytic method is presented in Appendix D.

3.2.3.1. Capacitor Lead Loop

The approach used for the capacitor lead loop is the same as that for the package characterization. The difference is that the pin grid array is omitted from the circuit; the inductance is formed from a loop of the capacitor's leads which approximates the geometry of the capacitor's leads in Figure 13. The resonant frequency is considerably higher for this small inductance than for the circuit including the package. For the package characterization with a 250 pF nominal capacitance, the resonant frequencies were in the 60 - 90 MHz range. The resonant frequency of the capacitor lead loop with the same nominal capacitance was in the 120 - 160 MHz range. Also, as indicated by the

results of the analysis of the lossy inductance, the amplitude of the resonance is quite small. This was seen to be in the 1.0 to 1.5 db range. Table 6 summarizes results of measurements of the capacitor lead loop.

Table 8: Resonant frequency and inductance of the capacitor lead loop.

Data Summary for Capacitor Lead Loop Inductance			
Capacitor	Capacitance	Frequency	Inductance
68	215.4 pF	155.6 MHz	2.42 nH
47	220.3	152.1	2.48
63	224.2	129.6	3.37
67	258.8	129.4	2.92

We conclude from the results of Table 6 that 2.4 nH is a lower limit for the inductance of the leads of the capacitor used for the package characterization.

3.2.3.2. Resonance Magnitude Variation

Another method which could be used to determine the inductance of the capacitor leads depends upon measuring the magnitude of the resonance. Equation 9 may be specialized to resonance and manipulated algebraically to obtain the relationship:

$$Z(\omega=\omega_0) = \frac{(\omega_0^2 R L_1 C - j\omega_0 R^2 C)\left[1-\dfrac{L_2}{L_1+L_2}\right]}{\omega_0^2 R^2 C^2} \tag{12}$$

Clearly, the magnitude of the resonance is a strong function of L_2.

There are two experimental methods that could be used to extract the parasitic inductance of the capacitor with this technique. The first would be to attempt to accurately place the test leads indicated in Figure 13. Measurements of the inductance magnitude could be made with the test leads at the junction of the PGA and capacitor leads and also as close to the capacitor body as possible. The difference between the resonance magnitudes would be indicative of the capacitor lead inductance. The other technique would be to take two measurements of the resonance magnitude where one of the leads was displaced a measured distance between the measurements. An inductance per unit length for the capacitor leads could then be extracted. Neither of these techniques were pursued on account of the success of the capacitor lead loop technique.

3.3. Characterization Results

Table 7 gives the results of the package parasitic inductance measurements. The characterized package, a 144 lead pin grid array manufactured by Kyocera, is symmetric about its center point. For each pin, there is an equivalent pin 90 degrees away. These equivalent pins are grouped together in Table 7. The pin number references are explained in Appendix C. The resonant frequency shown is the mean of 3 measurements. 'Indicated Inductance' is the inductance as computed from the resonant frequency before correction for the parasitic inductance of the capacitor. This is the inductance per lead, since the LC resonator gives a response for two leads. The last column includes the correction of 1.2 nH (2.4 divided by 2) for the parasitic inductance of the capacitor.

We conclude from Table 7 that the inductance of the best leads of the PGA is in the range of 5.4 to 6.1 nH. This is for pins H3, J3, N8, N9 H13, G13, C8 and C7. These pins are located at the middle of each side of the package cavity, with pins at the inside of the

Table 9: Results of package parasitic inductance evaluation.

Data Summary for Pin Grid Array Characterization				
Pin Numbers	Capacitance	Mean Frequency	Indicated Inductance	Corrected Inductance
H3-J3	262.7 pF	85.62 MHz	6.58 nH	5.4 nH
N8-N9	234.8	85.82	7.32	6.1
C7-C8	220.7	89.70	7.13	5.9
F1-G1	267.4	68.84	9.96	8.8
Q6-Q7	231.5	73.94	10.01	8.8
L2-L3	233.1	68.04	11.74	10.5
N11-P11	232.0	64.84	12.98	11.8
B5-C5	221.7	64.88	13.57	12.4
D3-E3	252.4	74.90	8.94	7.7
N4-N5	230.1	79.36	8.74	7.5
L13-M13	231.5	79.56	8.64	7.4
C11-C12	202.0	87.28	8.23	7.0
A3-B3	230.5	63.18	13.77	12.6
P13-Q13	220.8	64.18	13.98	12.8
A1-B1	262.2	57.27	14.50	13.3
Q1-Q2	231.8	60.88	14.74	13.5
P15-Q15	236.3	57.66	16.12	14.9
A14-A15	284.3	52.92	15.91	14.7

array. Thus, they have the shortest interconnection distance internal to the package. These pins are also advertised by the manufacturer to have low resistance, 250 $m\Omega$, versus 900 $m\Omega$ for other pins. It should be expected that lowest the resistance pins also should

be the lowest inductance pins, although there is no strict relationship between resistance and inductance. The other pins range from 9 nH to 15 nH. The pins D3, N4, M13 and C12 are exceptions. These pins are specified to have a resistance of 300 $m\Omega$. Because of the measurement technique, the value of the inductance of these pins had to be taken along with that of a neighboring pin of presumably higher inductance. It is thus anticipated that the values given for the inductance of these pins is in error on the high side.

4. Pad Design

4.1. Issues for Pad Design in High Pin-out Chips

Areas of concern for pad design for high pin-out integrated circuits vary to some extent from those in conventional chips. Typically, these circuits are pad limited. That is, their sizes are determined by the packing density of the I/O pads along their sides. Economical manufacture then requires pad designs which allow pads to be spaced on a 200 micron pitch, i.e., the center-to-center spacing of pads is 200 microns. 200 microns is the lower limit of current wire bonding technology. As mentioned before, the high pin-out chip will typically be packaged in a pin grid array. This imposes some other constraints on the pads. PGA's are square and for ease of bonding, it is best to have an equal number of pads on each side of a chip. PGA's with more than 150 pins often have a double tier of bonding pads in their package cavities. To utilize these pads, the chip will have to have a double row of pads as well. As a result of the package characterization results of the previous section, it is important to place power and ground pins at the center of the sides of the chip to make use of the low inductance leads located there.

As in previous generations of pad design for CMOS circuits, latch-up and electrostatic discharge (ESD) are also important concerns. Figure 14 is a schematic for the input protection structure.

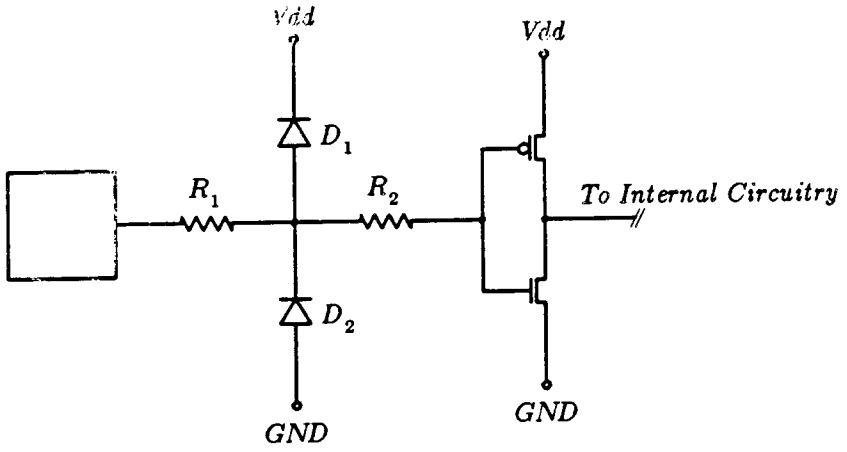

Figure 14: Schematic diagram of input protection structure.

As far as ESD protection is concerned, the diodes D_1 and D_2 are the most important feature of Figure 14. When the chip is connected to a power supply and is struck by a high voltage pulse, one of the diodes will forward bias to dissipate the charge of the pulse. Resistor R_1 has a value of about 50 Ω. This is present to prevent high currents from destroying the input in the event that the chip is improperly connected. Resistor R_2 has a value of about 500 Ω. The value of this resistor is somewhat questionable. Some designers would place it in the input protection device arguing that, to protect the gates, the current path through the diodes should be lower than that to gates. Others would argue that no protection can be gained by achieving a voltage drop across R_2; if there ever is a voltage drop across R_2, the current that caused it has already destroyed the gates it was supposed to protect. In addition to the structures shown in Figure 14, diode connected transistors are occasionally added to input protection structures. These may be in parallel with standard input protection diodes or as a substitute for them, especially in

NMOS processes where both types of diodes are not readily available. Diode connected transistors for input protection need not be formed by the thin gate oxide. As an alternative, the thick isolation oxide may be used. This would provide a device with a threshold several times the usual power supply voltage. The inverter indicated in Figure 14 is usually a TTL input buffer. It is ratioed to transition between the 0.8 V maximum TTL logic zero level and the 2.0 V minimum TTL logic one level. ESD protection for output pads is not specificly addressed. This is because the output drivers act as oversized protection diodes which generally keep this pad from being damaged by ESD.

Referring to Figures 4, 5 and 14, consider the currents involved when the ESD protection diodes are forward biased. If the input (or output) pad goes more than a diode turn-on voltage below GND level, the N+ junction to the P- substrate will forward bias. If the input pad goes more than a diode turn-on voltage above the supply level, the P+ junction to the n-well will be forward biased. These cases cause substrate and well currents which, as mentioned in the section on clean and dirty supply lines, are latch-up hazards. On account of this hazard, it is desirable to design the pads in such a way that the feedback path, as illustrated in Figure 5, which causes latch-up is broken. Guard rings and spacing rules are the usual method by which this is done. The cross-section of an input protection structure is shown in Figure 15. Figure 16 illustrates how guard rings work. Take, for example, the p+/n+ diode at the right of Figure 15. When this becomes forward biased, there is injection of electrons into the substrate. Avoiding latch-up requires that the protection structure limit flow of these electrons in the substrate. The adjacent n-well, the guard ring, removes these unwanted carriers from the substrate. Note that the electrons injected into the substrate only become a problem when the travel beyond the region around the p+/n+ diode and n-well guard ring. The other circuitry on the chip includes p+ junctions in n-well which complete the n-p-n-p structure which is

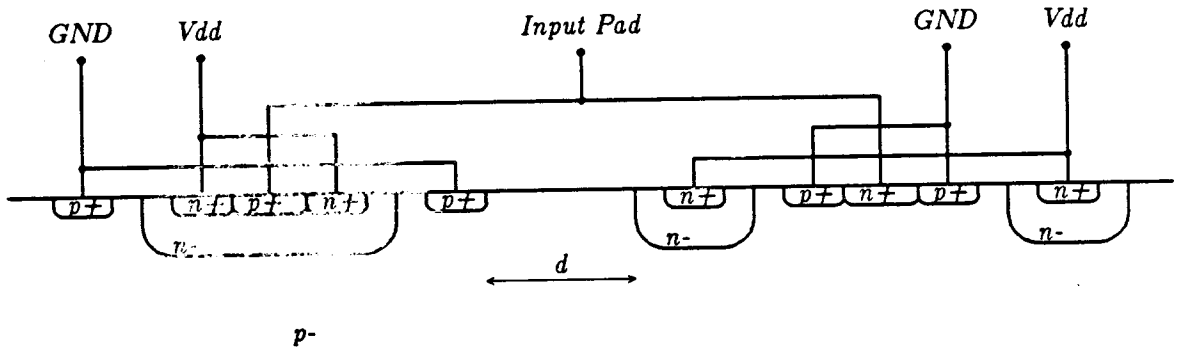

Figure 15: Input protection structure cross section showing guard rings.

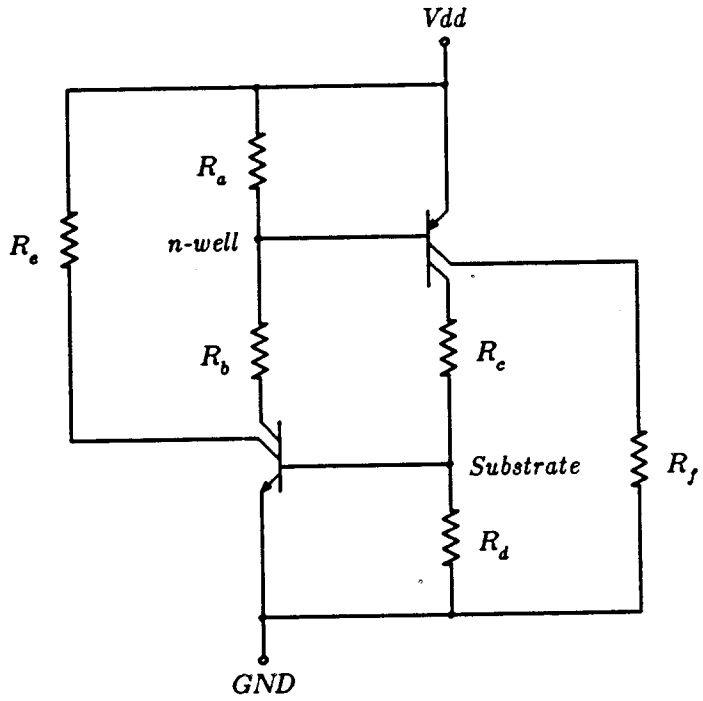

Figure 16: Schematic of bipolar transistors in input protection structure including guard rings.

susceptible to latch-up. Figure 16 illustrates this by means of a schematic of the parasitic junction transistors involved. The npn transistor is the equivalent of the p+/n+ diode and n-well guard ring. This npn transistor has two collectors. One is the n-well guard ring and the other is the n-well at the left of Figure 15, or any other n-well containing p+ junctions. The current which is collected by the n-well won't cause any problems. It is

dissipated through R_c, which is presumed to be a very small resistance. Alternatively, current collected in an n-well has the potential to cause a voltage drop on R_a and R_b, which would turn on the pnp transistor and feedback to the npn transistor.

What is it that we can do to ensure that current injected into the substrate is collected by the guard ring, instead of by junctions in the circuitry? First, we must make the guard ring as effective a collector as possible. The guard ring should completely surround the p+/n+ diode and be as close to the p+/n+ diode as possible. It should be wide and have a large area. Also, n-wells for the remainder of the circuitry, as well as the n-well for the other input protection diode, should be spaced as far as possible from p+/n+ diode. That is, the distance d in Figure 15 should be as large as possible.

Although only the case of the substrate/n+ diode is discussed in the previous two paragraphs, the same argument applies to the n-well/p+ diode and p+ guard ring.

Note that if it were possible to have a perfectly collecting guard ring of either type for all the circuits on the chip, the feedback loop for latch-up would be broken. This is effectively the solution obtained in building CMOS circuits on an epitaxial substrate. If the entire substrate, except for the top 5 microns, were heavily doped and grounded p+, this substrate could collect holes in the substrate more effectively than a guard ring. As an example, in the Xerox process used in for the SPUR project the n+ to p+ design rule is 12 micron. The heavily doped substrate of epitaxial silicon only 5 microns away is much more effective. Moreover, the epitaxial substrate protects all circuits in the chip--not just the few places where the added area of a guard ring is tolerable.

4.2. Description of Berkeley SPUR Pads

A set of twelve pads were designed for the Berkeley SPUR project. Of these, seven are compatible with a single row of bonding pads on the periphery of a chip and five are compatible with a double row of bonding pads. Within each of these two sets, all pads tile properly when abutted together. All pads are oblong in shape. The long dimension is perpendicular to the edge of the chip since the intended application of the pads is for high pin-out chips. lots of the pads are provided in the User's Guide of Appendix A.

The single row pads are 650 microns high and 200 microns wide. The bonding pads are 100 microns by 200 microns. This is the size of the passivation (glass) opening for the pad. The large size pad is provided to allow for rework of bonding wires. For the input pads, the protection diode is 12 microns by 98 microns. The output drivers are of the following sizes: p-channel: W = 450 microns, L = 2.0 microns, n-channel: W = 113 microns. The input protection diodes and output driver devices have guard rings at least 16 microns wide. A 65 micron ground bus and a 96 micron Vdd bus is provided. These bus widths are set to disallow accidentally placing circuitry in positions inside the chip where they might cause latch-up. The wide power and ground busses also are significant in reducing parasitic inductance on the chip.

The double row pads are 1200 microns high and 200 microns wide. The bonding pads are 100 x 100 microns. These smaller pads were chosen because of the large vertical dimension of the pad cells. The input protection diodes, output drivers and guard rings are of the same size as for the single row pads. The Vdd bus is 65 microns wide. There are two ground busses. The one at the periphery of the chip is 65 microns wide. The inside ground bus is 106 microns wide. The layout of the double row pads also disallows use of the pads in a way which would risk latch-up. Figure 17 illustrates the general

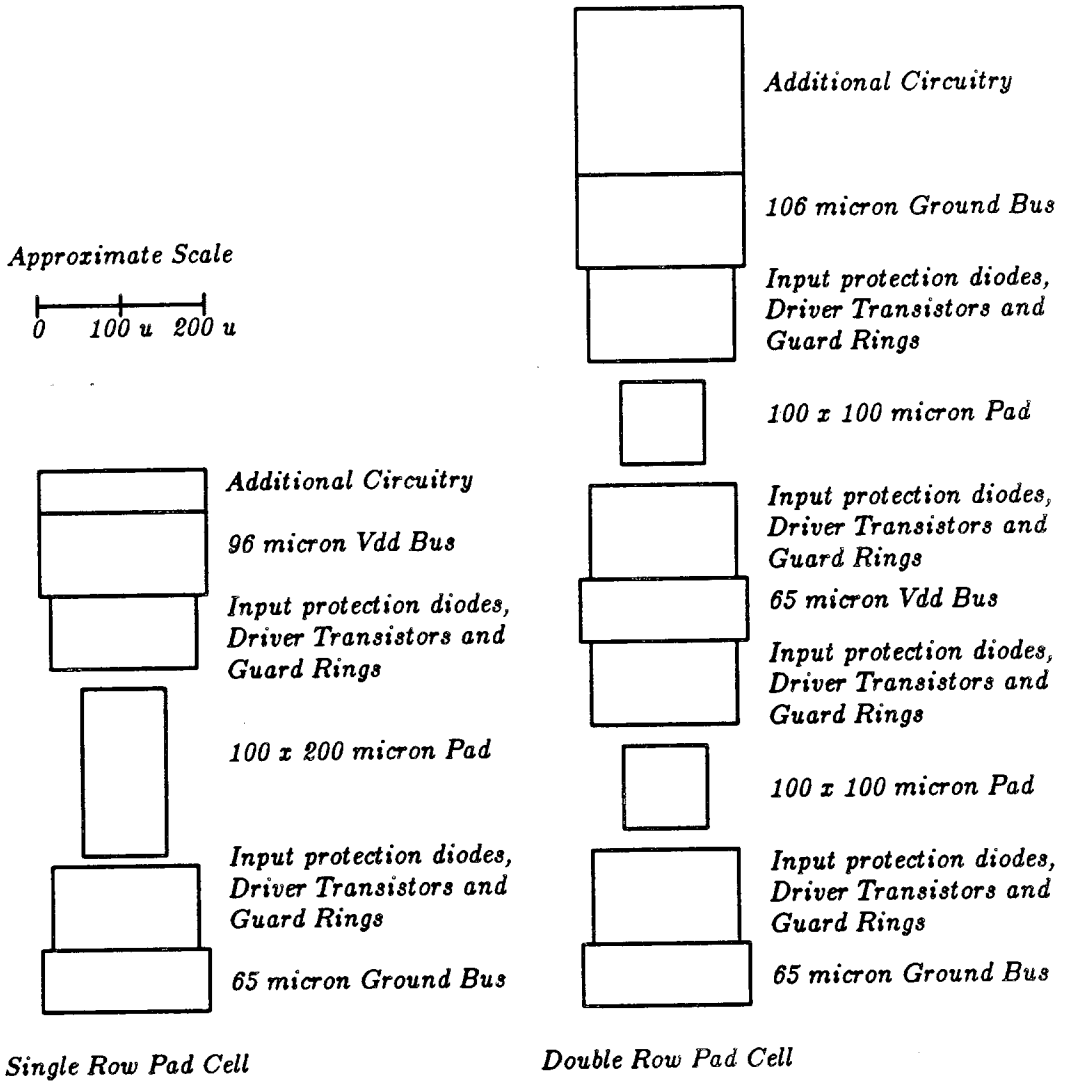

Figure 17: Diagram of single and double row bonding pad cells.

layout of both sets of pads.

The general rule of thumb for use of these pads is to include one power and one ground pin for each 6 output pins. The power and ground pins should be placed in the same vicinity as the corresponding output pins. 1500 microns is the recommended maximum distance. This is on account of inductance present on the chip itself. As much as possible, the pins of a PGA used for power and ground should be near the center of

each side of the pin array. Preferably, the pins on the inner ring of pins should be used. The pins in the far corners of the PGA have the highest inductance, as seen in the section on PGA characterization.

Since both n-well contacts and p-well contacts are explicitly included in the layout for these pads, the pad cells could, strictly from a layout standpoint, be used in either a p-well or an n-well process. From a circuit standpoint, the pads are much less process independent. Obviously, the pads would be slower in a process whose average performance was less than that of the Xerox process. There would be additional voltage spiking on the power and ground lines if these pads were used in a process whose best case performance was faster than the Xerox process. There could also be problems if these pads were used in a process where the ratio of the n-channel device performance to the p-channel device performance was different than in the Xerox process. If the device performance were skewed, the V_{IL} and V_{IH} of TTL input buffers would change and there would be a risk of current spikes through the output drivers. This could occur if both transistors in the output buffer were simultaneously in the *on* state briefly.

At present, the pad cells are located in the directory */bnf2/spur/kell/cad/spurpad* on the UC Berkeley *envy* file server. Along with the cells is the file *currentpads* which is a directory of the current pad revisions. All pads are marked with a revision number and date at the upper right hand corner.

5. Summary and Conclusions

This report has illustrated that high speed current switching in integrated circuits causes voltage transients on chip power and ground busses. This noise affects inputs and must be minimized by proper design of the output buffers and placement of appropriate

Table 10: File names and functions of pad cells.

File Names and Functions of Pad Cells	
Pad Cells for a Single Row of Pads	
File Name	Function
iopad.mag	Tri-state input or output pad
inpad.mag	Non-inverting TTL input pad
inpadck.mag	Clocked Non-inverting TTL input pad
outpad.mag	Non-inverting output pad
outpadck.mag	Clocked Non-inverting output pad
vddpad.mag	Vdd
gndpad.mag	Ground
Pad Cells for a Double Row of Pads	
File Name	Function
ioio.mag	Non-inverting TTL input pad
inin.mag	Clocked Non-inverting TTL input pad
outout.mag	Non-inverting output pad
vddgnd.mag	Clocked Non-inverting output pad
gndvdd.mag	Vdd

numbers of power and ground pins on the chip. It was seen that pad driver and power and ground design are specific to each chip and each process--power and ground designs are not generally scalable. Characterization of packages is quite important. Parasitic inductance varies by as much as a factor of three from pin to pin on a pin grid array. As dimensions decrease through scaling, integrated circuit pin-outs, bus widths and clock frequencies all are increasing. Each of these trends further complicates power and ground design.

A number of areas for further investigation present themselves. Experimental verification of both the power and ground noise simulations, as well as the pad cells would be valuable. Additional work could be done examining the assumptions used for the power and ground design. Assuming all conditions to be worst case leads to a perhaps overly conservative design. It may be acceptable for a system to exhibit a certain failure rate at final test, in exchange for enhanced performance from a more aggressive design. Package and chip inductance values are difficult to estimate with our present design tools

Our current tools can effectively extract capacitance because the parallel plate capacitor model is a reasonable description of most situations in circuit design. Inductance, by contrast, is highly dependent on the geometry of package leads and chip busses. A design tool which, given a description of a package, chip or printed circuit board, could calculate the inductance of the leads could be valuable.

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Appendix A: User's Guide to Berkeley SPUR Pad Cell Library

NAME

iopad

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Iopad is a tri-state output pad driver or input buffer which is compatible with TTL signal levels.

PROPERTIES

Size

200 x 650 λ

Inputs

output: Chip signal to be output when output is enabled
enable: Output enable control

Output

pad: Driven output signal input: Buffered version of signal at pad

Delay

		Output Driver Load		
		20 pF	30 pF	60 pF
Worst Case	t_{input}	27.5 ns	33.0 ns	48.5 ns
	t_{enable}	26.5	33.0	48.5
Typical Case	t_{input}	16.5	20.0	28.5
	t_{enable}	14.5	18.0	27.0
t_{input}: Delay from signal input to valid output. t_{enable}: Delay from enable input to valid output.				

		Input Buffer Load		
		0.5 pF	1.0 pF	1.5 pF
Worst Case	t_{input}	12.0 ns	13 ns	13.75 ns
Typical Case	t_{input}	6.75	7.5	8.25

DC Current Capability

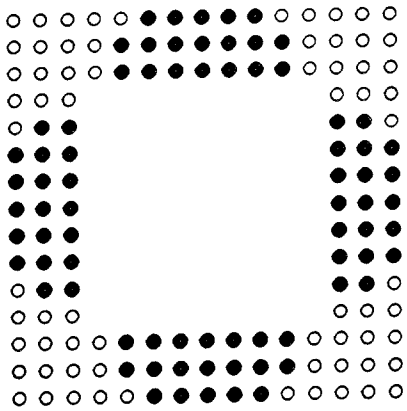
Sourced by I/O Driver: 4.50 mA minimum
Sunk by I/O Driver: -3.00 mA minimum

DESCRIPTION

Iopad is a output driver (when *enable* is high) or an input buffer (when *enable* is low). When *enable* is low, the output is in a high impedance state. TTL output levels of $\leq 0.4\ V$ for logic zeroes and $\geq 2.4\ V$ for logic ones are provided. Input levels are $\leq 0.8\ V$ for logic zeroes and $\geq 2.0\ V$ for logic ones. The output driver transistors act as diodes for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection.

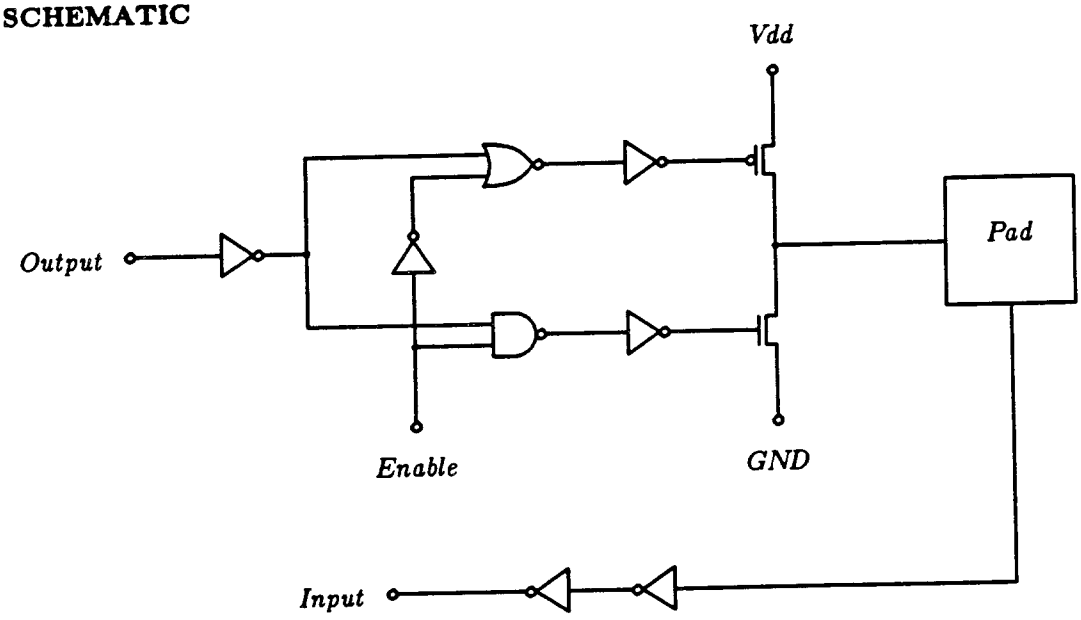
SUPPLY REQUIREMENTS

For every six instances of outpad, outpadck or iopad, one instance of vddpad and one instance of gndpad must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

SCHEMATIC



STATUS

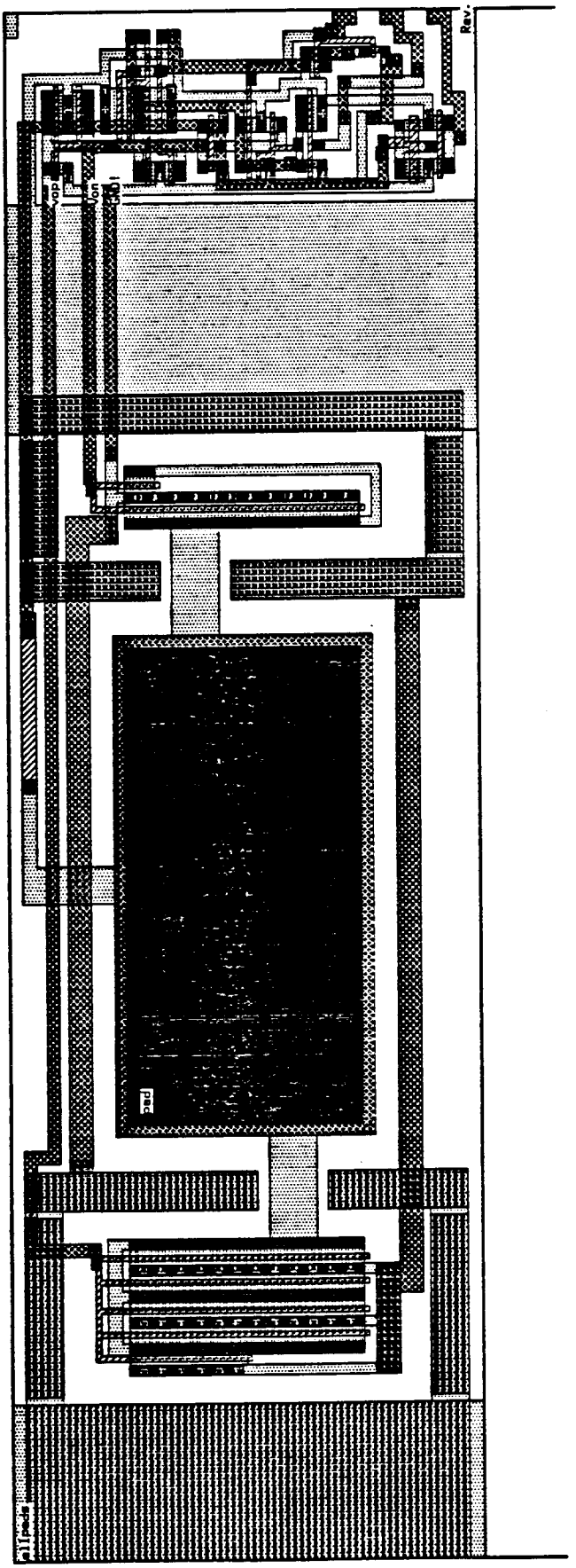
Circuit performance simulated using SPICE.

SEE ALSO

outpad, outpadck

BUGS

Not process independent. Power and ground requirements and TTL input levels are dependent on the Xerox 2 μ process device performance.


Rev.
pad
pad

NAME

inpad

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Inpad is a non-inverting input pad which is compatible with TTL signal levels.

PROPERTIES

Size

200 x 650 λ

Input

pad: Bonding Pad

Output

input: Buffered version of signal at pad.

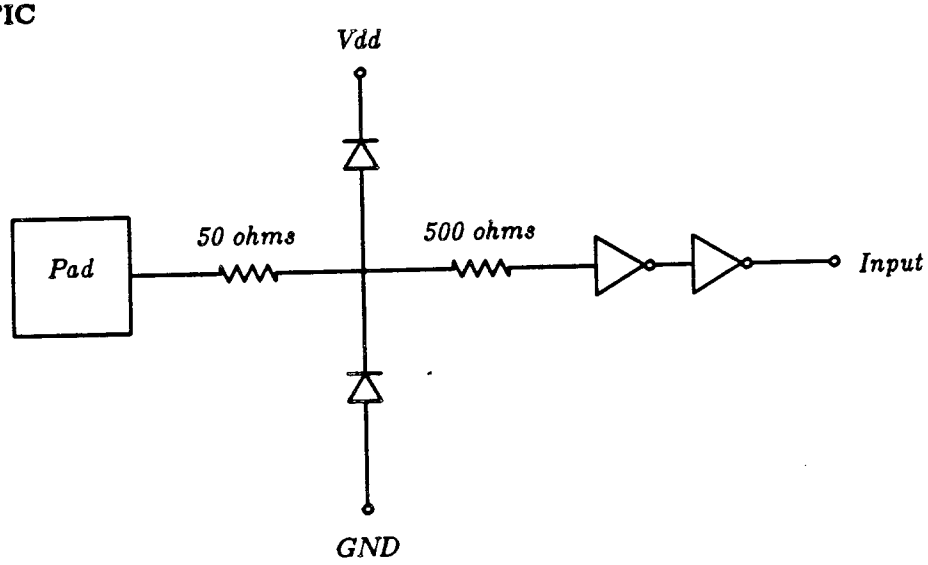
Delay

	Input Buffer Load		
	0.5 pF	1.0 pF	1.5 pF
Worst Case	12.0 ns	13.0 ns	13.75 ns
Typical Case	6.75	7.5	8.25

DESCRIPTION

Inpad is a non-inverting input pad which responds to TTL levels. TTL input levels are $\leq 0.8\ V$ for a logic zero and $\geq 2.0\ V$ for a logic one. Two diodes and two resistors are provided for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection.

SCHEMATIC



STATUS

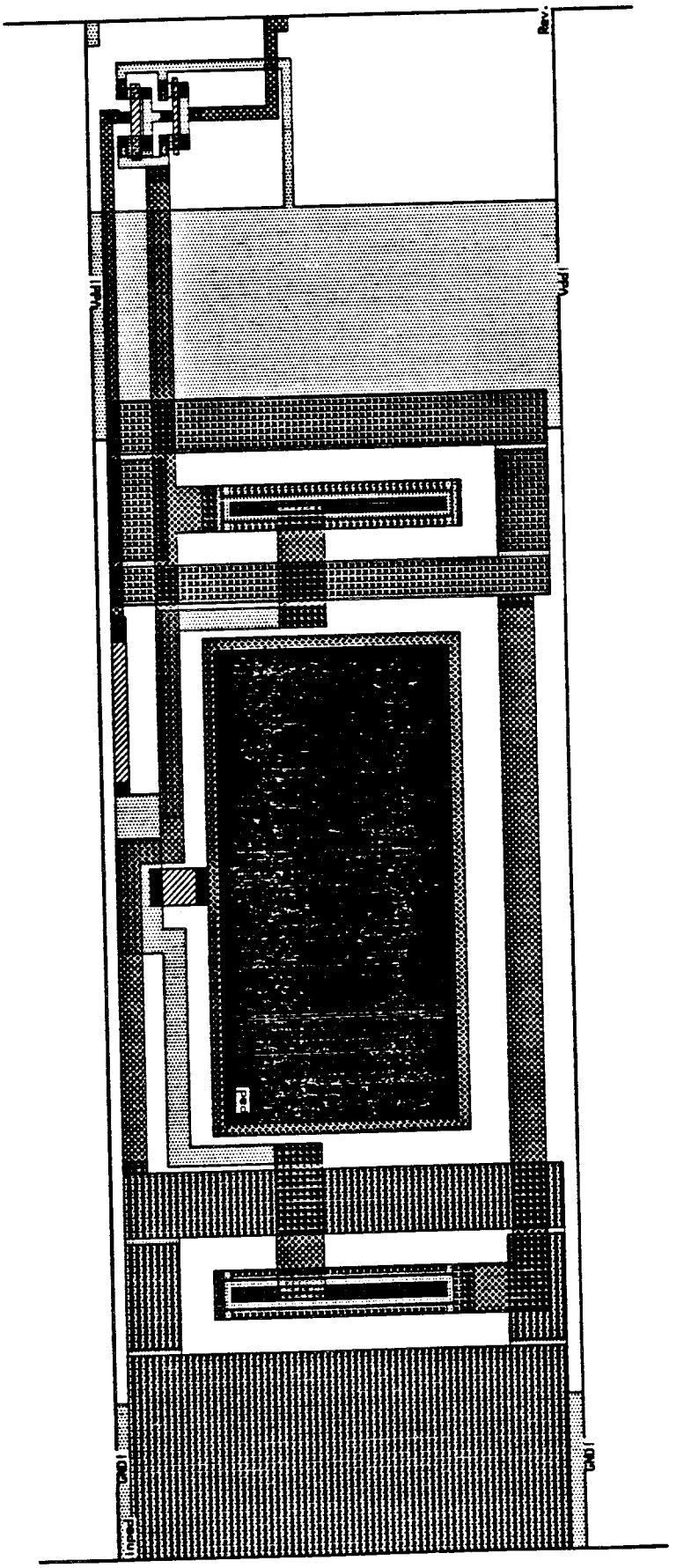
Circuit performance simulated using SPICE. ESD and latch-up performance to be evaluated pending test chip fabrication.

SEE ALSO

Inpadck

BUGS

Not process independent. TTL input level is dependent on the Xerox 2 μ process device performance.



NAME

inpadck

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Inpadck is a clocked non-inverting input pad which is compatible with TTL signal levels.

PROPERTIES

Size

200 x 650 λ

Input

pad: Bonding Pad
clock: Clock input
clockb: Inverted clock input

Output

input: Clocked, buffered version of signal at pad.

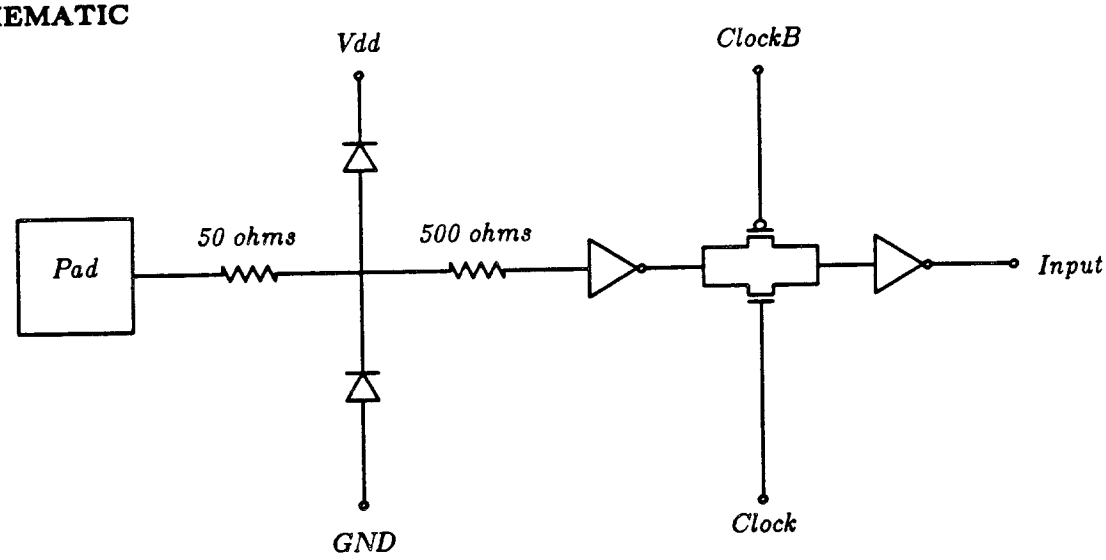
Delay

		Input Buffer Load		
		0.5 pF	1.0 pF	1.5 pF
Worst Case	t_{input}	16.5 ns	17.5 ns	18.75 ns
	t_{clock}	6.25	9.5	13.0
Typical Case	t_{input}	8.75	9.25	10.25
	t_{clock}	3.5	4.75	6.25
t_{input}: Delay from signal input to valid output. t_{clock}: Delay from clock input to valid output.				

DESCRIPTION

Inpadck is a clocked non-inverting input pad which responds to TTL levels. TTL input levels are $\leq 0.8\ V$ for a logic zero and $\geq 2.0\ V$ for a logic one. The two diodes and two resistors are provided for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection. The pass gate ensures that the buffer output changes only when the *clock* input is valid. The *clockb* input must be the inverted version of the *clock* input.

SCHEMATIC



STATUS

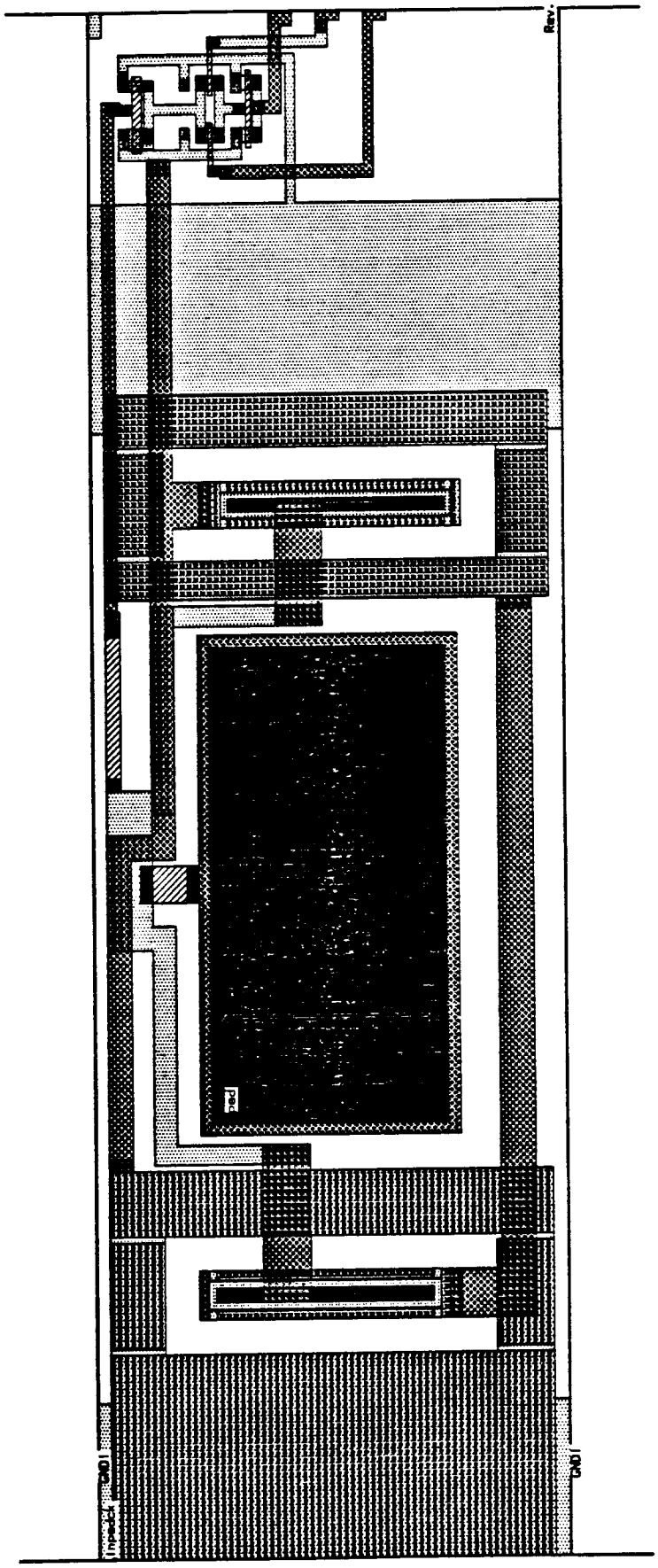
Circuit performance simulated using SPICE. ESD and latch-up performance to be evaluated pending test chip fabrication.

SEE ALSO

Inpadck

BUGS

Not process independent. TTL input level is dependent on the Xerox 2 μ process device performance.


Rev
PAD
GND!
inpadck
GND!

NAME

outpad

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Outpad is a non-inverting pad driver which is compatible with TTL signal levels.

PROPERTIES

Size

200 x 650 λ

Input

output: Chip signal to be output

Output

pad: Driven output signal

Delay

	Output Driver Load		
	20 pF	30 pF	60 pF
Worst Case	23.5 ns	27.5 ns	43.0 ns
Typical Case	14.0	17.0	25.5

DC Current Capability

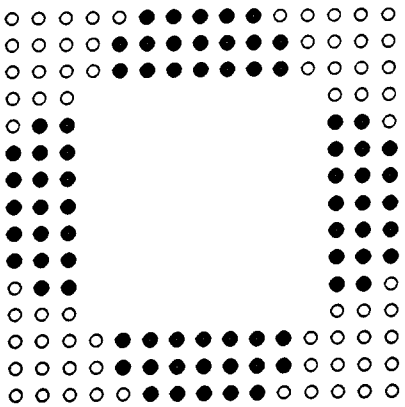
Sourced by Output Driver: 4.50 mA minimum
Sunk by Output Driver: -3.00 mA minimum

DESCRIPTION

Outpad is a non-inverting output pad which provides TTL levels. Worst case TTL output levels are $\leq 0.4\ V$ for a logic zero and $\geq 2.4\ V$ for a logic one. The output driver transistors act as diodes for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection.

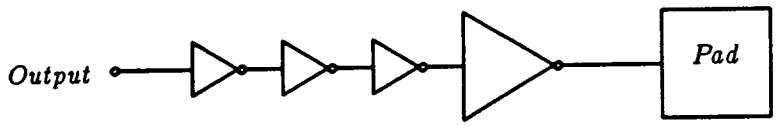
SUPPLY REQUIREMENTS

For every six instances of outpad, outpadck or iopad, one instance of vddpad and one instance of gndpad must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

SCHEMATIC



STATUS

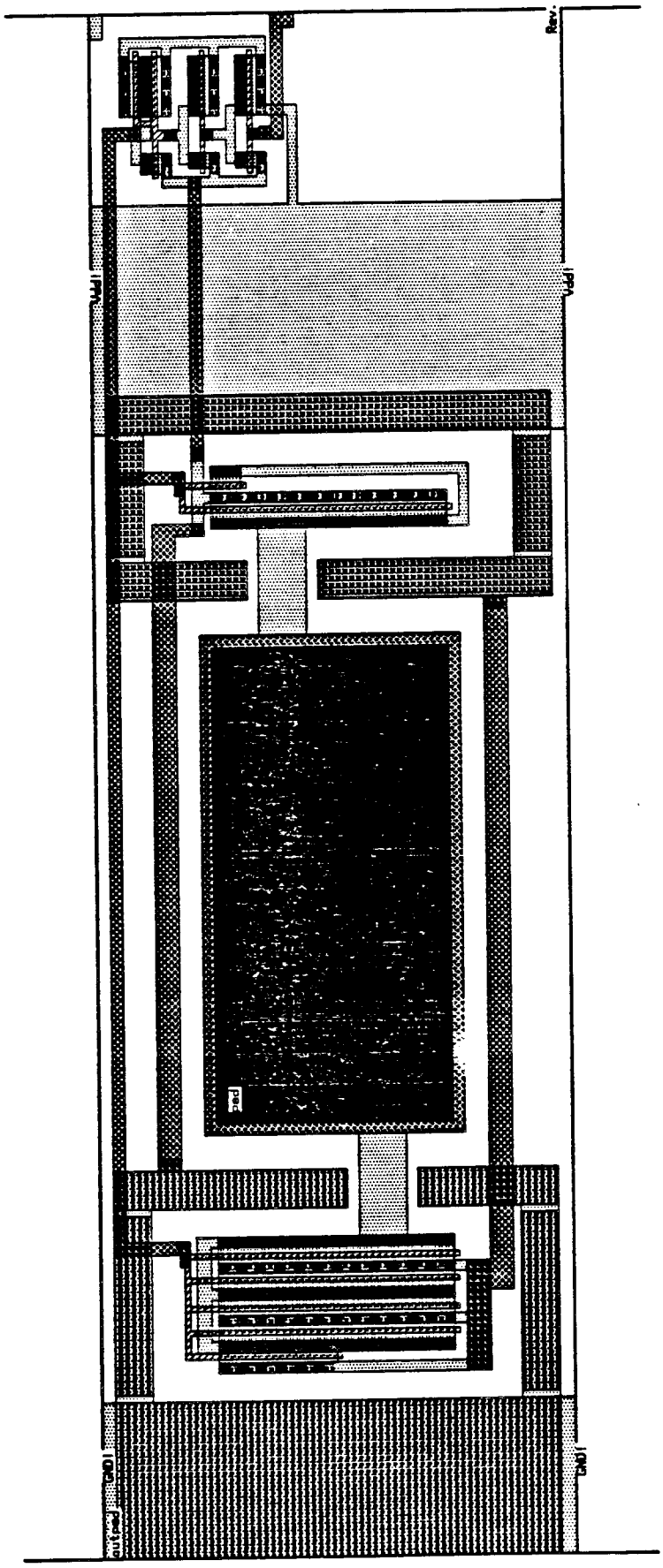
Circuit performance simulated using SPICE. ESD and latch-up performance to be evaluated pending test chip fabrication.

SEE ALSO

outpadck, iopad

BUGS

Not process independent. Power and ground requirements are dependent on the Xerox 2 μ process device performance.


Rev
VDD
PAD
PAD
GND
outpad

NAME

outpadck

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Outpadck is a clocked, non-inverting pad driver which is compatible with TTL signal levels.

PROPERTIES

Size

200 x 650 λ

Inputs

output: Chip signal to be output
clock: Clock input
clockb: Inverted clock input

Output

pad: Driven clocked output signal

Delay

		Output Driver Load		
		20 pF	30 pF	60 pF
Worst Case	t_{input}	25.5 ns	29.5 ns	44.0 ns
	t_{clock}	25.0	29.5	43.5 ns
Typical Case	t_{input}	14.5	17.5	25.5
	t_{clock}	14.5	17.0	26.0
t_{input}: Delay from signal input to valid output. t_{clock}: Delay from clock input to valid output.				

DC Current Capability

Sourced by Output Driver: 4.50 mA minimum
Sunk by Output Driver: -3.00 mA minimum

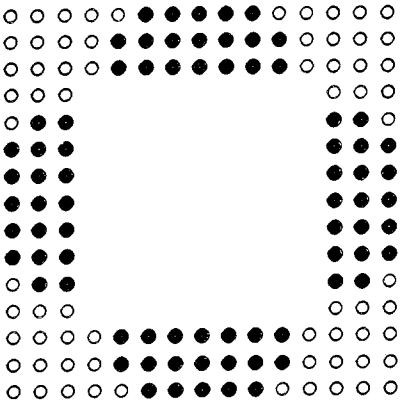
DESCRIPTION

Outpad is a clocked non-inverting output pad which provides TTL levels. Worst case TTL output levels are $\leq 0.4\ V$ for a logic zero and $\geq 2.4\ V$ for a logic one. The output driver transistors act as diodes for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection. The pass gate ensures that the buffer output changes only when the *clock* input is valid. The *clockb* input must be the inverted version of the *clock* input.

SUPPLY REQUIREMENTS

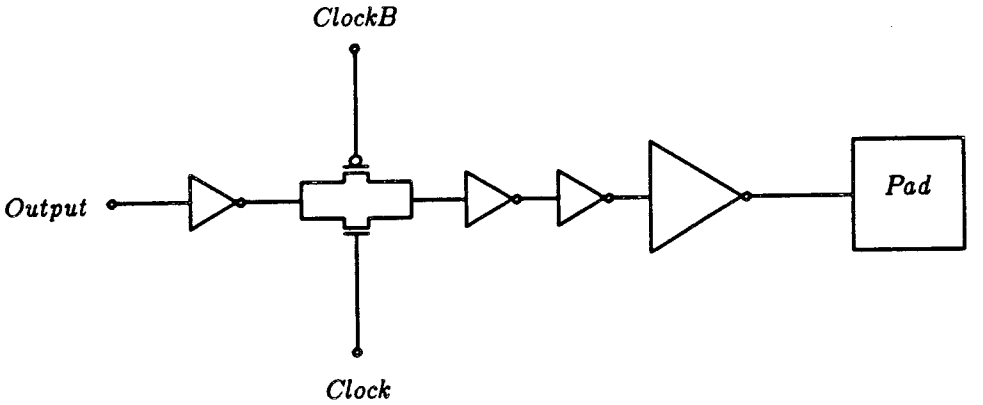
For every six instances of outpad, outpadck or iopad, one instance of vddpad and one instance of gndpad must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins

specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

SCHEMATIC



STATUS

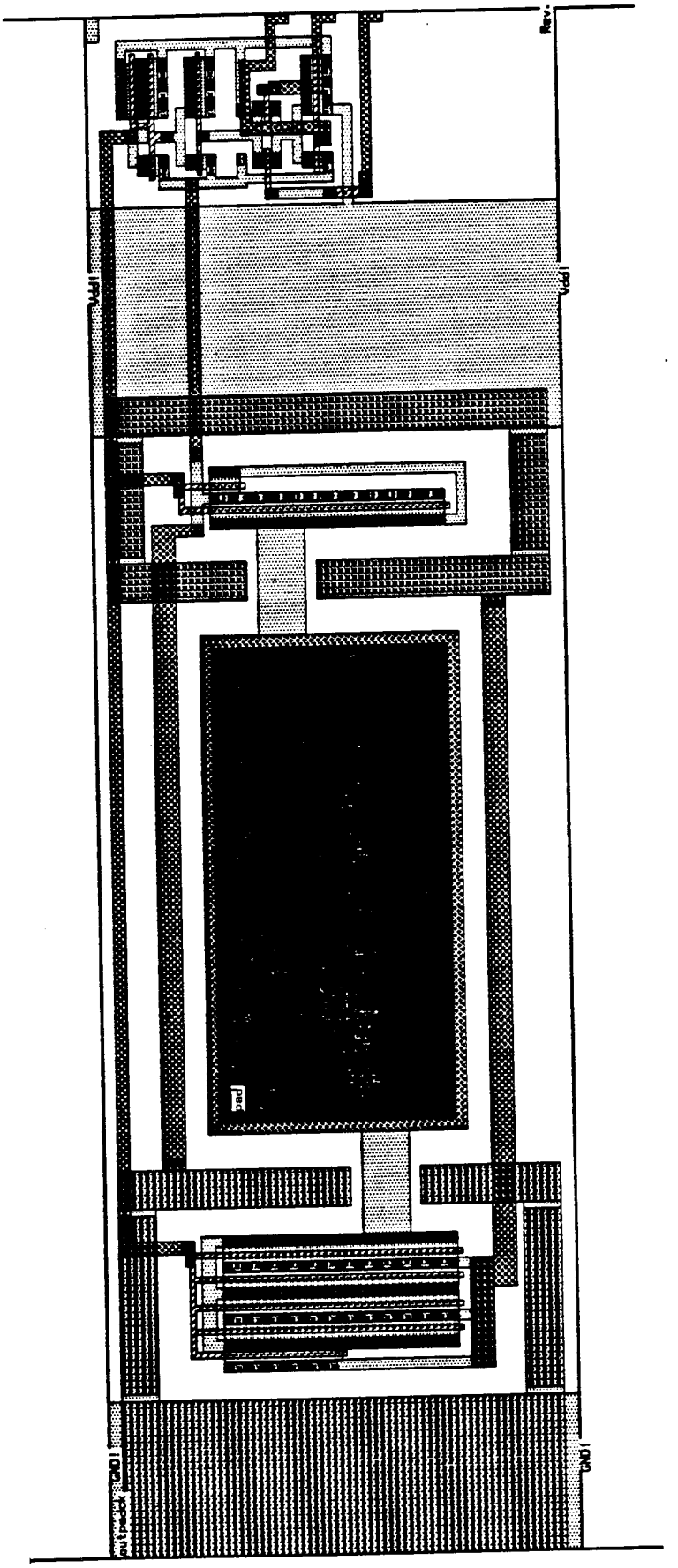
Circuit performance simulated using SPICE. ESD and latch-up performance to be evaluated pending test chip fabrication.

SEE ALSO

Outpad, Iopad

BUGS

Not process independent. Power and ground requirements are dependent on the Xerox 2 μ process device performance.


Rev:
VDD!
GND!
pad

NAME

vddpad

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Vddpad is a power supply pad.

PROPERTIES

Size

200 x 650 λ

Inputs

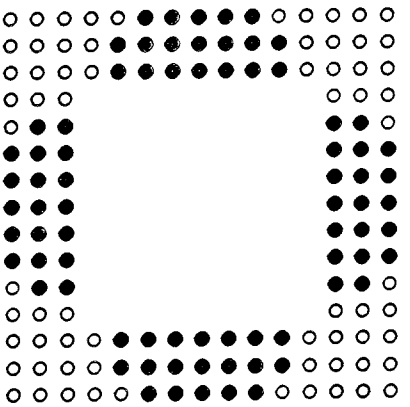
pad: 5 V power supply

DC Current Capability

50 mA

SUPPLY REQUIREMENTS

For every six instances of outpad, outpadck or iopad, one instance of vddpad and one instance of gndpad must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

STATUS

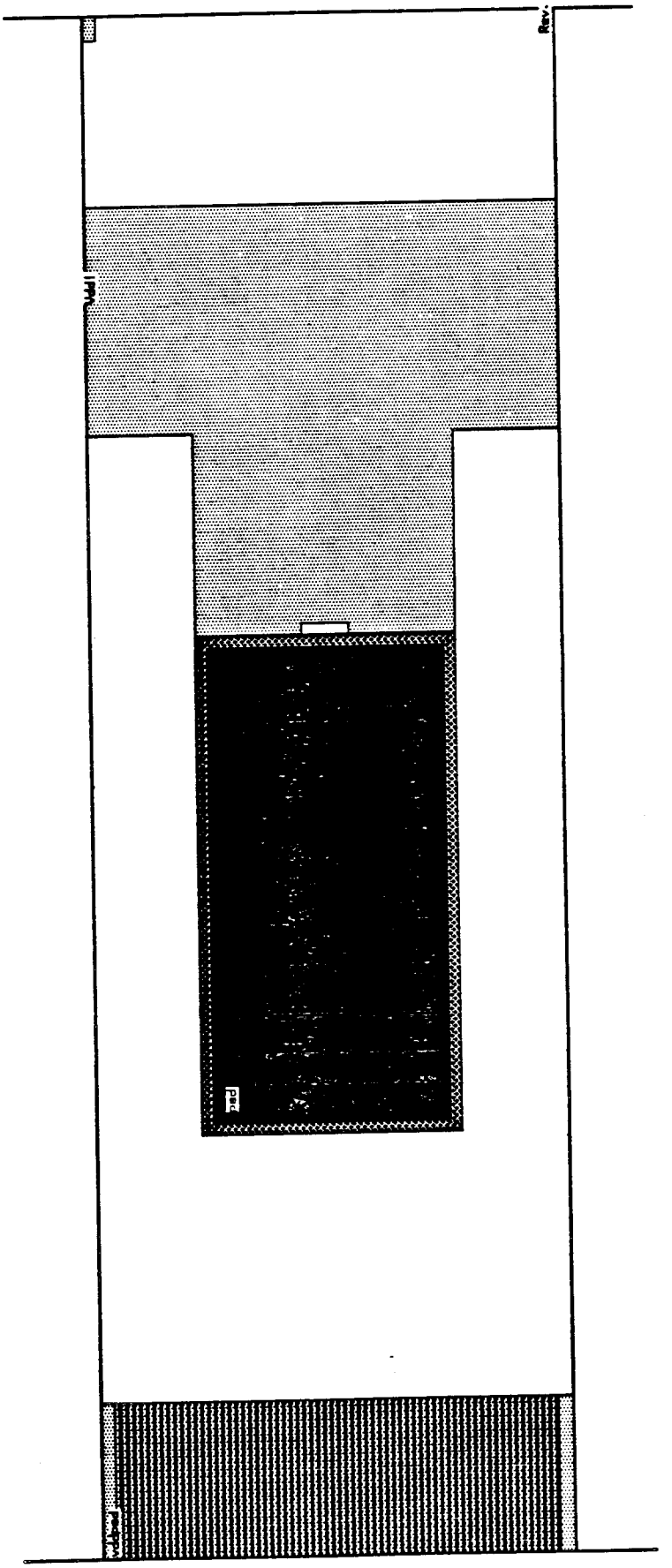
Layout to be evaluated pending test chip fabrication.

SEE ALSO

gndpad

BUGS

No known bugs.


Rev.
Pad

NAME

gndpad

PAD FRAME STRATEGY

Single row of pads

SYNOPSIS

Gndpad is a ground pad.

PROPERTIES

Size

200 x 650 λ

Inputs

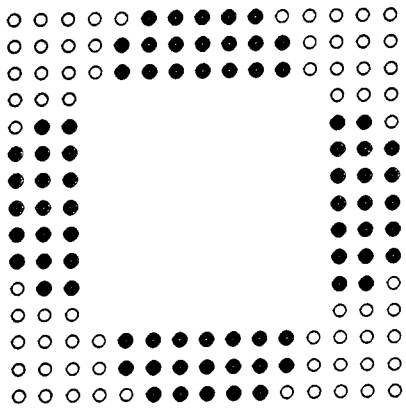
pad: Ground

DC Current Capability

20 mA

SUPPLY REQUIREMENTS

For every six instances of outpad, outpadck or iopad, one instance of vddpad and one instance of gndpad must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

STATUS

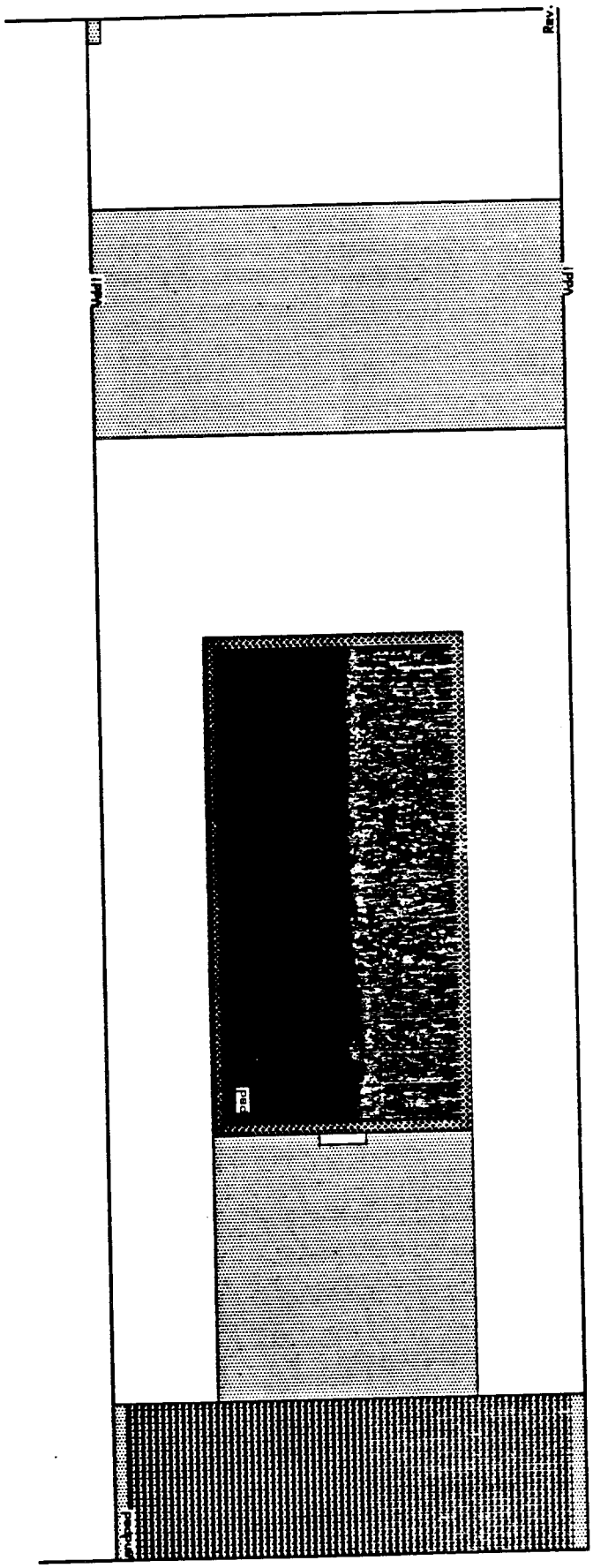
Layout to be evaluated pending test chip fabrication.

SEE ALSO

vddpad

BUGS

No known bugs.


Rev.
Vdd!
Vdd!
Pad
Pad

NAME

ioio

PAD FRAME STRATEGY

Double row of pads

SYNOPSIS

Ioio contains a pair of tri-state output pad driver or input buffer combinations. Both input and output buffers are compatible with TTL signal levels.

PROPERTIES

Size

200 x 1200 λ

Inputs

output1: Chip signal to be output on lower pad
output2: Chip signal to be output on upper pad
enable1: Output enable control for buffer 1
enable2: Output enable control for buffer 2

Outputs

pad1: Driven pad signal on lower pad
pad2: Driver pad signal on upper pad
input1: Buffered version of signal at pad1
input2: Buffered version of signal at pad2

Delay

		Output Driver Load		
		20 pF	30 pF	60 pF
Worst Case	t_{input}	27.5 ns	33.0 ns	48.5 ns
	t_{enable}	26.5	33.0	48.5
Typical Case	t_{input}	16.5	20.0	28.5
	t_{enable}	14.5	18.0	27.0
t_{input}: Delay from signal input to valid output. t_{enable}: Delay from enable input to valid output.				

		Input Buffer Load		
		0.5 pF	1.0 pF	1.5 pF
Worst Case	t_{input}	12.0 ns	13 ns	13.75 ns
Typical Case	t_{input}	6.75	7.5	8.25

DC Current Capability

Sourced by I/O Driver: 4.50 mA minimum
Sunk by I/O Driver: -3.00 mA minimum

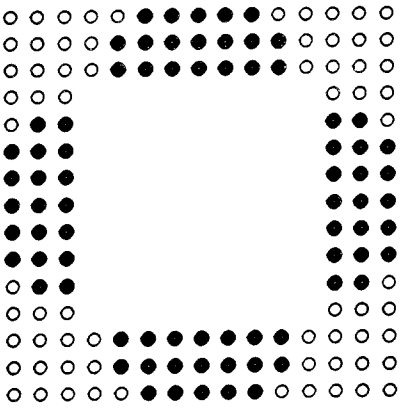
DESCRIPTION

Ioio includes a pair of independent tri-state buffers. Each is a output driver (when *enable* is high) or an input buffer (when *enable* is low). When *enable* is low, the output is in a high impedance state. TTL output levels of $\leq 0.4\ V$ for logic zeroes and $\geq 2.4\ V$ for logic ones are provided. Input levels are $\leq 0.8\ V$ for logic zeroes and $\geq 2.0\ V$ for logic ones. The output driver transistors act as diodes for protection from damage due to electrostatic

discharge (ESD). Large guard rings are provided for latch-up protection.

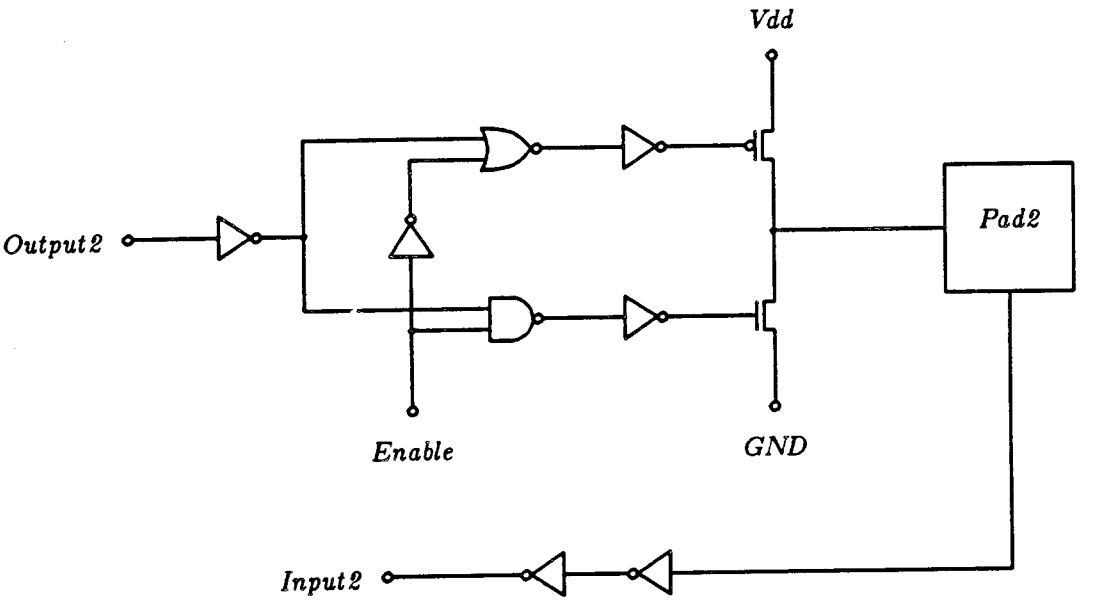
SUPPLY REQUIREMENTS

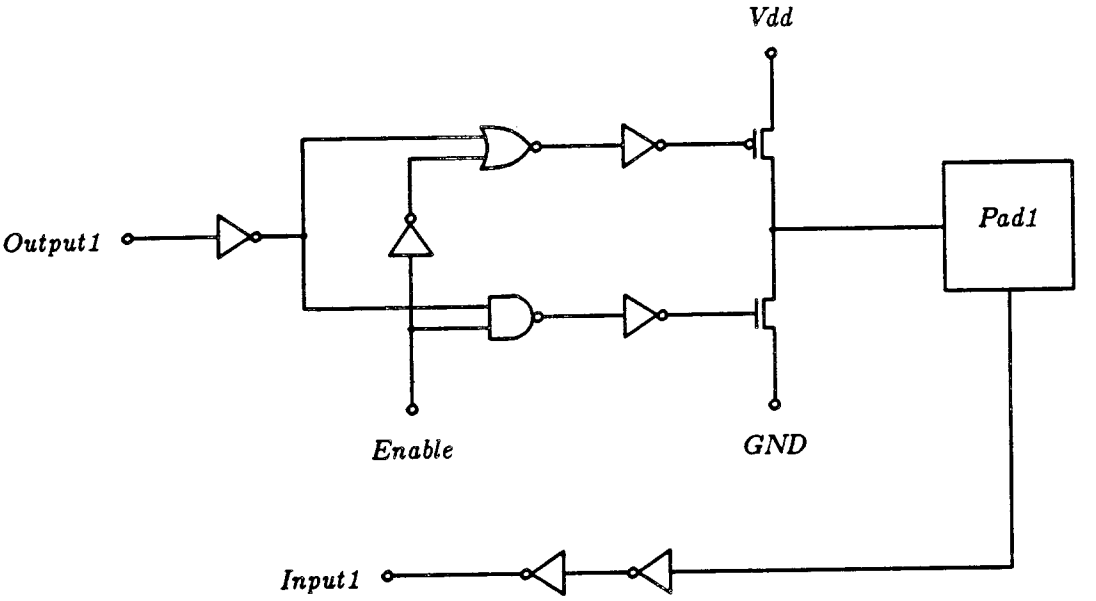
For every three instances of outout or ioio, one instance of vddgnd or one instance of gndvdd must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

SCHEMATIC





STATUS

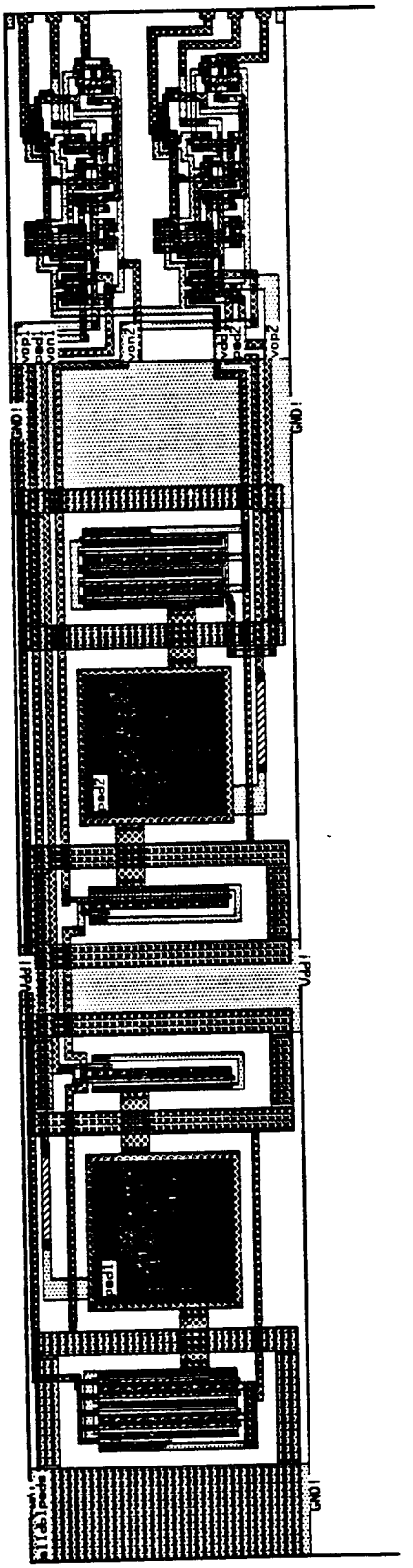
Laid out. Circuit performance simulated using SPICE.

SEE ALSO

inin

BUGS

Not process independent. Power and ground requirements are dependent on the Xerox 2μ process device performance.


GND!
PPA
GND!

NAME

inin

PAD FRAME STRATEGY

Double row of pads

SYNOPSIS

Inin contains a pair of non-inverting pads which are compatible with TTL signals.

PROPERTIES

Size

200 x 1200 λ

Inputs

pad1: Lower Bonding Pad pad2: Upper Bonding Pad

Outputs

input1: Buffered version of signal at pad1. input2: Buffered version of signal at pad2.

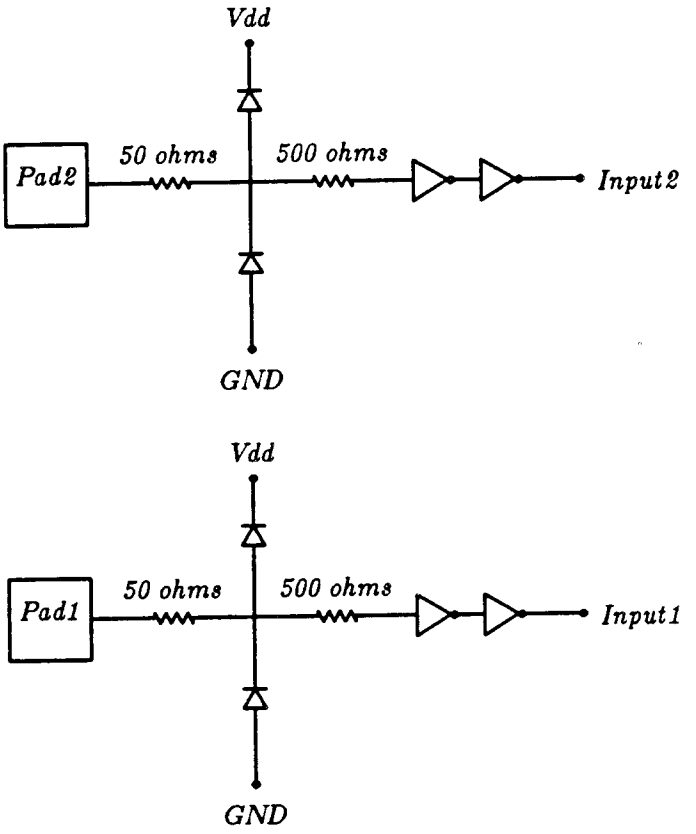
Delay

	Input Buffer Load		
	0.5 pF	1.0 pF	1.5 pF
Worst Case	12.0 ns	13.0 ns	13.75 ns
Typical Case	6.75	7.5	8.25

DESCRIPTION

Inin is a pair of non-inverting input pads which respond to TTL levels. TTL input levels are $\leq 0.8\ V$ for a logic zero and $\geq 2.0\ V$ for a logic one. Two diodes and two resistors are provided for each input pad for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection.

SCHEMATIC



STATUS

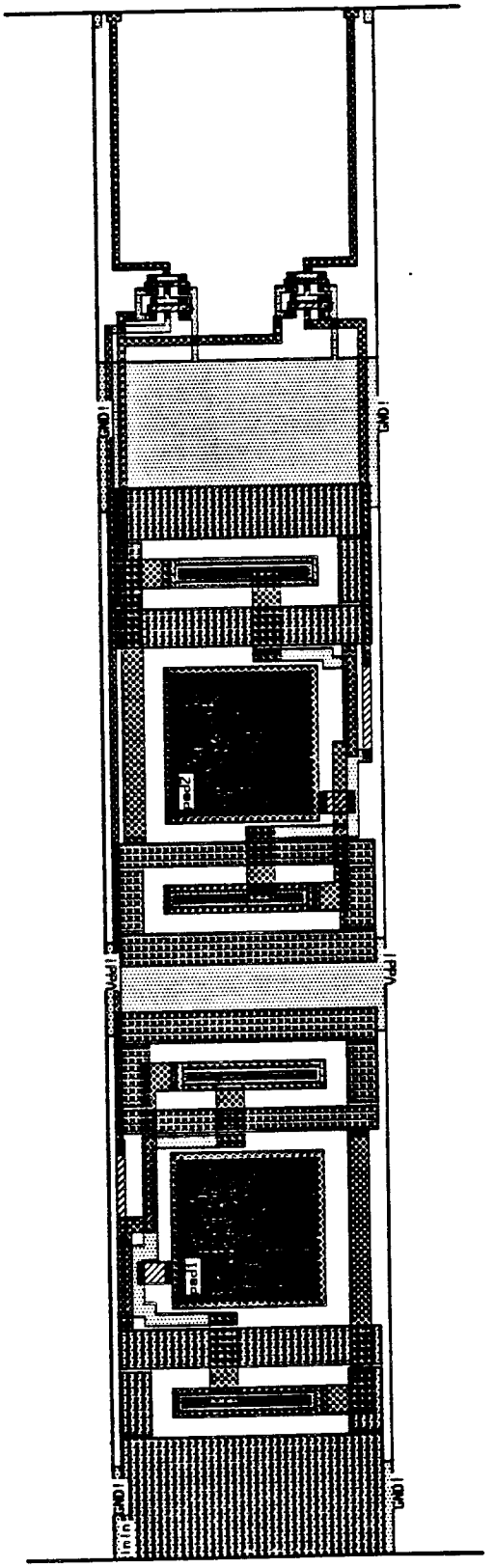
Laid out. Circuit performance simulated using SPICE.

SEE ALSO

inpad, inpadck

BUGS

Not process independent. TTL input level is dependent on the Xerox 2 μ process device performance.


GND!
VDD!
PAD
GND!

NAME

outout

PAD FRAME STRATEGY

Double row of pads

SYNOPSIS

Outout contains a pair of non-inverting pad drivers which are compatible with TTL signals levels.

PROPERTIES

Size

200 x 1200 λ

Inputs

output1: Chip signal to be output on lower pad
output2: Chip signal to be output on upper pad

Outputs

pad1: Driven pad signal on lower pad
pad2: Driver pad signal on upper pad

Delay

	Output Driver Load		
	20 pF	30 pF	60 pF
Worst Case	23.5 ns	27.5 ns	43.0 ns
Typical Case	14.0	17.0	25.5

DC Current Capability

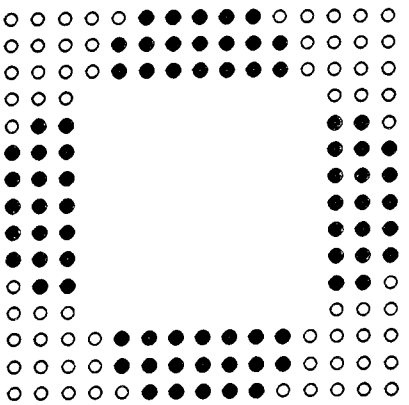
Sourced by Output Driver: 4.50 mA minimum
Sunk by Output Driver: -3.00 mA minimum

DESCRIPTION

Outout is a pair of non-inverting output pads which provide TTL levels. Worst case TTL output levels are $\leq 0.4\ V$ for a logic zero and $\geq 2.4V$ for a logic one. The output transistors act as diodes for protection from damage due to electrostatic discharge (ESD). Large guard rings are provided for latch-up protection.

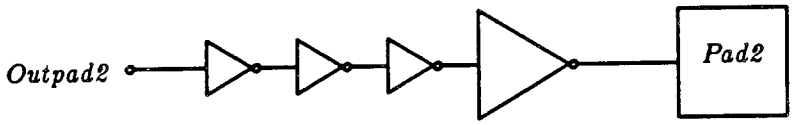
SUPPLY REQUIREMENTS

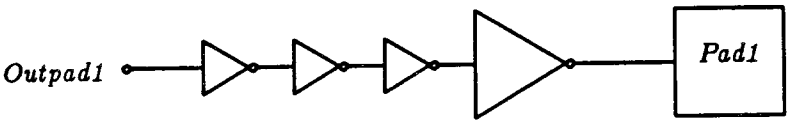
For every three instances of outout or ioio, one instance of vddgnd or one instance of gndvdd must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

SCHEMATIC





STATUS

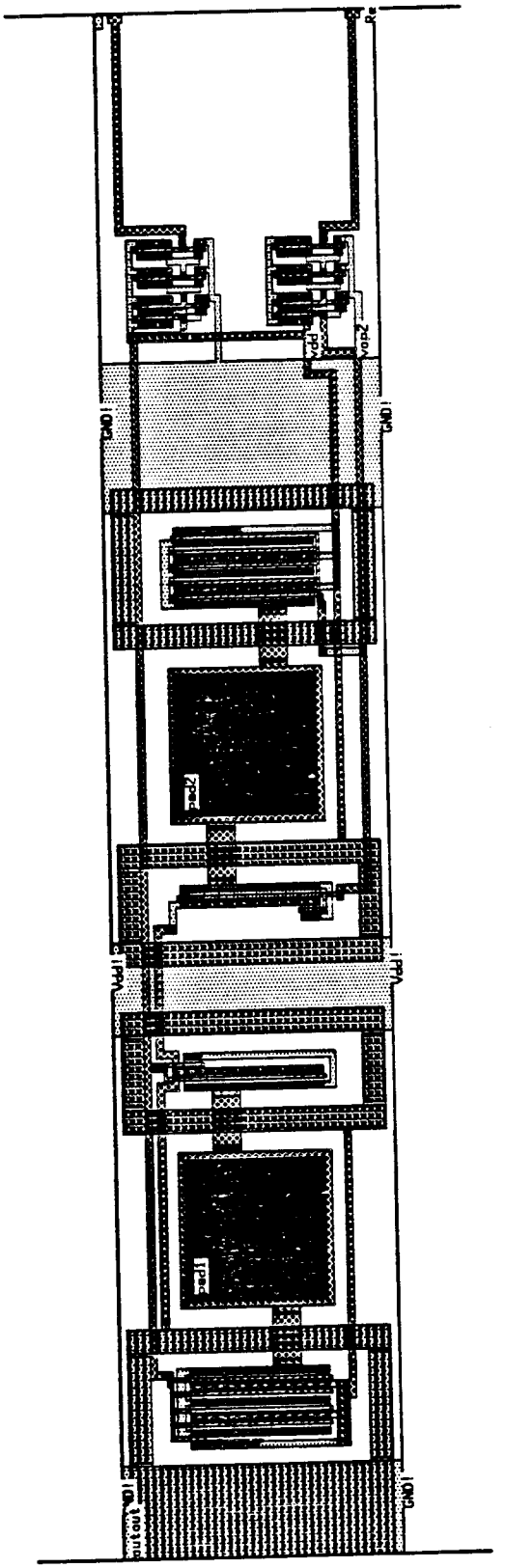
Laid out. Circuit performance simulated using SPICE.

SEE ALSO

ioio

BUGS

Not process independent. Power and ground requirements are dependent on the Xerox 2μ process device performance. process device performance.


VDD
GND
PPA
NPA
2pad
1pad
outout

NAME

vddgnd

PAD FRAME STRATEGY

Double row of pads

SYNOPSIS

Vddgnd contains a power supply pad and a ground pad.

PROPERTIES

Size

200 x 1200 λ

Inputs

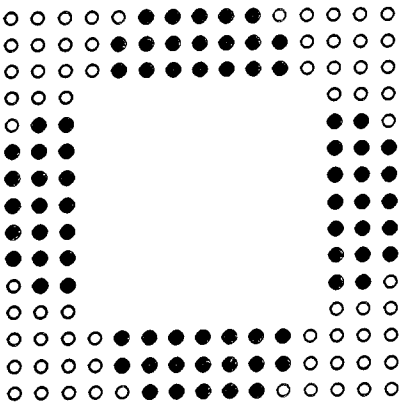
pad1: 5 V power supply
pad2: Ground

DC Current Capability

Vdd: 50 mA
GND: 20 mA

SUPPLY REQUIREMENTS

For every three instances of outout or ioio, one instance of vddgnd or one instance of gndvdd must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

STATUS

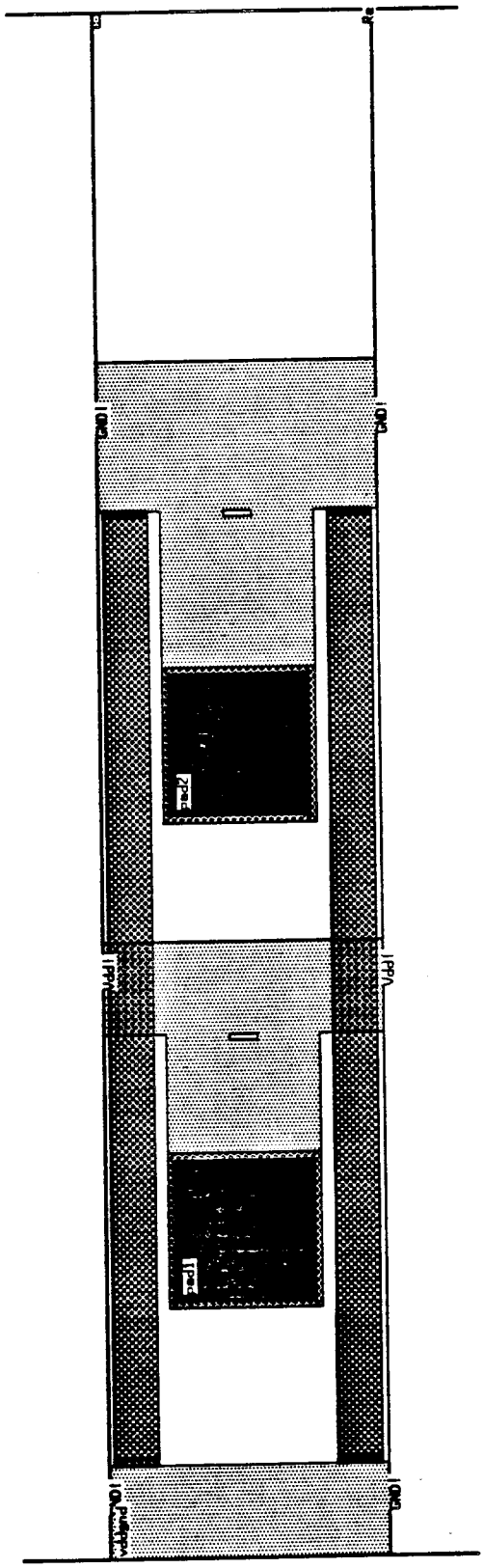
Laid out.

SEE ALSO

gndvdd

BUGS

No known bugs.



NAME

gndvdd

PAD FRAME STRATEGY

Double row of pads

SYNOPSIS

Gndvdd contains a power supply pad and a ground pad.

PROPERTIES

Size

200 x 1200 λ

Inputs

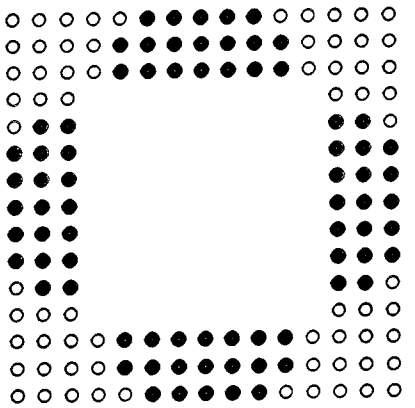
pad1: Ground
pad2: 5 V power supply

DC Current Capability

Vdd: 50 mA
GND: 20 mA

SUPPLY REQUIREMENTS

For every three instances of outout or ioio, one instance of vddgnd or one instance of gndvdd must be provided. The Vdd and GND pads must be located within 1500 μ of their respective output pads. When used on an integrated circuit to be packaged in a pin grid array, these Vdd and GND pads must be bonded to that half of the PGA pins which have the least parasitic inductance. The pins with the least parasitic inductance are those that are closest to the center of each side of the pin array. As an example, the following figure shows the recommended pins of a 144 pin PGA. Additionally, any pins specified by the pin grid array manufacturer to be low resistance pins are highly recommended.



● *Recommended Pins for Supply and Ground*
○ *Not Recommended for Supply and Ground*

STATUS

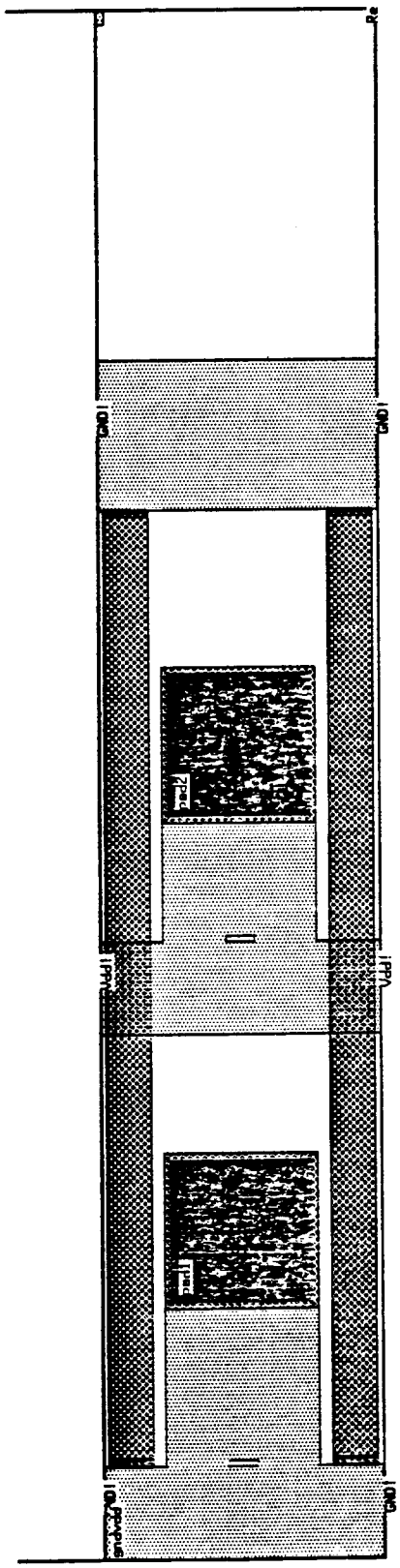
Laid out.

SEE ALSO

vddgnd

BUGS

No known bugs.


GND
GND
PAD
IPPV
IPPV
PAD
GND
GND

Appendix B: Xerox 2u Process SPICE Models

The following SPICE models were used for MOS devices in the Xerox 2u process. The parameters were given in the design rules for the process. This document was dated 1983. Since the design rules gave tolerances for the parameters, these were used for *best* and *worst* case speed simulations. In addition to these parametric variations, the power supply and temperature were varied when doing simulations. The supply was 4.5 V for worst case simulations and 5.5 V for best case. The temperature was 0.0 degrees celsius for best case simulations and 100.0 degrees celsius for worst case simulations. With these assumptions and models, the total speed variation in the simulations was a factor of 2.59 from best case to worst case.

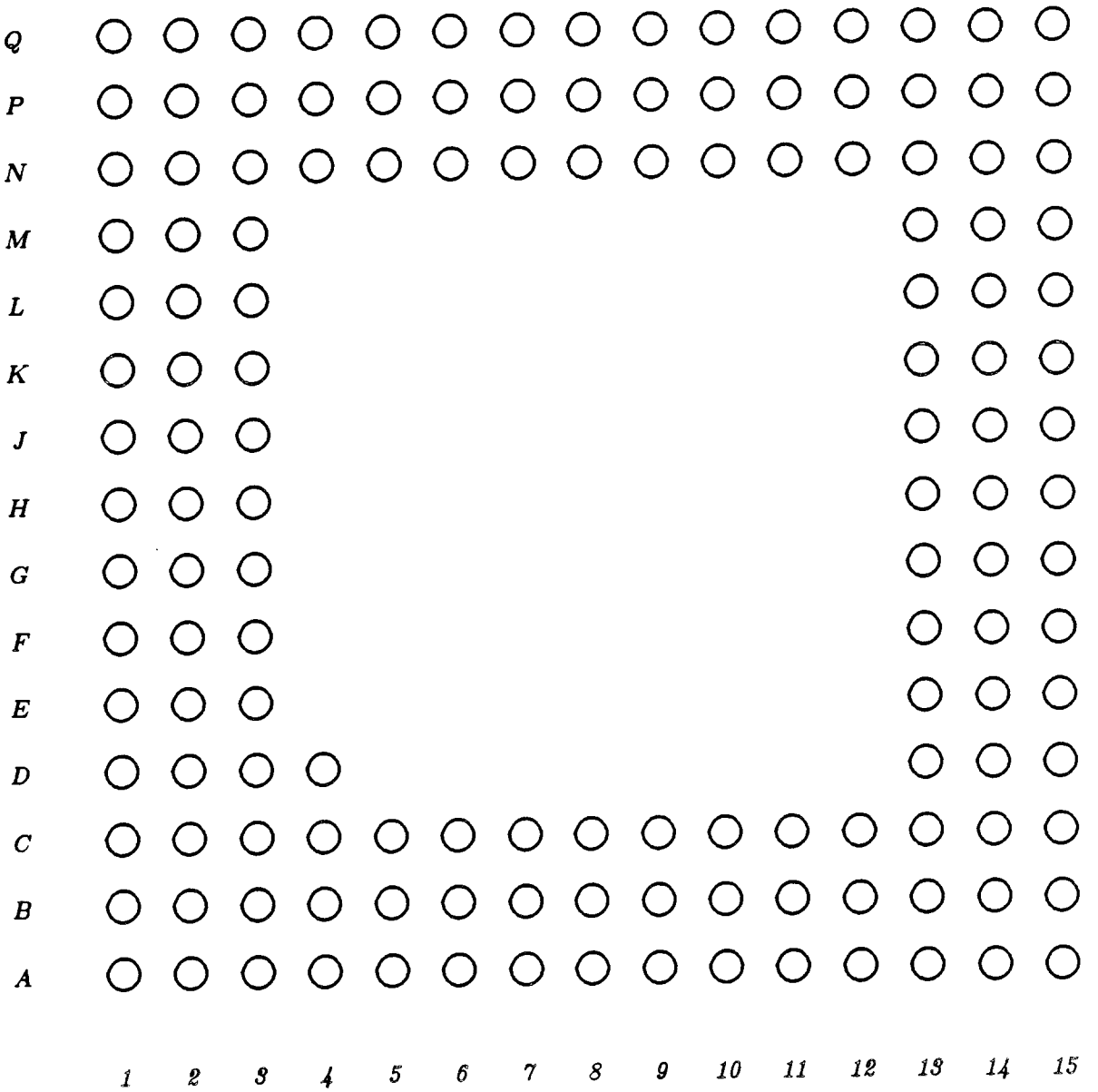
While this range of process models for simulations give some idea of the tolerance of the circuits designed to speed variations, more accurate simulations could be made with the results of an in depth characterization of the process. For example, no the process models do not indicate any gate length variation. Also, the effective conductance of the n-channel devices, as indicated by the models, is about eight times that of the p-channel device.

```
* xerox typical case device parameters
+ rsh=35 cj=2.75e-4 cjsw=1.5e-10 tox=30n xj=.3u ld=.225u tpg=-1
+uexp=.06 vmax=5.7e4 cgso=2.7e-10 cgdo=2.7e-10 cgbo=1.4e-10
+ rsh=120 cj=3.1e-4 cjsw=3.0e-10 tox=30n xj=.5u ld=.375u tpg=-1
+uexp=.44 vmax=9.0e4 cgso=4.5e-10 cgdo=4.5e-10 cgbo=1.4e-10


* xerox worst case device parameters
+ rsh=40 cj=3.0e-4 cjsw=1.9e-10 tox=31.5n xj=.27u ld=.203u tpg=-1
+uexp=.06 vmax=5.7e4 cgso=2.7e-10 cgdo=2.7e-10 cgbo=1.4e-10
+ rsh=150 cj=3.4e-4 cjsw=3.8e-10 tox=31.5n xj=.45u ld=.338u tpg=-1
+uexp=.44 vmax=9.0e4 cgso=4.5e-10 cgdo=4.5e-10 cgbo=1.4e-10


* xerox best case device parameters
+ rsh=30 cj=2.5e-4 cjsw=1.1e-10 tox=28.5n xj=.33u ld=.248u tpg=-1
+uexp=.06 vmax=5.7e4 cgso=2.7e-10 cgdo=2.7e-10 cgbo=1.4e-10
+ rsh=90 cj=2.7e-4 cjsw=2.2e-10 tox=28.5n xj=.55u ld=.413u tpg=-1
+uexp=.44 vmax=9.0e4 cgso=4.5e-10 cgdo=4.5e-10 cgbo=1.4e-10
```

Appendix C: Pin Number Map for Kyocera 144 Lead Pin Grid Array

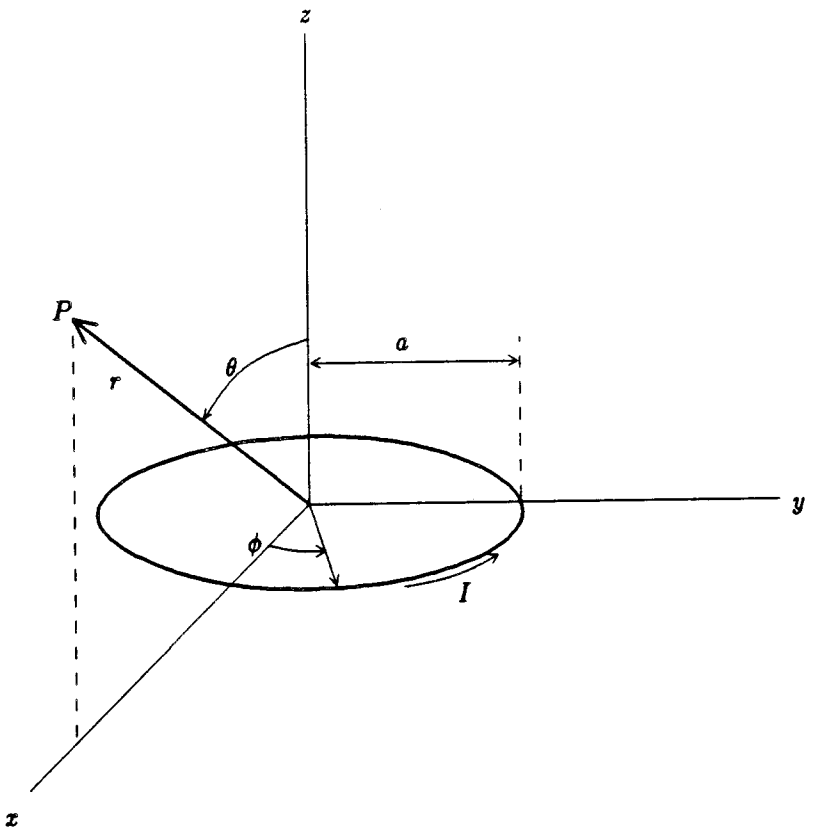


Bottom View

Extra pin at lower left is an index marker.

Appendix D: Analytic Solution for Inductance of Capacitor Lead Loop

The leads of the capacitor in the capacitor lead loop problem of section 3.2.3.1. may be modeled by a circular loop of wire. An analytic solution for the inductance of the circular loop of wire may be obtained where the loop of wire has radius a and the radius of the wire is given as b [Karn85]. Spherical coordinates are chosen to describe the problem. The following diagram illustrates the problem.



The expression for the vector potential is:

$$\mathbf{A}(\mathbf{x}) = \frac{1}{c}\int \frac{\mathbf{J}(\mathbf{x}')}{|\,\mathbf{x}-\mathbf{x}'\,|} d^3x' \tag{D1}$$

where c is the speed of light. For the circular loop of wire, the only component of the current density is in the ϕ direction. This is given as:

$$J_\phi = I \sin\theta' \, \delta(\cos\theta') \, \frac{\delta(r'-a)}{a} \tag{D2}$$

Applying (D2) to (D1) and integrating over the delta functions gives:

$$A_\phi = \frac{Ia}{c} \int_0^{2\pi} \frac{\cos\phi \, d\phi}{(a^2+r^2-2ar\sin\theta\cos\phi)^{1/2}} \tag{D3}$$

(D3) is an elliptic integral which can be expressed in terms of the complete elliptic integrals, $K(k)$ and $E(k)$ [Jack75]. This result is also specialized to the region in which we are interested, the surface enclosed by the loop.

$$A_\phi = \frac{4I}{c(a+r)k^2} \left[(2-k^2)K(k) - 2E(k) \right] \tag{D4}$$

where

$$k^2 = \frac{4ar}{(a+r)^2} \tag{D5}$$

$$K(k) = \int_0^{\pi/2} \frac{d\phi}{(1-k^2\sin^2\phi)^{1/2}} \tag{D6}$$

$$E(k) = \int_0^{\pi/2} (1-k^2\sin^2\phi)^{1/2} d\phi \tag{D7}$$

The definition of the inductance of the loop is:

$$L = \frac{\Phi}{Ic} = \frac{1}{Ic} \int_{loop} \mathbf{B}\cdot\hat{\boldsymbol{\theta}} \, da \tag{D8}$$

$$= \frac{1}{Ic} 2\pi \int_0^{a-b} |B_\theta| \, r \, dr$$

where the integration limits are from the center of the loop to the wire. The wire must

here take a finite thickness, otherwise there is a pole in the magnetic field as r approaches a. Also, the assumption is made that $b<<a$. Since the magnetic field is given as the curl of the vector potential and the vector potential has only a component in the $\hat{\phi}$ direction, we obtain:

$$r \mid B_\theta \mid = \frac{\partial}{\partial r}(rA_\phi) \tag{D9}$$

The integral in (D8) and partial derivative in (D9) then cancel each other and the inductance is given as:

$$L = \frac{2\pi}{Ic} rA_\phi \mid_0^{a-b} \tag{D10}$$

The term for $r=0$, will be zero if A_ϕ is less than some finite number. Using the definition, $\epsilon \equiv b/a$ ($\epsilon<<1$), and a binomial expansion for k^2, the inductance then becomes:

$$L = \frac{2\pi a}{c^2}(2-\epsilon)\left[\left[1+\frac{1}{4}\epsilon^2\right]K(k)-2E(k)\right] \tag{D11}$$

Tables of mathematical formulas [Dwig61] give expansions of $K(k)$ and $E(k)$ as:

$$K(k') = \ln\left[\frac{4}{k'}\right] + \frac{1}{4}\left[\ln\frac{4}{k'} - 1\right]k'^2 + \cdots \tag{D12}$$

$$E(k') = 1 + \frac{1}{2}\left[\ln\frac{4}{k'} - \frac{1}{2}\right]k'^2 + \cdots \tag{D13}$$

where

$$k' = (1-k^2)^{1/2} = \frac{\epsilon}{2}$$

and only the terms of signficance at least k'^2 are saved to this point. Using (D12) and

(D13) in (D11), simplifying, saving terms of significance at least ϵ, and replacing ϵ with b/a gives:

$$L = \frac{4\pi}{c^2} a \left[\ln\left[\frac{8a}{b}\right] - 2 - \frac{b}{2a}\ln\left[\frac{8a}{b}\right] + \frac{b}{a} \right] \tag{D14}$$

The conversion to MKSA units is accomplished by use of the relationships:

$$L_{Gaussian} = 4\pi\epsilon_0 L_{MKSA}$$

and

$$c^2 = \frac{1}{\epsilon_0 \mu_0}$$

giving:

$$L_{MKSA} = \mu_0 a \left[\ln\left[\frac{8a}{b}\right] - 2 - \frac{b}{2a}\ln\left[\frac{8a}{b}\right] + \frac{b}{a} \right] \tag{D15}$$

This was evaluated for geometries of a=1.8 mm and b=0.32 mm used in the capacitor lead loop measurements and gave a result of 3.23 nanohenry. Note from Table 8 in the text of the report that this value is within the range of measured values.

References

[Dwig61] *Tables of Integrals and Other Mathematical Data,* H. B. Dwight, MacMillan, New York, New York, 1961

[Jack75] *Classical Electrodynamics,* J. D. Jackson, Wiley, New York, New York, 1975

[Karn85] A. J. Karn, University of California-Berkeley, Personal communication, August 10, 1985