LOW DISTORTION SWITCHED CAPACITOR FILTERS

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Memorandum No. UCB/ERL M86/12

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Robert G Meyer

Chairman of Committee

Abstract

Distortion mechanisms in switched-capacitor circuits are investigated by theoretical analysis and closed form expressions relating harmonic distortion to circuit parameters are derived. The relative importance of each distortion source has been determined from the theoretical results.

Design techniques for low distortion applications are discussed and are applied to some test circuits, which include a 6^{th} order experimental filter, a switched-capacitor integrator, test operational amplifiers, and test capacitors. The filter design uses a fully differential, class A/B op amp with a continuous-time common-mode feedback circuit, and a node voltage scaling technique A novel four-phase clock is also implemented in these test circuits to test the relative importance of the effect of clock related noise.

Distortion measurements on the test circuits show that the measurements agree well with the theoretical results; and for the 6^{th} order switched-capacitor filter the THD is 0.02% within the whole 4kHz bandwidth for 82dB dynamic range (relative to the noise floor).

ACKNOWLEDGEMENTS

I am very grateful to my advisor, Professor Robert G. Meyer for his technical guidance and assistance throughout the project. I have also benefitted greatly from the advice and support of Professors Paul R. Gray, and Robert W. Broderson. I am also indebted to many of the fellow graduate students in the Integrated Circuit Group, for their useful discussions and assistance. They have made my graduate study in Berkeley a wonderful and illuminating experience.

Special thanks goes to the microelectronics lab staff, and the MOSIS [1] crew, for their help on the fabrication of the experimental chips.

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CHAPTER 1

INTRODUCTION

1.1. The Problem

Since switched capacitor filters were first used in PCM applications, rapid progress has been made in the development of switched capacitor filtering techniques[1, 2, 3]. However, the internally-generated noise and harmonic distortion in switched capacitor filters often impose an upper limit on the available dynamic range for applications which require higher performance[4, 5].

One example of such a high performance application is the anti-aliasing filter used in 14-bit or 16-bit digital audio systems[6, 7]. As in many other digital signal processing systems (Figure 1.1) this filter appears twice in the system, once in recording (before the audio signal enters the analog/digital converter), and once in reproduction (after the signal exits the digital/analog converter). The first filter is used to eliminate the outband noise so it will not "fold back" into the passband after the following sample/hold action. The second filter is used to eliminate the high frequency aliases so the following stages will not have to slew too fast. As a required characteristic of these anti-aliasing low-pass filters, ripple of +/- 0.2 dB at 20Hz-20kHz is essential because the audio signal has to be filtered twice. Furthermore, because of the high attenuation (> 80dB) needed beyond half the sampling frequency, a complicated ladder filter with order higher than six is usually required. Presently, the manufacturers of digital audio systems uses passive components (R,L,C) to implement these filters. This approach is both time-consuming and uneconomical because: (1) it is necessary to adjust the values of each individual filter components upon manufacture, by altering the coil dc resistance and the suspended (stray) capacitance. (2) the current concentration in the

A TYPICAL DIGITAL SIGNAL PROCESSING SYSTEM

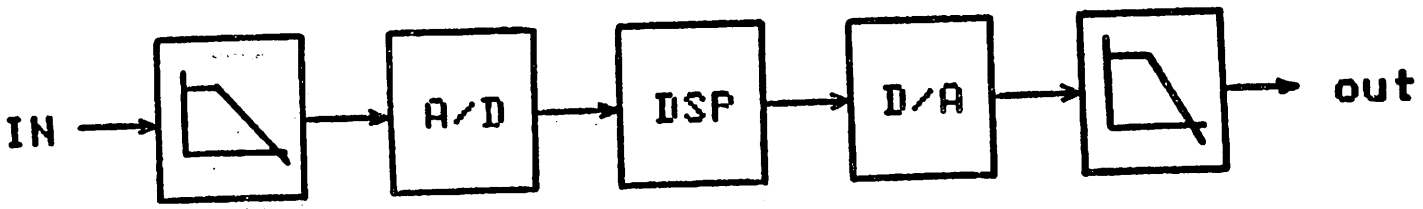


Figure 1.1 A typical digital signal processing system with analog interface.

inductors can have large variations over different signal levels. the inductor core material has to be carefully chosen such that nonlinearity of the coil core material (due to the signal level change) is not reflected as the filter distortion. (3) precision passive components can be bulky and expensive. On the other hand. while the precision of the passband characteristics of the switched capacitor filters is very good. the noise and distortion properties are not satisfactory for the aforementioned high quality audio applications.

Another example of the high performance filtering applications can be found in the design of data modems (MOdulator/DEModulator). A typical modem structure and its passband characteristics [8] are shown in Figure. 1.2. Since the echo from the adjacent channel is often larger than the desired in-band signal. it is often preferred to filter the received signal first to eliminate the out-of-band noise before sending it for the demodulation and further processing (here the demodulation can be done by either digital or analog means). Consider the operating condition where the modem is transmitting in the low band and receiving at high band. When the echo from the transmitter is large enough. the second harmonic of the low band signal falls right into the receiving band (high band) and distorts the desired signal. Usually the dynamic range required for the filter is in the range of 60 - 70 dB[9]. That is. given the peak input signal. both the harmonics and the noise have to be smaller than -60 to -70 dB. Since more and more modems are manufactured in MOS integrated circuit technology. a high dynamic range (both noise and distortion) switched capacitor filter can be very useful in these modem designs.

Other than the examples mentioned above. high dynamic range requirements can be found in many other switched capacitor filter applications. Some previous workers have demonstrated the feasibility of designing and fabricating switched capacitor filters with baseband noise less than -100dB[10]. Nevertheless the distortion levels of the

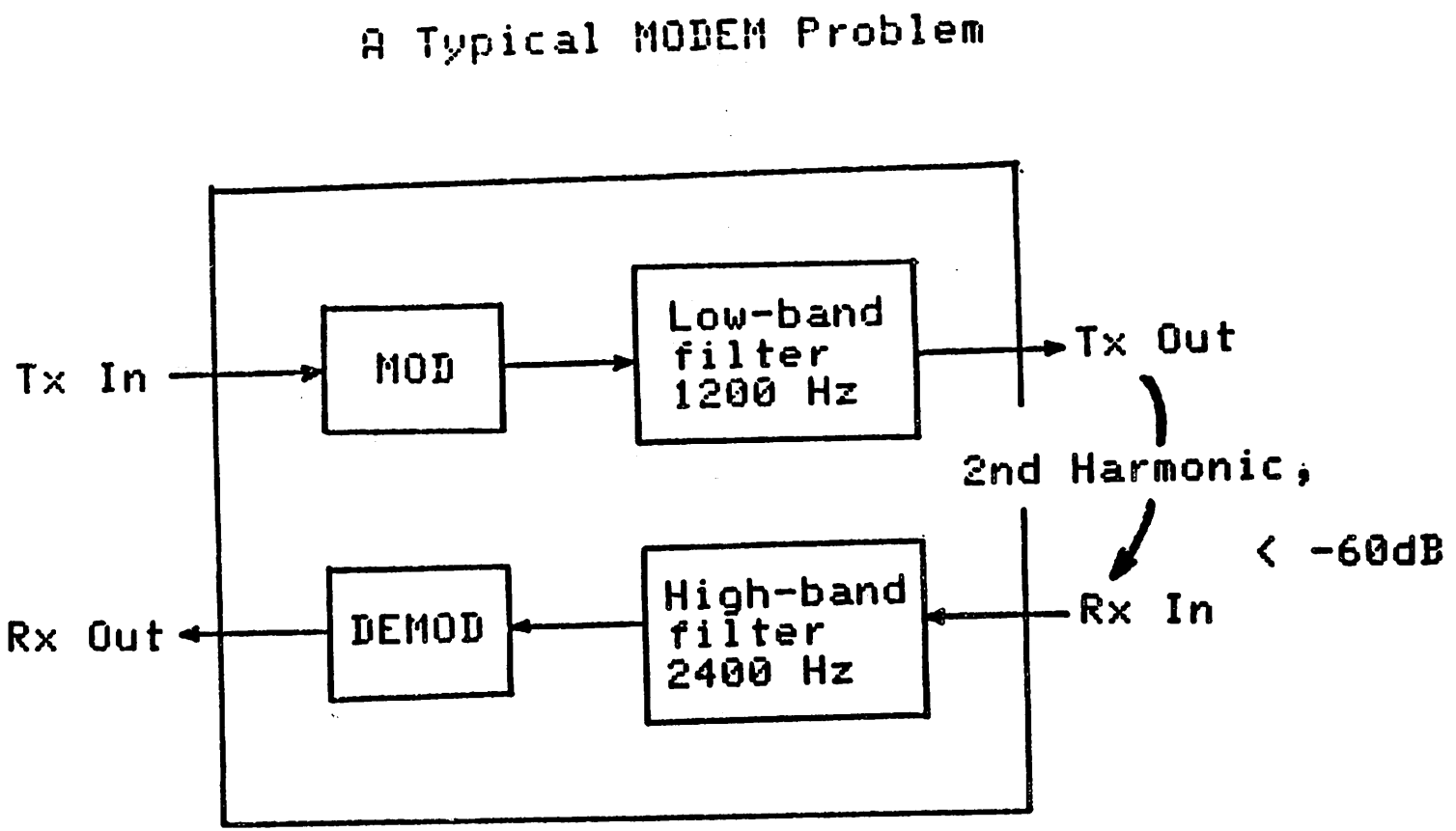


Figure 1.2 A typical low speed modem, which transmits at low band, and receives at high band.

presently available switched capacitor filters remain in the vicinity of -50dB. The purpose of this research is to investigate the distortion sources in switched capacitor circuits and to develop techniques for reducing harmonic distortion in switched capacitor circuits.

1.2. The Research

The effort has been concentrated in two areas. The first is the identification of different distortion sources in switched capacitor integrators and the analysis of their effects on filter distortion. The second is the investigation of the optimum filter and operational amplifier configurations for achieving the lowest possible harmonic distortion. Theoretical analyses and computer simulations of various distortion sources in switched capacitor integrators have been carried out with the emphasis on : operational amplifier slew rate, operational amplifier gain nonlinearity, capacitor nonlinearity, and the voltage-dependent clock feedthrough of MOS switches. The distortions induced by these sources are found to range from -50dB to -80dB given the present-day process technology.

A key problem in the implementation of low-distortion switched capacitor filters is the implementation of an operational amplifier which simultaneously achieves high slew-rate and a small settling time with a large (several pF) capacitive load. This problem is less severe if class A/B operational amplifiers are used, because for this type of amplifiers the output drive is more or less proportional to the input level and therefore has more linear response comparing with the slew-limited operational amplifiers.

Another major contribution of the filter distortion is from the capacitor nonlinearity. It has been reported [11] that by carefully controlling the doping concentration of the capacitor plates, the voltage-coefficients of integrated circuit capacitors can be significantly reduced. The analysis shows that, by suitably designing high speed/high

linearity operational amplifiers and low voltage-coefficient capacitors, the harmonic distortion can be reduced to below -80dB.

In Chapter 2 the sources of distortions in switched capacitor circuits are investigated and their effects estimated quantitatively. In Chapter 3 the design aspects of the operational amplifier and the filter are discussed. In Chapter 4 the measured results from some experimental circuits are presented. In Chapter 5, conclusions are drawn and future directions are suggested. The procedure of a typical CMOS process (the Berkeley CMOS Process) is also included in Appendix I as a reference.

CHAPTER 2

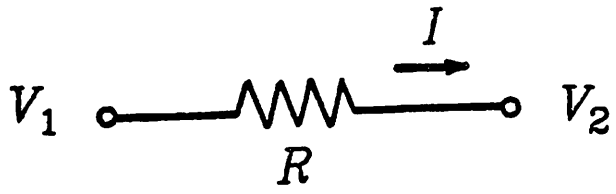
DISTORTION SOURCES IN SWITCHED CAPACITOR CIRCUITS

This chapter begins with a brief review of the basic switched capacitor concept and the development of the switched capacitor integrator. The following sections discuss the distortion sources in switched capacitor circuits and the design techniques that can be used to improve the filter performance.

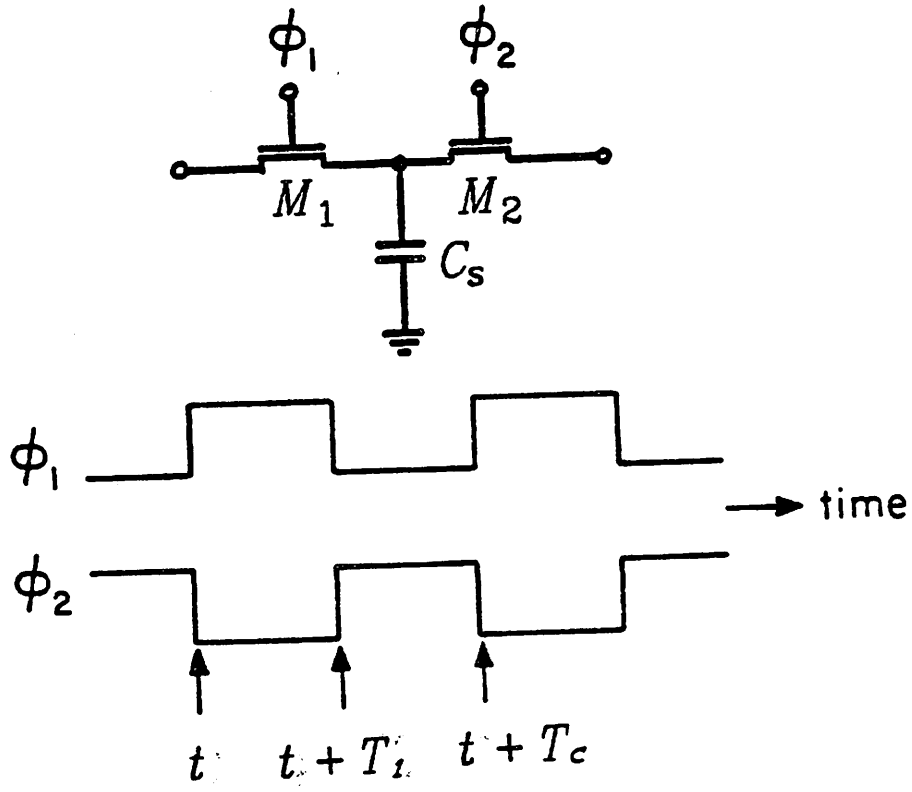
2.1. The Basic MOS Switched Capacitor Concept

Large resistance values are difficult to obtain in integrated circuits due to the lack of high resistivity regions. Even when large resistors do exist in integrated circuits. they often have significant temperature and voltage coefficients. and occupy large chip area if good matching is required. By contrast. MOS capacitors always have much smaller temperature and voltage coefficients and much better matching properties[12. 13]. Therefore. for MOS technology. it is advantageous to replace resistors by switched capacitors whenever possible.

The operation of the switched capacitor "resistor" is shown in Figure 2.1(b). At time t. clock ϕ_1 turns on MOSFET M_1 so that the capacitor C_s is charged to the voltage V_1. At time $(t + T_1)$. ϕ_2 turns on MOSFET M_2 (M_1 is now turned off). and the capacitor is discharged to the voltage V_2. The amount of charge which flows into V_2 from t to $(t + T_c)$ is thus $Q = C_s(V_1 - V_2)$. Since the charge transfer process happens in a period of time T_c. the equivalent current flowing from V_1 to V_2 during this time is



(a)



(b)

Figure 2.1

(a) Resistor, and (b) switched capacitor equivalent of a resistor, and the two-phase clock.

$$I = \frac{Q}{T_c} = \frac{C_s \left| V_1 - V_2 \right|}{T_c} \tag{2.1}$$

where T_c is the sampling period. Comparing with the current flowing through the resistor in Figure 2.1(a) during the same period of time

$$I = \frac{V_1 - V_2}{R}. \tag{2.2}$$

an equivalent switched capacitor resistance can be defined as

$$R_{eq} = \frac{T_c}{C_s} = \frac{1}{f_c C_s} \tag{2.3}$$

where f_c is the sampling frequency. If the switching rate is much larger than the signal frequency of interest, then the time sampling of the signal can be ignored in a first-order analysis and the switched capacitor can be considered as a direct replacement for a conventional resistor. If this condition is not met, more exact sampled-data analysis is required[14].

2.2. The MOS Switched Capacitor Integrator

Conventional filters used for audio and other low-frequency filtering functions require RC integrators (Figure 2.2(a)) with long time constants. If the time constants were realized in the form of RC products, large chip area would be required. Another disadvantage of this approach is that the absolute values of both R and C have to be tightly controlled to insure the precision of the time constants. This is extremely difficult to do with typical temperature and processing variations.

These difficulties are overcome by using the switched capacitor integrator in Figure 2.2(b), in which the resistor R in Figure 2.2(a) is replaced by the switched capacitor C_s. By switching capacitor C_s at a clock rate f_c, an equivalent resistance $R = \frac{1}{f_c C_s}$ is obtained. This results in an integrator gain constant of

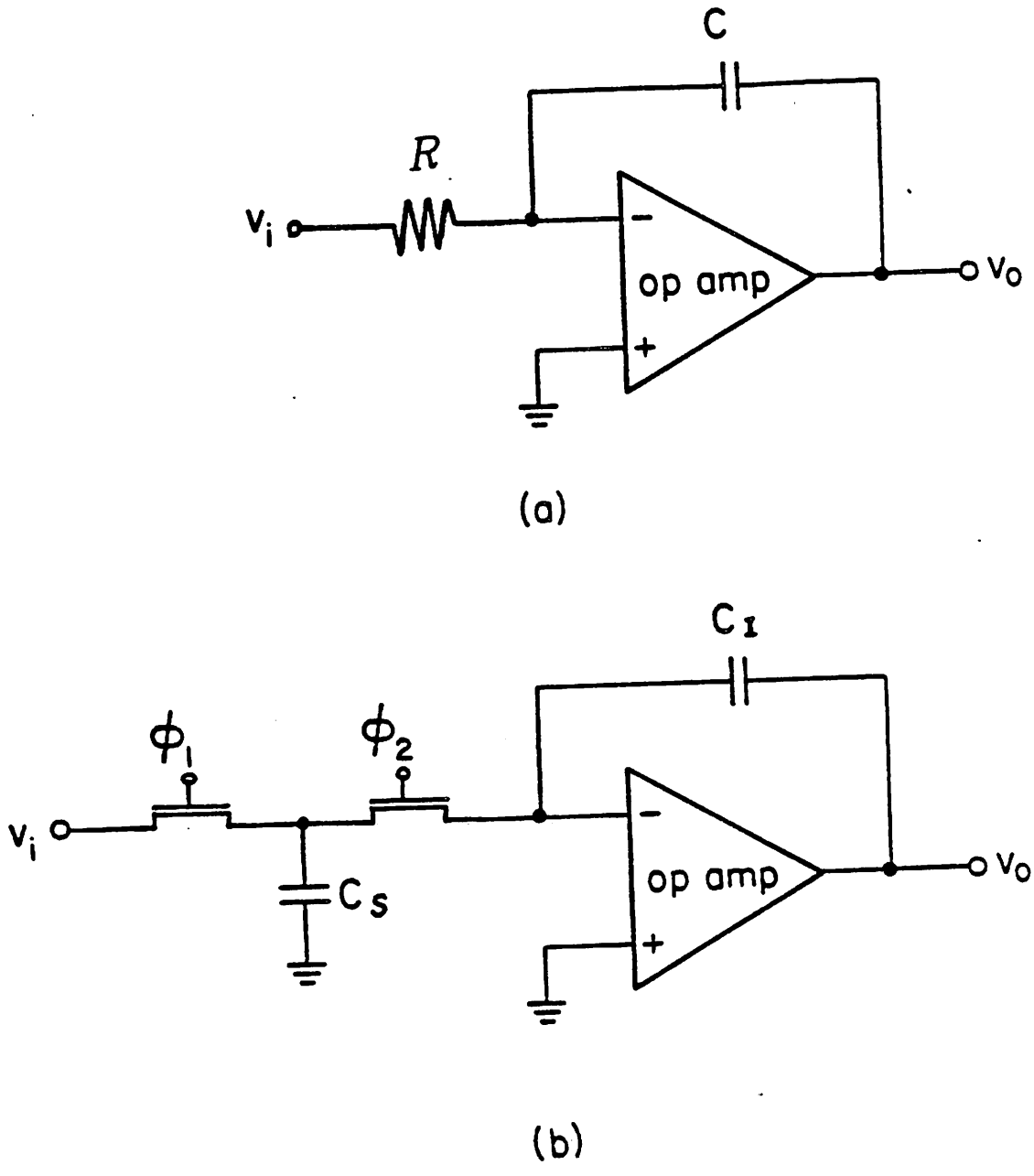


Figure 2.2

(a) R-C integrator, and (b) switched capacitor integrator.

$$\omega_0 = \frac{1}{R_{eq} C} = f_c \left| \frac{C_s}{C_I} \right| . \tag{2.4}$$

The circuit in Figure 2.2(b) can also be analyzed using the z-domain analysis and the principle of charge conservation. The z-domain transfer function can be shown to be [15

$$H(z) = - \frac{C_s}{C_I} \left| \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \right| \tag{2.5}$$

when the output of the integrator is sampled at ϕ_2. This integrator is commonly known as LDI (Lossless Digital Integrator)[16]. Assuming $f \ll f_c$, the s-domain expression of (2.5) can be obtained by replacing z by the Taylor series expansion of $e^{s T_c}$.

$$H(s) \approx - \left| \frac{C_s}{C_I} \right| \frac{f_c}{s} . \tag{2.6}$$

Hence the gain constant derived from (2.6) agrees with the intuitive result of (2.4).

Notice that in (2.4) and (2.6), the resistance value and the time constant are inversely proportional to clock frequency. Therefore by using adequate clock rate, the switched capacitor can realize very large resistance values, and therefore long time constants in a small silicon area. Meanwhile, since the integrator gain constant of (2.4) is now determined by a ratio of monolithic capacitors, high matching accuracy and excellent temperature stability are obtained in monolithic MOS implementation.

The next section will examine the various distortion sources in MOS capacitor integrators.

2.3. Distortion Sources in Switched Capacitor Circuits

The discussion in this section will be concentrated on the distortion caused by (1) nonlinearity of the capacitors, (2) nonlinearity of the operational amplifiers, (3) finite slew rate of the operational amplifiers, and (4) charge injection and clock feedthrough of the MOS switches. One major source of error in the early switched capacitor circuits is the nonlinear parasitic capacitors (e.g. the parasitic capacitors at nodes A and B in Figure 2.3 (a). However, due to the many parasitic insensitive designs [17] proposed later (for example, the bottom-plate S.C. integrator as shown in Figure 2.3 (b)), this is no longer a serious problem and will not be discussed here.

All the discussions in this section can be applied to parasitic insensitive design as well as the basic parasitic sensitive design.

2.3.1. Distortion Caused by the Finite Voltage Coefficient of Capacitors

Integrated capacitors have been widely used in MOS circuits for their excellent stability, linearity, and matching properties. These capacitors, especially the types with thermally grown silicon dioxide dielectric layers, have provided sufficient accuracy for MOS circuits like A/D converters and switched-capacitor filters. However, without extreme caution, the implementation of the systems which require 10-bit or better accuracy can be hampered by the nonidealities of capacitors. Specifically, the nonlinearity of MOS capacitors can induce significant harmonic distortion. This point is manifested by the following calculation.

For convenience, the typical single-ended LDI integrator shown in Figure 2.2(b) is repeated in Figure 2.4. The charge balance equation can be written as

$$C_2 v_o \left| (n + \frac{1}{2}) T_c \right| - C_2 v_o \left| (n - \frac{1}{2}) T_c \right| = - C_1 v_i (n T_c) . \qquad (2.7)$$

To simplify the notations, throughout this section, v_o^+, v_o^-, and v_i will be used to

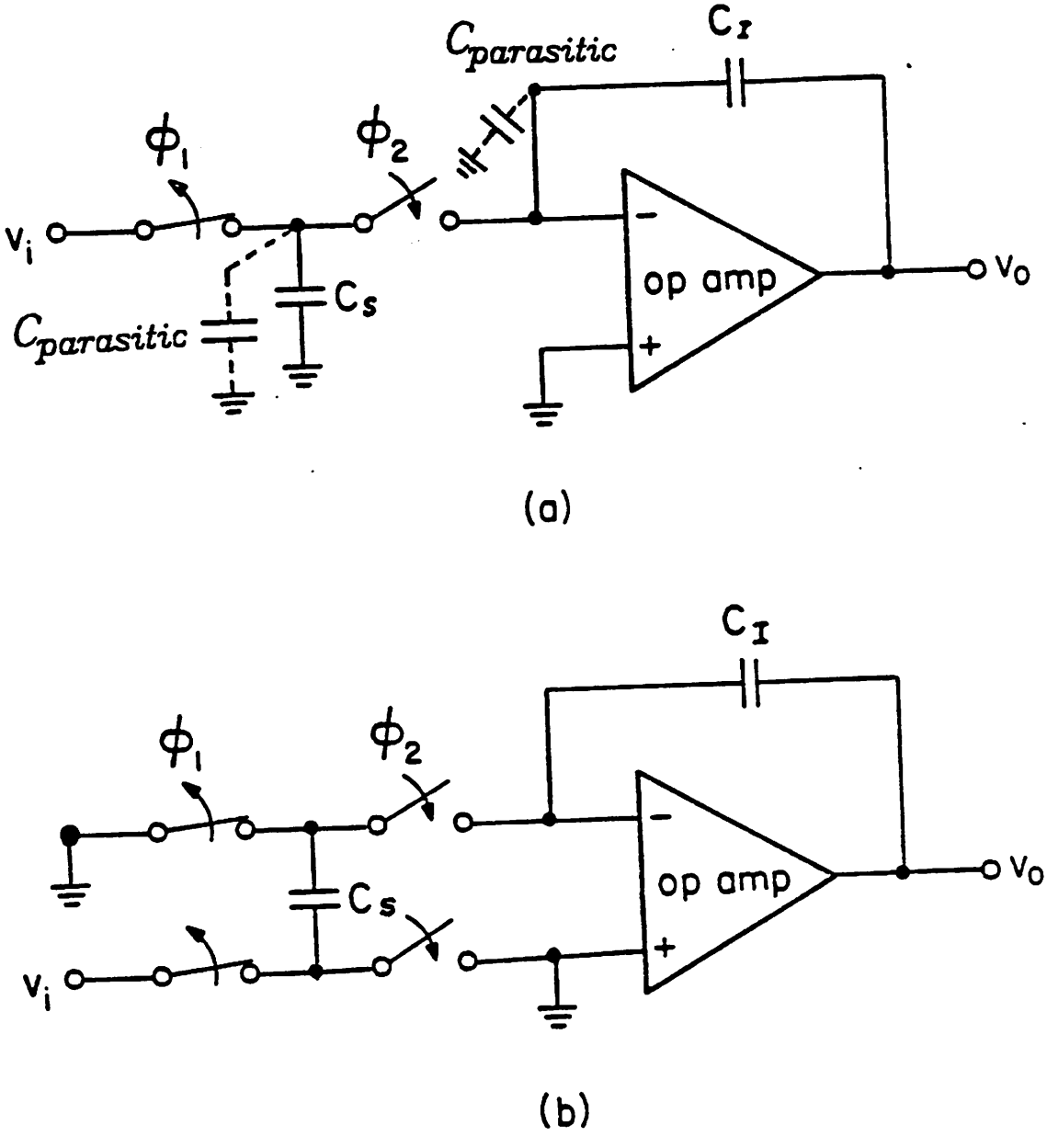
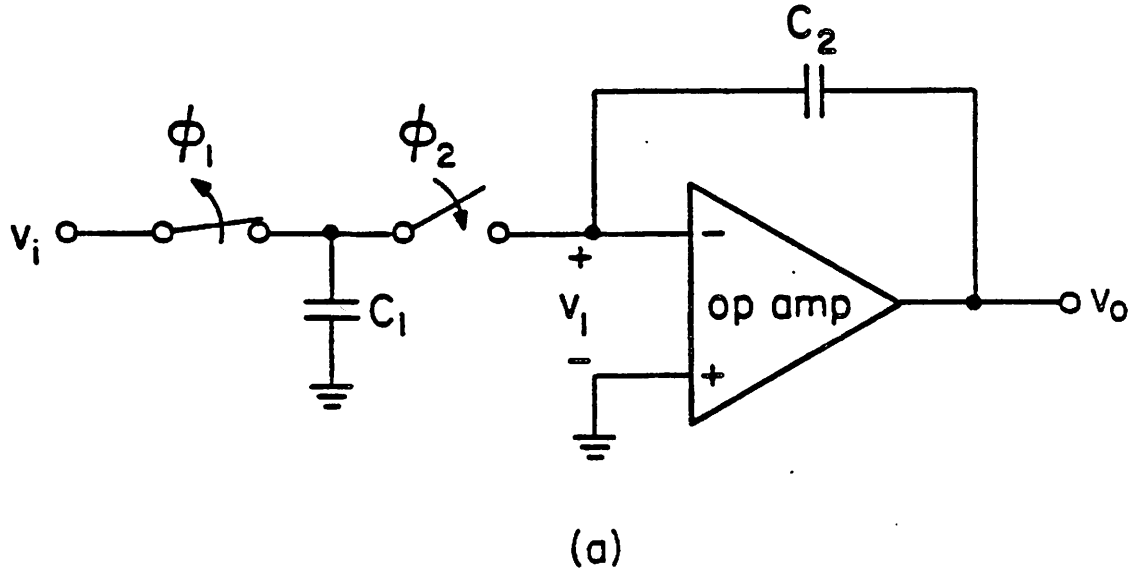


Figure 2.3

(a) Parasitic capacitors in S.C. integrator, and (b) a bottom-plate S.C. integrator, which is insensitive to paracitic capacitances.



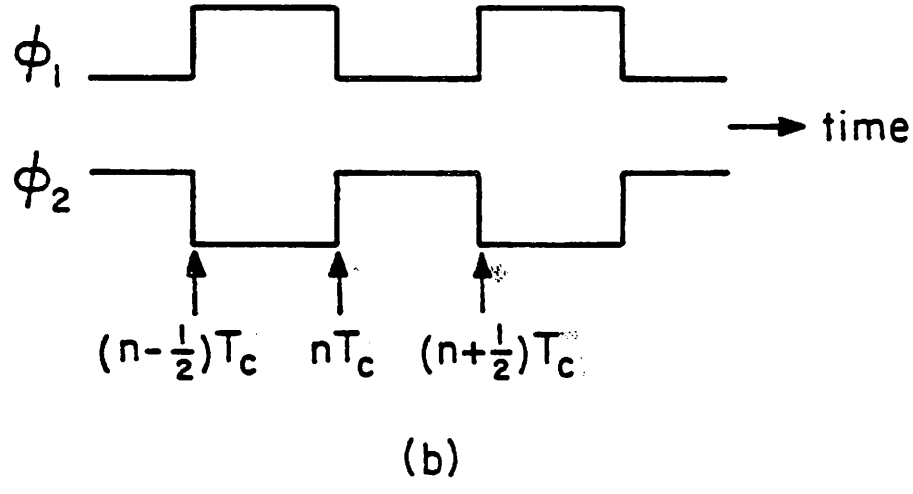


Figure 2.4

(a) Single-ended, LDI, S.C. integrator, and (b) two-phase clock.

replace $v_o\left[(n+\frac{1}{2})T_c\right]$, $v_o\left[(n-\frac{1}{2})T_c\right]$, and $v_i\ (n\ T_c)$, respectively. Equation (2.7) then becomes

$$C_2\, v_o^+ - C_2\, v_o^- = -C_1\, v_i\ . \tag{2.8}$$

Now assume everything else being ideal (i.e., ideal op-amps, ideal switches, no parasitics, etc.) and the only nonideality comes from the voltage dependence of the capacitances. Express capacitance as a function of voltage and expand it by Taylor series :

$$C_i(v) = \frac{q(v)}{v} = C_{i0}(1 + \alpha_1 v + \alpha_2 v^2 + \cdots) \qquad i = 1,2\ .$$

Retain the first three terms only, the following expressions are obtained for C_1, C_2.

$$C_i(v) \approx C_{i0}(1 + \alpha_1 v + \alpha_2 v^2) \qquad i = 1,2\ . \tag{2.9}$$

Here C_{1o}, C_{2o} are the nominal values of the capacitors at quiescent voltage, and α_1 and α_2 are the linear and quadratic voltage coefficients of the capacitance. Substitute (2.9) into (2.8) and rearrange the terms,

$$v_o^+ - v_o^- \approx -\frac{C_{10}}{C_{20}} \frac{(1 + \alpha_1 v_i + \alpha_2 v_i^2)\, v_i}{1 + \alpha_1(v_o^+ + v_o^-) + \alpha_2\left[(v_o^+)^2 + v_o^+ v_o^- + (v_o^-)^2\right]}\ .$$

Since α_1, α_2 are usually very small, the above equality can be approximated by

$$v_o^+ - v_o^- \approx -\frac{C_{10}}{C_{20}}\left\{ v_i + \alpha_1 v_i\,(v_i - v_o^+ - v_o^-) + \alpha_2 v_i\left[v_i^2 - (v_o^+)^2 - v_o^+ v_o^- - (v_o^-)^2\right]\right\}. \tag{2.10}$$

Comparing (2.10) with (2.8), it becomes obvious that each voltage step at the output now includes the errors caused by the nonlinearity of the capacitors. It can also be said

that this distorted output (by capacitor nonlinearity) is equivalent to the output of an ideal integrator with perfectly linear capacitors when all the terms in the braces of (2.10) were fed into the input of this ideal integrator. Therefore the second and the third terms in the braces of (2.10) can be considered as the input referred errors caused by the capacitor nonlinerity.

The nature of the error terms in (2.10) can be seen more clearly by considering the sinusoidal case. When the input to the integrator is a sampled sinusoid, and the errors caused by the capacitor voltage coefficients are small, v_i and $v_o^{\pm}$ in the error terms of (2.10) can be approximated to the first order by the input and output of an ideal integrator [15], i.e.

$$v_i = V_{i1}\cos\omega_1 nT_c + V_{i2}\cos\omega_2 nT_c . \tag{2.11a}$$

$$v_o^{\pm} = V_{o1}\sin\omega_1(n \pm \frac{1}{2})T_c + V_{o2}\sin\omega_2(n \pm \frac{1}{2})T_c \tag{2.11b}$$

$$= -\frac{C_{10}}{C_{20}}\frac{V_{i1}}{2\sin\frac{\omega_1 T_c}{2}}\sin\omega_1(n \pm \frac{1}{2})T_c \tag{2.11c}$$

$$-\frac{C_{10}}{C_{20}}\frac{V_{i2}}{2\sin\frac{\omega_2 T_c}{2}}\sin\omega_2(n \pm \frac{1}{2})T_c .$$

Here V_i , ω_o are the amplitude and the radian frequency of the input signal, respectively, and T_c is the period of the sampling clock. Substitute (2.11) into (2.10), (2.10) becomes

$$v_o^{+} - v_o^{-} \approx -\frac{C_{10}}{C_{20}}\left[A_0 + A_1\cos\omega_1 nT_c + A_2\cos\omega_2 n_c T + A_3\cos(2\omega_1 nT_c + \theta_a)\right. \tag{2.12}$$

$$\left. + A_4\cos(2\omega_2 nT_c + \theta_b) + A_5\cos((\omega_1 + \omega_2)nT_c + \theta_c)\right.$$

$$+ A_6 \cos((\omega_1 - \omega_2)\, nT_c + \theta_d) + A_7 \cos 3\omega_1 nT_c + A_8 \cos 3\omega_2 nT$$

$$+ A_9 \cos((\omega_1 + 2\omega_2)\, nT_c) + A_{10} \cos((\omega_1 - 2\omega_2)\, nT_c)$$

$$+ A_{11} \cos((2\omega_1 + \omega_2)\, nT_c) + A_{12} \cos((2\omega_1 - \omega_2)\, nT_c) \Big|$$

where A_0–A_{12} are the amplitudes of different frequency components. Parameters $\theta_1, \theta_2, \theta_3$, and θ_4 are the phase angles of the harmonic terms. The exact expressions of these coefficients are not given here for the sake of brevity.

The error terms in (2.12) are input referred. When observed at the integrator output, the harmonic terms are listed below. Here the often encountered condition : $\omega T_c \ll 1$ is applied. The condition $V_{i1} = V_{i2}$ is also assumed to simplify the expressions.

$$HD_2 \approx \frac{\alpha_1}{2} \sqrt{V_o^2 + (\frac{V_i}{2})^2}. \tag{2.13a}$$

$$HD_3 \approx \frac{\alpha_2}{4} (Vo^2 + \frac{V_i^2}{3}). \tag{2.13b}$$

$$IM_2(\omega_1 + \omega_2, \omega_1) \approx \frac{\omega_1}{\omega_1 + \omega_2} \alpha_1 (V_{o1} + V_{o2}). \tag{2.13c}$$

$$IM_2(\omega_1 - \omega_2, \omega_1) \approx \frac{\omega_1}{\omega_1 - \omega_2} \alpha_1 (V_{o2} - V_{o1}). \tag{2.13d}$$

$$IM_3(2\omega_1 + \omega_2, \omega_1) \approx \frac{\omega_1}{2\omega_1 + \omega_2} \frac{3\alpha_2}{4} (V_{o1}^2 + 2V_{o1}V_{o2}). \tag{2.13e}$$

$$IM_3(2\omega_1 + \omega_2, \omega_2) \approx \frac{\omega_2}{2\omega_1 + \omega_2} \frac{3\alpha_2}{4} (V_{o1}^2 + 2V_{o1}V_{o2}). \tag{2.13f}$$

$$IM_3(2\omega_1 - \omega_2, \omega_1) \approx \frac{\omega_1}{2\omega_1 - \omega_2} \frac{3\alpha_2}{4} (V_{o1}^2 - 2V_{o1}V_{o2}). \tag{2.13g}$$

$$IM_3(2\omega_1 - \omega_2, \omega_2) \approx \frac{\omega_2}{2\omega_1 - \omega_2} \frac{3\alpha_2}{4} (V_{o1}^2 - 2V_{o1}V_{o2}). \tag{2.13h}$$

Note that only half of the possible expressions of the harmonic terms are listed here.

The other half can be obtained by replacing ω_1 by ω_2, and V_{o1} by V_{o2}. The harmonic distortion of a S.C. integrator for some typical circuit parameters is plotted in Figure 2.5. The above results are also verified by the simulation program SWAP[18].

Note that when $V_i \ll V_o$ is true, analogy to the continuous-time circuits can be drawn. First, as in the case of continuous-time circuits, HD_2 is proportional to the output voltage and HD_3 proportional to the square of the output voltage. Another analogy also becomes evident when $\omega_1 \approx \omega_2$, where $IM_2 \approx HD_2 + 6\,dB$ and $IM_3 \approx HD_3 + 9.5\,dB$ [19].

The above analysis is valid when the integrator is single-ended. It can be seen from equation (2.10) that for a fully differential integrator, the squared terms (the terms associated with α_1) in the positive and negative outputs cancel each other and no second harmonic is generated in the differential output. Other advantages of using the fully differential approach include better power supply rejection and the reduction of clock feedthrough. The penalties for using the fully differential approach are the increased chip area and the more complex circuit.

2.3.2. Distortion Caused by Op Amp Gain Nonlinearity

While an ideal op amp with perfectly linear gain does not introduce any harmonic distortion, real op amps usually have some nonlinearity in their gain characteristics and therefore introduce distortion into the S.C. circuits. When the nonlinearity is small, the magnitude of this distortion can be estimated as follows.

Again consider the integrator in Figure 2.4, and assume that the only nonlinearity exists in the op amp. Also assume that the op amp has a finite gain, and that its output voltage can be expressed as a power series in terms of the op amp input voltage

$$v_o = a_1 v_1 + a_2 v_1^2 + a_3 v_1^3 + \cdots \tag{2.14}$$

Here v_1 is the voltage across the op amp input terminals as shown in Fig. 2.4. Using

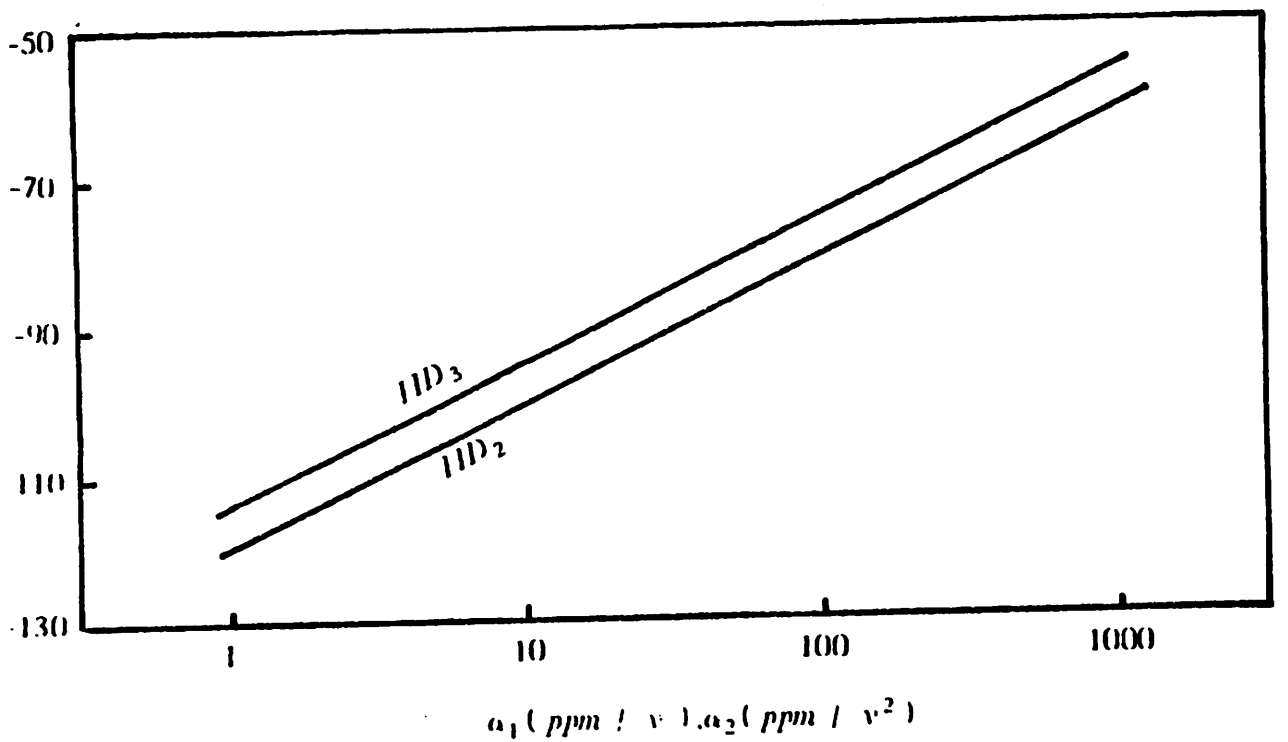


Figure 2.5 Harmonic distortion vs. voltage coefficients of capacitor : V_o = 3v, C_2 / C_1 = 5, f_{signal} = 10kHz , f_{clock} = 500kHz .

the notations developed in the previous subsection, the charge conservation equation can be written as

$$C_1 v_i = C_1 v_1^+ + C_2 \left[(v_1^+ - v_o^+) - (v_1^- - v_o^-) \right]. \tag{2.15}$$

Use (2.14) in (2.15) and assume that (1) only the first three terms on the right hand side of (2.14) are significant, and (2) the first (linear) term is much larger than the other two terms. Then (2.15) can be written as

$$v_o^+ - v_o^- \approx -\frac{C_1}{C_2} \left\{ (1 + \frac{1}{a_1 \beta}) v_i - \frac{a_2}{a_1^3 \beta} \left[v_i \, (v_o^+ + v_o^-) - (v_o^+)^2 \right] \right. \tag{2.16}$$

$$\left. - \frac{a_3}{a_1^4 \beta} \left[v_i \left[(v_o^+)^2 + (v_o^+)(v_o^-) + (v_o^-)^2 \right] - (v_o^+)^3 \right] \right\}.$$

where $\beta = \frac{C_2}{(C_1 + C_2)}$ is the feedback factor of the integrator. Following the same argument used for (2.10), the second and third terms in the braces represent the input referred errors. Furthermore, comparing the equations (2.10) and (2.16), it can be seen that they have very similar forms so the same technique can be applied to (2.16) to obtain the harmonics. That is, (2.11a) and (2.11b) can be used in (2.16) to derive the input-referred harmonic terms. The complete result is rather involved. However, applying the conditions $V_{i1} = V_{i2}$, and $\omega T_c \ll 1$ again, the harmonics caused by op-amp gain nonlinearity can be listed below.

$$HD_2 \approx \frac{a_2}{2 a_1^3 \beta} V_o \sqrt{1 + (\frac{V_o}{2 V_i})^2}. \tag{2.17a}$$

$$HD_3 \approx \frac{a_3}{4 a_1^4 \beta} V_o^2 (1 + \frac{V_o}{3 V_i}). \tag{2.17b}$$

$$IM_2(\omega_1 + \omega_2, \omega_1) \approx \frac{a_2}{a_1^3 \beta} \frac{\omega_1}{\omega_1 + \omega_2} \frac{1}{V_{i1}} \sqrt{(V_{o1} V_{o2})^2 + (V_{i1} V_{o2} + V_{i2} V_{o1})^2}. \tag{2.17c}$$

$$IM_2(\omega_1-\omega_2,\omega_1)\approx\frac{a_2}{a_1^3\beta}\frac{\omega_1}{\omega_1-\omega_2}\frac{1}{V_{i1}}\sqrt{(V_{o1}V_{o2})^2+(V_{i1}V_{o2}-V_{i2}V_{o1})^2}\quad(2.17d)$$

$$IM_3(2\omega_1+\omega_2,\omega_1)\approx\frac{3a_3}{4a_1^4\beta}\frac{\omega_1}{2\omega_1+\omega_2}\left(V_{o1}^2-\frac{2V_{o1}V_{o2}}{3}-\frac{V_{o1}^2V_{o2}}{V_{i1}}\right).\quad(2.17e)$$

$$IM_3(2\omega_1+\omega_2,\omega_2)\approx\frac{3a_3}{4a_1^4\beta}\frac{\omega_2}{2\omega_1+\omega_2}\left(V_{o1}^2-\frac{2V_{o1}V_{o2}}{3}-\frac{V_{o1}^2V_{o2}}{V_{i2}}\right).\quad(2.17f)$$

$$IM_3(2\omega_1-\omega_2,\omega_1)\approx\frac{3a_3}{4a_1^4\beta}\frac{\omega_1}{2\omega_1-\omega_2}\left(V_{o1}^2+\frac{2V_{o1}V_{o2}}{3}+\frac{V_{o1}^2V_{o2}}{V_{i1}}\right).\quad(2.17g)$$

$$IM_3(2\omega_1-\omega_2,\omega_2)\approx\frac{3a_3}{4a_1^4\beta}\frac{\omega_2}{2\omega_1-\omega_2}\left(V_{o1}^2+\frac{2V_{o1}V_{o2}}{3}+\frac{V_{o1}^2V_{o2}}{V_{i2}}\right).\quad(2.17h)$$

Again the above results are verified by the simulation program SWAP. Note that the input/output relationship (2.11c) is no longer valid here, due to the assumption that the op-amp has a finite gain. Given an op-amp with finite gain A_0, the input/output relationship can be approximated by

$$\frac{V_o}{V_i}\approx\frac{A_0}{1+j\frac{C_2}{C_1}A_0\omega T}\quad(2.18)$$

Equation (2.18) has to be used in the calculation of (2.17). Frequency dependence is found when substituting (2.18) into (2.17). For example, low frequency poles and zeroes can be found when substituting (2.18) into (2.17b) :

$$f_{pole}\approx\frac{C_1f_s}{2\pi A_0C_2}\quad(2.19a)$$

$$f_{zero}\approx\frac{C_1f_s}{6\pi C_2}\quad(2.19b)$$

Note that the term $\frac{C_1f_s}{C_2}$ in (2.19) corresponds to the factor $\frac{1}{RC}$ in the continuous-time case[20]. From the above discussion, it is obvious that the DC gain of the op amp has to be sufficiently high in order to reduce the harmonic distortion at low frequencies. The harmonic distortion caused by op amp nonlinearity for some typical circuit

parameters is plotted in Figure 2.6.

Similar to the capacitor nonlinearity case, when the op amp is fully differential and the gain characteristics is symmetrical for the positive and negative polarities, the even harmonics will disappear, as can be seen from (2.16).

Also note again that at sufficiently high frequency (at frequencies higher than the pole and zero frequencies in (2.19)), HD_2 and HD_3, are proportional to the voltage and the square of the voltage, respectively. This property is also similar to that in the continuous-time circuits.

The results derived in the last two subsections can also be obtained by using the method of Volterra series (see Appendix II).

2.3.3. Distortion Caused by the Finite Slew Rate of Amplifiers

Due to the sampled-data nature of the switched capacitor filter, all the voltage signals within the filter exist in the sampled-data form, and only the output of the last op-amp goes out continuously. So, unlike the previously described distortion types, the distortion caused by the finite slew rate occurs only in the last op-amp. For small-signal steps the op-amp does not slew limit, whereas for large signal steps it does and this represents a nonlinearly behavior. Figure 2.7(a) shows the output, v_o, of an ideal amplifier with zero rise time. A more realistic output - that of an amplifier which is always linear and has a constant rise time - is shown in (b) and labeled as v_l. Shown in (c) is the response, v_s, of a slew-limited amplifier with an output that always changes at a finite rate. Error signals $v_o - v_l$ and $v_o - v_s$ are shown in (d) and (e). Clearly (c) is nonlinear since doubling the input would not double the error. Instead both the height and width of the error triangle change with the input.

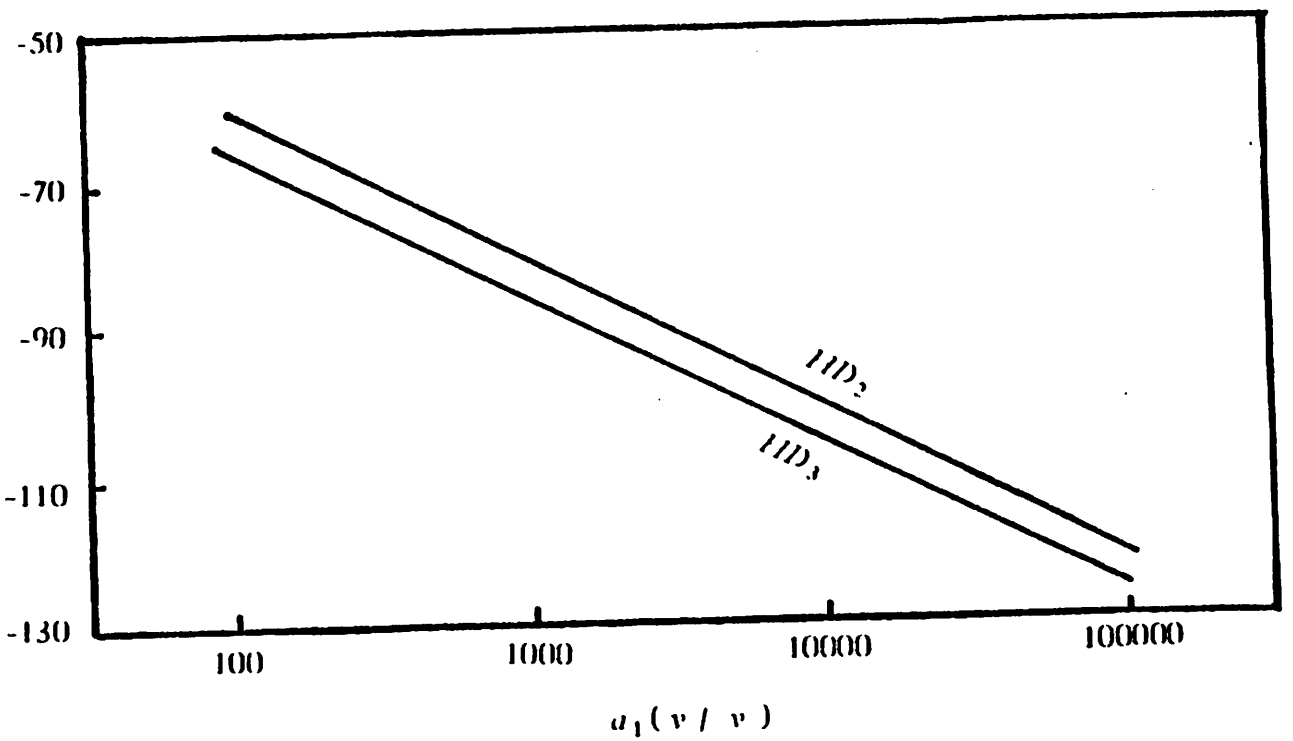


Figure 2.6 Harmonic distortion vs. op amp DC gain: $C_2 / C_1 = 5$, $f_{signal} = 10kHz$, $f_{clock} = 500kHz$, $a_2 v_1 / a_1 = 0.1$, $a_3 v_1^2 / a_1 = 0.1$.

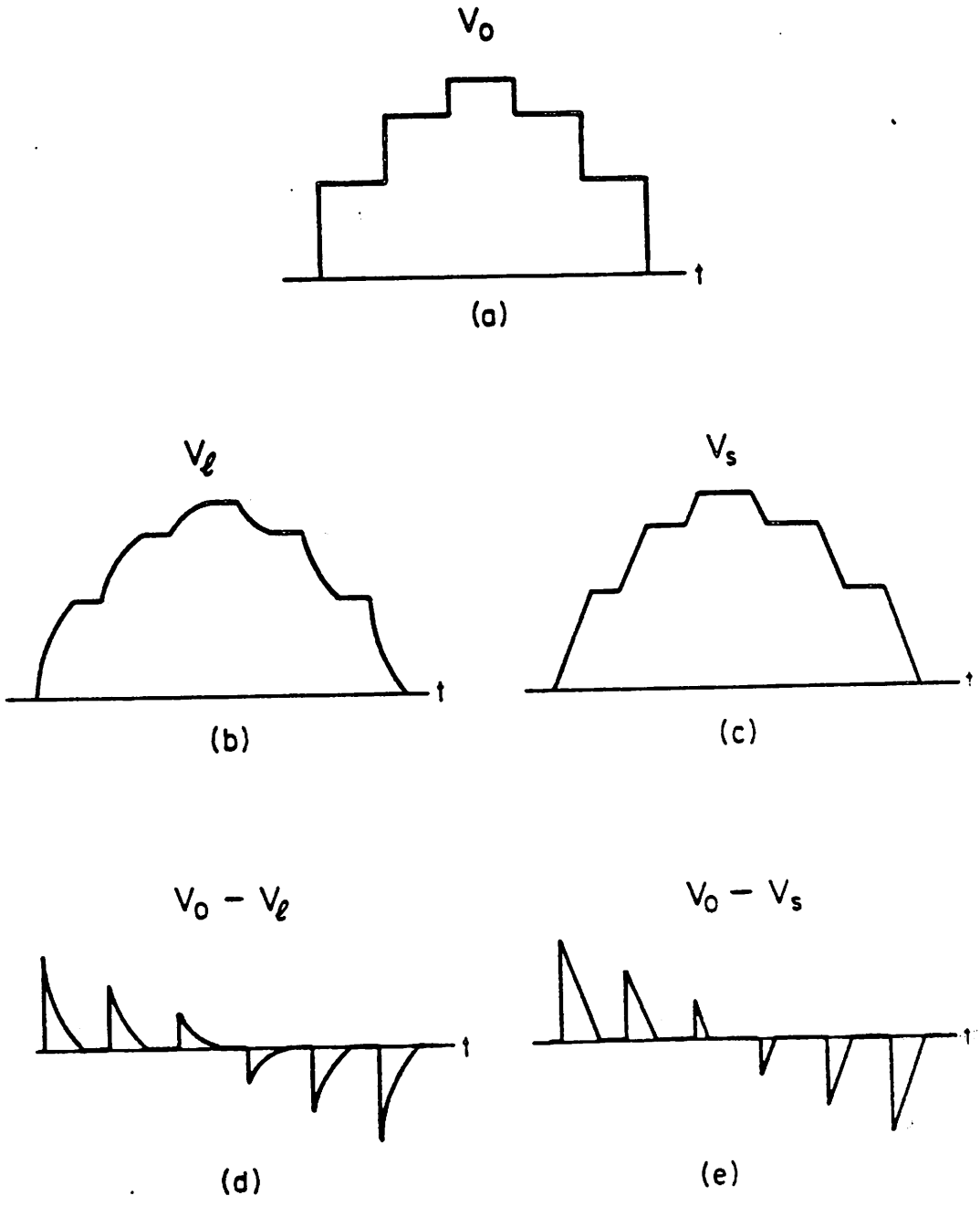


Figure 2.7

(a) Ideal output with zero rise time, (b) "linear" output (constant rise time), (c) slew-limited output, (d) difference between (a) and (b), and (e) difference between (a) and (c).

To obtain a feeling for the kind of distortion caused by slew rate limiting, consider the following model (Figure 2.8)[21]. As long as the output error is a series of narrow pulses, a reasonable first-order model is an impulse stream. The weights of the impulses should vary as the square of the transition voltage (this transition voltage is defined as the difference between the present output voltage and the output voltage at the previous sampling instant), reflecting the modulation of both the height and width of the triangular pulse. In this model, v_o is the desired output. $x(t)$ is the transition voltage as defined above. The distortion box $y = x|x|$ generates the nonlinear dependence of the error. Notice that the function y has the same sign as $x(t)$ while the magnitude is the square of $x(t)$. The model is complete except for the specification of the impulse weights. Assume that in a certain transition the op-amp slews V_x volts in τ seconds. Then an error of area $V_x\tau/2$ volt-seconds results. Since the model gives rise to $x(t) = V_x$, $y(t) = V_x^2$. Then the error predicted is AV_x^2. Therefore the impulse weight A is $\tau/2V_x$, or $1/2S_r$ where S_r is the slew rate of the op-amp.

Now consider a sinusoidal output. If the signal $v_o(t)$ consists of samples of the sinusoid

$$v_o(t) = V_o \sin \omega_o n T_c . \qquad n T_c \leqslant t < (n+1)T_c .$$

Then from the definition of $x(t)$, it is obvious that

$$x(t) = V_o \sin \omega_o n T_c - V_o \sin \omega_o (n-1) T_c$$

$$= 2 V_o \sin \frac{\omega_0 T_c}{2} \cos \omega_o \left(n - \frac{1}{2}\right) T_c . \qquad n T_c \leqslant t < (n+1)T_c . \tag{14}$$

The difference operation thus generates samples of a cosine waveform that has been phase shifted and changed in magnitude. Since it is not relevant to the final result, the phase shift will be ignored here. The output of the distortion generator $y = x|x|$

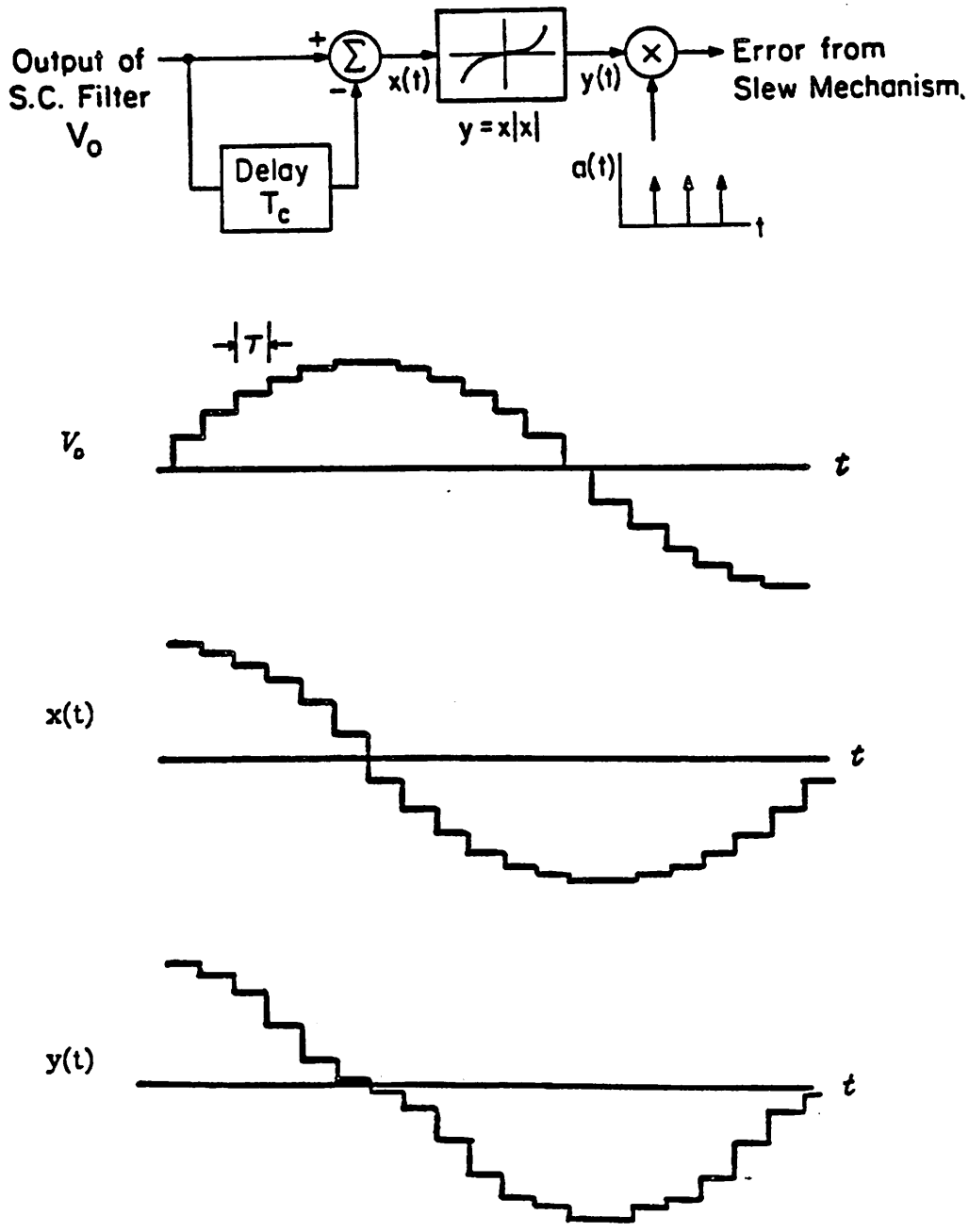


Figure 2.8

Model for slew distortion.

consists samples of a harmonically distorted sinusoid:

$$y'(t) = (2V_o \sin\frac{\omega_o T_c}{2})^2 \cos\omega_o t \ |\cos\omega_o t\ |. \tag{15}$$

$$y(t) = y'(n T_c). \qquad n T_c \leq t < (n+1)T_c .$$

The waveform $y'(t)$ contains only odd harmonics whose magnitudes are

$$Y'(k) = \frac{4(2V_o \sin\frac{\omega_o T_c}{2})^2}{\pi k (k^2-4)}; \qquad k = 1, 3, 5, 7, \cdots . \tag{16}$$

This signal $y(t)$ is then multiplied by the impulse train $a(t)$. Each of the harmonic magnitudes of $y'(t)$ is thereby multiplied by the weighting factor $\frac{1}{2S_r T_c}$. Thus the k^{th} harmonic becomes

$$HD_k = \frac{Y'(k)}{V_o} = \frac{1}{2S_r T_c} \frac{4(2V_o \sin\frac{\omega_o T_c}{2})^2}{\pi k (k^2-4)} \frac{1}{V_o}$$

$$= \frac{8(\sin\frac{\omega_o T_c}{2})^2}{\pi k (k^2-4)} \frac{V_o}{S_r T_c}; \qquad k = 1, 3, 5, 7, \cdots . \tag{17}$$

Note that the result derived here represents the worst case, since the slew-limiting is assumed for all the rise and fall edges.

The above derivation shows that, as long as the slew rate is symmetrical , only odd harmonics can be present. Even harmonics are introduced only when the slew rate is not symmetrical for different polarities. The slew induced distortion as function of the signal-sampling frequency ratio for two typical cases are shown in Figure 2.9.

From Figure 2.9(a) it is seen that the slew rate has to be very high in order to reduce HD_3 to below -80 dB for signal frequencies lower than 20kHz. This constraint

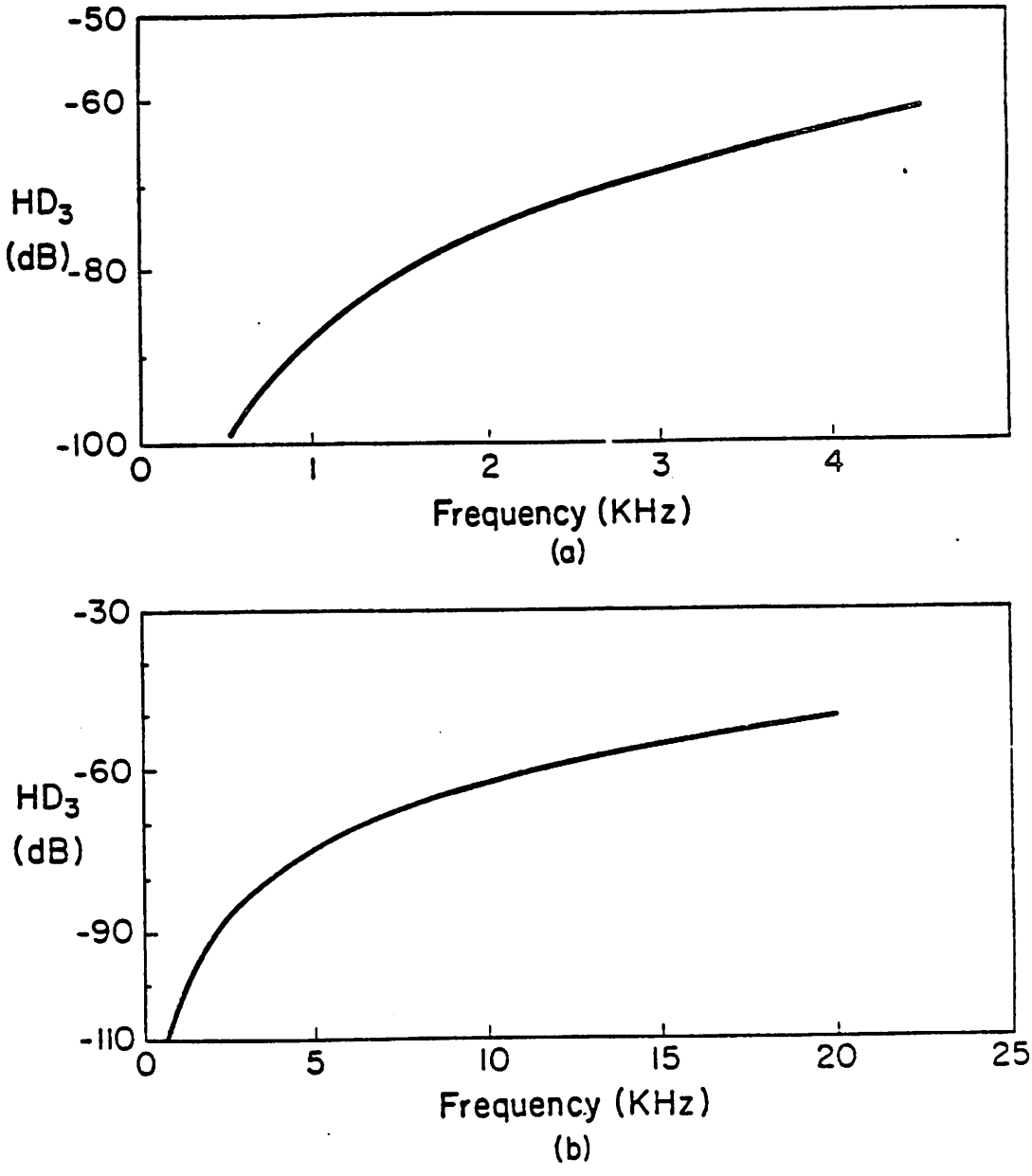


Figure 2.9

Slew induced distortion, (a) 4kHz bandwidth, n = 3 , f_{clock} = 128kHz, S_r = 1 v/usec , V_o = 3v , (b) 4kHz bandwidth, n = 3 , f_{clock} = 500kHz, S_r = 1 v/usec , V_o = 3v .

significantly increases the design difficulty as well as the power consumption of the operational amplifier. There are two approaches to resolve this problem : (1) resample the output of the operational amplifier with a very fast sample-hold circuit; (2) design the op-amp such that each step in the output voltage always rises in a linear fashion (e.g. exponential rise). This can be done only when the output current never saturates regardless of the magnitude of the input, and a class A/B operational amplifier can be a good candidate for this purpose. Shown in Figure 2.10 is the simulated step response of an integrator using a typical class A/B operational amplifier (see Chapter 3). This step response is very close to that of an ideal linear system since it always has approximately the same rise time regardless of the step amplitude.

2.3.4. Distortion Caused by the Clock Feedthrough and Charge Injection

MOS switches can introduce a significant amount of error due to the clock feedthrough via the gate/source and gate/drain overlap capacitance and the injection of the channel charge stored in the MOS transistors (Figure 2.11) [22]. Given an MOS switch, the error generated on an adjacent node is a complex function of the clock fall time, the sampling capacitor size, node voltage, and the impedance level seen at that node. For a typical $5\,\mu m \times 5\,\mu m$ MOS transistor, the error due to each clock transition can be as high as 20 mv. Since this error is often voltage dependent, it is an important source of harmonic distortion and has to be minimized. Traditionally three design approaches were used to minimize this error for a given process. The first approach is to increase the size of the switched capacitor such that the induced voltage error is smaller. The second approach is to use a dummy switch [23], as shown in Figure 2.12. Here a dummy switch M_2 is used. This transistor switch has half the gate area of M_1 and opposite clocking. During a clock transition the dummy switch generates the same amount of charge with opposite polarity and cancels the charge injection effect of the switch M_1. The third approach is to use transmission gates, where a p-channel

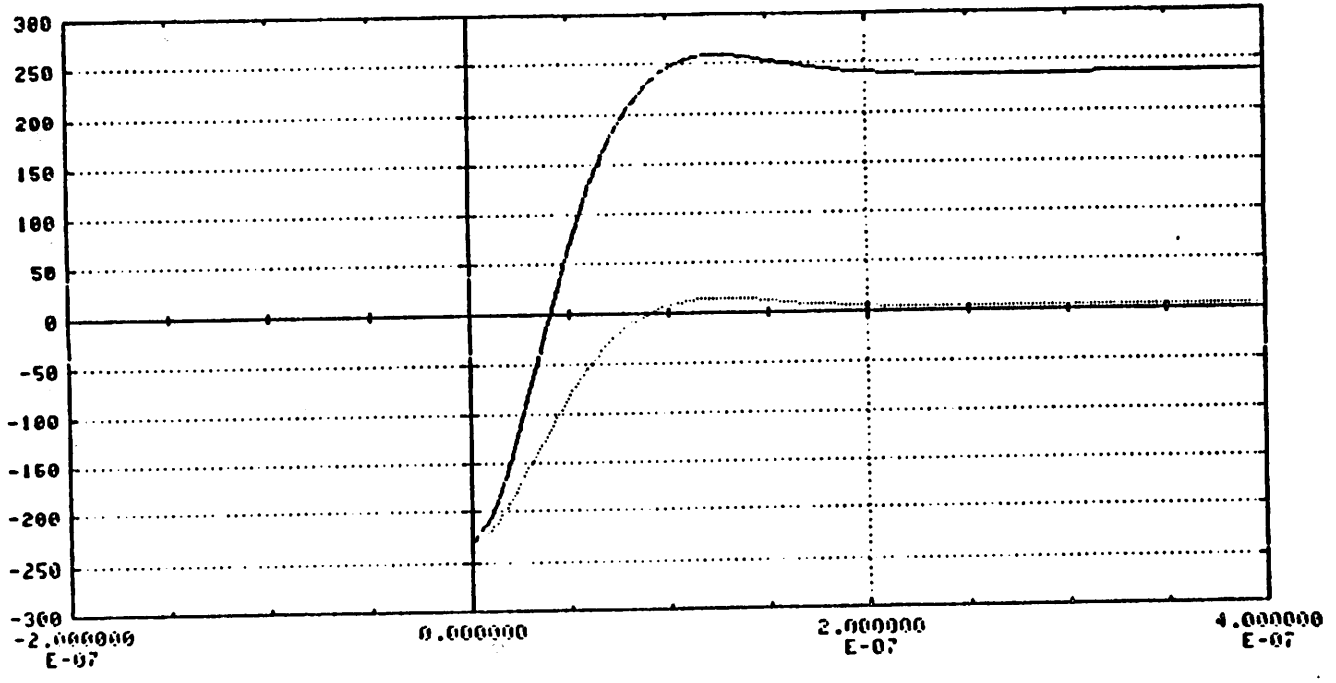
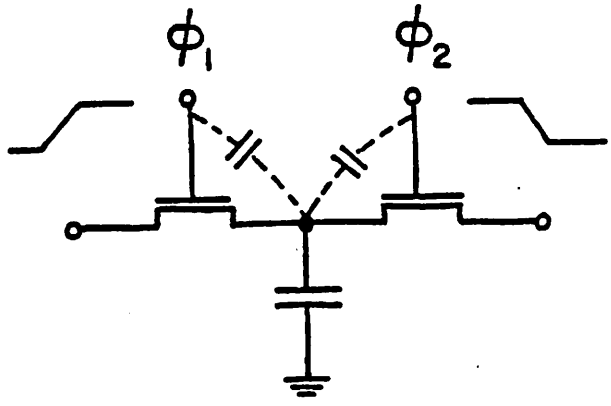
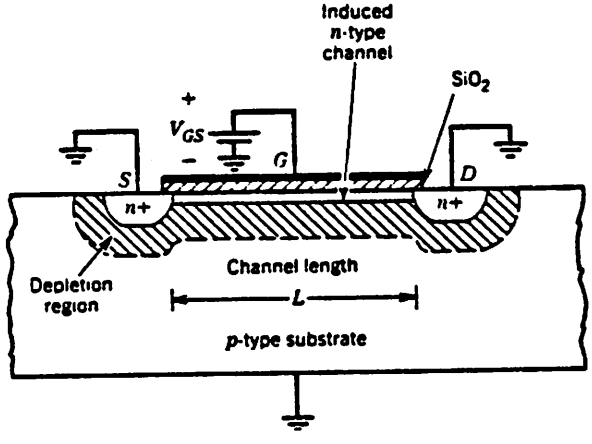


Figure 2.10 Simulated step response of class A/B op amp.



(a)



(b)

Figure 2.11

Parasitic capacitance and clock feedthrough (Reprinted from "Analysis and Design of Analog Integrated Circuits", P. R. Gray and R. G. Meyer, 1984).

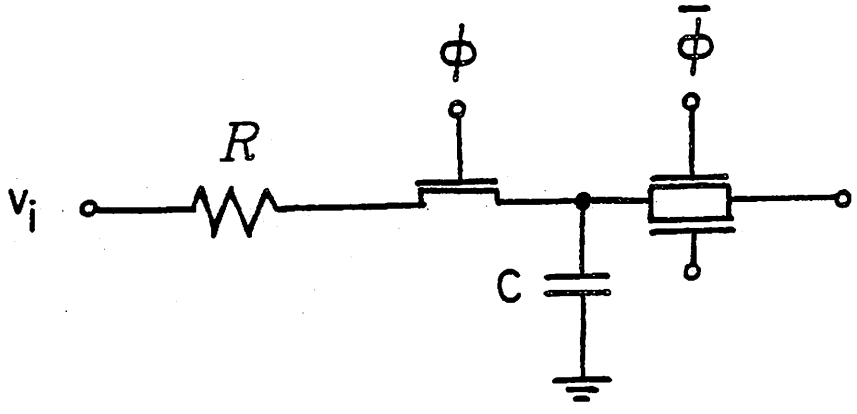


Figure 2.12

Adding a dummy switch to reduce charge injection errors.

transistor is connected in parallel with an n-channel transistors. Since channel charges of different polarities are induced for different transistors. the clock related errors can be partially cancelled. These approaches and the improved versions of them will either reduce the speed of the circuit or increase the circuit complexity and still cannot obtain exact cancellation of the clock related errors.

In the next chapter. a new clock error cancellation scheme will be proposed. This scheme can theoretically eliminate. and experimentally reduce the clock related errors. as will be seen in the next two chapters.

CHAPTER 3

DESIGN CONSIDERATIONS FOR LOW DISTORTION S.C. FILTERS

In the last chapter, it was shown that the harmonic distortion of a S.C. integrator is related to the nonlinearity of the op amps, the peak signal level of the output nodes, the nonlinearity of the MOS capacitors, the op amp slew rate, and the clock related noise (clock feedthrough and channel charge injection). It was also shown that, due to the usually small voltage coefficients of the MOS capacitors, the total harmonic distortion (THD) is usually dominated by the other sources.

In this chapter, the results obtained in the last chapter are applied toward the design of low-distortion S.C filters. Design techniques for eliminating or reducing errors from different distortion sources are discussed.

3.1. Dynamic-Range Considerations and Node Voltage Scaling

The dynamic range of a S.C. filter [1, 24] is usually defined as the ratio of the RMS output voltage at a given THD level to the total output noise RMS voltage within a specified bandwidth. However, as shown in Figure 3.1, the filter output voltage does not always experience the largest swing among all the filter nodes, and the voltages at some filter internal nodes may be larger than the filter output voltage. In that case these internal nodes will be clipped first and become the major limiting factor in the filter dynamic range. The maximum dynamic range of the filter is achieved when all the op amp outputs have the same peak voltage. Therefore, it is advantageous to scale the voltages at different nodes such that the dynamic range is optimized for noise and distortion. A scaling technique which can be used to independently scale all internal nodes (either current or voltage nodes) is described as follows.

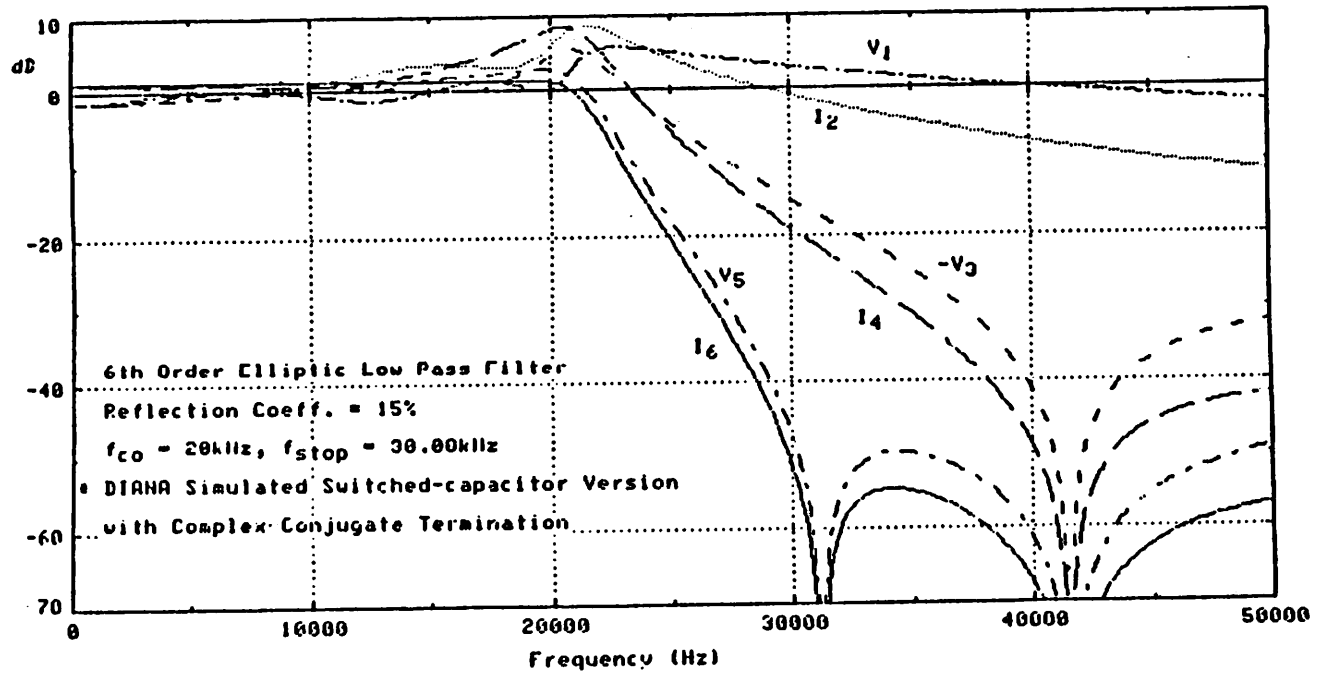


Figure 3.1 A typical frequency response of filter internal nodes.

A section of an unscaled, LDI S.C. ladder filter is shown in Figure 3.2. In the z-domain, the three unscaled output voltages are as follows:

$$V_{n-1}(z) = \left[\frac{f\ C_u}{C_{n-1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\left[V_{n-2}(z) - V_n(z)\right]. \qquad (3.1a)$$

$$V_n(z) = \left[\frac{f\ C_u}{C_n}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\left[V_{n-1}(z) - V_{n+1}(z)\right]. \qquad (3.1b)$$

and

$$V_{n+1}(z) = \left[\frac{f\ C_u}{C_{n+1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\left[V_n(z) - V_{n+2}(z)\right]. \qquad (3.1c)$$

Assume that it is desired to scale the voltage V_n by a factor of k without affecting the other output nodes, so that after scaling,

$$\frac{V_n(z)}{k} = \left[\frac{f\ C_u}{k\ C_n}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\left[V_{n-1}(z) - V_{n+1}(z)\right]. \qquad (3.2)$$

From this equation, it is apparent that the voltage at any node can be scaled by simply changing the gain constant for that integrator, i.e. $C_n \rightarrow k\ C_n$. In addition, if a node is scaled by k, the inputs driven from that node must be scaled by $\frac{1}{k}$ in order to insure that the other integrator outputs are unchanged. For the previous example, this requires that

$$V_{n-1}(z) = \left[\frac{f\ C_u}{C_{n-1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]V_{n-2}(z) - \left[\frac{k\ f\ C_u}{C_{n-1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\frac{V_n(z)}{k}, \qquad (3.3a)$$

and

$$V_{n+1}(z) = \left[\frac{k\ f\ C_u}{C_{n+1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]\frac{V_n(z)}{k} - \left[\frac{f\ C_u}{C_{n+1}}\right]\left[\frac{z^{-1/2}}{1-z^{-1}}\right]V_{n+2}(z). \qquad (3.3b)$$

Equation (3.3) shows that all of the switched capacitors driven from a scaled node, $\frac{V_n(z)}{k}$, are changed to a value of $k\ C_u$. In general, two additional switched capacitors

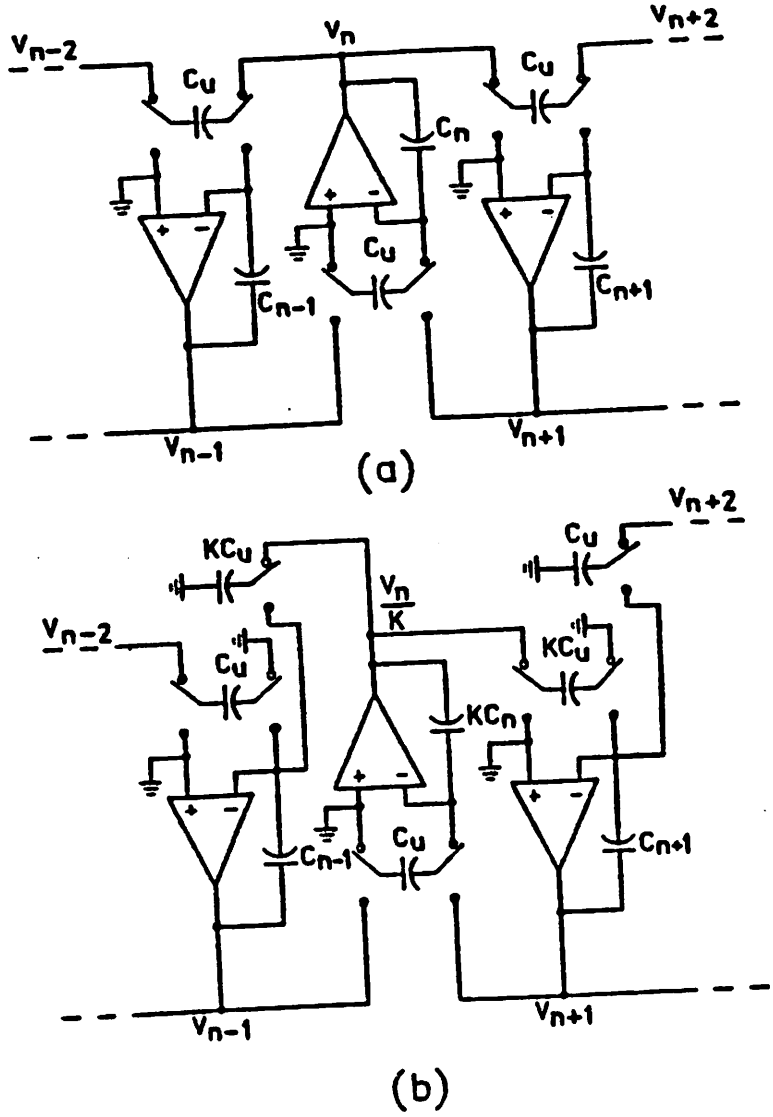


Figure 3.2

A section of a switched capacitor ladder filter (a) before and (b) after node-voltage scaling (reprint from D. Allstot's Ph.D. dissertation).

are added for each scaled node, and if k is not an integer, the capacitor matching accuracy between the different sized switched capacitors is slightly reduced.

However, there is a tradeoff between noise and distortion. This tradeoff is illustrated by assuming that the gain from the input to the output of the filter is constant. For an arbitrary internal node, V_x, the following relationships apply for the unscaled and scaled versions, respectively:

$$\frac{V_{out}}{V_{in}} = \left|\frac{V_{out}}{V_x}\right|\left|\frac{V_x}{V_{in}}\right|. \tag{3.4a}$$

and

$$\frac{V_{out}}{V_{in}} = \left|\frac{V_{out}}{V_x / k}\right|\left|\frac{V_x / k}{V_{in}}\right| = \left|\frac{k\,V_{out}}{V_x}\right|\left|\frac{V_x}{k\,V_{in}}\right|. \tag{3.4b}$$

The first term in both equations is a measure of the noise gain from V_x to the output of the filter, and the second term represents the magnitude of the peak signal at node V_x relative to the input. Hence, the first term determines the noise performance, and the second term determines the distortion performance. Notice from equation (3.4b), that as the noise gain is increased by k, the peak amplitude at V_x is reduced by k and vice-versa. Thus, there is a direct tradeoff between noise and distortion, and it is for this reason that the peak amplitudes are set equal for all stages in order to maximize dynamic range.

3.2. Fully-Differential Operational Amplifier Design

The filter performance depends largely on the characteristics of the op amps used in the filter. Therefore special attention has to be paid to the design of the op amps. In this section, topics involved in choosing the appropriate op amp for low distortion S.C applications will be discussed. Issues such as : using fully-differential or single-ended configurations, using conventional (two-stage, class A) or single-stage class A/B op

amps, and the detailed circuit design will be discussed.

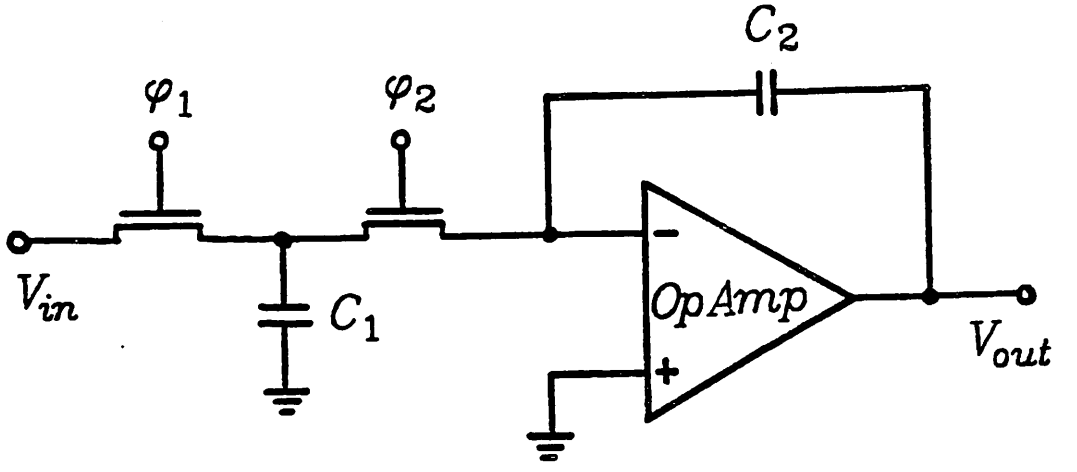
3.2.1. Single-ended vs. Fully Differential Op Amps

Figure 3.3 shows two S.C. integrators implemented in single-ended topology and fully-differential topology, respectively. Note that the input of the fully differential integrator is defined as V_{in}^{+}, V_{in}^{-}, and the output is defined as V_{out}^{+}, V_{out}^{-}. Also note that there are two different signal paths with opposite phases for the fully differential approach.

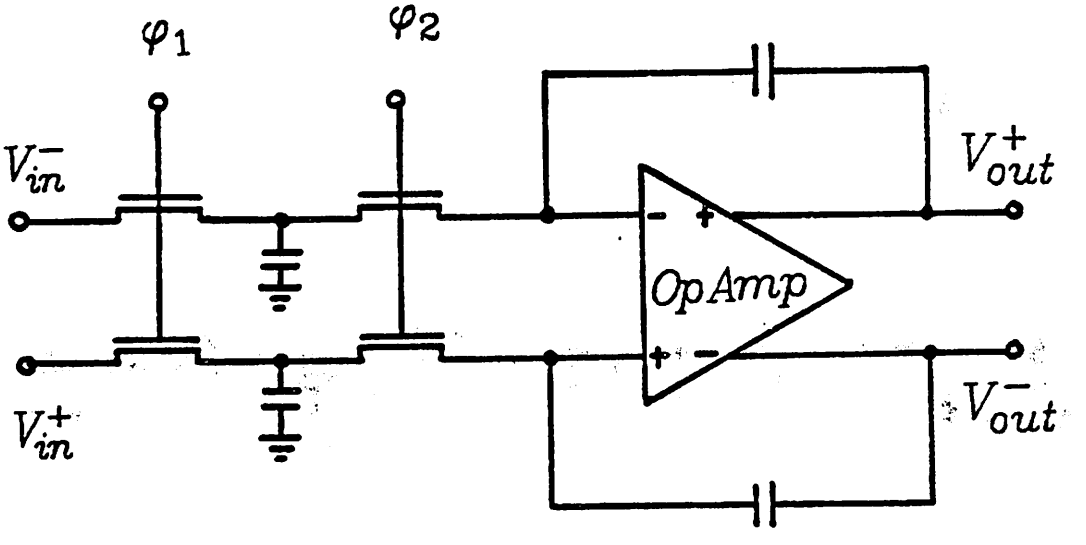
While the single-ended op amp topology has the merit of being simpler, has less device count (and therefore less silicon area), and has less power consumption, the the fully differential topology improves all the amplifier performance over the single-ended op amp. The advantages of using fully differential approach is briefly explained below[25].

The major advantages of adopting fully differential op amps is that both the power supply rejection ratio (PSRR) and common-mode rejection ratio are improved. This is because the output of fully differential circuits usually has very small common-mode gain due to its symmetrical structure, so that any common-mode signal which is simultaneously applied to the two input nodes will be rejected. Likewise, any external disturbance to the power supply (e.g. power supply noise, clock noise, etc.), are coupled into the two signal paths and are canceled at the output. This is especially important for S.C circuits, since they are often combined with a large amount of digital circuitry on the same chip. Since the switching of large a amount of current is very common among digital circuits, large noise spikes can be generated on the power supplies.

The fully differential topology has other definite advantages in addition to those describerd above :



(a)



(b)

Figure 3.3

(a) Single-ended S.C. integrator, and (b) differential S.C. integrator.

(1) fully differential op amps have more symmetrical transfer curves for positive and negative voltages, and therefore introduce much less even harmonic distortion at the integrator output;

(2) from equation (2.16), it is seen that the even harmonics caused by nonlinearity can be canceled to the first order;

(3) clock feedthrough and channel charge injection effects are much reduced, since similar noise signal are coupled into both signal paths during clock switching.

In summary, a fully-differential configuration has many advantages over the single-ended configuration for low distortion applications. The penalty is that larger area, and larger power have to be used. Also common-mode feedback circuits are always needed for fully differential amplifiers. These common-mode feedback circuits are usually difficult to design, and consume more power than the forward path amplifier itself, as will be discussed later.

3.2.2. Single Stage, Class A/B Op Amp Design

As described in Chapter 2, the use class A/B op amps has the potential of achieving more linear response and reducing the distortion introduced by the finite slew rate of the op amps. In other words, the large current and power consumption (and therefore the high slew rate) required by the low distortion S.C. circuits can be lessened.

A single stage configuration is preferred for S.C. applications due to the reasons discussed below. First, since the high impedance node, or the dominant pole is usually located at the output, the capacitance associated with the load is often large enough to guarantee stability. Therefore, no extra compensation capacitors are required. Second, due to the elimination of the compensation capacitors, the poor power supply rejection problem often encountered in multistage amplifier can be much improved. Finally, in

the multistage configurations. the input referred wideband noise is hard to eliminate since the latter stages have very wide bandwidth and the high frequency gain of the first stage is low. But for the single stage case. the input referred high frequency noise is eliminated by eliminating the latter stages. This is a major advantage for sampled-data systems. for which S.C. system is a good example. Only when the high frequency noise is low. do the inband aliases caused by sampling high frequency noise not impose a serious problem.

A simplified schematic of the op amp [26] is shown in Figure 3.4. Transistors M_1-M_4 form a cross-coupled input stage which split the input signal into two paths and provide the class A/B operation. M_5-M_8 and the two $5\,\mu$A current sources perform the level shifting and provide proper bias for the cross-coupled input devices. Transistors M_9-M_{20} form four current mirrors which duplicate the currents of the input devices with a 1:1 ratio.

It can be seen that. with careful design. the input devices $M_1 - M_4$ do not have to enter the triode region even when the largest possible signal is applied at the op amp input. This means that the output currents keep increasing as the input voltage increases. although the output current still is not a linear function of the input voltage. For a S.C. integrator. the nonlinearity is further reduced by the large loop gain around the integrator. and the slewing behavior often observed in class A amplifiers is much reduced. An exact analysis of this phenomenon is rather difficult. Computer simulation is used to verify this result. Output voltage steps for a S.C. integrator using the op amp described here is shown in Figure 3.5. where responses for two different step sizes are simulated. It can be seen that this integrator keeps almost constant rise time for different step size. and therefore behaves very much like a linear system with no slew-limiting observable. From SPICE [27] simulation. for the device sizes as listed in Table 3.1. the maximum current available for charging the output capacitors is approximately

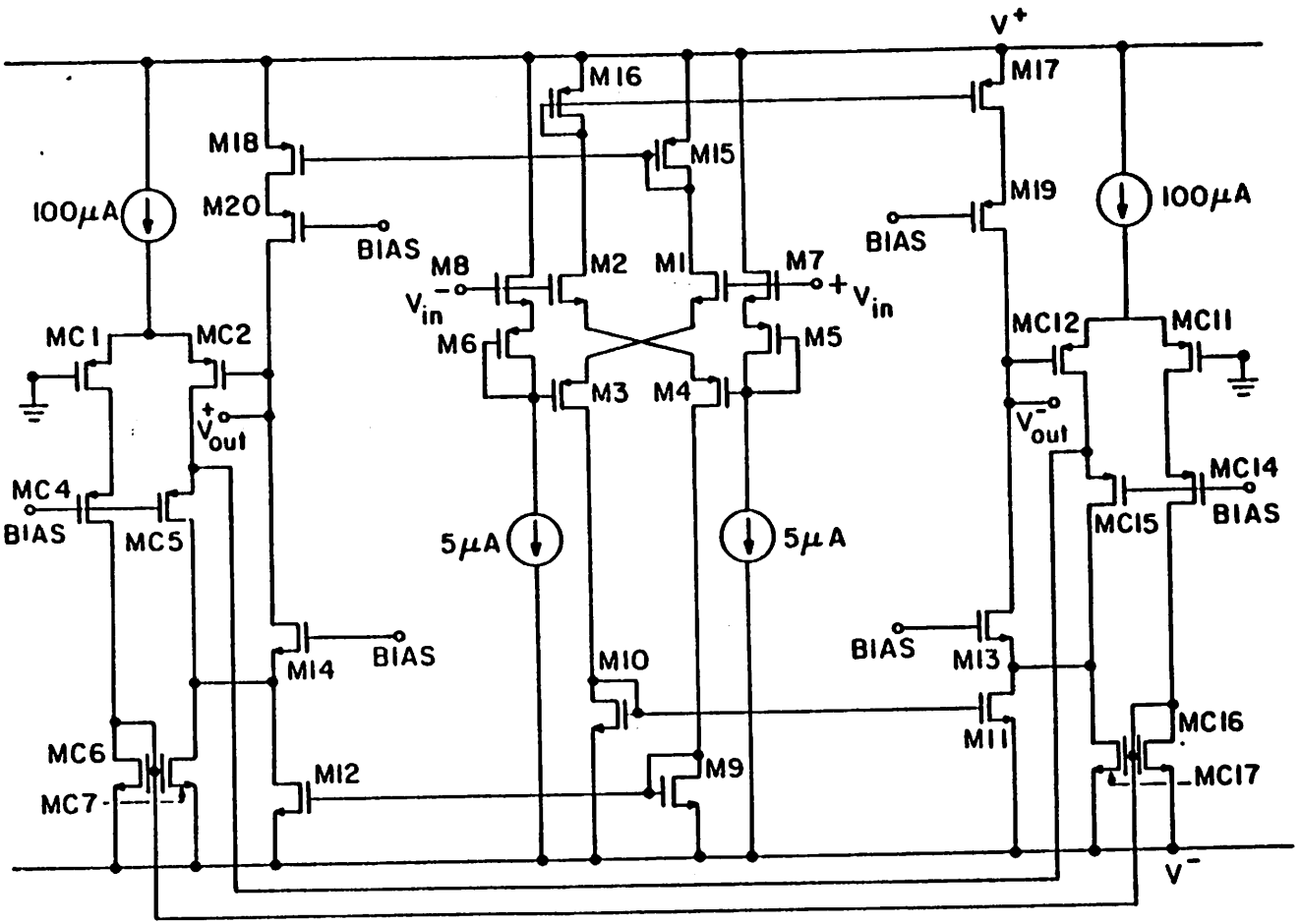


Figure 3.4 Simplified schematic of a class A/B op amp.

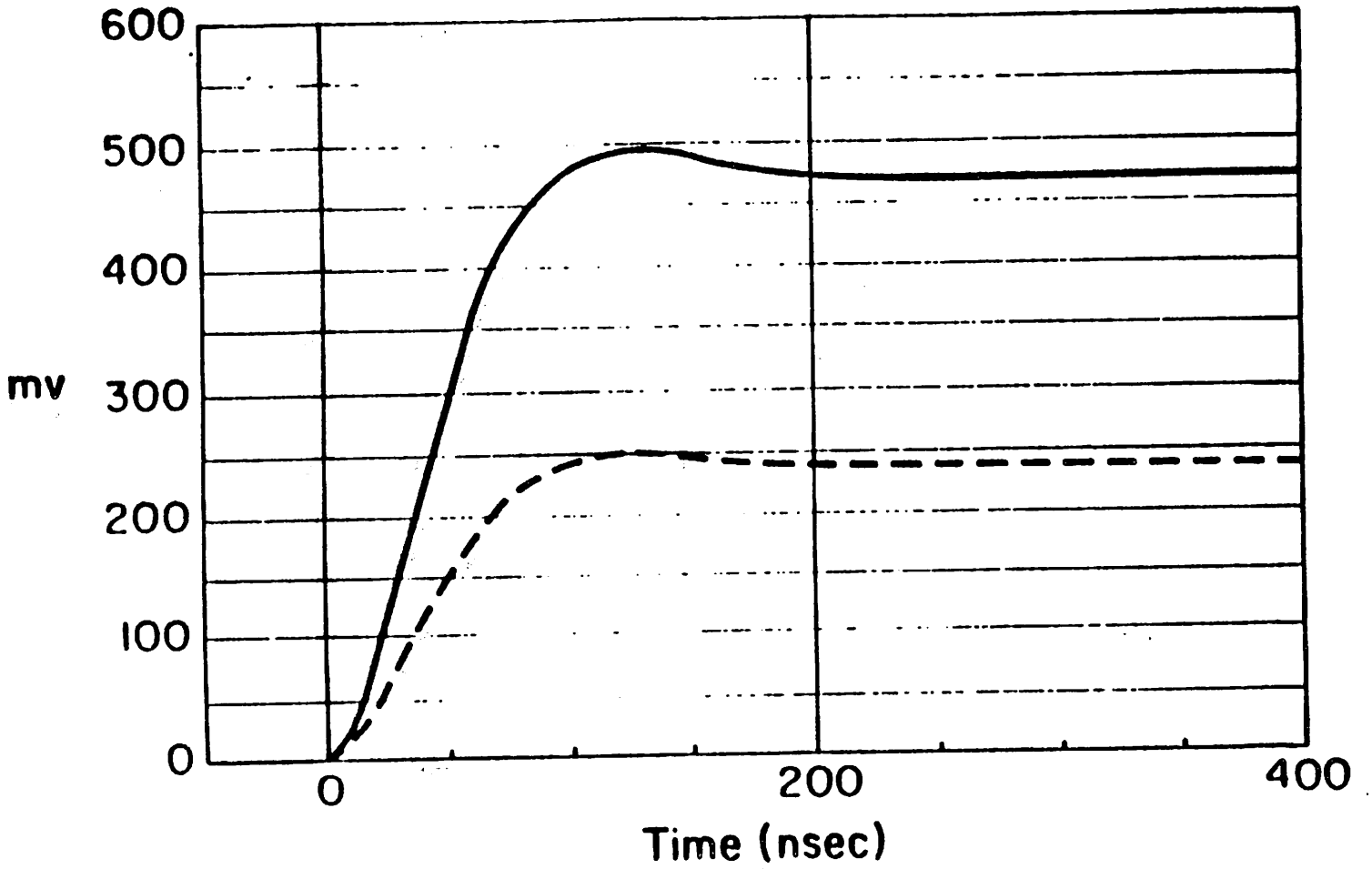


Figure 3.5 Output voltage steps of a S.C. integrator using a class A/B op apm.

$200\mu A$ for an integrator with capacitor ratio of 5 and input voltage of ± 2.5V. This is approximately 40 times more than the quiescent bias current.

Since a fully differential op amp design is used here, a common-mode feedback (CMFB) circuit must be applied to stablize the common-mode voltage of the op amp. In Figure 3.4, the transistors $MC_1 - MC_7$, $MC_{11} - MC_{17}$, and the two 100 μA current sources form the CMFB circuit, which fixes the op amp output common-mode voltage around 0V. If the common-mode voltage of the op amp output is centered around 0V, the transistors MC_5, MC_6, and MC_7 (MC_{15}, MC_{16}, MC_{17}) all have the same amount of current flowing through, and there should be no current passing through the connections between the drains of MC_5 and M_{12} (MC_{15} and M_{11}). On the other hand, if the output common-mode voltage is higher than zero, the currents flowing through the transistors MC_1, MC_4, MC_6, and MC_7 (MC_{11}, MC_{14}, MC_{16}, and MC_{17}) are larger than the currents flowing through MC_5 (MC_{15}). Extra currents will be taken from the sources of M_{13} and M_{14} by the common-mode circuit, and the common-mode voltage be pulled down. A similar argument can be used when the common-mode voltage is lower than 0V.

A continuous-time CMFB circuit is adopted for this op amp design in order to obtain better power-supply rejection at high frequency and to avoid the complication of introducing more switches required by the dynamic CMFB scheme [28], although increased power consumption and slightly limited output voltage swing are the disadvantages of this approach.

Figure 3.6 shows the complete schematic of the class A/B op amp being used in the test structure (see next chapter). Here transistors M_{14}, M_{15}, M_{19}, M_{20}, M_{21}, M_{22}, M_{25}, and M_{26} are added to provide dynamic biasing. The advantage of the dynamic biasing can be explained by using one cascode device as an example. During the stand-by mode, the sources of M_{16} is biased at relatively low voltage. But when the op amp has a large

Devices	W / L (micron/micron)
M1. M2. M3. M4	150 / 6
M5. M6	180 / 6
M7. M8	150 / 6
M9. M12. M13	26 / 6
M10. M11. M18	26 / 6
M14. M15	8 / 6
M16. M17	60 / 6
M19. M22. M24	50 / 6
M20. M21. M23	50 / 6
M25. M26	14 / 6
M27. M28	120 / 6
MC1. MC2. MC11. MC12	10 / 10
MC4. MC5. MC14. MC15	150 / 6
MC6. MC7. MC16. MC17	150 / 6

Table 3.1

Device sizes for the op amp shown in Figure 3.6.

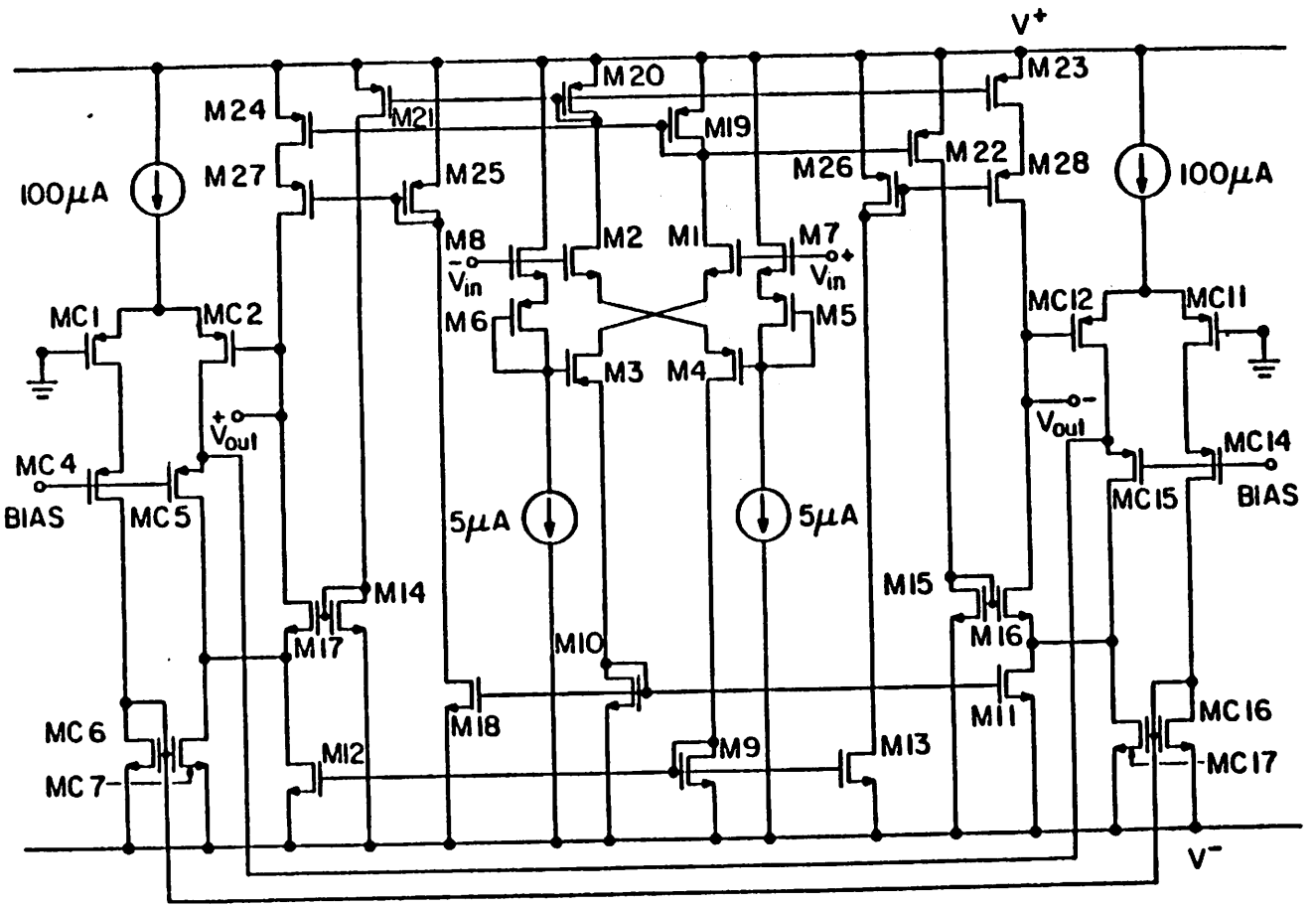


Figure 3.6 Complete schematic of a class A/B op amp.

positive input, the transistor M_{15} has a large current flowing through and its gate is pulled up. Then the source of M_{16} is also pulled up and the larger current can flow through M_{11} without making M_{11} going into the linear region. Similar argument can be used for other cascode devices. Thus the four current mirrors are always kept in saturation region and the op amp gain and voltage swing can be kept large simultaneously.

For device sizes as listed in Table 3.1, some simulated op amp characteristics are listed in Table 3.2.

3.3. Reduction of the Clock Feedthrough and Channel Charge Injection

Here a new error cancellation scheme is proposed. It is easy to implement since it is the combination of the original two-phase clock and a delayed version of it. Although its effects are difficult to analyze quantitatively, it can be shown by physical reasoning that, for a fully differential integrator (Figure 3.7 (a)), by changing the conventional two-phase clock (Figure 3.7 (b)) to a simple four-phase clock (Figure 3.7 (c)), this error can be much reduced (for a similar argument, readers are referred to [29]).

The switching sequence and the error mechanism during different time periods for the four-phase clock is qualitatively explained below. A switched capacitor integrator with the relevant parasitic capacitors is shown in Figure 3.7 (a) for which a full clock cycle is divided into five time intervals (Figure 3.7 (c)) :

(1) Δt_1 : $\phi_{1a} = \phi_{1b} = high$. $\phi_{2a} = \phi_{2b} = low$. M_1, M_2 (M_1' , M_2') are turned on. The capacitors C and C' are charged by the amplifier of the previous stage;

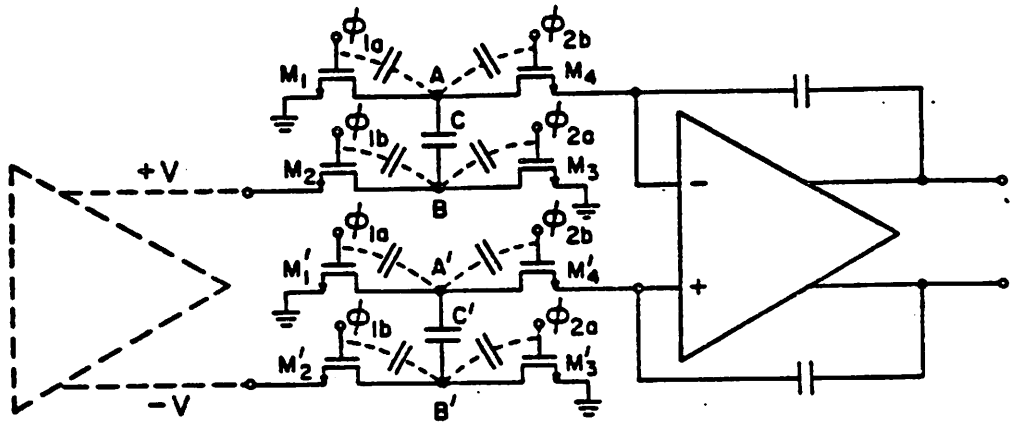
(2) Δt_2 : ϕ_{1a} : $high \rightarrow low$. The equivalent circuit before M_1, M_1' are turned off is shown in Figure 3.8 (a). The falling edge of ϕ_{1a} works as if it generates an equivalent current source which charges the sampling capacitor through the R-C

SIMULATED OP-AMP PERFORMANCE

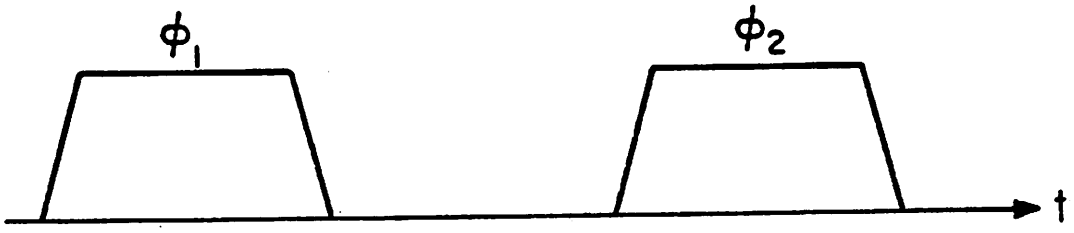
Supply voltage	±5	V
DC gain	83	dB
Unity-gain bandwidth	6	MHz
Phase margin	45	degree
Settling time (1V step, 0.01%)	600	ns
CMRR with ± 3 V output	>80	dB
PSRR with ± 3 V output (<50kHz)	>80	dB
Gain Nonlinearity (= 3V output)	2	%
Power dissipation	1.8	mW

Table 3.2

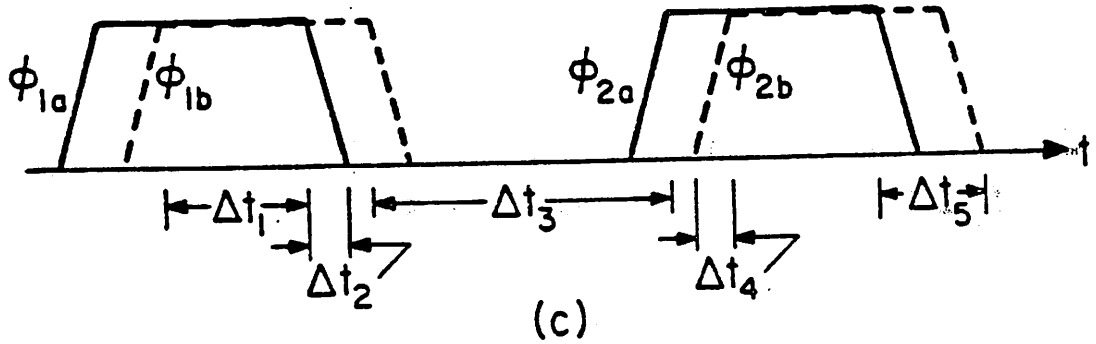
Simulated performance of the op amp shown in Figure 3.6.



(a)



(b)



(c)

Figure 3.7

(a) Clock feedthrough for one differential stage, (b) two-phase clock, and (c) four-phase clock.

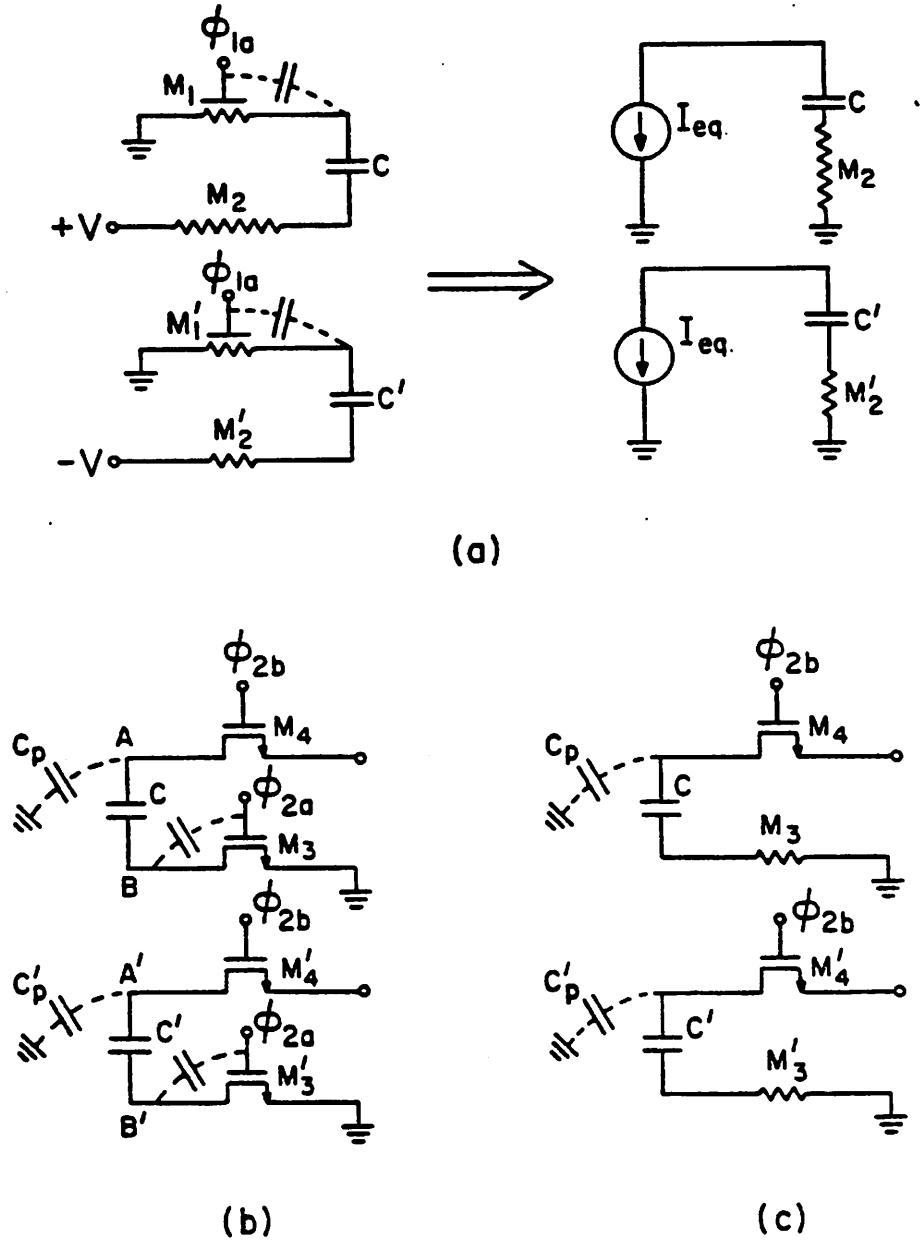


Figure 3.8

(a) Equivalent circuit for step (2), (b) Equivalent circuit for step (3), and (c) Equivalent circuit for step (4).

combination formed by C and M_2 (C' and M_2'). Note that the channel resistance of M_2 and M_2' are different because of the different channel voltages. The capacitors C and C' are thus charged to different voltages at the end of the clock transition and an error is generated;

(3) Δt_3: ϕ_{1b} : *high* $\rightarrow$ *low* . ϕ_{2a} : *low* $\rightarrow$ *high* . The equivalent circuit for this period is shown in Figure 3.8 (b), in which all the parasitic capacitances associated with node A (A') are lumped into a single capacitor C_p (C_p'). In this case, since the charges in the top plate of C and C_p (C' and C_p') are conserved, no error can be induced by the transition of ϕ_{1b} and ϕ_{2a} . In other words, whenever an error charge is induced on C by the transition of ϕ_{1b} or ϕ_{2a} , an equal and opposite charge is induced on C_p (C_p'). Thus when the transistors M_3 . M_4 (M_3' . M_4') are turned on and the nodes A . B . A' .and B' go back to zero voltage, all the error charges will recombine and have no effect on the differential output;

(4) Δt_4: ϕ_{2b} : *low* $\rightarrow$ *high* . The equivalent circuit is shown in Figure 3.8 (c). As described in (3), this transition does not induce error at the differential output;

(5) Δt_5: ϕ_{2a} : *high* $\rightarrow$ *low* . ϕ_{2b} : *high* $\rightarrow$ *low* . Since all the nodes adjacent to M_3 . M_4 . M_3' . M_4' have the same voltage and impedance now, a perfectly balanced condition is created and any error generated in the top half of the circuit is offset by the same error in the bottom half and no differential error can be transmitted.

In the above discussion, the only place where a differential error is introduced is in (2) where the on-resistances of M_2 and M_2' are not equal. This error can be minimized by using complementary switches (or transmission gates, as shown in Figure 3.9) instead of the single-channel switches M_2 . M_2' , since complementary switches have much smaller resistance variation as the source/drain voltage changes. As shown in

Figure 3.9. for transistors from a typical CMOS process and with source/drain voltages at +3V and -3V, the ratio of their on-resistances can be improved by a factor of three by using the complementary switches. In the experimental filter to be described in the next chapter, complementary switches are used for all the switches correspond to the switches M_2 and M_2' in Figure 3.7 (a), while single channel NMOS switches are used elsewhere.

Further thought reveals the reasons that the four-phase clock is better than the conventional two-phase clock. For example, since in the latter case if M_1, M_2, M_1', M_2' are all turned off by the same clock transition, M_2 can be turned off long before M_2' is turned off because M_2 has a higher source voltage than M_2'. Thus an unbalanced situation is created and a large error can be introduced.

In the above discussion, we considered the case where the input voltages are connected to the noninverting inputs of the integrator. The same argument can be used when the inputs are fed into the inverting inputs of the integrator. By doing so the conclusion can be reached that the transistors M_3 and M_3' also have to be replaced by transmission gates for the same reason as we mentioned in (2).

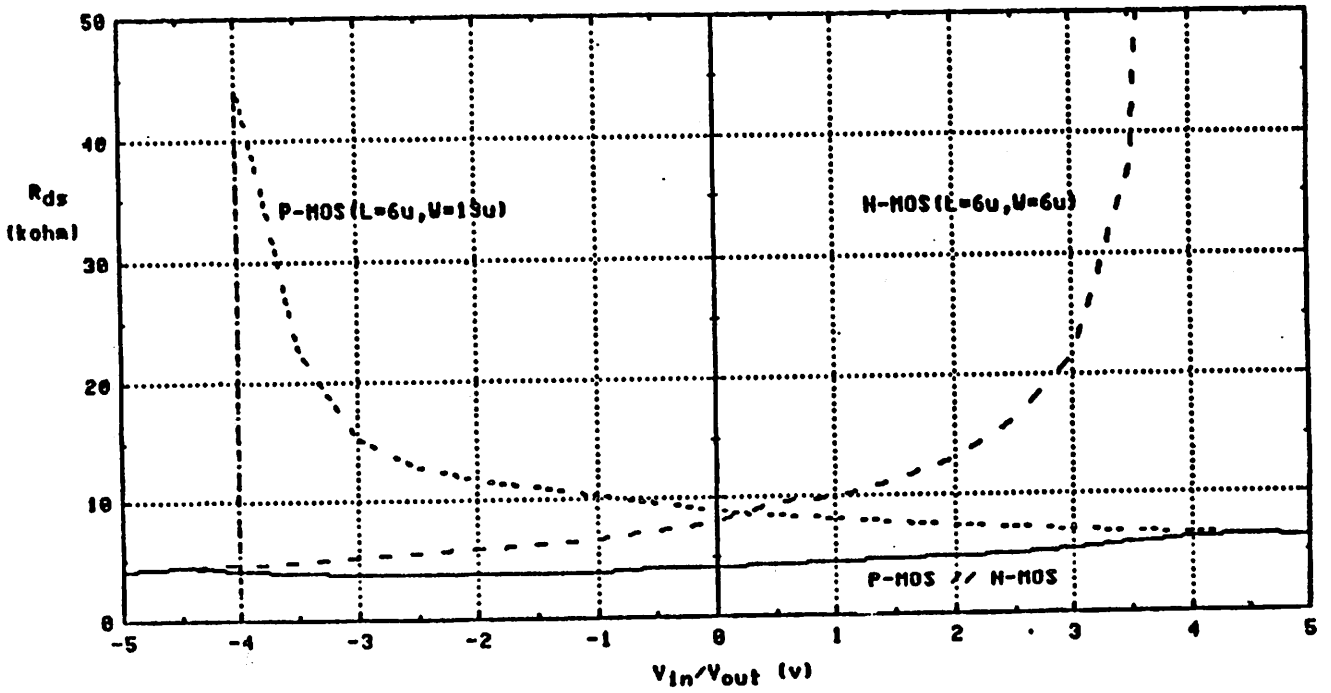


Figure 3.9 Output resistance across the source/drain nodes for NMOS, PMOS, and transmission gates.

CHAPTER 4

EXPERIMENTAL RESULTS

To verify the validity of the theoretical results developed in Chapter 2, and to demonstrate the relative merits of the design techniques described in Chapter 3, test circuits were built and tested. These test circuits include a 6^{th} order S.C. low-pass filer, a S.C. integrator, test op amps, and test capacitors. The 6^{th} order low-pass filter provides the characteristics of an audio band filter (20 kHz) at a sampling frequency of 500kHz. The S.C. integrator is a stand-alone integrator which includes a bottom plate S.C. integrator and the provisions for DC voltage feedback (as described below) to maintain the DC stability of the integrator. The op amps are built on-chip so that the properties and parameters of the op amps (e.g. gain, nonlinearity, etc.) can be measured independently. For similar reasons, separate MOS capacitors are included on the chips so the voltage coefficients can be measured. Output source followers are also included in the filter and integrator circuits to provide capability for driving off-chip loads.

All the test circuits are implemented with 5 μm CMOS technology. The test chips were mainly fabricated through MOS Implementation Service (MOSIS). [1] which provides 5 μ, p-well, CMOS processes with double-poly capacitors.

In this chapter, the design methodology and the measured performance of the integrator and filter chips will be discussed in detail.

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[1]MOSIS is a division under the University of Southern California sponsored by Defense Advance Research Projects Agency (DARPA).

4.1. A 6th Order Elliptic Low-pass Filter

The implementation and test of the 6^{th} order elliptic filter will be discussed in the following two sub-sections.

4.1.1. Filter Design and Implementation

Figure 4.1 shows the R-L-C prototype of the 6^{th} order low-pass filter and the associated component values [30]. These component values are chosen such that the stop band frequency is normalized to 1Hz. This filter uses standard active ladder structure since it is less sensitive to component variations [16]. It also uses parasitic-insensitive bottom-plate S.C. integrators to reduce the effect of parasitic capacitance. This specific filter response was chosen because it provides the desired characteristics of a low-pass filter that can be used in a digital audio system [6]. (one example of the desired low-pass filter for digital audio systems has the specifications as listed in Table 4.1).

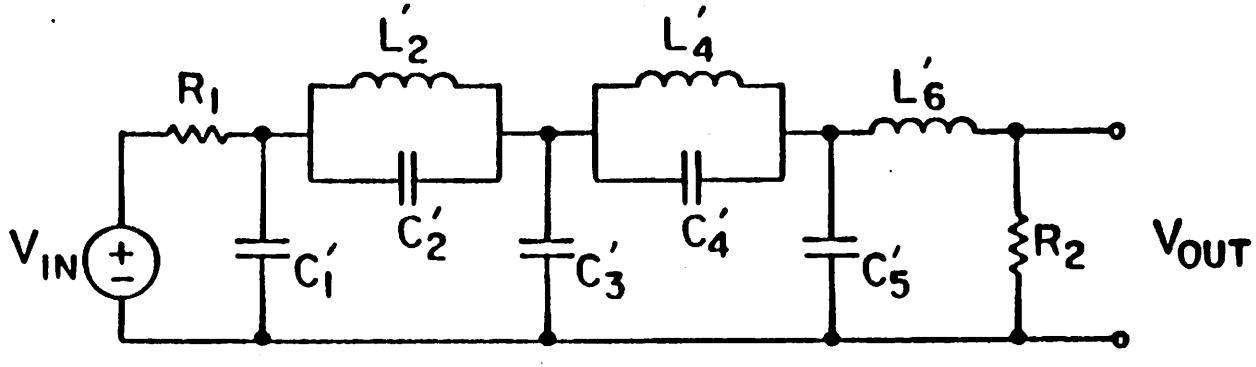
With the component values shown in Figure 4.1, the cutoff frequency is normalized to 1. Since a 20kHz bandwidth is desired, the method of frequency normalization [31] has to be used. After the frequency normalization, the prototype filter is transformed into the circuit shown in Figure 4.2, with component values which are different from the original prototype filter.

After the frequency normalization, the Thevenin equivalent circuit of the passive prototype is derived to eliminate the capacitor loop, as shown in Figure 4.3. The associated loop and node equations are listed below.

$$V_0 = V_{in} - V_1. \tag{4.1a}$$

$$I_0 = \frac{V_0}{R_1}. \tag{4.1b}$$

$$I_1 = I_0 - I_2. \tag{4.1c}$$



$R_1 = 1\Omega$ $C_3' = 1.6450F$ $L_6' = 0.8714H$

$C_1' = 0.9967F$ $L_4' = 1.0910H$ $R_2' = 0.7391\Omega$

$L_2' = 1.1810H$ $C_4' = 0.3832F$

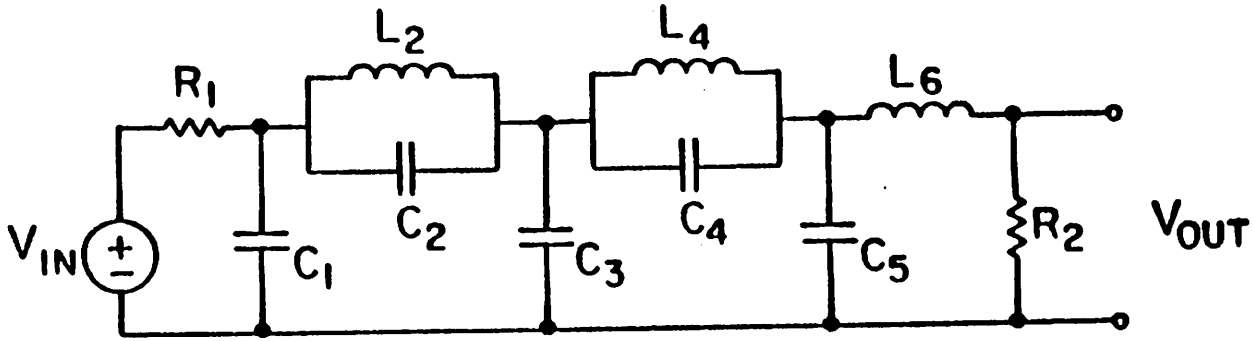
$C_2' = 0.2010F$ $C_5' = 1.6110F$

Figure 4.1 **Prototype low-pass filter with component values.**

AUDIO PERFORMANCE REQUIREMENTS	
PARAMETERS	**VALUE**
FREQUENCY RESPONSE	20Hz - 20kHz
QUANTIZATION, PER CHANNEL	16-bit linear
SIGNAL-TO-NOISE RATIO	> 90 dB
DYNAMIC RANGE	> 90 dB
CHANNEL SEPARATION	> 90dB
HARMONIC DISTORTION	< 0.05 %

Table 4.1

Typical Audio Performance Requirements



$R_1 = 1\Omega$ $C_3 = 13.090\mu F$ $L_6 = 6.9344\mu H$

$C_1 = 7.9315\mu F$ $L_4 = 8.6819\mu H$ $R_2 = 0.7391\Omega$

$L_2 = 9.3981\mu H$ $C_4 = 3.0494\mu F$

$C_2 = 1.5995\mu F$ $C_5 = 12.820\mu F$

Figure 4.2 Prototype low-pass filter with component values after frequency normalization.

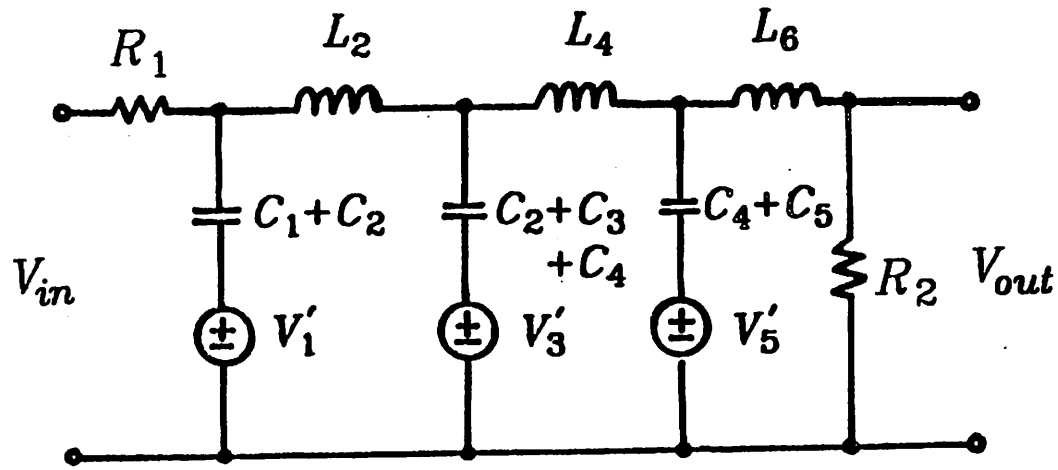


Figure 4.3 Thevenin equivalence of the circuit in Figure 4.2.

$$V_1 = \left(\frac{1}{s(C_1+C_2)}\right) I_1 + \left(\frac{C_2}{C_1+C_2}\right) V_5. \tag{4.1d}$$

$$V_2 = V_1 - V_3. \tag{4.1e}$$

$$I_2 = \left(\frac{1}{s L_2}\right) V_2. \tag{4.1f}$$

$$I_3 = I_2 - I_4. \tag{4.1g}$$

$$V_3 = \left(\frac{1}{s(C_2+C_3+C_4)}\right)(I_2-I_4) + \left(\frac{C_2}{C_2+C_3+C_4}\right) V_1 + \left(\frac{C_4}{C_2+C_3+C_4}\right) V_5. \tag{4.1h}$$

$$I_4 = \left(\frac{1}{s L_4}\right) V_4. \tag{4.1i}$$

$$V_4 = V_3 - V_5. \tag{4.1j}$$

$$V_5 = \left(\frac{1}{s(C_4+C_5)}\right)(I_4-I_6) + \left(\frac{C_4}{C_4+C_5}\right) V_3. \tag{4.1k}$$

$$I_5 = I_4 - I_6. \tag{4.1l}$$

$$I_6 = \left(\frac{1}{s L_6}\right) V_6. \tag{4.1m}$$

$$V_6 = V_5 - V_{out}. \tag{4.1n}$$

and

$$I_6 = \frac{V_{out}}{R_2}. \tag{4.1o}$$

At this point, a signal flow graph can be derived from Figure 4.3, as shown in Figure 4.4. If the S.C. filter is implemented according to this signal flow graph, the distribution of the internal node voltage swings would be as shown in Figure 4.5 (which is duplicated from Figure 3.1 for convenience). Note that the internal nodes do not peak at the same level. The method of node voltage scaling can then be used such that all nodes limit at the same level. Node voltage scaling can be effected by consideringthe circuit in Figure 4.4 to determine the relative voltage amplitude of each node. Then the

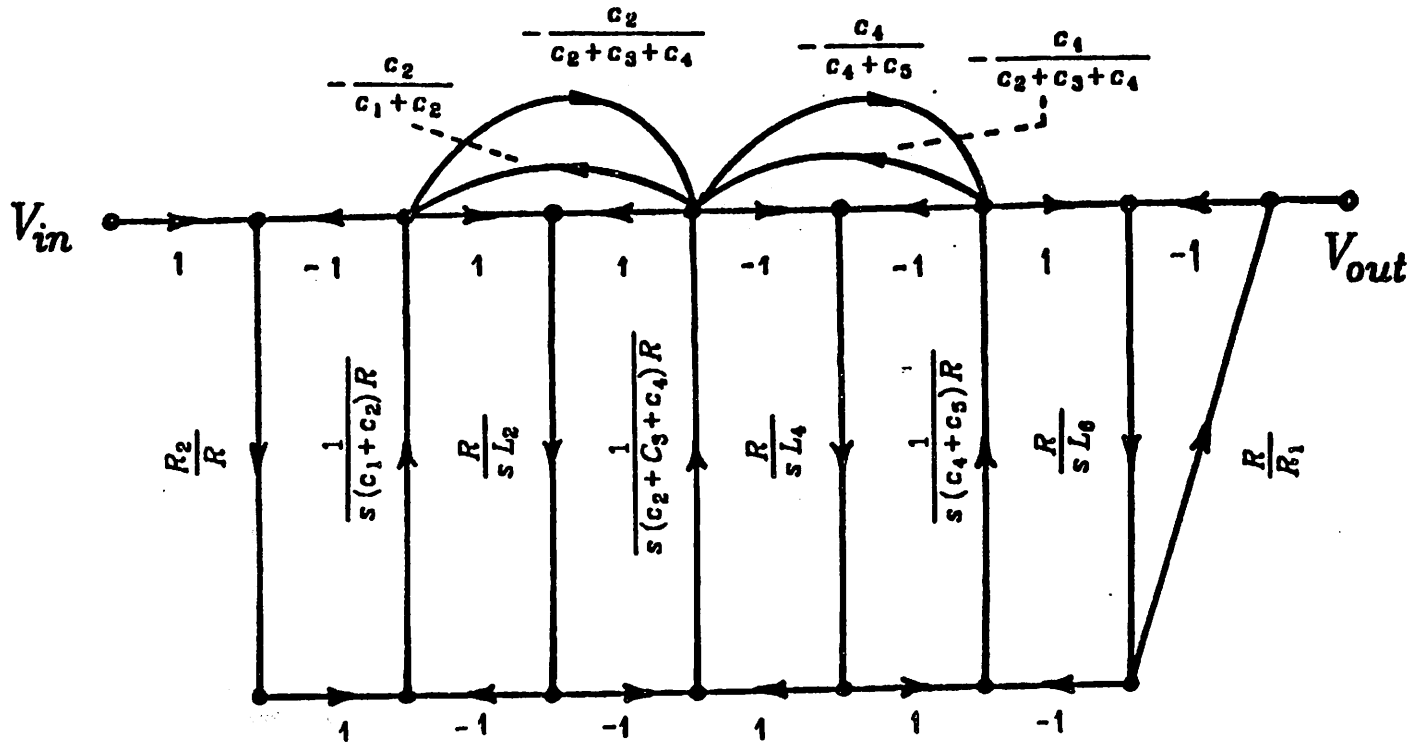


Figure 4.4 Signal flow graph of the low-pass filter.

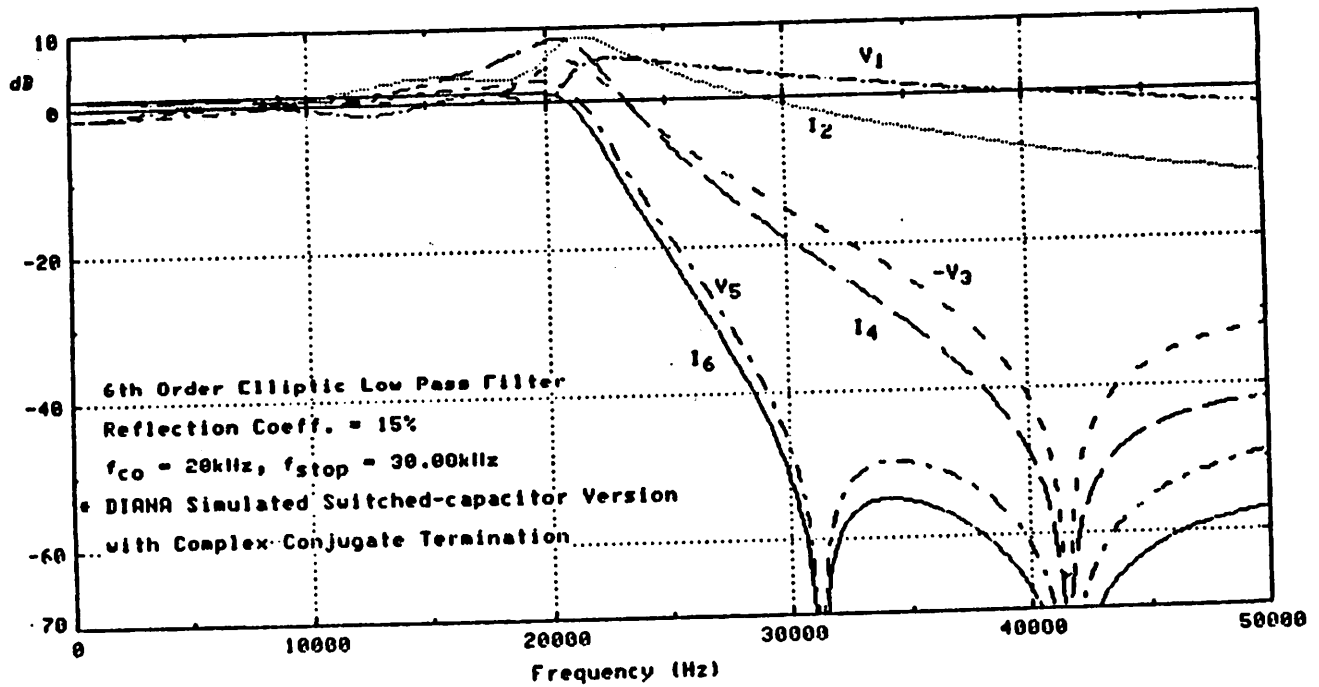


Figure 4.5 Distribution of the filter intenal node voltage.

technique described in Section 3.1 can be applied loop by loop to normalize the node voltages. Note that once a coefficient is multiplied to one branch of a certain loop, the inverse of this coefficient has to be multiplied to the opposite branch such that the total loop gain is kept constant. The signal flow graph after voltage scaling is shown in Figure 4.6. As noted in Section 3.1, an extra pair of switched capacitors has to be added to each integrator to accommodate the different gains associated with the two adjacent loops.

The S.C. implementation of the circuit in Figure 4.6 is shown in Figure 4.7, and the capacitor ratio for this circuit is shown in Table 4.2. The simulated frequency response is shown in Figure 4.8. Note that for this circuit all the internal nodes peak at the same level.

Other than the node voltage scaling described above, the test filter also incorporates the fully differential, class A/B op amp design, and provisions for changing from the conventional two-phase clock to the four-phase clock as proposed in Chapter 3.

4.1.2. Measurements and Test Circuits

A photograph of the filter test chip is shown in Figure 4.9. Using 6 μm gate length, the active area of the filter is approximately 105 x 49 mils.

The frequency response of this filter is measured by using the circuit shown in Figure 4.10. In this configuration, the sweep signal is first converted into a differential signal by the single-ended to differential converter before passing through the filter. The filter output is then converted into a single-ended signal and sent to the spectrum analyzer. In order to drive the off-chip load, source followers are included on the filter chip. These source followers are located in independent p-wells and have sources connected to the wells, so that the distortion introduced by the body effect can be elim-

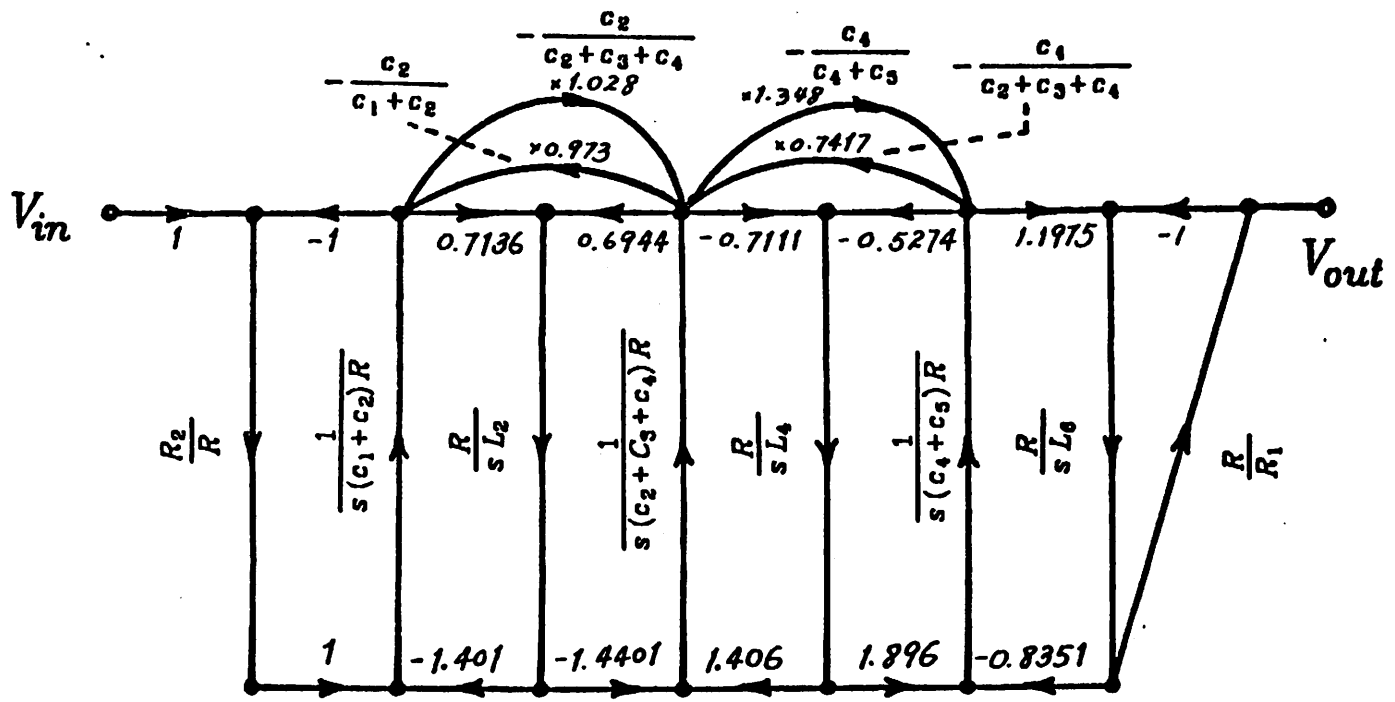


Figure 4.6 Signal flow graph after voltage scaling.

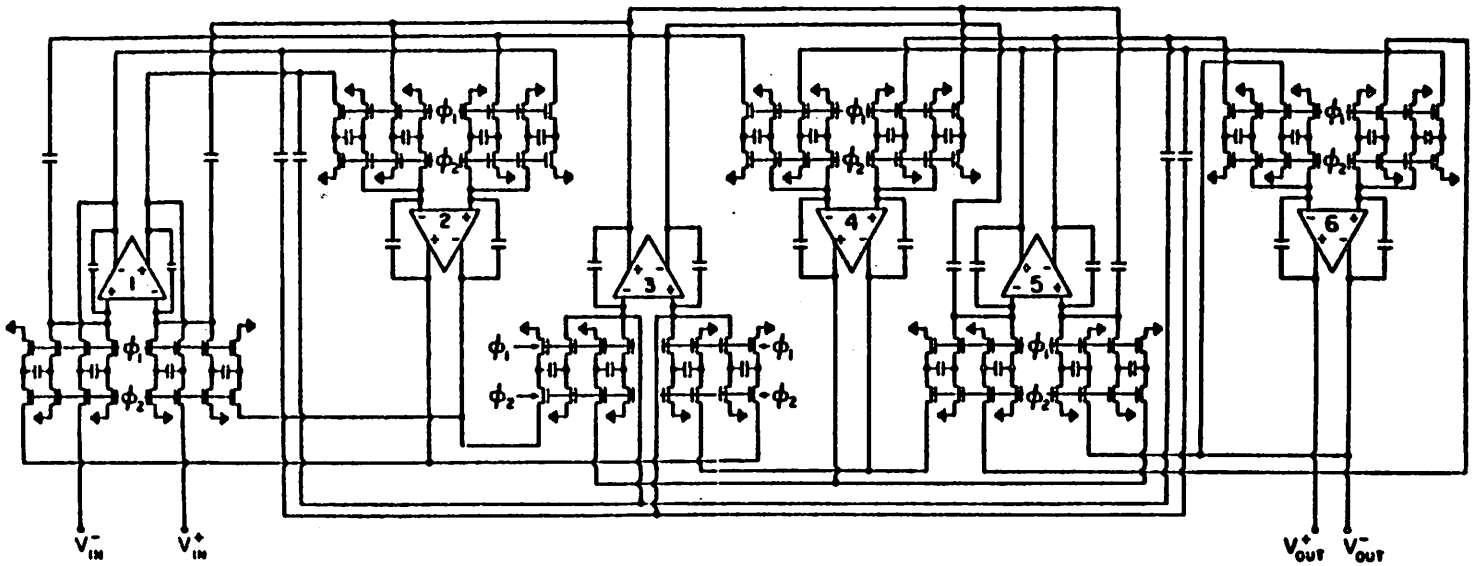


Figure 4.7 S.C. implementation of circuit in Figure 4.6.

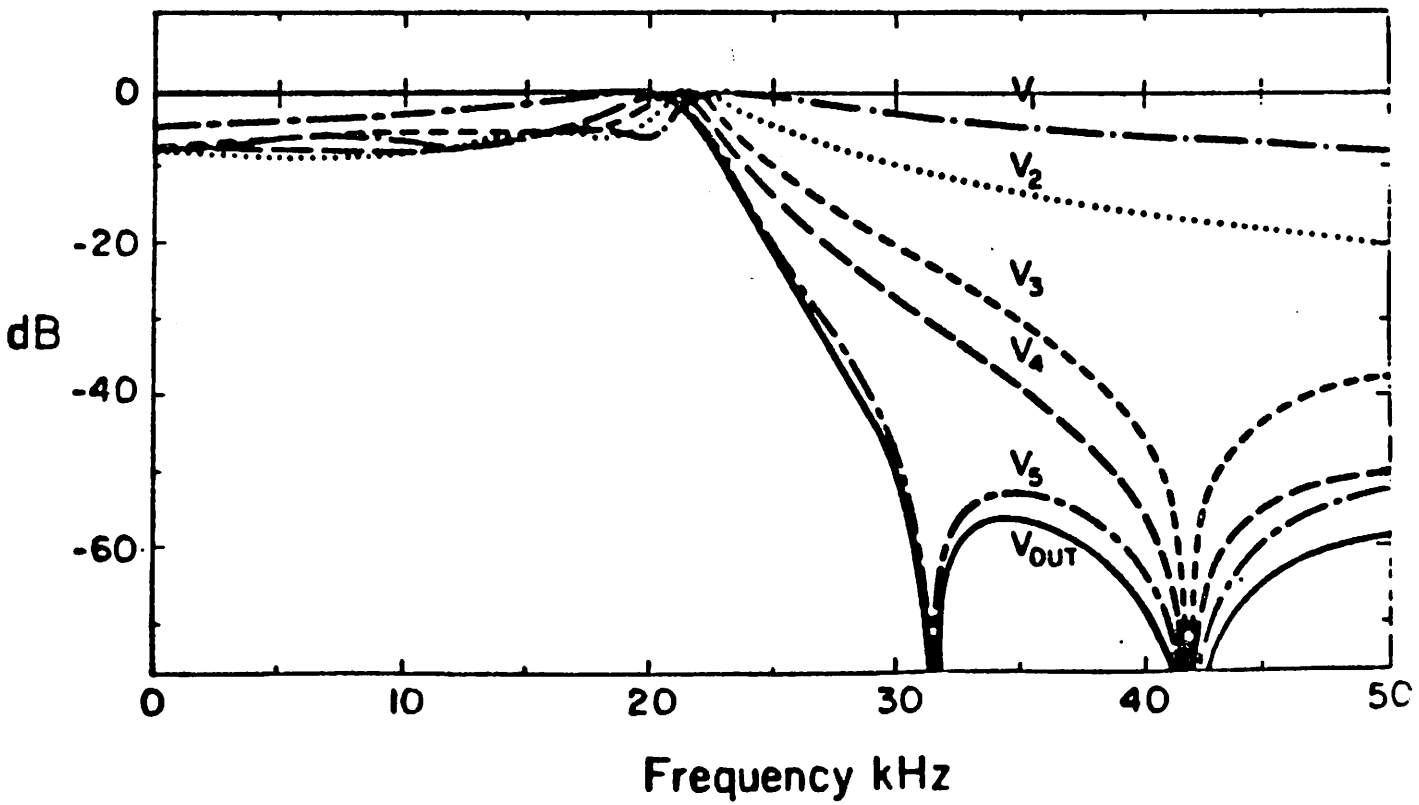


Figure 4.8 Distribution of the filter intenal node voltage after voltage scaling.

$$\frac{C_{I1}}{C_{u1}} = 4.7655 . \qquad \frac{C_{I5}}{C_{u5}} = 4.1849 .$$

$$\frac{C_{I1}}{C_{u1}} = 3.4008 . \qquad \frac{C_{I5}}{C_{u5}} = 9.5022 .$$

$$\frac{C_{I2}}{C_{u2}} = 6.5847 . \qquad \frac{C_{I6}}{C_{u6}} = 2.8952 .$$

$$\frac{C_{I2}}{C_{u2}} = 6.7671 . \qquad \frac{C_{I6}}{C_{u6}} = 4.6911 .$$

$$\frac{C_{I3}}{C_{u3}} = 6.1589 . \qquad \frac{C_{13}}{C_{u1}} = 0.5845 .$$

$$\frac{C_{I3}}{C_{u3}} = 6.3073 . \qquad \frac{C_{31}}{C_{u1}} = 0.7782 .$$

$$\frac{C_{I4}}{C_{u4}} = 6.1043 . \qquad \frac{C_{35}}{C_{u1}} = 2.0514 .$$

$$\frac{C_{I4}}{C_{u4}} = 8.2304 . \qquad \frac{C_{53}}{C_{u1}} = 0.8042 .$$

Table 4.2 Capacitor Ratio for the Voltage-Scaled Filter.

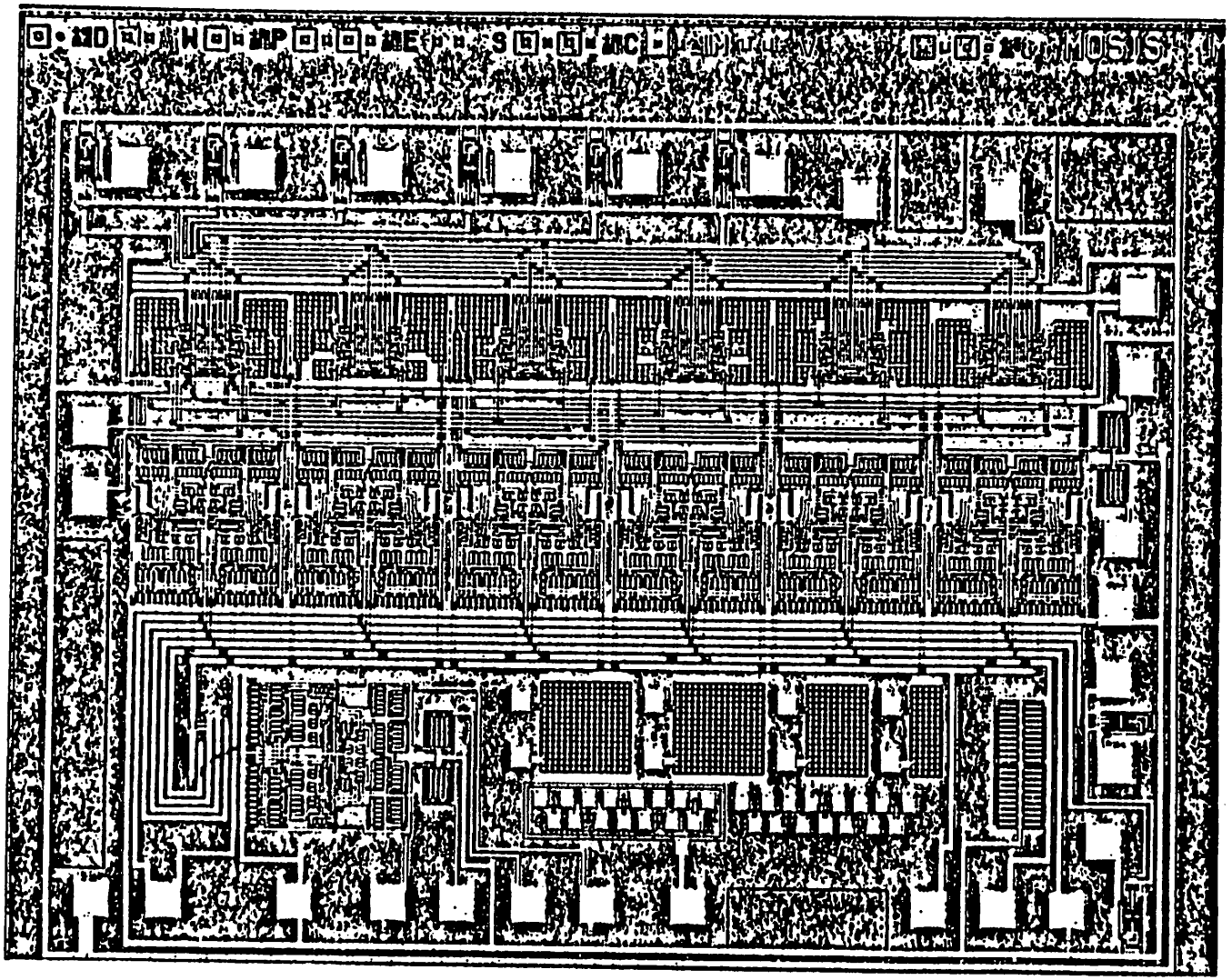


Figure 4.9 Photograph of filter test chip.

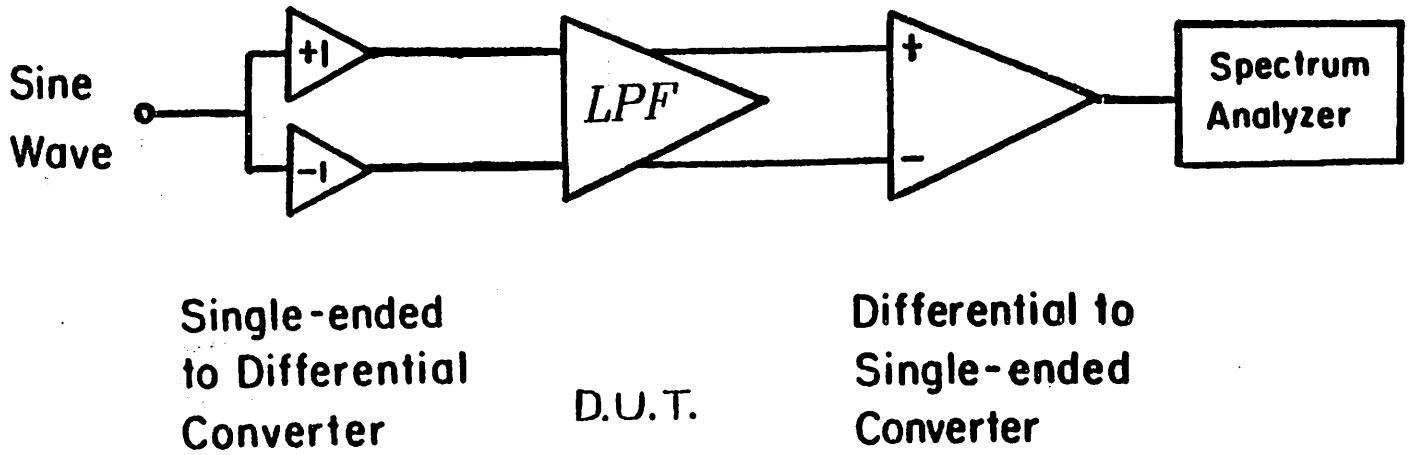


Figure 4.10 Test circuit of the filter test chip.

inated [32]. The circuits performing the single-ended to differential and differential to single-ended conversions are shown in Figure 4.11 and 4.12, respectively.

The coarse and detailed filter responses for a clock frequency of 500kHz are shown in Figure 4.13. These responses generally agree with the simulated results from the S.C. simulation program SWAP[33].

The power-supply rejection as a function of frequency for two different frequency ranges are shown in Figure 4.14. As can be seen the positive supply rejection is above 40dB and the negative supply rejection is above 30dB, for the whole frequency range.

Some of the measured filter characteristics for this sampling frequency are listed in Table 4.3. Note that the CMFB circuits consumes approximately 80% of the total power required by the op amp. Since it will be seen that the clock feedthrough and charge injection have limited effects (see below) on the filter distortion, dynamic CMFB circuits could be used to reduce the power consumption drastically [26].

By replacing the sweeping signal source in Figure 4.10 by a low-distortion sinewave generator, the distortion characteristics of this filter can be measured. Photographs of the output spectrum for three different signal frequencies : 1kHz, 10kHz, and 15kHz are shown in Figure 4.15, where the signal amplitude is 10Vp-p. Intermodulation distortion is also measured by applying two pairs of frequencies : 9 and 10kHz, 15 and 16kHz to the filter, where each frequency component has an amplitude of 2Vp-p. Photographs for these spectra are shown in Figure 4.16. Total harmonic distortion (THD) for signal frequencies across the whole passband at different signal amplitudes are plotted in Figure 4.17 for two different bandwidths : 4kHz and 20kHz. It can be seen from Figure 4.17 that in general THD increases at higher signal frequencies. This is because (1) as the signal frequency is closer to the band edge, the voltages swing higher at the op amp output nodes such that the nonlinear op amp gain introduces more distortion, and (2) the op amps need a longer time to settle for each step as the signal

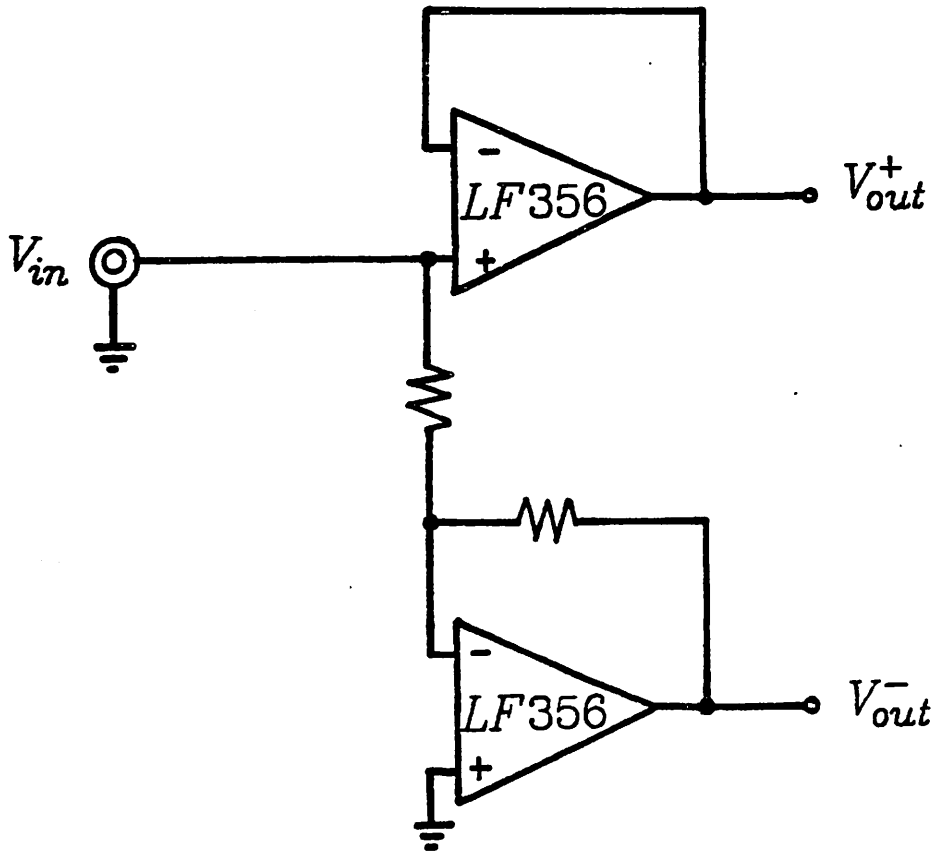


Figure 4.11

Single-ended to differential converter.

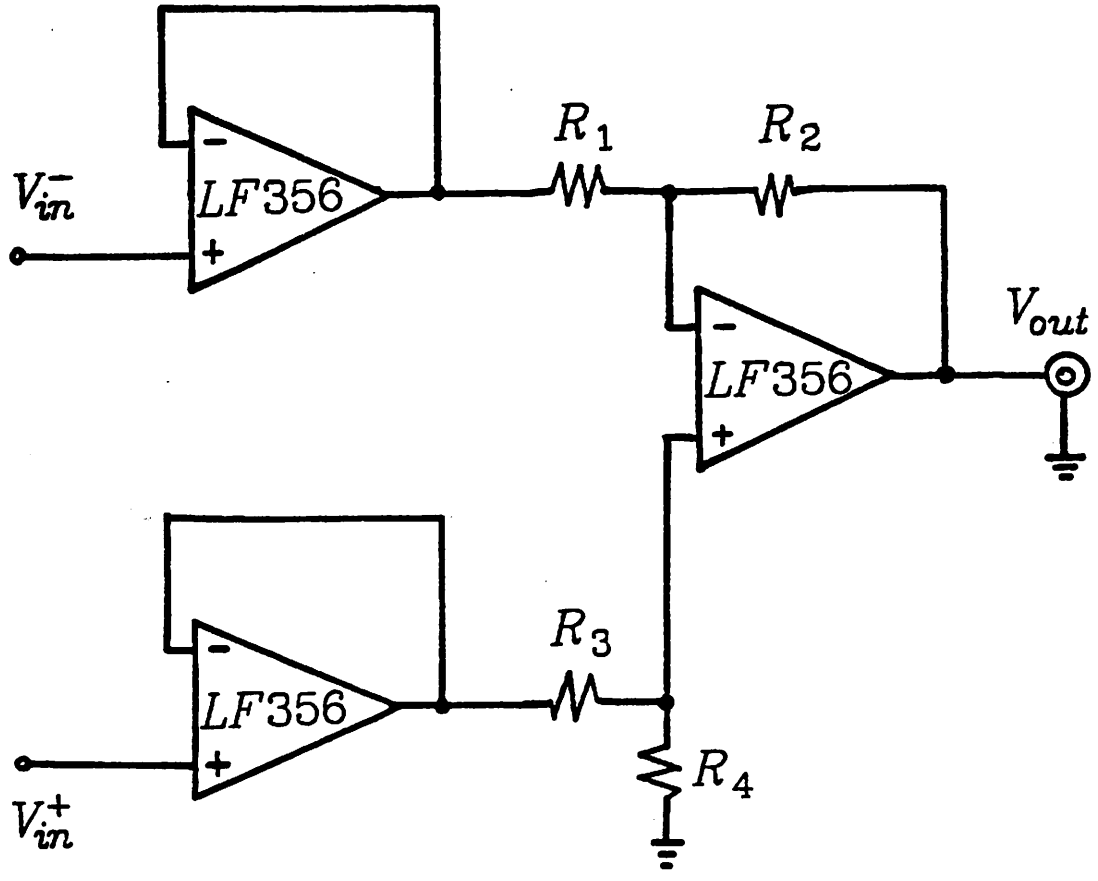


Figure 4.12

Differential to single-ended converter.

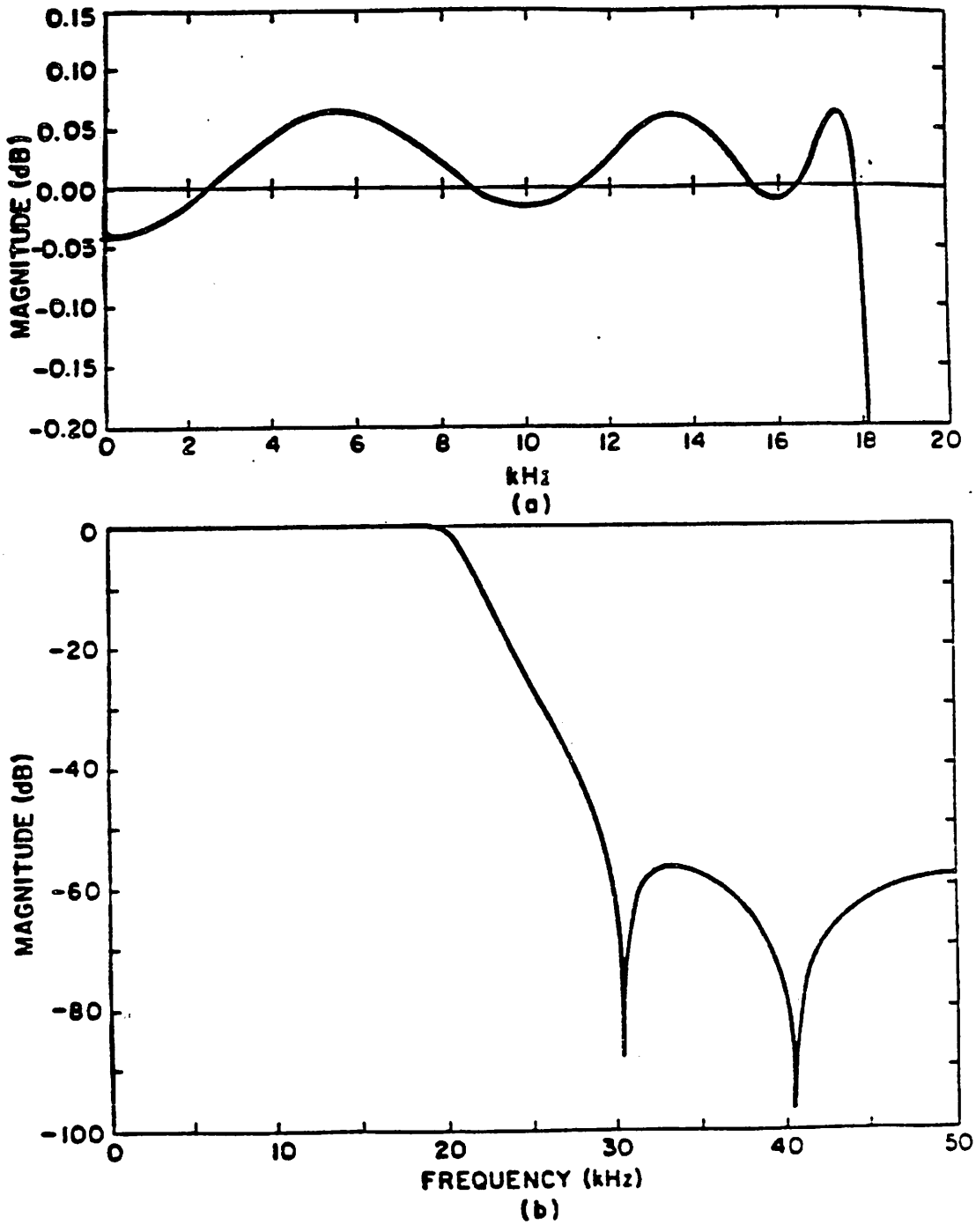


Figure 4.13

(a) Measured detail passband frequency response of the 20kHz filter, and (b) coarse frequency response of the filter.

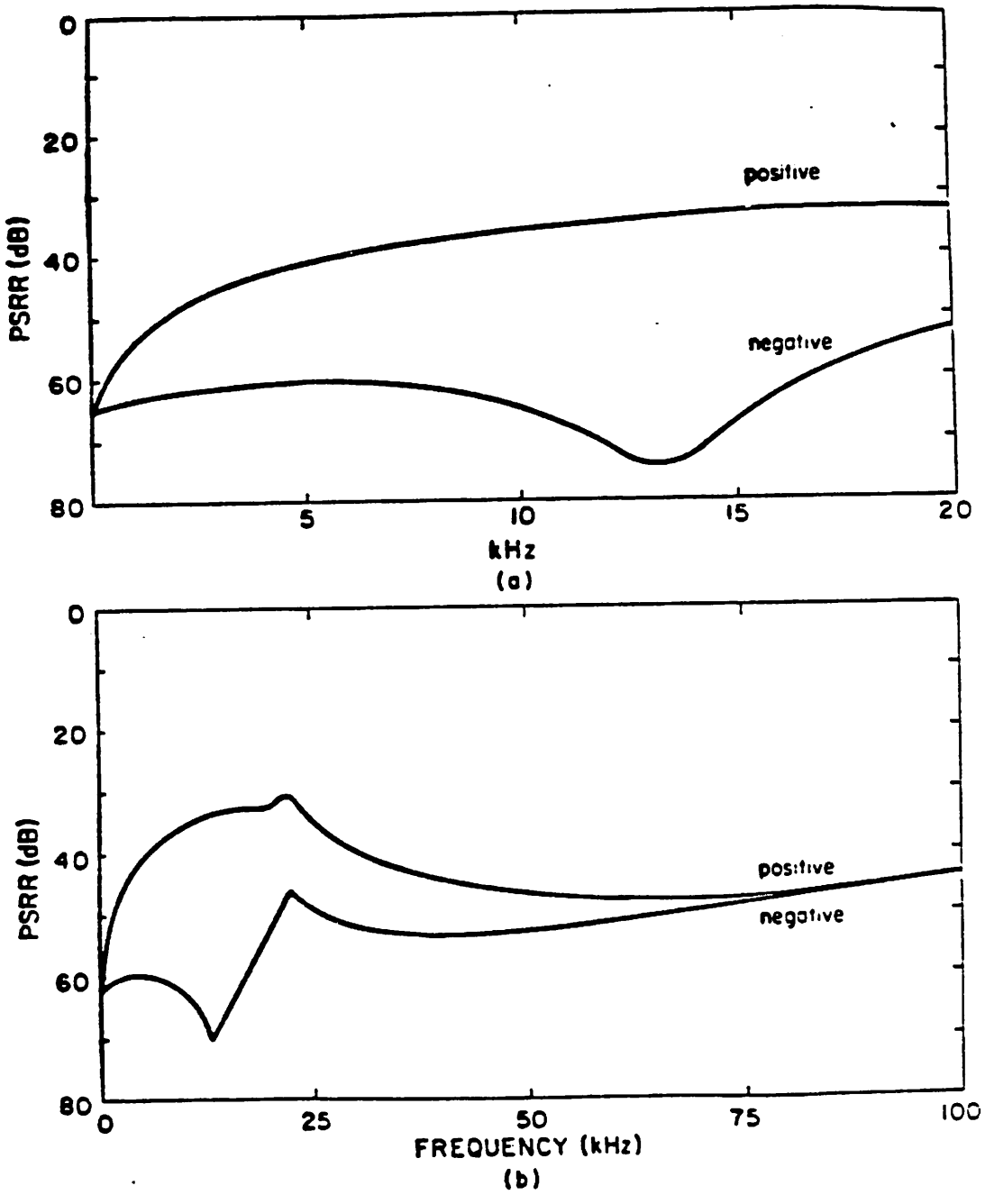


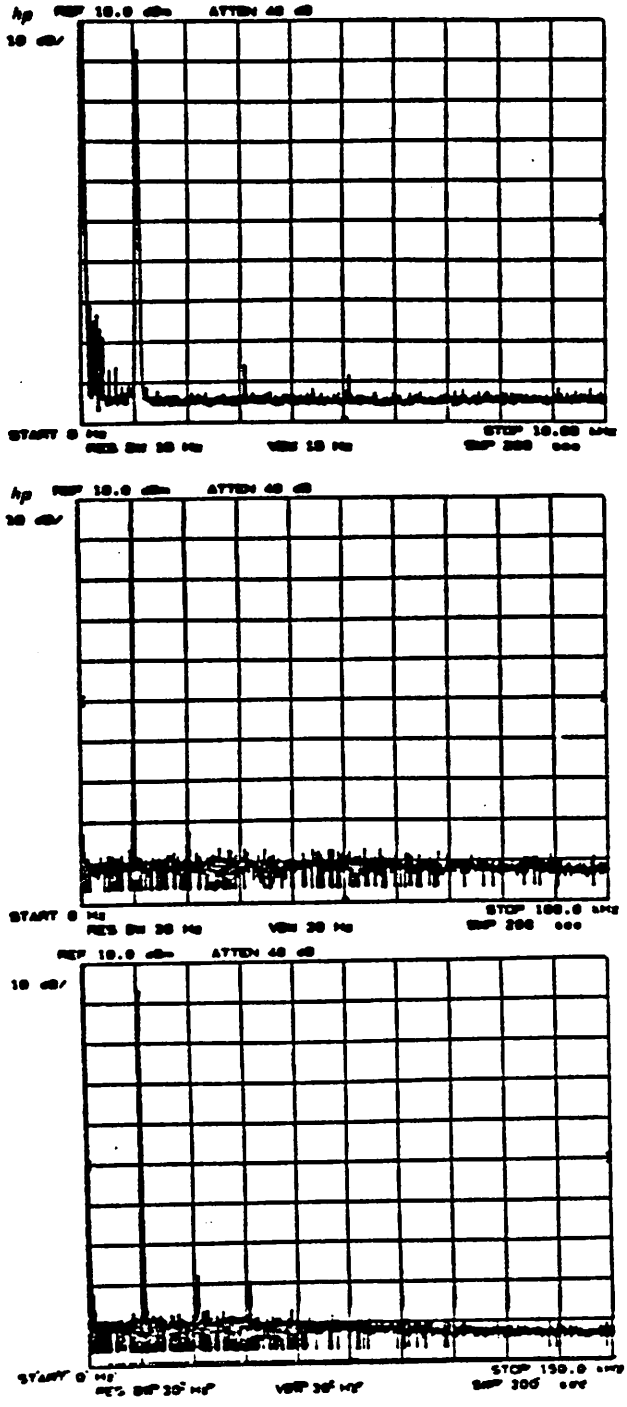
Figure 4.14

PSRR : (a) in 0 - 20kHz range, and (b) in 0 - 100kHz range.

TYPICAL FILTER CHARACTERISTICS		
FILTER PARAMETERS	**CONDITION**	**VALUE**
BANDWIDTH	500kHz clock	20kHz
PASSBAND RIPPLE		.12 dB
STOPBAND ATTEN.		57dB
P.S.R.R.	1kHz, positive supply	53 db
	1kHz, negative supply	63 dB
IDLE NOISE	20kHz bandwidth	350 μV
OUTPUT SWING (DIFFERENTIAL)	0.1% THD in 20kHz band	5 Vrms
DYNAMIC RANGE	20kHz band, 0.07% THD	82 dB
POWER CONSUMPTION	±5 V supply	16 mW
AREA		5170 $mils^2$

Table 4.3

Typical Filter Characteristics



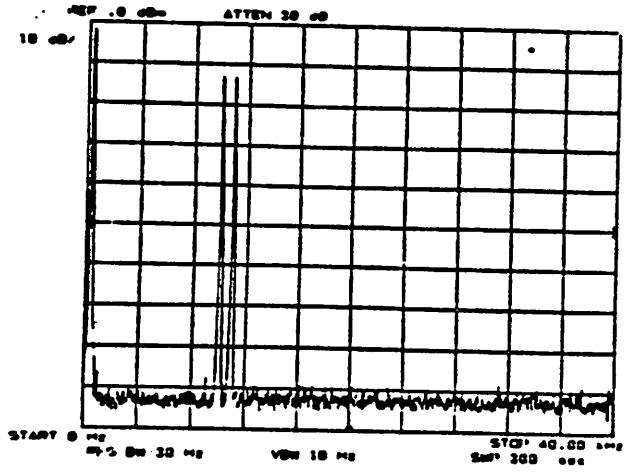
(a)

(b)

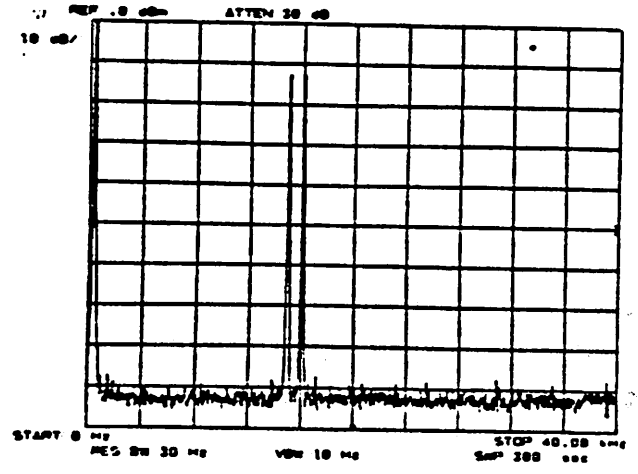
(c)

Figure 4.15

Harmonic distortion for 10Vp-p signals at filter output : (a) 1kHz, (b) 10kHz, and (c) 15kHz.



(a)



(b)

Figure 4.16

Intermodulation distortion for two pairs of signals, 2Vp-p for each frequency component : (a) 9kHz and 10kHz, (b) 15kHz and 16kHz.

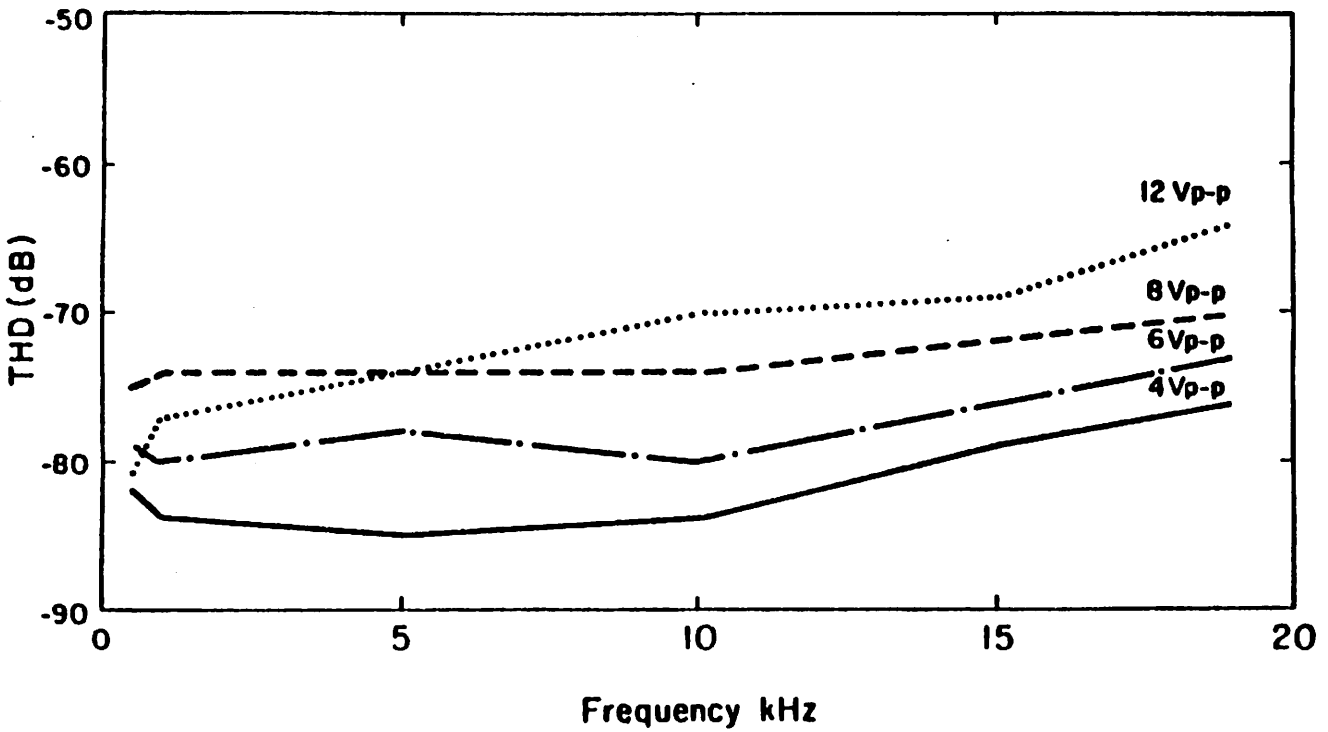


Figure 4.17 THD vs. signal frequency for (a) 20kHz bandwidth,

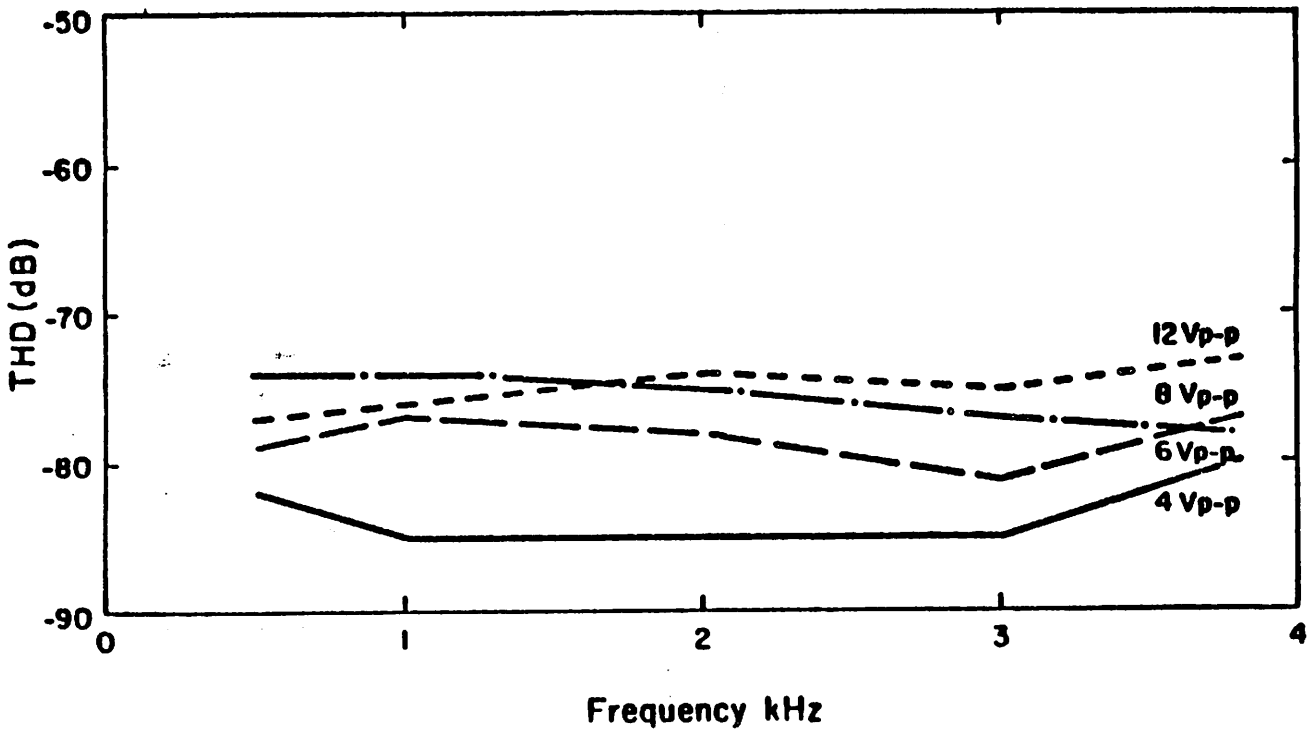


Figure 4.17 THD vs. signal frequency for (b) 4kHz.

frequency becomes higher, and (3) the residual nonlinearity of the initial "slewing" period, although reduced by the class A/B action, still introduces more distortion for higher signal frequencies. It can also be seen that the THD curve for 12Vp-p crosses the THD curve for 8Vp-p. This is is due to the shape of the op amp gain transfer curve (Figure 4.18), which has its first inflection at approximately 5V. Note that these distortion levels represent approximately an order of magnitude improvement over our measurements on several commercially available S.C. filters. The op amp is tested using the test circuit in Figure 4.19[34].

The noise spectrum of the 20kHz filter is shown in Figure 4.20, along with the filter characteristics. The total in-band noise ($\frac{1}{f}$ noise, $\frac{kT}{C}$ noise, op amp thermal noise, etc.) is approximately 350 μV. Combining with Figure 4.17 (a), it can be seen that for 0.07% THD the signal-to-noise ratio is larger than 82dB within the whole 20kHz range. Similarly, it can also be seen from Figure 4.17 (b) that for 4kHz bandwidth a 0.02% THD can be obtained for 82dB signal-to-noise ratio.

Although it is difficult to theoretically calculate the exact distortion level of the whole filter, some estimation can be made to compare the measured filter distortion with the theoretical results derived in Section 3.2. The measured capacitor voltage coefficients are $\alpha_1 = 20\,ppm\,/\,V$ and $\alpha_2 = 2\,ppm\,/\,V^2$. As discussed in Section 3.2, the second harmonic caused by the capacitor nonlinearity is canceled by the fully differential approach. From equation (2.10) and (2.16), the third harmonic introduced by capacitor nonlinearity is much smaller than the distortion caused by the op amp gain nonlinearity, and therefore can be neglected. The measured coefficients of the op amp gain transfer curve are $a_1 = -1180$, $a_2 = -1.26\times10^4\,/\,V$, and $a_3 = -1.81\times10^7\,/\,V^2$. The third harmonic distortion at the filter output is calculated by adding the contributions from all integrators. Note that different op amps have different gains to the filter output, and the contributions from each op amp should be

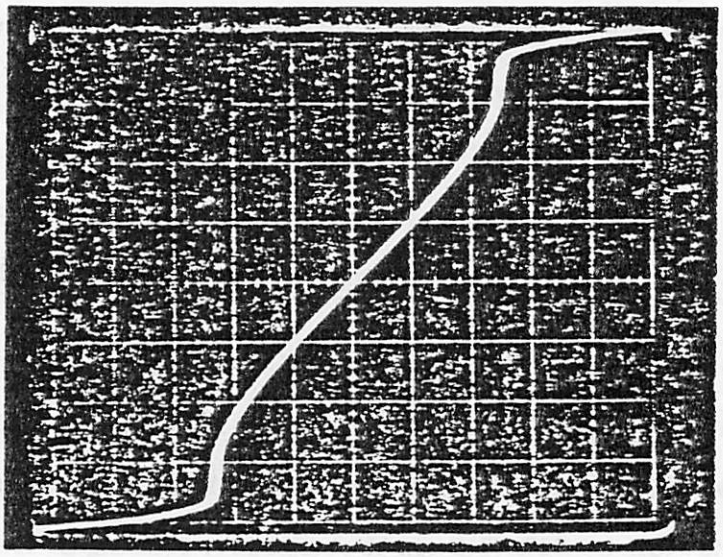


Figure 4.18

Op amp gain transfer curve. horizontal : 1.5mV/div, vertical : 2V/div.

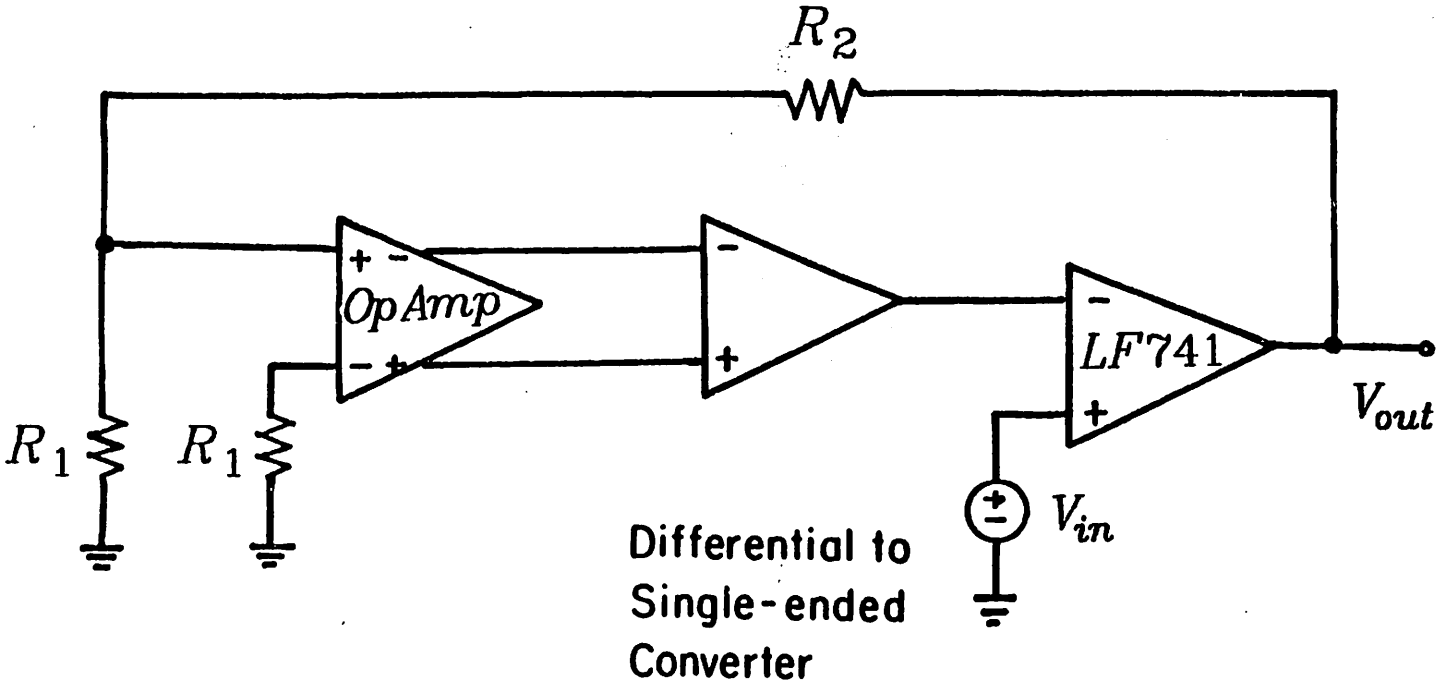
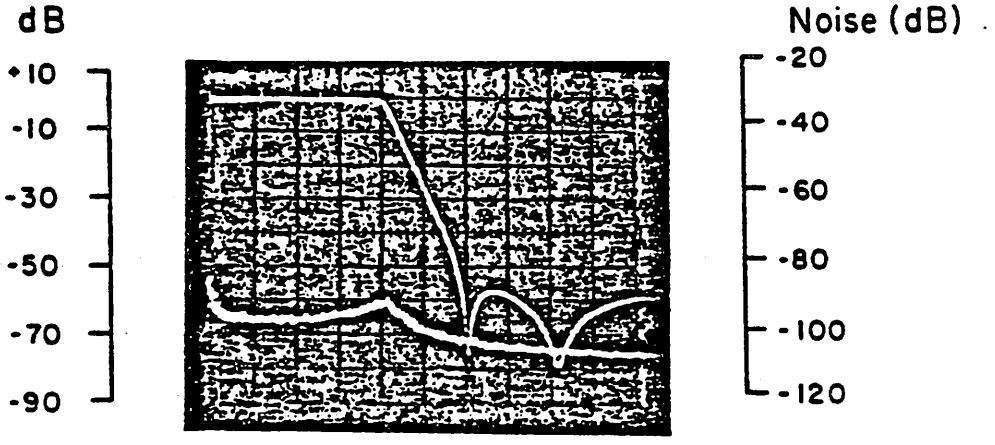


Figure 4.19 Op amp open-loop gain test circuit.



Filter response and noise, horizontal : 1.5mV/div, vertical : 2V/div.

weighted accordingly. For 8Vp-p filter output, the calculated HD_3 due to the op amp gain nonlinerity is approximately -80dB, which is several dB less than the measured values (Figure 4.17). This might be caused by the slight difference in the op amp gain transfer curves and the difference in bias condition for each op amp in the filter. From the above estimation, it is evident that the op amp performance (gain, linearity, speed) is the dominant factor limiting the distortion level in present S.C. filters. With some improvements in op amp design, 0.01% or even lower THD level should be achievable.

The effect of the 4-phase charge cancellation scheme is also tested by using different signal amplitudes. In this test the conventional two-phase clock and the four-phase clock proposed in the last section are both used for a 100kHz sampling rate and a 1kHz signal. The signal and clock frequencies are reduced here in order to reduce the effects of op amp settling and slewing. The result is shown in Figure 4.21. It is seen that the four-phase clock is always better than the conventional two-phase clock. However, this difference is less visible for high signal or high clock frequencies due to other more prominent distortion sources, such as the settling time and the slewing distortion. This result also suggests at which level the clock feedthrough and channel charge injection start to have an effect on the harmonic distortion, and therefore gives information about the fundamental limitations on the distortion of S.C circuits.

The effect of the clock frequency is shown in Figure 4.22. Here harmonic distortion as a function of clock frequency is plotted for two different signal frequencies. It is apparent that, when the clock frequency is above 500kHz, the distortion increases as the clock frequency increases. Also, above 500kHz, the distortion is higher for higher signal frequency.

Some important op amp characteristics are listed in Table 4.4 for supply voltages of $\pm$5V.

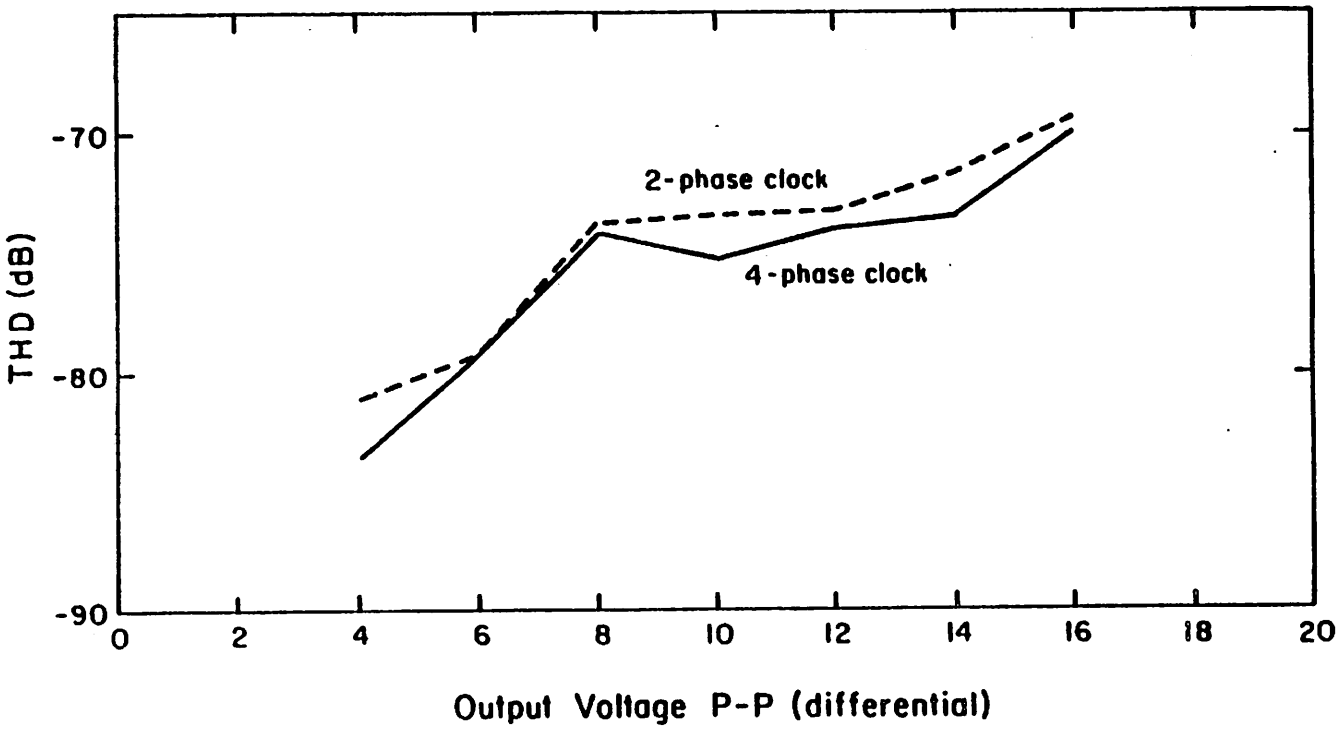


Figure 4.21 THD for two different clocking schemes.

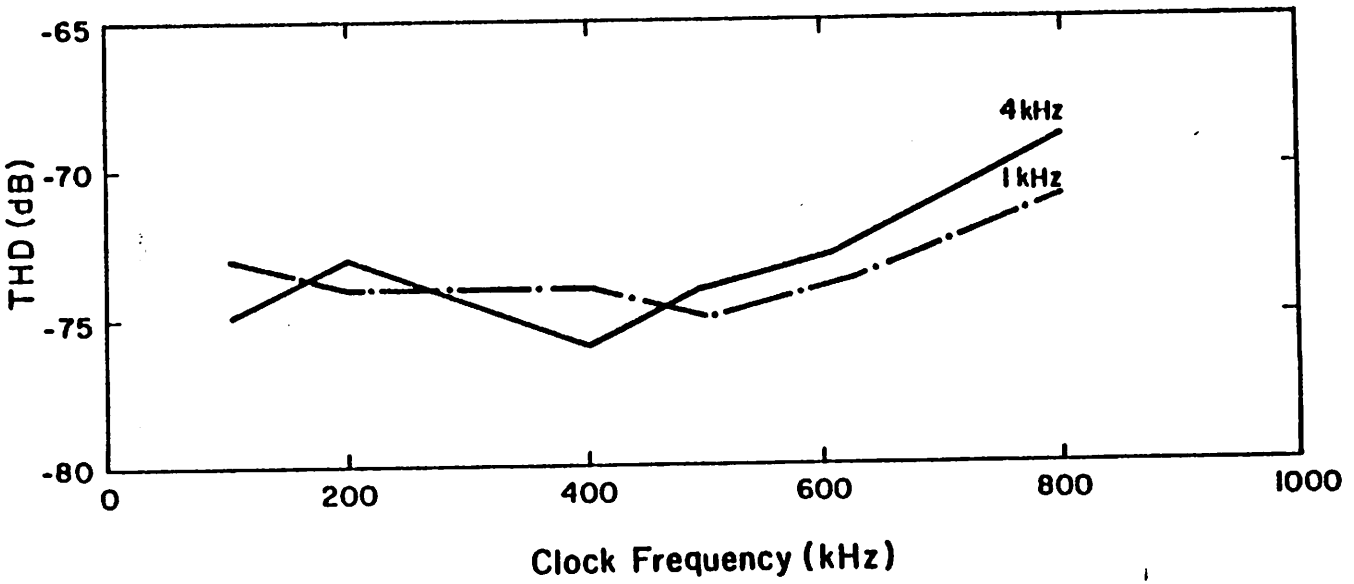


Figure 4.22 THD vs. clock frequency for 1kHz and 4kHz signals.

TYPICAL OP AMP CHARACTERISTICS (± 5V power supply)	
GAIN	1180
UNITY GAIN FREQUENCY	10MHz
C.M.R.R.	61 dB
POWER CONSUMPTION	2.3 *mW*
AREA	290 $mils^2$

Table 4.4

Typical Op Amp Characteristics

4.2. S.C. Integrator Measurements

Although the filter measurements provide some insight to the distortion behavior, more direct measurements are desired in order to verify the validity of the previous calculations. A stand-alone S.C. integrator is therefore included in a test chip, which is also implemented in the $5\mu m$ CMOS technology mentioned previously. This test chip also includes a separate differential op amp, and double-poly capacitors. A photograph of the test circuit is shown in Figure 4.23.

In conventional single-ended S.C. circuits the errors caused by the clock related effects, such as clock feedthrough (capacitive coupling of clock transitions) and channel charge injection, are so large that low level distortion caused by other sources are often masked by these effects. In the test circuit described here, the fully differential approach is used to alleviate these clock related error sources. By doing so, even harmonics are also much reduced at the same time, as explained in the previous chapters. Furthermore, a class A/B op amp is adopted in order to reduce the effect caused by the slew distortion.

The test configuration is shown in Figure 4.24. In Figure 4.24, the circuit circled by the dashed line is included in the test chip, while external single-ended to differential and differential to single-ended converters are used. Extra R-C low pass filters are also included in the feedback path to provide DC stability to the circuit.

Equation (2.13) can be used to estimate the distortion caused by capacitor nonlinearity. The sampling frequency is 100kHz, and the capacitor ratio $\frac{C_2}{C_1}$ for the test integrator is 4.7. The measured capacitor voltage coefficients are $\alpha_1 = 20\ ppm/V$ and $\alpha_2 = 2\ ppm/V^2$. From equation (2.13(b)), the third harmonic introduced by capacitor nonlinearity is close to -100dB for a single integrator. This is much smaller than the distortion caused by the op amp gain nonlinearity (equation (2.17)), and thus can be neglected. The measured coefficients of the op amp gain transfer curve are $a_1 = -950$,

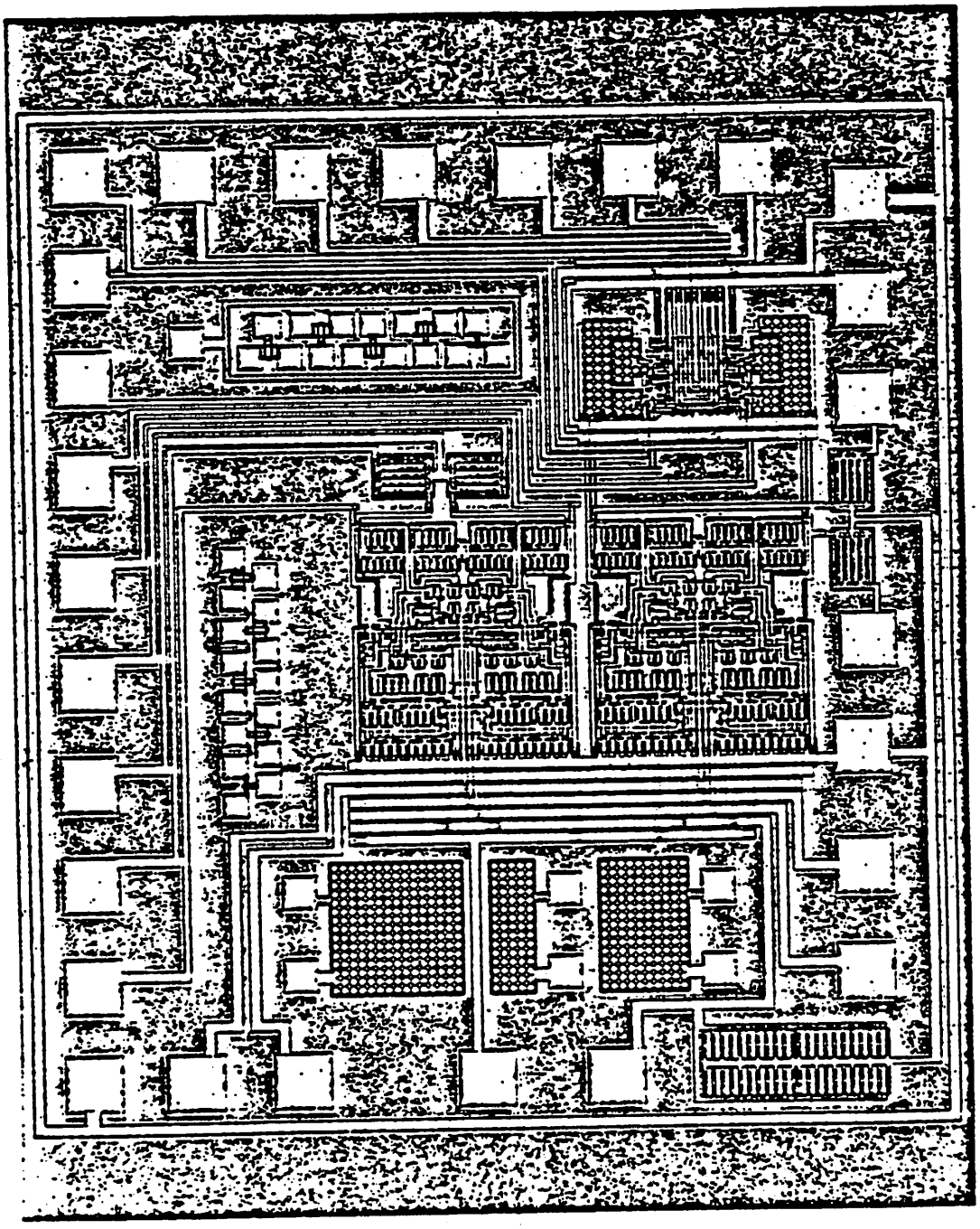


Figure 4.23 Integrator test chip.

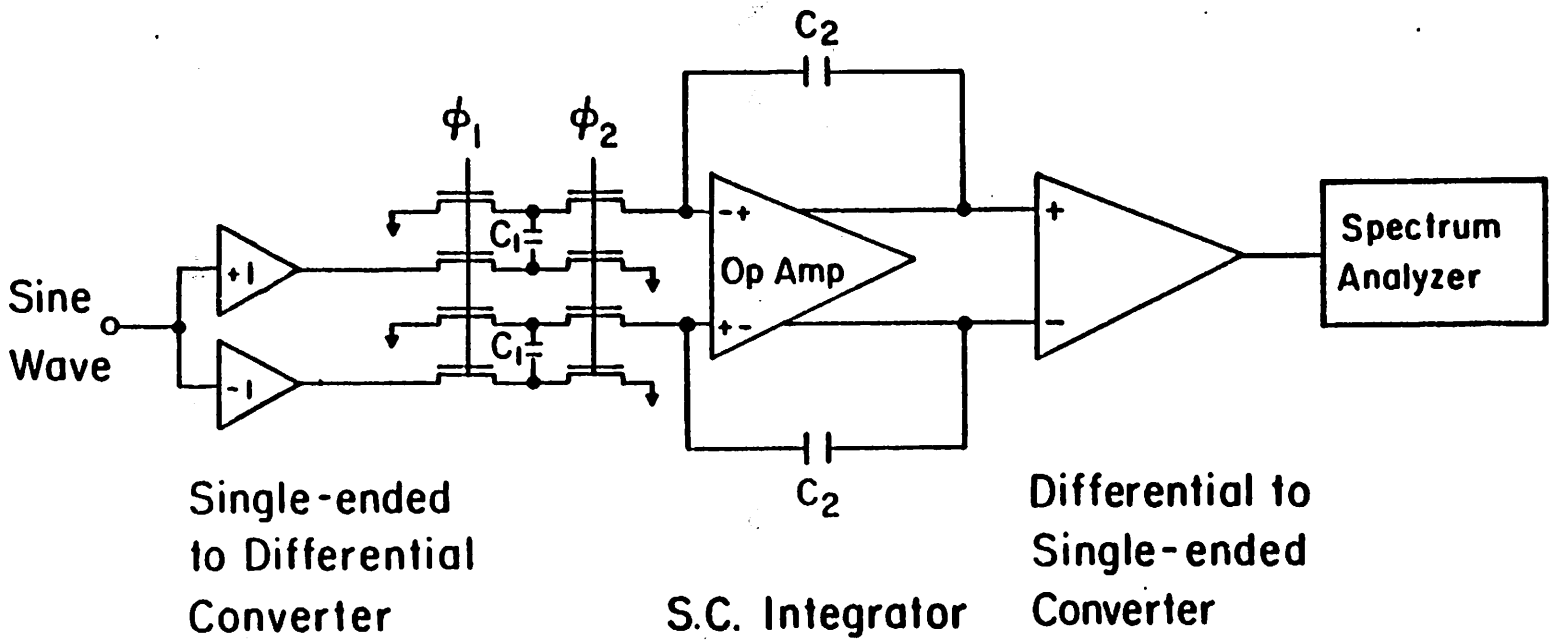


Figure 4.24 Test circuit for integrator test chip.

$a_2 = -2.62\times10^4 / V$, and $a_3 = -3.03\times10^7 / V^2$. The measured harmonic distortion for signals below 10kHz is shown in Figure 4.25. The measurements are made for two different frequency ranges, since the output amplitude is inversely proportional to signal frequency and the fundamental itself becomes very small at high frequencies. In Figure 4.25, the measured results are plotted against the theoretically derived results (equations (2.17 (a) and (b)). It can be seen that the theoretical and measured data have the same general trend, but the absolute values are different. The discrepancy may be caused by the shift of DC bias point as the integrator is connected in the feedback loop. Also, for low distortion levels (between -80 and -90dB), the measured data tend to deviate from the theoretical curve and become frequency independent. This is caused by the distortion induced by other sources, such as the clock feedthrough and charge injection.

In another measurement, the signal frequency is kept at 1kHz while the signal amplitude is varied. The result is shown in Figure 4.26. From Figure 4.26 it is evident that HD_2 is inversely proportional to V_o, and HD_3 inversely proportional to V_o^2. This also agrees with equations (2.17 (a) and (b)).

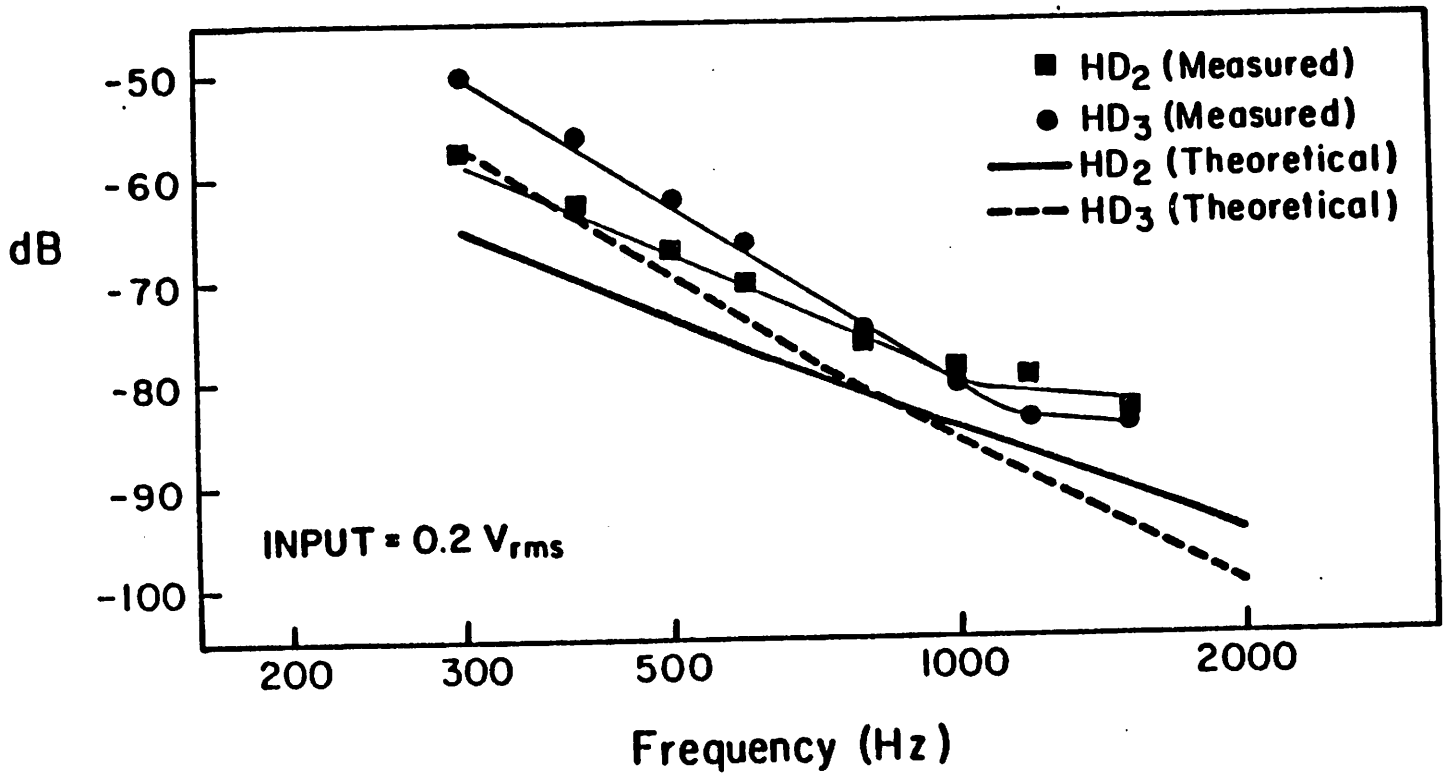


Figure 4.25 (a) Integrator harmonic distortion vs. signal frequency.

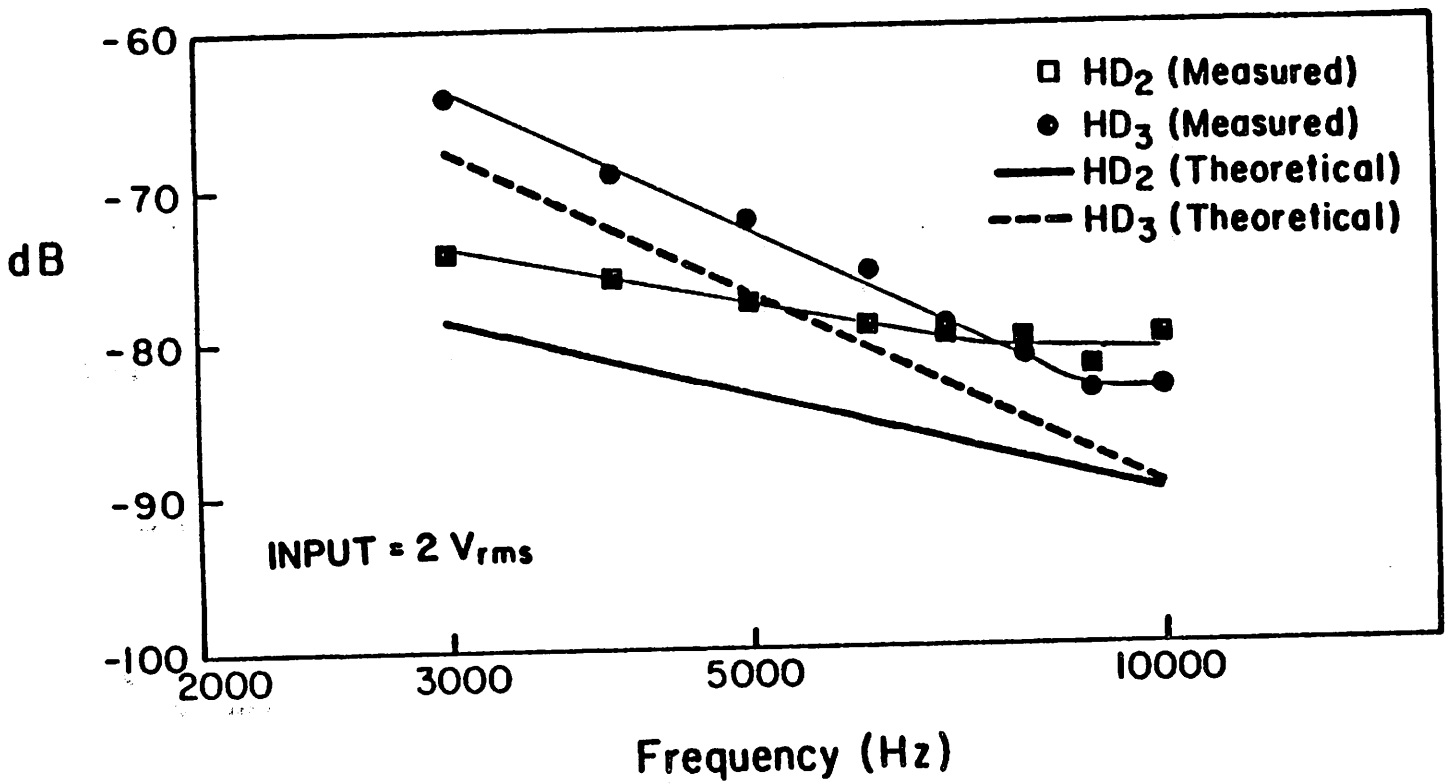


Figure 4.25 (b) Integrator harmonic distortion vs. signal frequency.

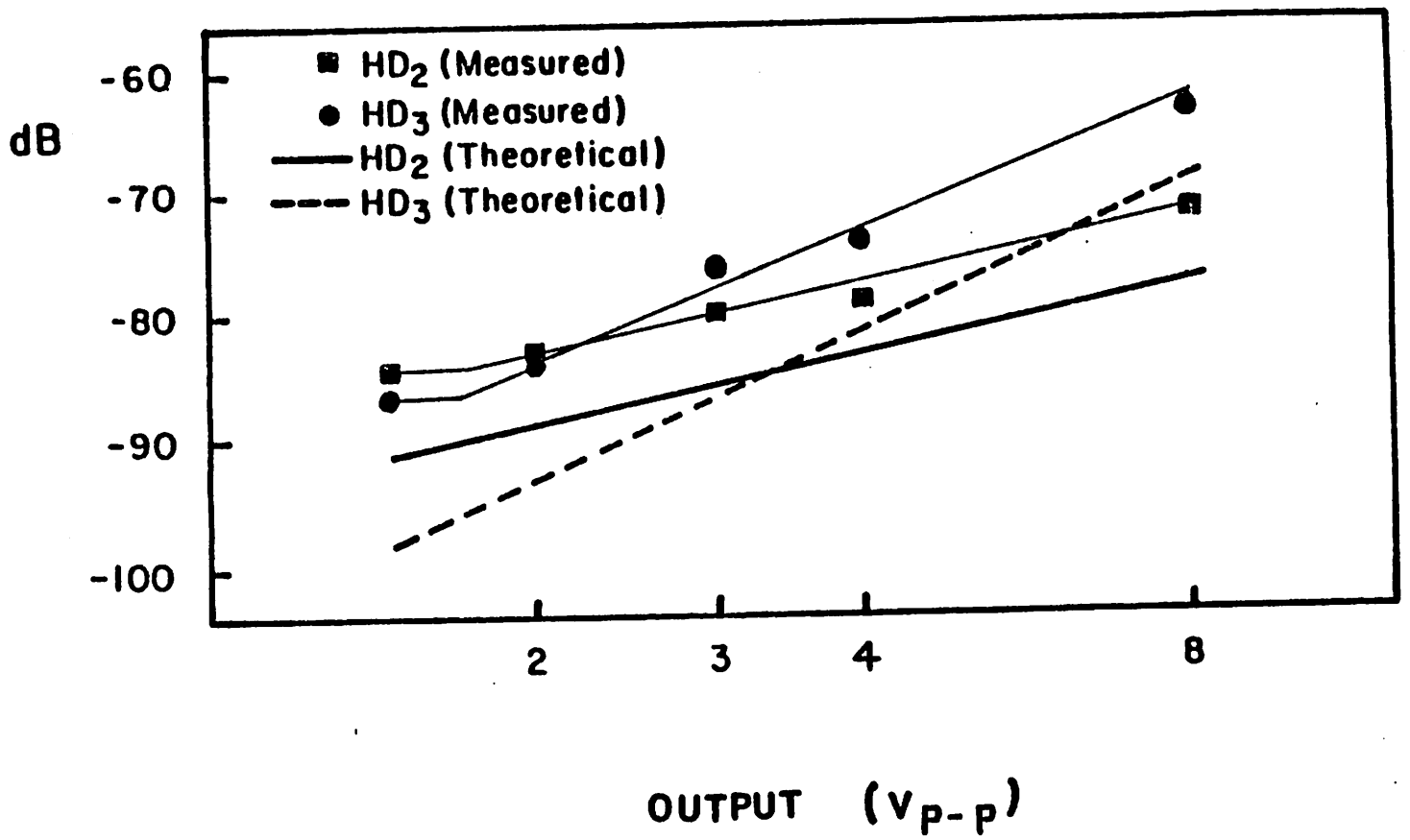


Figure 4.26 Integrator harmonic distortion vs. signal amplitude.

CHAPTER 5

SUMMARY AND CONCLUSIONS

The distortion mechanisms in S.C. circuits have been investigated. and closed form relationships between S.C. circuit parameters and harmonic distortion have been derived. It has been shown that the op amp gain nonlinearity. capacitor nonlinearity. finite op amp slew rate. and the effect of charge injection all introduce significant distortion.

The effects of these distortion sources can be either eliminated or reduced by circuit design techniques. Of the techniques discussed in this work. it is believed that using fully differential op amps and designing sufficiently high op amp gain are the most important. It is also demonstrated that for a fully differential S.C. circuit. the harmonic distortion induced by the clock feedthrough and charge injection is in the range of -80dB or lower. That seems to be the most fundamental limitation on further reducing the harmonic distortion in S.C. circuits.

Future work should be directed toward : (1) improving further the op amp performance. such as gain. speed. linearity; (2) shrinking the sizes of the differential op amps so that it is economical to use this kind of high performance op amps; (3) improving the capacitor linearity by processing techniques; and (4) applying novel clocking techniques to eliminate the clock related noise and errors.

APPENDICES

APPENDIX I BERKELEY CMOS PROCESS

APPENDIX II DISTORTION CALCULATION USING VOLTERRA SERIES

THE BERKELEY CMOS PROCESS (May 1984)

1. INITIAL WAFER PREPARATION

A. Wafer Cleaning

a. Spin the wafer on the wafer spinner and carefully slide a Q-tip soaked with TCA across the wafer several times.

b. With the wafer still spinning, direct a jet of acetone onto the wafer to remove any trace of TCA.

c. Using a squirt bottle, spray the wafer with methanol. Wait 20 seconds and the stop the spinner.

d. Inspect under collimated light.

e. Repeat (a) through (d) if the wafers are spotted.

B. Piranha Clean 5 min

C. Water Break Test HF:DI/1:10

Immerse the cleaned wafer into the dilute HF solution for approximately 10 seconds. Slowly pull out the wafer. If the wafer has been properly cleaned, the HF solution will sheet off from the surface.

2. INITIAL OXIDATION

Initial Ox Furnace
TCA clean prior to use.
1100 °C target: 315nm

Push	N_2	10.0	5 min
Ox	O_2	11.0	240 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	5 min

3. N-WELL DEFINITION

A. Standard Photolithography

HMDS	3 min on/5 min N2 purge
	(only enough bubbles to surround the tube)
AZ-1350J	6000 rpm/30 sec
Softbake	90 °C /15 min
Pattern	6.3
Develop	Micro-Dev:DI/1:1 30 sec
Hardbake	115 °C /20 min

The nominal exposure is 5.6. However, it is advised that you perform an exposure test to ascertain the optimal exposure setting. The exposed pattern under optimal condition should develop in 60 to 70 seconds.

B. Oxide Etch BHF/until well area becomes hydrophobic (2 min)

C. N-Well Implantation

Phos/100 Kev/8 ° /1.5 x 10^{13}

D. Photoresist Removal

Acetone 1 min/MeOH & DI rinse /Piranha 5 min

E. N-Well Drive In

Buried Layer Furnace
TCA clean prior to use
Piranha Clean 5 min

1100 °C

Push	N_2	15	3 min
Ox	O_2	15	280 min

Ramp furnace to 1150 °C

Drive	N_2:O_2	5.0:15	720 min
Anneal	N_2	10.0	20 min
Pull	N_2	10.0	3 min

The N-Well drive in is performed in a 10% O_2 atmosphere.

4. BUFFER OX OXIDATION

A. Oxide Etch Back

HF:DI 1:5 Etch until wafer becomes hydrophobic (~ 8 mins)

B. Piranha Clean5 min

C. Oxidation

Dry throughly
N-Drive Furnace
TCA Clean prior to use

1000 °C target: 55 nm

Push	N_2	10.0	3 min
Ox	O_2	11.0	50 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	3 min

5. NITRIDE DEPOSITION

Use dummy slats to smooth out the gas flow.
Place the wafers on the boat with the active faces of wafers facing each other.
Nitride should be deposited right after gate oxidation. This will prevent the gate from becoming contaminated. Nitride is an excellent barrier to contaminants.
The nitride deposition rate is higher at the outer surface than at the inner surface. Furthermore, the uniformity is better on the latter.

Gas flows are to be set to:

NH3	600mT	
SiH4	100mT	Determine the time by the dummy run

Deposit 150 nm (at the thinest area) of Nitride
2 hours and 15 mins facing outward.

6. ACTIVE DEFINITION

A. Standard Photolithography (Dry it thoughly double the dring time)

B. Nitride Etch

Preheat	N_2/1 Torr/60 W/ 70 oC
Descum	O_2/.76 Torr/10 W/5 min
Use parallel plate	SF_6–O_2/60 °C /100 W/ 15min

7. P-Field Definition

A Photoresist Removal

Acetone-Methonal-DI-Piranha 5 min

B Bake 115 °C/5 min

C Standard Photolithography

D P-Field Implantation

Boron/100 Kev/1.5x 10^{13}

E. Backside Implantation

a. Strip off photoresist
   Acetone-Methanel-DI-Piranha
b. Bake 115 °C /5 min
c. Spin on protective photoresist
   HMDS 3/5
   AZ-1350J 6000 rpm/30 sec
   Hardbake 115 °C /10 min
d. Backside oxide etch
   BHF
e. Implantation
   BF_2 /195Kev/2x 10^{15}
f. Strip off photoresist
   Acetone-Methanel-DI-Piranha

8. LOCOS

P Drive-in Furnace
950 °C target: 850 nm

Push	N_2	5.0	5 min
Ox	Steam	2.0	determine by test run (4hr and 15min)
	Set the bubbler heater to 110V.		
Anneal	N_2	10.0	20 min
Pull	N_2	10.0	5 min

* Approximately 2~ 3 refills of the bubbler is
* required at this heater setting. Make sure that
* you refill the bubbler before the water has
* completely evaporated. During the refill process
* switch the gas to N2.

9. NITRIDE REMOVAL

A. Oxide dip 1:10 HF/DI 40 sec

B. Nitride Remove Hot phosphoric Acid @ 155 °C use reflux about 30 min * 5% Sulfaric Acid will help the selective

10. THRESHOLD IMPLANTATION

Boron 50Kev/7.5x 10^{11}
Compensate for Noise

11. CAPACITOR DEFINITION

A. Standard Photolithography

B. Pre-implantation Bake

Plasma bake the photoresist
N_2/1 Torr/60 W/30 min

C. Implantation

Phos '80 Kev/2.5x 10^{15}
* Limit the implatation current(~ 2uA) to avoid photoresist getting too hard.

12. Buffer Oxide Removal

A Photoresist Removal

Ash off photoresist use reactor #1
O2/1 Torr/120 W/30 min

B Piranha clean 10 min

C Remove buffer oxide

DI/HF 10:1 ~ 100sec (about 5A per sec)
*Careful not to overetch

13. GATE OXIDATION

N Drive-in Furnace
TCA clean prior to use
1000 °C target: 50 nm

Push	N_2	10.0	5 min
Ox	O_2	11.0	45 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	5 min

14. POLY DEPOSITION/DOPING

A. Piranha Clean 10 min

B. Poly Deposition

Place the wafers on the boat with the active faces of the wafers facing each other.

Gas Flow:
SiH_4 600mT
Determine by dummy run(about 20min)..... 300 ~ 400 nm of poly

C. Poly Doping

950 °C @ N-predep furnace, turn on the source cooling 30 min prior to use

Push	N_2	10	3 min
Ox	O_2:N_2	4.5:9.0	5 min
Dope	O_2:N_2:$POCl_3$	4.5:9.0:13.0	30 min
Anneal	N_2	10.0	5 min
Pull	N_2	10.0	3 min

Perform V/I measurement to ascertain polysilicon doping.

15. NMOS DEFINITION

A. Deglaze

The phosphorous glass must be removed prior to photolithography. Photoresist will not adhere to phosphorous-rich glass.

HF:DI 1:10 10" 20 sec
Do the water break test to determine the time.
Do not dipe over 1 min.
Piranha Clean 5 min. (Grow a thin layer of oxide to get better adhesion)

B. IR Bake 30 min (Lower the IR lamp and Dry it very thoughly)

C. Standard Photolithography

D. Standard Polysilicon Etch

Preheat N2/1 Torr/60 W/70 oC
Descum O2/.76 Torr/10 W/5 min
Use parallel plate SF_6-O_2/60 °C/50W/" 3min
Flow rate for SF_6 is 20 and O_2 is 2

* Polysilicon etches faster than nitride. We
* advise that you etch one wafer at a time.
* The parallel plate plasma etcher etch faster toward
* the center. Put the wafer's flat side outward.
* Use the end-point detecter to prevent over etch.

E. Photoresist Removal

Acetone 1 min/MeOH & DI Rinse/Piranha 5 min

F. Implantation

As/180 Kev/3x 10^{15}

16. PMOS DEFINITION

A. Piranha Clean 5 min

B. Standard Photolithography

C. Standard Polysilicon Etch

Be very careful when defining the PMOS poly gate. Visual detection of end-point is next to impossible. Therefore, etch in SF6-O2 for 50% of the time required during NMOS gate definition. Inspect the wafers under the microscope, and etch again if necessary. Be very careful not to over-etch. Averagely it takes less time than the NMOS etching time.

D. Pre-implantation Bake

N2/1 Torr/60 W/45 min

E. Implantation

Boron/60 KeV/ 2×10^{15}

F. Photoresist Removal

Ash off photoresist
O2/1 Torr/120 W/40 min

G Poly Reoxidation

Piranha clean 5 min
P Drive-in furnace
1000 °C.

Push	N_2	10.0	5 min
Ox	O_2	11.0	30 min
Anneal	N_2	10.0	10 min
Pull	N_2	10.0	5 min

17. PASSIVATION

A. Piranha Clean 5 min

B. CVD Deposition

350 nm undoped CVD oxide
650 nm 7% PSG oxide
* Due to high reflow temperature, a sandwich
* layer of CVD oxide is necessary in order to
* prevent the counter-doping of the p+ diffusions.

C. Reflow and Densification

N-Drive Furnace
1050 °C

Push	N_2	5.0	3 min
Densify	N_2	5.0	20 min
Pull	N_2	5.0	3 min

18. CONTACT DEFINITION

A. Standard Photolithography (Increase the light dose to 6.0~6.2. use dummy wafer to test the best exposer time)

B. Oxide Etch

Determine the PSG etch rate from the blank dummy wafers. Use this etch rate to gauge your etch-bake time cycle..
(1. 15sec 2. 30sec 3. 30sec 4. 45sec 5. 60sec...
after 6 min increase every two mins)

Etch/Bake/Etch to prevent contact cuts from blooming.

Etch BHF
Bake 130 °C/10 min

Repeat as many times as required.

C. Remove Photoresist

Acetone 1 min /Rinse with Methanel & DI/Piranha 5 min

19. METALLIZATION

A. Oxide Dip

HF:DI/1:10 5 sec

This oxide dip removes the thin oxide which
was grown over the vias during piranha cleaning.

B. IR Bake 20 min

C. Aluminum Sputtering target: 500~ 1000A

Set the sputtering machine 470V/1.5A /10mT
Open the shutter for 15 sec then cool down for 4 min
Repeat as many time as needed.
Growth rate is about 0.35u/min at center. 0.25 at edge

20. METAL RUN DEFINITION

A. Standard Photolithography

Use 5.5 for exposer time
Reduce exposure time by 25%
Canon each nobe is 6%

B. Metal Etch

Aluminum Etchant Type A 45 °C

C. Photoresist Remo . al

Acetone 5 min

21. BACKSIDE PREPARATION

A. IR Bake 10 min
B. Spin on protective photoresist
C Etch the back poly either in barrel reactor or parallel plate
D. Oxide etch (Etch till hydrophobic)
E. Aluminum sputter on the backside target: 1 um
F. Photo Resist Removal Acetone 5 min

22. SINTERING

Forming gas N_2:H_2 10:1	15 cm	20 min	350 °C

APPENDIX II

DISTORTION CALCULATION USING VOLTERRA SERIES

In Chapter 2, some of the theoretical results are derived based on time-domain analysis. These results can also be derived by analysis in frequency-domain, namely the method of Volterra series. This analysis will be illustrated below to calculate the distortion introduced by the operational amplifier gain nonlinearity.

First, as in Chapter 2, the charge conservation equation of the integrator (see Figure 2.4) can be written as

$$C_s v_i(n-\frac{1}{2}) = C_s v_1(n) + C_f[(v_1(n)-v_o(n))-(v_1(n-1)-v_o(n-1))] \quad (1)$$

Or, it can be written as

$$C_s v_i(n-\frac{1}{2}) = C_s v_1(n) + C_f \Delta[v_1(n)-v_o(n)], \quad (1a)$$

where $\Delta[\cdot]$ represents taking difference of a certain function for two consecutive time instants.

Meanwhile the relationship between v_1 and v_o can be expressed as power series

$$v_o = a_1 v_1 + a_2 v_1^2 + a_3 v_1^3 + \cdots . \quad (2)$$

$$v_1 = b_1 v_o + b_2 v_o^2 + b_3 v_o^3 + \cdots . \quad (3)$$

Here the relationship between a_i's and b_i's can be expressed as

$$b_1 = \frac{1}{a_1}, \quad (4a)$$

$$b_2 = -\frac{a_2}{a_1^3}, \quad (4b)$$

$$b_3 = \frac{2a_2^2 - a_1 a_3}{a_1^5}, \quad (4c)$$

Substitute (3) into (1a), (1a) becomes

$$C_s v_i(n-\tfrac{1}{2}) = C_s\left[b_1 v_o(n) + b_2 v_o^2(n) + b_3 v_o^3(n) + \cdots\right] + C_I\Delta\left[(b_1-1)v_o(n) + b_2 v_o^2(n) + b_3 v_o^3(n) + \cdots\right] \quad (5)$$

Assume

$$v_o = A_1(j\omega) o v_i + A_2(j\omega_1, j\omega_2) o v_i^2 + A_3(j\omega_1, j\omega_2, j\omega_3) o v_i^3 \ldots. \quad (6)$$

Substitute (6) into (5) and equate v_i, v_i^2, v_i^3 terms on both sides. For v_i term,

$$C_s e^{-j\frac{\omega T}{2}} = C_s b_1 A_1(j\omega) - 2j C_I e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}[(b_1-1)A_1(j\omega)], \quad (7)$$

and therefore

$$A_1(j\omega) = \frac{C_s e^{-j\frac{\omega T}{2}}}{b_1 C_s - 2j C_I e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}(b_1-1)} \approx -\frac{C_s}{2j C_I \sin\frac{\omega T}{2}}. \quad (8)$$

Similarly, by euating the v_i^2 term,

$$A_2(j\omega_1, j\omega_2) = -\frac{b_2 A_1(j\omega_1)A_1(j\omega_2)\left[1 + 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{(\omega_1+\omega_2)T}{2}} \sin\frac{(\omega_1+\omega_2)T}{2}\right]}{b_1 - 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{(\omega_1+\omega_2)T}{2}} \sin\frac{(\omega_1+\omega_2)T}{2}}. \quad (9)$$

By equating the v_i^3 term,

$$0 = A_3(j\omega_1, j\omega_2, j\omega_3) Y_1(\omega_1+\omega_2+\omega_3) + \left[2b_2 A_1(j\omega_1)A_2(j\omega_1, j\omega_2) + b_3 A_1(j\omega_1)A_2(j\omega_2)A_1(j\omega_3)\right] \cdot Y_2(\omega_1+\omega_2+\omega_3), \quad (10)$$

where

$$Y_1(\omega) = b_1(cs + 2j C_I e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}) - 2j \sin\frac{\omega T}{2} e^{-j\frac{\omega T}{2}}.$$

$$Y_2(\omega) = C_s + 2j\, C_I\, e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}.$$

Solving for $A_3(j\omega_1, j\omega_2, j\omega_3)$.

$$A_3(j\omega_1 j\omega_2, j\omega_3) = -\frac{Y_2(\omega_1+\omega_2+\omega_3)\left[2b_2A_1(j\omega_1)A_2(j\omega_2, j\omega_3) + b_3A_1(j\omega_1)A_1(j\omega_2)A_1(j\omega_3)\right]}{Y_1(\omega_1+\omega_2+\omega_3)}$$

$$= -\frac{C_s + 2j\, C_I\, e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}}{b_1 C_s - 2j\, C_I\, e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}}\left[2b_2A_1(j\omega_1)A_2(j\omega_2, j\omega_3) + b_3A_1(j\omega_1)A_1(j\omega_2)A_1(j\omega_3)\right].$$

$$\approx -\frac{C_s + 2j\, C_I\, e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}}{b_1 C_s - 2j\, C_I\, e^{-j\frac{\omega T}{2}} \sin\frac{\omega T}{2}}\left[b_3\left(\frac{C_s}{C_I}\right)^3 \frac{1}{8j \sin\frac{\omega_1 T}{2}\sin\frac{\omega_2 T}{2}\sin\frac{\omega_3 T}{2}}\right]. \qquad (11)$$

The harmonic distortion can be obtained from A_1, A_2, A_3 as illustrated below.

$$HD_2 = \left| \frac{b_2A_2(j\omega, j\omega)\frac{V_i^2}{2}}{A_1(j\omega)V_i} \right| \qquad (12a)$$

$$= \left| \frac{b_2V_i}{2} A_1(j\omega) \frac{1 + 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{\omega T}{2}}\sin\omega T}{b_1 - 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{\omega T}{2}}\sin\omega T} \right| \qquad (12b)$$

$$= \left| \frac{b_2V_o}{2} \frac{1 + 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{\omega T}{2}}\sin\omega T}{b_1 - 2j\left(\frac{C_I}{C_s}\right)e^{-j\frac{\omega T}{2}}\sin\omega T} \right| \qquad (12c)$$

$$\approx \frac{b_2V_o}{2}\sqrt{1 + \left(\frac{V_o}{2V_i}\right)^2}. \qquad (12d)$$

The third harmonic can be obtained by similar method :

$$HD_3 = \left| \frac{b_3 A_3(j\omega, j\omega, j\omega)\frac{v_i^3}{4}}{A_1(j\omega)V_i} \right| \tag{13a}$$

$$\approx \left| b_3 A_1(j\omega)A_1(j\omega)A_1(j\omega)\frac{\frac{V_i^3}{4}}{A_1(j\omega)V_i} \right| \tag{13b}$$

$$= \left| \frac{b_3\left[A_1(j\omega)V_i\right]^2}{4}\frac{1+2j\left(\frac{C_f}{C_s}\right)e^{-j\frac{3\omega T}{2}}\sin\frac{3\omega T}{2}}{b_1-2j\left(\frac{C_f}{C_s}\right)e^{-j\frac{3\omega T}{2}}\sin\frac{3\omega T}{2}} \right|. \tag{13c}$$

$$\approx \frac{b_3 V_o^2}{4}\left(1+\frac{V_o}{3V_i}\right). \tag{13d}$$

Using the same method, other harmonics can also be obtained. Note that the above results agree with the results given in Chapter 2 from time-domain analysis.

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