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I. Introduction

When developing an integrated circuit (IC) process one would like to have the ability both to electrically test the circuit during its development and also to monitor the process in situ once a recipe has been established. The purpose of the test is to reject wafers on which devices do not meet process specifications, thus, saving additional processing cost. Usually, test structures are included to monitor the process rather than checking the actual devices. These test structures should incorporate the processing steps of the IC without requiring any special processing themselves.

This research was motivated by the goal to begin fabricating GaAs integrated circuits at UC Berkeley. The initial work in designing a process begins with calibrating and understanding each process step. For GaAs MESFET technology to be implemented in LSI, an excellent understanding and control of the ion implant and anneal is essential; therefore, in this research test structures and techniques have been explored for characterizing the implant. The implant profile is complicated both by an inability to totally activate the dopant with annealing and by compensating defects. Characterization techniques may be used to understand the migration and aggregation of defects during annealing and their influence on device performance.

In the course of this endeavor a large quantity of experience was accumulated in GaAs processing techniques and considerations. The processing experience involves methods for fabricating Schottky diodes on ion implanted and annealed semi-insulating (SI) GaAs. In the final phase of this research, simple MESFET structures were fabricated for use in studying the ion implanted layer with conductance DLTS. A Schottky barrier can be used for current-voltage (I-V), capacitance-voltage (C-V), and Deep Level Transient Spectroscopy (DLTS) while Hall and 4-point probe measurements only requires an ohmic contact. With these measuring techniques, information can be obtained about the ion implant profile, effectiveness of the anneal, and process cleanliness.

In this paper, background information will be given on a number of electrical techniques used to monitor the implanted region. The test structures will be outlined and the processes described along with a discussion of considerations necessary for processing with GaAs. The results of different matrix studies will be given for the I-V and C-V measurements. In addition, an example of a typical DLTS measurement on Si will be provided.

II. Measurement Techniques

If a device is to be used for an AC application, DC measurements are not sufficient; likewise, it is imperative to consider the external effects when performing measurements. Photo currents and voltages can significantly alter many measurements on GaAs including changing the contact resistance between probes and pads. In addition, the samples should be kept at uniform temperature and precautions taken against current-induced resistive heating since the temperature coefficient of resistivity for semiconductors is significant. Unwarranted sources, such as leakage paths, stray capacitance, inadequate grounding, and electromagnetic noise, which may overwhelm the signal of interest, must also be eliminated. Diode characteristics have also been observed to vary as a function of probe pressure.

A. Current-Voltage Measurements (I-V)

An I-V measurement is a fundamental test for most device characterization. The diode ideality factor, n, and information concerning the conduction mechanism in effect is obtained by fitting the log-plot from an I-V measurement to the simple diode equation from thermionic emission theory: $J=J_s(e^{V/nV_T}-1)$, where $V_T = \frac{kT}{q}$. The ideality factor is a measure of the change in the Schottky barrier height with applied bias, and a near unity value may be interpreted as an ideal metal-semiconductor interface (i.e. near intimate contact). For a Schottky diode the saturation current is:

$$J_s=KT^2e^{-\phi_B/V_T} \tag{2.1}$$

where: K = an empirical constant and ϕ_B = the barrier height between the metal and semiconductor.

The barrier height is the most important parameter of a Schottky diode since it is a measure of the leakage current. Interface states due to defects can pin the Fermi level, thus, affecting the Schottky barrier height. Consequently, ϕ_B is a very sensitive measure

of surface preparation procedures. In the event that no interfacial impurities exist, the ideality factor will still be bias sensitive due to image-force effects.[1]

$$\frac{1}{n} = 1-\frac{1}{4}\left[\frac{q^3 N_d}{8\pi^2 \epsilon_s^3}\right]\left[\phi_B - V - (E_c - E_F) - \frac{kT}{q}\right]^{-3/4} \tag{2.2}$$

B. Capacitance-Voltage Measurements (C-V)

The C-V measurement is used to determine the semiconductor doping profile using the facts that

$$W = \frac{A\epsilon}{C} \tag{2.3}$$

and for uniformly doped semiconductors

$$C = \left[\frac{q\epsilon N}{2(V_{bi}-V)}\right]^{1/2}. \tag{2.4}$$

where N = the doping density and V_{bi} = the built in zero bias voltage (across space charge region), and more generally,

$$\frac{d(1/C^2)}{dV} = \frac{2}{q\epsilon N}. \tag{2.5}$$

From Equations (2.3) and (2.5) a plot of N_{doping} vs. x may be drawn. For the case of varying doping with depth (eg. implants and diffusions), the C-V measurement results in the free carrier profile which may be quite different from the doping profile. This is due to compensation from deep levels traps and free carrier diffusion from heavily doped to lightly doped regions.

Even though both I-V and C-V measurements are quasi-static, the C-V measurement is affected by both the large population of defects[2, 3] introduced by the implant (Figure 2.1) and the deep levels in as grown material, such as EL_2, which is observable as a transient in a C-V measurement if the sample is heated above room temperature. These traps will tend to affect the response of the sample to the small-signal AC probe as a function of sample temperature and emission rate of the trap. At the metal-semiconductor interface there may exist an undefined region which contains ionic species and both fast and slow

surface states which can affect shallow profiling; however, as the sample is further reverse biased, the surface states exhibit less influence.

The conventional C-V measurement assumes perfect diode and bulk characteristics. Sample preparation and metalization procedures have been observed to affect the profiles obtained. Other consideration when performing a C-V profile are device leakage current and series resistance. Leakage current is a low-bias effect which is manifest as a decrease in the depletion width for an increased reverse bias since the electrons traversing the space charge region compensate the ionized donors. Consequently, the meter should be set to measure in parallel mode so that it can compensate for the high leakage (i.e. low resistance). Series resistance effects become important when the depletion edge is located deep in the tail of the implant. As the bias is increased, the conducting region is pinched between the depletion edge and the SI GaAs so that the RC time constant increases quickly, and at this point, the capacitance reading becomes questionable as both it and the Q of the system approach zero and may go negative. This is an instrument effect which has been observed on various HP LCZ meters using the parallel measurement mode.

C. Resistivity Measurements

Resistivity measurements are a common technique for obtaining reasonable values for free carrier concentration. The standard four-point probe apparatus places four probes collinearly with current passing through the outer two probes and the voltage drop measured by the center two. For equally spaced probes residing on a semi-infinite surface, the resistivity is:

$$\rho = 2\pi L\frac{V}{I} \tag{2.6}$$

where L is the probe spacing. For finite samples the equation is:

$$\rho = CF\frac{V}{I} \quad \text{where CF = correction factor.} \tag{2.7}$$

A correction factor of 4.53 [4] is used for thin samples with boundaries > 20L from the

probes. With lightly doped GaAs the technique is limited since the two outer probes form Schottky diodes with one diode operating in forward bias and the other in reverse. Attempts were made to use this technique on lightly implanted ($1x10^{12}$ cm^{-2} and $1x10^{13}$ cm^{-2}) SI GaAs but the current source usually exceeded its output capability while $1x10^{14}$ cm^{-2} material was measurable. A few four-point probe stations employ probes that are plated with a dopant which dopes the GaAs before probing (or hot probes).

Fabricated ohmic contacts and contactless measurements are regularly employed to measure the resistivity of GaAs. The latter approach is preferred if the sample is not to be damaged; however, fabricated contacts are most popular since the process is rather straight forward. Fabricated resistive devices may use a geometry similar to that of the four-point probe; but usually, the van der Pauw [5] method, which is described in the next section, is preferred. The non-contact measurements most commonly employed are either a capacitive-coupled resistance measurement or a measure of the perturbation of a microwave system by the sample. Microwave measurements require that either a waveguide or cavity be characterized with calibrated samples such that the perturbation of various resistive samples is known. One method is to measure the transmission properties of the sample in a waveguide but this results in a measurement of the implant plus substrate and is usually destructive since the sample is cut to fit into the waveguide. A more appropriate approach places the sample on the the end of a waveguide and the attenuation and phase of the reflected wave is measured. This provides the capability to measure just the resistivity of the implanted or epitaxial layer.[6] Resistance measurements using capacitance coupling are generally carried out at megahertz frequencies and consists of a sample with the probes separated from the surface by a thin insulator. All methods take advantage of the influence of resistivity and applied electric field on the transfer of charge in the semiconductor with both bridges and Q-meter measurements being reported.[7, 8]

D. Mobility Measurement

It is essential to characterize the anneal process such that the carrier mobility in the implanted channel may be optimized in order to maximize the device speed. The enthusiastic interest in GaAs devices is motivated by the fact that the bulk electron mobility can be 8500 $cm^2/ V-s$ as compared with 1500 $cm^2/ V-s$ for Si (300°K); however, this value is not usually attained in the channel region (Figure 2.2). In GaAs three major scattering mechanisms which affect the mobility are present: acoustic scattering due to crystal imperfections ($\mu_l \propto T^{-3/2}$), ionized impurities scattering ($\mu_i \propto T^{3/2}$), and optical phonon scattering which occurs when the electrons move in to the low mobility side band minima which is 0.31 eV above the minima at k=0. Consequently, the effectiveness of the anneal and implant is commonly monitored with a mobility measurement.

Mobility may be determined by the relation:

$$J = \mu nqE \tag{2.8}$$

where a resistivity measurement, $\rho = \frac{1}{\mu nq}$ plus a value for free carrier concentration, n, will yield the mobility. However, it is more common to determine n and the mobility with a Hall measurement. This measurement yields the Hall coefficient, R, and Hall mobility, μ_H, which are defined by [9]

$$|R|\,\sigma = \mu_H \tag{2.9}$$

where

$$R=\frac{r}{q}\frac{p\mu_h^2-n\mu_e^2}{(n\mu_e+p\mu_h)^2} \tag{2.10}$$

The numerical factor r varies between 1 and 2 depending on the degeneracy in the conduction band and dominant scattering mechanism. The channel of a MESFET is n-type so $p \simeq 0$ and $R = \frac{-r}{nq}$.

When calibrating and monitoring a process, one usually does not cut out a special Hall "bar" to measure the mobility but rather the method introduced by van der Pauw

[5,10] is used. This method requires a flat solid of uniform thickness containing no enclosed holes (ie. a lamella). Point contacts are placed arbitrarily along the periphery and labeled consecutively A, B, C, D (Figure 2.3a). Two resistances are defined:

$$R_{AB,CD} = \frac{V_B - V_C}{I_{AB}} \tag{2.11}$$

and similarly,

$$R_{BC,DA} = \frac{V_A - V_D}{I_{BC}} \tag{2.12}$$

where for I_{12} the current enters at 1 and exits at 2. By using elementary electromagnetic boundary theory, it can be shown that for a semi-infinite plane with contacts along the boundary that

$$\exp^{-\frac{\pi t}{\rho}R_{AB,CD}} + \exp^{-\frac{\pi t}{\rho}R_{BC,DA}} = 1 \tag{2.13}$$

where t is the sample thickness and ρ the resistivity. Using conformal-mapping techniques this solution is proven to hold for a sample of arbitrary periphery so long as no holes are contained. Usually, Hall measurements are performed on symmetric samples such that $R_{AB,CD} = R_{BC,DA}$. Thus, Equation (2.13) has a simple solution for ρ :

$$\rho = \frac{\pi t}{\ln 2}. \tag{2.14}$$

The general solution of Equation (2.13) is:

$$\rho = \frac{\pi t}{\ln 2} \frac{R_{AB,CD} + R_{BC,DA}}{2} \, f\left[\frac{R_{AB,CD}}{R_{BC,DA}}\right] \tag{2.15}$$

where the function f varies from 1 to 0 and is plotted by van der Pauw. This function contains cosh as expected from the form of Equation (2.13).

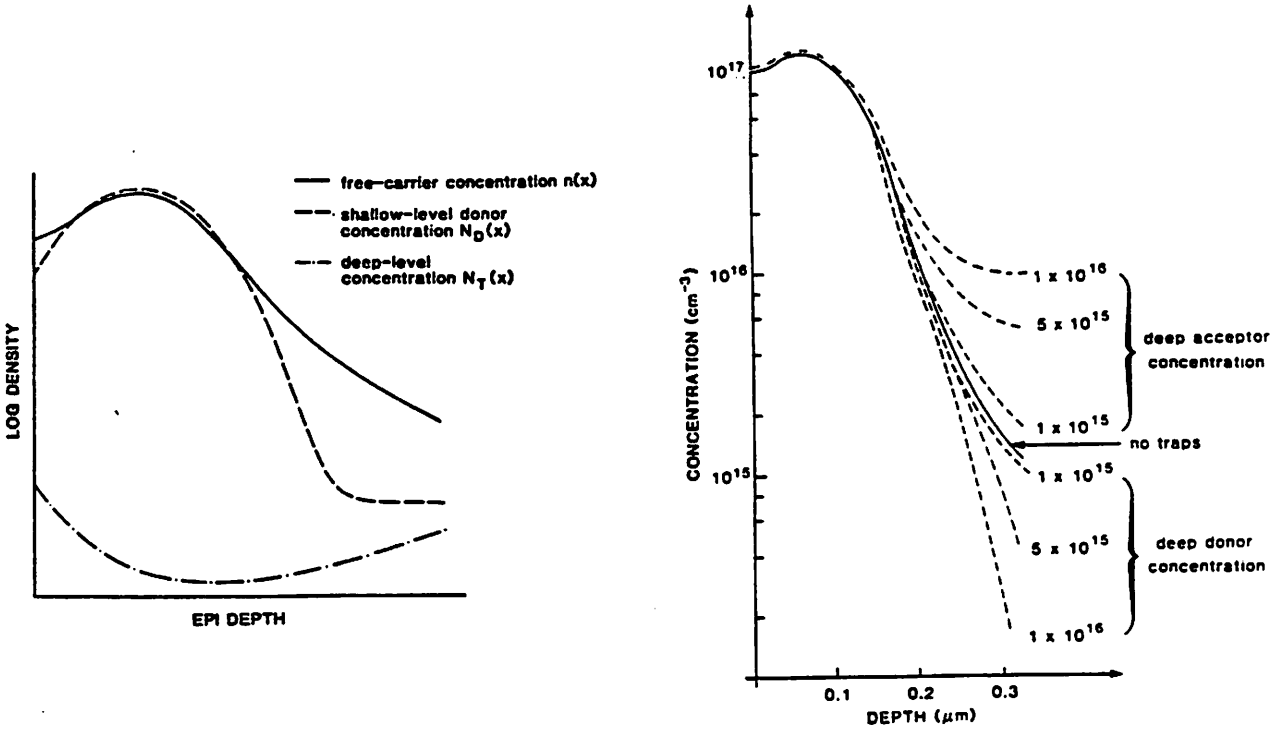
The Hall mobility can be determined if the sample is placed perpendicular to a magnetic field. The change in $R_{AB,CD}$ induced by the field is measured and the Hall mobility given by:

$$\mu_H = \frac{t}{B} \frac{\Delta R_{AB,CD}}{\rho} \tag{2.16}$$

where B is the magnetic induction. This assumes that the contacts are sufficiently small so

that the field is not shorted on the periphery and that the current flux is not disturbed by the field.

In van der Pauw's derivation, the contacts are assumed to have negligible area, and various geometries have been designed to minimize the effect of finite contact area. A common pattern is to use a clover-leaf shaped sample which is suitable for ion implants into SI GaAs since the pattern may either be implant in a geometry like Figure (2.3b) or the whole region implanted and then isolated with a mesa etch. A more popular procedure employs square samples with balls of indium pressed into the corners and sintered. The correction for finite contacts on squares is discussed by Chwang *et al.* [11]



(a) (b)

Figure 2.1 [3] Typical concentration profiles measured using C-V and the influence of deep-levels on the interpretation of the measurement.

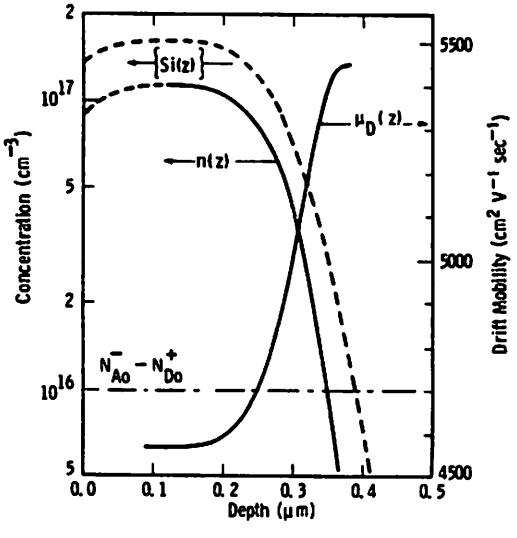


Figure 2.2 [12] Net donor concentration profile for Si implanted into GaAs and the calculated channel mobility assuming good removal of the damage by annealing. The mobility is a function of impurity concentration and is much higher is the bulk.

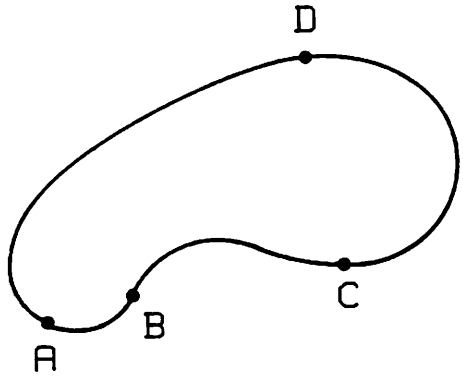


Figure 2.3a A thin arbitrarily shaped solid (lamella) can be used for Hall measurements. Notice that no holes are enclosed. The letter convention corresponds to van der Pauw's notation.

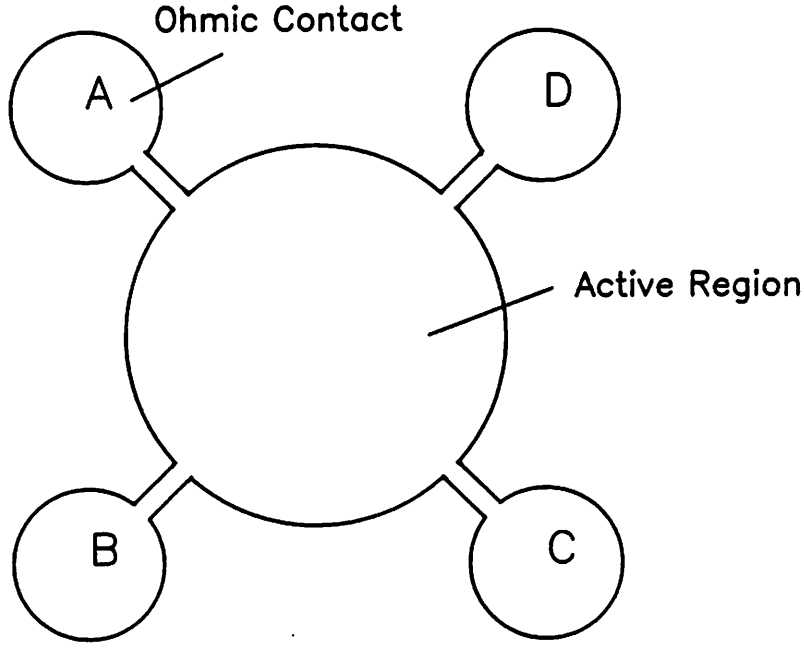


Figure 2.3b Typical geometry that might be used for a Hall measurement. Large areas are provided for ohmic contacts while small area contacts are provided to the periphery of the circle. The structure is either isolated by etching of by selectively implanting.

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III. DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

A. Capacitance DLTS

Deep level transient spectroscopy (DLTS) was initially proposed by Lang[1] in 1974, and it has since become a popular method for studying deep levels and defects in semiconductors. Capacitance transient studies were widely employed to study deep levels prior to DLTS, but Lang was the first to propose a simultaneous temperature ramp. Presently, the fixed temperature capacitance transient methods, are still used if it is necessary to obtain an in-depth understanding of the deep level. In the interrum, there has been a proliferation of related methods which improve on some aspect of Lang's original idea: constant capacitance DLTS;[2] current transient spectroscopy;[3] reverse bias pulsed DLTS;[4, 5] and conductance DLTS.[6] A number of computerized DLTS systems have been reported[7, 8] and Day *et al.* [9] have compared the results from a dual-channel boxcar integrator with that of a lock-in amplifier.

Since the initial proposal of generation-recombination via deep levels by Shockley-Hall-Read (SHR), much work has been directed towards characterizing these centers and their effect on solid state device performance. With DLTS it is possible to determine the energy of the level, capture cross-section, and trap density profile. The performance of an implanted FET is related to the concentration profile and transport characteristics as a function of depth; however, device parameters are complicated by impurity compensation from deep levels. The deep levels act as a source of noise in MESFETs through fluctuation in trap occupancy and free carrier population. This usually is evidenced by excess gate noise.[10] Deep levels also have a tendency to "soften" the pinch-off characteristics of a MESFET. DLTS is suited for rapidly monitoring deep and intermediate levels (> 0.1 eV from band edge) with the sensitivity necessary to make practical studying spectroscopically a large number of traps in a series of samples. On the other hand, photo luminescence [11] in conjunction with Hall measurements is used to study the shallow radiative levels

where the luminescences locates the energy level and the Hall measurement is used to estimate the population.

DLTS may be used to characterize both the minority and majority deep levels in a semiconductor. The measurement is initiated by first filling the trap (voltage pulse, light, etc.) and then monitoring the capacitance transient as the traps emit their occupants (Figure 3.1). If the temperature is slowly scanned, plots of capacitance transient versus temperature can be obtained from which the energy of the traps is determined. In the following discussion, the standard DLTS theory for a Schottky diode on uniformly doped n-type semiconductor will be presented; Lang's original theory will be followed. Unfortunately, only the majority traps can be measured with a Schottky diode since a forward current does not inject minority carriers. The minority traps may also be studied if the sample is illuminated with light of the appropriate wavelength during the filling pulse.[12]

The capacitance transient method makes use of the fact that carrier emission is a thermally stimulated process. Emission from a trap is modeled by SHR theory as:

$$e_i = \frac{1}{\tau} = (\sigma \langle v_i \rangle N_c / g_t) \exp^{-E_t / kT} \tag{3.1}$$

where σ is the carrier capture cross-section; $\langle v_i \rangle$ the mean thermal velocity of the carriers; N_c the conduction band effective density of states; g_t the degeneracy of the trap level; and positive energy is measured from the conduction band to the trap level. Since $\langle v_i \rangle \propto T^{1/2}$ and $N_c \propto T^{3/2}$, e_i may be written as:

$$e_i = \psi \sigma T^2 \exp^{-E_t / kT} \tag{3.2}$$

where ψ is constant with respect to temperature. Taking the natural log of Equation (3.2), results in:

$$\ln \frac{e_i}{T^2} = \frac{-E_t}{kT} + \ln(\psi\sigma). \tag{3.3}$$

If the temperature dependence of σ is neglected, the final term is constant with respect to temperature. The time constant of the trap, which is the reciprocal of the the emission rate, can be conveniently measured with DLTS. After the emission rate has been measured

at several temperatures, an Arrhenius plot of $\ln \frac{e_i}{T^2}$ vs. $\frac{1000}{T}$ can be drawn. The resulting line has a slope of $\frac{-E_t}{k}$ which is the apparent signature of the trap (Figure 3.5, 3.6). This is the result often reported in the literature, but a complete analysis should include the temperature dependence of σ.

The small-signal capacitance of a diode depends on the ionized charge within the depletion region; however, the emission of carriers from traps within this region causes a measurable change in capacitance. For most systems, a reverse bias applied to the diode is the steady state condition (Figure 3.1a). The traps in the space charge region are filled by pulsing the diode towards zero bias. DLTS analysis assumes the pulse is sufficiently long to fill all traps. When the pulse is turned off, the reverse bias raises a portion of the traps within the depletion region above the Fermi level so that they now emit to the conduction band. The emission rate of these traps is assumed to be exponential with time and is dependent on the ambient temperature and on the energy of the trap. Non-exponential decay may also be studied; however, the emission mechanism must be understood before quantifying trap parameters. Since the filled majority traps compensate the ionized space charge, the depletion region is wider and capacitance lower than at steady state. Therefore, as the electrons are emitted the depletion width decreases while the capacitance increases (Figure 3.2).

The DLTS plot is drawn by applying some weighting function to the measured capacitance transient. In Lang's study, the weighting function is a double boxcar integrator which is used to detect the transient and the resulting DLTS plot is a measure of the capacitance at times, t_1 and t_2, after the filling pulse is turned off (Figure 3.3). $C(t_1) - C(t_2)$ is plotted on the y-axis against temperature and as the kT product is increased around the activation energy of a trap, the DLTS plot will exhibit an extremum. For majority traps, $C(t_1) < C(t_2)$, so that a minimum occurs in the DLTS plot while a minority trap is distinguished by a maximum in the plot.

The extremum of the DLTS curve correspond to the condition where the sample transient matches the pre-set rate window (t_1, t_2) and the emission rate derived from this point can be used to make an Arrhenius plot of the trap characteristics. Using Lang's notation, the normalized DLTS signal is defined as:

$$S(T) = \frac{C(t_1) - C(t_2)}{\Delta C(0)} \tag{3.4}$$

where $\Delta C(0)$ is the change in capacitance at $t = 0$ due to the pulse (Figure 3.2). Substituting an exponential capacitance transient into Equation (3.4) results in

$$S(T) = [\exp^{-t_1/\tau} - \exp^{-t_2/\tau}]. \tag{3.5}$$

The time constant at the extremum, τ_m, is found by setting the first derivative of S(T) with respect to τ equal to zero

$$\frac{d}{d\tau}S(T) = 0 = \frac{-1}{\tau_m^2}[t_1\exp^{-t_1/\tau_m} - t_2\exp^{-t_2/\tau_m}]. \tag{3.6}$$

Rearranging terms the desired expression is obtained:

$$\tau_m = \frac{(t_2 - t_1)}{\ln(t_2/t_1)} \tag{3.7}$$

Thus, τ_m is known exactly once the sampling times of the capacitance transient have been selected. The temperature at which the peak occurs is the only other data required to draw the Arrhenius plot. This can be measured from the plot or with a software peak detector. The plotted results are compared with published data and plots of $\tau_m T^2$ vs. $\frac{1000}{T}$ (GaAs[13] and Si[14]).

In the previous paragraph it was shown that a quick DLTS scan can be used to locate the traps within the energy gap. When making a DLTS measurement, it is important that the temperature ramp rate is slow so that the recorded temperature reflects the actual sample conditions. A quick ramp would shift the peaks and might influence the shape of the transient. Trap concentration, N_t, can be obtained by measuring the pulsed capacitance difference. Since the trap filling pulse creates a non-equilibrium condition, the magnitude of the capacitance change, ΔC, reflects the magnitude of N_t and can be used to calculate the

trap concentration. The equation for capacitance of a Schottky diode on uniformly doped semiconductor is:

$$C = \left\{ \frac{q\epsilon_s N}{2(V_{bi} - V)} \right\}^{1/2} \tag{3.8}$$

where $N = N_D - N_A - N_t$ and for uniform doping and trap concentration

$$\frac{\Delta C}{C} = \frac{C(t=0) - C(t=\infty)}{C(t=\infty)} = \frac{N_t}{2(N_D - N_A)} \tag{3.9}$$

where $C(t=\infty)$ is attained when the trap population has returned to equilibrium. The value of N_t obtained is only approximate since the traps near the metal-semiconductor interface are never below the Fermi level; and therefore, never filled while the traps along the depletion edge are always below the Fermi level and thus always filled. It was previously assumed that the trap concentration is constant throughout the depletion region; however, this may not be true. The trap concentration may be roughly profiled by varying the filling pulse height for a fixed quiescent reverse bias.[15] Using the values of e_i and E_t measured, and a knowledge of N_c, $\langle v \rangle$, and g an apparent capture cross-section may be calculated from Equation (3.1). For a more complete solution, the temperature dependence of σ is included. The capture cross-section is then determined by measuring the peak transient height as a function of trap filling pulse width. The change in DLTS signal due to the partially filled traps is:

$$\Delta S(t_f) = \Delta C_{max}(t=0)[1 - \exp^{-t_f/\tau_c}] \tag{3.10}$$

where t_f designates the time length of the filling pulse and τ_c, the capture time constant, is:

$$c_n = \frac{1}{\tau_c} = n\langle v \rangle \sigma \tag{3.11}$$

where n is the free carrier concentration. Conventional emission DLTS assumes $t_f \gg \tau_c$; thus, all the traps are filled.

With Schottky barriers on ion implanted SI GaAs, both large leakage currents and large series resistances have affected C-V measurements. Likewise, it would be expected that this is be the same case with DLTS measurements which are also high frequency C-V measurements. Day *et al.*[16] have proposed a method to measure leaky diodes employing a

capacitance bridge and using the test diode along with a "dummy" diode of similar characteristics. Usually the sample impedance in a DLTS measurement is assumed to be purely capacitance, but it has been shown by Broniatowski *et al.*[17] that the resistance in series with the diode can strongly reduce and even reverse the sign of the DLTS signal which would result in confusion between a majority and minority trap. The type of gate metal used and preparation techniques have been shown to also affect the DLTS measured signal. Yahata and Nakajima[18] report this for Al and Au diodes on n-GaAs.

B. Example of DLTS Analysis

A SPC Electronics Corp. 17060D DLTS system was available during the first part of this research, and a number of Schottky diodes on silicon were measured. The DLTS measurement and analysis technique is described here using a diode on gold doped silicon ($N_D = 1x10^{16}\ cm^{-3}$). The 17060D uses a square wave weighting function[19] rather than the double boxcar integrator approach of Lang. The capacitance transient is shifted by the delay time t_d , multiplied by the square wave in Figure (3.2c), and averaged over the period, $2t_s$.

$$S(T) = \frac{\Delta C(t=0)}{2t_s}\left\{\int_{t_d}^{t_s+t_d}[\exp^{-t/\tau}]dt - \int_{t_s+t_d}^{2t_s+t_d}[\exp^{-t/\tau}]dt\right\} \tag{3.12}$$

$$S(T) = \frac{-2\Delta C}{t_s/\tau}\exp\left[\frac{-t_d}{\tau}\right]\left\{1-\exp\left[-t_s/\tau\right]\right\}^2. \tag{3.13}$$

τ can be maximized in Equation (3.13) in a similar manner as in Equation (3.7) to obtain:

$$\exp^{t_s/\tau_m} = \frac{1+\frac{t_d+2t_s}{\tau_m}}{1+\frac{t_d}{\tau_m}} \tag{3.14a}$$

which reduces to

$$\exp^{t_s/\tau_m} = 1+\frac{2t_s}{\tau_m} \tag{3.14b}$$

for $t_d=0$. However, due to the switching transient, t_d should not be set to zero since the

transient would be incorporated into S. Many high speed sampling DLTS systems must also gate off the capacitance meter in this region to avoid overloading from the transient.[20]

Since t_s and t_d are known τ_m can be found iteratively and the Arrhenius plot drawn using the measured peak temperatures. Below are tables of measured peak temperatures and values of S for the peaks occurring around 160°K and 260°K in Figure (3.5). The steady state capacitance as a function of temperature is plotted in Figure (3.4). ΔC and N_t were calculated using Equations (3.13) and (3.9) respectively.

t_d=4ms

Table 3.1a: Measured Data - Trap #1

t_s (ms)	Peak Temp. (°K)	DLTS Signal: S(T) (fF)	C(t=∞) (pF)
16	170.72	105	43.0
32	166.73	109.2	41.4
64	161.58	112.3	38.8
128	155.93	120	36.2
256	151.33	130	34.4

Table 3.1b: Calculated Data - Trap #1

t_s (ms)	τ_m (ms)	$\tau_m T^2$ ($^\circ K^2$ s)	ΔC (fF)	N_t (10^{13} cm^{-3})
16	17.610	513.25	168	7.81
32	30.505	848.01	154.7	7.54
64	56.084	1464.2	148.6	7.66
128	107.09	2603.8	153.1	8.46
256	209.00	4786.3	162.7	9.46

The above peak data is plotted in Figure (3.6a) and the trap energy calculate at E_t = 0.25 eV. The DLTS software package calculated $N_t = 3.37 \times 10^{14}$ cm^{-3}. The larger value is expected since Equation (3.9) includes the entire depletion region in the calculation of N_t; however, only a portion of the depletion region contributes to the DLTS signal during a complete DLTS scan as is shown in Figure (3.1). Consequently, the value calculated here for N_t is $\frac{Q'}{W}$ rather than $\frac{Q'}{\Delta x}$. Q' is the number of traps/area contributing to the measured DLTS signal, W is the steady state depletion width, and Δx the actual region which contributes to the signal through trap filling and emptying (Note: $W > \Delta x$, in this case $W \simeq 4\Delta x$).

Table 3.2a: Measured Data - Trap #2

t_s (ms)	Peak Temp. (°K)	DLTS Signal: S(T) (fF)	C(t=∞) (pF)
16	271.26	18.0	54.6
32	264.98	19.8	54.5
64	258.94	21.01	54.2
128	253.03	21.7	53.8
256	247.04	22.0	53.8

Table 3.2b: Calculated Data - Trap #2

t_s (ms)	τ_m (ms)	$\tau_m T^2$ ($°K^2$ s)	ΔC (fF)	N_t (10^{13} cm^{-3})
16	17.610	1295.8	28.8	1.05
32	30.505	2141.9	28.05	1.03
64	56.084	3760.4	27.8	1.03
128	107.09	6856.3	27.68	1.03
256	209.00	12755	27.53	1.02

The above peak data is plotted in Figure (3.6b) and the trap energy calculated at E_t = 0.549 eV. Au electron trap levels have been reported at 0.55 eV and 0.24 eV. [14] The value for N_t calculated by the computer for trap #2 is 5.24×10^{13} cm^{-3}. The steady state capacitance curve in Figure (3.4) varies markedly over the temperature scan range such that the depletion region decreases by a factor of 2. This must be considered when profiling an implant. To remove this complication constant capacitance DLTS (CCDLTS) is used. This technique keeps the depletion width constant through out the scan by maintaining the steady state capacitance constant with a feedback loop which adjusts the reverse bias.

C. CONDUCTANCE DLTS (CDLTS)

The information obtained with conductance DLTS is potentially more applicable since test MESFETs and final devices are fabricated simultaneously and tested at the completion of the process; therefore, the process will influence the parameters of all devices which improves the correlation of the defect data to the MESFET and IC characteristics. Conduction DLTS simplifies the measurement of ion implanted material though the processing complexity is greatly increased over conventional DLTS. Capacitance DLTS analysis assumes the series resistance in the Schottky diode device is negligible; however, Broniatowski *et al.* [17] claims that the series resistance can make DLTS data incomprehensible. For Schottky diodes on ion implanted SI GaAs, the series resistance of a device increases considerably with increasing reverse bias which depletes into the tail of the implant. With ion implanted materials the tail of the implant is of great interest since a large portion of the damage is in this region. An adequate knowledge of the traps in the tail region of the implant is necessary to determine the pinch-off characteristics of the MESFET. CDLTS is not affected by diode series resistance; therefore, it is useful in monitoring traps in the implant tail. Capacitance measurements also are not suitable for real devices since the capacitance of an average gate is to small (1 < pF) to be able to monitor precisely the transients introduced by the traps.

The conductance technique is implemented to observe deep levels in the channel, at the substrate/channel interface and also at the semiconductor surface.[10] Electron traps in the channel introduce excess microwave noise, while traps at the channel/substrate interface introduce a backgating effect.[10] The backgating effect arises from negative charge accumulating on the traps on the substrate side of the channel/substrate interface which produces a positive space charge region that extends into the channel. Surface states, especially if not passivated, result in gate leakage. CDLTS was first suggested by Collet [21] for use on CCDs and by Adlerstein[6] for GaAs MESFET applications and the analysis refined for MESFETs by Golio.[22, 23]

I_{DS}, the drain to source current, is the measured parameter in conductance DLTS. This current is modulated by holding the gate at some bias such that the channel is nearly depleted and then momentarily pulsing the gate towards shallow depletion (ie. near to 0 V) to fill the traps. After the gate pulse is switched off, the depletion region will be slightly deeper than at steady state since the filled traps compensate some of the ionized donors in the space charge region (it is also possible to deplete deeper using an emission pulse or to monitor the channel/substrate interface by using a substrate bias). This mechanism is the same as that of capacitance DLTS and the depletion depth will return to its equilibrium value after some time. If now a small bias, V_{DS}, is applied between the drain and source, modulation of the current, I_{DS}, can be observed (Figure 3.7 and 3.8). It is important to keep V_{DS} small since grading of the depletion edge with a large drain bias will complicate a calculation of the trap profile.

A long channel device operating in the linear region will be analyzed with an abrupt depletion edge assumed. To obtain meaningful values for trap concentration, the steady state depletion width should be kept constant throughout an entire temperature scan. This may be accomplished by using a feedback loop such that the gate voltage is adjusted to maintain constant capacitance in a similar way as constant capacitance DLTS (CCDLTS) is configured. Alternatively, if the effects of deep levels is neglected, the free carrier profile and mobility data as a function of depth and temperature can be used to maintain a constant channel width. I_{DS} can then be calculated as a function of temperature for a fixed channel width, and then the gate bias adjusted to maintain I_{DS}. A further simplification also neglects the temperature dependence of the carrier concentration; then I_{DS} as a function of temperature can be determined.

The analysis of the trap energy proceeds in much the same fashion as with conventional DLTS. The contact and bulk resistance of the source and drain should first be removed from the data; this is necessary since the voltage drop across these parasitics will vary with the current transient. The remainder of this discussion will assume that the

data has been corrected for these parasitics.

$$I = gV = g(V_{applied} - V_{contact} - V_{source} - V_{drain}) \tag{3.15}$$

The conductance of the channel is

$$g(T) = \frac{qZ}{L}\int_a^W \mu_o(x,T)n(x,T)\,dx \tag{3.16}$$

where Z is the gate width, a the depth of the channel/substrate interface, W the depletion edge, and $\mu_o(x,T)$ the mobility which varies in x according to the doping profile, N, not the free carrier profile, n. Following the same analysis as Lang and using a box-car integrator, the CDLTS signal is

$$S = g(t_1) - g(t_2) \tag{3.17}$$

$$= \frac{qZ}{L}\left\{\int_a^{W(t_1)} \mu_o(x)n(x)\,dx - \int_a^{W(t_2)} \mu_o(x)n(x)\,dx\right\} \tag{3.18}$$

$$= \frac{qZ}{L}\int_{W(t_2)}^{W(t_1)} \mu_o(x)n(x)\,dx \tag{3.19}$$

To determine the energy location of the deep levels no further information is needed if the mobility in the region $W(t_1)$ to $W(t_2)$ is assumed constant. In general, some error will be introduced since the mobility is quite sensitive to impurity concentration (Figure 2.2).

$$S = \frac{qZ}{L}\mu_o n_{to}\left\{\exp^{-t_1/\tau} - \exp^{-t_2/\tau}\right\} \tag{3.20}$$

where n_{to} is the maximum number of occupied traps at $t = 0$. This can be maximized with respect to τ as previously done in Equations (3.4) to (3.7) with the maximum signal occurring at

$$\tau_m = \frac{t_2 - t_1}{\ln \frac{t_2}{t_1}} \tag{3.7}$$

If one point on the transient curve is taken and a value for μ_o assumed, an order of magnitude estimate of n_{to} can be made.

The previous description is only a first order CDLTS analysis. A more rigorous solution requires a knowledge of the free carrier profile, trap profile, doping profile, relationship between doping and mobility, and finally the temperature dependence of all four.

Since the trap profile is unknown, it's influence has to be neglected. This may be checked later but the nature of the analysis minimizes the trap influence except in the region $W(t_1)$ to $W(t_2)$. The dopants may be assumed to be totally ionized so that the doping profile is independent of temperature. If deep level compensation of the free carriers is neglected, the free carrier concentration becomes temperature insensitive (except at extreme temperatures) so that the profile can be obtained with a low frequency C-V analysis described in Section II.B. Since the C-V analysis of ion implanted SI GaAs is questionable in the tail, a Gaussian may be fitted or another standard profile. Then the mobility profile can be calculated. The analysis proceeds from Equation (3.19) and is only simplied if relations for μ_o and n are known.

The previous analysis has assumed that the mobility can be determined and an equation for the temperature dependence is known. However, when compared against the data plotted in Figure (3.4), the assumption of free carrier insensitivity to temperature becomes invalid. Over the range plotted, the capacitance changes by a factor of 2 which represents a factor of 4 change in doping concentration. Likewise, in a complicated case such as incomplete annealing of the implant damage, theoretical equations may not accurately describes the relation of mobility as a function of depth and temperature. Consequently, a more practical system would define all parameters empirically. This system would use constant capacitance feedback to adjust the steady state reverse bias to maintain the edge of the depletion region at the same depth. The constant depletion width would simplify analysis and provide spatial profiling capabilities. The doping and mobility profiles would be generated at various temperatures and the curves interpolated through out the measurement range. These interpolations would then be compared to the measured steady state source/drain current, I_{DS}, as a function of temperature. A practical implementation would be to collect the empirical parameters on the temperature ramp down which in some systems requires as much time as the heating cycle. The measured CDLTS signal could then be corrected so that the exponential decay of the traps is recorded which would simplify the

analysis to that of the previous DLTS discussion.

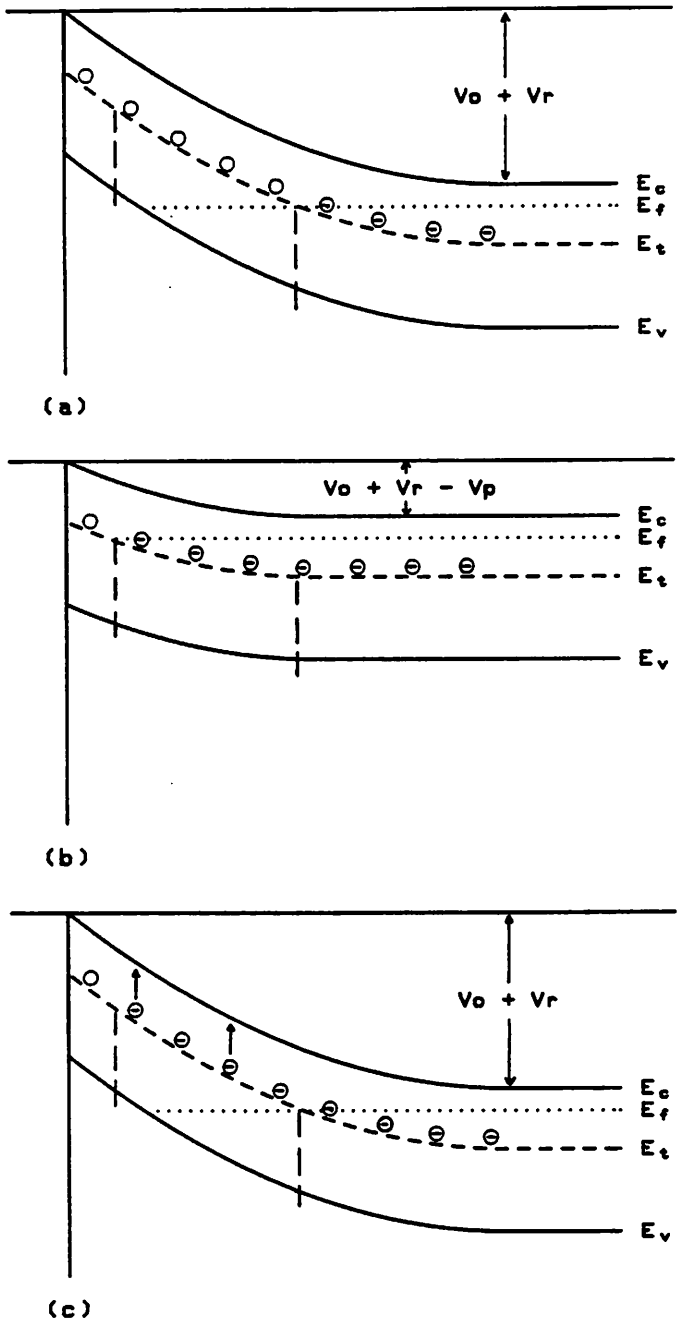

Figure 3.1 The trap filling and emission is depicted. At quiescent reverse bias (a) all traps above the Fermi level are empty. The Fermi level is then raised (b) and a portion of the traps fall below the Fermi level and capture electrons. The pulse is switched off; however, a non-equilibrium condition exists with filled traps above the Fermi level (c). These traps emit at a characteristic time constant, τ, which is a function of temperature and trap energy.

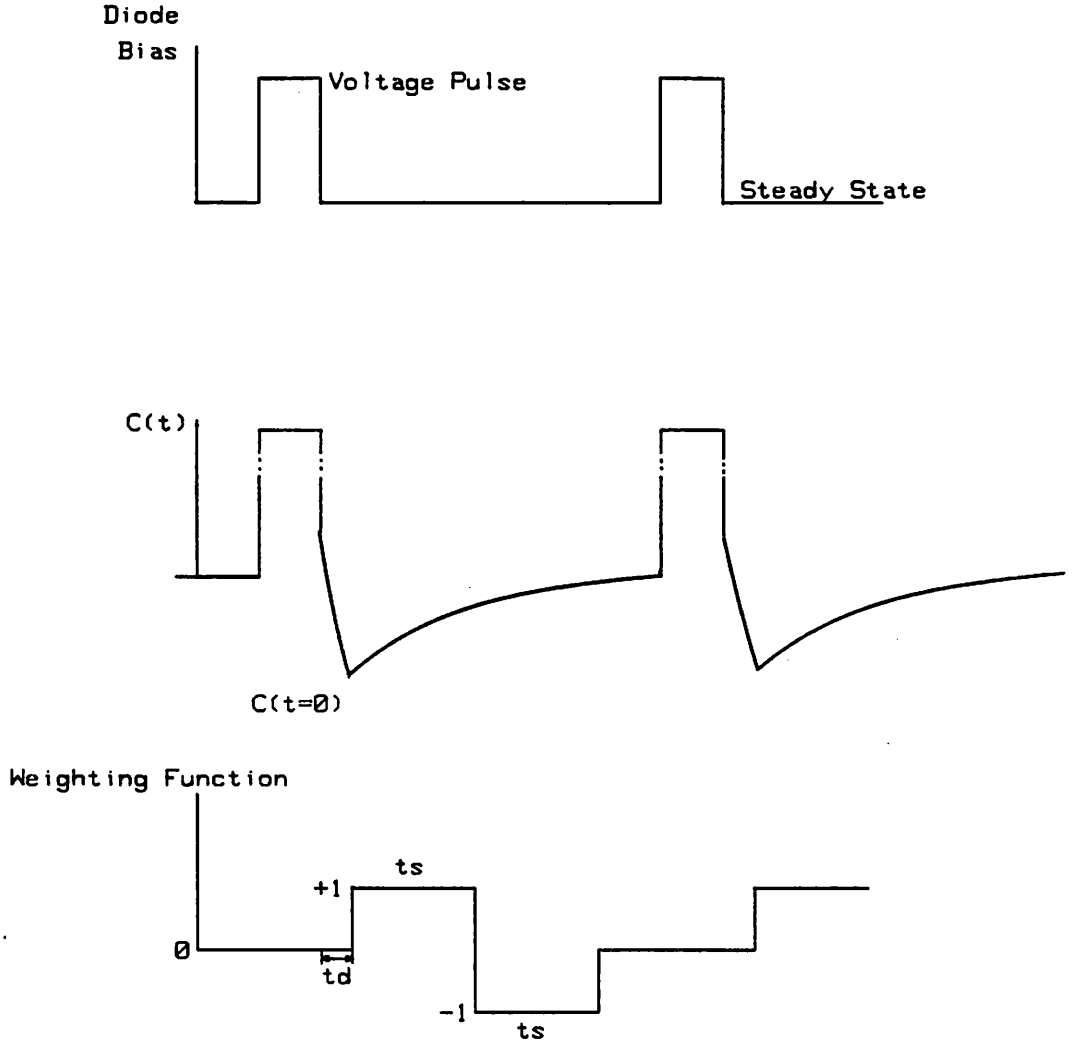

Figure 3.2 The diode biasing condition (a) and measured capacitance as a function of time (b). In the SPC 17060D a square wave weighting function (c) is applied to the capacitance signal to obtain a DLTS signal.

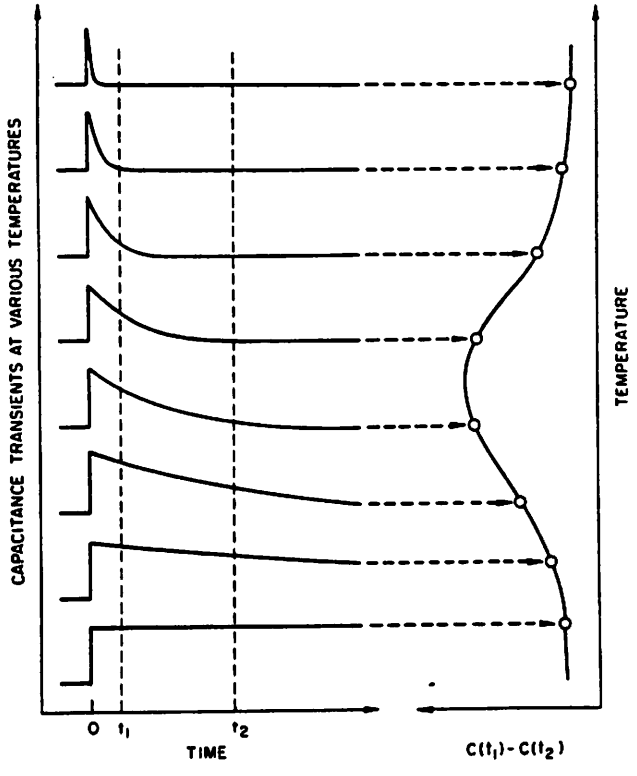

Figure 3.3 The DLTS signal (on the right) is obtained by applying a double boxcar weighting function to the capacitance transient.

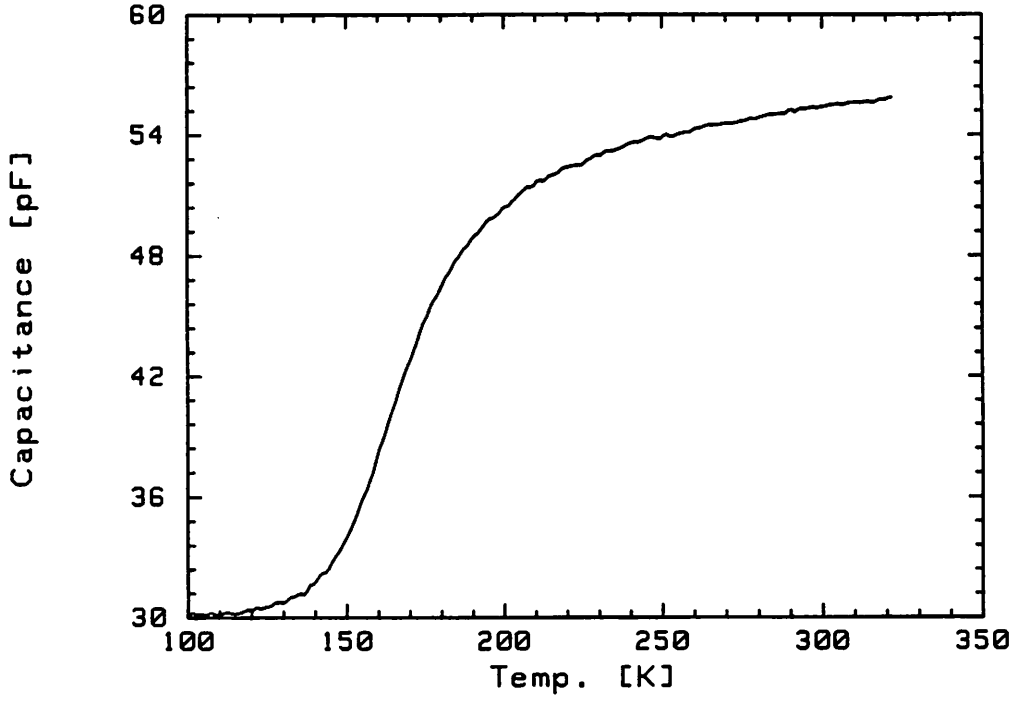

Figure 3.4 Steady state capacitance of measured diode as a function of temperature.

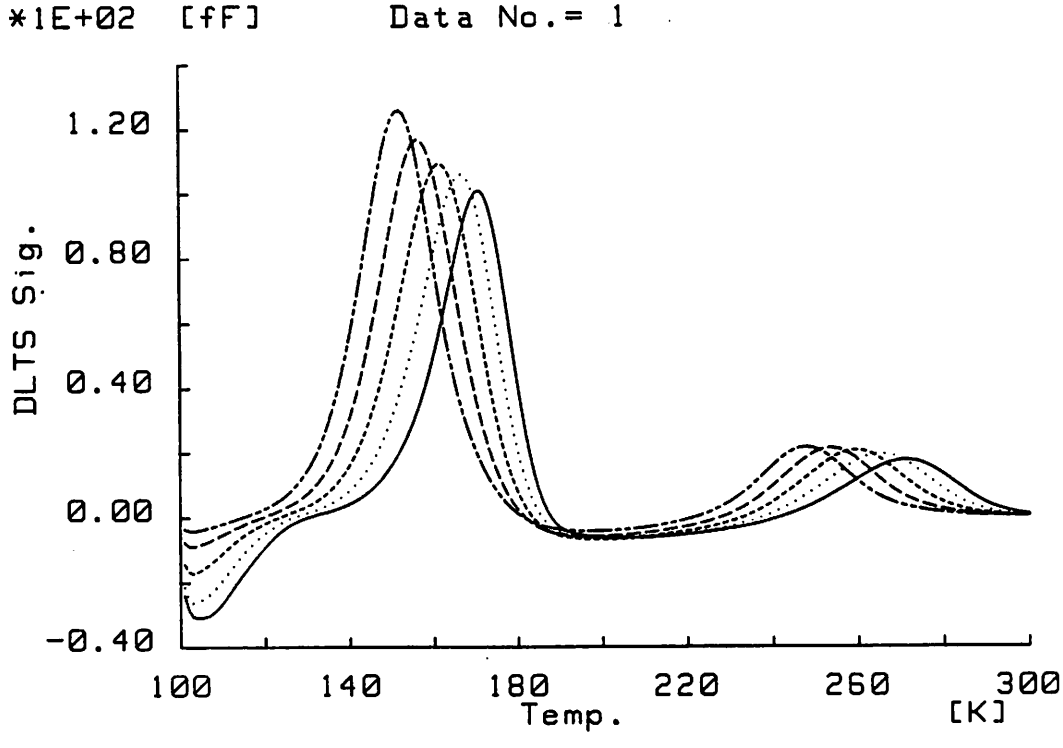

Figure 3.5a The DLTS signal for a Au doped Si sample measured with an SPC 17060D system. The system inverts the peak so that the two maximums represent majority traps. The sampling window increases for the curves having extrema at lower temperatures.

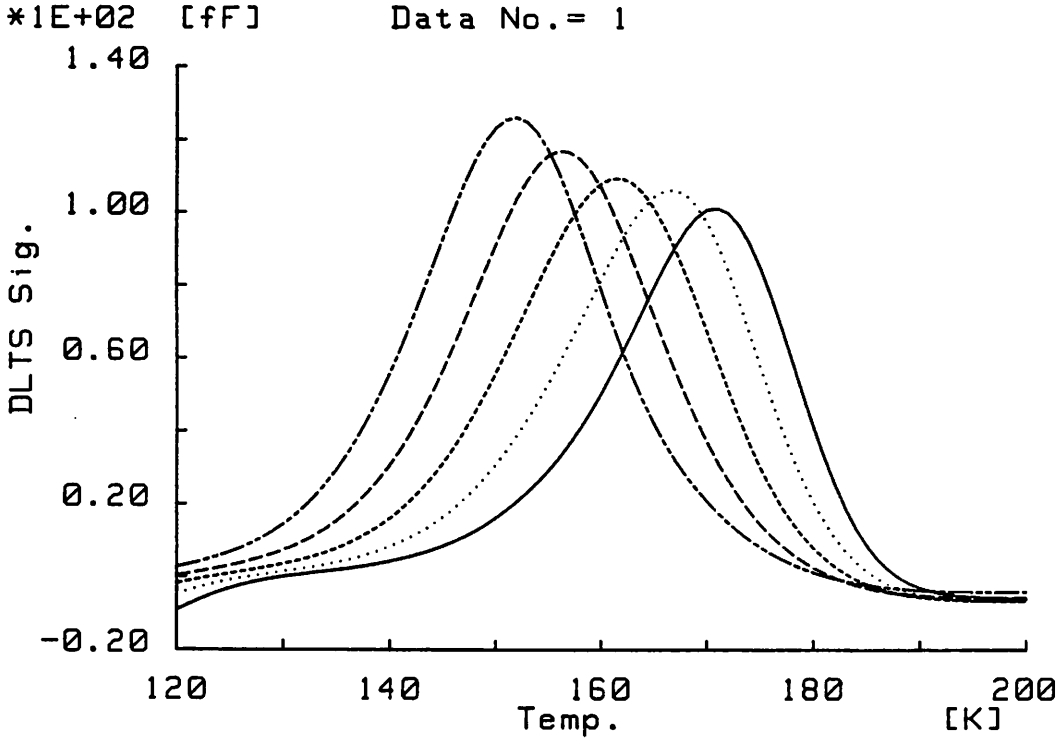

Figure 3.5b Magnification of DLTS signal in Figure (3.5a). The sampling window increases for the curves having extrema at lower temperatures.

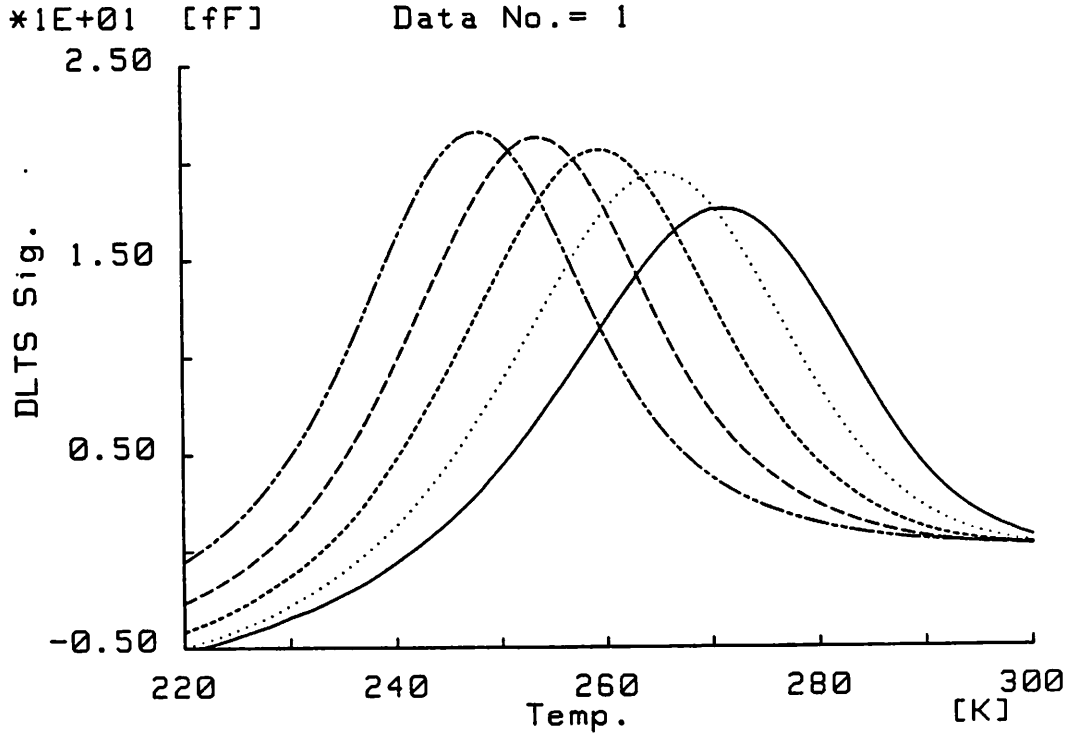

Figure 3.5c Magnification of DLTS signal in Figure (3.5a).

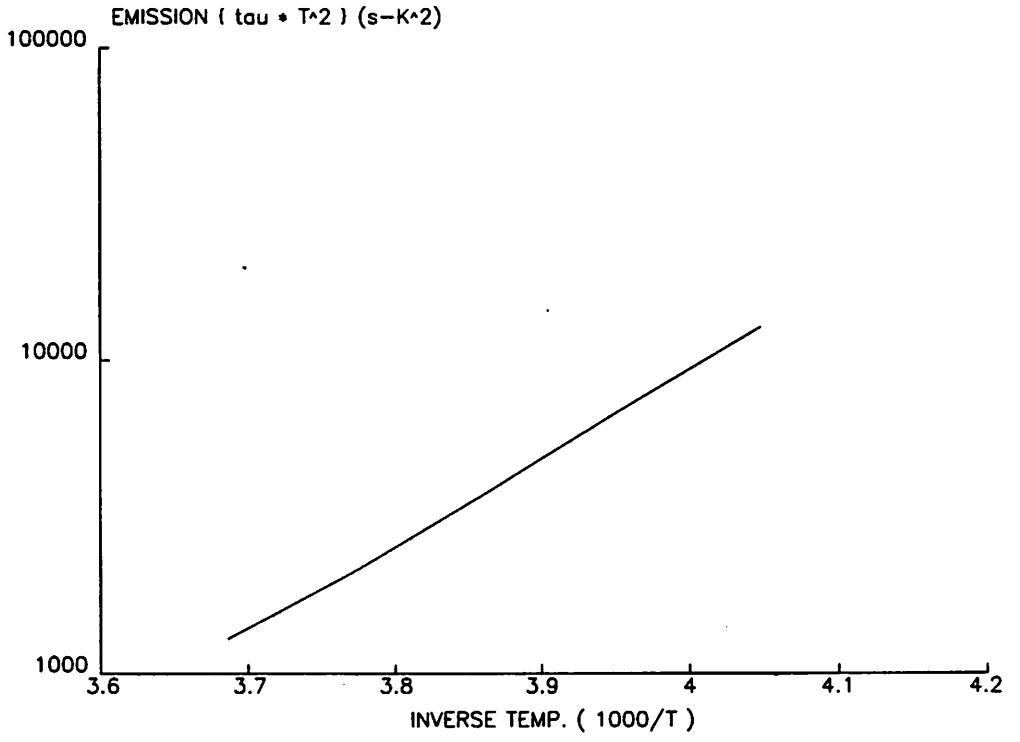

Figure 3.6a Arrhenius plot constructed from the curves in Figure (3.5a). The activation energy of this trap is E_t = 0.25 eV.

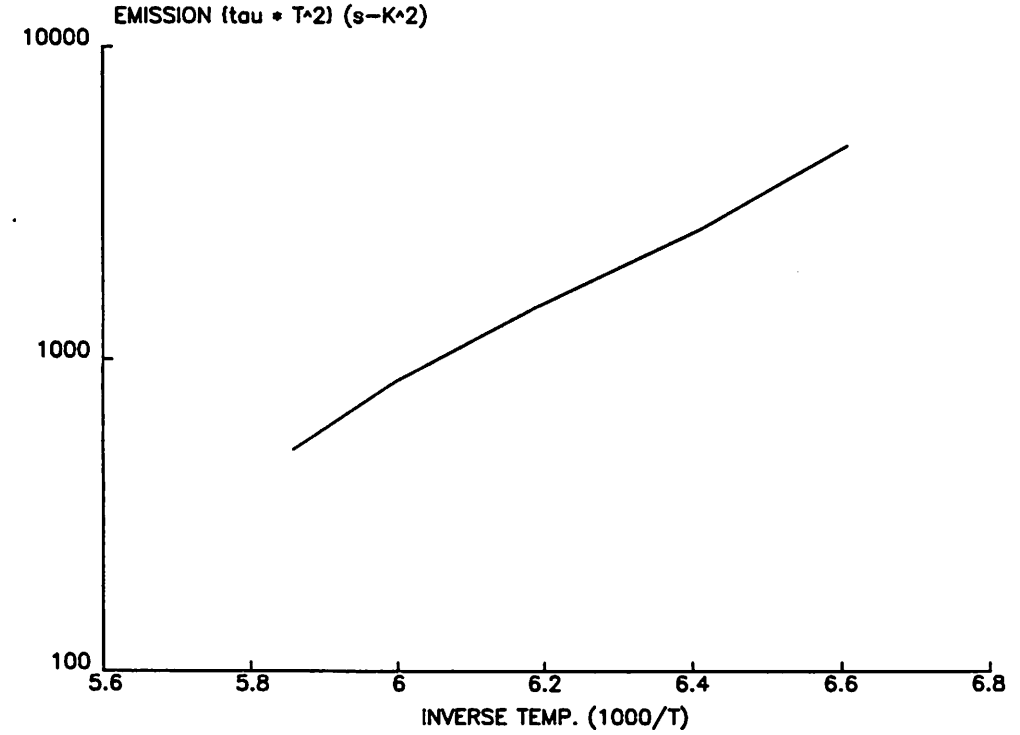

Figure 3.6b Arrhenius plot constructed from the curves in Figure (3.5a). The activation energy of this trap is E_t = 0.549 eV.

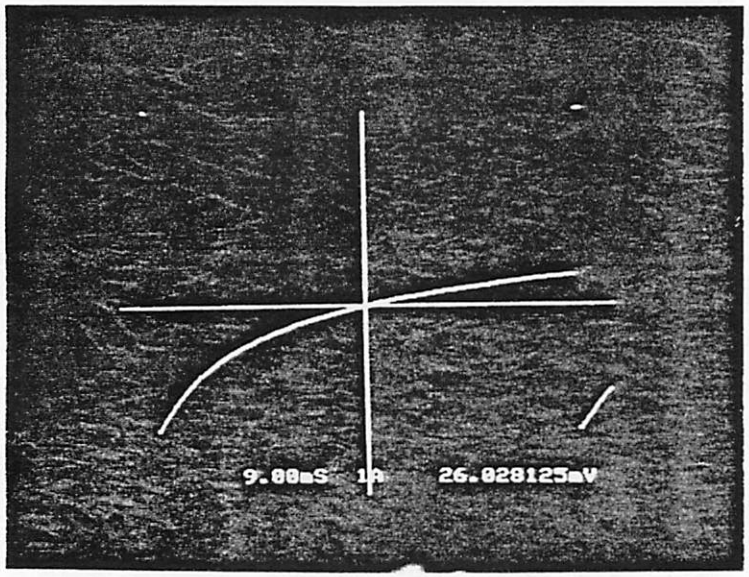

Figure 3.7 A typical conductance DLTS transient measured on a commercial MESFET at Xerox PARC.

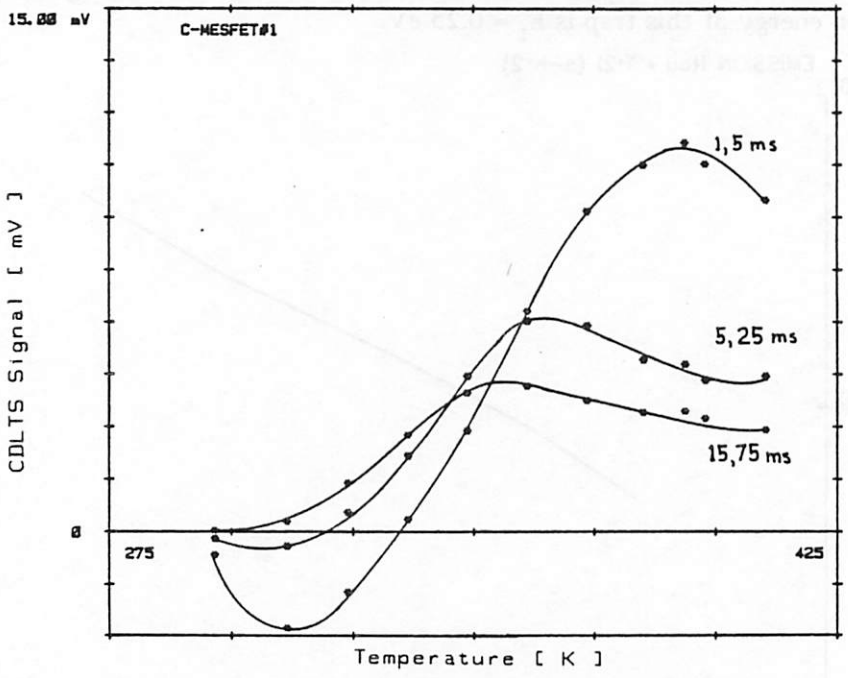

Figure 3.8 CDLTS plot ($I_{DS}(t_1) - I_{DS}(t_2)$) for the same device which generated the signal in Figure (3.7). The current was kept constant over the temperature scan in an attempt to maintain the same depletion depth.

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IV. PROCESSING

Simplified processes are used to fabricate the four devices in this research. Initially process parameters are drawn from the author's experience at IBM Yorktown and Van Tuyl *et al.* [1] though Willardson and Beer[2] is also a good reference. Adjustments were made to the standard process to accommodate the different device requirements. The most widely used device was a single-level metalization on GaAs where rings of metal are lifted off to form diode/capacitors. The second structure is a modification of the previous structure in that Au/Ge is used for the ohmic contact. The last two devices are MESFETs which were used for conductance DLTS. In many portion of the process the steps are characterized to a level necessary for meaningful results; however, the parameters are for the most part not optimized so that the process specifications are given only as a guide. The major components of the process are: cleaning; ion implantation; annealing; photolithography; and metalization.

A. Cleaning

Cleaning of GaAs involves more than removing contaminants and particulates. it is also necessary to perform a chemical etch of the surface to remove polishing damage. Standard etches, which oxidize the Ga and then etch the oxide, are usually used to remove 1 μm of the surface. Scribing of samples requires special attention because the particles produced have a high affinity for the surface. To minimize the particles generated, the wafer is turned face down on a new lint-free cloth and cleaved with care taken not to slide the face of the GaAs on to the generated particles. It was found that the best method for wafer cleaving uses a very fine tip scribe to notch a front edge and then the sample is cleaved by pressing on the back in the vicinity of the scribe.

The standard degreasing procedure is:

10 minutes in 60 °C TCA
Rinse with Acetone
5 minutes in boiling Acetone
Rinse with Methanol
2 minutes hot Methanol
Rinse in room temperature DI
Blow dry with N_2

A mechanical scrub of the wafer surface may be required; this entails using an ultrasonic to remove particulates. A Q-tip can be used to remove gross contaminates followed by 10 seconds in ultrasonic acetone to remove particles and lint. Sub-wafer size samples are easily broken in an ultrasonic clean; therefore, care should be exercised. A low ultrasonic speed should be used and the beaker containing acetone and the sample held off the bottom of the tank. The ultrasonic is the only method to remove some particles such as those generated when scribing.

Two chemical mixtures were tested for etching the surface. The combination of $NH_4OH:H_2O_2:H_2O$ is found to produced no pitting but the surface is rough and plane boundaries are visible (a 1:1:5 mixture was tried). The etch which is standard through much of the research is a 1:1:5 mixture of $H_2SO_4:H_2O_2:H_2O$. This mixture is exothermic so the etch rate is controlled by the temperature at which the etching is performed. The etch is usually cooled to less than 10°C for processes which have stringent surface morphology requirements, such as MBE or MOCVD. The etch rate is also dependent on the concentration of H_2O_2 which oxidizes the GaAs with the resulting oxide removed by the acid. In this research the solution is allowed to cool to 65°C before the sample is introduced into the etchant. At this temperature the etch rate is about 1 μm/min. The surface is generally very good except for some pitting near the edges and occasional surface waviness due to uneven flow of the etchant. An important consideration when etching is the ability to quench the reaction repeatably and uniformly. Running water directly into the beaker is often used for quenching; however, this is probably also the cause of the surface unevenness since the reaction could not be quenched uniformly and the sample is subjected

to flowing solution which would tend to etch faster than a stagnant etchant. The other difficulty with using H_2SO_4 is that it tends to stick to all surfaces so care must be taken to rinse thoroughly before exposing to air.

A more meticulous etching process, that may be used with good results, is to dip the sample into H_2SO_4 before and after the etch. The initial dip into H_2SO_4 removes the H_2O from the surface of the GaAs so that the etch can proceed uniformly. The sample with a film of H_2SO_4 is then immediately put into the etch. After etching the sample is removed from the etchant and put into H_2SO_4 where the reaction is quenched. It is important that the surface of the sample is covered with etchant when removed and put into the H_2SO_4 . The H_2SO_4 is then diluted with running DI water. Alternatively, rather than removing the sample from the etchant, H_2SO_4 can be poured directly into the center of the beaker to quench the reaction and then the beaker placed under running DI water. For best results, the beaker should contain only a small quantity of etchant so that the H_2SO_4 can significantly dilute the etch. This approach also tends to minimize the native oxide thickness since the H_2SO_4 dilutes the oxidizer, H_2O_2.

Usually before putting down the encapsulant the sample is degreased and the native oxide removed. A dip in pure HCl for 20 seconds is used to remove the oxide. The remaining oxide thickness is then measured with an ellipsometer. Before metalization an HCl dip is also used to improve interface quality. On one occasion the sample was not blown dry after the degrease, but rather, put straight into HCl from the DI rinse: the oxide measured with an ellipsometer was 30Å thicker than the normal post-etch measured thickness of 20 to 30Å.

B. Ion Implantation

For large scale circuit integration, it is important to have good control of the channel doping of each FET. The diffusion coefficient of n-type dopants in GaAs is quite low which necessitates diffusion at high temperatures. This tends to badly degrade the substrate due

to decomposition; consequently, ion implantation is an attractive technique for highly controlled profiles, and correspondingly, uniform FET characteristics across the wafer. In the survey paper by Stephens,[3] it is reported that the final electrical activation of the dopant is higher if the substrate temperature is held at a few hundred degrees Celsius during implantation. The majority of the research in this report deals with the implant. Since GaAs is expensive, samples sizes of 1 cm^2 to quarter wafers were implanted. The average implanter takes 2" or 4" wafers; thus, these small samples must be glued down in the implanter. Indium is often used or the samples may be affixed to Si wafers which also serve as rigid carriers. Photoresist was used to affix the GaAs to 2" Si wafer (described in photolithography section); however, some types of black wax or epoxy which can withstand elevated temperatures, do not attack or dope the GaAs, and are dissolved readily in a solvent may be preferred since the resist can get on to the face of the sample when cleaning. Epoxies do exist with no cure agent which might be suitable. They become soft at about 150 to 200°C which is above most processing temperatures.

The parameters for the implants during most of this research are: 8° off axis, 120keV, Si^{29}, and a low current so as not to carbonize the resist. Si^{29} is chosen since it is attainable in the lab and does not contaminate silicon VLSI processes. It is necessary to choose mass 29 since both N_2 and CO are difficult to separate from the Si^{28} line; however, the maximum donor concentration attainable is limited because Si is an amphoteric dopant. Also, to be considered when selecting a dopant is the crystal damage introduced and the final activation attainable. Damage increases with ion mass so low mass ions are preferred. Dosage is one of the variables studied; generally, three values are used. The projected range for 120 keV implants is 1025Å and the standard deviation 510Å (Gibbons[4]). The sheet resistance is calculated below using $R_s = \frac{1}{n_s q \mu}$ assuming a constant mobility of 1000 $cm^2/V\text{-}s$ and 100% activation. Complete activation, however, is not usually realized because it is a function of implant dosage. Lower dose implants tend to activate better since the maximum donor concentration obtained with annealing is approximately

1×10^{18} cm^{-3}. Thus, the relation between between resistivity and implant dosage weakens for higher dosages.

Dosage cm^{-2}	Peak Concentration cm^{-3}	Sheet Resistance Ω
1E12	8.2E16	6241
1E13	8.2E17	624.1
1E14	8.2E18	62.41

C. Annealing

Annealing of implant damage in GaAs has received considerable attention because it is both the least understood and least controllable process. Due to the volatility of As, whose partial pressure is much higher at annealing temperatures than that of Ga, precautions must be taken to prevent crystal decomposition. The maximum carrier concentration attainable with ion implantation is lower than material intentionally doped during growth. The activation of amphoteric dopants like Si is limited since high anneal temperatures result in a loss of As which causes the dopant to go onto the As acceptor sites and compensate the donor concentration. In order to restrict the dopant from going onto the As acceptor sites an As implantation may be added.[5] The initial criterion in selecting a substrate is that the bulk resistance of the SI GaAs remains stable during annealing. With Cr doped substrates the resistivity may decrease during annealing due to re-distribution of the Cr atoms which may cause the device leakage current to becomes unacceptable. Generally, a better recovery of the crystallinity, higher electrical activation, and shorter anneal time is obtained with higher anneal temperatures; however, the likelihood of surface degradation due to As out-diffusion is also increased.

Furnace annealing has been the most popular method with both encapsulated and bare surface techniques used in combination with a variety of ambient gases. The limitations of capped annealing arise from stress induced redistribution of deep levels. There is also some diffusion of Ga and As into the cap while oxygen may diffuse from the encapsulating layer into the substrate and form a mid-gap level. The integrity of the cap is important since As may diffuse along the grain boundaries and voids. Thomas *et al.* [2] specifies that a good encapsulation is achieved with Si_3N_4 when the refractive index is between 1.91 and 1.96. When annealing in a H_2 ambient, Hughes and Li[6] observed a p-type thermal conversion near the GaAs surface due to a decrease in electrically active EL_2. Capless annealing necessitates placing the sample in an As ambient where the As overpressure prevents the surface from decomposing. Ordinarily this is accomplished by flowing As through the furnace which results in the hazards of gaseous compounds of As. Alternatively, proximity capping may be used where the sample is placed face down on a virgin GaAs wafer. A new method suggests using a partially enclosed crucible with GaAs powder supplying the ambient overpressure.[7]

Laser annealing exhibits good activation but the activation is not thermally stable. A loss of constituents from the melted region during annealing can introduce defects [8] during regrowth which has lessened the prospect of this annealing technique. Rapid thermal annealing (RTA) is an emerging technology which provides better activation than the 10^{18} cm^{-3} limit attainable with furnace annealing.[9] The activation is not as high as that of laser annealing but resistivity is lower due to higher mobility. Since higher temperatures are used with RTA, short anneal times are required. Therefore, less damage to the sample through As loss has been observed with a corresponding lower movement of the original implant. Encapsulants appear to withstand temperatures in excess of 1000°C for short times while it is still questionable if a cap is necessary at lower temperature RTA. In this work, preliminary studies shows that thermal erosion occurs above 950°C for capless RTA. With RTA there is the possibility of stress due to rapid temperature variations; in this

research formation of slip planes is observed in some instances (Figure 4.1).

Throughout the majority of this research capped furnace annealing is used. Since SiO_2 is readily available it is used even though Si_3N_4 is reported to be superior.[3] An anneal of 850°C was performed on a sample capped with 1000Å of sputtered SiO_2, which resulted in complete destruction of the GaAs surface from thermal etch pits. It was decided to use plasma enhanced chemical vapor deposition (PECVD) to put down the SiO_2 since 1000Å could be deposited in 7 minutes rather than the hour required to sputter the same thickness, and the surface damage from sputtering was minimized. The surface was studied for different thicknesses of PECVD SiO_2 (Figure 4.2), and the thermal erosion was eliminated with a 7000Å cap. For PECVD SiO_2 a good encapsulant is obtained when the index of refraction is 1.46. The integrity of the SiO_2 is observed to be important since a few percent change of the index of refraction of the SiO_2 caused the anneal surface to be littered with thermal etch pits.

The procedure for annealing begins with a thorough clean of the surface. Since the implant peak is approximately 1000Å below the surface, the GaAs can not be etched as previously described, rather the sample is degreased as usual and then dipped into HCl for 20 seconds to remove the native Ga_2O_3 which grows during exposure to air. Then 7000Å of SiO_2 is deposited on the face of the wafer and 5000Å on the back. The samples are then ready for annealing which consisted of a 5 minute push and pull in a 3" tube with flowing nitrogen and an anneal of the designated time less 4 minutes which is attributed to annealing during the push/pull. The samples are placed face down on a Si wafer during annealing which is thought to reduce thermal etching of the front surface due to a decrease in thermal shock. The SiO_2 is then stripped with buffered HF (10:1) and the surface inspected both optically for damage and with an ellipsometer to monitor the remaining oxide.

D. Photolithography

This recipe originated at a lab which had hot plates available and has been modified for use with oven baking which is present in the lab. The difference between oven and hot plate baking is that the former has an ambient temperature which may change if the air is disturbed by opening the door while the latter uses constant heat from the bottom. It is necessary to use a longer bake time with ovens since a skin tends to form on the photoresist that restricts the evaporation of solvents and slows the resist cure. A hot plate bake on the other hand drives the solvents out from the bottom up before any skin has formed. Consequently, hot plate baking is preferred since degradation of resist from trapped solvents is less probable.

To facilitate the handling of small and fragile pieces of GaAs, the samples are affixed to 2" Si wafers with photoresist. A small amount of resist is spread on to the Si wafer and then the sample is pressed into place. The resist is then hardened in an oven or on a hot plate at 70°C for 10 minutes. Excess resist may be removed by squirting the sample with Acetone and then quenching in Methanol/H_2O followed by water. The sample should immediately be blown dry with the N_2 gun held perpendicular to the surface. When cleaning large samples, such as quarter wafers, some difficulties may be encountered since the dissolved resist from underneath the sample can flow onto the surface.

The sample is baked for 10 minutes at 120-150°C which improves the adhesion of the resist by driving the water from surface. Throughout the research a spin speed of 4750 rpm is used which results in a resist thickness of about 1.5 μm. The resist is then baked at 70°C for 30 minutes.

If the resist will be used in a lift-off process rather than for an etch mask, the wafers are only baked for 20 minutes followed by a soak in Toulene for 5 minutes then another bake of 10 minutes. The Toulene (Chlorobenzene is an alternative) is necessary to harden the top surface of the resist which allows the developer to slightly undercut the pattern.

The undercut is used to minimize the chance of bridging with the lift-off process.

The resist is then ready to be exposed and developed. Presently, with the Kasper Mask Aligner in the UCB Microelectronics Lab an 8 second exposure is used followed by an 18 second develop in 4:1 H_2O: 351 Shipley Developer. These parameters should be adjusted accordingly as the light source in a mask aligner varies with age as does the strength of the developer. It is recommended that the sample be developed for approximately 75% of the time specified, the partially developed pattern viewed under a microscope with a yellow filter, and then the development completed. The final step in the lithography process is a cure for 20 minutes at 90°C.

E. Metalization

When selecting a gate metal for Schottky diodes[10, 11] a number of factors must be considered: easy of deposition and compatibility with processing temperature; stability of metal and sample heating during deposition, metal adhesion to semiconductor including expansion coefficient, electrical behavior, and chemical reaction with the interface. Titanium was selected as the gate metal to be used in this research. It was chosen in part due to prior experience with the metal and because of its successful use in commercial devices. Ti has very good adhesion capability and is often used as a first layer metal for this reason. Its electrical properties on n-GaAs are reported by Sinha *et al.*[12] The common sandwich of Ti/Pt/Au was not used since there had been no prior experience with evaporating Pt in the Veeco 401 evaporator available for this research. The melting point of Pt is 1773°C and thus it should be easily evaporated with the equipment available since it is possible to evaporate Ti which melts at 1660°C (Ti oxides melt around 1800°C). The only other difficulty is the configuration of a three-boat system that would minimize cross contamination. On the other hand, previous researchers at the facility have been unsuccessful with evaporating good Ti Schottky barriers on GaAs.

Ti/Pt/Au is used since Ti forms a good Schottky barrier with GaAs (ideality factor: n = 1.05, barrier height: ϕ_B = 0.8 eV). Au is desired for both its low resistance and easy with which it wire bonds. The Pt is sandwiched in between to prevent the Au from diffusing in to the Ti and degrading the Schottky barrier.

Using only Ti for the gate metal presents a few complications. First, Ti reacts readily with many materials and is consequently used as a getters in UHV systems. Thus, it is important that the residual gas pressure be low and the system extremely clean to minimize the contamination of the Ti film during evaporation. In addition, it is also important that the Ti source be heated slowly allowing time for any contaminates and oxides to outgas before commencing evaporation. Once the metal starts evaporating, the shutter is not opened for 10 to 20 seconds. This allows the pressure to fall to the mid 10^{-7} Torr range due to Ti covering the cold side walls which prevents outgassing. Secondly, a high temperature is required to evaporate Ti so the sample must be properly heat sunk and shielded from the heat when ever possible so that the photoresist is not carbonized. Thirdly, the boats used to evaporate are made of tungsten which alloys with Ti so occasionally the evaporation may be unexpectedly terminated by a broken boat. When heating a metal, the temperature should be raised slowly around the melting point since large metal pieces tend to spatter out of the boat due to expansion stress when melting.

The standard ohmic contact used for GaAs is an eutectic of Au/Ge (88%/12%). After the alloy is deposited it is sintered for 30-40 seconds at 450°C to diffuse in the Ge. During this sintering the alloy tends to ball-up since it does not wet the surface (Figure 4.3). To eliminate this, a thin film of Ni or Cr is evaporated on top followed by a thick film of Au which is used for interconnecting and bonding. The Ni wets the surface so that the Au/Ge remains uniform across the surface. In this research only Au/Ge is used and followed by a film of Au or Ti after the sintering is completed. Given a three-boat set-up the sandwich of AuGe/Ni/Au can be easily realized in the available Veeco 401. A review of ohmic contacts to GaAs is given by Sharma.[13]

The preferred procedure for lift-off uses a soak in 60°C acetone for 5 to 10 minutes. The pattern might not lift-off by itself, especially if it is Au, so the sample should be slightly agitated. If the metal is still affixed, a longer acetone soak is required. As a last step the ultrasonic may be used to remove stubborn metal, but it may rip the pattern. Usually a lift-off will leave behind a few metal "hairs" which are easily removed in the ultrasonic. All acetone soaks should be followed by methanol to remove the acetone and then blown dry.

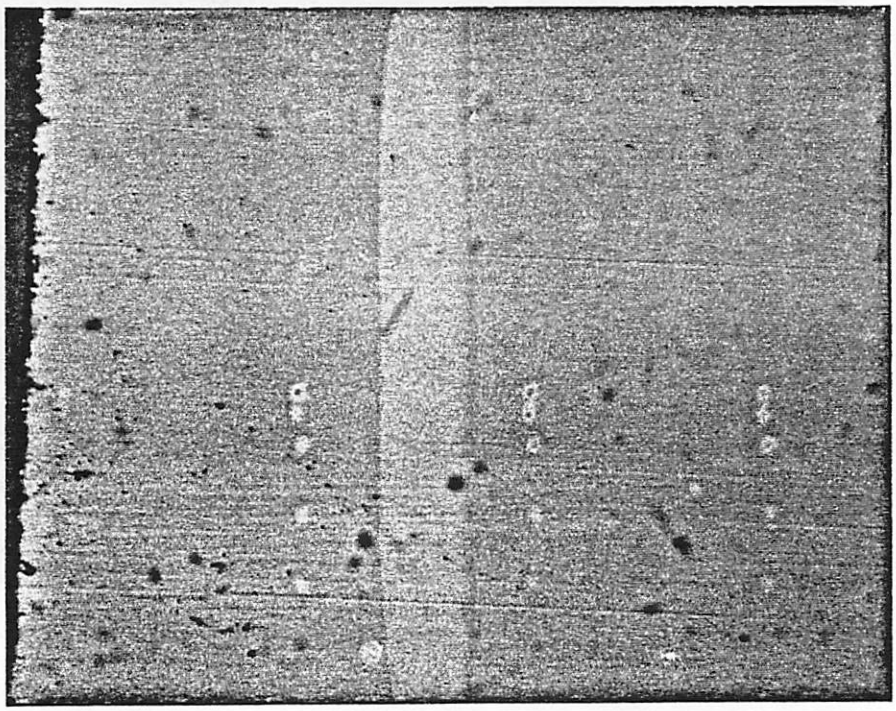
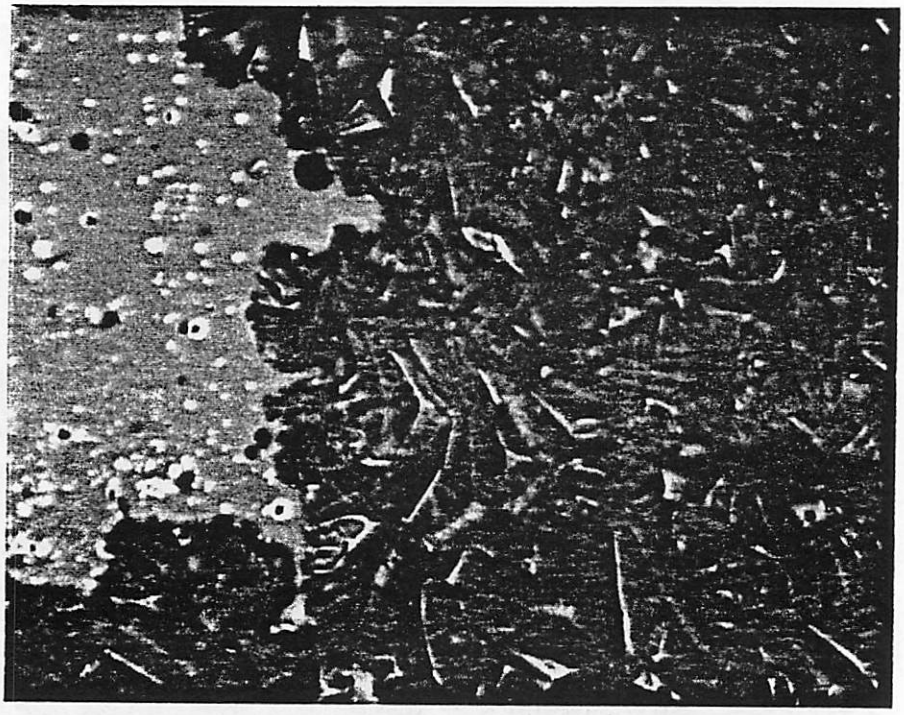
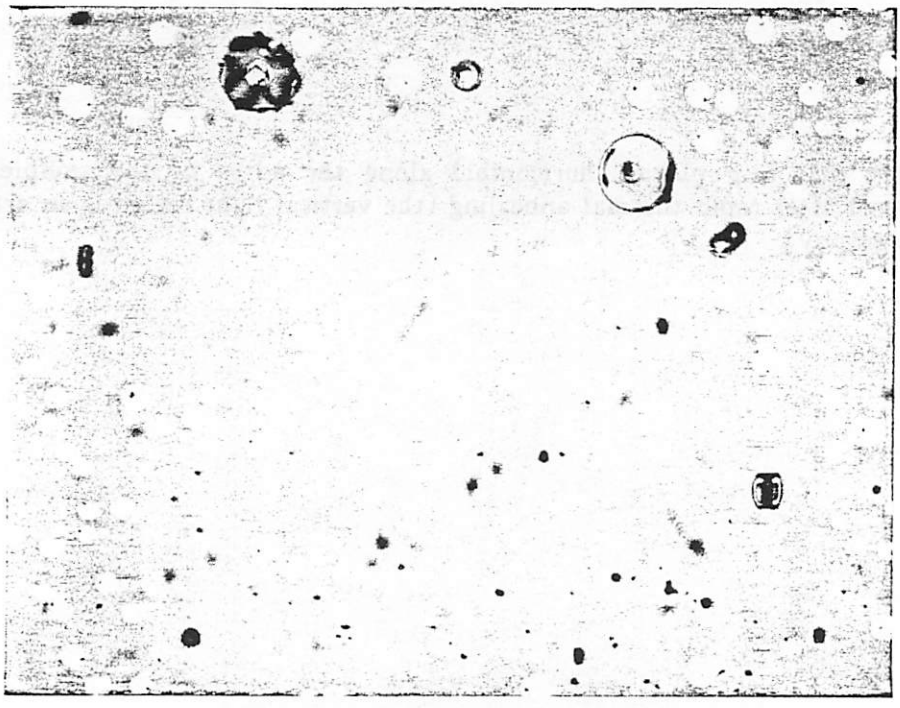


Figure 4.1 Slip planes (horizontal) along the edges of the samples are often observed after rapid thermal annealing (the vertical light region is an artifact of the photography).

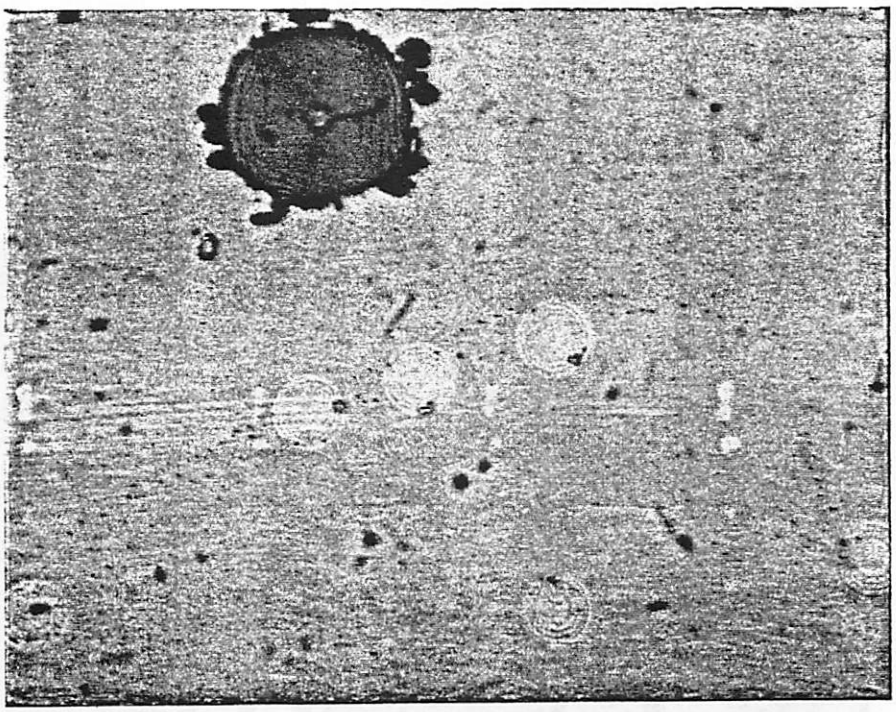
Figure 4.2 Surface conditions of implanted SI GaAs after annealing at 840°C for 30 minutes in flowing nitrogen. These samples were annealed face up.



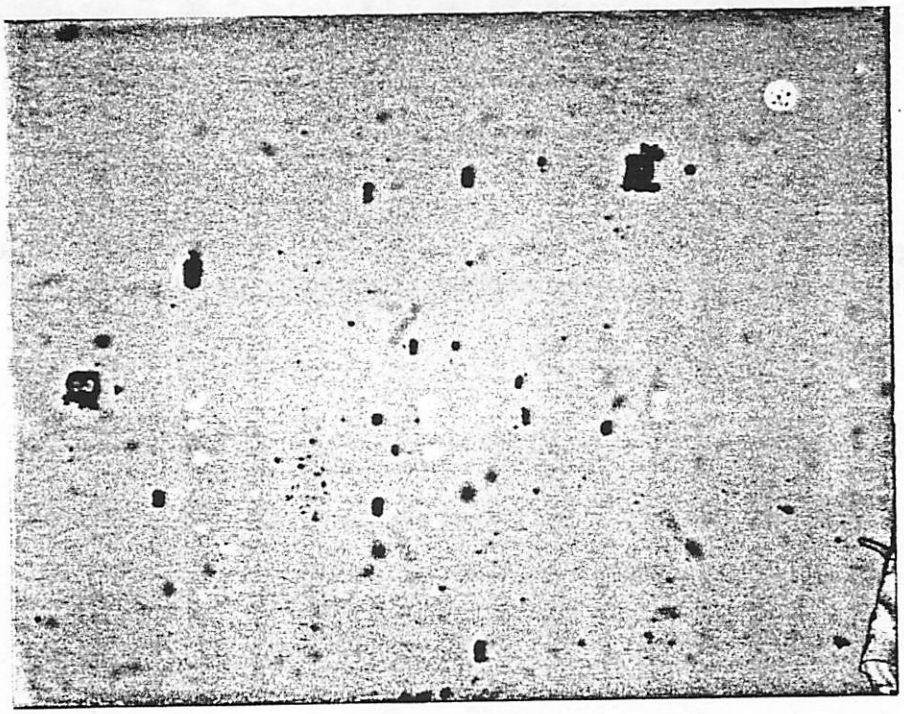
2000Å



4000Å



5000 Å



6000 Å

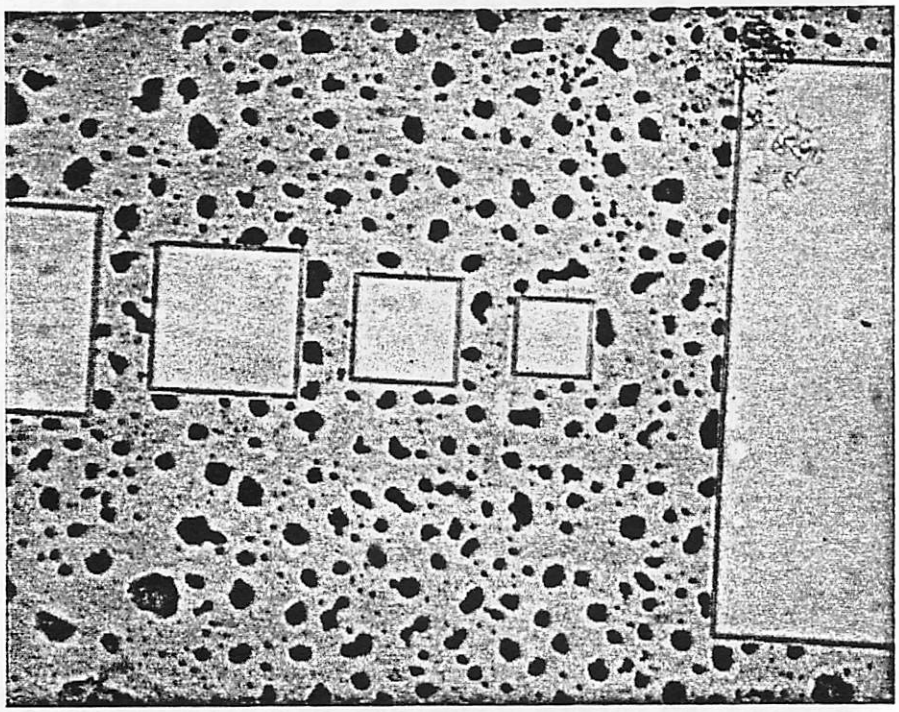


Figure 4.3 Au/Ge ohmic contacts which surround these diodes balled up during sintering. The large dark areas represent accumulated metal.

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V. DEVICE FABRICATION

A. Single-Metal Schottky Diode

The motivation for this device is to develop the capability to monitor the process after the deposition of the gate metal. As mentioned in the introduction, it is desirable to test wafers in-process so that those failing to meet specifications can be rejected in order that additional processing cost be avoided. Since all diodes have an inherent reverse leakage current which is dependent on the area of the diode, two back-to-back diodes can be fabricated from one metalization eliminating the deposition of a metal for the ohmic contact. The device is constructed by fabricating a circular diode which is surrounding by a diode of larger area (Figure 5.1); an area ratio greater than 100 is required to be able to observe forward characteristics that are not overwhelmed by series resistance. The diode I-V characteristics should be similar to that of a conventional diode except the forward current is limited by the product of the area and the leakage current density (Figure 6.1).

The devices fabricated use standard cleaned GaAs with the dosage, energy of the implant, and the anneal conditions varied. Six diodes sizes are constructed in each lot with the area increasing by a factor of two from .04 mm^2 to 1.28mm^2. The devices are fabricated by lifting off " donuts" of Ti metal; the "donut hole" being the small area diode and the large area diode the surrounding metal. The distance between the two diodes is 30μm. Usually 1200Å to 1500Å of Ti is evaporated for these devices. No annealing of the diodes is possible since when covered with a SiO_2 encapsulant, the Ti is etched away by the hydrofluoric acid when removing the SiO_2. Also, as mentioned before, Ti is very reactive and thus annealing while exposed to oxygen or other gases could degrades the Schottky barrier.

B. Two-Metal Schottky Diode

This device is a conventional planar diode with square geometry (Figure 5.2). The Au/Ge is deposited first and then sintered followed by a Ti evaporation to form the Schottky diode. It is designed with rather lax tolerances so that the gate to ohmic contact spacing is 10μm and the Ti to Ti spacing 5μm. Diode area ranged from .02 mm^2 to 1.28 mm^2. The expected characteristics are similar to the previous diodes except the forward current saturates at a higher bias and the series resistance is lower.

C. Mesa Isolated MESFET

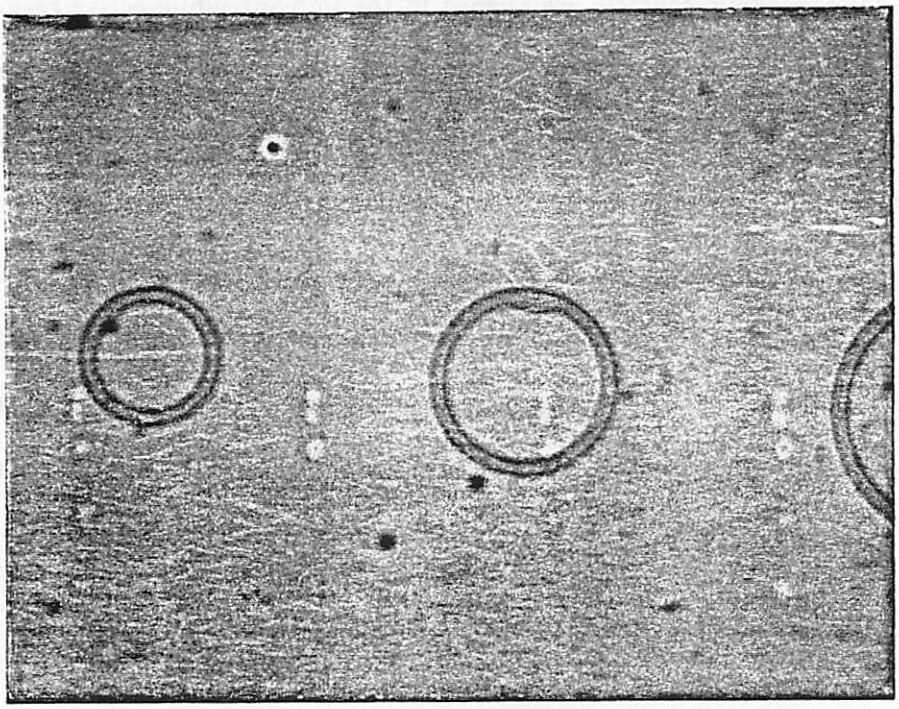
This is a quick three mask-level MESFET (Figure 5.3) which was fabricated in order to demonstrate the feasibility of conductance DLTS. The alignment tolerance is 10μm for the gate to drain/source spacing (Figure 5.4); thus, it is not an optimized device due to this large parasitic source/drain resistance. The gate width is 50 μm with gate lengths of 10, 20, 40, and 100 μm. After a standard cleaning the wafer is blanket implanted and annealed. The Au/Ge ohmic contact are then evaporated and sintered followed by a mesa etch with $NH_4OH:H_2O_2:H_2O$ 1:1:20 for 30 seconds which etches 5000Å through the implant to isolate the source and drain from the gate contact pad and from other devices. The Ti gate is then evaporated to complete the device.

D. Selectively Implanted MESFET With Passivation

Since the mesa isolated MESFET exhibited excessive noise during conductance DLTS, an improved version was fabricated (Figure 5.6). A possible problem with the previous MESFET is that it relies on bare GaAs for isolation. This new structure uses SiO_2 for isolation and passivation to minimize surface leakage. The mesa may also contribute to leakage plus it is not desirable to have steps of 5000Å since correct crystal orientation is required and difficulties with step coverage may be encountered for non-perpendicular evaporation

(Figure 5.5). Critical alignment on this new MESFET is 3 μm for the gate to drain/source spacing and 8 μm for the oxide to channel spacing (i.e. overlap of Ti onto the SI GaAs) (Figure 5.7). The ohmic contacts are aligned to the implant while active region windows etched into the oxide and gate metal aligned to the ohmic contact. The gate width is 100 μm and gate lengths available are 2, 4, 8, 16, 32 μm. Diodes similar to those mentioned in part B are also fabricated.

The GaAs sample is given a standard clean and then approximately 5500Å of SiO_2 are deposited using a Technics PECVD system. Holes are etched in to the SiO_2 to pattern the implant of the active regions, alignment marks, and test devices. Alignment marks are then etched into the GaAs with 1:1:20, $NH_4OH:H_2O_2:H_2O$, for 20 seconds using the holes etched through the oxide in the previous step to pattern the etch (Figure 5.8). With only the oxide mask on the wafer, it is implanted after which the SiO_2 is stripped off and an anneal cap of PECVD SiO_2 deposited. For samples to be annealed by RTA approximately 1500Å is deposited on both the front and back while for furnace annealing the samples receive 7500Å on the front and 5000Å on the back. After annealing the oxide is again stripped, remaining oxide checked with the ellipsometer, and surface damage inspected with an optical microscope. A PECVD SiO_2 cap 1200Å is deposited and holes etched through using the ohmic contact mask to pattern the etch with oxide undercutting occurring. 1200 Å of Au/Ge is evaporated and then lifted off prior to sintering. The oxide undercut improves the lift-off since the probability of bridging is reduced.[1] The SiO_2 is then etched to expose the implant region for deposition of the gate and contacts to the source and drain. 1500Å of gate metal is evaporated followed by lift-off (Figures 5.7, 5.9). The Au contact pads which are 2000Å thick are then evaporated. It is necessary to deposited 200Å of Ti prior to the Au to improve adhesion to the SiO_2. Au regularly forms bridges over the resist edge so the photolithography must be carefully performed. Lifting off Au that has bridged is difficult and will result in torn patterns. The final step is a 1000Å sputter SiO_2 passivation layer with windows etched through to the pads.



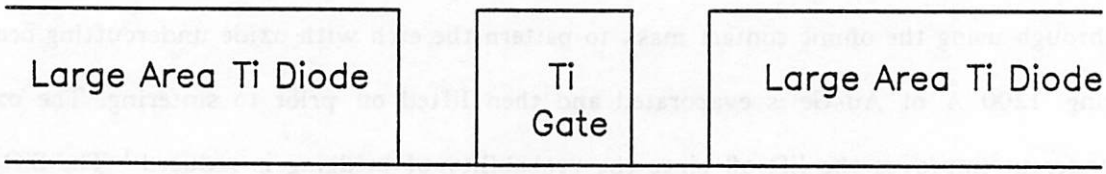
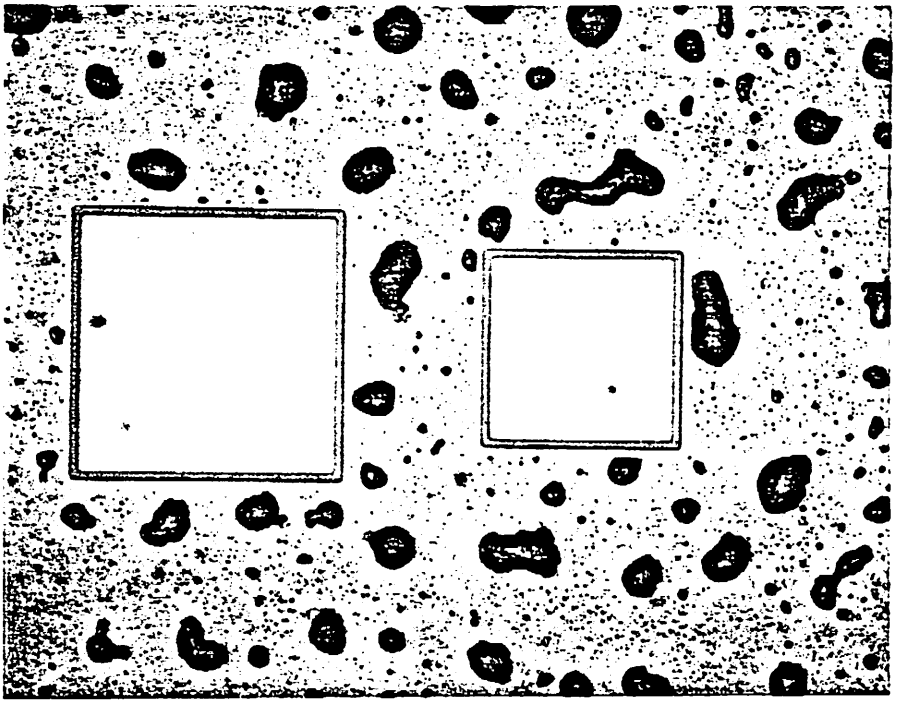


Figure 5.1 A top view of the single-metal diode and cross-section. The spacing between diodes (ring thickness) is 30 μm.



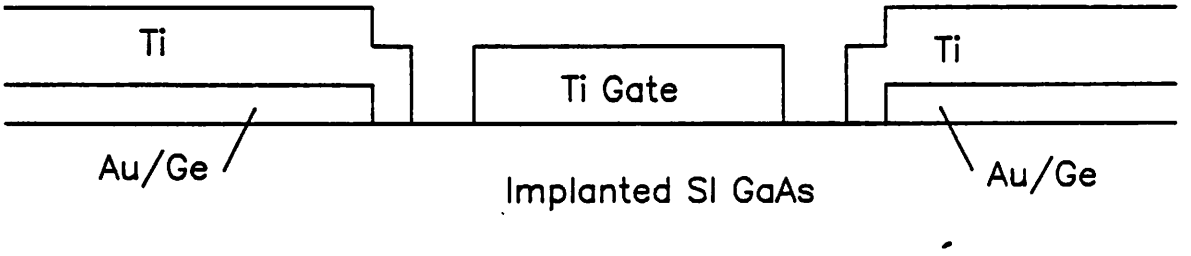
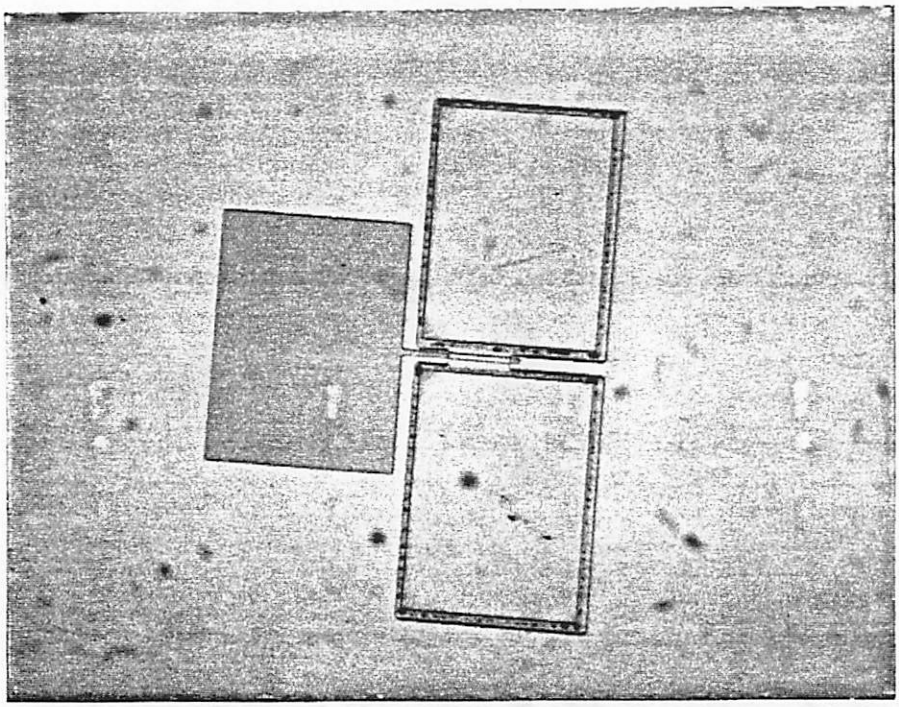


Figure 5.2 A top view and cross-section of the two-metal Schottky diodes. It is possible to see in the picture that the Au/Ge ohmic metal is recessed in from the edge. This allows a 10 μm alignment tolerance yet it improve the series resistance since the metalization gap is only 5μm. The fringe of gate metal has the same characteristics as the single-metal Schottky diodes. The large dark accumulation of metal are formed since Au/Ge does not wet the GaAs surface.



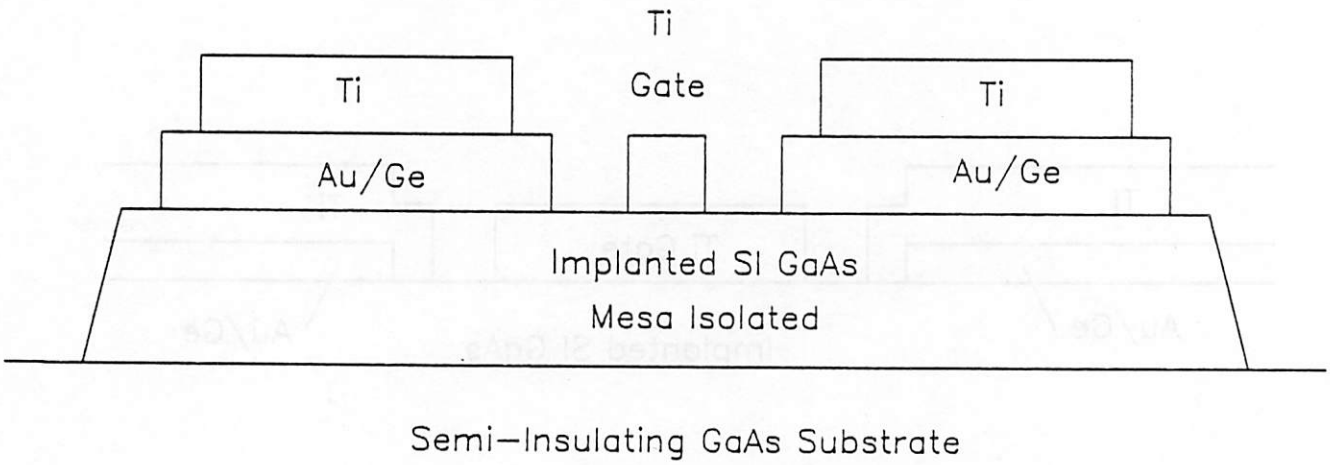


Figure 5.3 This MESFET uses a mesa etch to isolate the active region from other devices and the gate pad.

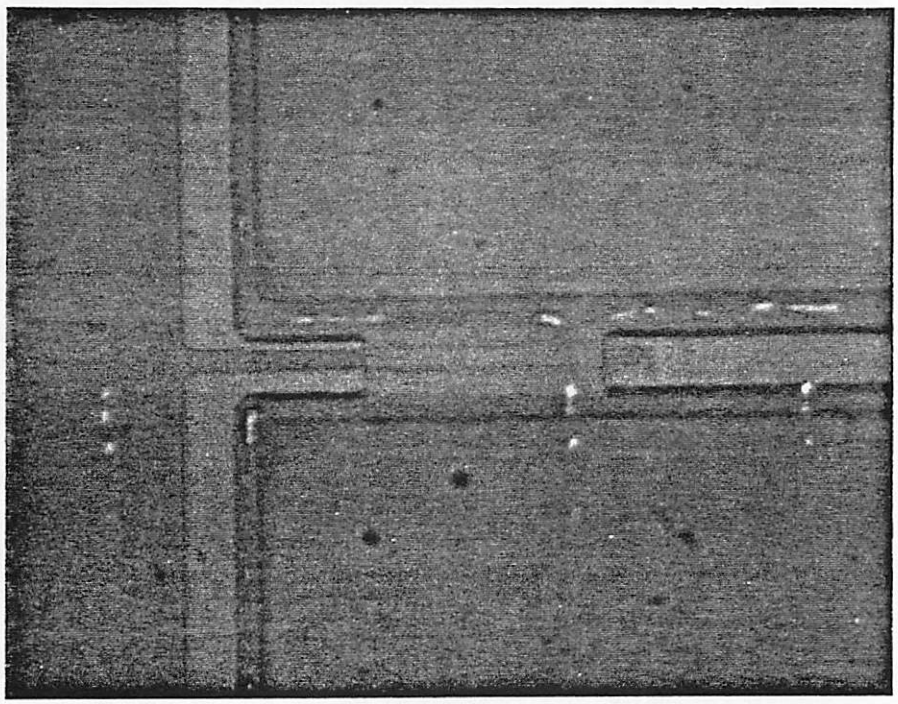


Figure 5.4 The tolerance on the mesa isolated MESFET is 10μm which expedites alignment.

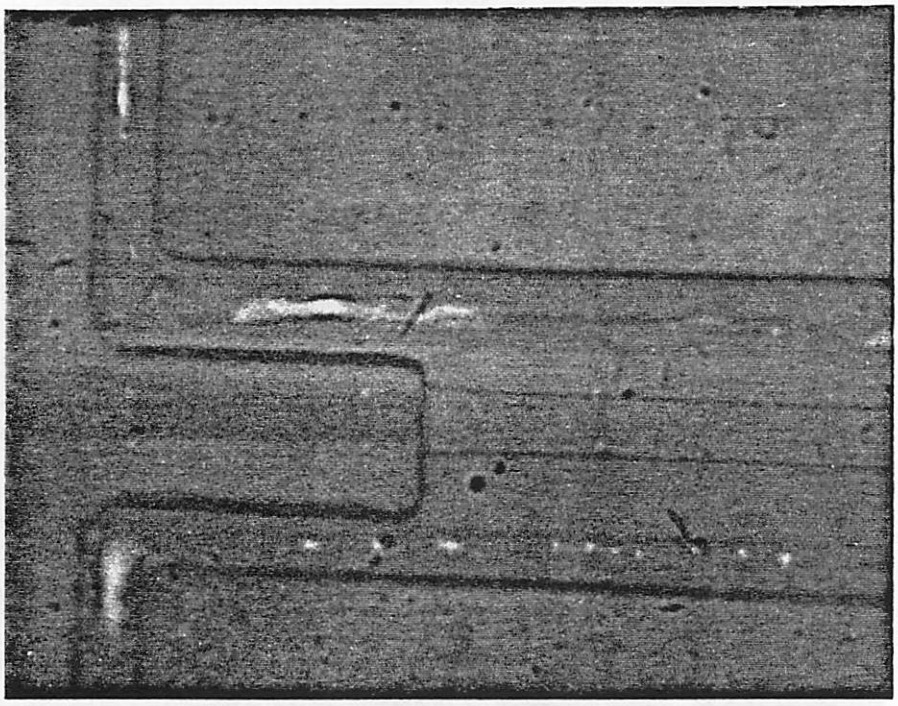


Figure 5.5 A thick layer of metal has to be deposited so that the step does not degrade the interconnect. Here, the crystal was mis-oriented so that the mesa undercuts at the step. Also, the etch was deeper than specified.

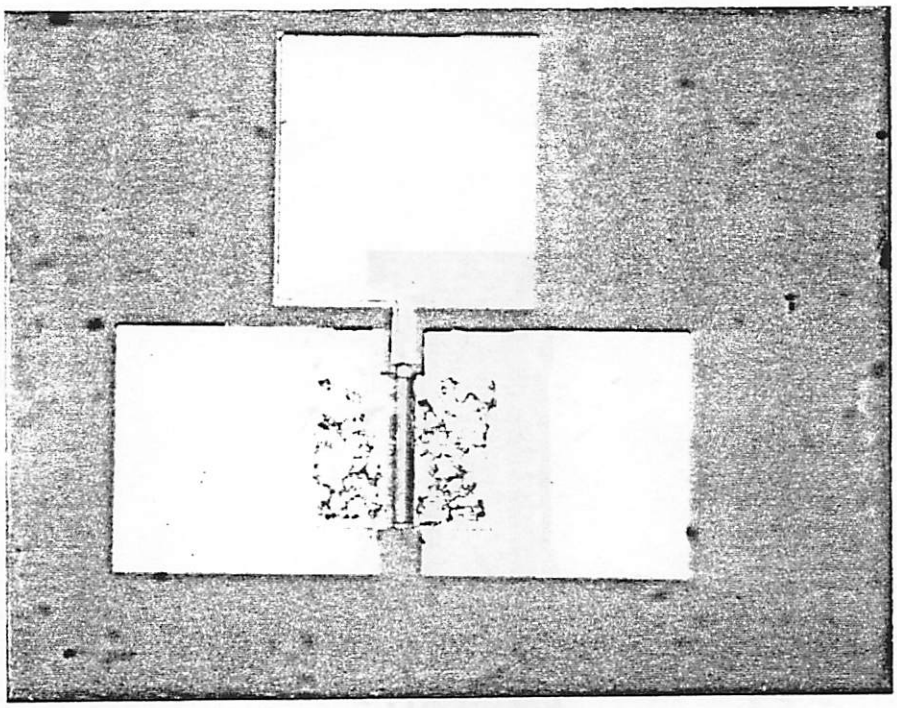


Figure 5.6a A completed MESFET with SiO_2 passivation and vias etched to the contact pads.

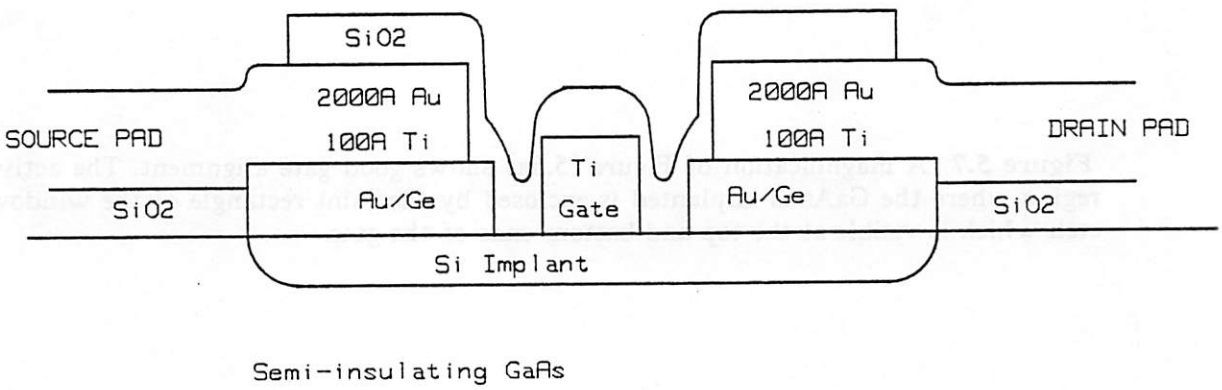


Figure 5.6b A cross-section of the selectively implanted MESFET.

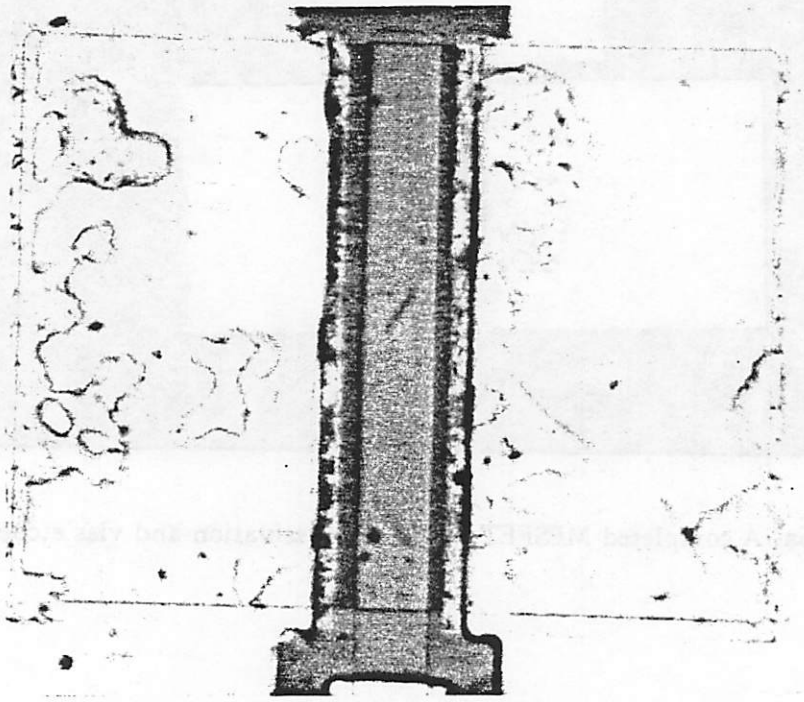


Figure 5.7 A magnification of Figure (5.6a) shows good gate alignment. The active region where the GaAs is implanted is enclosed by the faint rectangle of the window etch which is visible at the top and bottom ends of the gate.

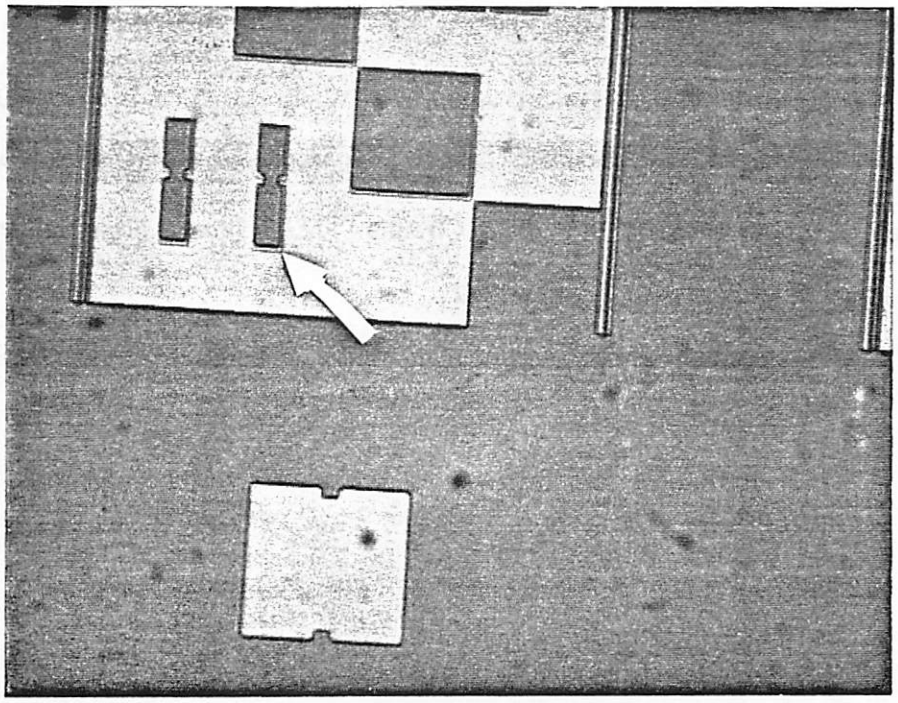


Figure 5.8a This represents a previous process where the alignment marks were etched before the implant mask; however, this introduced additional alignment difficults. Here both the implant mask and an etched mesa alignment mark underneath a SiO_2 cap can be seen.

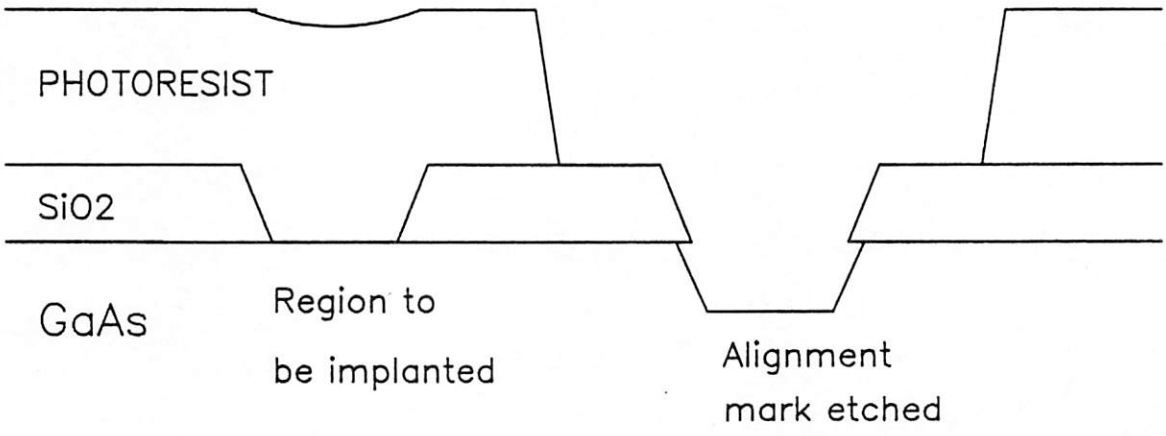


Figure 5.8b A SiO_2 layer is put down and then both windows for the implant and alignment marks etched. The alignment marks are then etched using photoresist to mask the implant region; thus, there is no alignment error between the etched marks and implant.

References

1. R. L. Van Tuyl, V. Kumar, D. C. D'Avanzo, T. W. Taylor, V. E Peterson, D. P. Hornbuckle, R. A. Fisher, and D. B. Estreich, "A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits," *IEEE Trans. Electron Devices*, vol. ED-29, no. 7, pp. 1031-1037, July 1982.

VI. EXPERIMENT & ANALYSIS

The majority of the analysis is based on I-V and C-V measurements. As was mentioned in the section on measurements, measuring technique is important so as not to introduce excessive error. For instance, improper zeroing of the capacitance meter and parasitics capacitances can shift the calculated depth of the doping profile peak. Another difficulty with C-V measurements is the leakage current which may cause the capacitance to initially increase for increasing bias (Figure 6.13). This mechanism will produce an infinite value for doping when the slope of the C-V capacitance curve changes sign. The affect of leakage current on a doping profile can be seen in Figure (6.2b) where the initial falling curve was caused by the large current near zero bias which effectively decreases the width of the space charge region. Other considerations include the proper measuring mode: either parallel or series. The proper mode is determined by the black box being measured in series with a resistor of in parallel with a resistor (diode leakage model).

A. Single-Metal Schottky Diode

The forward current of this device is limited by the product of the area and leakage current, J_s, of the large area diode. The device is modeled by the measured diode, D_g, in series with a ladder network of resistors and diodes operating in the opposite bias mode (Figure 6.1). A n-type GaAs substrate was initially used since many of the process steps were new. This eliminated the process variations due to the implant and anneal steps. The goal was not only to obtain working devices but also to adjust the process until diodes were obtained with similar characteristics as the published barrier height and ideality factor (for titanium, Sinha *et al.*[1] ϕ_B=0.82 to 0.84 and n=1.03 to 1.04).

The evaporation procedure for the Schottky metal, titanium, was the initial concern. First, the evaporations were carried out at temperatures which baked the photoresist making lift-off impossible. In other instances, bad adhesion was observed with the metal lift-

ing off the substrate due to stress. Excess heating was resolved by using a shutter to shield the samples during outgassing of the evaporant. The positioning of the electrodes relative to the boat was also observed to be critical. When the boat was clamped at the ends, current had to pass through the entire length of the boat providing a large heat source. Clamping close to the evaporant holder, on the other hand, resulted in only a small portion of the evaporant melting since the electrodes acted as heat sinks. Removing heat from the substrate by placing heat sinks, such as Al blocks, on the back of the Si carriers improved the lift-off of samples at hot-spots in the evaporation system. Electrical characteristics measured for deposition with and without heat sinks were approximately the same. The improved Schottky metal deposition did not result from any one process modification, but rather the problem was resolved by a consciousness of resist heating and a cleaner system due to metal evaporation on to components. With these new techniques best values of ϕ_B=0.81eV and n=1.07 (Figure 6.2) were obtained while the minimums were ϕ_B=0.74 eV and n=1.28 (Figure 6.3). ϕ_B was measured in the 0.60 to 0.68 eV range for a small area sample (Figure 6.4), for a sintered sample (Figure 6.5), and for a sample dipped in NH_4OH prior to evaporation (Figure 6.6). The sintered sample had been cleaved from material which had previously yielded "good" diodes. The sintering, however, lowered the ideality factor to 1.00. There may have been a variation inherent with processing small samples since the effect of small sample size did not appear in latter work. For the "good" diodes, C-V measurements resulted in values for N_{sub} of 10^{18} as expected (Figure 6.2b). Other evaporation procedures were also investigated. The best diode characteristics obtained (Figure 6.7) used a 10 to 20 second evaporation on to the shutter prior to evaporating on to the sample. This "pre-evaporation" covers internal surfaces resulting in a cleaner system such that the pressure during evaporation reached the mid 10^{-7} Torr range.

With the fixed process parameters understood, however not necessarily always repeatable, the focus shifted to annealing of ion implanted SI GaAs samples. The first diodes were annealed at 850°C for 30 minutes which are conditions previously reported in

the literature. The required SiO_2 thickness had already been calibrated using scrap GaAs; consequently, the appearance of thermal etch pits after annealing was unexpected. In fact, the quality of the PECVD SiO_2 could be monitored by the population of thermal etch pits after annealing. An increased SiO_2 thickness was used to some success; however, the best solution was continuous monitoring of the refractive index of the encapsulant and deposition parameters, and re-calibrating when slight deviations appeared. Since the population of etch pits is dependent on the anneal conditions, a less severe anneal should improve the surface quality. Using material implanted with $7.5x10^{13}cm^{-2}$ at 120 keV, two sets of samples were annealed at various temperatures. In the first set the temperature was varied from 800 to 860°C with reasonable results only at 850 and 860°C (Figure 6.8). The results of this test were questionable due to a poor quality SiO_2 encapsulant so another set was fabricated with anneal conditions of 700, 750, 800, and 900°C for 30 minutes in forming gas. Again, only the high temperature anneal provided working diodes (Figure 6.9). A similar anneal at 850°C in forming gas yielded mixed results with all the one-metal Schottky diodes exhibiting no forward characteristics while good two-metal diodes (next section) were obtained with this anneal. A control sample which was not annealed had characteristics of a low-value resistor (Figure 6.10). The large conduction was probably the result of a thin amorphous layer introduced by the implant.

The initial set of samples with varying implant conditions yielded diodes with leakage currents in the range of 10^{-3} A/ cm^2 (Figure 6.11). This large leakage may have been caused by an oxygen ash, used to remove organic contaminates, prior to annealing. Consequently, an additional set of twelve samples of varying implant dosage ($1x10^{11}$ to $8x10^{14}$) were prepared and processed in batches of four. Dosages below $8x10^{11}$ cm^{-2} exhibited no forward characteristics. The second lot processed had low barrier heights which was evidently a process problem either in the anneal or metalization; otherwise, there was no major trend in ϕ_B (Figure 6.12b). The ideality factor remained relatively constant with respect to implant dosage (Figure 6.12a). Image force effects should

cause the ideality factor to increase with doping; consequently, the ideality factor was probably affected by surface states whose density would increase with implant dosage. The doping profiles of a number of samples were calculated from measured C-V data (Figure 6.14). This analysis is complicated by an initial rise in the capacitance (Figure 6.13) due to the large reverse leakage seen at low bias by the measuring equipment. The doping peak is not expected to go above 10^{18} cm^{-3} since the dopant activation limits in this range. Generally, the doping concentration appears to increase with implant dosage, but the location of the peak is not constant so capacitance off-set is probably present in the measurement.

Since wire-bonding would be required in future processes a two-step evaporation of Au on Ti was tested. A side by side comparison with a Ti only gates fabricates in the same lot resulted in a 0.01 eV difference in barrier heights which is beyond the accuracy of the process. An interesting experiment would be to observe the change in electrical properties when the sample is heated and the Au diffuses to the interface.

The direct dependence of the electrical characteristics on sample size is a obstacle for single-metal diodes. Previous figures show that the forward current saturates at a lower current than expected while others saturate at about 0.1 A/ cm^2. This early saturation is caused by the limited amount of reverse current that the large area diode can accommodate. In most case, the ratio was approximately 100:1. A rough calculation shows that the ratio between forward and reverse current is similar to the ratio of large area to small area diodes.

B. Post-Anneal Surface Quality

The experience gained fabricating diodes on n-type substrates had been applied to implanted material; however, after trying various anneal conditions, the best diode measured had an ideality factor of 1.09 and a barrier height of 0.74 eV (Figure 6.15). Usually, ϕ_B was in the range of 0.62 to 0.66 eV. Clearly, a problem existed with the surface

integrity which was evidenced by the low ϕ_B. Since the SiO_2 quality was being monitored with an ellipsometer, it was easy to also check the native oxide thickness on the bare GaAs. Initially the film measured on the GaAs was 20 to 30Å, but after the encapsulant was deposit, the sample annealed and then the SiO_2 removed, values were obtained in the range of 80 to 150 Å. A control sample which was not annealed but had SiO_2 deposited and stripped showed no increase in measured film thickness (Figure 6.10). Typical Ga_2O_3 etches, HCl and buffered HF, were tested, but the thickness measured was the same or slightly greater. H_2SO_4:H_2O_2:H_2O was also tried with no improvement. Finally, a weak solution of NH_4OH:H_2O_2:H_2O removed the film and brought the ellipsometer reading back to the pre-annealed value. Presently, the composition of this film is unknown as is the mechanism which causes it. It is possible that a limited amount of arsenic diffused from the surface into the SiO_2 or that the SiO_2 was oxygen rich and diffused into the GaAs. Thus, the measured values are probably erroneous since the parameters for Ga_2O_3 were used in the calculations. The diode electrical characteristics are the final test of the expedience of a NH_4OH:H_2O_2:H_2O dip to remove this film. Two samples were etched with NH_4OH:H_2O_2:H_2O and values of ϕ_B of 0.70 and 0.77 eV and ideality factor of less than 1.1 (Figure 6.16) were measured.

Since the anneal time had always been 30 minutes, a less severe anneal of 20 minutes at 850°C was introduced. A decrease in the post-anneal film thickness measured with the ellipsometer and a better surface by visual inspection (ie. a lower population of thermal etch pits) were observed. The doping profiles from C-V measurements for both 20 and 30 minute anneals appear to be similar (Figure 6.17). The measured reverse leakage current also is improved for a shorter anneal (Figure 6.18).

The reduced annealing time was used in conjunction with a 1:1:100 NH_4OH:H_2O_2:H_2O etch (2000Å/ min) to profile the affect of the etch. The two-metal diode structure was fabricated on material implanted with $1x10^{12}$ cm^{-2} at 120 keV; this was not a good choice, however, since the zero bias depletion of the unetched sample is

already past the implant peak.

Etch time (sec)	Ideality Factor	Barrier Height (eV)	Peak Depth (μm)	Peak Concentration (cm^{-3})
0	1.16	.82	.15	5E16
15	1.13	.86	.18	2E16
30	1.4	.86	1.4	2E13

Note: peak depth and concentration represent first measurable data point.

The data demonstrates the etching of the GaAs substrate with sufficient etching taking place so that a sample etched for 45 seconds had no forward characteristics. Since the "film" thickness decreased after some etching it would appear to be a surface phenomena. An additional experiment would consider the effects of the anneal on different implant species and on unimplanted material. Given that the "film" thickness showed no trend and the measured value was lower for RTA samples, this film is a surface effect possibly from implant damage or interaction with the encapsulant. Thus, it is evidence of a change in the optical properties of the surface and not a measure of Ga_2O_3. An anneal using forming gas rather than nitrogen resulted in lower film thicknesses, but it is unclear whether this was due to a better encapsulant. Since some of the samples did not produce working diodes, the ambient gas is also suspected. Again additional research is necessary.

C. Two-Metal Schottky Diode

The standard two-metal Schottky was fabricated to remove the area dependence from the I-V characteristics. The processing of this device is more complicated than the prior one so it would be implemented in a different part of a process monitoring cycle. The circuit model is similar to that of the previous diode (Figure 6.1) except that the diodes, D_o through D_n are replaced with fixed contact resistances. The first devices exhi-

bited improved electrical characteristics with both larger forward to reverse currents ratio and a slightly higher barrier height.

A matrix of 12 samples was fabricated with implant dosage and the RTA temperature the two variables. The samples were processed in lots of the same implant dosage. The electrical characteristics, which are rather mixed, are plotted in Figure (6.19). There appears to be a slight decrease in barrier height for increasing anneal temperature while the ideality factor appears to be constant with respect to anneal temperature but strongly a function of implant dosage. Even though the data represents the average good diodes, to show repeatability and eliminate process variation, (decrease error bars) additional experiments should be run. The surface damage as measured both optically and by the ellipsometer increased with increasing dosage and anneal temperature. The slight negative slope of barrier height with respect to temperature may reflect this surface damage. On the other hand, low temperature anneals were not as successful with activating the implant (Figure 6.20). The shape of the profile is not as expected (near Gaussian); this may be the result of the RTA anneal. The lower ideality factor for lower dosages is attributable to a doping dependence of ideality factor which may be an image charge effect (see Equation 2.2). Since no cross-processing existed and the trend in ideality factor was repeatably, process variations may be neglected in this instance.

D. MESA Isolated MESFET

This structure was developed as the preliminary test vehicle for conduction DLTS measurements. Due to the alignment limitations of the available mask aligner, the source-gate and drain-gate spacing were each 10 μm. This spacing introduces a large resistance which must be included when evaluating the parameters of the MESFET. Substrates that had been implanted with $1x10^{12}$, $1x10^{13}$, and $1x10^{14}$ cm^{-2} were selected for fabrication and annealed for 20 minute at 850°C in flowing nitrogen. The mask set also included large area two-metal test diodes of the size previously used since the gate areas are usually to

small to measure precisely the necessary data. These diodes provided information concerning the Schottky barrier and effectiveness of the anneal.

Implant Dosage (cm^{-2})	Barrier Height (eV)	Ideality Factor -
1E12	.687	1.067
1E13	.65	1.1
1E14	.61	1.15

These electrical characteristics are reasonable but better data was previously obtained. The decreasing trend in diode electrical quality with increased doping density has been seen before. However, the anneal was very effective as evidenced by the doping profiles in Figure (6.21).

The MESFETs were tested with an HP4145, but only the $1x10^{12}$ cm^{-2} dosage sample provided working devices. Devices were considered non-operational when the drain current could not be modulated by an applied gate bias (Figure 6.22). The probe was placed directly on to one 100μm gate to check if an open existed but again no transistor action was observed. Consequently, given that the I-V and C-V characteristics were reasonable, the reason why the MESFETs were non-operational is unknown. Since the process was more complicated than prior processes contamination is a leading suspect.

In Figure (6.23) standard V_D vs. I_D curves for the various gate lengths of the functioning devices are plotted. The device transconductance can be calculated from these plots.

$$g_m(V_D) = \frac{I_D(V_{G_{start}}) - I_D(V_{G_{start}} + V_{G_{step}})}{V_{G_{step}}} \qquad (6.1)$$

Units for g_m reported in the literature are mS/mm where a 1μm gate length is assumed and the transconductance is reported per mm of gate width. The mobility may also be calculated after fixing $V_G = 0$. The calculated mobility is not the actual channel mobility since the effect of the source-gate and drain-gate spacing and contact resistance has not

been removed.

$$\mu = \frac{1}{n_s q R_s} = \frac{L}{n_s q w} \frac{I_D}{V_D} \tag{6.2}$$

where w = the gate width = 5μm, L = the gate length + 20μm, and n_s = sheet free carrier concentration $\simeq$(implant dosage x activation).

For comparison, g_m is calculated at V_D = 1.2 V. To calculate the mobility for the four gate lengths an 80% activation of the $1x10^{12}$ cm^{-2} implant is assumed.

Gate Length μm	g_m mS/mm	μ cm^2/V-s	V_p V
10	36	960	1.8
20	58	910	1.2
40	64	824	2.0
100	33	1650	1.8

The measured data shows a decrease in mobility with increasing gate length (except the 100μm gate). This is expected since the resistivity under the gate should be higher than the undepleted source-gate and drain-gate spacing. The large gate lengths are influenced less by the spacer; thus, for no spacer a lower mobility would be expected. Additionally, it was previously mentioned that at zero bias a $1x10^{12}$ cm^{-2} sample is depleted to the peak so that about half of the implant is depleted. Therefore, the mobility of the channel implant is significantly higher since the value of n_s used was appreciably over stated. On the other hand, the transconductance values are reasonable for this first structure. Transconductances reported in the literature are slightly above 100 mS/mm. The pinch-off voltage, V_p, is determined by selecting the lowest voltage at which I_{DS} is minimized. This usually fall in the mid 10^{-10} A range. The data shows no trend in V_p so additional devices should be tested across the wafer to look for variations.

A 20 μm device was tested in the conduction DLTS apparatus at Xerox PARC. At room temperature there was already a measurable transient due to traps; however, when the sample was heated up to investigate EL_2 the noise increased rapidly until the signal was no longer observable (Figure 6.24).

E. Selectively Implanted MESFET with Passivation

Since the motivation for the previous device was to demonstrate feasibility of conduction DLTS, the next step was to develop a MESFET process which was compatible with circuit integration. This process uses masked implants so that individual devices are isolated by the substrate. Dielectric passivation of the surface is also used. Due to a time restraint, an in depth study of the failure mechanism of the previous MESFET process was not undertaken. It was assumed that this was process related and would not appear later.

Four quarter-wafer samples were processed; two pieces were implanted with $1x10^{12}$ cm^{-2} Si^{29} while the other two were implanted with $1x10^{14}$ cm^{-2}. A sample from each dose was annealed at 850°C for 20 minutes in flowing N_2 and the remaining samples annealed in a RTA furnace at 950°C for 7 seconds in 15% H_2/Ar. This two by two matrix was selected for observing trends in deep levels induced by various anneal/dosage conditions.

The furnace annealed samples were measured with the ellipsometer and a "film" thickness of 105Å was measured. After etching in 1:1:200 $NH_4OH:H_2O_2:H_2O$ for 18 seconds (300Å) this film had increased to 165Å. Rather than aggravating the problem or etching to deep into the implant, etching was terminated. The two samples that were annealed in the RTA furnace had a few slip planes along the edges and the measured "film" thickness was 40Å.

Originally, 1200Å of Au/Ge was evaporated and the pattern lifted off prior to sputtering a 1000Å layer of SiO_2 used as a sintering cap and for isolation. This was done

on the two furnace annealed samples; however, when the low-dose sample was sintered, the Au/Ge flowed underneath the SiO_2 cap which shorted a majority of the gates (Figure 6.25). Consequently, the process was modified to its present form with the SiO_2 deposition prior to the Au/Ge evaporation. The high-dose, furnace annealed sample was reworked with the new process so that no gates were visibly shorted.

Devices were testable after the Au pads had been deposited which was prior to the surface passivation in the source-gate and drain-gate regions. Diode characteristics for the $1x10^{14}$ cm^{-2} doped, furnace annealed sample were quite leaky. On the other hand, the RTA annealed samples were mixed. The low-dose sample exhibited no forward characteristics which was similar to samples which had not been sufficiently annealed while the high-dose sample provide ϕ_B = .77 eV and n = 1.30 (Figure 6.26).

After sputtering a SiO_2 passivation layer on to portions of the three samples, they were sintered for 10 minutes at 100°C in forming gas in hopes of improving the Schottky characteristics. The reverse leakage increased; however, the low-dose RTA annealed sample provided measurable diode characteristics between the gate and source (Figure 6.27). Additional sintering at 200°C for another 10 minutes further degraded the diodes (Figure 6.28).

A HP4145 was used to measure the MESFETs which all turned out to be nonfunctional. A large number of MESFETs were measured in random locations on each sample with no gate modulation of the source-drain current observed in any device (Figure 6.29). Device-to-device leakage was measured to check whether the implant had been masked sufficiently or a surface leakage layer existed. This was done by placing probes on the sources of two adjacent devices and measuring current for a 1 volt bias. The resistance of the high-dose, furnace annealed sample was $5x10^8$ Ω while the comparable RTA annealed sample was measured at $1.4x10^8$ Ω Both of these values agree well with the resistivity specified at $> 10^6$ Ω-cm for the SI GaAs. Thus, the anneal did not create a conducting interface layer since the device coupling is in the correct range.

Source to drain resistance was measured for floating gate bias. The low-dose sample was not measurable since the curves were neither linear nor symmetrical. Two reasons for this could be that there was some depletion under the gate or that the implant was not sufficiently annealed to provide an adequate conduction path. The latter is interesting since this same dosage provided operating MESFETs in the first run. Data was measured for the two high-dosage samples (Figure 6.30).

Gate Length	Resistance (Ω)	
(μm)	Furnace	RTA
2	82	49
4	83	47
8	92	65
16	135	78
32	-	99

A simple model can be used to interpret this data if it is assumed that the sheet resistance over the area is constant and there is no influence from depletion regions.

$$R = 2R_c + \frac{R_s L}{W} = 2R_c + \frac{R_s(6 + L_{gate})}{100} \tag{6.3}$$

$$= mx + b \tag{6.4}$$

where: $x = L_{gate}$

$m = \text{slope} = \frac{R_s}{100}$

$b = 2R_c + \frac{6R_s}{100}$

A linear fit of the data provides these two equations:

$$R_{furnace} = 3.93x + 68.5 \tag{6.5a}$$

$$R_{RTA} = 1.73x + 46.1 \tag{6.5b}$$

The value for sheet resistance can be obtained from the slope.

Anneal Type	Sheet Resistance (Ω)	Contact Resistance (Ω)
Furnace	393	27.4
RTA	173	17.8

Though the resistivity is improved by RTA, a statement on the effectiveness of the anneal method cannot be made since the furnace annealed sample had 300Å etched away. The estimated sheet resistance for a $1x10^{14}$ cm^{-2} dose assuming mobility of 1000 cm^2/V-s and 100% activation is 62 Ω.

The reason for the device failure is not evident. It cannot be said that the problem is related to the mesa-isolated MESFETs since the test diodes were functional in the latter case. The major processing difference in the two cases was a different implanter and a two-month break in processing which allowed for unobserved equipment drift. The quality of the SiO_2 encapsulant can not be faulted since it has very little importance when a RTA anneal is used. All glassware was cleaned prior to commencing processing; however, during the first two mask steps the DI water quality was sporadic which might have introduced contamination. The most probable cause was the gate deposition. The evaporation components used only in this process had been contaminated so it was necessary to clean them followed by evaporations of gate metal to trap in remaining contaminates. In addition, during the two month absence the evaporator had become increasingly contaminated with bluish carbon deposits visible. Since the titanium evaporation is carried out at high temperatures, it would be easy for the carbon to outgas. Contamination was also evidenced by a higher evaporation pressure; previously, the mid 10^{-7} Torr range had been obtained but in this run only the low 10^{-6} range was obtained. gate metal is the variations seen in previous diode characteristics for similarly processed samples; for example, the mid-dosage set in the two-metal Schottky experiment (Figure 6.19b).

In retrospect, the previous MESFET was designed with isolation and passivation in mind. An improved version would remove photoresist from contacting the surface of the

active region throughout the process and eliminate one mask. The first step would be to reverse mask #1 and mask #2 which would improve alignment resolution and remove resist from the active region (Figure 5.8b). In order to protect the surface, the anneal encapsulant is not stripped, but rather after patterning the photoresist for metal deposition, the resist is used to pattern the SiO_2 etch prior to evaporation. This removes the need to expose the active region and to bring the gate metal up over the oxide edge to the pad. Thus, the gate is brought out to a contact which can then be contacted with the first-level metalization/pad. For the furnace annealed samples with about 7500Å of SiO_2 for encapsulation, the step should not be difficult since HF attacks SiO_2 isotropically making a gently step for the 2000Å first-level metal.

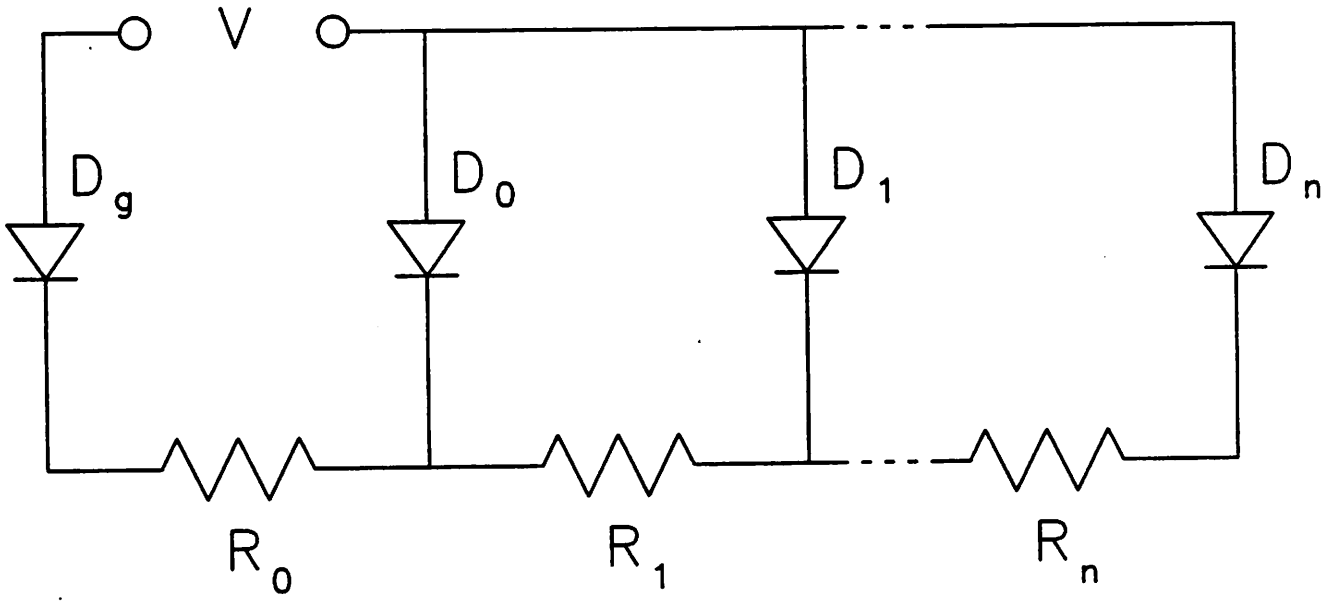


Figure 6.1 Circuit model for the single-metal Schottky diode. The resistance of the semi-insulating substrate is assumed to be infinite. The response to an applied bias is measured at V.

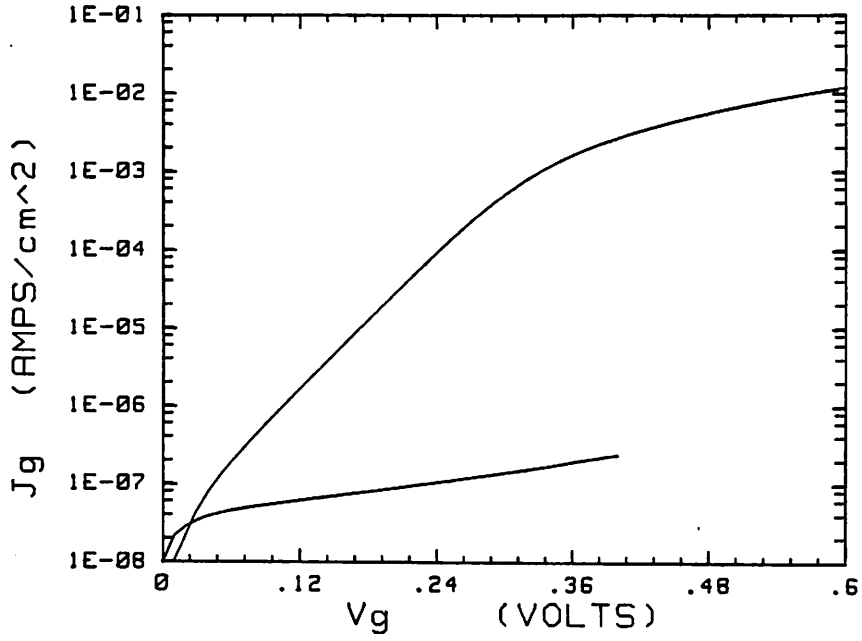


Figure 6.2a ϕ_B = .81eV. n = 1.07 and sample area = 2.5 cm^2. This was the best electrical characteristics obtained for Ti on n-type GaAs (10^{18} cm^{-3} Te doped).

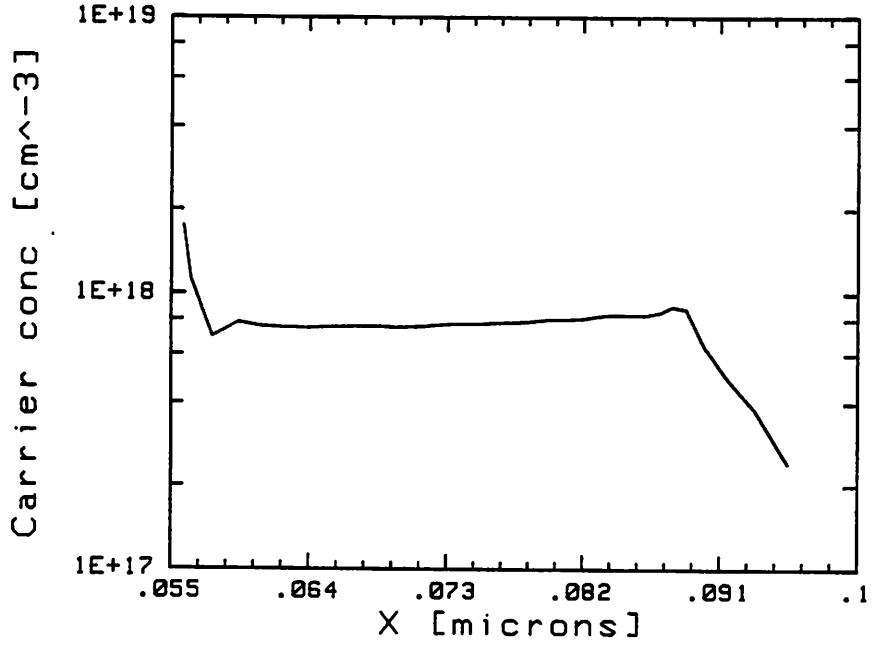


Figure 6.2b A C-V measurement on the above sample provided a doping profile in good agreement with manufactures doping specifications. The drop on the right is caused by large gate leakage above 3.0 V while the drop on the left is caused by leakage current effectively decreasing the depletion width.

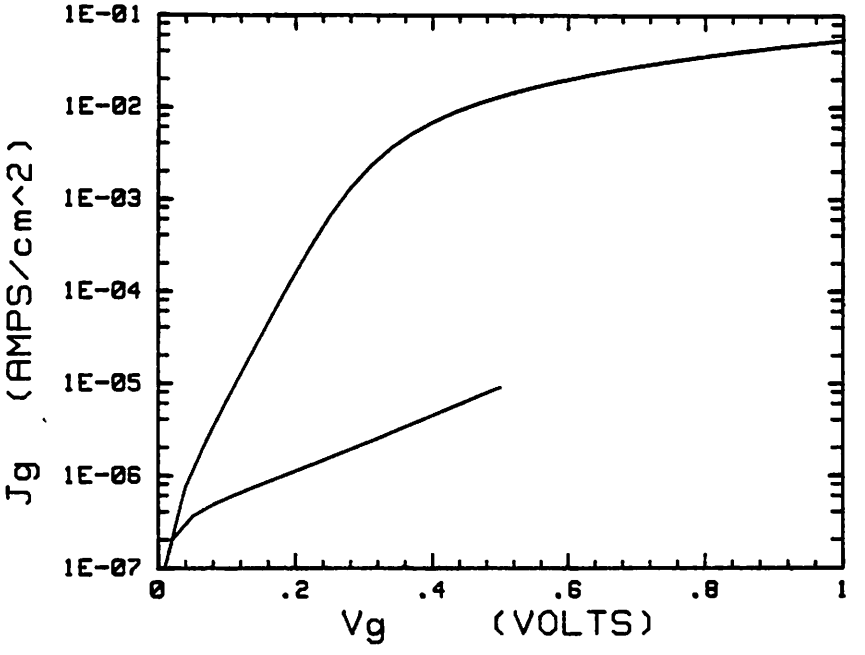


Figure 6.3 ϕ_B = .74 eV, n = 1.28 and sample area = 2.0 cm^2. This sample was processed with the previous sample (Figure 6.2); however, the metal was deposited on this sample prior to the previous sample. One possible explanation is that the electrical characteristics improve with usage of the evaporation system.

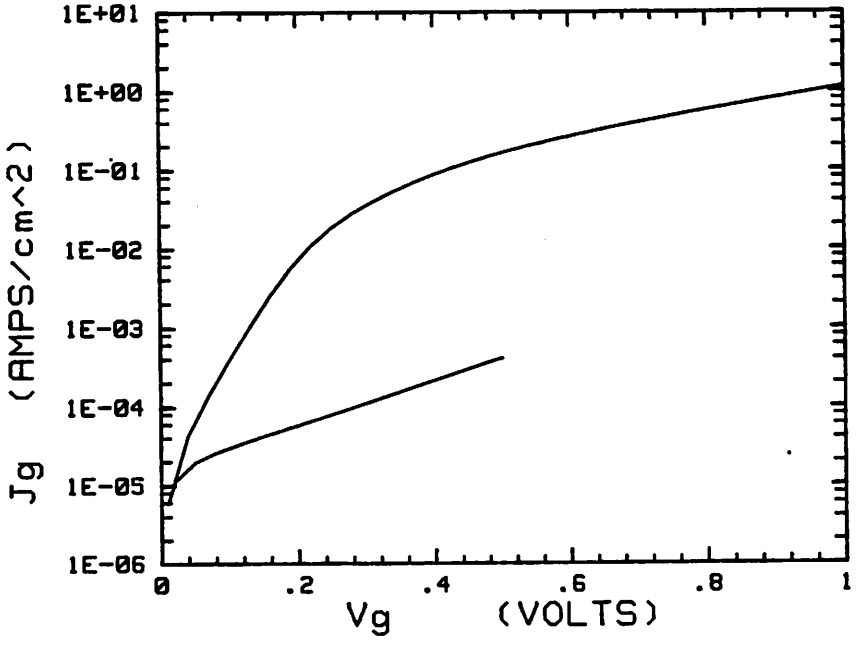


Figure 6.4 ϕ_B = .64 eV, n = 1.16 and sample area = 0.5 cm^2. The metal deposition was concurrent with the sample of Figure (6.3).

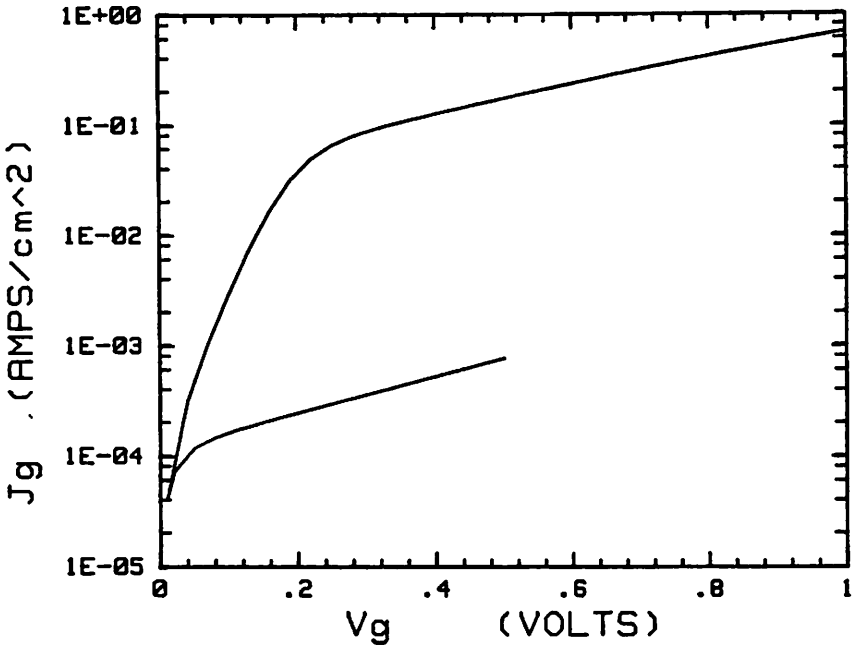


Figure 6.5 ϕ_B = .60 eV, n = 1.00 and sample area = 0.4 cm^2. This sample was cleaved from the sample measured in Figure (6.2) and then sintered in flowing nitrogen for 35 minutes at 250°C. Sintering caused a large drop in barrier height but improved the ideality factor.

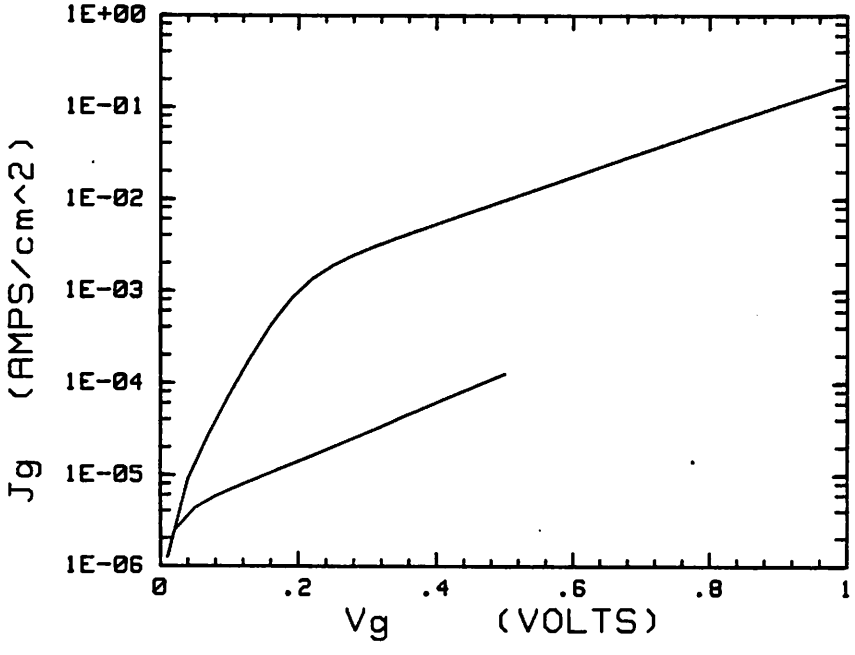


Figure 6.6 ϕ_B = .68 eV, n = 1.21 and sample area = 0.5 cm^2. This sample was etched with 1:1:50 $NH_4OH:H_2O_2:H_2O$ prior to metal deposition rather than with HCl.

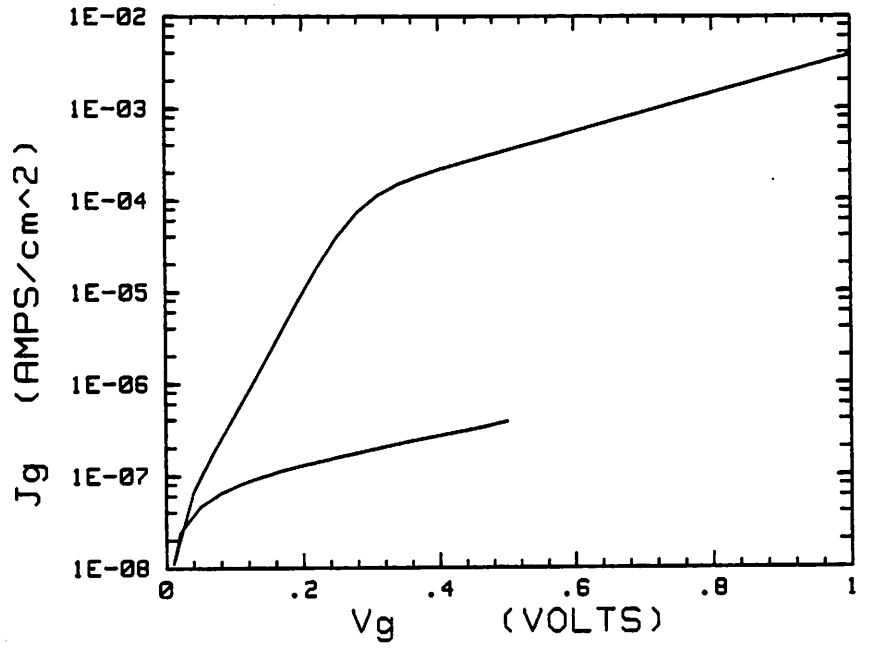


Figure 6.7 ϕ_B = .81 eV, n = 1.27 and sample area = 0.5 cm^2. An improved barrier height was obtained with an initial 10 to 20 second "pre-evaporation" prior to opening the shutter and evaporating on to the sample. This technique coats the internal surfaces of the evaporation chamber with metal which reduces contamination.

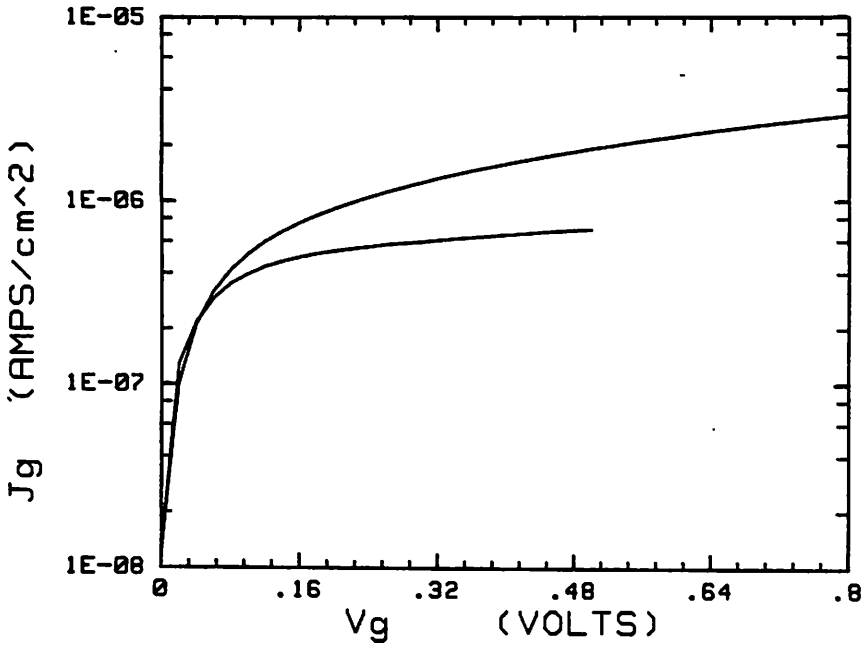


Figure 6.8a After annealing at 800°C for 30 minutes in flowing nitrogen this sample exhibits no forward characteristics. These J-V characteristics resemble a constant resistance.

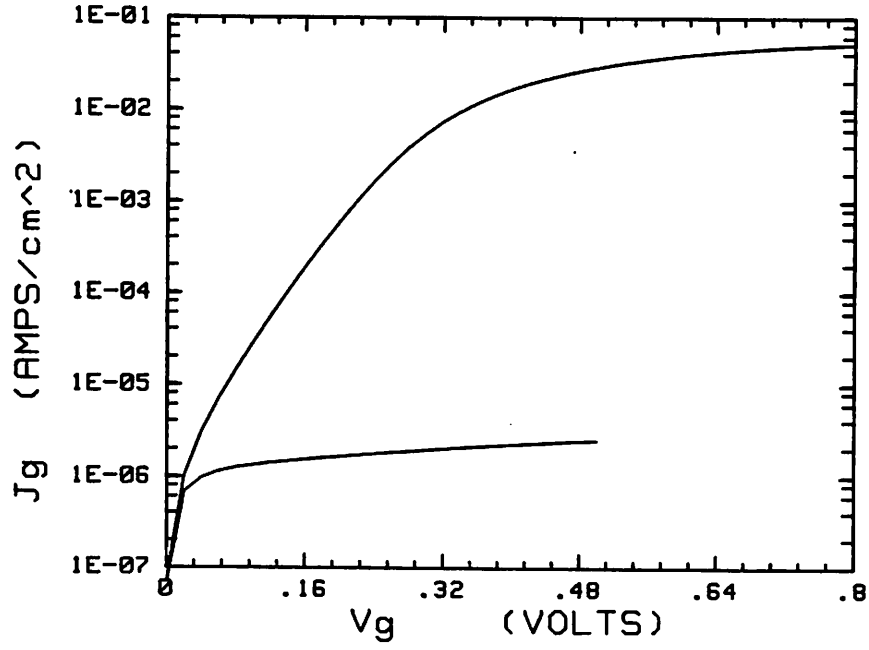


Figure 6.8b ϕ_B = .70 eV and n = 1.21. after annealing at 850°C for 30 minutes in flowing nitrogen reasonable J-V characteristics were obtained even though poor quality SiO_2 caused a bad surface.

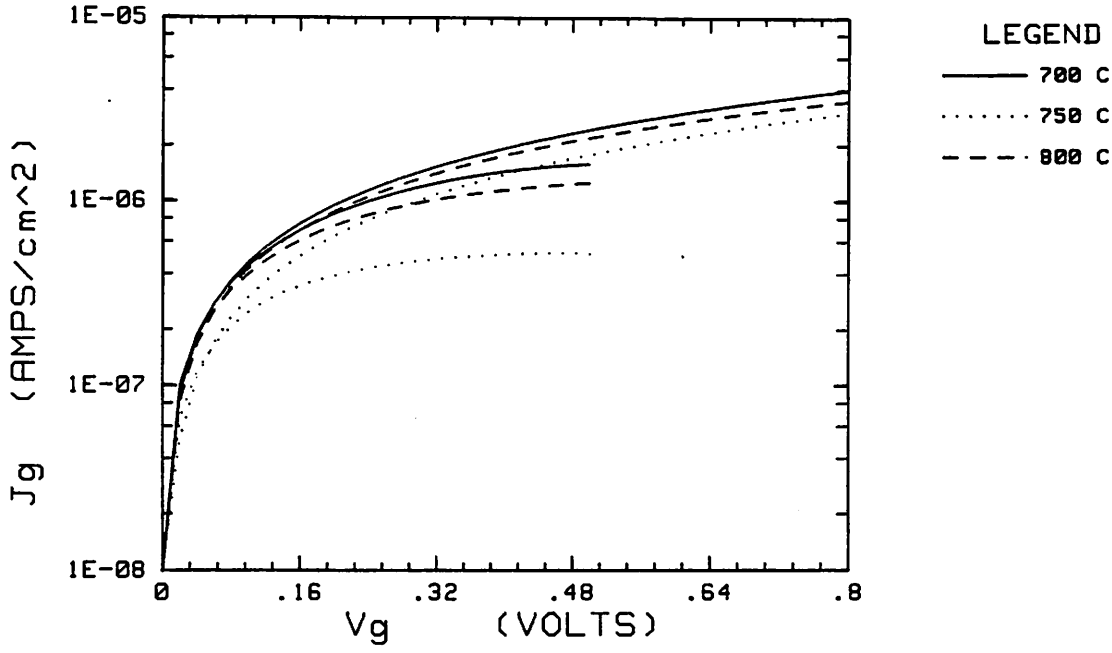


Figure 6.9a No forward characteristics could be measured for these 3 samples which were annealed at the indicated temperatures in forming gas for 30 minutes.

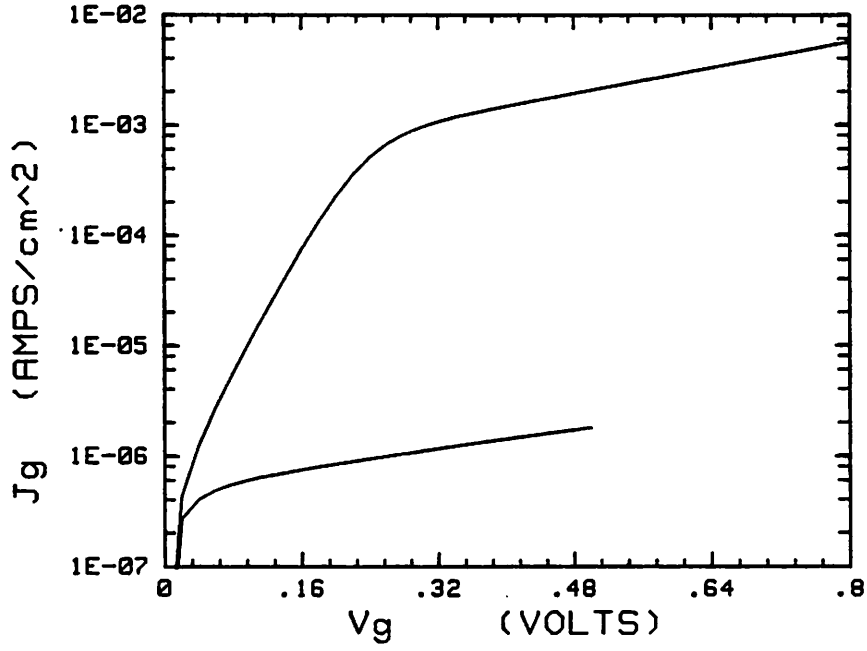


Figure 6.9b ϕ_B = .735 eV and n = 1.14. This sample was metalized together with the previous samples but the 900°C anneal temperature appears to have activated the dopant and restored the crystallinity.

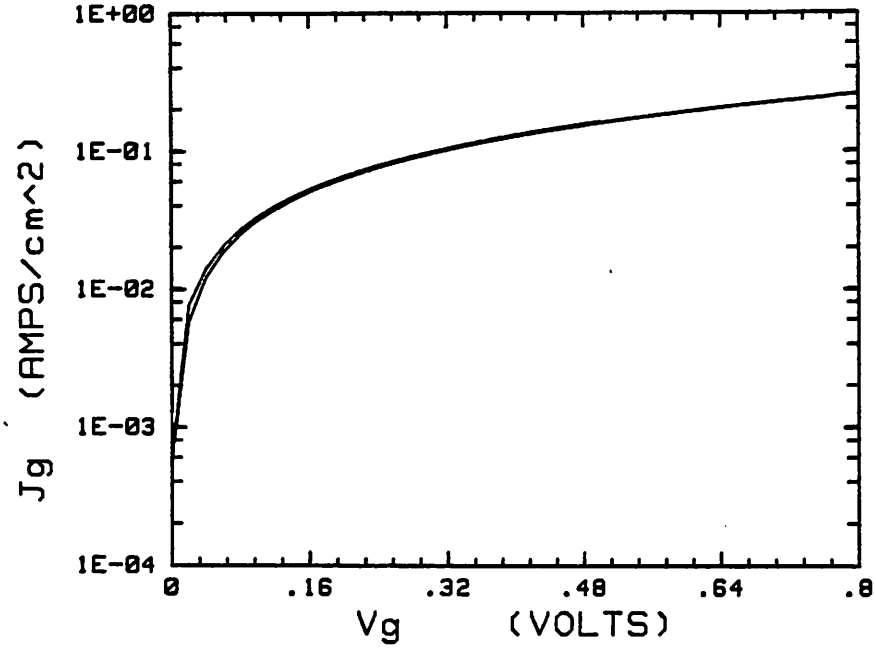


Figure 6.10 This control sample which was not annealed shows no diode characteristics. The amorphous layer created by the implant is probably the cause of the high device conductance.

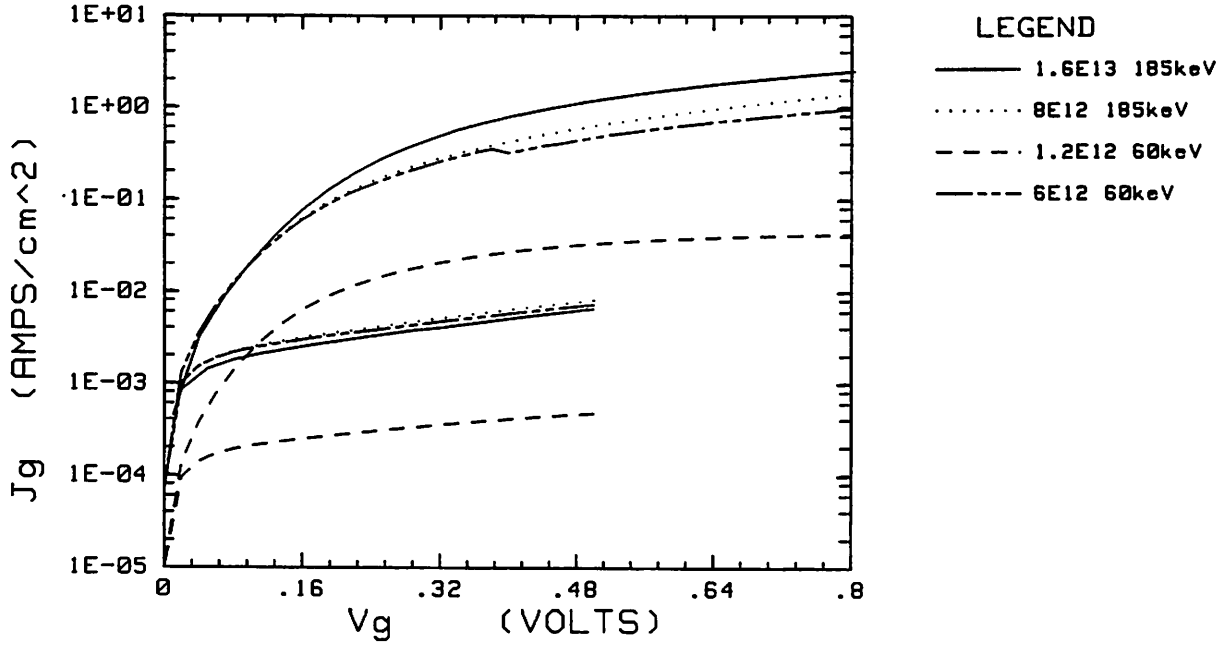


Figure 6.11 The high reverse leakage current (ie. low barrier height) may have been caused by an oxygen ash, prior to annealing, used to remove organic contaminates.

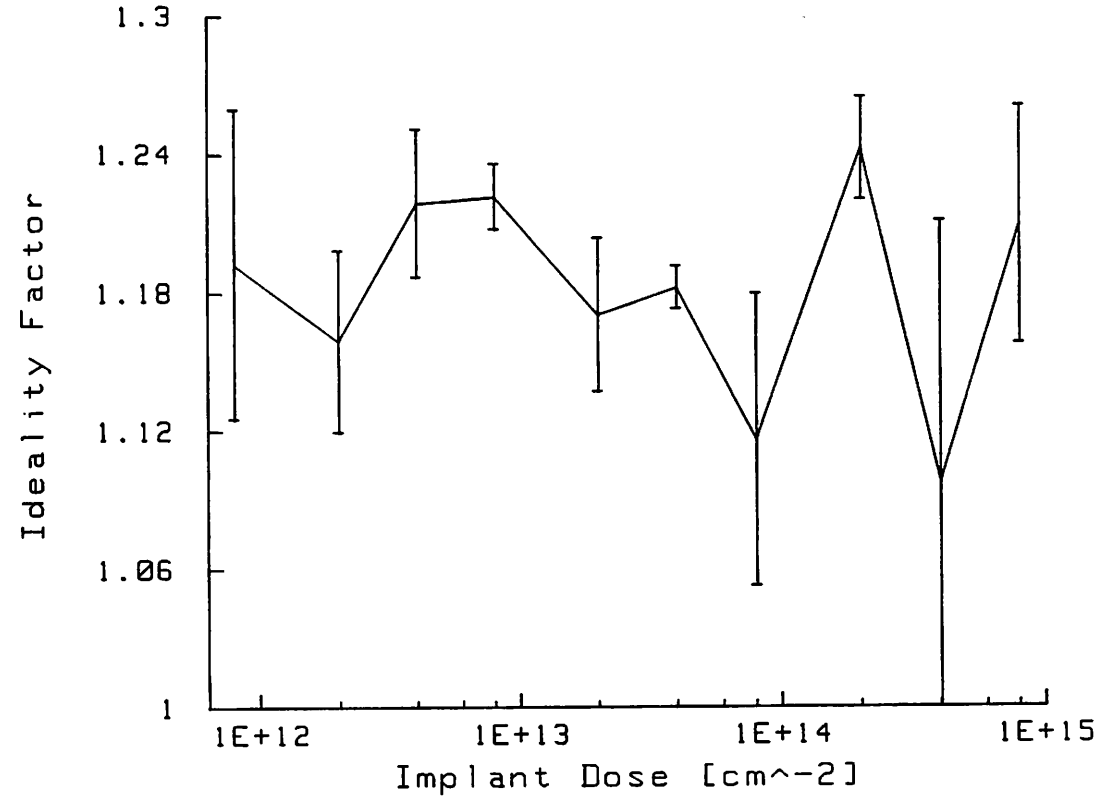


Figure 6.12a Ideality factors for 12 samples processed in lots of four. The implant energy was 120 keV and the samples were annealed face down in flowing nitrogen for 30 minutes. The data represents the average of at least three devices with one sigma error bars.

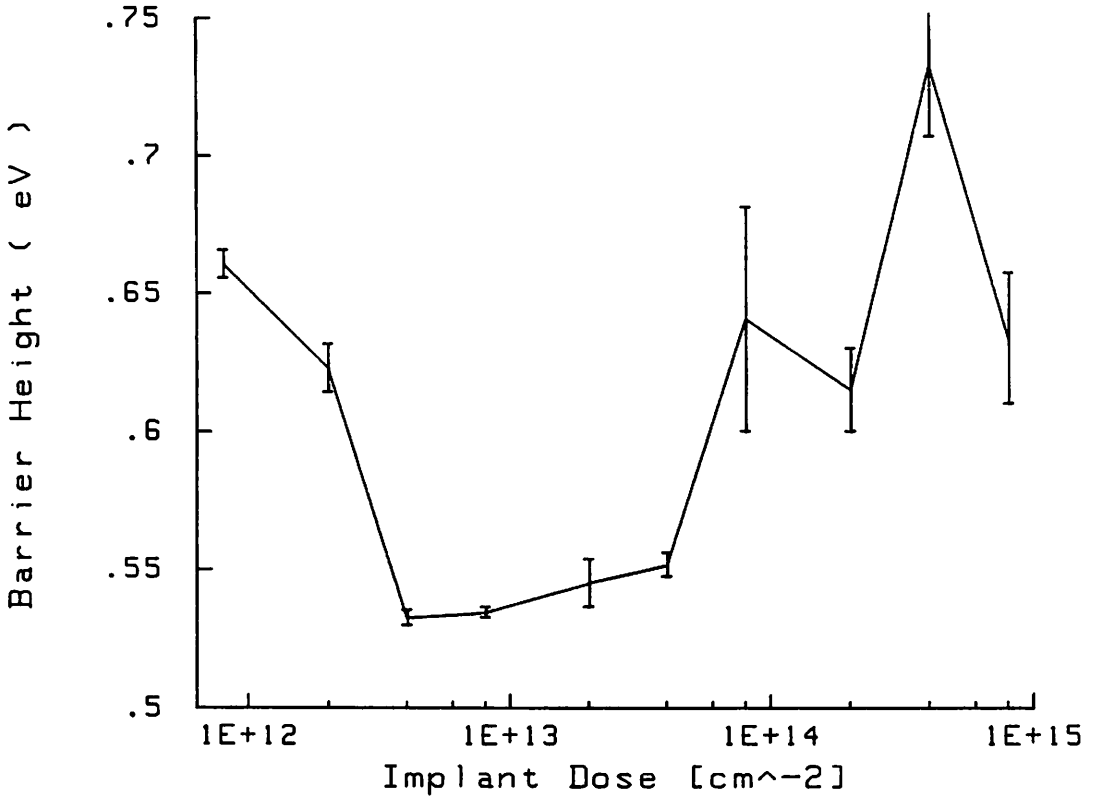


Figure 6.12b The barrier heights measured from the samples of Figure (6.12a). The data represents the average of at least three devices with one sigma error bars.

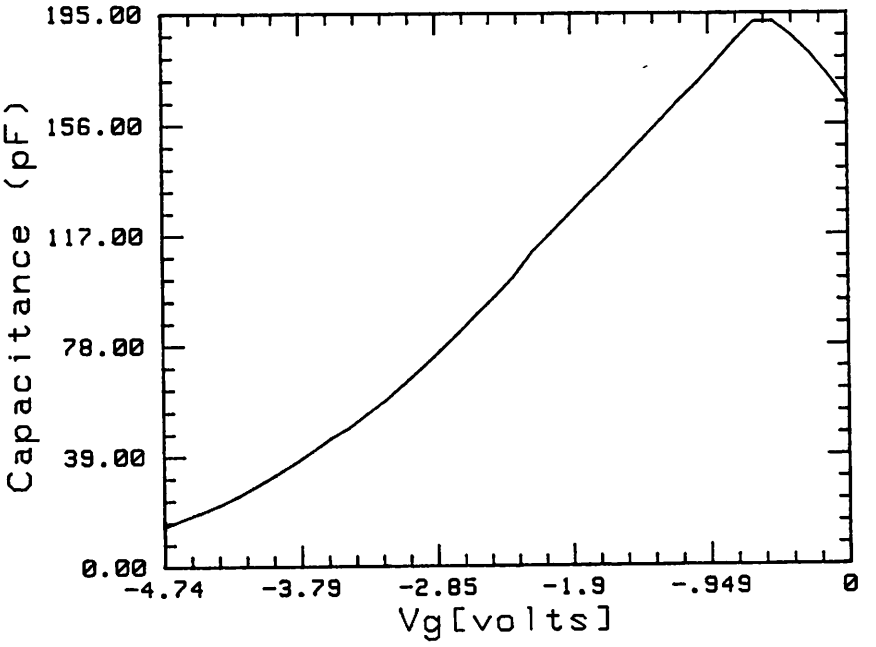


Figure 6.13 The initial rise in capacitance for increased reverse bias is displayed in this typical C-V plot. The rise is due to an effective decrease in depletion width due to a large reverse leakage current. Calculating a doping profile from the first part of this curve will result in an infinite doping concentration where the slopes changes.

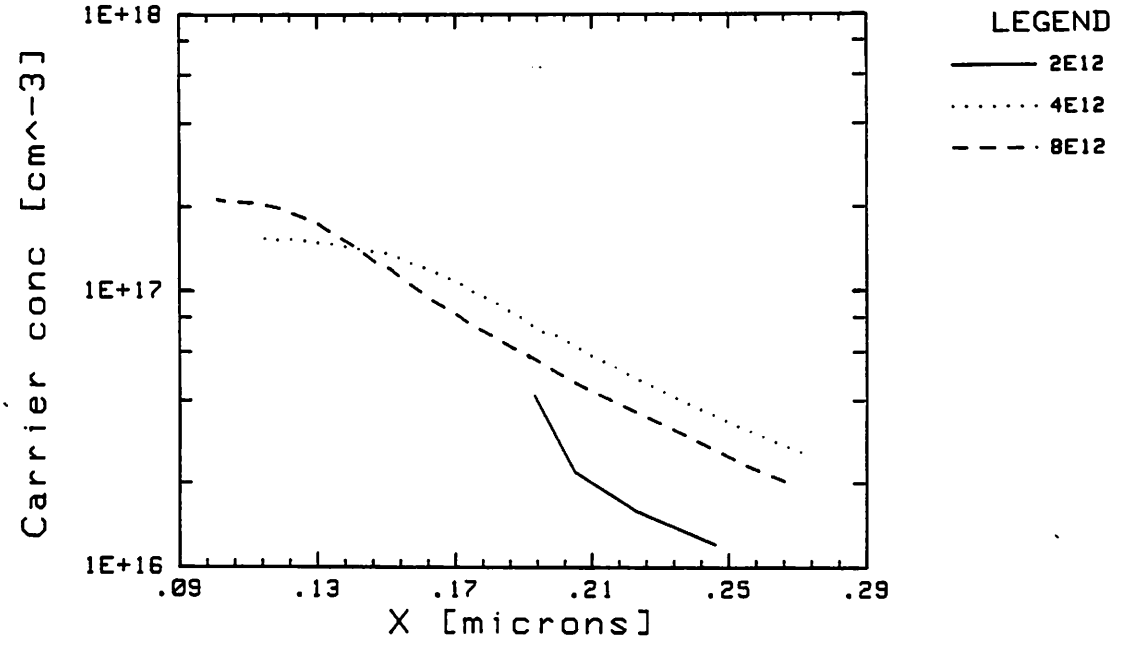


Figure 6.14a Doping profiles for the samples plotted in Figure (6.12).

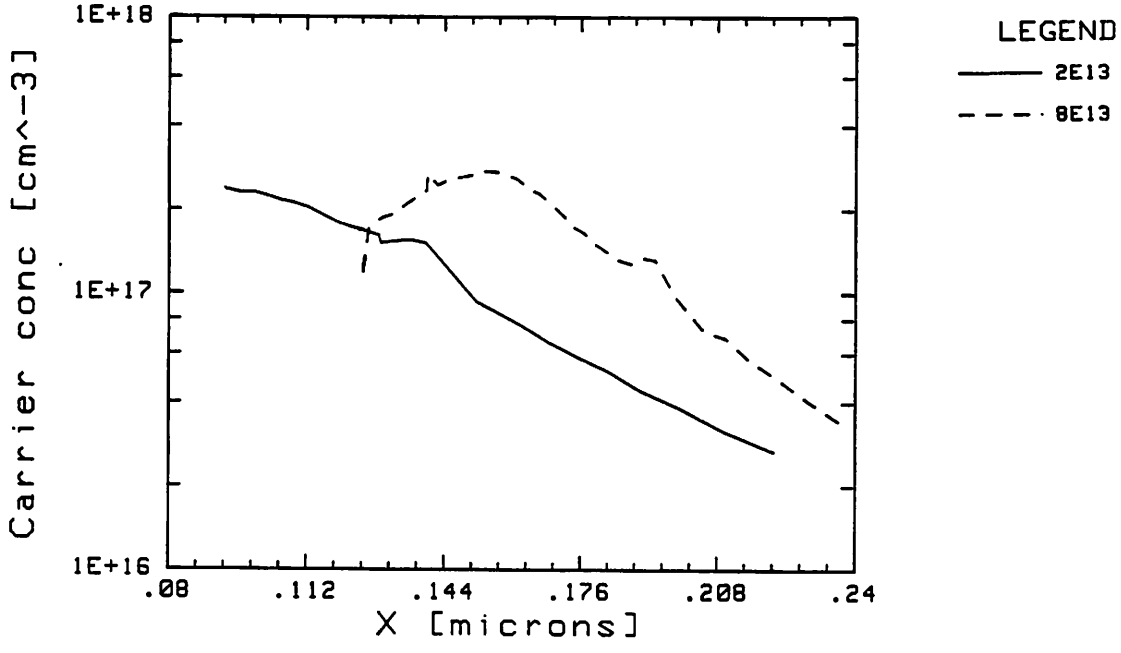


Figure 6.14b Doping profiles for the samples plotted in Figure (6.12).

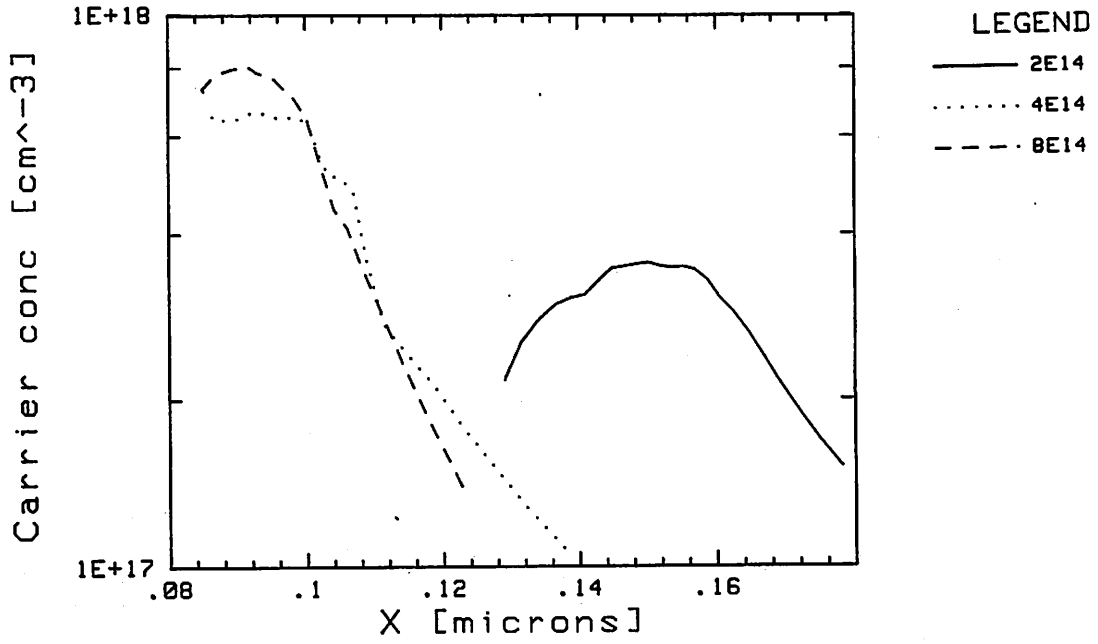


Figure 6.14c Doping profiles for the samples plotted in Figure (6.12).

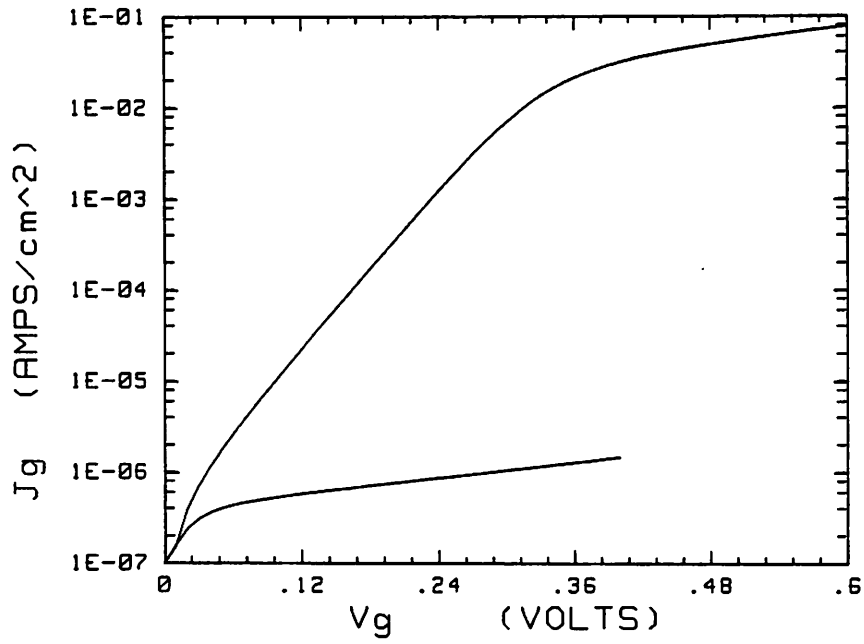


Figure 6.15 ϕ_B = .74 eV and n = 1.09. The best J-V characteristics attained with the present annealing techniques. The anneal conditions are 26 minutes at 850°C in flowing nitrogen with push and polls of 5 minutes each. The samples were encapsulated with 7500Å of SiO_2 on the front and 5000Å on the back and placed face down on a Si wafer.

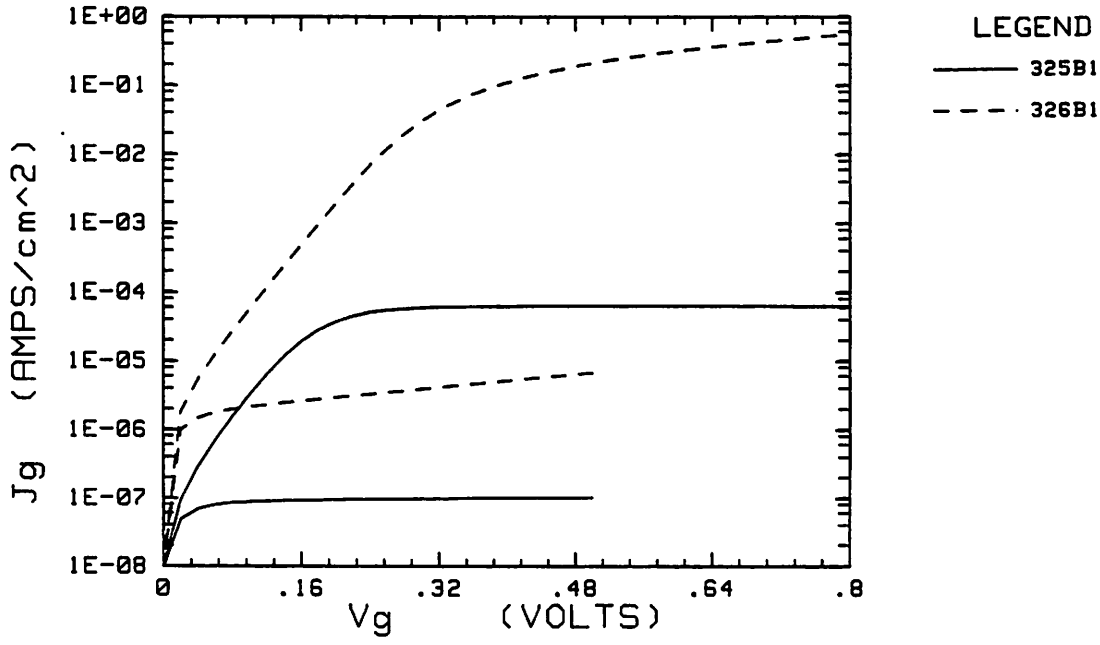


Figure 6.16 Sample 325B1: ϕ_B = .70 eV and n = 1.0. Sample 326B1: ϕ_B = .77 eV and n = 1.0. The J-V characteristics improved when the samples were etched in 1:1:100 $NH_4OH:H_2O_2:H_2O$ for 20 seconds.

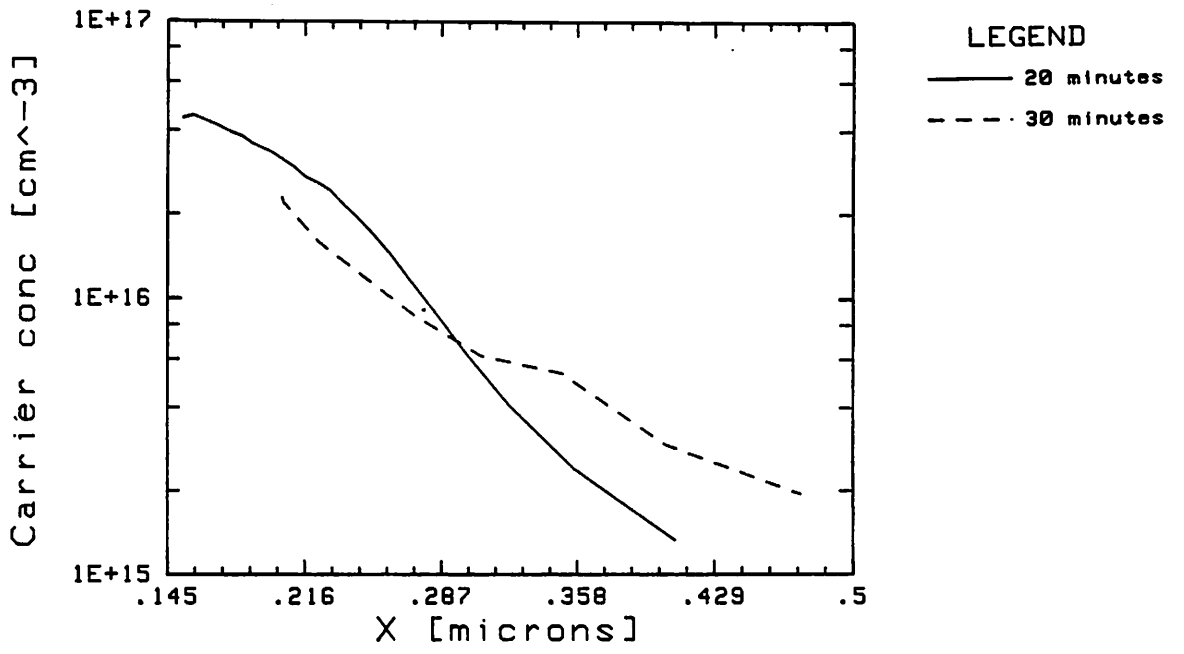


Figure 6.17 Approximately the same activation is obtained with both a 20 minute and 30 minute anneal.

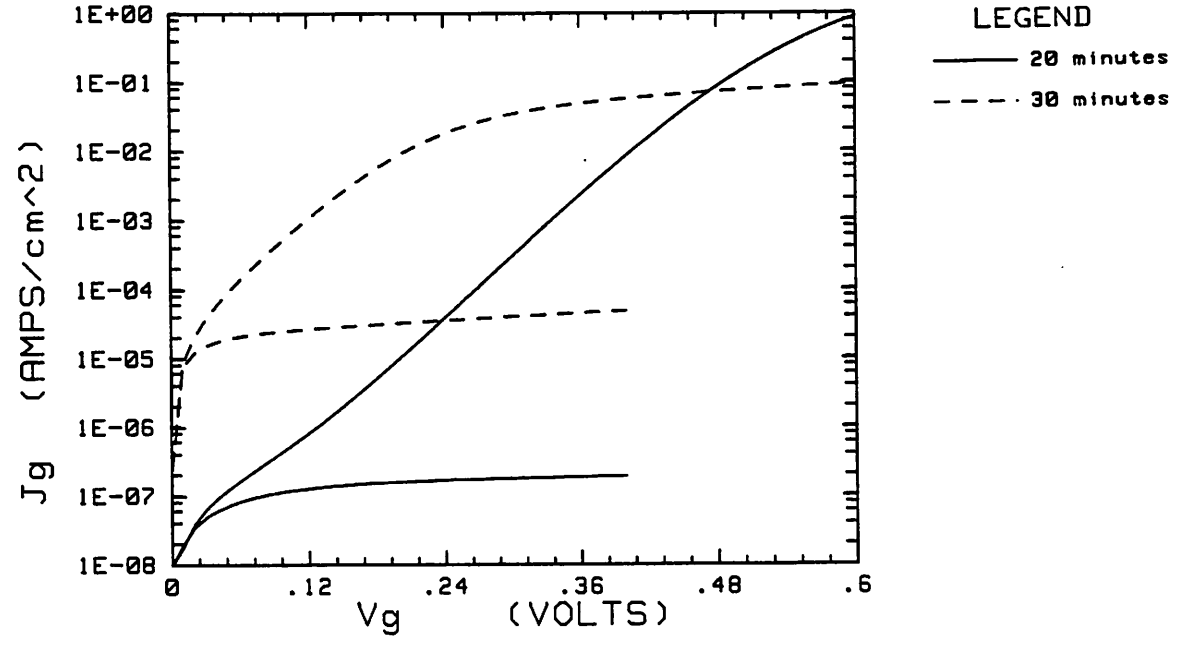


Figure 6.18 A better surface is obtained with a shorter anneal which is demonstrated here by the improved diode reverse leakage current. The sample annealed for 20 minutes (ϕ_B = .82 eV and n = 1.15) was fabricated with the two-metal Schottky structure which may account for part of the improved results.

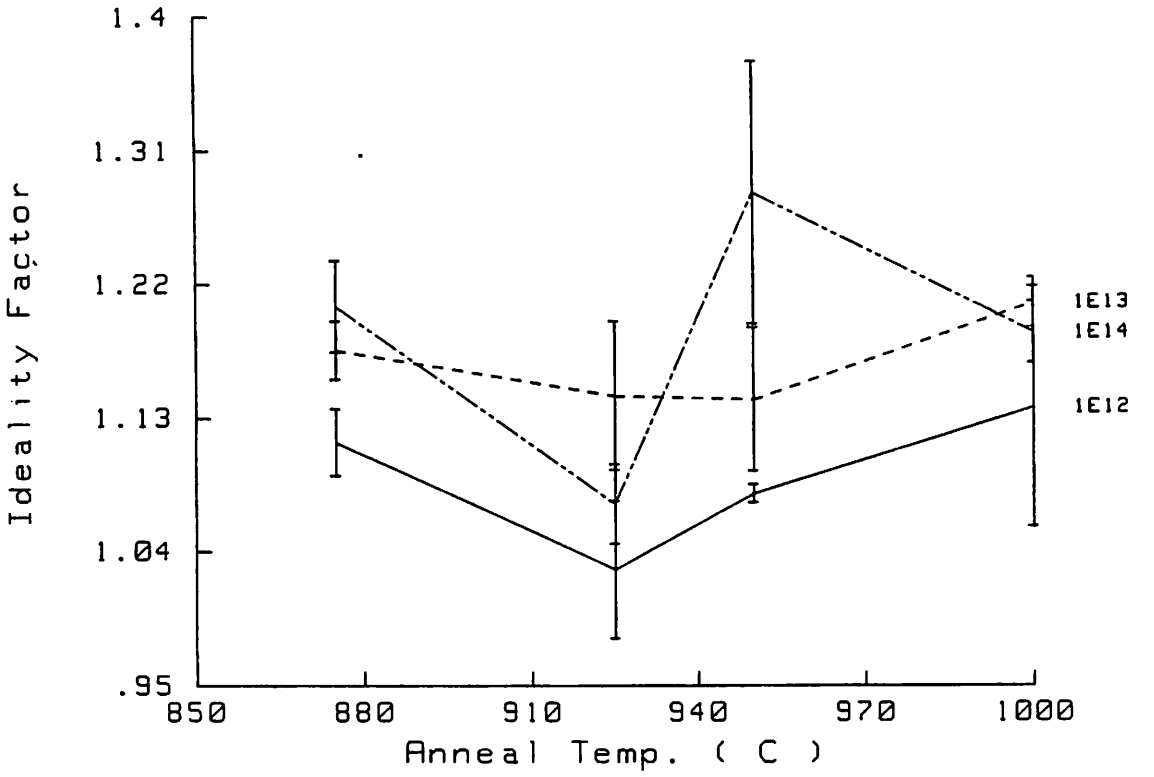


Figure 6.19a These samples were annealed in a RTA furnace for 5 seconds in 15%H_2/Ar. The samples were metalized in batches according to their dosage. The data represents the average of at least three devices with one sigma error bars.

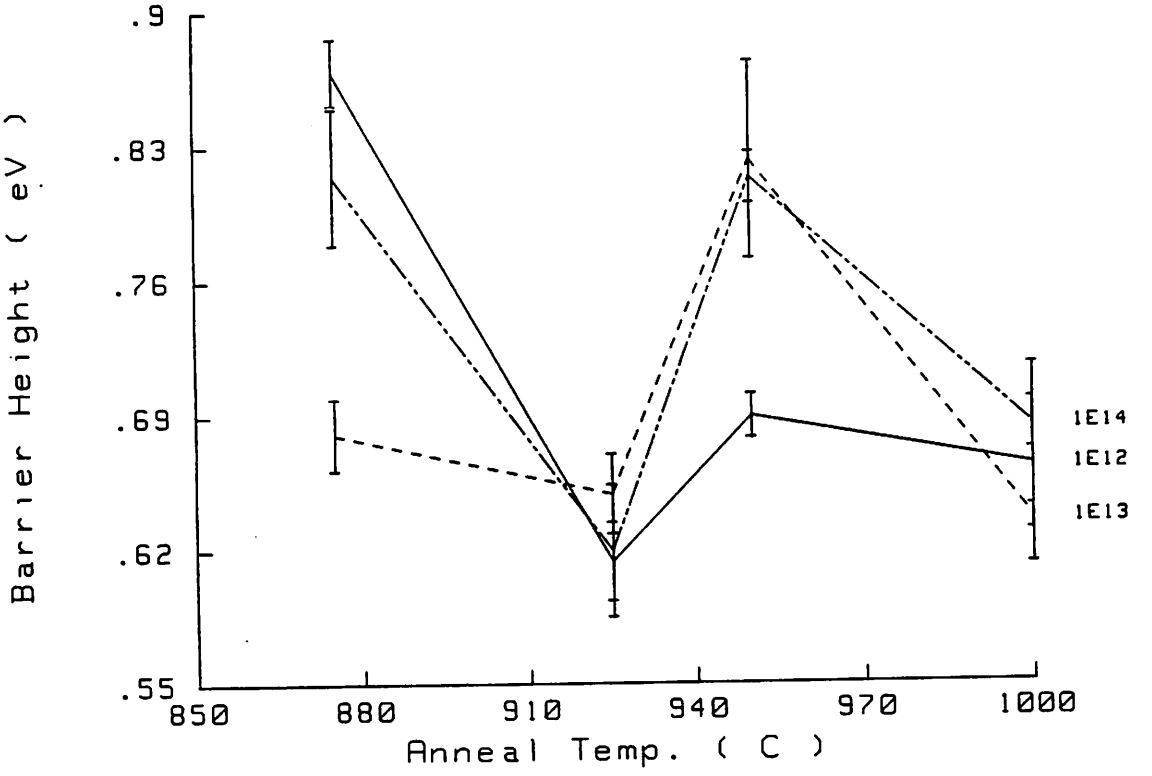


Figure 6.19b The barrier heights for the samples in Figure (6.19a). The data represents the average of at least three devices with one sigma error bars.

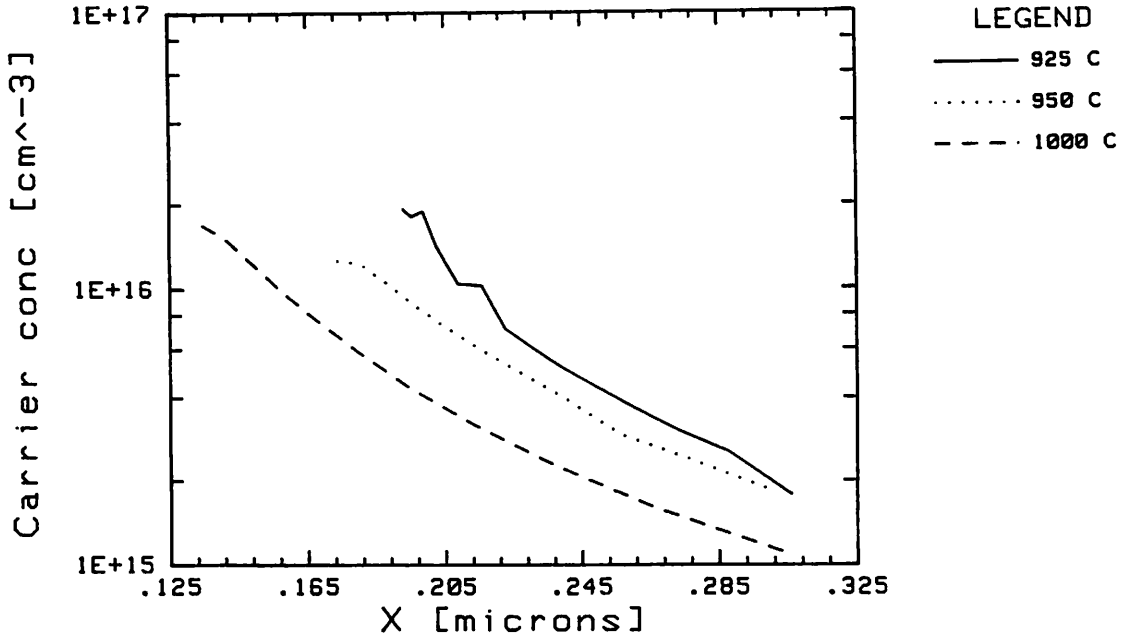


Figure 6.20a The activation of a $1x10^{12}$ cm^{-2} implant for various RTA temperatures.

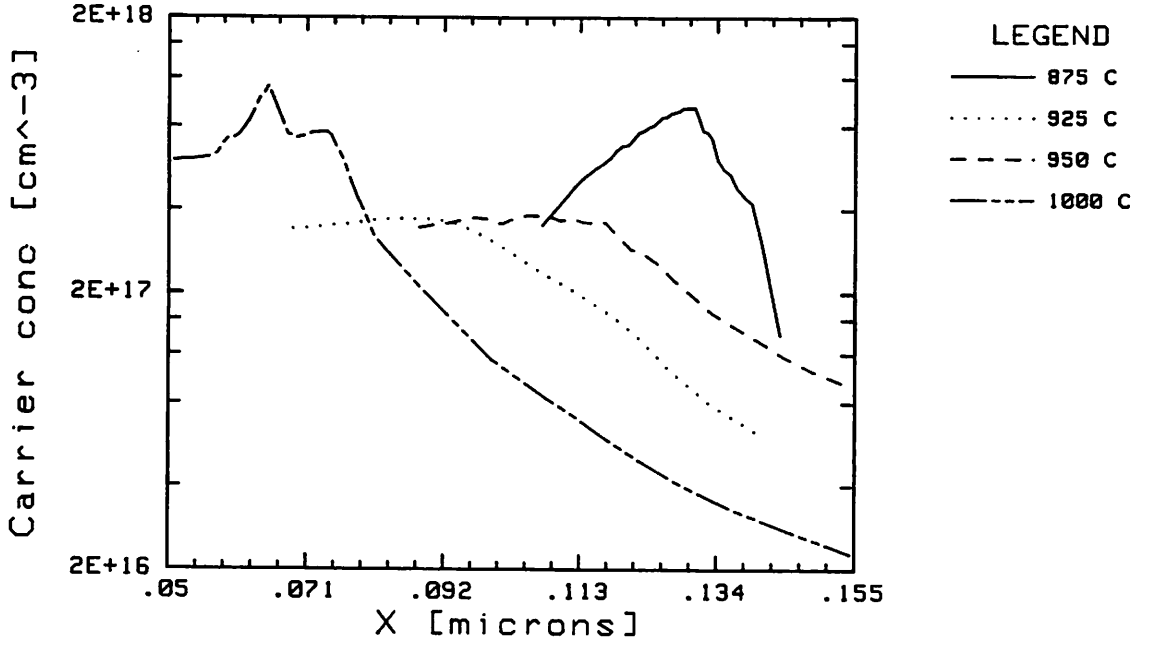


Figure 6.20b The activation of a $1x10^{13}$ cm^{-2} implant for various RTA temperatures.

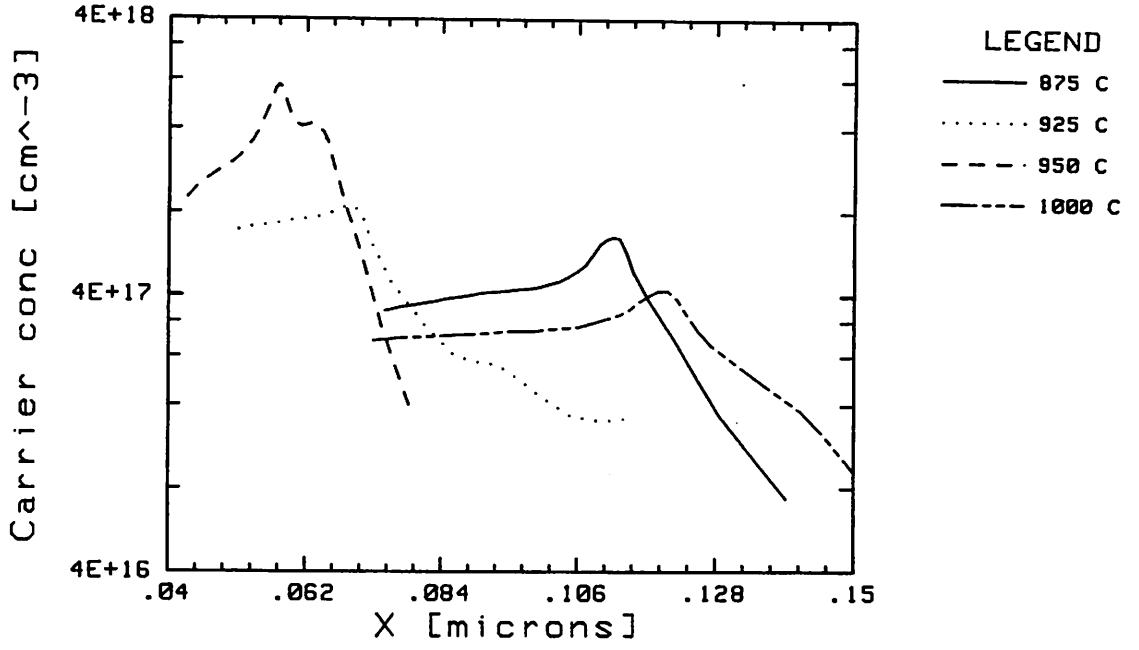


Figure 6.20c The activation of a $1x10^{14}$ cm^{-2} implant for various RTA temperatures.

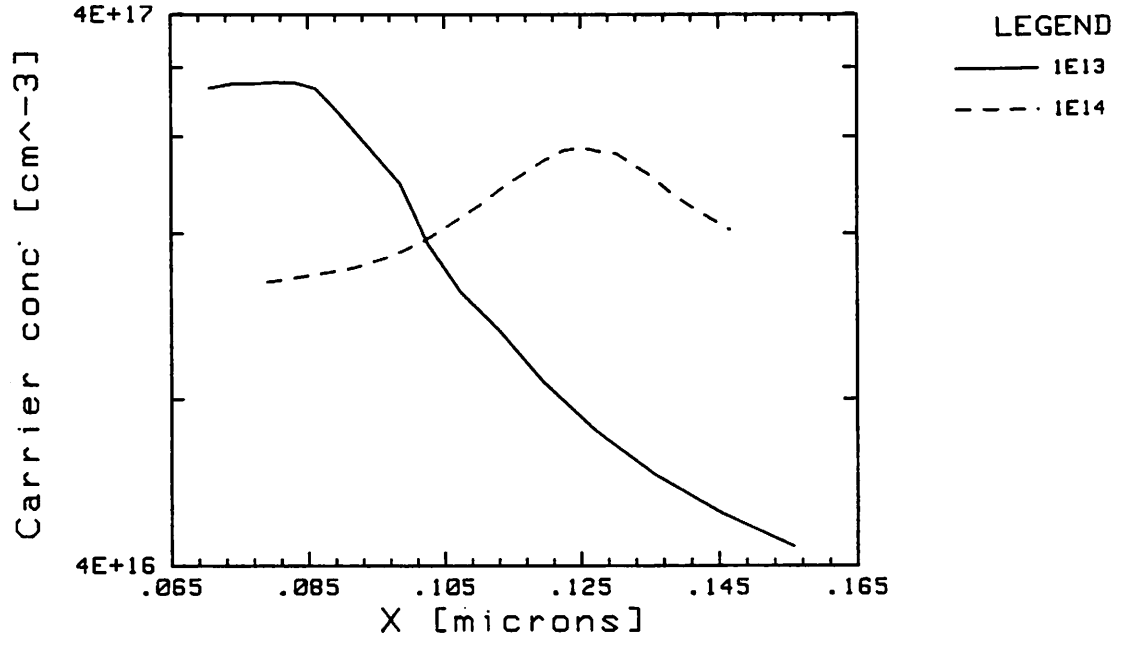


Figure 6.21 Doping profiles calculated from C-V measurements of test diodes on the 3 samples fabricated with mesa-isolated MESFETs.

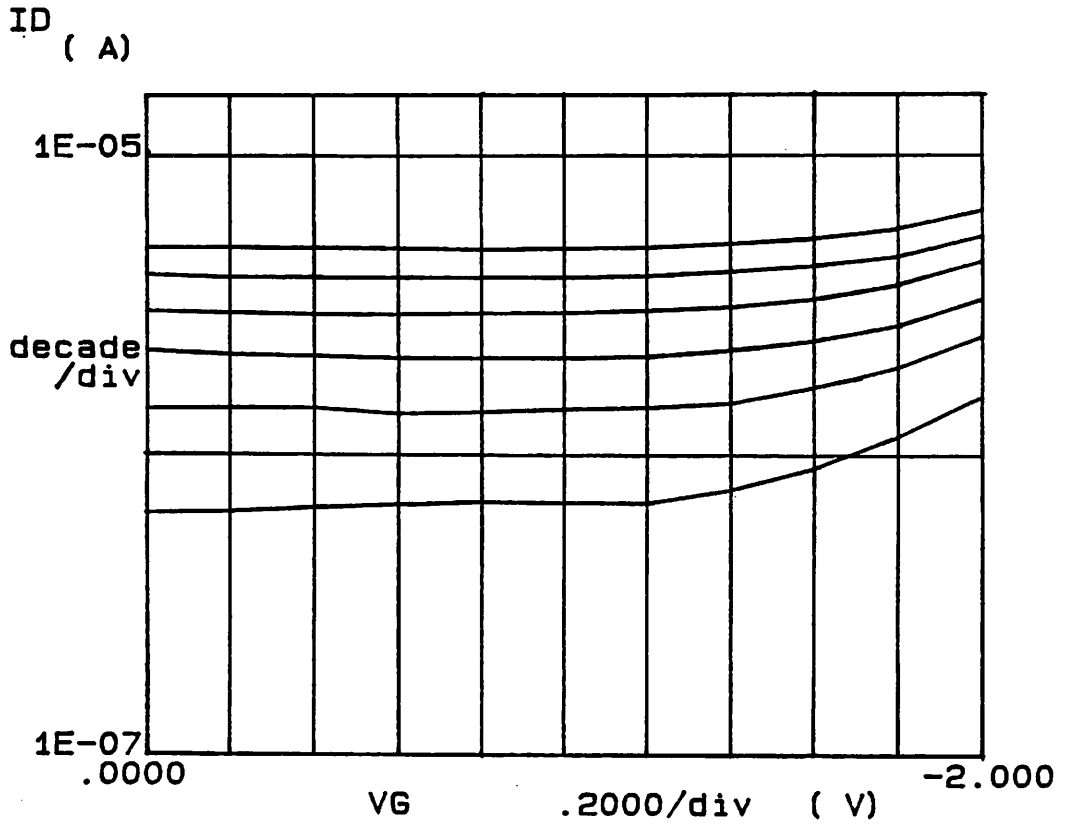


Figure 6.22a $V_{D_{start}}$ = .05 V and $V_{D_{step}}$ = .05 V. No drain modulation is exhibited by the 100μm gate MESFET which was implanted with $1x10^{13}$ cm^{-2}. Gate leakage current is responsible for the upward curve on the right. The mobility calculated from these curves is approximately $\frac{750}{\lambda}$ cm^2/ V–s where λ is the fraction of electrical activation (neglecting contact resistance).

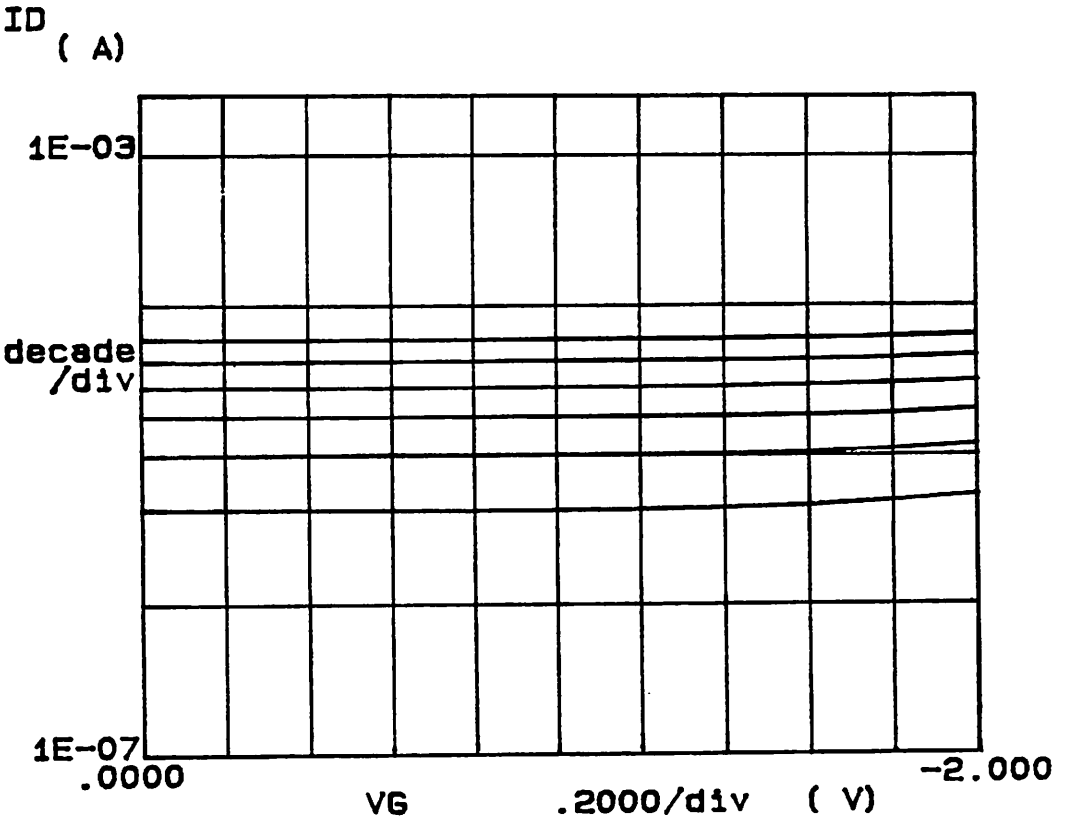


Figure 6.22b $V_{D_{start}}$ = .05 V and $V_{D_{step}}$ = .05 V. No drain current modulation is exhibited by this 100 μm MESFET which was implanted with $1x10^{14}$ cm^{-2}. The mobility calculated from these curves is approximately $\frac{533}{\lambda}$ cm^2/ V–s where λ is the fraction of electrical activation (neglecting contact resistance).

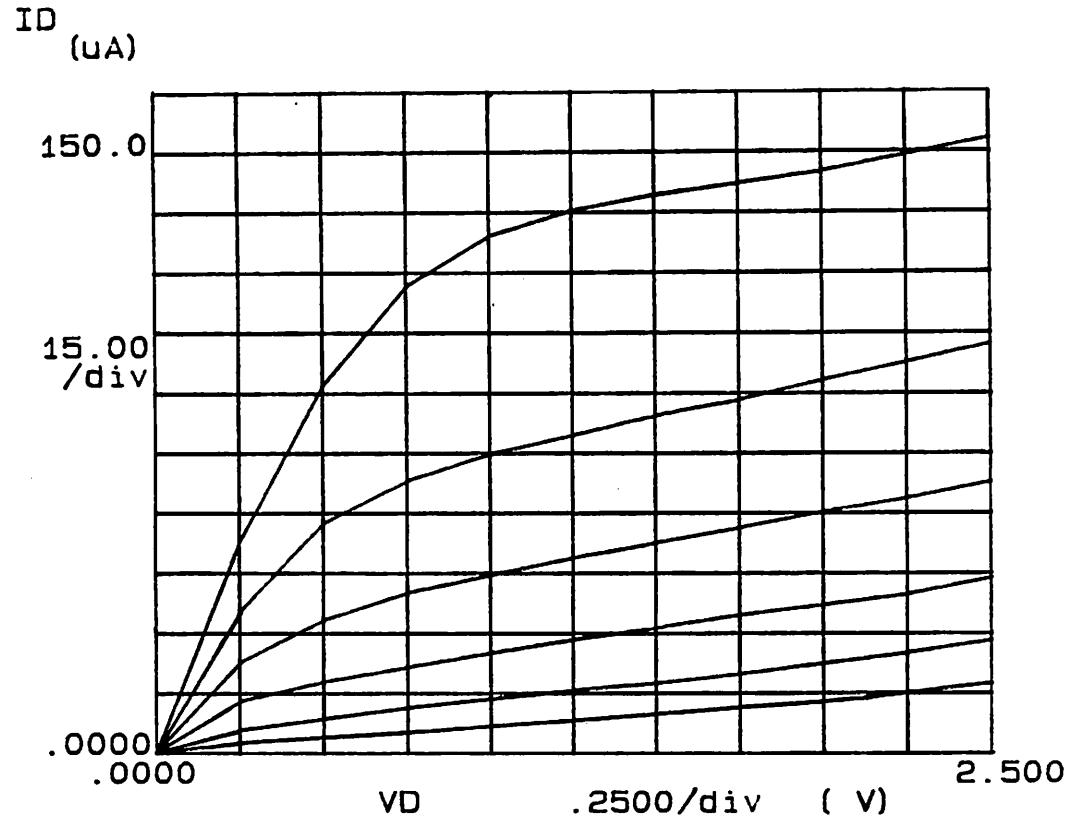


Figure 6.23a $V_{G_{start}} = 0$ V and $V_{G_{step}} = -0.3$ V. I-V characteristics for a 10 μm gate length implanted with $1x10^{12}$ cm^{-2} Si^{29}.

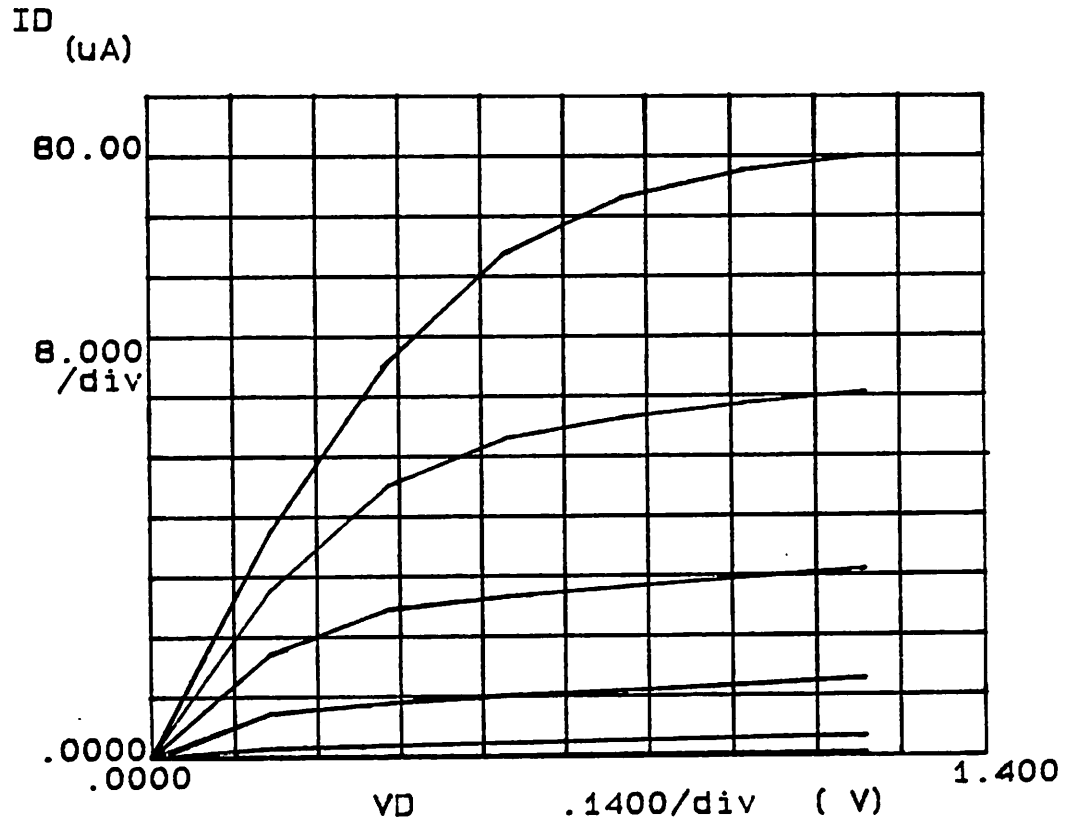


Figure 6.23b $V_{G_{start}} = 0$ V and $V_{G_{step}} = -0.18$ V. I-V characteristics for a 20 μm gate length implanted with $1x10^{12}$ cm^{-2} Si^{29}.

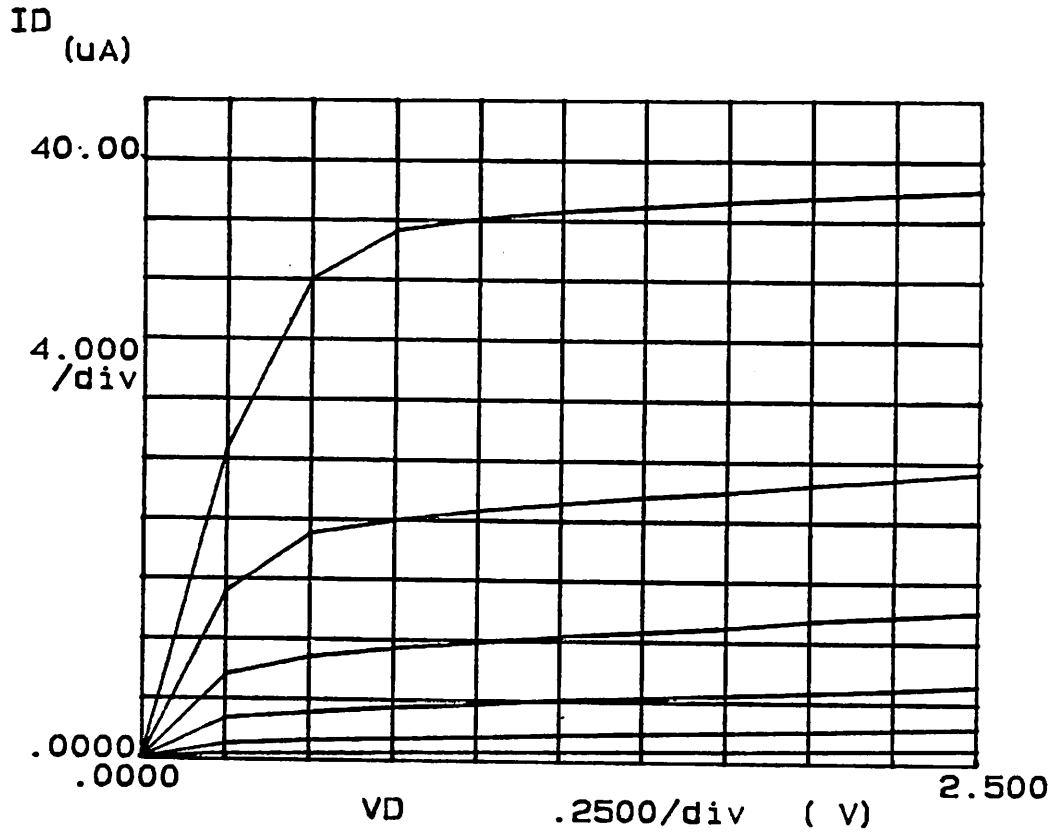


Figure 6.23c $V_{G_{start}}$ = 0 V and $V_{G_{step}}$ = −0.3 V. I-V characteristics for a 40 μm gate length implanted with $1x10^{12}$ cm^{-2} Si^{29}.

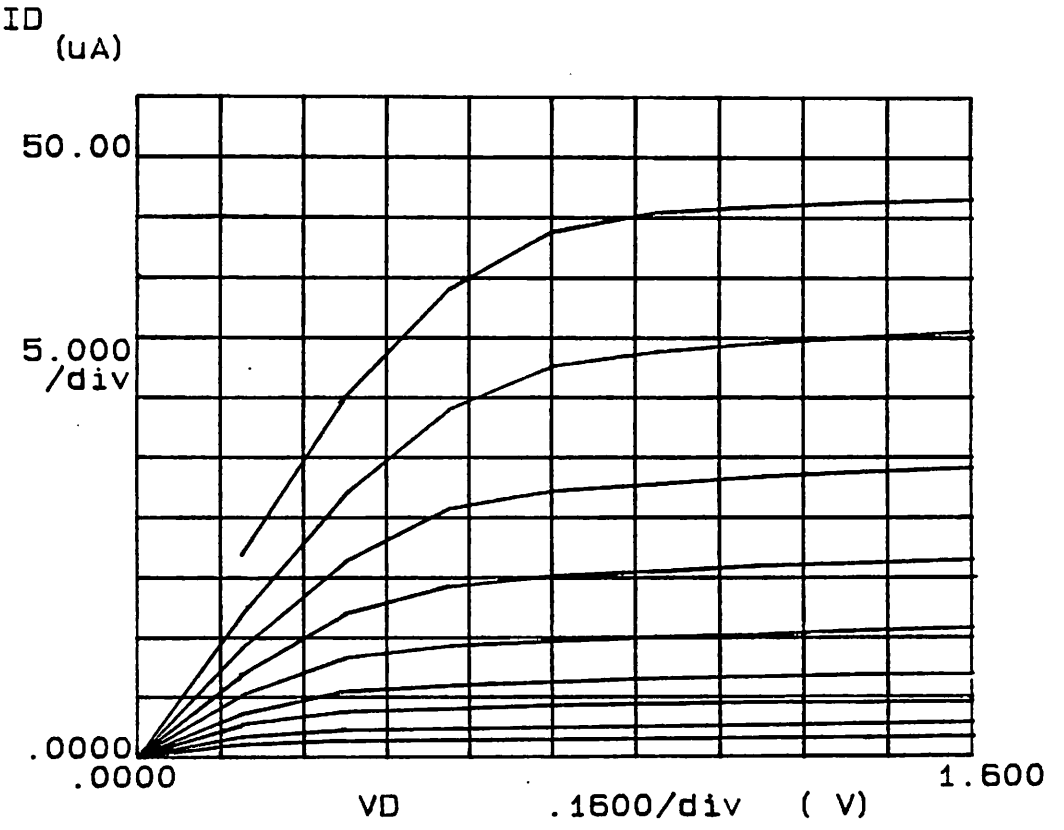


Figure 6.23d $V_{G_{start}}$ = 0 V and $V_{G_{step}}$ = 0.6 V. I-V characteristics for a 100 μm gate length implanted with $1x10^{12}$ cm^{-2} Si^{29}.

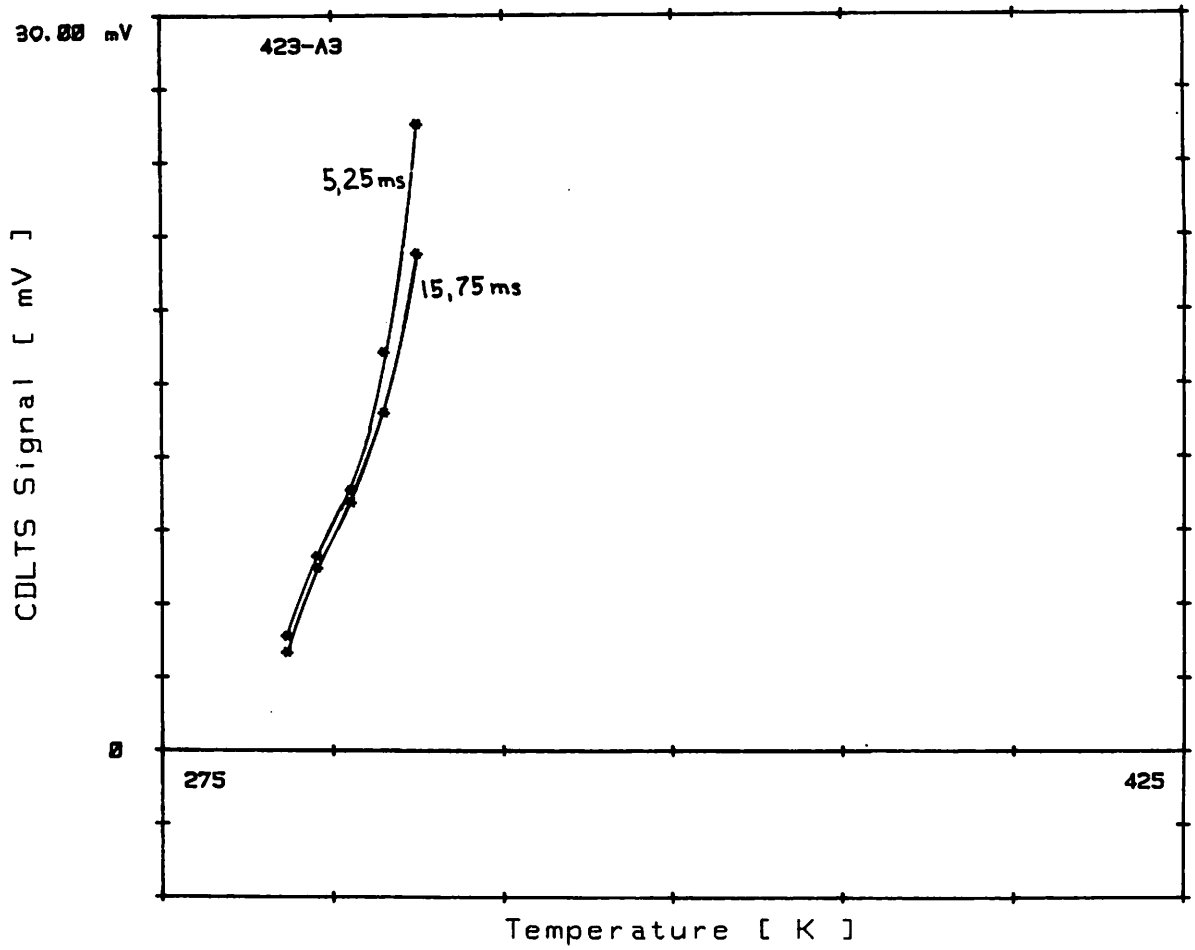


Figure 6.24 Conduction DLTS plot for a 20 μm gate MESFET. The two curves are for rate windows of 5, 25 ms and 15, 75 ms. A large transient was already observable at low temperature but the device noise made it impossible to maintain constant I_D. The signal is measured across a 5.6 kΩ resistor connecting between the source and ground.

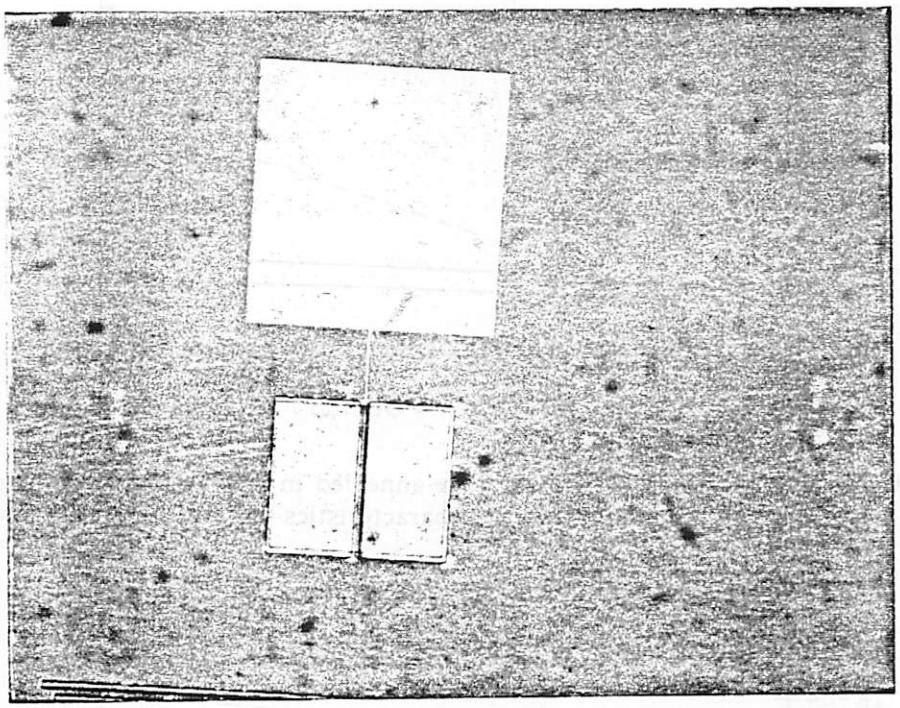


Figure 6.25 A 2μm Ti gate. Au/Ge that has flowed under the oxide cap can be seen around the perimeter.

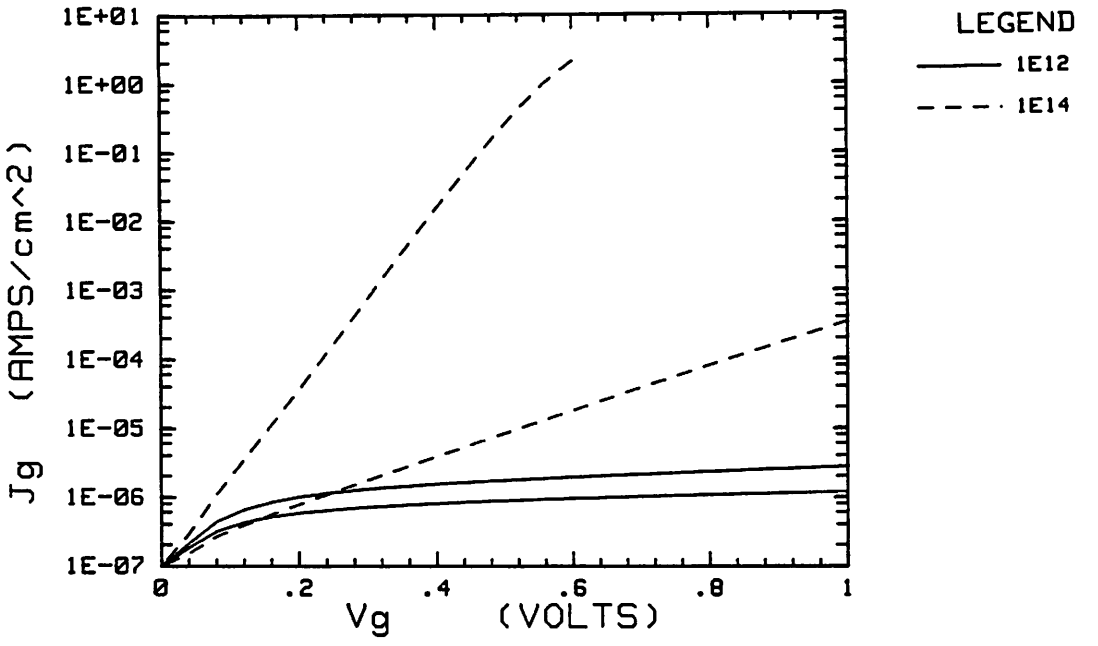


Figure 6.26 These two samples were annealed in a RTA furnace. but only the high dose sample has reasonable forward characteristics (ϕ_B = .77 eV and n = 1.30).

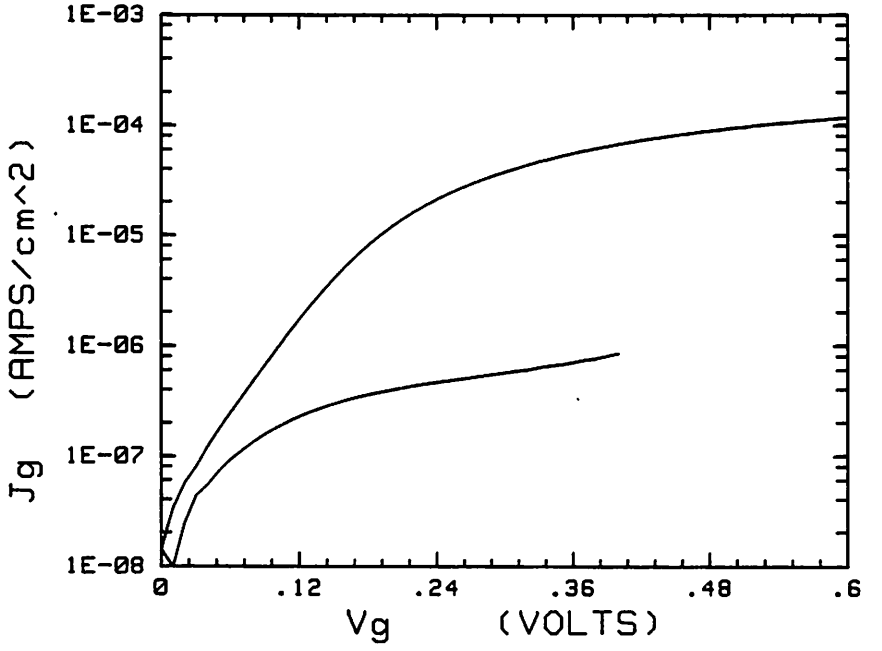


Figure 6.27 The J-V characteristics for a gate to source connection of a 32μm MES-FET (ϕ_B = .79 eV and n = 1.24). This device was implanted with $1x10^{12}$ cm^{-2} and annealed with RTA (Figure 6.25). After passivation, a 10 minute sinter at 100°C yielded these characteristics.

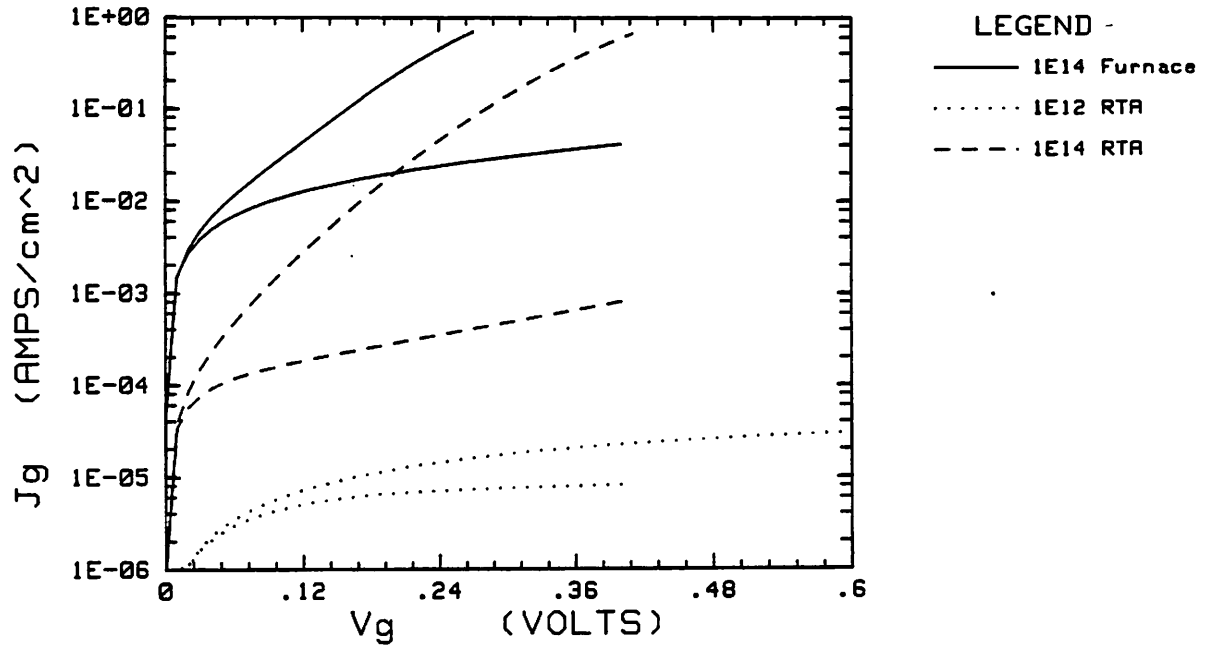


Figure 6.28 A sinter at 100°C for 10 minutes followed by a sinter at 200°C resulted in these J-V curves.

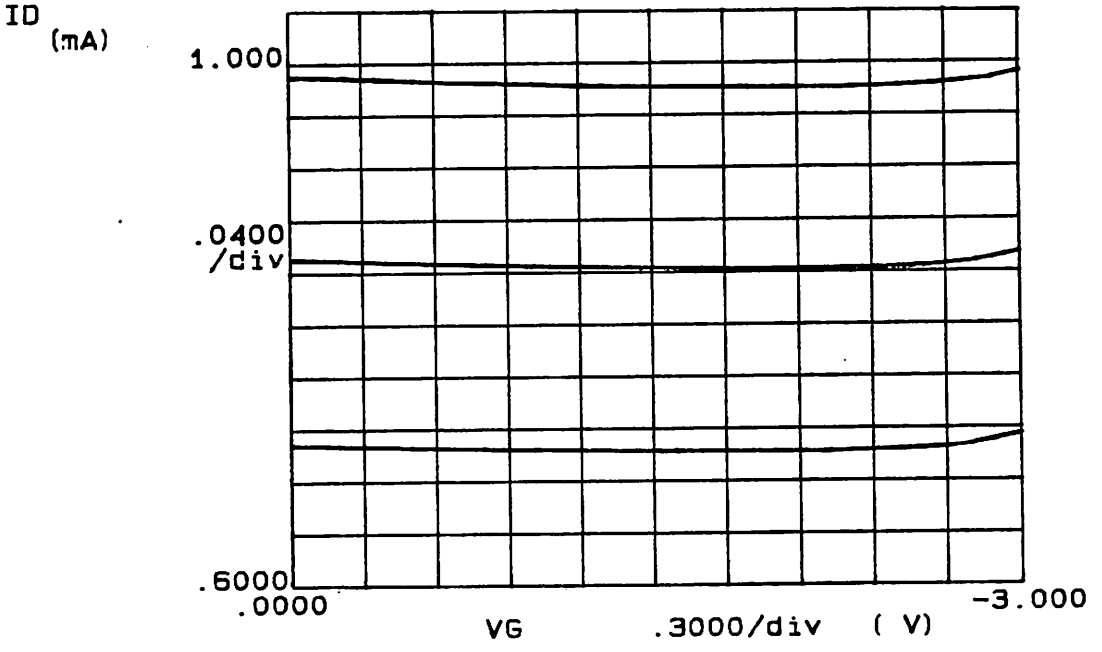


Figure 6.29 $V_{D_{start}}$ = .05 V and $V_{D_{step}}$ = .01 V. These I_D vs. V_G characteristics for a $1x10^{14}$ cm^{-2} implanted, furnace annealed 8μm device are representative of all the devices measured.

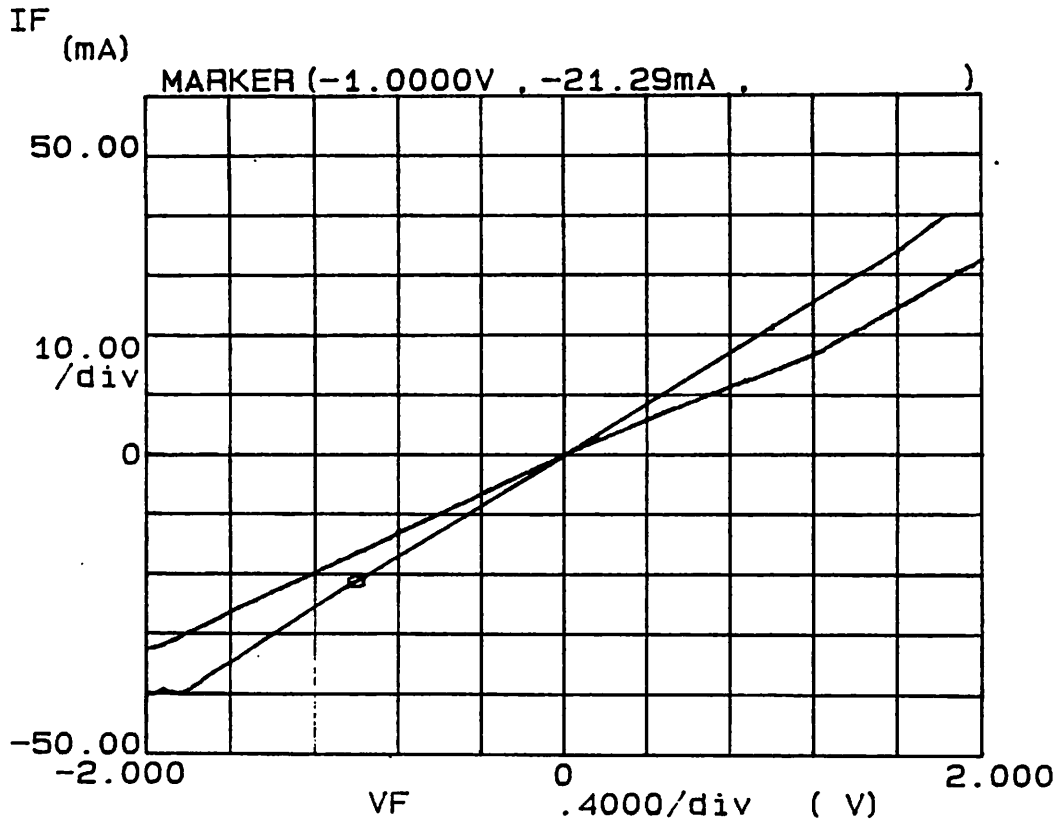


Figure 6.30 Typical constant resistance curves were obtained when measuring drain to source current with a floating gate. The steeper curve represents a 8μm gate and the other a 4μm gate. Both MESFETs have implants of $1x10^{14}$ cm^{-2} and were annealed with RTA.

References

1. A. K. Sinha, T. E. Smith, M. H. Read, and J. M. Poate, "n-GaAs Schottky Diode Metalized with Ti and Pt/Ti," *Solid-State Electron.*, vol. 19, no. 6, pp. 489-492, Pergamon, 1976.

VII. CONCLUSION

Both characterization and process techniques were developed in this research. Implanted GaAs diodes are difficult to measure with DLTS due to high resistance in the tail of the implant. Likewise, this same effect was observed to complicate C-V measurements. The importance of measuring technique was made evident by shifts in the calculated depth of the implant profile due to stray capacitance. Additionally, measuring variations from probe pressure and light were observed. GaAs MESFETs were also fabricated in this research with which conductance deep level transient spectroscopy was demonstrated.

The quality of the SiO_2 encapsulant was observed to be very critical for furnace annealing; therefore, continuous monitoring of the encapsulant deposition parameters was required. Also, degradation of the GaAs surface was seen after furnace annealing. A shorter anneal time improved the surface quality while RTA had little effect on the surface. The quality of the Schottky barrier was observed to be affected by contamination, and a clean, gate metal deposition system improved the electrical characteristics. Similarly, contamination during the gate deposition was probably a major contributor to low MESFET yield.